PEQAE

Erie 10AS/10ASG

LA-7291P REV 1.0 Schematic

AMD Llano FS1 Processor / Hudson M2/M3
Whistler LP & Whistler Pro

2011-04-26 Rev 1.0

Toshiba Satellite P7xx P755

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/11/11	Deciphered Date	2011/11/11
Title	SCHEMATIC MB A7291		
Size B	Document Number 4019CQ		Rev B
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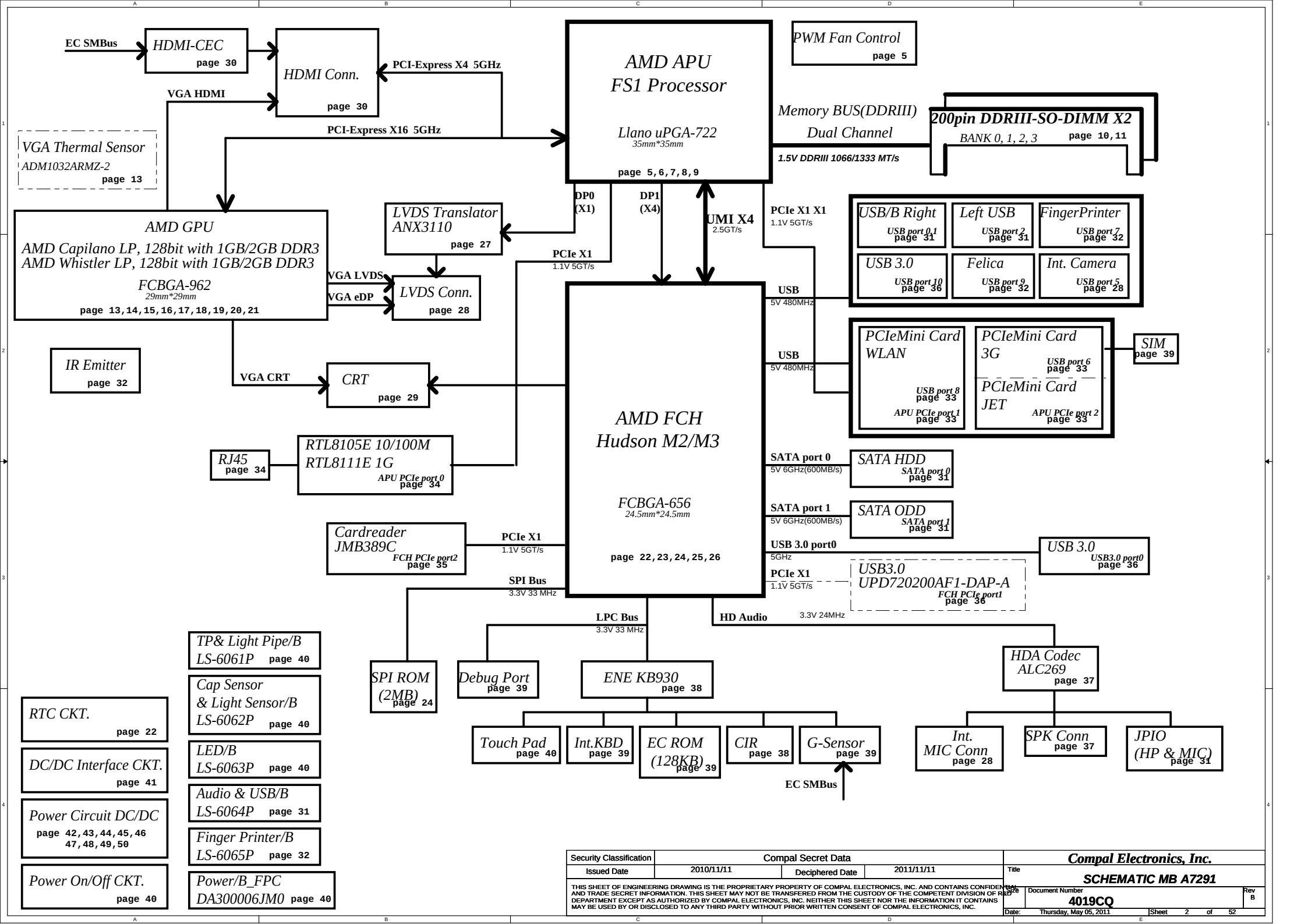

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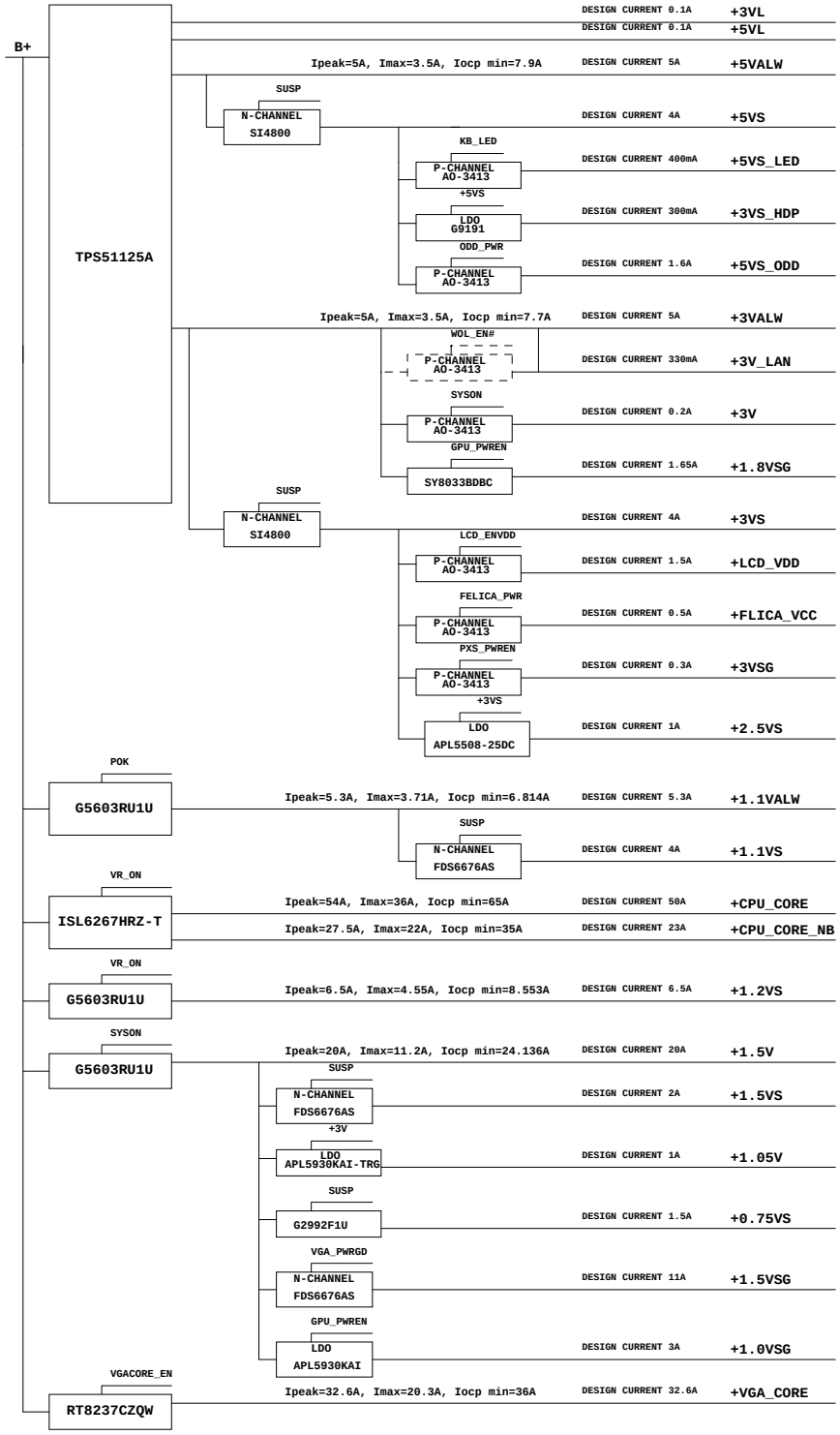

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VSG +1.8VSG +1.5VSG +1.0VSG
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress	Discrete	COMMON	CEC	UMA	PowerXpress	Discrete
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function	MINI PCI-E SLOT	LAN			Fingerprint	CIR	KB Light
description	3G	LAN			Fingerprint	CIR	KB Light
explain	3G	10/100M		GIGA	Fingerprint	CIR	KB Light
BTO	3G@	8105ELDO@	8105ESWR@	8111E@	FP@	CIR@	KBL@

Function	Felica	G-SENSOR	Cam & Mic	Panel		
description	Felica	G-SENSOR	Cam & Mic	Panel (DIS@)		
explain	Felica	G-SENSOR	Cam & Mic	3D LVDS	eDP	Non-3D & EDP
BTO	FELICA@	GSENSOR@	CAM@	3D@+NOEDP@	EDP@	NO3D@+NOEDP@

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		Renesas USB3.0	FCH		EC	
description	PowerXpress		Renesas USB3.0	FCH		EC	
explain	BACO mode	Non-BACO	Renesas USB3.0	Hudson-M2	Hudson-M3	KB-930	KB-9012
BTO	BACO@	NOBACO@	RENE@	M2@	M3@	KB930@	KB9012@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 000X b
+3VS	DDR SO-DIMM 1	A2 H	1010 001X b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	CPU Thermal Sensor	98 H	1001 1001 b
+3VS	GPU Thermal Sensor	82 H	1000 0010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b
+3VS	LVDS EEPROM	A8 H	1010 1000 b
+3VS	3D - Bootloader	C0 H	1100 0000 b
+3VS	3D - Slave	60 H	0110 0000 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

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<12> PCIE_GTX_C_FRX_P[0..15]
<12> PCIE_GTX_C_FRX_N[0..15]

PCIE_FTX_C_GRX_P[0..15] <12>
PCIE_FTX_C_GRX_N[0..15] <12>

JAPUA @

PCI EXPRESS

GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C1	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C2	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C3	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C4	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C9	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C22	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3	W8	P_GFX_RXP3	P_GFX_TXP3	W2	PCIE_FTX_GRX_P3	C23	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C24	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4	V7	P_GFX_RXP4	P_GFX_TXP4	V2	PCIE_FTX_GRX_P4	C25	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C26	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C27	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5	U6	P_GFX_RXN5	P_GFX_TXN5	V5	PCIE_FTX_GRX_N5	C28	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N5
PCIE_GTX_C_FRX_P6	U8	P_GFX_RXP6	P_GFX_TXP6	U2	PCIE_FTX_GRX_P6	C29	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P6
PCIE_GTX_C_FRX_N6	U9	P_GFX_RXN6	P_GFX_TXN6	U3	PCIE_FTX_GRX_N6	C30	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N6
PCIE_GTX_C_FRX_P7	T7	P_GFX_RXP7	P_GFX_TXP7	T2	PCIE_FTX_GRX_P7	C31	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P7
PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C32	VGA@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N7
PCIE_GTX_C_FRX_P8	R5	P_GFX_RXP8	P_GFX_TXP8	T4	PCIE_FTX_GRX_P8	C33	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P8
PCIE_GTX_C_FRX_N8	R6	P_GFX_RXN8	P_GFX_TXN8	T5	PCIE_FTX_GRX_N8	C34	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N8
PCIE_GTX_C_FRX_P9	R8	P_GFX_RXP9	P_GFX_TXP9	R2	PCIE_FTX_GRX_P9	C35	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P9
PCIE_GTX_C_FRX_N9	R9	P_GFX_RXN9	P_GFX_TXN9	R3	PCIE_FTX_GRX_N9	C36	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N9
PCIE_GTX_C_FRX_P10	P7	P_GFX_RXP10	P_GFX_TXP10	P2	PCIE_FTX_GRX_P10	C37	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P10
PCIE_GTX_C_FRX_N10	P8	P_GFX_RXN10	P_GFX_TXN10	P1	PCIE_FTX_GRX_N10	C38	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N10
PCIE_GTX_C_FRX_P11	N5	P_GFX_RXP11	P_GFX_TXP11	P4	PCIE_FTX_GRX_P11	C39	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P11
PCIE_GTX_C_FRX_N11	N6	P_GFX_RXN11	P_GFX_TXN11	P5	PCIE_FTX_GRX_N11	C40	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N11
PCIE_GTX_C_FRX_P12	N8	P_GFX_RXP12	P_GFX_TXP12	N2	PCIE_FTX_GRX_P12	C41	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P12
PCIE_GTX_C_FRX_N12	N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12	C42	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N12
PCIE_GTX_C_FRX_P13	M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13	C43	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P13
PCIE_GTX_C_FRX_N13	M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13	C44	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N13
PCIE_GTX_C_FRX_P14	L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14	C45	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P14
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PCIE_GTX_C_FRX_P15	L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15	C47	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_P15
PCIE_GTX_C_FRX_N15	L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15	C48	DIS@ 0.1U_0402_16V7K	PCIE_FTX_C_GRX_N15

For PowerXpress

Place R1 ~ R8 close to C33 ~ C40

PCIE_FTX_GRX_P8	R1	HDMI@	0_0402_5%	UMA_HDMI_TX2+ <30>
PCIE_FTX_GRX_N8	R2	HDMI@	0_0402_5%	UMA_HDMI_TX2- <30>
PCIE_FTX_GRX_P9	R3	HDMI@	0_0402_5%	UMA_HDMI_TX1+ <30>
PCIE_FTX_GRX_N9	R4	HDMI@	0_0402_5%	UMA_HDMI_TX1- <30>
PCIE_FTX_GRX_P10	R5	HDMI@	0_0402_5%	UMA_HDMI_TX0+ <30>
PCIE_FTX_GRX_N10	R6	HDMI@	0_0402_5%	UMA_HDMI_TX0- <30>
PCIE_FTX_GRX_P11	R7	HDMI@	0_0402_5%	UMA_HDMI_TXC+ <30>
PCIE_FTX_GRX_N11	R8	HDMI@	0_0402_5%	UMA_HDMI_TXC- <30>

GPP

LAN

<34> PCIE_FRX_C_LANTX_P0	PCIE_FRX_C_LANTX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_LANRX_P0	C49	0.1U_0402_16V7K	PCIE_FTX_C_LANRX_P0 <34>
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		AA5	P_GPP_RXP3	P_GPP_TXP3	AB4				
		AA6	P_GPP_RXN3	P_GPP_TXN3	AB5				

WLAN

JET

UMI-LINK

<22> UMI_MTX_C_FRX_P0	UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C55	0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 <22>
<22> UMI_MTX_C_FRX_N0	UMI_MTX_C_FRX_N0	AF7	P_UMI_RXN0	P_UMI_TXN0	AF2	UMI_FTX_MRX_N0	C56	0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 <22>
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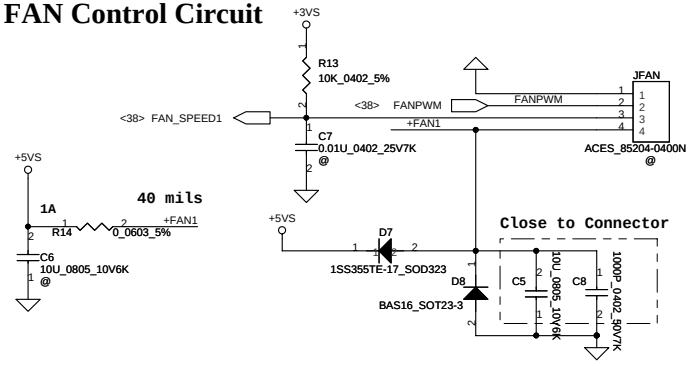
+1.2VS — R9 196_0402_1% — P_ZVDDP K5 — P_ZVDDP

P_ZVSS K4 — R10 196_0402_1% — P_ZVSS

AMD_TOPEDO_FS-1

FAN Control Circuit



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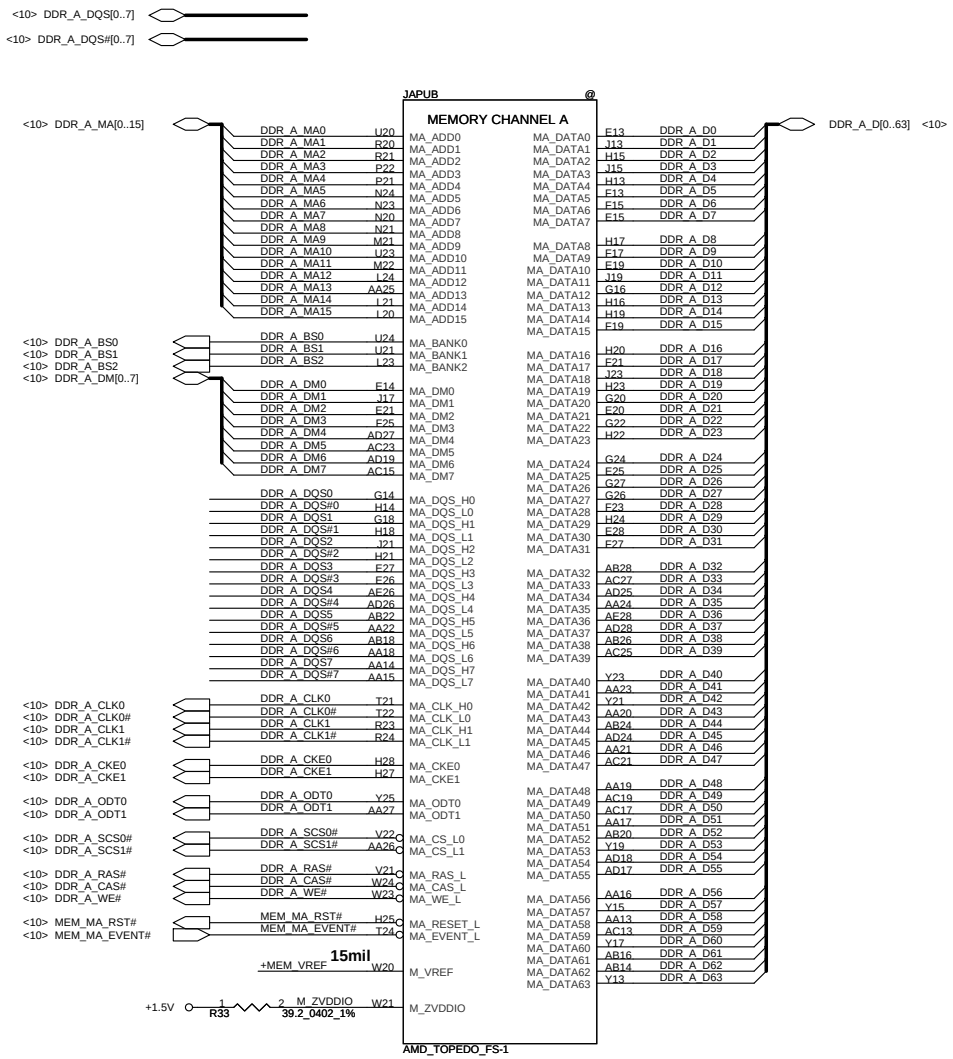
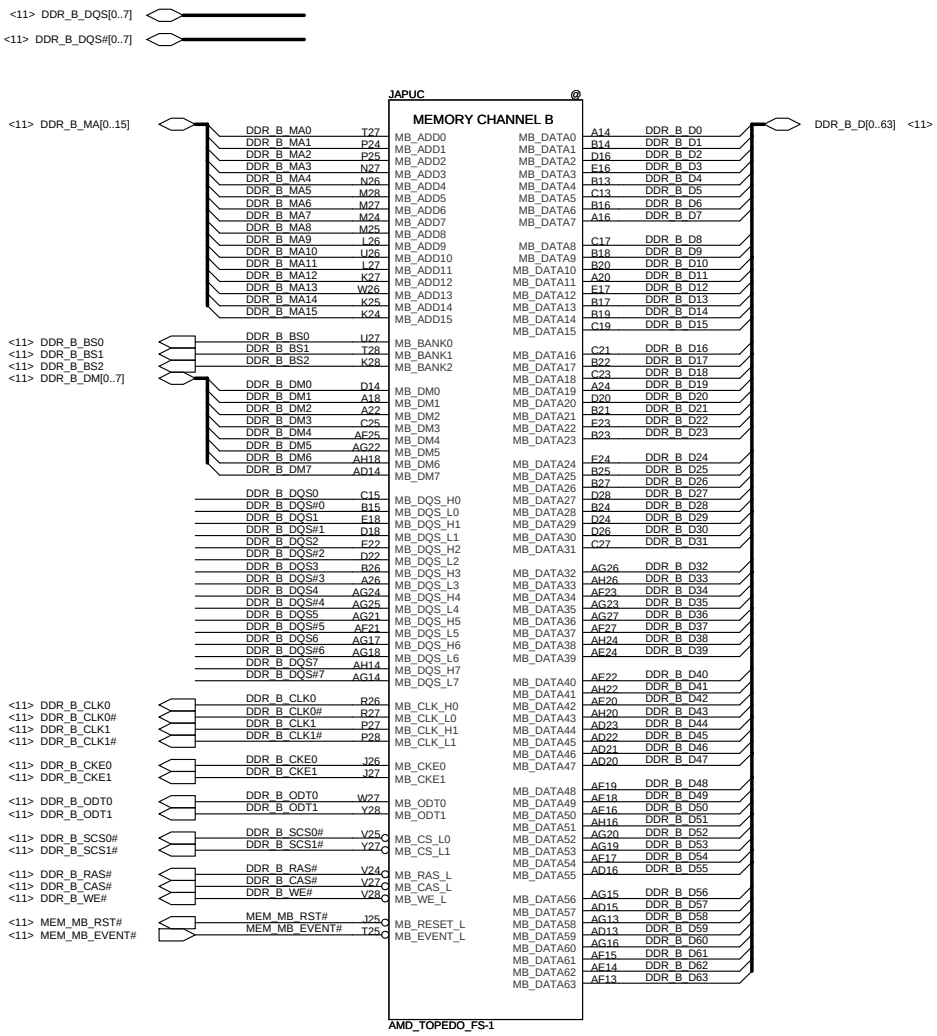
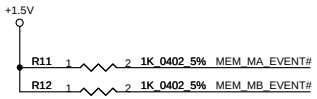
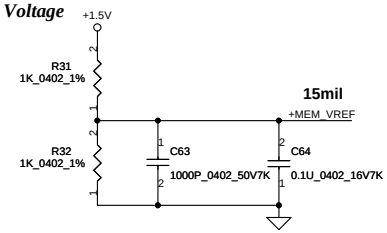




EVENT# pull high



0.75V Reference Voltage



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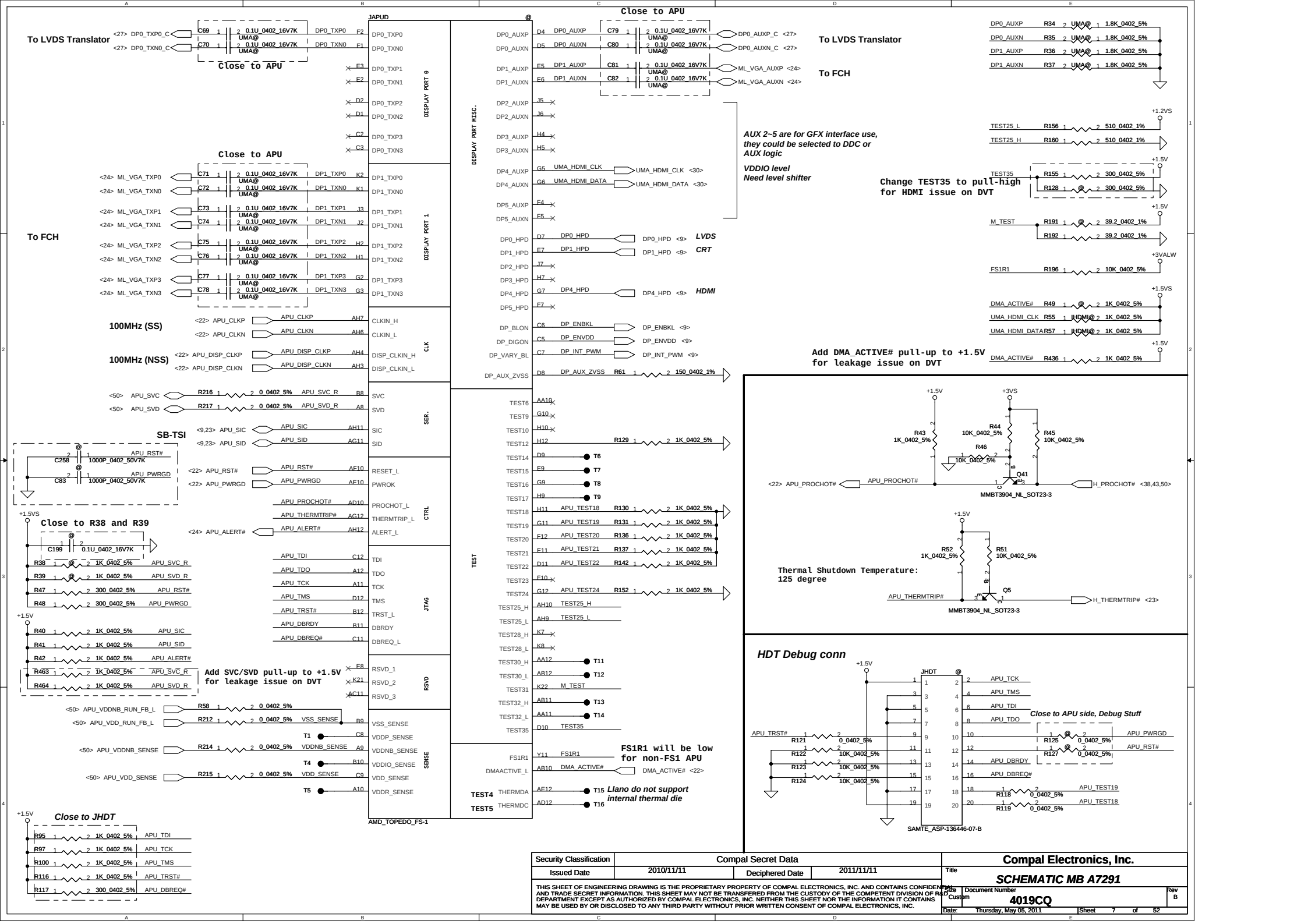

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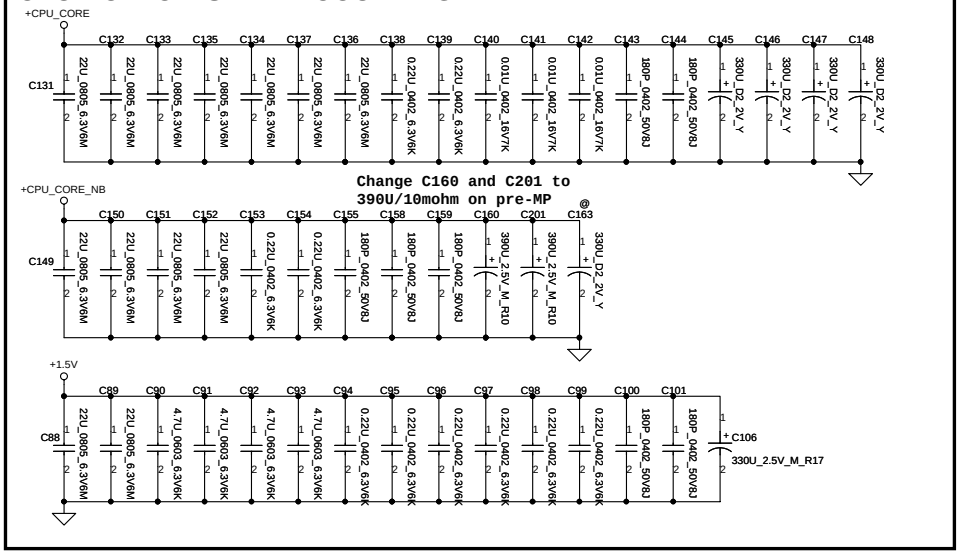
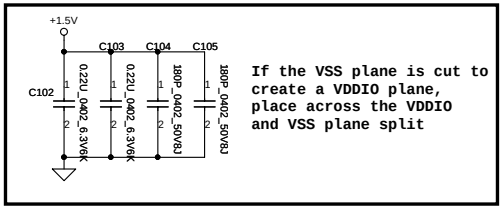
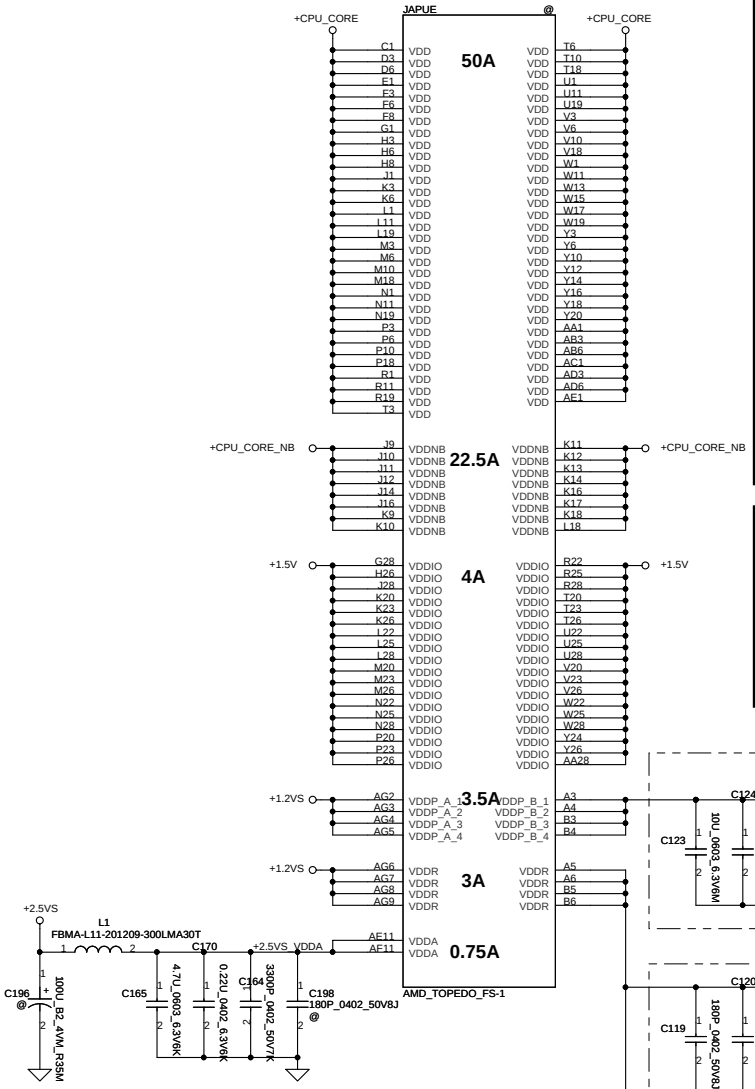
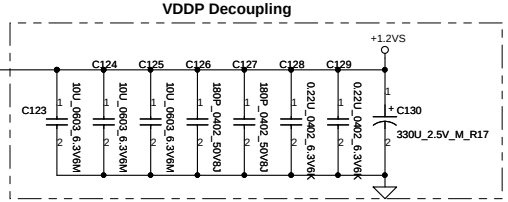
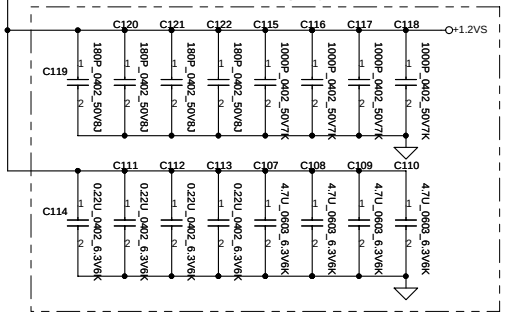
CPU BOTTOM SIDE DECOUPLING

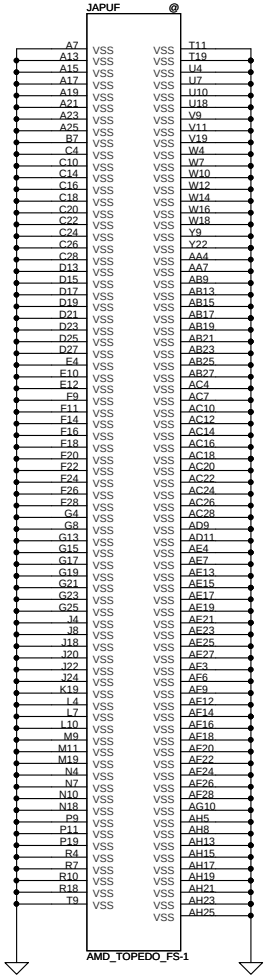












CRB Decoupling Capacitor (include PWM side) :

VDD:	VDDNB:	VDDIO:	VDDP/R_PWM:	VDDP:	VDDR:	VDDA:
470uF x 6 22uF x 9 0.22uF x 2 0.01uF x 3 180pF x 2	470uF x 4 22uF x 6 0.22uF x 2 180pF x 3	680uF x 1 330uF x 1 22uF x 2 4.7uF x 4 0.22uF x 8 180pF x 4	470uF x 2 10uF x 1	10uF x 3 0.22uF x 2 180pF x 2	4.7uF x 4 0.22uF x 4 1nF x 4 180pF x 4	100uF x 1 4.7uF x 1 0.22uF x 1 3.3nF x 1

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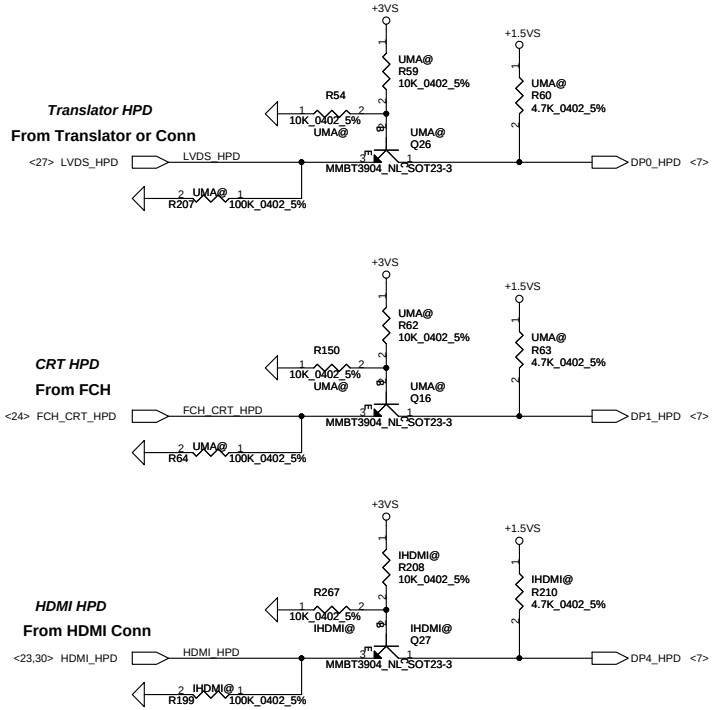
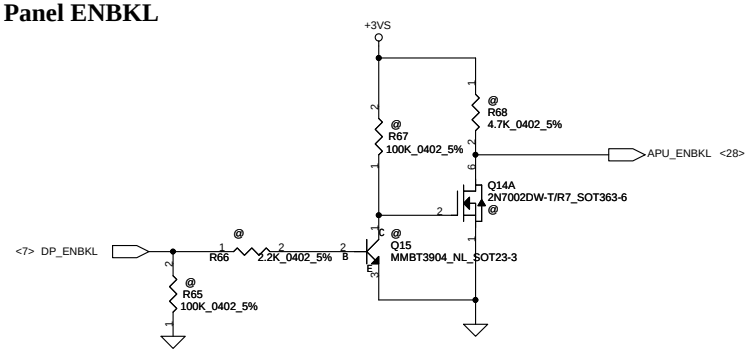
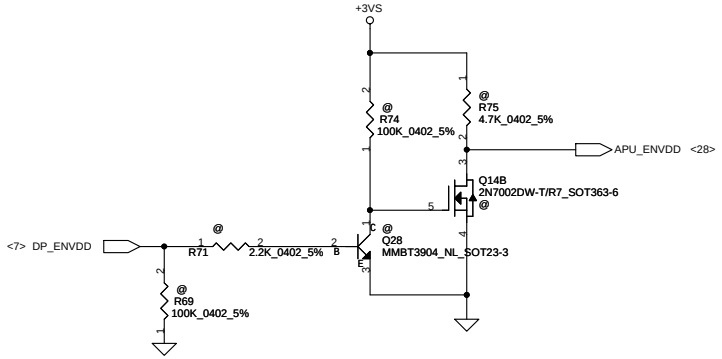
HPD



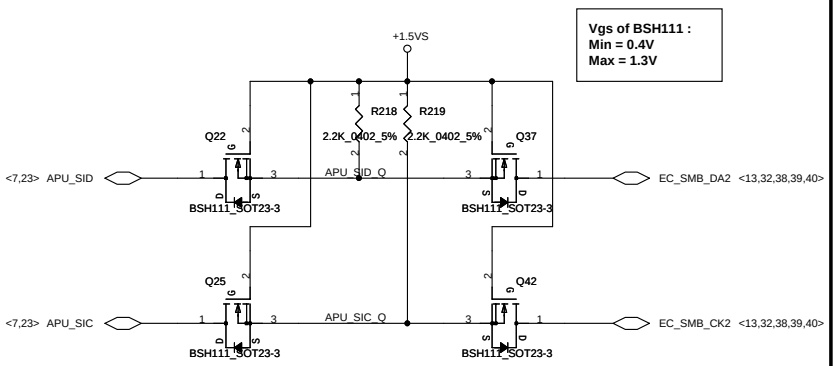
Panel ENBKL



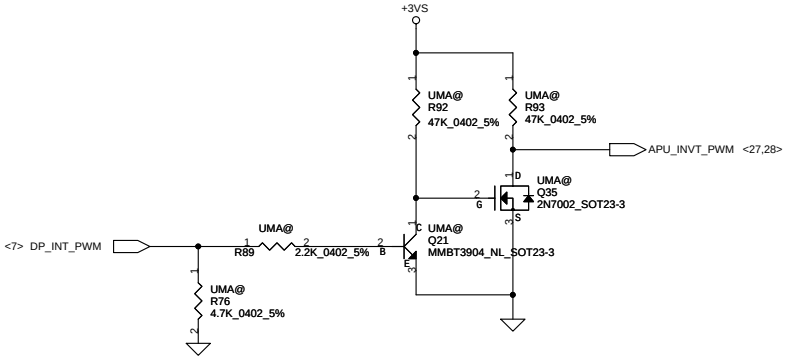
Panel ENVDD



SB-TSI



Panel PWM



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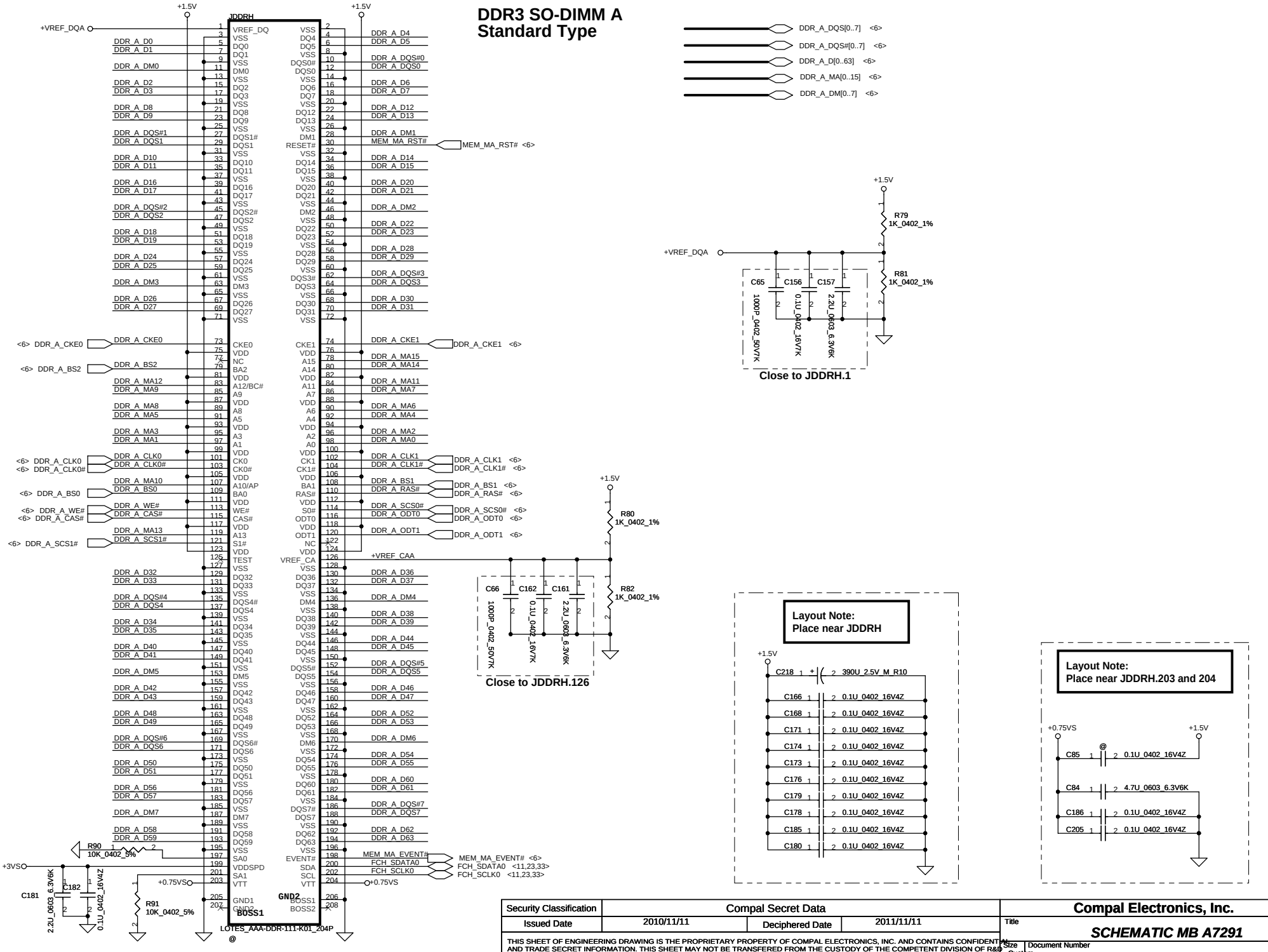
DDR3 SO-DIMM A
Standard Type



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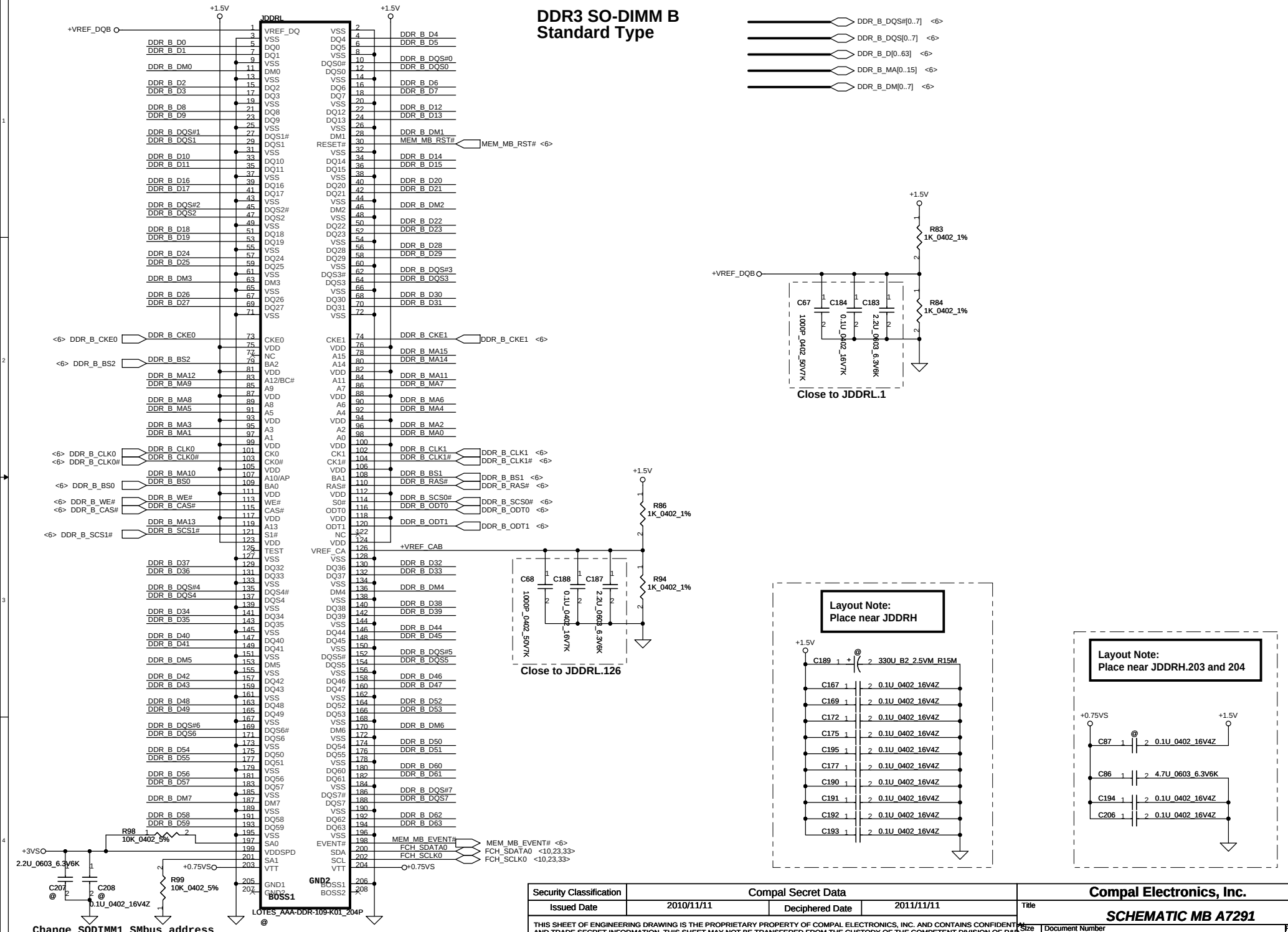
DDR3 SO-DIMM B
Standard Type



DDR_B_DQS#[0..7] <6>
DDR_B_DQS[0..7] <6>
DDR_B_D[0..63] <6>
DDR_B_MA[0..15] <6>
DDR_B_DM[0..7] <6>

Close to JDDRL.1

Close to JDDRL.126

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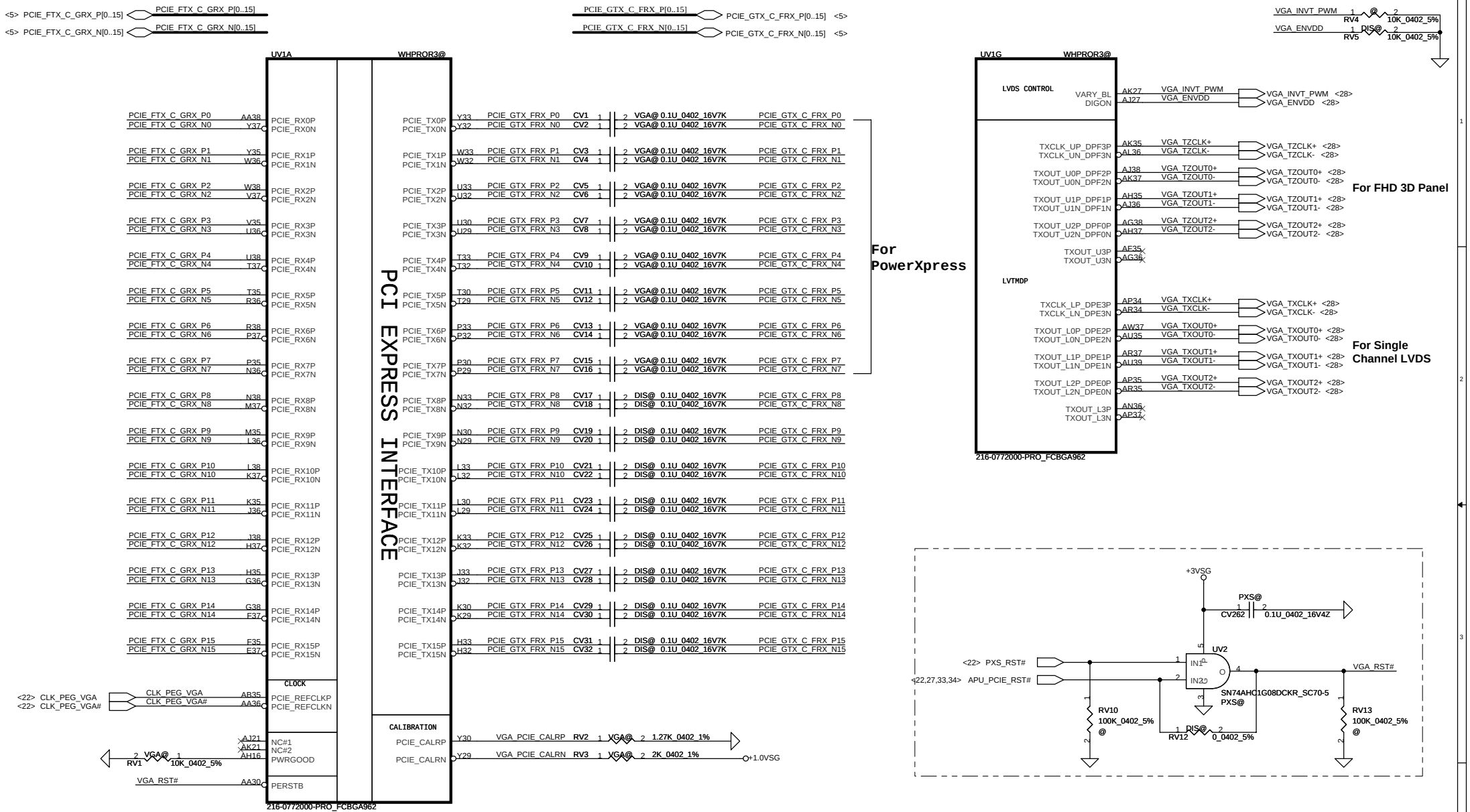

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Strap Name	Pin Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN_V2SYNC (GENLK_VSYNC)	GPIO9	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 128 MB 000 * 256 MB 001 64 MB 010 32 MB 011	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 1: Enable 0: Diable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	NC

Don't have this strap for Whistler

External VGA Thermal Sensor
(Address: 0x9A H)

Close to UV3

UV3 ADM1032ARMZ-2REEL_MSOP8

Internal Thermal Sensor
Address: 0x82 H

2N7002DW-T/R7_SOT363-6

For 3D eDP Panel

NC for Whistler

NC for Whistler
Except A2VSSQ change to TSVSSQ

Close to GPU

For Debug

For DDR3/GDDR3

For GDDR5

For Capilano

VRAM STRAP
(VRAM_ID[0:3] internal pull-down)

VRAM \ Location	VRAM_ID0	VRAM_ID1	VRAM_ID2	VRAM_ID3
Samsung (1GB)	0	0	0	0
HYNIX (1GB)	1	0	0	0
Samsung (2GB)	0	1	0	0
HYNIX (2GB)	1	1	0	0

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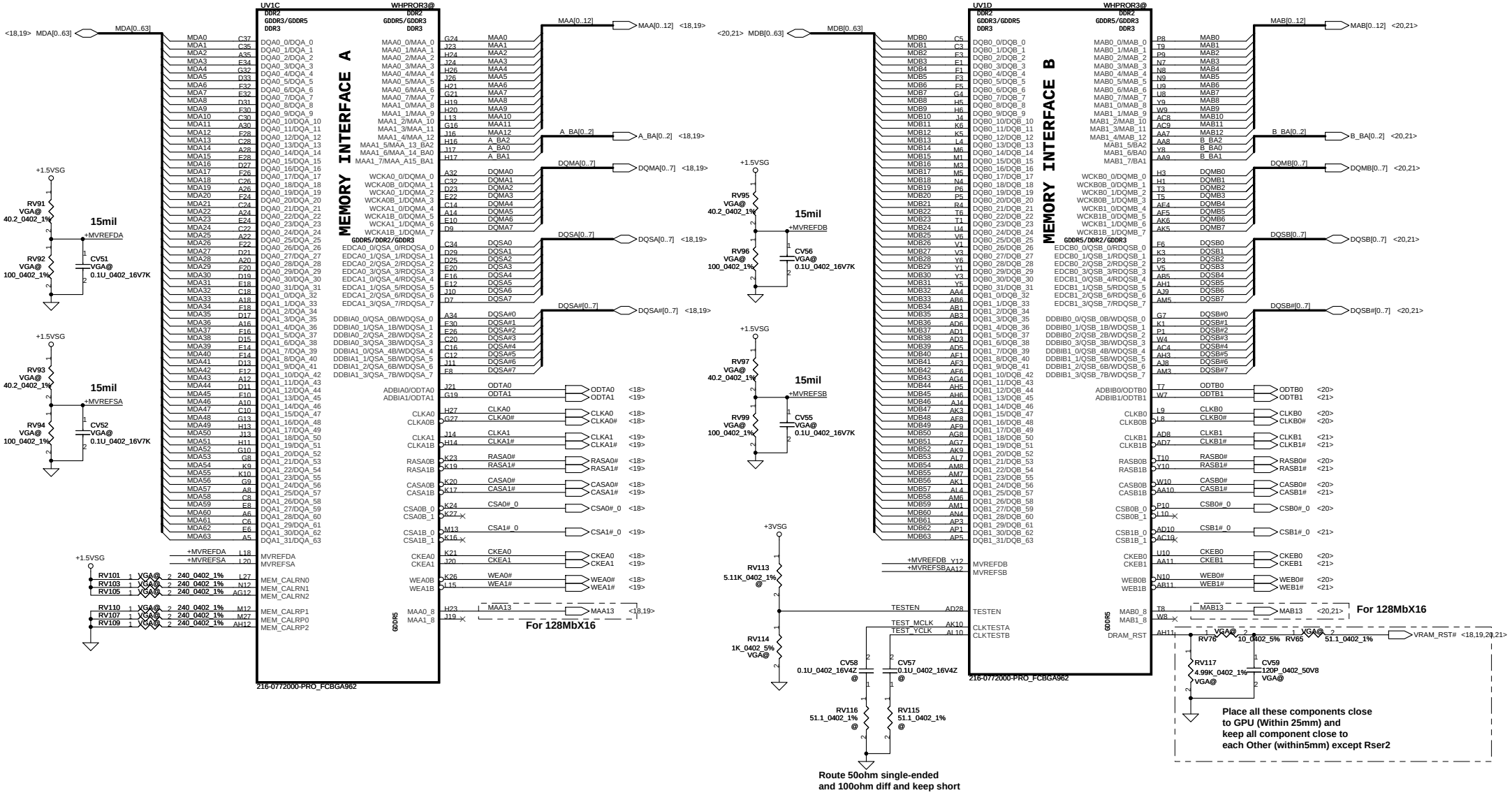

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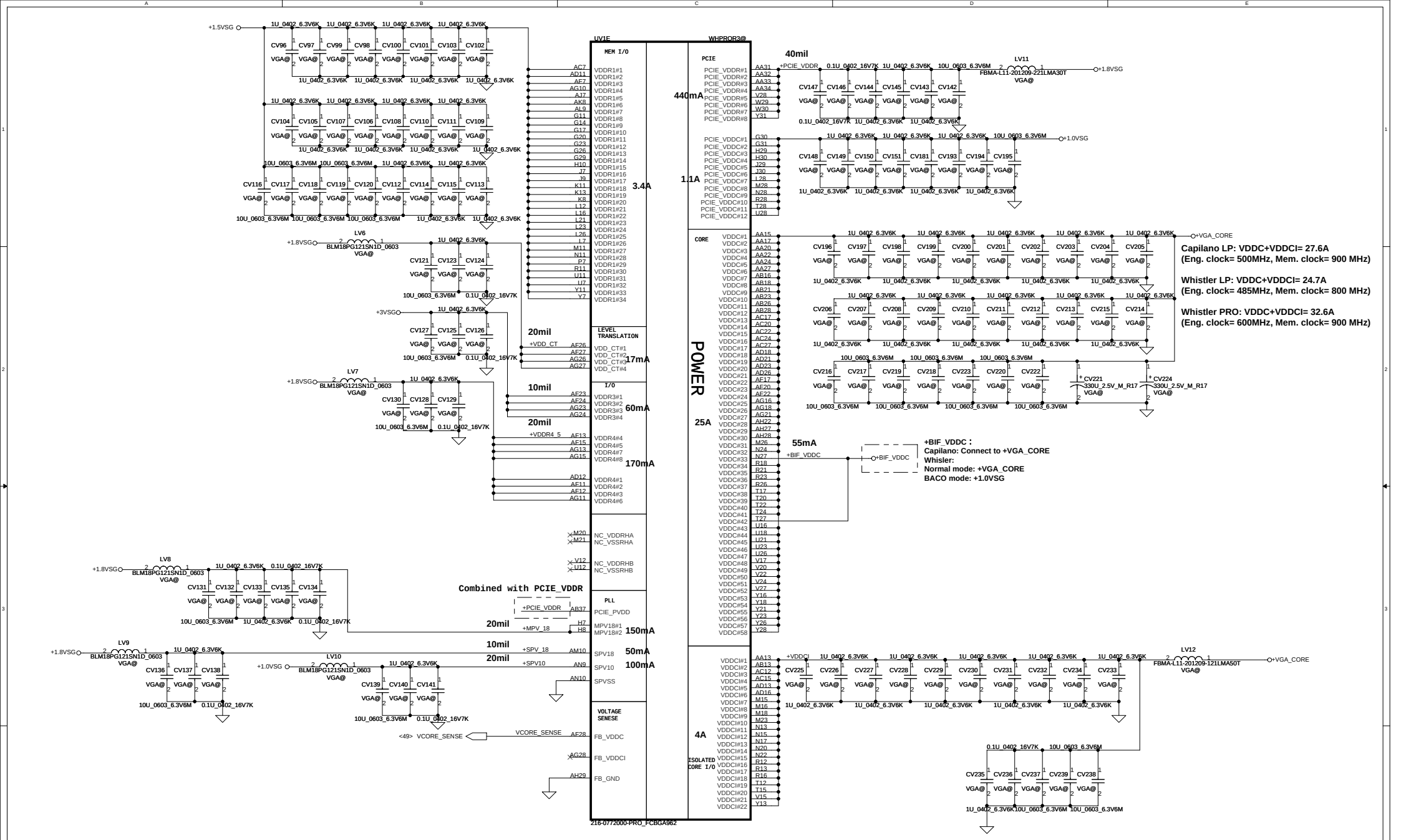

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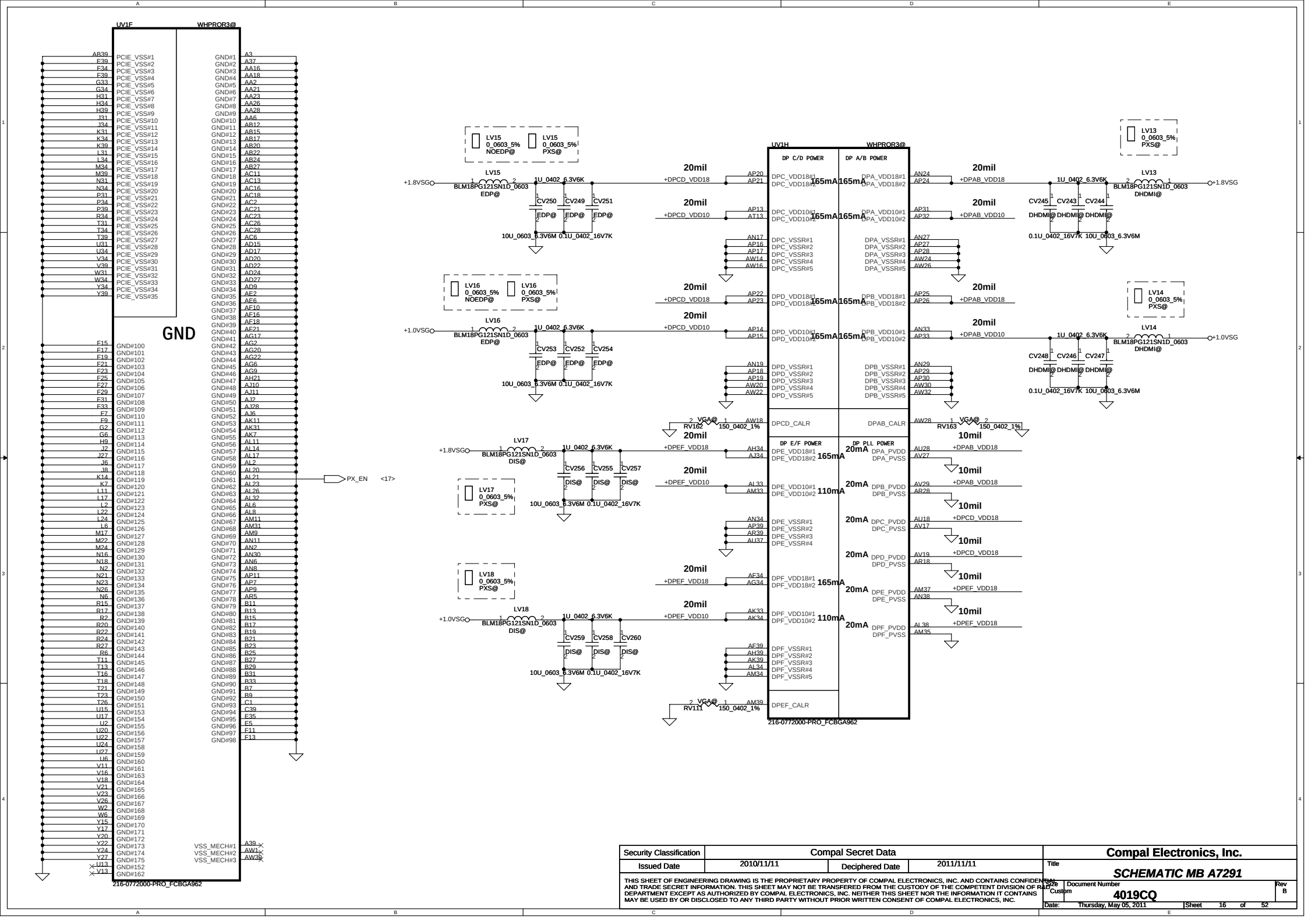

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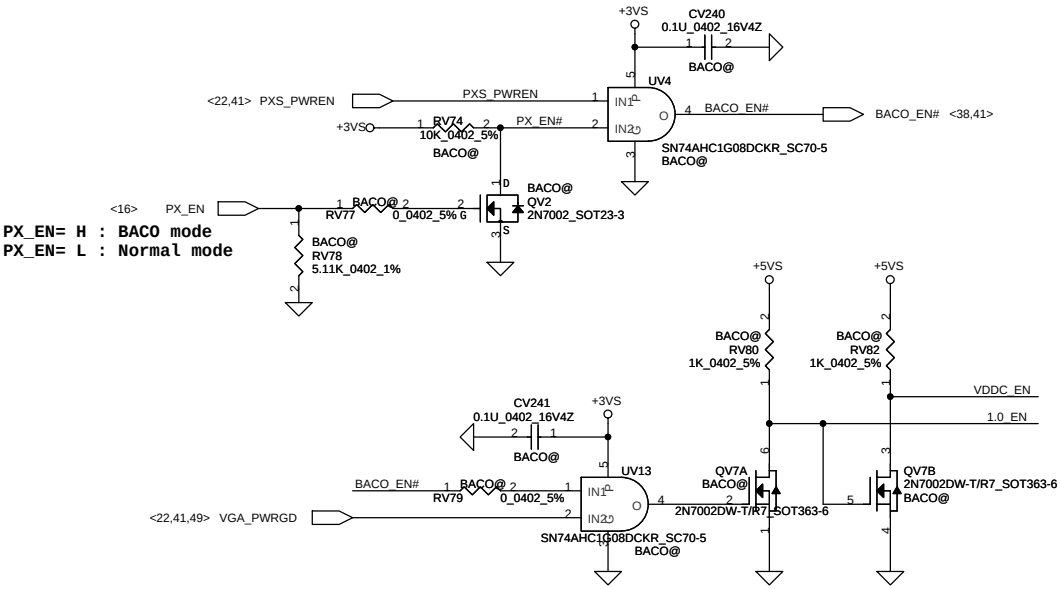

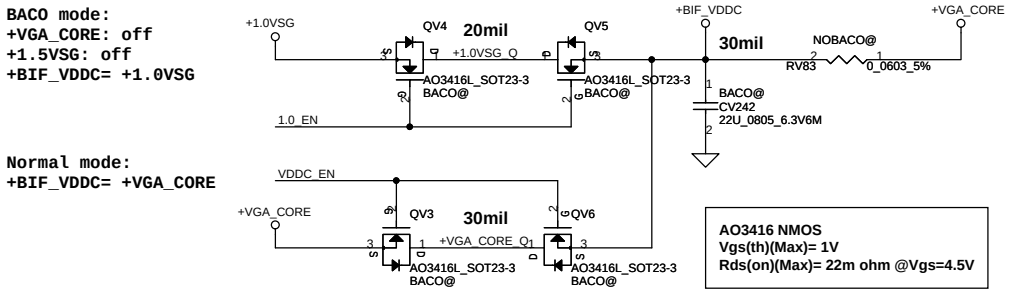

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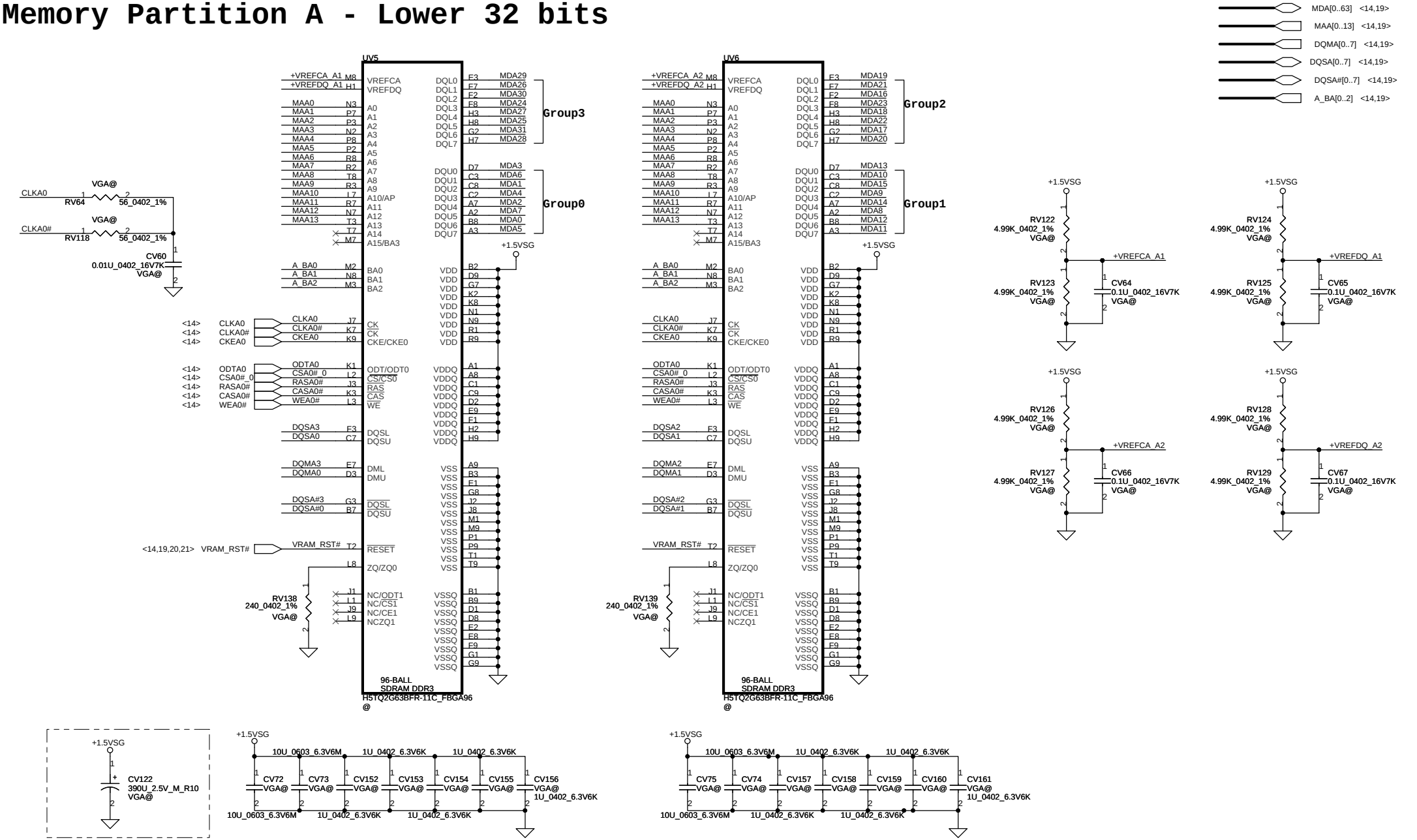
Memory Partition A - Lower 32 bits



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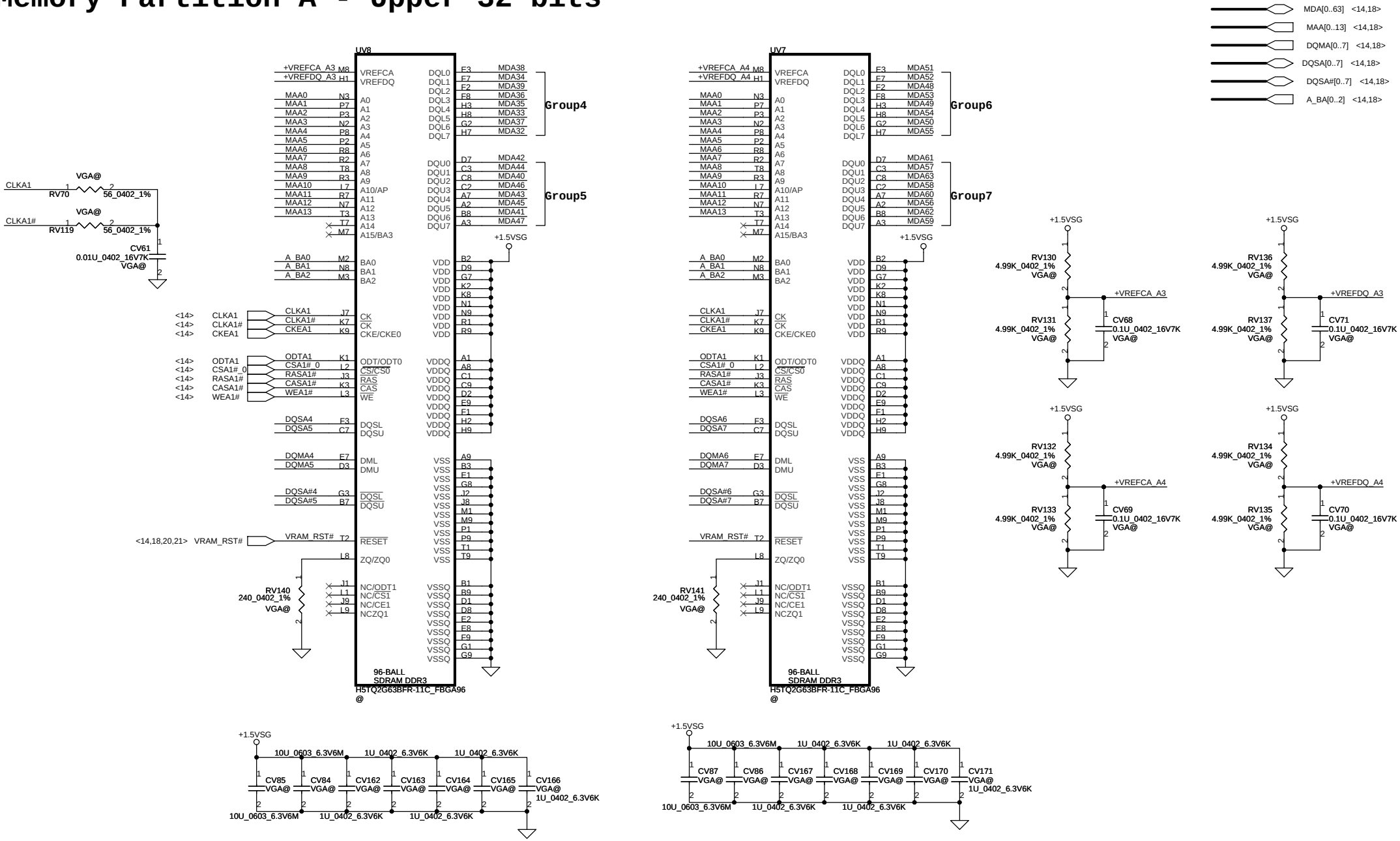
Memory Partition A - Upper 32 bits



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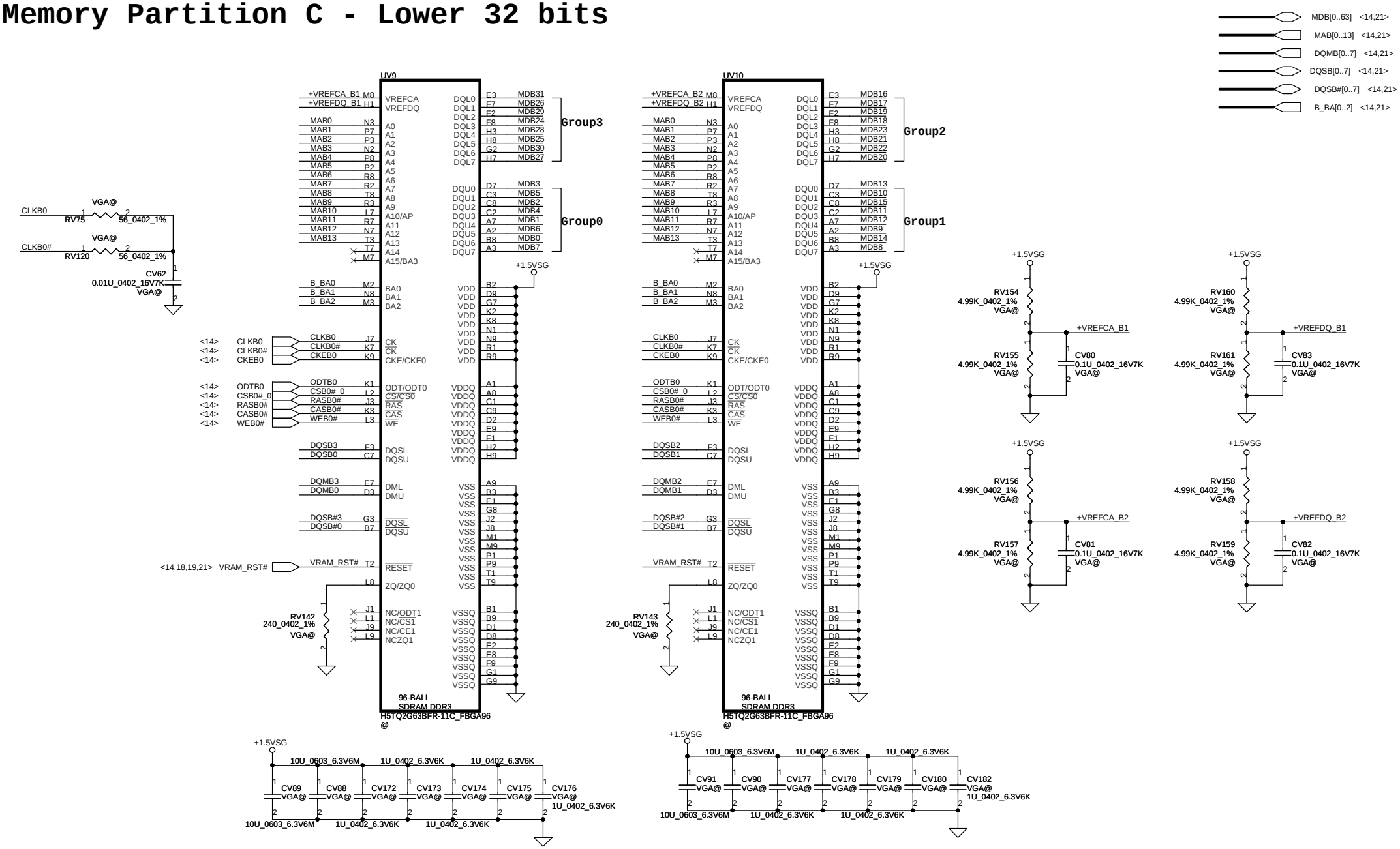
Memory Partition C - Lower 32 bits



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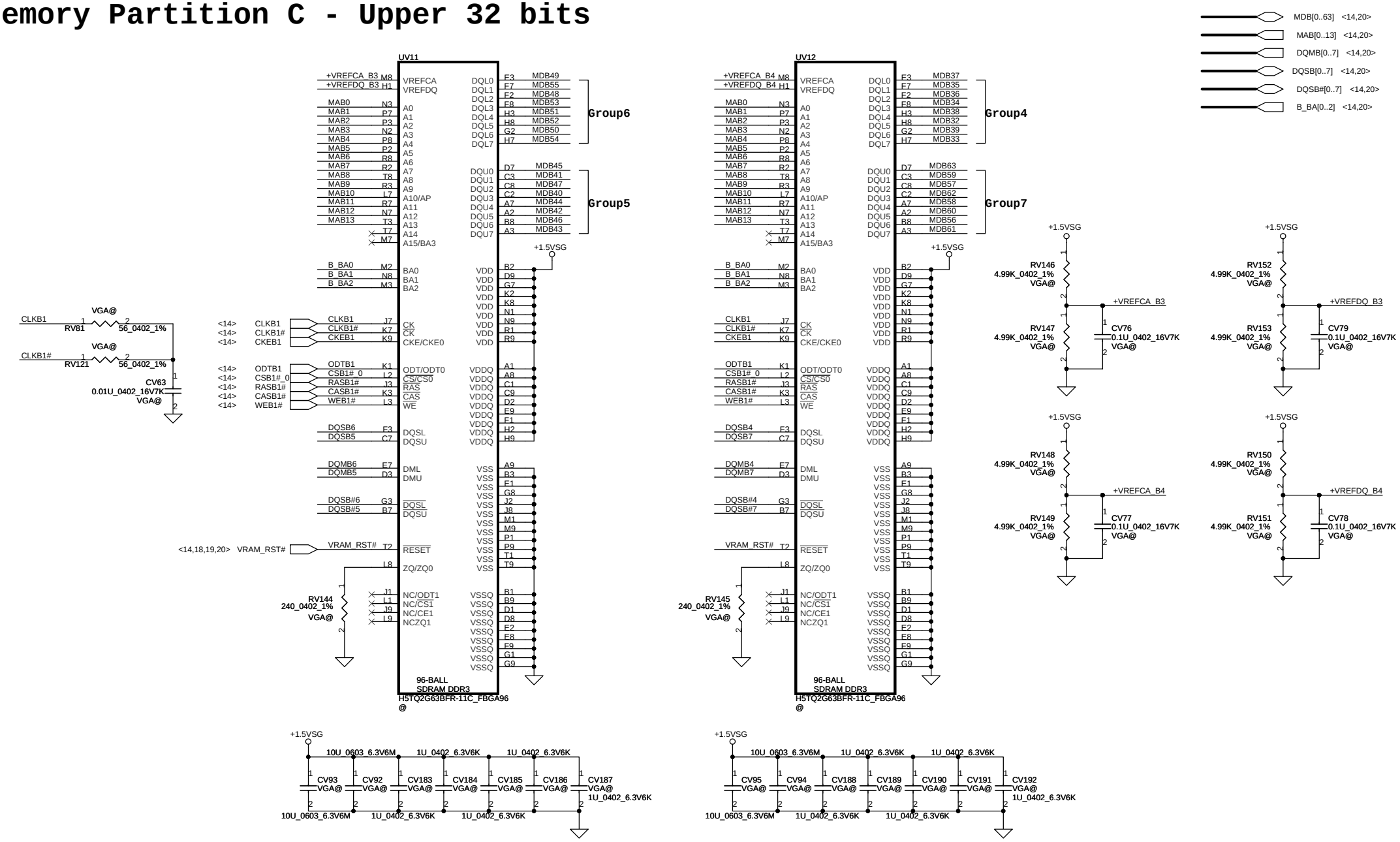
Memory Partition C - Upper 32 bits



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Issued Date	2010/11/11	Deciphered Date	2011/11/11

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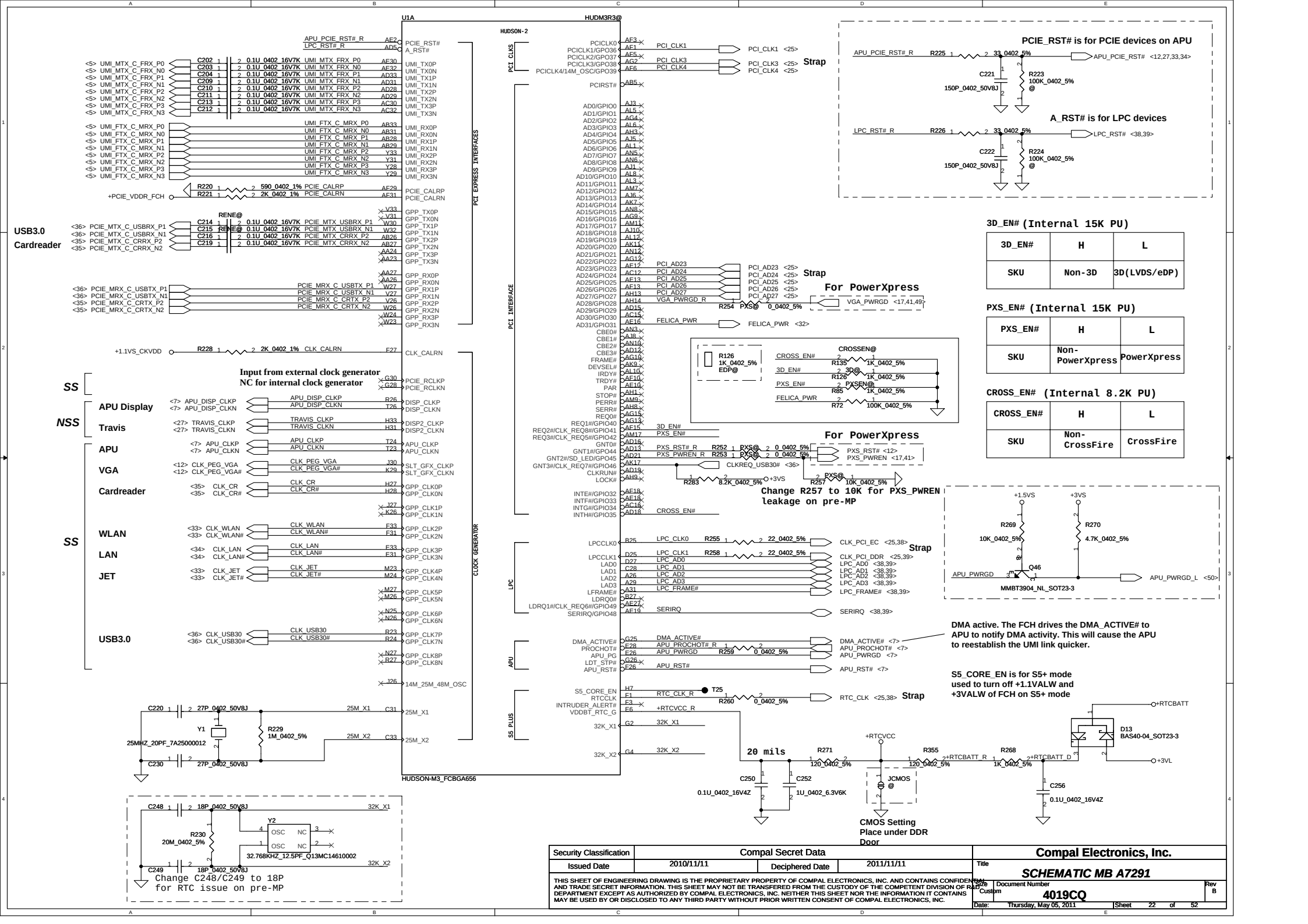

3D_EN#	H	L
SKU	Non-3D	3D(LVDS/eDP)

PXS_EN#	H	L
SKU	Non-PowerXpress	PowerXpress

CROSS_EN#	H	L
SKU	Non-CrossFire	CrossFire

Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/11/11

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PCIE_RST2# is for PCIE devices on FCH

U1D

HUDSON-2

HUDM3R3@

R227 2 @ 1 100K_0402_5%
C19 1 2 150P_0402_50V8J
R222 33_0402_5%

<35,36> FCH_PCIE_RST#
FCH_PCIE_RST#_R AB6 PCIE_RST2#/PCI_PME#/GEVENT4#
<38> EC_LID_OUT# EC_LID_OUT# R2 RI#/GEVENT22#
T57 W7 SPI_CS3#/GBE_STAT1/GEVENT21#
<38> SLP_S3# SLP_S3# T3 SLP_S3#
<38> SLP_S5# SLP_S5# W2 SLP_S5#
<38> PBTN_OUT# PBTN_OUT# J4 PWR_BTN#
<38> FCH_PWRGD FCH_PWRGD N7 PWR_GOOD

TEST0 T9 TEST0
TEST1 T10 TEST1/TMS
TEST2 V9 TEST2

<38> GATEA20 GATEA20 AE22 GA20IN/GEVENT0#

<38> KB_RST# KB_RST# AG19 KBRST#/GEVENT1#
<38> EC_SCI# EC_SCI# R8 LPC_PME#/GEVENT3#
<38> EC_SMI# EC_SMI# C28 LPC_SMI#/GEVENT23#
T31 T5 LPC_PD#/GEVENT5#
U4 SYS_RESET#/GEVENT19#
<34,36> FCH_PCIE_WAKE# FCH_PCIE_WAKE# K1 WAKE#/GEVENT8#
T55 V7 IR_RX1/GEVENT20#
<7> H_THERMTRIP# H_THERMTRIP# R10 THRMTRIP#/SMBALERT#/GEVENT2#
+3VS R279 10K_0402_5% WD_PWRGD AF19 WD_PWRGD

<38> EC_RSMRST# EC_RSMRST# U2 RSMRST#

<33> CLKREQ_JET# CLKREQ_JET# AG24 CLK_REQ4#/SATA_IS0#/GPIO64
<34> CLKREQ_LAN# D17 RB751V40_SC76-2 CLKREQ_LAN#_R AE24 CLK_REQ3#/SATA_IS1#/GPIO63
R361 0_0402_5% SMARTVOLT1/SATA_IS2#/GPIO50
CLKREQ_CR# AE22 CLK_REQ0#/SATA_IS3#/GPIO60
AH17 SATA_IS4#/FANOUT3/GPIO55
AG18 SATA_IS5#/FANIN3/GPIO59

<37> FCH_SPKR FCH_SPKR AF24 SPKR/GPIO66
<10,11,33> FCH_SCLK0 FCH_SCLK0 AD26 SCL0/GPIO43
<10,11,33> FCH_SDATA0 FCH_SDATA0 AD25 SDA0/GPIO47
FCH_SCLK1 T7 SCL1/GPIO227
FCH_SDATA1 R7 SDA1/GPIO228
<33> CLKREQ_WLAN# CLKREQ_WLAN# AG25 CLK_REQ2#/FANIN4/GPIO62
AG22 CLK_REQ1#/FANOUT4/GPIO61
T30 J2 IR_LED#/LLB#/GPIO184
AG26 SMARTVOLT2/SHUTDOWN#/GPIO51
<25> VGA_PD R292 1 @ 2 0_0402_5% VGA_PD_FCH V8 DDR3_RST#/GEVENT7#/VGA_PD
W8 GBE_LED0/GPIO183
T54 Y6 SPI_HOLD#/GBE_LED1/GEVENT9#
HDMI_HPD_Q V10 GBE_LED2/GEVENT10#
AA8 GBE_STAT0/GEVENT11#
<13> PEG_CLKREQ# PEG_CLKREQ# AF25 CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#

<36> USB30_SMI# USB30_SMI# M7 BLINK/USB_OC7#/GEVENT18#
R8 USB_OC6#/IR_TX1/GEVENT6#
<31> ODD_PLUGIN# ODD_PLUGIN# T1 USB_OC5#/IR_TX0/GEVENT17#
ODD_DA#_FCH P6 USB_OC4#/IR_RX0/GEVENT16#
<31,38> USB_OC3# USB_OC3# F5 USB_OC3#/AC_PRES/TDO/GEVENT15#
<35> CR_CPPE# CR_CPPE# P5 USB_OC2#/TCK/GEVENT14#
<33,36,38> USB_OC1# USB_OC1# J7 USB_OC1#/TDI/GEVENT13#
<31,38> USB_OC0# USB_OC0# T8 USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#

<37> AZ_BITCLK_HD R320 1 2 33_0402_5% HDA_BITCLK AB3 AZ_BITCLK
<37> AZ_SDOUT_HD R321 1 2 33_0402_5% HDA_SDOUT AB1 AZ_SDOUT
<37> AZ_SDIN0_HD AZ_SDIN0_HD AA2 AZ_SDIN0/GPIO167
V5 AZ_SDIN1/GPIO168
Y3 AZ_SDIN2/GPIO169
Y1 AZ_SDIN3/GPIO170
<37> AZ_SYNC_HD R322 1 2 33_0402_5% HDA_SYNC AD6 AZ_SYNC
<37> AZ_RST_HD# R323 1 2 33_0402_5% HDA_RST# AE4 AZ_RST#

T26 K19 PS2_DAT/SDA4/GPIO187
T27 J19 PS2_CLK/CEC/SCL4/GPIO188
CIR@ CIR_EN# J21 SPI_CS2#/GBE_STAT2/GPIO166
R442 1K_0402_5%

ACIN_FCH# D21 PS2KB_DAT/GPIO189
C20 PS2KB_CLK/GPIO190
D23 PS2M_DAT/GPIO191
C22 PS2M_CLK/GPIO192
<13,38,40,44> ACIN 2N7002DW-T/R7_SOT363-6 Q208B

T33 F21 KSO_0/GPIO209
T32 F20 KSO_1/GPIO210
T35 E20 KSO_2/GPIO211
T34 A22 KSO_3/GPIO212
T37 E18 KSO_4/GPIO213
T36 A20 KSO_5/GPIO214
T38 J18 KSO_6/GPIO215
T39 H18 KSO_7/GPIO216
T45 G18 KSO_8/GPIO217
T44 B21 KSO_9/GPIO218
T46 K18 KSO_10/GPIO219
T47 D19 KSO_11/GPIO220
T41 A18 KSO_12/GPIO221
T40 C18 KSO_13/GPIO222
T42 B19 KSO_14/GPIO223
T43 B17 KSO_15/GPIO224
T49 A24 KSO_16/GPIO225
T48 D17 KSO_17/GPIO226

HUDSON-M3_FCBGA656

USB MISC
USB 1.1
ACPI / WAKE UP EVENTS
USB 2.0
GPIO
HD AUDIO
USB 3.0
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC G8
USB_RCOMP B9 USB_RCOMP R329 1 2 11.8K_0402_1%

USB_FSD1P/GPIO186 H1
USB_FSD1N H3
USB_FSD0P/GPIO185 H6
USB_FSD0N H5

USB_HSD13P H10
USB_HSD13N G10
USB_HSD12P K10
USB_HSD12N J12
USB_HSD11P G12
USB_HSD11N F12
USB_HSD10P K12 USB20_P10 USB20_P10 <33>
USB_HSD10N K13 USB20_N10 USB20_N10 <33>
USB_HSD9P B11 USB20_P9 USB20_P9 <32>
USB_HSD9N D11 USB20_N9 USB20_N9 <32>
USB_HSD8P E10 USB20_P8 USB20_P8 <33>
USB_HSD8N F10 USB20_N8 USB20_N8 <33>
USB_HSD7P C10 USB20_P7 USB20_P7 <32>
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USB_HSD6N G9 USB20_N6 USB20_N6 <33>
USB_HSD5P A8 USB20_P5 USB20_P5 <28>
USB_HSD5N C8 USB20_N5 USB20_N5 <28>
USB_HSD4P F8
USB_HSD4N E8
USB_HSD3P C6
USB_HSD3N A6
USB_HSD2P C5 USB20_P2 USB20_P2 <31>
USB_HSD2N A5 USB20_N2 USB20_N2 <31>
USB_HSD1P C1 USB20_P1 USB20_P1 <31>
USB_HSD1N C3 USB20_N1 USB20_N1 <31>
USB_HSD0P E1 USB20_P0 USB20_P0 <31>
USB_HSD0N E3 USB20_N0 USB20_N0 <31>

USB 3.0 (For Hudson M3 only)
Felica
WLAN (BT)
Finger Printer
3G
Int. Camera
USB-Left
USB-Right2
USB-Right1

Hudson-M2/M3 OHCI (DEV-20, FUN-5)
Hudson-M2 OHCI (DEV-22, FUN-0) EHCI (DEV-22, FUN-2)
Hudson-M3 XHCI (DEV-16, FUN-0) XHCI (DEV-16, FUN-1)
Hudson-M2/M3 OHCI (DEV-19, FUN-0) EHCI (DEV-19, FUN-2)
Hudson-M2/M3 OHCI (DEV-18, FUN-0) EHCI (DEV-18, FUN-2) <Support Wakeup>

USBSS_CALRP C16 USBSS_CALRP R330 1 M3@ 2 1K_0402_1%
USBSS_CALRN A16 USBSS_CALRN R334 1 M3@ 2 1K_0402_1%
+VDDANCR_11_SSUSB

USB_SS_TX3P A14
USB_SS_TX3N C14
USB_SS_RX3P C12
USB_SS_RX3N A12
USB_SS_TX2P D15
USB_SS_TX2N B15
USB_SS_RX2P E14
USB_SS_RX2N F14
USB_SS_TX1P F15
USB_SS_TX1N G15
USB_SS_RX1P H13
USB_SS_RX1N G13
USB_SS_TX0P J16 USB30_TX0P USB30_TX0P <36>
USB_SS_TX0N H16 USB30_TX0N USB30_TX0N <36>
USB_SS_RX0P J15 USB30_RX0P USB30_RX0P <36>
USB_SS_RX0N K15 USB30_RX0N USB30_RX0N <36>

USB 3.0 (For Hudson M3 only)

Hudson-M3 XHCI (DEV-16, FUN-0) XHCI (DEV-16, FUN-1)

SCL2/GPIO193 H19 R326 1 2 10K_0402_5% +3VALW
SDA2/GPIO194 G19 R328 1 2 10K_0402_5%
SCL3_LV/GPIO195 G22 FCH_SIC
SDA3_LV/GPIO196 G21 FCH_SID R338 1 2 0_0402_5% APU_SIC <7,9>
R343 0_0402_5% APU_SID <7,9>
EC_PWM0/EC_TIMER0/GPIO197 F22
EC_PWM1/EC_TIMER1/GPIO198 H22
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 J22 EC_PWM2 EC_PWM2 <25>
EC_PWM3/EC_TIMER3/GPIO200 H21

KSI_0/GPIO201 K21
KSI_1/GPIO202 K22
KSI_2/GPIO203 F22
KSI_3/GPIO204 F24
KSI_4/GPIO205 E24
KSI_5/GPIO206 B23
KSI_6/GPIO207 C24
KSI_7/GPIO208 F18

SB-TSI
Strap

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

USB_OC3# is for USB port2
USB_OC1# is for USB port10
USB_OC0# is for USB port0 and port1

+3VS
R301 1 @ 2 8.2K_0402_5% PEG_CLKREQ#
R295 2 VGA@ 1 1K_0402_5%

+3VALW
R421 10K_0402_5% CR_CPPE#
R293 @ 10K_0402_5% VGA_PD_FCH
R278 10K_0402_5% H_THERMTRIP#
R288 10K_0402_5% FCH_SCLK1
R289 10K_0402_5% FCH_SDATA1
R272 @ 10K_0402_5% EC_LID_OUT#
R276 10K_0402_5% FCH_PCIE_WAKE#
RENE@ R306 10K_0402_5% USB30_SMI#
R318 10K_0402_5% USB_OC0#
R319 10K_0402_5% USB_OC1#
R489 10K_0402_5% USB_OC3#

+3VS
R286 2.2K_0402_5% FCH_SCLK0
R287 2.2K_0402_5% FCH_SDATA0
R291 @ 8.2K_0402_5% CLKREQ_WLAN#
R290 @ 8.2K_0402_5% CLKREQ_JET#
R281 @ 8.2K_0402_5% CLKREQ_CR#
R282 1K_0402_5%
R284 @ 8.2K_0402_5% CLKREQ_LAN#_R
R280 100K_0402_5% EC_RSMRST#
R324 @ 10K_0402_5% HDA_BITCLK
R325 @ 10K_0402_5% AZ_SDIN0_HD

+3VALW
R273 @ 2.2K_0402_5% TEST0
R274 @ 2.2K_0402_5% TEST1
R275 @ 2.2K_0402_5% TEST2

<9,30> HDMI_HPD
Q39 CEC@ 2N7002_SOT23-3
R313 10K_0402_5%
HDMI_HPD_Q

+3VALW
+3VS
R312 10K_0402_5% @
R311 10K_0402_5%
ODD_DA#_FCH R425 0_0402_5% ODD_DA#_Q
C363 0.1U_0402_16V4Z @
Q208A 2N7002DW-T/R7_SOT363-6
ODD_DA# <31>

Change ACIN_FCH to low-active for ACIN LED issue on DVT

Set cardreader clock as free-running

For FCH internal debug use (Internal 10K pull-down)

Place R425 and C363 close to FCH for ESD

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HDMI_EN# (Internal 8.2K PU)

HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU

Add R454 and R455 for UMA CRT DDC pull-high on DVT

To avoid LED flashing

Place JPW under DDR Door

For MP phase

For EMI

Socket: SP07000F500/SP07000H900

Q32B in page40

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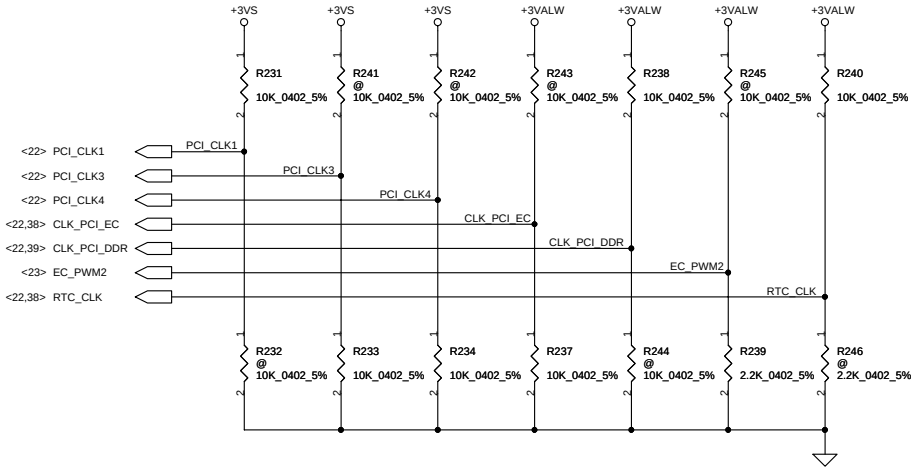
STRAP PINS

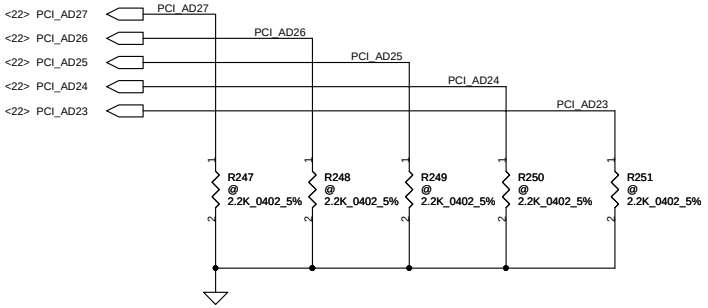
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



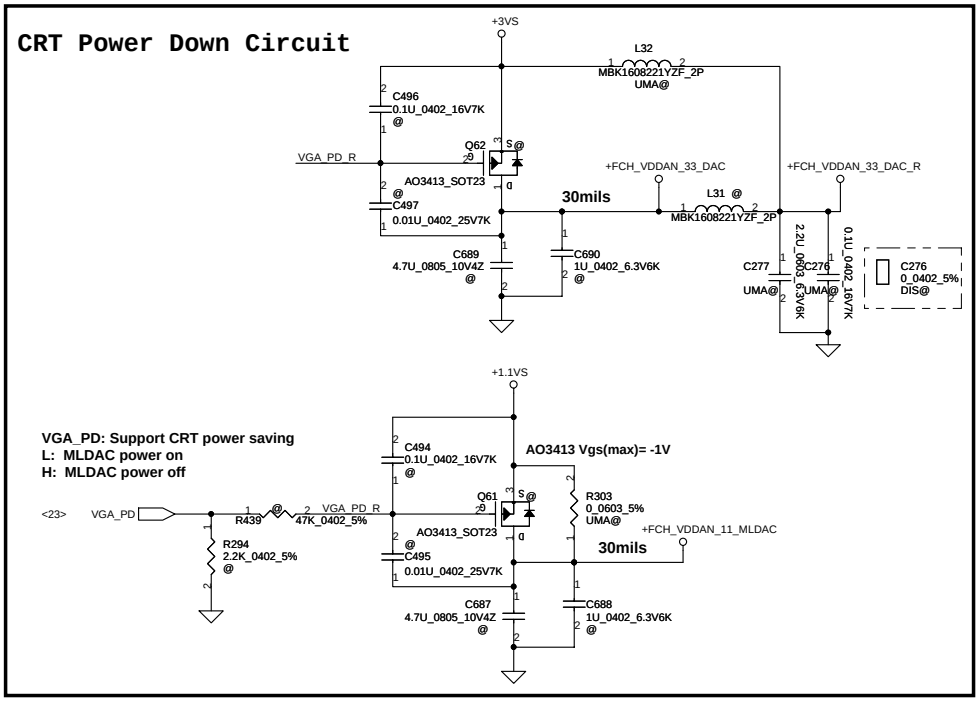
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



CRT Power Down Circuit



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Add Q56 to avoid +1.1VS_CKVDD leakage issue on DVT
Remove Q56 and stuff R371 after A13 version

VDDPL_33_SSUSB_S
For Hudson M3 USB3.0 only
For Hudson M2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB output

U1C HUDM3R3@ HUDSON-2

VDDIO_33_PCIGP_1	AB17	10mils	
VDDIO_33_PCIGP_2	AB18		
VDDIO_33_PCIGP_3	AE9		
VDDIO_33_PCIGP_4	AD10		
VDDIO_33_PCIGP_5	AG7		
VDDIO_33_PCIGP_6	AC13		
VDDIO_33_PCIGP_7	AB12		
VDDIO_33_PCIGP_8	AB13		
VDDIO_33_PCIGP_9	AB14		
VDDIO_33_PCIGP_10	AB16		102mA
VDDPL_3.3V	H24	10mils	
VDDPL_33_SYS	V22	47mA	
VDDPL_33_MLDAC	U22	10mils	
VDDPL_33_DAC	T22	20mA	
VDDPL_33_ML	L18	10mils	
VDDAN_33_DAC	D7	12mA	
VDDPL_33_SSUSB_S	AH29	10mils	
VDDPL_33_USB_S	AG28	11mA	
VDDPL_33_PCIE	M31	10mils	
VDDPL_33_SATA	V21	12mA	
LDO_CAP	Y23	15mils	
VDDPL_11_DAC	V24	7mA	
VDDAN_11_ML_1	V25	20mils	
VDDAN_11_ML_2	AB10		
VDDAN_11_ML_3	AB11		226mA
VDDAN_11_ML_4	AA11		
VDDIO_33_GBE_S	AA9		
VDDCR_11_GBE_S_1	AA10		
VDDCR_11_GBE_S_2	G7	30mils	
VDDIO_GBE_S_1	H8		
VDDIO_GBE_S_2	J8		
VDDAN_33_USB_S_1	K8		
VDDAN_33_USB_S_2	K9		
VDDAN_33_USB_S_3	M9		
VDDAN_33_USB_S_4	M10		
VDDAN_33_USB_S_5	N9		
VDDAN_33_USB_S_6	N10		
VDDAN_33_USB_S_7	M12		470mA
VDDAN_33_USB_S_8	N12		
VDDAN_33_USB_S_9	M11		
VDDAN_33_USB_S_10	U12	20mils	
VDDAN_33_USB_S_11	U13		
VDDAN_33_USB_S_12			
VDDAN_11_USB_S_1			140mA
VDDAN_11_USB_S_2	T12		
VDDCR_11_USB_S_1	T13		42mA
VDDCR_11_USB_S_2	P16	40mils	
VDDAN_11_SSUSB_S_1	M14		
VDDAN_11_SSUSB_S_2	N14		
VDDAN_11_SSUSB_S_3	P13		
VDDAN_11_SSUSB_S_4	P14		282mA
VDDAN_11_SSUSB_S_5			
VDDCR_11_SSUSB_S_1	N16		
VDDCR_11_SSUSB_S_2	N17		
VDDCR_11_SSUSB_S_3	P17		424mA
VDDCR_11_SSUSB_S_4	M17		

HUDSON-M3_FCBGA656

VDDCR_11_1	T14	50mils	
VDDCR_11_2	T17		
VDDCR_11_3	T20		
VDDCR_11_4	U16		
VDDCR_11_5	U18		
VDDCR_11_6	V14		
VDDCR_11_7	V17		
VDDCR_11_8	V20		
VDDCR_11_9	Y17		1007mA
VDDAN_11_CLK_1	H26	20mils	
VDDAN_11_CLK_2	J25		
VDDAN_11_CLK_3	K24		
VDDAN_11_CLK_4	L22		
VDDAN_11_CLK_5	M22		340mA
VDDAN_11_CLK_6	N21		
VDDAN_11_CLK_7	N22		
VDDAN_11_CLK_8	P22		
VDDAN_11_PCIE_1	AB24	50mils	
VDDAN_11_PCIE_2	Y21		
VDDAN_11_PCIE_3	AE25		
VDDAN_11_PCIE_4	AD24		
VDDAN_11_PCIE_5	AB23		1088mA
VDDAN_11_PCIE_6	AA22		
VDDAN_11_PCIE_7	AF26		
VDDAN_11_PCIE_8	AG27		
VDDAN_11_SATA_1	AA21	60mils	
VDDAN_11_SATA_4	Y20		
VDDAN_11_SATA_2	AB21		
VDDAN_11_SATA_3	AB22		
VDDAN_11_SATA_5	AC22		
VDDAN_11_SATA_6	AC21		1337mA
VDDAN_11_SATA_7	AA20		
VDDAN_11_SATA_8	AA18		
VDDAN_11_SATA_9	AB20		
VDDAN_11_SATA_10	AC19		
VDDIO_33_S_1	N18	10mils	
VDDIO_33_S_2	L19		
VDDIO_33_S_3	M18		
VDDIO_33_S_4	V12		
VDDIO_33_S_5	V13		59mA
VDDIO_33_S_6	Y12		
VDDIO_33_S_7	Y13		
VDDIO_33_S_8	W11		
VDDXL_33_S	G24	10mils	5mA
VDDCR_11_S_1	N20	10mils	187mA
VDDCR_11_S_2	M20		
VDDPL_11_SYS_S	J24	10mils	70mA
VDDAN_33_HWM_S	M8	10mils	12mA
VDDIO_AZ_S	AA4	10mils	26mA

POWER

U1E HUDM3R3@ HUDSON-2

A3	VSS	VSS	T25
A33	VSS	VSS	T27
B7	VSS	VSS	U6
B13	VSS	VSS	U14
D9	VSS	VSS	U17
D13	VSS	VSS	U20
E5	VSS	VSS	U21
E12	VSS	VSS	U30
E16	VSS	VSS	U32
E29	VSS	VSS	V11
F7	VSS	VSS	V16
F9	VSS	VSS	V18
F11	VSS	VSS	W4
F13	VSS	VSS	W6
F16	VSS	VSS	W25
F17	VSS	VSS	W28
F19	VSS	VSS	Y14
F23	VSS	VSS	Y16
F25	VSS	VSS	Y18
F29	VSS	VSS	AA6
G6	VSS	VSS	AA12
G16	VSS	VSS	AA13
G32	VSS	VSS	AA14
H12	VSS	VSS	AA16
H15	VSS	VSS	AA17
H29	VSS	VSS	AA25
J6	VSS	VSS	AA28
J9	VSS	VSS	AA30
J10	VSS	VSS	AA32
J13	VSS	VSS	AB25
J28	VSS	VSS	AC6
J32	VSS	VSS	AC18
K7	VSS	VSS	AC28
K16	VSS	VSS	AD27
K27	VSS	VSS	AE6
K28	VSS	VSS	AE15
L6	VSS	VSS	AE21
L12	VSS	VSS	AE28
L13	VSS	VSS	AF8
L15	VSS	VSS	AF12
L16	VSS	VSS	AF16
L21	VSS	VSS	AF33
M13	VSS	VSS	AG30
M16	VSS	VSS	AG32
M21	VSS	VSS	AH5
M25	VSS	VSS	AH11
N6	VSS	VSS	AH18
N11	VSS	VSS	AH19
N13	VSS	VSS	AH21
N23	VSS	VSS	AH23
N24	VSS	VSS	AH25
P12	VSS	VSS	AH27
P18	VSS	VSS	AJ18
P20	VSS	VSS	AJ28
P21	VSS	VSS	AJ29
P31	VSS	VSS	AK21
P33	VSS	VSS	AK25
R4	VSS	VSS	AL18
R11	VSS	VSS	AM21
R25	VSS	VSS	AM25
R28	VSS	VSS	AN1
T11	VSS	VSS	AN18
T16	VSS	VSS	AN28
T18	VSS	VSS	AN33
N8	VSSAN_HWM	VSSPL_DAC	T21
		VSSAN_DAC	L26
K25	VSSXL	VSSANQ_DAC	K33
		VSSIO_DAC	N28
H25	VSSPL_SYS		
		EFUSE	R6

GROUND

HUDSON-M3_FCBGA656

Connect to GND through a dedicated via

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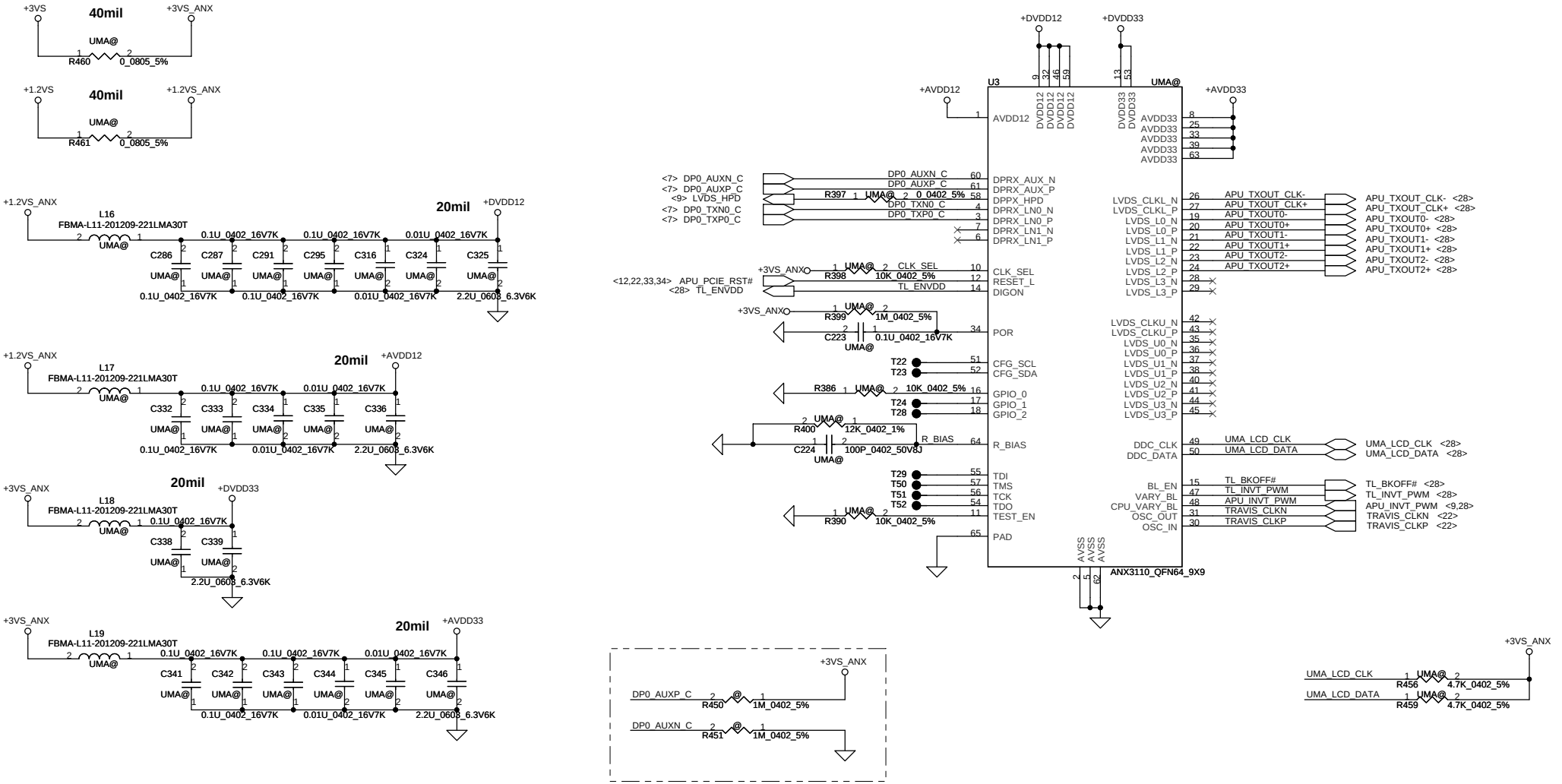

Place via on each trace bus and let resistor very close the via

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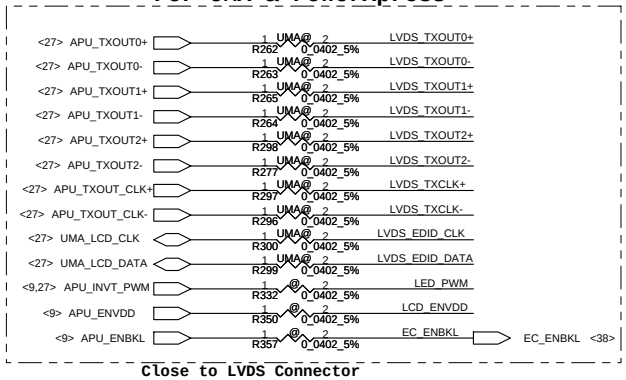
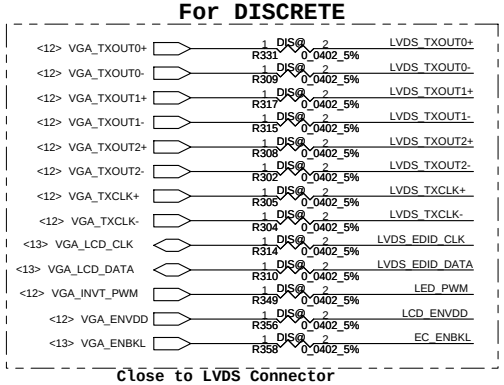
For UMA & PowerXpress



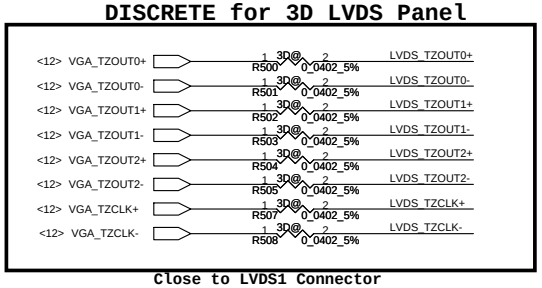
Close to LVDS Connector

For DISCRETE



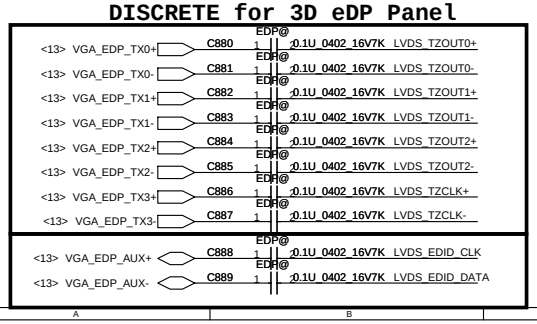
Close to LVDS Connector

DISCRETE for 3D LVDS Panel



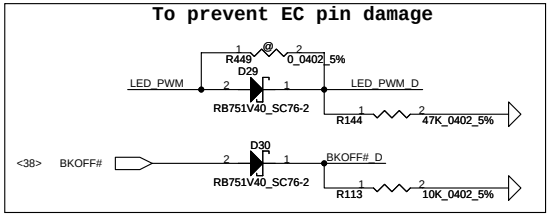
Close to LVDS1 Connector

DISCRETE for 3D eDP Panel

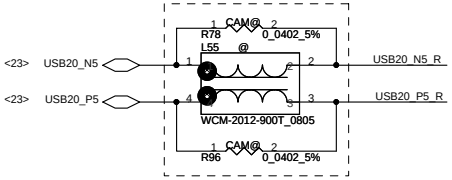


Close to LVDS Connector

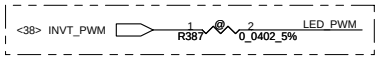
To prevent EC pin damage



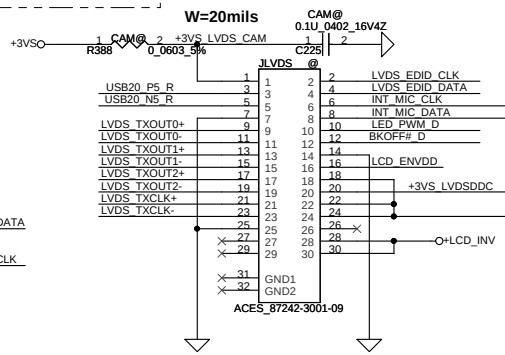
Reserve for EMI request

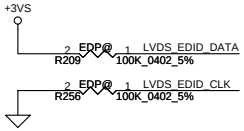


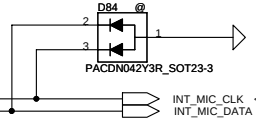
EC PWM

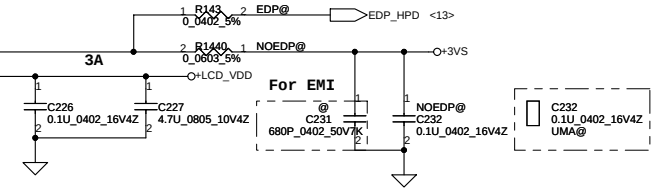


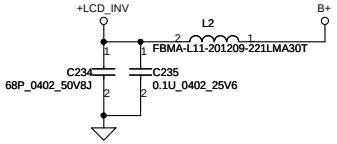
LCD/PANEL BD. Conn.



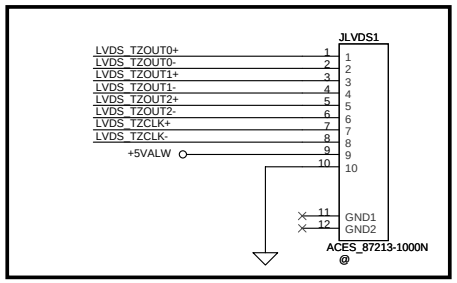


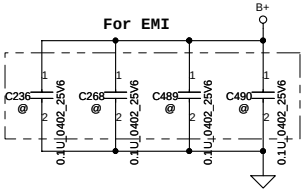


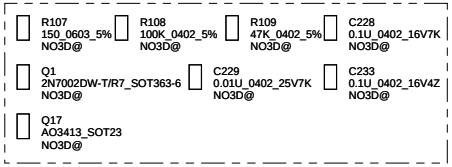




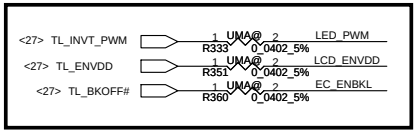
For 3D LVDS Panel







For LVDS Translator



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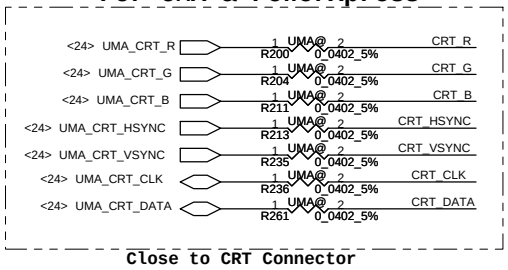
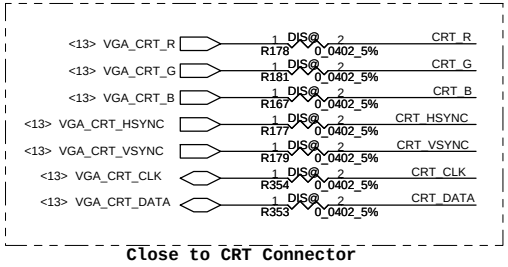
CRT CONNECTOR

For UMA & PowerXpress

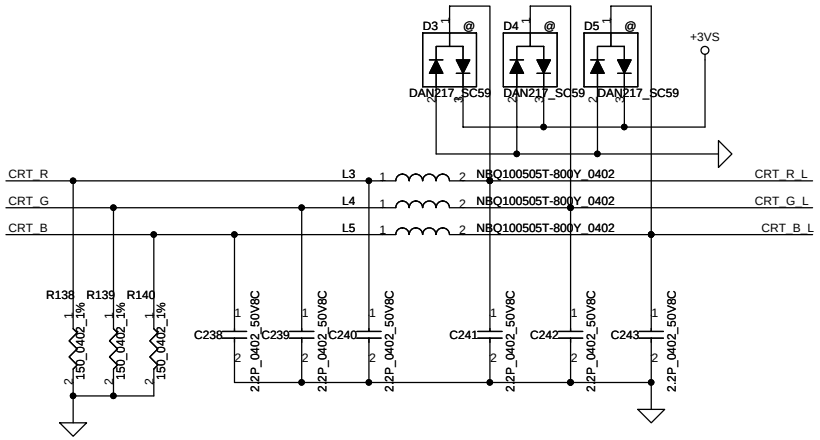


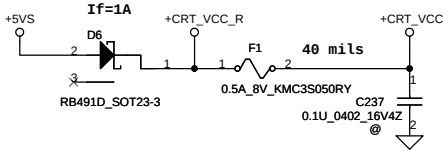
Close to CRT Connector

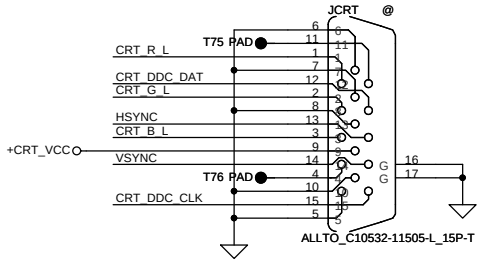
For DISCRETE

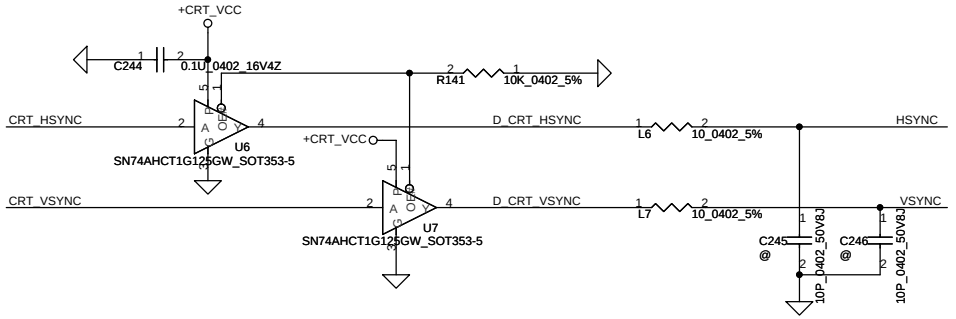


Close to CRT Connector

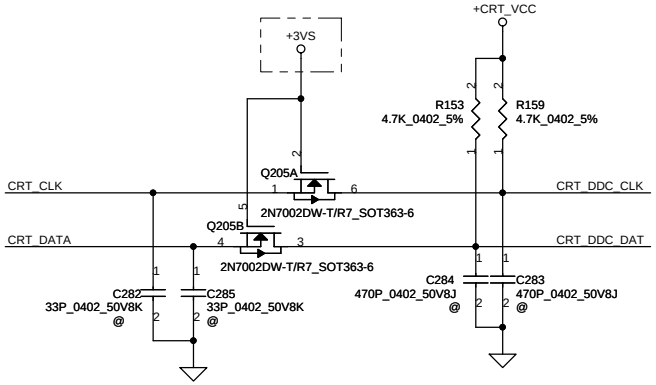








Change Q205 power to +3VS on DVT



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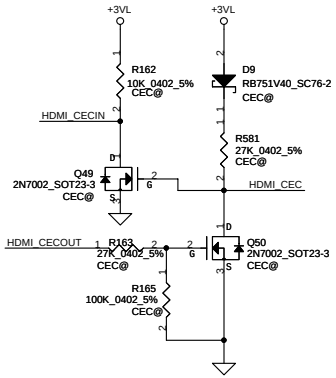
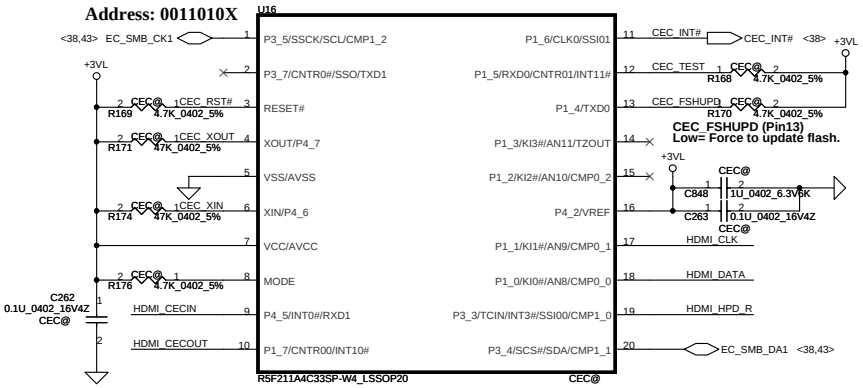
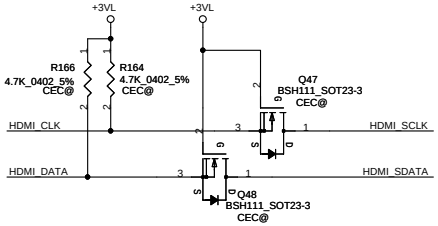
HDMI CEC Controller



Address: 0011010X



CEC_FSHUPD (Pin13)
Low= Force to update flash.

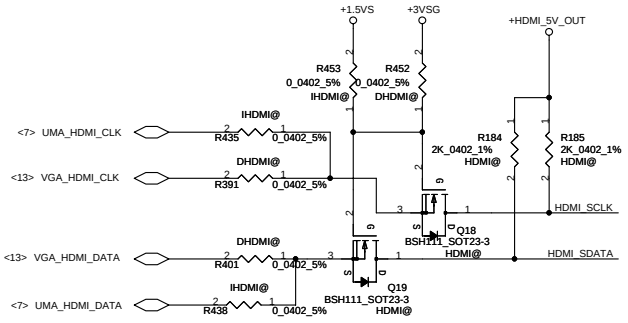


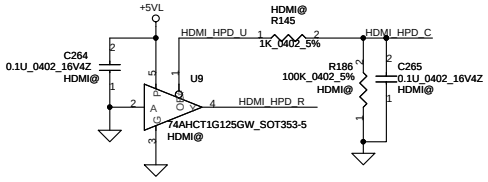
For DISCRETE

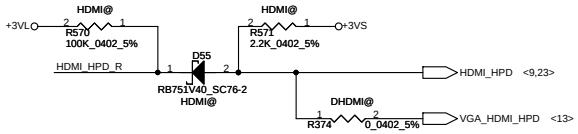
<13> VGA_HDMI_CLK+	CV296	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXC+
<13> VGA_HDMI_CLK-	CV293	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXC-
<13> VGA_HDMI_TX0+	CV294	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD0+
<13> VGA_HDMI_TX0-	CV297	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD0-
<13> VGA_HDMI_TX1+	CV299	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD1+
<13> VGA_HDMI_TX1-	CV298	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD1-
<13> VGA_HDMI_TX2+	CV295	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD2+
<13> VGA_HDMI_TX2-	CV300	0.1U_0402_16V7K DHDMI@	VGA_DVI_TXD2-

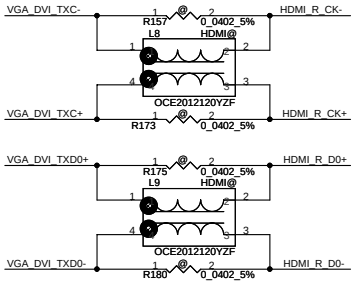
For UMA & PowerXpress

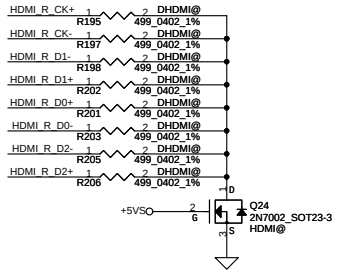
<5> UMA_HDMI_TXC+	CV308	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC+
<5> UMA_HDMI_TXC-	CV304	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXC-
<5> UMA_HDMI_TX0+	CV306	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0+
<5> UMA_HDMI_TX0-	CV302	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD0-
<5> UMA_HDMI_TX1+	CV303	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1+
<5> UMA_HDMI_TX1-	CV301	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD1-
<5> UMA_HDMI_TX2+	CV307	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2+
<5> UMA_HDMI_TX2-	CV305	0.1U_0402_16V7K IHDMI@	VGA_DVI_TXD2-

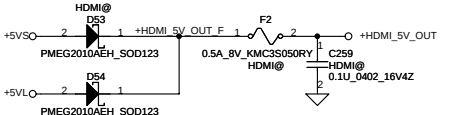






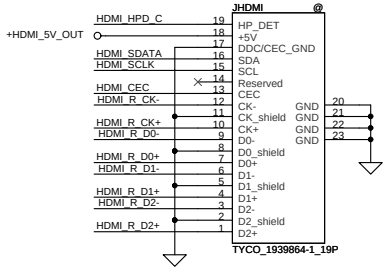






R195 604_0402_1% IHDMI@		R197 604_0402_1% IHDMI@	
R198 604_0402_1% IHDMI@		R202 604_0402_1% IHDMI@	
R201 604_0402_1% IHDMI@		R203 604_0402_1% IHDMI@	
R205 604_0402_1% IHDMI@		R206 604_0402_1% IHDMI@	

HDMI Connector



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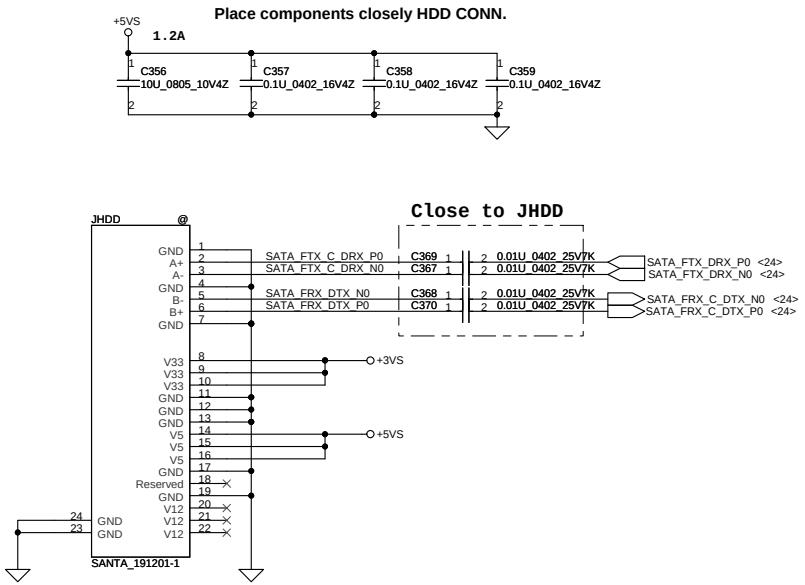
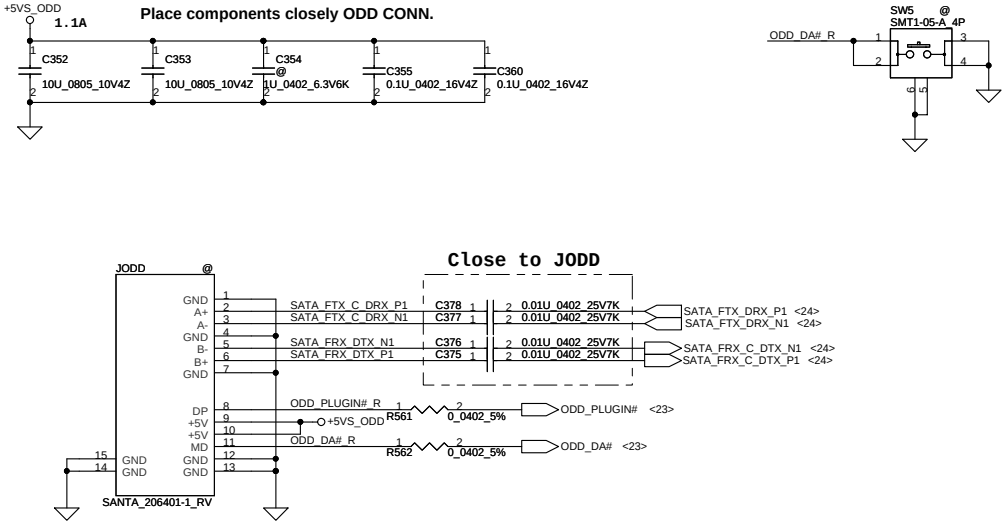
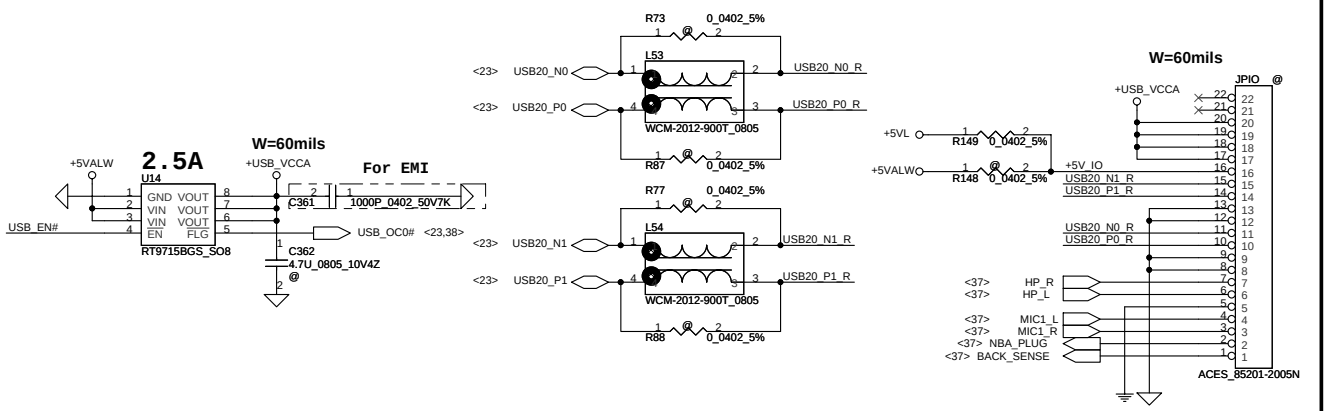
SATA HDD Conn.



SATA ODD Conn.

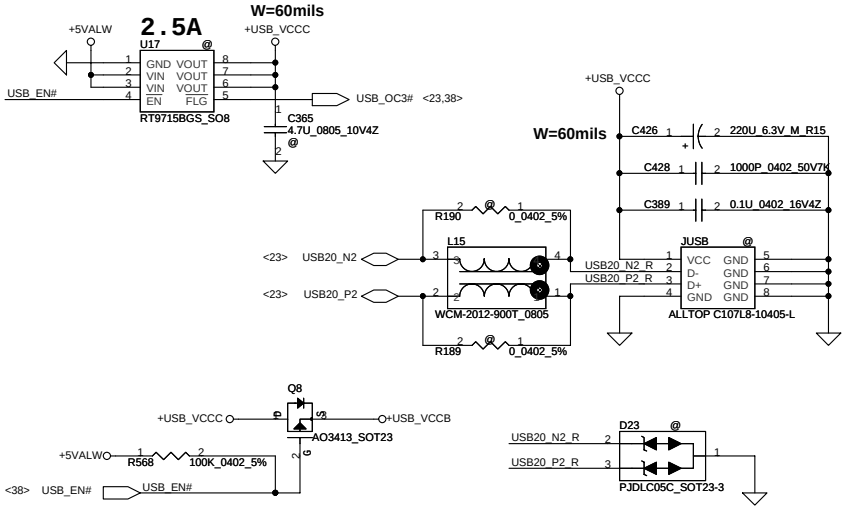


USB Board@ Right Side



USB Board@ Left Side

Add U17 for left USB2.0 wake-up issue on PVT



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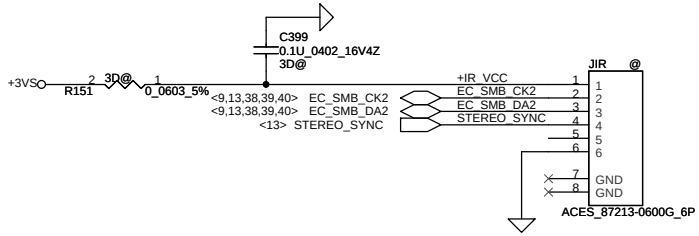
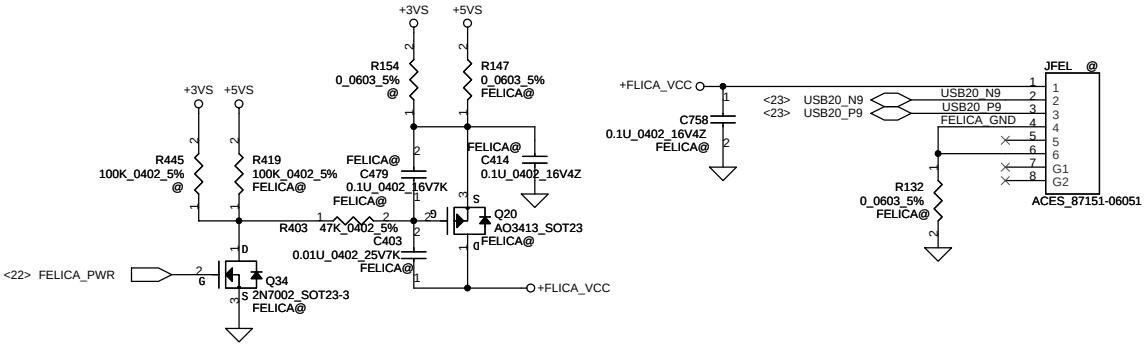
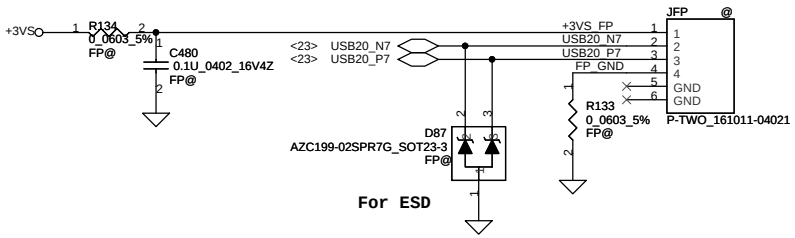
IR Emitter Connector



Felica



Finger printer



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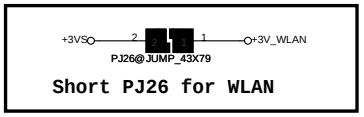
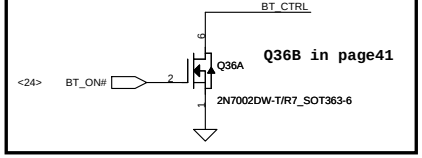
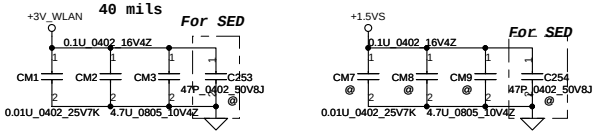
Slot 1 Half PCIe Mini Card-WLAN

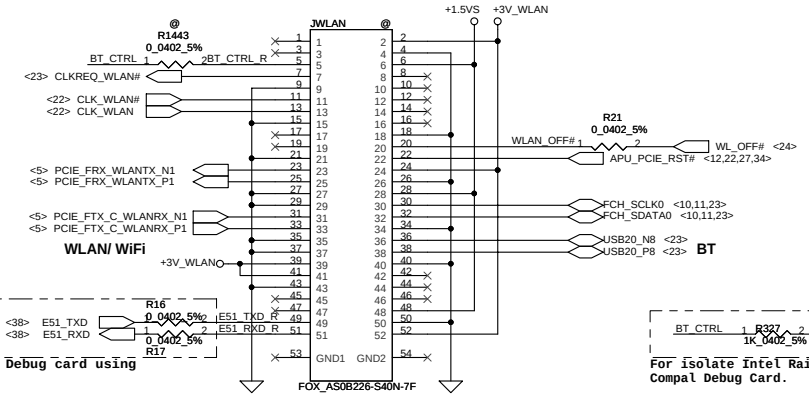


WLAN&BT Combo module circuits

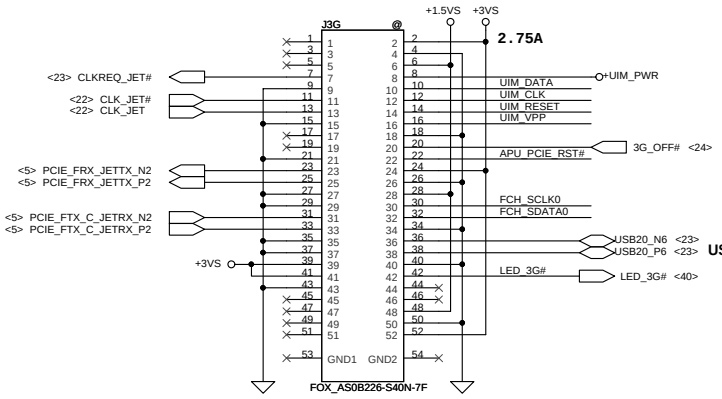
	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H

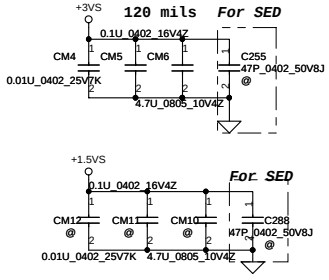


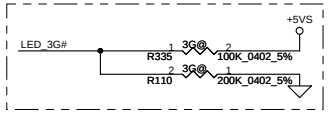


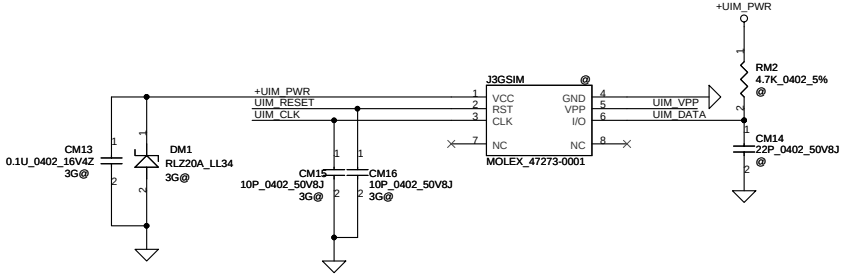


Slot 2 Full PCIe Mini Card- 3G
Half PCIe Mini Card- JET



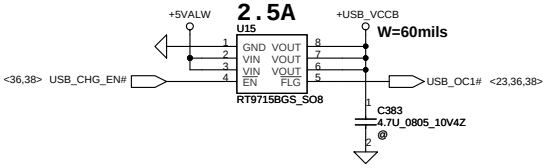


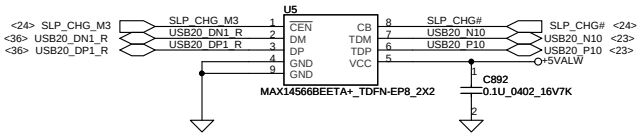




USB Sleep & Charge:
Auto-Mode
Mode3

MAX14566B		
CB SLP_CHG#	CEN# SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM





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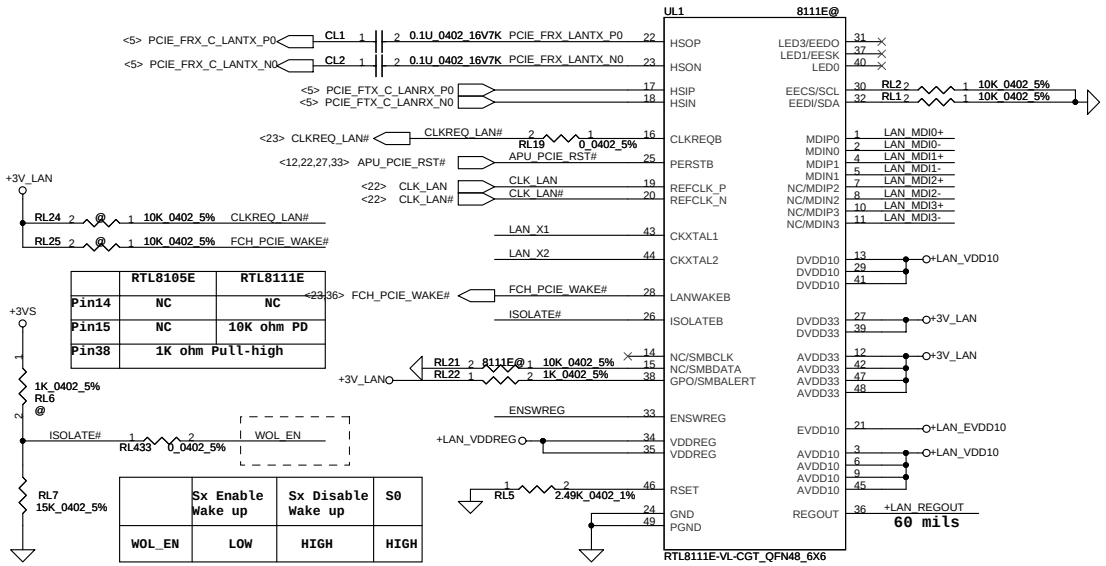
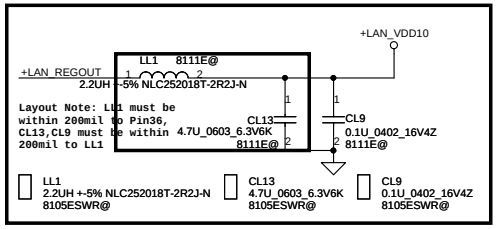
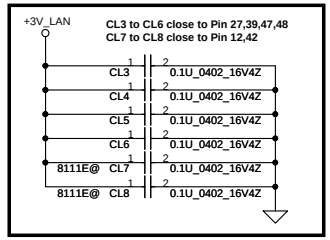
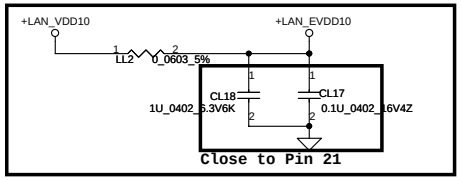


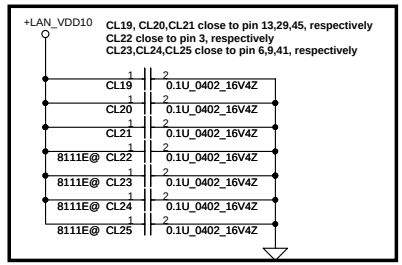
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

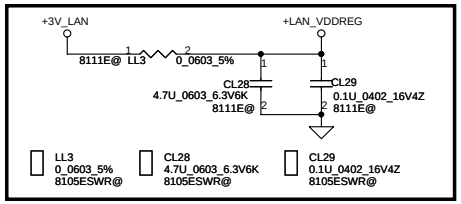
	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN	LOW	HIGH	HIGH

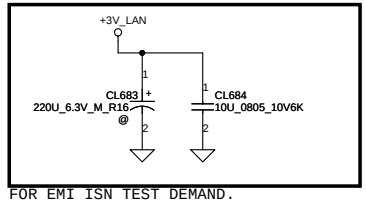






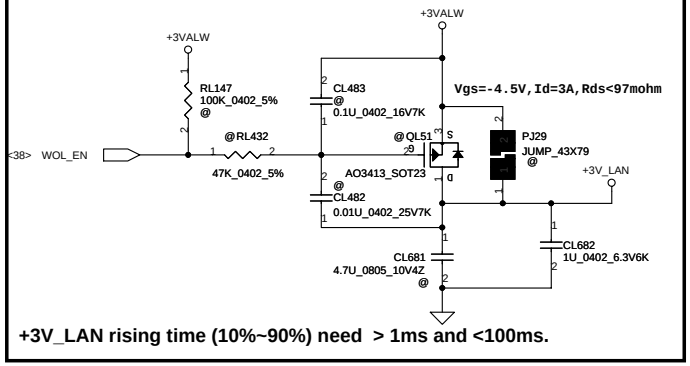




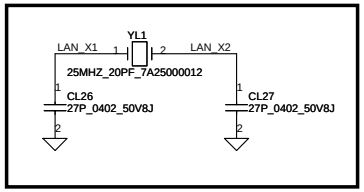


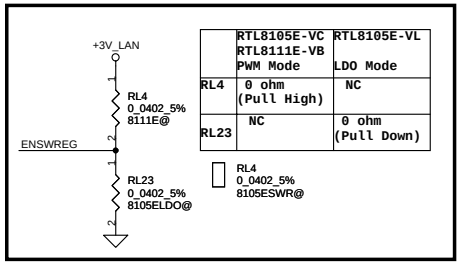
FOR EMI ISN TEST DEMAND.

+3VALW TO +3V_LAN



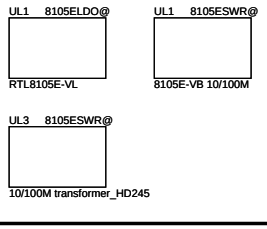
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

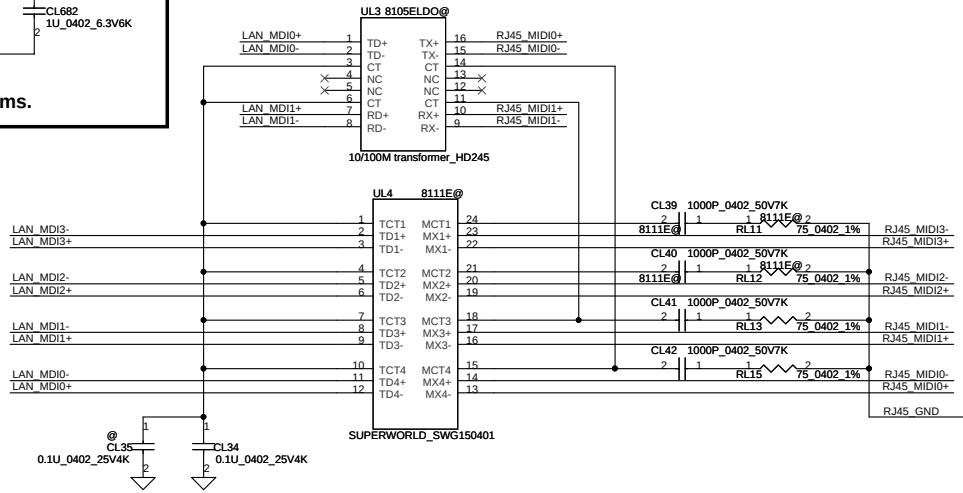




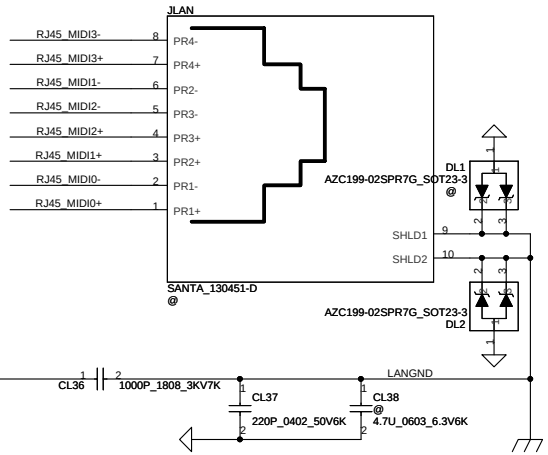
	RTL8105E-VC RTL8111E-VB PWM Mode	RTL8105E-VL LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

For P/N and footprint
Please place them to ISPD page





LAN Conn.



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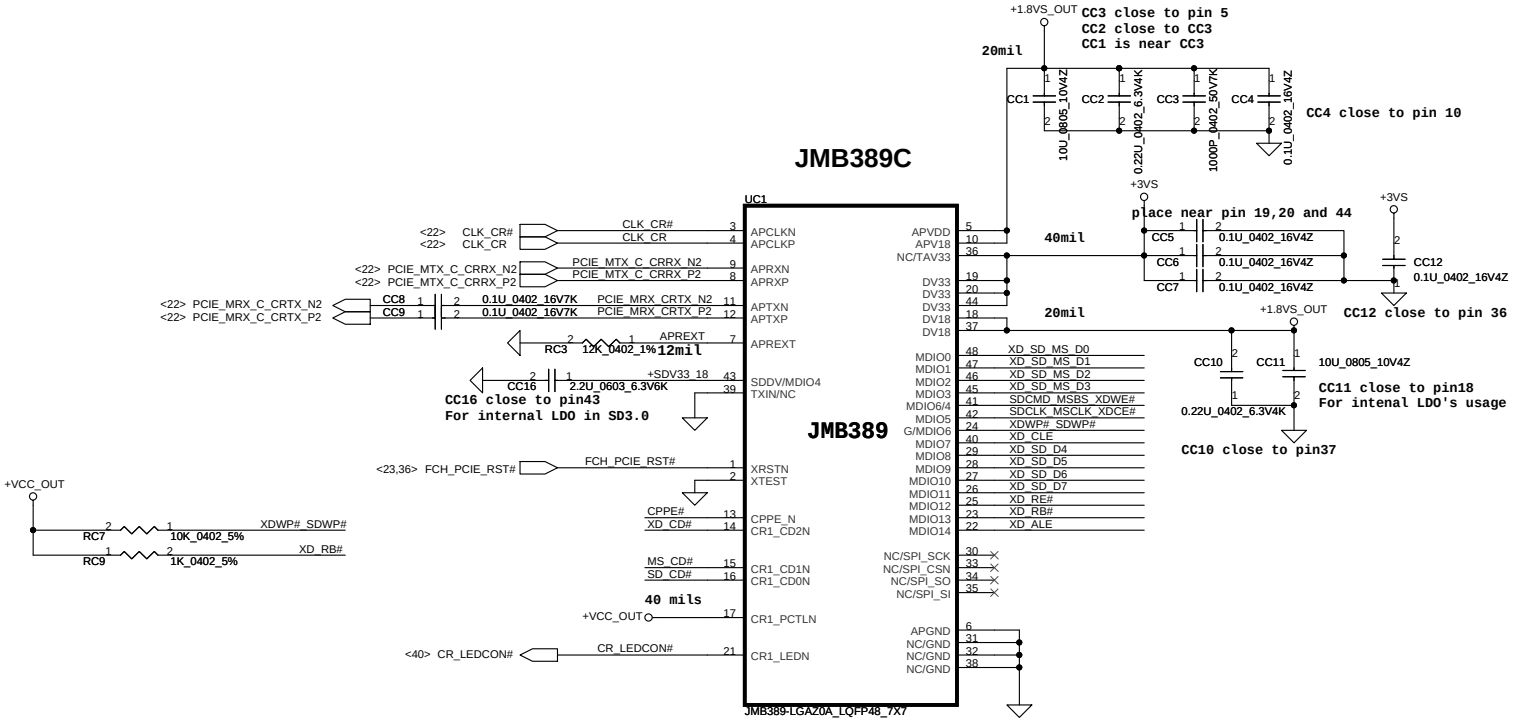
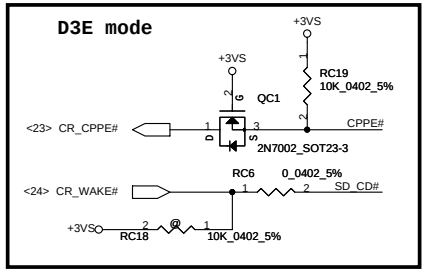
JMB389C

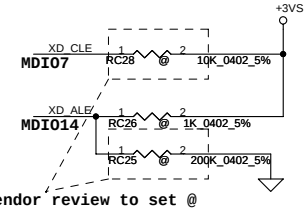


D3E mode

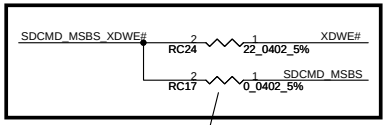


Power On Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LEDCON# high active	CR_LEDCON# low active★

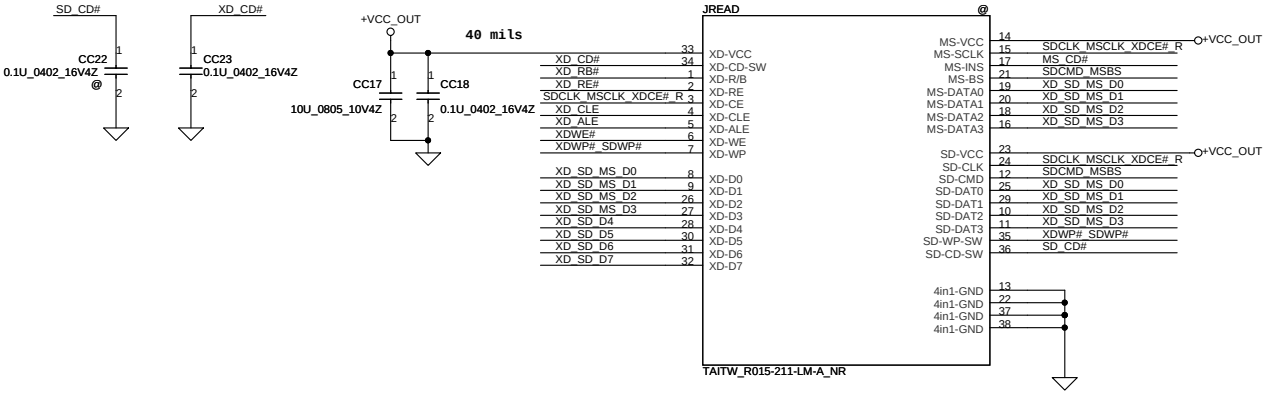


Add RC24 and RC17 close to UC1 for xD issue

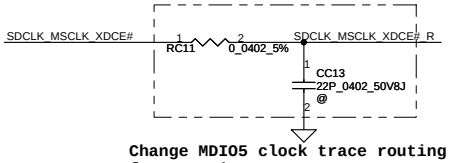


Change RC17 to 0 ohm for SDXC performance low issue on PVT

5 in 1 Card Reader



Reserved for EMI,close to UC1.42



Change MDIO5 clock trace routing for SDHC issue on DVT

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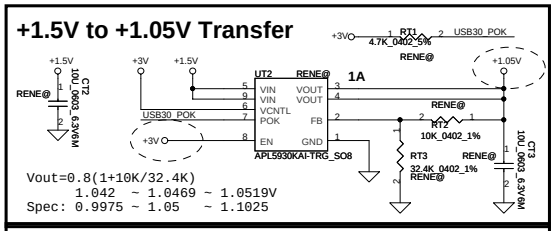
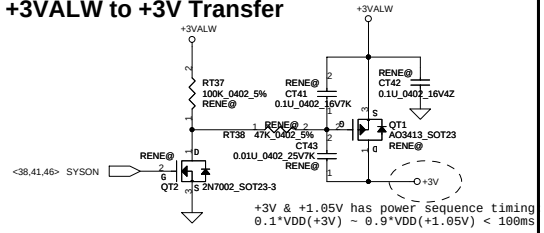
+1.5V to +1.05V Transfer



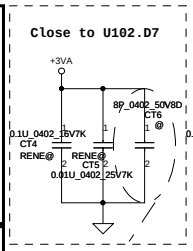
Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

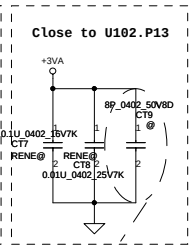


+3V & +1.05V has power sequence timing
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms

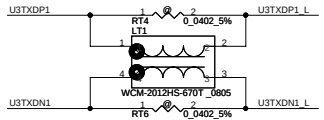
Close to U102.D7

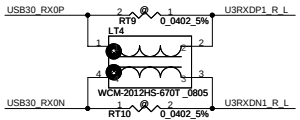


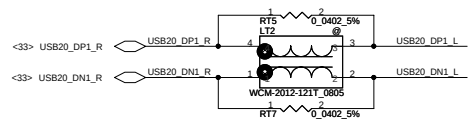
Close to U102.P13



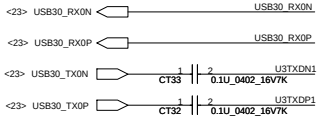
Follow Vendor recommend.

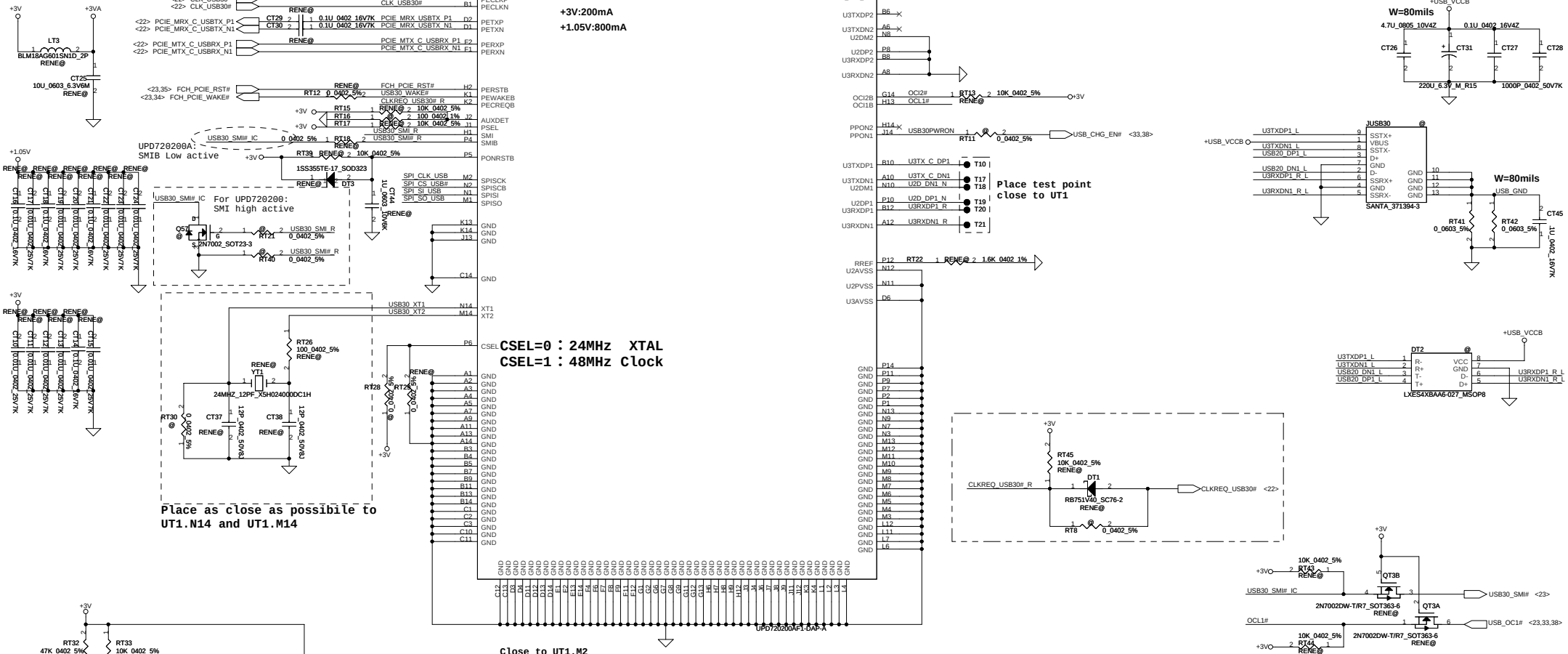




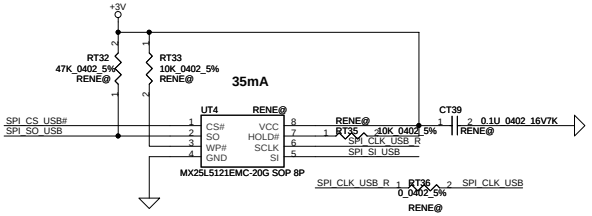


Remove USB3.0 co-layout resistor on DVT

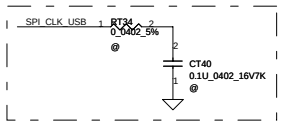




UPD720200A:
SMB Low active



Close to UT1.M2



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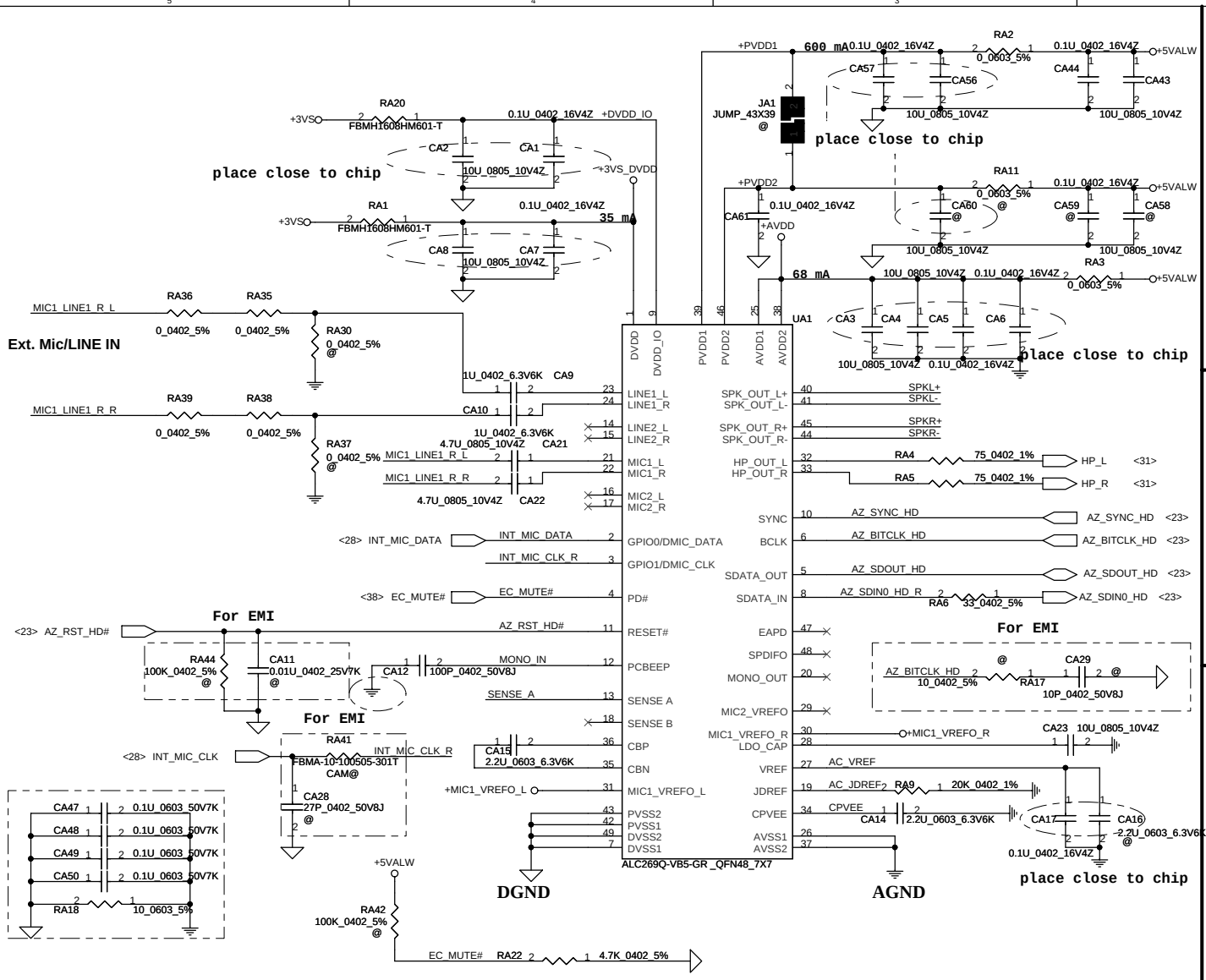
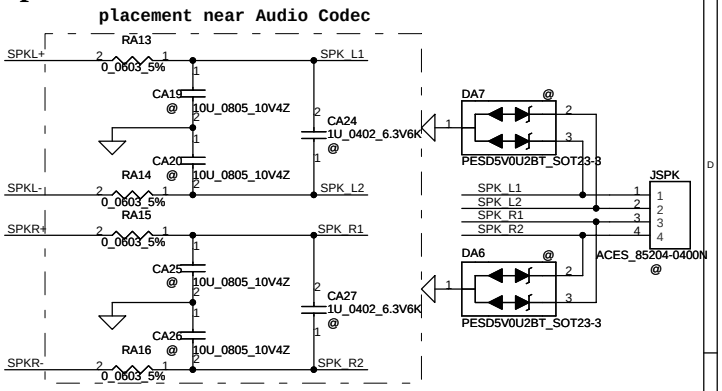


Speaker Connector

placement near Audio Codec



Beep sound

EC Beep

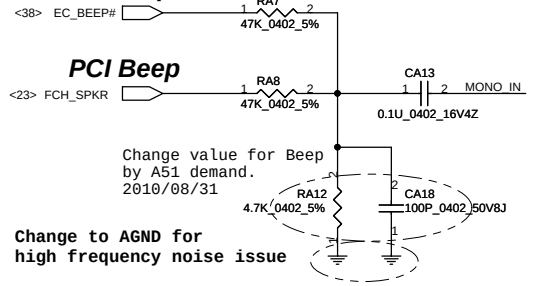
<38> EC_BEEP#

PCI Beep

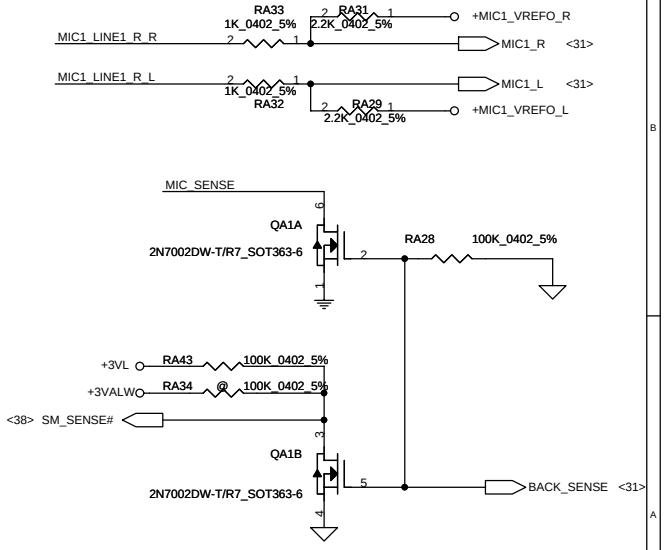
<23> FCH_SPKR

Change value for Beep by A51 demand. 2010/08/31

Change to AGND for high frequency noise issue

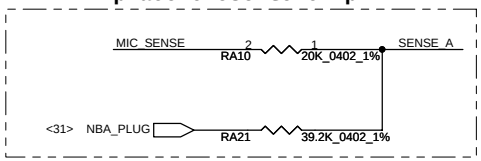


Ext.MIC/LINE IN JACK



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

place close to chip



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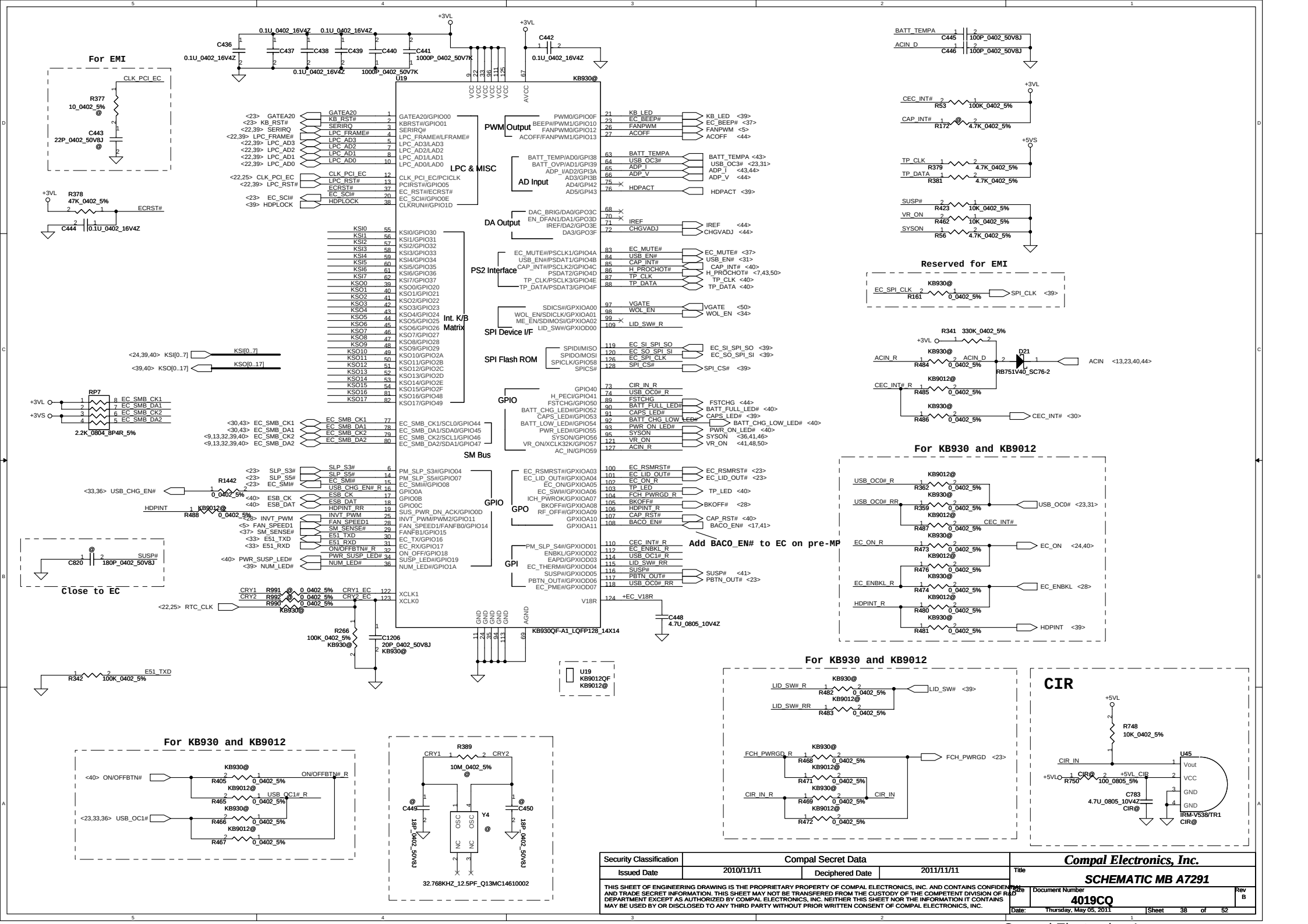

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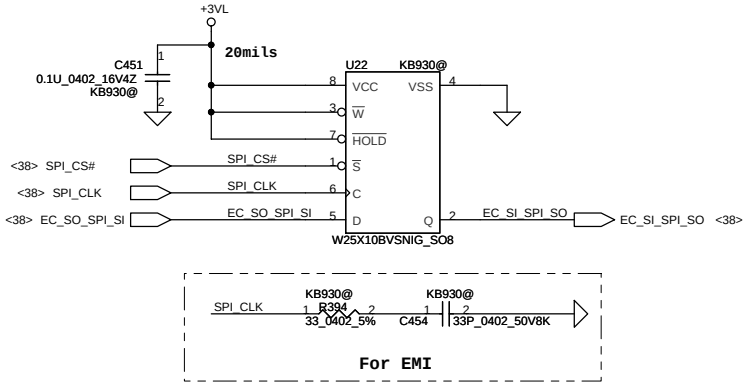
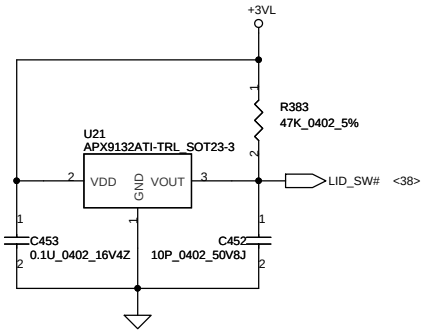
SPI Flash (128KB)

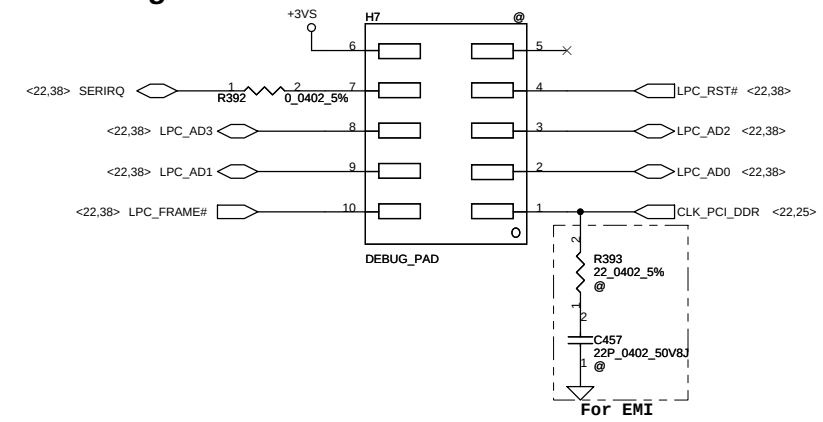


Lid SW

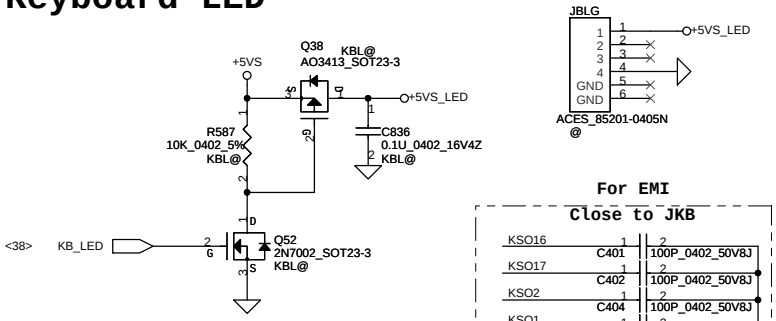


LPC Debug Port

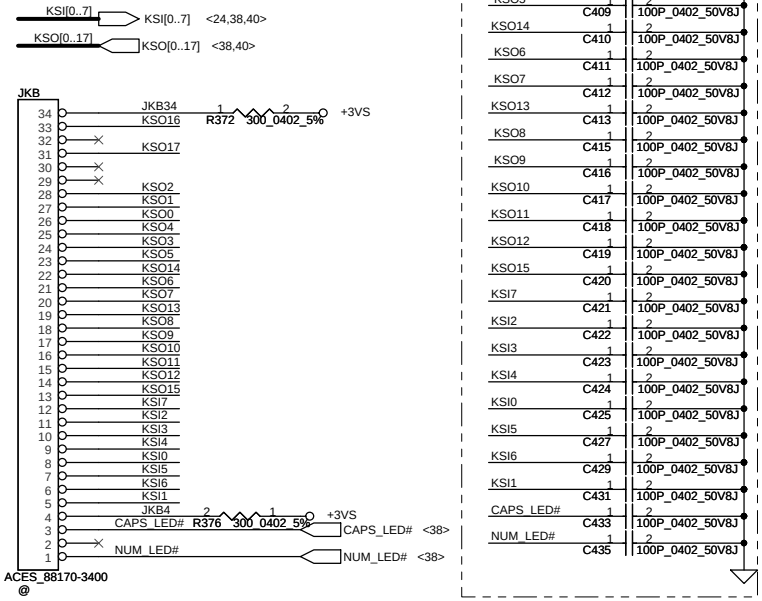
Place the PAD under DDR DIMM.



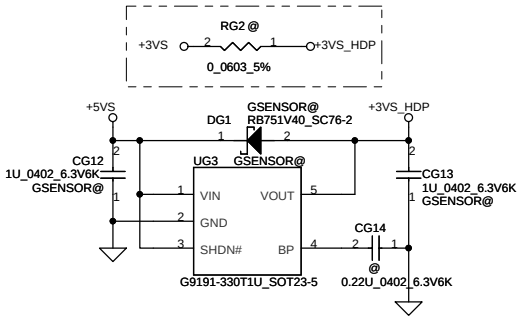
Keyboard LED



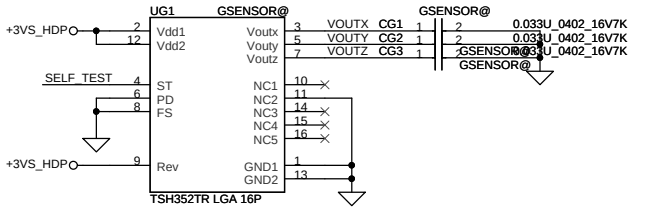
KEYBOARD CONN.

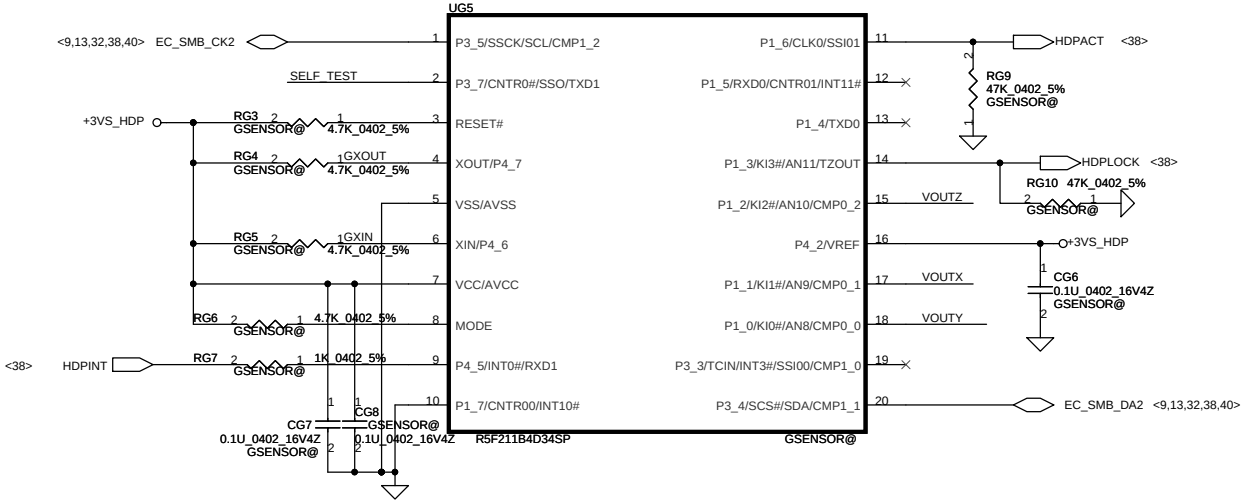


G-Sensor



Place UG1 on TOP Layer





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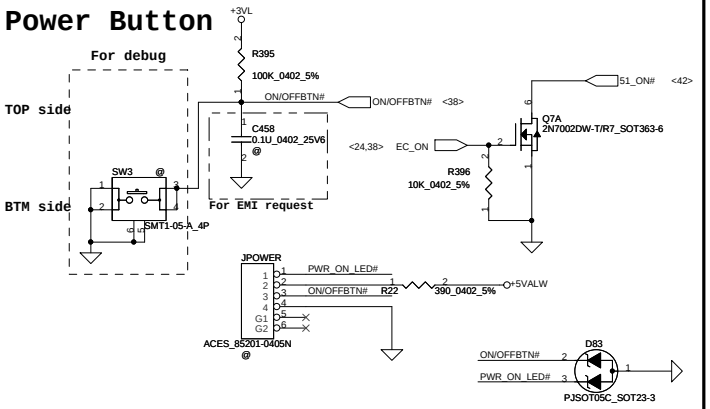
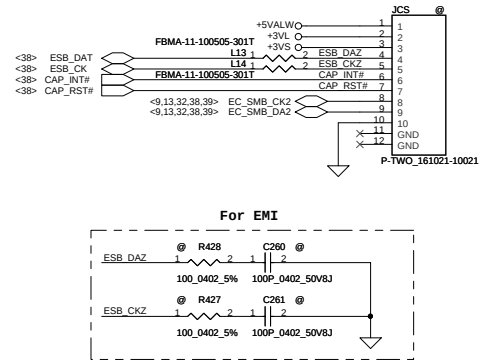
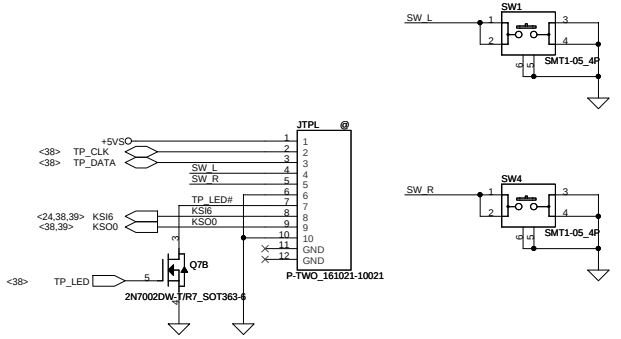
Power Button



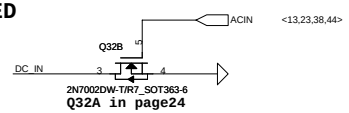
Caps Sensor/Light Sensor Conn.



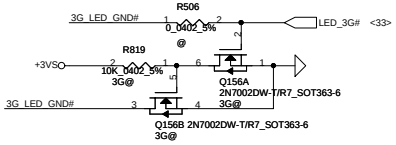
Touchpad & Light Pipe Connector



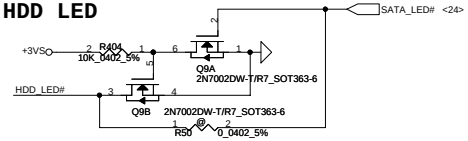
DC-IN LED



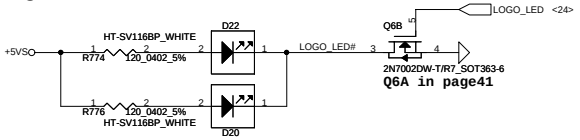
3G LED



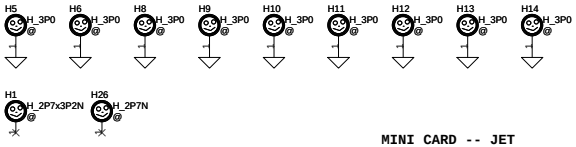
HDD LED



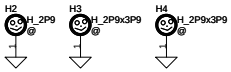
Logo LED



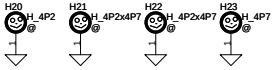
Screw Hole



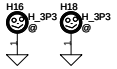
VGA



CPU

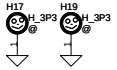


MINI CARD -- JET

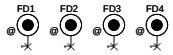


MINI CARD -- 3G

MINI CARD -- WLAN

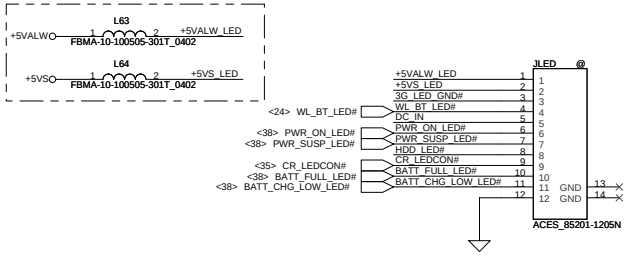


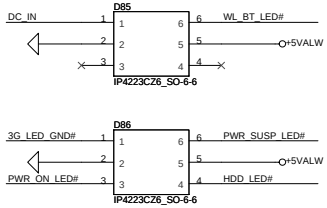
PCB Fedical Mark PAD



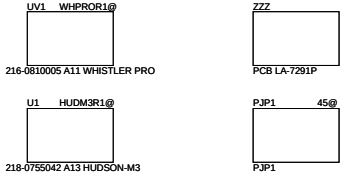
LED/B Connector

Add L63 and L64 for EMI on PVT





ISPD



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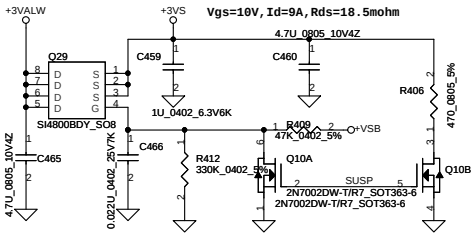
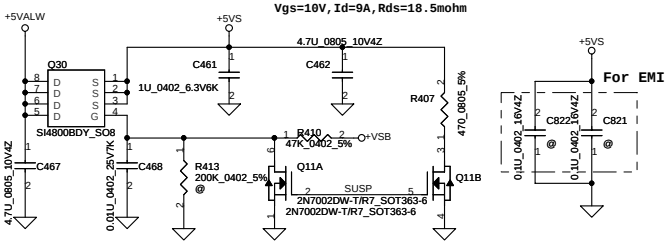
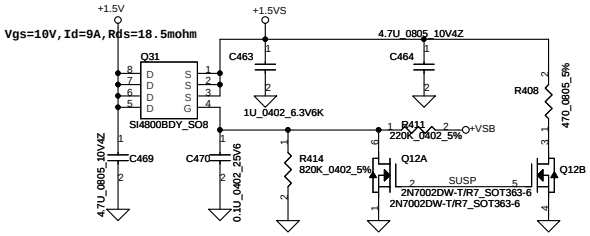
+3VALW TO +3VS



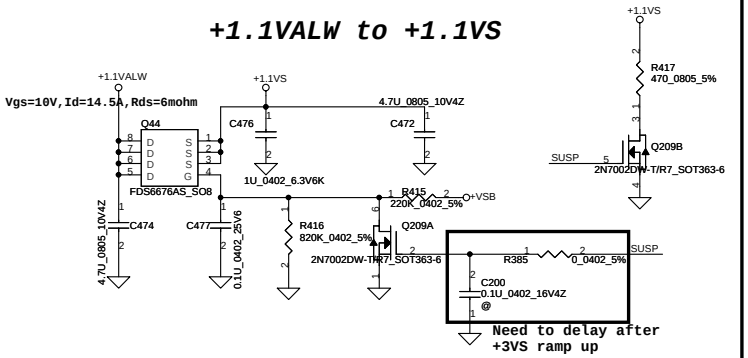
+5VALW TO +5VS

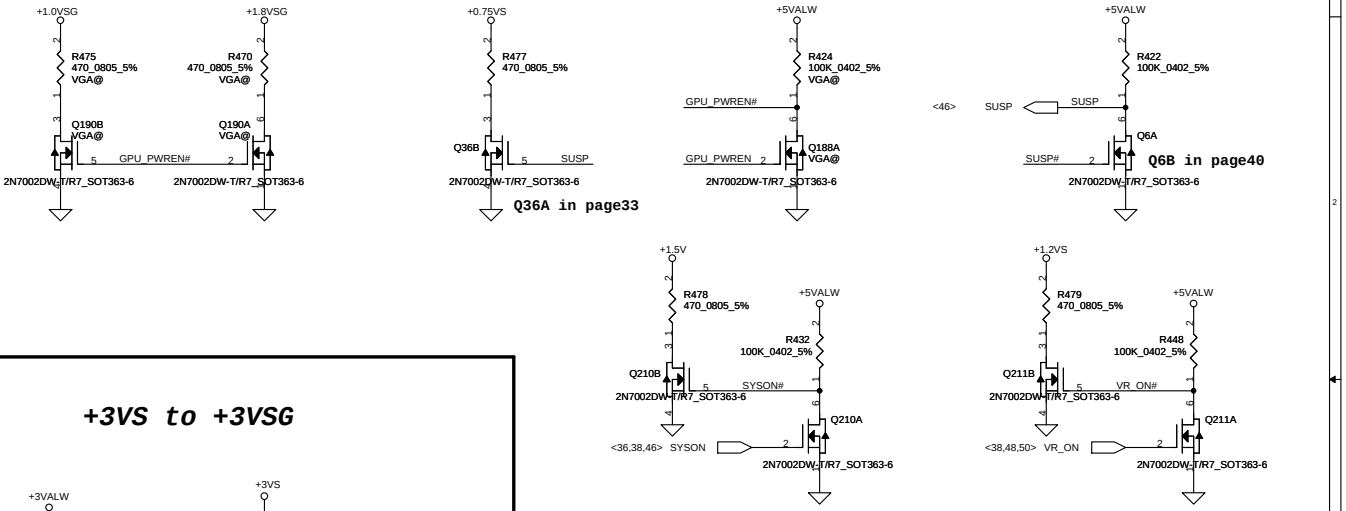


+1.5V to +1.5VS

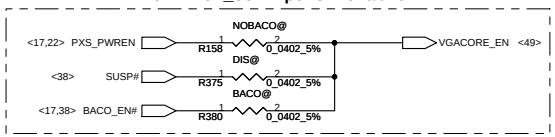


+1.1VALW to +1.1VS

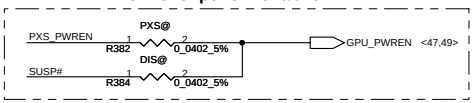




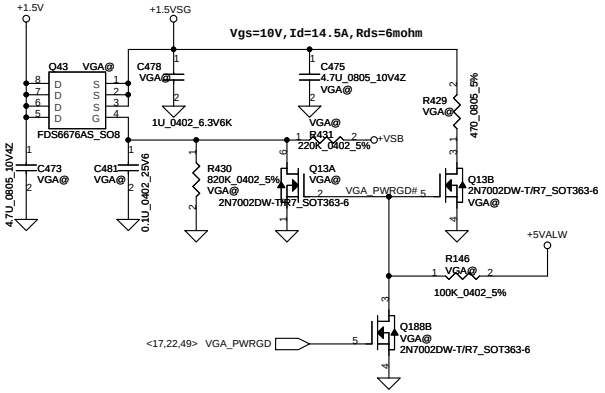
For +VGA_CORE power enable



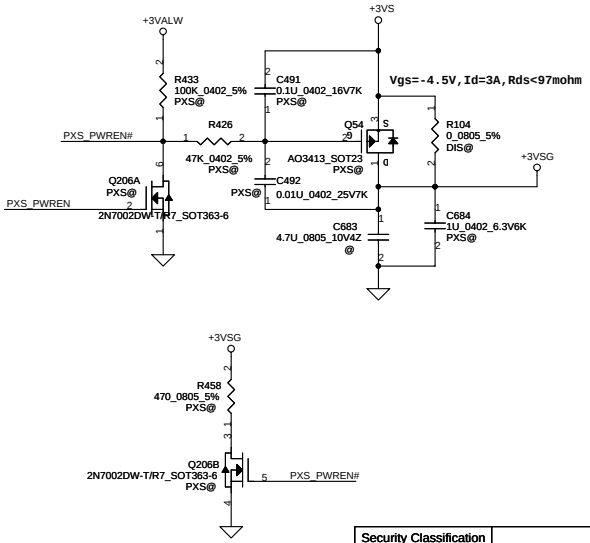
For GPU power enable



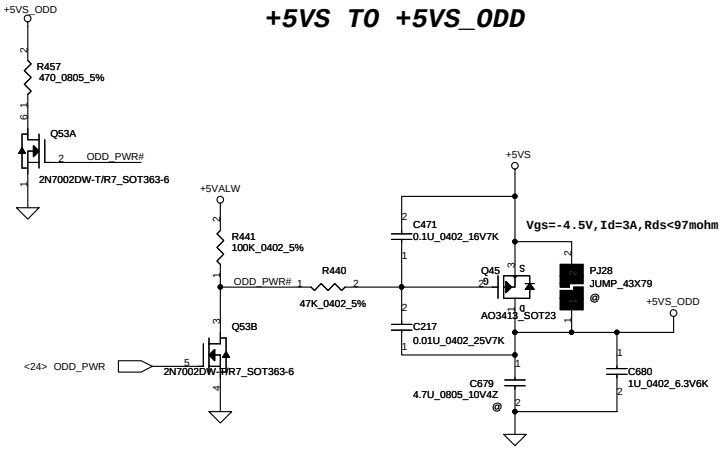
+1.5V to +1.5VSG



+3VS to +3VSG



+5VS TO +5VS_ODD



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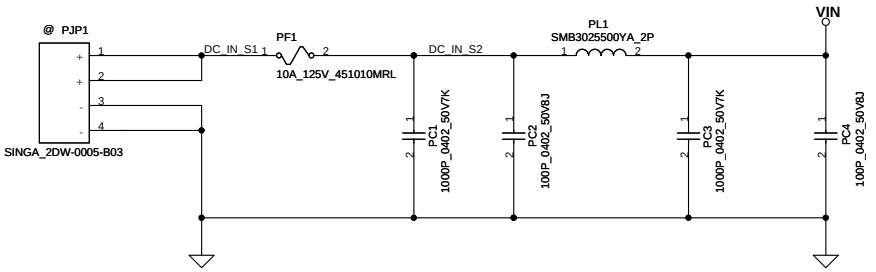
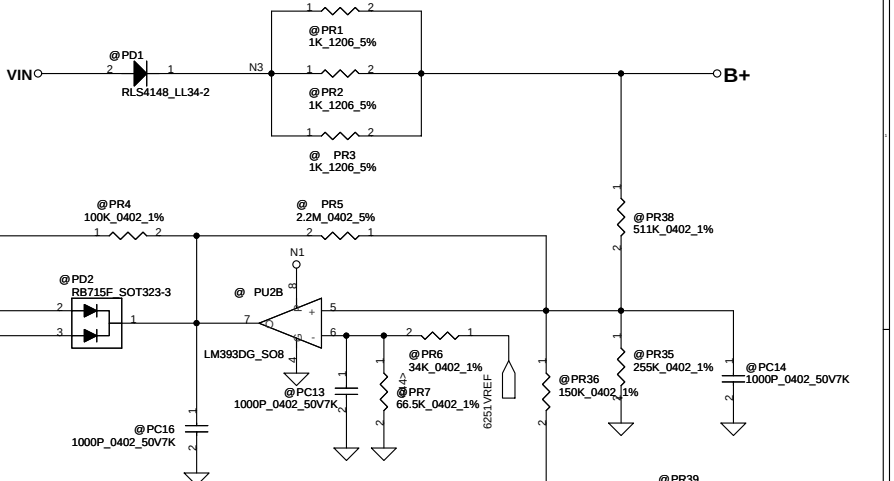
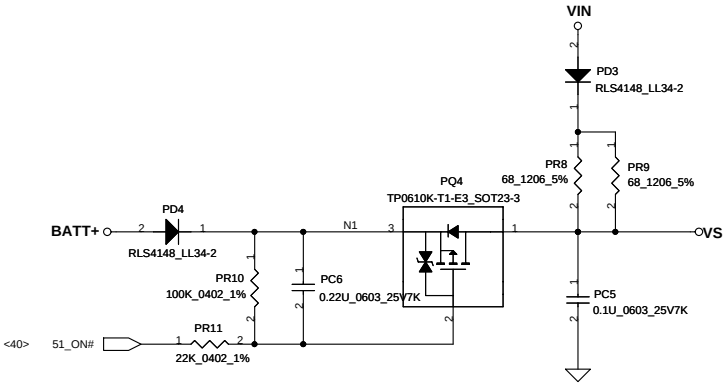
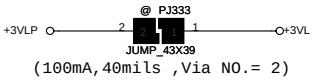
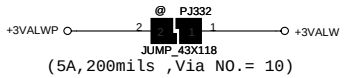




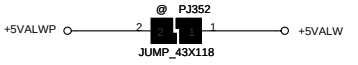




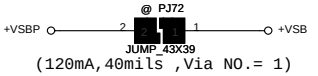
(100mA,40mils ,Via NO.= 2)



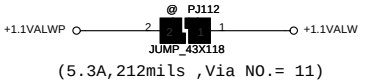
(5A,200mils ,Via NO.= 10)
OCP=7.7A



(5A,200mils ,Via NO.= 10)
OCP=7.9A

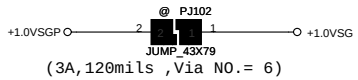


(120mA,40mils ,Via NO.= 1)

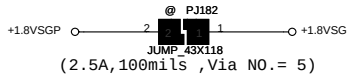


(5.3A,212mils ,Via NO.= 11)

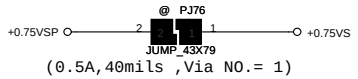
OCP=6.814A



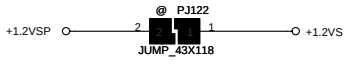
(3A,120mils ,Via NO.= 6)



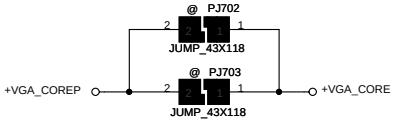
(2.5A,100mils ,Via NO.= 5)



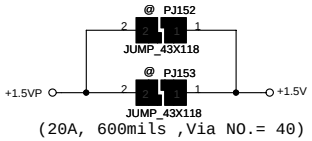
(0.5A,40mils ,Via NO.= 1)



(6.5A,260mils ,Via NO.= 13)
OCP=8.553A

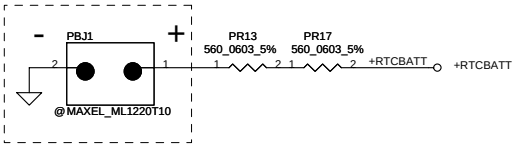


(28A,1120mils ,Via NO.= 56)
OCP=36A



(20A, 600mils ,Via NO.= 40)
OCP=24.136A

RTC Battery



SP093MX0000

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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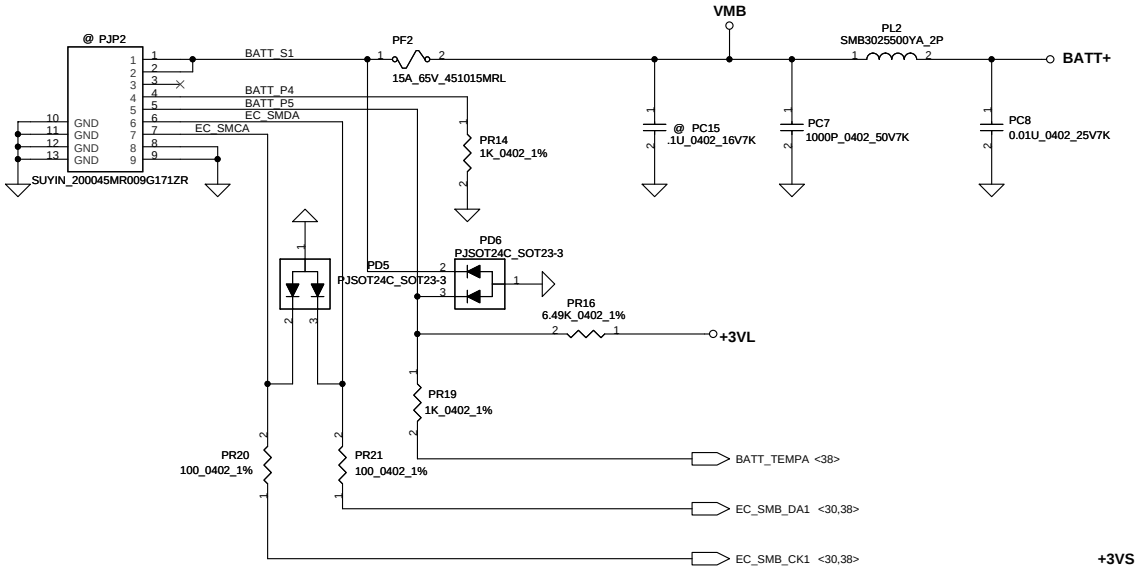
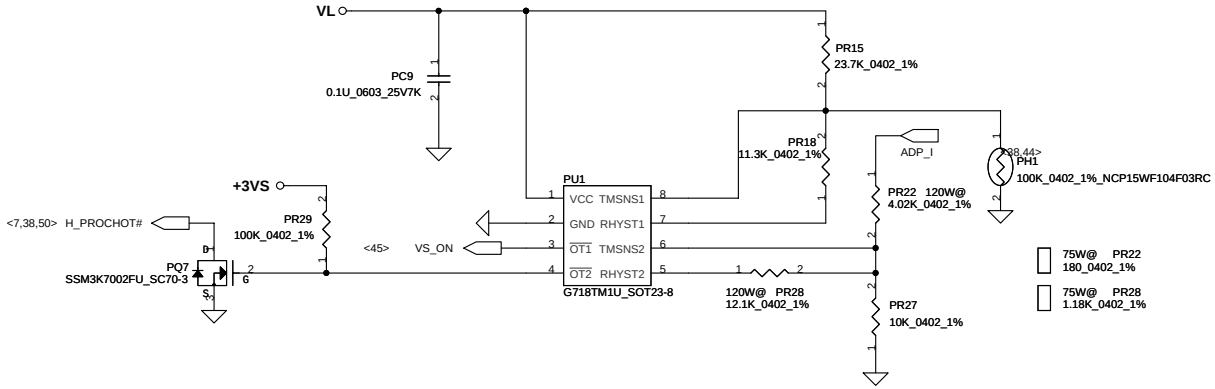
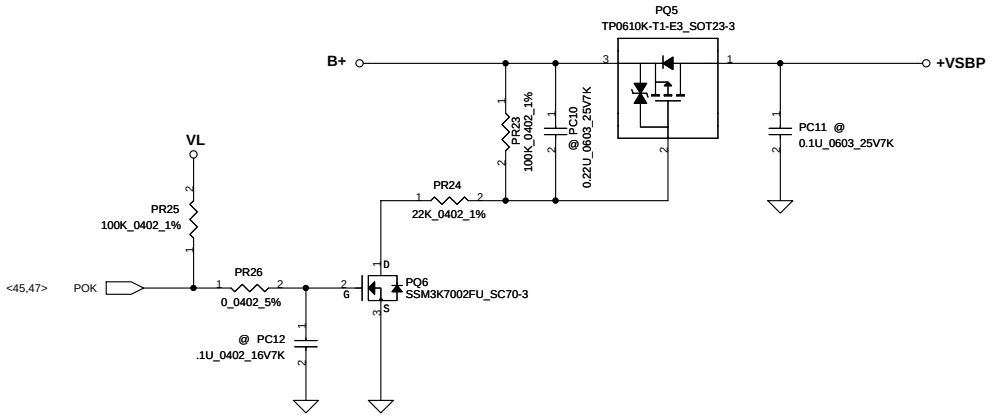


PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
Rset = 3 * 7.87K = 23.61K ==> 23.7K
Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K





Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
120W	148.73W	2.34V	115.2W	1.81V
75W	86.64W	1.82V	72W	1.51V

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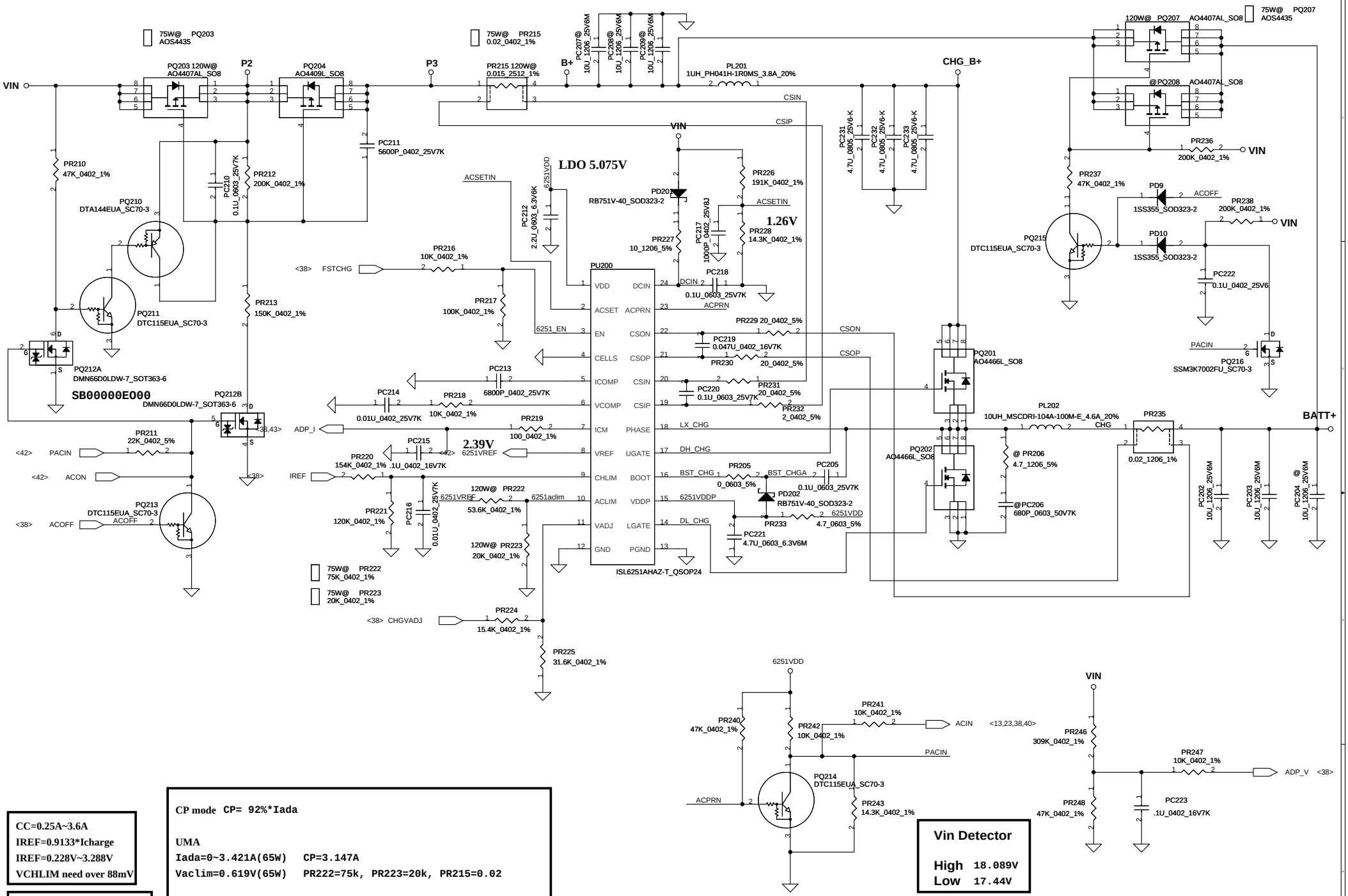

CC=0.25A~3.6A
IREF=0.9133*Icharge
IREF=0.228V~3.288V
VCHLIM need over 88mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

CP mode CP= 92%*Iada

UMA
Iada=0~3.421A(65W) CP=3.147A
Vaclim=0.619V(65W) PR222=75k, PR223=20k, PR215=0.02

DIS
Iada=0~4.74A(90W) CP=4.36A
Vaclim=0.735V(90W) PR222=53.6k, PR223=20k, PR215=0.015

Vin Detector

High 18.089V
Low 17.44V

1.26 / 14.3 * 205.3 = 18.089V

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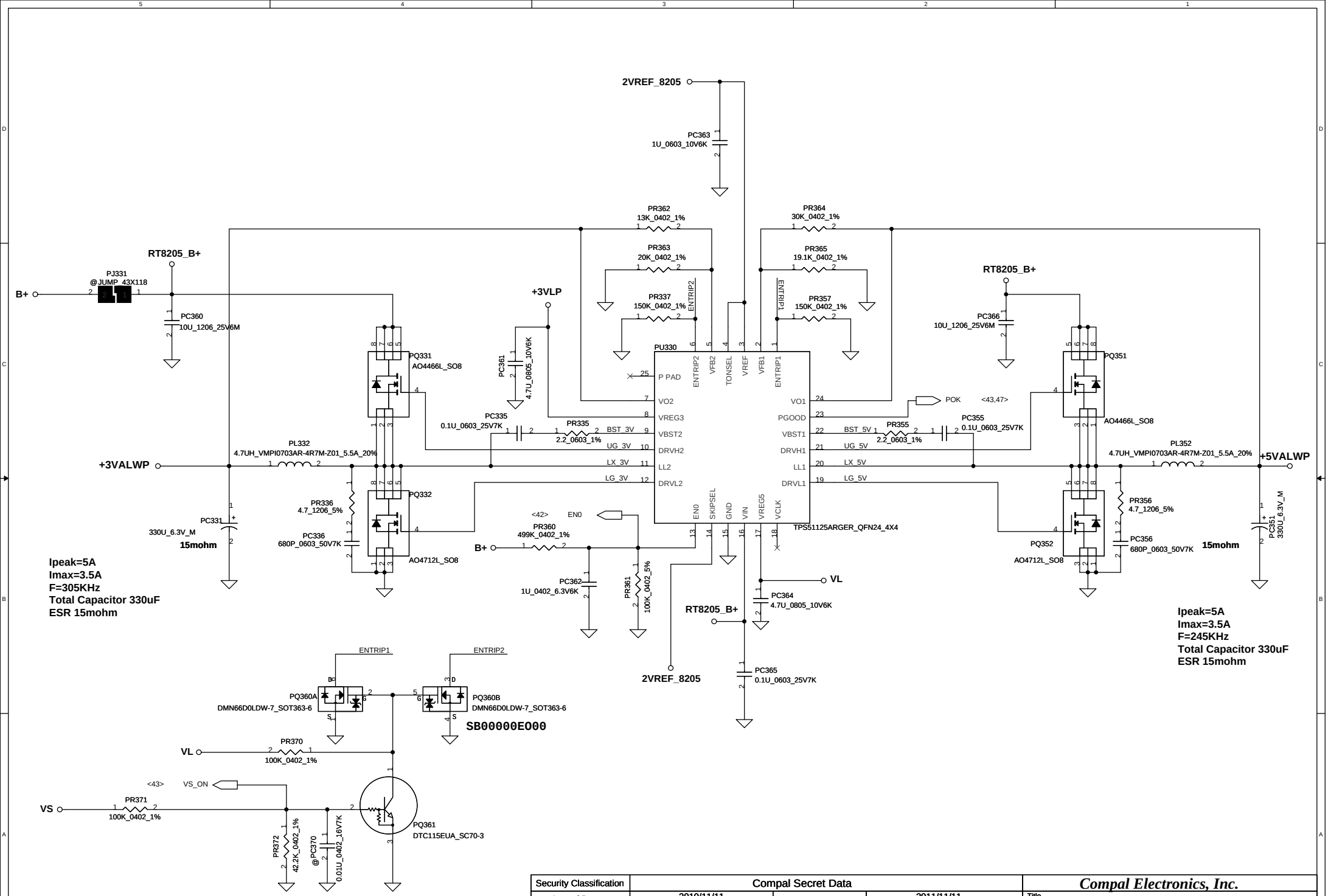

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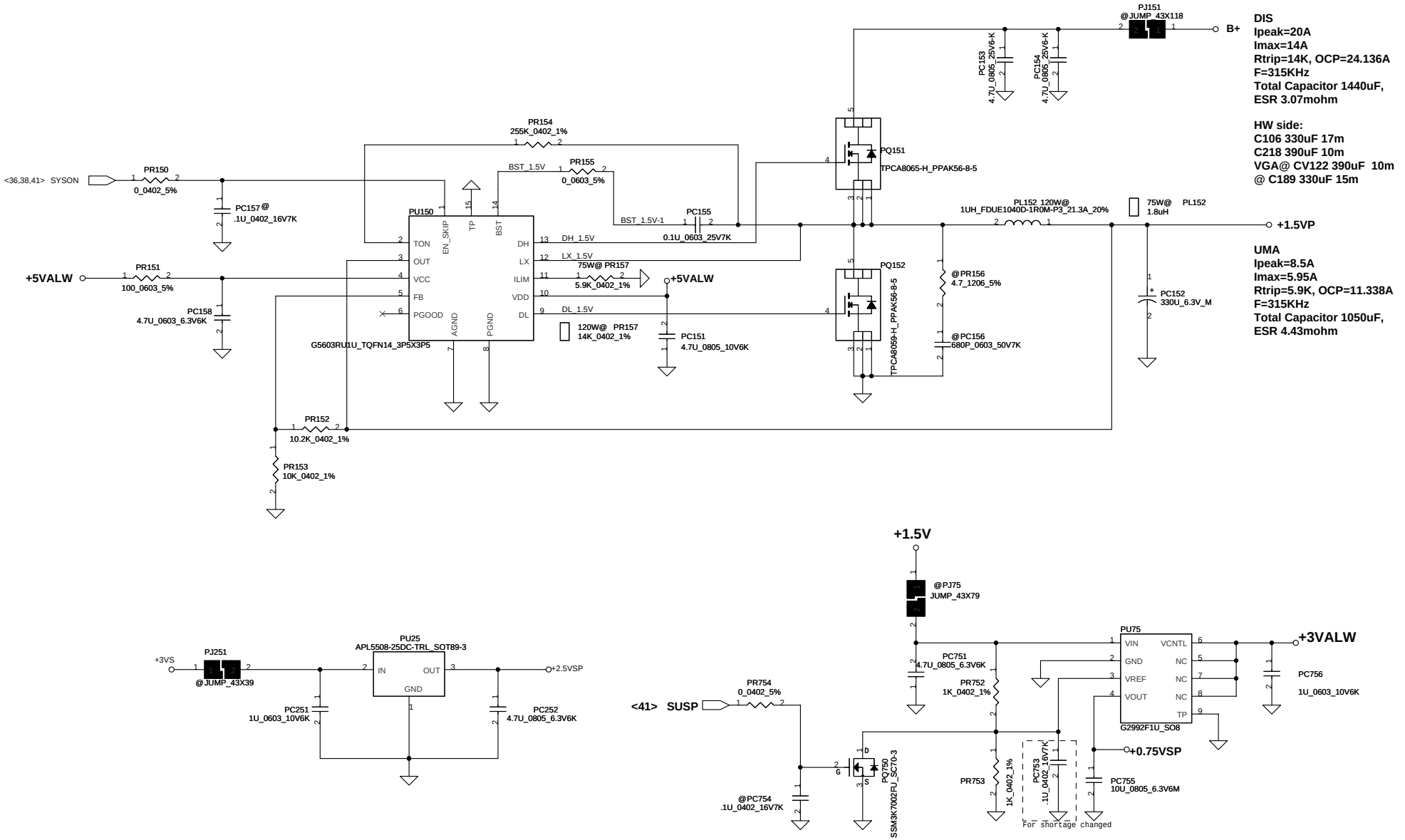

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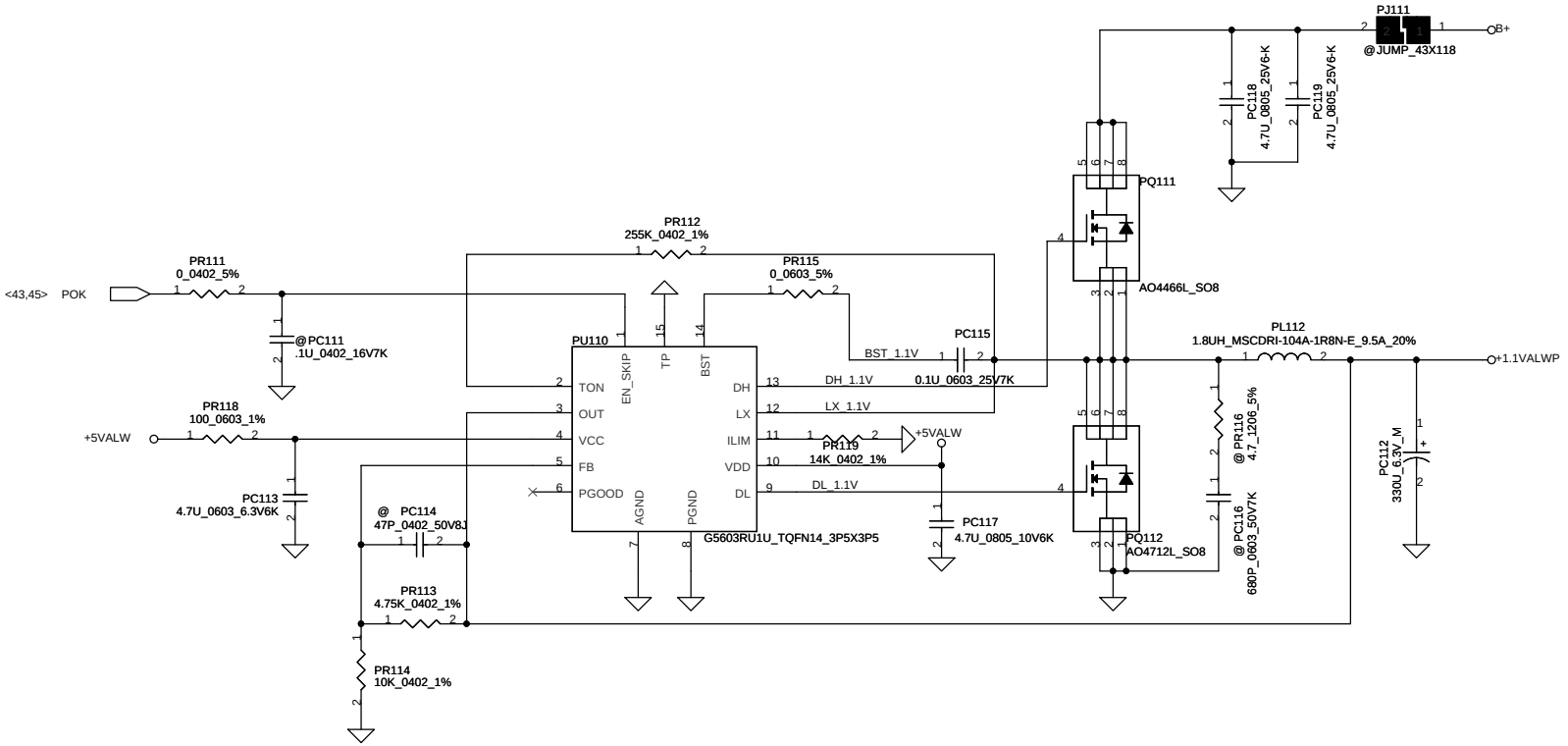
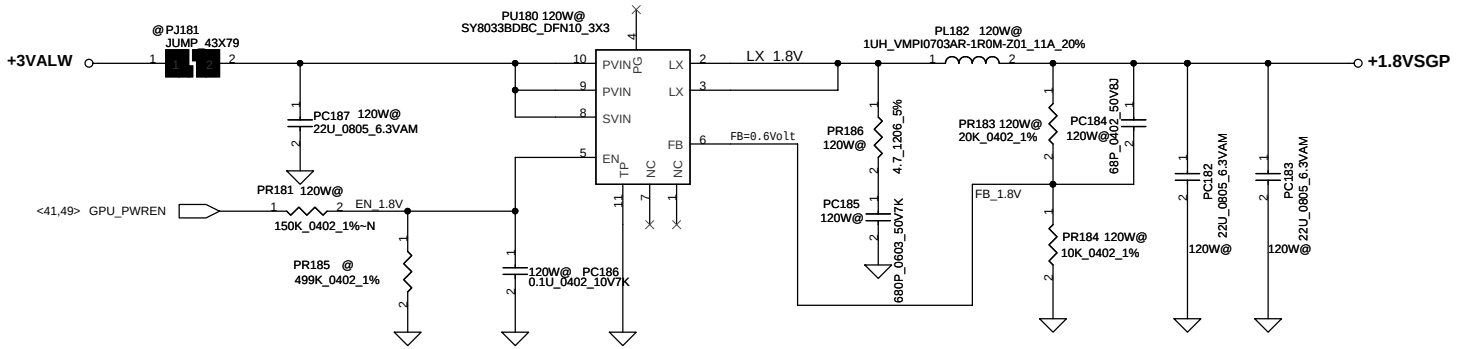


Ipeak=5.3A
Imax=3.71A
Rtrip=14K, OCP=6.814A
F=315KHz
Total Capacitor 330uF,
ESR 15mohm



Ipeak=2.5A
ILIM = 4A
F=1MHz
Total Capacitor 44uF,

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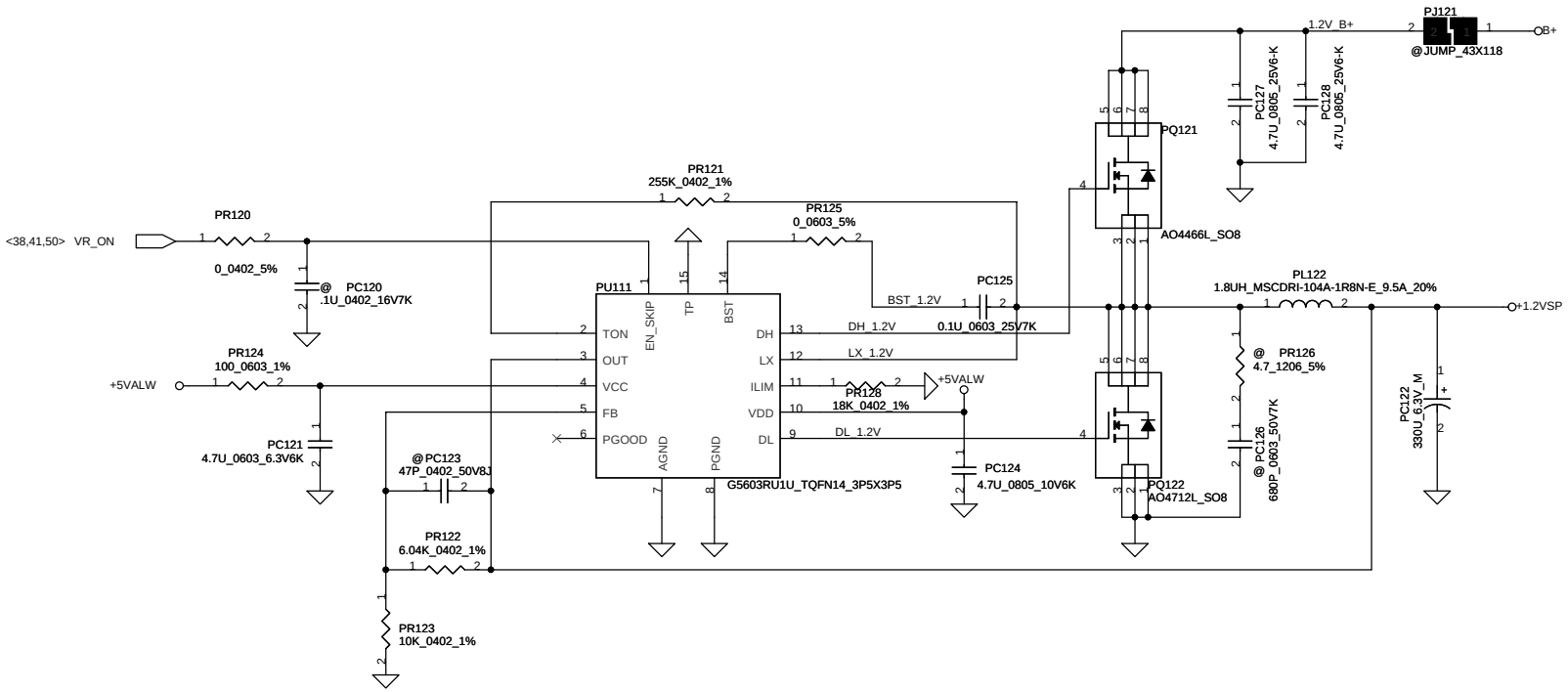

Ipeak=6.5A
Imax=4.55A
Rtrip=18K, OCP=8.553A
F=315KHz
Total Capacitor 660uF,
ESR 7.97mohm

HW side:
C130 330uF 17m

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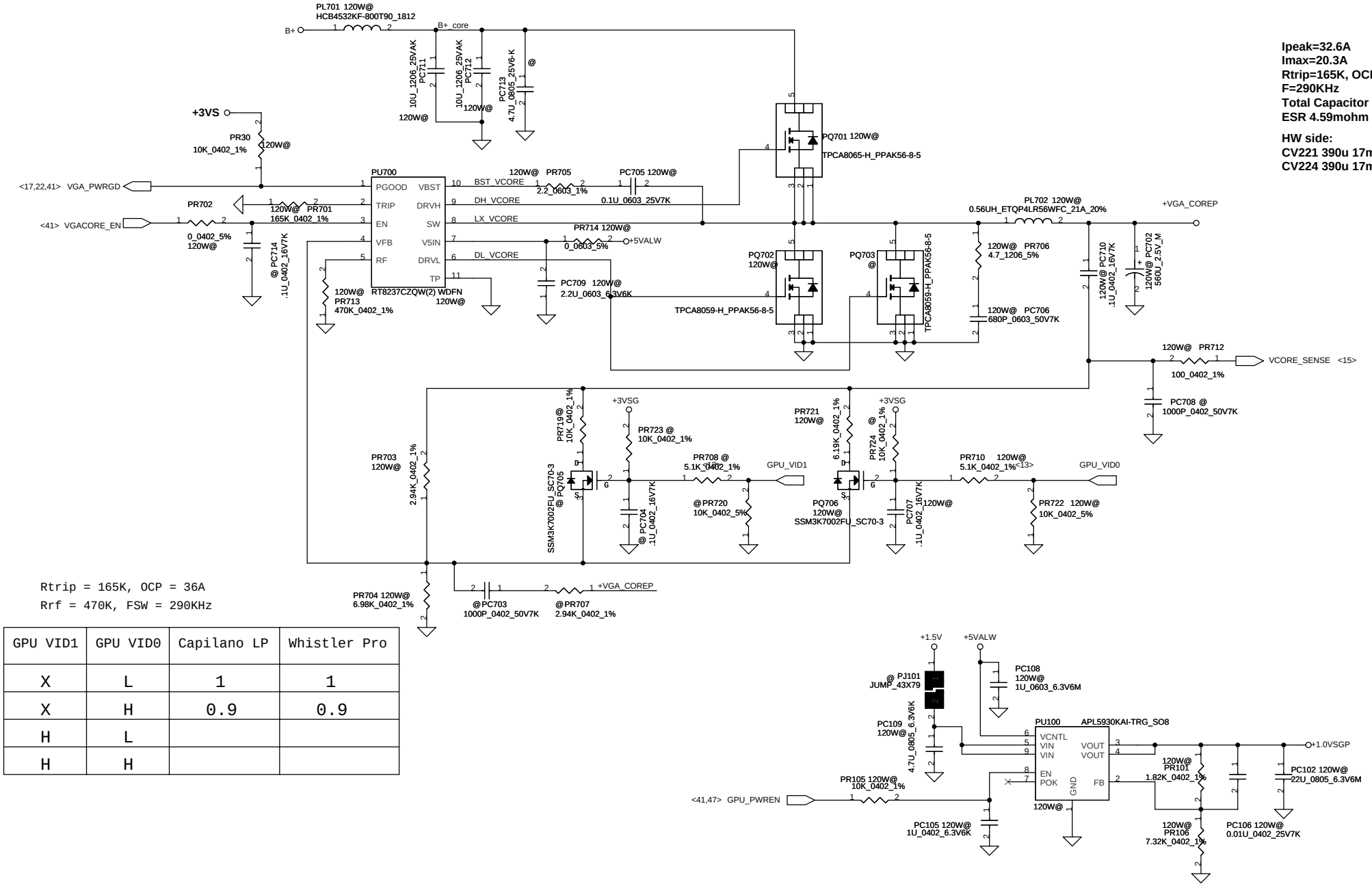

GPU VID1	GPU VID0	Capilano LP	Whistler Pro
X	L	1	1
X	H	0.9	0.9
H	L		
H	H		

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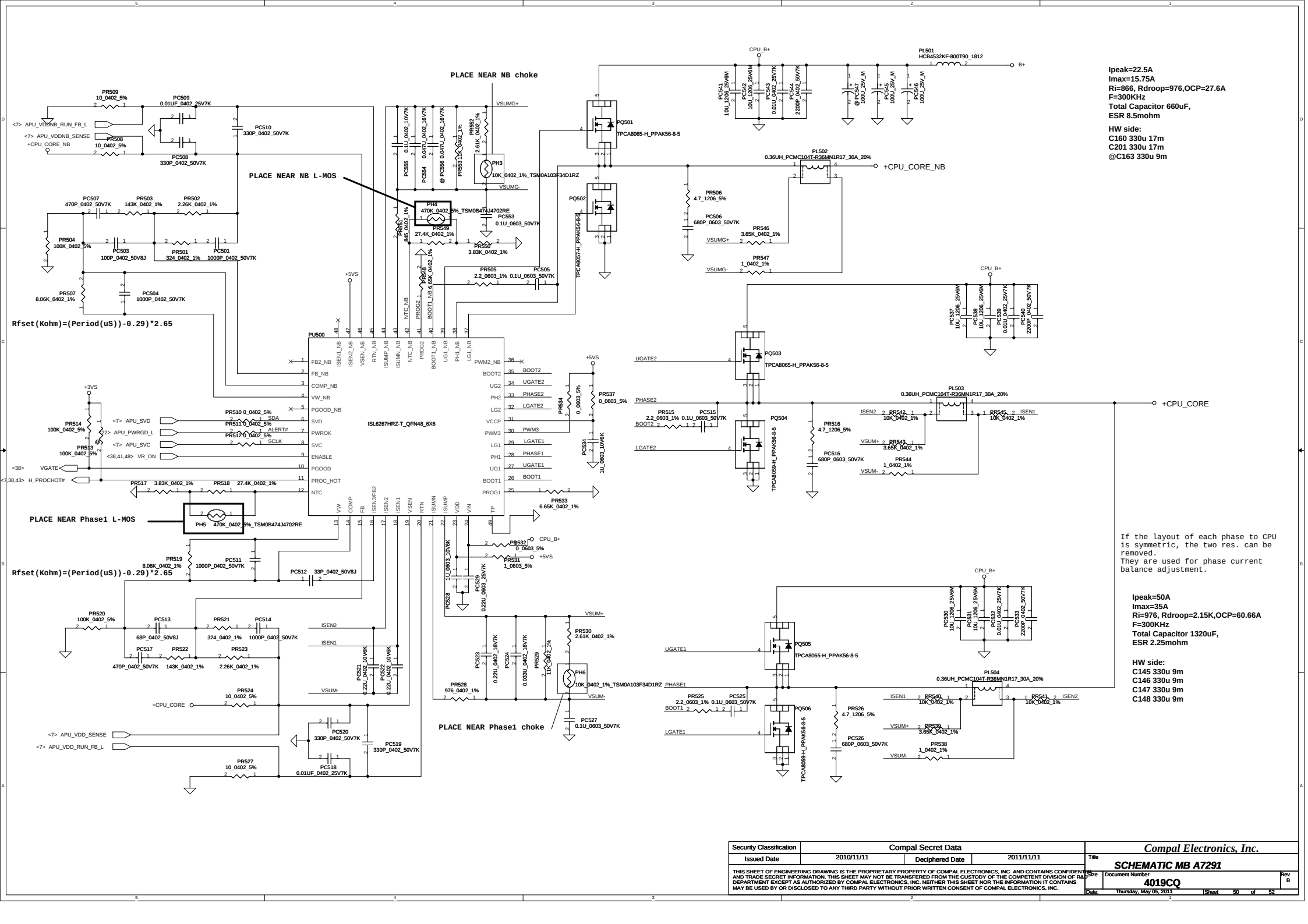

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2011/01/03	P47-PWR_+1.1VALWP/+1.8VSP	Add +1.8VSG components BOM structure to 120W@	Circuit modify
2.	2011/01/03	P49-PWR_VGA_COREP/+1.0VSP	Move PR720 and PR722 to PR708 and PR710 pin2 and change PR720 and PR722 resistor value to 10K ohm	Avoid voltage divide too small
3.	2011/01/03	P50-PWR_+CPU_CORE/+CPU_CORE_NB	PC501 to 1000pF, PC503 to 100pF, PC507 to 470pF PC508 to @, PC510 to @, PC512 to 33pF PC513 to 68pF, PC514 to 1000pF, PC517 to 470pF PC519 to @, PC520 to @, PC523 to 0.22uF	Tune the compensation value
4.	2011/02/14	P44-PWR-CHARGER	Change PQ203,PQ207,PQ208 to AO4407AL	Use Halogen Free PN
5.	2011/02/14	P44-PWR-CHARGER	Change PD202 to SCS00005I00	Use low VF diode for G5209S31U
6.	2011/02/14	P50-PWR_+CPU_CORE/+CPU_CORE_NB	Change PR529 to 11k,PR530 to 2.61k	Modify for CPU_CORE load line
7.	2011/02/14	P49-PWR_VGA_COREP/+1.0VSP	Change PR701 to 150k	Adjust VGA_CORE OCP to 38A
8.	2011/02/14	P49-PWR_VGA_COREP/+1.0VSP	Change PC702 to SF000004R00	For cost down
9.	2011/02/14	P48-PWR_+1.2VSP	Change PC122 to SF000002000	Use same PN
10.	2011/03/21	P44-PWR-CHARGER	Change PL202 to SH000009R00	Use molding type
11.	2011/03/21	P45-PWR_+3VALWP/+5VALWP	Change PL332,PL352 to SH00000KN00	Use molding type
12.	2011/03/21	P45-PWR_+3VALWP/+5VALWP	Change PR335,PR355 to 2.2 Ohm and Add PR336,PR356 4.7 Ohm, add PC336,PC356 680pF	Add boost and snubber for EMI request
13.	2011/03/21	P46-PWR_+1.5VP/+0.75VSP	Change PL152 to SH00000IP00	Use molding type
14.	2011/03/21	P46-PWR_+1.5VP/+0.75VSP	Change PR157 to 5.9k(UMA),14k(DIS)	Adjust OCP value
15.	2011/03/21	P46-PWR_+1.5VP/+0.75VSP	Remove PC574 0.1u	Prevent SUSP sequence delay
16.	2011/03/21	P47-PWR_+1.1VALWP/+1.8VSP	Change PL112 to SH00000IP00	Use molding type
17.	2011/03/21	P47-PWR_+1.1VALWP/+1.8VSP	Change PR119 to 14k	Adjust OCP value
18.	2011/03/21	P47-PWR_+1.1VALWP/+1.8VSP	Add PC186 0.1u,change PR181 to 150k	For 1.8VSG sequence
19.	2011/03/21	P48-PWR_+1.2VSP	Change PL122 to SH00000IP00	Use molding type
20.	2011/03/21	P48-PWR_+1.2VSP	Change PR128 to 18k	Adjust OCP value
21.	2011/03/21	P48-PWR_+1.2VSP	Change PR105 to 10k, PC105 to 1u	For 1.0VSG sequence
22.	2011/03/21	P50-PWR_+CPU_CORE/+CPU_CORE_NB	Change PR505,PR515,PR525 to 2.2 Ohm Add PR506,PR516,PR526 4.7 Ohm Add PC506,PC516,PC526 680pF	Add boost and snubber for EMI request Add PR506,PR516,PR526 4.7 Ohm
23.	2011/03/21	P50-PWR_+CPU_CORE/+CPU_CORE_NB	Change PC509,PC518 to 0.01u,add PR504,PR520 100k Add PC508,PC510,PC519,PC520 330pF change PC524 to 0.033u, change PH3,PH6 to 1% tol	For CPU and NB CORE load line
24.	2011/03/21	P43-PWR_BATTERY CONN / OTP	Change PR22 to 180 Ohm,PR28 to 1.18k for UMA Change PR22 to 4.02k Ohm,PR28 to 12.1k for DISA	For adapter protection
25.	2011/03/21	P44-PWR-CHARGER	Change PQ207 to AO 4435	Cost down
26.	2011/03/21	P44-PWR-CHARGER	Change PR222 to 75k	Use 65W adapter for UMA SKU
27.	2011/03/21	P49-PWR_VGA_COREP/+1.0VSP	Change PR701 to 165k	Adjust OCP value
28.	2011/03/21	P49-PWR_VGA_COREP/+1.0VSP	Change PR705 to 2.2 Ohm Add PR706 4.7 Ohm,PC706 680pF	Add boost and snubber for EMI request
29.	2011/03/21	P44-PWR-CHARGER	Change PR236 to 200k,PR237 to 47k	For wrong adapter issue
30.	2011/03/23	P46-PWR_+1.5VP/+0.75VSP	Change PR152 to 10.2k	HW request to adjust 1.5V to 1.515V
31.	2011/03/23	P44-PWR-CHARGER	Change PR222 to 53.6k,PR223 to 20k Remove PQ208	Use 90W adapter for DIS SKU

Security Classification	Compal Secret Data		
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HW PIR (Product Improve Record)

PEQAE LA-7291P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2011/02/14

Item	Date	Page	Solution	Request
1.	1/20	P29	Change Q205 BOM structure to always stuff	For CRT function
2.	1/20	P24	Add R454 and R455	For CRT function
3.	1/20	P11	Change SODIMM1 SMbus address to A2(SA0=1, SA1=0)	For CRB common design
4.	1/21	P34	Change Giga LAN to RTL8111E-VL (SA00004LR00)	For cost down
5.	1/26	P36	Remove USB3.0 co-layout resistors with Renesas	For USB3.0 signal quality
6.	1/26	P29	Change Q205 power to +3VS	For CRT function
7.	1/31	P27	Change LVDS translator from RTD2132 to ANX3110	For customer request
8.	2/9	P7	Change TEST35 to pull-high	For HDMI issue
9.	2/9	P23	Change ACIN_FCH to low-active	For ACIN LED issue under DC mode
10.	2/10	P35	Change MDIO5 clock trace routing	For SDHC issue
11.	2/10	P7	Add DMA_ACTIVE# pull-up to +1.5V	For leakage issue
12.	2/10	P7	Add SVC/SVD pull-up to +1.5V	For leakage issue
13.	2/10	P26	Add isolation between +1.1VS_CKVDD and +1.1VS	For leakage issue
14.	2/17	P23	Change R284, R290 and R291 to @	FCH has internal pull-up
15.	2/17	P35	Change RC18 to @	JMB389 has internal pull-up

REVISION CHANGE: 0.2 TO 0.3
GERBER-OUT DATE: 2011/03/18

Item	Date	Page	Solution	Request
1.	3/10	P23	Remove level-shifter for ODD_PLUGIN#	ODD has internal 1K pull-down
2.	3/10	P35	Add level-shifter for CR_CPPE#	For leakage issue
3.	3/10	P40	Add L63 and L64	For EMI request
4.	3/11	P23	Change HDMI_HPD to GEVENT10#	GEVENT9# internal pull-up can't be disabled
5.	3/15	P38	Add co-layout resistors for KB9012 and KB930	For cost down
6.	3/15	P24	Change LOGO_LED to GPIO176 and WL_BT_LED to GPIO177	For LED flash issue after power-on
7.	3/17	P22	Change JCOMS to JCMOS	For naming rule
8.	3/17	P23	Add T31,T35,T57 and R313	For debug
9.	3/17	P35	Change RC17 to 0 ohm	For SDXC performance low issue
10.	3/18	P23	Add USB_OC3# and R489	For left-USB2.0 wake-up issue
11.	3/18	P31	Add USB power switch U17	For left-USB2.0 wake-up issue
12.	3/21	P26	Remove Q56 and stuff R371	For M3 A13 version
13.	3/23	P10&P11	Add C157,C161,C183 and C187	For DDR VREF ripple issue

REVISION CHANGE: 0.3 TO 1.0
GERBER-OUT DATE: 2011/04/20

Item	Date	Page	Solution	Request
1.	4/13	P8	Change C160 and C201 to 390U/10mohm	For dynamic +CPU_CORE_NB fail
2.	4/14	P38	Add BACO_EN# to EC	For GPU thermal sensor initial
3.	4/14	P22	Change R257 to 10K	For PXS_PWREN leakage issue
4.	4/19	P22	Change C248 and C249 to 18P	For RTC issue

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