EA30_BM
Schematics Document

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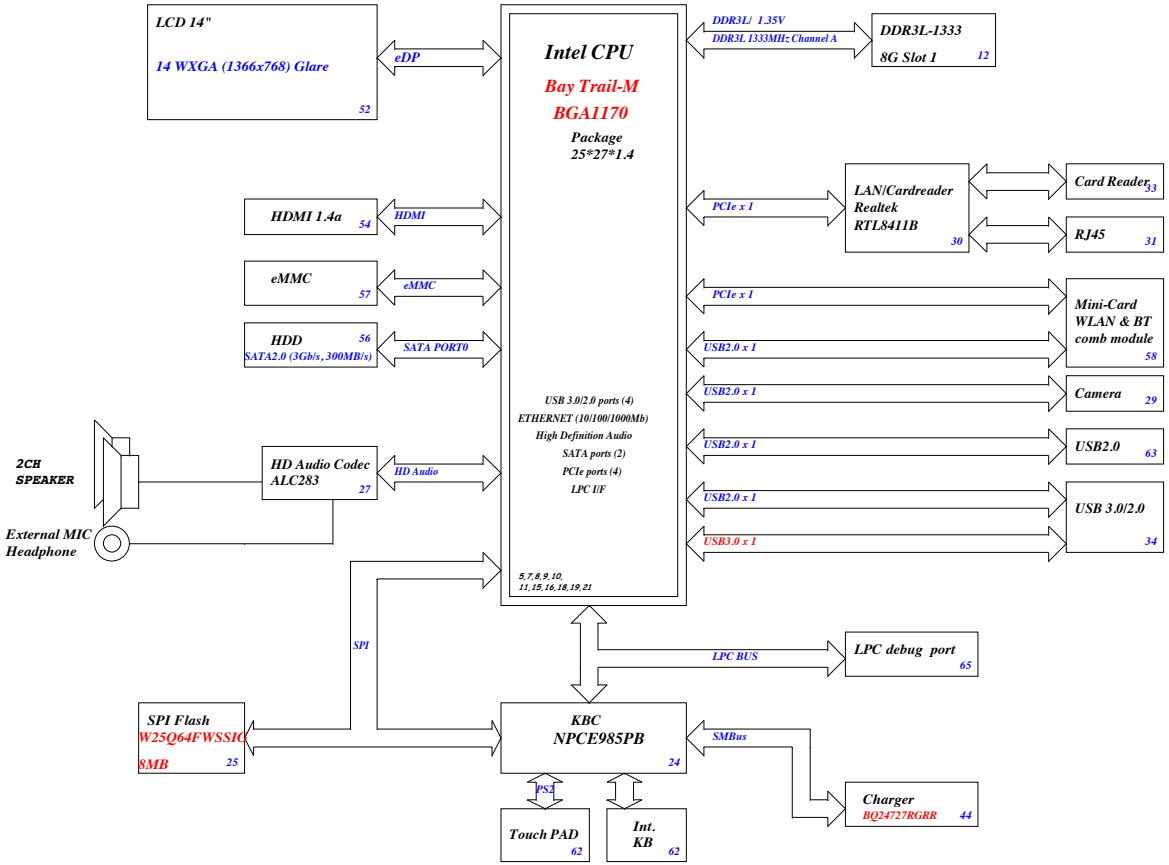
Title	Cover Page	
Size A3	Document Number EA30_BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 1 of 102	

EA30_BM Board Block Diagram

Project code :
PCB P/N : 14221
Revision : SB



CHARGER BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC ISL95833	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SY8208	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

SYSTEM DC/DC SY8208DQNC	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM LDO TLV70218	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM LDO S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

SYSTEM LDO TLV70012	51
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5

Step Down Regulator SYW232	51
INPUTS	OUTPUTS
1D0V_S0_PG	1D05V_S0

GPU Core RT8812	82
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

LOAD SWITCH TPS22966	37
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0

LOAD SWITCH TPS22965	37
INPUTS	OUTPUTS
1D0V_S5	1D0V_S0

SYSTEM DC/DC SY8208	83
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

LOAD SWITCH TPS22966	83
INPUTS	OUTPUTS
1D05V_S0	1D5V_VGA_S1
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title: Block Diagram

Size	Document Number	Rev
Custom	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 2 of 102

5 4 3 2 1

D

C

B

A

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Title

(Reserved)

Size	Document Number	Rev
A4	**EA30 BM**	**-1**

Date: Tuesday, July 08, 2014 Sheet 3 of 102

SSID = CPU

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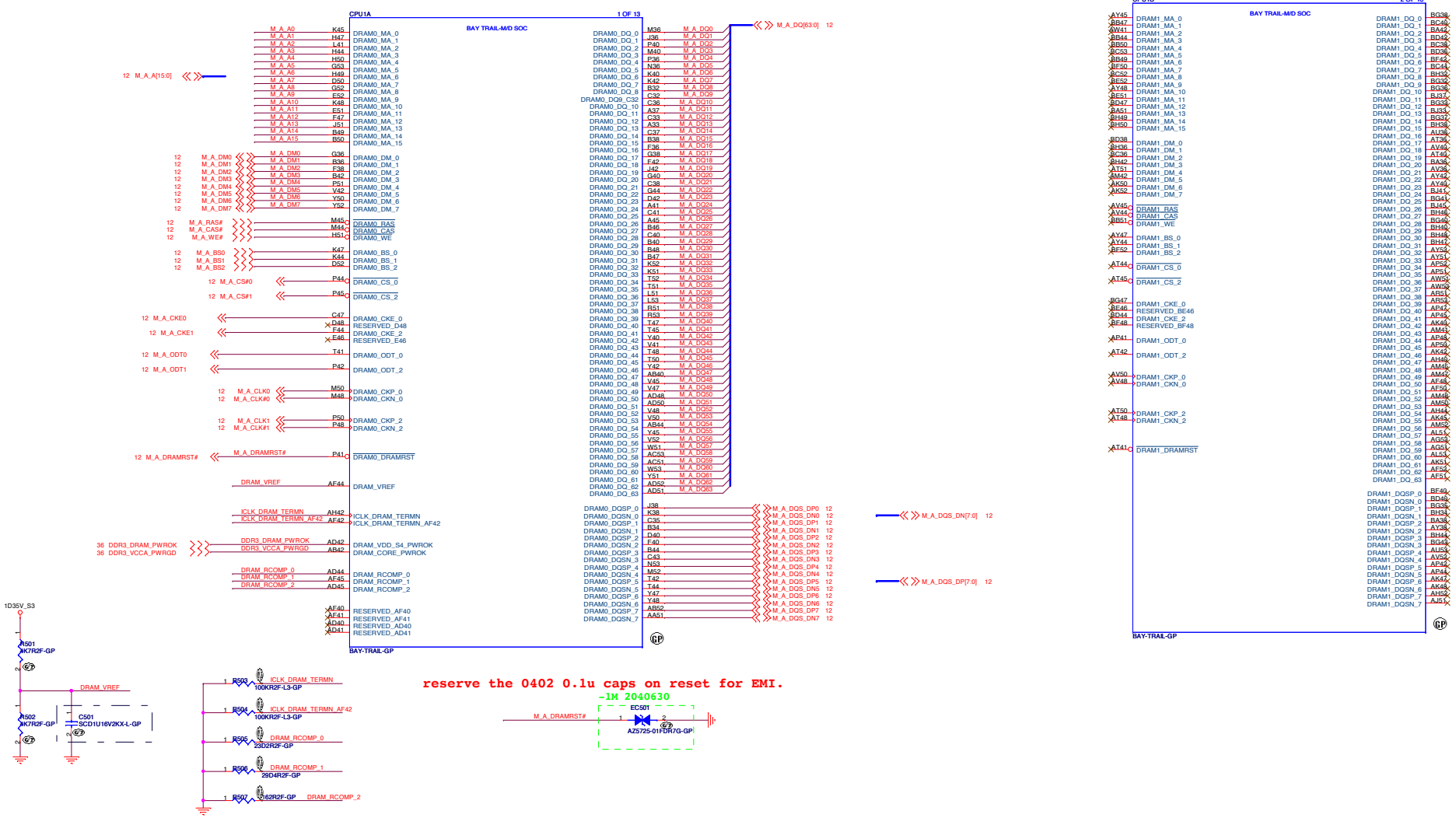
Title	CPU (Reserved)	
Size A4	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 4 of 102	

SSID = CPU



reserve the 0402 0.1u caps on reset for EMI.

-1M 2040630

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Title: CPU (DDR)

Size	Document Number	Rev
A2	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 5 of 102

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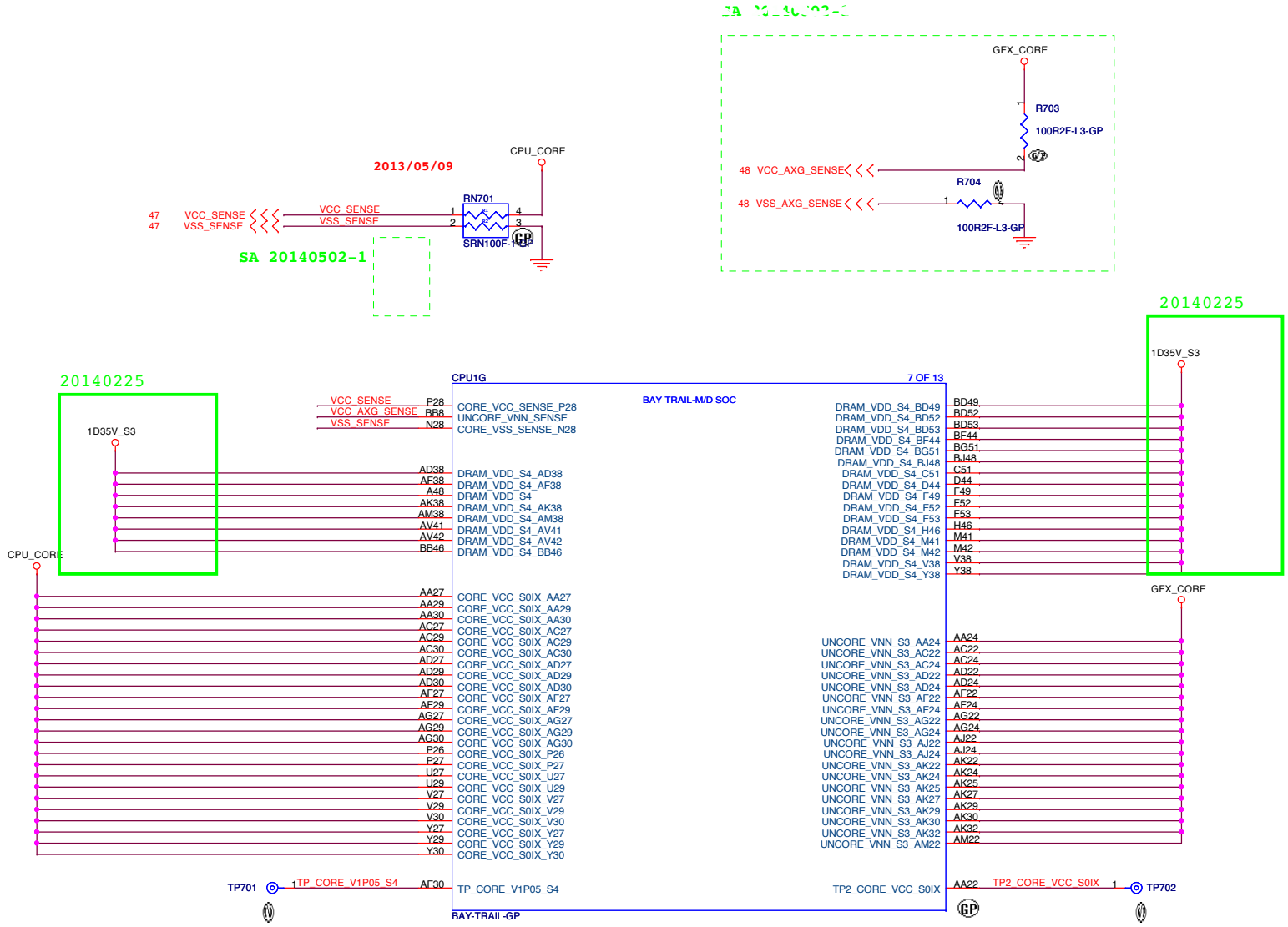
Title	CPU (CFG)	
Size A4	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 6 of 102	

SSID = CPU



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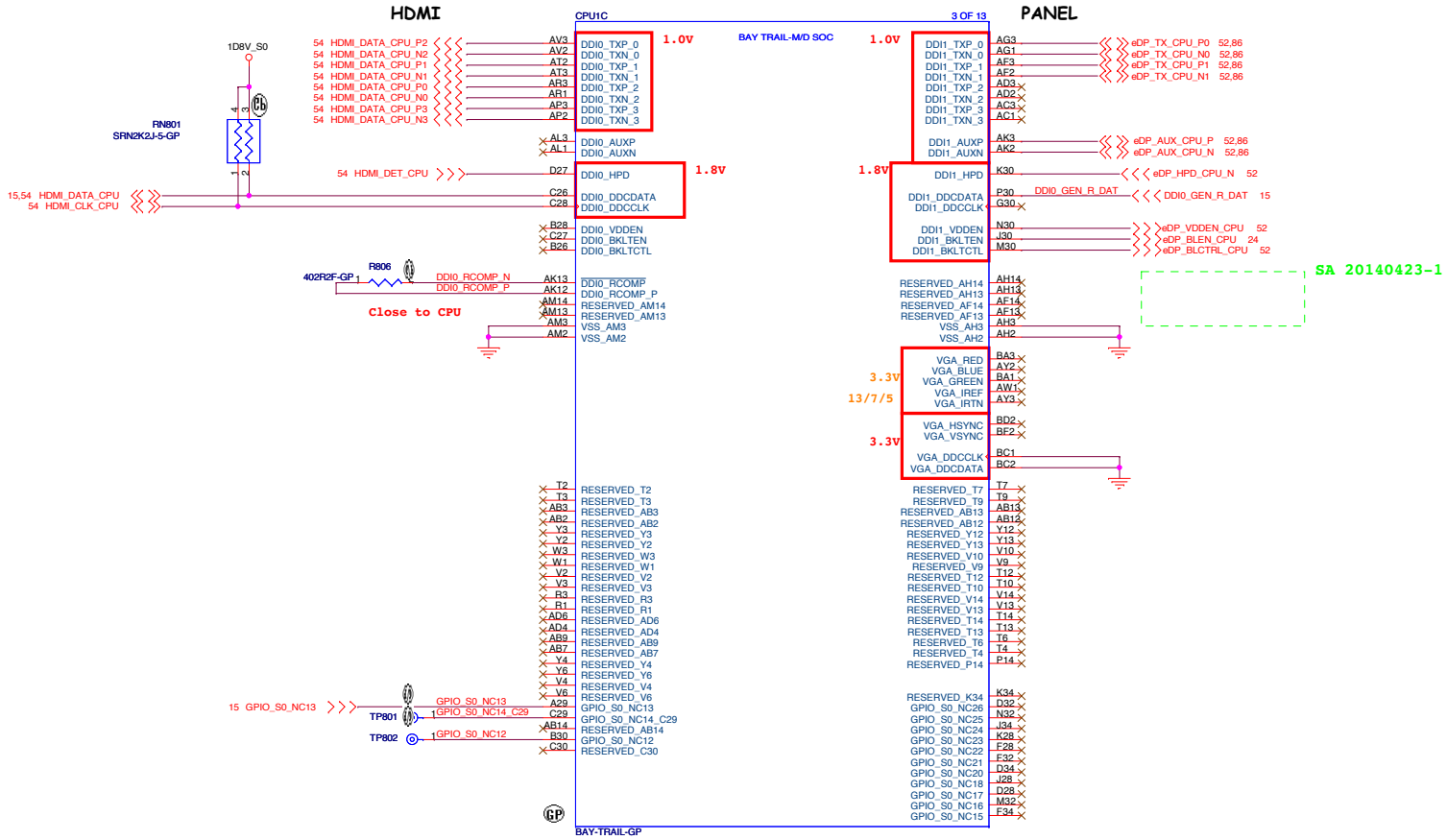
Title: CPU (VCC_CORE)

Size: A3 | Document Number: EA30_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 7 of 102

SSID = CPU



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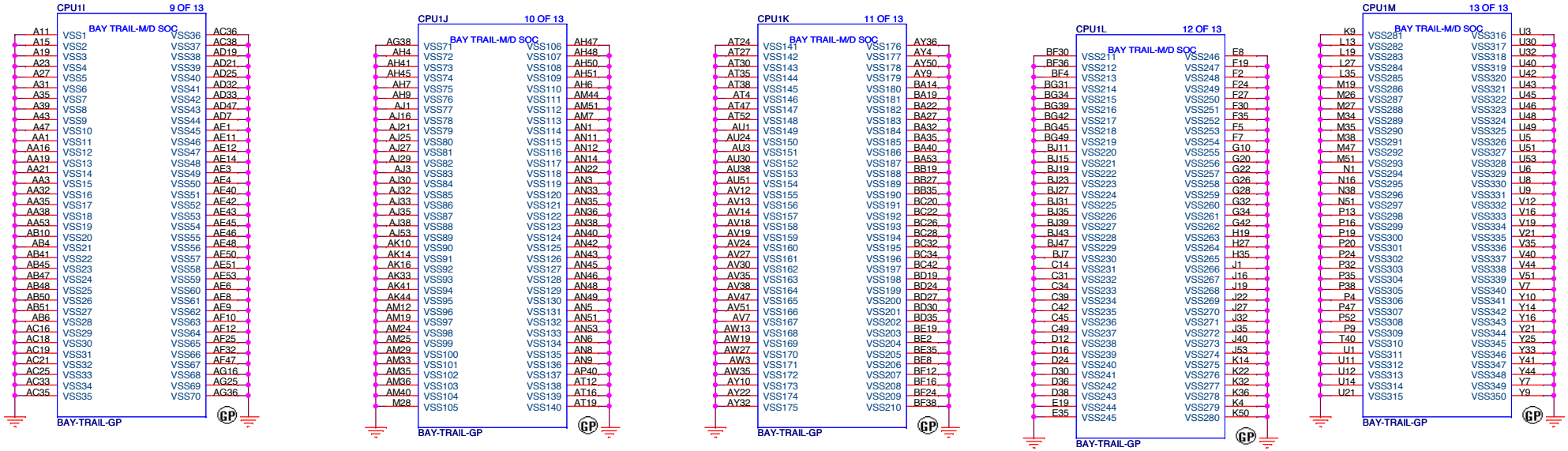
Title: CPU (DDI/EDP/GPIO)

Size	Document Number	Rev
Custom	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 8 of 102

SSID = CPU



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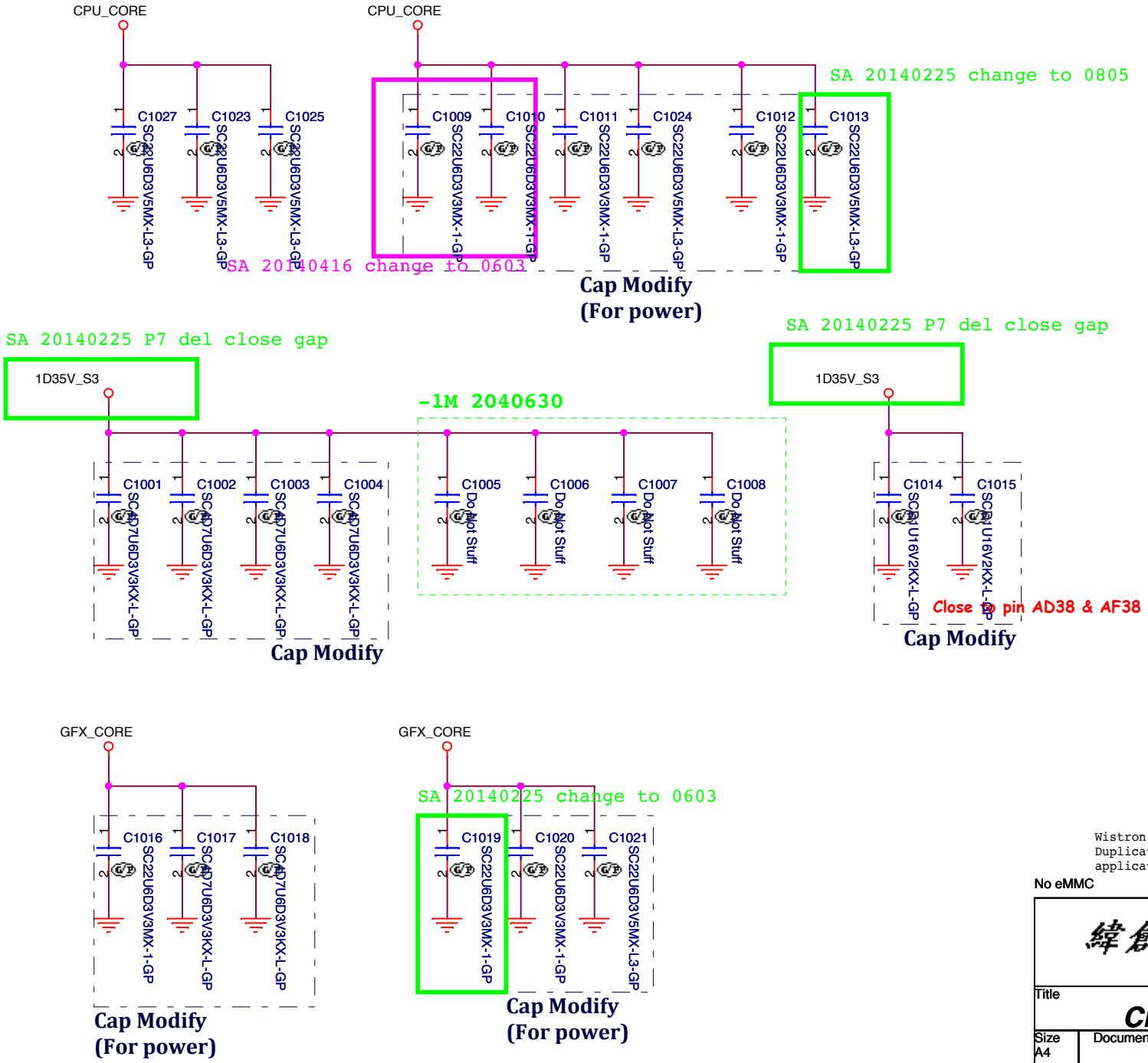
Title: **CPU (VSS)**

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 9 of 102



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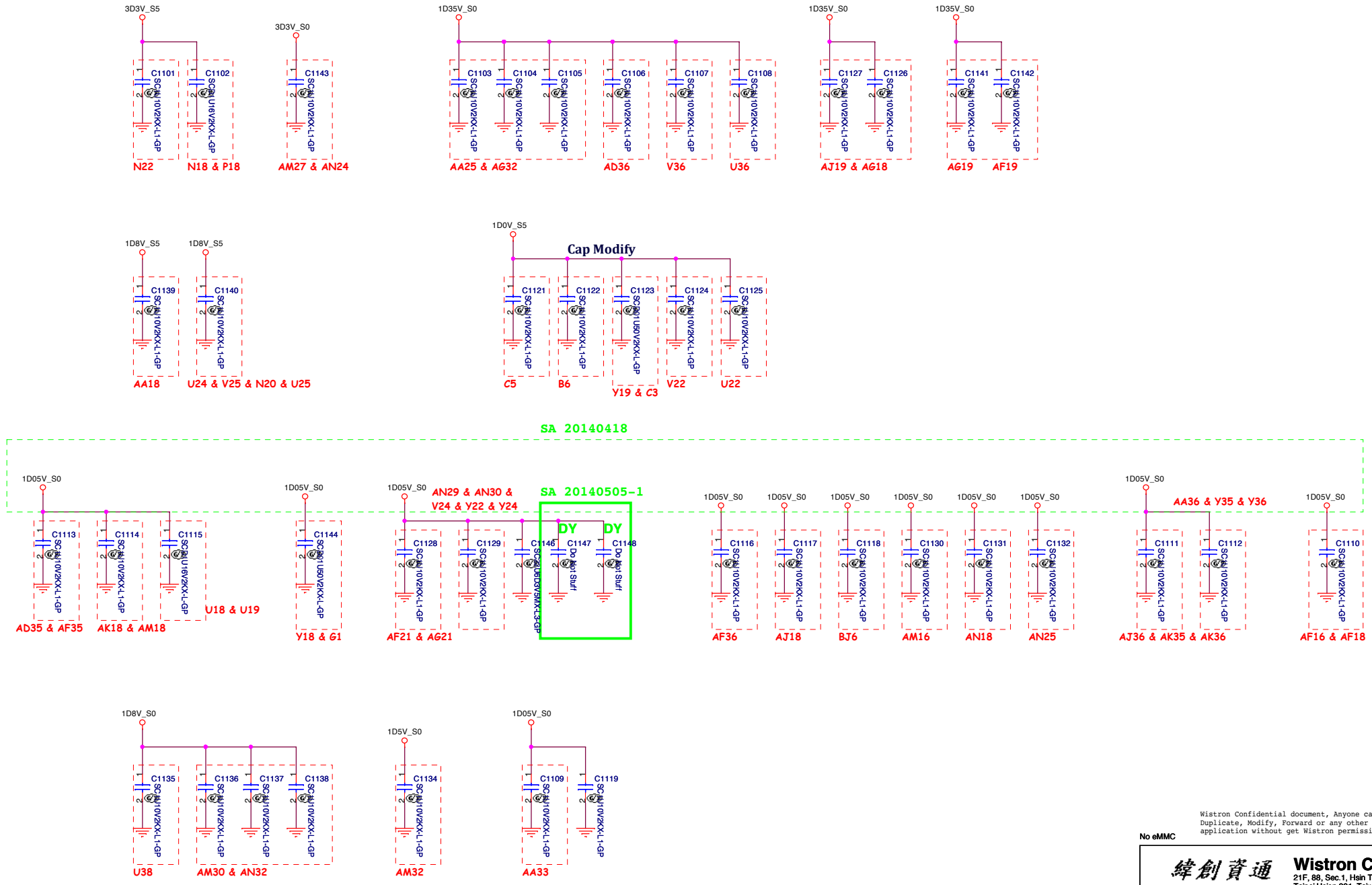
Title: CPU (Power CAP1)

Size: A4 | Document Number: EA30 BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 10 of 102

Cap Modify



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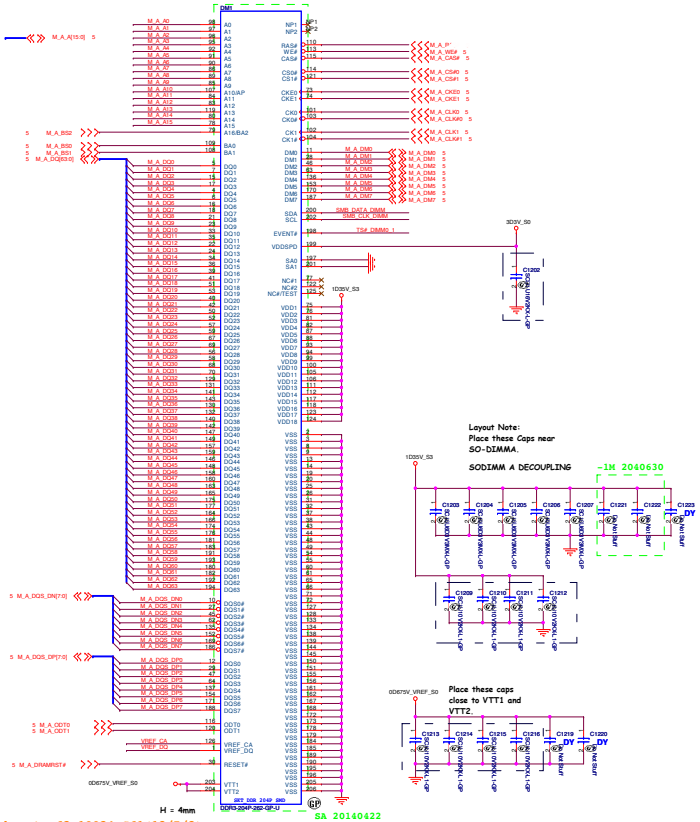
Title: CPU (Power CAP2)

Size: A3 | Document Number: EA30_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 11 of 102

SSID = MEMORY



Layout Note:
Place these Caps near
SO-DIMMA.

SODIMM A DECOUPLING

-1M 2040630

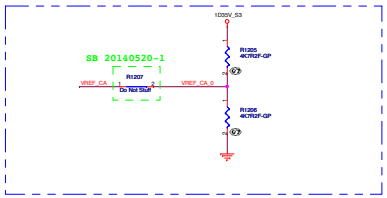
Place these caps
close to VTT1 and
VTT2.

SA 20140422

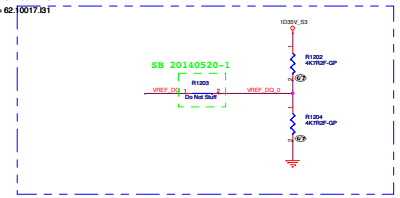
DM1 change part number to 62.10024.S61(13/7/3)

1st = 62.10024.S21
2nd = 62.10024.O61
3rd = 62.10024.M31
4th = 62.10017.I31

For Intel Recommend Close to DIMM(Bay Trail)



For Intel Recommend Close to DIMM(Bay Trail)

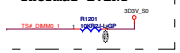


Note:
If S[illegible] SA[illegible] Addr[illegible] is [illegible]
SO-DIMM[illegible] S Addr[illegible] is 0x30

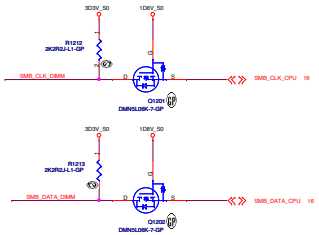
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

0726_SA

Thermal EVENT



Level shift



VGS(th) = 1V

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Title: DDR3-SODIMM1

Size	Document Number	Rev
A1	EA30_BM	-1

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SSID = MEMORY

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Title: DDR3-SODIMM2

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A2	EA30_BM	-1

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Title	***Reserved***	
Size A4	Document Number **EA30_BM**	Rev **-1**
Date: Tuesday, July 08, 2014	Sheet 14 of 102	

SSID = STRAP

STRAP RESISTORS SHOULD BE F CLO OC
SHOULD BE PLACED OUTSIDE KOZ AREA

SA 20140222

Description	BIOS Boot Selection	Security Flash Descriptors	DDI1 Detect	DDI0 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI1_DDCDATA	DDI0_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic	1D8V_S0 R1509 10KR2F-L1-GP LPE_I2S2_FRM 19 R1510 DY Do Not Stuff	1D8V_S0 R1511 10KR2F-L1-GP LPE_I2S2_DATAOUT 19,24 R1512 DY Do Not Stuff 公版S0，GPIO table要求S5的電？	1D8V_S0 R1506 DY Do Not Stuff HDMI_DATA_CPU 8,54 R1508 DY Do Not Stuff	2013/04/11 1D8V_S0 R1502 2K2R2J-L1-GP DDI0_GEN_R_DAT 8 R1504 DY Do Not Stuff	1D8V_S0 R1501 DY Do Not Stuff GPIO_S0_NC13 8 R1503 10KR2F-L1-GP	1D8V_S0 R1505 DY Do Not Stuff GPIO_S0_SC_56 16 R1507 DY Do Not Stuff
High	SPI	Normal Operation	RN801 PH DDI1 detected	DDI0 detected	DDI1 detected	
Low	LPC	Override	DDI1 not detected	DDI0 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Defaul t	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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Title: CPU(STRAP)

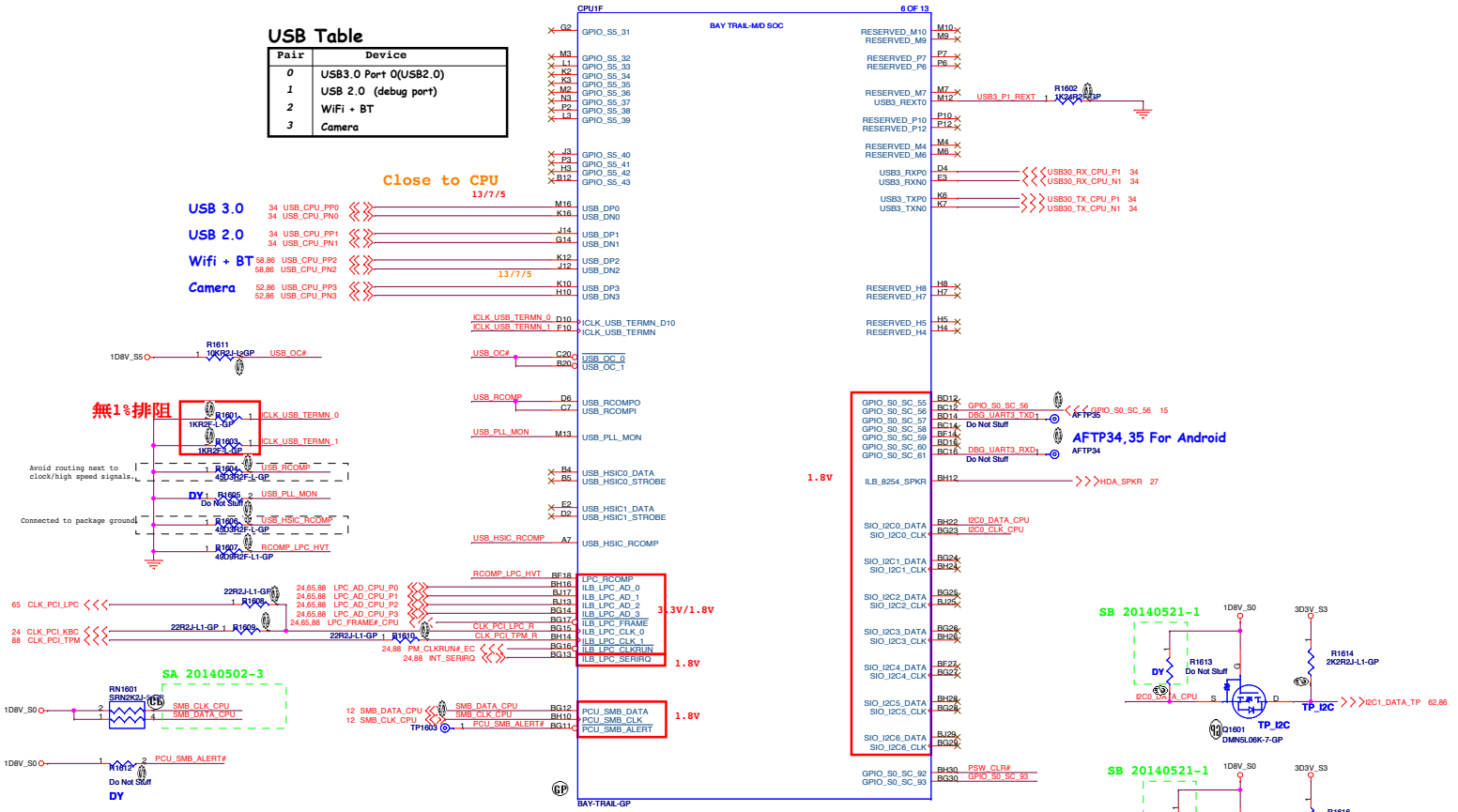
Size: A3 | Document Number: EA30_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 15 of 102

SSID = PCH

USB Table

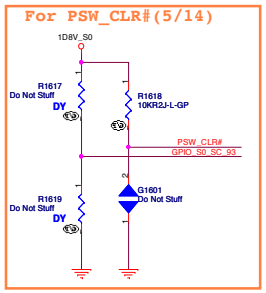
Pair	Device
0	USB3.0 Port 0(USB2.0)
1	USB 2.0 (debug port)
2	WiFi + BT
3	Camera



USB Port Routing Guide for Bay Trail-M

WO/ Lighting Bolt(Can support 3 USB I/O Ports)

USB2/3	Camera	Touch	USB Hub
			↓
		USB2	USB2	BT



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Title: CPU (USB/LPC/GPIO)

Size: A2 | Document Number: EA30_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 16 of 102

SSID = PCH

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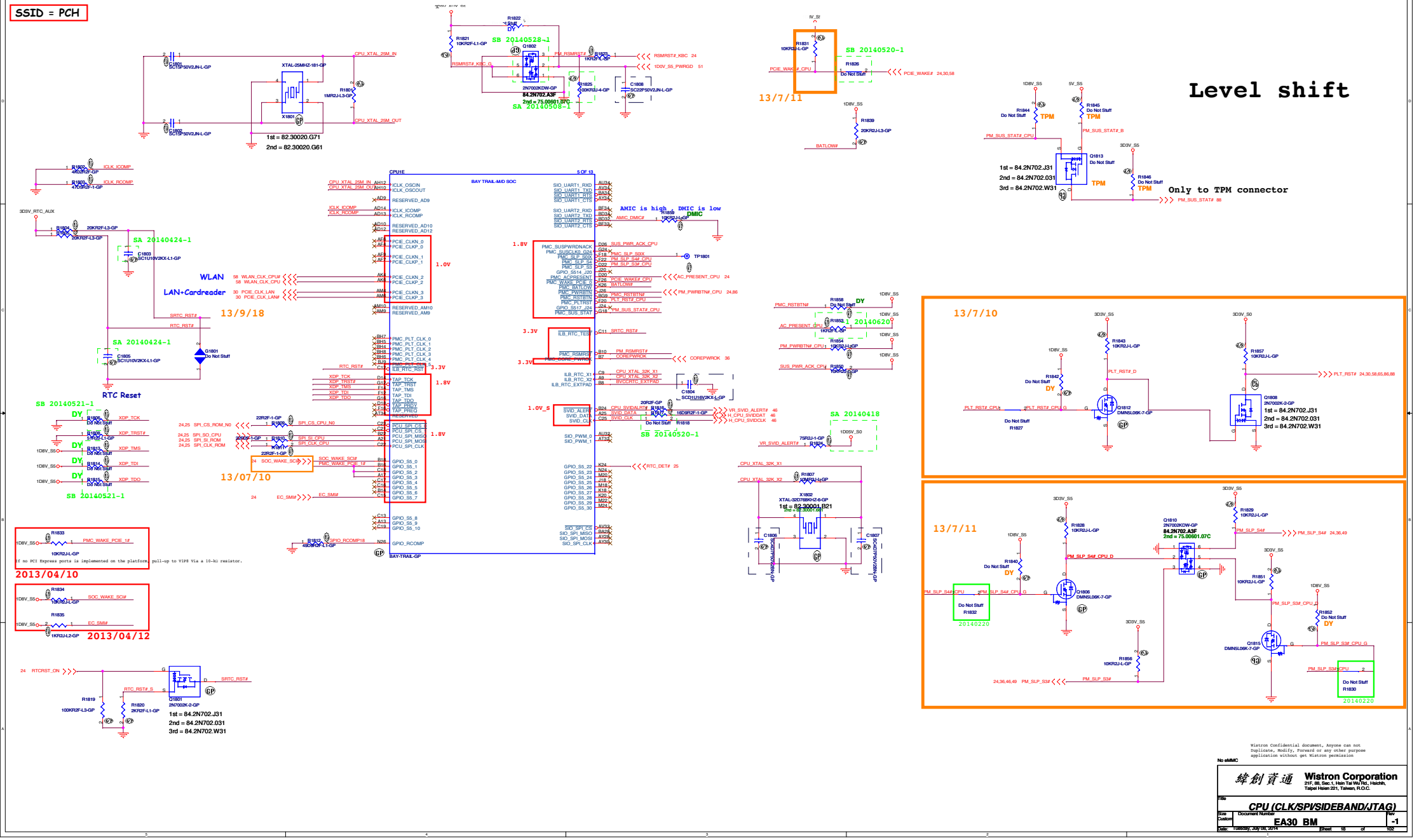
Title: CPU (DMI/FDI/PM)

Size	Document Number	Rev
A4	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 17 of 102

SSID = PCH

Level shift



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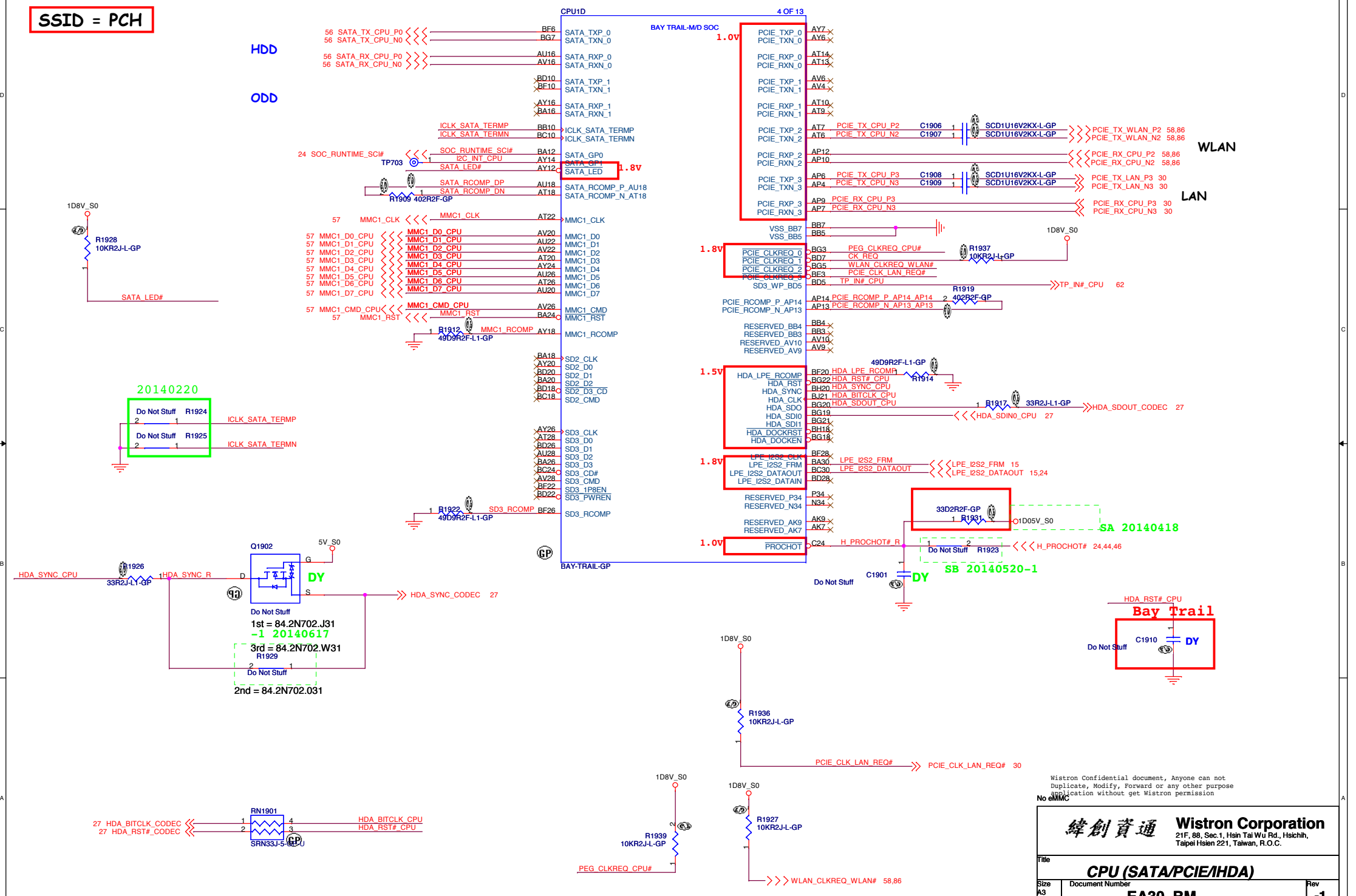
Title: CPU (CLK/SPI/SIDEBAND/JTAG)

Size: Custom | Document Number: EA30 BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 18 of 102


SSID = PCH
CPU1D
4 OF 13
BAY TRAIL-M/D SOC
BAY-TRAIL-GP
HDD
ODD
WLAN
LAN
1.0V
1.8V
1.5V
SATA_TXP_0
SATA_TXN_0
SATA_RXP_0
SATA_RXN_0
SATA_TXP_1
SATA_TXN_1
SATA_RXP_1
SATA_RXN_1
ICLK_SATA_TERMP
ICLK_SATA_TERMN
SATA_GP0
SATA_GP1
SATA_LED
SATA_RCOMP_P_AU18
SATA_RCOMP_N_AT18
MMC1_CLK
MMC1_D0
MMC1_D1
MMC1_D2
MMC1_D3
MMC1_D4
MMC1_D5
MMC1_D6
MMC1_D7
MMC1_CMD
MMC1_RST
MMC1_RCOMP
SD2_CLK
SD2_D0
SD2_D1
SD2_D2
SD2_D3_CD
SD2_CMD
SD3_CLK
SD3_D0
SD3_D1
SD3_D2
SD3_D3
SD3_CD#
SD3_CMD
SD3_1P8EN
SD3_PWREN
SD3_RCOMP
PCIE_TXP_0
PCIE_TXN_0
PCIE_RXP_0
PCIE_RXN_0
PCIE_TXP_1
PCIE_TXN_1
PCIE_RXP_1
PCIE_RXN_1
PCIE_TXP_2
PCIE_TXN_2
PCIE_RXP_2
PCIE_RXN_2
PCIE_TXP_3
PCIE_TXN_3
PCIE_RXP_3
PCIE_RXN_3
PCIE_CLKREQ_0
PCIE_CLKREQ_1
PCIE_CLKREQ_2
PCIE_CLKREQ_3
PCIE_RCOMP_P_AP14
PCIE_RCOMP_N_AP13
HDA_LPE_RCOMP
HDA_RST
HDA_SYNC
HDA_CLK
HDA_SDO
HDA_SDI0
HDA_SDI1
HDA_DOCKRST
HDA_DOCKEN
LPE_I2S2_CLK
LPE_I2S2_FRM
LPE_I2S2_DATAOUT
LPE_I2S2_DATAIN
PROCHOT
20140220
Do Not Stuff R1924
Do Not Stuff R1925
ICLK_SATA_TERMP
ICLK_SATA_TERMN
Q1902
5V_S0
HDA_SYNC_CPU
HDA_SYNC_R
R1926
33R2J-L1-GP
DY
HDA_SYNC_CODEC 27
Do Not Stuff
1st = 84.2N702.J31
-1 20140617
3rd = 84.2N702.W31
R1929
Do Not Stuff
2nd = 84.2N702.031
1D8V_S0
R1928
10KR2J-L-GP
SATA_LED#
R1909 402R2F-GP
R1912
49D9R2F-L1-GP
R1922
49D9R2F-L1-GP
TP703
SOC_RUNTIME_SCI#
I2C_INT_CPU
PCIE_TX_CPU_P2
PCIE_TX_CPU_N2
PCIE_TX_CPU_P3
PCIE_TX_CPU_N3
PCIE_RX_CPU_P3
PCIE_RX_CPU_N3
C1906
C1907
C1908
C1909
SCD1U16V2KX-L-GP
PCIE_TX_WLAN_P2 58,86
PCIE_TX_WLAN_N2 58,86
PCIE_RX_CPU_P2 58,86
PCIE_RX_CPU_N2 58,86
PCIE_TX_LAN_P3 30
PCIE_TX_LAN_N3 30
PCIE_RX_CPU_P3 30
PCIE_RX_CPU_N3 30
PEG_CLKREQ_CPU#
CK_REQ
WLAN_CLKREQ_WLAN#
PCIE_CLK_LAN_REQ#
TP_IN#_CPU
R1937
10KR2J-L-GP
R1919
402R2F-GP
PCIE_RCOMP_P_AP14 AP14
PCIE_RCOMP_N_AP13 AP13
49D9R2F-L1-GP
R1914
HDA_SDOUT_CODEC 27
HDA_SDIN0_CPU 27
R1917
33R2J-L1-GP
LPE_I2S2_FRM 15
LPE_I2S2_DATAOUT 15,24
33D2R2F-GP
R1931
1D05V_S0
SA 20140418
H_PROCHOT# 24,44,46
Do Not Stuff R1923
SB 20140520-1
C1901
DY
Do Not Stuff
HDA_RST# CPU
Bay Trail
C1910
DY
Do Not Stuff
R1936
10KR2J-L-GP
PCIE_CLK_LAN_REQ# 30
R1939
10KR2J-L-GP
PEG_CLKREQ_CPU#
R1927
10KR2J-L-GP
WLAN_CLKREQ_WLAN# 58,86
RN1901
SRN33J-5-GP-U
27 HDA_BITCLK_CODEC
27 HDA_RST#_CODEC
HDA_BITCLK_CPU
HDA_RST# CPU
No eMMC
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (SATA/PCIE/IHDA)
Size A3
Document Number EA30_BM
Rev -1
Date: Tuesday, July 08, 2014
Sheet 19 of 102

SSID = PCH

Blanking

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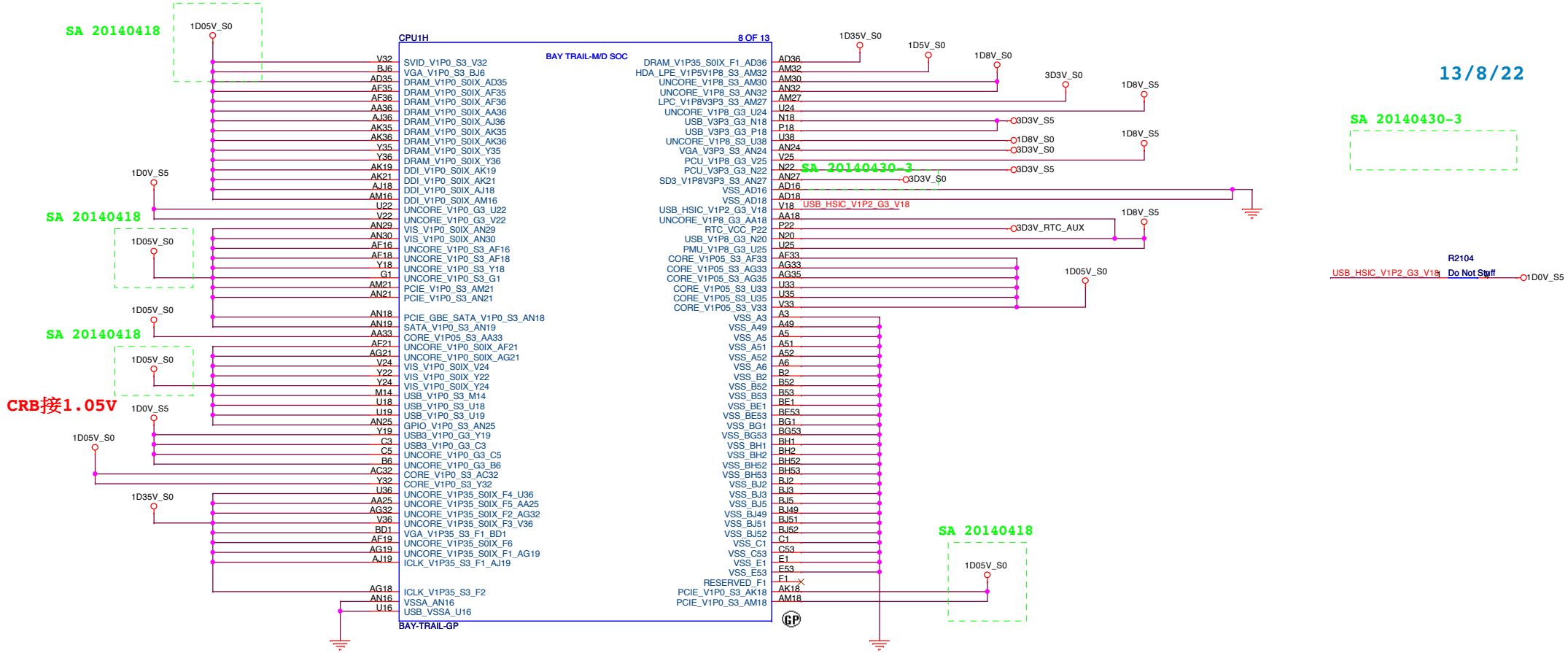
Title: *Reserved*

Size	Document Number	Rev
A4	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 20 of 102



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Title: **CPU (POWER1)**

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 21 of 102

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Title

Reserved

Size	Document Number	Rev
Custom	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 22 of 102

SSID = PCH

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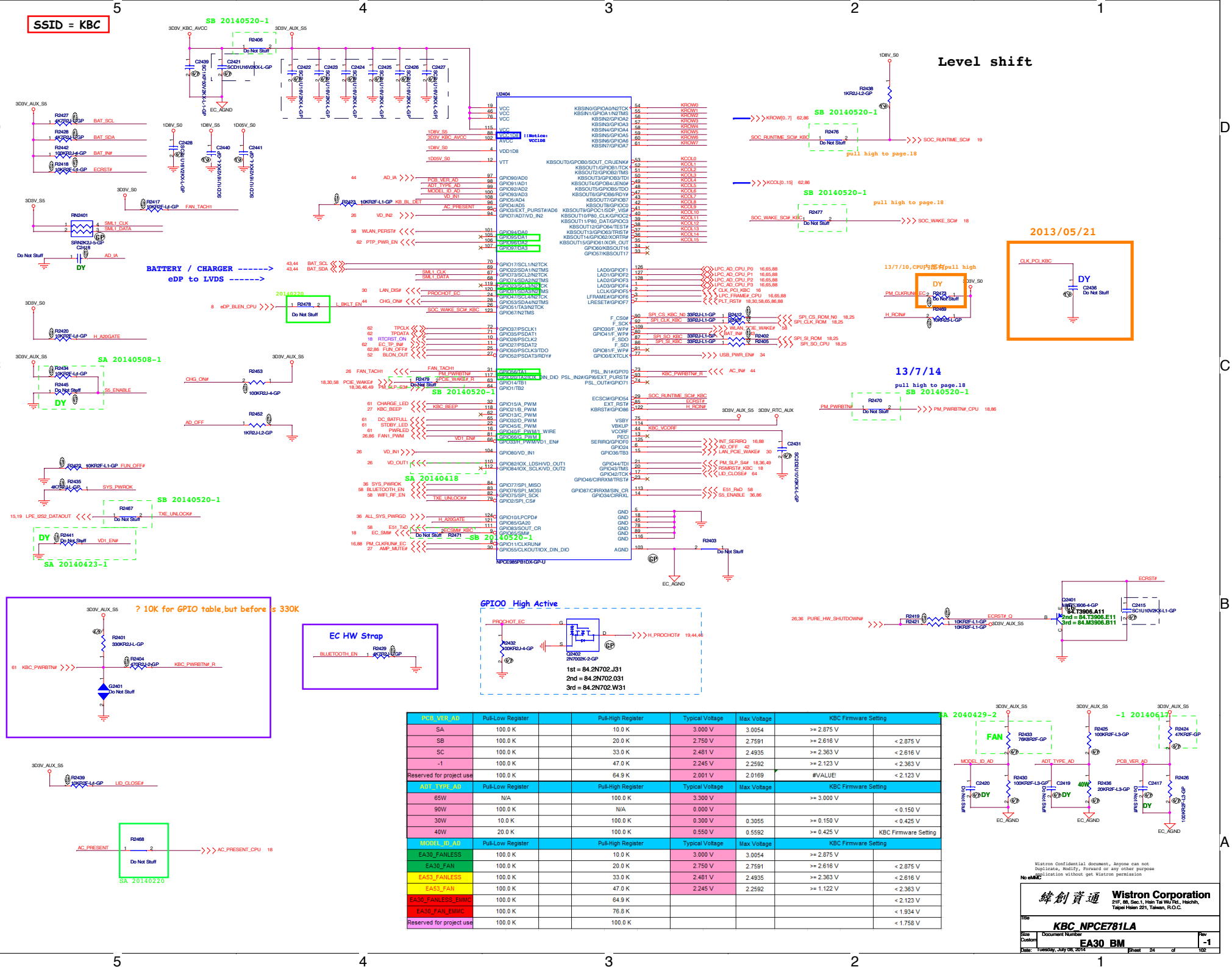
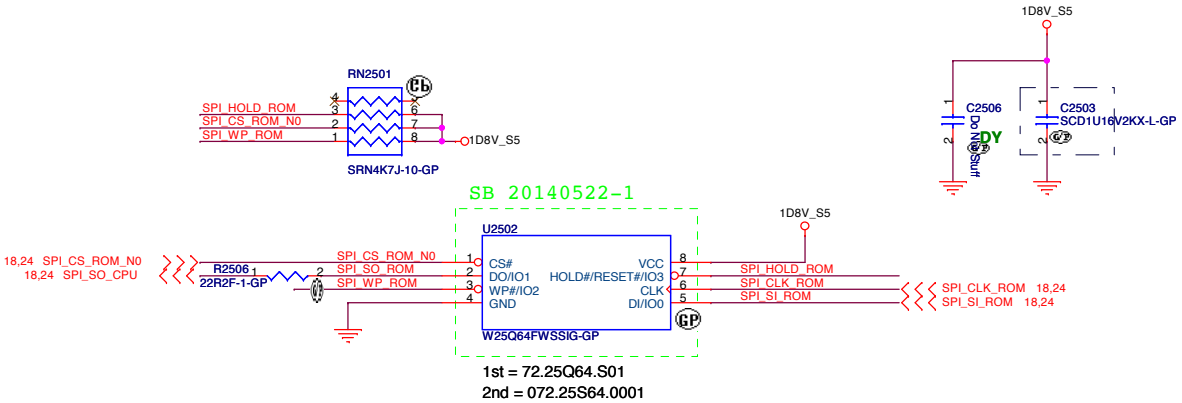
Title	CPU (VSS)	
Size: Custom	Document Number: EA30_BM	Rev: -1
Date: Tuesday, July 08, 2014	Sheet 23 of 102	



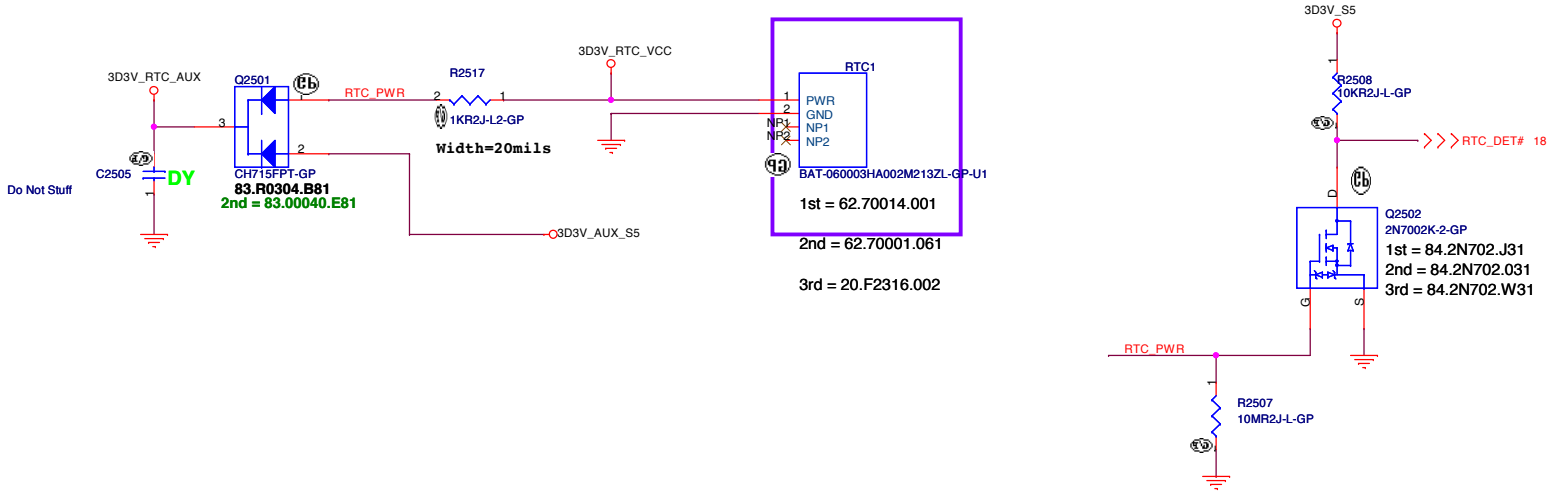
PCB_VER_AD	Pull-Low Register		Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K		10.0 K	3.000 V	3.0054	>= 2.875 V	
SB	100.0 K		20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
SC	100.0 K		33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
-1	100.0 K		47.0 K	2.245 V	2.2592	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K		64.9 K	2.001 V	2.0169	#VALUE!	< 2.123 V
ADT_TYPE_AD	**Pull-Low Register**		**Pull-High Register**	**Typical Voltage**	**Max Voltage**	**KBC Firmware Setting**	
65W	N/A		100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K		N/A	0.000 V			< 0.150 V
30W	10.0 K		100.0 K	0.300 V	0.3055	>= 0.150 V	< 0.425 V
40W	20.0 K		100.0 K	0.550 V	0.5592	>= 0.425 V	KBC Firmware Setting
MODEL_ID_AD	**Pull-Low Register**		**Pull-High Register**	**Typical Voltage**	**Max Voltage**	**KBC Firmware Setting**	
EA30_FANLESS	100.0 K		10.0 K	3.000 V	3.0054	>= 2.875 V	
EA30_FAN	100.0 K		20.0 K	2.750 V	2.7591	>= 2.616 V	< 2.875 V
EA53_FANLESS	100.0 K		33.0 K	2.481 V	2.4935	>= 2.363 V	< 2.616 V
EA53_FAN	100.0 K		47.0 K	2.245 V	2.2592	>= 1.122 V	< 2.363 V
EA30_FANLESS_EMMC	100.0 K		64.9 K				< 2.123 V
EA30_FAN_EMMC	100.0 K		76.8 K				< 1.934 V
Reserved for project use	100.0 K		100.0 K				< 1.758 V

SSID = Flash.ROM

SPI FLASH ROM (8M Byte) for PCH



SSID = RBAT



SPI FLASH ROM (128k byte) for EC

SPI ROM Equal length need to less than 500mil

72.25010.N01

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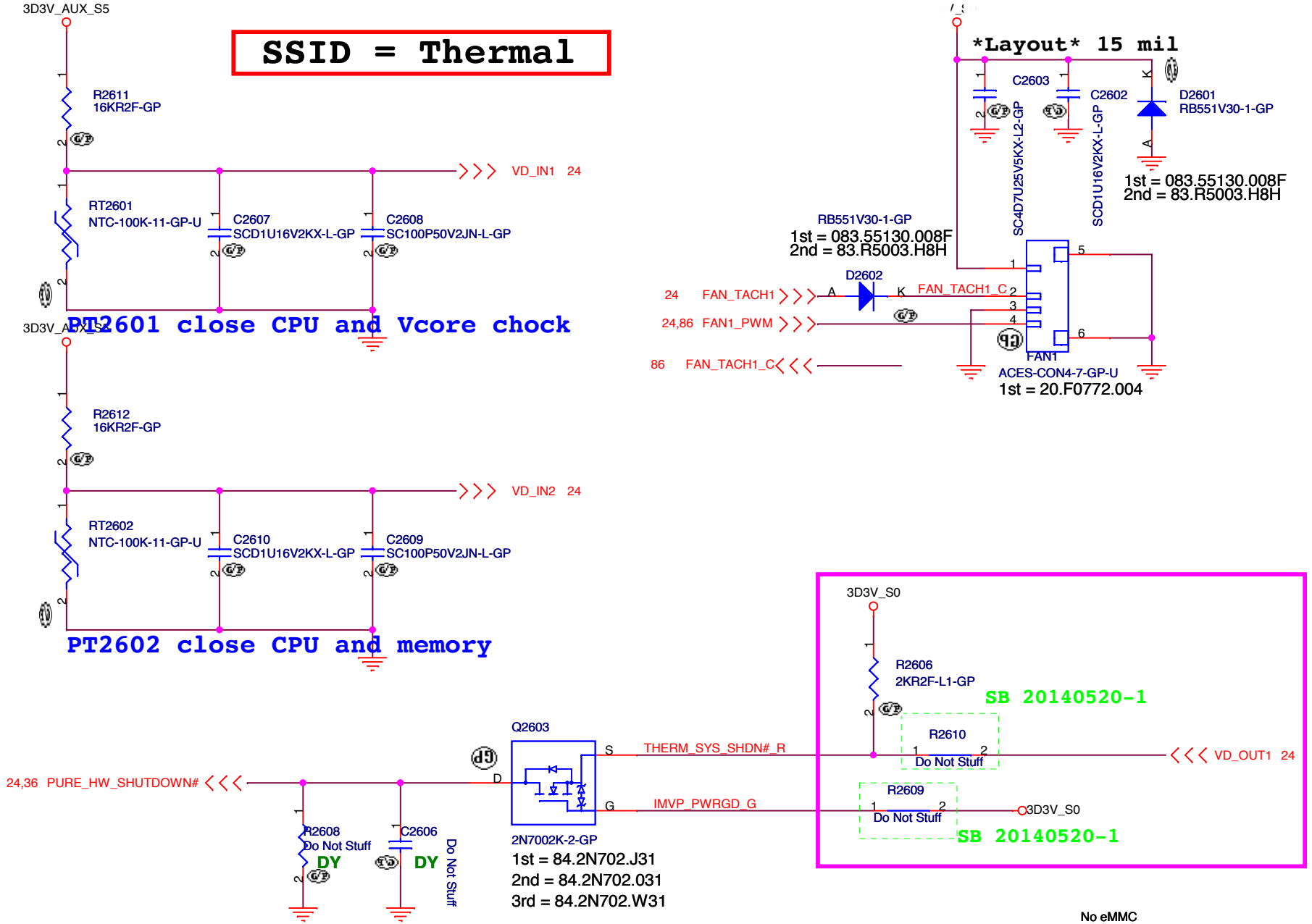
Title: Flash(KBC+PCH)/RTC

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 25 of 102



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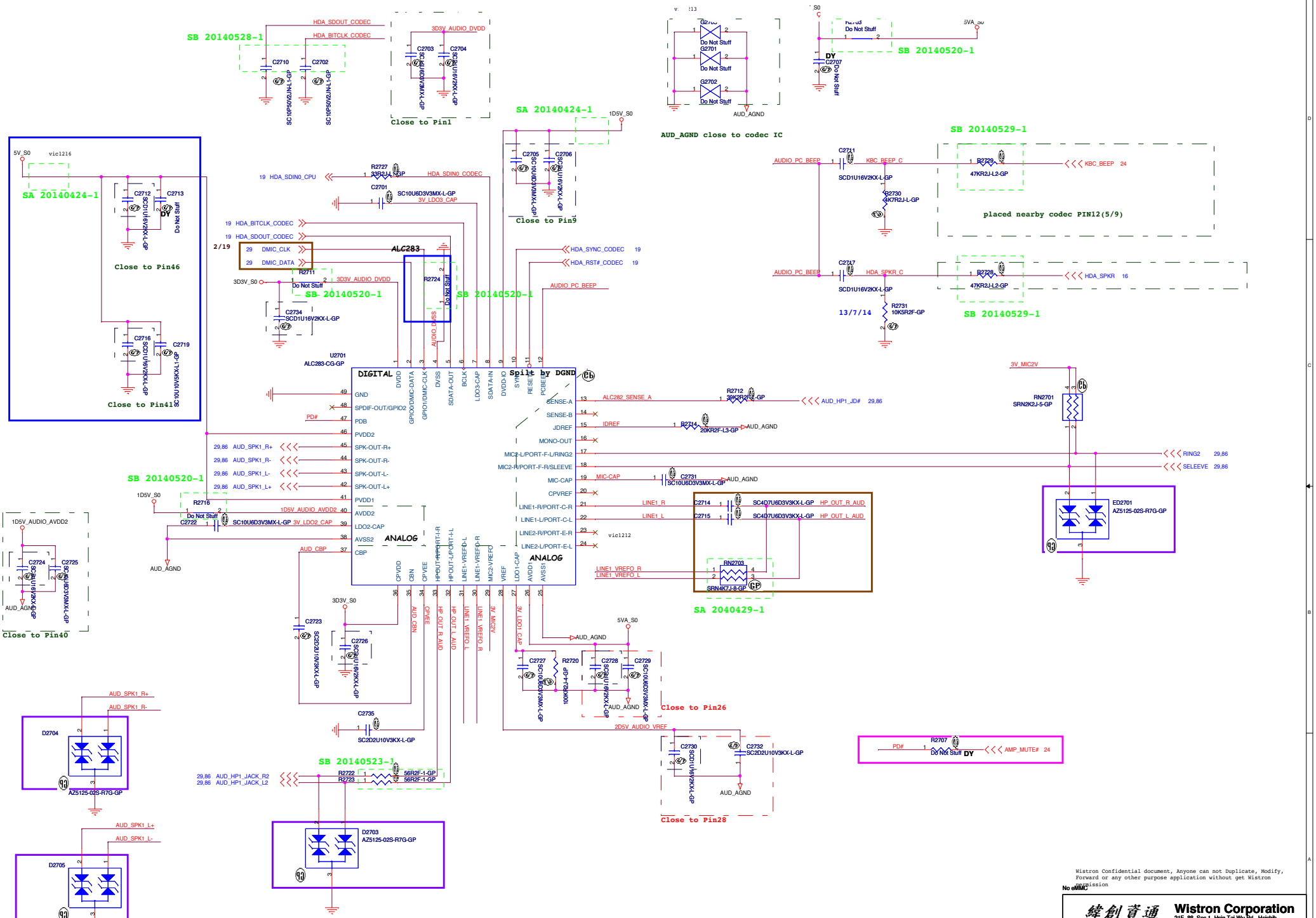
Taipei Hsien 221, Taiwan, R.O.C.

Title
G788P81/Fan Controllor P2793

Size	Document Number	Rev
A4	**EA30 BM**	**-1**

Date: Tuesday, July 08, 2014 Sheet 26 of 102



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Title: **Audio Codec_ALC3225**

Size	Document Number	Rev
C	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 27 of 102

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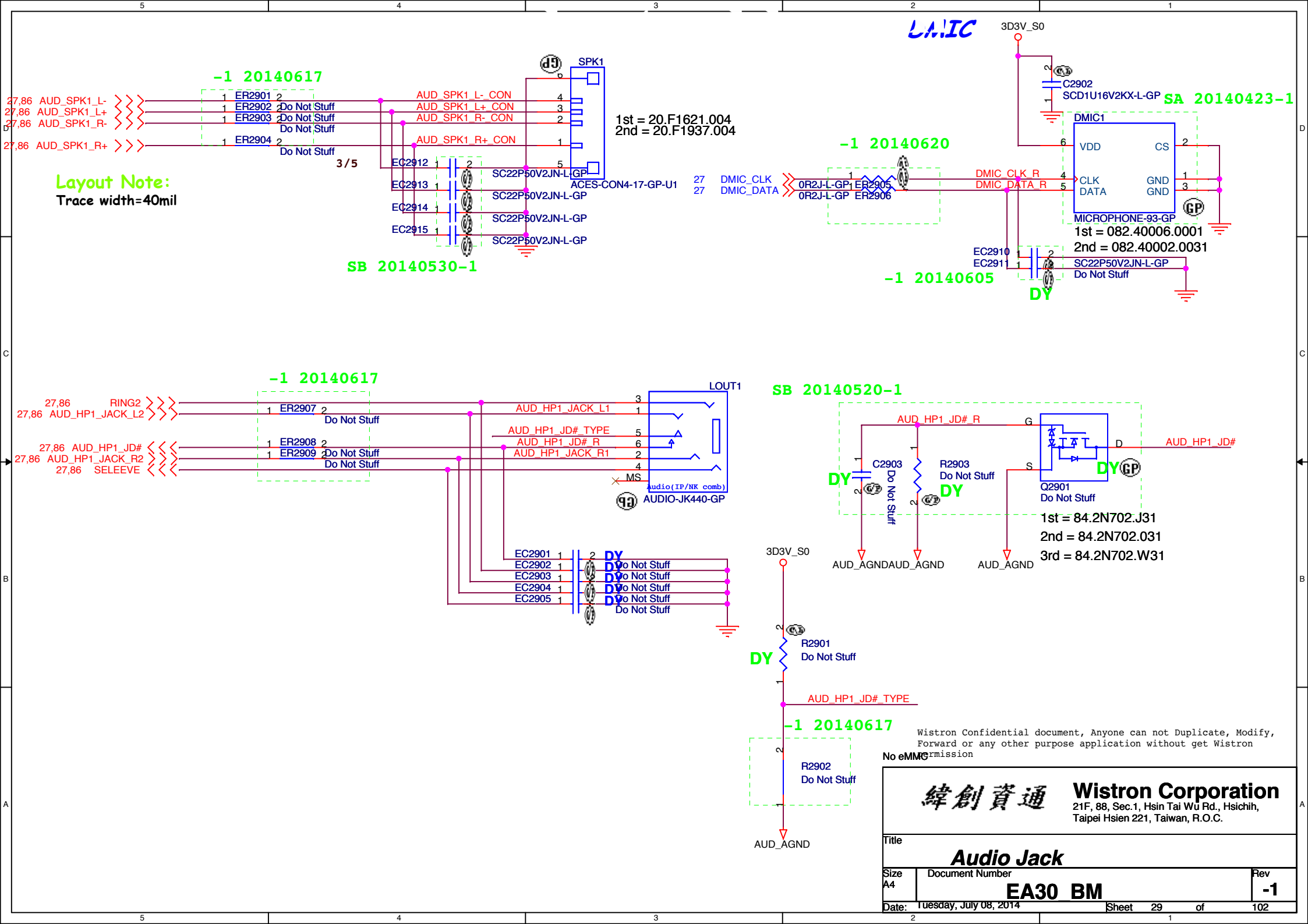
Title

Audio AMP_1001

Size	Document Number	Rev
A4	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 28 of 102


LAIC
-1 20140617
27,86 AUD_SPK1_L-
27,86 AUD_SPK1_L+
27,86 AUD_SPK1_R-
27,86 AUD_SPK1_R+
ER2901 Do Not Stuff
ER2902 Do Not Stuff
ER2903 Do Not Stuff
ER2904 Do Not Stuff
AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON
3/5
EC2912
EC2913
EC2914
EC2915
SC22P50V2JN-L-GP
SPK1
ACES-CON4-17-GP-U1
1st = 20.F1621.004
2nd = 20.F1937.004
SB 20140530-1
Layout Note:
Trace width=40mil
3D3V_S0
C2902
SCD1U16V2KX-L-GP
SA 20140423-1
DMIC1
VDD
CS
CLK
DATA
GND
GND
MICROPHONE-93-GP
-1 20140620
27 DMIC_CLK
27 DMIC_DATA
0R2J-L-GP ER2905
0R2J-L-GP ER2906
DMIC_CLK_R
DMIC_DATA_R
1st = 082.40006.0001
2nd = 082.40002.0031
EC2910
EC2911
SC22P50V2JN-L-GP
Do Not Stuff
-1 20140605
DY
-1 20140617
27,86 RING2
27,86 AUD_HP1_JACK_L2
27,86 AUD_HP1_JD#
27,86 AUD_HP1_JACK_R2
27,86 SELEEVE
ER2907 Do Not Stuff
ER2908 Do Not Stuff
ER2909 Do Not Stuff
AUD_HP1_JACK_L1
AUD_HP1_JD#_TYPE
AUD_HP1_JD#_R
AUD_HP1_JACK_R1
MS
LOUT1
Audio(IP/NK comb)
AUDIO-JK440-GP
EC2901
EC2902
EC2903
EC2904
EC2905
DY
Do Not Stuff
SB 20140520-1
AUD_HP1_JD#_R
C2903
Do Not Stuff
R2903
Do Not Stuff
Q2901
Do Not Stuff
AUD_HP1_JD#
AUD_AGND
1st = 84.2N702.J31
2nd = 84.2N702.031
3rd = 84.2N702.W31
3D3V_S0
R2901
Do Not Stuff
AUD_HP1_JD#_TYPE
-1 20140617
R2902
Do Not Stuff
AUD_AGND
No eMMC
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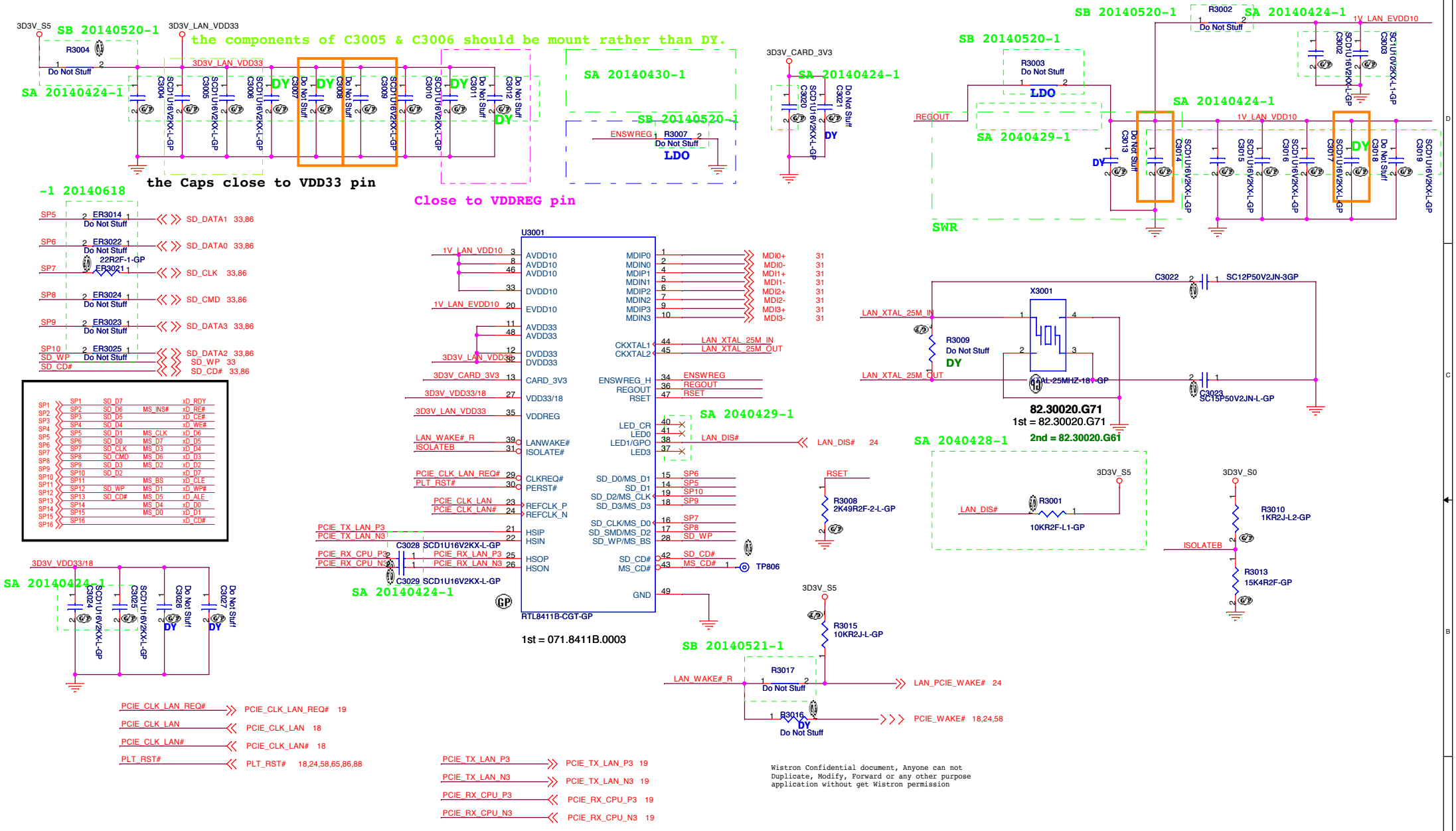
Title
Audio Jack
Size A4
Document Number
EA30 BM
Rev -1
Date: Tuesday, July 08, 2014
Sheet 29 of 102



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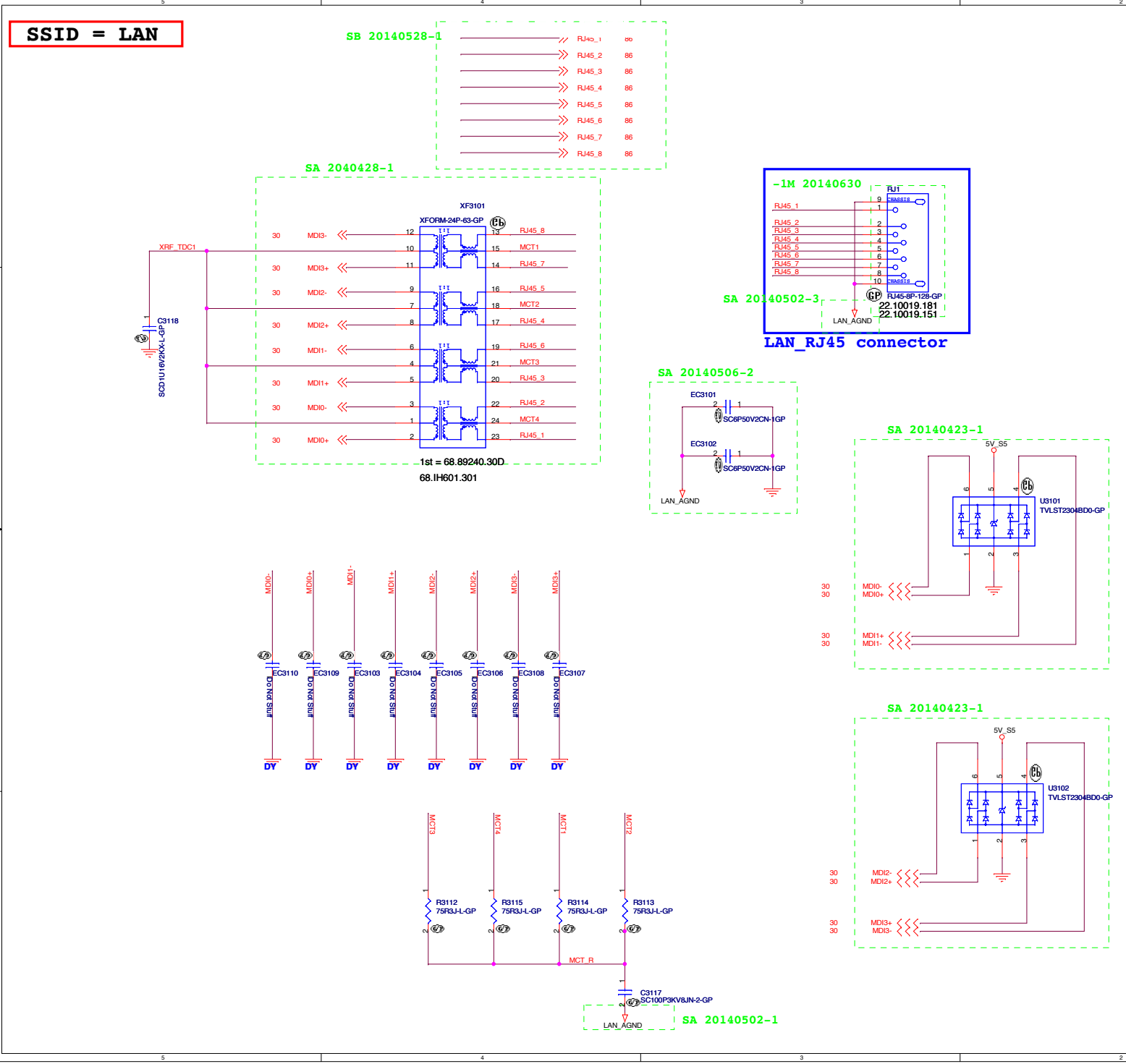
Title	***LAN(RTL8411)***
Size A3	Document Number **EA30 BM** Rev **-1**
Date: Tuesday, July 08, 2014	Sheet 30 of 102



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Title	***(LAN+VGA) CONNECTOR***
Size: Custom	Document Number: **EA30_BM**
Rev	**-1**
Date: Tuesday, July 08, 2014	Sheet 31 of 102

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Title

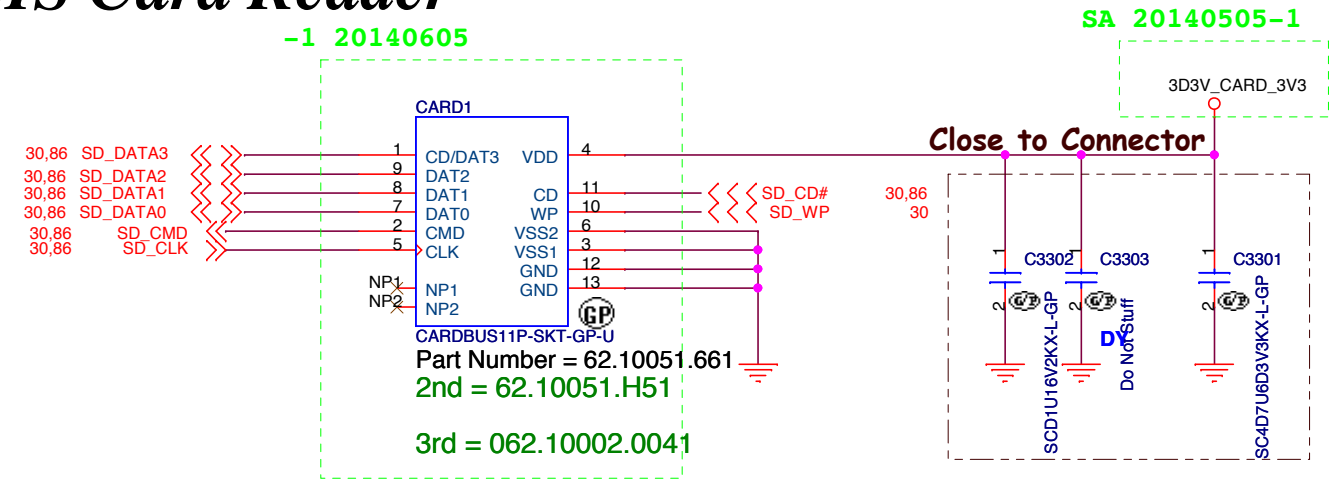
RTS5229(CARD READER)

Size	Document Number	Rev
A4	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 32 of 102

SSID = SDIO

SD//MS Card Reader



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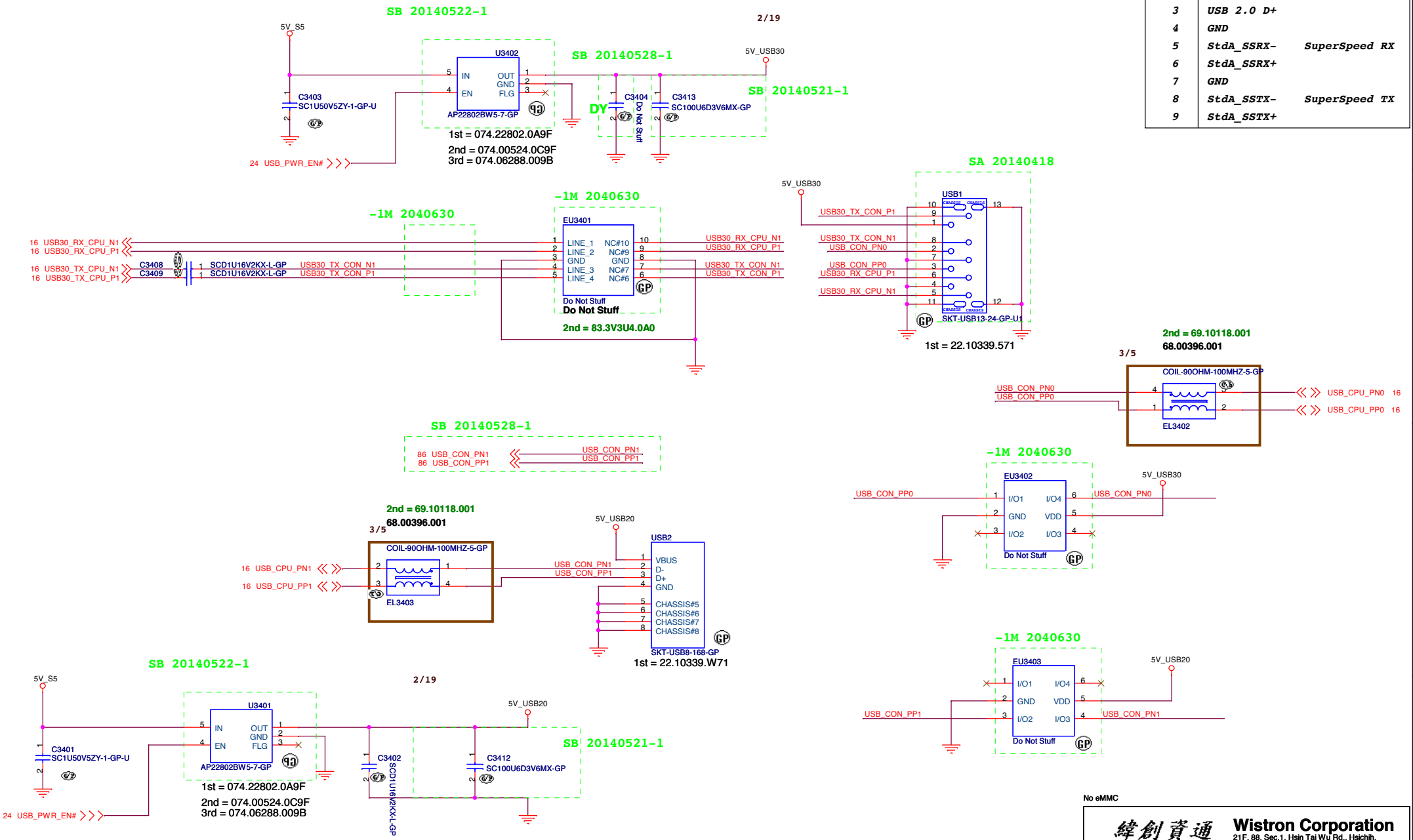
Title		
CARD Reader CONN		
Size: Custom	Document Number: EA30_BM	Rev: -1
Date: Tuesday, July 08, 2014	Sheet 33 of 102	

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



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Title: **USB 2.0 / 3.0 Port**

Size	Document Number	Rev
A3	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 34 of 102

No eMMC

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Title

USB CHARGER

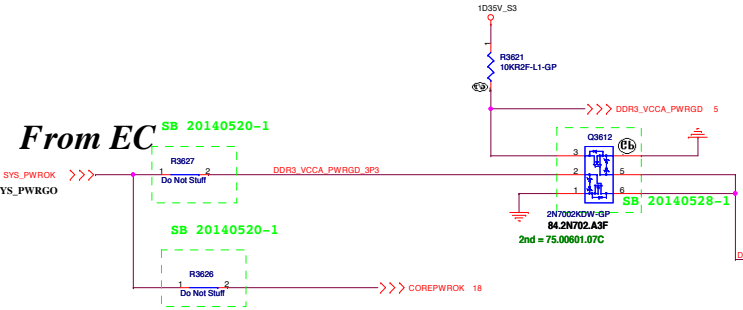
Size	Document Number	Rev
A3	EA30_BM	-1

Power Sequence

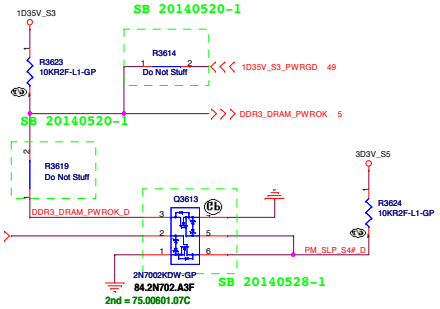
Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

DDR3_VCCA_PWRGD



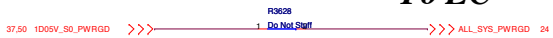
DDR3_DRAM_PWROK



ALL_SYS_PWRGD

13/8/22

To EC

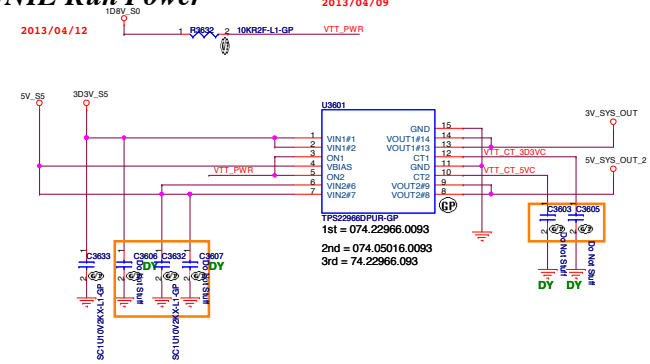


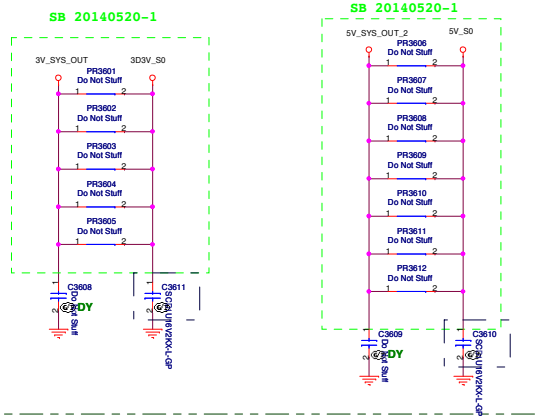
ANNIE Run Power

13/9/18

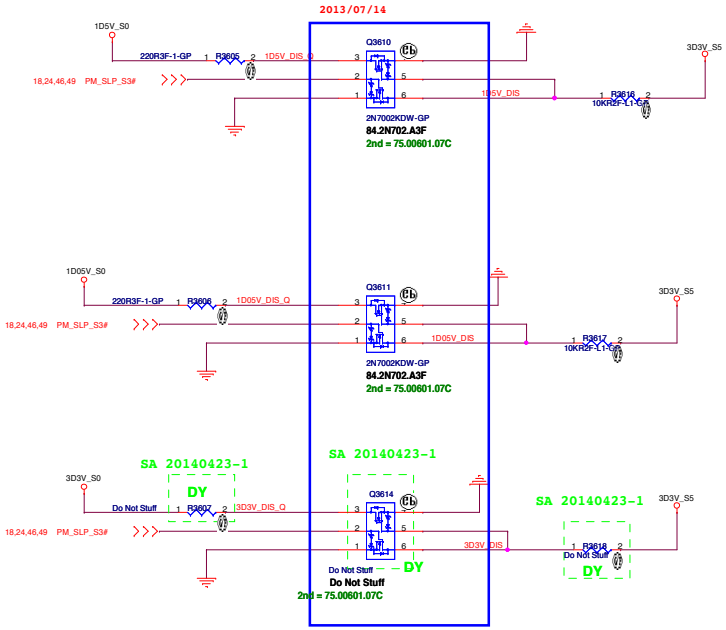
2013/04/09

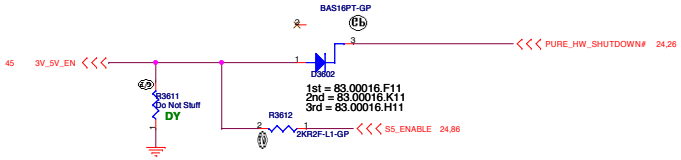
2013/04/12





Discharge circuit





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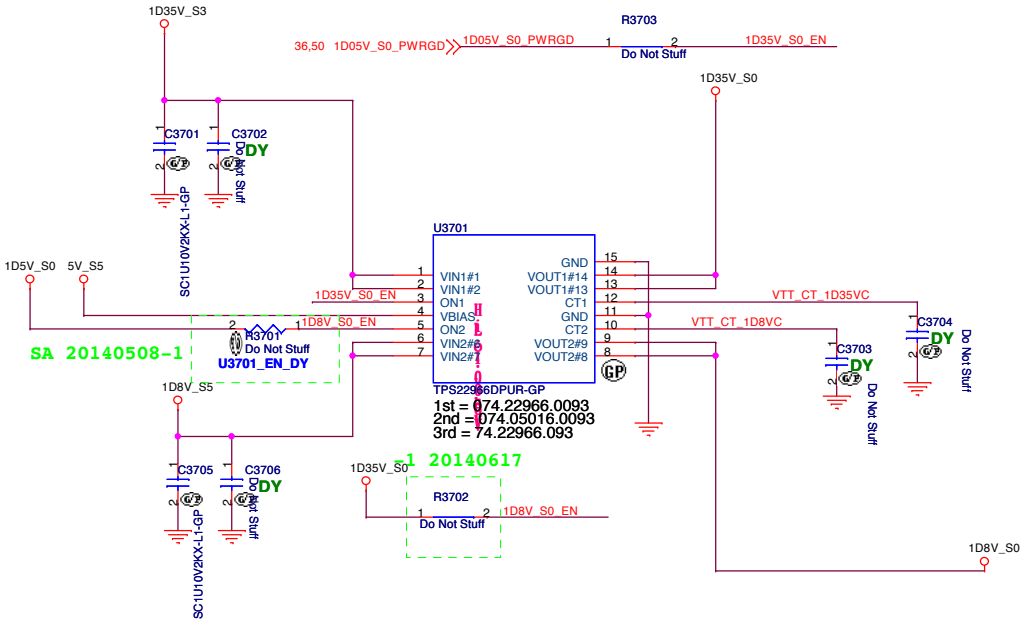
Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: EA30_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 36 of 102

1D35V_S0
1D8V_S0



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Title: ADAPTER OCP / S3 reduction

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 37 of 102

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Title

DS3

Size	Document Number	Rev
A4	EA30 BM	-1

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Power Sequence

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Title	1D05_M	
Size: Custom	Document Number: EA30_BM	Rev: -1
Date: Tuesday, July 08, 2014	Sheet 39 of 102	

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Title

Connected Standby1

Size	Document Number	Rev
A	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 40 of 102

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Title

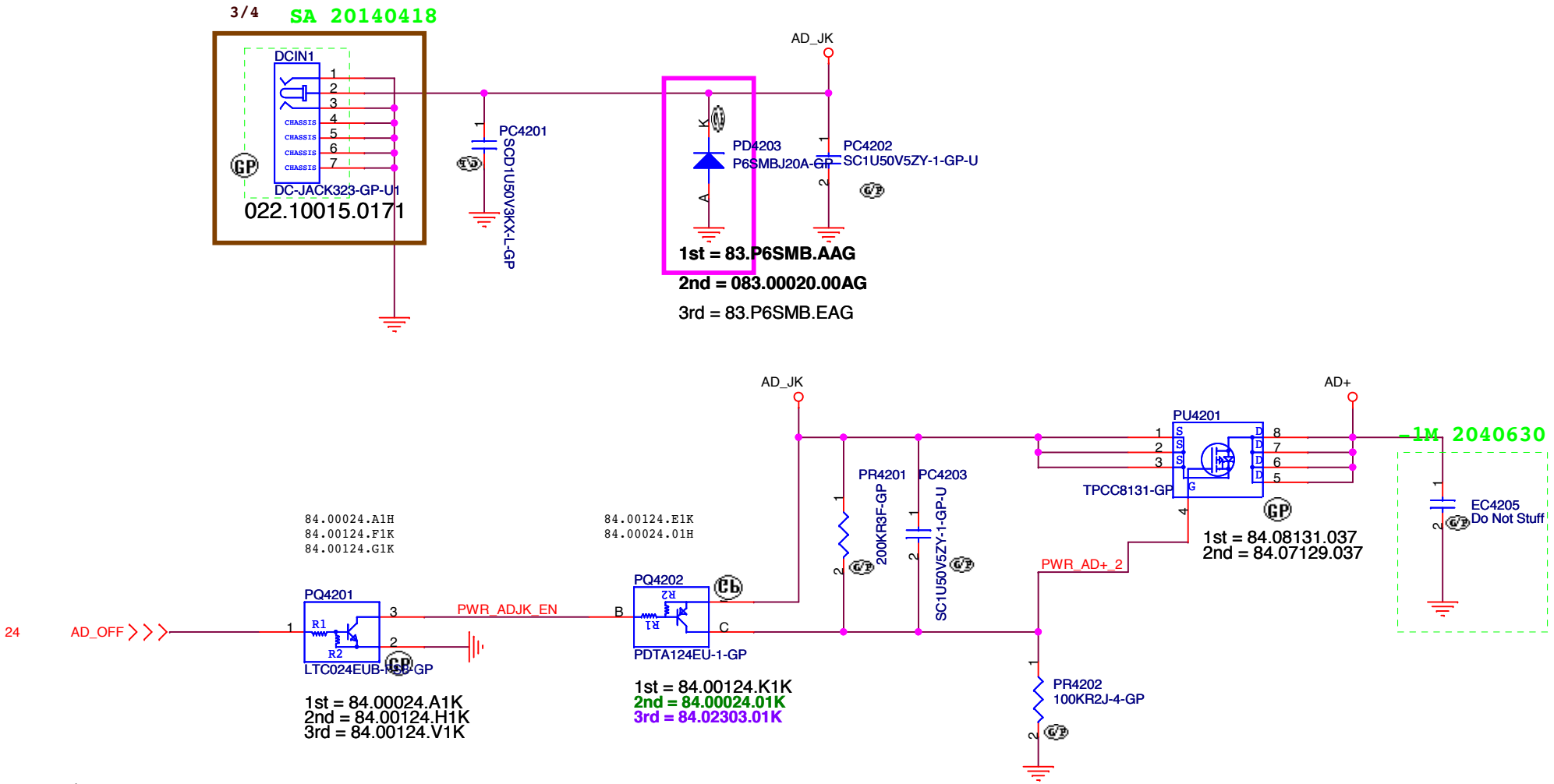
Connected Standby2

Size	Document Number	Rev
A	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 41 of 102

ANNIE solution

Adaptor in to generate DCBATOUT



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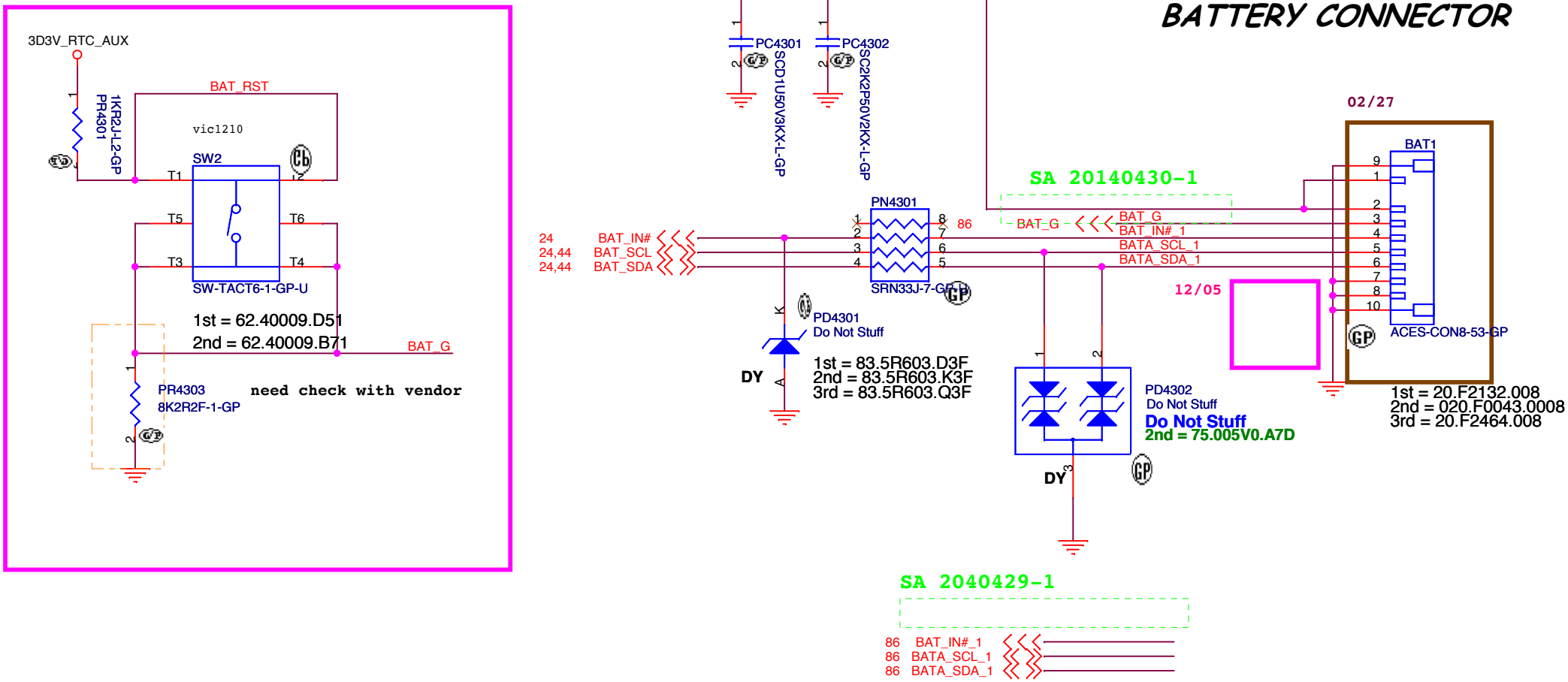
Title	DCIN JACK	
Size A4	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 42 of 102	

BATTERY CONNECTOR



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No eMMC

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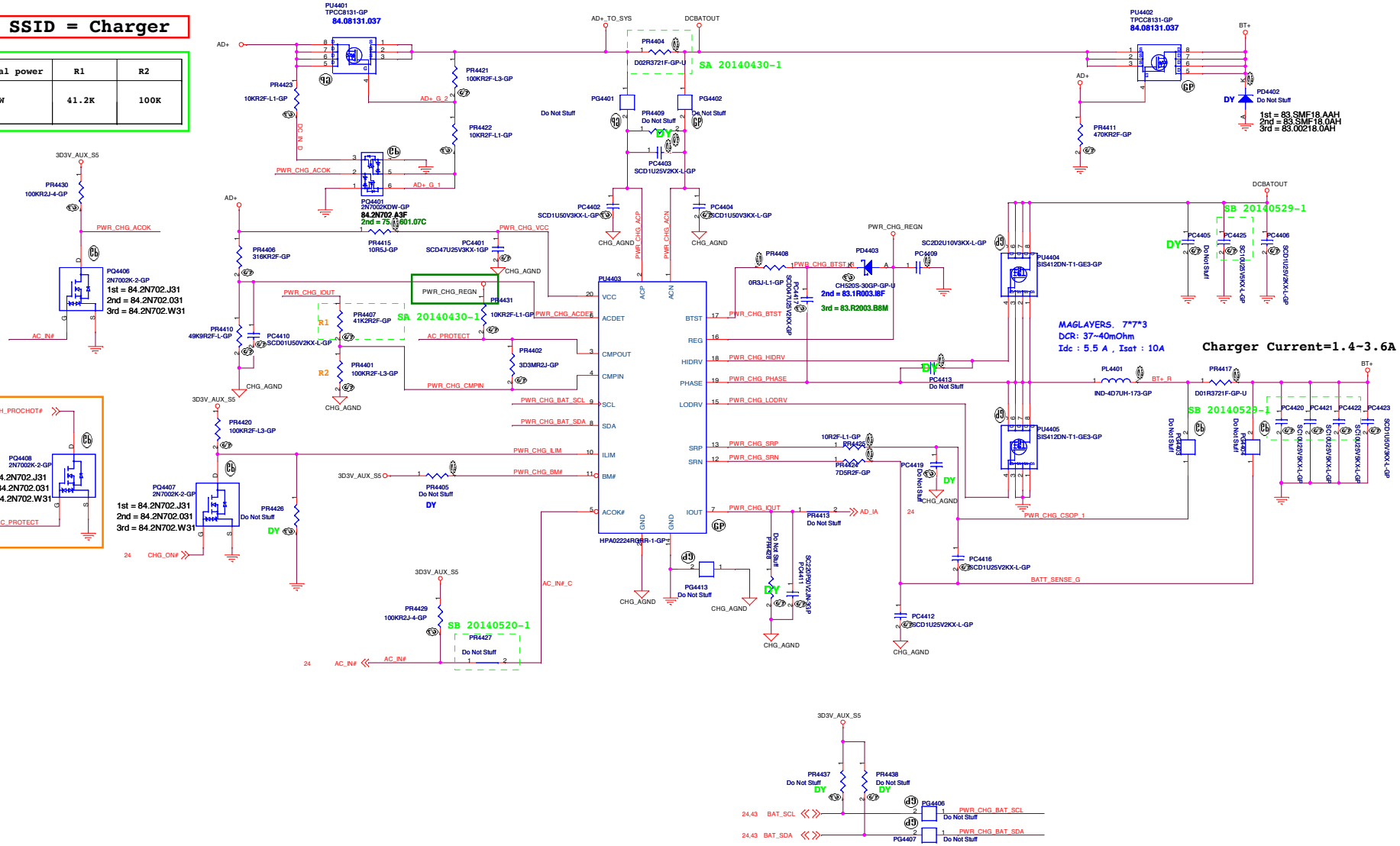
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size A4	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 43 of 102	

SSID = Charger

SSID = Charger

AD+ total power	R1	R2
40W	41.2K	100K



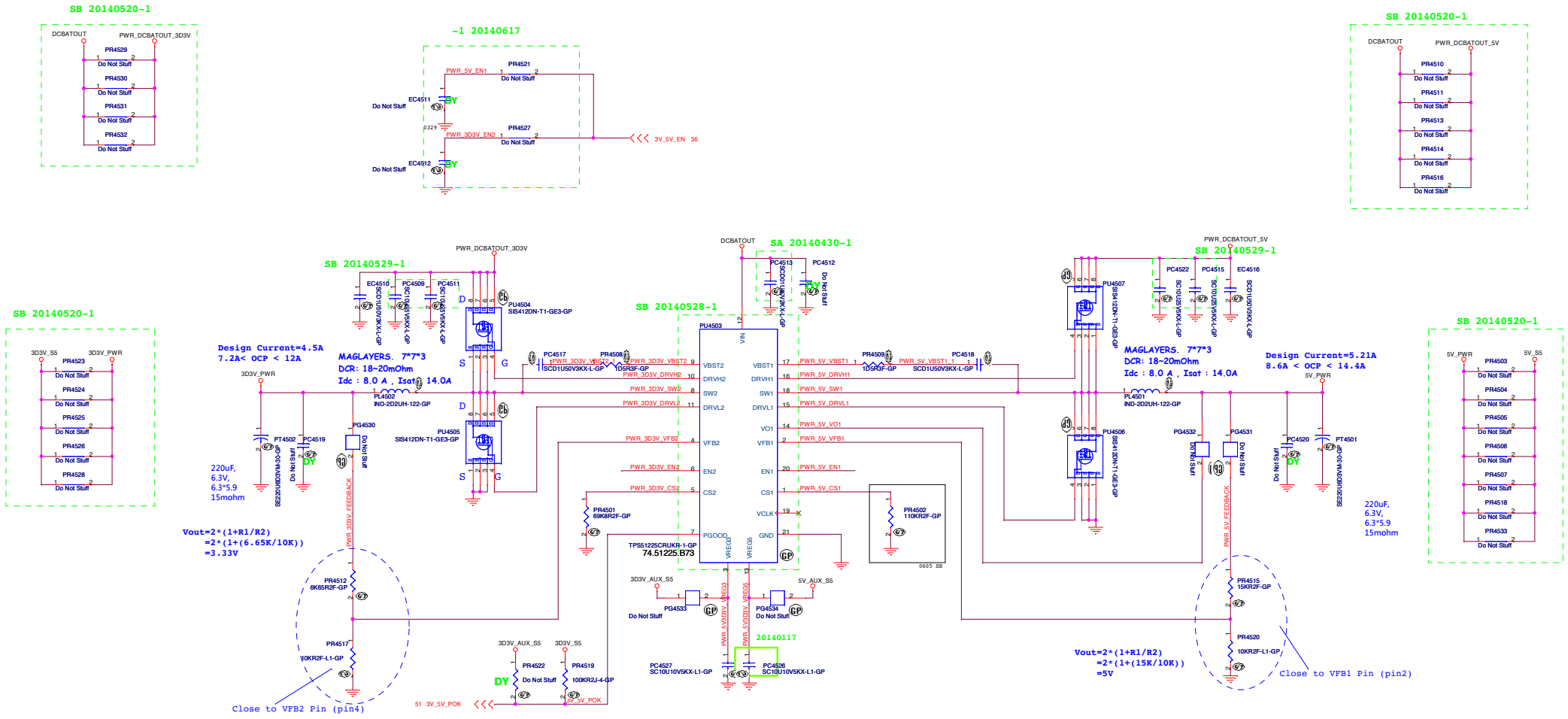
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER_BQ24727

Size: A2 | Document Number: EA51_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 44 of 102

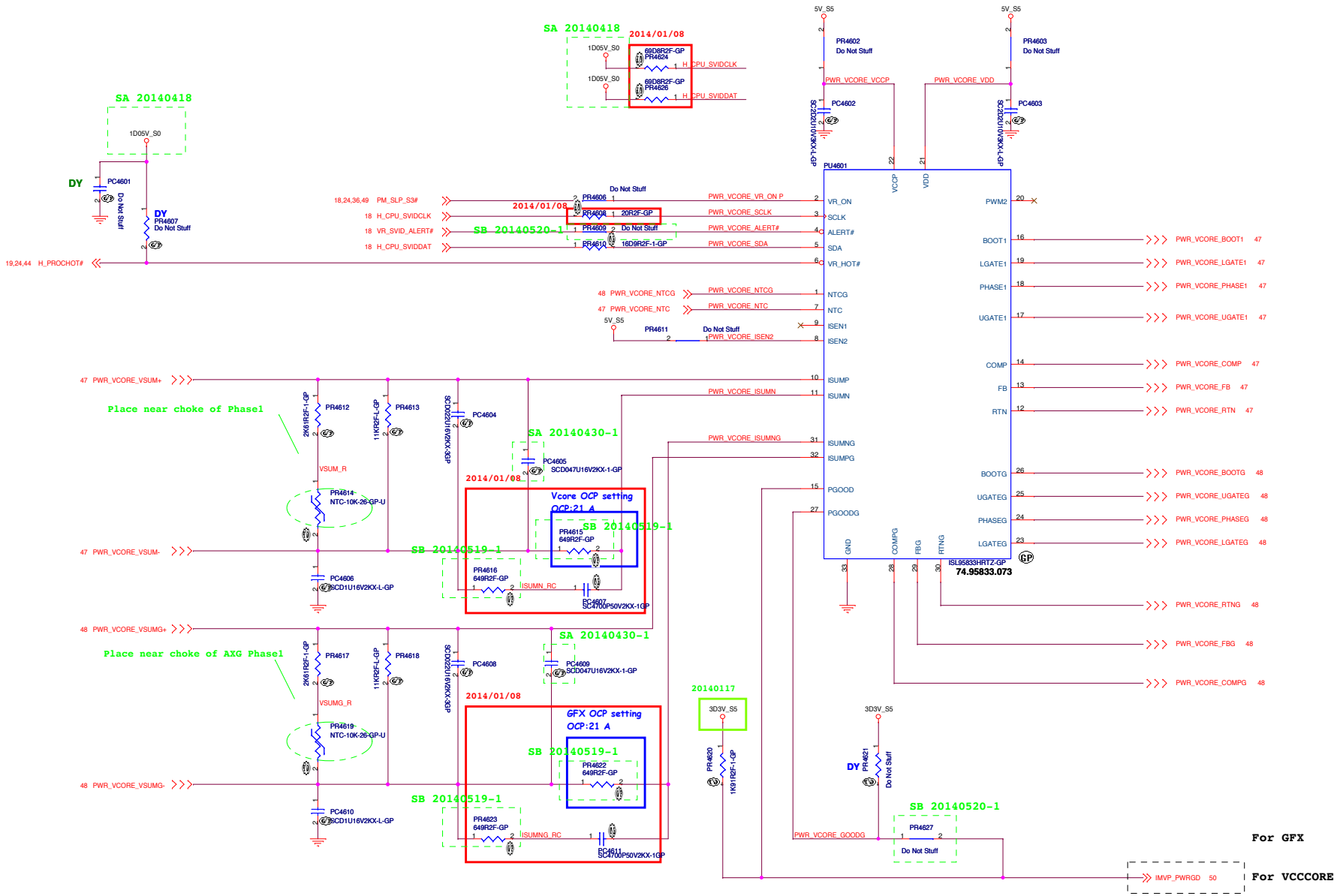
SSID = PWR.Plane.Regulator_3p3v5v



No eMMC

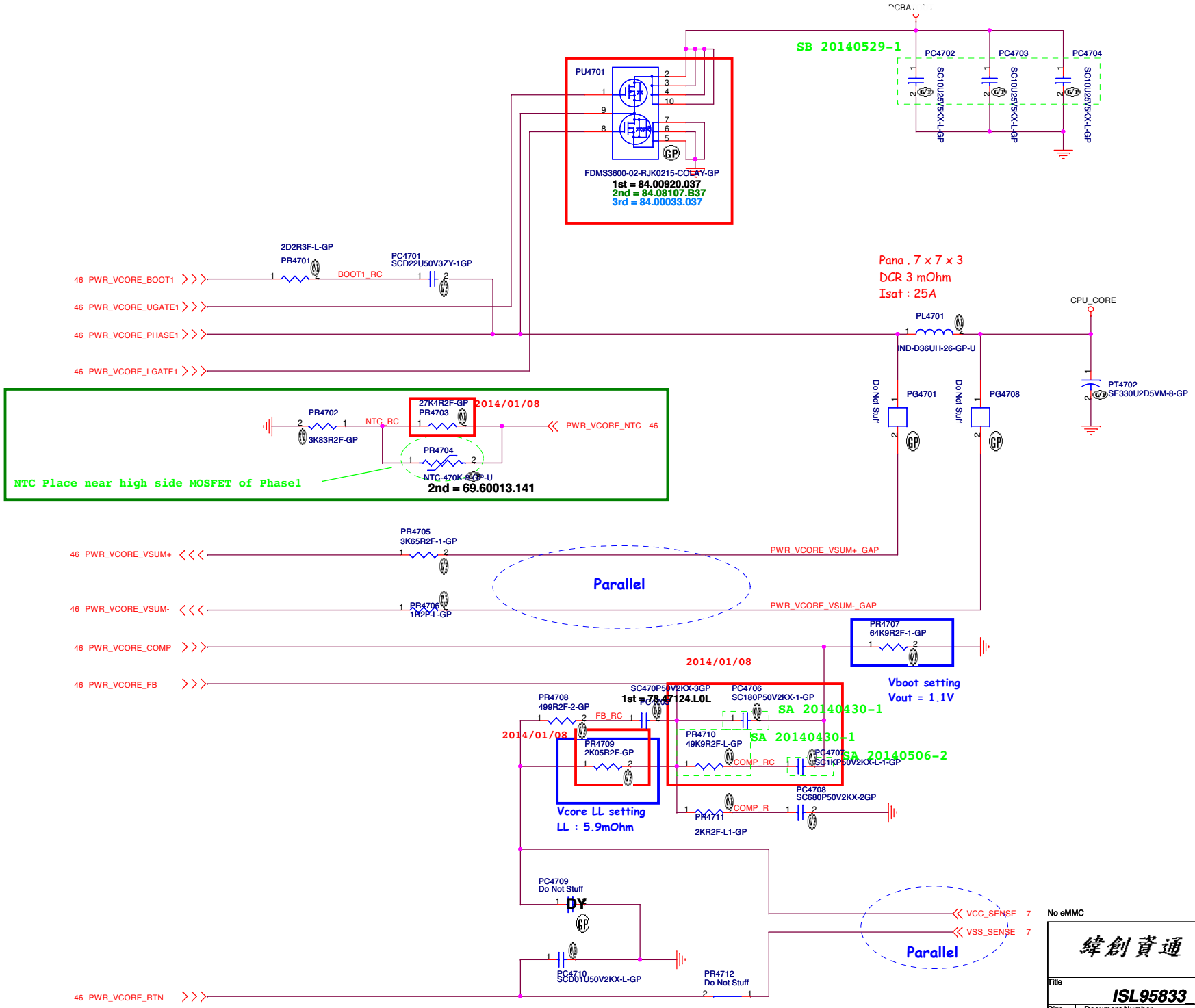
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51225_5V/3D3V		
Size: A2	Document Number: EA51_BM	Rev: -1
Date: Tuesday, July 08, 2014	Sheet 45 of 102	

SSID = CPU.Regulator

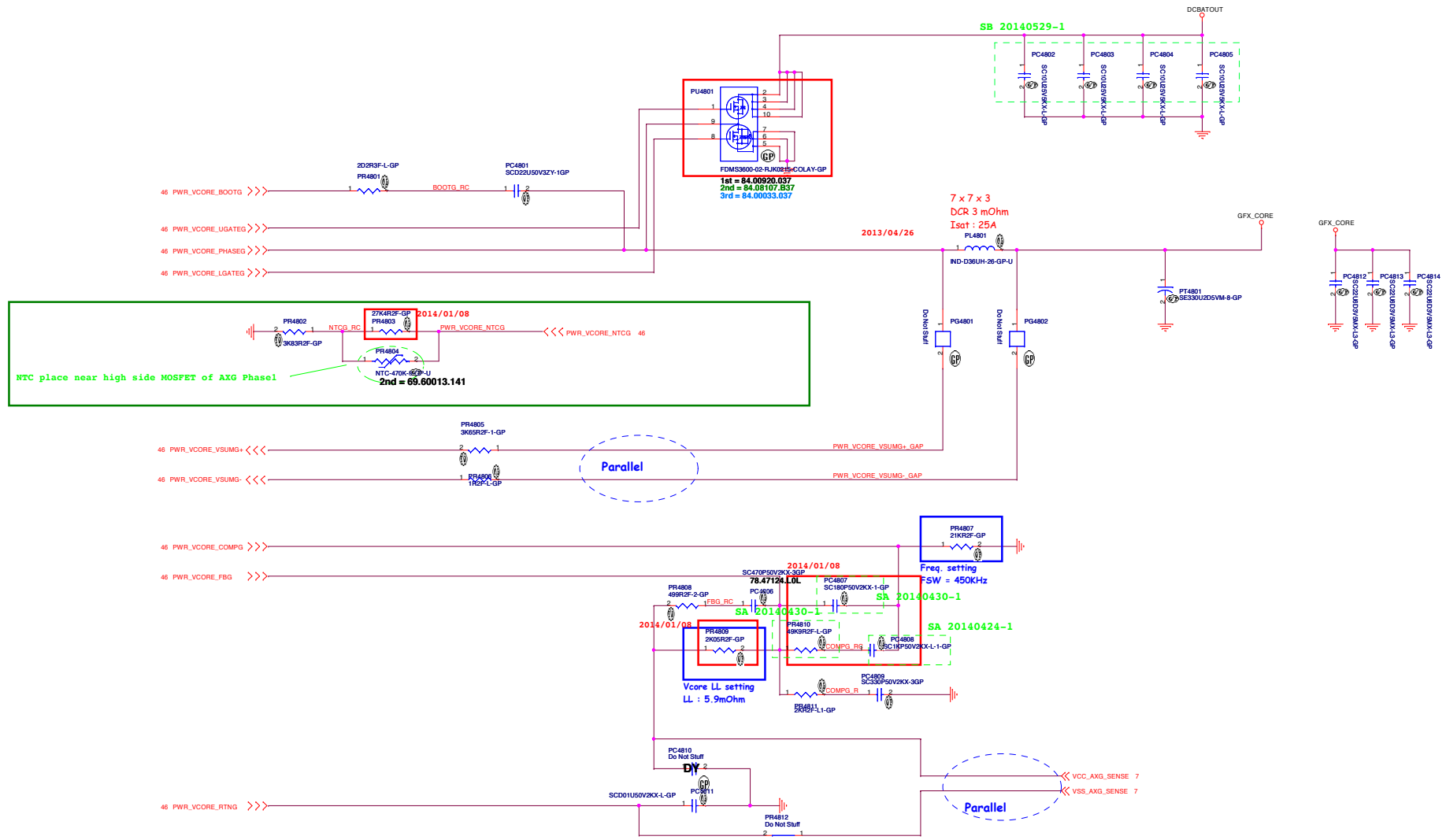


No eMMC

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL95833_CPUCORE(1/3)	
Size C	Document Number EA51_BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 46 of 102	



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL95833_CPUCORE(2/3)
Size A3	Document Number EA51_BM
Rev	-1
Date: Tuesday, July 08, 2014	Sheet 47 of 102



No eMMC

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

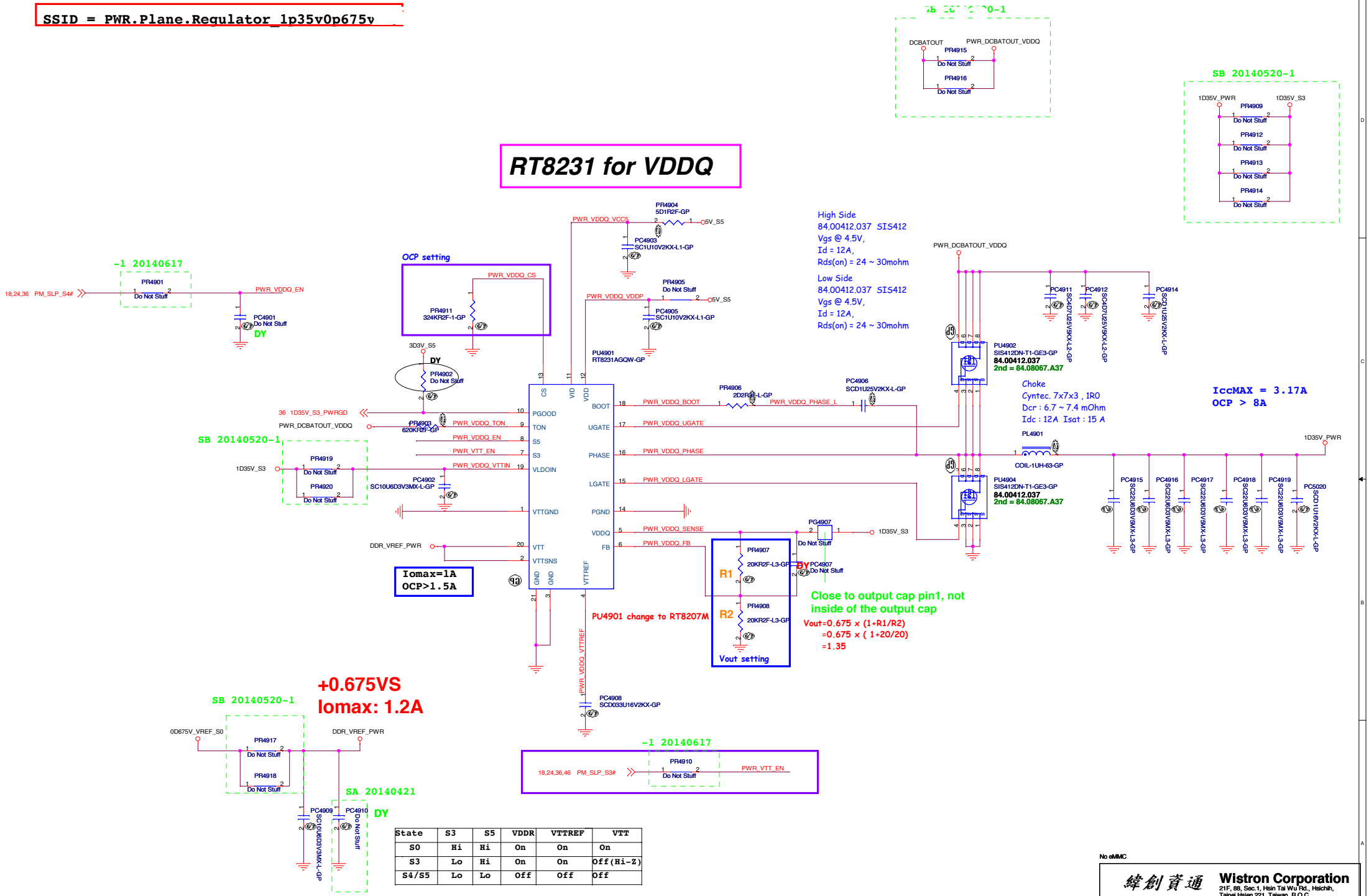
Title: *ISL95833_AGX_CORE(3/3)*

Size	Document Number	Rev
A2	EA51_BM	-1

Date: Tuesday, July 08, 2014 Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v

RT8231 for VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

No eMMC

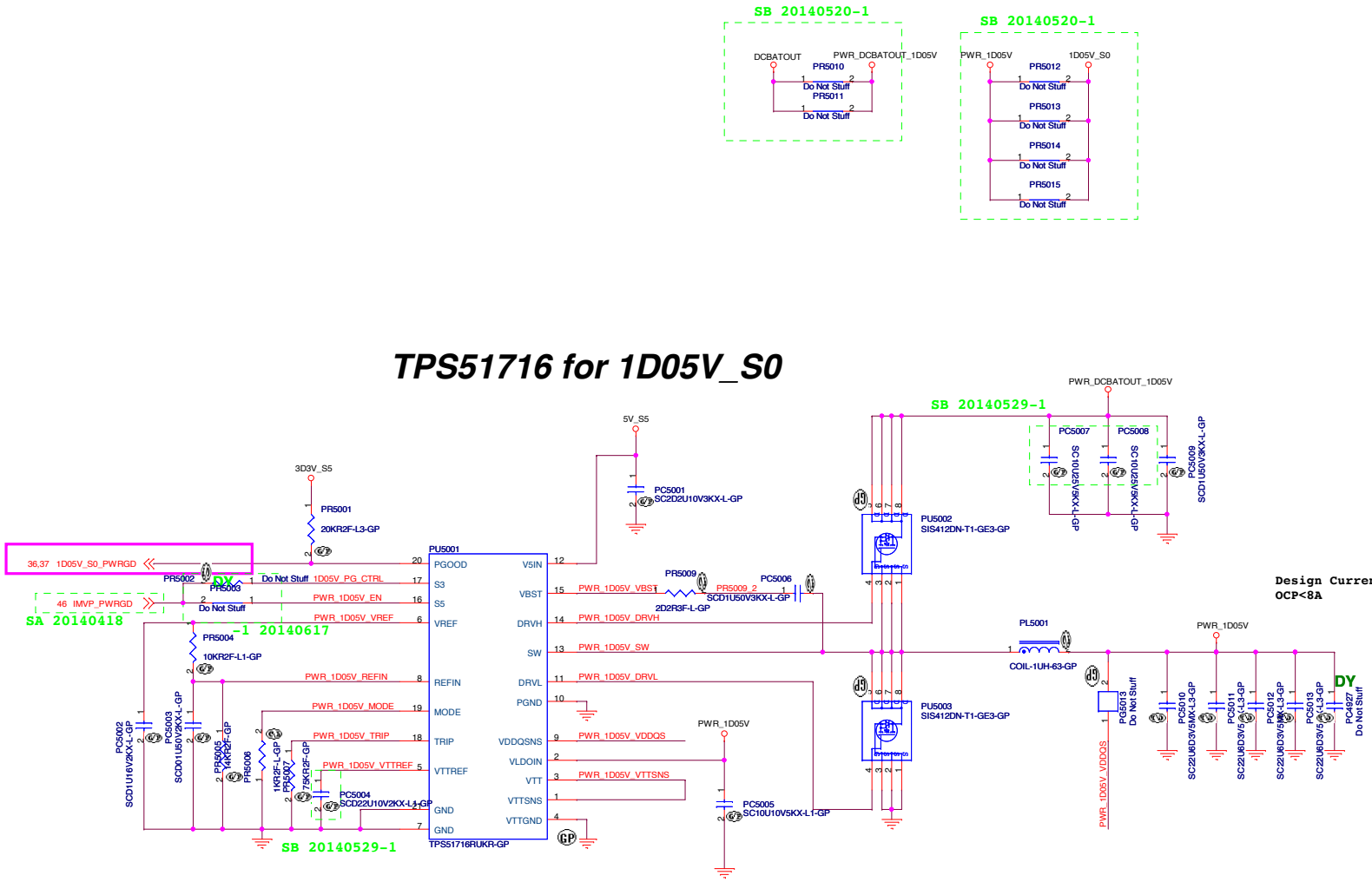
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231(1.35V_S3/0.675V_S0)

Size: Custom | Document Number: EA51_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 49 of 102

SSID = PWR.Plane.Regulator_1p05v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

No eMMC

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

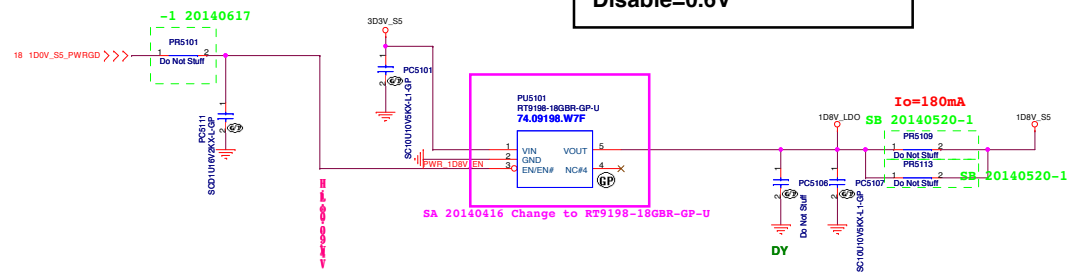
Title: DC to DC_1D05V(RT8231A)

Size: Custom | Document Number: EA51_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 50 of 102

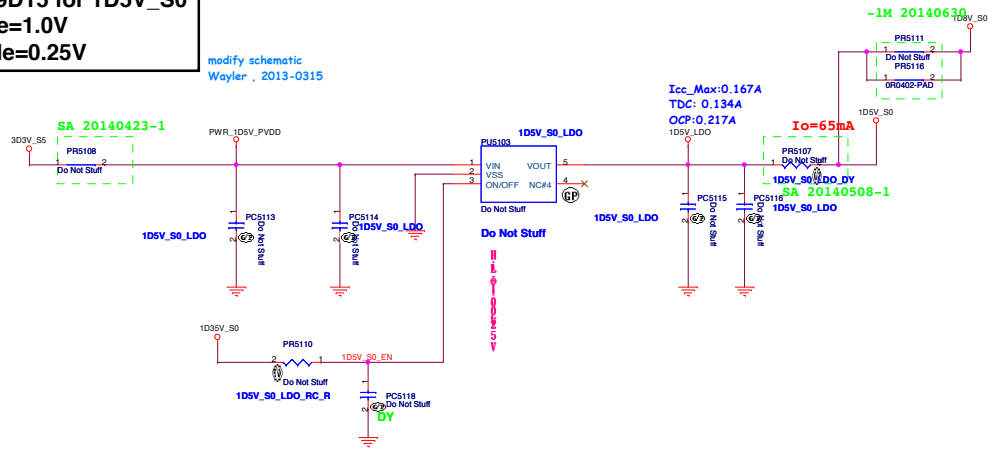
SSID = PWR.Plane.Regulator_1p8v

TLV70218DBVR for 1D8V_S5
Enable=0.9V
Disable=0.6V



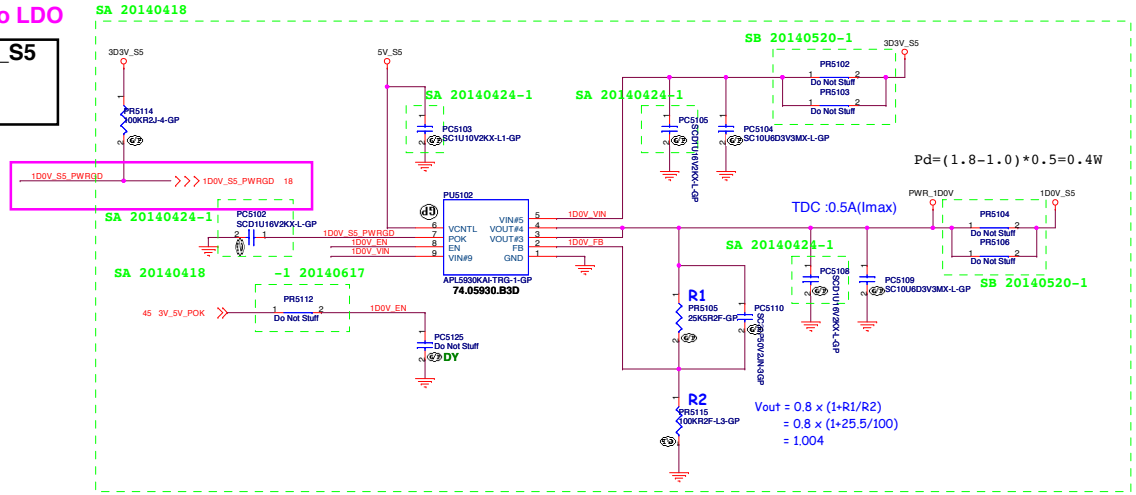
S-1339D15 for 1D5V_S0
Enable=1.0V
Disable=0.25V

modify schematic
Wayler , 2013-0315



20140418 Change to LDO

APL5930 for 1D0V_S5
Enable=1.1V
Disable=0.5V



No eMMC

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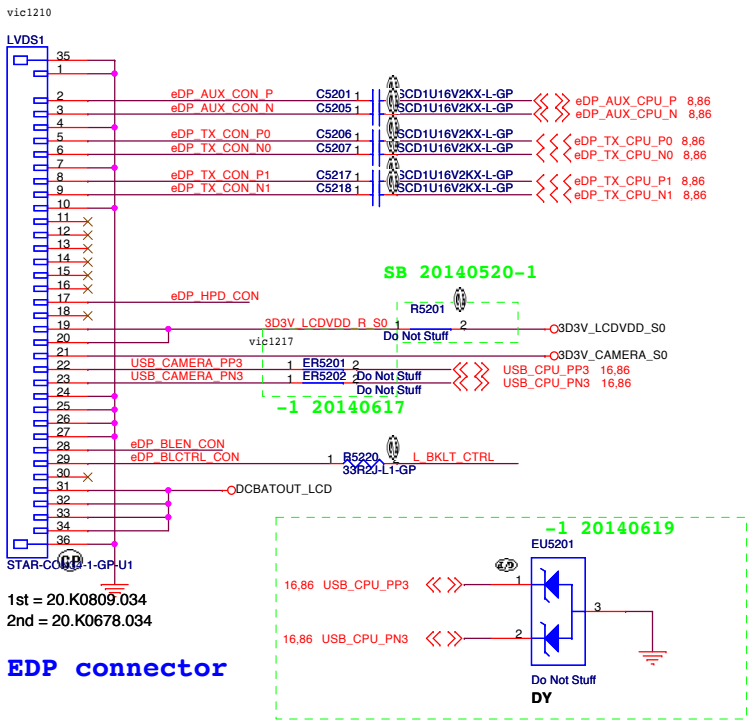
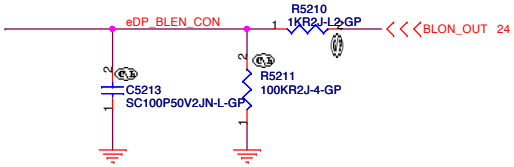
Title: LDO_1D8V&1D5V(SYW232)		
Size: A2	Document Number: EA51_BM	Rev: -1
Date: Tuesday, July 08, 2014	Sheet 51 of 102	

SSID = VIDEO

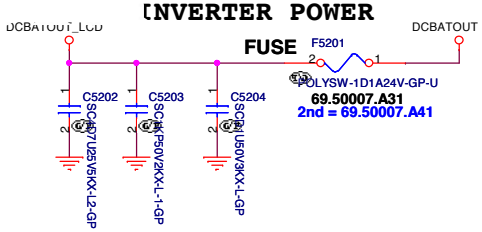


1st = 20.K0809.034
2nd = 20.K0678.034

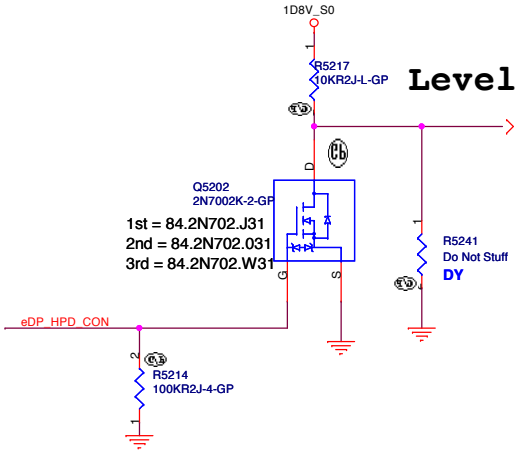
EDP connector



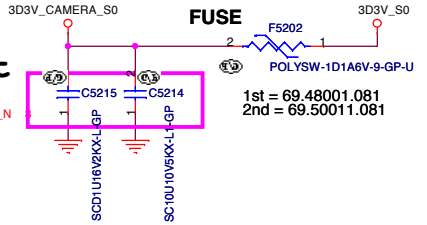
INVERTER POWER



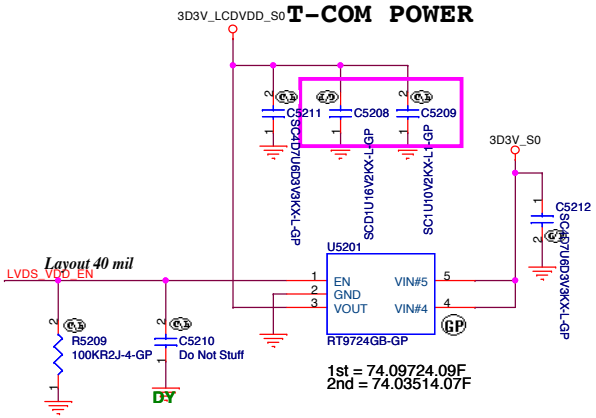
Level shift

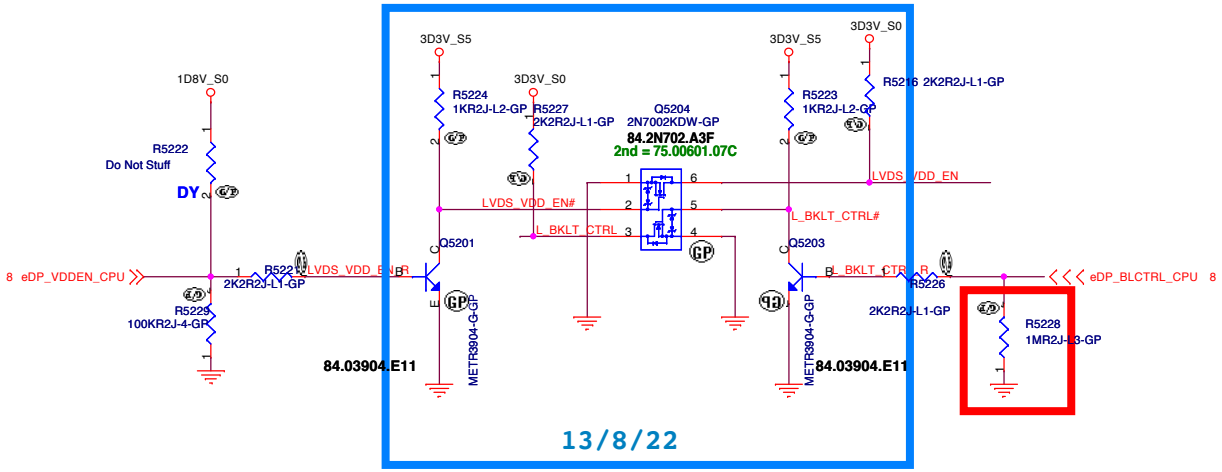


Camera Power



T-COM POWER





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No eMMC

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Title	EDP Connector	
Size A3	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 52 of 102	

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Title

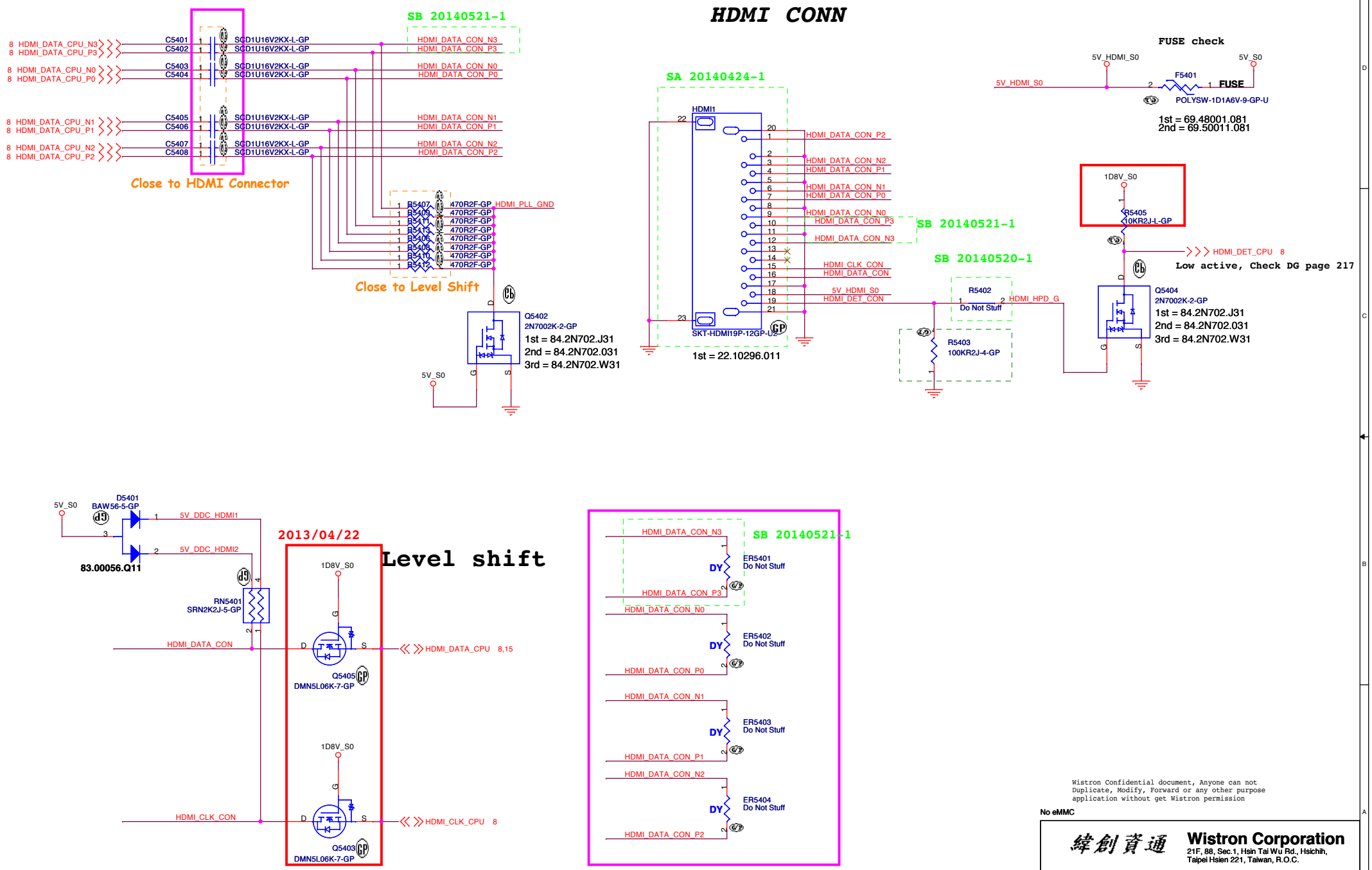
CRT Board Connector

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 53 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: EA30_BM | Rev: -1

Date: Tuesday, July 08, 2014 | Sheet 54 of 102

No eMMC

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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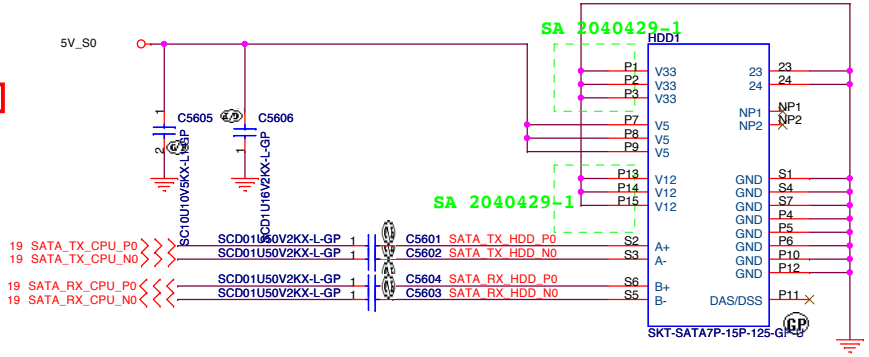
Title: **Display Port**

Size	Document Number	Rev
A3	EA30_BM	-1

SSID = SATA

SATA HDD Connector

SSID = SATA



1st = 22.10300.I11

2nd = 22.10300.891

3rd = 22.10300.991

AC coupling caps near connector<100 mils

No eMMC

緯創資通 Wistron Corporation
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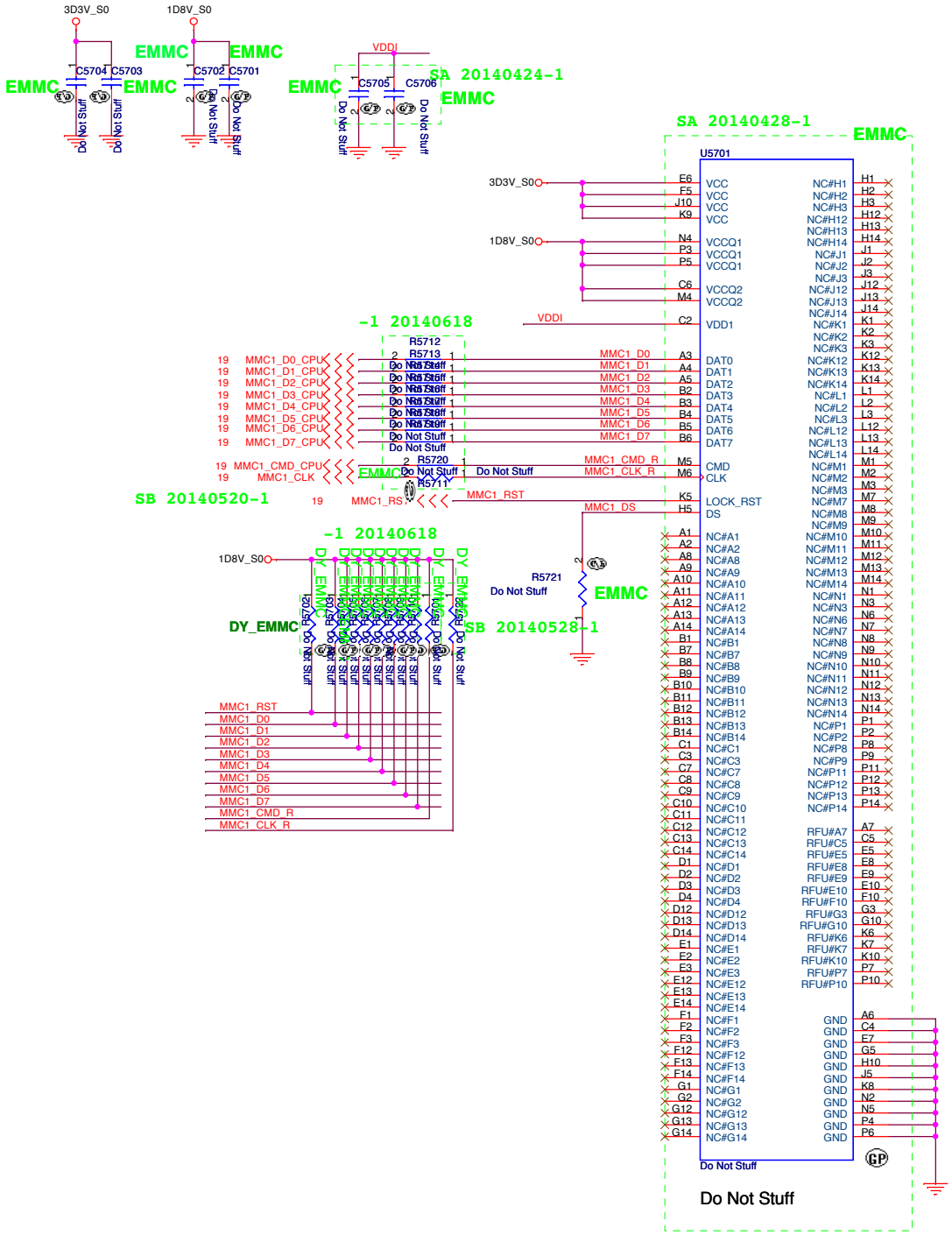
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD / NGFF_SSD

Size	Document Number	Rev
A3	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 56 of 102



No eMMC

緯創資通 Wistron Corporation
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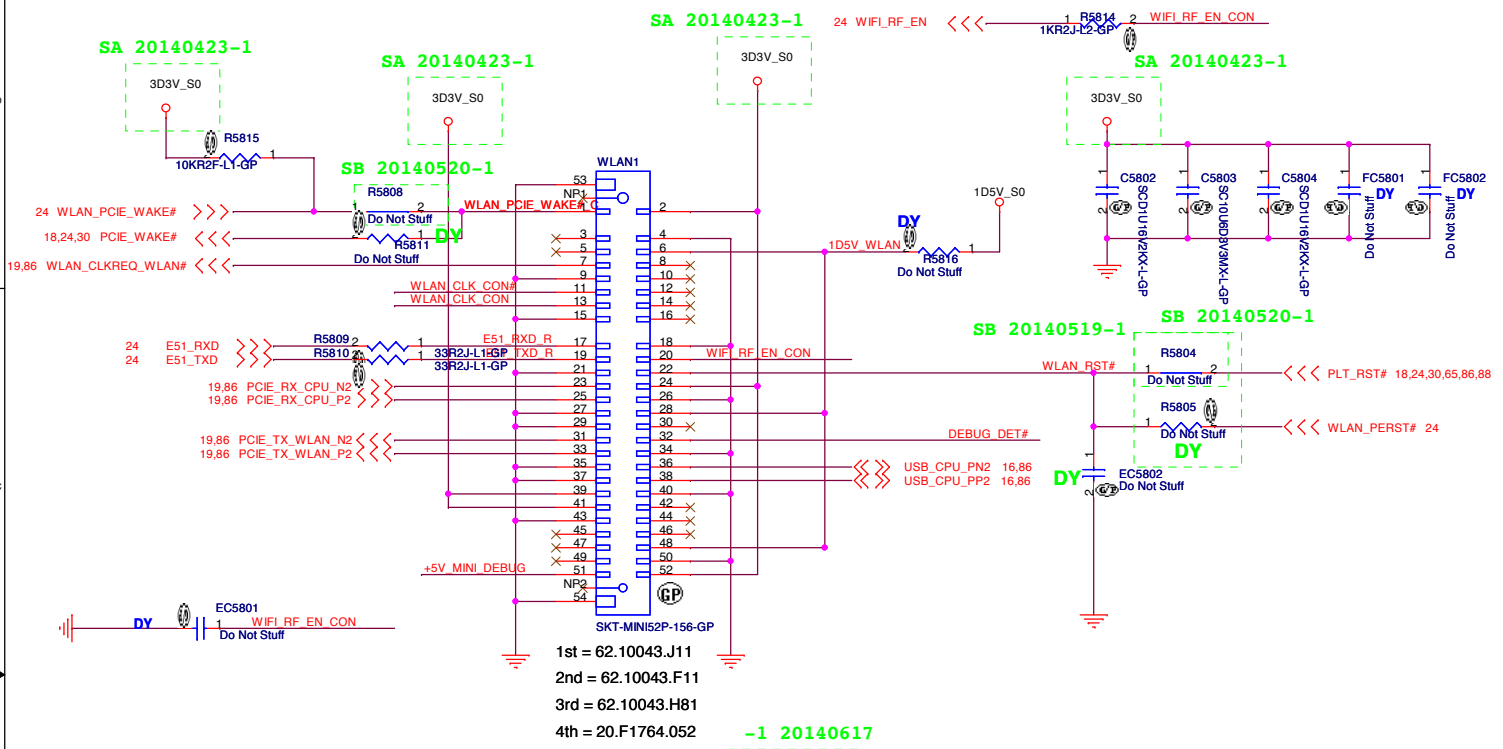
Taipei Hsien 221, Taiwan, R.O.C.

Title: **eMMC**

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 57 of 102

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



No eMMC

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINICARD(WLAN)***
Size A3	Document Number **EA30_BM** Rev **-1**
Date: Tuesday, July 08, 2014	Sheet 58 of 102

SSID = Wireless

Mini Card Connector(mSATA)

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No eMMC

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Title	WWAN CONN	
Size A4	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 59 of 102	

SSID = mSATA

Mini Card Connector(mSATA)

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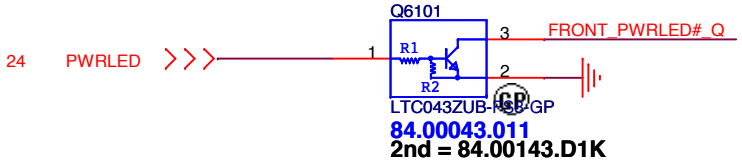
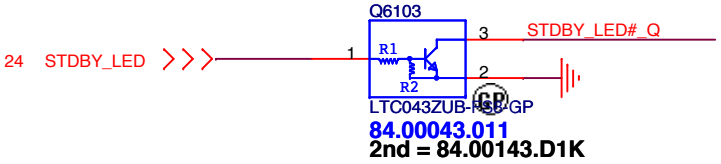
Title	mSATA Connector	
Size A4	Document Number EA30 BM	Rev -1
Date: Tuesday, July 08, 2014	Sheet 60 of 102	

SSID = User.Interface

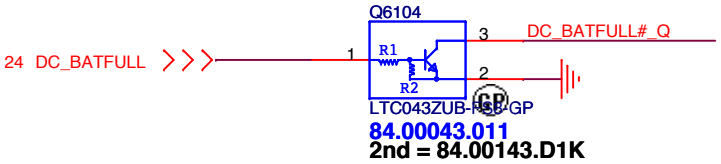
Power button_LED



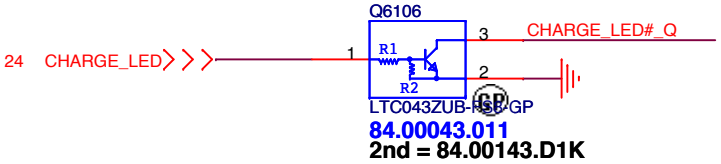
Power STDBY_LED

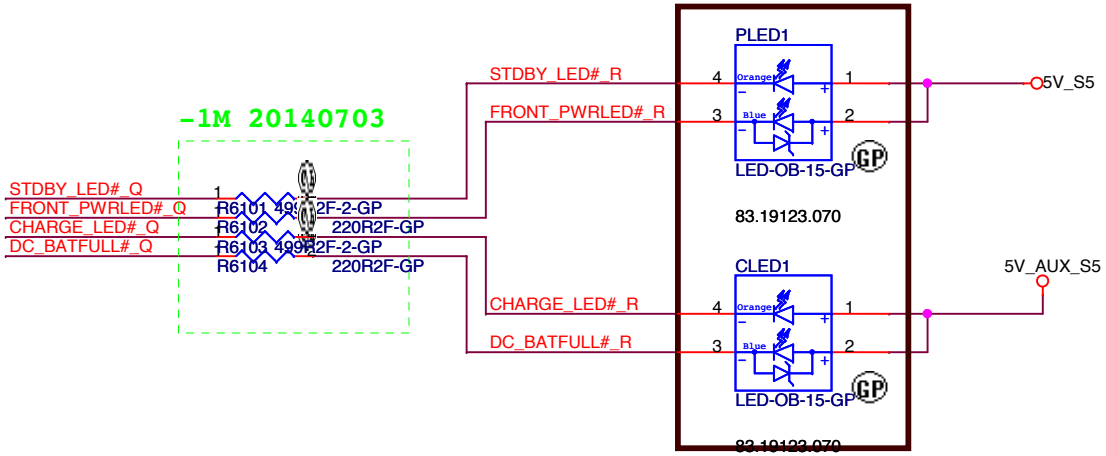


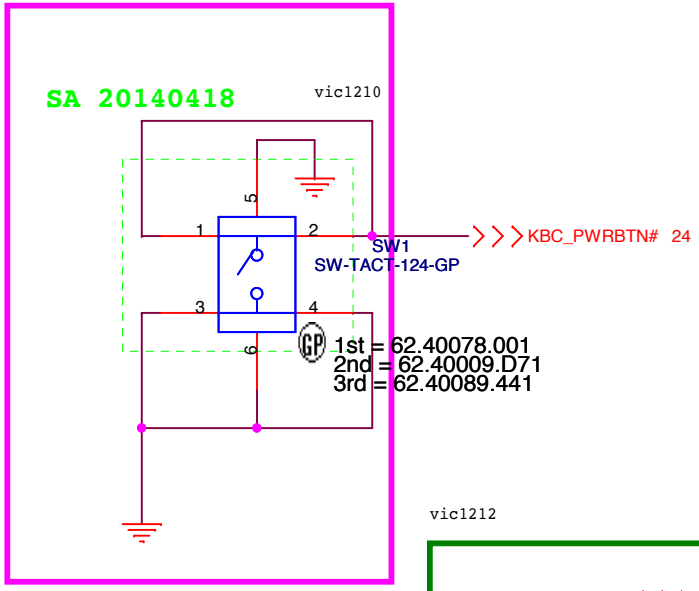
Battery LED2(DC_BATFULL)



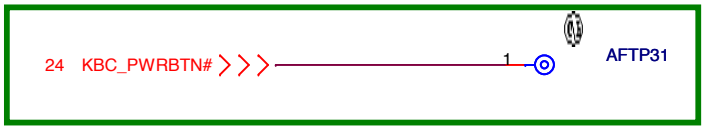
Battery LED1(CHARGE)







vic1212



No eMMC

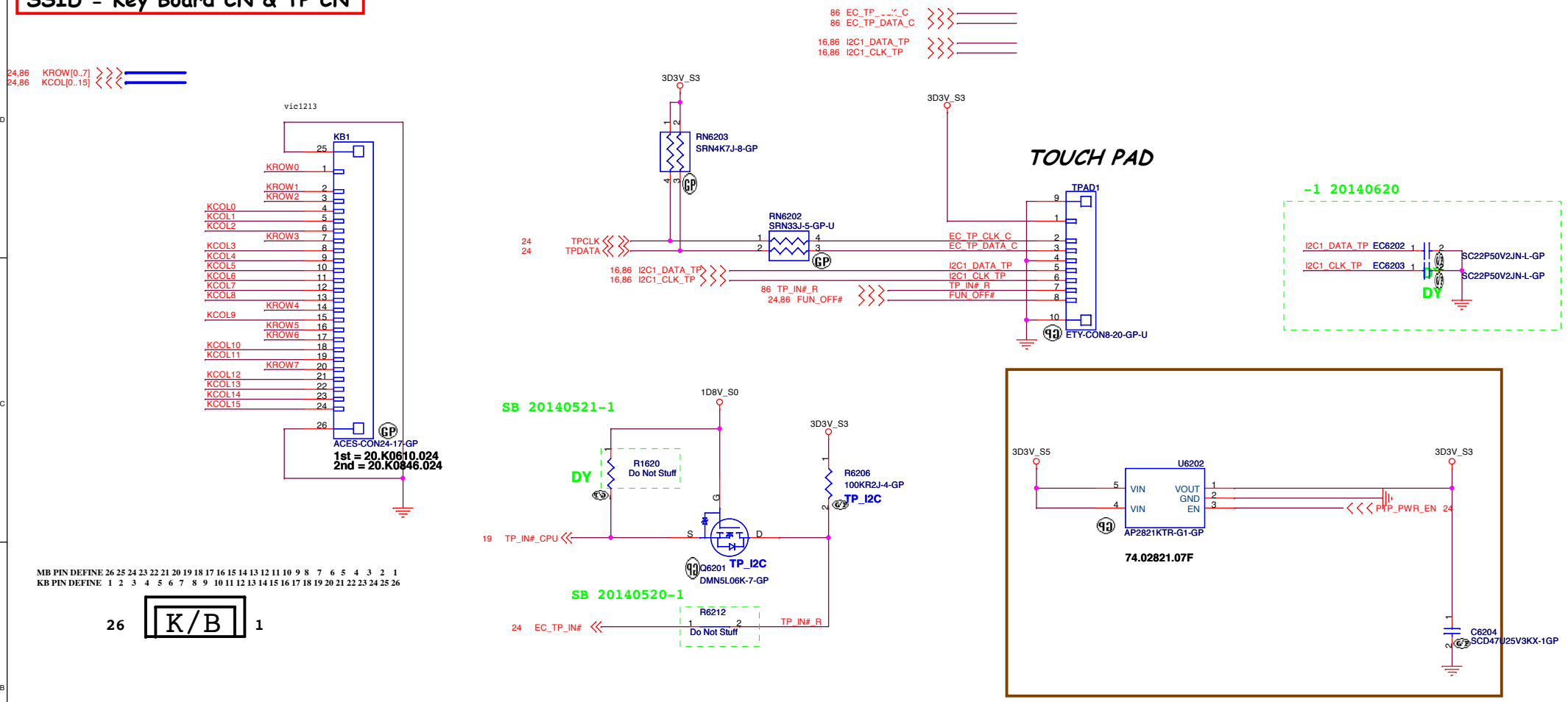
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A4	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 61 of 102

SSID = Key Board CN & TP CN



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

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No eMMC

緯創資通 Wistron Corporation
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Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 62 of 102

vic1211

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No eMMC

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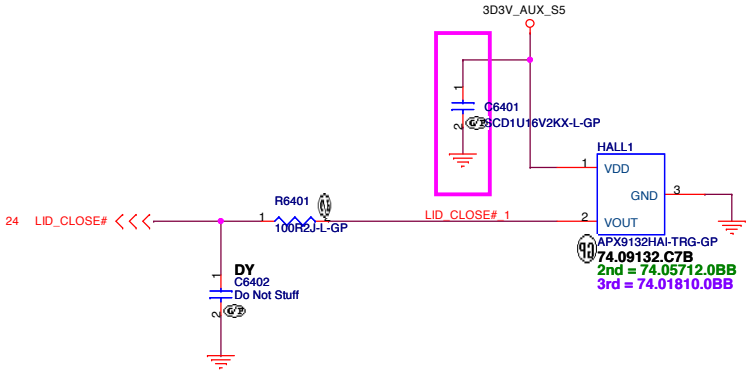
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO Board Connector

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 63 of 102



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No eMMC

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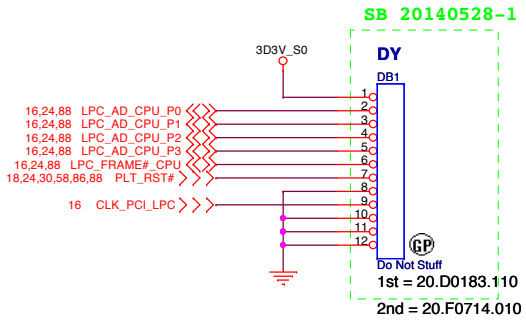
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 64 of 102



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No eMMC

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **Dubug connector**

Size	Document Number	Rev
A3	EA30_BM	-1

Date: Tuesday, July 08, 2014 Sheet 65 of 102

(Blanking)

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No eMMC

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR HUB

Size	Document Number	Rev
A3	EA30 BM	-1

Date: Tuesday, July 08, 2014 Sheet 66 of 102

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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No eMMC

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Title	G Sensor	
Size A	Document Number EA30_BM	Rev -1
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Title: *Thunderbolt (1/5)*

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GPU(PEG)

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GPU (DIGITALOUT)

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Title: ***GPU (VRAM I/F)***

Size	Document Number	Rev
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Size: Custom / Document Number	EA30 BM
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Title: GPU (POWER/GND)

Size	Document Number	Rev
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GPU-VRAM1,2 (1/4)

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Title: GPU-VRAM3,4 (2/4)

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GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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Title

RT8812A_VGA_CORE

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Title: **DISCRETE VGA POWER**

Size	Document Number	Rev
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Switchable GFX LCD(1/2)

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Switchable GFX LCD(2/2)

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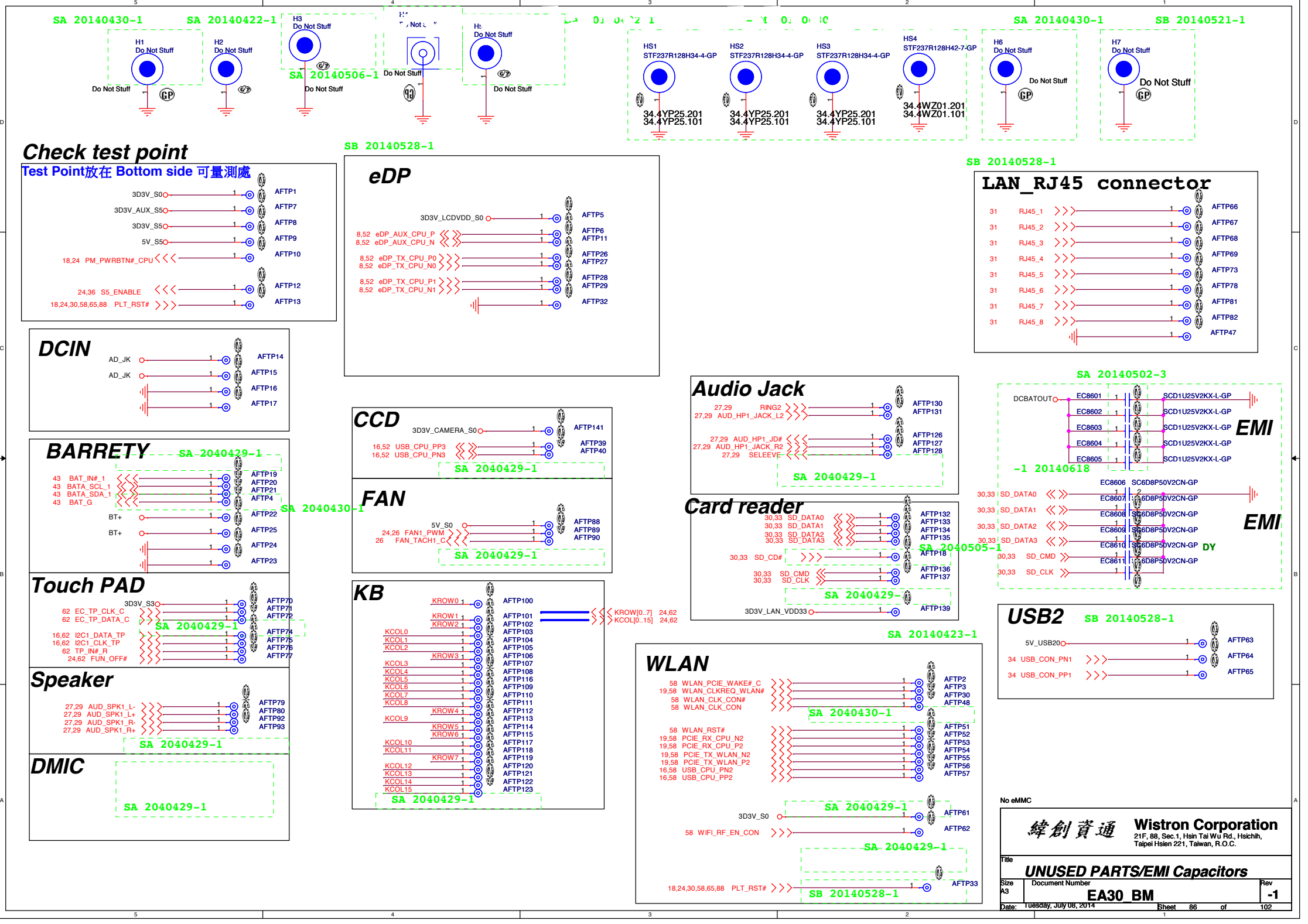
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SA 20140422-1
H1
Do Not Stuff
H2
Do Not Stuff
H3
Do Not Stuff
SA 20140506-1
Do Not Stuff
Do Not Stuff
Do Not Stuff
Do Not Stuff
Do Not Stuff
HS1
STF237R128H34-4-GP
HS2
STF237R128H34-4-GP
HS3
STF237R128H34-4-GP
HS4
STF237R128H42-7-GP
34.4YP25.201
34.4YP25.101
34.4YP25.201
34.4YP25.101
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34.4YP25.101
34.4WZ01.201
34.4WZ01.101
SA 20140430-1
SB 20140521-1
H6
Do Not Stuff
Do Not Stuff
H7
Do Not Stuff
Do Not Stuff
Check test point
Test Point放在 Bottom side 可量測處
3D3V_S0 AFTP1
3D3V_AUX_S5 AFTP7
3D3V_S5 AFTP8
5V_S5 AFTP9
18,24 PM_PWRBTN#_CPU AFTP10
24,36 S5_ENABLE AFTP12
18,24,30,58,65,88 PLT_RST# AFTP13
SB 20140528-1
eDP
3D3V_LCDVDD_S0 AFTP5
8,52 eDP_AUX_CPU_P AFTP6
8,52 eDP_AUX_CPU_N AFTP11
8,52 eDP_TX_CPU_P0 AFTP26
8,52 eDP_TX_CPU_N0 AFTP27
8,52 eDP_TX_CPU_P1 AFTP28
8,52 eDP_TX_CPU_N1 AFTP29
AFTP32
SB 20140528-1
LAN_RJ45 connector
31 RJ45_1 AFTP66
31 RJ45_2 AFTP67
31 RJ45_3 AFTP68
31 RJ45_4 AFTP69
31 RJ45_5 AFTP73
31 RJ45_6 AFTP78
31 RJ45_7 AFTP81
31 RJ45_8 AFTP82
AFTP47
DCIN
AD_JK AFTP14
AD_JK AFTP15
AFTP16
AFTP17
BARRETY
SA 2040429-1
43 BAT_IN#_1 AFTP19
43 BATA_SCL_1 AFTP20
43 BATA_SDA_1 AFTP21
43 BAT_G AFTP4
SA 2040430-1
BT+ AFTP22
BT+ AFTP25
AFTP24
AFTP23
CCD
3D3V_CAMERA_S0 AFTP141
16,52 USB_CPU_PP3 AFTP39
16,52 USB_CPU_PN3 AFTP40
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FAN
5V_S0 AFTP88
24,26 FAN1_PWM AFTP89
26 FAN_TACH1_C AFTP90
SA 2040429-1
Audio Jack
27,29 RING2 AFTP130
27,29 AUD_HP1_JACK_L2 AFTP131
27,29 AUD_HP1_JD# AFTP126
27,29 AUD_HP1_JACK_R2 AFTP127
27,29 SELEEVE AFTP128
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SA 20140502-3
DCBATOUT
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EC8602 SCD1U25V2KX-L-GP
EC8603 SCD1U25V2KX-L-GP
EC8604 SCD1U25V2KX-L-GP
EC8605 SCD1U25V2KX-L-GP
EMI
-1 20140618
EC8606 SC6D8P50V2CN-GP
30,33 SD_DATA0
EC8607 SC6D8P50V2CN-GP
30,33 SD_DATA1
EC8608 SC6D8P50V2CN-GP
30,33 SD_DATA2
EC8609 SC6D8P50V2CN-GP
30,33 SD_DATA3
EC8610 SC6D8P50V2CN-GP
DY
30,33 SD_CMD
EC8611 SC6D8P50V2CN-GP
30,33 SD_CLK
EMI
Card reader
30,33 SD_DATA0 AFTP132
30,33 SD_DATA1 AFTP133
30,33 SD_DATA2 AFTP134
30,33 SD_DATA3 AFTP135
SA 2040505-1
30,33 SD_CD# AFTP18
30,33 SD_CMD AFTP136
30,33 SD_CLK AFTP137
SA 2040429-
3D3V_LAN_VDD33 AFTP139
Touch PAD
3D3V_S3 AFTP70
62 EC_TP_CLK_C AFTP71
62 EC_TP_DATA_C AFTP72
SA 2040429-1
16,62 I2C1_DATA_TP AFTP74
16,62 I2C1_CLK_TP AFTP75
62 TP_IN#_R AFTP76
24,62 FUN_OFF# AFTP77
KB
KROW0 AFTP100
KROW1 AFTP101
KROW2 AFTP102
KCOL0 AFTP103
KCOL1 AFTP104
KCOL2 AFTP105
KROW3 AFTP106
KCOL3 AFTP107
KCOL4 AFTP108
KCOL5 AFTP116
KCOL6 AFTP109
KCOL7 AFTP110
KCOL8 AFTP111
KROW4 AFTP112
KCOL9 AFTP113
KROW5 AFTP114
KROW6 AFTP115
KCOL10 AFTP117
KCOL11 AFTP118
KROW7 AFTP119
KCOL12 AFTP120
KCOL13 AFTP121
KCOL14 AFTP122
KCOL15 AFTP123
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KCOL[0..15] 24,62
USB2
SB 20140528-1
5V_USB20 AFTP63
34 USB_CON_PN1 AFTP64
34 USB_CON_PP1 AFTP65
Speaker
27,29 AUD_SPK1_L- AFTP79
27,29 AUD_SPK1_L+ AFTP80
27,29 AUD_SPK1_R- AFTP92
27,29 AUD_SPK1_R+ AFTP93
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DMIC
SA 2040429-1
SA 20140423-1
WLAN
58 WLAN_PCIE_WAKE#_C AFTP2
19,58 WLAN_CLKREQ_WLAN# AFTP3
58 WLAN_CLK_CON# AFTP30
58 WLAN_CLK_CON AFTP48
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58 WLAN_RST# AFTP51
19,58 PCIE_RX_CPU_N2 AFTP52
19,58 PCIE_RX_CPU_P2 AFTP53
19,58 PCIE_TX_WLAN_N2 AFTP54
19,58 PCIE_TX_WLAN_P2 AFTP55
16,58 USB_CPU_PN2 AFTP56
16,58 USB_CPU_PP2 AFTP57
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3D3V_S0 AFTP61
58 WIFI_RF_EN_CON AFTP62
SA 2040429-1
18,24,30,58,65,88 PLT_RST# AFTP33
SB 20140528-1
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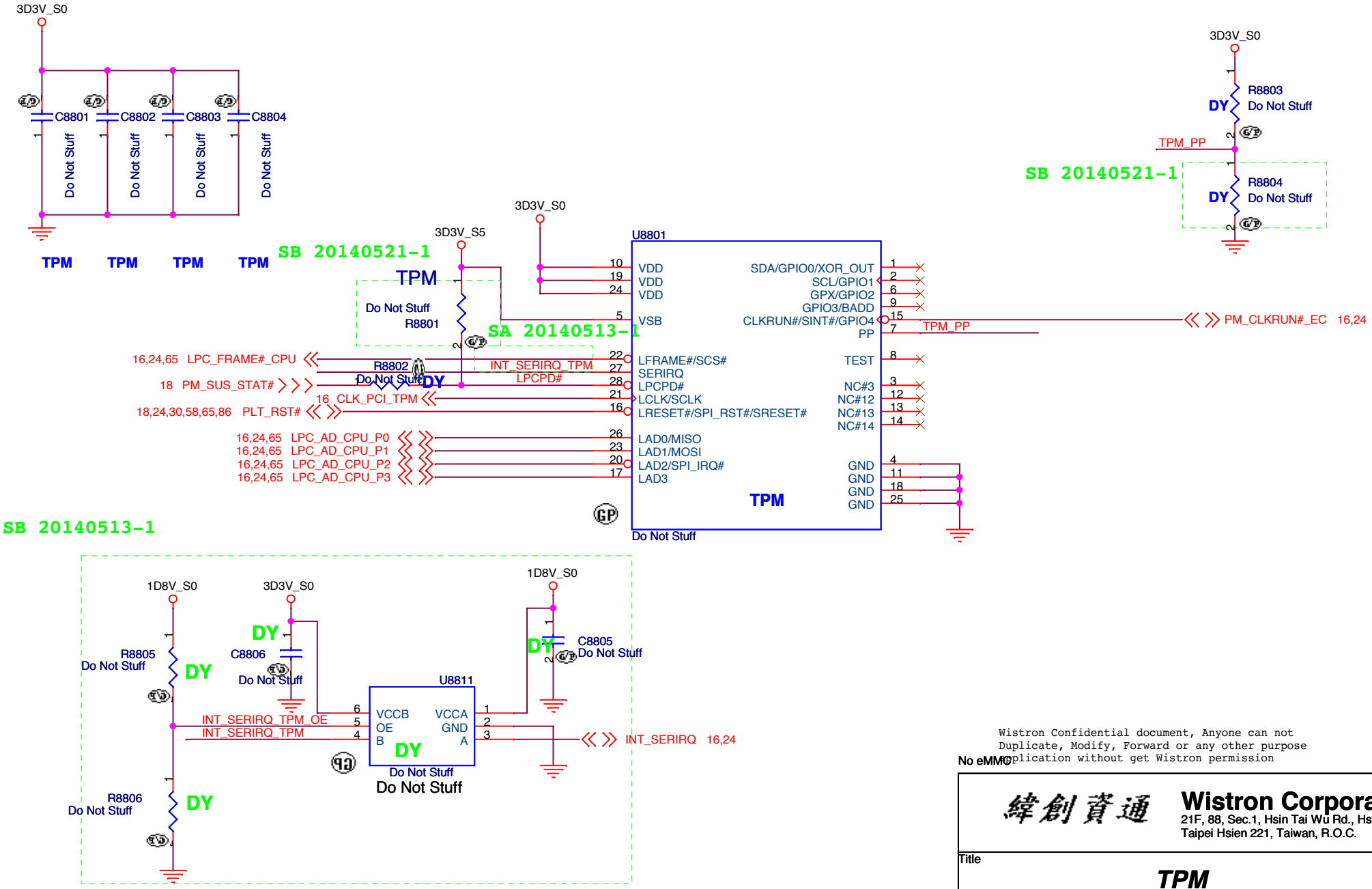

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Smart Card socket

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Switchable GFX eDP

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Bottom Docking

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LAN Switch

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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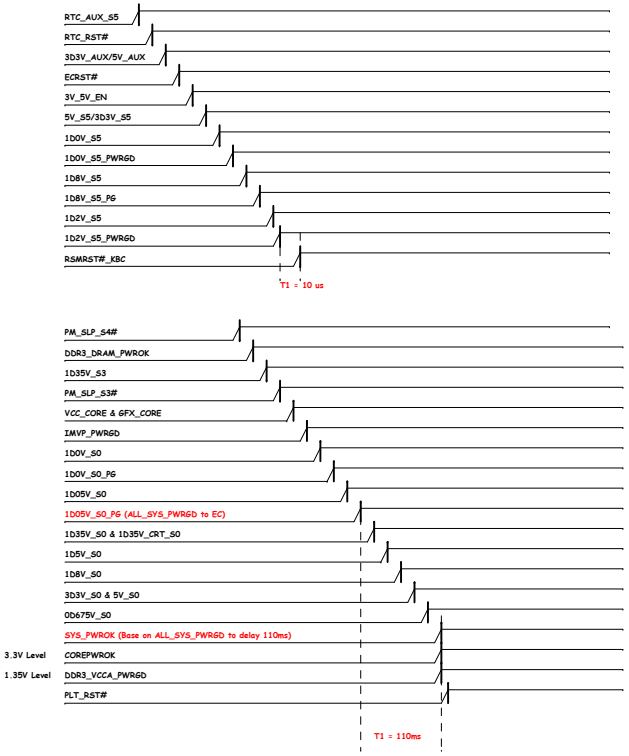
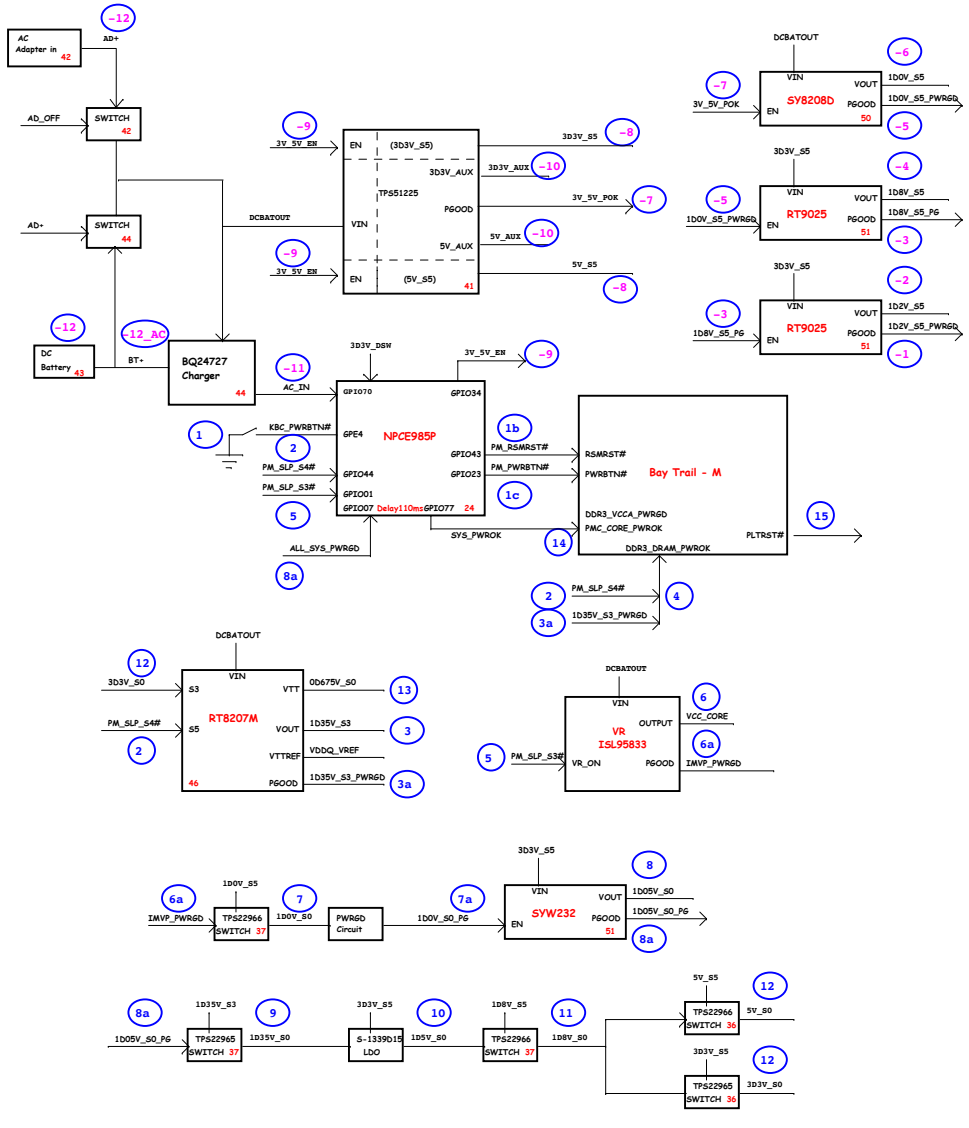
Intel-Power Up Sequence with non-S0ix



Bay Trail - M POWER UP SEQUENCE DIAGRAM



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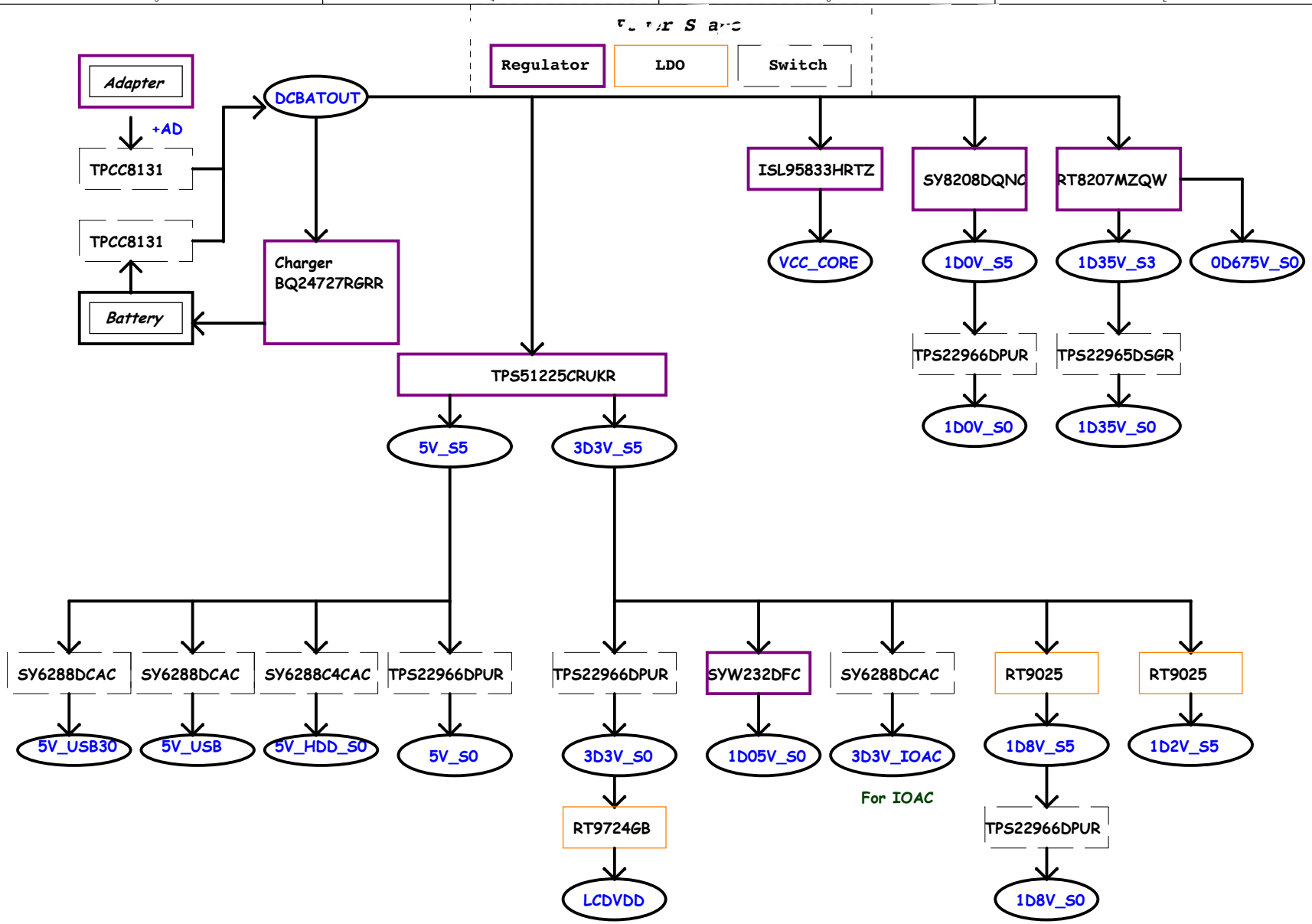

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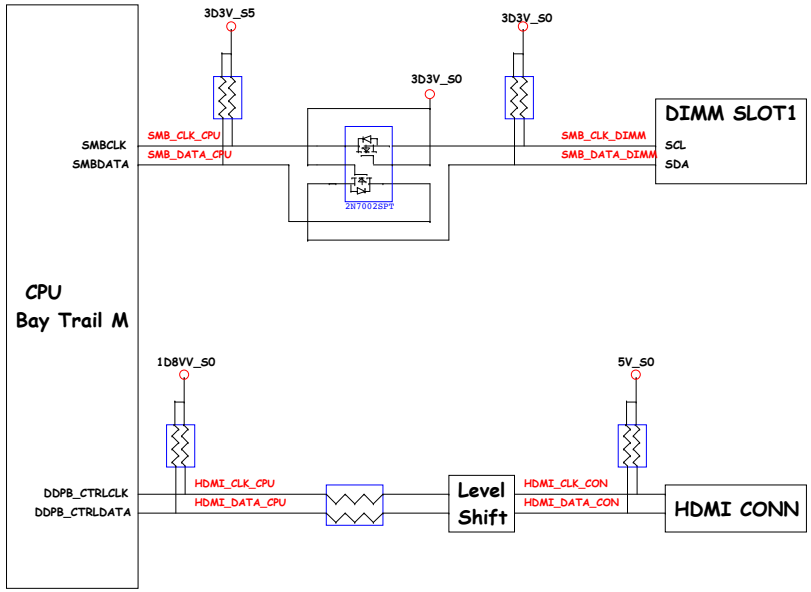
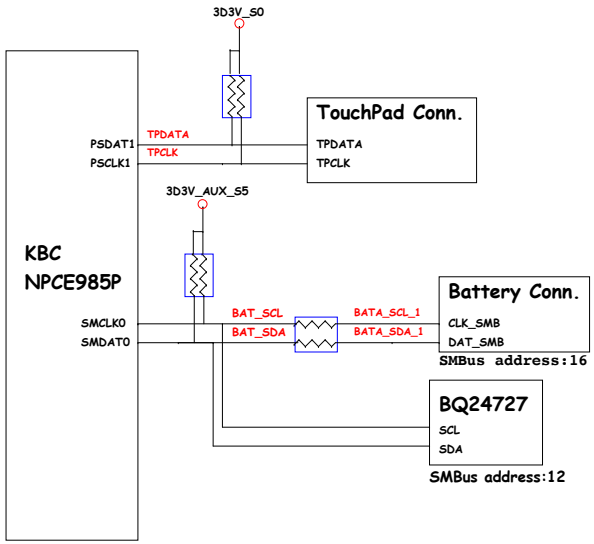
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title	SMBUS BLOCK DIAGRAM	
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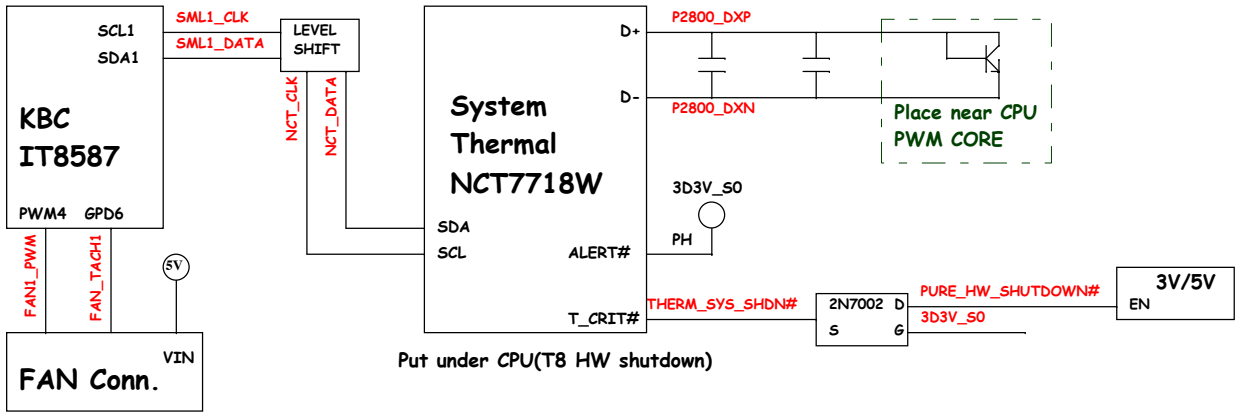
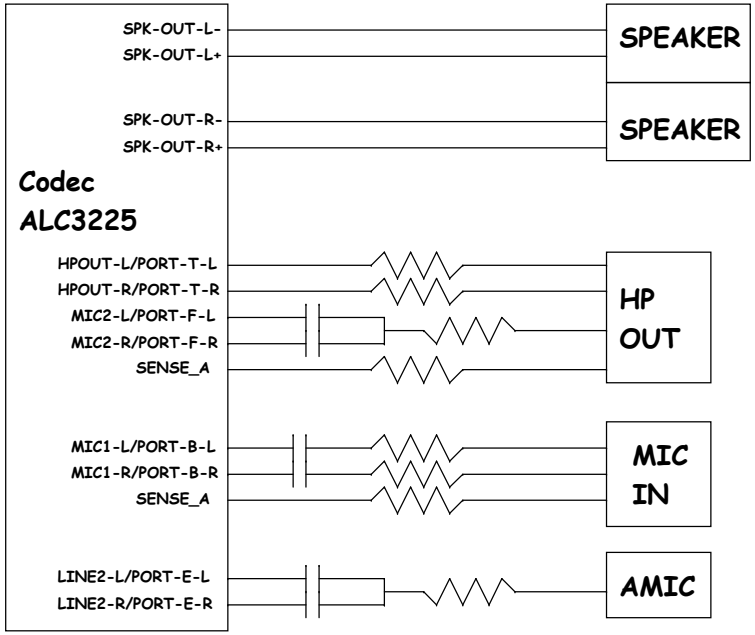
Thermal Block Diagram



Audio Block Diagram



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