Compal Confidential

Schematics Document

Intel Huron River

Sandy Bridge with Couger Point core logic

2010-10-27

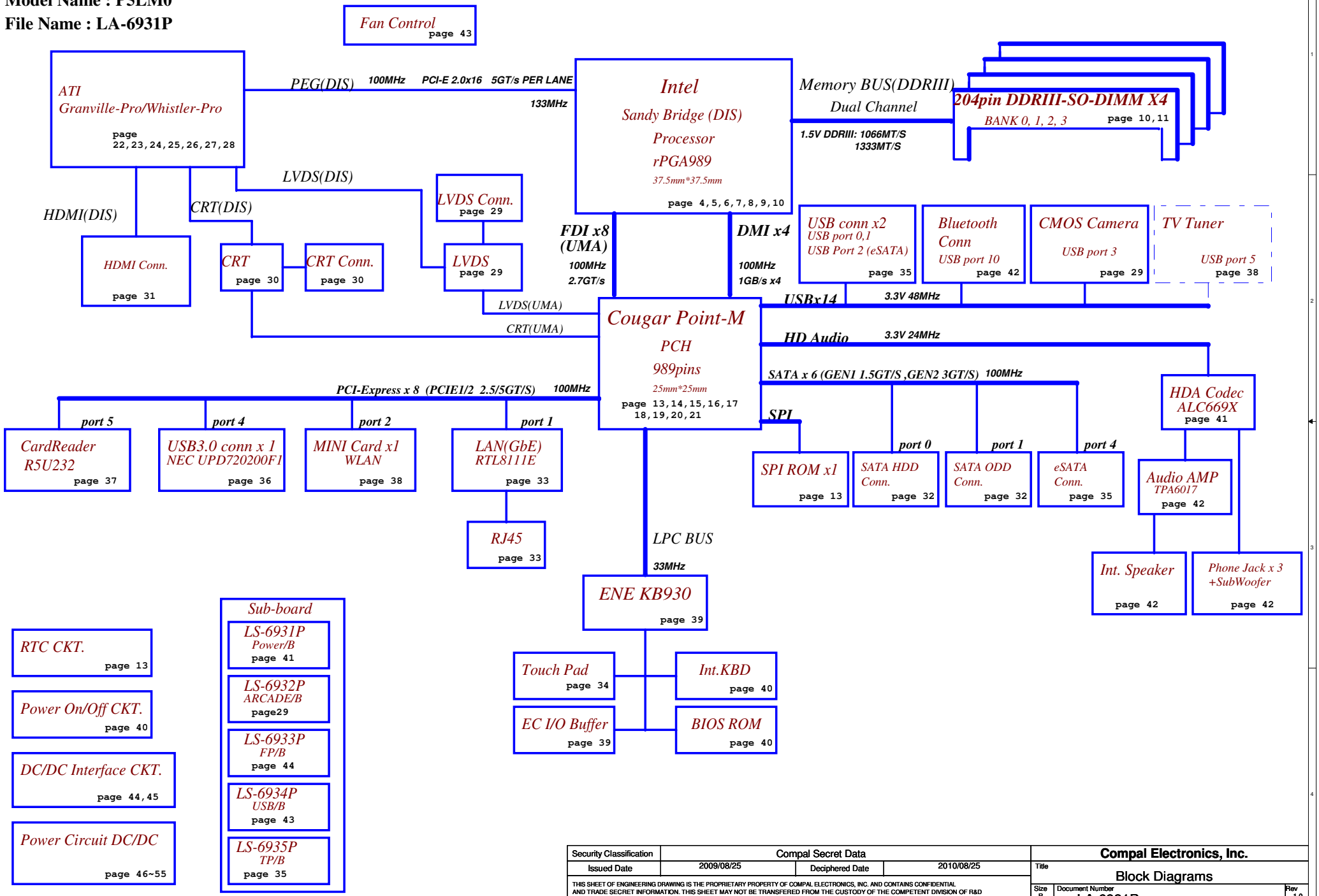
REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-6931P	Rev: 1.0
Date: Wednesday, October 27, 2010	Sheet 1 of 58	

Compal Confidential

Model Name : P5LM0
File Name : LA-6931P



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Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
B	LA-6931P	1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (DIS)	IGPU (SG)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS_VCCP	1.05V switched power rail for CPU (PCH)	ON	OFF	OFF		
+VGFX_CORE	Core voltage for IGPU	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3VALW_PCH	3.3V power rail for PCH	ON	ON	ON*		
+LAN_IO	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+VGA_CORE	5V power rail for GPU	ON	OFF	OFF	ON	OFF
+1.5VSDGPU	1.5V power rail for VRAM	ON	OFF	OFF	ON	OFF
+1.8VSDGPU	1.8V switched power rail for GPU	ON	OFF	OFF	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
* 3	0.4
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIS Only	DIS@
Switchable Graphics	SG@
Granville	GRA@
Whistler	WHI@
For CIR	CIR@
USB2.0 bus	USB2@
DDR M1	M1@
DDR M3	M3@
For 45 level	45@

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB/B
		1	USB Conn.
	UHCI1	2	
		3	
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	eSATA USB
	UHCI5	10	CMOS Camera
		11	Finger Print
	UHCI6	12	USB3.0 @
		13	Blue Tooth

43 Level BOM Config

Granville DIS: GRA@ DIS@ CIR@ M1@
Whistler SG: WHI@ SG@ CIR@ M1@

45 Level BOM Config

45@

VRAM BOM Config

X76255BOL01: HYNIX 1G (old die)
X76255BOL02 HYNIX 1G (new die)
X76255BOL04 HYNIX 2G

Compal Electronics, Inc.
Title: Notes List
Size: B | Document Number: LA-6931P | Rev: 1.0
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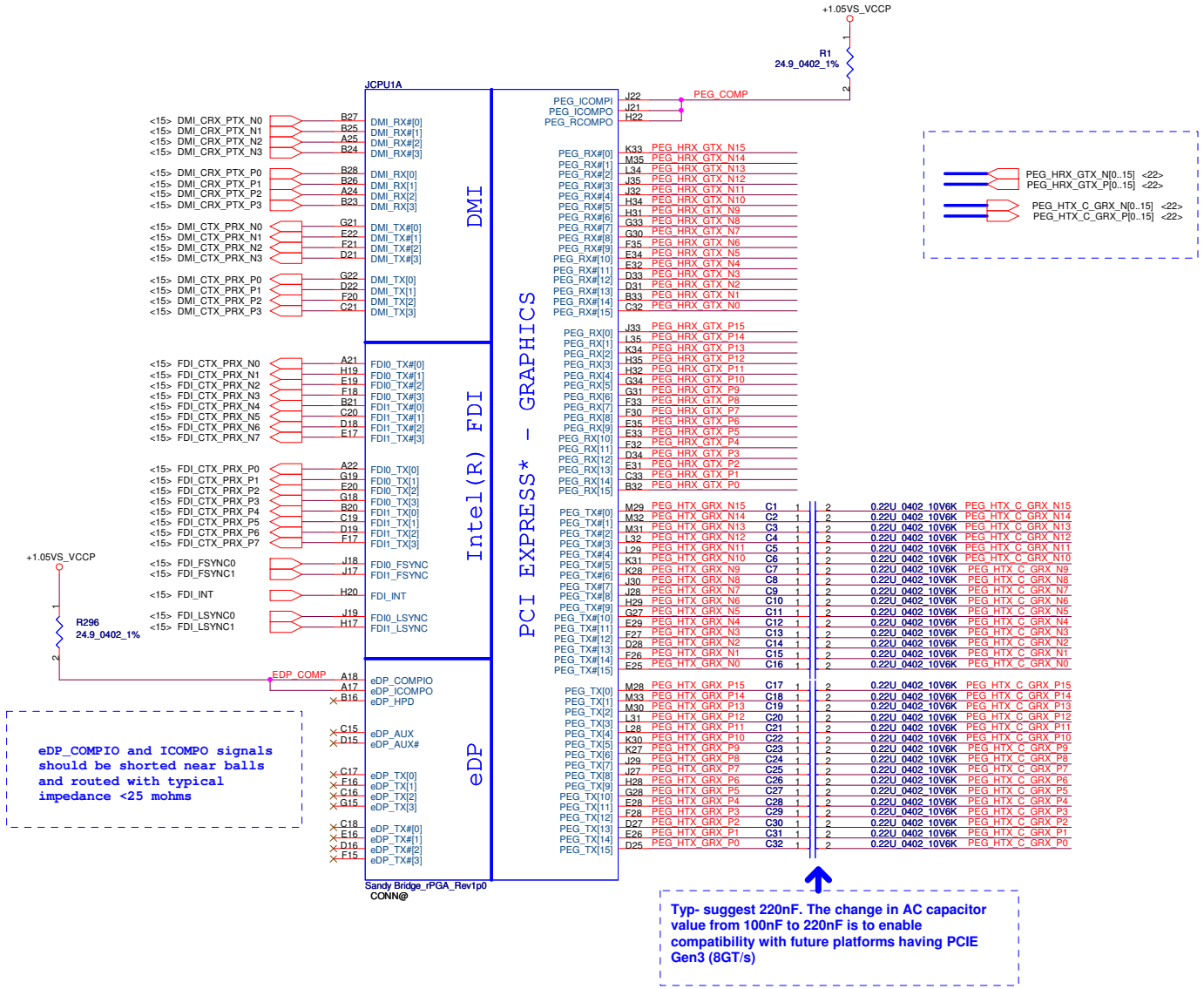

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

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Processor Pullups

+1.05VS_VCCP

R6 2 1 62_0402_5% H_PROCHOT#

R8 2 1 10K_0402_5% H_CPUPWRGD_R

C916 2 1 220P_0402_50V7K

10/11

For ESD

JCPU1B

<17> H_SNB_IVB# → C26 PROC_SELECT#

AN34 SKTOCC#

MISC

T1 PAD H_CATERR# AL33 CATERR#

R7 0_0402_5%

<18,40> H_PECI 1 2 H_PECI_ISO AN33 PECI

R9 56_0402_5%

<40,50> H_PROCHOT# 1 2 H_PROCHOT#_R AL32 PROCHOT#

R10 0_0402_5%

<18> H_THRMTRIP# 1 2 H_THEMTRIP#_R AN32 THERMTRIP#

THERMAL

R11 0_0402_5%

<15> H_PM_SYNC 1 2 H_PM_SYNC_R AM34 PM_SYNC

R15 0_0402_5%

<18> H_CPUPWRGD 1 2 H_CPUPWRGD_R AP33 UNCOREPWRGOOD

R18 130_0402_5%

PM_SYS_PWRGD_BUF 1 2 PM_DRAM_PWRGD_R V8 SM_DRAMPWROK

BUF_CPU_RST# AR33 RESET#

PWR MANAGEMENT

Sandy Bridge_rPGA_Rev1p0

CONN@

CLOCKS

BCLK A28 CLK_CPU_DMI_R R2 1 2 0_0402_5% CLK_CPU_DMI <14>

BCLK# A27 CLK_CPU_DMII#_R R3 1 2 0_0402_5% CLK_CPU_DMI# <14>

DPLL_REF_CLK A16 CLK_DP_R R4 1 2 0_0402_5% CLK_DP <14>

DPLL_REF_CLK# A15 CLK_DP#_R R5 1 2 0_0402_5% CLK_DP# <14>

DDR3 MISC

SM_DRAMRST# R8 H_DRAMRST# <6>

SM_RCOMP[0] AK1 SM_RCOMP0

SM_RCOMP[1] A5 SM_RCOMP1

SM_RCOMP[2] A4 SM_RCOMP2

JTAG & BPM

PRDY# AP29 XDP_PRDY# PAD T31

PREQ# AP27 XDP_PREQ# PAD T32

TCK AR26 XDP_TCK PAD T33

TMS AR27 XDP_TMS PAD T38

TRST# AP30 XDP_TRST# R902 2 1 51_0402_5% +1.05VS_VCCP

TDI AR28 PAD T39

TDO AR26 XDP_TDO R25 2 1 51_0402_5%

DBR# AL35 XDP_DBRESET# XDP_DBRESET# <15>

BPM#[0] AT28 XDP_BPM#0 PAD T40

BPM#[1] AR29 XDP_BPM#1 PAD T42

BPM#[2] AR30 XDP_BPM#2 PAD T44

BPM#[3] AT30 XDP_BPM#3 PAD T46

BPM#[4] AP32 XDP_BPM#4 PAD T47

BPM#[5] AR31 XDP_BPM#5 PAD T48

BPM#[6] AT31 XDP_BPM#6 PAD T49

BPM#[7] AR32 XDP_BPM#7 PAD T50

Buffered reset to CPU

+3VS

C35 0.1U_0402_16V4Z

U1 SN74LVC1G07DCKR_SC70-5

<17,34,37,39,40> PLT_RST# PLT_RST#

BUFO_CPU_RST#

+1.05VS_VCCP

R13 75_0402_5%

R17 43_0402_1%

BUF_CPU_RST#

@ R19 0_0402_5%

+3VS

+3VALW

C36 0.1U_0402_16V4Z

U3 74AHC1G09GW_TSSOP5

R29 10K_0402_5%

<15> PM_DRAM_PWRGD

PM_SYS_PWRGD_BUF

+1.5V_CPU_VDDQ

R26 200_0402_5%

@ R30 39_0402_5%

<45,53> SUSP SUSP

@ Q1 2N7002H_SOT23-3

10/18 Remove XDP Connector

DDR3 Compensation Signals

SM_RCOMP0 R20 2 1 140_0402_1%

SM_RCOMP1 R21 2 1 25.5_0402_1%

SM_RCOMP2 R22 2 1 200_0402_1%

+3VS

XDP_DBRESET# R31 2 1 1K_0402_5%

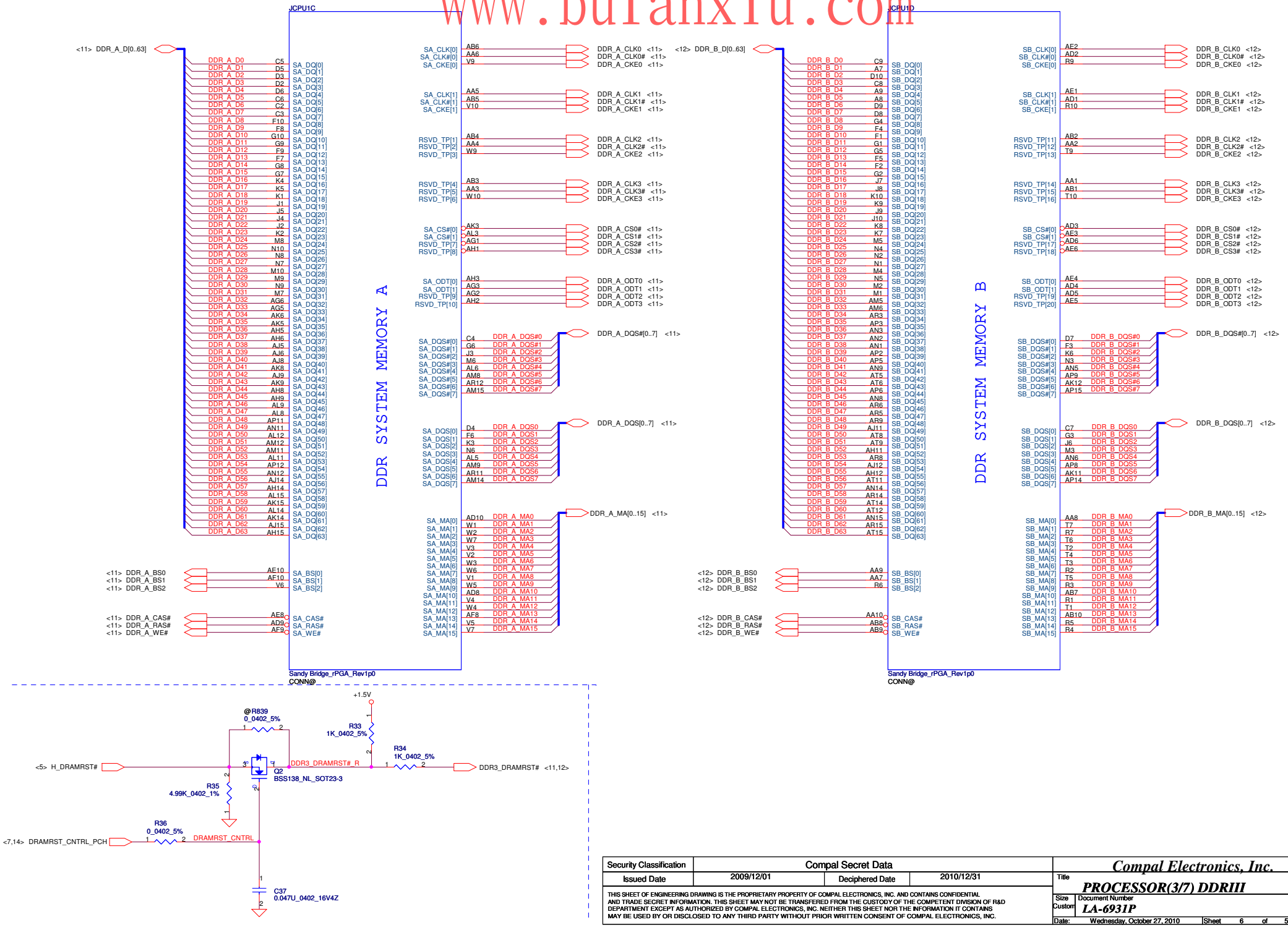
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 5 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-6931P	1.0

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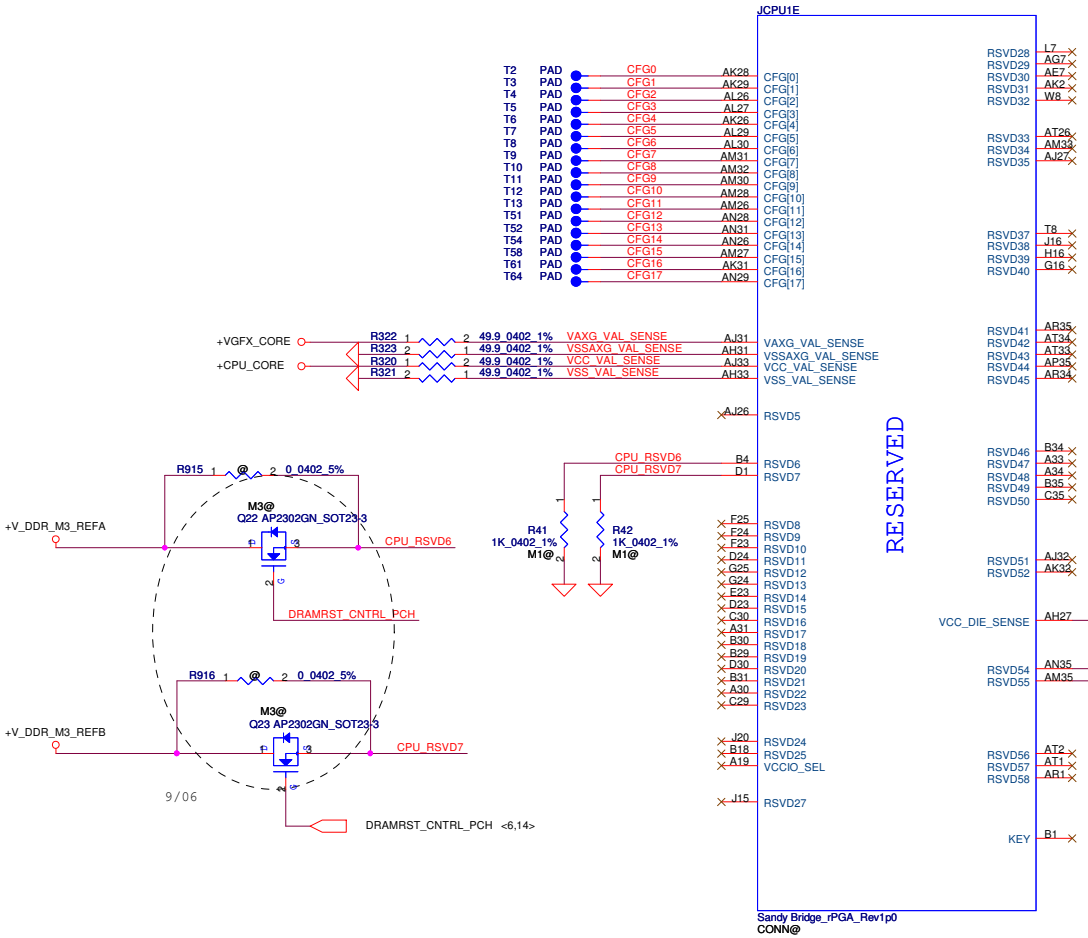
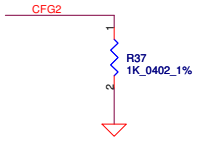
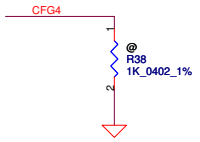
CFG Straps for Processor

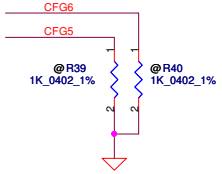




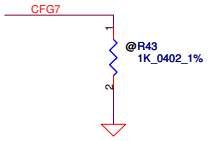
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Title	Compal Electronics, Inc. PROCESSOR(4/7) RSVD,CFG
Size	Custom
Document Number	LA-6931P
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POWER

SV type CPU

JCPU1E

53A

18A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Bottom Socket Cavity

Top Socket Cavity

Top Socket Edge

Bottom Socket Edge

MB Bottom Socket Cavity

MB Top Socket Cavity

+CPU_CORE

+1.05VS_VCCP

VIDALERT#
VIDSCLK
VIDSOUT

VR_SVID_ALRT# <56>
VR_SVID_CLK <56>
VR_SVID_DAT <56>

Place the PU resistors close to VR

Place the PU resistors close to CPU

VCC_SENSE
VSS_SENSE

VCCSENSE <56>
VSSSENSE <56>

VCCIO_SENSE
VSSIO_SENSE

VCCIO_SENSE <53>
VSSIO_SENSE <53>

09/10

Sandy Bridge rPGA Rev1p0

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: LA-6931P | Rev: 1.0

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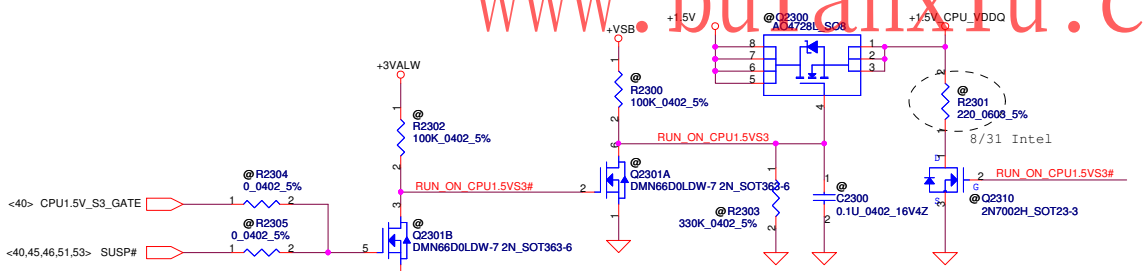
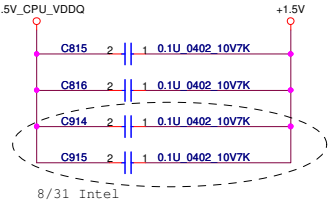
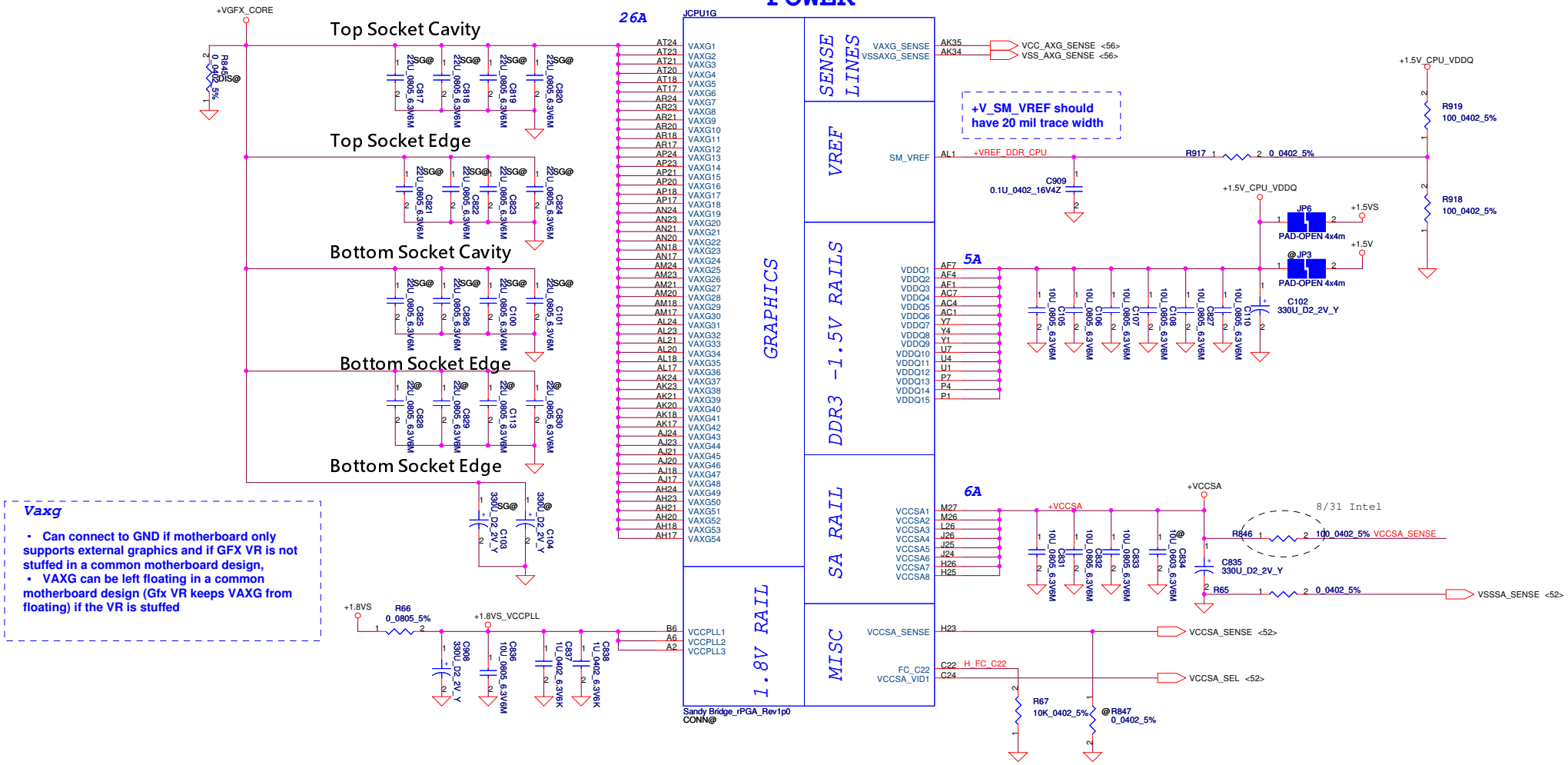
+1.5V_CPU_VDDQ Source





POWER



Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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Title	PROCESSOR(6/7) PWR		
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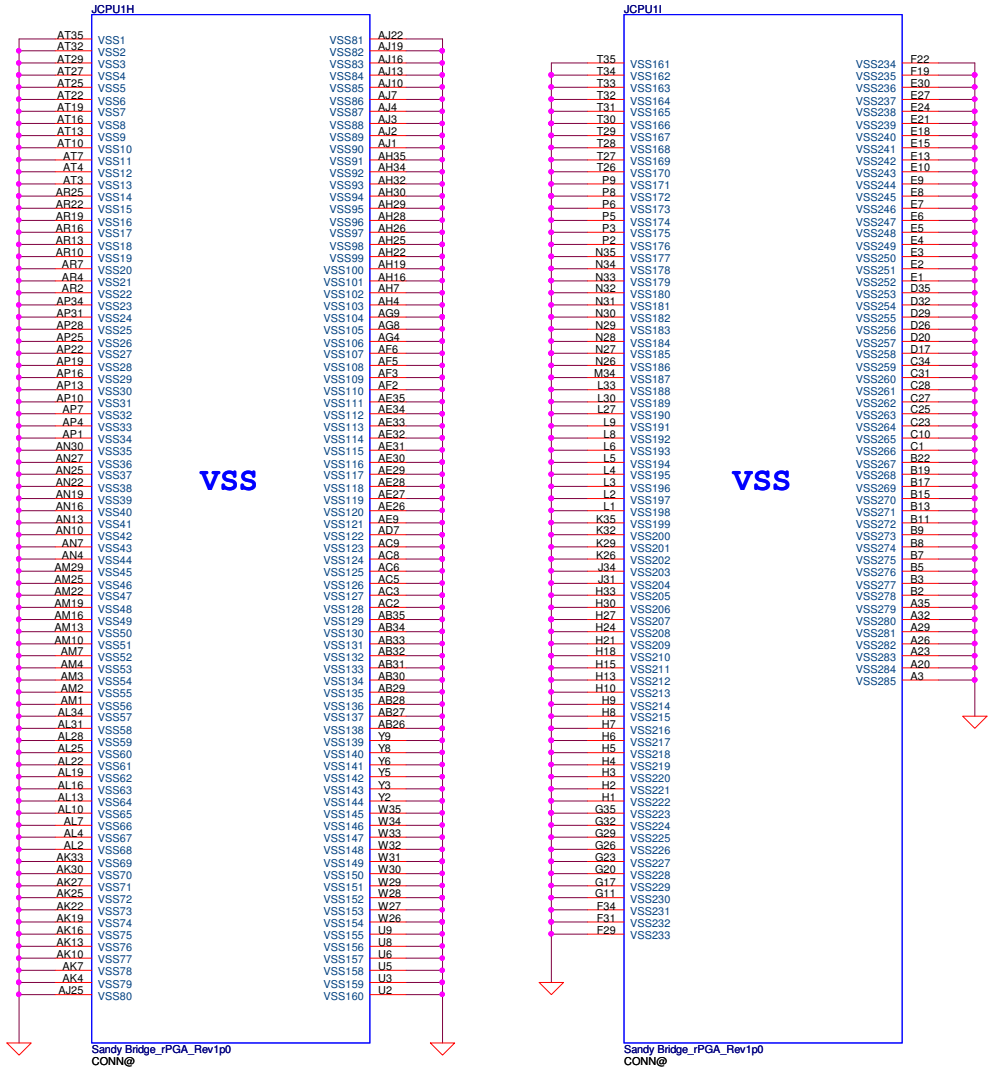

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Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-6931P	1.0

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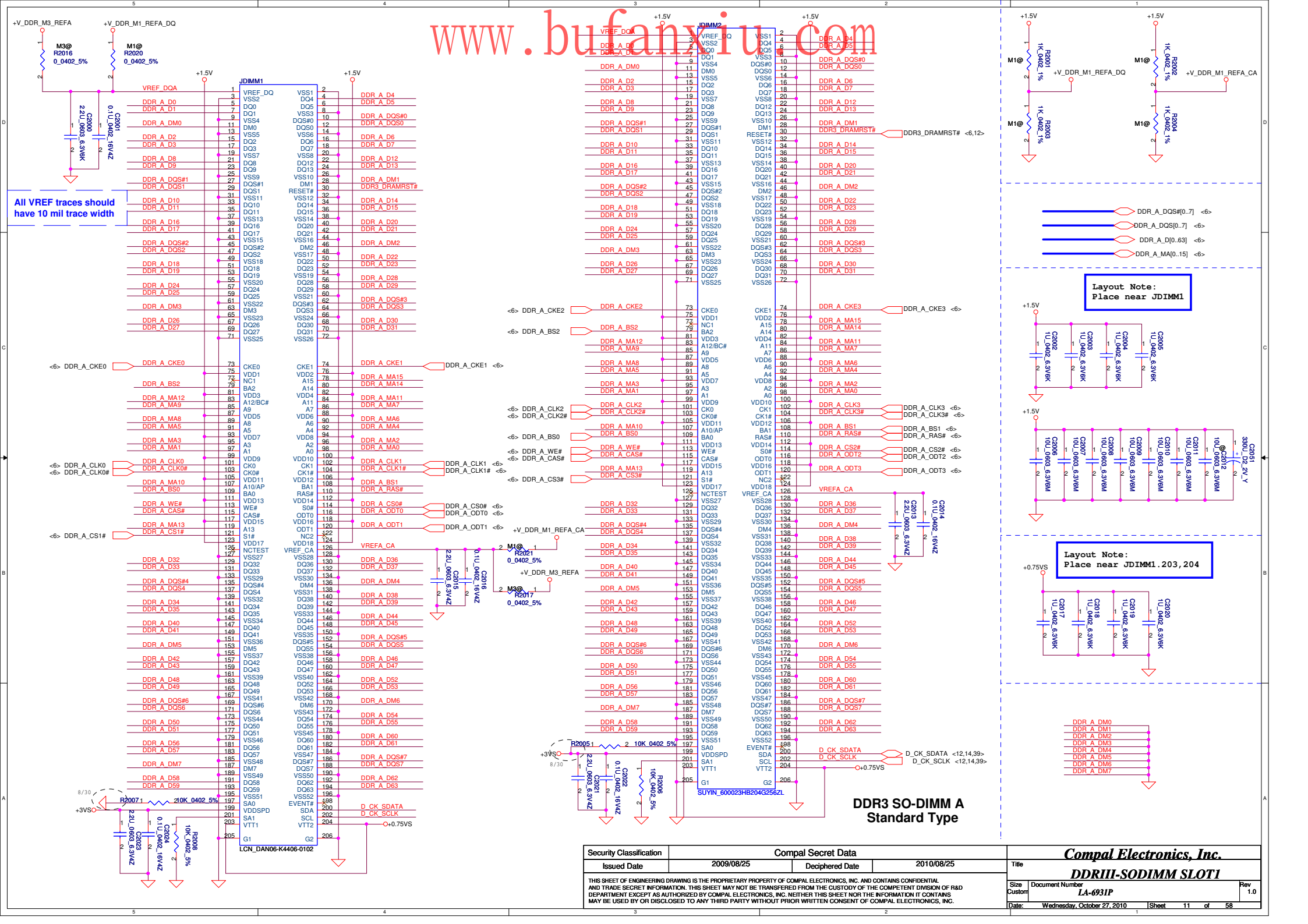
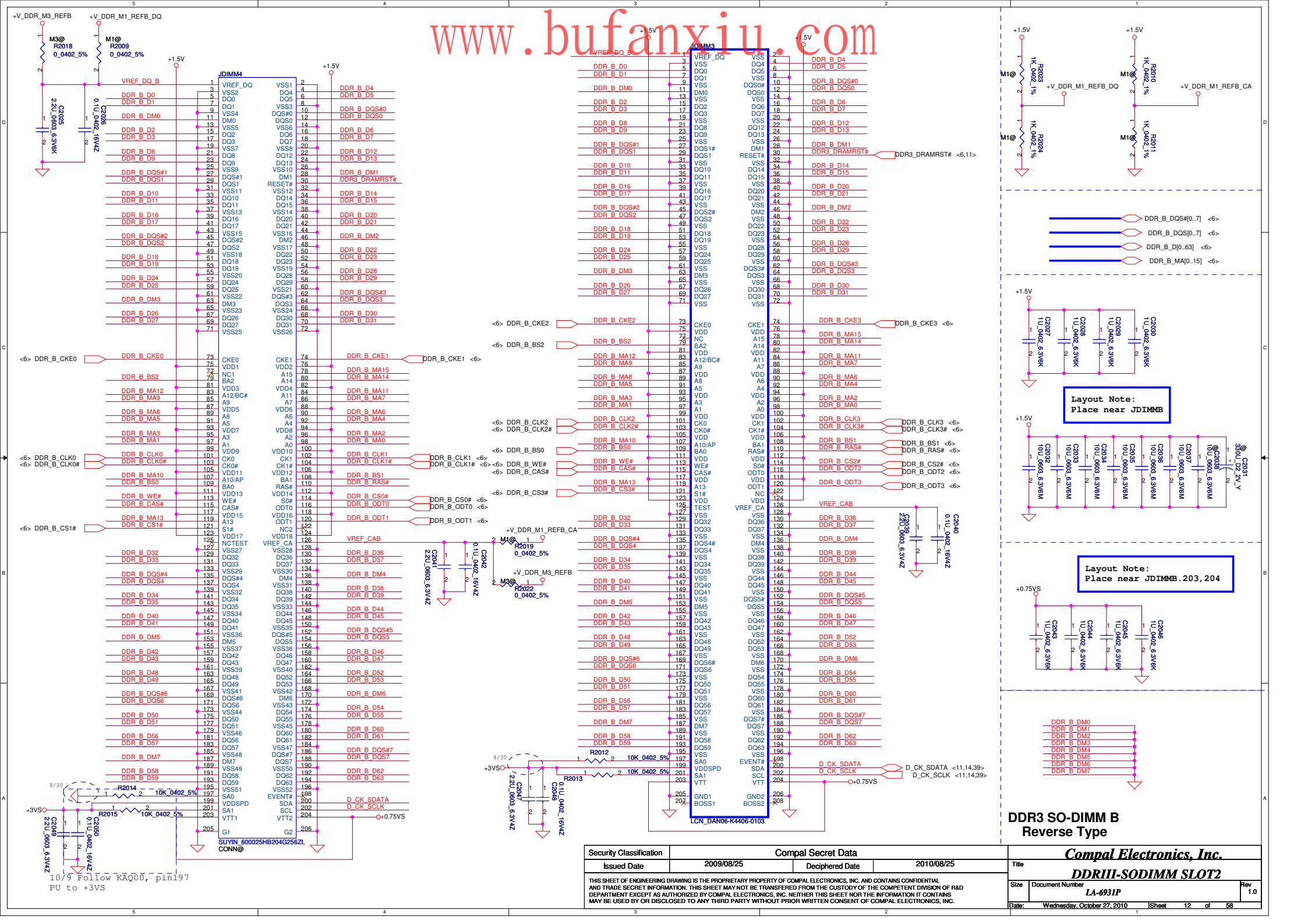


Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT1			
Size: Custom	Document Number: LA-6931P		Rev: 1.0
Date: Wednesday, October 27, 2010	Sheet 11 of 58		



DDR3 SO-DIMM B
Reverse Type

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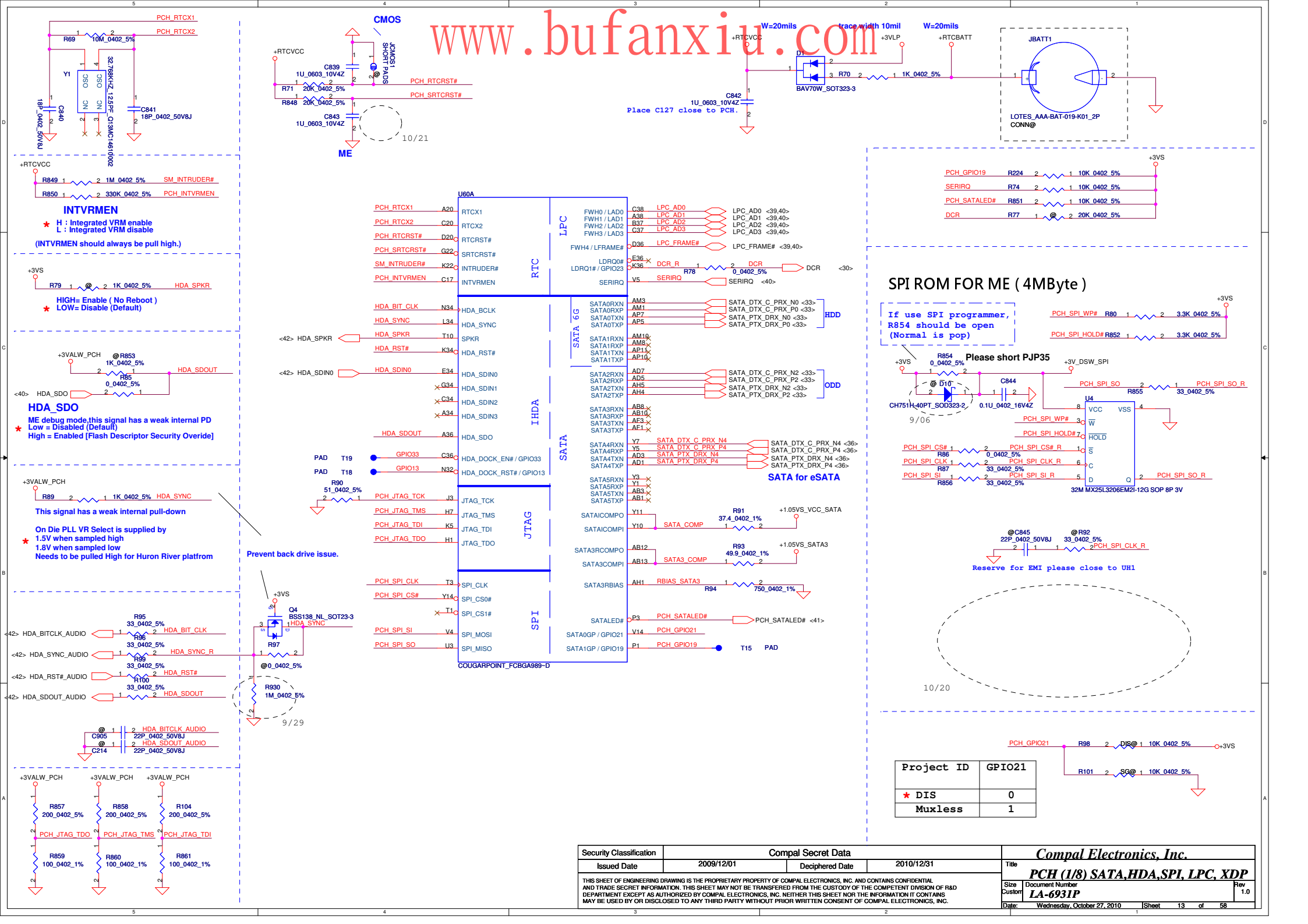
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number LA-6931P		Rev 1.0
Date: Wednesday, October 27, 2010	Sheet 12 of 58		



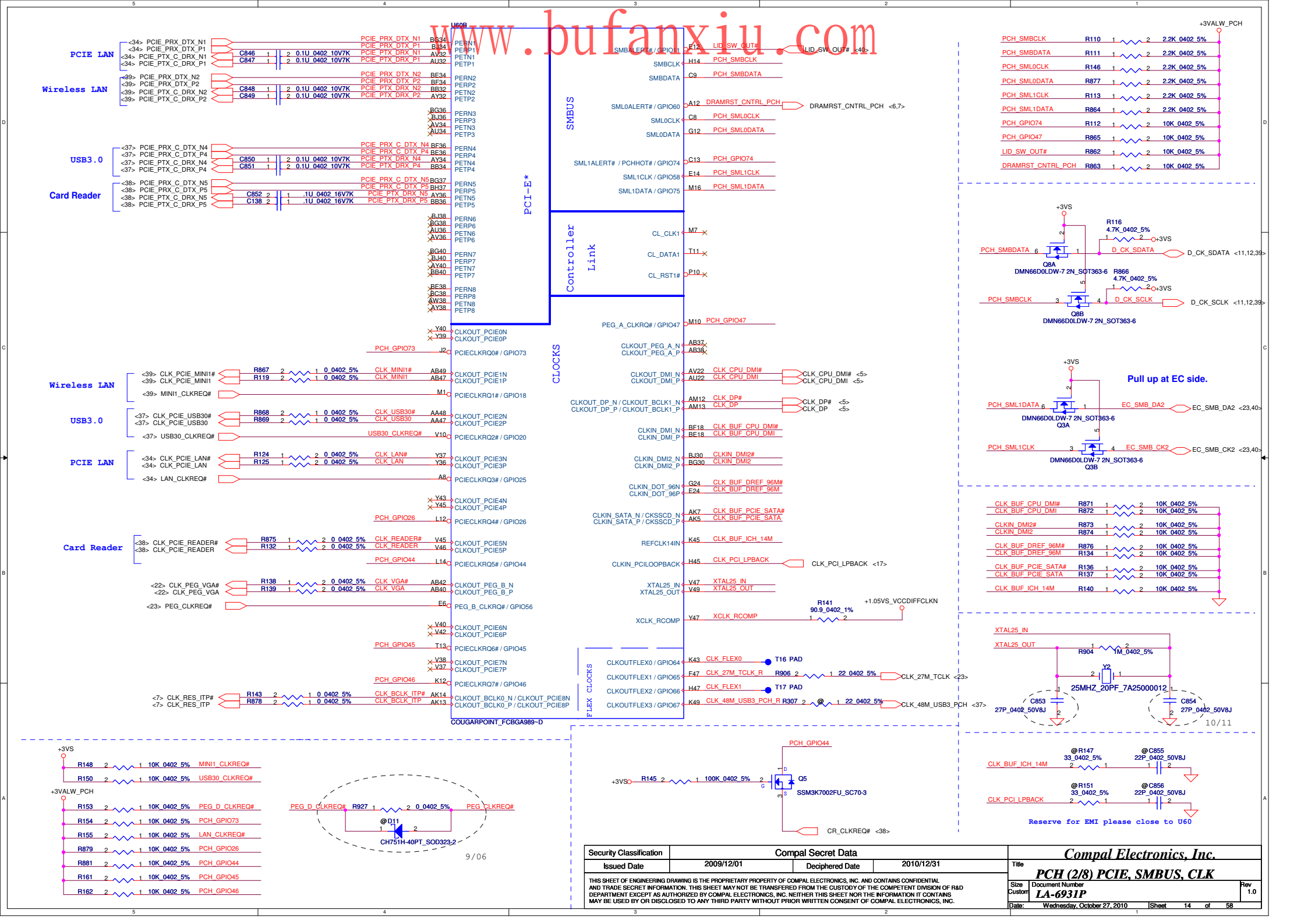
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 13 of 58



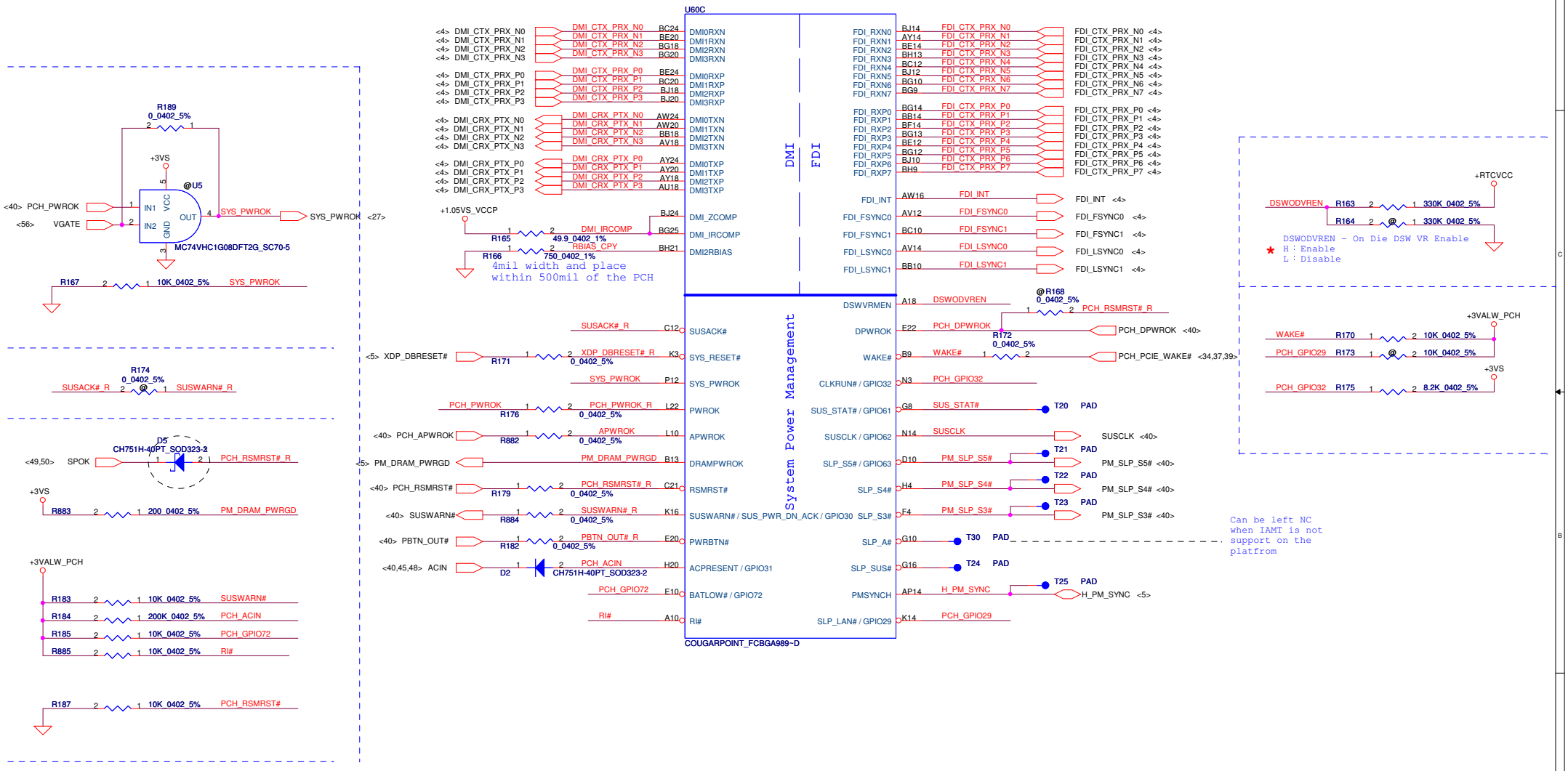
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 14 of 58



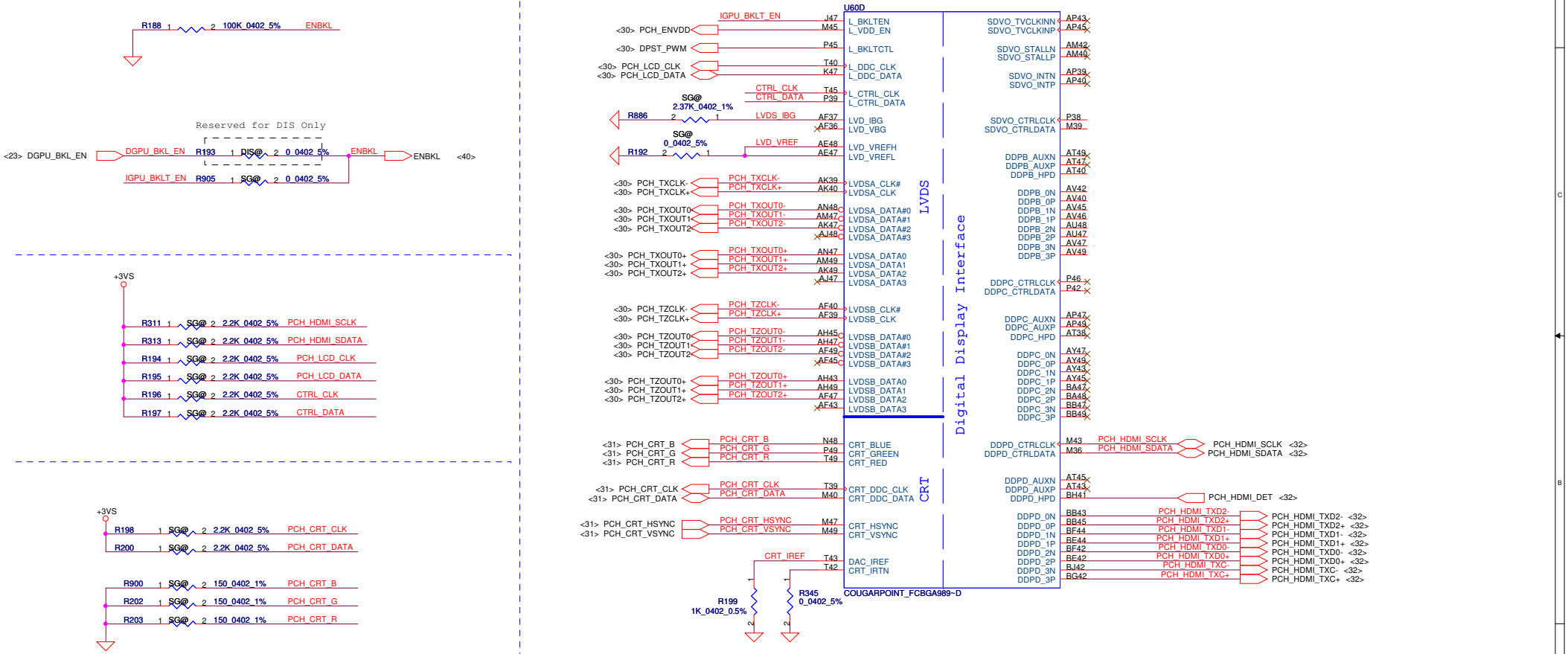
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 15 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PCH (4/9) LVDS,CRT,DP,HDMI			
Size: Custom	Document Number: LA-6931P		Rev: 1.0
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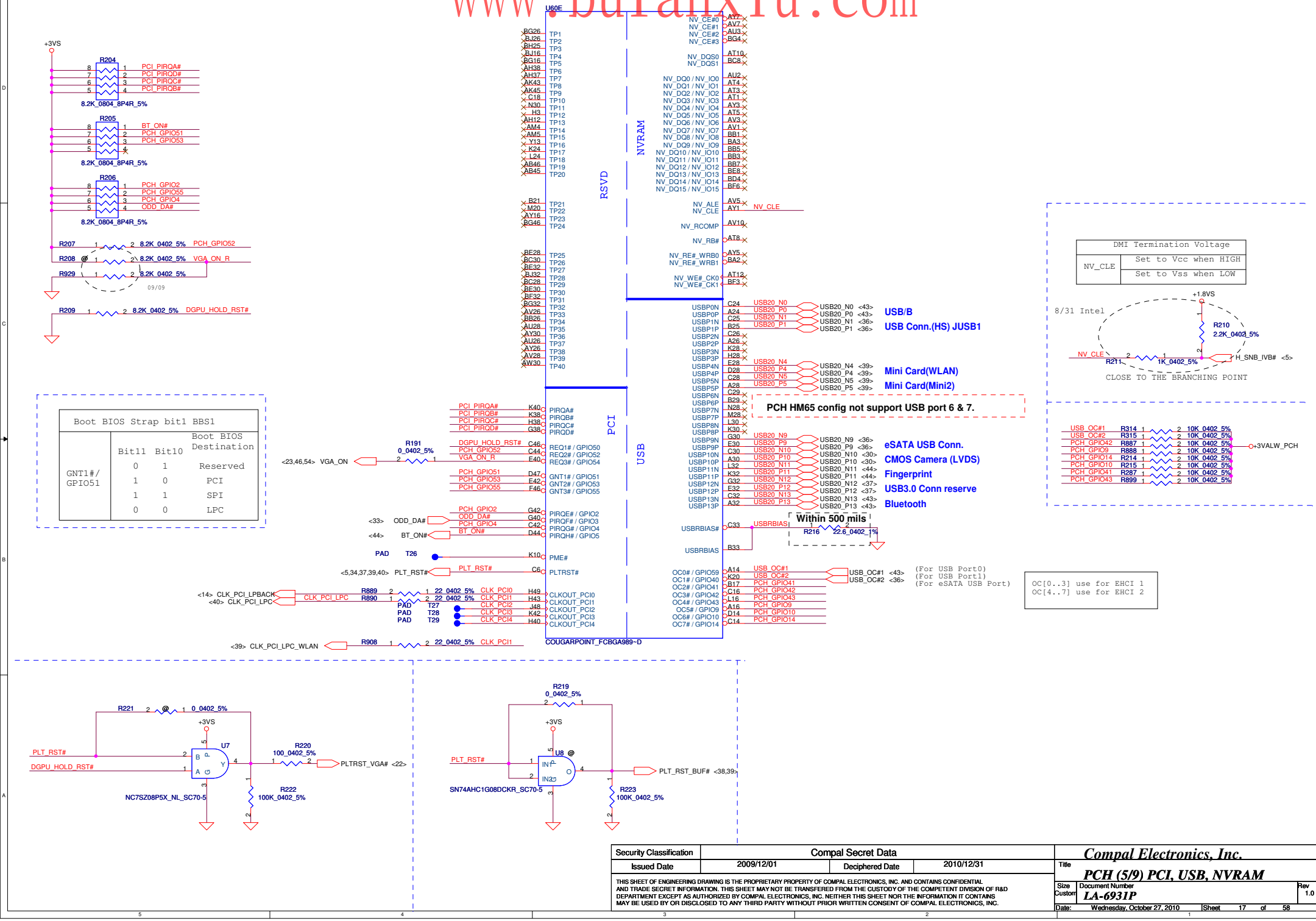

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size	Document Number	Rev
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GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R891 1 @ 2 1K_0402_5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
★High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R228 1 @ 2 10K_0402_5% PCH_GPIO27

PCH_GPIO37

+3VS
R230 1 @ 2 1K_0402_5% PCH_GPIO37
R232 1 2 100K_0402_5%

+3VS
R235 1 2 10K_0402_5% PCH_GPIO1
R894 1 2 10K_0402_5% DGPU_HPD_INT#
R895 1 2 10K_0402_5% PCH_GPIO16
R238 1 2 10K_0402_5% DGPU_PWROK
R239 1 2 10K_0402_5% PCH_GPIO22
R240 1 2 10K_0402_5% PCH_GPIO38
R241 1 2 10K_0402_5% PCH_GPIO39
R896 1 2 200K_0402_5% ODD_DETECT#
R243 1 2 10K_0402_5% PCH_GPIO34
R244 1 2 10K_0402_5% PCH_GPIO48
R245 1 2 10K_0402_5% PCH_GPIO49

+3VALW_PCH
R246 1 2 10K_0402_5% PCH_GPIO12
R247 1 2 1K_0402_5% SMIB_D
R897 1 2 10K_0402_5% PCH_GPIO57
R907 1 2 10K_0402_5% ODD_EN

10/26

R931 1 @ 2 10K_0402_5% ODD_DETECT#
R249 1 @ 2 10K_0402_5% PCH_GPIO35

SMIB_D R928 1 2 0_0402_5% SMIB
@D12 CH751H-40PT_SOD323-2

9/06

+3VS
R225 10K_0402_5%
CRT_DET
<31> CRT_DET# Q14 2N7002H_SOT23-3
High: CRT Plugged

+3VS
PCH_GPIO68 R909 1 2 10K_0402_5%
PCH_GPIO69 R910 1 2 10K_0402_5%
PCH_GPIO70 R911 1 2 10K_0402_5%
PCH_GPIO71 R912 1 2 10K_0402_5%

+3VS
EC_KBRST# R892 1 2 10K_0402_5%

U60F

CRT_DET	T7	BMBUSY# / GPIO0		TACH4 / GPIO68	C40	PCH_GPIO68
PCH_GPIO1	A42	TACH1 / GPIO1		TACH5 / GPIO69	B41	PCH_GPIO69
DGPU_HPD_INT#	H36	TACH2 / GPIO6		TACH6 / GPIO70	C41	PCH_GPIO70
<40> EC_SCI#	E38	TACH3 / GPIO7		TACH7 / GPIO71	A40	PCH_GPIO71
<40> EC_SMI#	C10	GPIO8				
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12				
<37> SMIB	G2	GPIO15		A20GATE	P4	GATEA20 <40>
PCH_GPIO16	U2	SATA4GP / GPIO16		PECI	AU16	PCH_PECI_R 0_0402_5% R893 H_PECI <5,40>
<22,27,55> VGA_PWROK	R233 0_0402_5%	DGPU_PWROK	D40	RCIN#	P5	EC_KBRST# EC_KBRST# <40>
		TACH0 / GPIO17		PROCPWRGD	AY11	H_CPUPWRGD <5>
PCH_GPIO22	T5	SCLOCK / GPIO22		THRMTRIP#	AY10	PCH_THRMTRIP#_R R234 390_0402_5% H_THRMTRIP# H_THRMTRIP# <5>
<33> ODD_EN	E8	GPIO24 / MEM_LED		INIT3_3V#	T14	
PCH_GPIO27	E16	GPIO27				
PCH_GPIO28	P8	GPIO28		NC_1	AH8	
PCH_GPIO34	K1	STP_PCI# / GPIO34		NC_2	AK11	
PCH_GPIO35	K4	GPIO35		NC_3	AH10	
<33> ODD_DETECT#	V8	SATA2GP / GPIO36		NC_4	AK10	
PCH_GPIO37	M5	SATA3GP / GPIO37		NC_5	P37	
<30> COLOR_ENG_EN	R920 0_0402_5%	PCH_GPIO38	N2	SLOAD / GPIO38		
PCH_GPIO39	M3	SDATAOUT0 / GPIO39				
PCH_GPIO48	V13	SDATAOUT1 / GPIO48		VSS_NCTF_15	BG2	T34 PAD
PCH_GPIO49	V3	SATA5GP / GPIO49		VSS_NCTF_16	BG48	T35 PAD
PCH_GPIO57	D6	GPIO57		VSS_NCTF_17	BH3	T36 PAD
				VSS_NCTF_18	BH47	T37 PAD
	A4	VSS_NCTF_1		VSS_NCTF_19	BJ4	
	A44	VSS_NCTF_2		VSS_NCTF_20	BJ44	T41 PAD
	A45	VSS_NCTF_3		VSS_NCTF_21	BJ45	T43 PAD
	A46	VSS_NCTF_4		VSS_NCTF_22	BJ46	T45 PAD
	A5	VSS_NCTF_5		VSS_NCTF_23	BJ5	
	A6	VSS_NCTF_6		VSS_NCTF_24	BJ6	
	B3	VSS_NCTF_7		VSS_NCTF_25	C2	
	B47	VSS_NCTF_8		VSS_NCTF_26	C48	
PAD T53	BD1	VSS_NCTF_9		VSS_NCTF_27	D1	
PAD T55	BD49	VSS_NCTF_10		VSS_NCTF_28	D49	
PAD T57	BE1	VSS_NCTF_11		VSS_NCTF_29	E1	
PAD T59	BE49	VSS_NCTF_12		VSS_NCTF_30	E49	
PAD T60	BF1	VSS_NCTF_13		VSS_NCTF_31	F1	
PAD T62	BF49	VSS_NCTF_14		VSS_NCTF_32	F49	

GPIO | CPU/MISC | NCTF

COUGARPOINT_FCBGA989~D

+3VS
R229 10K_0402_5%

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

9/22

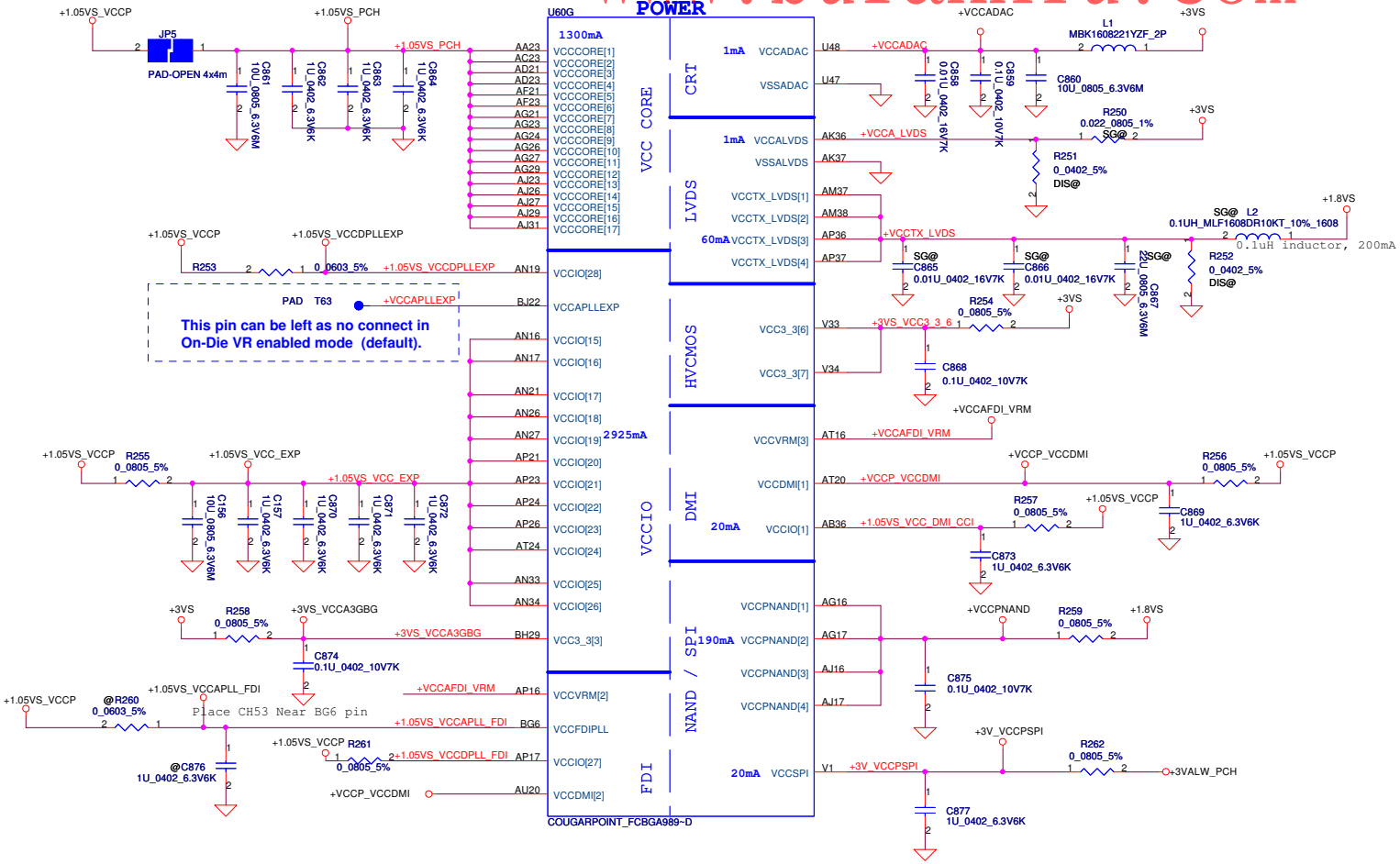
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 18 of 58



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 19 of 58

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec

POWER

U60J

COUGARPOINT_FCBGA989-D

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

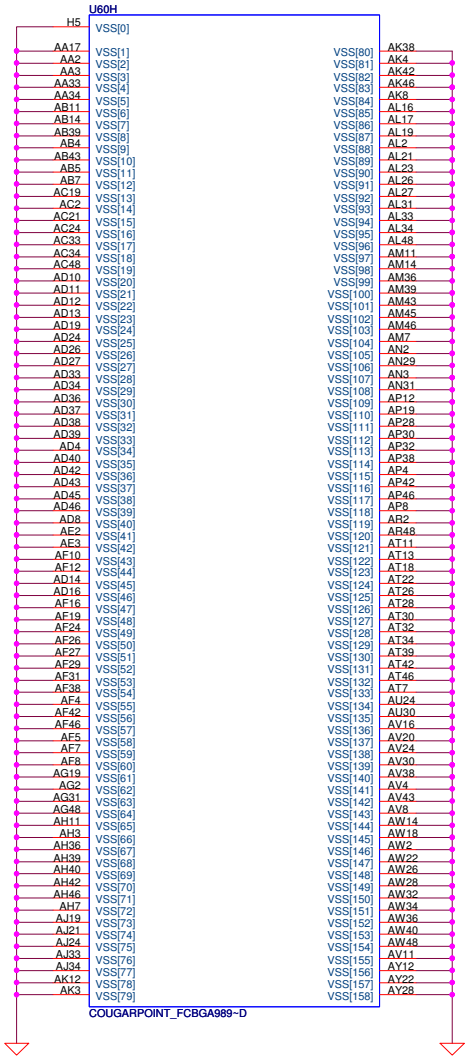
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

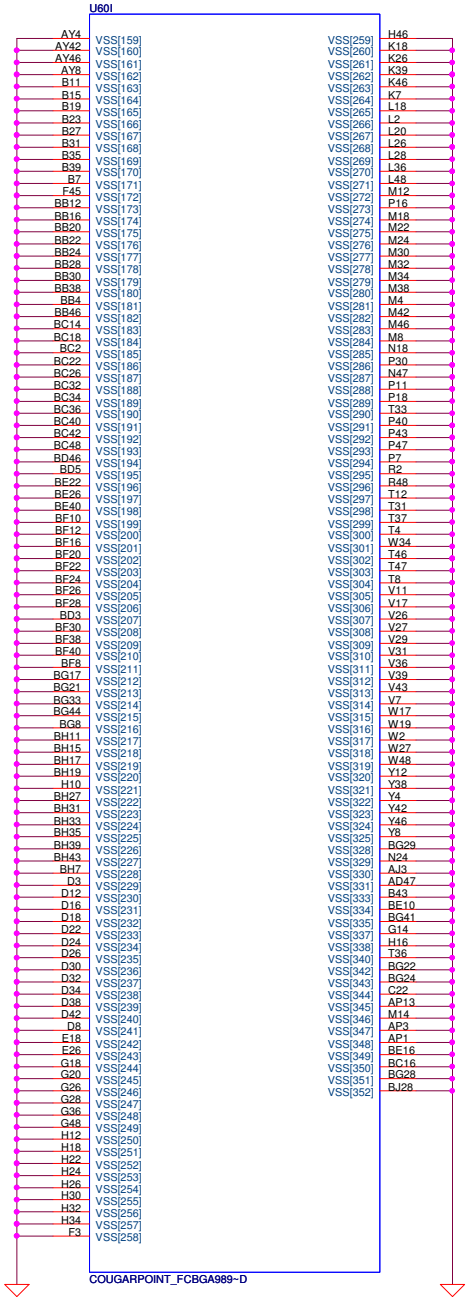
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 20 of 58





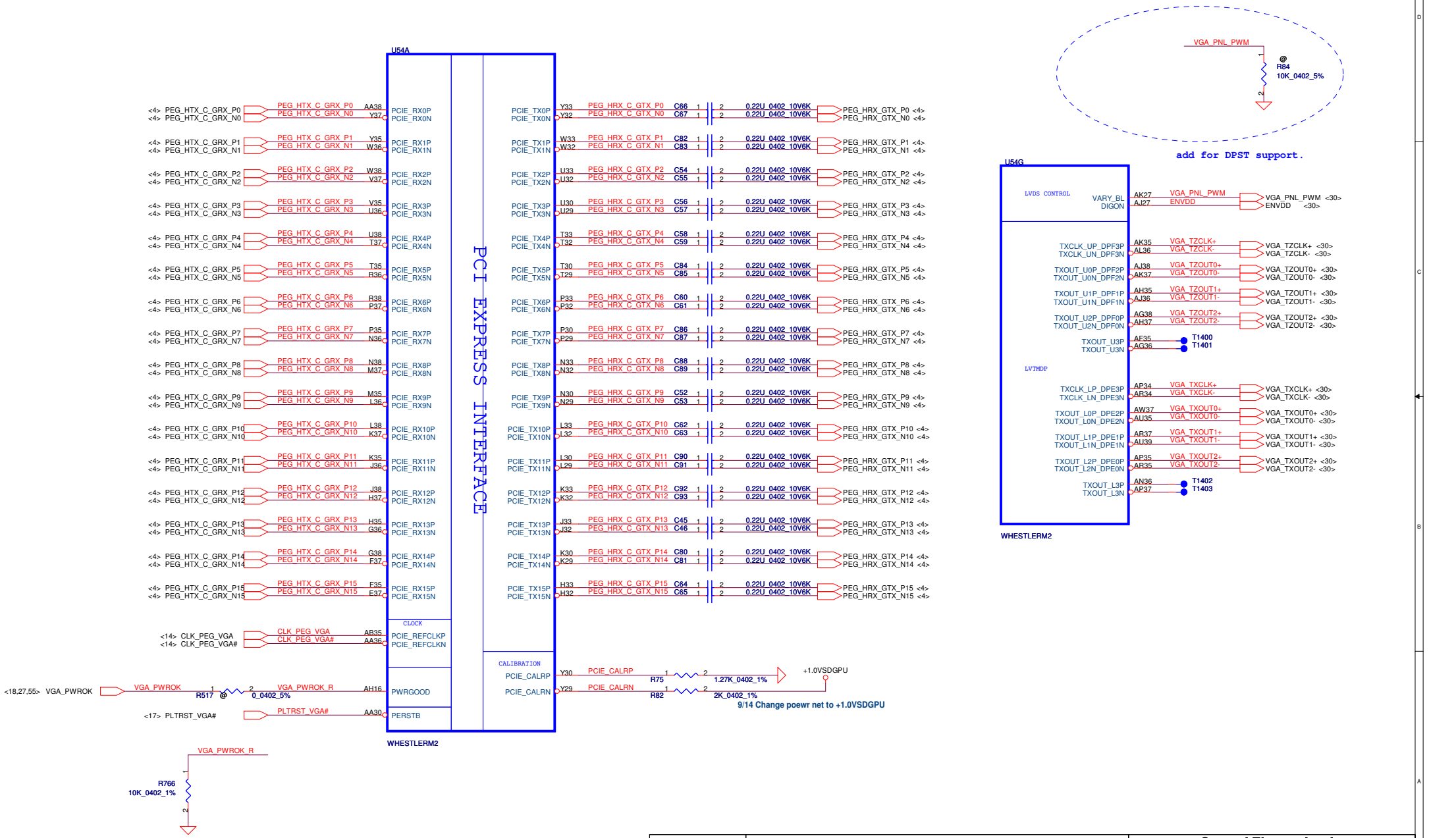
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 21 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_ PCIE / LVDS**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 22 of 58

Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE_STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

VRAM \ Location	VRAM_ID2	VRAM_ID1	VRAM_ID0	
Hynix(8pcs) 1GB (old) H5TQ1G63BFR-12C	O	O	1	
Hynix(8pcs) 1GB (900MHz) H5TQ1G63DFR-11C	O	1	O	
Samsung(8pcs) 1GB (900MHz) K4W1G1646G-BC11 LF	O	1	1	
Hynix(8pcs) 2GB (800MHz) H5TQ2G63BFR-12C	1	O	O	
Samsung(8pcs) 2GB (800MHz) K4W2G1646C-HC12	1	O	1	

External VGA Thermal Sensor

U15 @ ADM1032ARMZ-2REEL_MSOP8

+3VS_DELAY

3/2 Change Bom structure of C120 to mount,Change value of R525 to 24k ohm(1%)

Use boradway GPU, R28 change to 0 Ohm(SD028000080)

PWR Sequence

+3VS_DELAY
VGA_CORE (VDDC)
+1.8VS

M96 only

HDMI

CRT

Y3 must install on SG mode

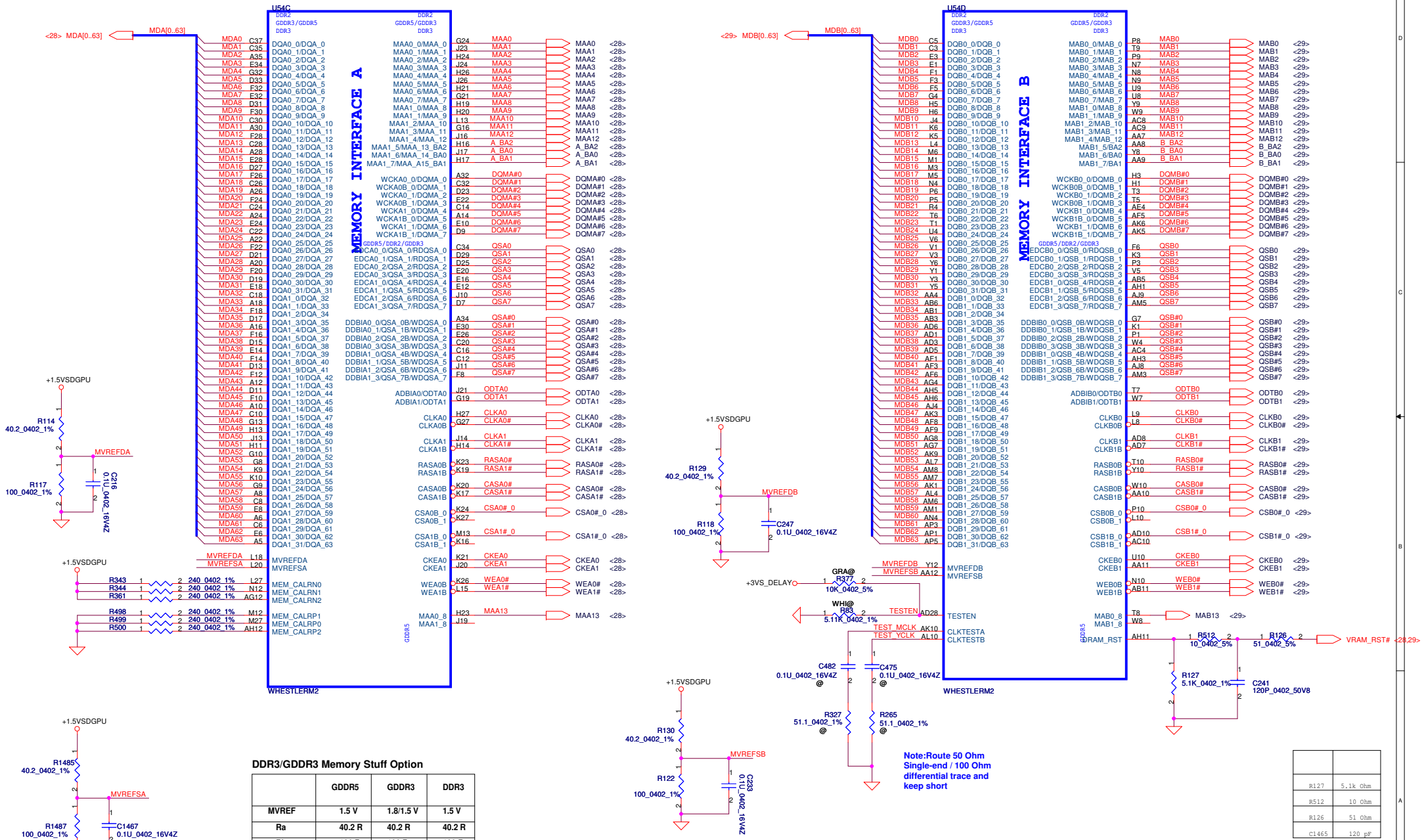
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Mannhatton_Strape/DP/HDMI//CRT

Size	Document Number	Rev
C	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 23 of 58



DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVREF	1.5 V	1.8/1.5 V	1.5 V
Ra	40.2 R	40.2 R	40.2 R
Rb	100 R	100 R	100 R

R127	5.1k Ohm
R512	10 Ohm
R126	51 Ohm
C1465	120 pF

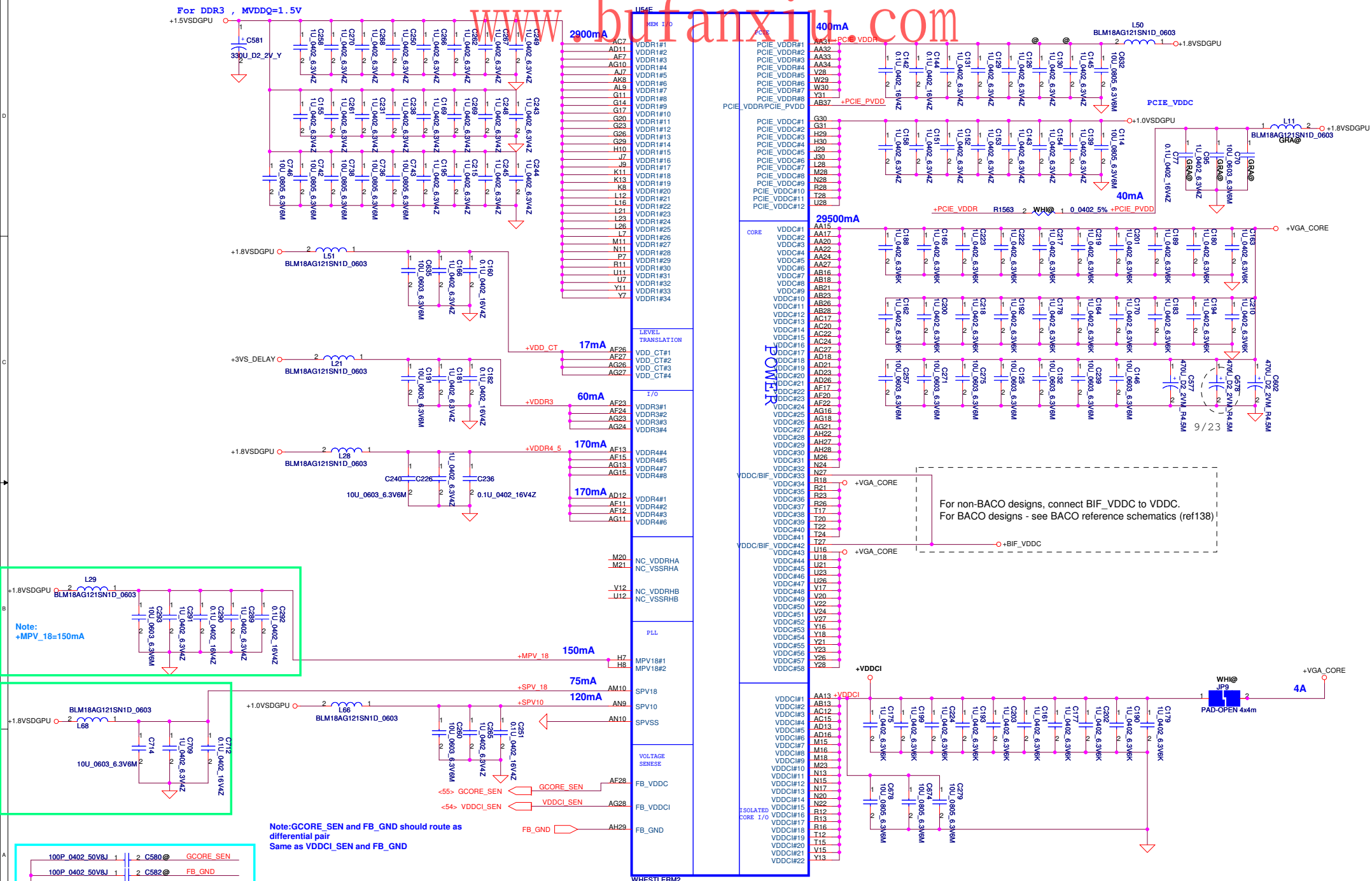
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_Memory**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 24 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_Power/GND**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 25 of 58

U54F

GND

WHESTLERM2

U54H

WHESTLERM2

DP C/D POWER

DP A/B POWER

DP E/F POWER

DP PLL POWER

For PX_EN, refer to the BACO reference schematics for detail

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

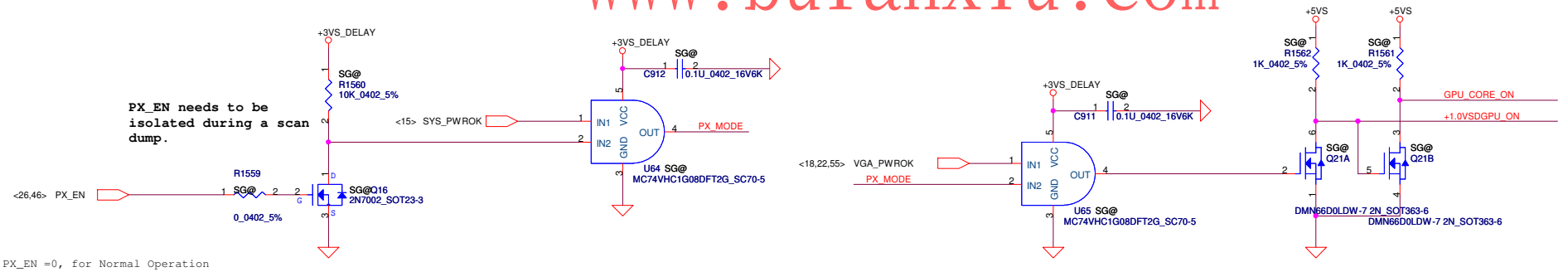
Compal Electronics, Inc.

Title: Mannhatton_Power/GND

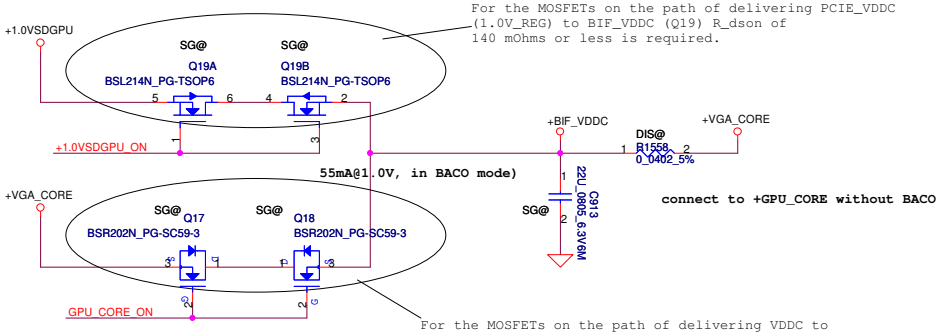
Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 26 of 58

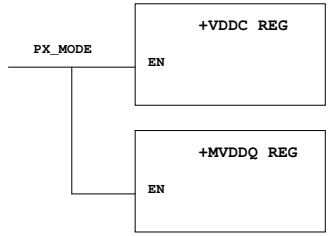
PX_MODE =1, for Normal Operation
PX_MODE =0, for BACO MODE



PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE



	Voltage	In BACO mode
VDDR1	1.5V	OFF
VDDC/VDDCI	0.85~1.15V	OFF
others		ON



power on sequence:
(1) +3VS_Delay ----> +VDDC ----> +1.8VS
(> 0ms) (reach 90%)
(2) +3VS_Delay ----> +1.8VS ----> +VDDC
(> 0ms) (reach 90%)

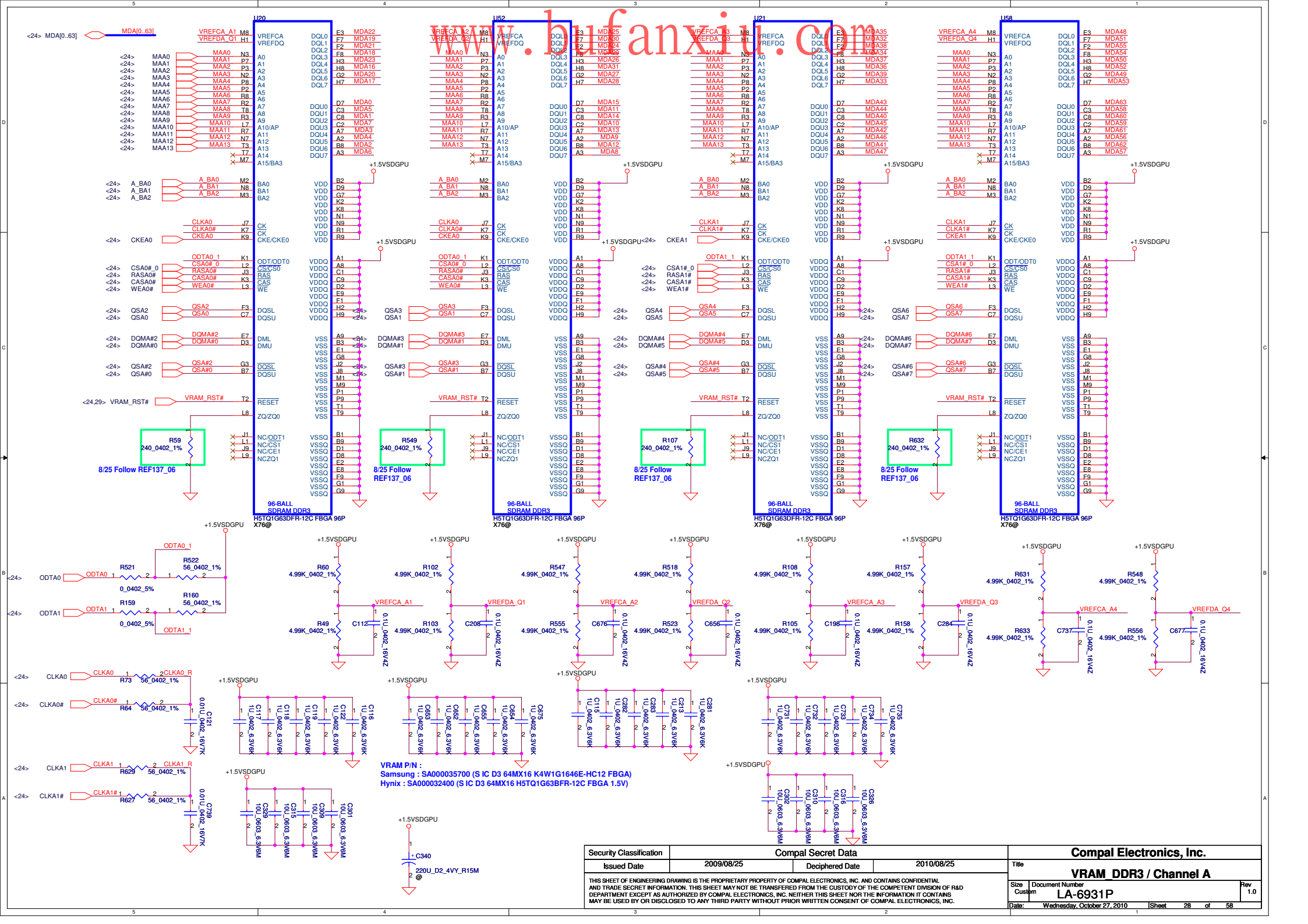
Security Classification	Compal Secret Data		
Issued Date	2009/11/12	Deciphered Date	2010/11/12

Compal Electronics, Inc.

Title: BACO

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 27 of 58



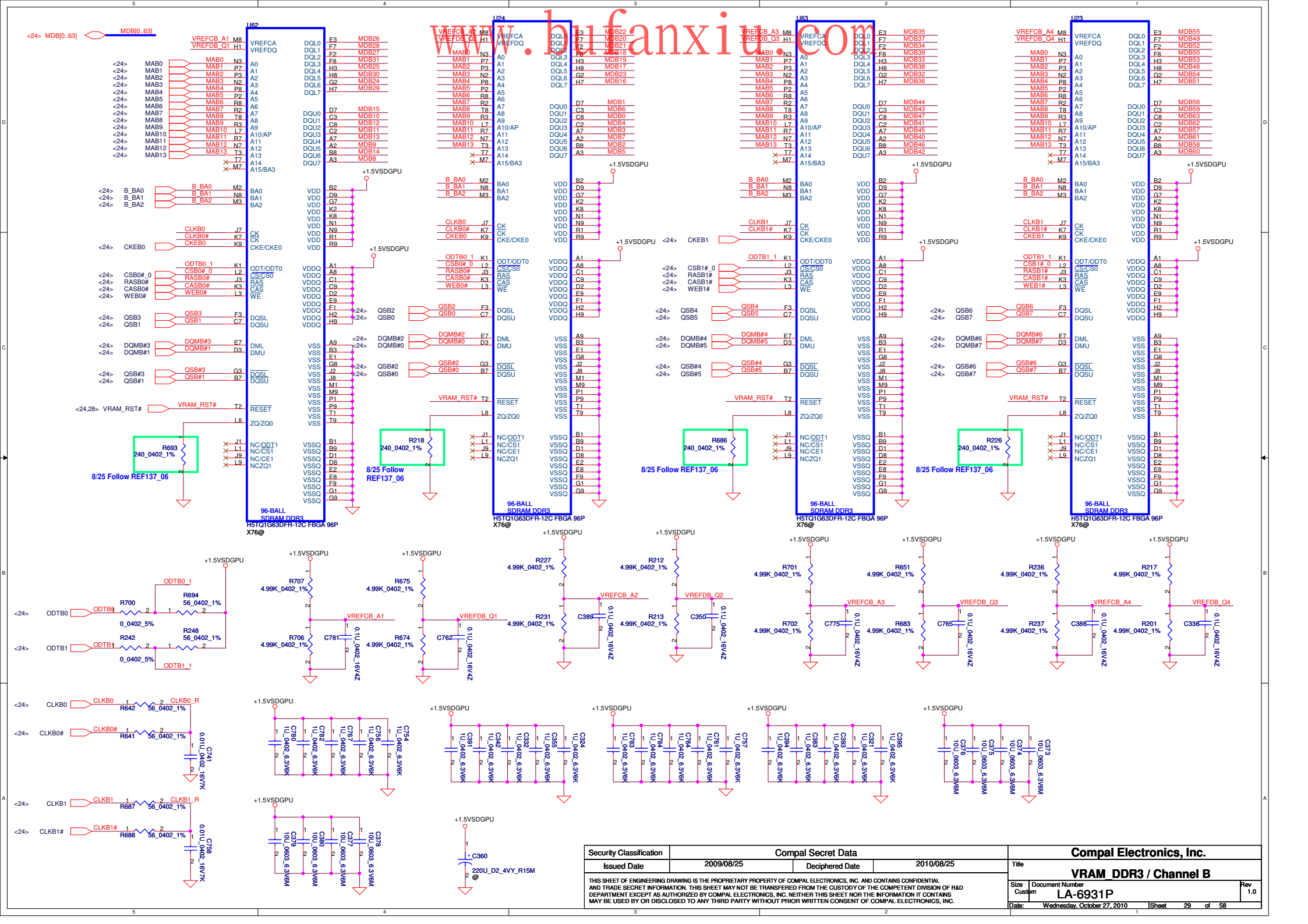
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **VRAM_DDR3 / Channel A**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 28 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

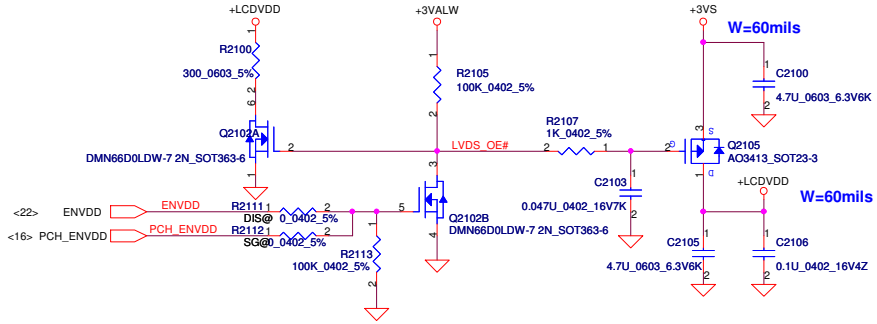
Compal Electronics, Inc.

Title: **VRAM_DDR3 / Channel B**

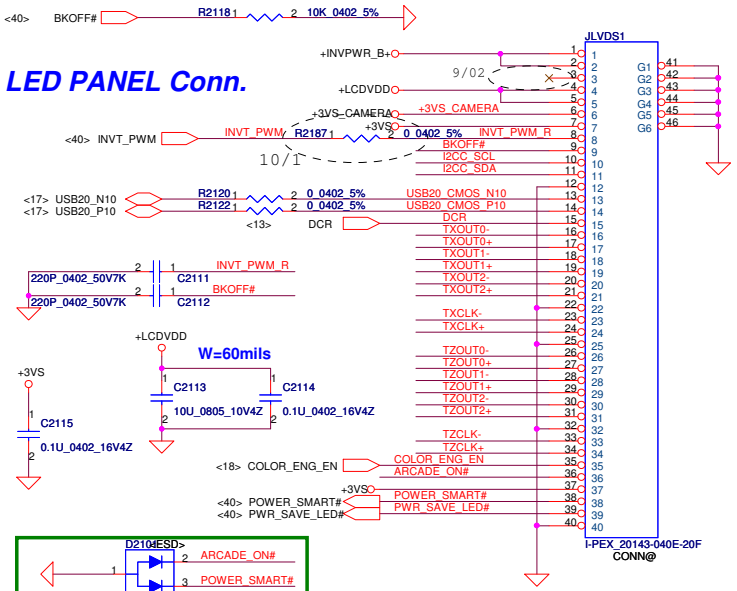
Size	Document Number	Rev
Custom	LA-6931P	1.0

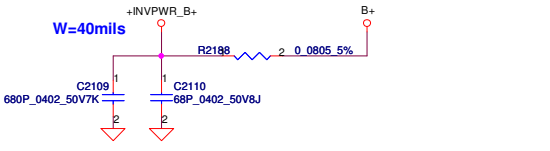
Date: Wednesday, October 27, 2010 | Sheet 29 of 58

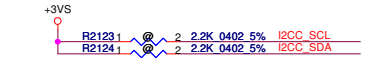
LCD POWER CIRCUIT

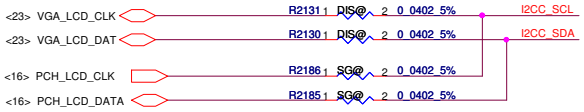


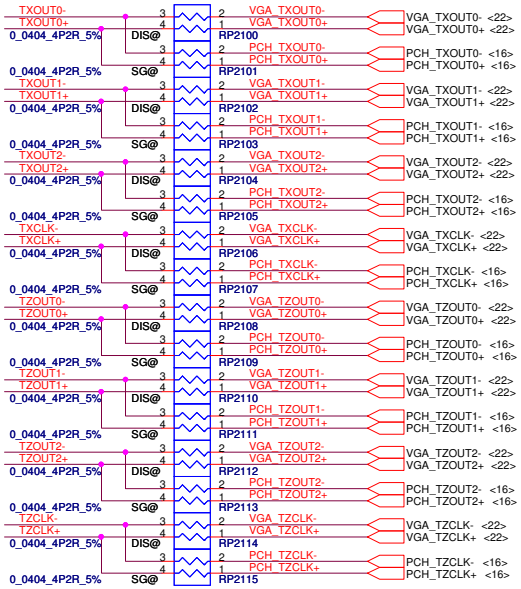
LED PANEL Conn.

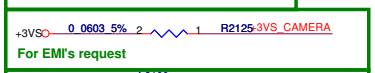


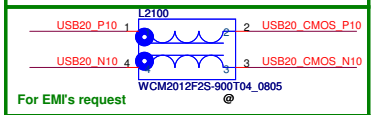


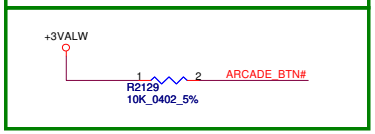


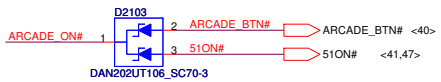


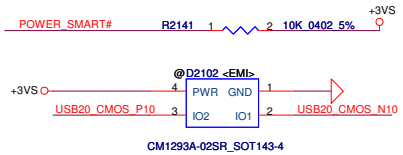












Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

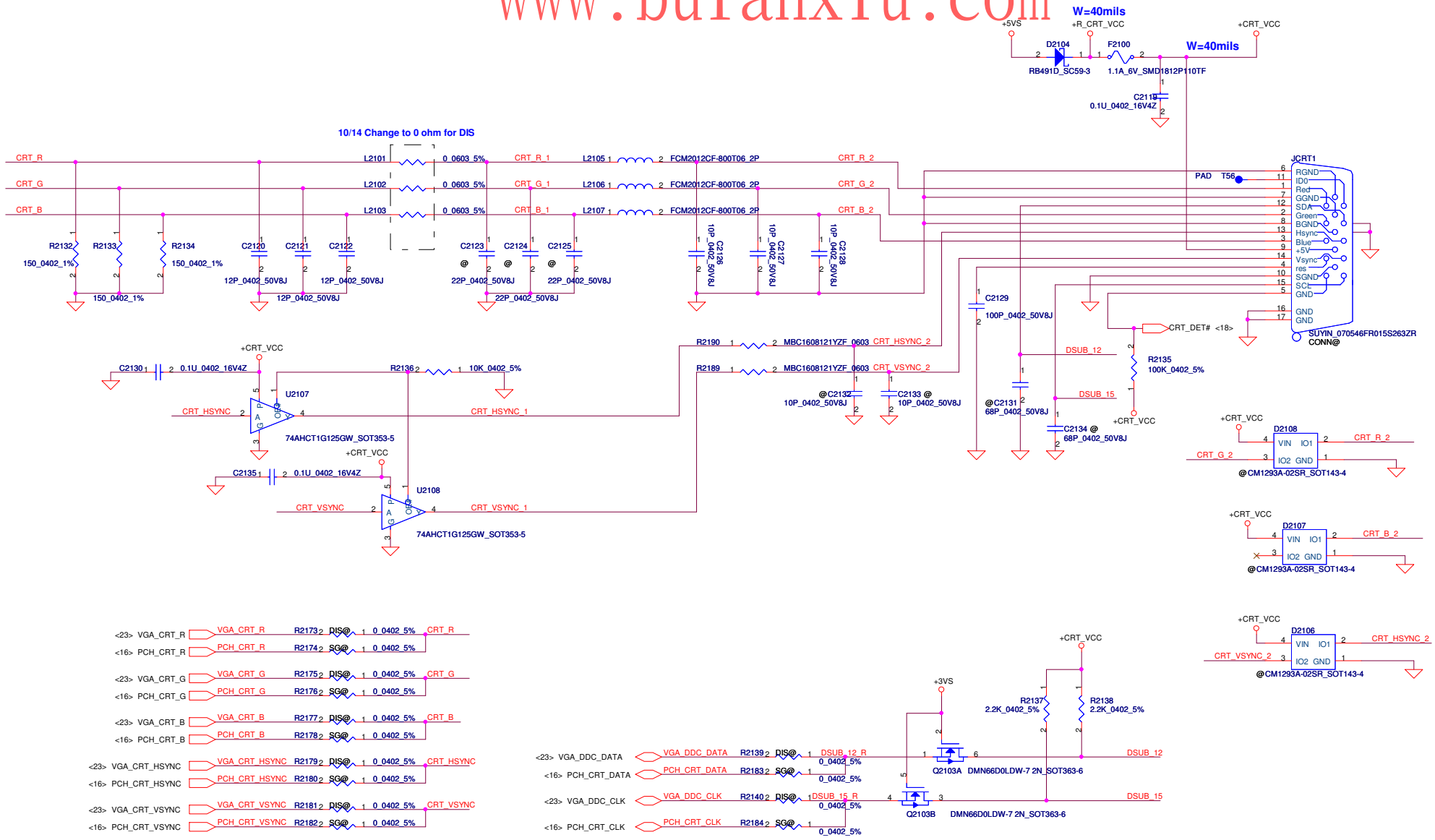
Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 | Sheet 30 of 58

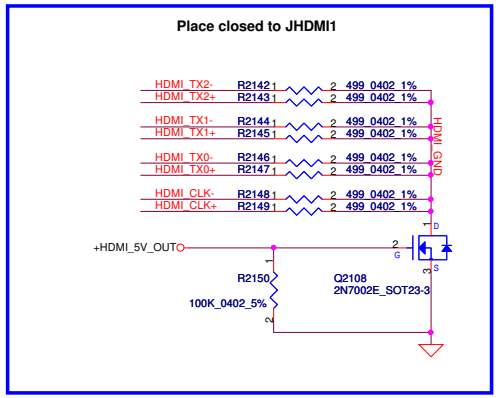
CRT Connector

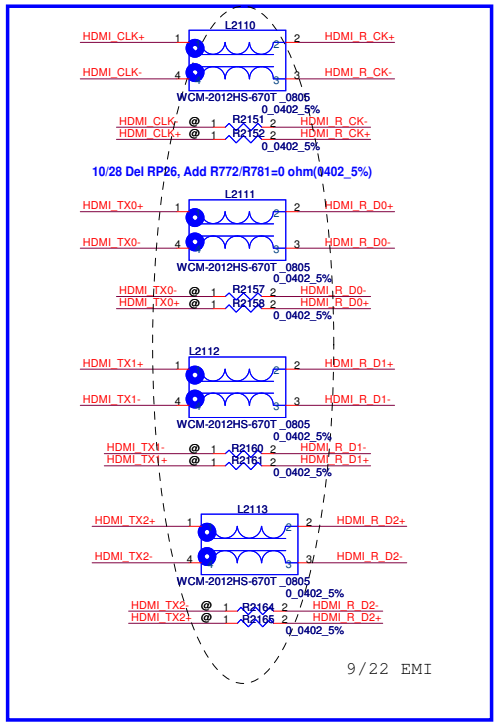


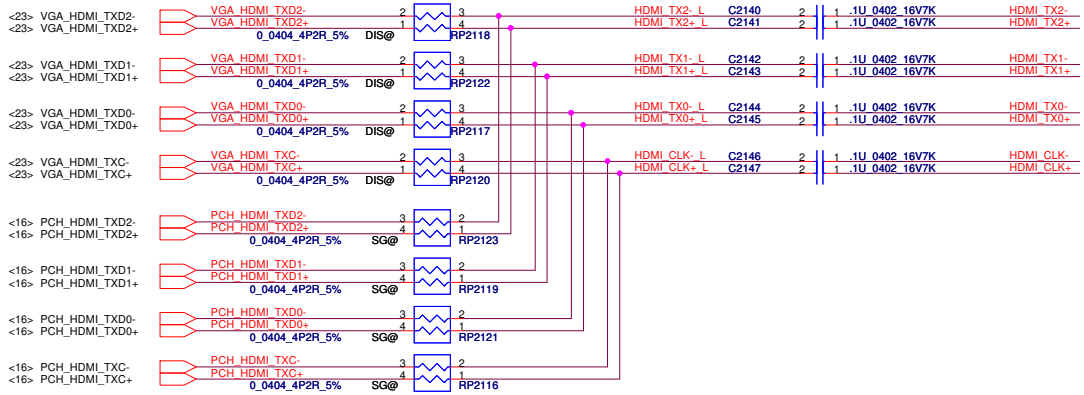
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

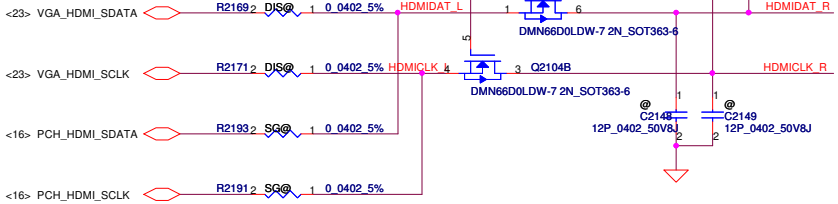
Compal Electronics, Inc.

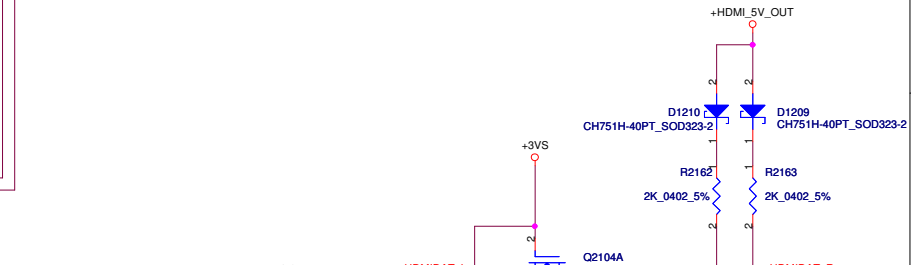
Title	CRT Connector	
Size B	Document Number LA-6931P	Rev 1.0
Date: Wednesday, October 27, 2010	Sheet 31 of 58	

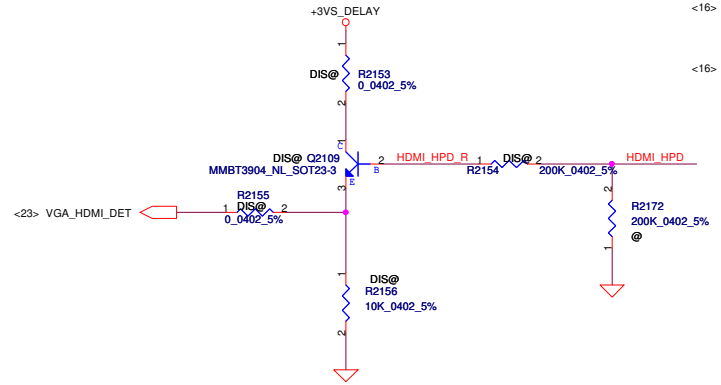


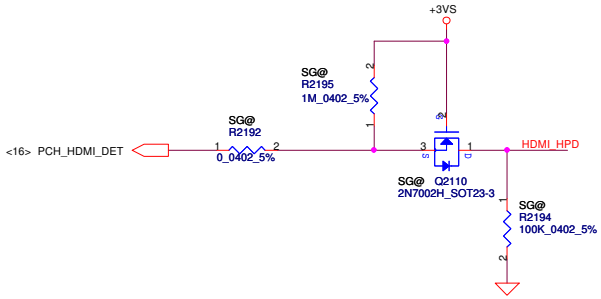


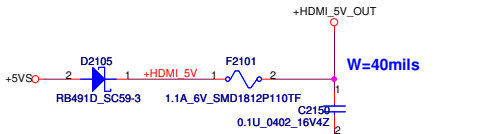


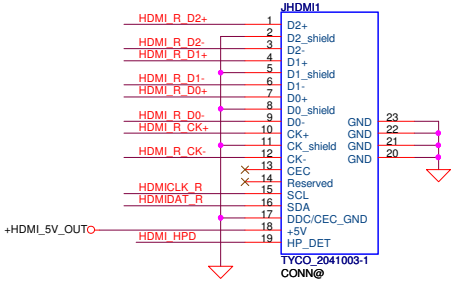












Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

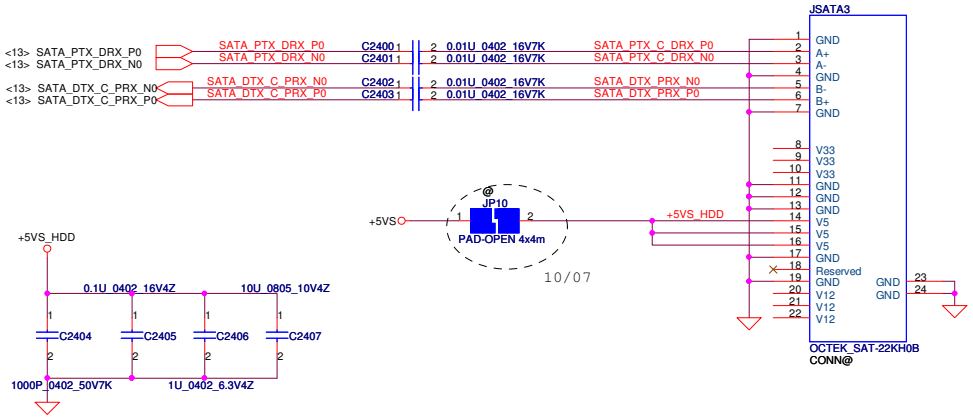
Title: HDMI Level Shife & Conn

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 32 of 58

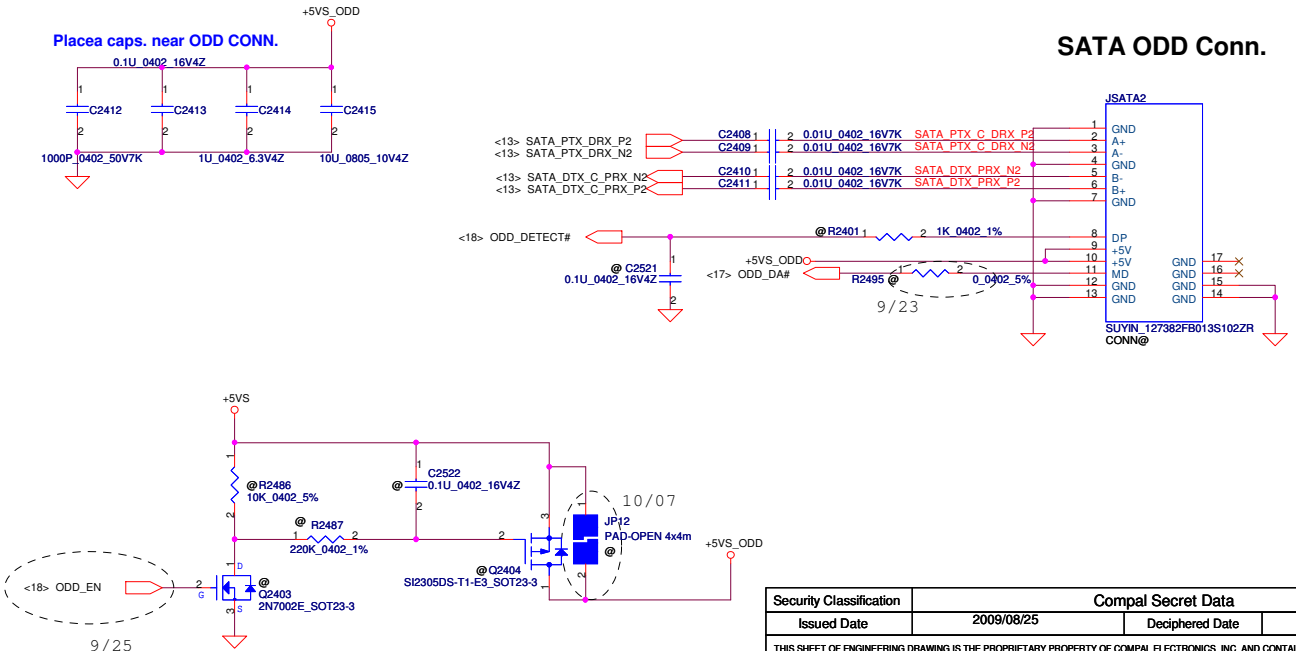
HDD

SATA HDD Conn.



ODD

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: LA-6931P		Rev: 1.0
Date: Wednesday, October 27, 2010	Sheet 33 of 58		

W=60mils

+3VALW → @ R1200 0_1206_5% → +LAN_IO

Q1201 SI2301BDS_SOT23 — 370mA

R1201 47K_0402_5%

R1202 47K_0402_5%

The +LAN_IO Rising time (10%~90%) need >1mS and <100mS

+3VALW → R1223 470K_0402_5% → Q1200 2N7002E_SOT23-3

C1231 10U_0603_6.3V6M

08/27

W=60mils

+LAN_IO 1.5A

C1201 C1202 C1203 C1204 C1205 C1206 0.1U_0402_16V7K

These caps close to U70 : Pin 12,27,39,42,47,48

U70 RTL8111E-GR_QFN48_6X6

<14> PCIE_PRX_DTX_P1	C1219 0.1U_0402_16V7K	PCIE_PRX_C_DTX_P1	22 HSOP
<14> PCIE_PRX_DTX_N1	C1220 0.1U_0402_16V7K	PCIE_PRX_C_DTX_N1	23 HSON
<14> PCIE_PTX_C_DRX_P1			17 HSIP
<14> PCIE_PTX_C_DRX_N1			18 HSIN
<14> LAN_CLKREQ#			16 CLKREQB
<5,17,37,39,40> PLT_RST#			25 PERSTB
<14> CLK_PCIE_LAN			19 REFCLK_P
<14> CLK_PCIE_LAN#			20 REFCLK_N
		XTLO	43 CKXTAL1
		XTLI	44 CKXTAL2
<40> EC_PME#			
<15,37,39> PCH_PCIE_WAKE#	R1209 @ 0_0402_5%		28 LANWAKEB
+3VS	R1210 1K_0402_5%	ISOLATEB	26 ISOLATEB
	R1211 10K_0402_5% / R1213 1K_0402_5%		14 NC/SMBCLK, 15 NC/SMBDATA, 38 GPO/SMBALERT
	R1214 0_0402_5%		33 ENSWREG
		+LAN_VDDREG	34 VDDREG, 35 VDDREG
	R1215 2.49K_0402_1%		46 RSET
			24 GND, 49 PGND

R1212 15K_0402_5%

3.3V : Enable switching regulator
0V : Disable switching regulator

		LED3/EEDO	31
		LED1/EESK	37 LANLINK_STATUS#
		LED0	40 LAN_ACTIVITY#
	R1205 10K_0402_5% / R1206 10K_0402_5%	EECS/SCL / EEDI/SDA	30, 32
		MDIP0 / MDIN0	1 LAN_MDI0+ / 2 LAN_MDI0-
		MDIP1 / MDIN1	4 LAN_MDI1+ / 5 LAN_MDI1-
		NC/MDIP2 / NC/MDIN2	7 LAN_MDI2+ / 8 LAN_MDI2-
		NC/MDIP3 / NC/MDIN3	10 LAN_MDI3+ / 11 LAN_MDI3-
		DVDD10	13, 29, 41 → +LAN_VDD
		DVDD33	27, 39
		AVDD33	12, 42, 47, 48 → +LAN_IO
		EVDD10	21 → +LAN_EVDD10
		AVDD10	3, 6, 9, 45 → +LAN_VDD
		REGOUT	36 → +LAN_SROUT1.05

+LAN_VDD: C1207 C1208 C1209 C1210 C1211 C1212 C1213 0.1U_0402_16V7K

These caps close to U70 : Pin 3,6,9,13,29,41,45

+LAN_VDD → R1204 0_0603_5% → +LAN_EVDD10

C1217 0.1U_0402_16V7K, C1218 1U_0402_6.3V6K

+LAN_IO → R1203 0_0603_5% → +LAN_VDDREG

C1215 4.7U_0603_6.3V6K, C1216 0.1U_0402_16V7K

+LAN_SROUT1.05 W=60mils → L1200 2.2UH +-5% NLC252018T-2R2J-N W=60mils → +LAN_VDD

C1221 4.7U_0603_6.3V6K, C1222 0.1U_0402_16V7K, C1224 @ 10U_0805_10V4Z

10/25

These components close to U70 : Pin 36
(Should be place within 200 mils)

C1224 27P_0402_50V8J — XTLI_R — R1217 0_0402_5% — XTLI

Y1200 25MHZ_12PF_X5H025000FC1H-H

XTLO — C1225 27P_0402_50V8J

C1223 @ 220P_0402_50V7K

LANLINK_STATUS# → R1216 510_0402_5% → LANLED_LINK#

JRJ45 SANTA_130452-D CONN@

Green LED-	9
Green LED+	10
PR1+	1
PR1-	2
PR2+	3
PR3+	4
PR3-	5
PR2-	6
PR4+	7
PR4-	8
Yellow LED-	11
Yellow LED+	12
G2	14
G1	13

+LAN_IO → RJ45_MDO0+, RJ45_MDO0-, RJ45_MDO1+, RJ45_MDO2+, RJ45_MDO2-, RJ45_MDO1-, RJ45_MDO3+, RJ45_MDO3-

LAN_ACTIVITY# → R1218 510_0402_5% → LANLED_ACT#

@C1226 220P_0402_50V7K

40mil

10/26 EMI

D1201 AZC199-02SPR7G_SOT23-3 @

D1202 AZC199-02SPR7G_SOT23-3 @

TS1 350uH_GSL5009LF

LAN_MDI3-	1 TCT1	MCT1	24
LAN_MDI3+	2 TD1+	MX1+	23 RJ45_MDO3-
	3 TD1-	MX1-	22 RJ45_MDO3+
	4 TCT2	MCT2	21
LAN_MDI2-	5 TD2+	MX2+	20 RJ45_MDO2-
LAN_MDI2+	6 TD2-	MX2-	19 RJ45_MDO2+
+V_DAC	7 TCT3	MCT3	18
LAN_MDI1-	8 TD3+	MX3+	17 RJ45_MDO1-
LAN_MDI1+	9 TD3-	MX3-	16 RJ45_MDO1+
	10 TCT4	MCT4	15
LAN_MDI0-	11 TD4+	MX4+	14 RJ45_MDO0-
LAN_MDI0+	12 TD4-	MX4-	13 RJ45_MDO0+

C1230 0.01U_0402_16V7K

R1219 R1220 R1221 R1222 75_0402_5% → RJ45_GND

RJ45_GND — C1227 1000P_1206_2KV7K — LANGND

@C1235 1000P_1206_2KV7K

C1232 0.1U_0402_16V4Z

C1233 4.7U_0603_6.3V6K

R1225 0_0402_5%

10/26 EMI

Security Classification	Compal Secret Data		
Issued Date	2010/3/09	Deciphered Date	2010/12/10

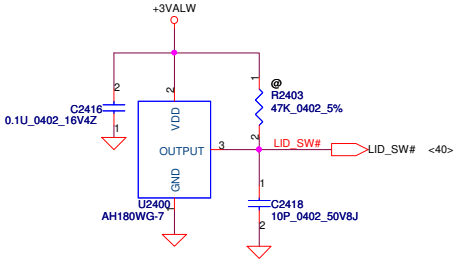
Compal Electronics, Inc.

Title: LAN Realtek RTL8111E

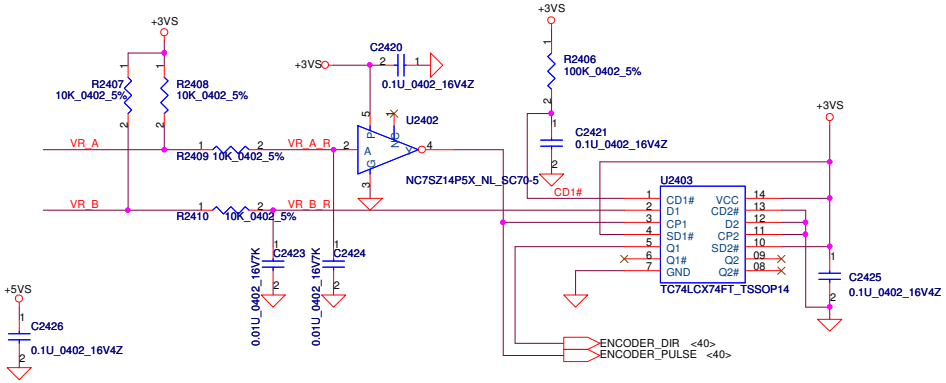
Size	Document Number	Rev
Custom	LA-6931P	1.0

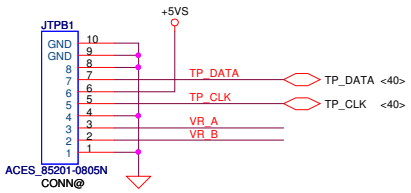
Date: Wednesday, October 27, 2010 Sheet 34 of 58

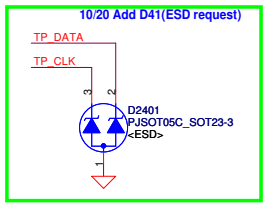
Lid Switch



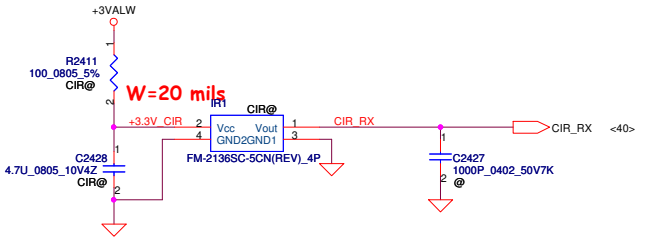
Touch Pad







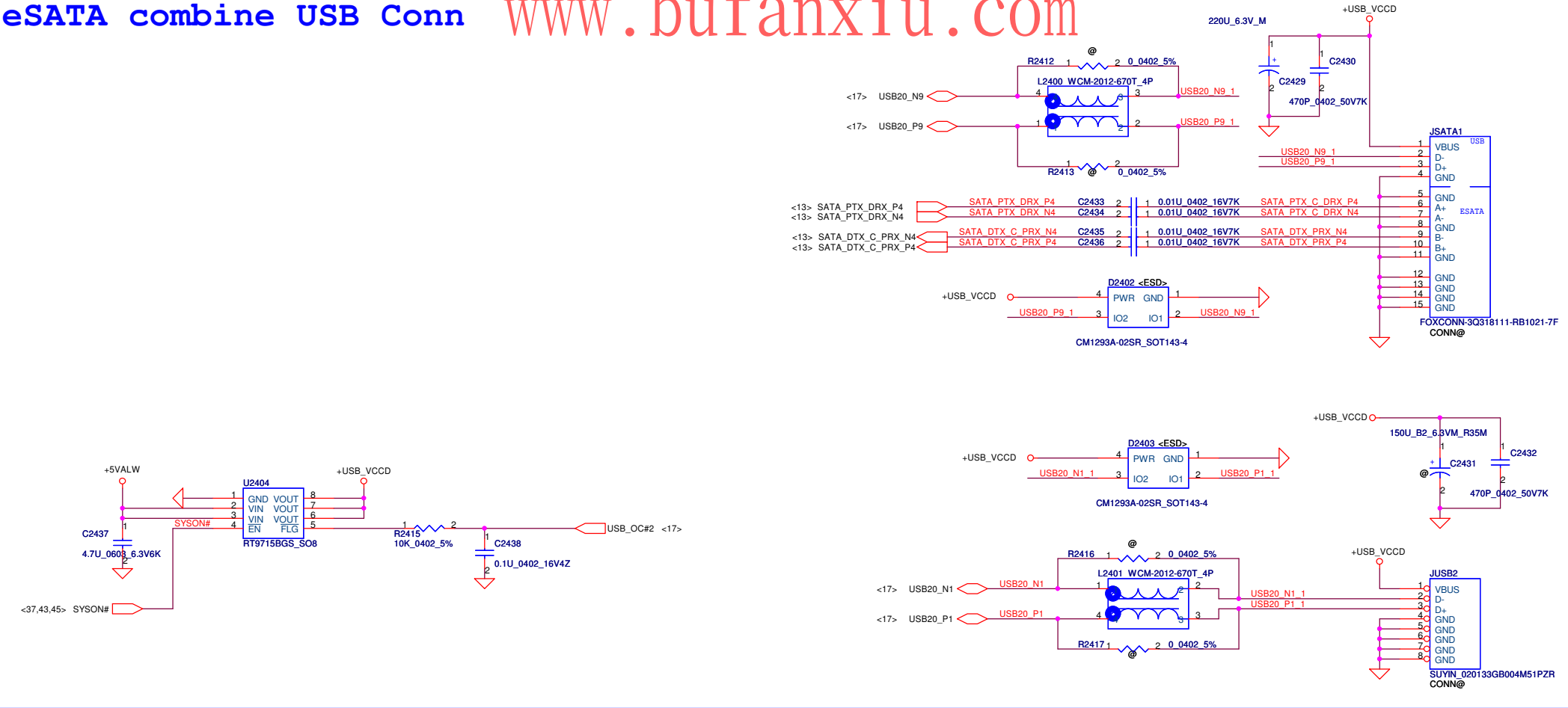
CIR



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: LID/RTC/CIR			
Size	Document Number: LA-6931P		Rev: 1.0
Date: Wednesday, October 27, 2010	Sheet 35 of 58		

eSATA combine USB Conn



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: USB / eSATA

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 36 of 58

+1.5V to +1.05V Transfer

U2413 APL5930KAI-TRG_SO8

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

U2414 RT9701-PB_SOT23-5

Close to U2407.D7

Close to U2407.P13

7K for customer request, can use other kind of capacitor, like Y5V.

For EMI request (need confirm)

DLP11TB800UL2L_4P

WCM-2012-670T_4P

D-case for customer request
can use B-case, either.

SPEC Max:+3V---200mA;+1.05V---800mA
Idle mode:0.489W:
+3V---43mA;+1.05V---328mA
D3 mode:0.066W:
+3V---5.4mA;+1.05V---45mA

PCI Express/ExpressCard select signal
1:others
0:Express Card or Mini card

Can be attach to EC, either.

As short as possible

Place as close as possible to U3.N14 and U3.M14

Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y2400,2440,C2474,C2475
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R2476,R2483

UPD720200AF1-DAP-A

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title: **USB3.0 PD720200**

Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 37 of 58

10/07

+3VS

40mil

C1300 1U_0402_6.3V6K
C1301 0.1U_0402_16V4Z
C1302 0.1U_0402_16V4Z
C1303 0.1U_0402_16V4Z

These caps close to U2 : Pin 12,37,48

Layout Note:
Place them close to U2

R5U232_XO — R1303 0_0402_5% — R5U232_XO_R
C1312 15P_0402_50V8J
X1300 24.576MHZ_16PF_7A24500022-D
R5U232_XI
C1313 15P_0402_50V8J

Memory Card Power

+3V_MCVCC

20mil

C1309 0.1U_0402_16V4Z
C1310 2.2U_0402_6.3V6
C1311 0.01U_0402_16V7K
C1327 47U_1206_6.3V6M

Layout Note:
Place them as close as possible to JREAD1
Place C1309 close to U2.36

+PCIE_PHY

C1304 10U_0805_10V4Z
C1305 0.1U_0402_16V4Z
C1306 0.1U_0402_16V4Z
C1307 0.1U_0402_16V4Z
C1308 0.1U_0402_16V4Z

These caps close to U2 : Pin 13,19,23,32,47

U2

Power
PCIE_VIN
PCIE_VIN
PCIE_VOUT
PCIE_VOUT
PCIE_VOUT
VCC_3V
VCC_3V
AVCC_3V
MF_VOUT
SD18C

PCIe
PERST#
REFCLKP
REFCLKN
RXP
RXN
TXP
TXN
RXC
CPO
RREF
UDIO1
UDIO2
UDIO3

IEEE1394
TPAP0 — IEEE1394_TPAP0
TPAN0 — IEEE1394_TPAN0
TPBP0 — IEEE1394_TPBP0
TPBN0 — IEEE1394_TPBN0
TPBIAS0 — IEEE1394_TPBIAS0
XI — R5U232_XO
XO — R5U232_XI

CardReader
MFCD0# — XDCD0# SDCD#
MFCD1# — XDCD1# MSCD#
MDIF00 — XD_D6_SD_D1_R
MDIF01 — XD_D5_SD_D0_R
MDIF02 — XD_D4_MS_D1
MDIF03 — XD_D3
MDIF04 — XD_D2_SDCLK_R
MDIF05 — XD_D1_MS_D0
MDIF06 — XD_D0
MDIF07 — XDWP_SDCMD_R
MDIF08 — XDWE#_MS_D2
MDIF09 — XD_ALE_SD_D3_R
MDIF10 — XD_CLE_SD_D2_R
MDIF11 — XDCE_MD_D3
MDIF12 — XD_RE
MDIF13 — XD_RB_MSCLK_R
MDIF14
TEST
GPAD

GND

R5U232-QFN48P_QFN48_6X6

+PCIE_PHY
+3VS
+3V_MCVCC
2A max
C1314 1U_0402_6.3V6K
XRSTN

Layout Note:
Add GND shield for Xtal
GND
GND

Impedance: 50 ohm (Microstrip)

XD_D2_SDCLK — R1304 30_0402_5% — Shield GND
C1316 10P_0402_50V8J — Shield GND
XD_RB_MSCLK — R1307 30_0402_5% — Shield GND
C1320 10P_0402_50V8J — Shield GND

<14> CLK_PCIE_READER#
<14> CLK_PCIE_READER
<14> PCIE_PTX_C_DRX_P5
<14> PCIE_PTX_C_DRX_N5
<14> PCIE_PRX_C_DTX_P5
<14> PCIE_PRX_C_DTX_N5
<14> CR_CLKREQ#

C1315 0.1U_0402_10V7K
C1317 0.1U_0402_10V7K
C1318 0.022UF_0402_16V7
C1319 1500P_0402_50V7K
R1305 5.1K_0402_1%
R1306 10K_0402_5%
R1308 47K_0402_5%

SROM Select: UDIO 2
Pull-Hi: Enable
Pull-Lo: Disable (Current Setting)

GND pad under IC Chip.
5 GND vias required at GND pad.
Pin 21 connect to GND pad on IC-mounted layer.

5 IN 1 CardRead

JREAD1

+3V_MCVCC
XD_D0
XD_D1_MS_D0
XD_D2_SDCLK
XD_D3
XD_D4_MS_D1
XD_D5_SD_D0
XD_D6_SD_D1
XD_D7_MSBS_SDWP
XDWE#_MS_D2
XDWP_SDCMD
XD_ALE_SD_D3
XD_CD#
XD_RB_MSCLK
XD_RE
XDCE_MD_D3
XD_CLE_SD_D2
XD GND
XD GND
SD CD/WP GND
SD CD/WP GND

XD-VCC
XD10-D0
XD11-D1
XD12-D2
XD13-D3
XD14-D4
XD15-D5
XD16-D6
XD17-D7
XD07-WE
XD08-WP
XD06-ALE
XD01-CD
XD02-R/B
XD03-RE
XD04-CE
XD05-CLE

SD4-VDD
MS9-VCC
SD5-CLK
SD7-DAT0
SD8-DAT1
SD9-DAT2
SD1-DAT3
SD2-CMD
SD-CD
SD-WP
SD6-VSS
SD3-VSS
MS8-SCLK
MS4-DATA0
MS3-DATA1
MS5-DATA2
MS7-DATA3
MS6-INS
MS2-BS
MS1-VSS
MS10-VSS

+3V_MCVCC
XD_D2_SDCLK
XD_D5_SD_D0
XD_D6_SD_D1
XD_CLE_SD_D2
XD_ALE_SD_D3
XDWP_SDCMD
XDCD0# SDCD#
XD_D7_MSBS_SDWP
XD_RB_MSCLK
XD_D1_MS_D0
XD_D4_MS_D1
XDWE#_MS_D2
XDCE_MD_D3
XDCD1# MSCD#
XD_D7_MSBS_SDWP

T-SOL_144-1300302600_NR
CONN@

<17,39> PLT_RST_BUF# — PLT_RST_BUF# — R1313 100_0402_5% — XRSTN
C1322 0.1U_0402_16V4Z

Layout Note:
Place them close to U2

XD_D5_SD_D0_R — R1320 30_0402_5% — XD_D5_SD_D0
XD_D6_SD_D1_R — R1321 30_0402_5% — XD_D6_SD_D1
XD_CLE_SD_D2_R — R1322 30_0402_5% — XD_CLE_SD_D2
XD_ALE_SD_D3_R — R1323 30_0402_5% — XD_ALE_SD_D3
XDWP_SDCMD_R — R1324 30_0402_5% — XDWP_SDCMD

Layout Note:
Add GND shield for 1394.

Layout Note:
Place them as close as possible to U2

C1321 270P_0402_50V7K
R1309 5.1K_0402_1%
R1310 56_0402_5%
R1317 56_0402_5%

IEEE1394_TPBN0 — R1312 0_0402_5% — IEEE1394_TPBN0_R
IEEE1394_TPBP0 — R1315 0_0402_5% — IEEE1394_TPBP0_R
IEEE1394_TPAN0 — R1316 0_0402_5% — IEEE1394_TPAN0_R
IEEE1394_TPAP0 — R1319 0_0402_5% — IEEE1394_TPAP0_R

J1394A
TPB- GND
TPB+ GND
TPA- GND
TPA+ GND
SUYIN_020015FB004S515ZL
CONN@

Layout Note:
Place them as close as possible to JP1394
Reserve them for test
if any EMI issue.

Layout Note:
Differential pair impedance=110+-6 Ohm
TPAP/N0 and TPBP/N0 mismatch <5mil

IEEE1394_TPBIAS0
R1318 56_0402_5%
R1317 56_0402_5%
C1328 0.01U_0402_16V7K
C1326 0.33U_0603_10V7K
@

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	–	D6
02	D0	–	D5
03	D7	D1	D4
04	D6	D5	D3
05	**CLK**	–	D2
06	–	D0	D1
07	D5	D4	D0
08	CMD	–	WP#
09	D4	D2	WE#
10	D3	D6	ALE
11	D2	–	CLE
12	–	D3	CE#
13	–	D7	RE#
14	–	**CLK**	R/B#

+3VS
R1314 47K_0402_5%
XD_CD#
XDCD0# SDCD#
XDCD1# MSCD#
D1300 DAN202UT106_SC70-3
C1323 270P_0402_50V7K
C1324 270P_0402_50V7K
C1325 270P_0402_50V7K

When these pins are both set to Low, the xD Picture Card is detected.

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

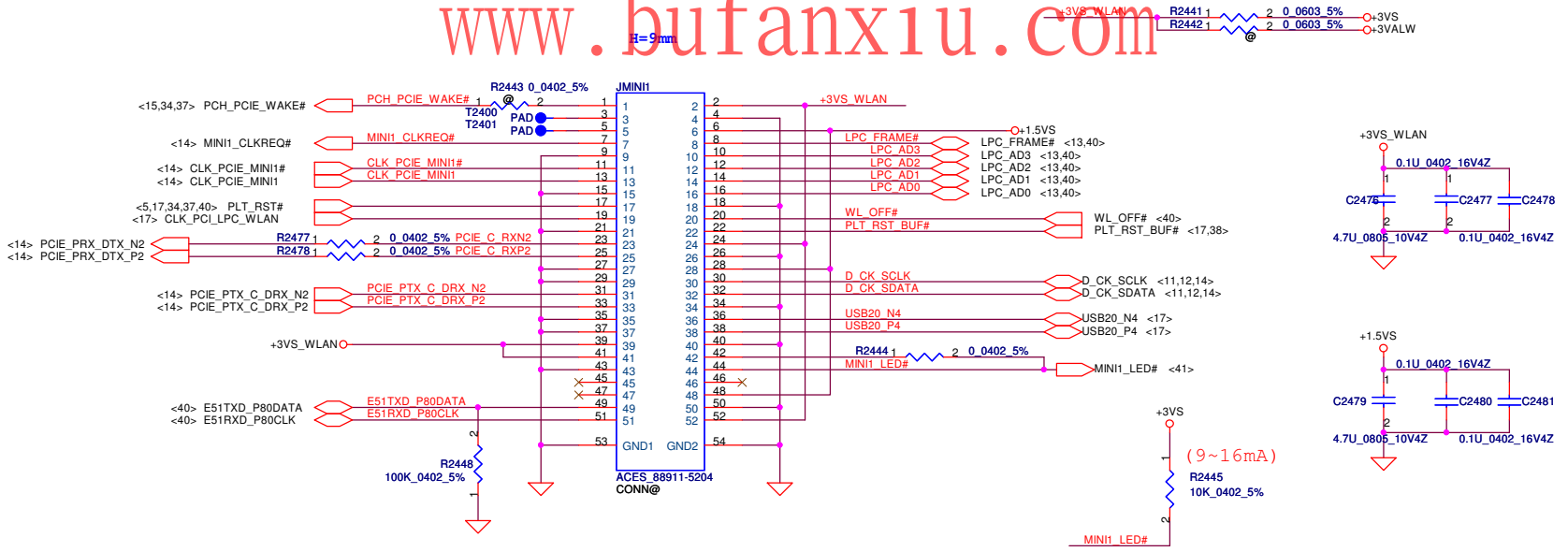
Compal Electronics, Inc.

Title: R5U232

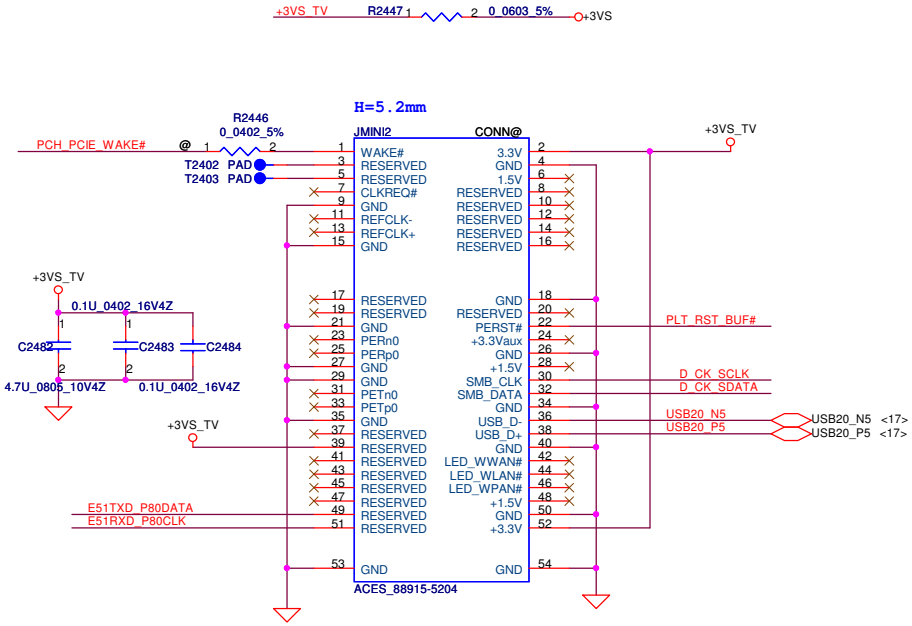
Size: Custom | Document Number: LA-6931P | Rev: 1.0

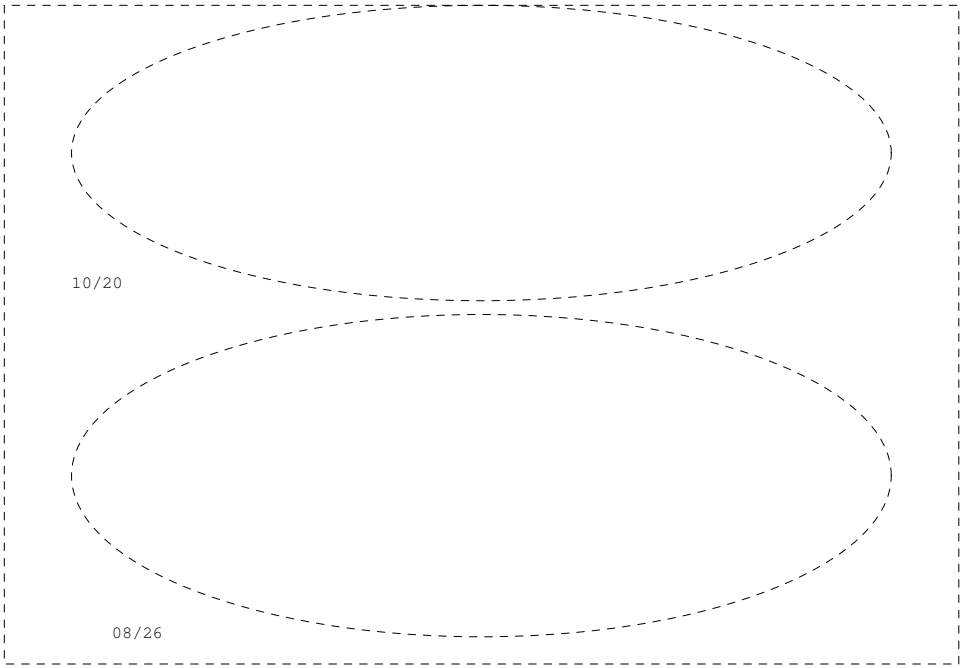
Date: Wednesday, October 27, 2010 | Sheet 38 of 58

WLAN



MINI





Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **WLAN&MINI**

Size	Document Number	Rev
Custom	LA-6931P	1.0

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R2237 2 10K_0402_5% PCH_PWROK
R2232 2 10K_0402_5% PCH_APWROK
R2207 2 10K_0402_5% VR_ON
R2227 2 100K_0402_5% PLT_RST#

@C2207 22P_0402_50V8J
@R2206 33_0402_5%
CLK_PCI_LPC

+3VALW R2208 2 47K_0402_5% EC_RST#
C2208 2 0.1U_0402_16V4Z

+3VALW
10/1 ENE Recommand
R2210 1 2 47K_0402_5% KSO1
R2211 1 2 47K_0402_5% KSO2
8/31
R2213 1 2 10K_0402_5% EC_SMI#
R2215 1 2 2.2K_0402_5% EC_SMB_DA1
R2216 1 2 2.2K_0402_5% EC_SMB_CK1
@ C2211 22P_0402_50V8J
@R2217 33_0402_5%
Reserve for EMI please close to U38

+3VS
R2218 1 2 2.2K_0402_5% EC_SMB_CK2
R2219 1 2 2.2K_0402_5% EC_SMB_DA2
R2224 1 2 10K_0402_5% EC_SCI#
R2238 1 2 10K_0402_5% ENCODER_PULSE

EC_XCLK1 EC_XCLK0
C2213 15P_0402_50V8J
C2214 15P_0402_50V8J
Y2200 32.768KHZ_12.5PF_Q13MC14610002

Board ID
Analog Board ID definition, Please see page 3.
+3VALW
Ra R2230 100K_0402_5%
AD_BID0
Rb R2231 33K_0402_5%
C2217 0.1U_0402_16V4Z
9/24

+3VALW R2200 0_0805_5%
C2200 0.1U_0402_16V4Z
C2201 0.1U_0402_16V4Z
C2202 0.1U_0402_16V4Z
C2203 0.1U_0402_16V4Z
C2204 100P_0402_50V7K
C2205 100P_0402_50V7K
+3VALW_EC
L2200 FBMA-L11-160808-800LMT_0603
+EC_VCCA
C2206 0.1U_0402_16V4Z
ECAGND
VCC 9, VCC 33, VCC 96, VCC 111, VCC 125, AVCC 67

U38

<18> GATEA20 — GATEA20 1 — GA20/GPIO00
<18> EC_KBRST# — EC_KBRST# 2 — KBRST#/GPIO01
<13> SERIRQ — SERIRQ 3 — SERIRQ#
<13,39> LPC_FRAME# — LPC_FRAME# 4 — LFRAME#
<13,39> LPC_AD3 — LPC_AD3 5 — LAD3
<13,39> LPC_AD2 — LPC_AD2 7 — LAD2
<13,39> LPC_AD1 — LPC_AD1 8 — LAD1
<13,39> LPC_AD0 — LPC_AD0 10 — LAD0
LPC & MISC
<17> CLK_PCI_LPC — CLK_PCI_LPC 12 — PCICLK
<5,17,34,37,39> PLT_RST# — PLT_RST# 13 — PCIRST#/GPIO05
EC_RST# 37 — ECRST#
<18> EC_SCI# — EC_SCI# 20 — SCI#/GPIO0E
<44> FP_LED# — FP_LED# 38 — CLKRUN#/GPIO1D

<41> KSI[0..7] — KSI[0..7] — KSI0 55 … KSI7 62 — KSI0/GPIO30 … KSI7/GPIO37
<41> KSO[0..17] — KSO[0..17] — KSO0 39 … KSO17 82 — KSO0/GPIO20 … KSO17/GPIO49
Int. K/B Matrix

<50> EC_SMB_CK1 — EC_SMB_CK1 77 — SCL1/GPIO44
<50> EC_SMB_DA1 — EC_SMB_DA1 78 — SDA1/GPIO45
<14,23> EC_SMB_CK2 — EC_SMB_CK2 79 — SCL2/GPIO46
<14,23> EC_SMB_DA2 — EC_SMB_DA2 80 — SDA2/GPIO47
SM Bus

<15> PM_SLP_S3# — PM_SLP_S3# 6 — PM_SLP_S3#/GPIO04
<15> PM_SLP_S5# — PM_SLP_S5# 14 — PM_SLP_S5#/GPIO07
<18> EC_SMI# — EC_SMI# 15 — EC_SMI#/GPIO08
<34> EC_PME# — EC_PME# 16 — LID_SW#/GPIO0A
<30> PWR_SAVE_LED# — PWR_SAVE_LED# 17 — SUSP#/GPIO0B
<39> WL_OFF# — WL_OFF# 18 — PBTN_OUT#/GPIO0C
<15> SUSWARN# — SUSWARN# 19 — EC_PME#/GPIO0D
<30> INVT_PWM — INVT_PWM 25 — EC_THERM#/GPIO11
<44> FAN_SPEED1 — FAN_SPEED1 28 — FAN_SPEED1/FANFB1/GPIO14
<45> PCH_PWR_EN — PCH_PWR_EN 29 — FANFB2/GPIO15
<39> E51TXD_P80DATA — E51TXD_P80DATA 30 — EC_TX/GPIO16
<39> E51RXD_P80CLK — E51RXD_P80CLK 31 — EC_RX/GPIO17
<41> ON/OFF — ON/OFF 32 — ON_OFF/GPIO18
<41> PWR_SUSP_LED# — PWR_SUSP_LED# 34 — PWR_LED#/GPIO19
<41> NUM_LED# — NUM_LED# 36 — NUMLED#/GPIO1A
GPIO

<15> SUSCLK — R2229 0_0402_5% — EC_XCLK1 122 — XCLK1
EC_XCLK0 123 — XCLK0
close to U38

GND 11, GND 24, GND 35, GND 94, GND 113, AGND 69
KB930QF A1 LQFP 128P
20mil
ECAGND — L2201 FBMA-L11-160808-800LMT_0603

PWM Output
INVT_PWM/PWM1/GPIO0F — FAN_PWM 21 — FAN_PWM <44>
BEEP#/PWM2/GPIO10 — BEEP# 23 — BEEP# <42>
FANPWM1/GPIO12 — PCH_DPWROK 26 — PCH_DPWROK <15>
ACOFF/FANPWM2/GPIO13 — ACOFF 27 — ACOFF <47,48>

AD Input
BATT_TEMP/AD0/GPIO38 — BATT_TEMP 63 — BATT_TEMP <50>
BATT_OVP/AD1/GPIO39 — AD_BID0 64
ADP_I/AD2/GPIO3A — ADP_I 65 — ADP_I <48,50>
AD3/GPIO3B — ARCADE_BTN 66 — ARCADE_BTN# <30>
AD4/GPIO42 — ENCODER_PULSE 75 — ENCODER_PULSE <35>
SELIO2#/AD5/GPIO43 — IMON_R 76 — R2212 0_0402_5% — IMVP_IMON <56>
C2209 100P_0402_50V8J ECAGND

DA Output
DAC_BRIG/DA0/GPIO3C — 65W/90W# 68 — 65W/90W# <48,50>
EN_DFAN1/DA1/GPIO3D — IREF 71 — IREF <48>
IREF/DA2/GPIO3E — CALIBRATE# 72 — CALIBRATE# <48>
DA3/GPIO3F

PS2 Interface
PSCLK1/GPIO4A — EC_MUTE# 83 — EC_MUTE# <43>
PSDAT1/GPIO4B — 3S/4S# 84 — 3S/4S# <48>
PSCLK2/GPIO4C — BACKUP_LED# 85 — BACKUP_LED# <41>
PSDAT2/GPIO4D — H_PROCHOT# 86 — H_PROCHOT# EC
TP_CLK/PSCLK3/GPIO4E — TP_CLK 87 — TP_CLK <35>
TP_DATA/PSDAT3/GPIO4F — TP_DATA 88 — TP_DATA <35>

SPI Device Interface
SDICS#/GPXOA00 — GFX_CORE_PWRGD 97 — GFX_CORE_PWRGD <56>
SDICLK/GPXOA01
SDIDO/GPXOA02 — HDA_SDO 99 — HDA_SDO <13>
SDIDI/GPXID0 — LID_SW# 109 — LID_SW# <35>

SPI Flash ROM
SPIDI/RD# — FRD# R 119 — R2220 1 2 0_0402_5% FRD#
SPIDO/WR# — FWR# R 120 — R2221 1 2 33_0402_5% FWR#
SPICLK/GPIO58 — SPI_CLK R 126 — R2223 1 2 33_0402_5% SPI_CLK
SPICS# — FSEL# R 128 — R2225 1 2 33_0402_5% FSEL#

GPIO
CIR_RX/GPIO40 — EC_RCIRRX 73
CIR_RLC_TX/GPIO41 — EC_PECI 74 — R2226 1 2 43_0402_1% H_PECI <5,18>
FSTCHG/SELIO#/GPIO50 — FSTCHG 89 — FSTCHG <48>
BATT_CHGI_LED#/GPIO52 — BATT_AMB_LED# 90 — BATT_AMB_LED# <41>
CAPS_LED#/GPIO53 — CAPS_LED# 91 — CAPS_LED# <41>
BATT_LOW_LED#/GPIO54 — BATT_BLUE_LED# 92 — BATT_BLUE_LED# <41>
SUSP_LED#/GPIO55 — PWR_LED# 93 — PWR_LED# <41>
SYSON/GPIO56 — SYSON 95 — SYSON <37,45,51>
VR_ON/XCLK32K/GPIO57 — VR_ON 121 — VR_ON <56>
AC_IN/GPIO59 — EC_ACIN 127 — EC_ACIN <56>

GPO
EC_RSMRST#/GPXO03 — PCH_RSMRST# 100 — PCH_RSMRST# <15>
EC_LID_OUT#/GPXO04 — LID_SW_OUT# 101 — LID_SW_OUT# <14>
EC_ON/GPXO05 — EC_ON 102 — EC_ON <41,49>
EC_SWI#/GPXO06 — RF_DISABLE# 103 — RF_DISABLE# <43>
ICH_PWROK/GPXO06 — PCH_PWROK 104 — PCH_PWROK <15>
BKOFF#/GPXO08 — BKOFF# 105 — BKOFF# <30>
WL_OFF#/GPXO09 — CPU1.5V_S3_GATE 106 — CPU1.5V_S3_GATE <9>
GPXO10 — PCH_APWROK 107 — PCH_APWROK <15>
GPXO11 — SA_PGOOD 108 — SA_PGOOD <52>

GPI
PM_SLP_S4#/GPXID1 — PM_SLP_S4# 110 — PM_SLP_S4# <15>
ENBKL/GPXID2 — ENBKL 112 — ENBKL <16>
GPXID3 — EAPD 114 — EAPD <42>
GPXID4 — POWER_SMART# 115 — POWER_SMART# <30>
GPXID5 — SUSP# 116 — SUSP# <9,45,46,51,53>
GPXID6 — PBTN_OUT# 117 — PBTN_OUT# <15>
GPXID7 — ENCODER_DIR 118 — ENCODER_DIR <35>

V18R — +V18R 124 — C2216 4.7U_0805_10V4Z

For WLAN Switch
SW3 NTC317-AB1G-C220C_2P
For Back up Key Switch
SW4 NTC317-AB1G-C220C_2P
09/08

+3VALW
EC_MUTE# R2201 2 @ 1 10K_0402_5%
65W/90W# R2202 2 1 100K_0402_5%
3S/4S# R2203 2 1 100K_0402_5%
+5VS
TP_CLK R2204 1 2 4.7K_0402_5%
TP_DATA R2205 1 2 4.7K_0402_5%

+3VALW
R2209 2 1 200K_0402_5%
D2200 2 1 CH751H-40PT_SOD323-2 ACIN <15,45,48>
EC_ACIN C2210 2 1 100P_0402_50V8J

+3VS
C2218 0.1U_0402_16V4Z
10/02
Follow PAW00
U2202 SN74LVC1G06DCKR_SC70-5
H_PROCHOT# EC
R2240 100K_0402_5%
R2214 0_0402_5%
VR_HOT# <56>
H_PROCHOT# <5,50>

+3VALW
LID_SW# R2222 2 1 100K_0402_5%

+3VALW
R2239 10K_0402_5%
D2201 CH751H-40PT_SOD323-2
<35> CIR_RX
EC_RCIRRX
08/26

SPI ROM
+3VALW
C2212 0.1U_0402_16V4Z
U2201 1M W25X10BVSNIG SOP 8P
20mils
VCC VSS W HOLD FSEL# SPI_CLK FWR# FRD#
@R2228 22_0402_5%
@C2215 100P_0402_50V8J
SPI_CLK_R
Reserve for EMI please close to U2201

+3VALW
<23> ACIN_BUF
U28 NC7SZ08P5X_NL_SC70-5
EC_ACIN

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.
Title: EC ENE-KB930
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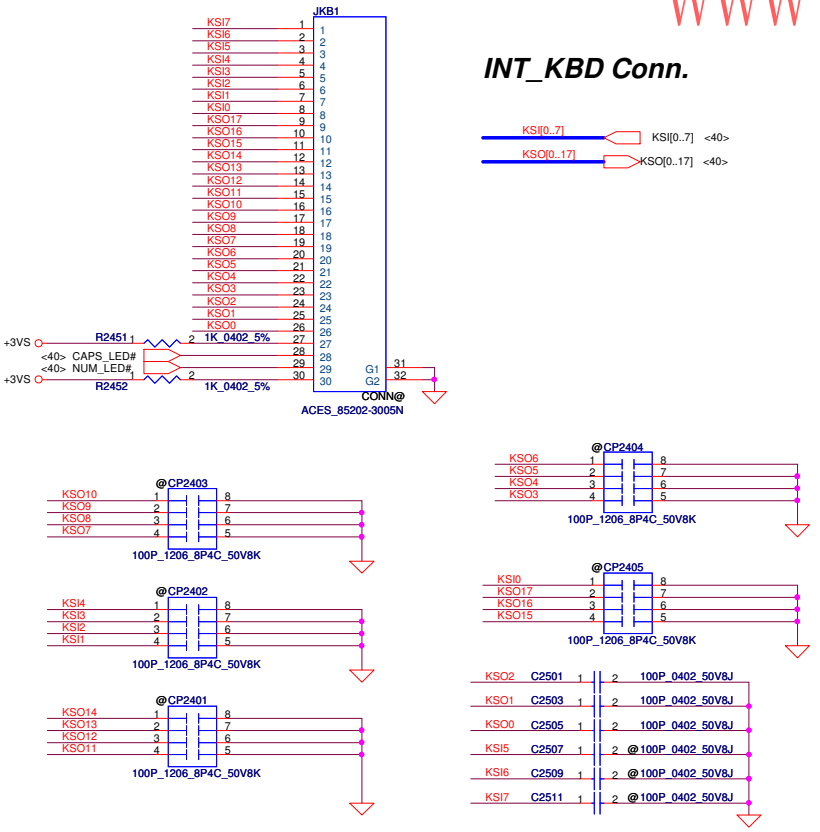
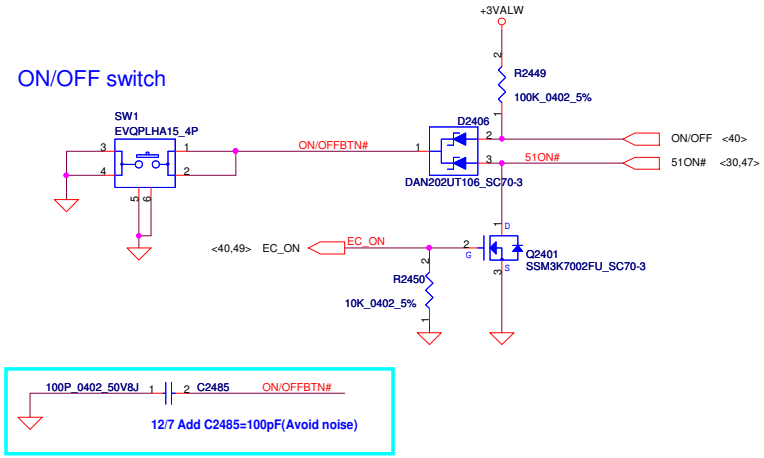
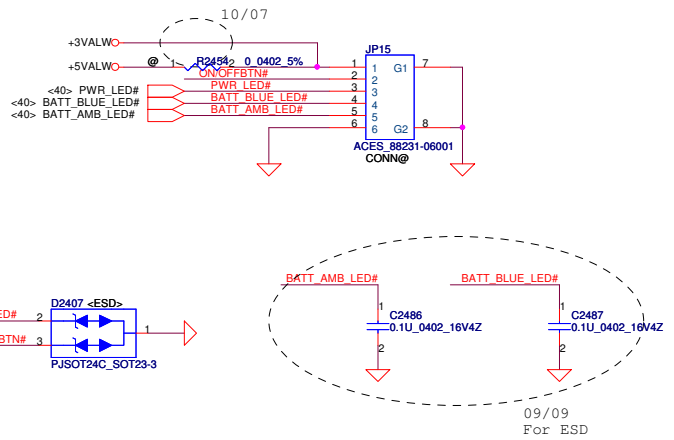
INT_KBD Conn.



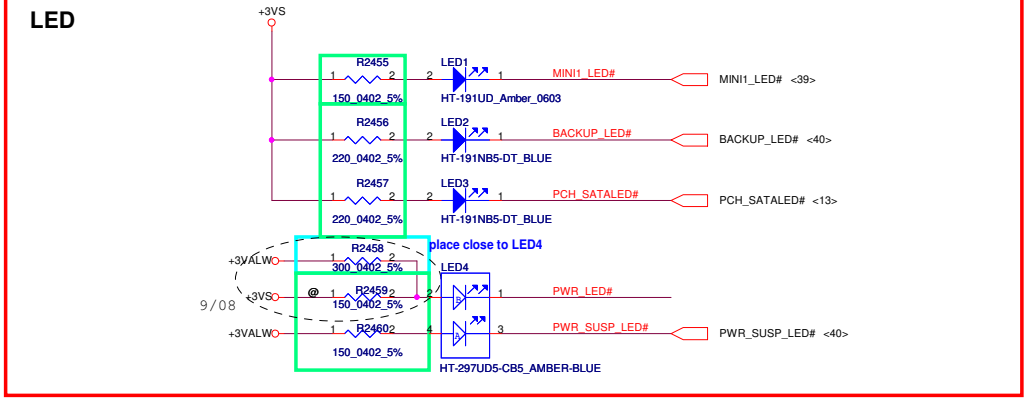
Power Button



Power Conn



LED



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Power OK, I/O Port & K/B Connector

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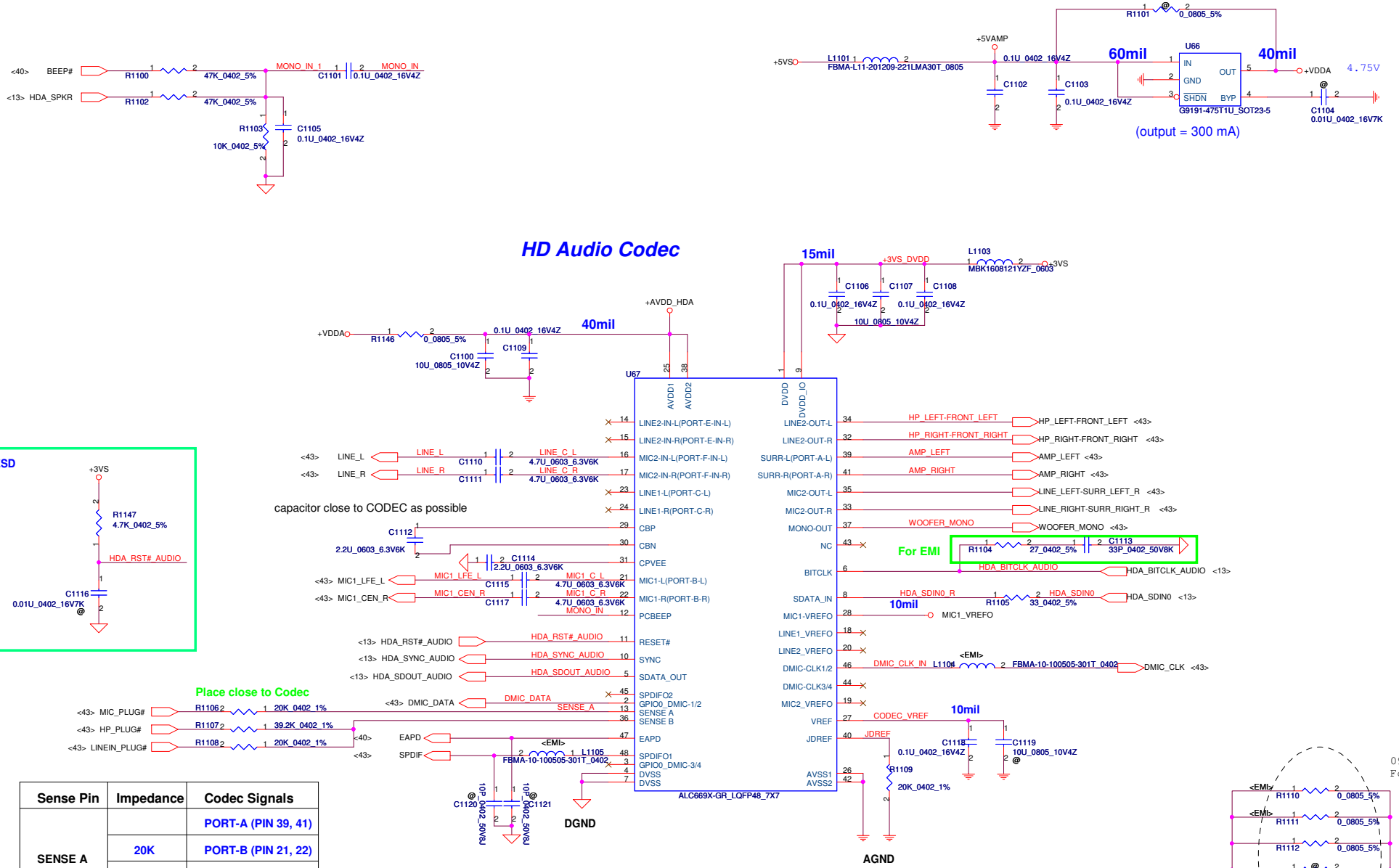

Sense Pin	Impedance	Codec Signals
SENSE A		PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: HD Audio Codec ALC669X

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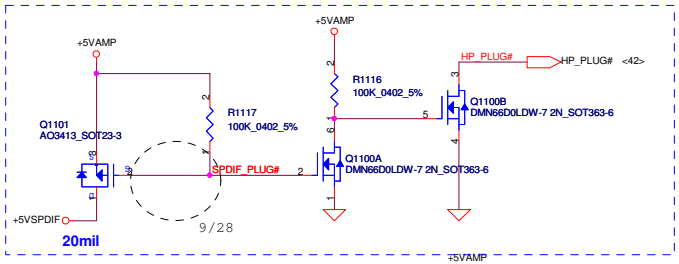
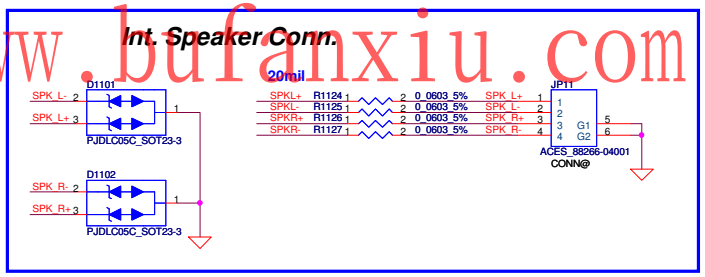
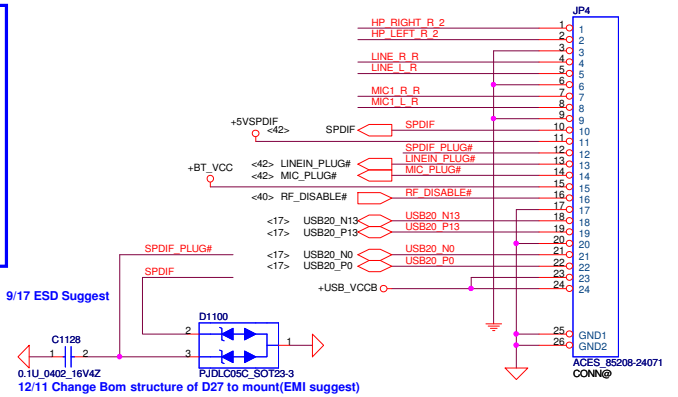
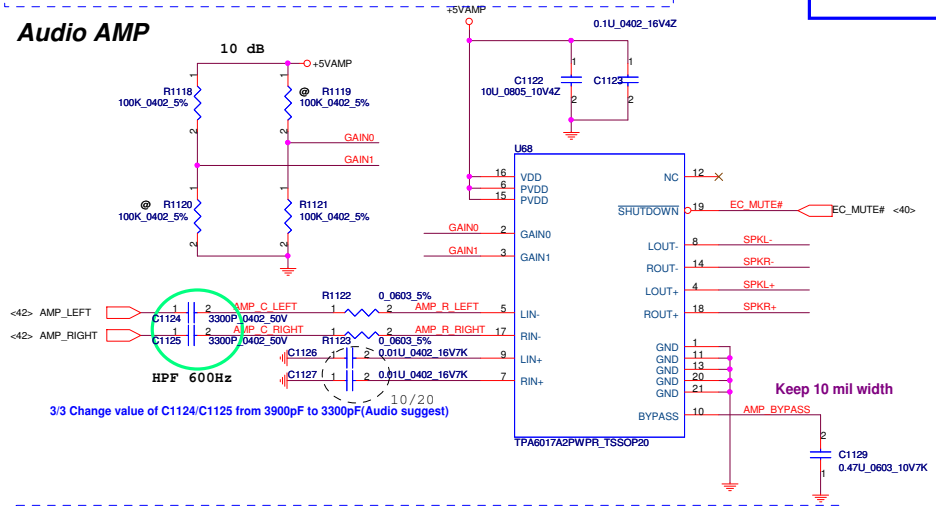


Int. Speaker Conn.



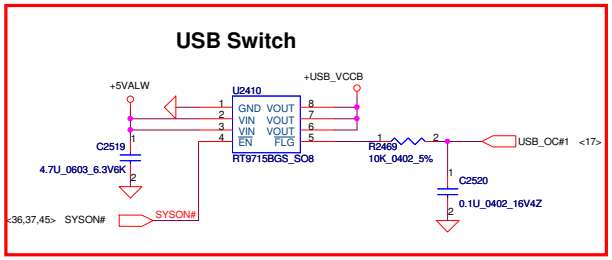


Audio AMP

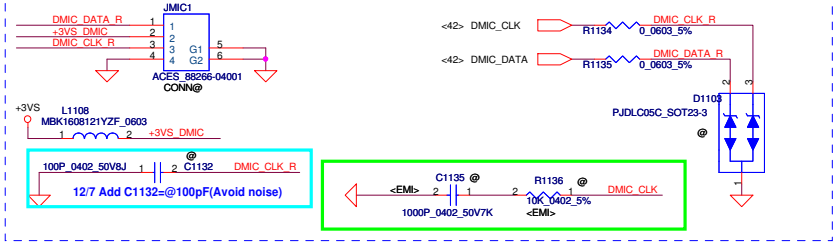


3/3 Change value of C1124/C1125 from 3900pF to 3300pF(Audio suggest)

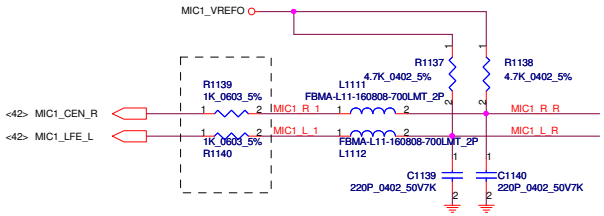
USB Switch



Digital MIC CONN

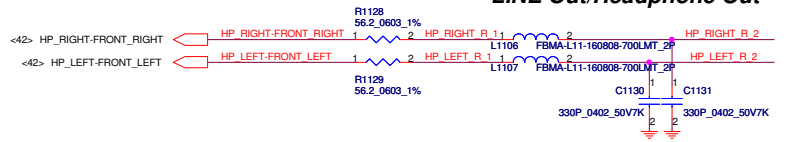


MIC JACK

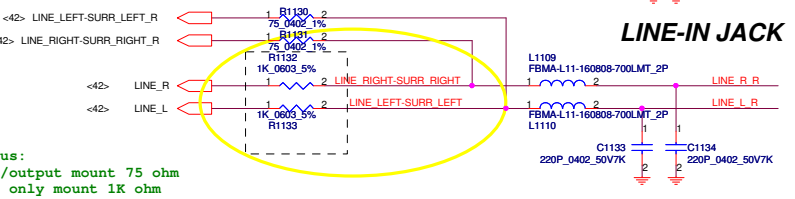


S/PDIF Out JACK

LINE Out/Headphone Out

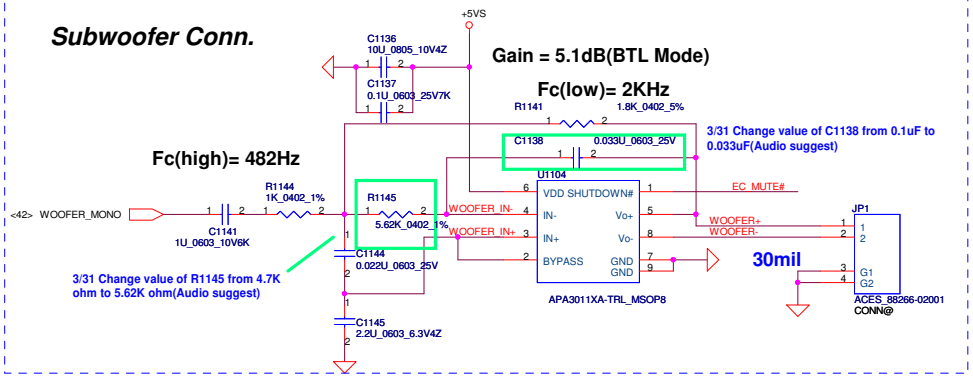


LINE-IN JACK



For ESD
I/O status:
a. input/output mount 75 ohm
b. input only mount 1K ohm

Subwoofer Conn.



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Amplifier & Audio Jack&USB

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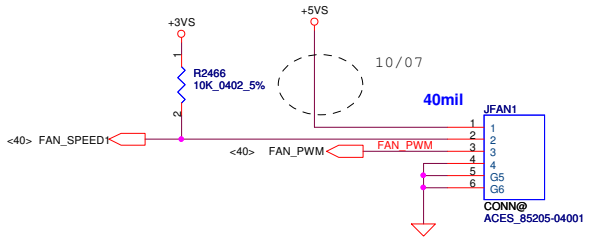
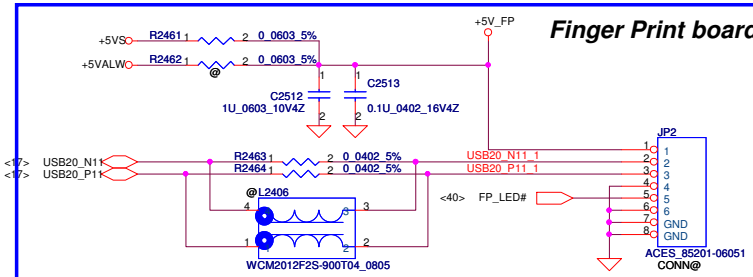
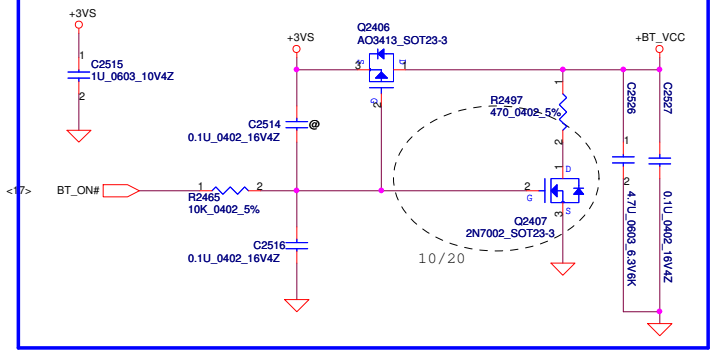
FAN1 Conn



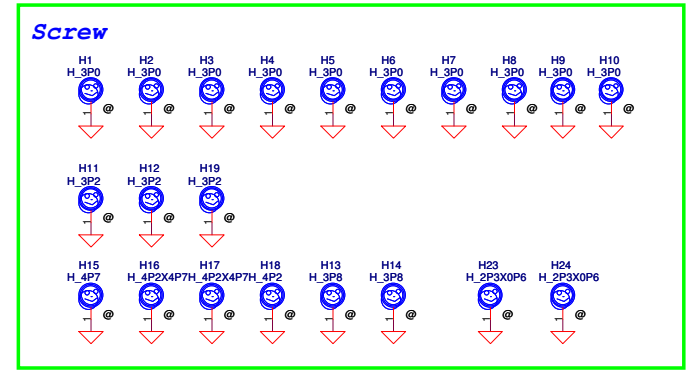
Finger Print board



BT

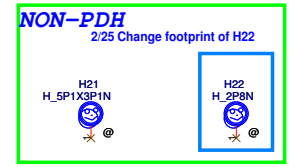


Screw



NON-PDH

2/25 Change footprint of H22



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
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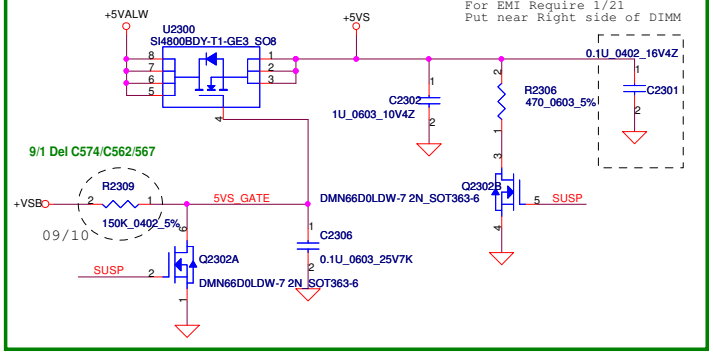
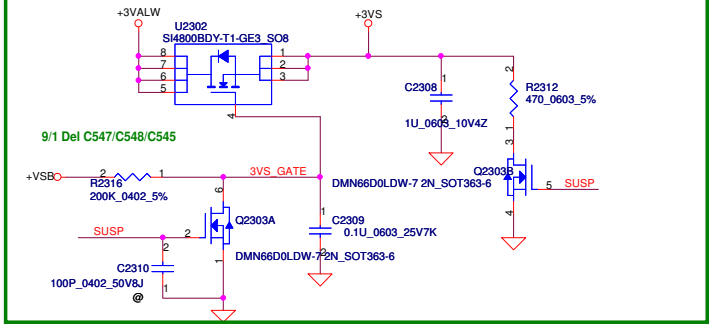
+5VALW TO +5VS

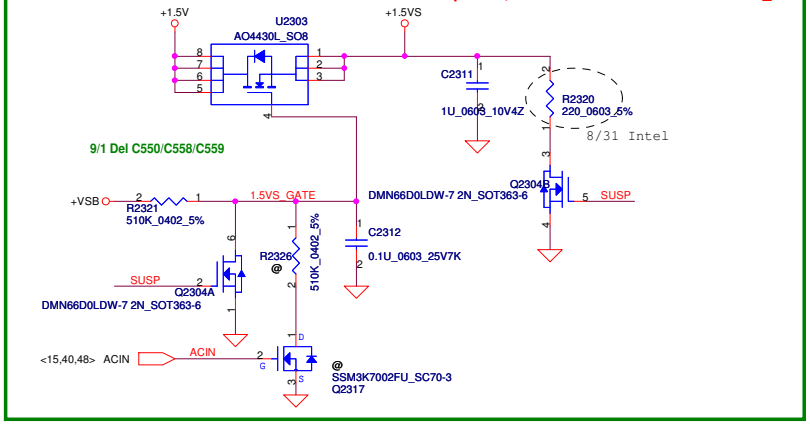


+3VALW TO +3VS



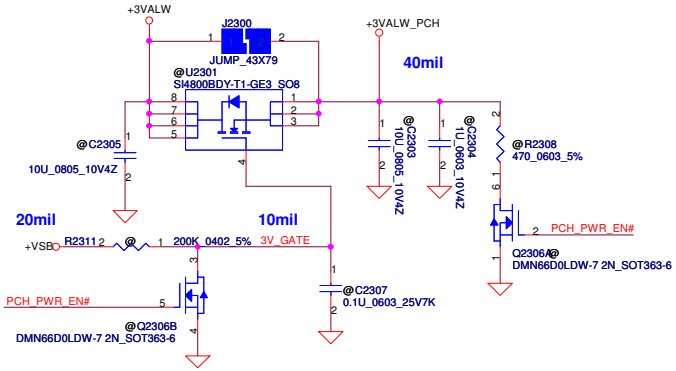
+1.5V to +1.5VS

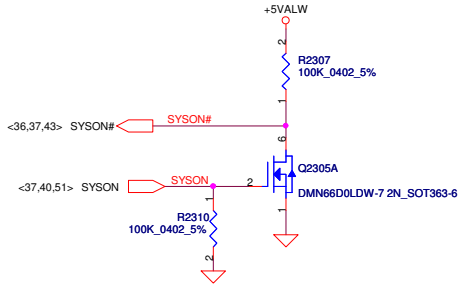
Optional, if +1.5VS can combine with +1.5V_1

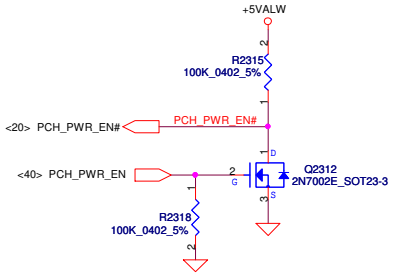


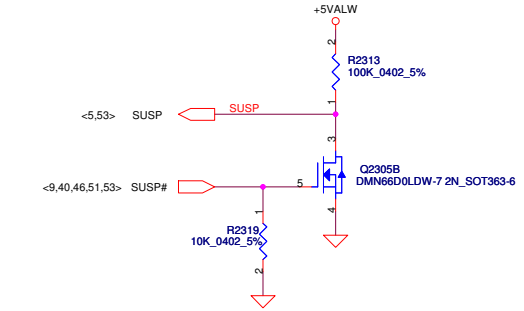
+3VALW TO +3VALW(PCH AUX Power)

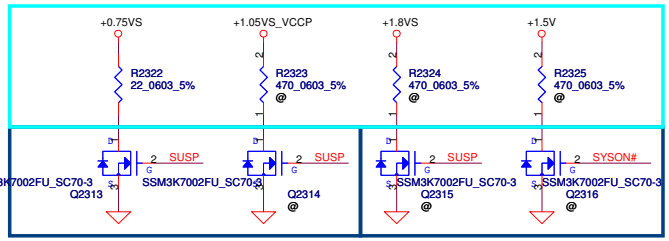
Short J5 for PCH VCCSUS3.3











Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	LA-6931P	1.0

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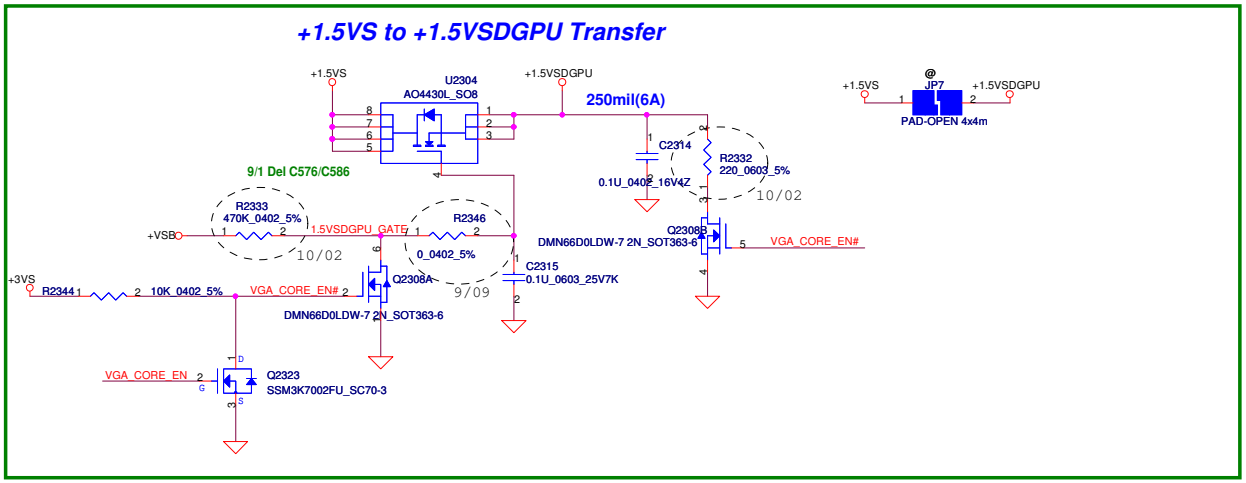
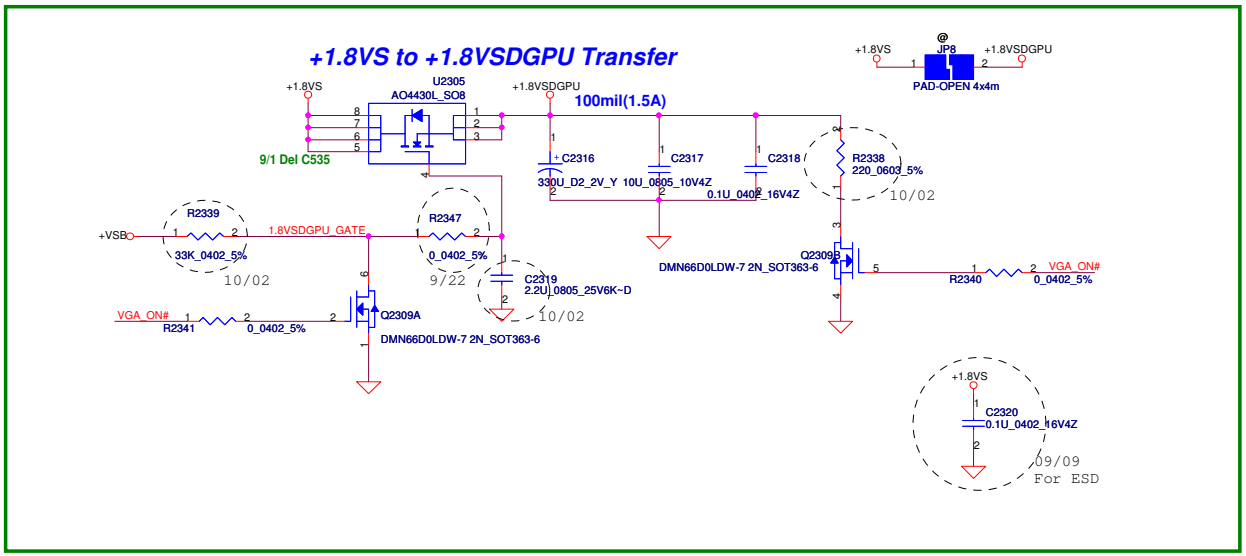
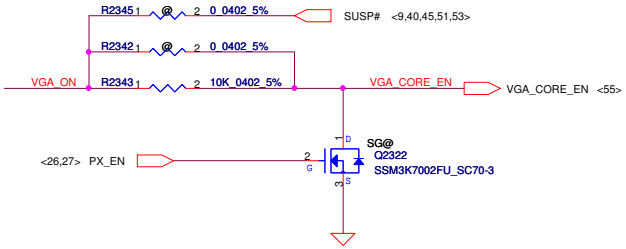
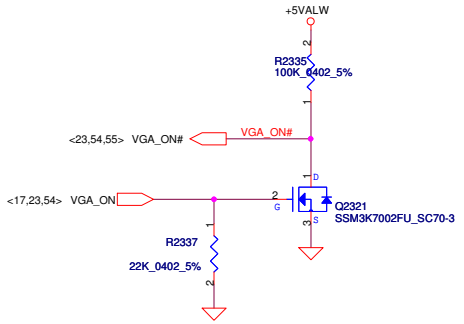
+1.5VS to +1.5VSDGPU Transfer



+1.8VS to +1.8VSDGPU Transfer







Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: VGA DC Interface

Size	Document Number	Rev
B	LA-6931P	1.0

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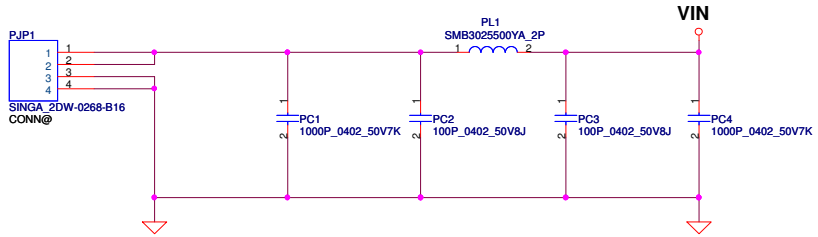
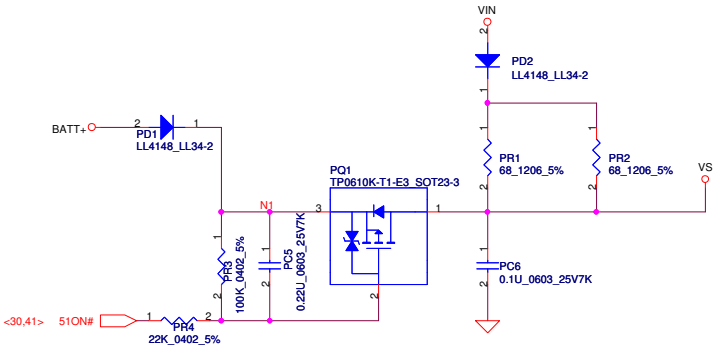
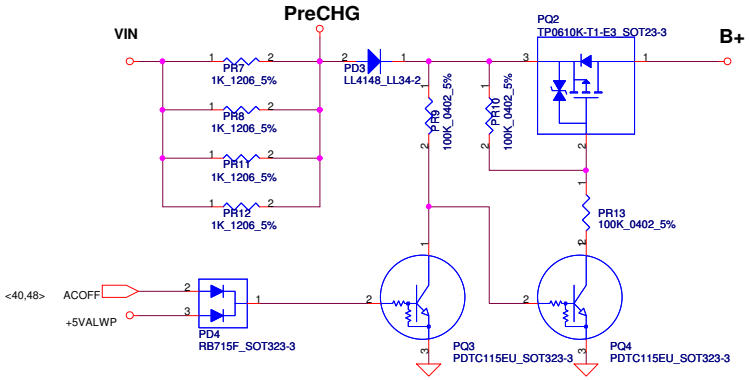






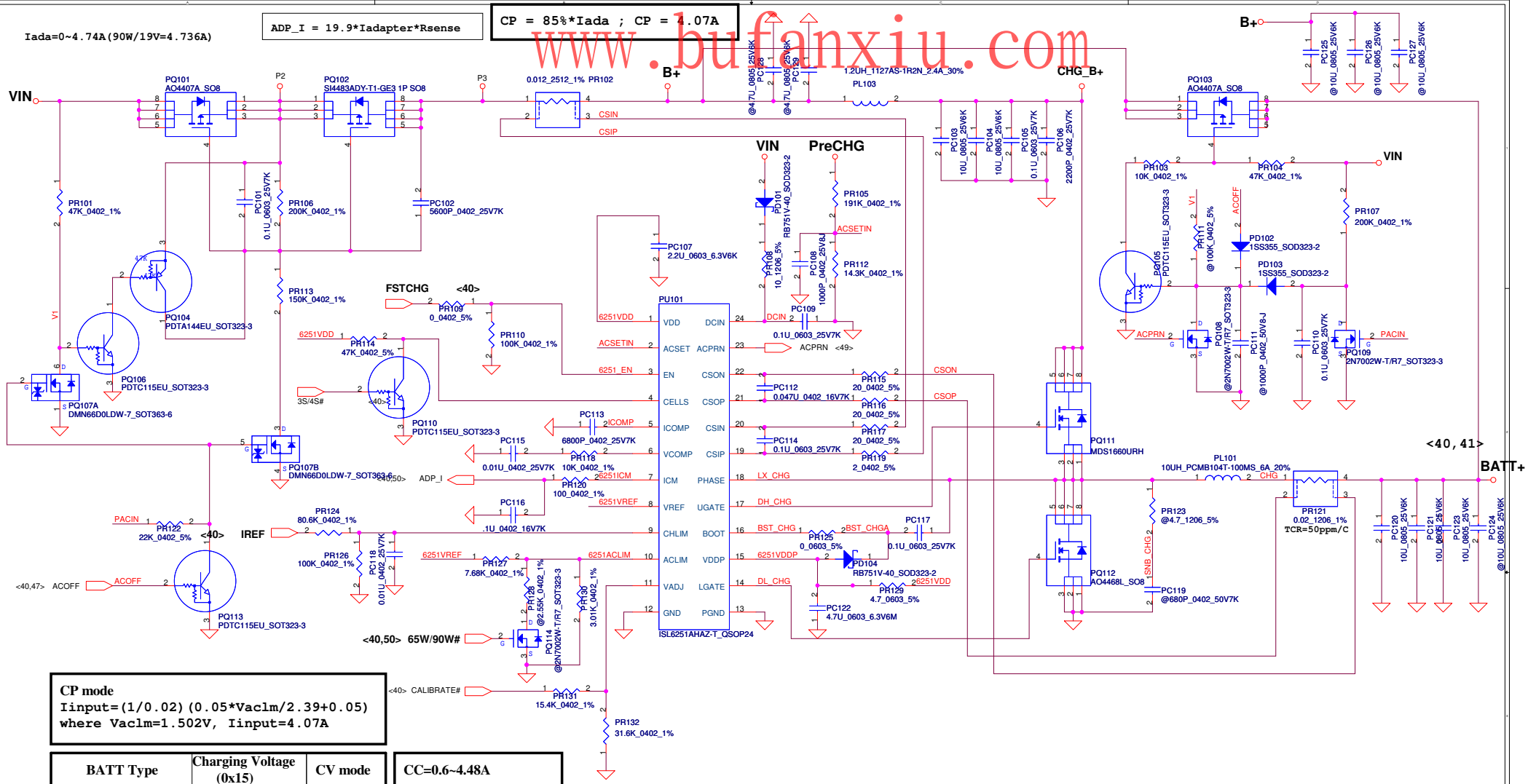
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PWR DCIN / Pre-charge		
Size: Custom	Document Number: LA-6931P		Rev: 0.1
Date: Wednesday, October 27, 2010	Sheet 47 of 10		

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode

$$I_{input} = (1/0.02)(0.05 * V_{aclm}/2.39 + 0.05)$$

where $V_{aclm} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki

Vchlim=Iref*(PR374/(PR372+PR374))

=Iref*(100K/(80.6K+100K))

=Iref*0.5537

Ichanrge=(165mV/PR369)*(Vchlim/3.3V)

=(165m/20m)*(1/3.3V)*Iref*0.5537

=1.3842*Iref

Iref=0.7224*Ichanrge =>Ki=0.7224

Kv

Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K

R=514K//31.6K//(15.4K+3k)=11.372K

r=514K//514K//31.6K=28.14K

Vcell=0.175*Vadj+3.99v

4.2V=0.175*Vadj+3.99V =>Vadj=1.2V

Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))

1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899

1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv

A=Vref*(R/(R+514K))=0.052

Kv=9.451

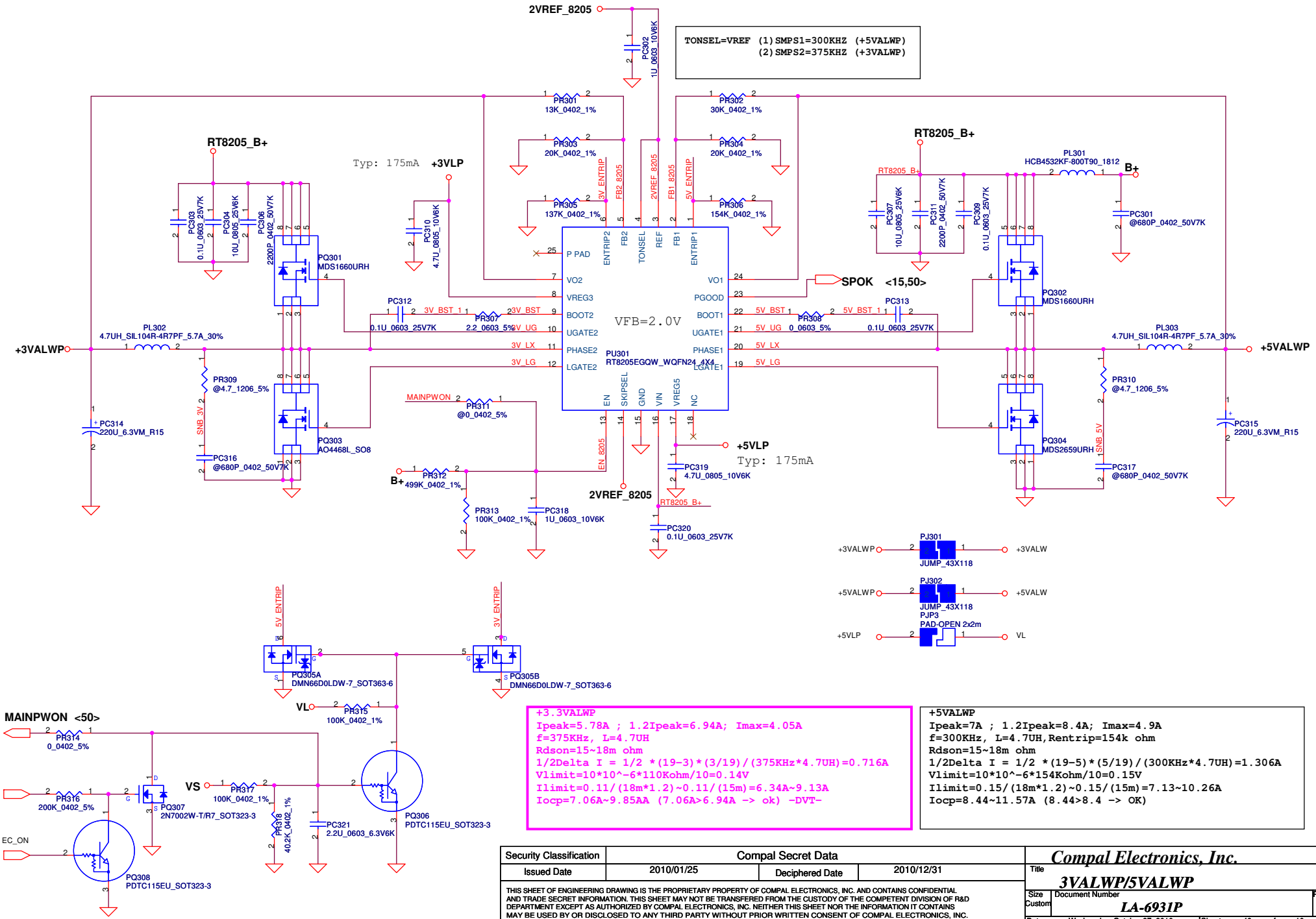
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: LA-6931P | Rev: 0.1

Date: Wednesday, October 27, 2010 | Sheet 48 of 10



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

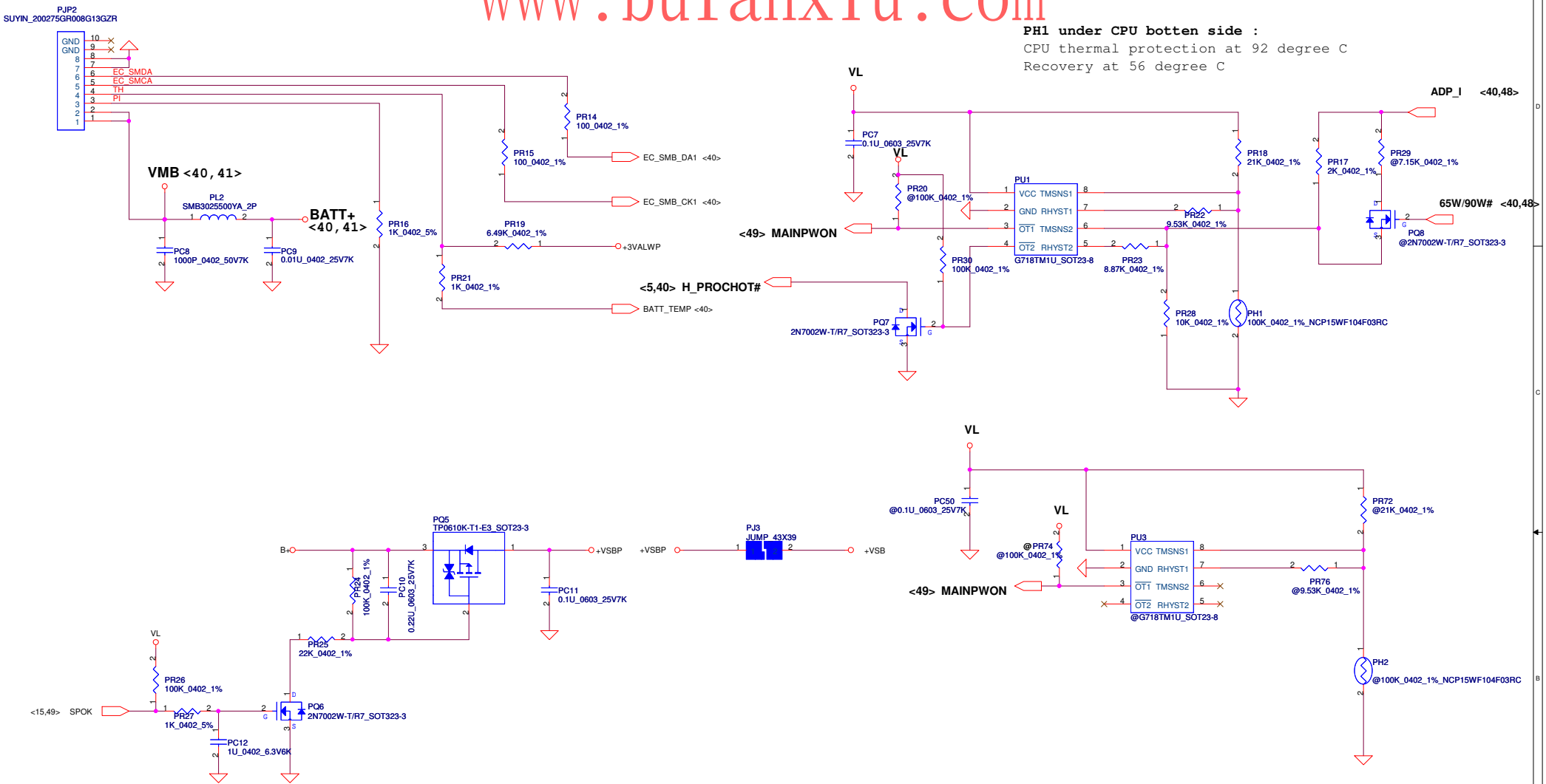
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: LA-6931P | Rev: 0.1

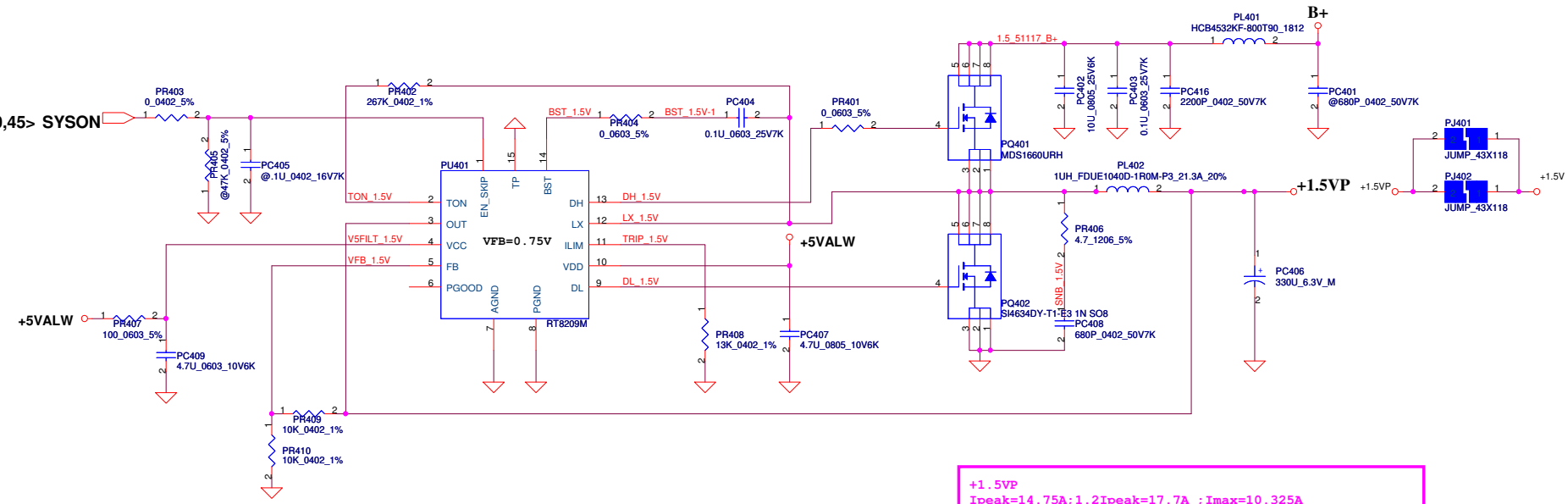
Date: Wednesday, October 27, 2010 | Sheet 49 of 10

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

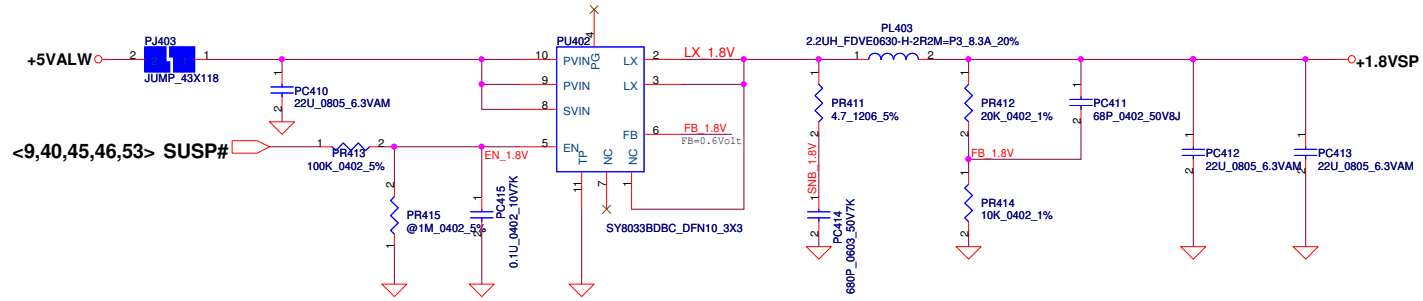


Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: LA-6931P		Rev: 0.1
Date: Wednesday, October 27, 2010	Sheet 50 of 10		



+1.5VP
Ipeak=14.75A;1.2Ipeak=17.7A ;Imax=10.325A
Rton=267K, Fsw=298KHz ,Rdson=4.5~5.6mohm
Rtrip=12K
Iocp=18.17~28.98A



1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V
-DVT-

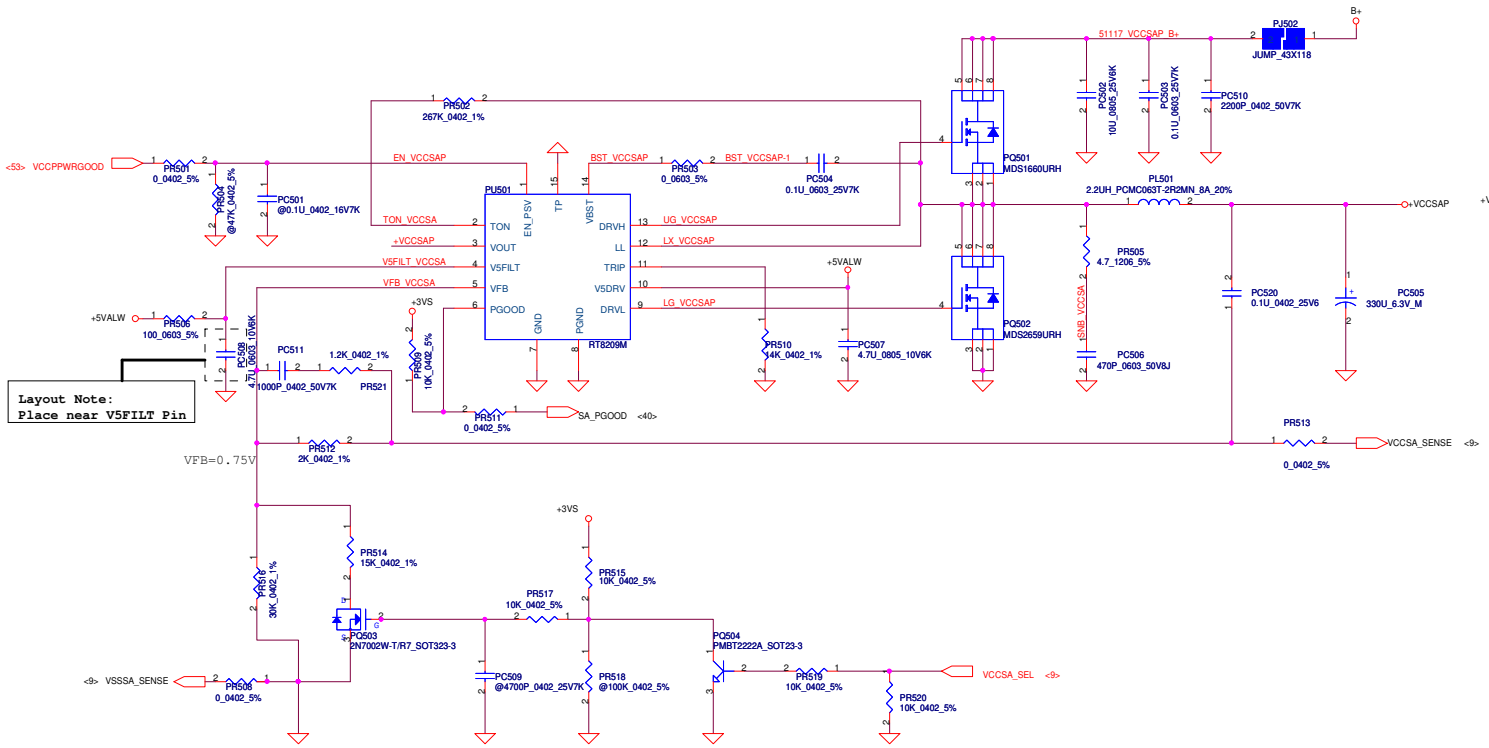
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: LA-6931P | Rev: 0.1

Date: Wednesday, October 27, 2010 | Sheet 51 of 10



+VCCSAP
Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A
DCR= 9 m(typ)~10 m(max)
Rlimit=12K,Rdson=15~18mohm
Ilimit=10uA
Iocp=Rlimit/Rdson*10^(-5)= 7.61~9.13A

VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=213KHz

Cesr=15m ohm
Ipeak=7.2A Imax=6.0A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0787V

Iocp=7.28~7.41A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	0	0.725V	No/Yes
1	1	0.675V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

the resister change
from @ to pop component

Add two jumpers on the HW's output cap of the
+VCCSA's PIN(+) and PIN(-) to sense the
feedback voltage for VCCSA_SENSE & VSSSA_SENSE.

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	LA-6931P	0.1

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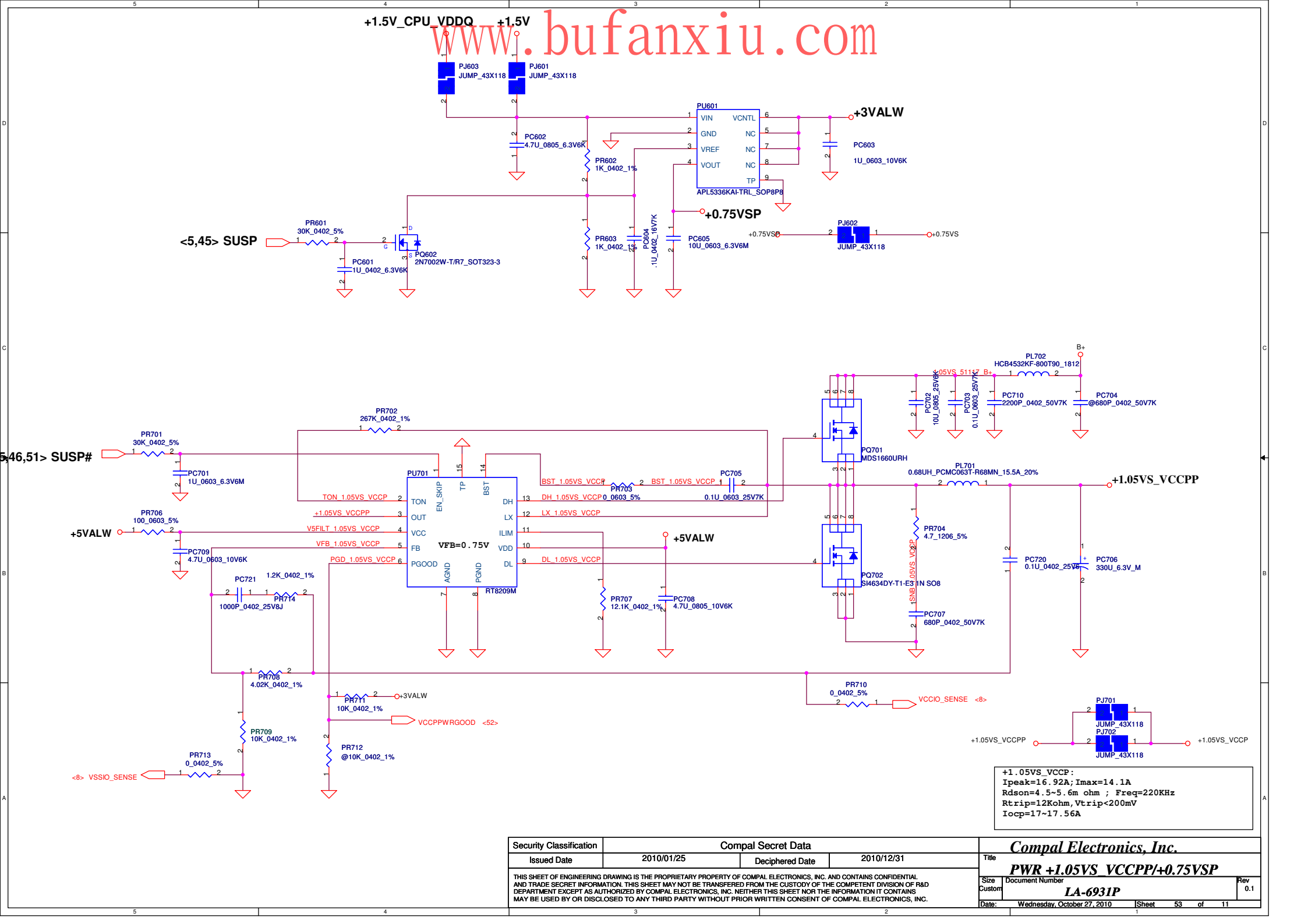

+1.05VS_VCCP:
Ipeak=16.92A;Imax=14.1A
Rdson=4.5~5.6m ohm ; Freq=220KHz
Rtrip=12Kohm,Vtrip<200mV
Iocp=17~17.56A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	LA-6931P	0.1

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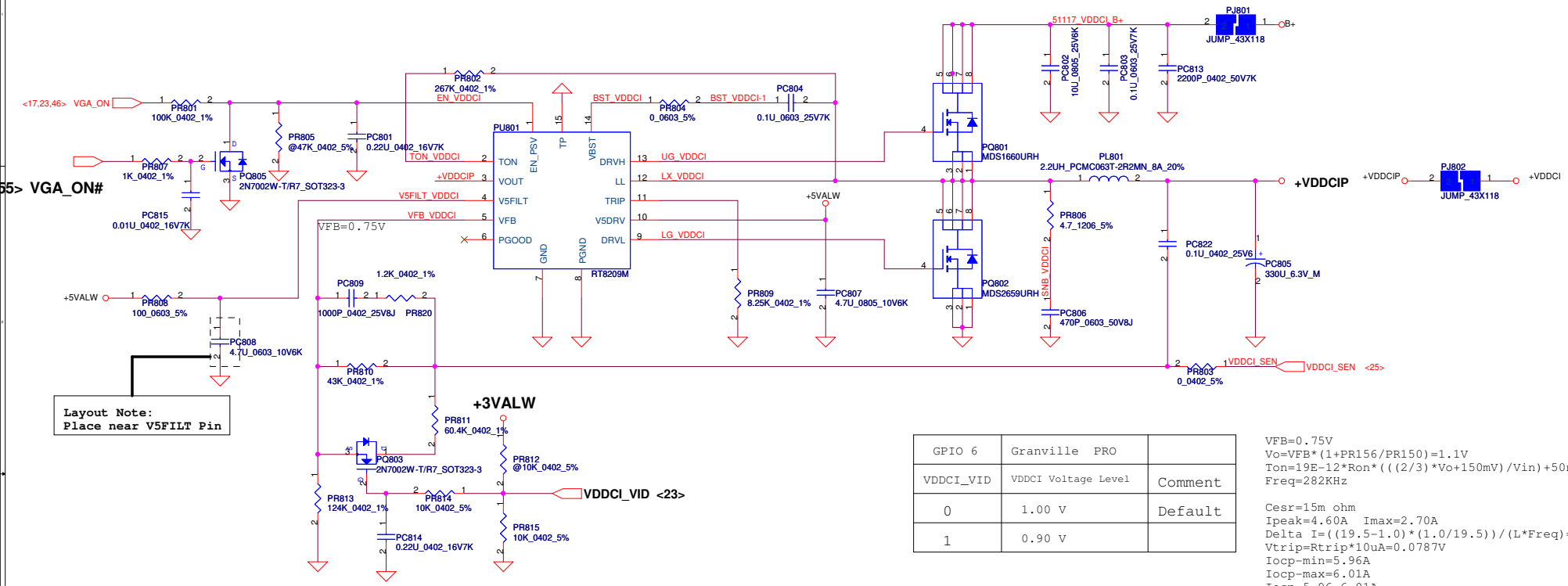
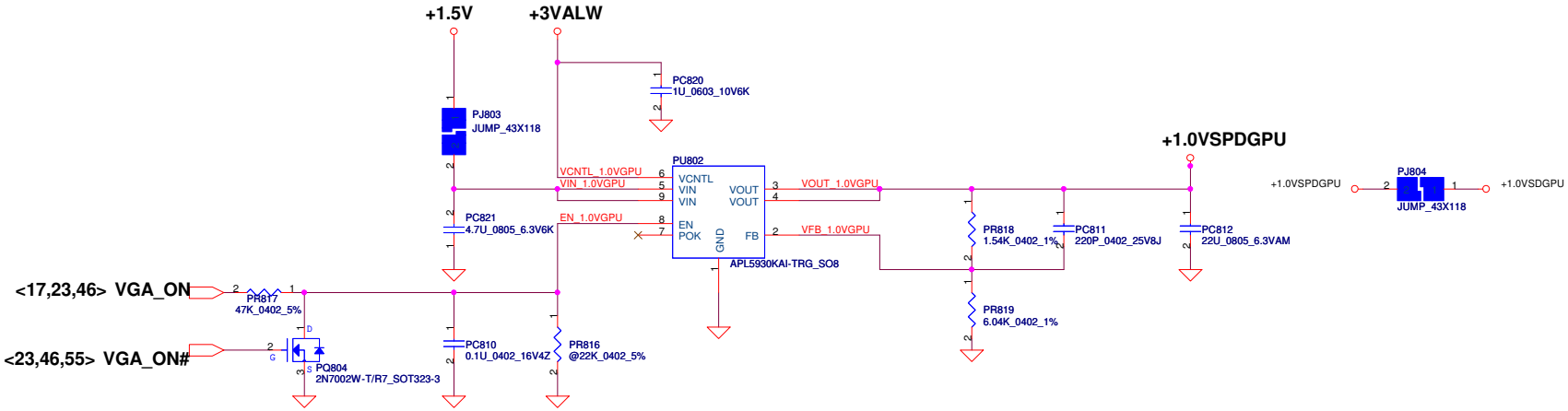


GPIO 6	Granville PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	

```
VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A  Imax=2.70A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0787V
Iocp-min=5.96A
Iocp-max=6.01A
Iocp=5.96~6.01A
```



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **VDDCIP/1.0VSDGPU**

Size	Document Number	Rev
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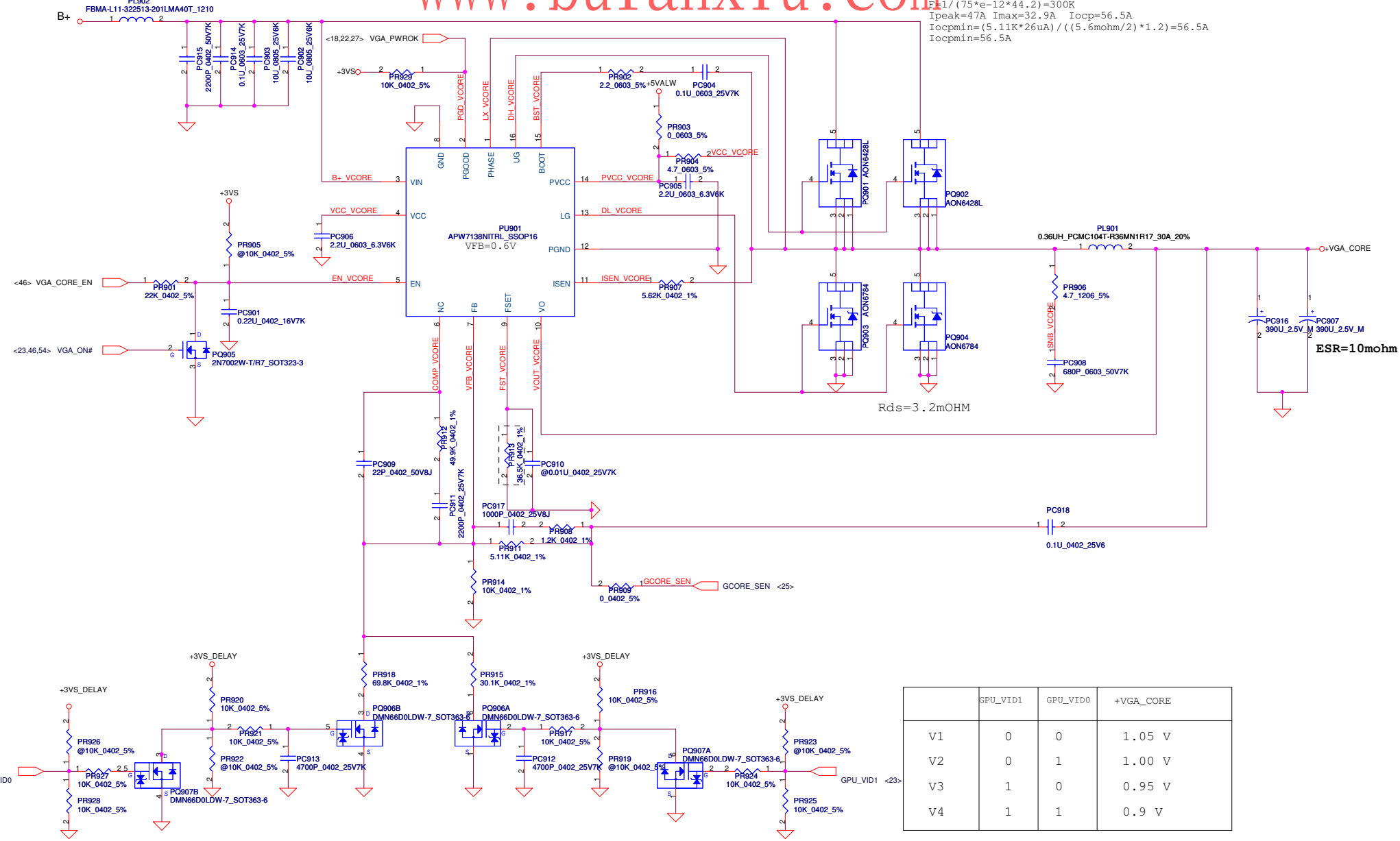
VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=47A Imax=32.9A Iocp=56.5A
Iocpmin=(5.11K*26uA)/((5.6mohm/2)*1.2)=56.5A
Iocpmin=56.5A



	GPU_VID1	GPU_VID0	+VGA_CORE
V1	0	0	1.05 V
V2	0	1	1.00 V
V3	1	0	0.95 V
V4	1	1	0.9 V

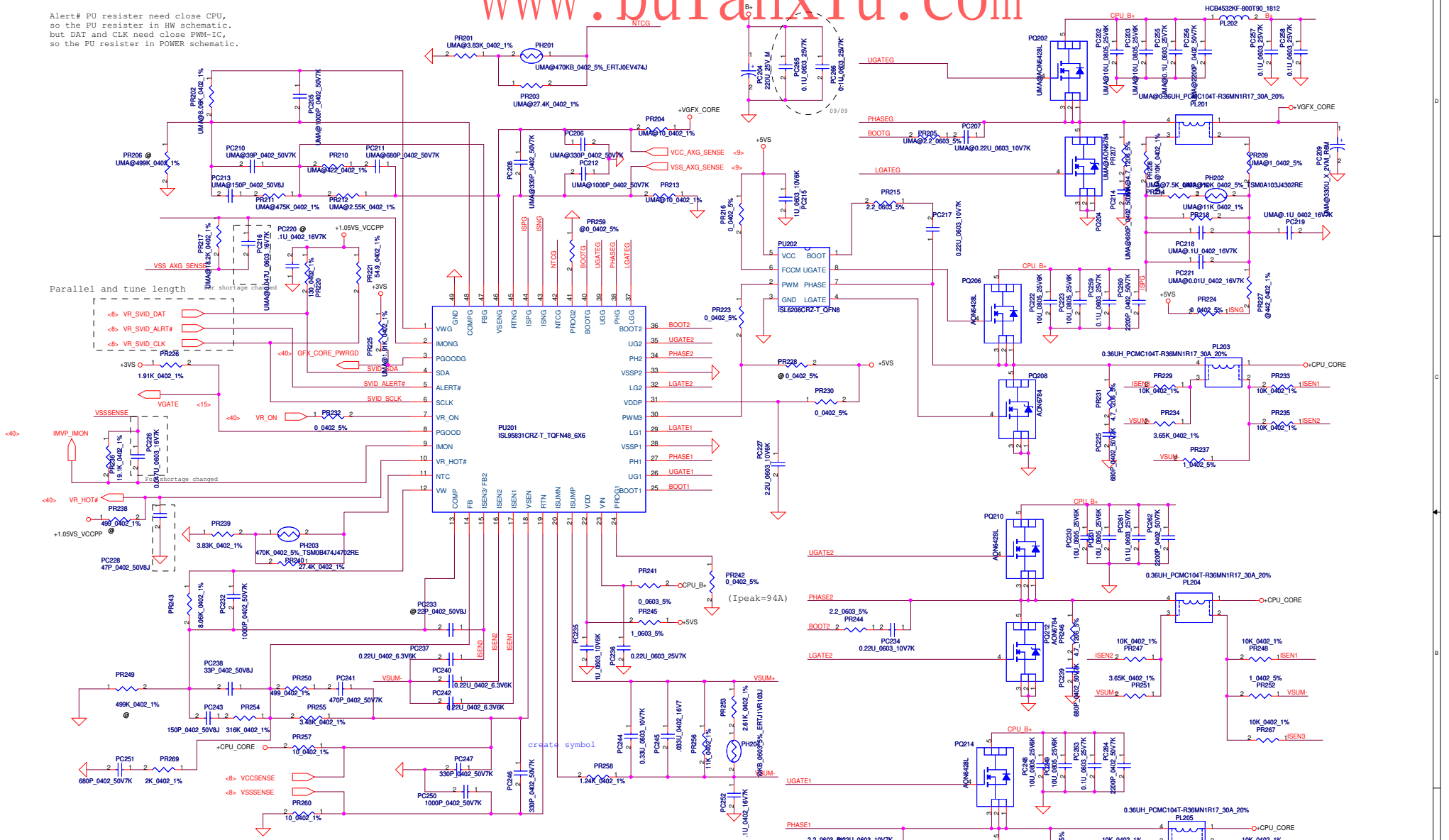
Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom	Document Number: LA-6931P	Rev: 0.2
Date: Wednesday, October 27, 2010	Sheet 55 of 11	

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.



*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

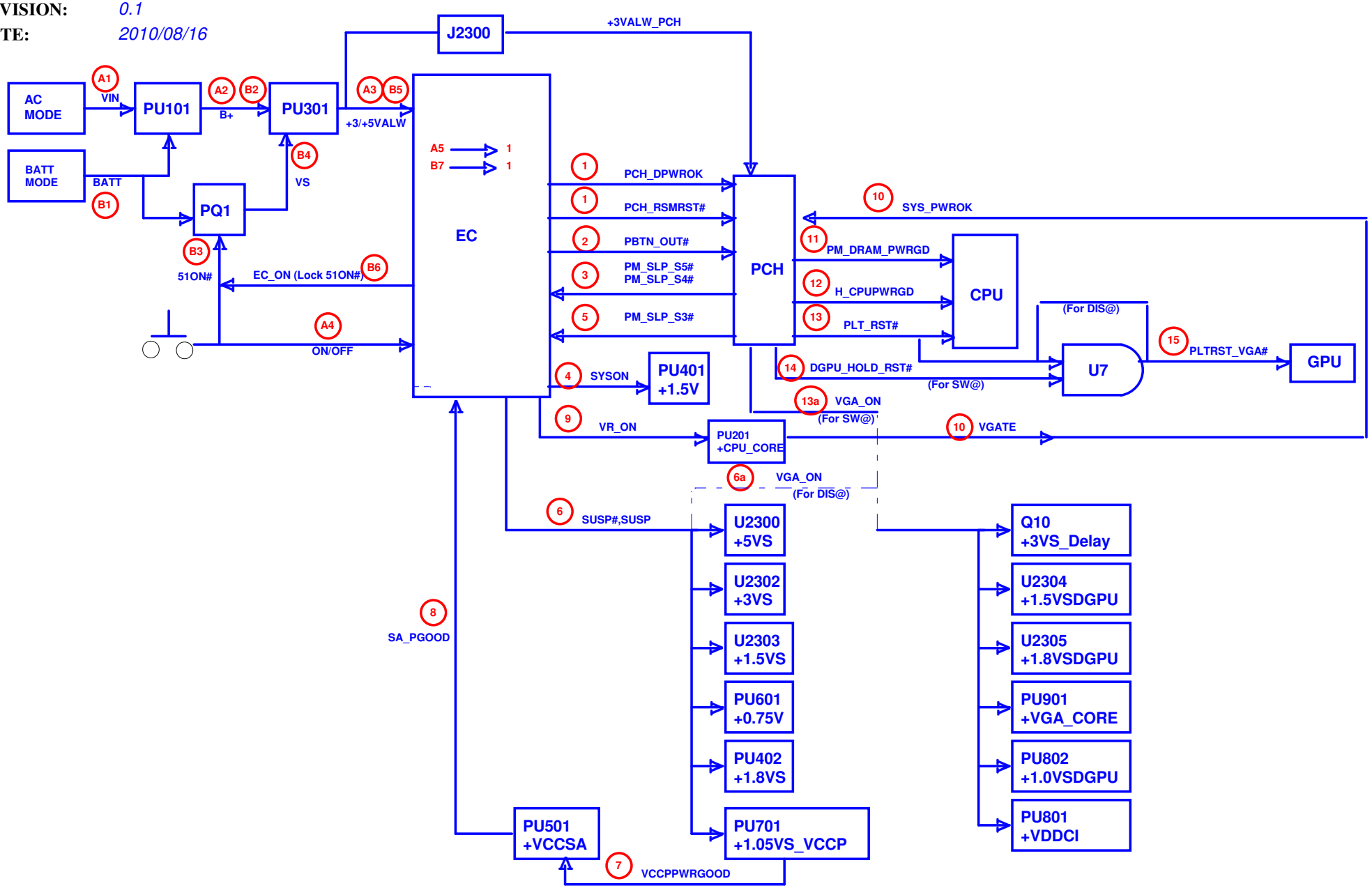
*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Title	PWR +CPU_CORE/+VGFX_CORE		
Size C	Document Number LA-6931P		Rev 0.1
Date: Wednesday, October 27, 2010	Sheet 56 of 10		

COMPAL CONFIDENTIAL

MODEL NAME: *P5LM0 Power Sequence Block Diagram*
PCB NAME: *LA-6931P*
REVISION: *0.1*
DATE: *2010/08/16*



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 57 of 58

Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	USB3.0	8/26	Compal	For USB3.0 wake up function	Instal R2423	0.3
2	30	LVDS	8/26	Compal	For LED panel EDID	Change R2130,R2131,R2185,R2186 from 2.2K to 0 Ohm	0.3
3	35	CIR	8/26	Compal	For CIR can't work	Add R2239,D2201 and pull up to +3VALW on EC side	0.3
4	34	LAN	8/27	Compal	Fine tune LAN_IO rising time	Add C1231 and change R1223 from 47K to 470K Ohm	0.3
5	40	KBC	8/28	Acer	For PWR LED function in low battery mode.	Pull up to +3VALW with R2240 (10K Ohm.)	0.3
6	40	KBC	8/30	Compal	Leakage for +5VS	Delete net "BT_ON" from KBC side	0.3
7	38	Card Reader	8/31	Compal	Card reader function fail	Chang C1318, C1319 to 0.022 uF and 1500 pF	0.3
8	13, 14	PCH	9/06	Compal	Leakage for +3VS	Add R927, D10, D11 to prevent leakage.	0.3
9	18	PCH	9/06	Compal	Leakage for +3V	Add R928, D12 to prevent leakage.	0.3
10	43	Audio	9/09	Compal	SPDIF jack's LED always on.	Add R1148.	0.3
11	33	ODD	9/23	Compal	Don't support ODD zero power	Add R2494, R2495	0.4
12	40	KBC	9/24	Compal	Board ID	Change R2231 from 8.2 K to 33K,	0.4
13	13	PCH	9/29	Compal	HDA_SYNC potential leakage concern.	Add pull down with 1M Ohm (R930) for HDA_SYNC.	0.4
14	30	LVDS	10/1	Compal	Fn+Left/Right hotKey no function, can not adjust brightness	Uninstall R2101 and install R2187	0.4 0.4
15	46	GPU DC-DC	10/2	Compal	Fine tune 1.5VSDGPU timing	Change R2333 from 510K to 470K	0.4
16	46	GPU DC-DC	10/2	Compal	Fine tune 1.8VSDGPU timing	Change R2339 to 33K and C2319 to 2.2u	0.4
17	46	GPU DC-DC	10/2	Compal	For 1.8VSDGPU discharge	Change R2338 from 470 to 220	0.4
18	46	GPU DC-DC	10/2	Compal	For 1.5VSDGPU discharge	Change R2332 from 470 to 220	0.4
19	34	LAN	10/7	Compal	For EMI's request	Add C1232, C1233	0.4
20	14	PCH	10/11	Compal	<RTC Accuracy>Add 90% loading,after 24h about 5s gap,can not meet spec +/-2.5s	Change C853, C854 from 18p to 27p	0.4
21	44	BT	10/20	Compal	For BT discharge	Add R2496, R2497 and Q2407	1.0
22	43	AUDIO	10/20	Compal	Has "po" noise when system enter/resume S3/S4/S5.	Change C1126, C1127 to 0.01u	1.0

Compal Electronics, Inc.			
Title	<Title>		
Size	Document Number	LA-6931P	Rev 1.0
Date:	Wednesday, October 27, 2010	Sheet 58 of 58	