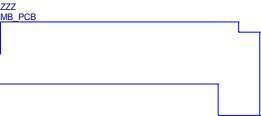


MODEL NAME : *VAZA0*
PCB NO : *LA-9262P (DAB0000I010)*
BOM P/N :

Dell/Compal Confidential

Schematic Document

Murcielgo MLK (Haswell ULT)

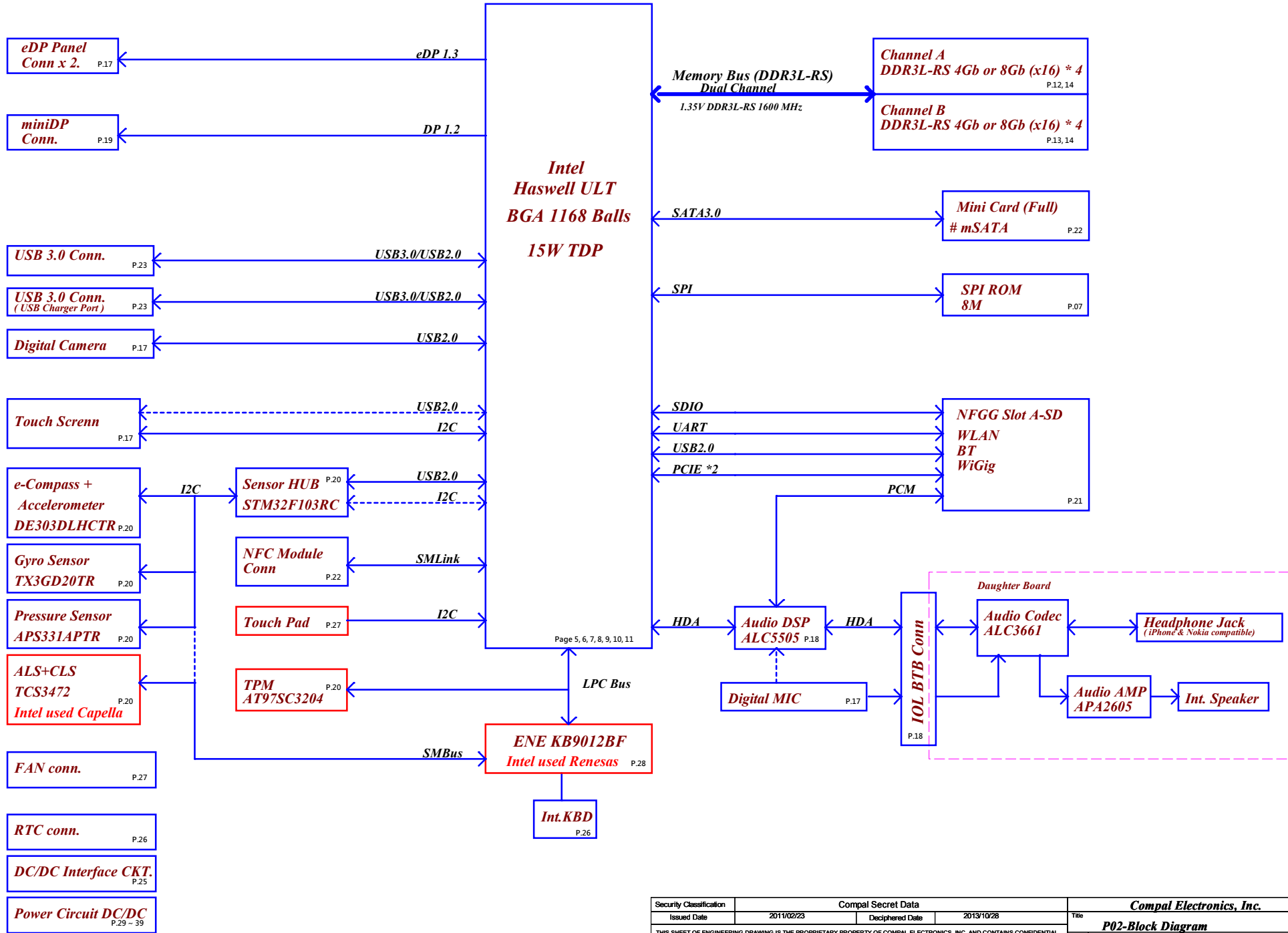


2013-04-19

Rev: 1.0

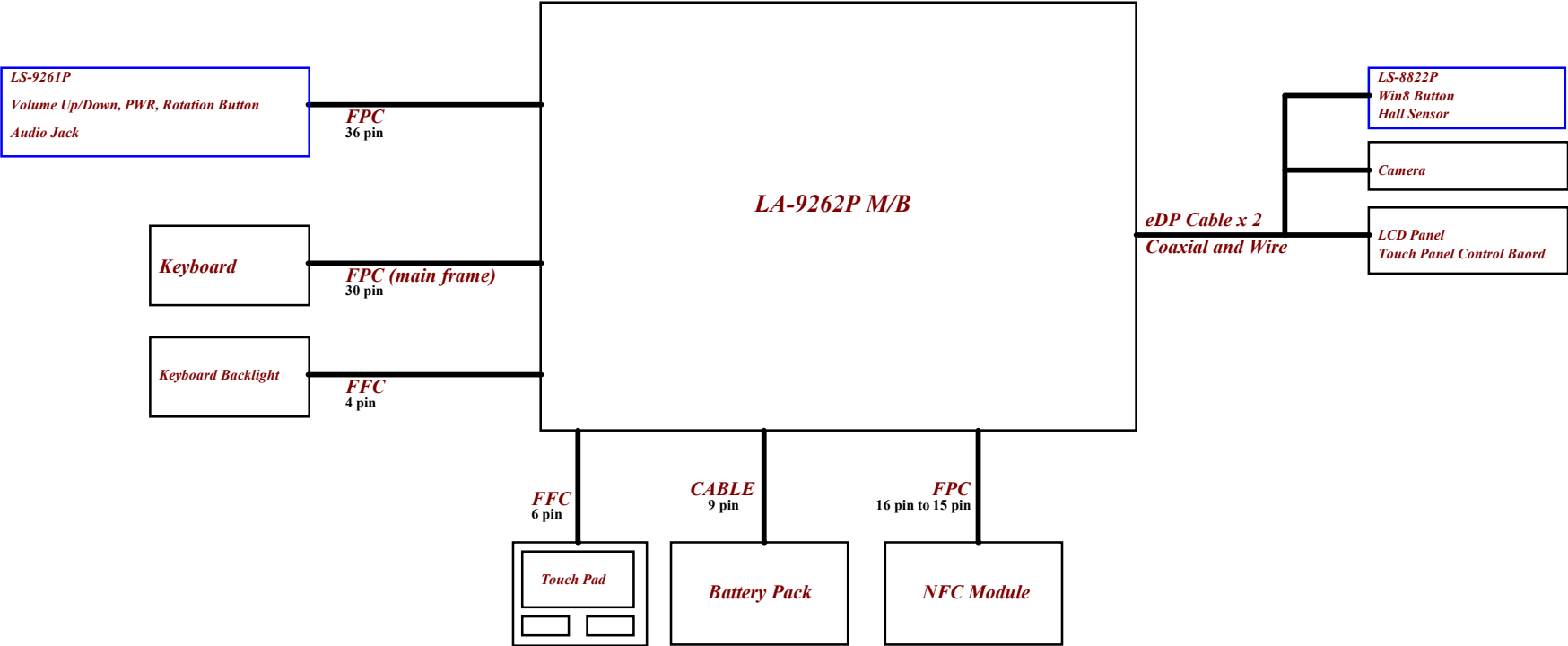
Highlight the short pad for 0 ohm

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		P01-Cover Page				
		Size	Document Number			Rev
		LA-9262P			1.0	
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Compal Confidential

Project Code : VAZA0
File Name : LA-9262P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

BOARD ID Table

Board ID	PCB Revision
0	CS 0.1
1	CS 0.2
2	CS 0.3
3	CS 0.4
4	CS 0.5
5	CS 1.0
6	
7	
8	
9	
10	Non-CS 0.1
11	Non-CS 0.2
12	Non-CS 0.3
13	Non-CS 0.4
14	Non-CS 1.0
15	
16	
17	
18	
19	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3
	1	External USB3
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	Sensors HUB
	6	
	7	

SMBUS Control Table

	SOURCE	NGFF	BATT	Charger	NFC	XDP	DDR3 SPD	ALS	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012							V	
PCH_SMLCLK PCH_SMLDATA	PCH	V			V				
PCH_SMLCLK PCH_SMLDATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH					V	V		V

Link

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	mini-DP
	C	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0		CLKOUT_LPC_0	EC LPC
	CLKOUT_PCIE1		CLKOUT_LPC_1	TPM
	CLKOUT_PCIE2			
	CLKOUT_PCIE3	NGFF CARD WLAN		
	CLKOUT_PCIE4			
	CLKOUT_PCIE5			

SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

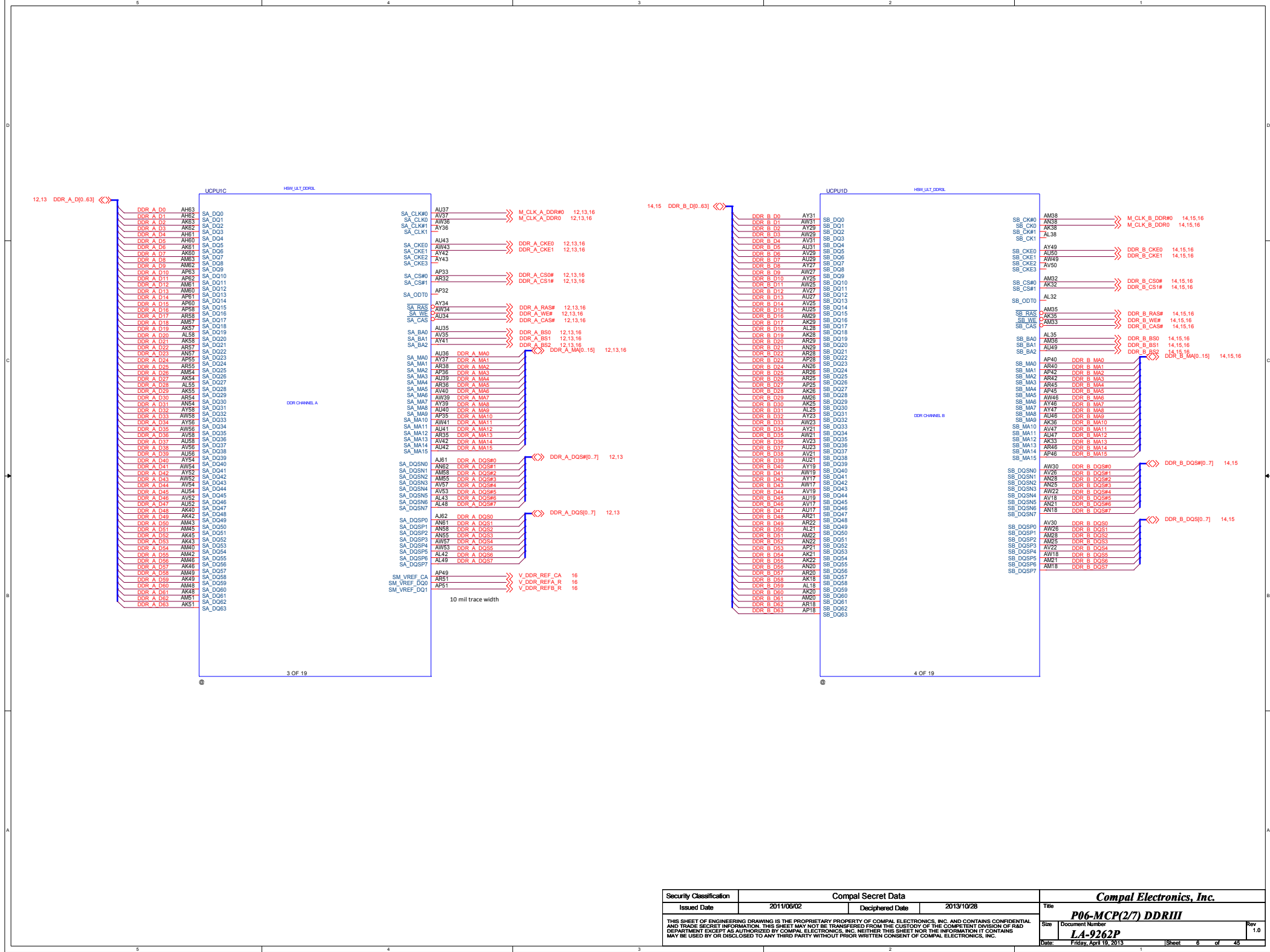
PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF CARD WLAN
Lane 4	NGFF CARD WLAN
Lane 5	
Lane 6	

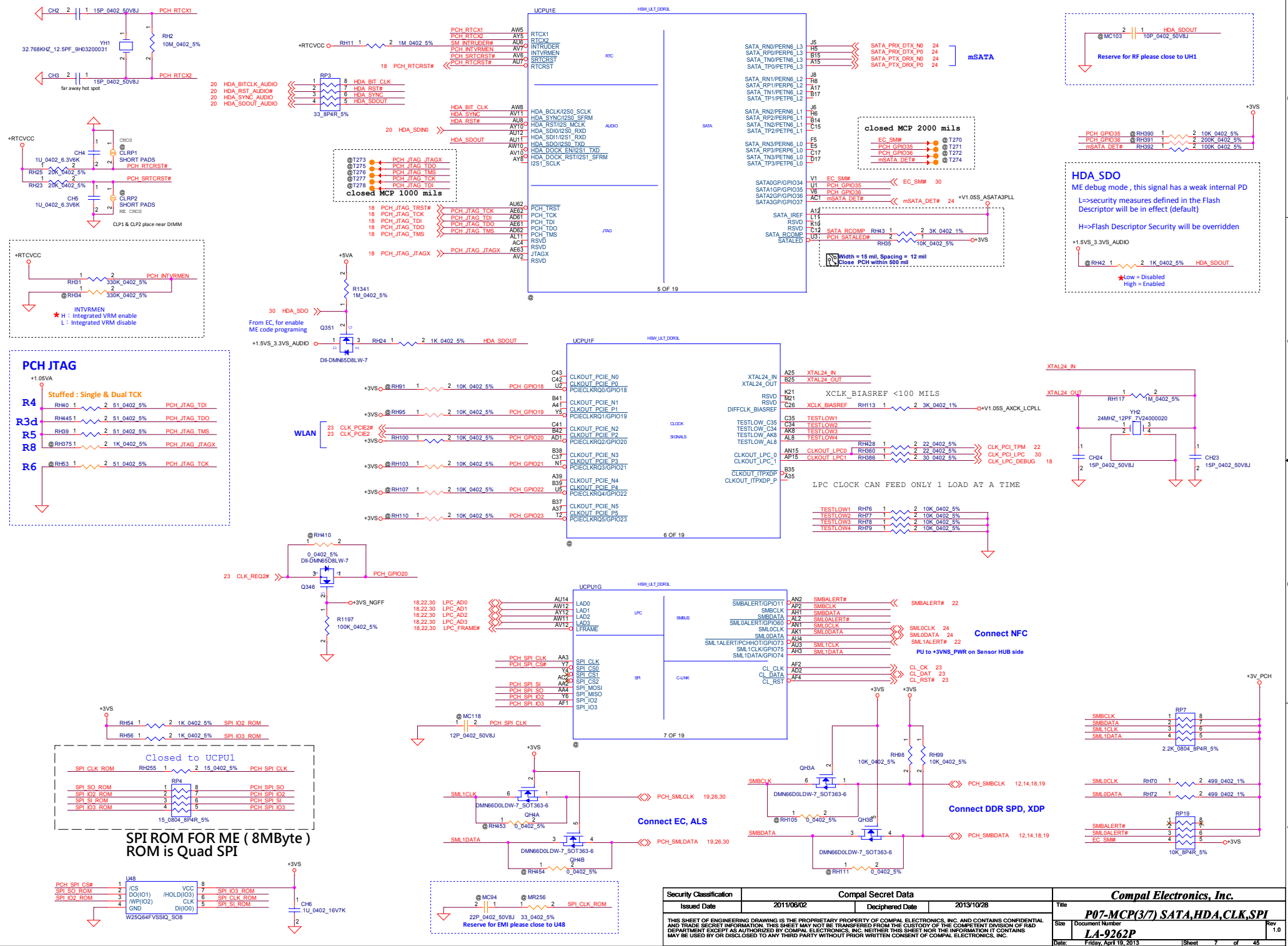
Symbol Note :

 : means Digital Ground

 : means Analog Ground

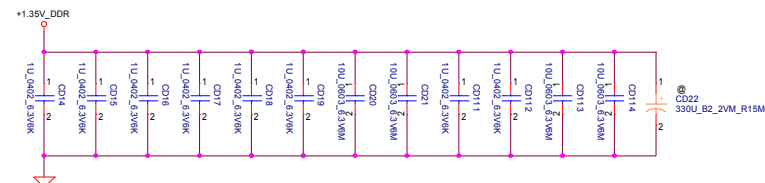
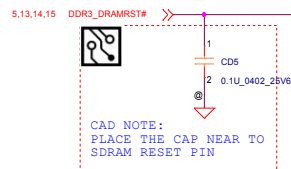
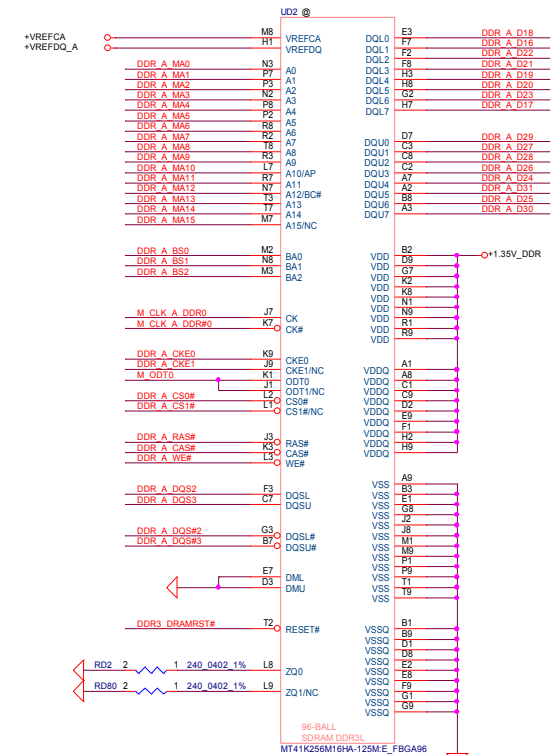
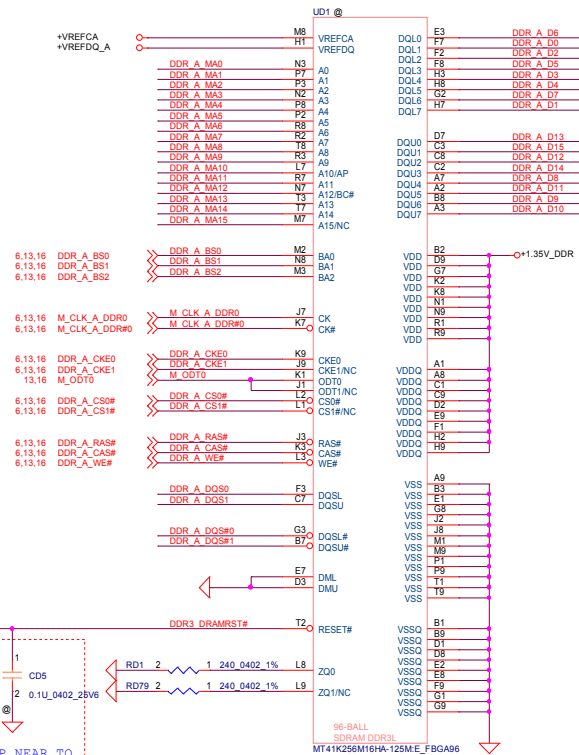
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[illegible]

6,13	DDR_A_DQS#[0..7]	《》	
6,13	DDR_A_DQS[0..7]	《》	
6,13	DDR_A_D[0..63]	《》	
6,13,16	DDR_A_MA[0..15]	《》	



7.14.18.19 PCH_SMBCLK
7.14.18.19 PCH_SMBDATA

+3VS

U03

1 VCC A0 1 1K 0402 5%
2 GND A1 2 1K 0402 5%
3 A2
4 SCL
5 SDA
6
7
8

AT24C02-02M-T SOP8

+3VS

1
2

U023
0.1u 0402_10V7K

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				P12-DDRIII Channel A Lower	
				Size	Document Number
				LA-9262P	Rev 1.0
Date:				Friday, April 19, 2013	Sheet 12 of 45

CD24 2 1 1.047uV 0.402 16V7K

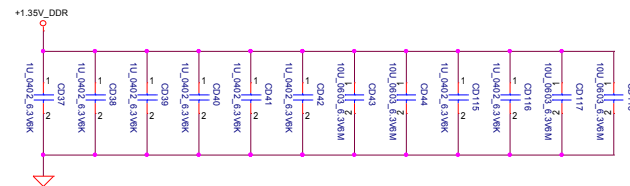
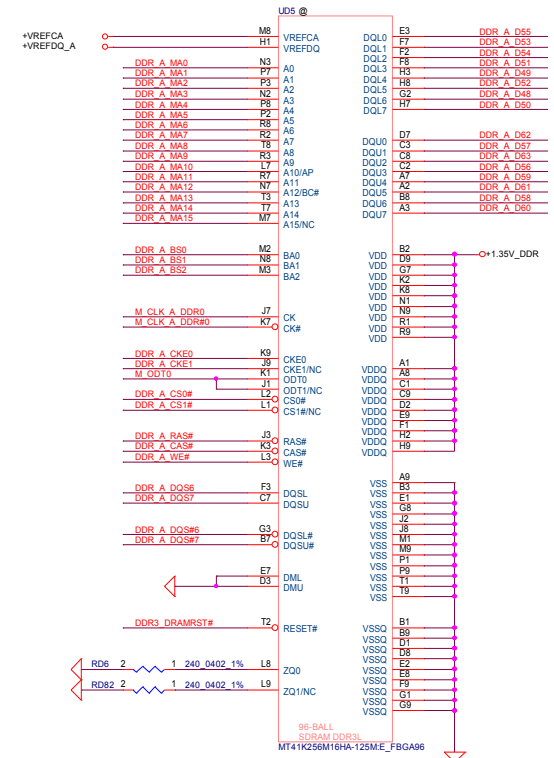
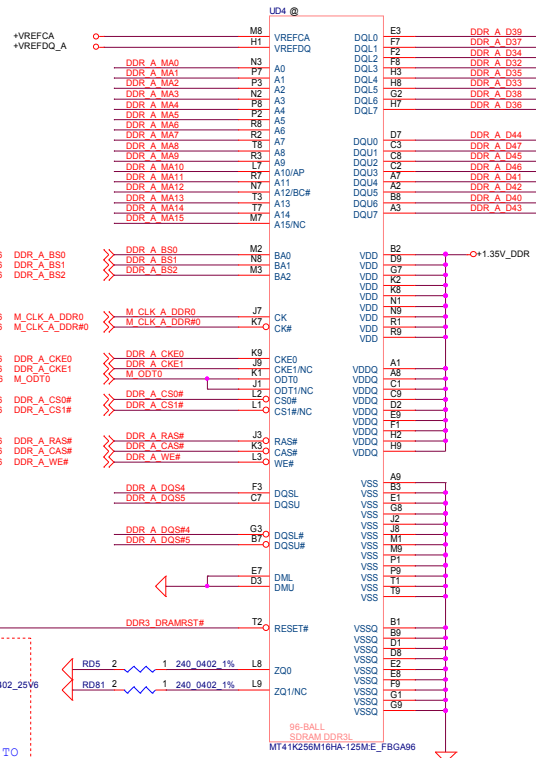
CD25 2 1 1.047uV 0.402 16V7K +VREFCA

CD26 1 2 1.047uV 0.402 16V7K

CD27 1 2 1.047uV 0.402 16V7K +VREFDQ_A

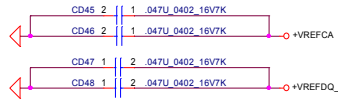


All VREF traces should have 10 mil trace width



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				P13-DDRIII Channel A Upper	
				Size Document Number LA-9262P	
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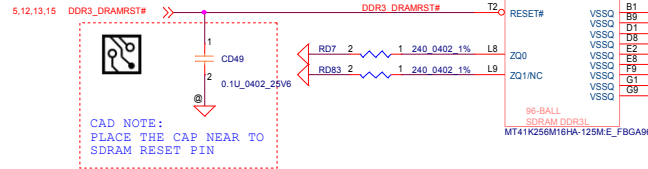
follow INTEL PDG



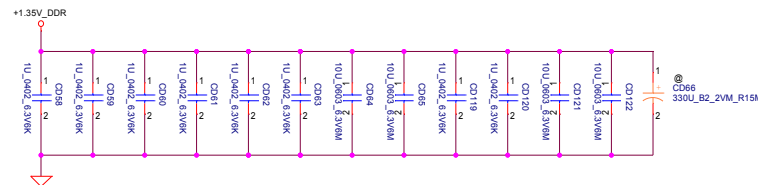
PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS



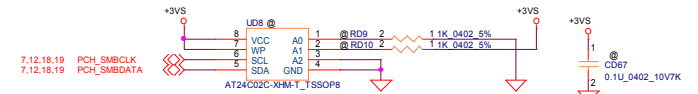
All VREF traces should
have 10 mil trace width



CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN

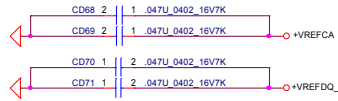


Memory Channel B SPD EEPROM



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				Size	Document Number
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follow INTEL PDG

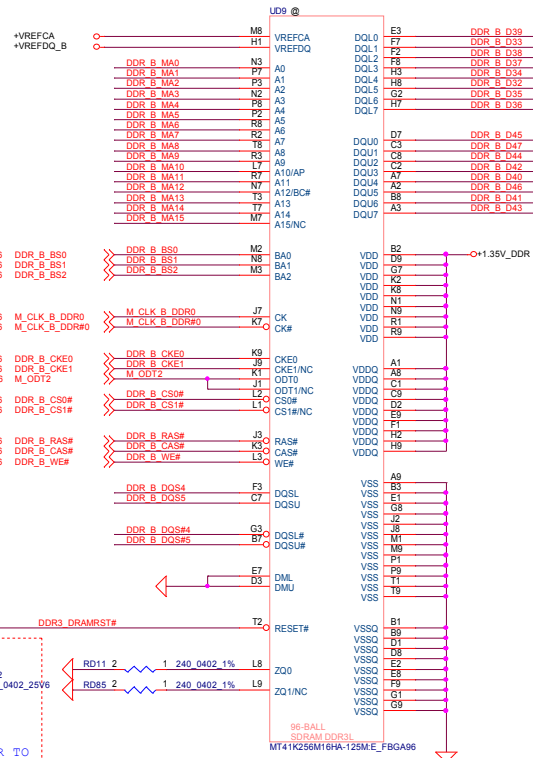


PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

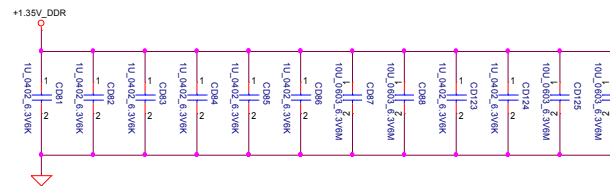
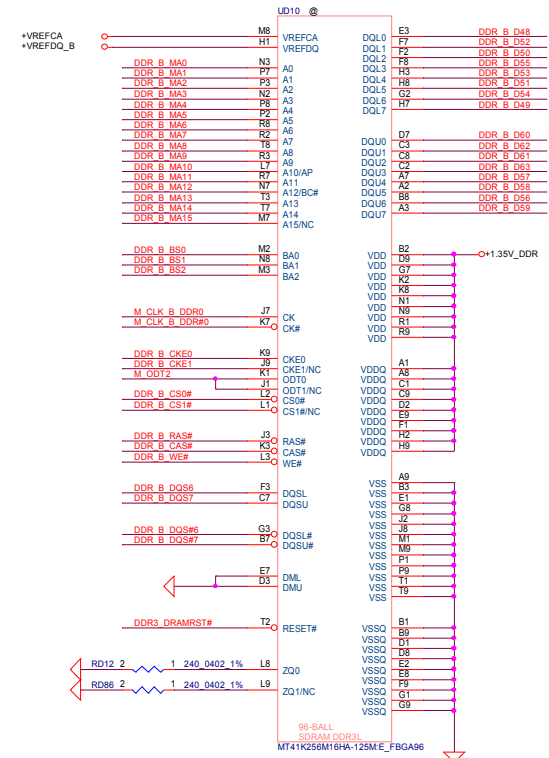


- 6.14 DDR_B_DQS#0..7
- 6.14 DDR_B_DQS#0..7
- 6.14 DDR_B_DQS#0..7
- 6.14.16 DDR_B_MA[0..15]

All VREF traces should
have 10 mil trace width



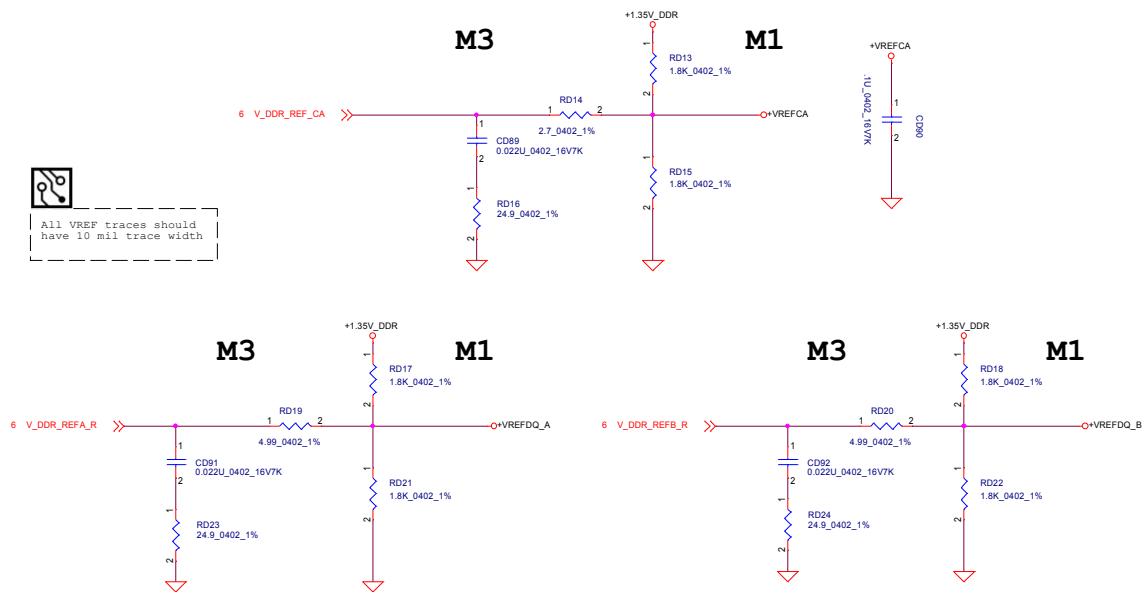
CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



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						LA-9262P					



All VREF traces should have 10 mil trace width



DDR A MA12 RD25 1 2 34.8 0402 1%
DDR A MA15 RD27 1 2 34.8 0402 1%
DDR A MA9 RD29 1 2 34.8 0402 1%
DDR A MA10 RD31 1 2 34.8 0402 1%

DDR A MA4 RD33 1 2 34.8 0402 1%
DDR A MA2 RD35 1 2 34.8 0402 1%
DDR A MA1 RD37 1 2 34.8 0402 1%
DDR A MA6 RD39 1 2 34.8 0402 1%

DDR A MA3 RD41 1 2 34.8 0402 1%
DDR A MA9 RD43 1 2 34.8 0402 1%
DDR A MA11 RD45 1 2 34.8 0402 1%
DDR A MA5 RD47 1 2 34.8 0402 1%

DDR A MA14 RD49 1 2 34.8 0402 1%
DDR A MA7 RD51 1 2 34.8 0402 1%
DDR A MA8 RD53 1 2 34.8 0402 1%
DDR A MA13 RD55 1 2 34.8 0402 1%

6.12.13 DDR_A_CKE0 RD57 1 2 34.8 0402 1%
6.12.13 DDR_A_RAS# RD59 1 2 34.8 0402 1%
6.12.13 DDR_A_CSM# RD61 1 2 34.8 0402 1%
6.12.13 DDR_A_CAS# RD63 1 2 34.8 0402 1%

6.12.13 DDR_A_WE# RD65 1 2 34.8 0402 1%
6.12.13 DDR_A_BS0 RD67 1 2 34.8 0402 1%
6.12.13 DDR_A_BS2 RD69 1 2 34.8 0402 1%
6.12.13 DDR_A_BS1 RD71 1 2 34.8 0402 1%

6.12.13 DDR_A_CKE1 RD87 1 2 34.8 0402 1%
6.12.13 DDR_A_CS1# RD89 1 2 34.8 0402 1%

12.13 M_ODT0 RD73 1 2 30 0402 1%

6.12.13 M_CLK_A_DDR0 RD75 1 2 26.1 0402 1%

6.12.13 M_CLK_A_DDR#0 RD77 1 2 26.1 0402 1%

DDR B MA12 RD26 1 2 34.8 0402 1%
DDR B MA15 RD28 1 2 34.8 0402 1%
DDR B MA9 RD30 1 2 34.8 0402 1%
DDR B MA10 RD32 1 2 34.8 0402 1%

DDR B MA14 RD34 1 2 34.8 0402 1%
DDR B MA6 RD36 1 2 34.8 0402 1%
DDR B MA4 RD38 1 2 34.8 0402 1%
DDR B MA2 RD40 1 2 34.8 0402 1%

DDR B MA8 RD42 1 2 34.8 0402 1%
DDR B MA1 RD44 1 2 34.8 0402 1%
DDR B MA13 RD46 1 2 34.8 0402 1%
DDR B MA7 RD48 1 2 34.8 0402 1%

DDR B MA3 RD50 1 2 34.8 0402 1%
DDR B MA9 RD52 1 2 34.8 0402 1%
DDR B MA11 RD54 1 2 34.8 0402 1%
DDR B MA5 RD56 1 2 34.8 0402 1%

6.14.15 DDR_B_CKE0 RD58 1 2 34.8 0402 1%
6.14.15 DDR_B_CSM# RD60 1 2 34.8 0402 1%
6.14.15 DDR_B_CAS# RD62 1 2 34.8 0402 1%
6.14.15 DDR_B_RAS# RD64 1 2 34.8 0402 1%

6.14.15 DDR_B_BS1 RD66 1 2 34.8 0402 1%
6.14.15 DDR_B_BS2 RD68 1 2 34.8 0402 1%
6.14.15 DDR_B_BS0 RD70 1 2 34.8 0402 1%
6.14.15 DDR_B_WE# RD72 1 2 34.8 0402 1%

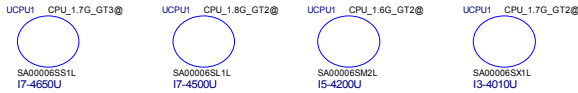
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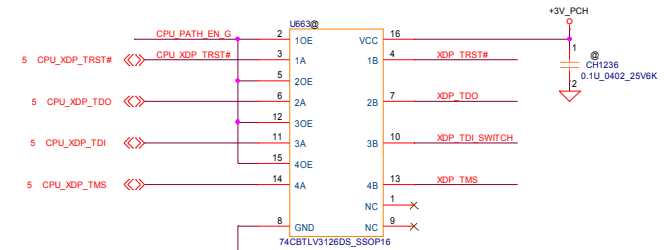
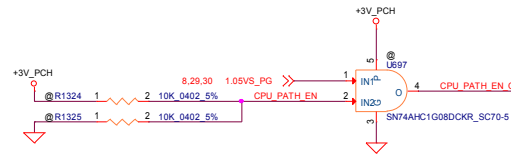
14.15 M_ODT2 RD74 1 2 30 0402 1%

6.14.15 M_CLK_B_DDR0 RD76 1 2 26.1 0402 1%

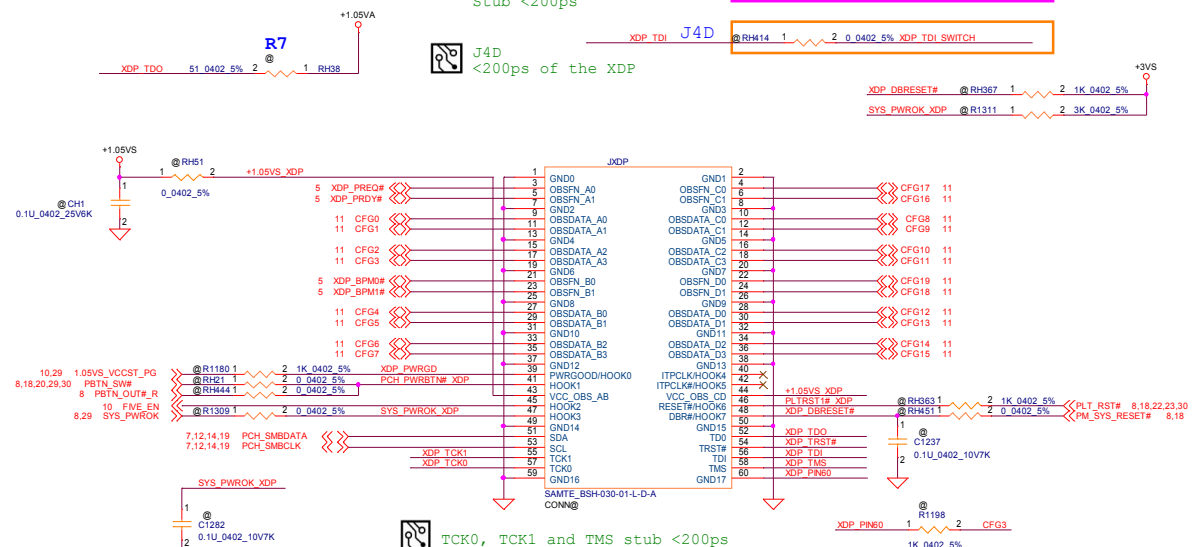
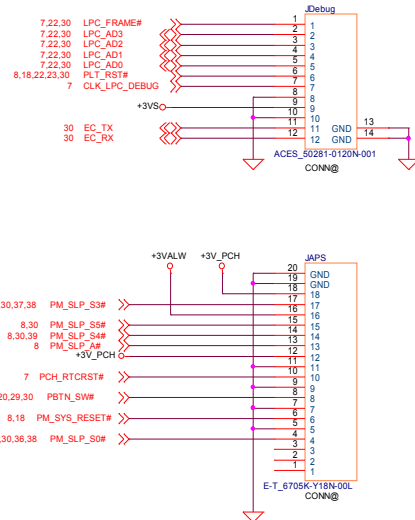
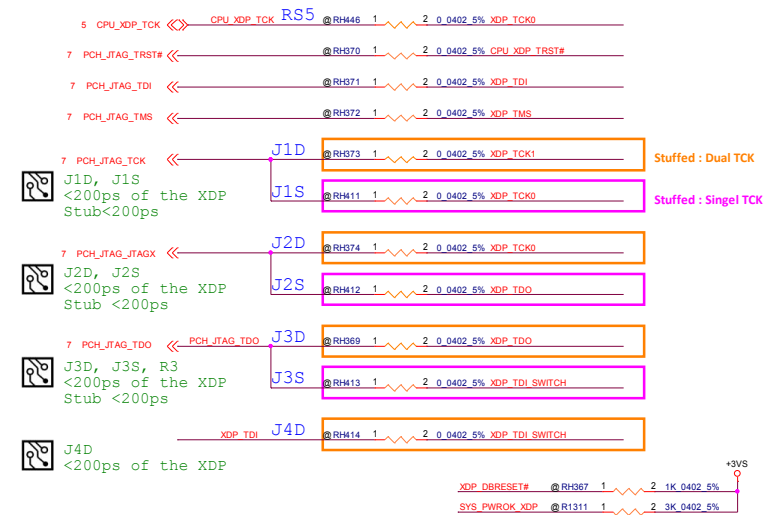
6.14.15 M_CLK_B_DDR#0 RD78 1 2 26.1 0402 1%

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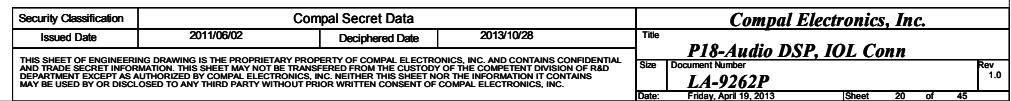
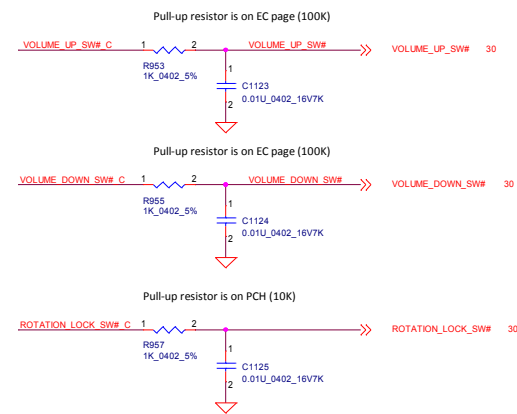




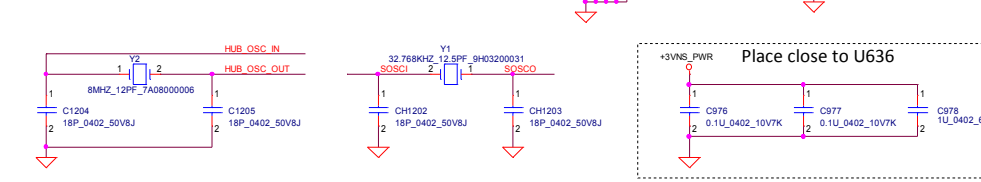
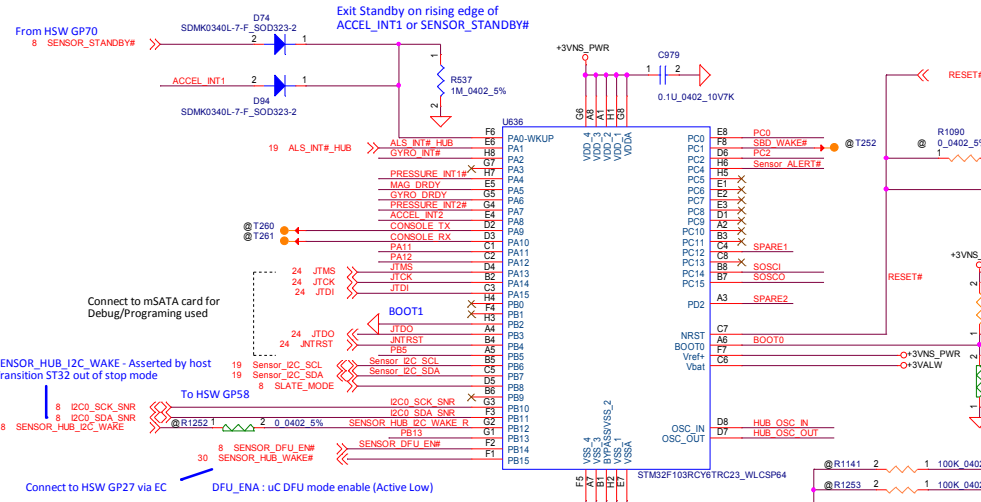
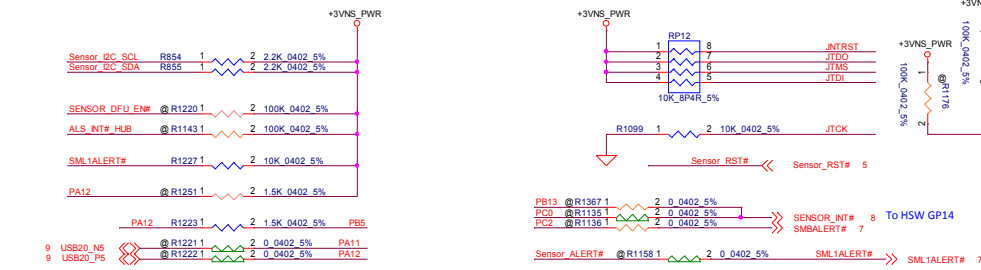
Topology	Description	Best Use for	Resistors Stuffed	Resistors Unstuffed
Default Setting: Dual TCK Scan Chains (also known as "Shared JTAG" in other document)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1, R2, J1d, J2d, J3d, J4d, R3, R4, R5	J1s, J2s, J3s
Single TCK scan chain (also known as "Common JTAG" in other document)	In this topology, PCH TDI-TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-Boundary Scan/Manufacturing test	J1s, J2s, J3s, R2, R3, R4, R5	R1, J1d, J2d, J3d, J4d



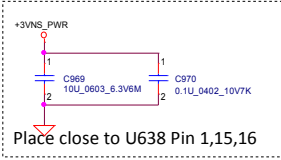
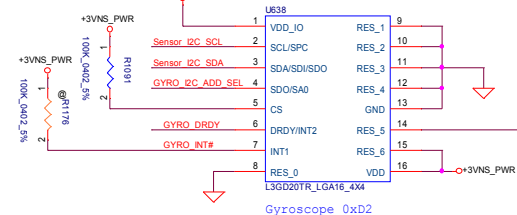
Security Classification	Compal Secret Data			Compal Electronics, Inc. Title P18-XDP,APS,Debug CONN Size Document Number LA-9262P Rev 1.0		
Issued Date	2011/06/02	Deciphered Date	2013/10/28			
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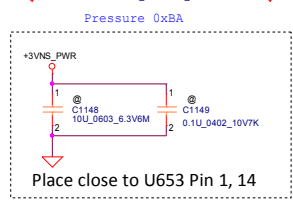
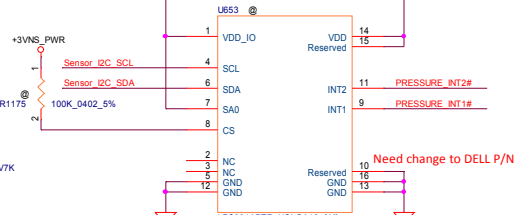
Sensor Fusion



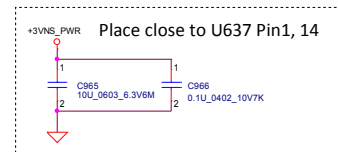
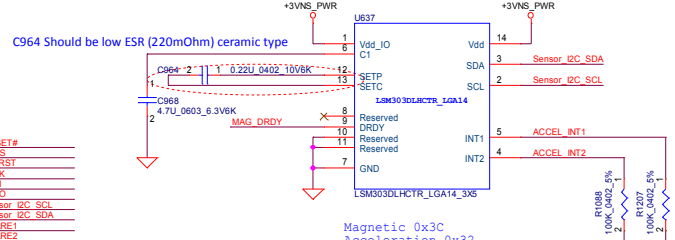
Gyro



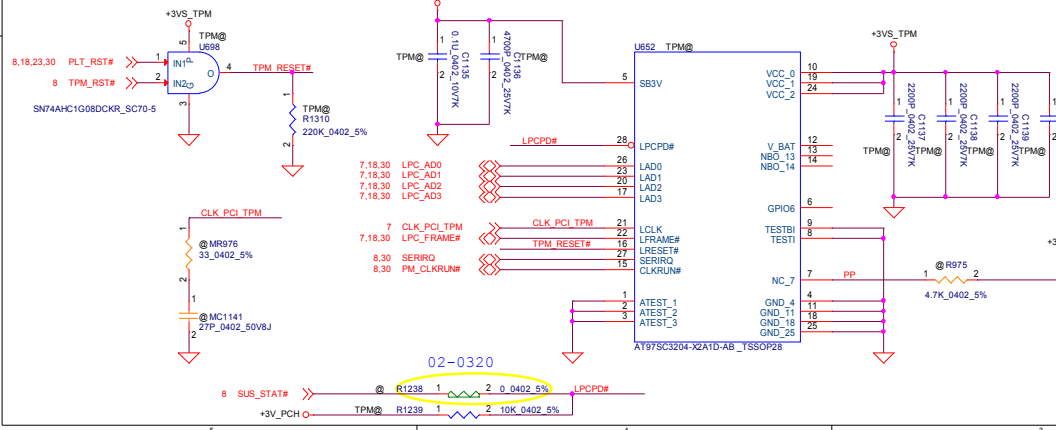
Pressure



e-Compass + Accelerometer

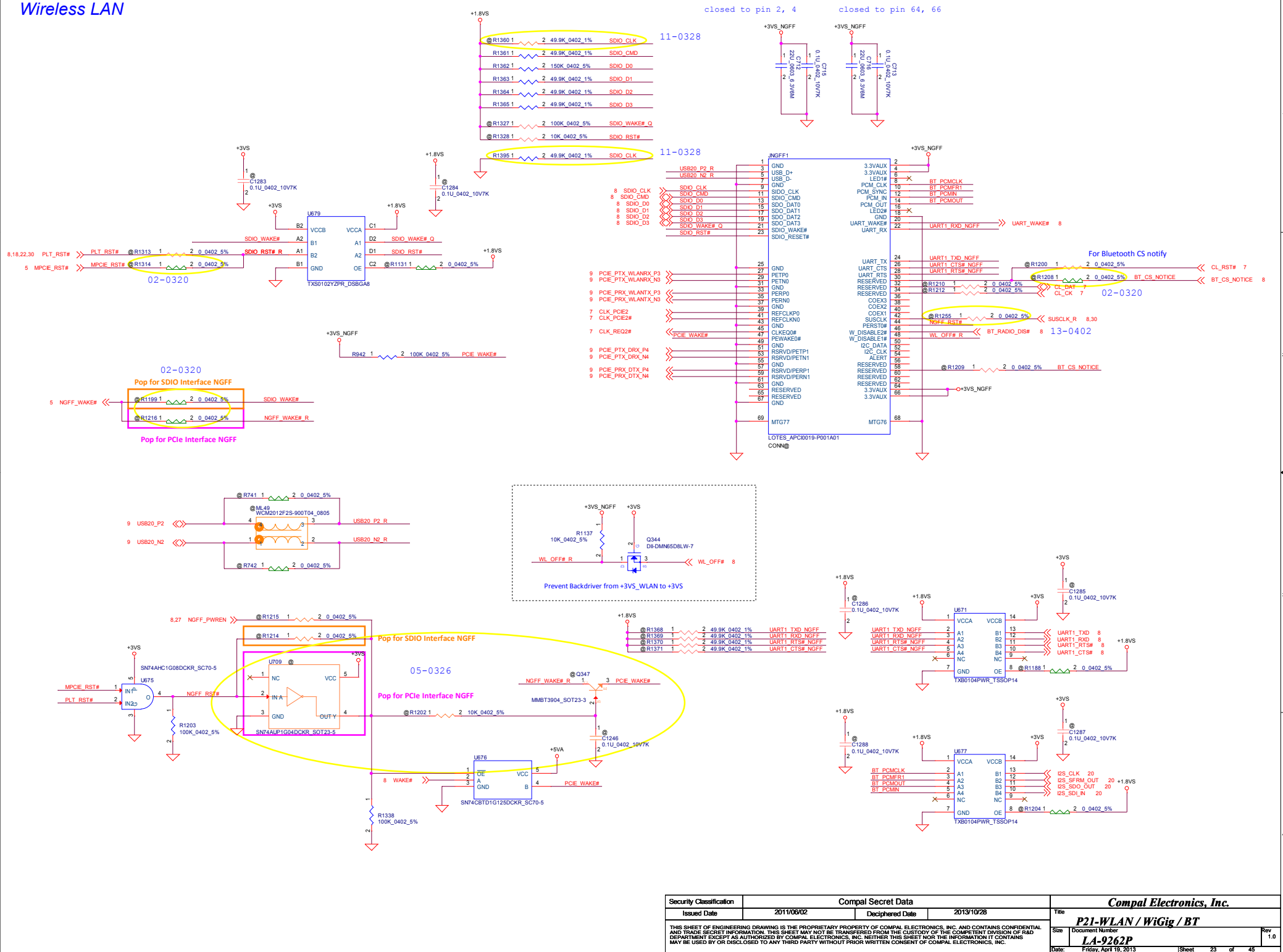


ATMEL TPM



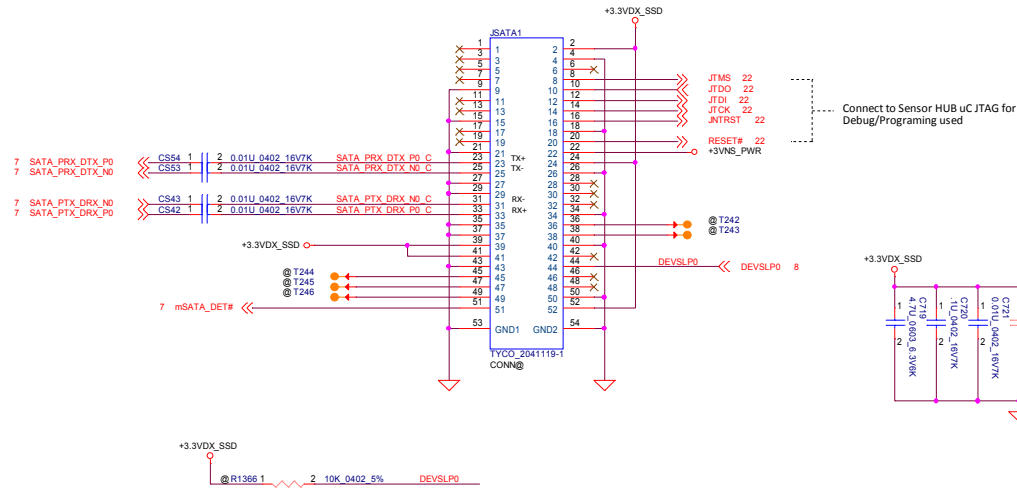
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/06/02		2013/10/28		P20-Sensor Fusion / TPM	
Size		Document Number		Rev	
1		LA-9262P		1.0	
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Wireless LAN

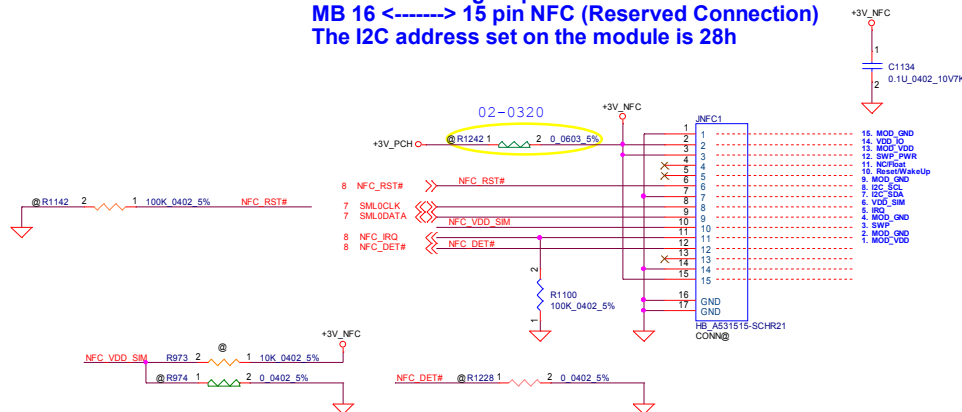


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Issued Date	2011/06/02	Deciphered Date	2013/10/28	P21-WLAN / WiGig / BT		
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mSATA Card

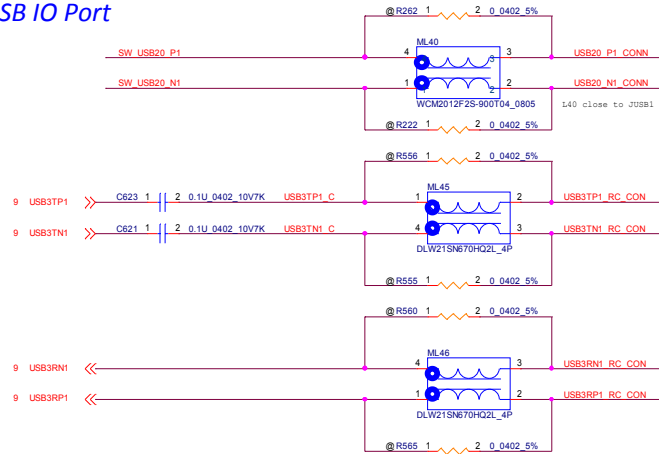


ME Decide using 16 pin conn
MB 16 <-----> 15 pin NFC (Reserved Connection)
The I2C address set on the module is 28h

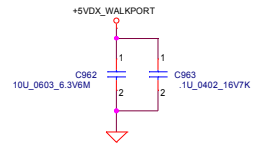
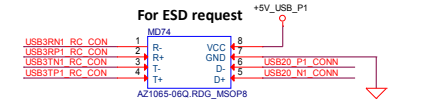
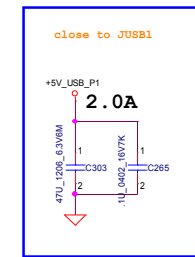
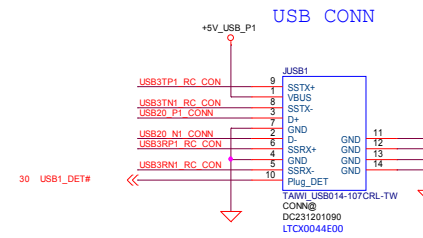
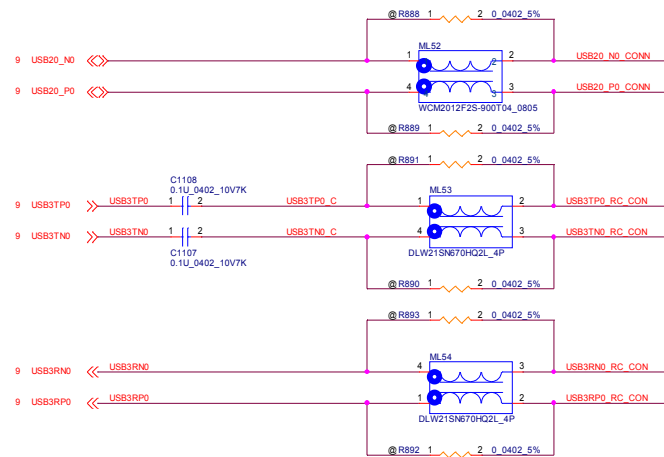


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				Size C	Document Number	Rev
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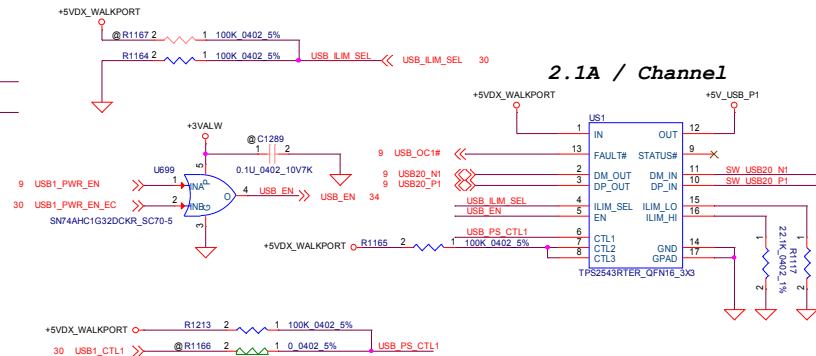
USB IO Port



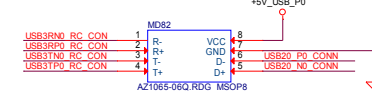
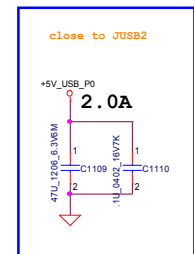
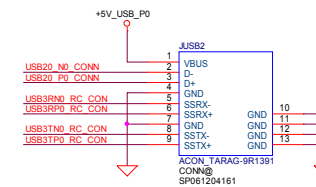
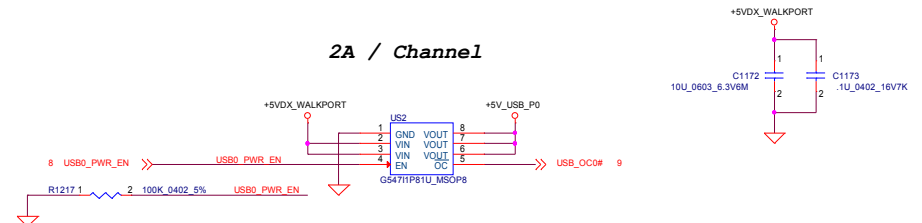
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDF
1	1	1	1	CDP



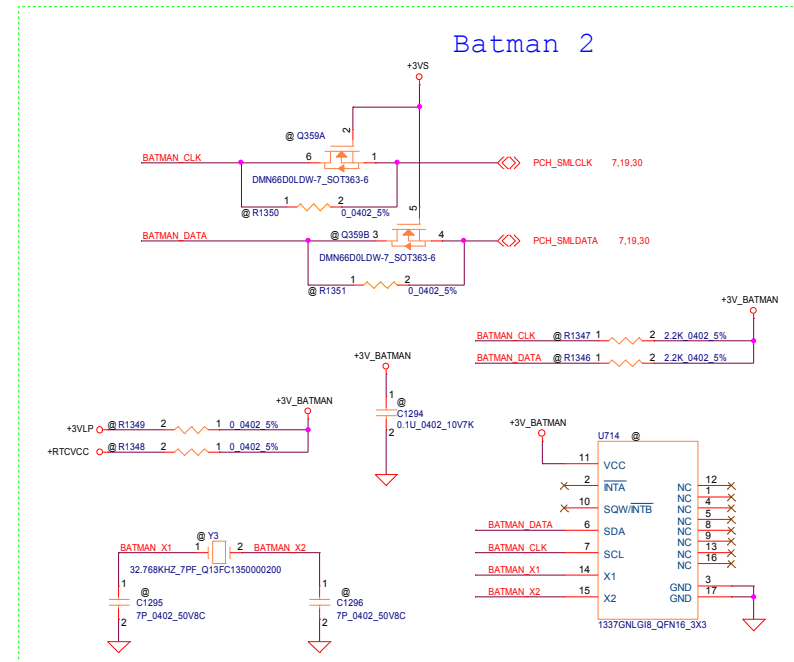
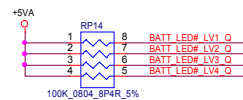
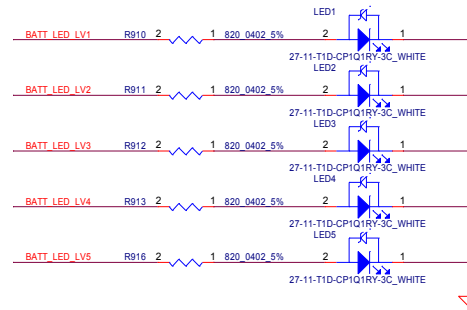
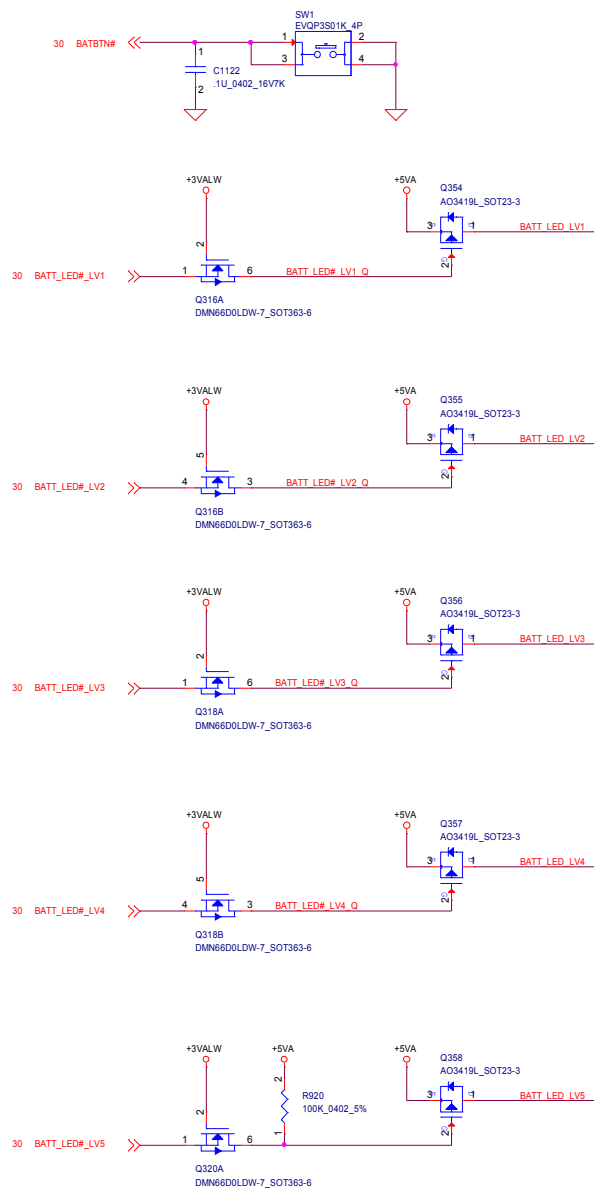
2.1A / Channel



2A / Channel

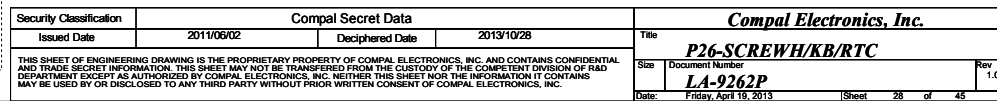


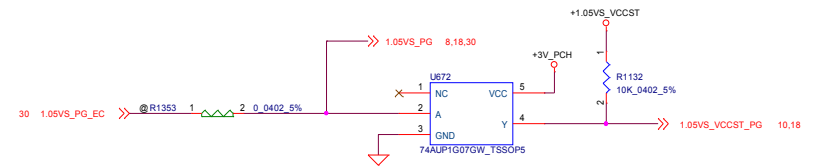
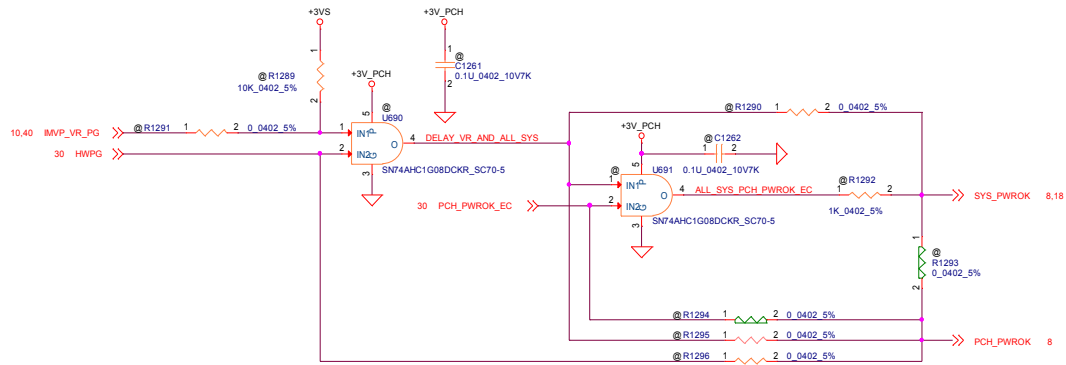
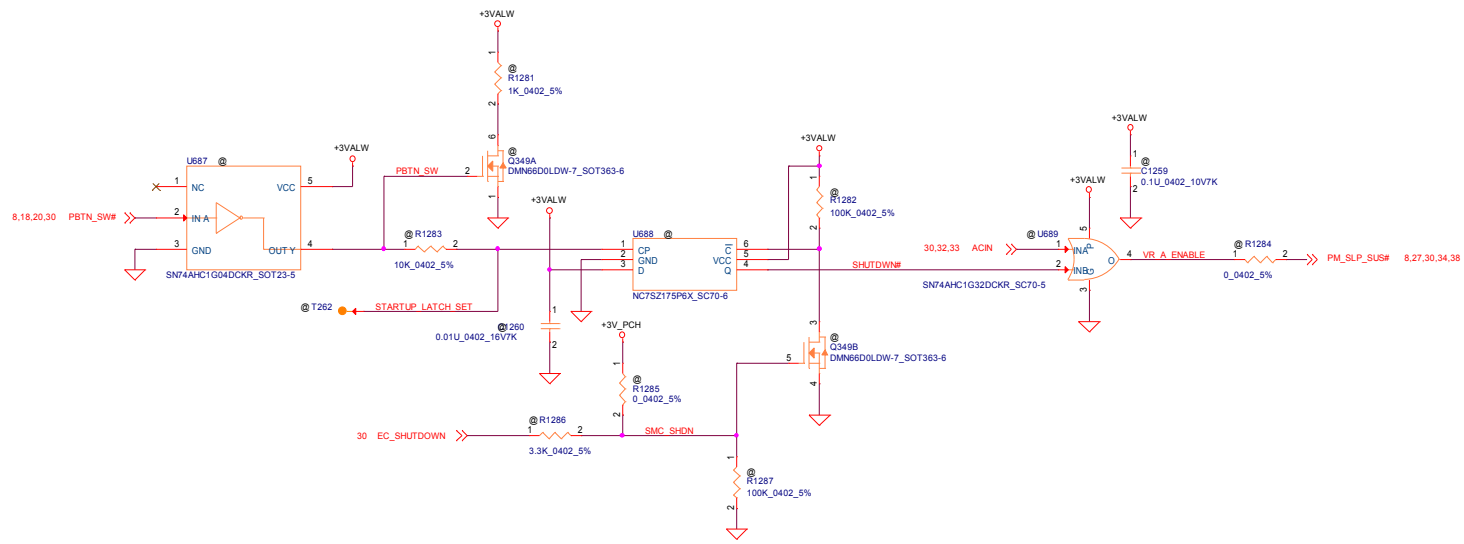
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P23-USB 3.0 IO CONN
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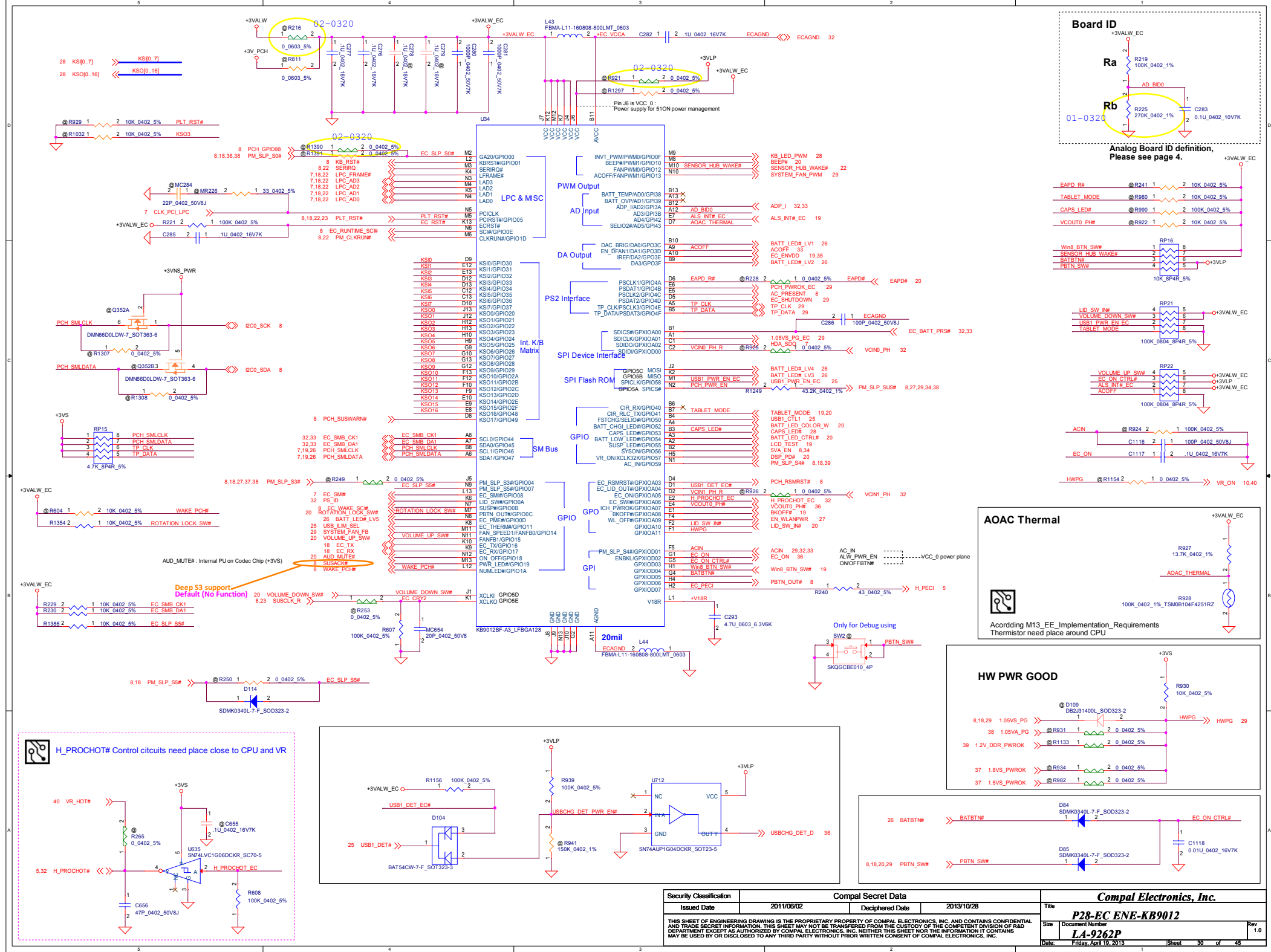


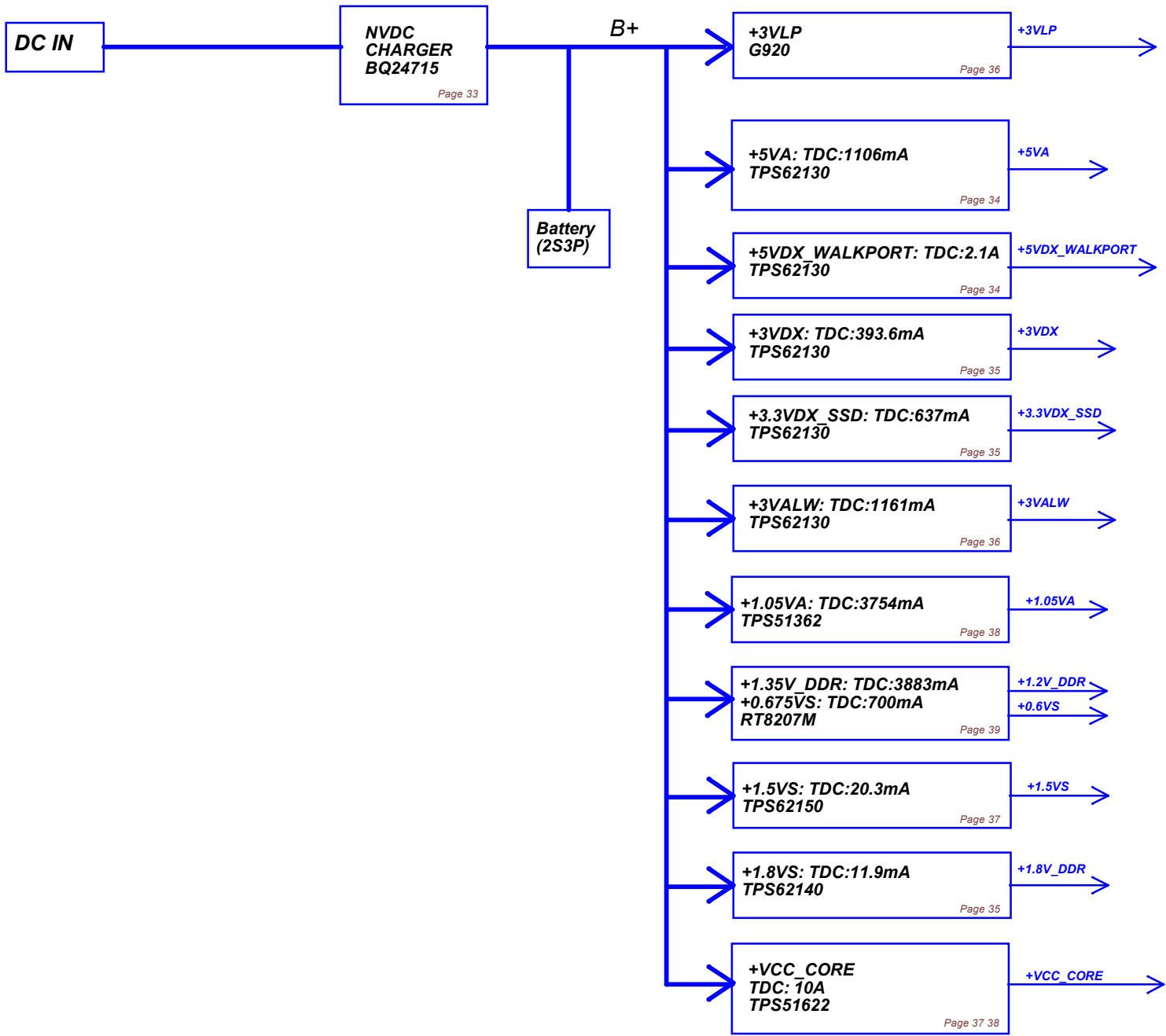
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/06/02		2013/10/28		P24-BAT LED	
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		LA-9262P		Rev	
		Date:		Friday, April 19, 2013	
		Sheet		26 of 45	

Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>	
Issued Date	2011/09/02	Deciphered Date	2013/10/28	Title	<i>P25-DC/DC Interface</i>
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				<i>LA-9262P</i>	
				Date:	Friday, April 19, 2013
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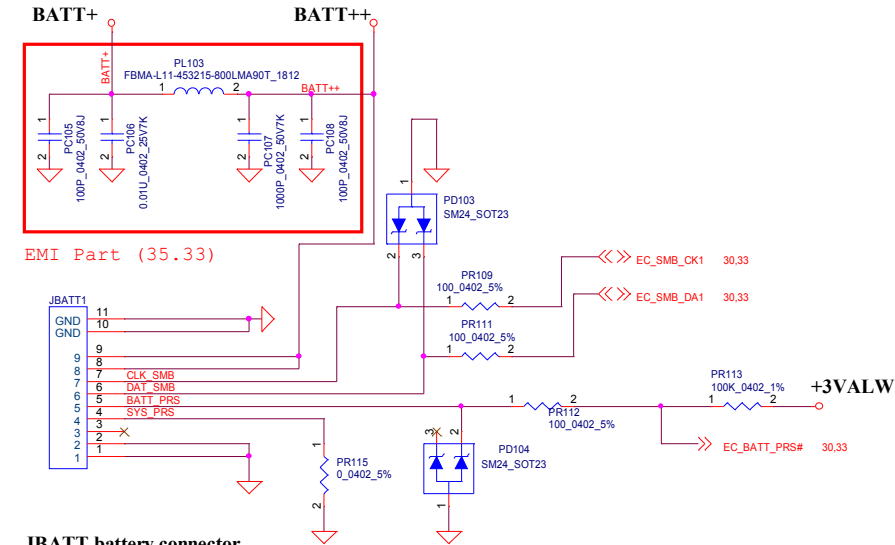








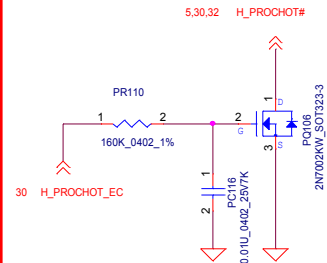
EMI solution for adaptor without ferrite bead
20120507



JBATT battery connector

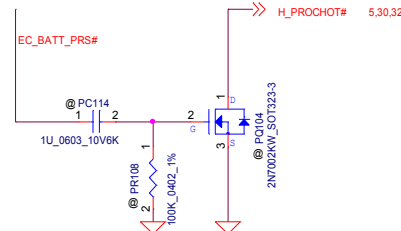
SMART Battery:
1.GND
2.GND
3.BAT_ALERT
4.SYS_PRES
5.BATT_PRS
6.DAT_SMB
7.CLK_SMB
8.BATT++
9.BATT++

Delay adaptor OC H_PROCHOT#
2ms while hybrid power transition



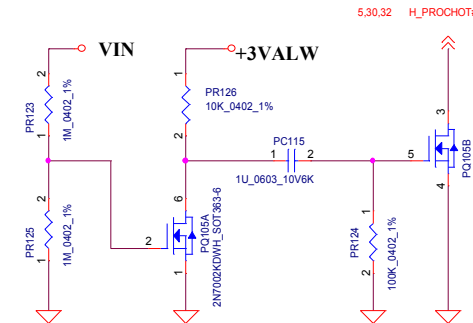
Adaptor protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep DNP in BOM since battery can not
be removed by end user



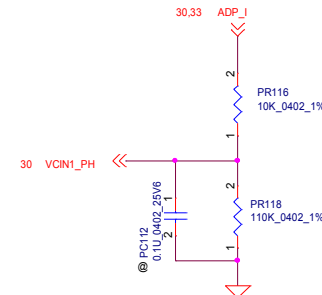
Battery protection:

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



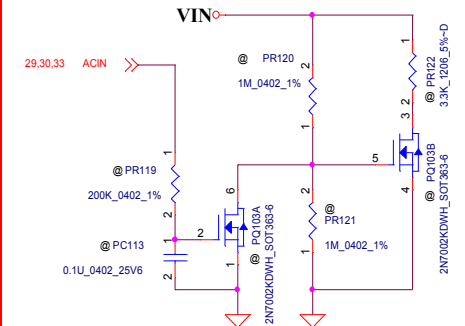
Adaptor protection:

if CP and IPCC failed, adaptor output
=rating 100% and over load 20W
then trigger the H_PROCHOT# by EC



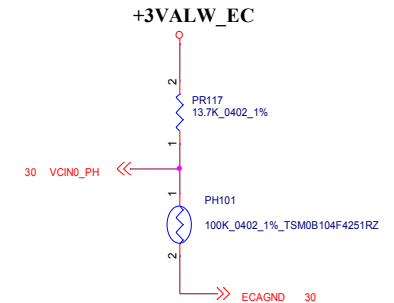
Erp lot6 Circuit

keep DNP in BOM since Dell 45W
adaptor has no hiccup mode

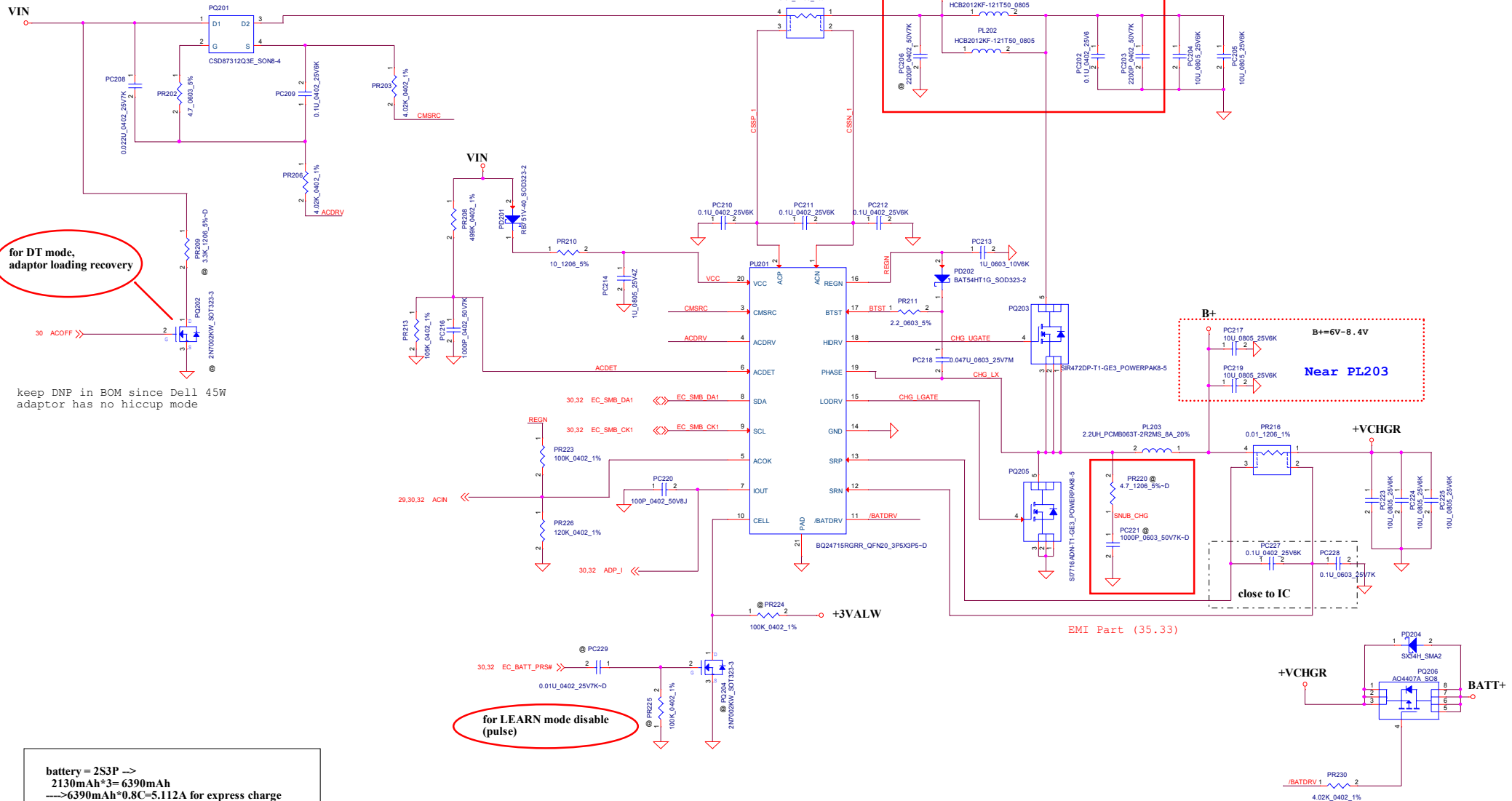


PH101 under CPU bottom side :

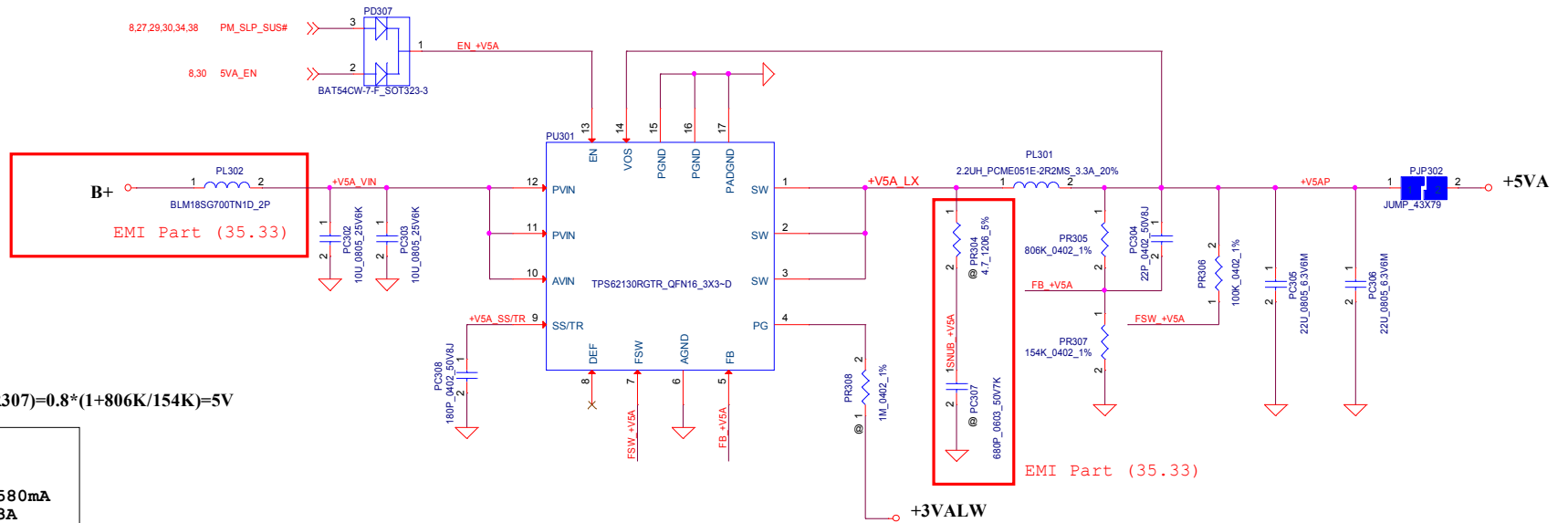
CPU thermal protection
@88+-3 degree C
Recovery at 80+-3 degree C



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P30-PWR DCIN/BATT CONN/OTP
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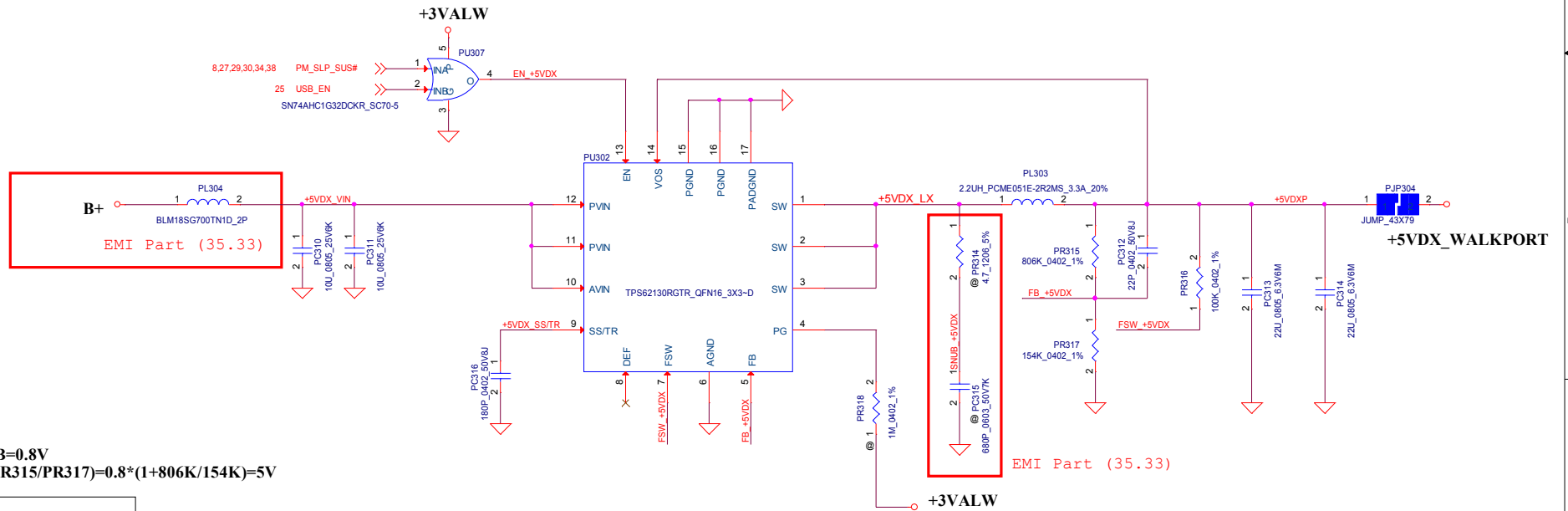


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P31-PWR NVDC CHARGER
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$\langle V_o = 5V \rangle$ $V_{FB} = 0.8V$
 $V_o = V_{FB} * (1 + PR305/PR307) = 0.8 * (1 + 806K/154K) = 5V$

+5VA
 TDC 1106mA
 Peak Current 1580mA
 OCP setting @ 3A



$\langle V_o = 5V \rangle$ $V_{FB} = 0.8V$
 $V_o = V_{FB} * (1 + PR315/PR317) = 0.8 * (1 + 806K/154K) = 5V$

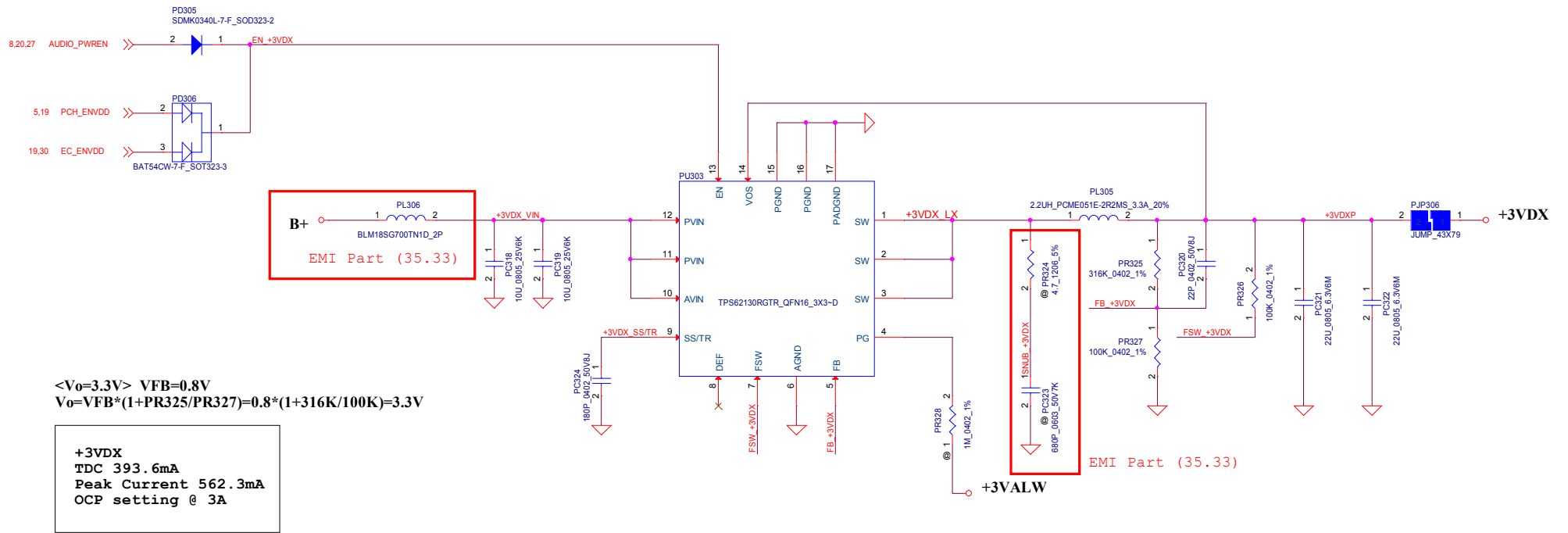
+5VDX WALKPORT
 TDC 2.1A
 Peak Current 3A
 OCP setting @ 3A

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/02				Title			
				Deciphered Date				2013/10/28			
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								Document Number			
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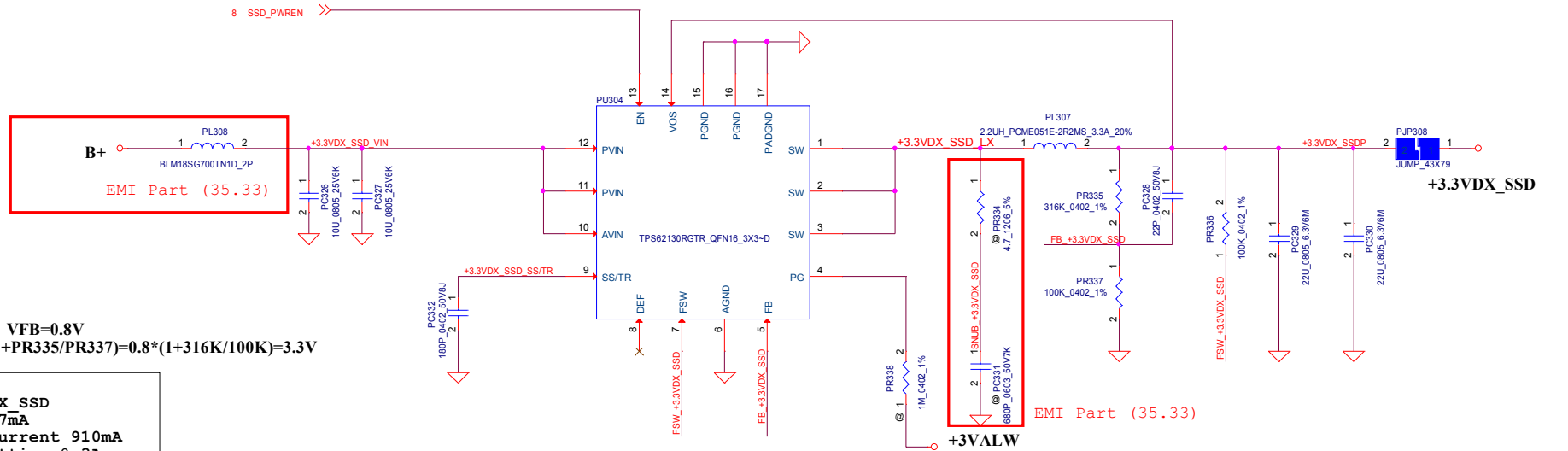
P32-PWR +5V_VR

Rev 1.0



<V_o=3.3V> VFB=0.8V
V_o=VFB*(1+PR335/PR337)=0.8*(1+316K/100K)=3.3V

+3.3VDX SSD
TDC 637mA
Peak Current 910mA
OCP setting @ 3A

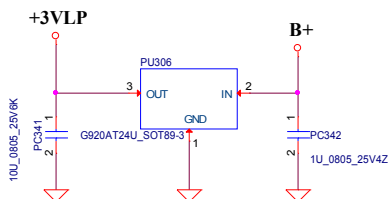
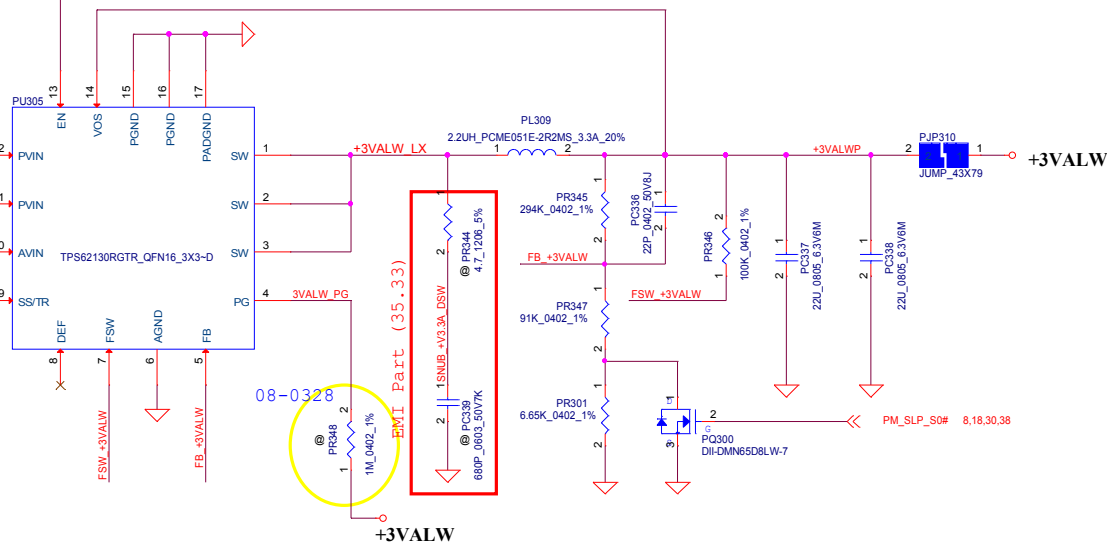
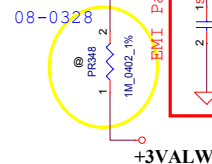
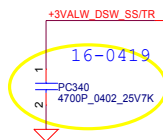


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Issued Date				2011/06/02				Title			
Deciphered Date				2013/10/28				P33-PWR +3.3V VR(1/2)			
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								LA-9262P			
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								1.0			
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								Friday, April 19, 2013			
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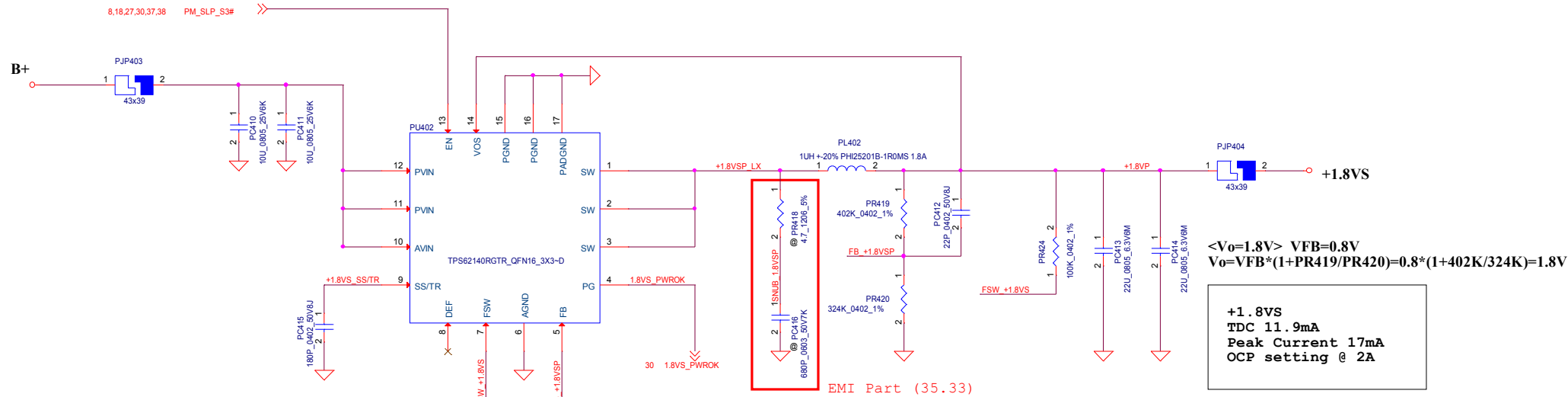
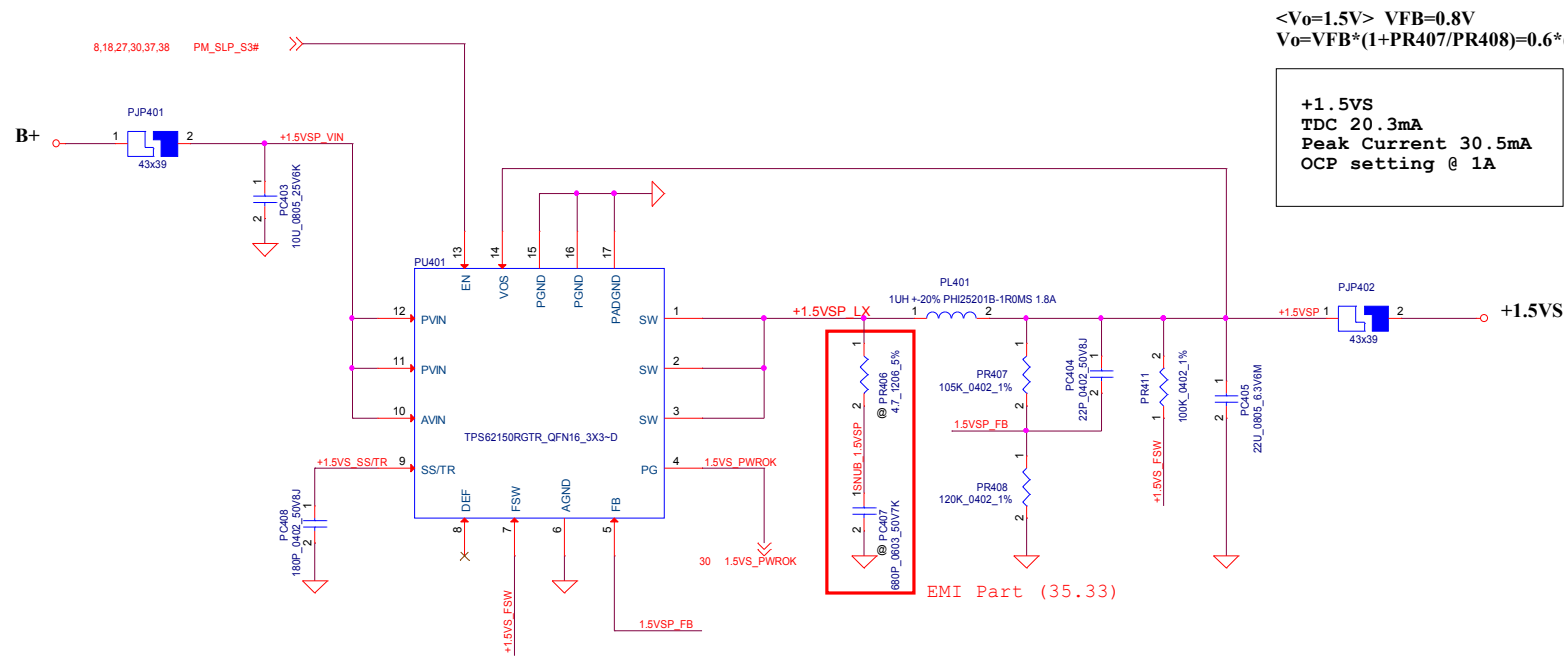


$\langle V_o = 3.3V \rangle$ $V_{FB} = 0.8V$
 $V_o = V_{FB} * (1 + PR345/PR347) = 0.8 * (1 + 316K/100K) = 3.3V$

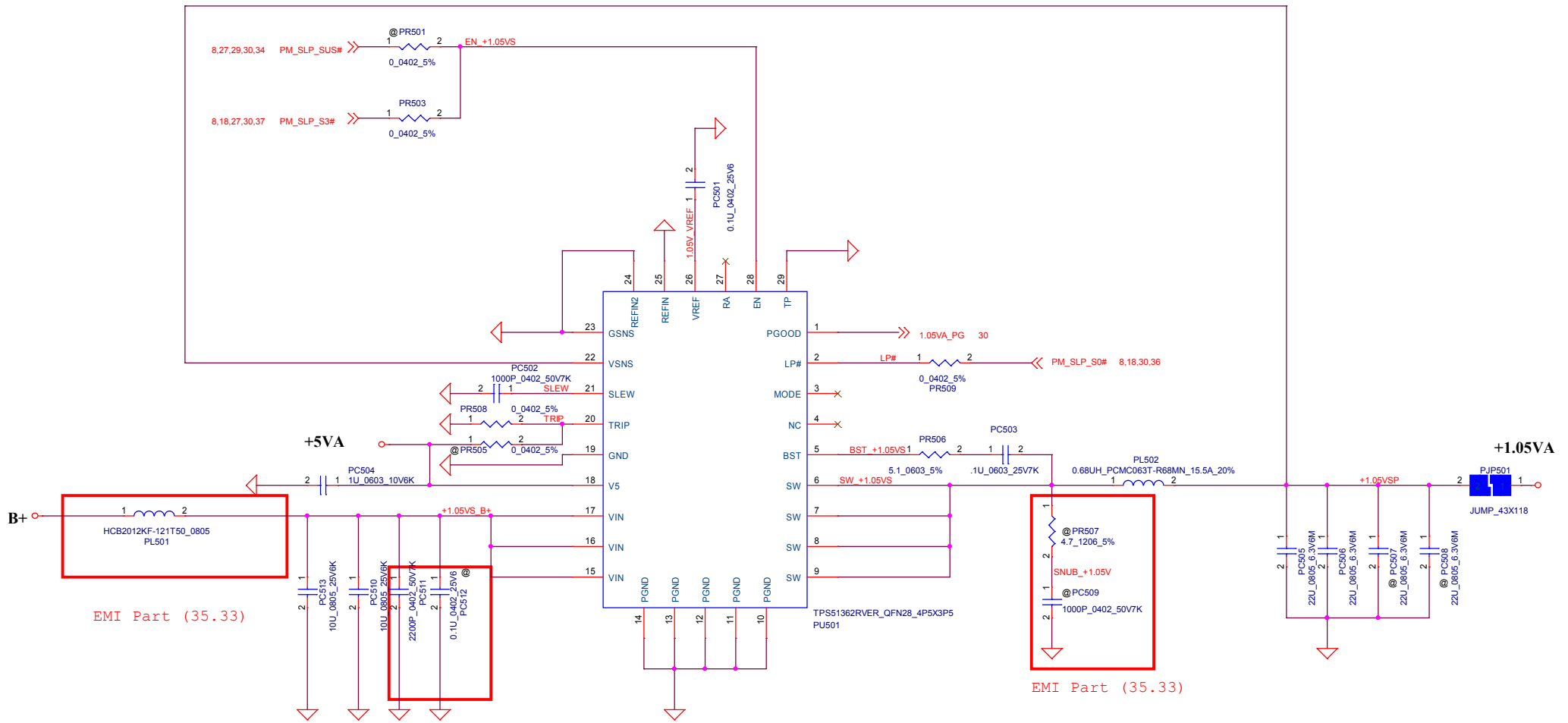
+3VALW
 TDC 161mA
 Peak Current 2301mA
 OCP setting @ 3A



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			Size Document Number	Rev
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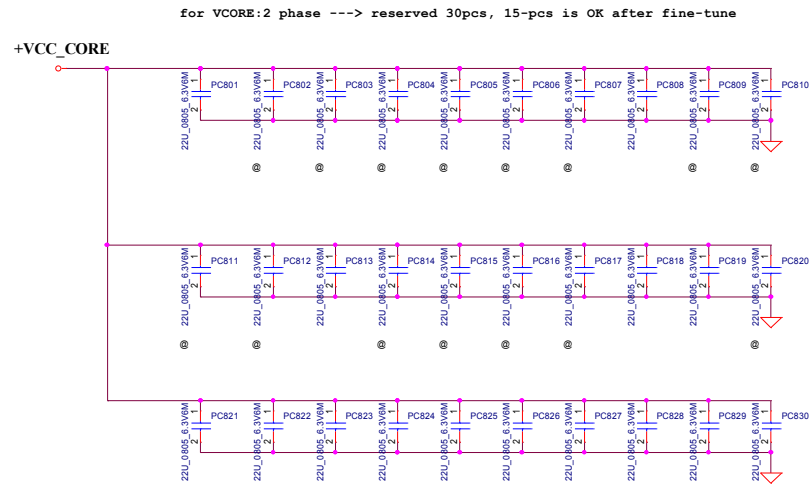


Security Classification				Compal Secret Data				Compal Electronics, Inc.		
Issued Date				2011/06/02				Title		
Deciphered Date				2013/10/28				P35-PWR +1.5VS/+1.8V DDR		
Size				Document Number				Rev		
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+1.05VA
TDC 3754mA
Peak Current 3942mA
OCP setting @ 8A

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Issued Date		2011/06/02	Deciphered Date		2013/10/28					
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						P39-PWR PROCESSOR DECOUPLING				
						Size	Document Number			
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Version Change List (P. I. R. List)

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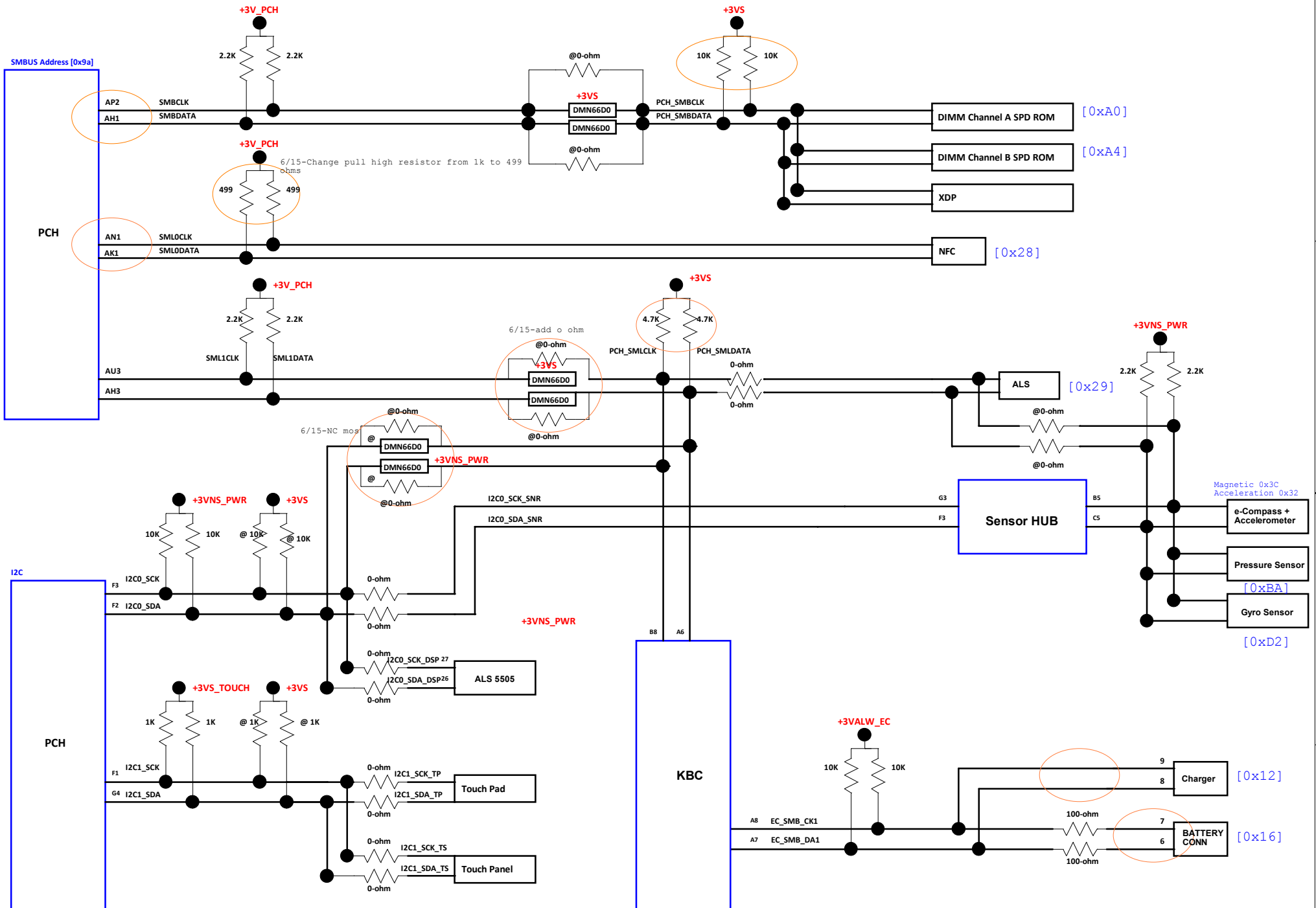
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	
36			20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
34			20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
34			20121018	Compal_Power	design change, delete PU301~PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
35							
36							
36			20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		
34			20121023	dell	reject power design change of 3.3V, 5V, 1.8V and 1.5V		
35							
36							
38			20121203	Compal_EMI	change PL501 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
39			20121203	Compal_EMI	change PL601 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
40			20121203	Compal_EMI	add PL703 for EMI	add PL701 HCB2012KF-121T50_0805	
38			20121203	Compal_Power	create PR509 0_0402_5% for debug	add PR509 0_0402_5%	
32			20121205	Compal_HW	create PR5107 10K_0402_1% for test	add PR107 10K_0402_1%	
40			20121213	Compal_Power	fine tune VR transient	de-pop PC714, change PR711 from 150K to be 100K	
40			20130122	Compal_Power	follow Intel's recommendation	change PR737 from 110 OHM to be 130 OHM	
33			20130131	Compal_RF	reserved a MLCC for RF consideration	create PC206 2200P_0402_50V7K	
40			20130221	Compal_RF	for RF noise reducing	pop PC703, PR719 and PC712, PR734 and PC722 for VCORE	
39			20130221	Compal_RF	for RF noise reducing	pop PR605 and PC613 for DDR	

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