

Sapporo 300P Rev 0.3 Schematics Document

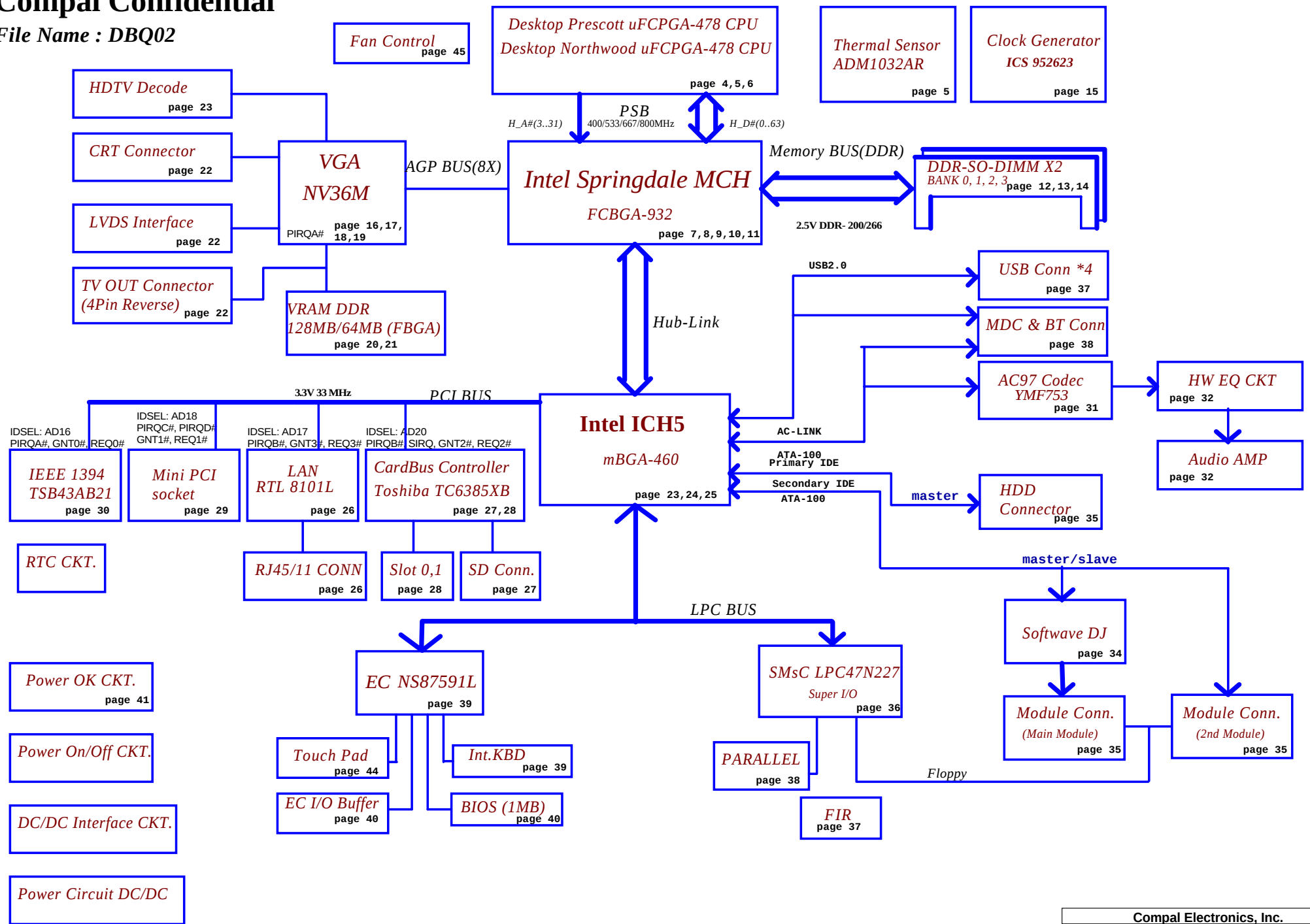
**Intel Prescott uFCPGA-478 / P4 Northwood
with Springdale / ICH5 / nVIDIA NV36M / HDTV chipset**

2003 / 11 / 25

Compal Electronics, Inc.		
Title		
Cover Sheet		
Size B	Document Number Sapporo 300P	Rev 0.3
Date: 星期一, 十二月 01, 2003	Sheet 1 of 57	E

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File Name : DBQ02



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Block Diagram			
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VTT_GMCH	+1.225V (Prescott) / +1.45V (Northwood)	ON	OFF	OFF
+VGA_CORE	1.3V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD22		

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ168	0011 0100 b
(24C04)	1011 000Xb		

EC SM Bus2 address

ICH5 SM Bus address

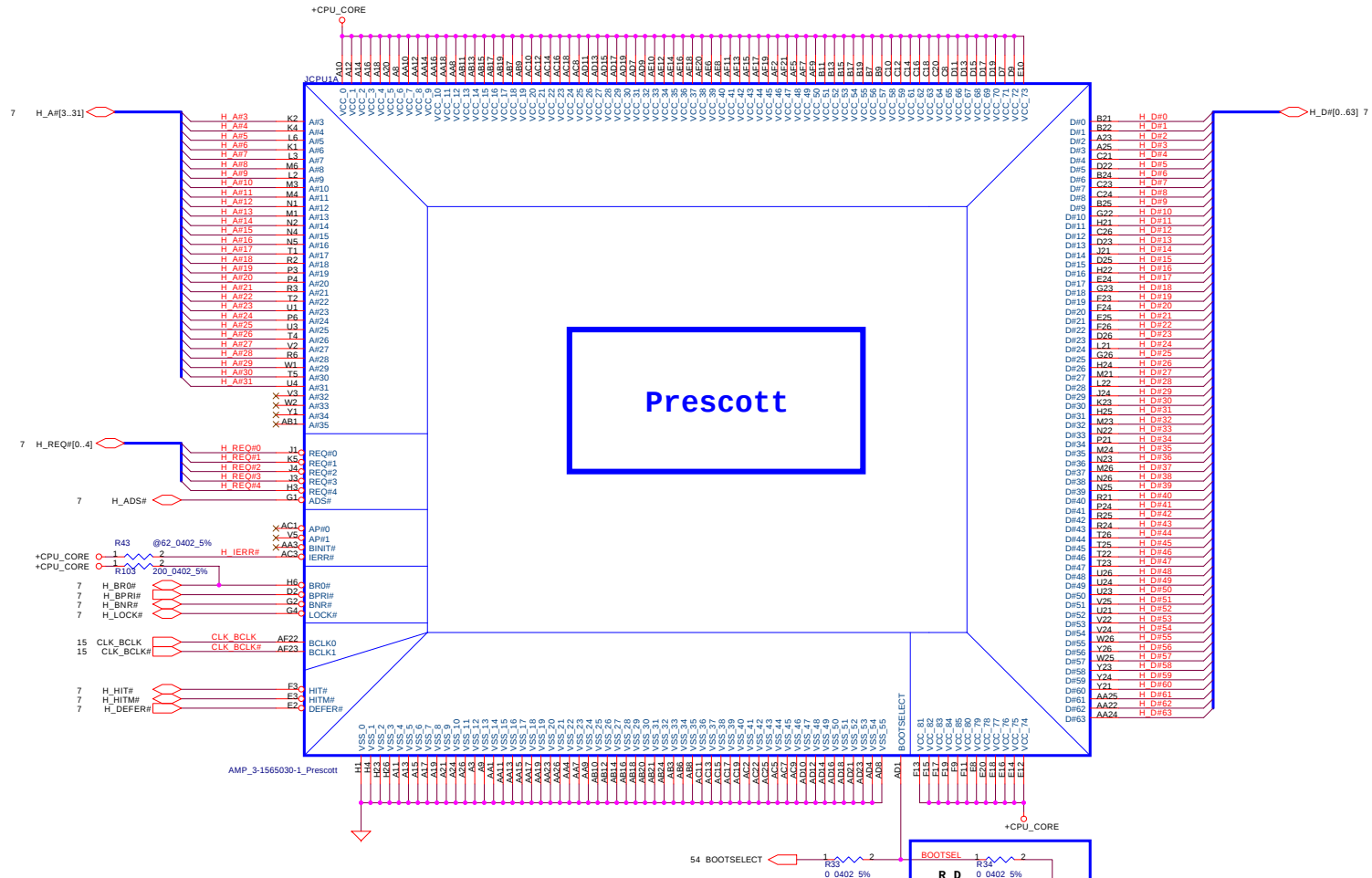
Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
Full ON									
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

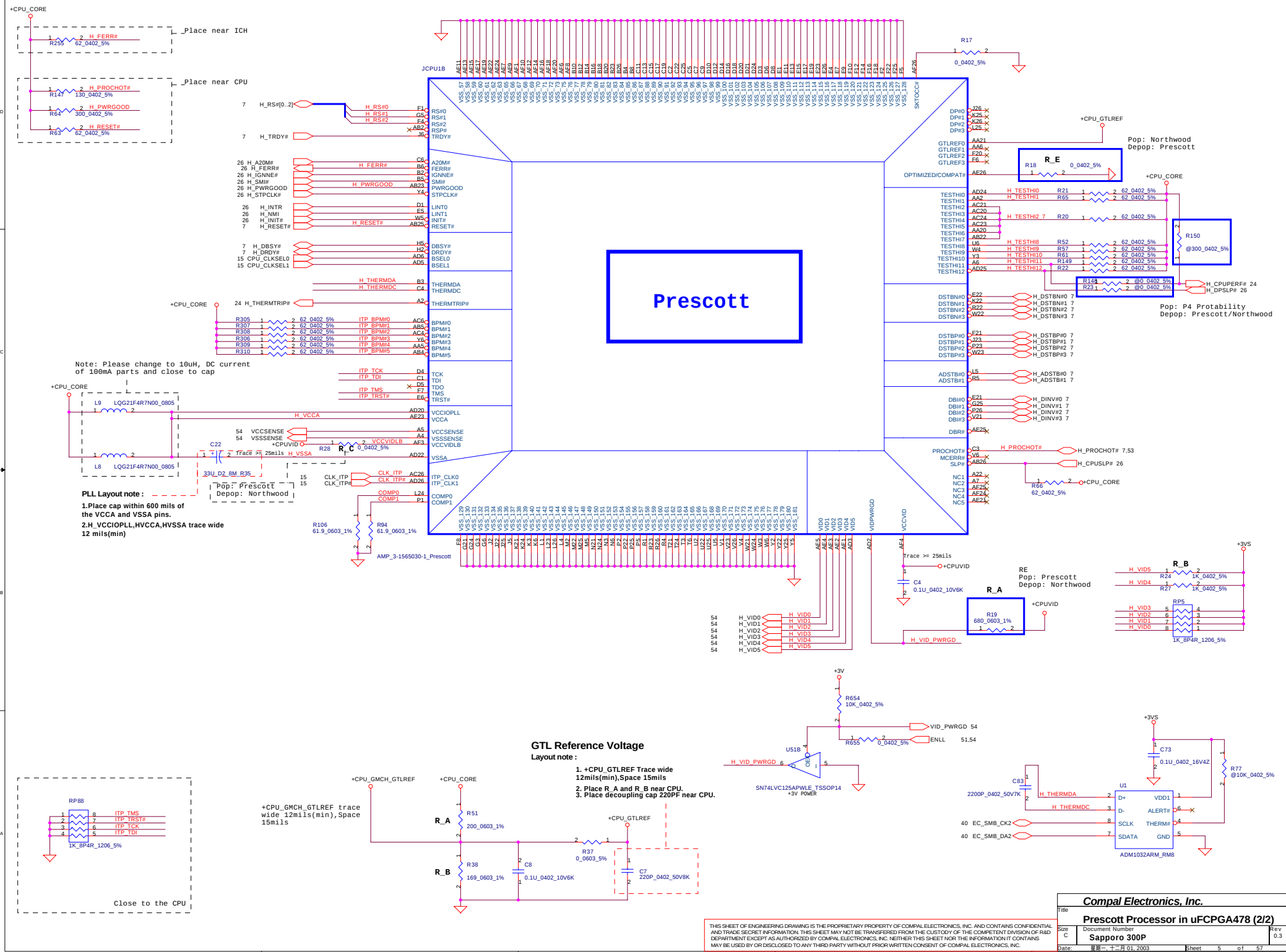
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

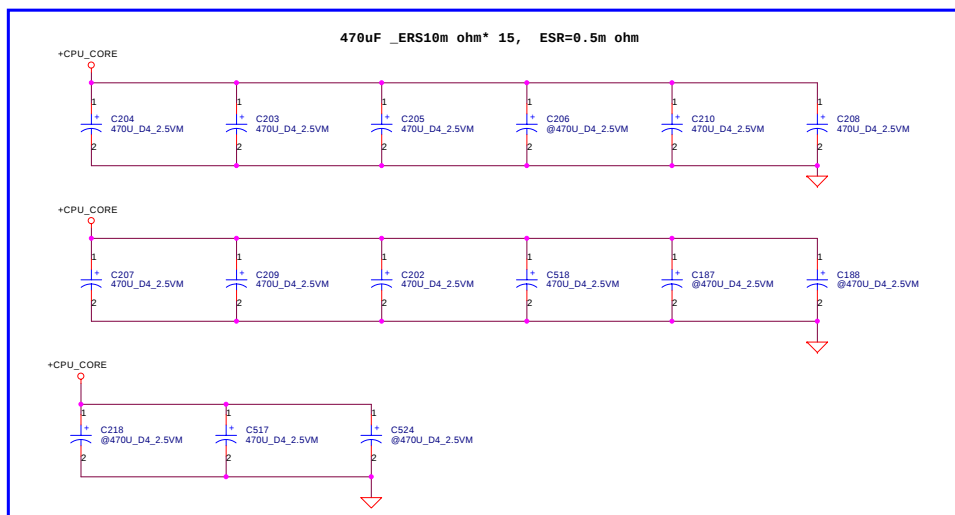
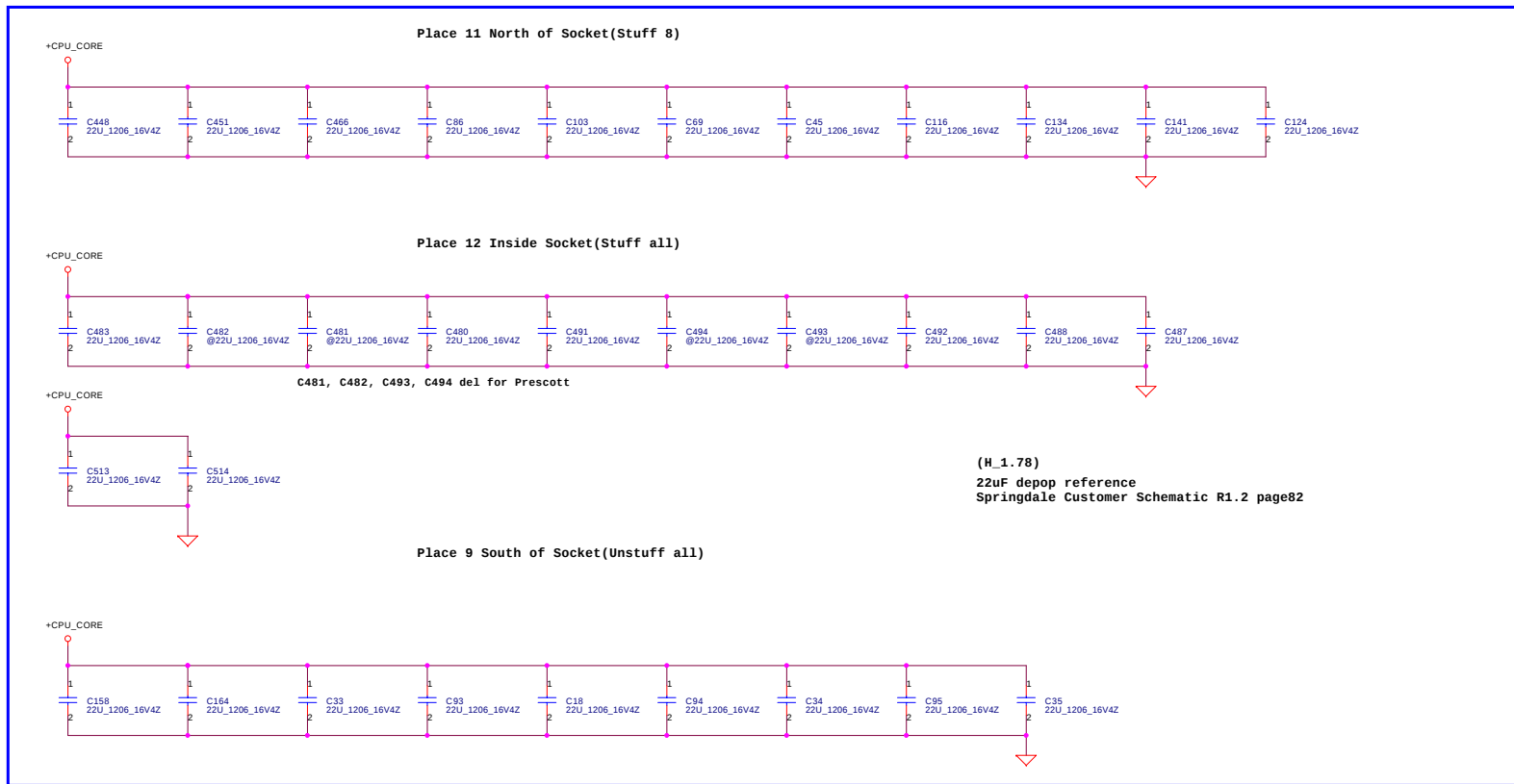
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	



Reference Intel document Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0 Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5						
Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood	Prescott
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PB6#	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AA20	ITPCLKOUT0	Pull-up 62ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 62ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AD2	NC	float	VIDPWRG0	Pull-up 8.2Kohm to +VCCVID	Depop	Pop
AD3	NC	float	VID5	Pull-up 1Kohm to +3VRUN & connect to PWRIC	Depop	Pop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	Depop	Pop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter		
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter		
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	Pop	Depop
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	Pop	Depop

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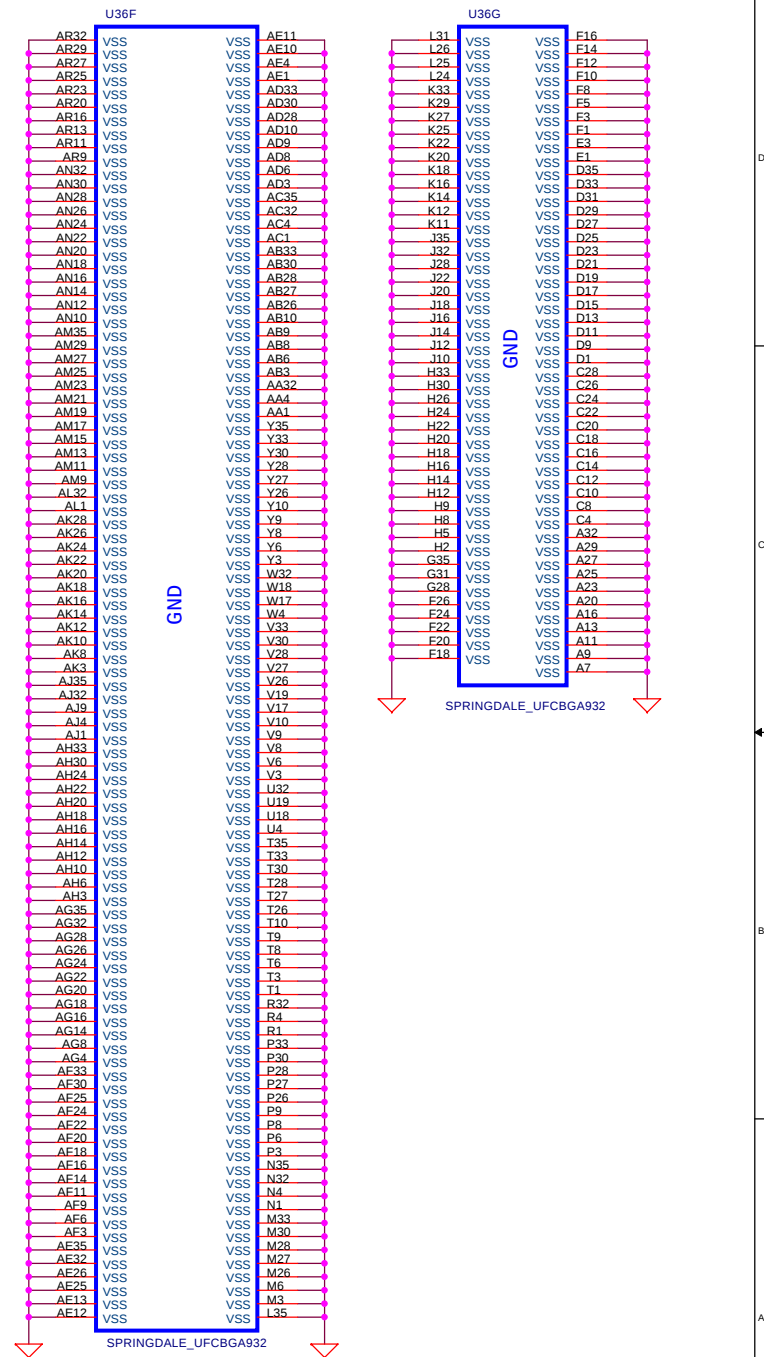
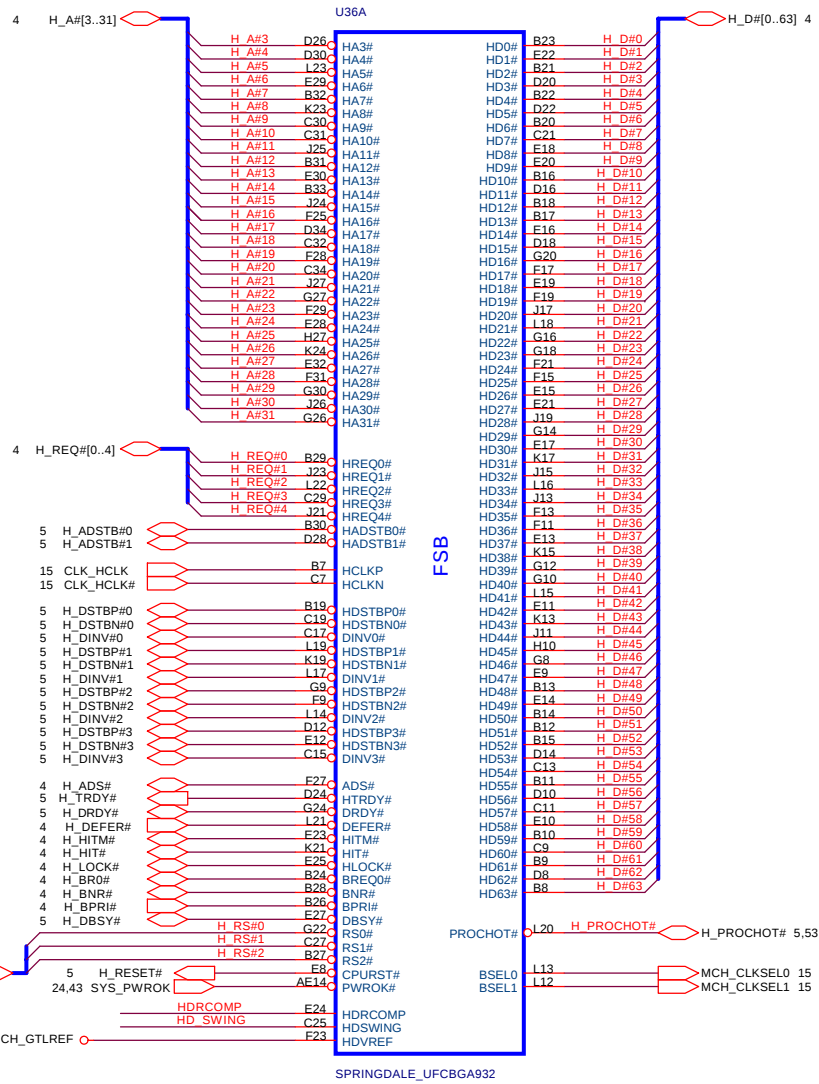
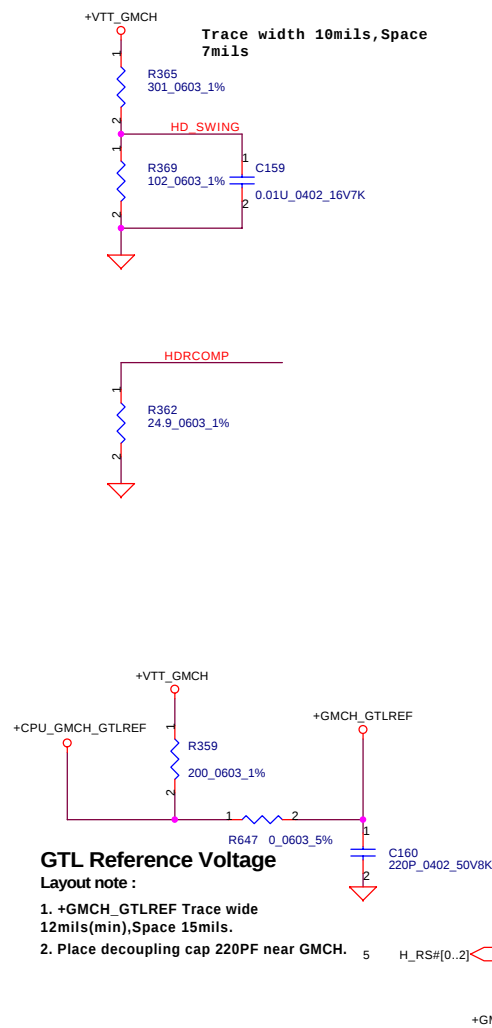


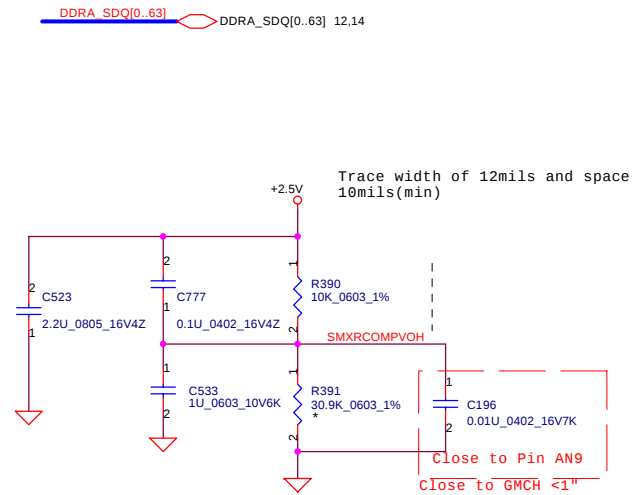
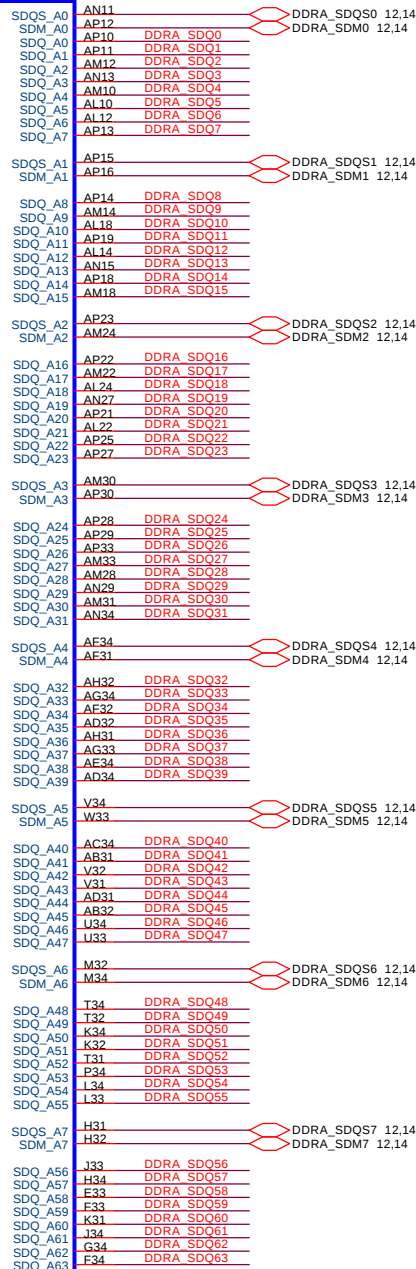
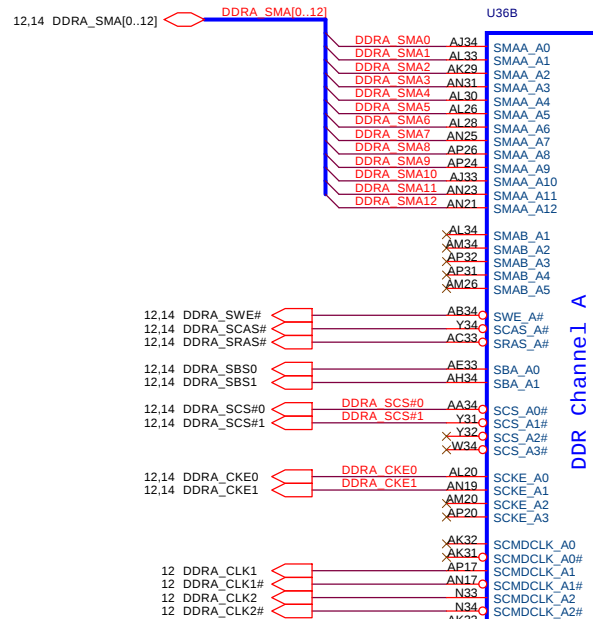


Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32

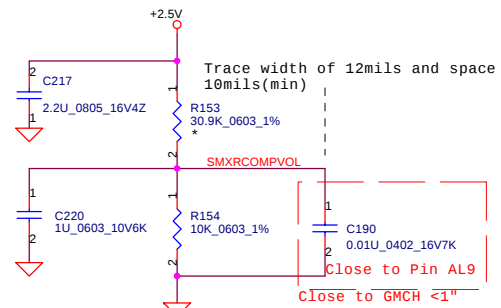
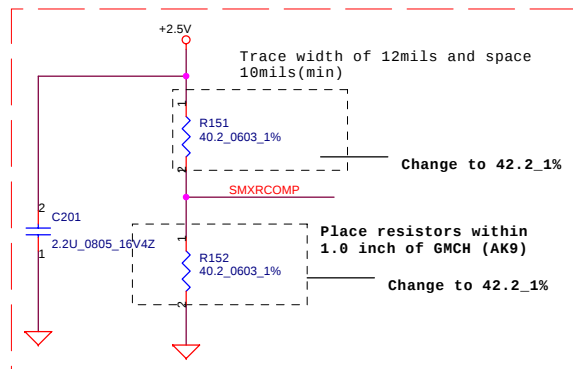
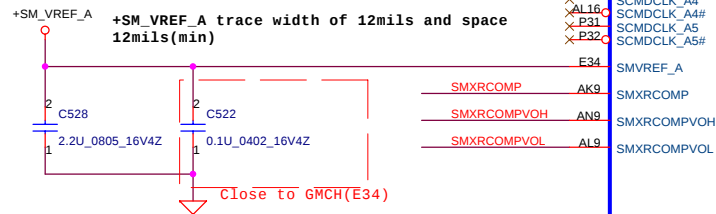
Trace width 10mils,Space
7mils





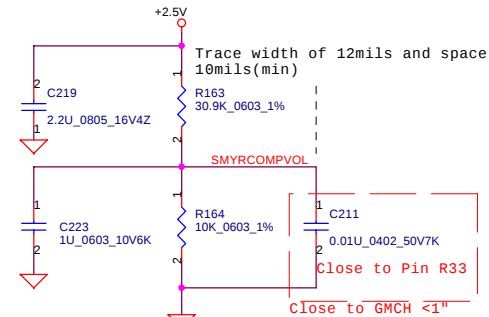
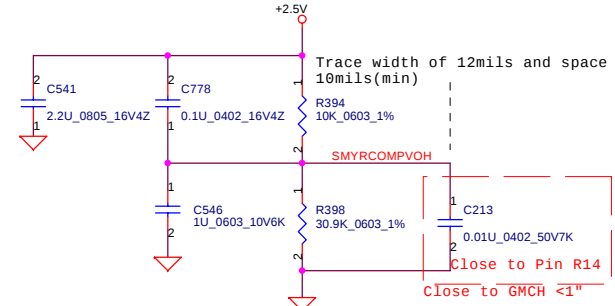
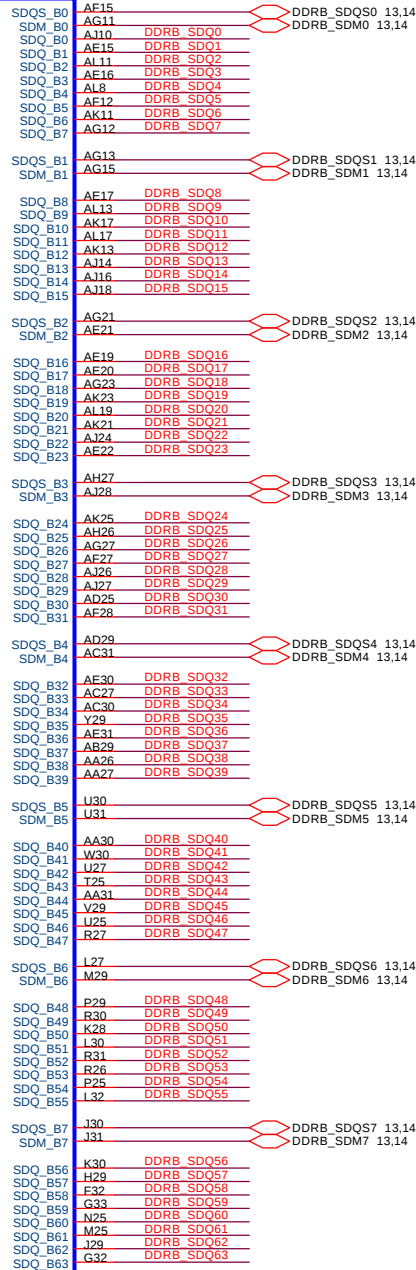
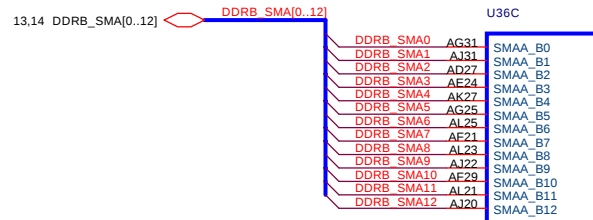
* Change to 31.12K

Follow Intel design guide
R1.11(12474) page124,125

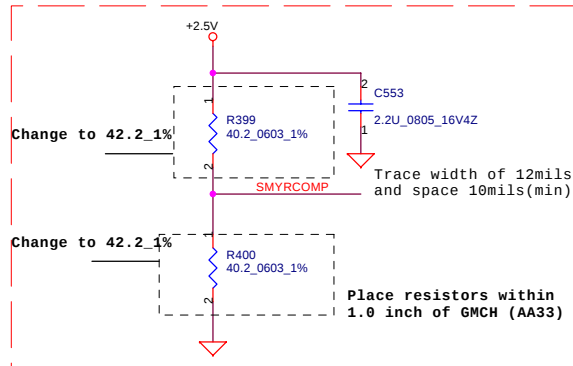
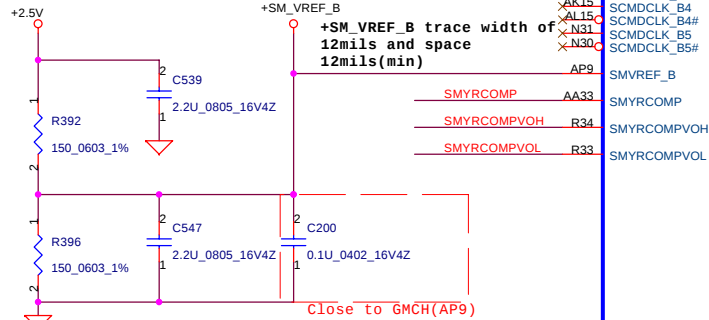


SPRINGDALE_UFCBGA932

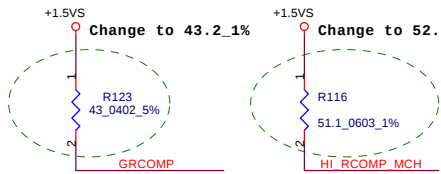
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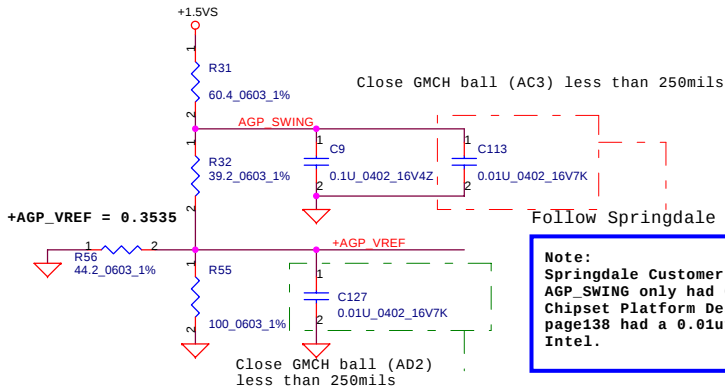
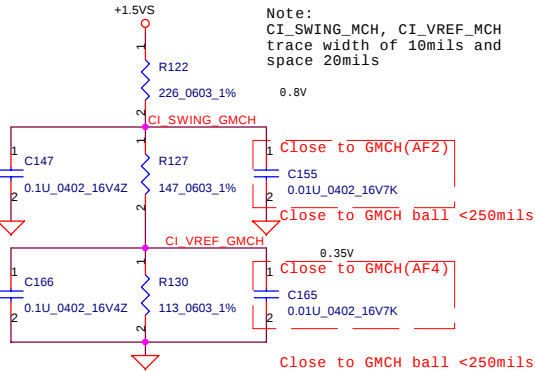
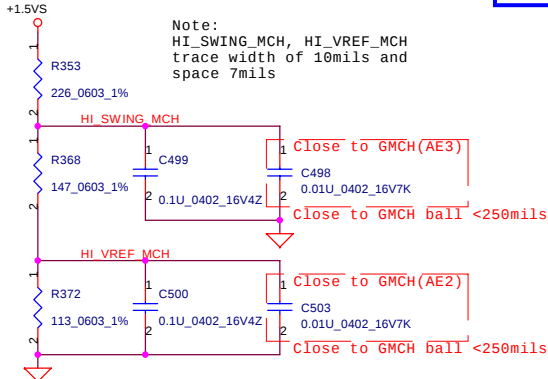
SM_VREF_B and SM_VREF_A are connected inside GMCH.



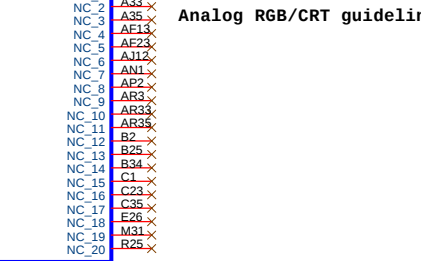
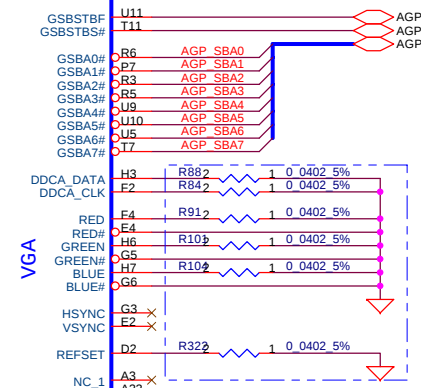
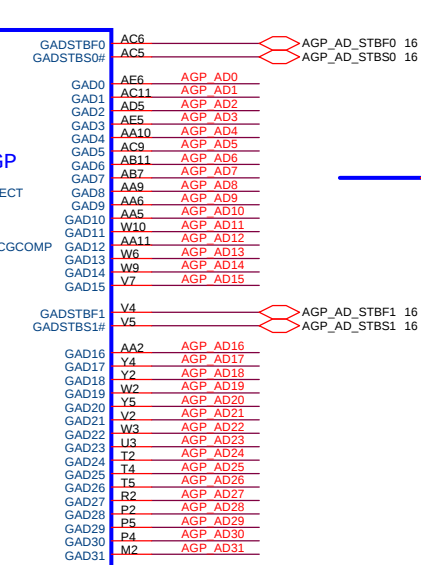
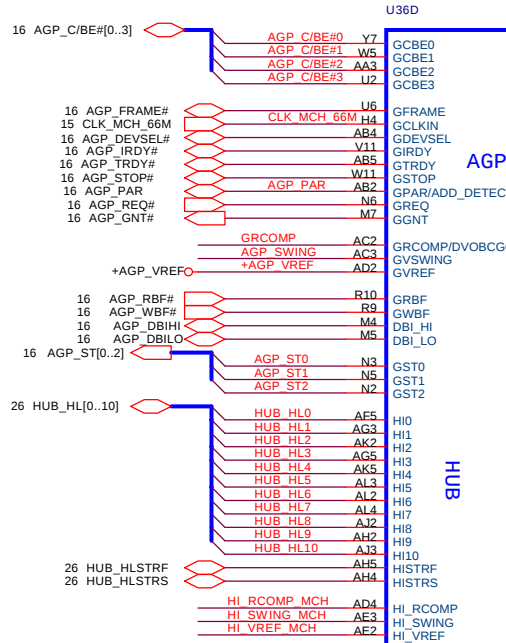
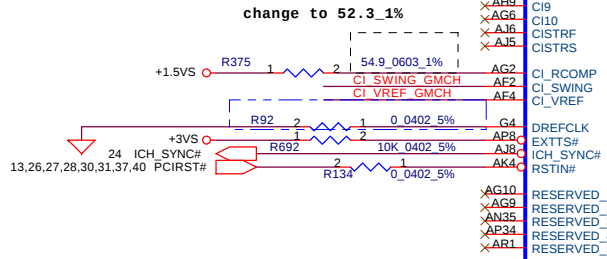
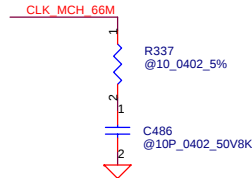
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1: External AGP
0: Internal Graphics

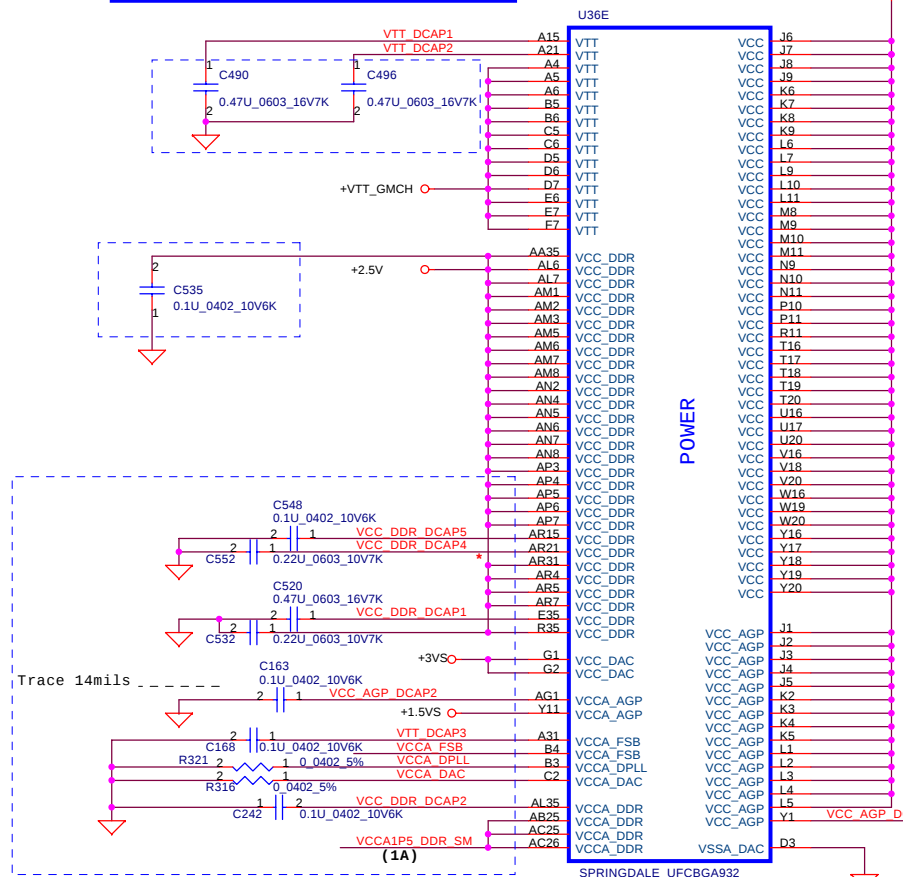


Note:
Springdale Customer Schematic R1.2 page18
AGP_SWING only had 0.1u cap ; But Springdale
Chipset Platform Design guide Rev1.11(12474)
page138 had a 0.01uf cap. need confirm with
Intel.



Analog RGB/CRT guidelines for Springdale-P

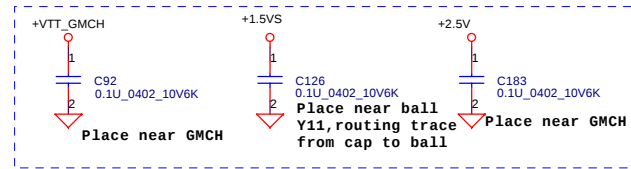
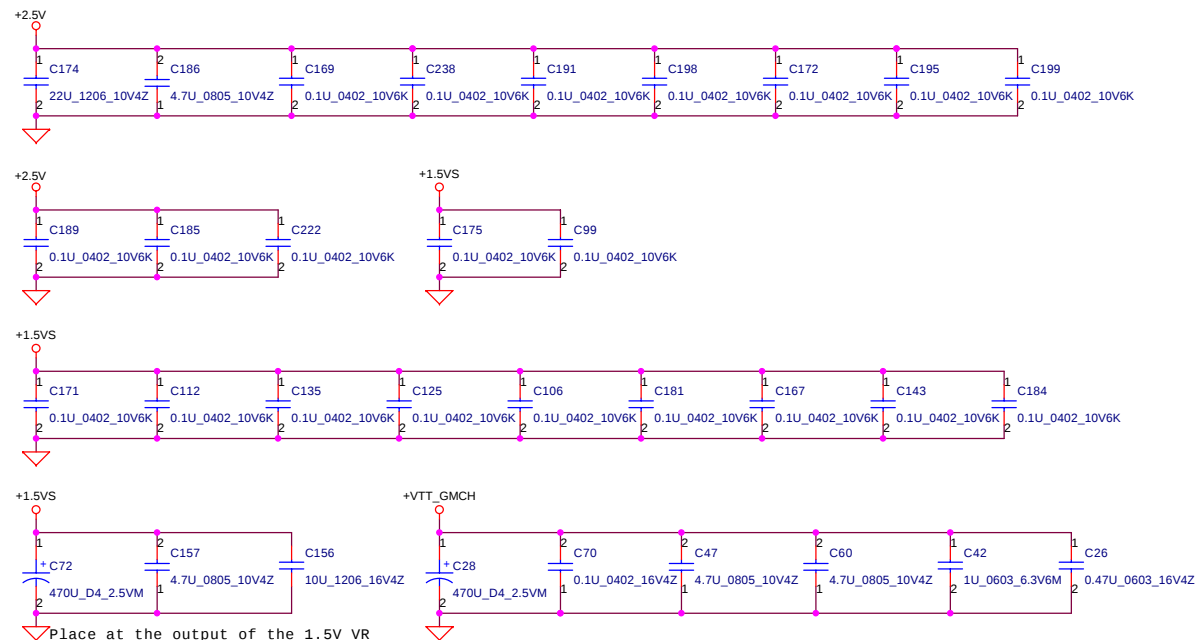
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via



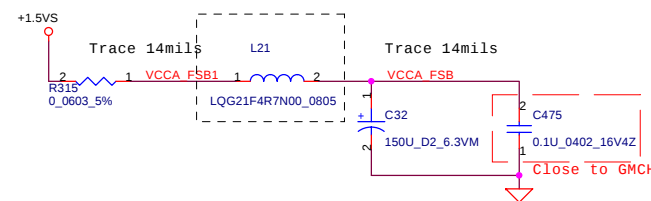
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via

Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page246,248

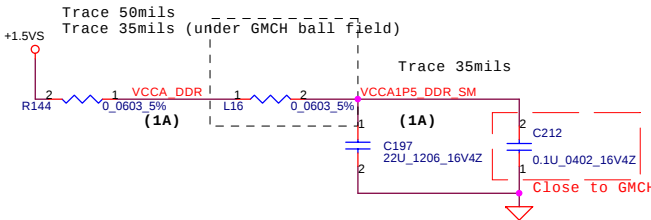
Decoupling Reference Document:
Springdale Customer Schematic R1.2 page84



Note: Please change to 0.82uH, DC current
of 30mA parts and close to cap



Note: Please change to 1uH(0.54uH-D-IN), DC current
of 1000mA parts and close to cap



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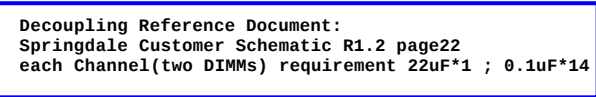
Springdale-Decoupling (5/5)

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AND TRADE SECRET IN



Decoupling Reference Document:

each Channel(two DIMMs) requirement 22uF*1 ; 0.1uF*14

Springdale Chipset Platform Design guide Rev1.11

(12474)pag 271 each DIMM(two) requirement 0.1uF*42

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DDR-SODIMM SLOT1

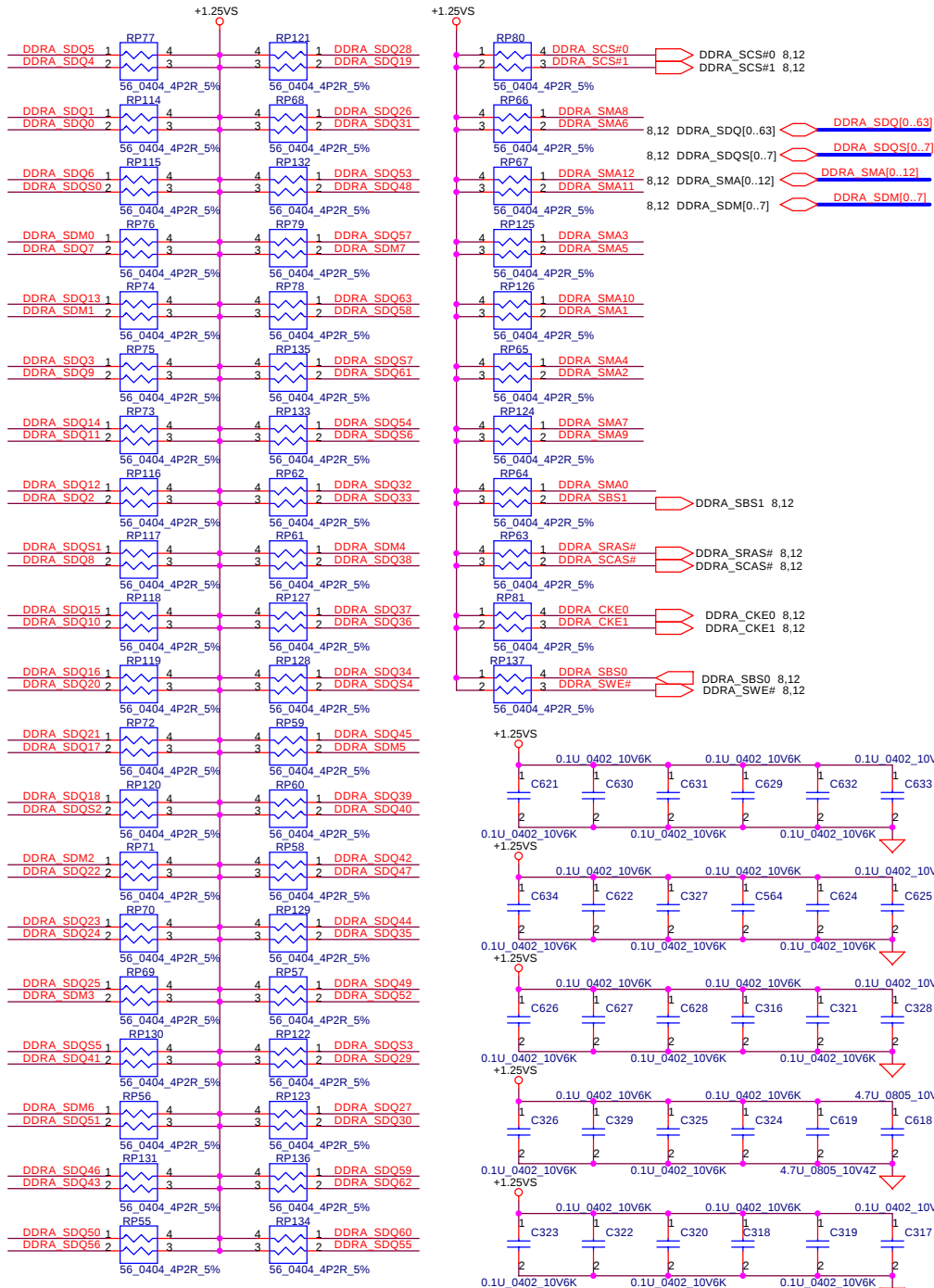
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DDR-SODIMM SLOT2			
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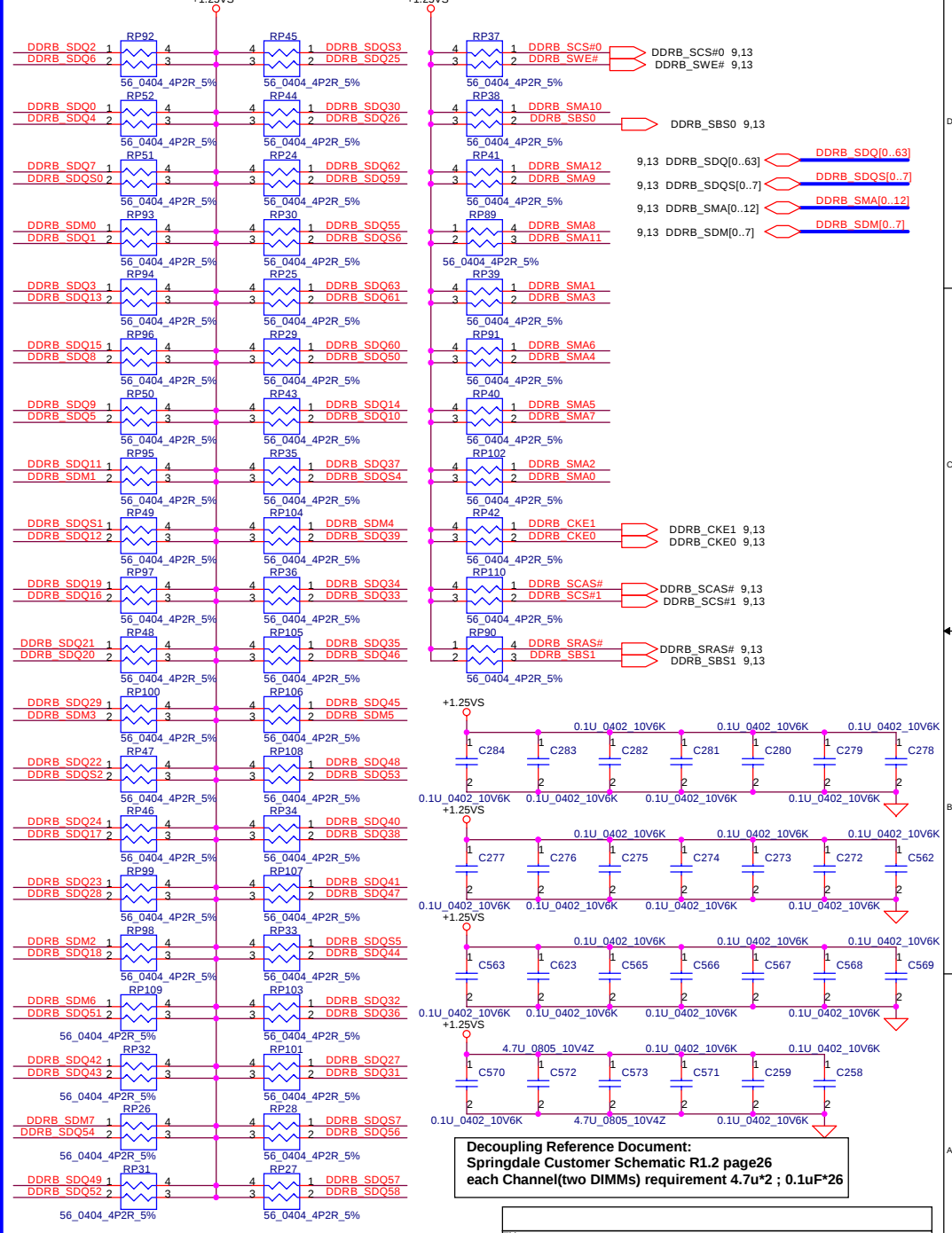
Channel A(DIMM0) Termination resistors & Decoupling caps



Decoupling Reference Document:
Springdale Customer Schematic R1.2 page22
each Channel(two DIMMs) requirement $4.7\mu^*2$; $0.1\mu F^*28$

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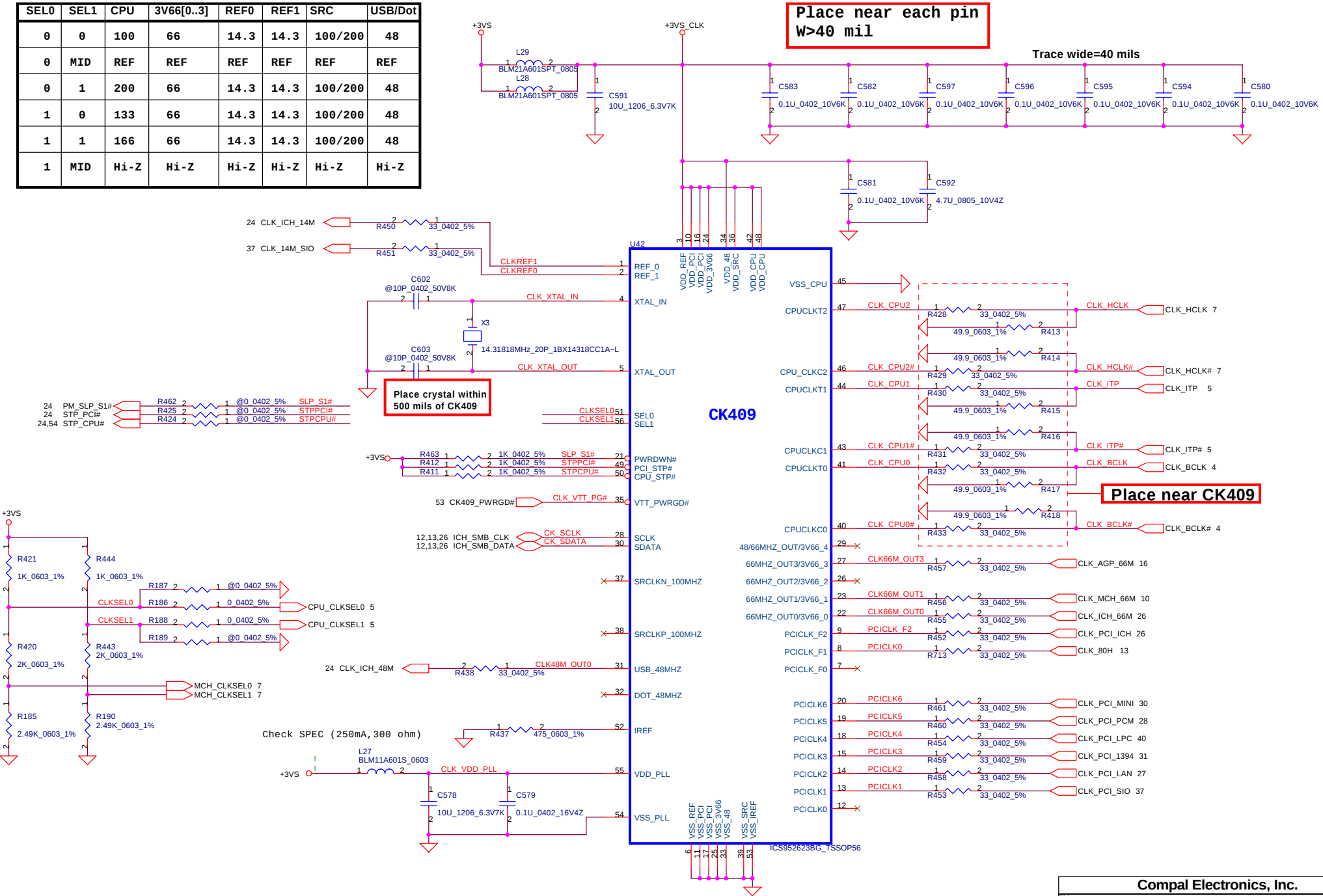
Channel B(DIMM1) Termination resistors & Decoupling caps



Decoupling Reference Document:
Springdale Customer Schematic R1.2 page26
each Channel(two DIMMs) requirement $4.7\mu^2$; $0.1\mu F^*26$

Title			
DDR Termination Resistors			
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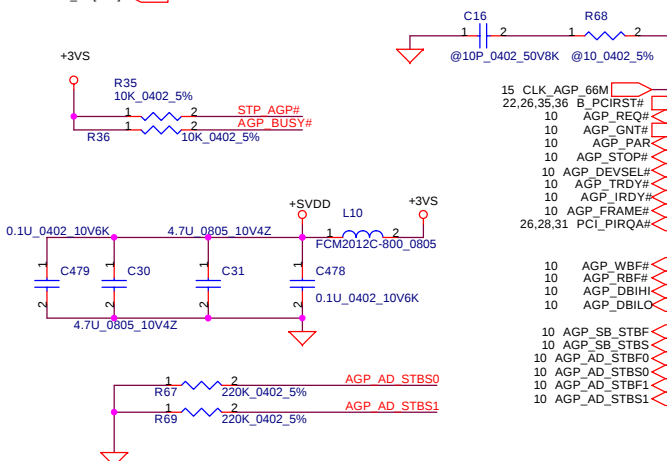
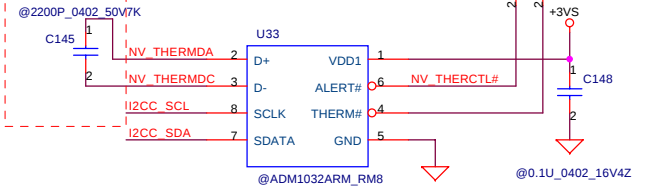
SEL0	SEL1	CPU	3V66[0..3]	REF0	REF1	SRC	USB/Dot
0	0	100	66	14.3	14.3	100/200	48
0	MID	REF	REF	REF	REF	REF	REF
0	1	200	66	14.3	14.3	100/200	48
1	0	133	66	14.3	14.3	100/200	48
1	1	166	66	14.3	14.3	100/200	48
1	MID	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z



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Clock Generator			
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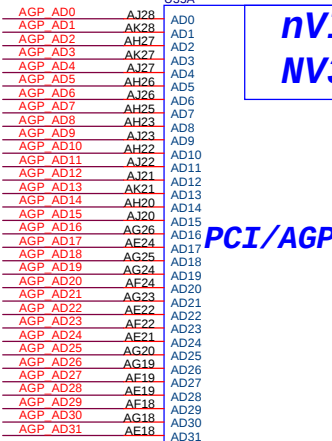
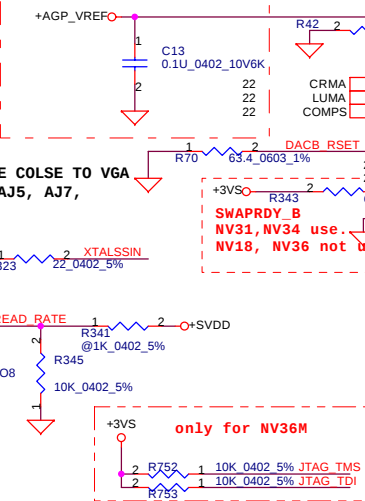
Place close
to pin
H2 & H3



Selection Table For W180

Modulation Setting	SST Ratio
SS%	
0	1.25%
1	3.75%

Close V6A ball (AK29)
less than 250mils



PCI/AGP

AGP4X/8X

nVIDIA
NV36M

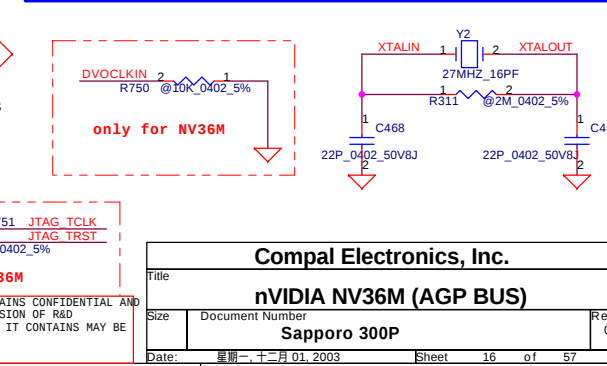
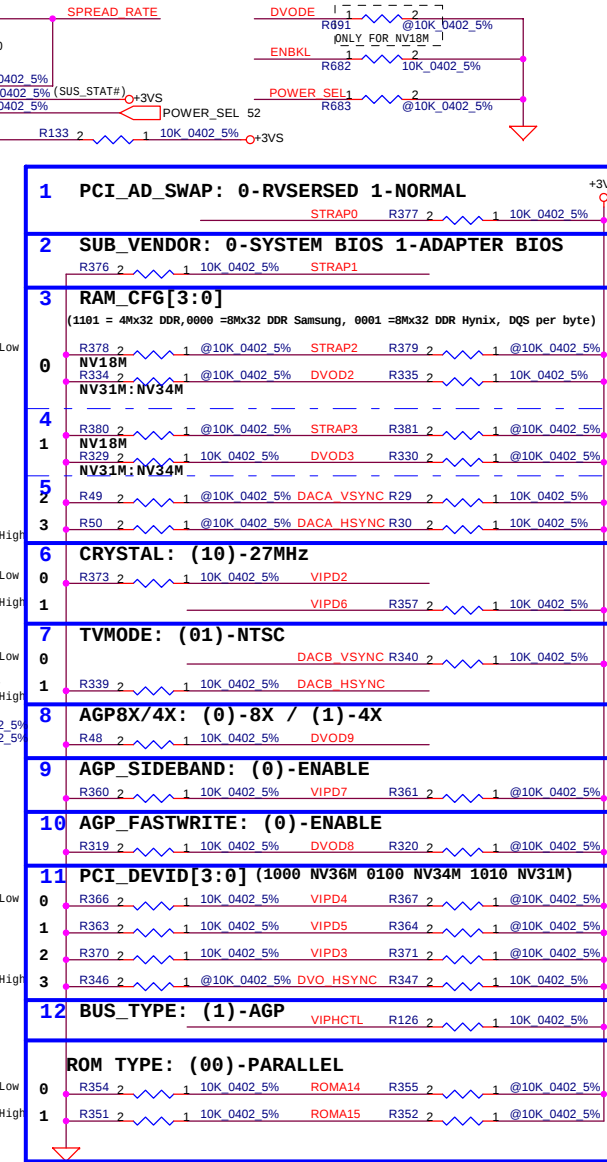
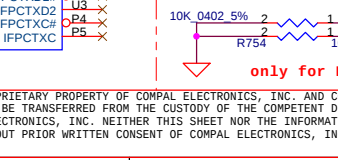
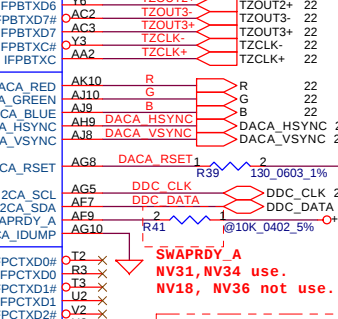
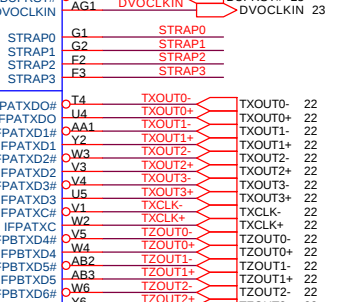
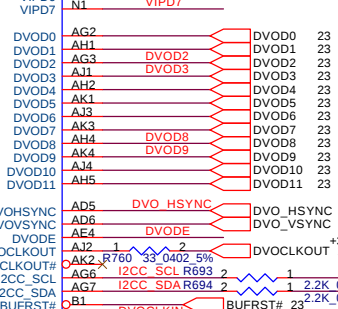
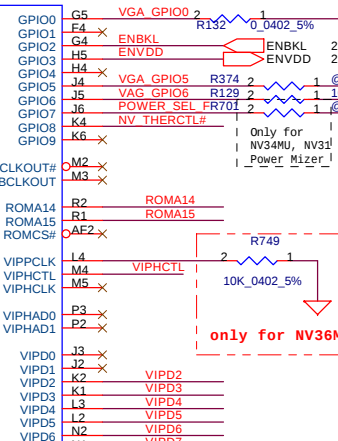
ZV PORT / EXT TMD5 / GPIO / ROM

LVDS

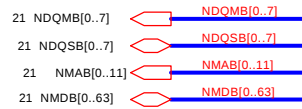
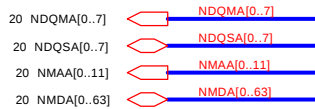
DAC1

DAC2

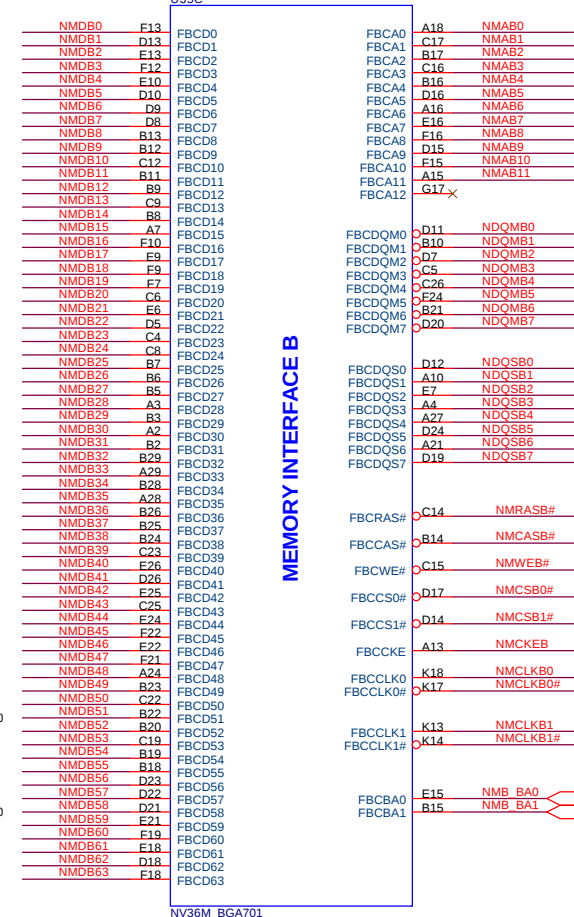
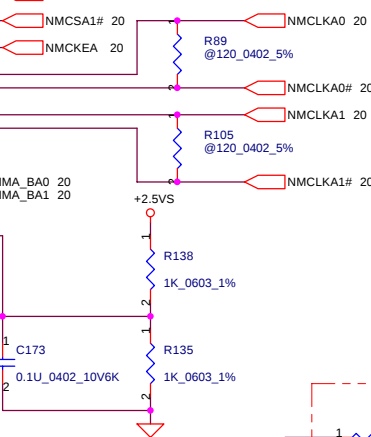
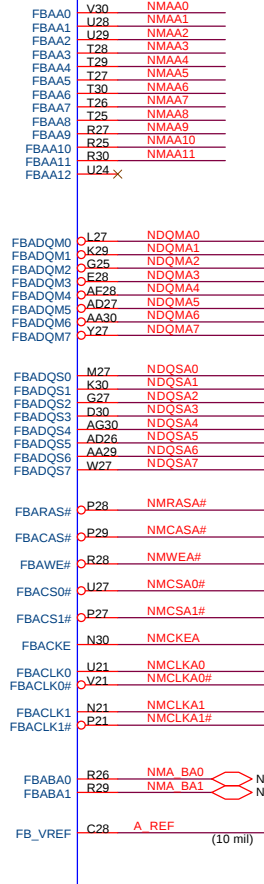
SSC



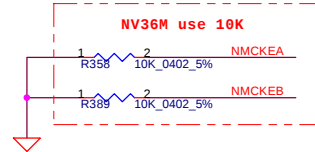
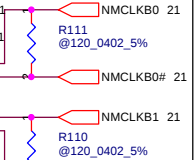
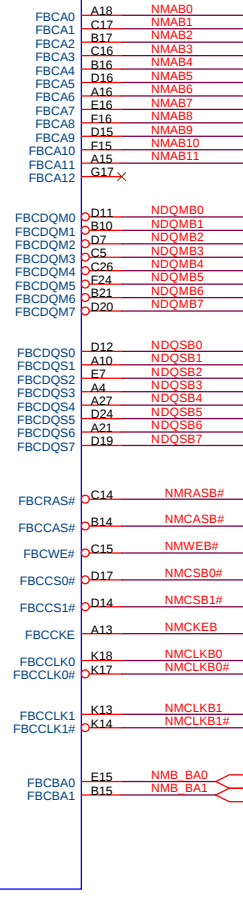
PROPRIETARY NOTE THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



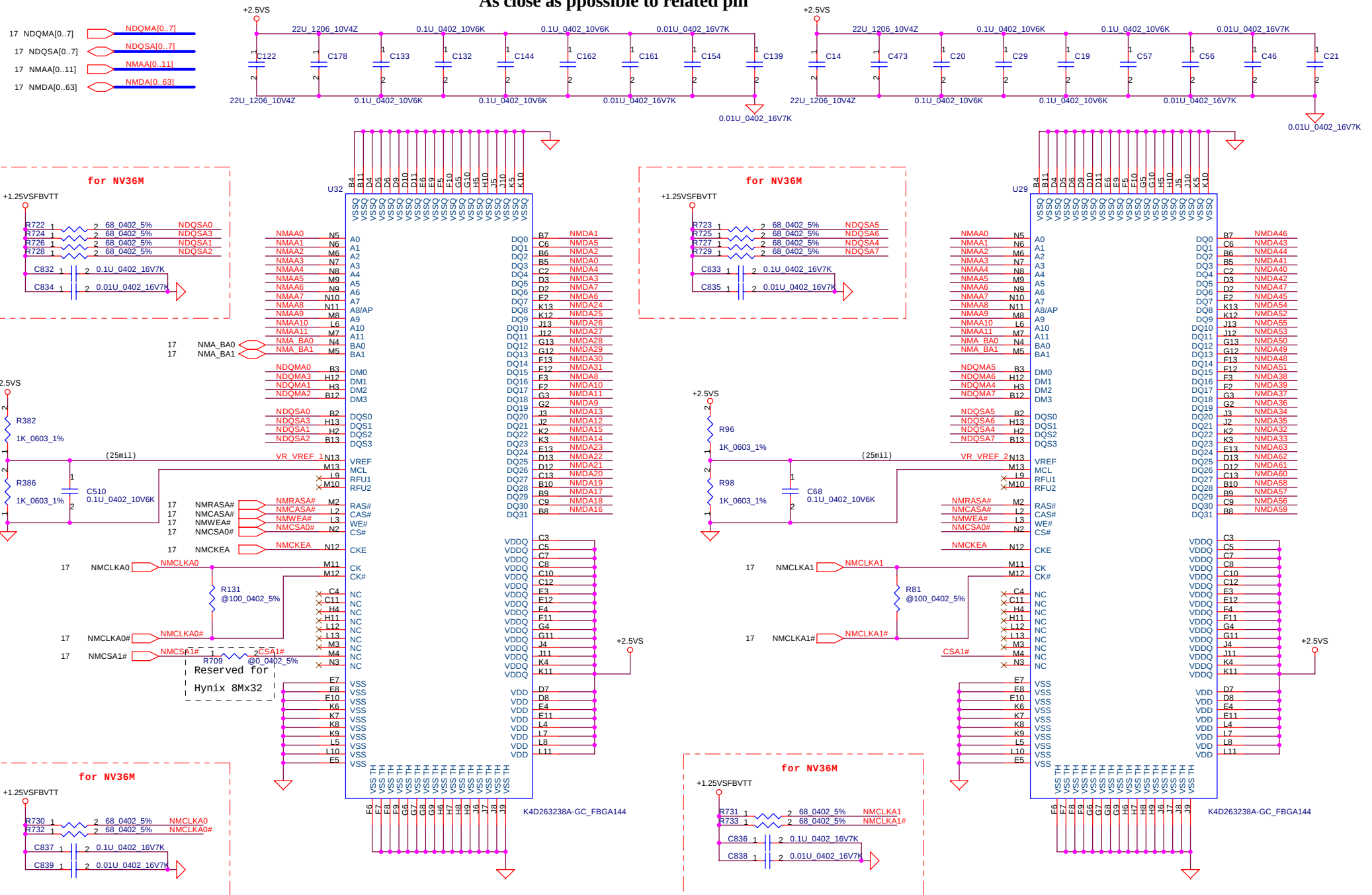
MEMORY INTERFACE A



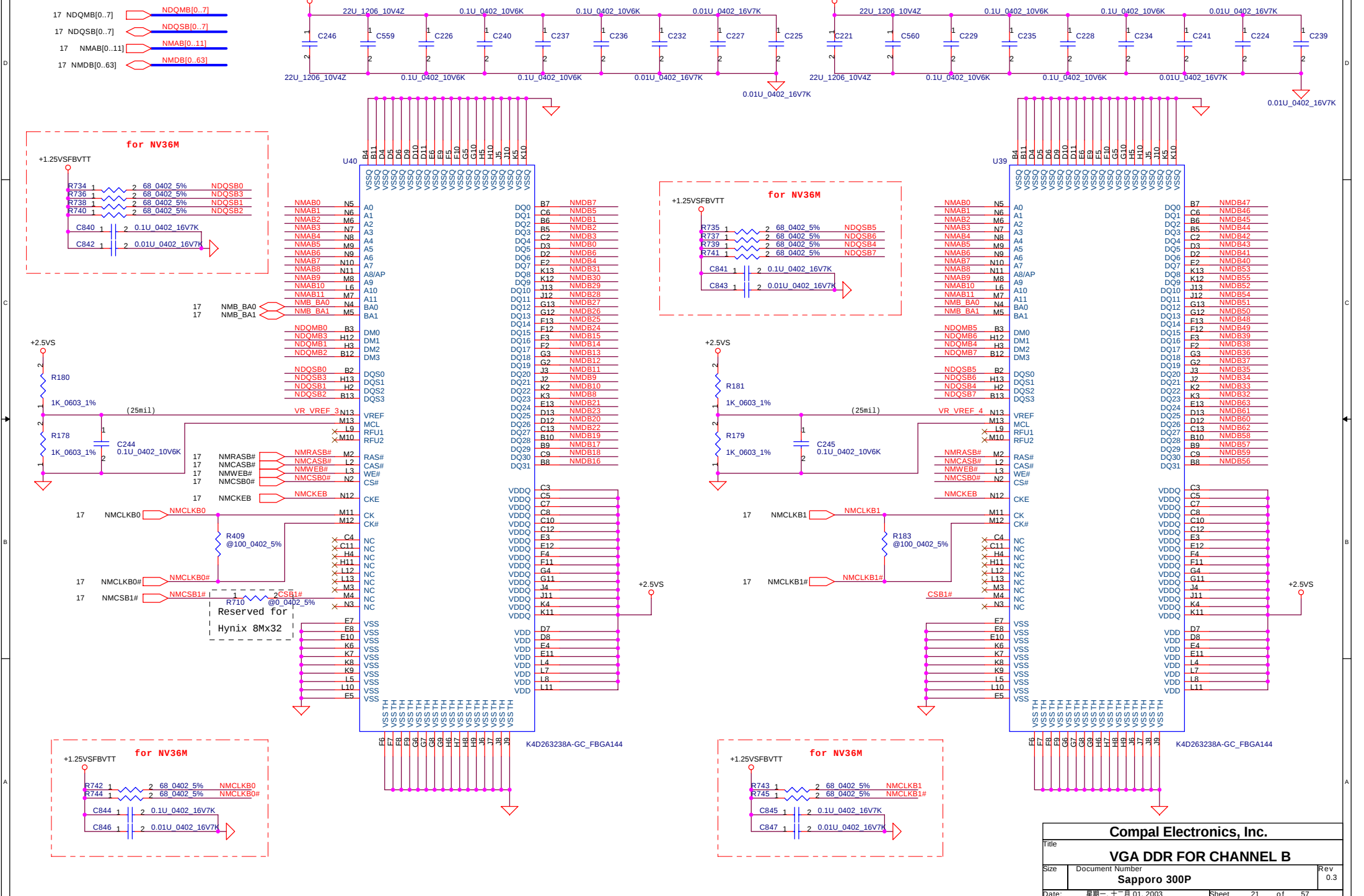
MEMORY INTERFACE B



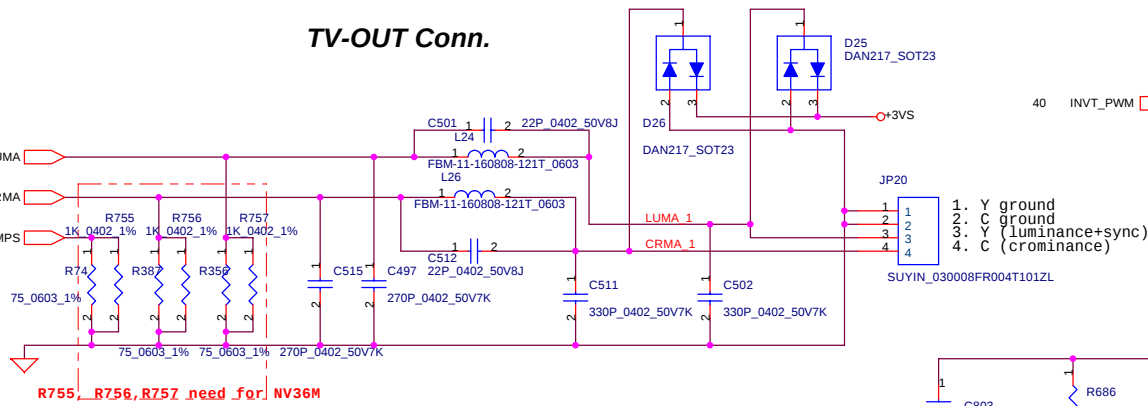
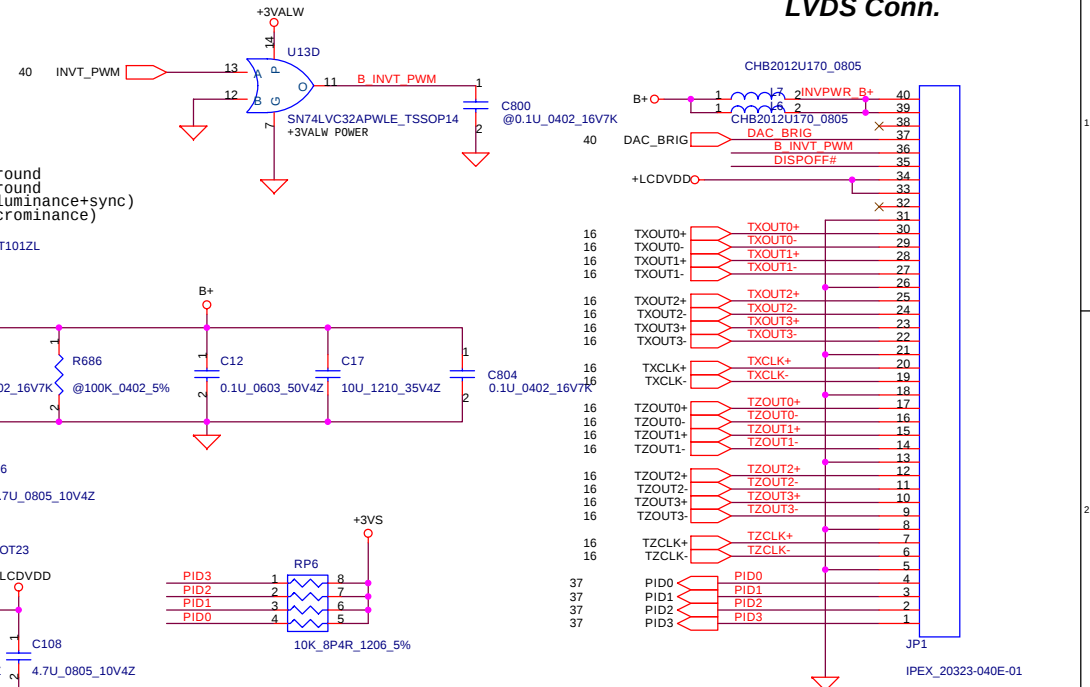
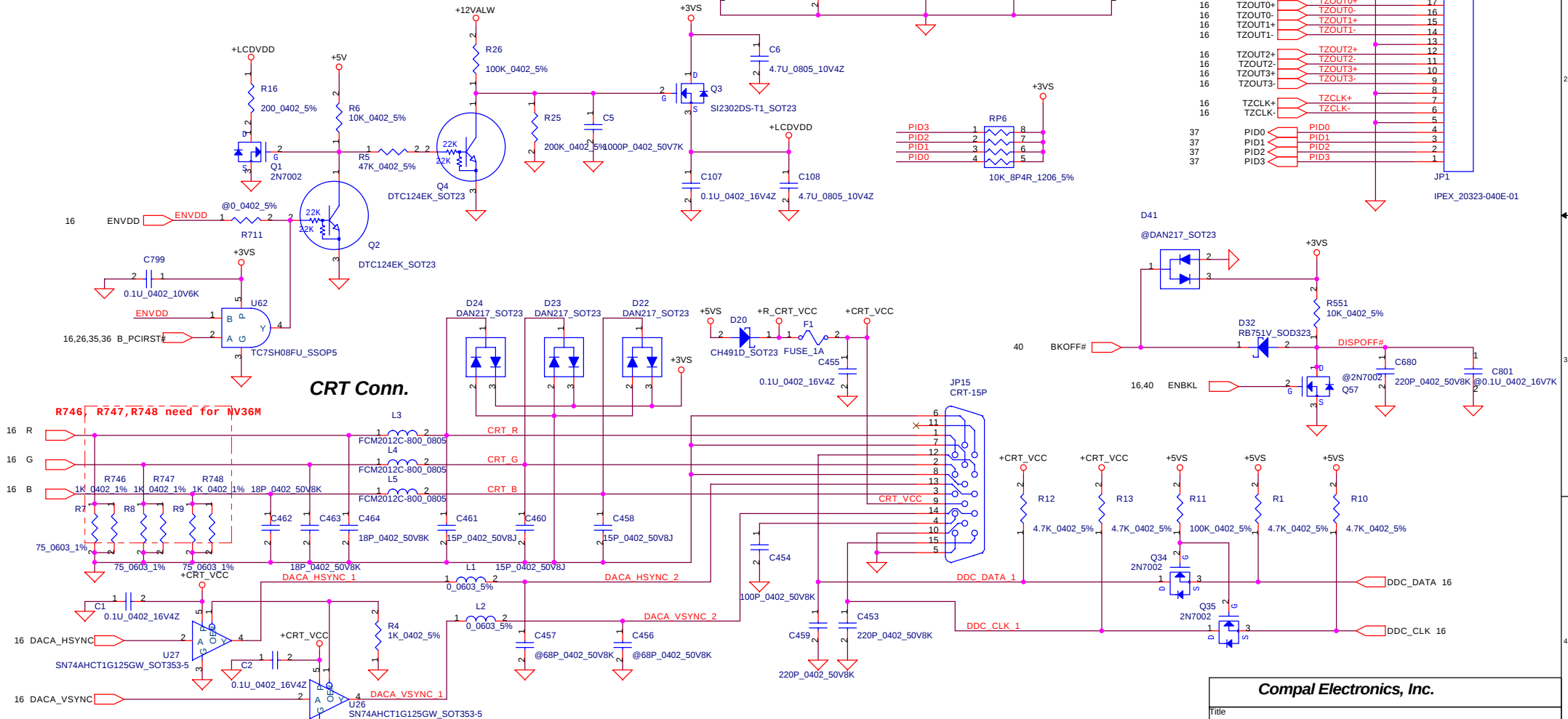
As close as possible to related pin



As close as ppossible to related pin



CRT, TV-OUT & LVDS CONNECTOR

TV-OUT Conn.**LVDS Conn.****CRT Conn.**

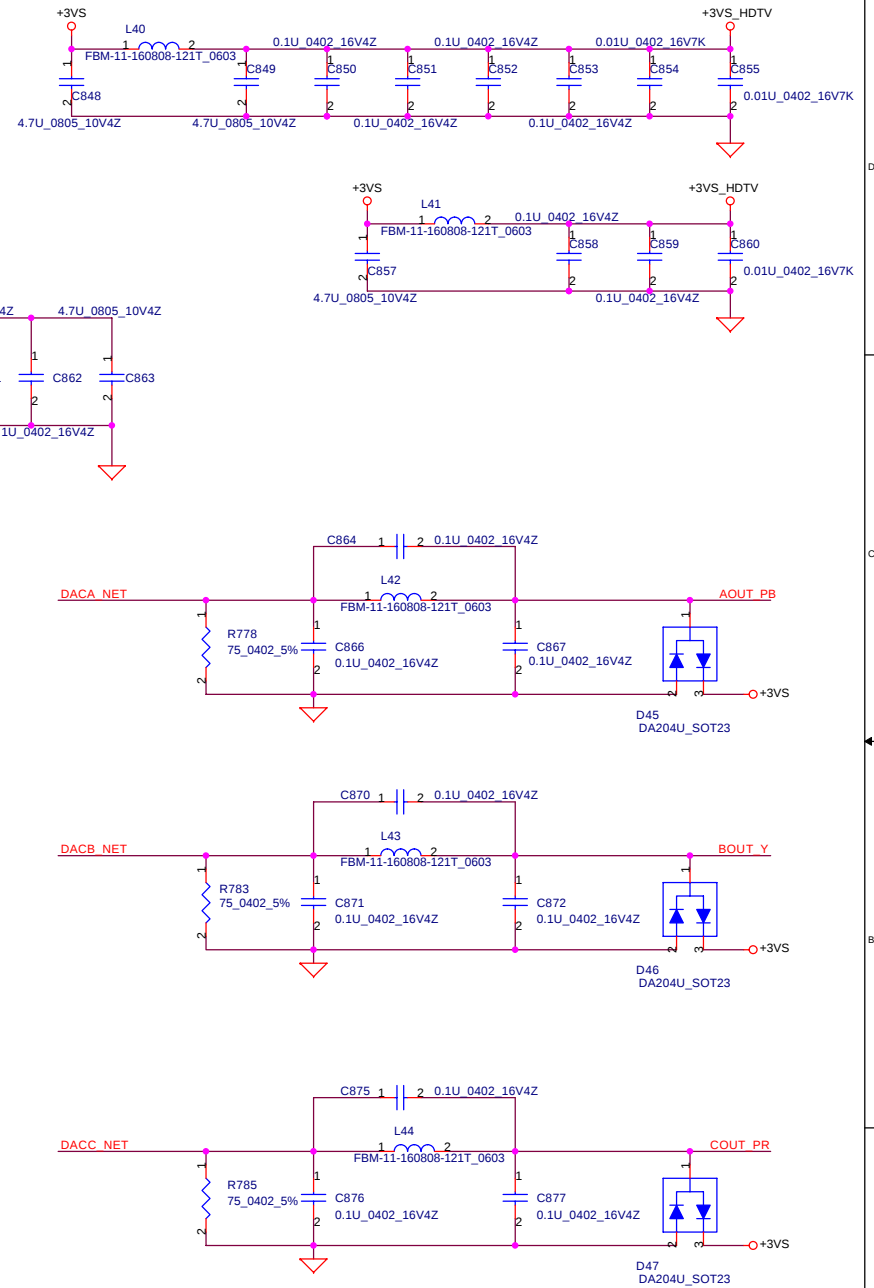
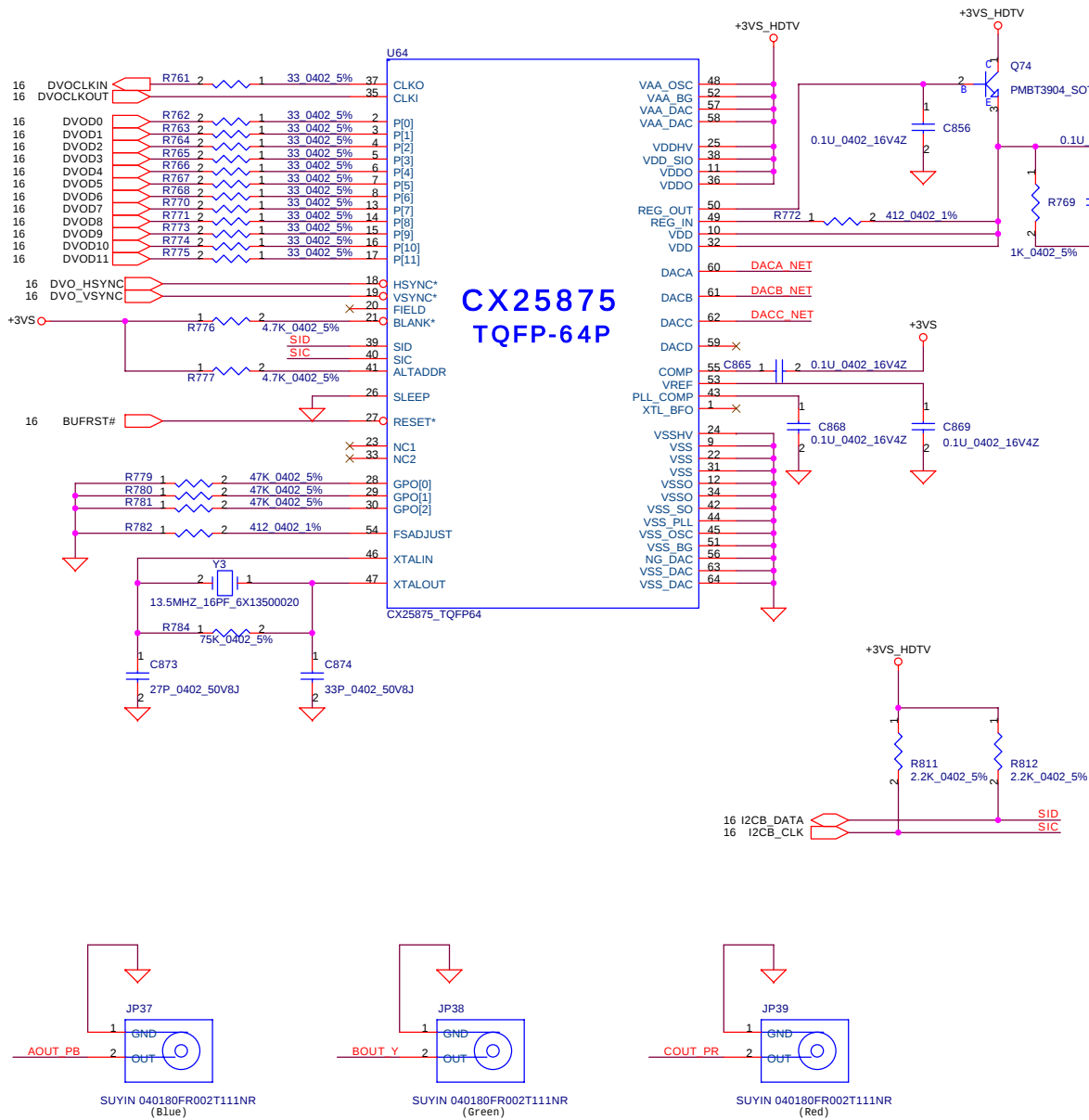
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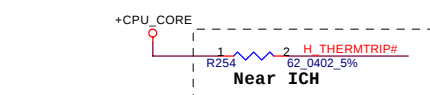
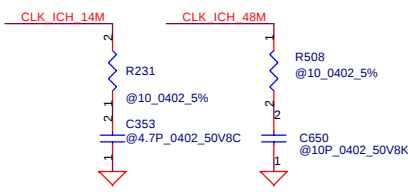
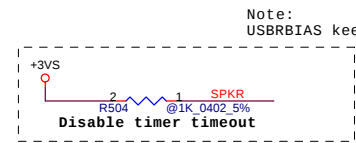
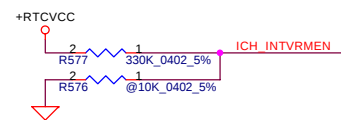
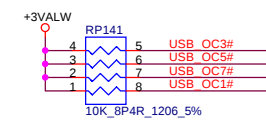
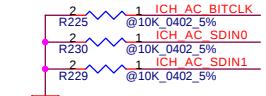
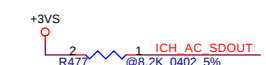
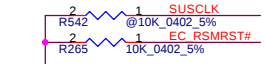
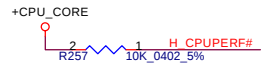
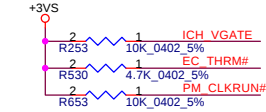
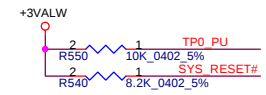
Compal Electronics, Inc.

CRT,TV-OUT & LVDS Connector

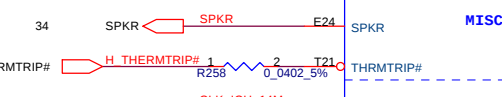
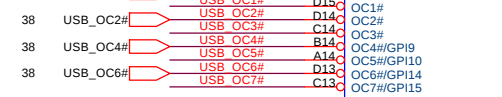
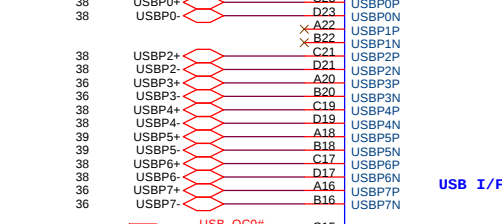
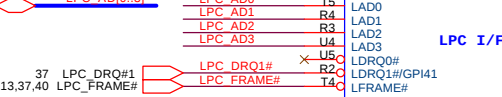
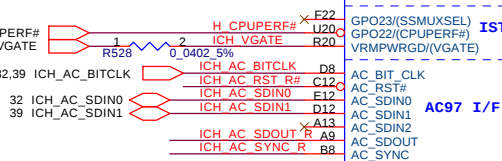
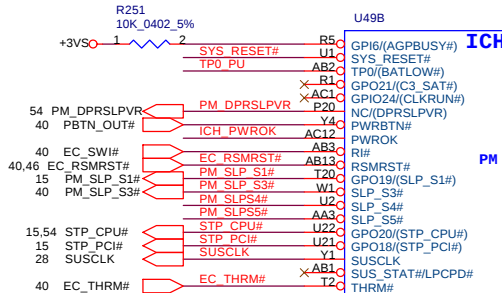
Size B	Document Number Sapporo 300P	Rev 0.3
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27,28,30,31,37,40 PM_CLKRUN#



ICH5/(ICH5-M)

GPI

PM

IST

AC97 I/F

LPC I/F

USB I/F

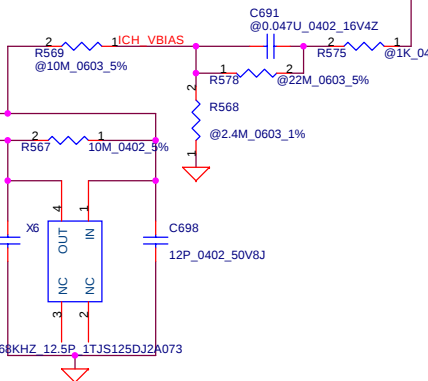
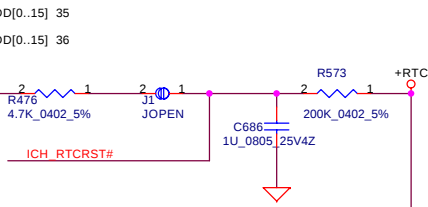
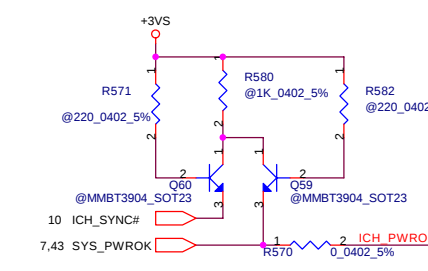
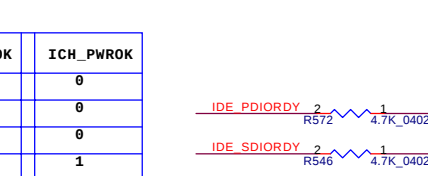
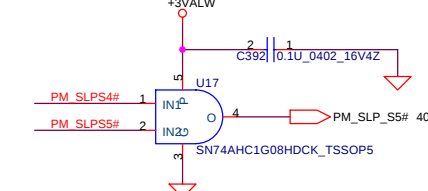
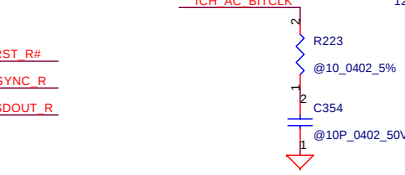
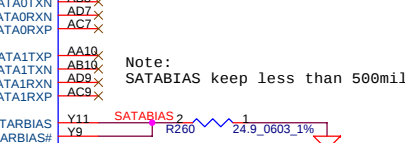
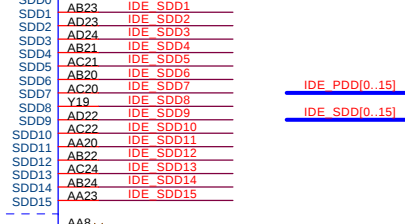
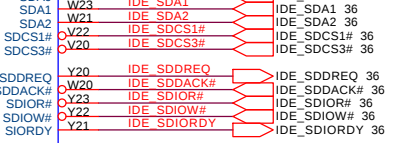
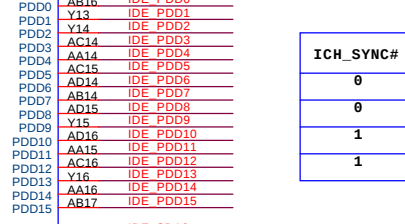
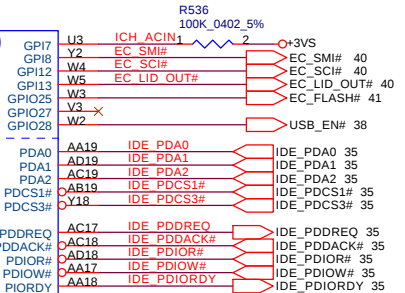
IDE I/F

SATA I/F

GPIO

MISC

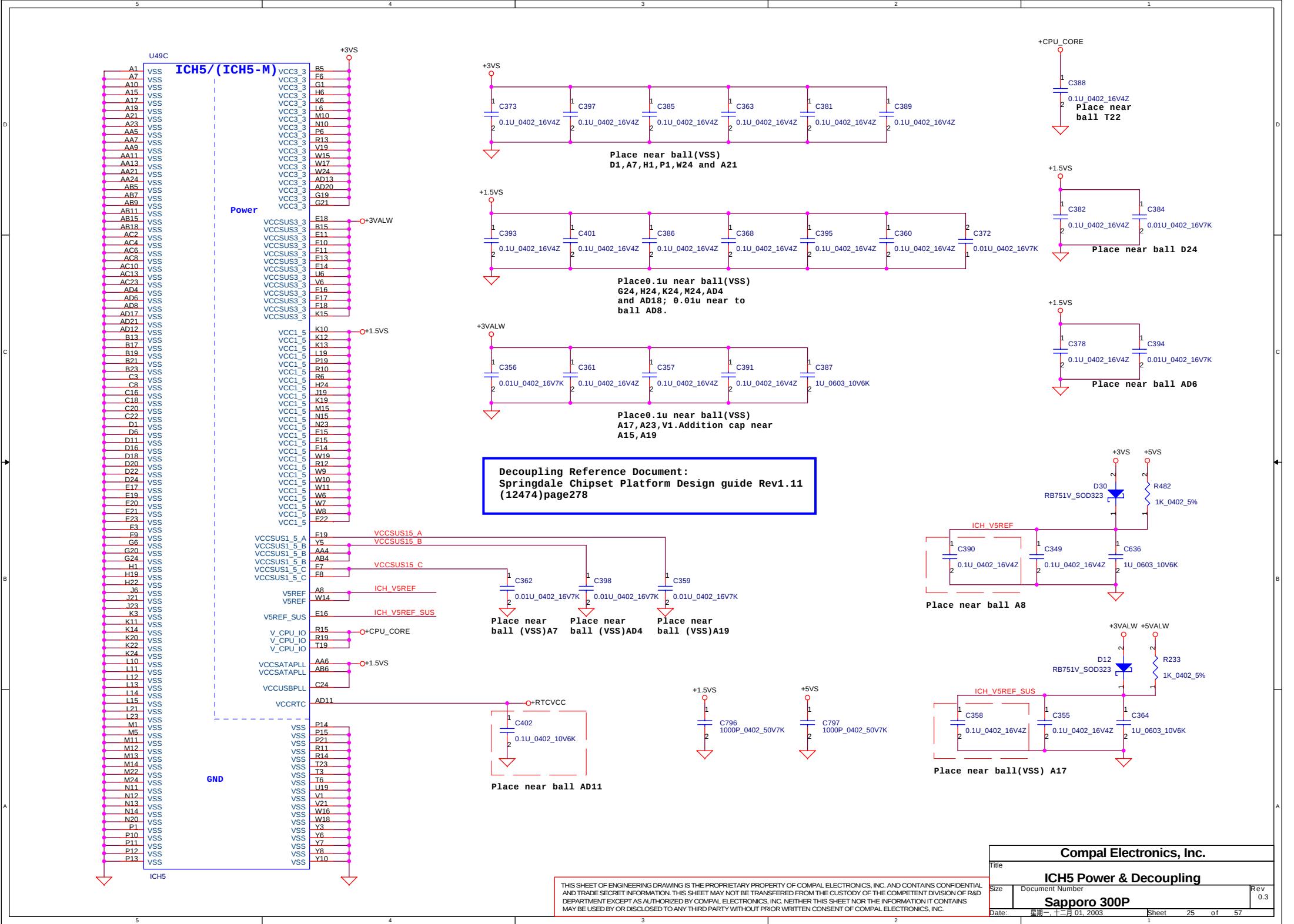
CLOCK

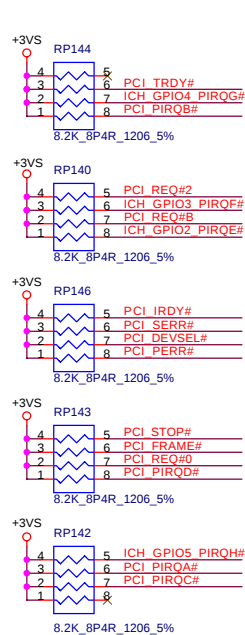


ICH_SYNC#	SYS_PWROK	ICH_PWROK
0	0	0
0	1	0
1	0	0
1	1	1

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Compal Electronics, Inc.		
Title ICH5-IDE/LPC/PM/GPIO/USB		
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27,28,30,31 PCI_AD[0..31]

10 HUB_HL[0..10]

ICH5/(ICH5-M)

PCI AD0

PCI AD1

PCI AD2

PCI AD3

PCI AD4

PCI AD5

PCI AD6

PCI AD7

PCI AD8

PCI AD9

PCI AD10

PCI AD11

PCI AD12

PCI AD13

PCI AD14

PCI AD15

PCI AD16

PCI AD17

PCI AD18

PCI AD19

PCI AD20

PCI AD21

PCI AD22

PCI AD23

PCI AD24

PCI AD25

PCI AD26

PCI AD27

PCI AD28

PCI AD29

PCI AD30

PCI AD31

PCI I/F

27,28,30,31 PCI_C/BE#0

27,28,30,31 PCI_C/BE#1

27,28,30,31 PCI_C/BE#2

27,28,30,31 PCI_C/BE#3

31 PCI_REQ#0

30 PCI_REQ#1

28 PCI_REQ#2

27 PCI_REQ#3

31 PCI_GNT#0

30 PCI_GNT#1

28 PCI_GNT#2

27 PCI_GNT#3

15 CLK_PCI_ICH

27,28,30,31 PCI_FRAME#

27,28,30,31 PCI_DEVSEL#

27,28,30,31 PCI_IRDY#

27,28,30,31 PCI_PAR#

27,28,30,31 PCI_PERR#

10,13,27,28,30,31,37,40 PCIRST#

27,28,30,31 PCI_SERR#

27,28,30,31 PCI_STOP#

27,28,30,31 PCI_TRDY#

35 PIDERST#

ICH5/(ICH5-M)

SMB I/F

CPU I/F

HUB I/F

Interrupt I/F

EEPROM I/F

LAN I/F

INTRUDER#

SMLINK0

SMLINK1

LINKALERT#

SMBCLK

SMBDATA

SMBALERT#/GPIO11

A20GATE

A20M#

NC

FERR#

IGNNE#

INIT#

INTR

NMI

CPUPWRGD/GPO49

RCIN#

CPUSLP#

SMI#

STPCLK#

NC(DPSLP#)

H20

H21

H22

H23

M23

M24

M25

M26

M27

M28

M29

K21

K22

K23

J24

N24

L24

L20

HI_RCOMP_ICH

HI_VREF_ICH

HI_SWING_ICH

PIRQA#

PIRQB#

PIRQC#

PIRQD#

ICH_GPIO2_PIRQ#

ICH_GPIO3_PIRQ#

ICH_GPIO4_PIRQ#

ICH_GPIO5_PIRQ#

IDE_IRQ14

IDE_IRQ15

IRQ_SERIRQ

EE_CS

EE_DIN

EE_DOUT

EE_SHCLK

LAN_RXD0

LAN_RXD1

LAN_RXD2

LAN_TXD0

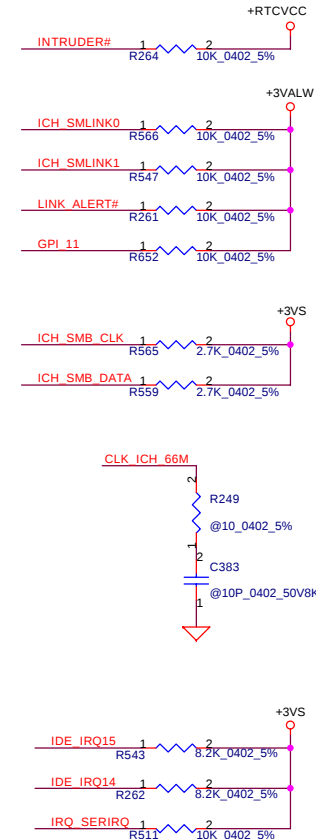
LAN_TXD1

LAN_TXD2

LAN_CLK

LAN_RSTSYNC

LAN_RST#

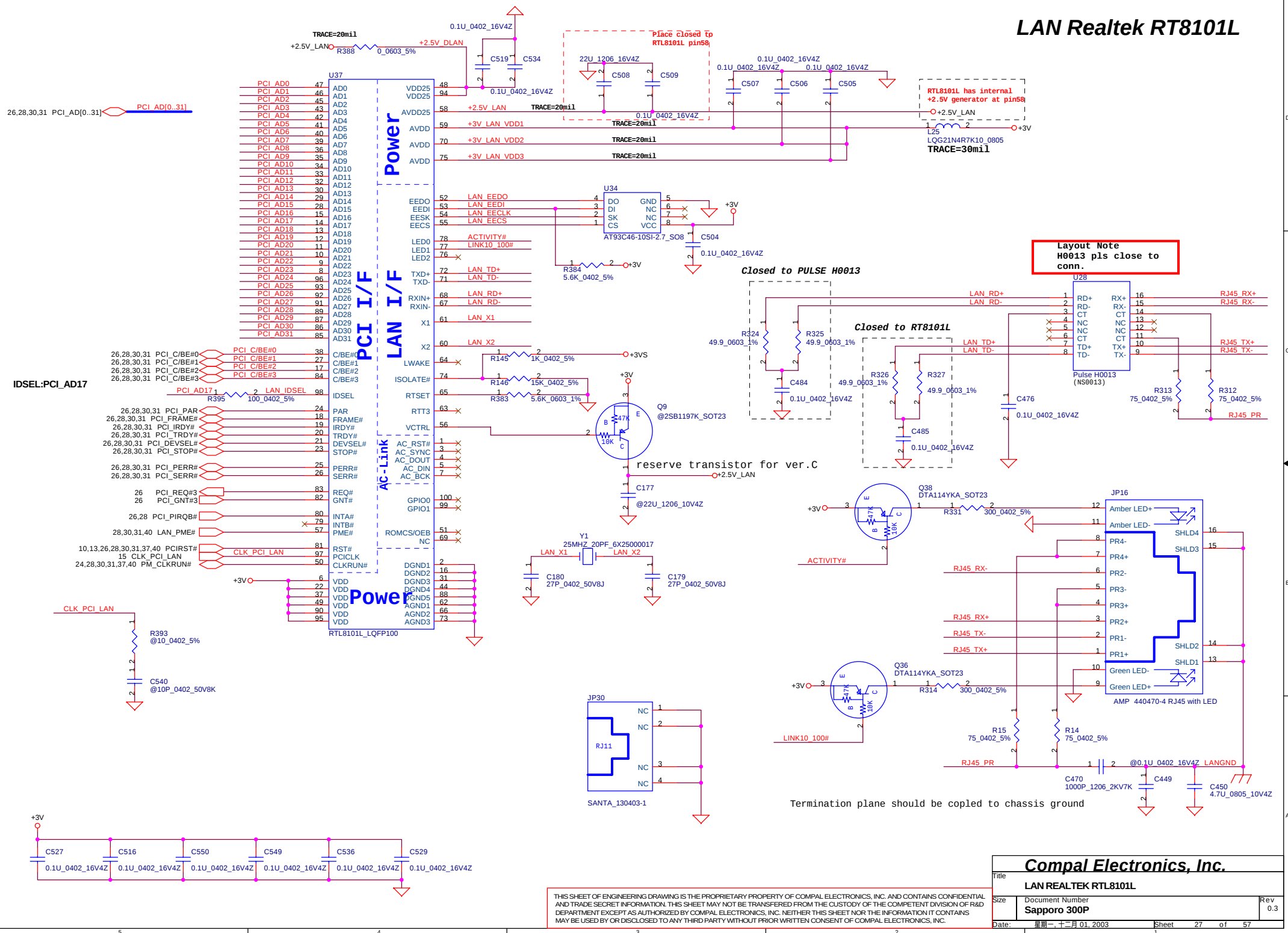


Note:
HI_SWING_MCH, HI_VREF_MCH
trace width of 10mils and
space 7mils

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Title ICH5-PCI/HUB/LAN		
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LAN Realtek RT8101L



Compal Electronics, Inc.

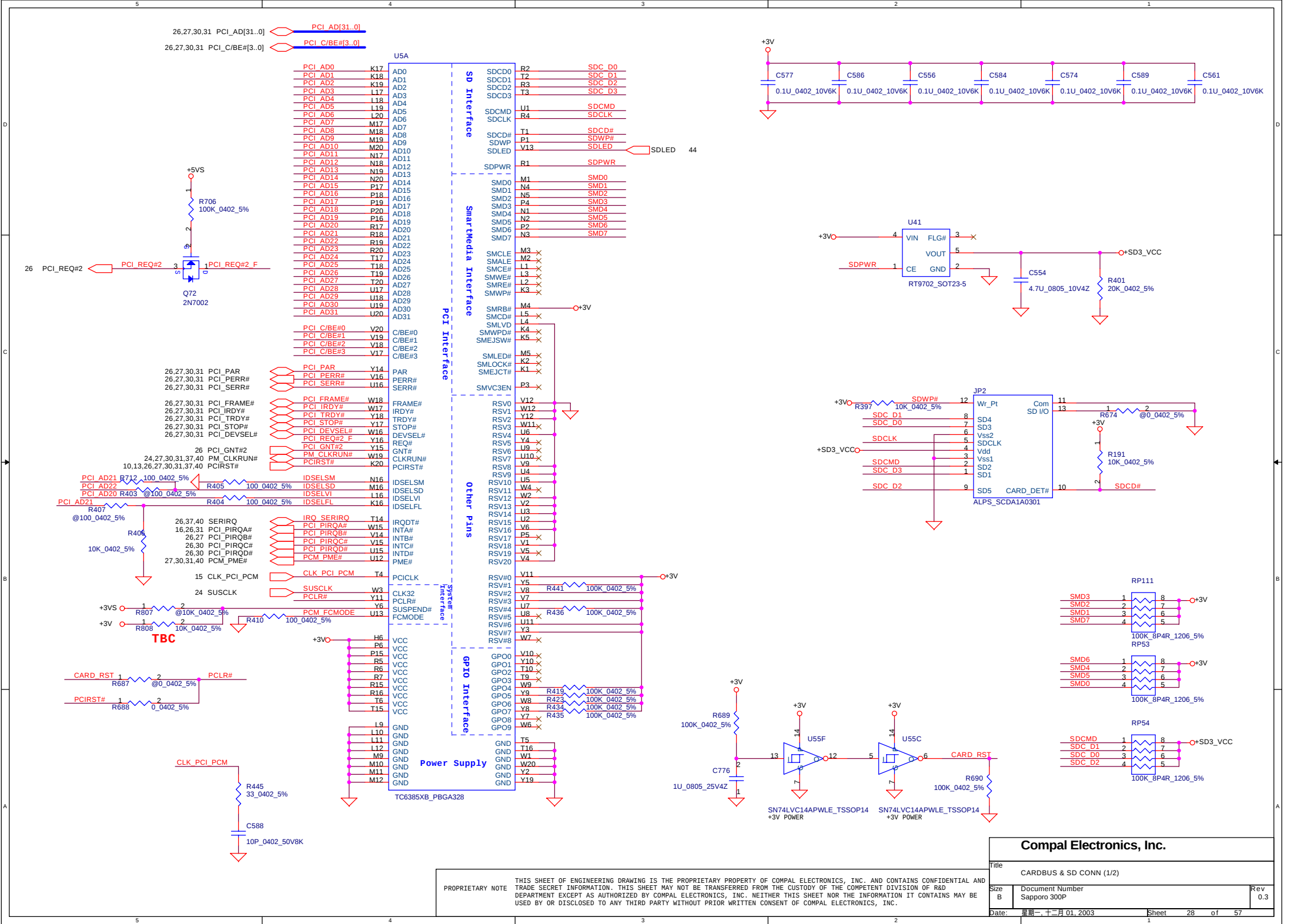
LAN REAI TEK RTI 8101I

Document Number
Sapporo 300F

星期一 十二月 01, 2003

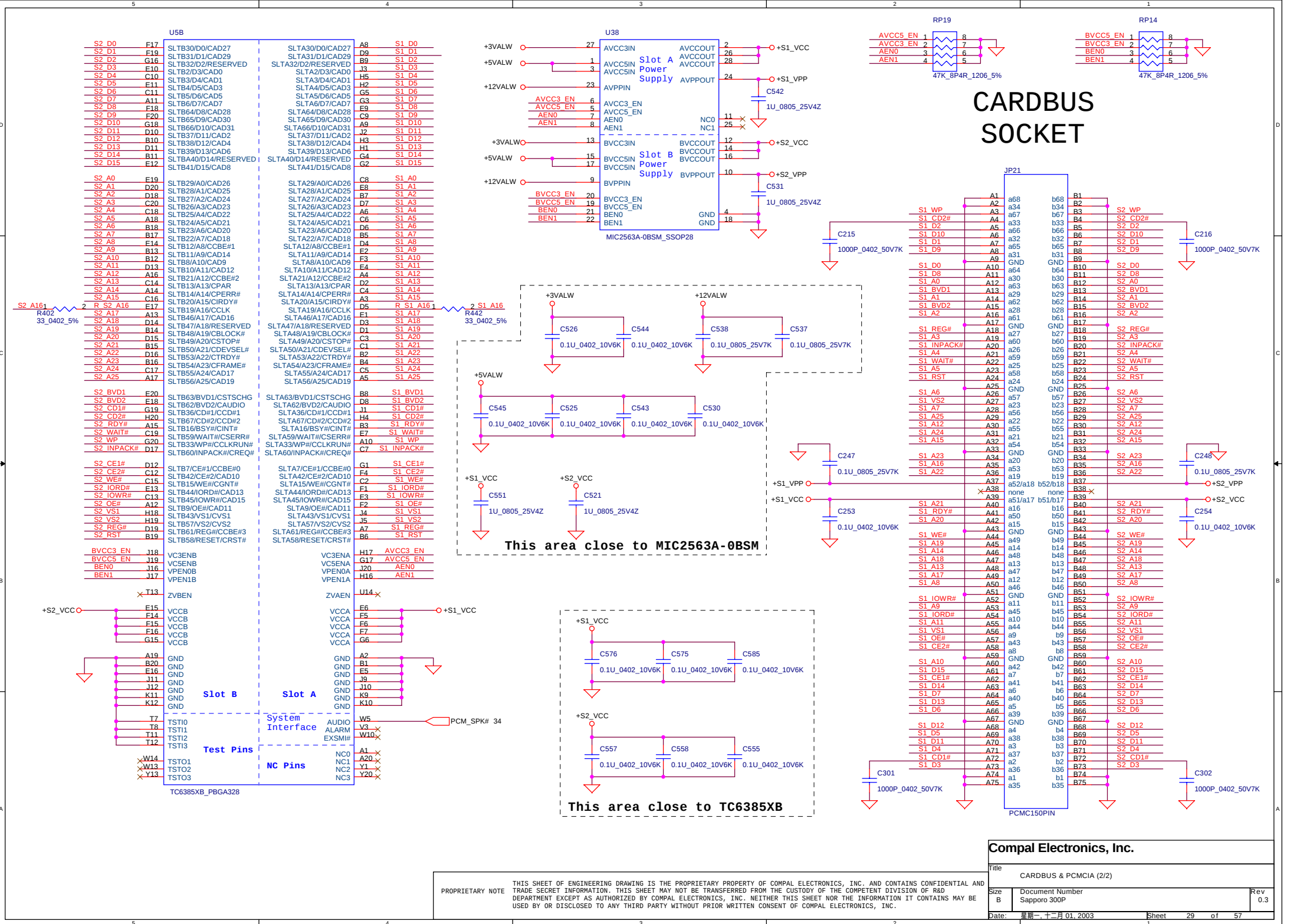
Sheet 27 of 57

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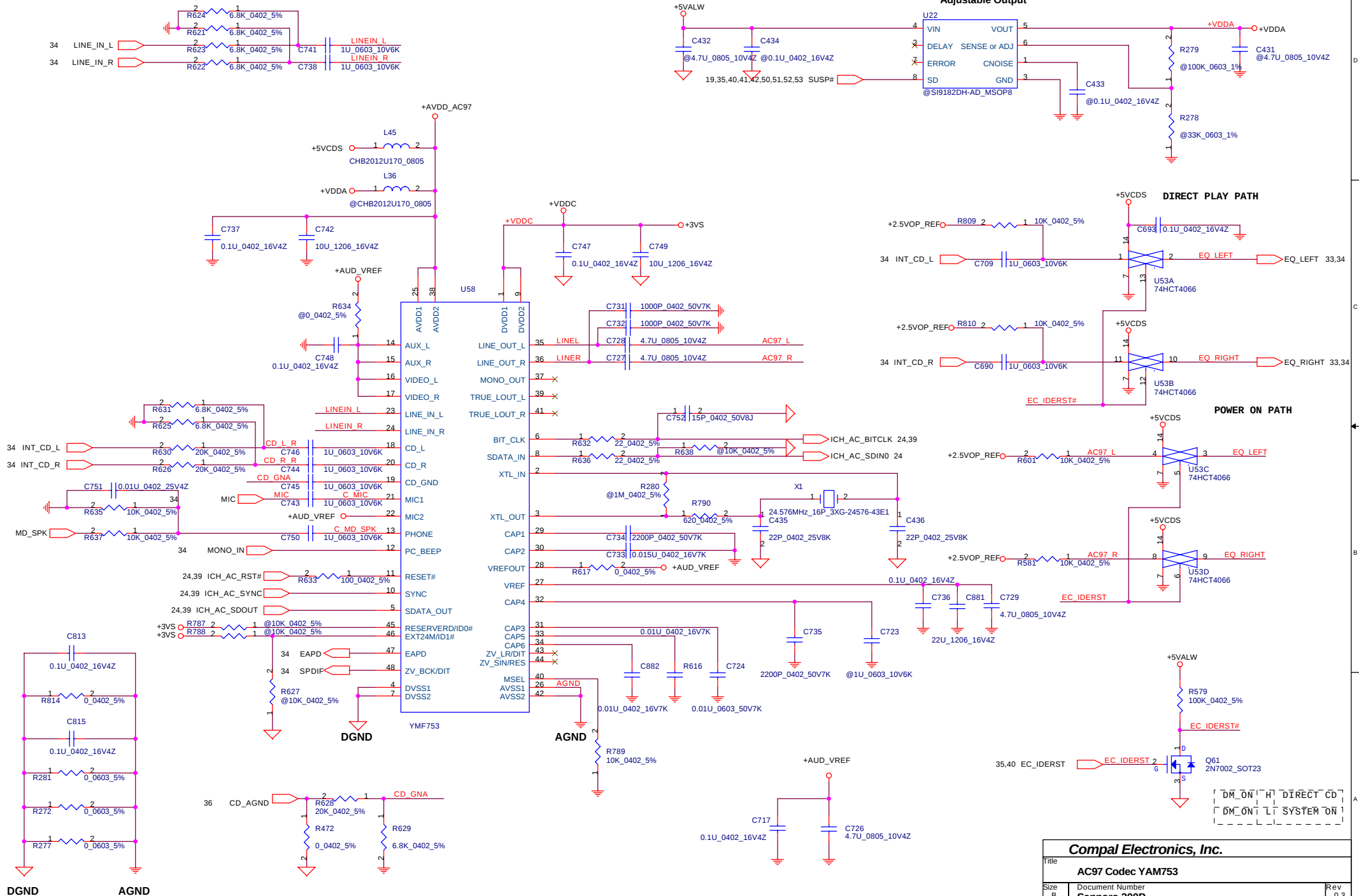
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Compal Electronics, Inc.			
Title			
CARDBUS & SD CONN (1/2)			
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AC97 Codec

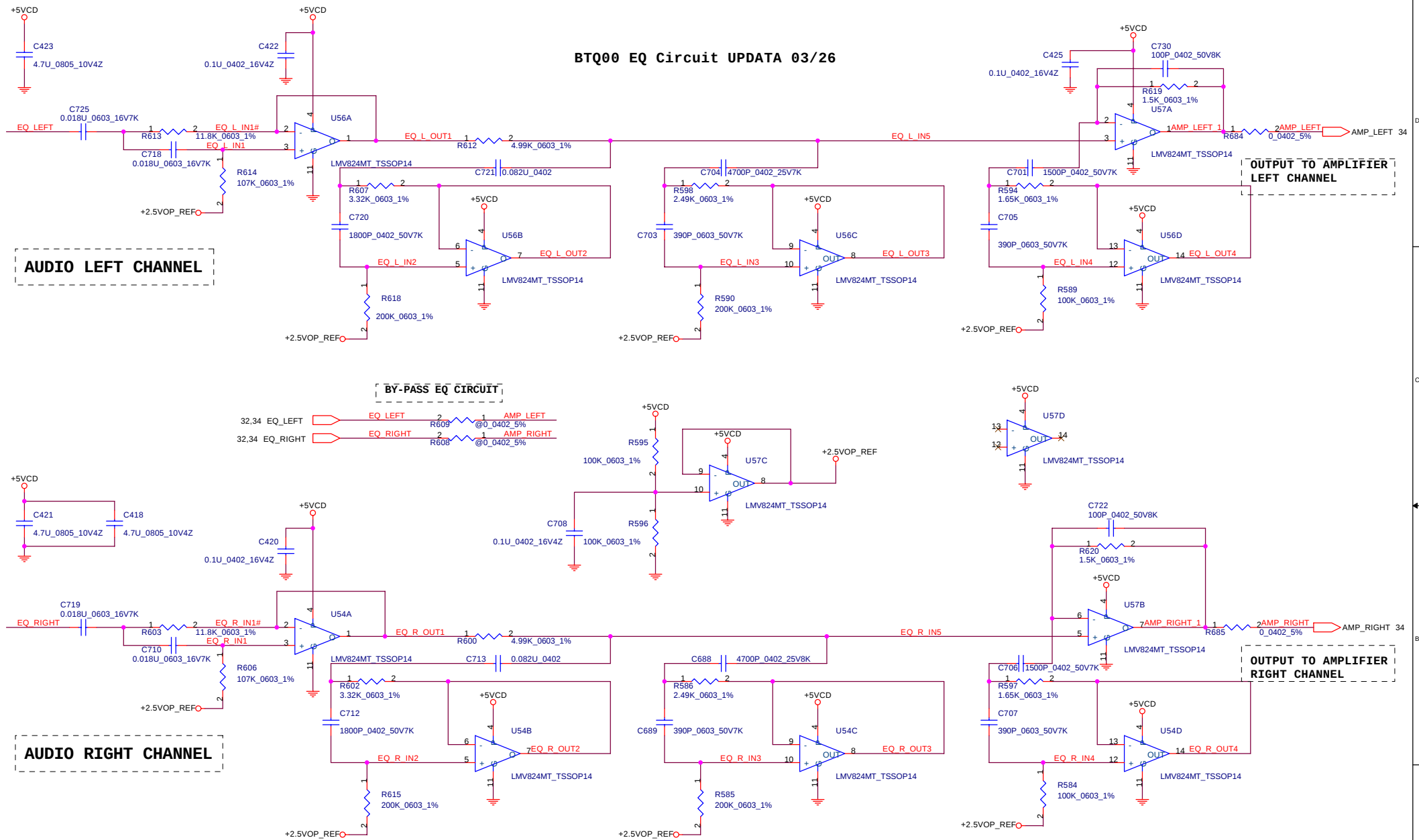
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Title			
AC97 Codec YAM753			
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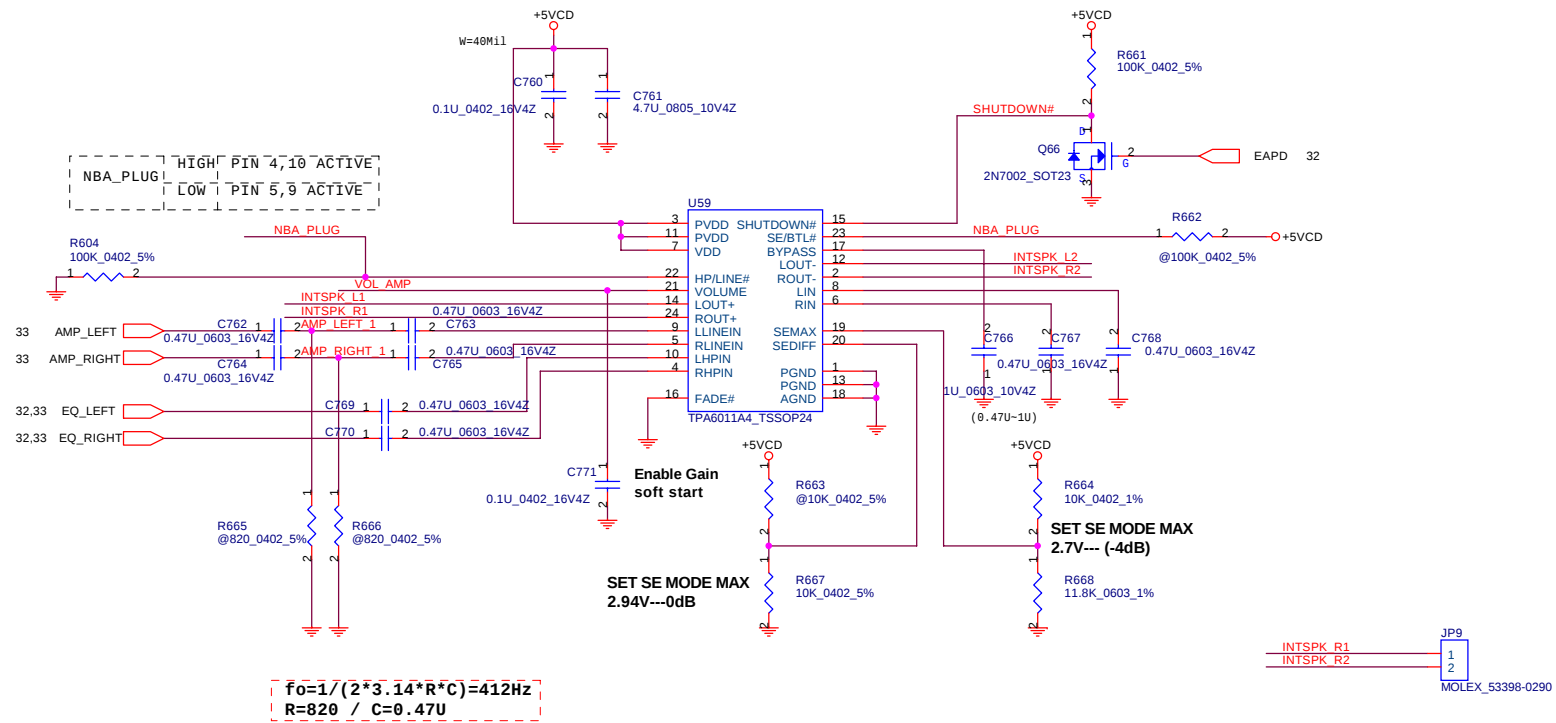
BTQ00 EQ Circuit UPDATA 03/26



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Compal Electronics, Inc.			
Title	HAREWARE EQ		
Size B	Document Number	Rev 0.3	
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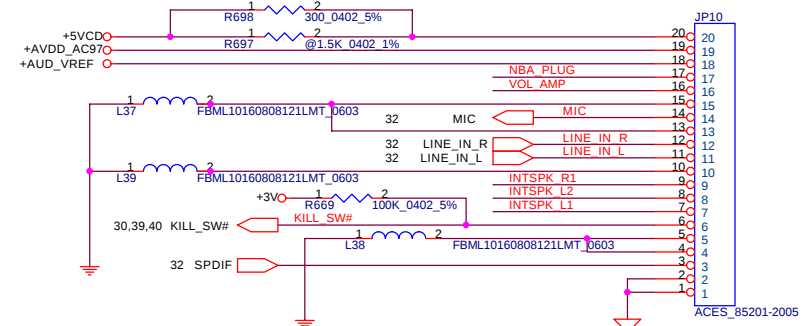
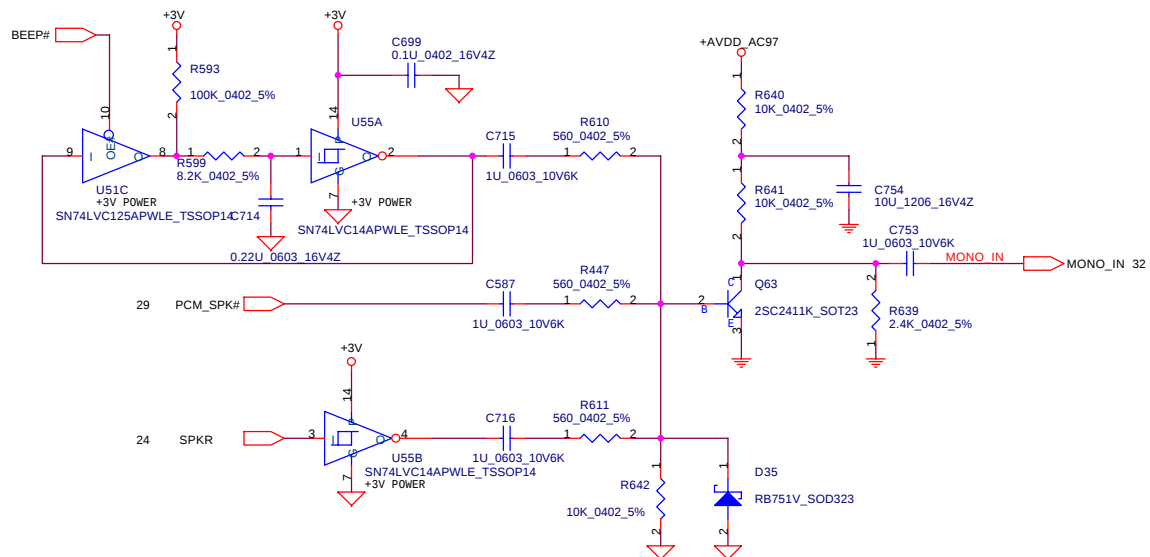
Audio AMP



AUDIO Board Conn.

R697(1.5K)-----10dB

R698(300)-----14dB



Compal Electronics, Inc.

Title

AMP & Audio Jack

Size

Document Number
Sapporo 300P

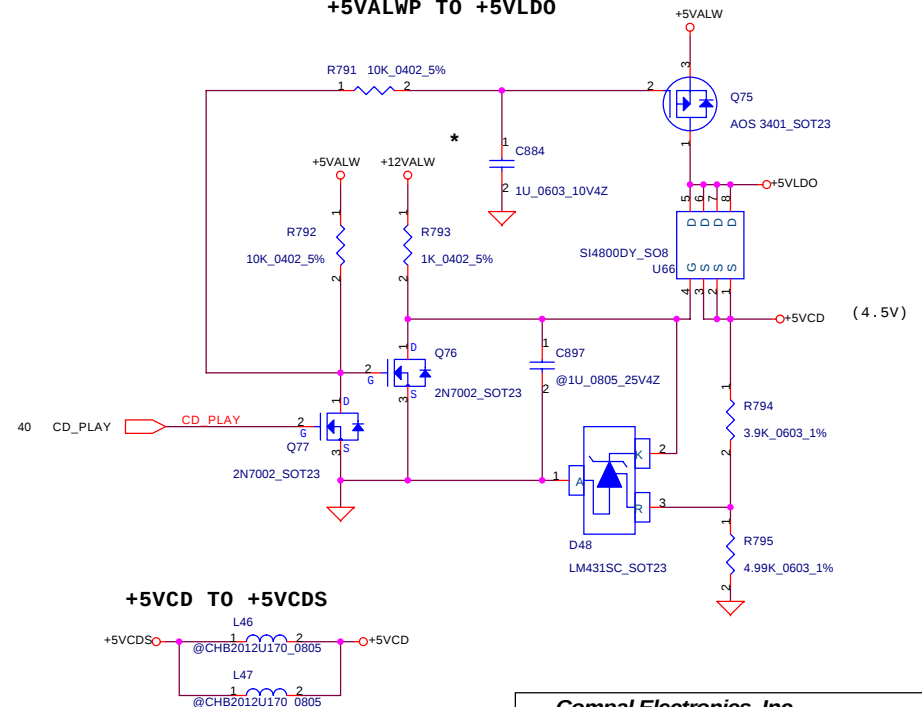
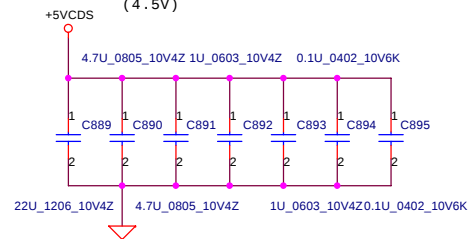
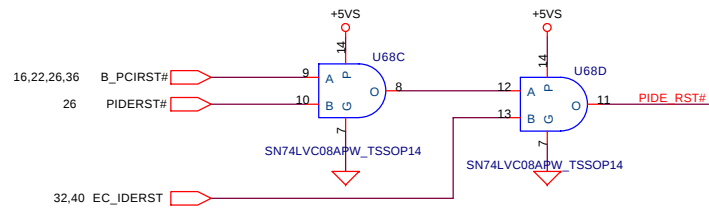
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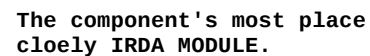
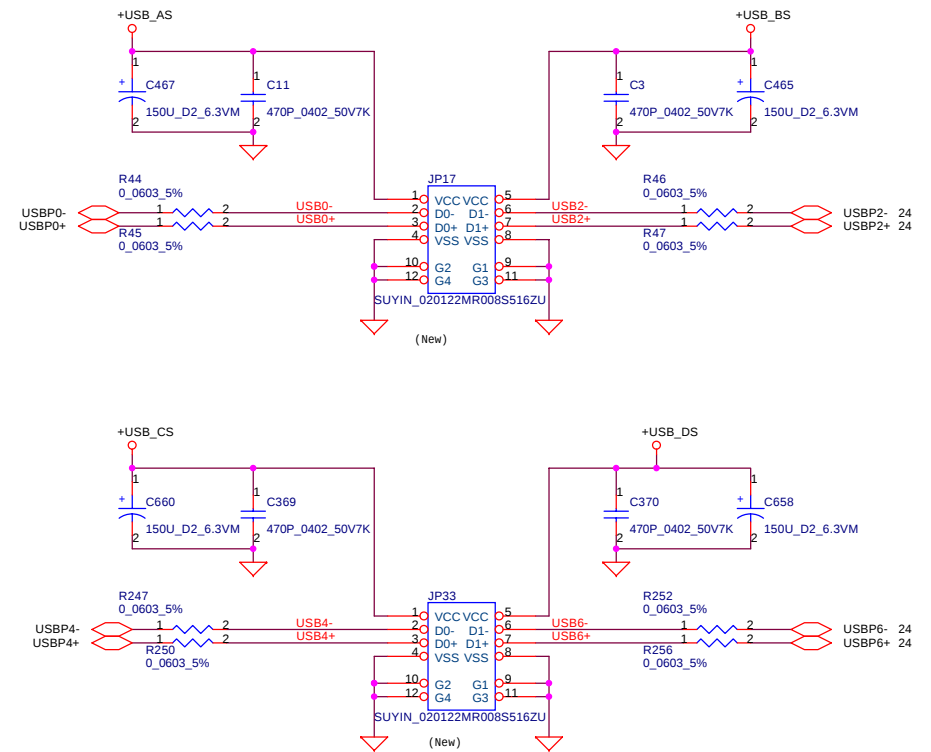
PROPRIETARY NOTE THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

24 IDE_PDD[0..15] IDE_PDD[0..15]



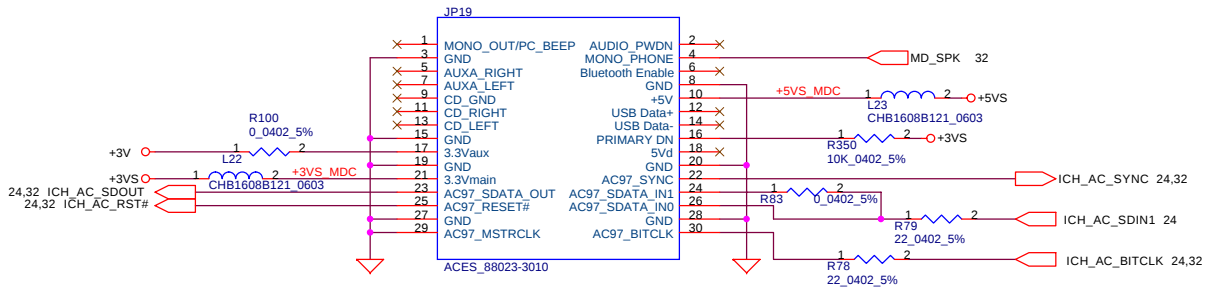
Title			
Softwave DJ			
Size	Document Number		Rev
B	Sapporo 300P		0.3
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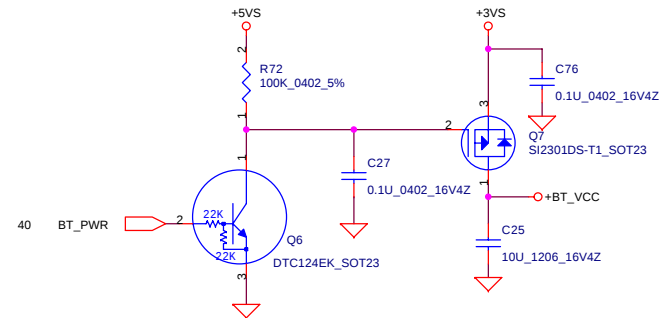


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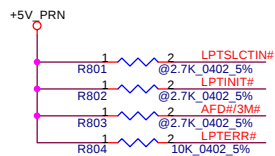
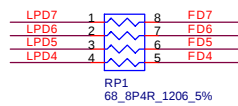
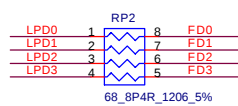
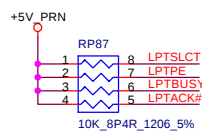
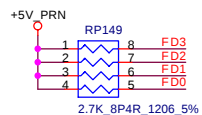
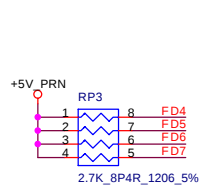
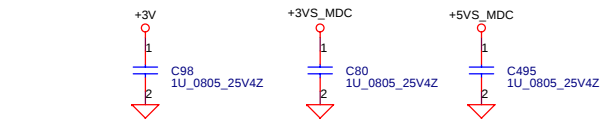
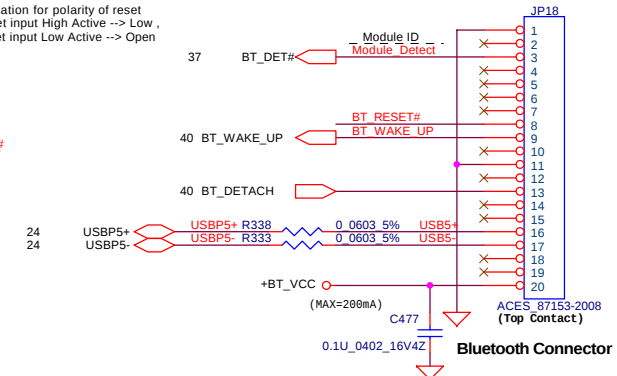
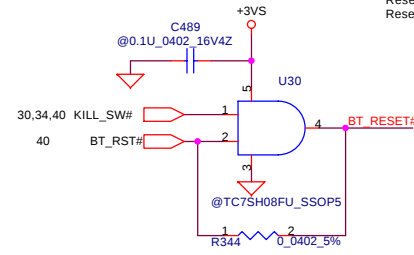
MDC CONN.



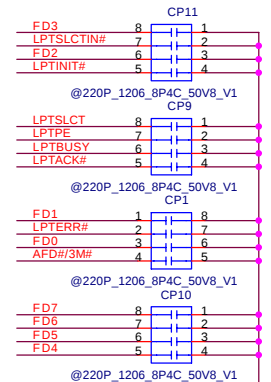
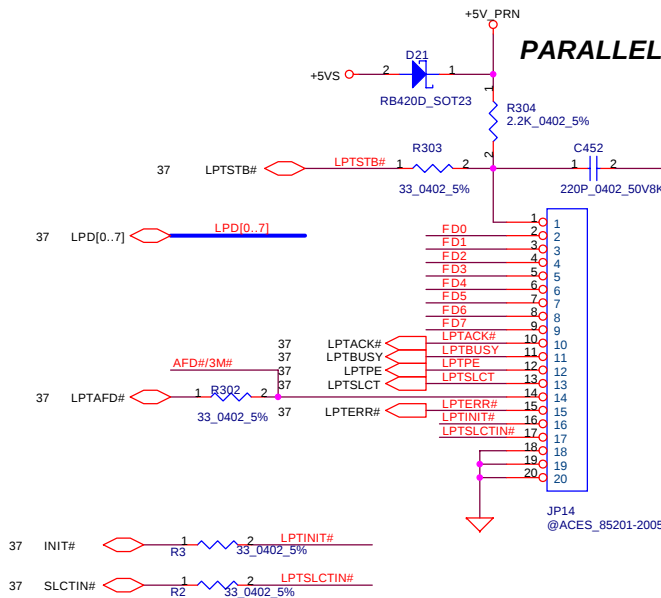
BlueTooth Interface



Module ID
Indication for polarity of reset
Reset input High Active --> Low ,
Reset input Low Active --> Open



PARALLEL PORT

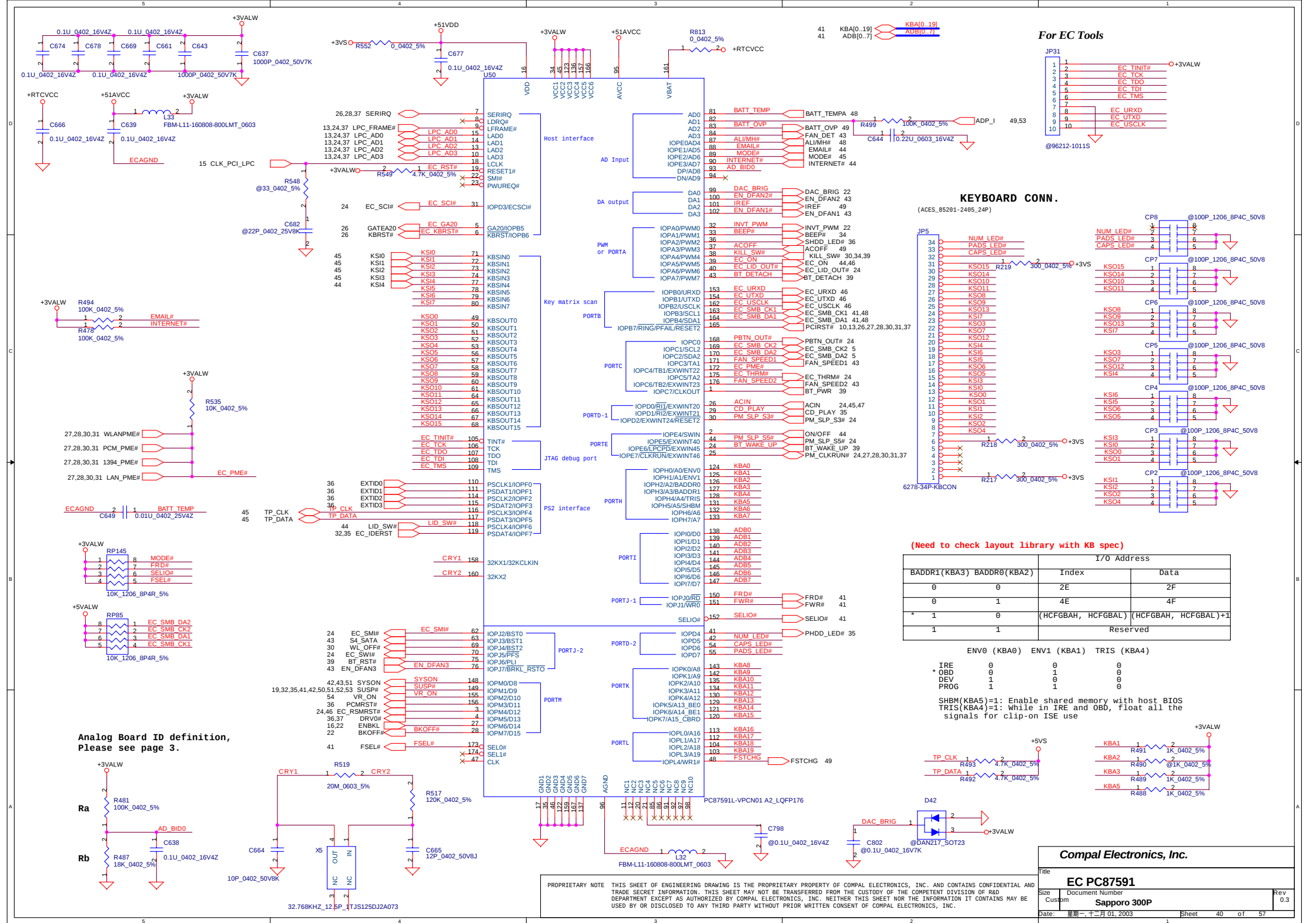


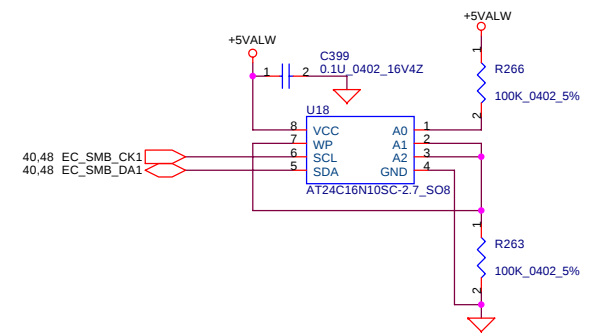
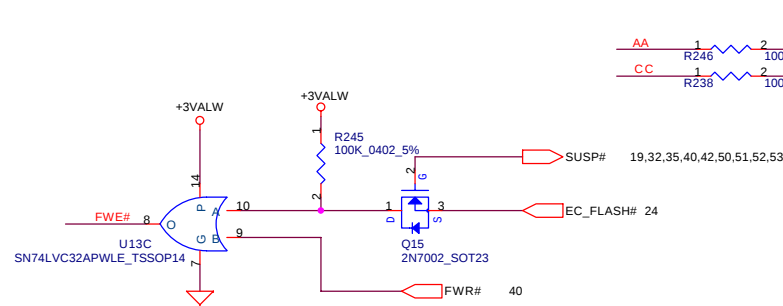
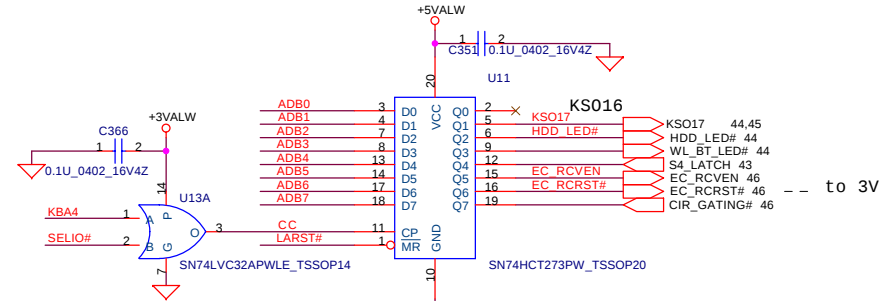
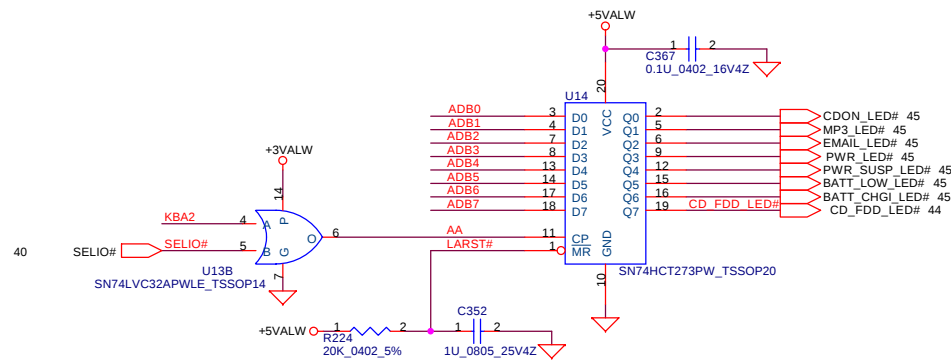
Compal Electronics, Inc.

PARALLEL/MDC PORT

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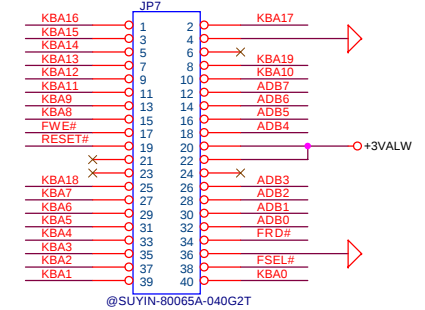
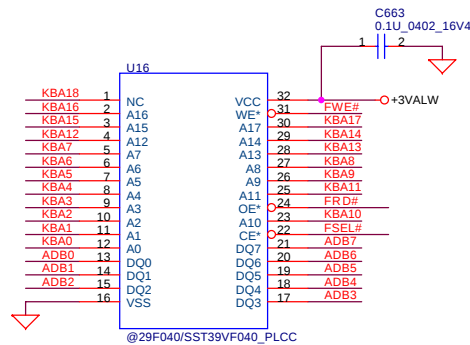
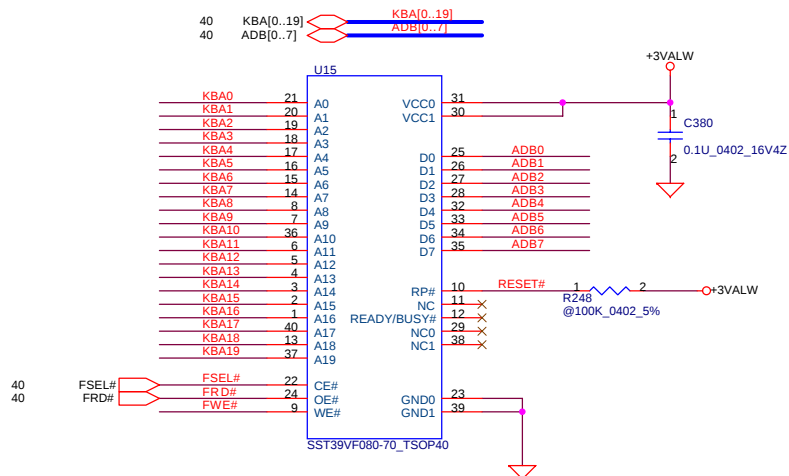




1MB Flash ROM

512KB Flash ROM

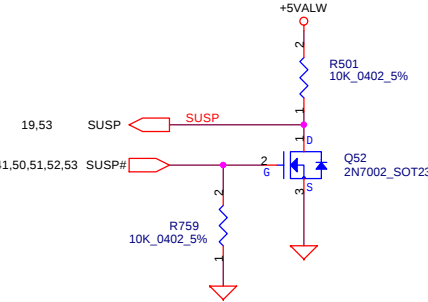
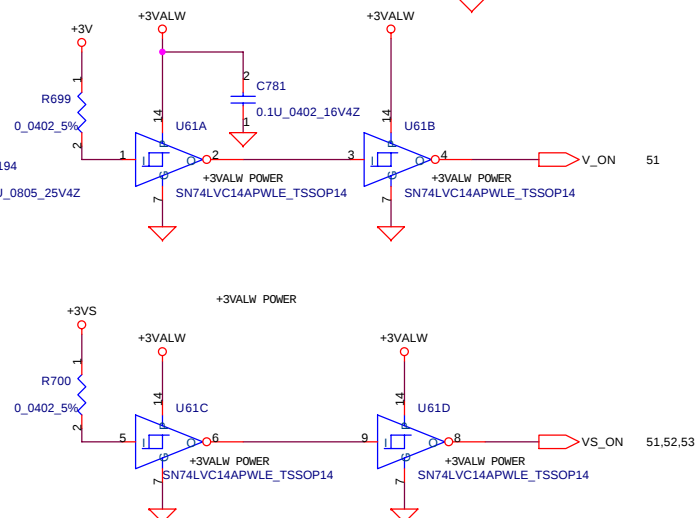
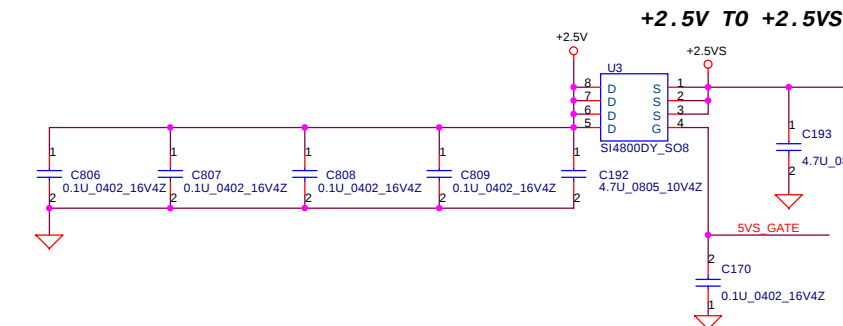
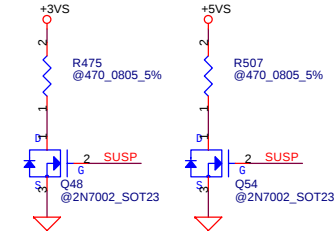
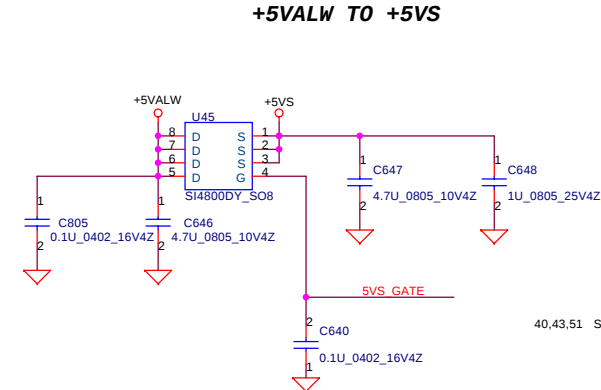
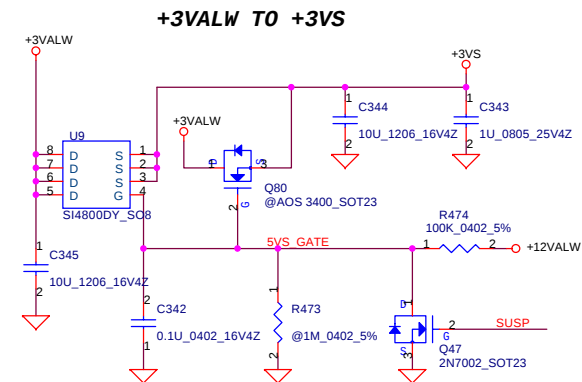
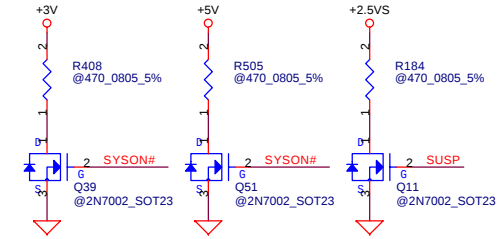
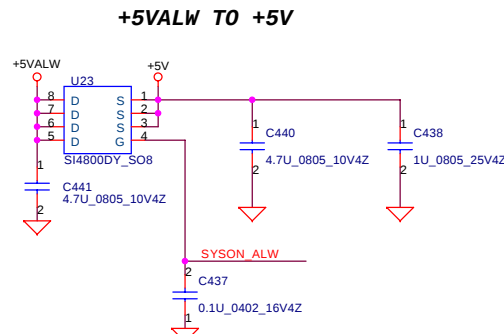
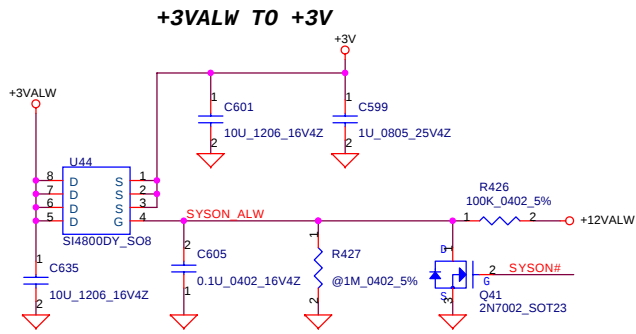
Flash ROM Socket Conn.



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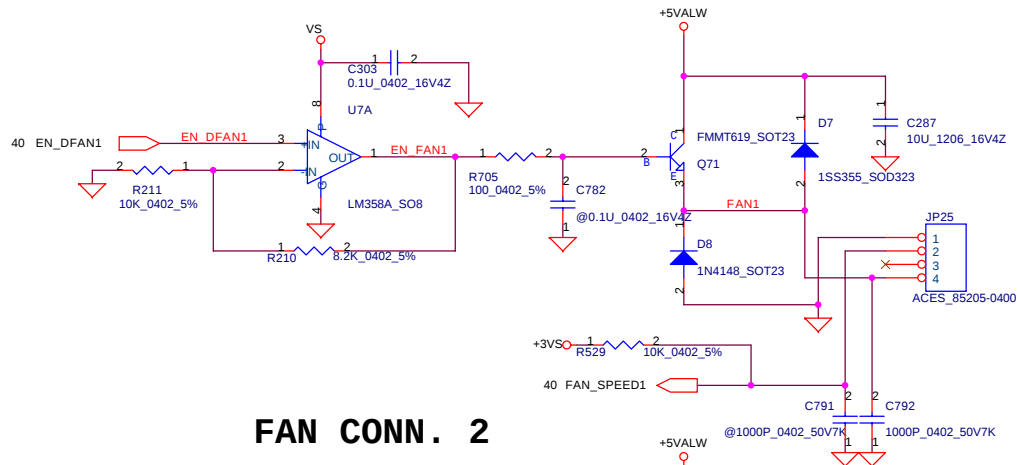
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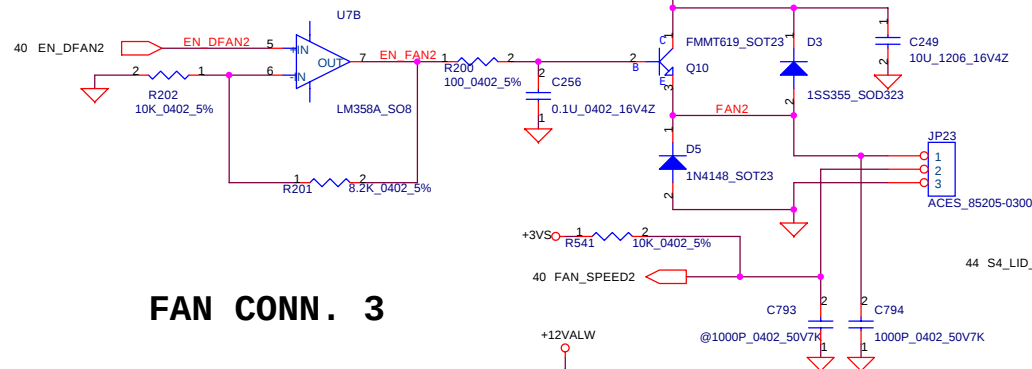
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Compal Electronics, Inc.		
Title		
POWER CONTROL CKT		
Size B	Document Number	Rev
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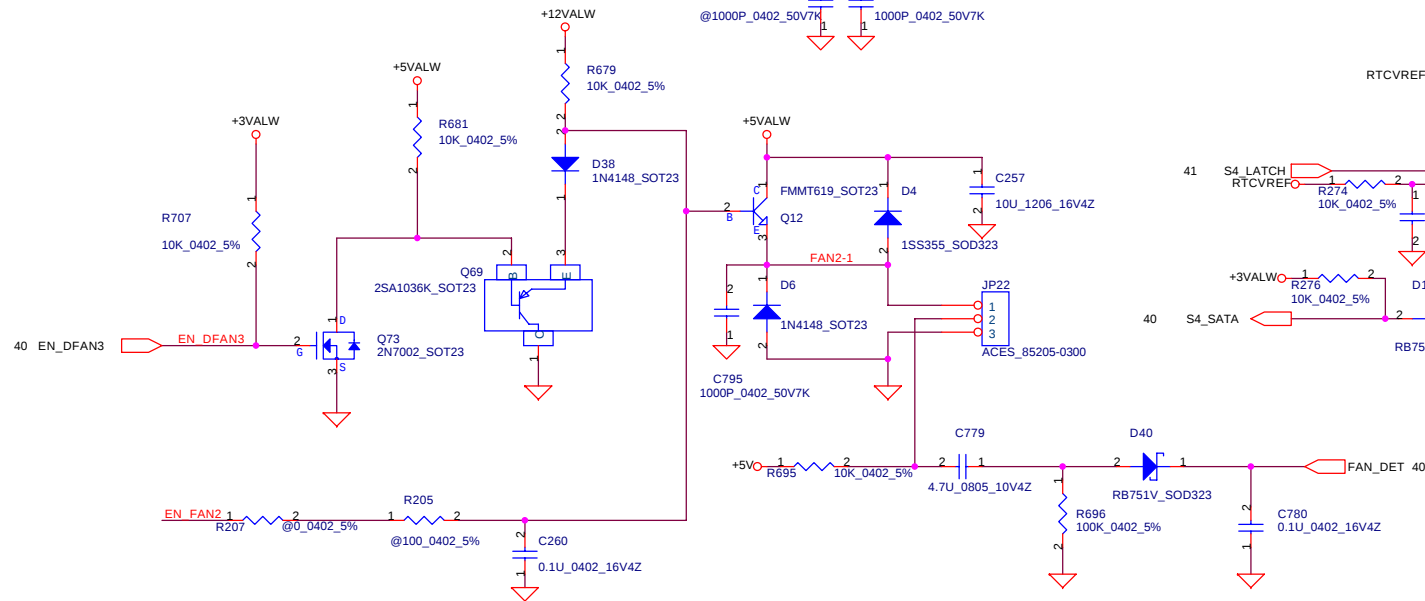
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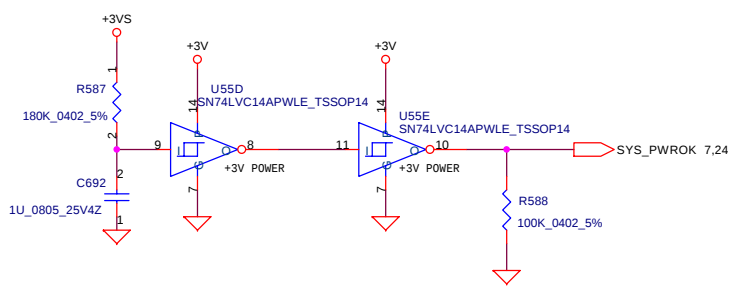
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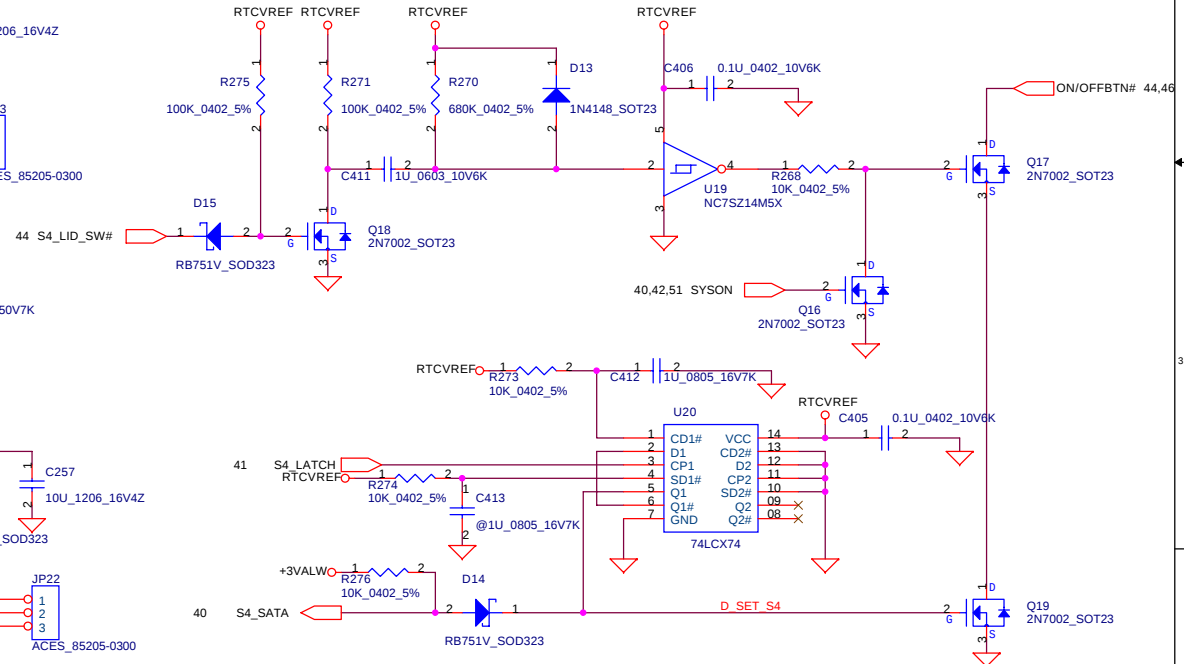
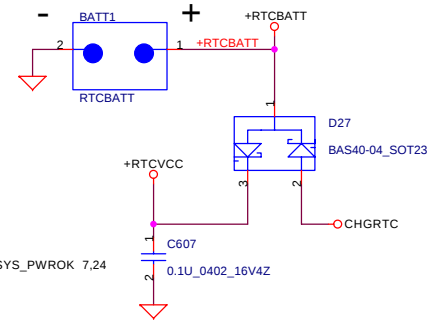
FAN CONN. 3



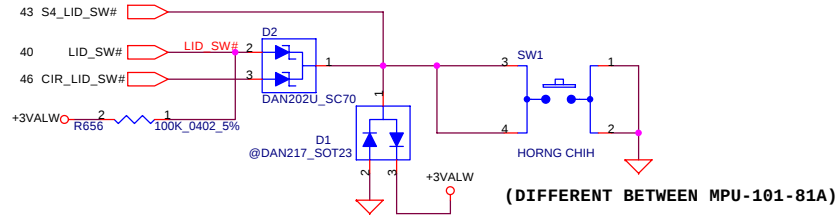
Power ON Circuit



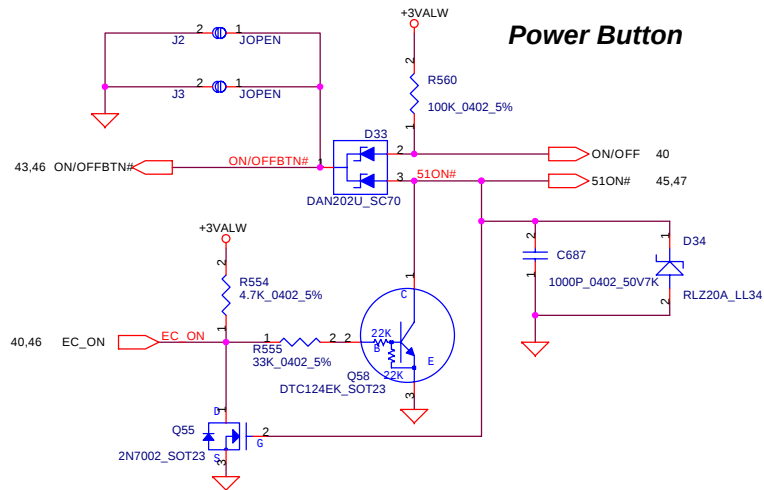
RTC Battery



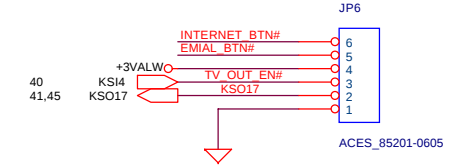
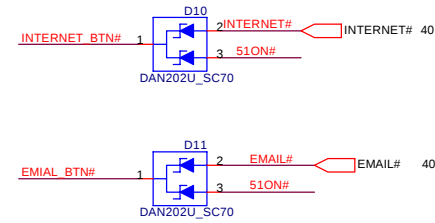
LID Switch



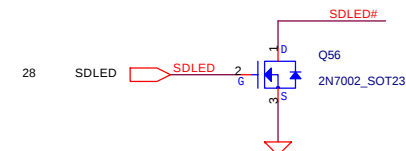
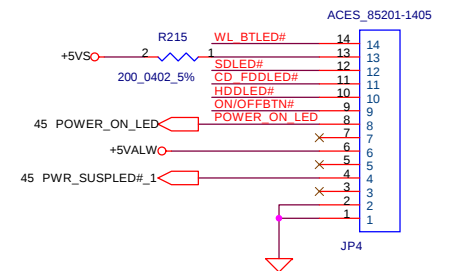
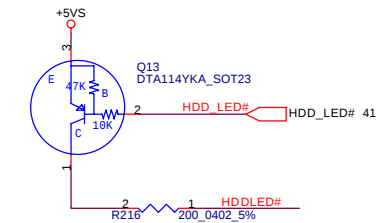
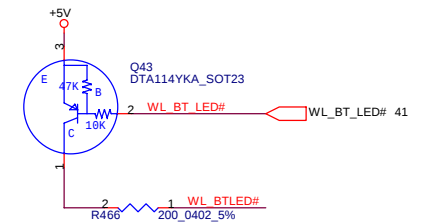
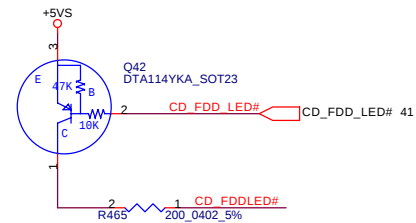
Power Button



Button FPC Conn.

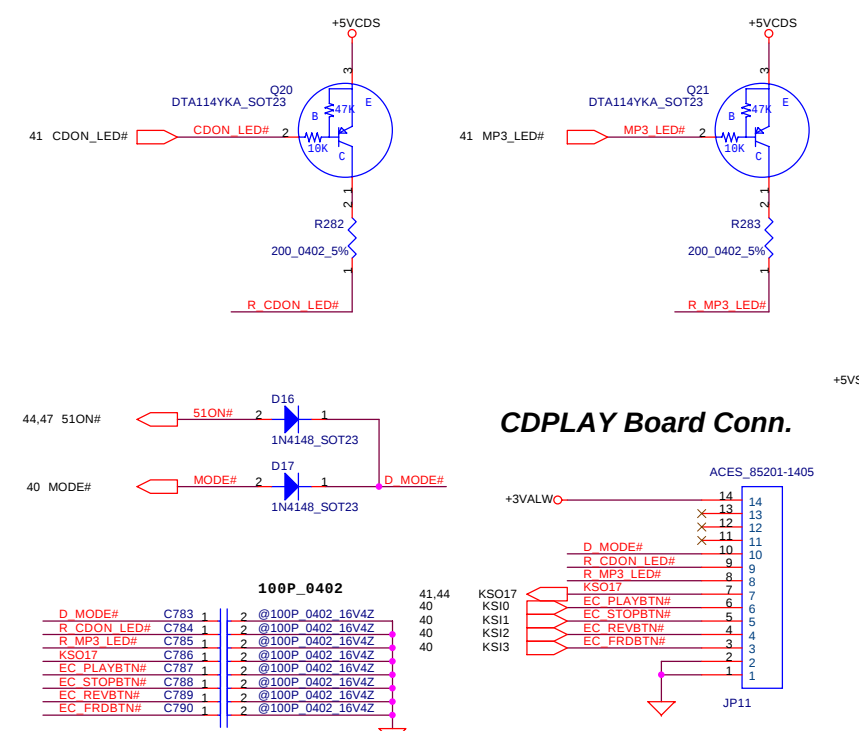
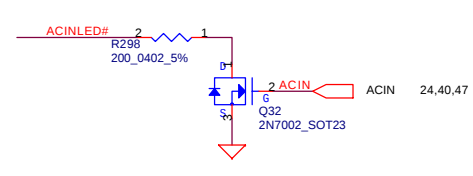
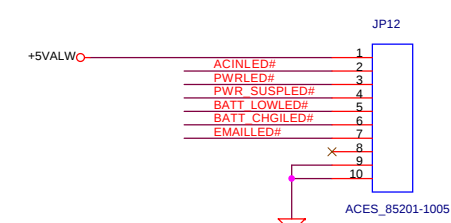
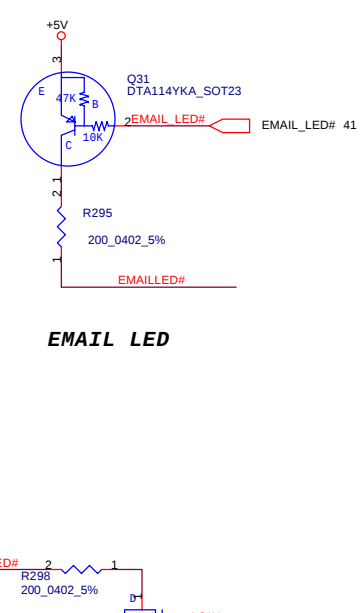
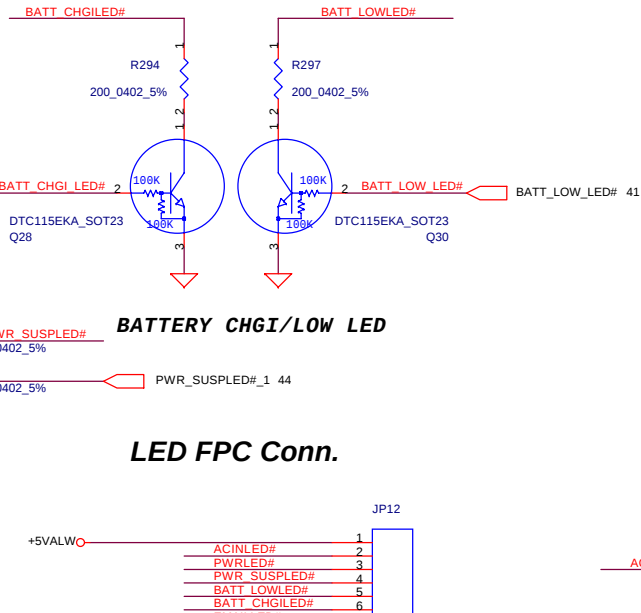
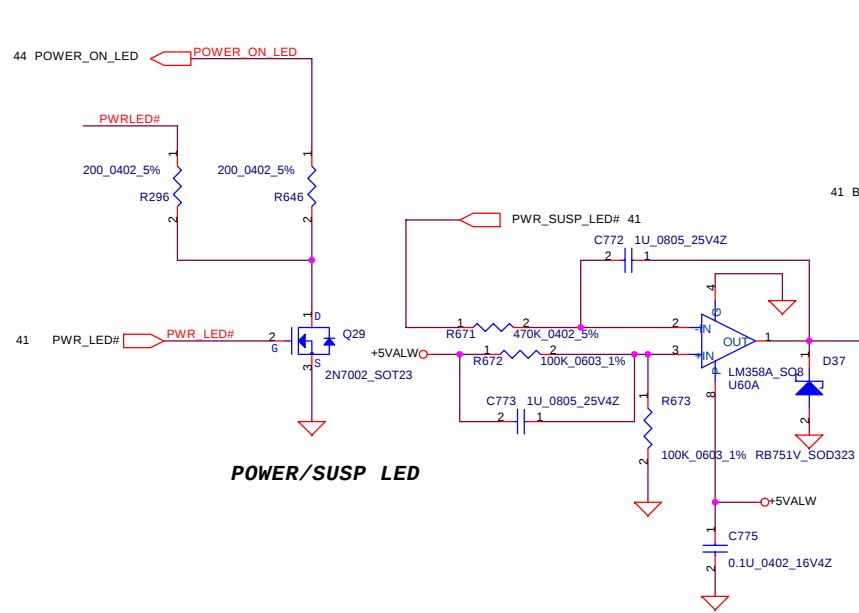


Power FPC Conn.

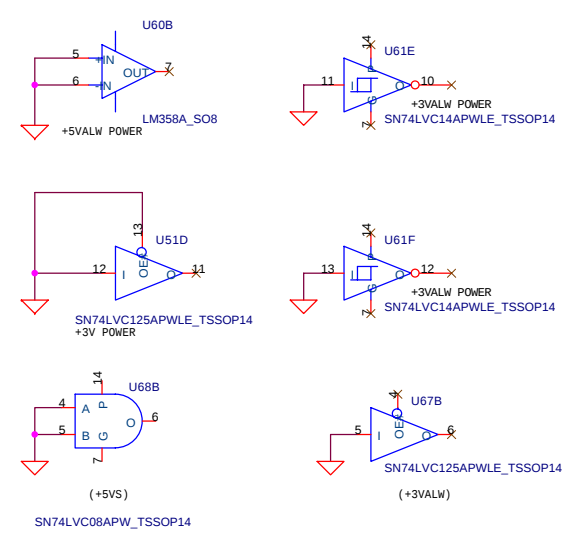
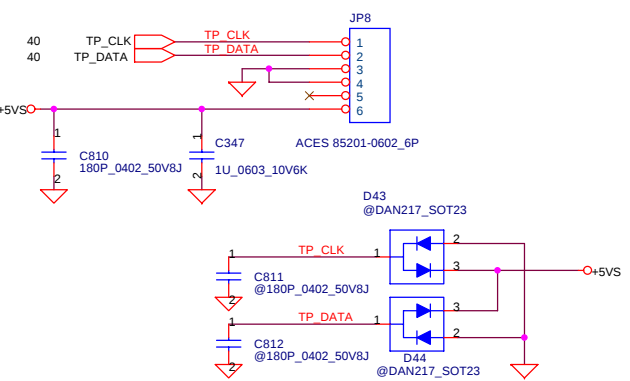


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Title		
Switches & Connectors		
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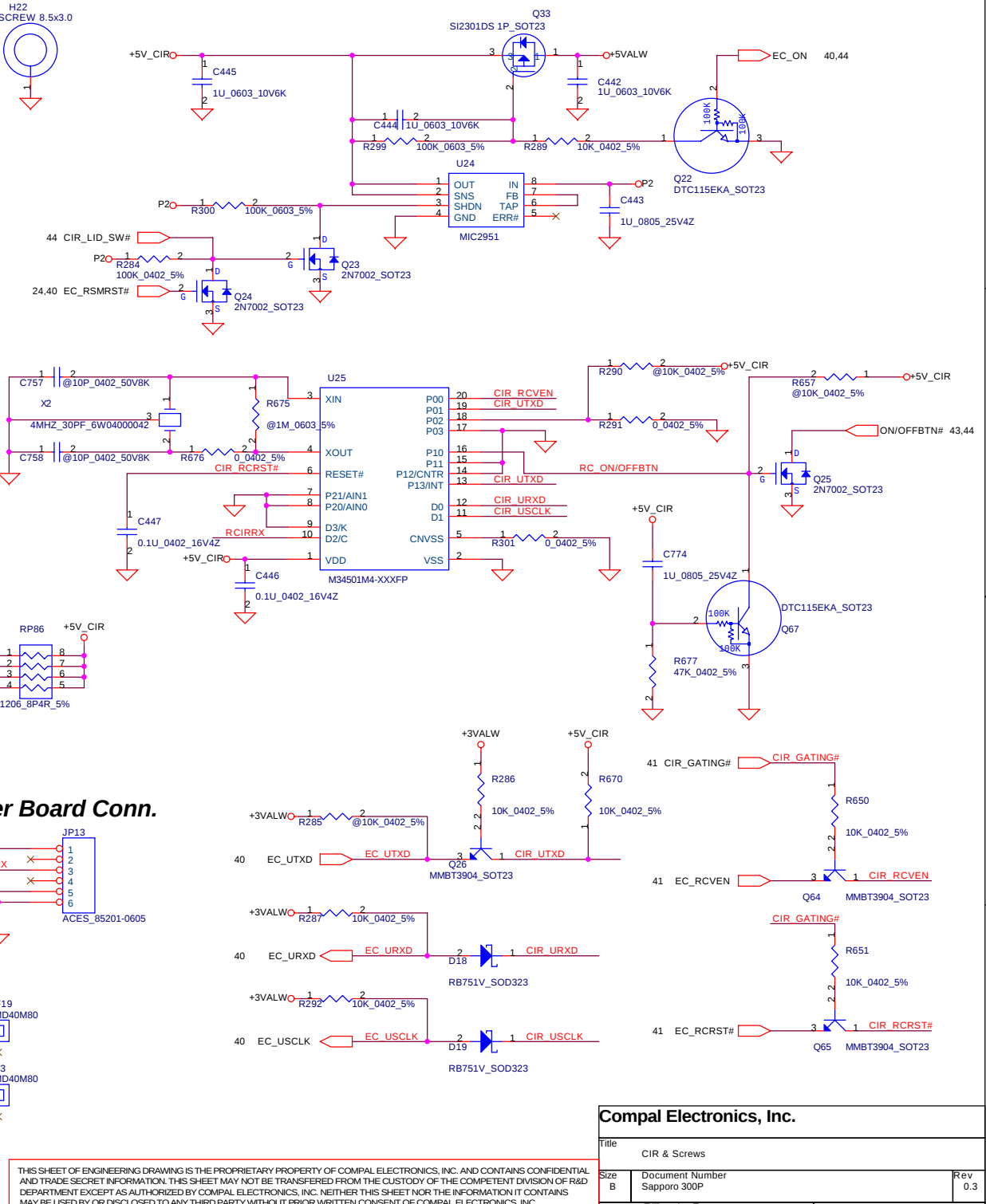
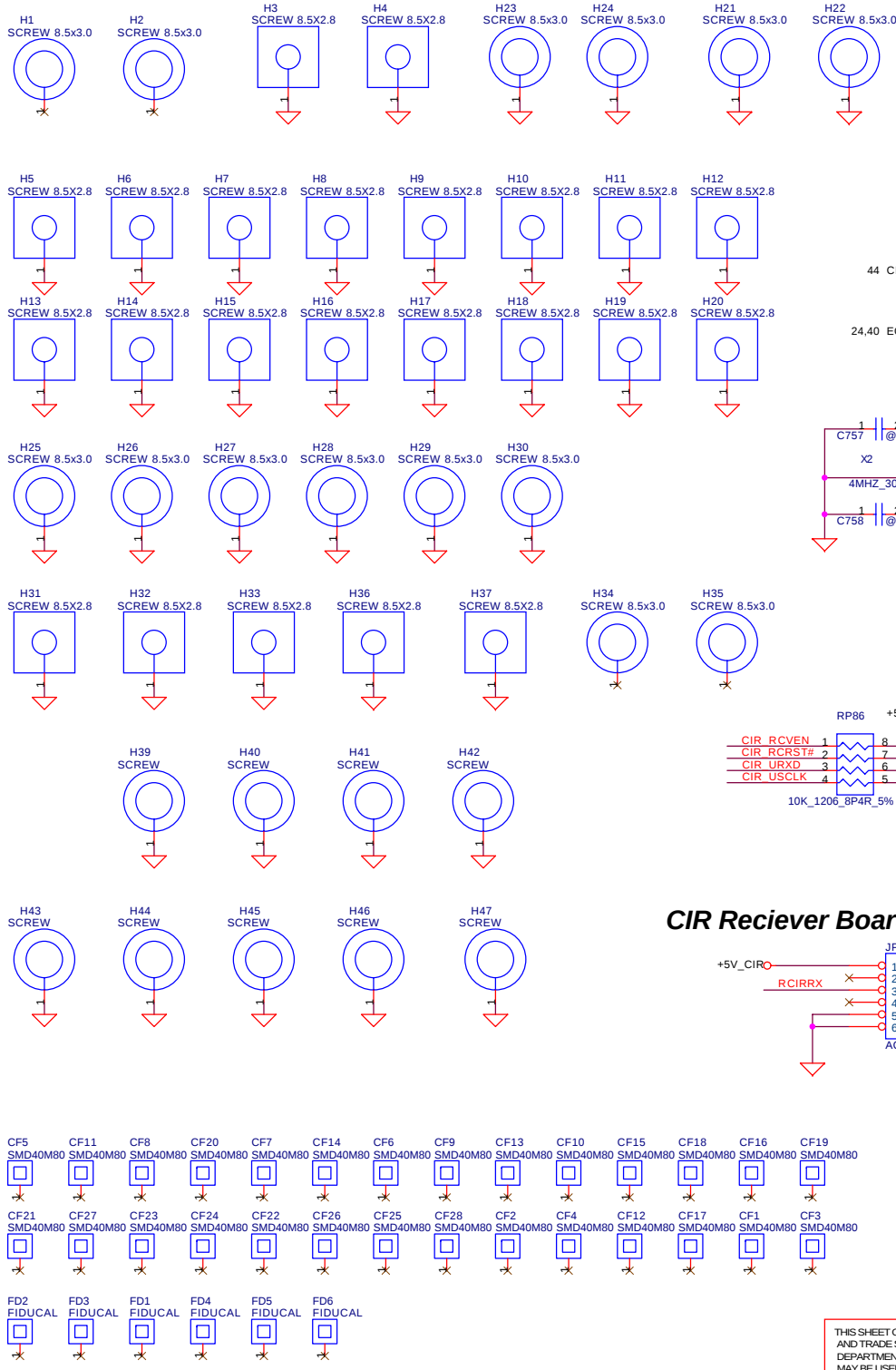


Touch Pad Connector



Compal Electronics, Inc.		
Title		
Switches & Connectors		
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B	Sapporo 300P	0.3
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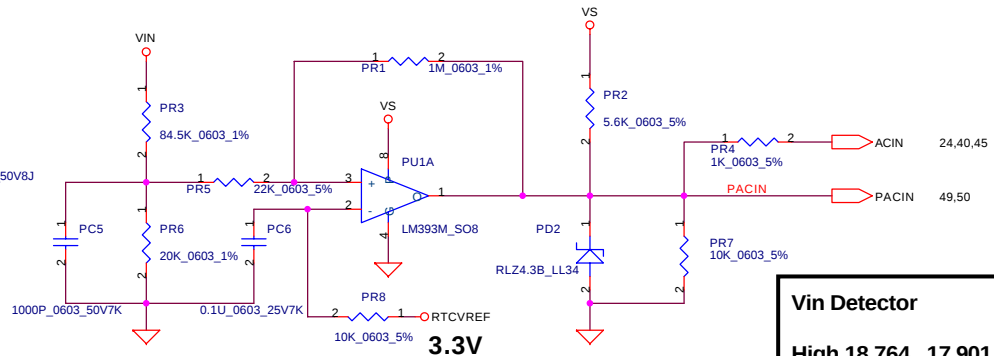
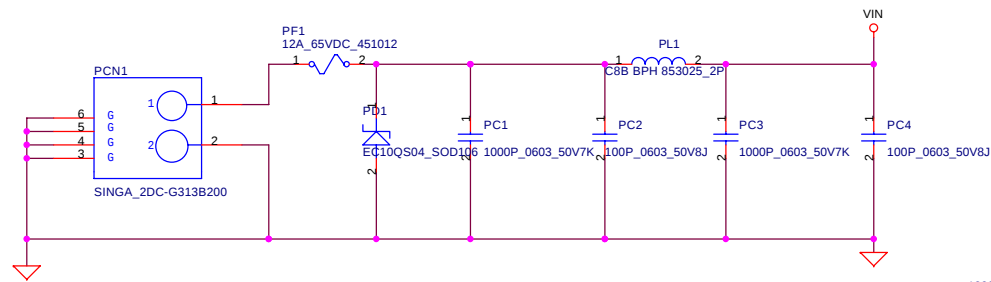
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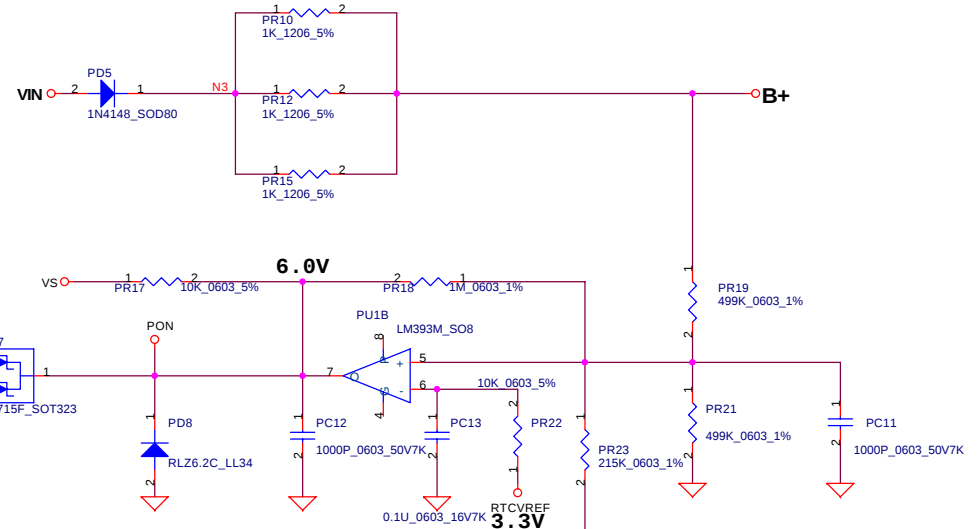
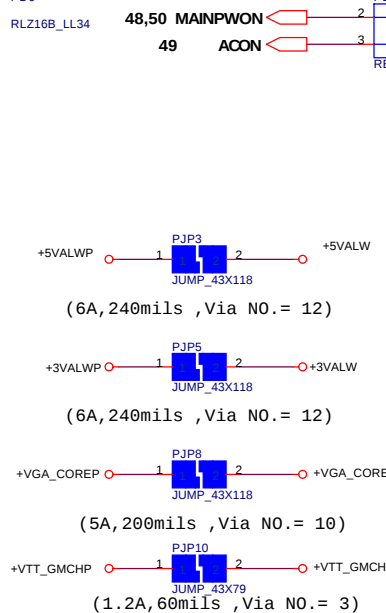
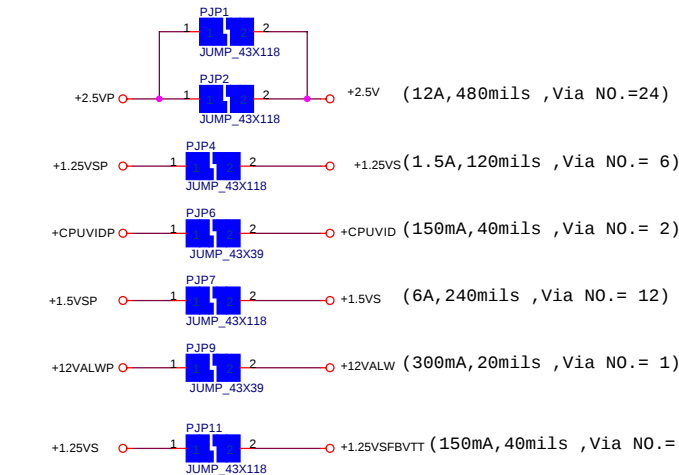
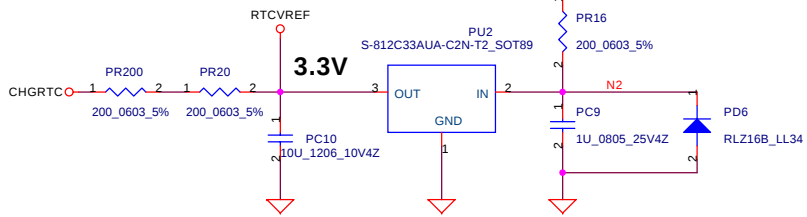
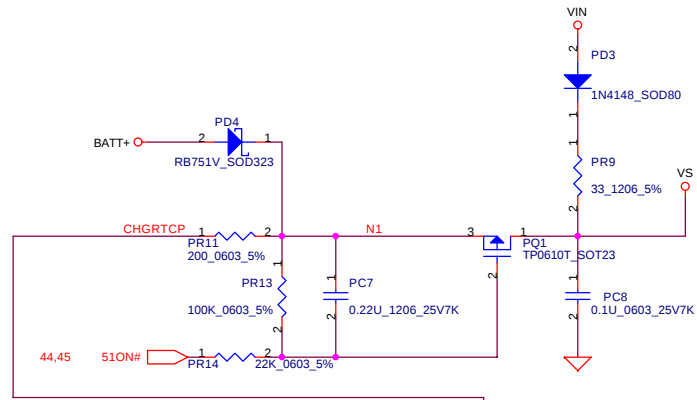
CIR Reciever Board Conn.

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Compal Electronics, Inc.		
Title CIR & Screws		
Size B	Document Number Sapporo 300P	Rev 0.3
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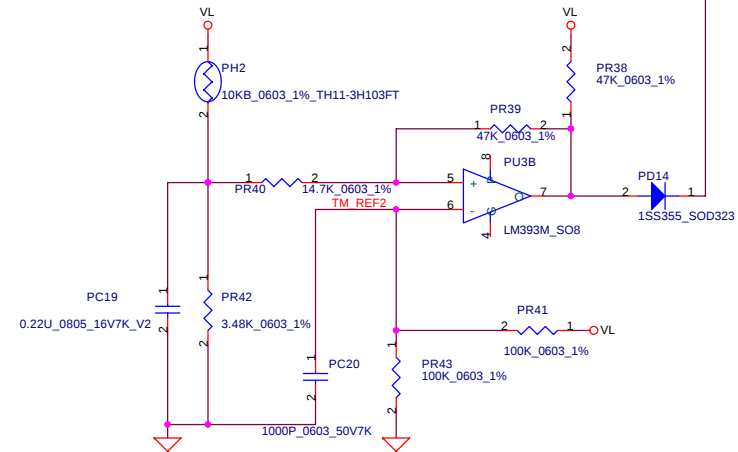
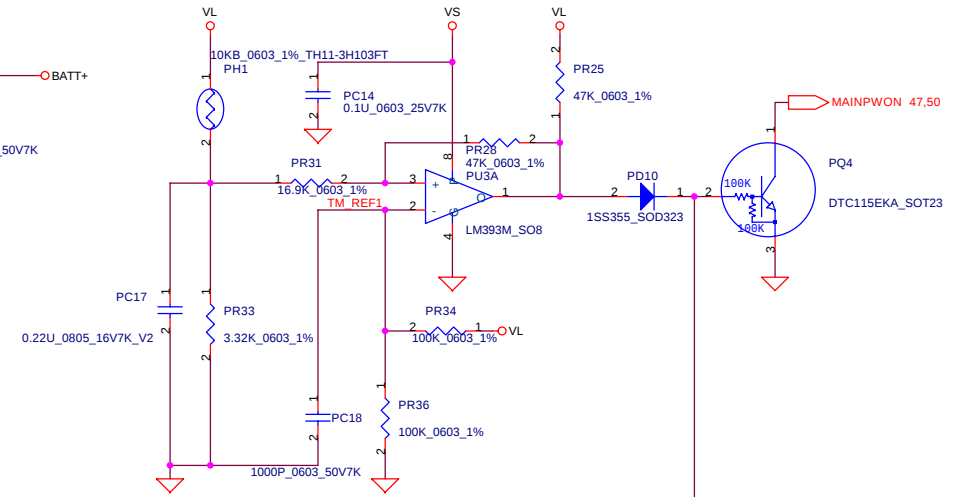
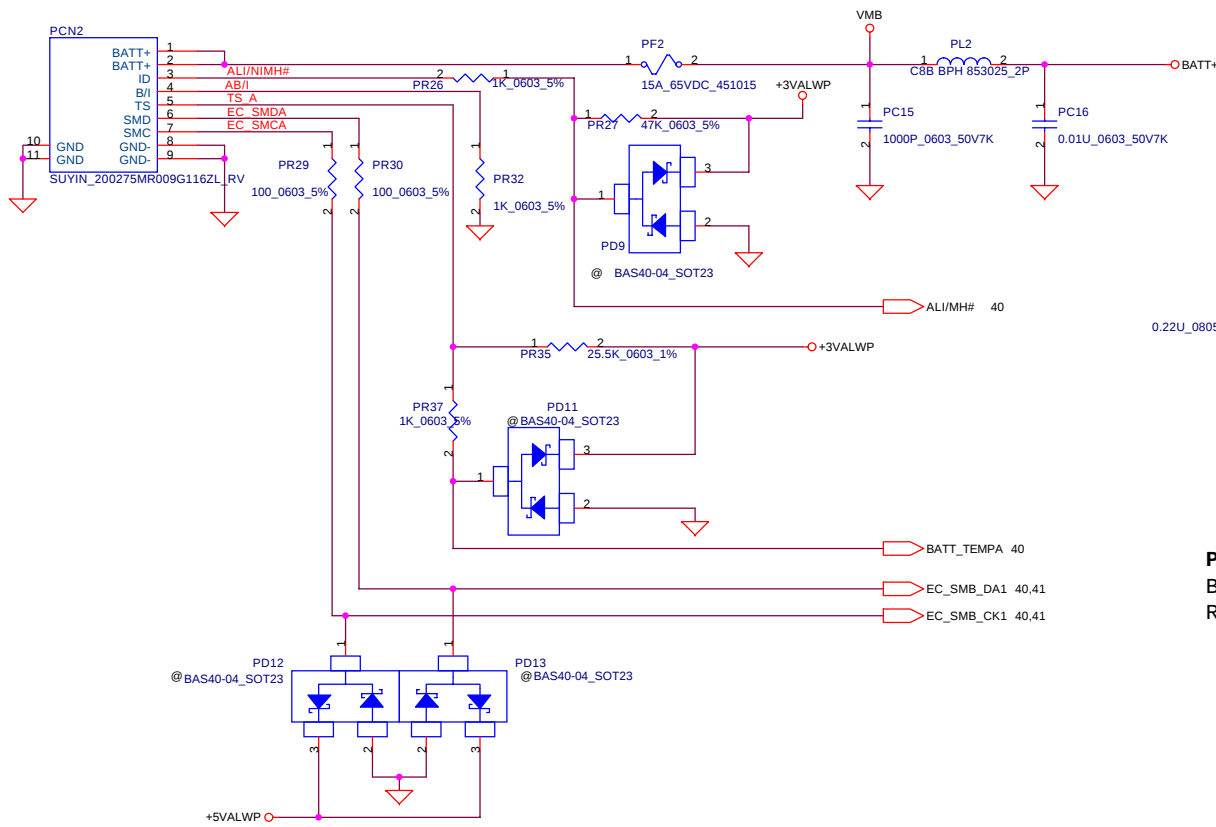
Vin Detector			
High	18.764	17.901	17.063
Low	17.745	16.903	16.038



Precharge detector			
15.34	15.90	16.48	
13.13	13.71	14.20	

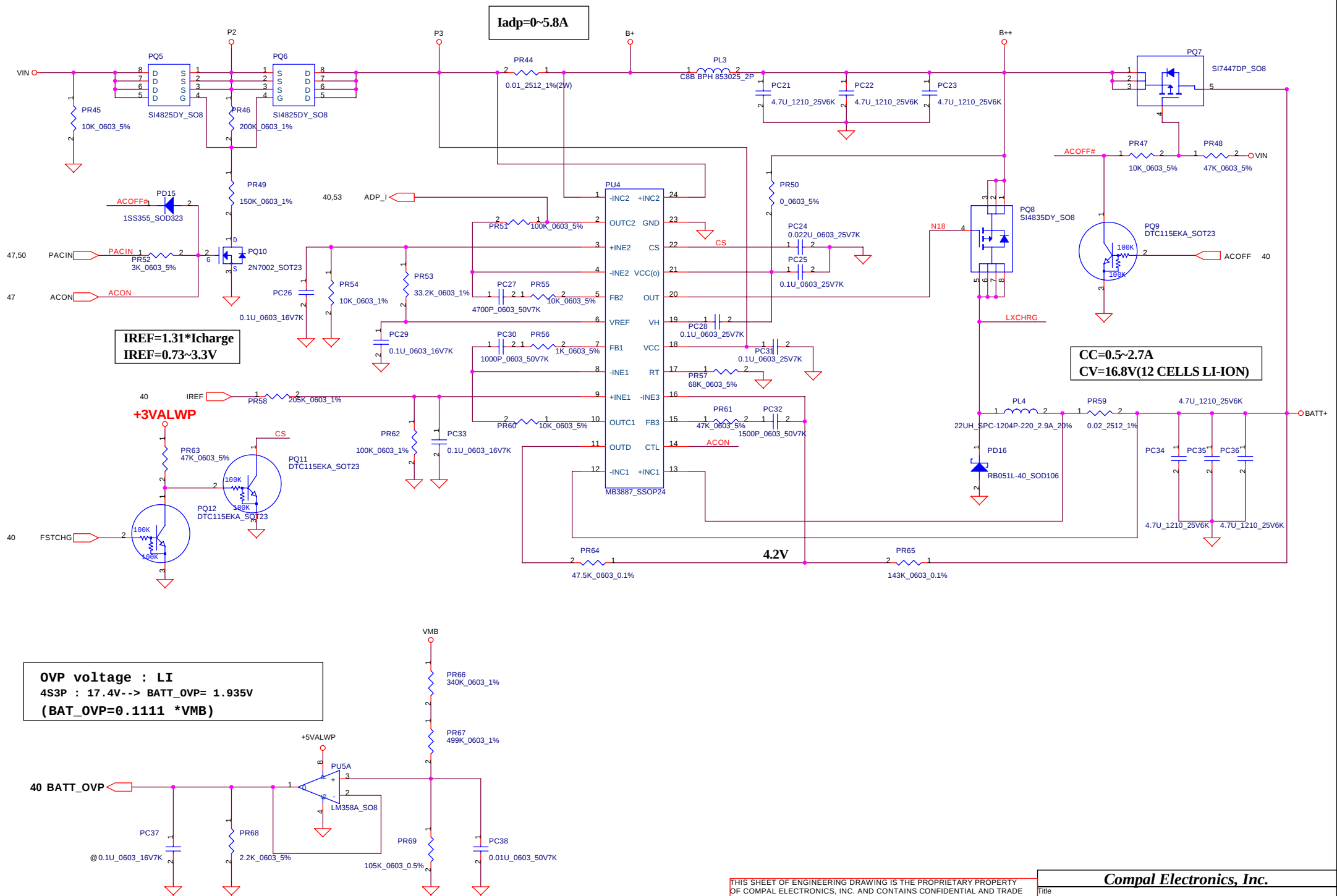
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Compal Electronics, Inc.			
Title			
DCIN & DETECTOR			
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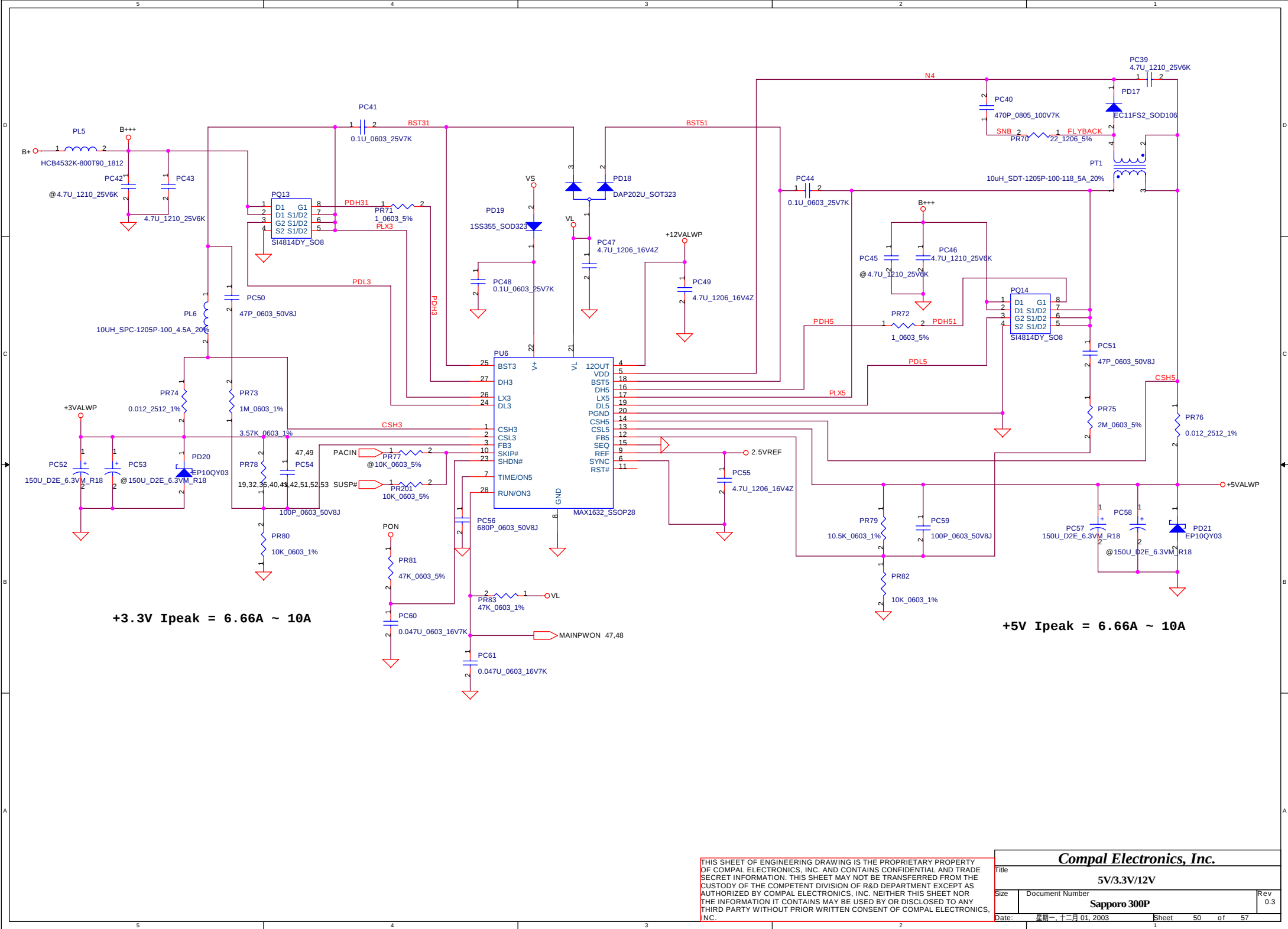
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Compal Electronics, Inc.			
Title			
BATTERY CONN/OTP			
Size	Document Number	Rev	
	Sapporo 300P	0.3	
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Compal Electronics, Inc.			
Title			
CHARGER			
Size	Document Number		Rev
	Sapporo 300P		0.3
Date:	星期一, 十二月 01, 2003	Sheet	49 of 57

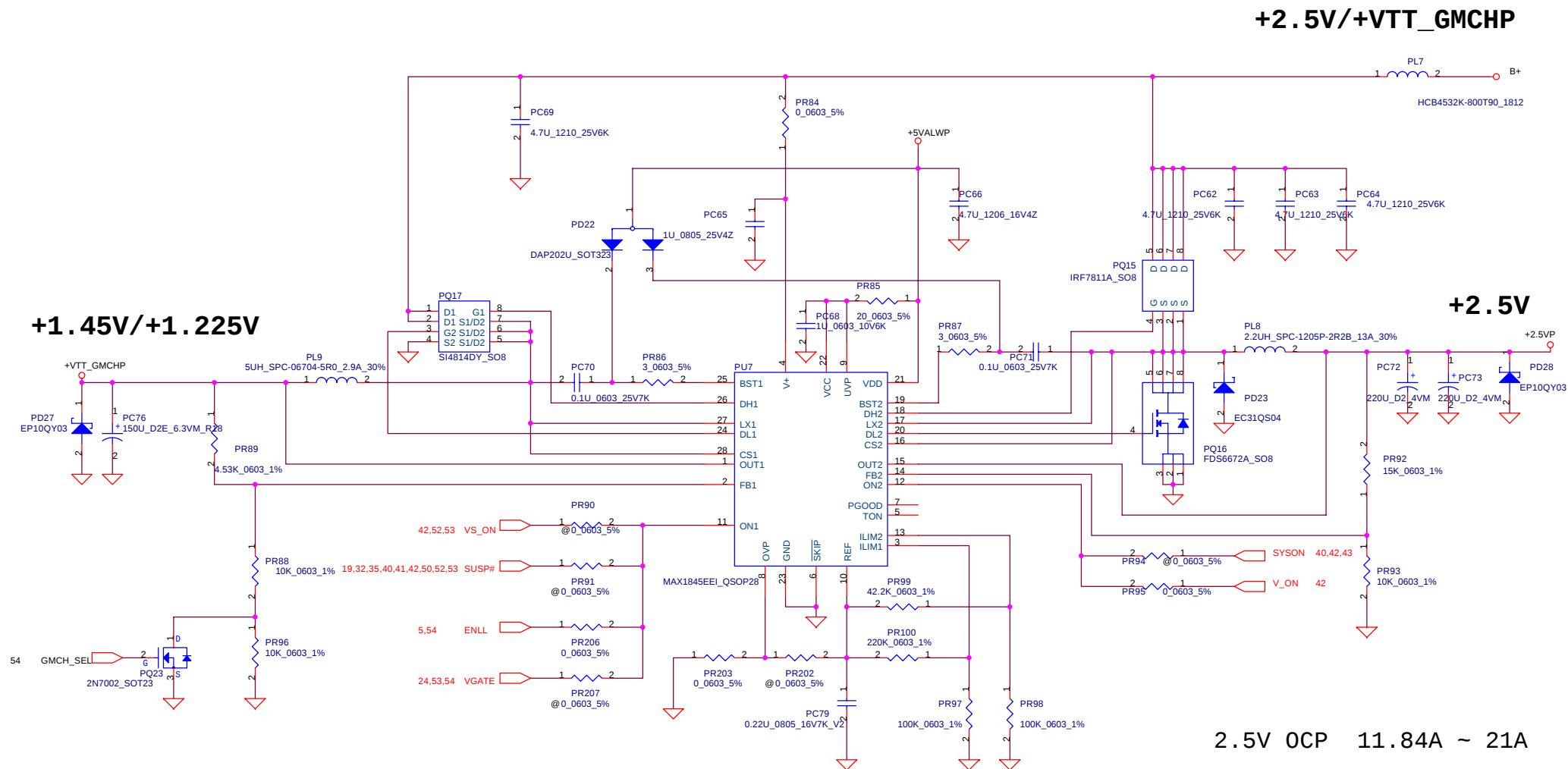


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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Compal Electronics, Inc.			
Title			
5V/3.3V/12V			
Size	Document Number		Rev
	Sapporo 300P		0.3
Date:	星期一, 十二月 01, 2003	Sheet	50 of 57



GMCH_SEL=0	PRESCOTT	VTT_GMCH=1.225V	OCP 1.92A ~ 3.71A
GMCH_SEL=1	NORTHWOOD	VTT_GMCH=1.45V	OCP 1.98A ~ 3.78A

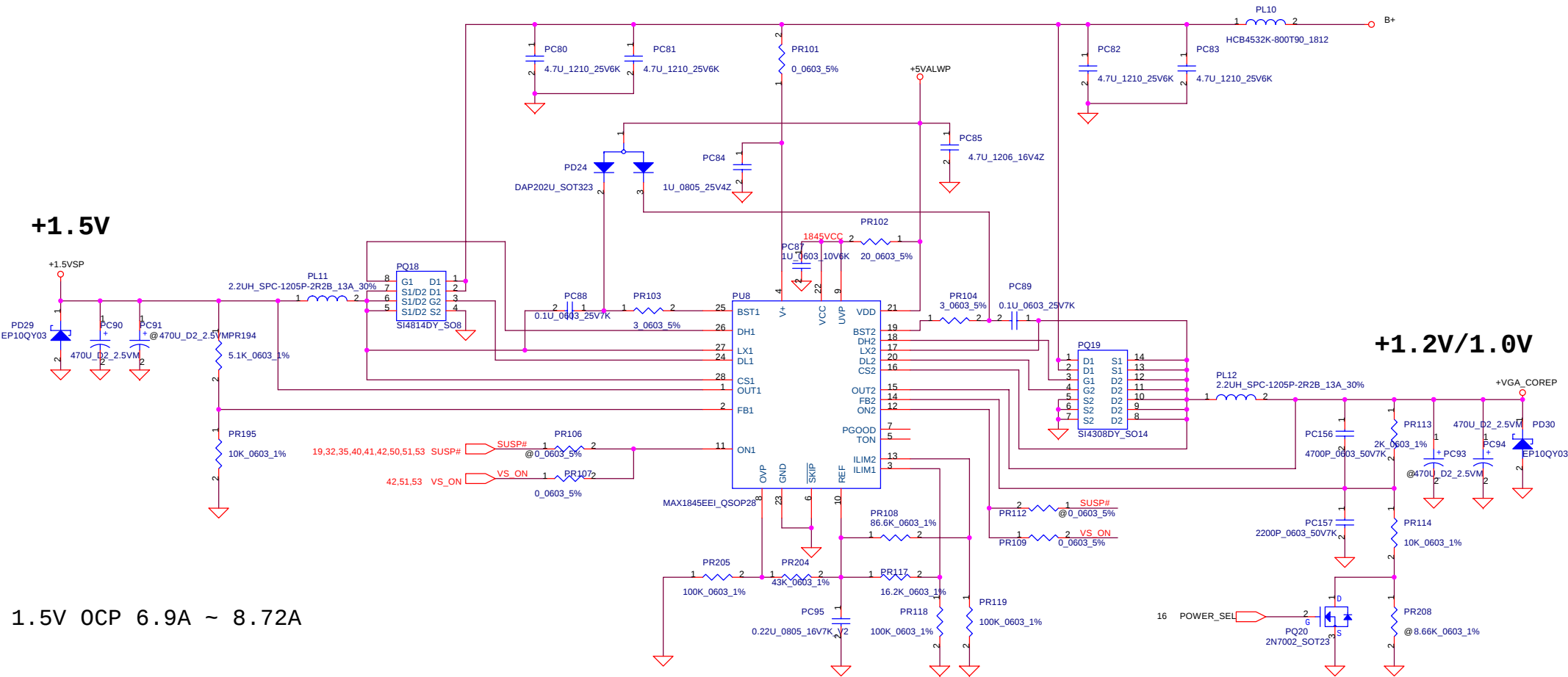
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Compal Electronics, Inc.			
Title			
DDR_2.5V/VTT_GMCH			
Size	Document Number		Rev
	Sapporo 300P		0.3
Date:	星期一, 十二月 01, 2003	Sheet	51 of 57

+1.5V

1.5V OCP 6.9A ~ 8.72A

+1.2V/1.0V

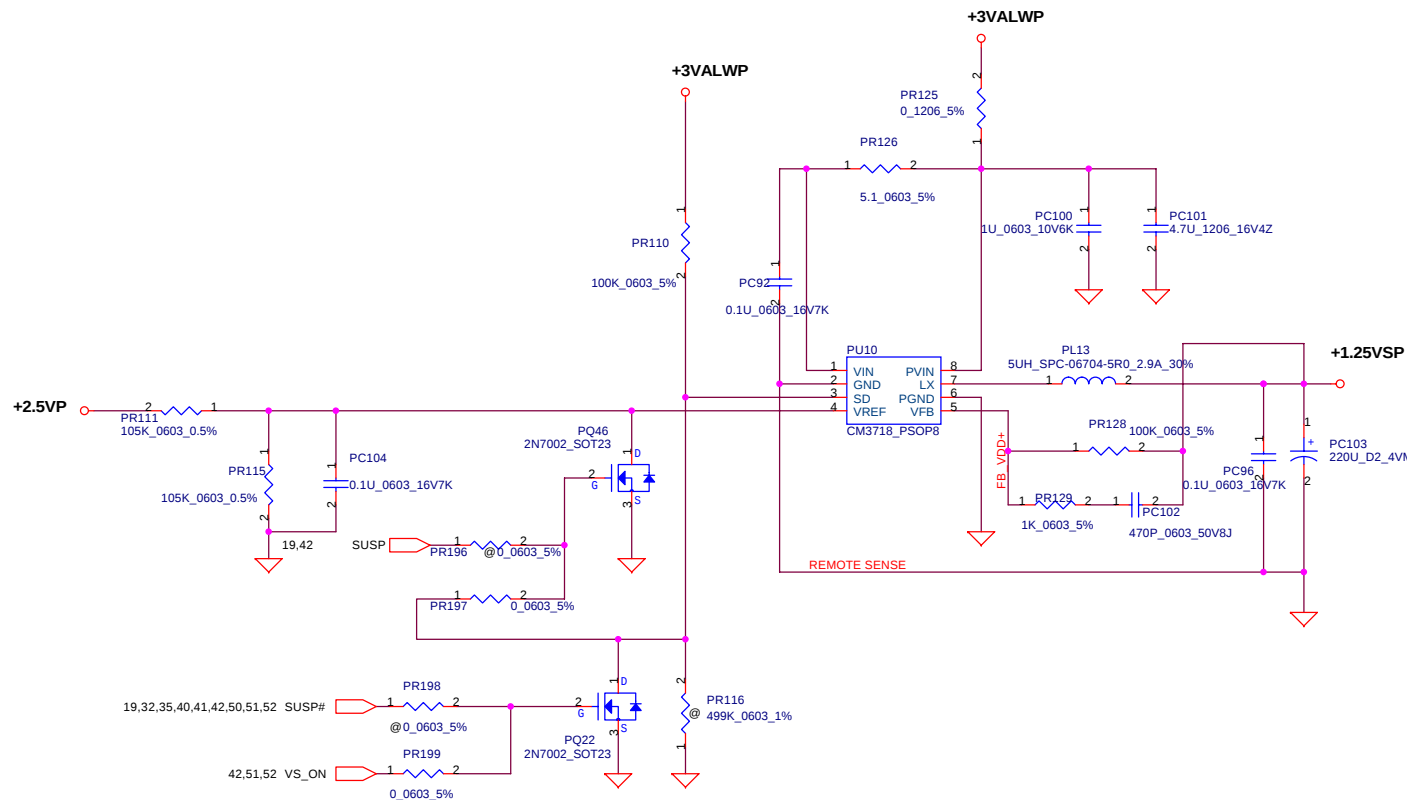
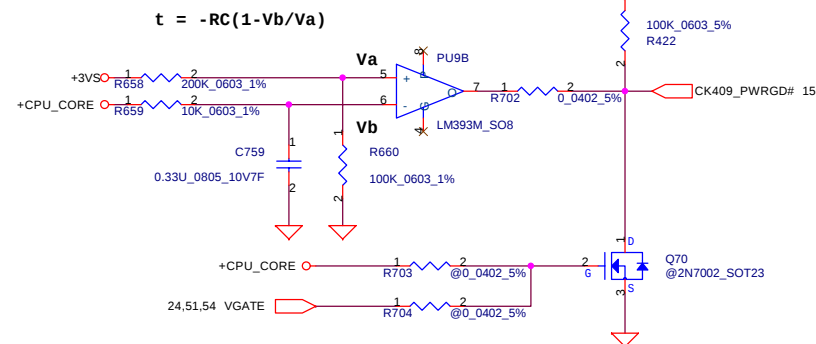
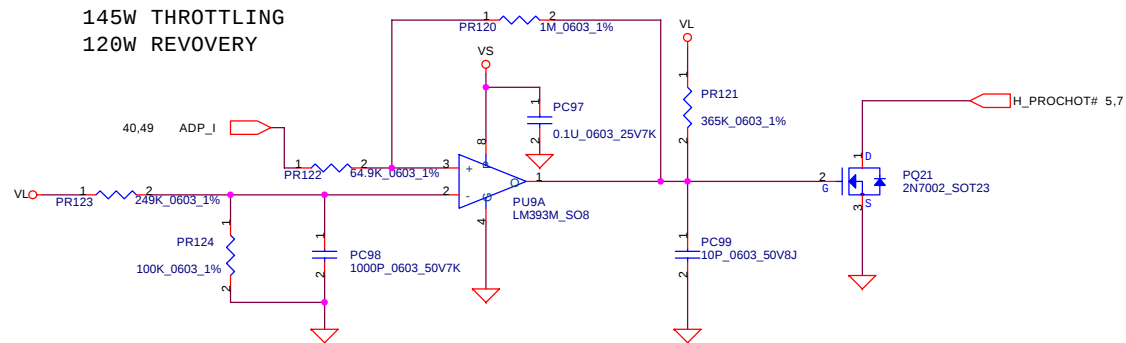


NV36		
POWER_SEL=1	VOUT=1.27V OCP 7.1A ~ 13.5A	PR113=2K_0603_1%
POWER_SEL=0	VOUT=1V OCP 7A ~ 13A	Unpop PR208

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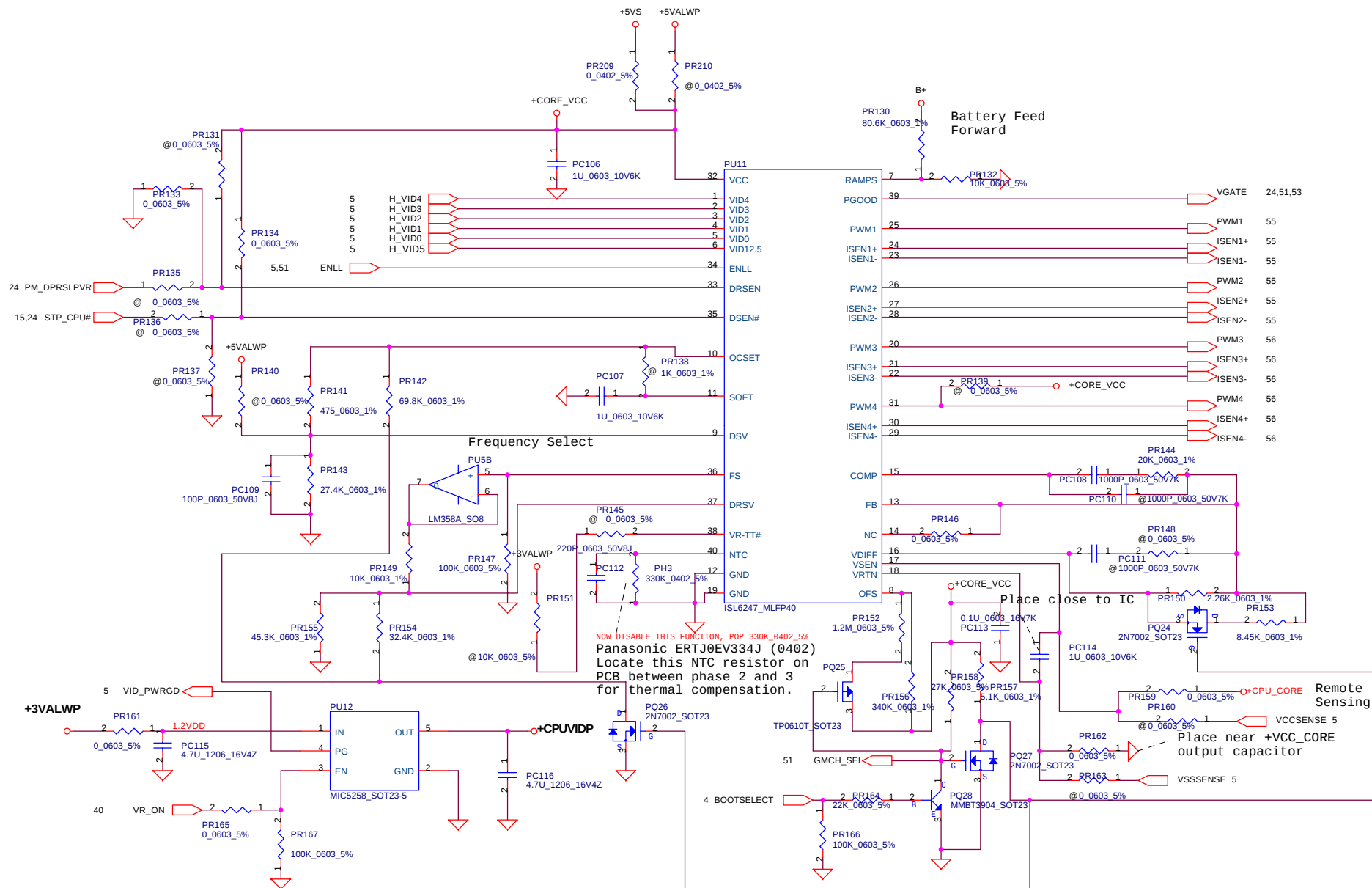
Compal Electronics, Inc.		
Title VGA_CORE/1.5V		
Size	Document Number Sapporo 300P	Rev 0.3
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145W THROTTLING 120W REV0VERY



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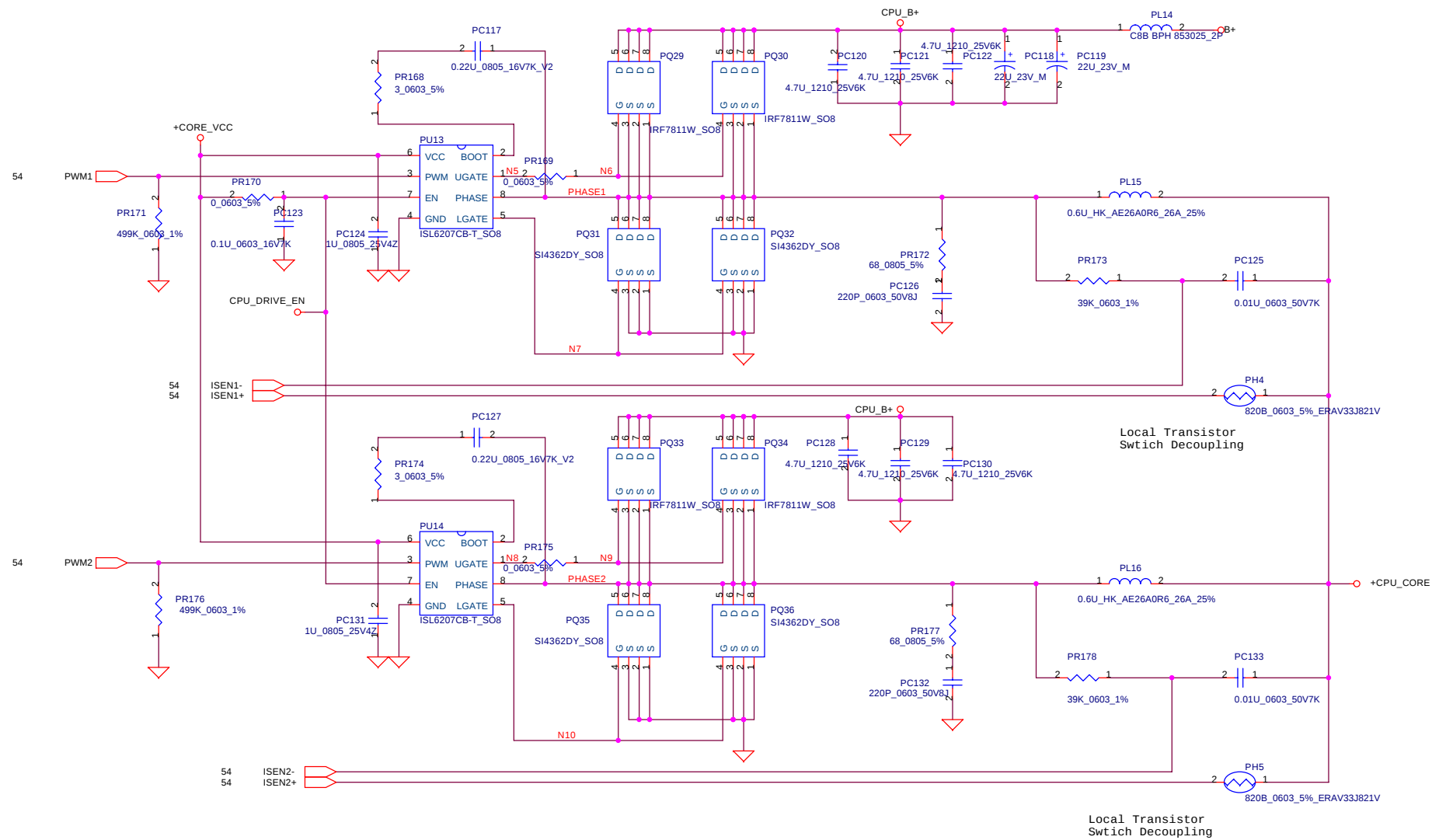
Compal Electronics, Inc.		
Title		
DDR_1.25V/CLOCK THROTTLING		
Size	Document Number	Rev
	Sapporo 300P	0.3
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BOOTSELECT=1 PRESCOTT

BOOTSELECT=0 NORTHWOOD

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Compal Electronics, Inc.			
Title			
CPU_CORE Power stage 1			
Size	Document Number		Rev
	Sapporo 300P		0.3
Date:	星期一, 十二月 01, 2003	Sheet	55 of 57

DBQ02 PIR LIST

***** Rev0.1 PIR List *****

10/28/2003 Writen by Jason Shih
Change from DBQ01 LA-2041

P16:New add R749, R750, R751, R752, R753, R754
Add @ to R41, R343, R701

P17:R358, R389 change from 1K to 10K

P18:Add @ to R71, R76, R112, R348, R349
Add @ to C23, C55
Change R385 from 0.0402 to 49.9.0603

P19:New add U63
Add @ to U63
New add C826, C827, C828, C829, C830, C831
Add @ to C826, C827, C828, C829, C830, C831

P20:New add R722 - R733 (12pcs)
New add C832 ~ R839 (8pcs)

P21:New add R734 - R745 (12pcs)
New add C840 - R847 (8pcs)

P22:New add R746, R747, R748

***** Rev0.2 PIR List *****

11/03/2003 Writen by Jason Shih

P5:R18 del @
P5:R19 del @, Change to 680.0603.1% ----- for Prescott CPU

P22:New add R755, R756, R757

P39:R487 change from 0.0402 to 8.2K.0402

P41:Add new R758, R759

***** Rev0.2A PIR List *****

11/13/2003 Writen by Jason Shih
Add HDTV, SW-DJ, Yamaha AC97 Codec Function

P23:HDTV Function (NewPage)

P32:New add R787, 789, R790, C881, C882, C883

P34:JP10 change from 16pin to 20pin
JP10.18 new add SPDIF signal

P35: -- Del 02-168 peripheral circuit --
Del U46, X4, D31, Q14, Q49, Q50, L34, L35, RP83, RP84
Del R228, R235, R237, R244, R495, R496, R497, R498, R506, R509, R510, R514, R518, R532, R533, R534, R538, R539
Del C365, C641, C642, C651, C659, C662, C673

Add new U66, U68, Q75, Q76, Q77, D48
Add new R791, R792, R793, R794, R795
Add new C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C897

P36:Del RP139, U47, U48, C645
Add new RP150, RP151, U67, U68, Q78
Add new R796, R797, R798, R799, R800
JP28.60 change from +SVCD to +5VCD5

P39:PR3, PR87 change from 10P8R to 8P4R
Add new PR149
Add new R801, R802, R803, R804

11/14/2003 Writen by Jason Shih

P22:R16 change from 100.0402 to 200.0402

11/18/2003 Writen by Jason Shih

P6:Add @ to C481, C482, C493, C494
P34:Add @ to R662
R604 del @

PWR PIR LIST

EVT

page	Reason for change	Modify list
47	Change DC-jack from 3D to 2.5D	Change PCN1 from 2DC-S113L200 to 2DC-G313B200