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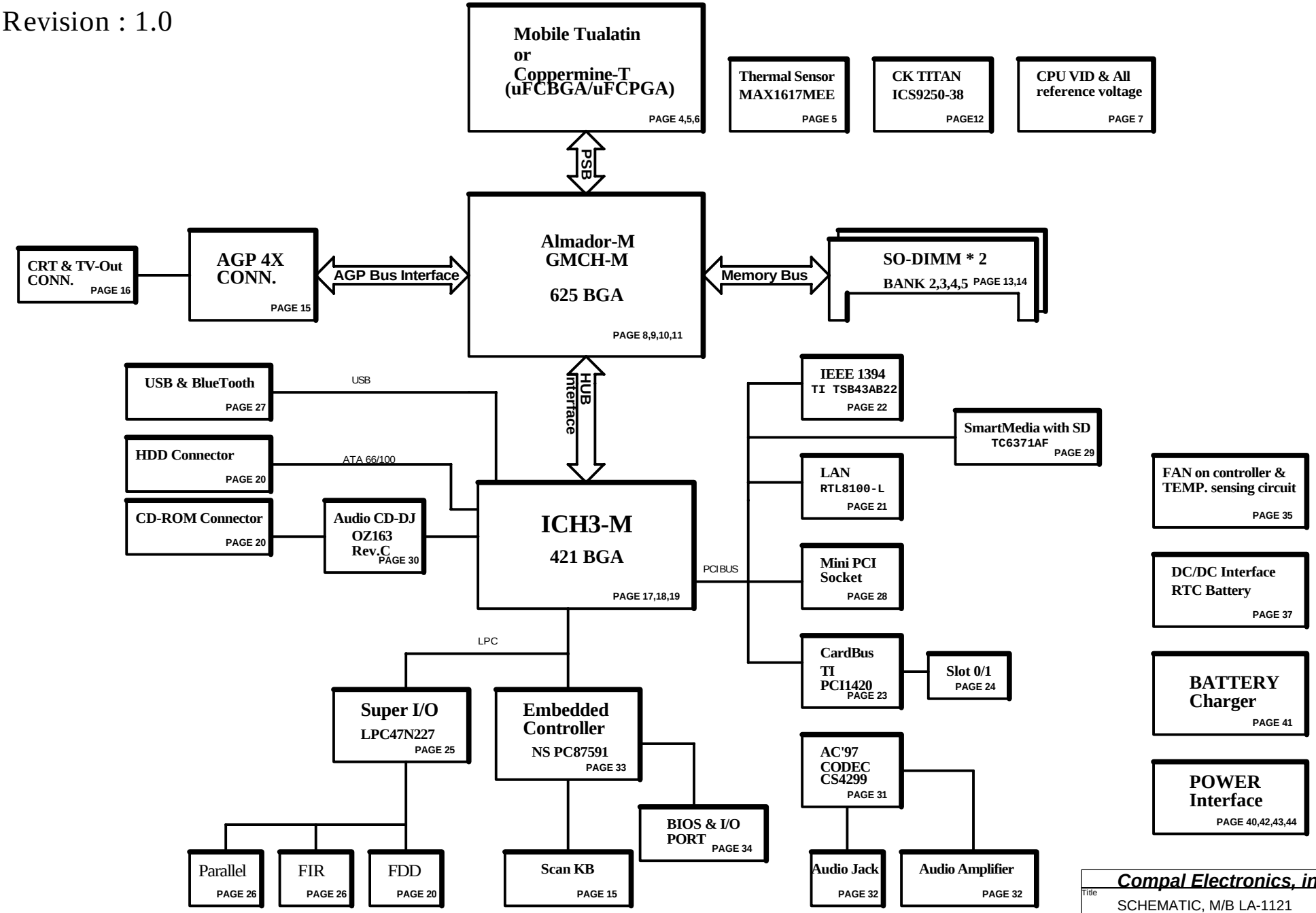
Model Name : 888M3
PCB No : LA-1121
Revision : 1.0

BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
AGP 4X CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM	AD22		PIRQC/PIRQD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

PIR

REV 0.2

Date	Page	Description
5/8	29	Modification toshiba SM+SD function
5/8	32	Modification audio volume control function
5/8	42	ADD system thermal protection
5/14	33	DEL R244 ,Add D44

REV 0.3

Date	Page	Description
5/23	5	**U8 Vcc plane modifty to +5VALW**
5/23	**18**	**DEL R90,R89,R281**
5/23	32	R448 change gnd to +5VCD, R479 change +5VCD to gnd.
5/23	37	U2.4 link to U20.8
5/23	30	Add R519.
5/23	5	U9.AF19 add R517 link to +1.5VS
5/23	25	Modifty LPC_RST# timing. Add U55,D45,R518.
5/31	27	JP15.8 connector to U29.57
5/31	25	ADD R520, Add net name BT_DET# to U29.57
5/31	34	Modifty net name ANT_SW to WL_OFF#, ADD R221
5/31	28	Modifty net name RFOFF# to WL_OFF#
5/31	35	DEL R19

REV 0.4

Date	Page	Description
7/3	16	Del L23,R14,R12,R10,R6,R8
7/3	27	ADD C720,C721,C722,C723,C724,C725
7/3	29	IDSEL0 change to PCI_AD26, INTA#/INTB# change to PIRQC#/PIRQD#
7/10	24	Add U58,U59,R531,R532,R533,R534,C718,C719
7/17	29	Del SD function
7/18	29	Change IDSEL to PCI_AD22
7/23	21	DEL C15

REV 0.5

Date	Page	Description
8/13	15	Add R544 reserve for sus_stat# and stp_agp#
8/13	29	Add R545 pull-up signal SM_LED to SMC_VCC,Add@ in U62,C729,R486
8/13	35	Change R543 pull-up form SMC_VCC to +5VS
8/13	29	Add R546,R547 signal PCIRST#,CBRST#
8/13	37	Del U2,Q4,R330
8/16	10	Add Signal TV_out_DDC2CCLK,TV_out_DDC2DATA ,VCH_I2CCLK,VCH_I2CDATA,AGP_DDCCLK,AGP_DDCDATA
8/16	10	Add R551.R552. DEL R225,R235
8/16	15	Add RP38,RP39
8/16	16	Add R553,R554,R555
8/17	34	Del R29, Add R557, R558
8/17	20	Add R556

REV 1.0

Date	Page	Description
8/31	5	Q6 RESERVE

REV 1.A

Date	Page	Description
9/6	12	Add D47 and R562

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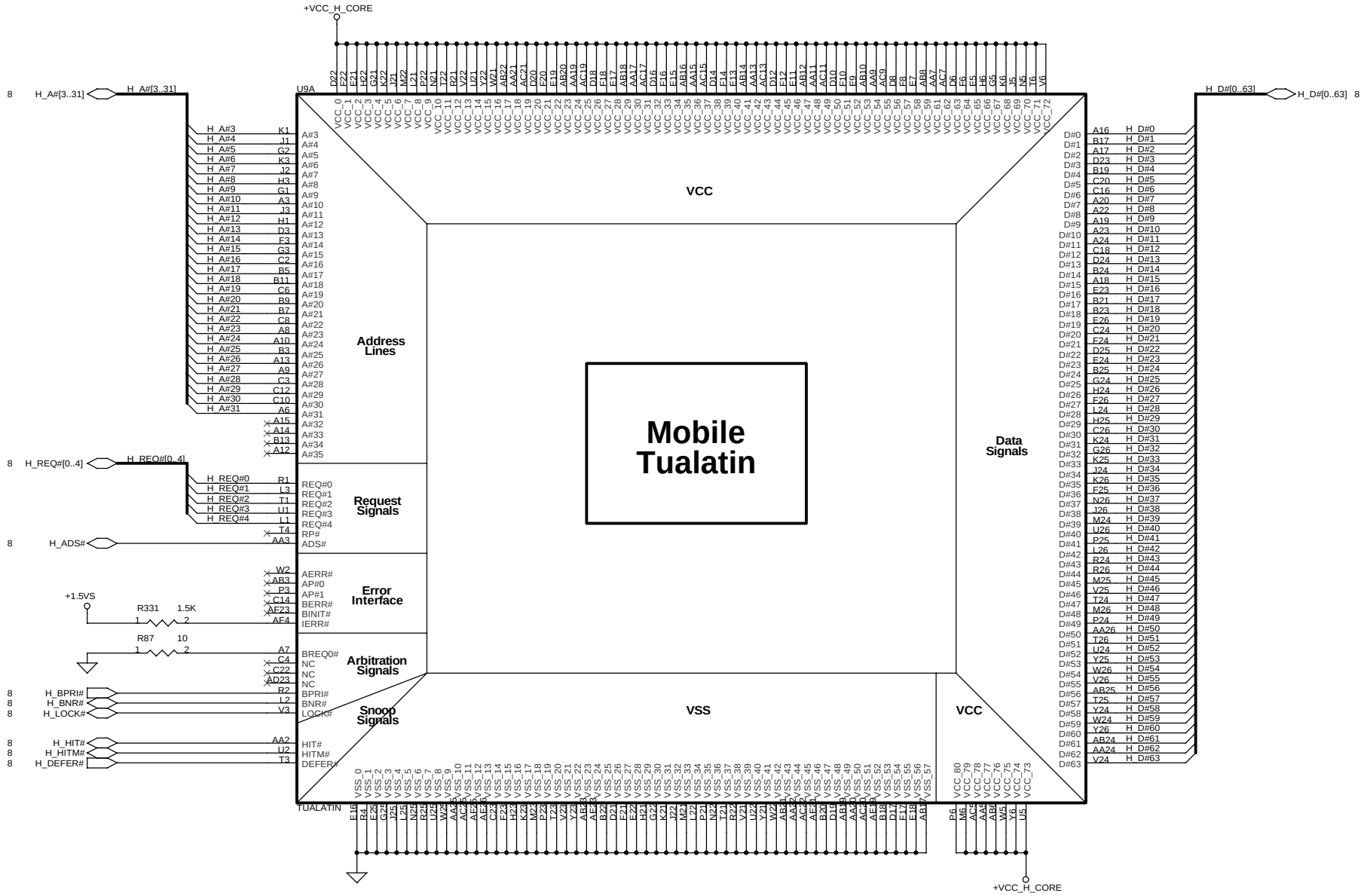

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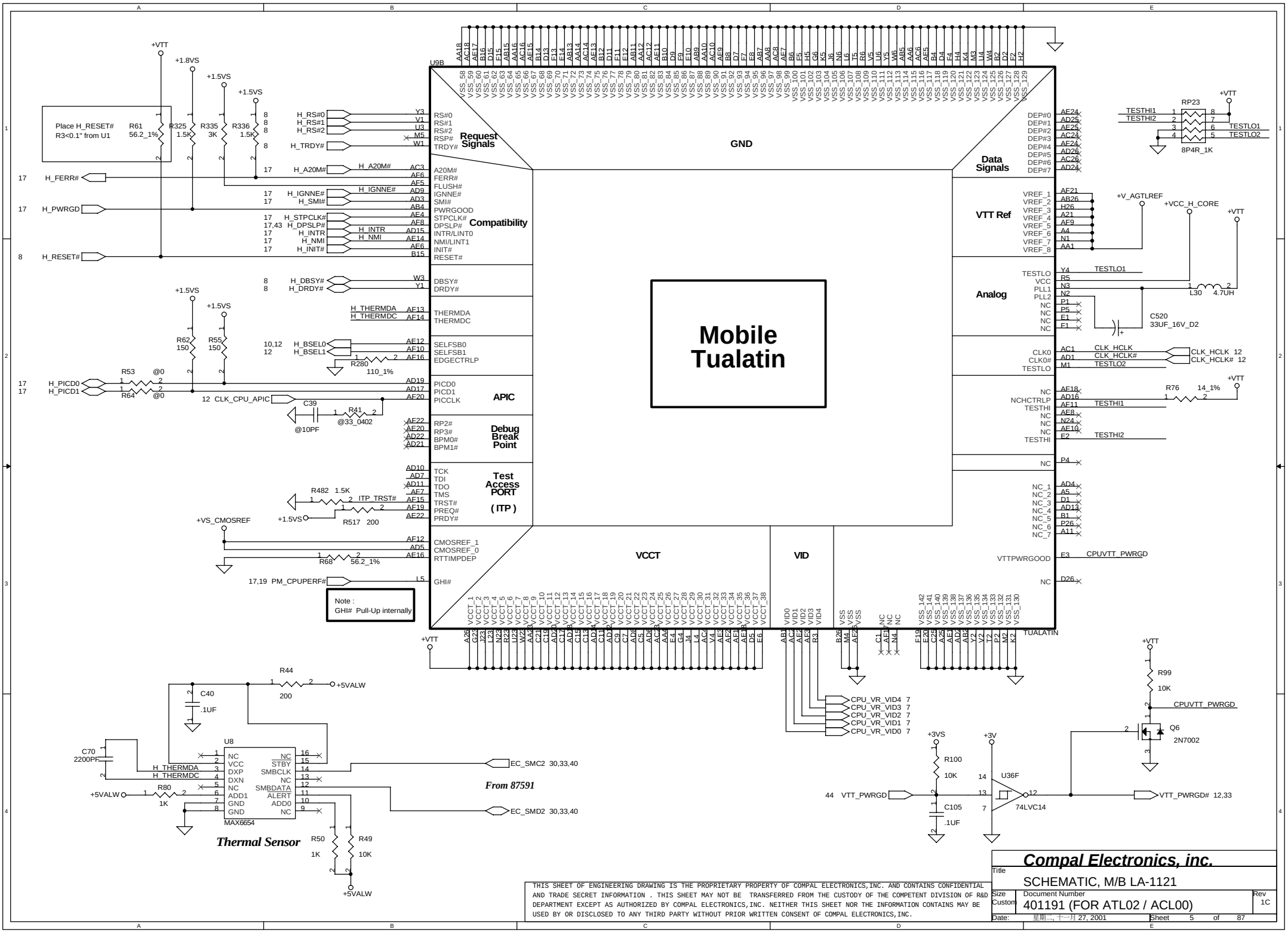

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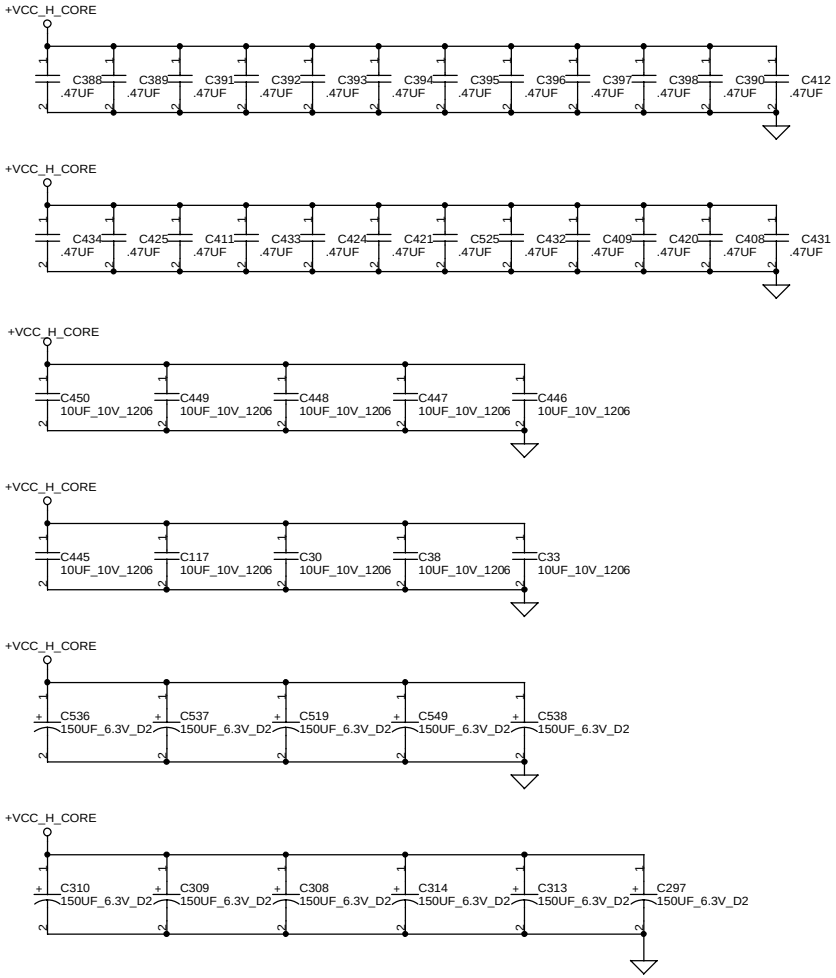
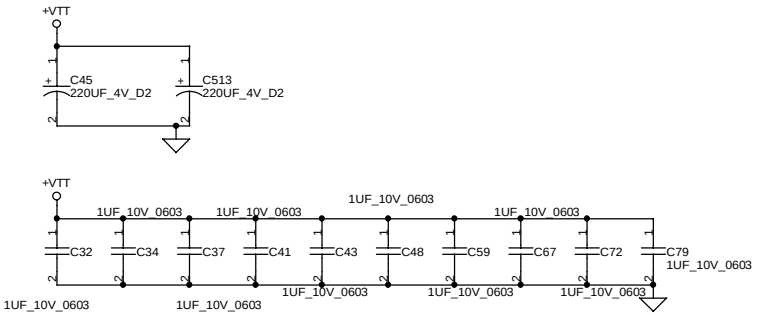
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.



Layout note :

Place close to CPU,
Use 2 vias per PAD.



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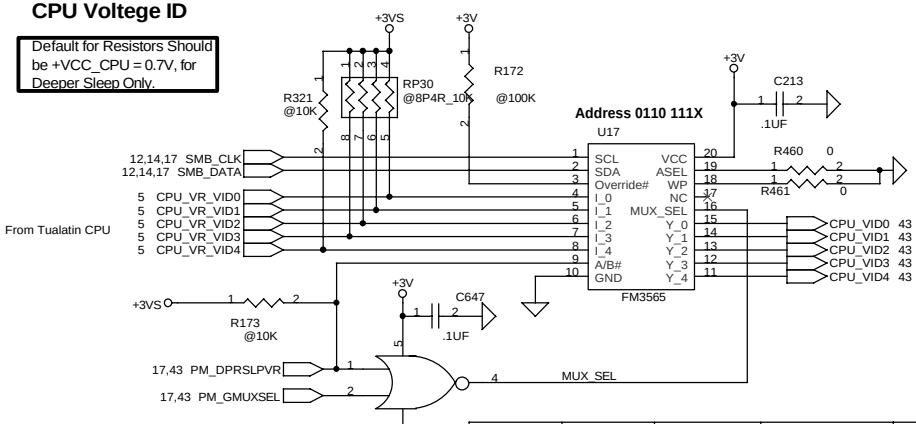
CPU Voltege ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1: for Deeper Sleep mode
0 : for Performance mode

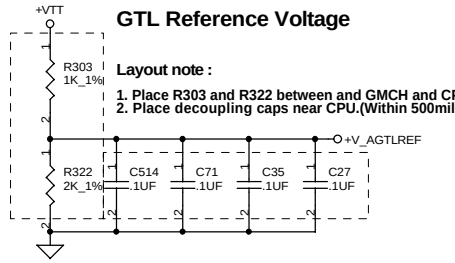
Override#	MUX_SEL	A/B#	MUX_outputs	Mode
1	1	X	MUX_inputs	Battery
1	0	0	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

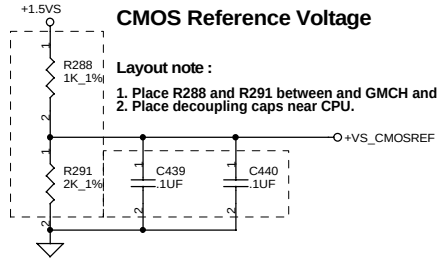
GTL Reference Voltage



Layout note :

1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)

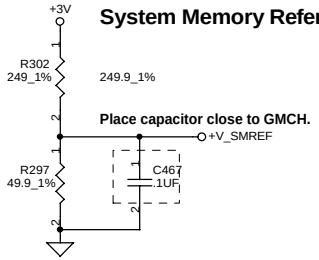
CMOS Reference Voltage



Layout note :

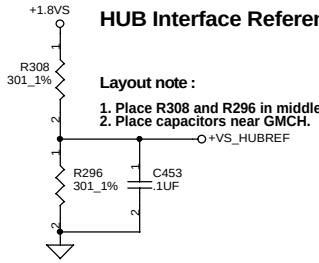
1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.

System Memory Reference



Place capacitor close to GMCH.

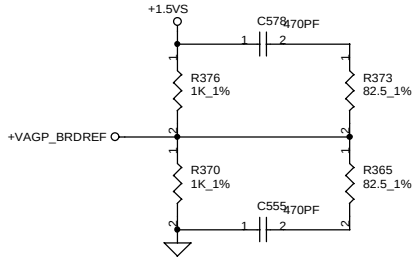
HUB Interface Reference



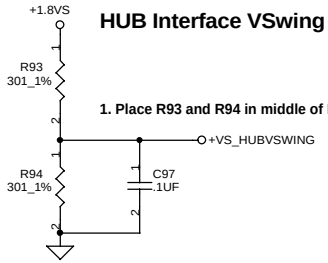
Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

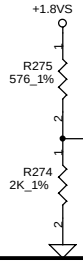
Place Reference Circuit near GMCH



HUB Interface VSwing Voltage



1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.

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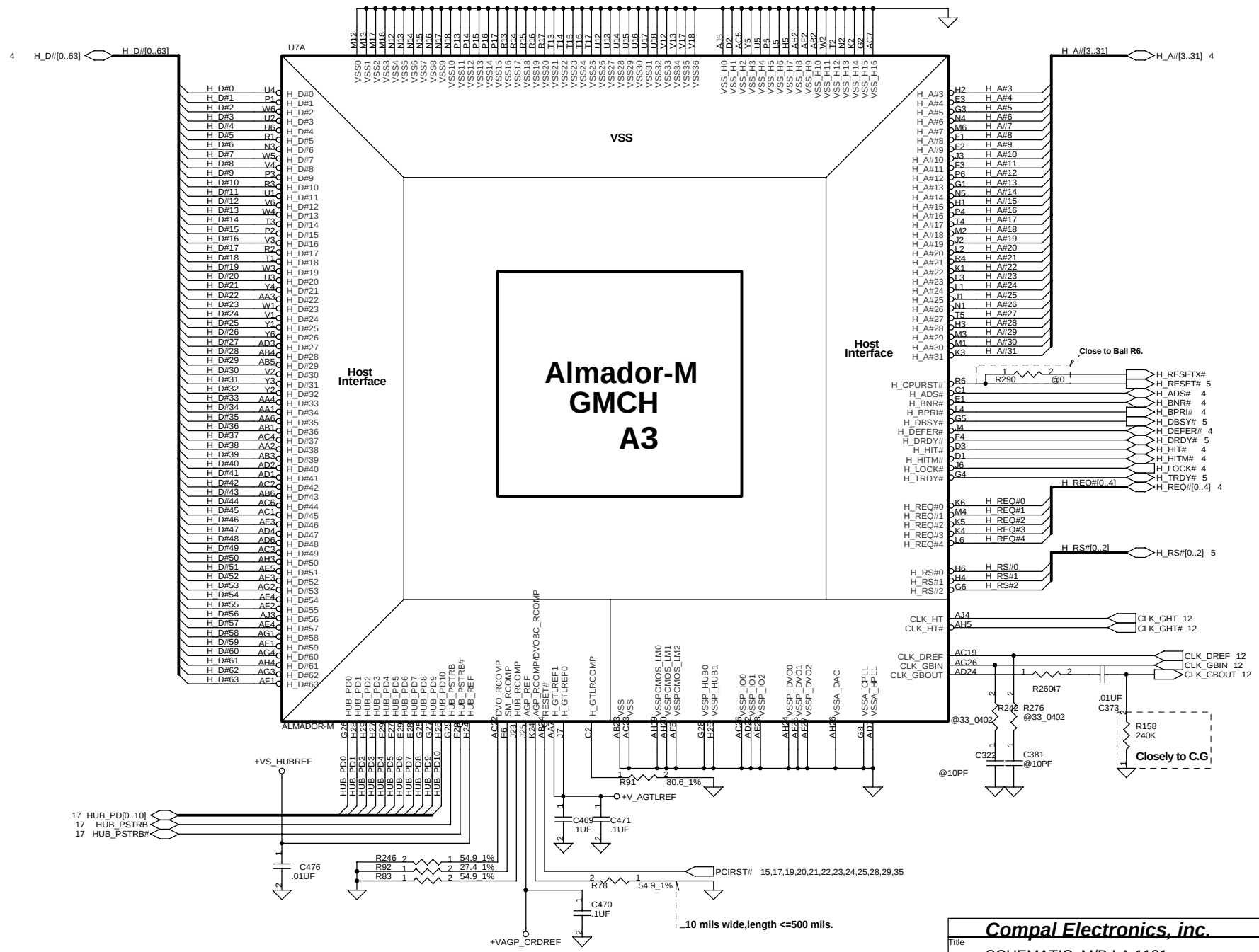

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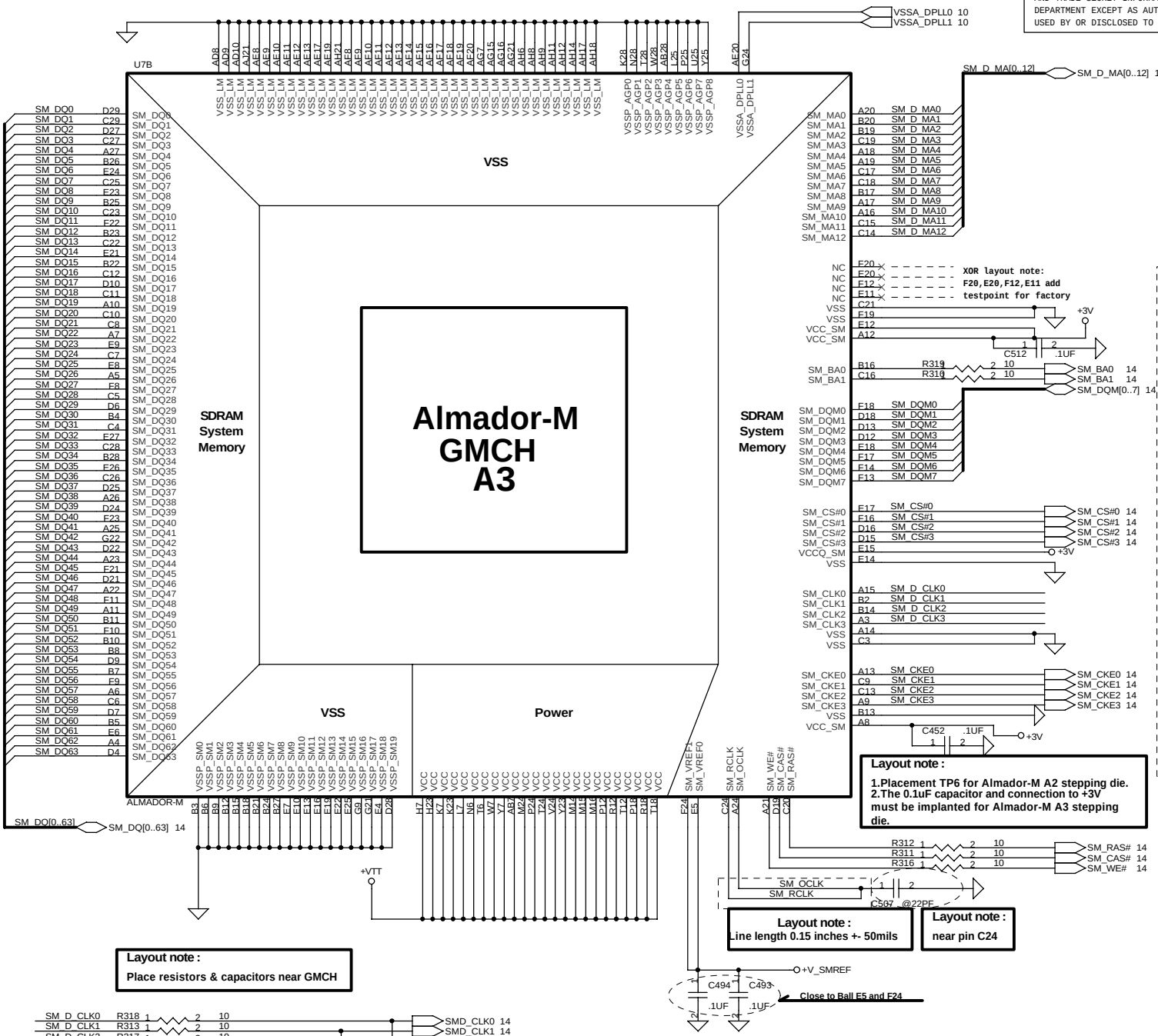

For Almador-M A3 stepping requirement.

The table below provides a summary of the ballout changes to the Almador-M chip

Table 4-1 Ballout Changes

Ball#	New Signal Name	Old Signal Name
A8	VCC_SM	SM_CKE5
A12	VCC_SM	SM_ECC7
E12	VCC_SM	SM_ECC6
G10	VCC_SM	VCCQ_SM
F7	VCCQ_SM	VCC_SM
G19	VCCQ_SM	VCC_SM
E15	VCCQ_SM	SM_CS4
F15	VCCQ_SM	VCC_SM
A14	VSS	SM_CLK4
B13	VSS	SM_CKE4
C3	VSS	SM_CLK5
C21	VSS	SM_ECC4
E14	VSS	SM_CS5
F19	VSS	SM_ECC5
E11	NC	SM_ECC3
E20	NC	SM_ECC1
F12	NC	SM_ECC2
F20	NC	SM_ECC0

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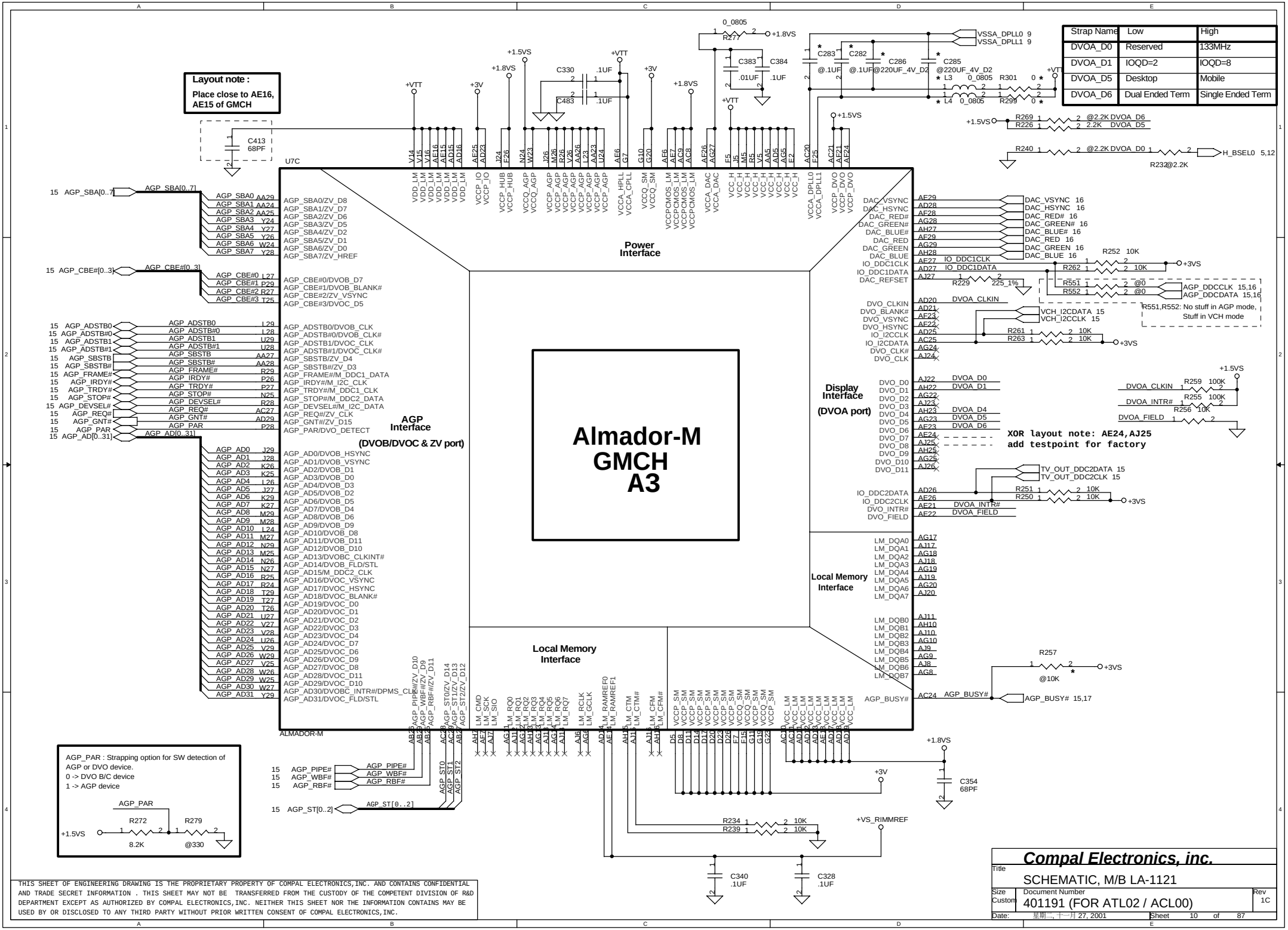

Strap Name	Low	High
DVOA_D0	Reserved	133MHz
DVOA_D1	IOQD=2	IOQD=8
DVOA_D5	Desktop	Mobile
DVOA_D6	Dual Ended Term	Single Ended Term

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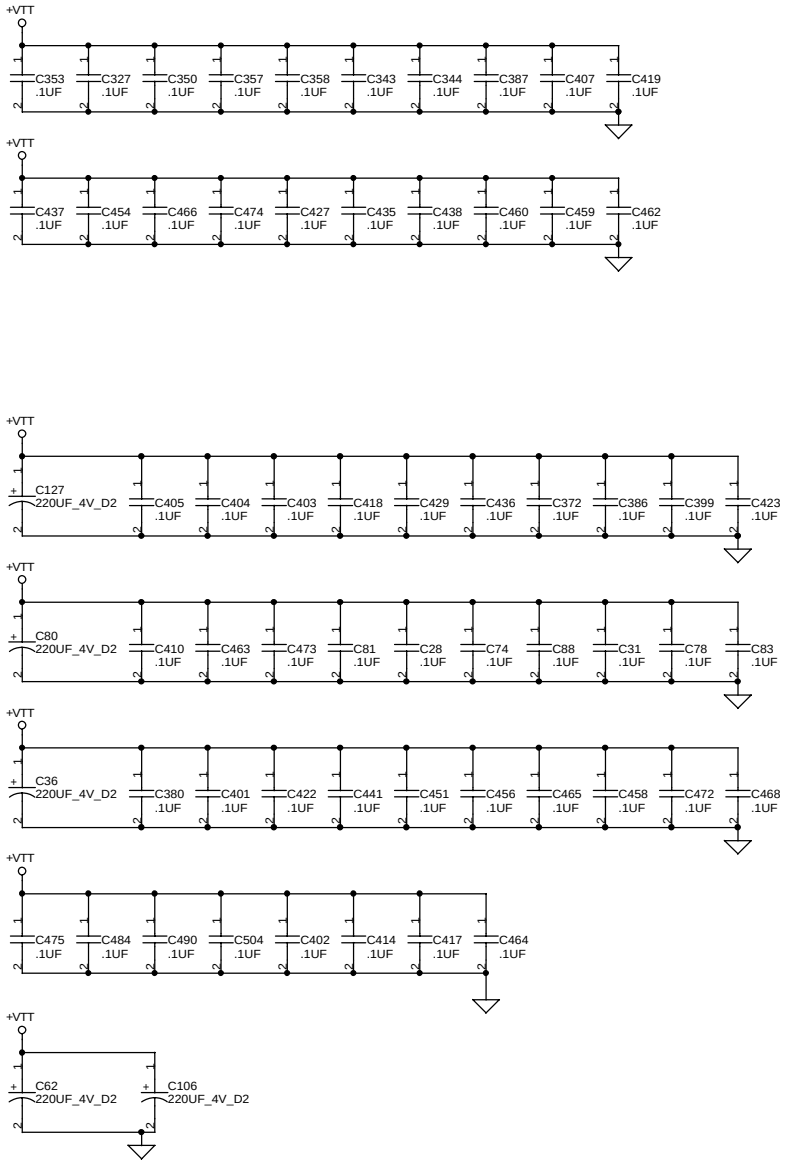
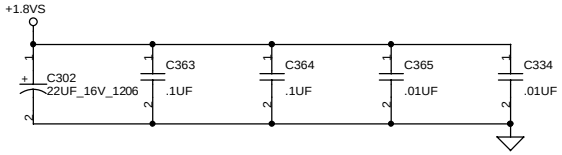
Layout note :

Distribute as close as possible to GMCH Processor Quadrant .



Layout note :

Distribute as close as possible to VCCPCMOS_LM .



Layout note :

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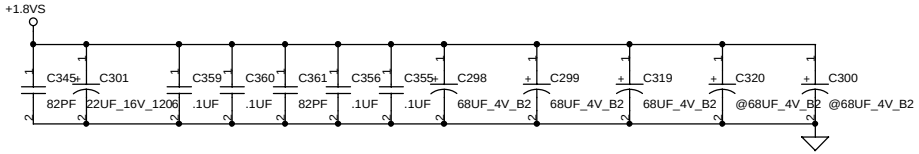
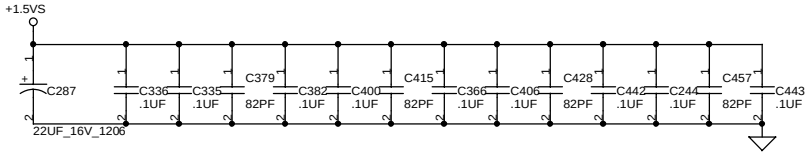


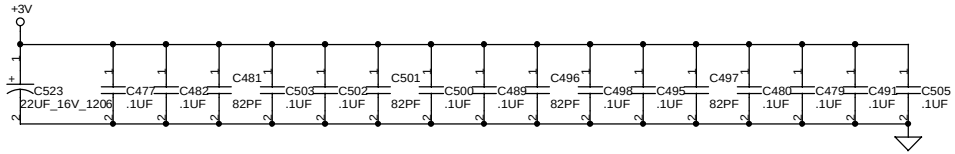
Layout note :

Distribute as close as possible to GMCH AGP/DVO Quadrant .



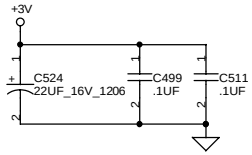
Layout note :

Distribute as close as possible to GMCH System Memory Quadrant .



Layout note :

Distribute as close as possible to IO Quadrant .



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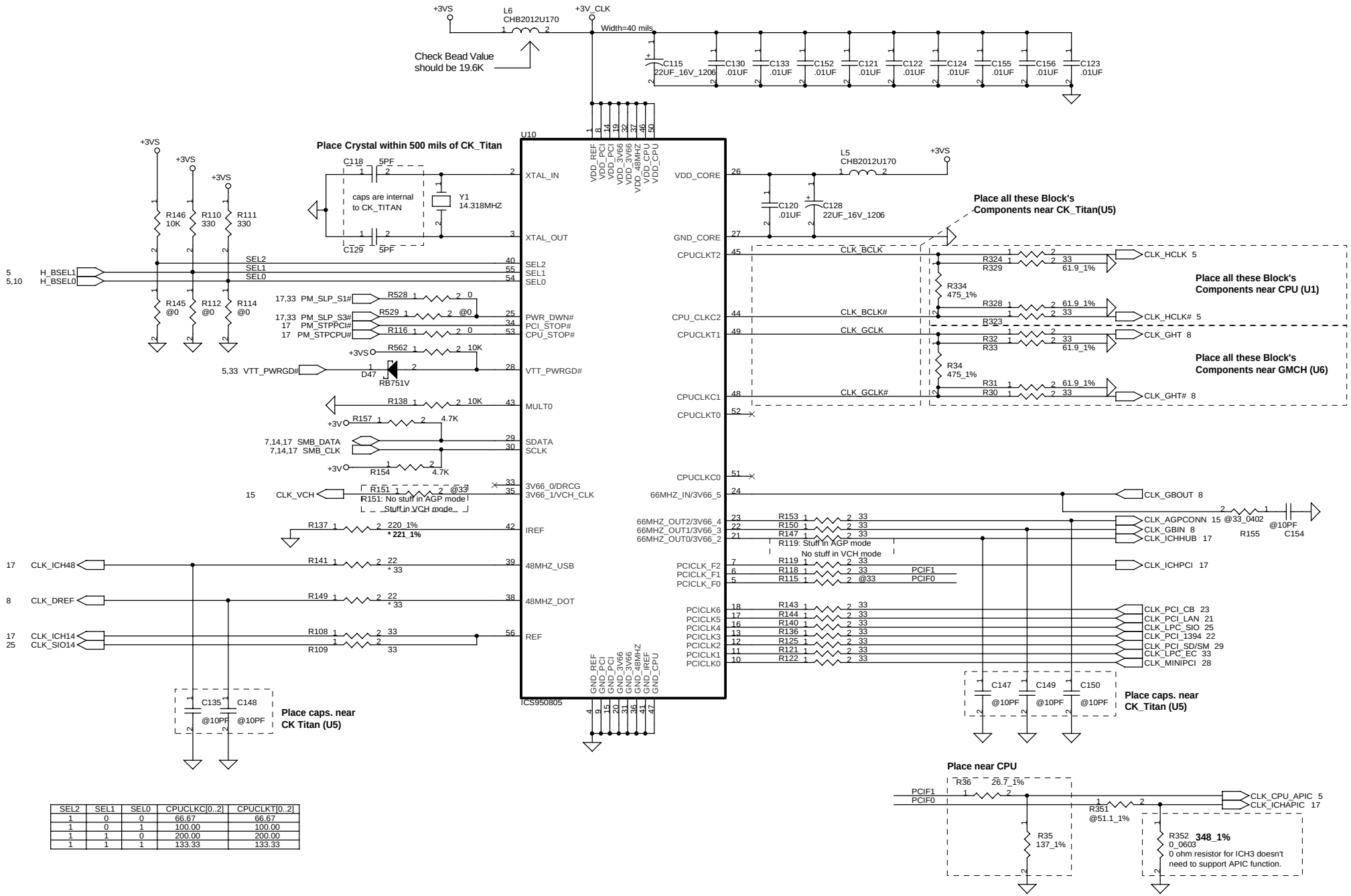

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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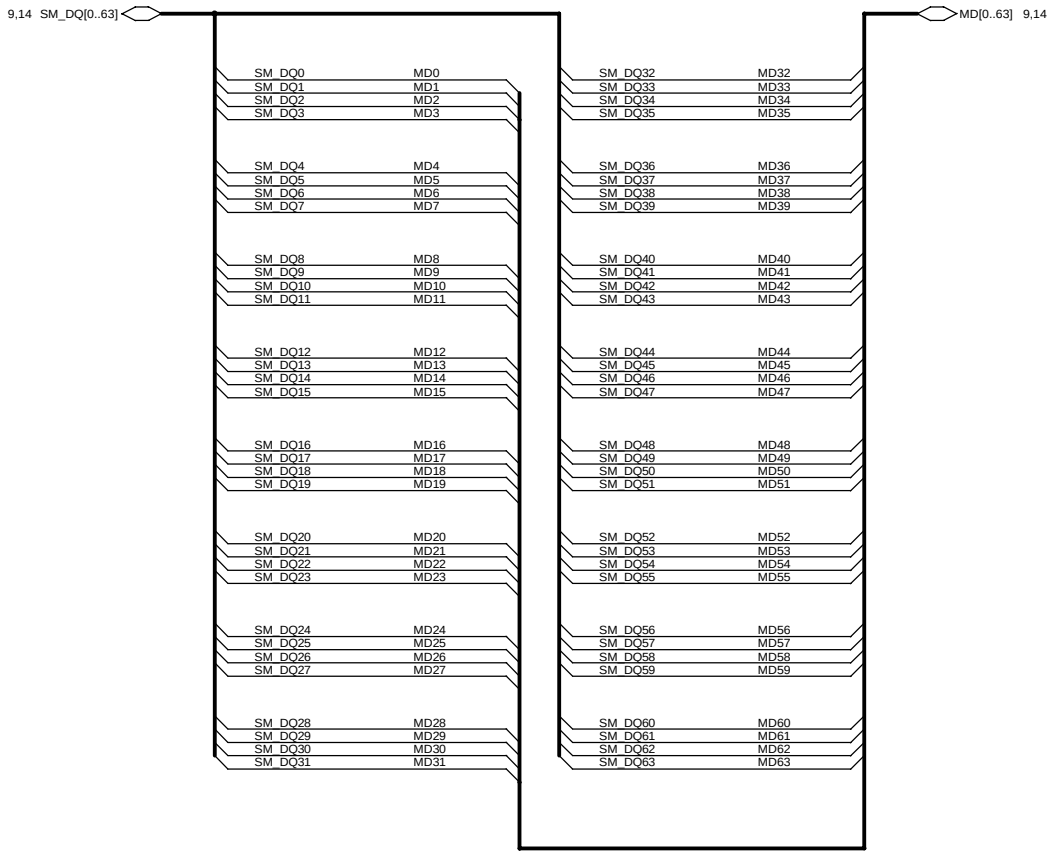
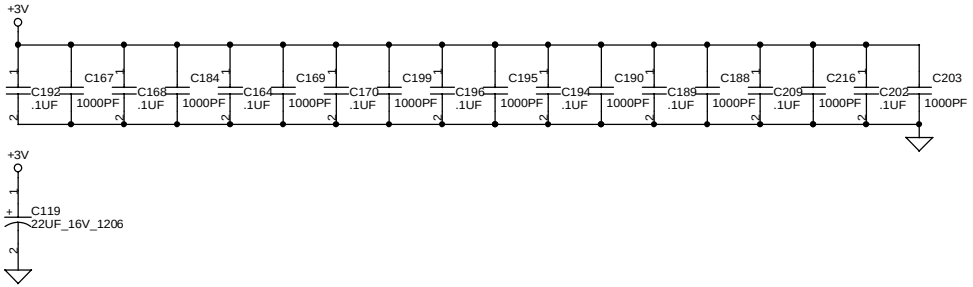


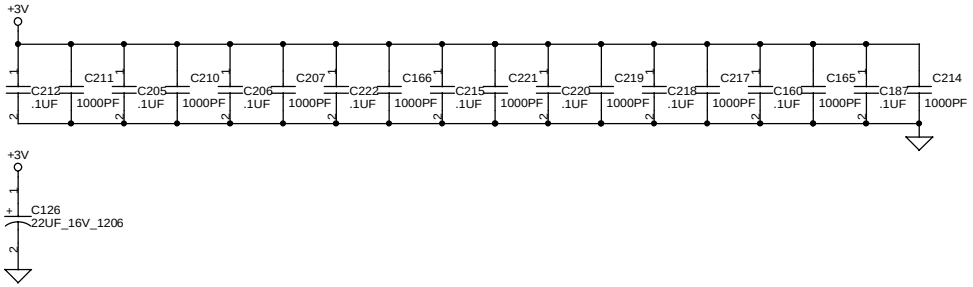
Layout note :

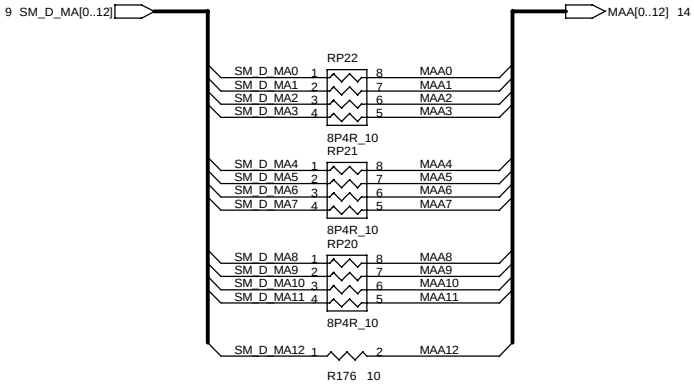
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :

One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .





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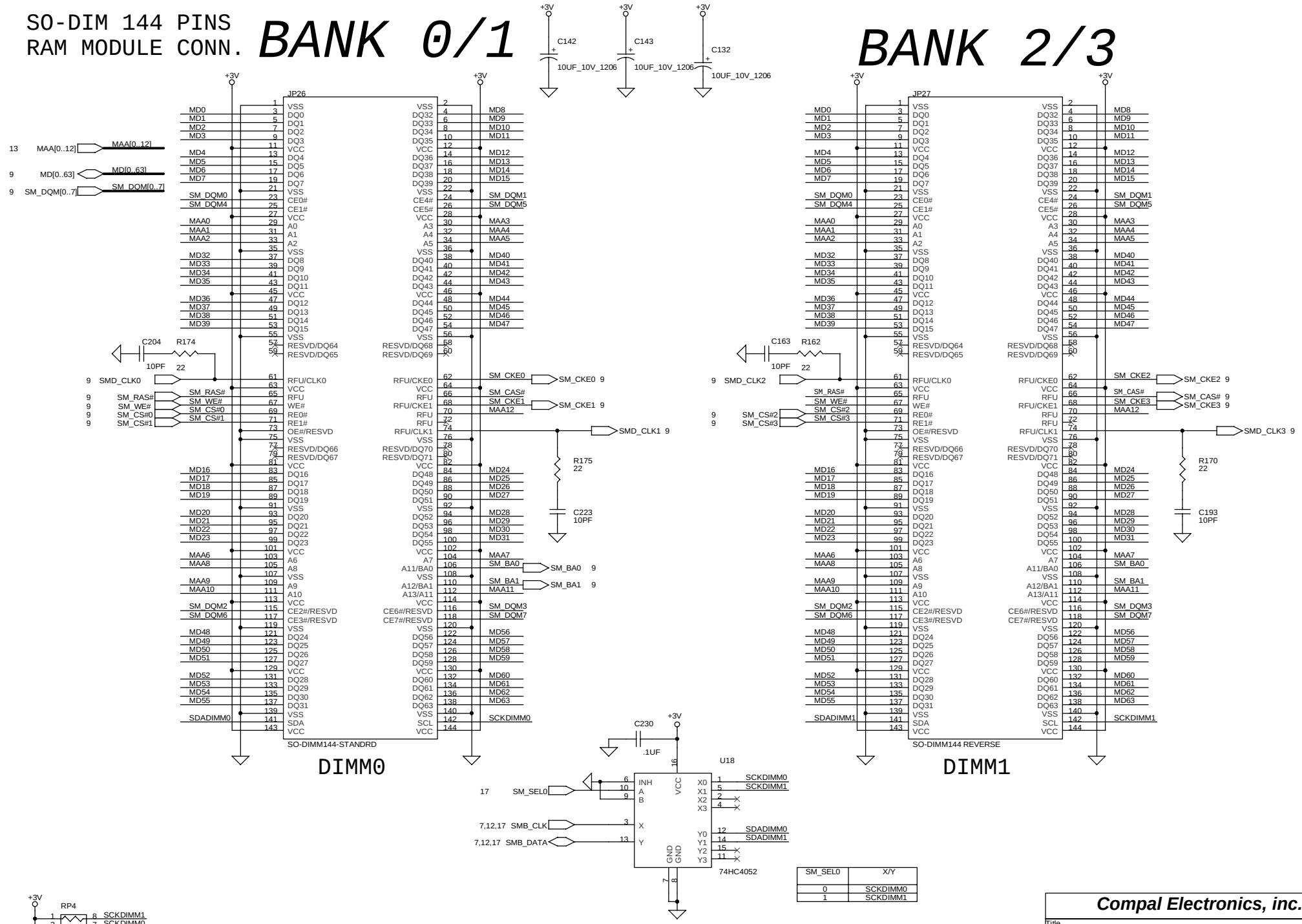
SO-DIM 144 PINS RAM MODULE CONN.



SM_SEL0	X/Y
0	SCKDIMM0
1	SCKDIMM1

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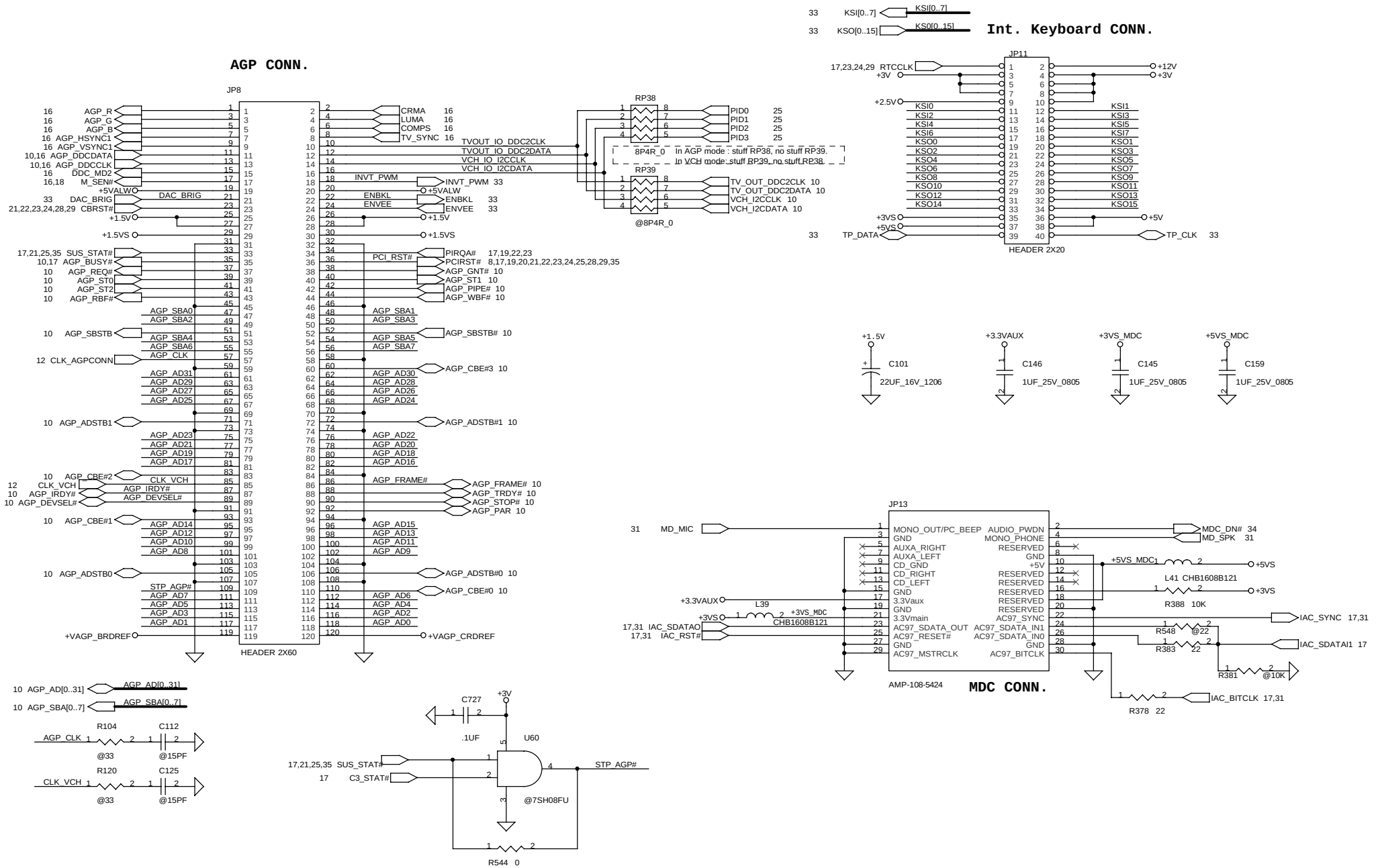

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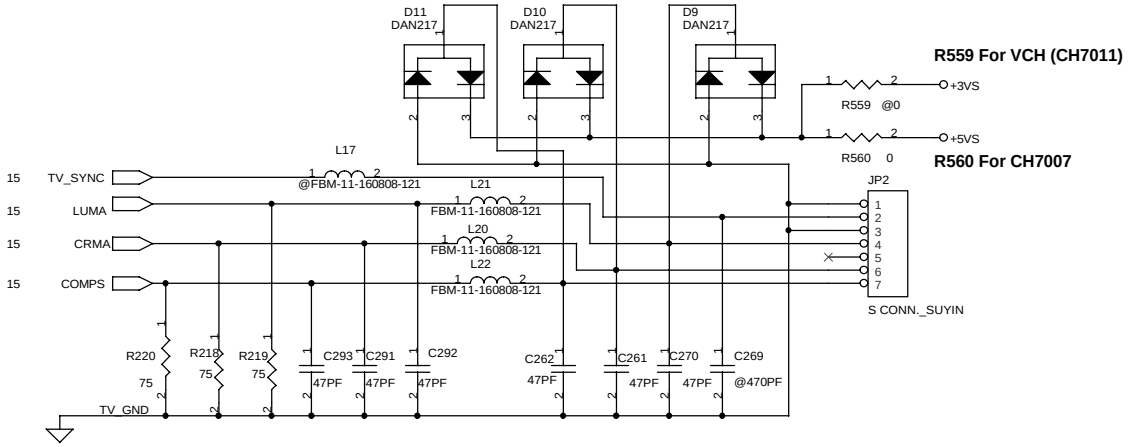
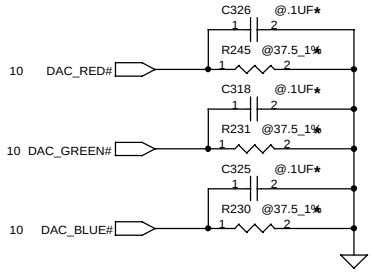
TV_OUT CONN.



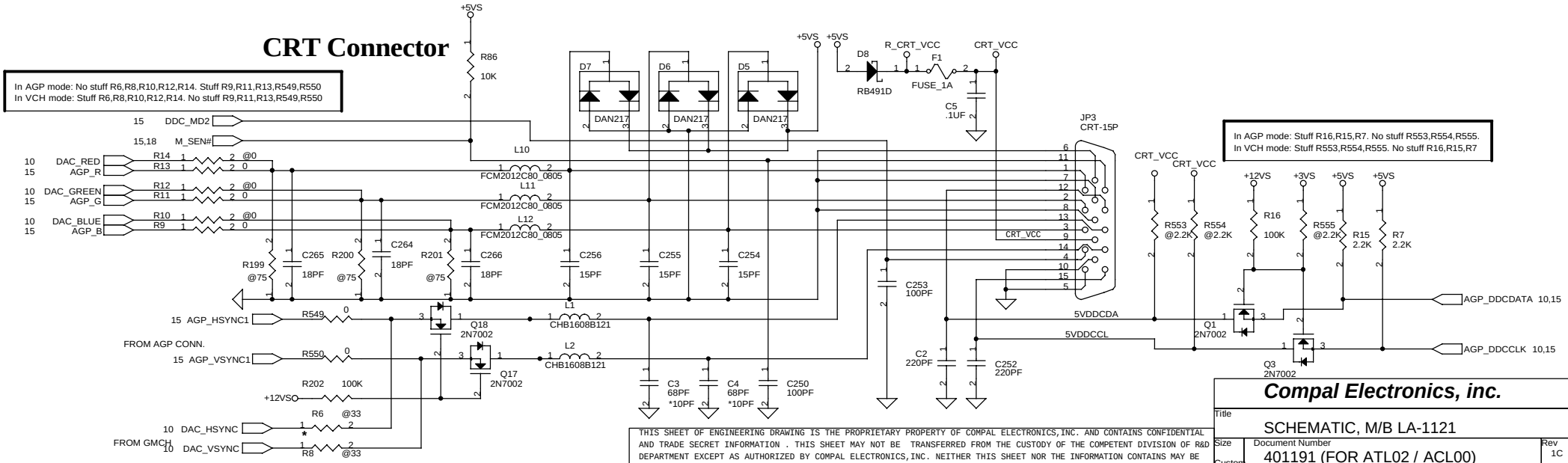
In AGP mode: No stuff C326,R245,C318,R231,C325,R230.
In VCH mode: Stuff C326,R245,C318,R231,C325,R230



CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550

In AGP mode: Stuff R16,R15,R7. No stuff R553,R554,R555.
In VCH mode: Stuff R553,R554,R555. No stuff R16,R15,R7



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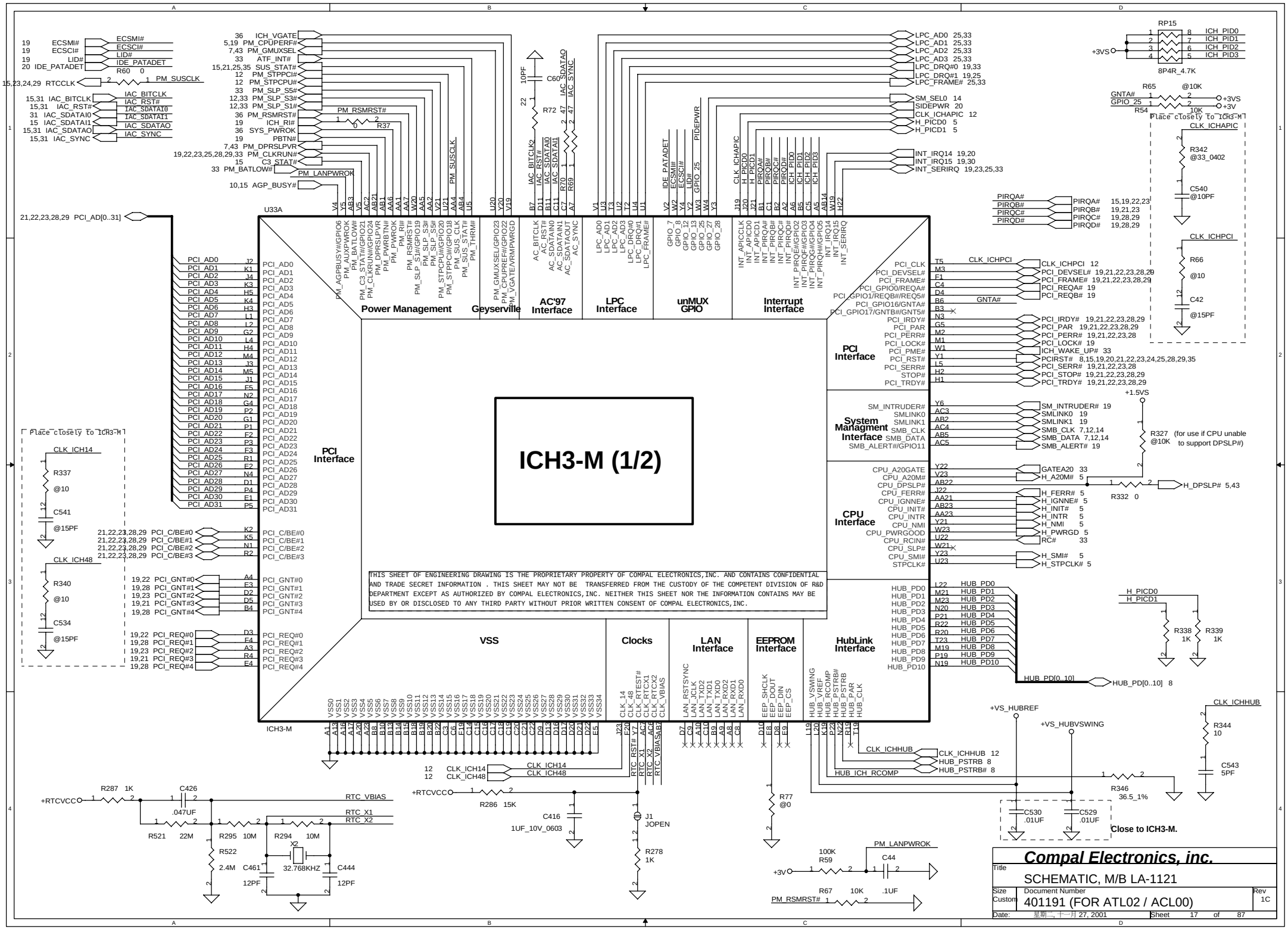
ICH3-M (1/2)
U33A
Power Management
Geyserville
AC'97 Interface
LPC Interface
unMUX GPIO
Interrupt Interface
PCI Interface
System Managment Interface
CPU Interface
VSS
Clocks
LAN Interface
EEPROM Interface
HubLink Interface
ICH3-M
Place closely to ICH3-M
Close to ICH3-M.
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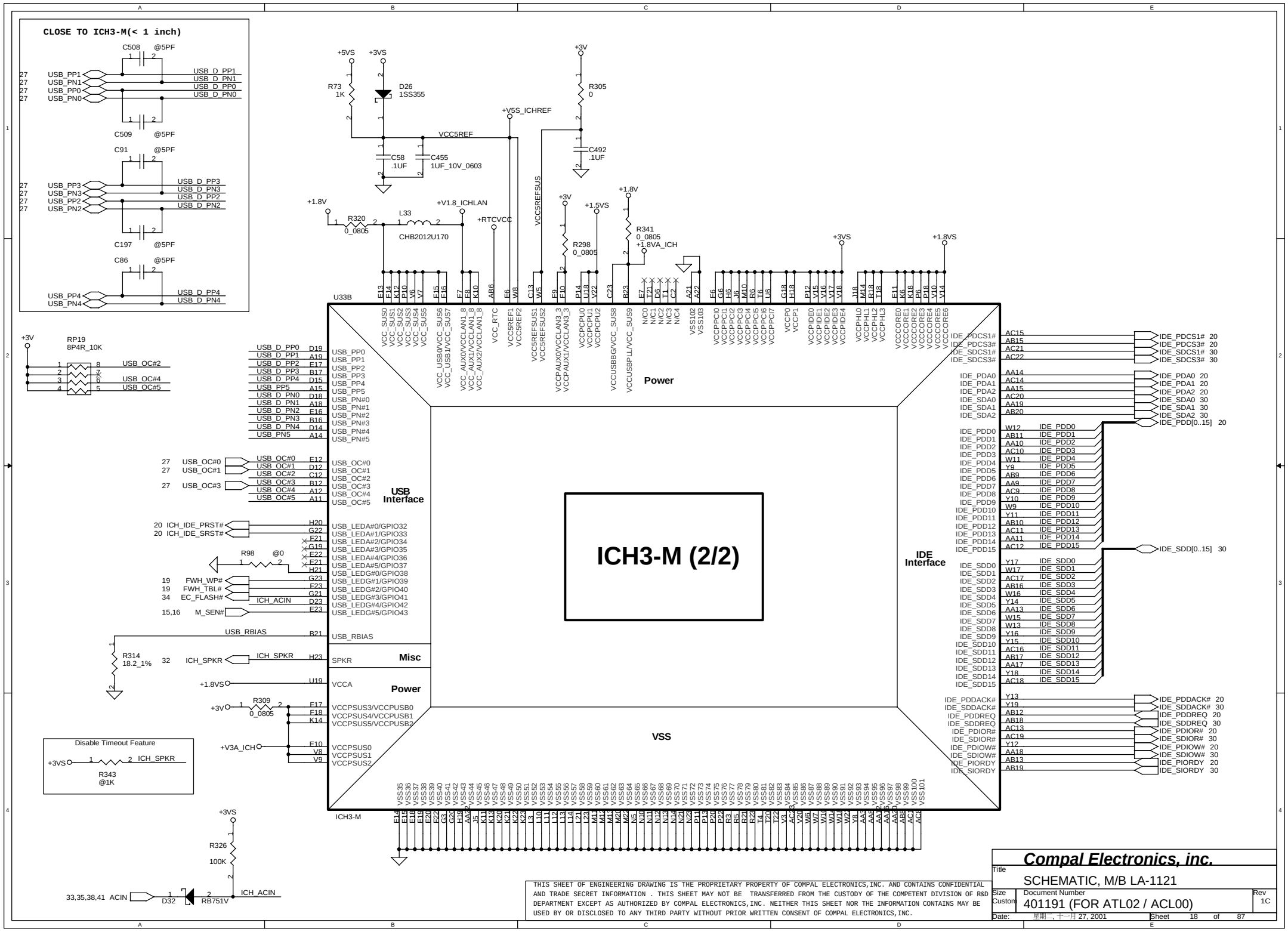

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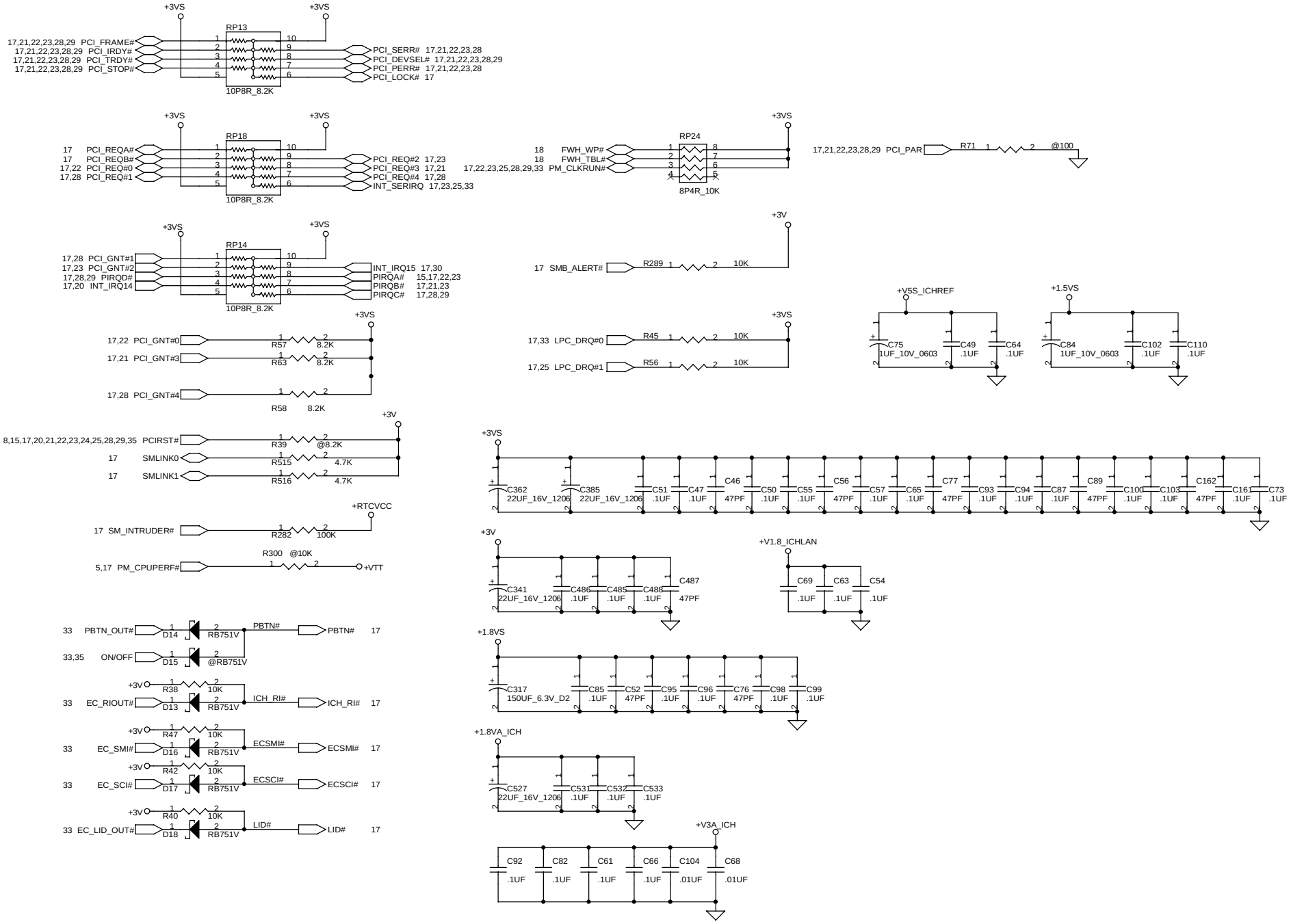

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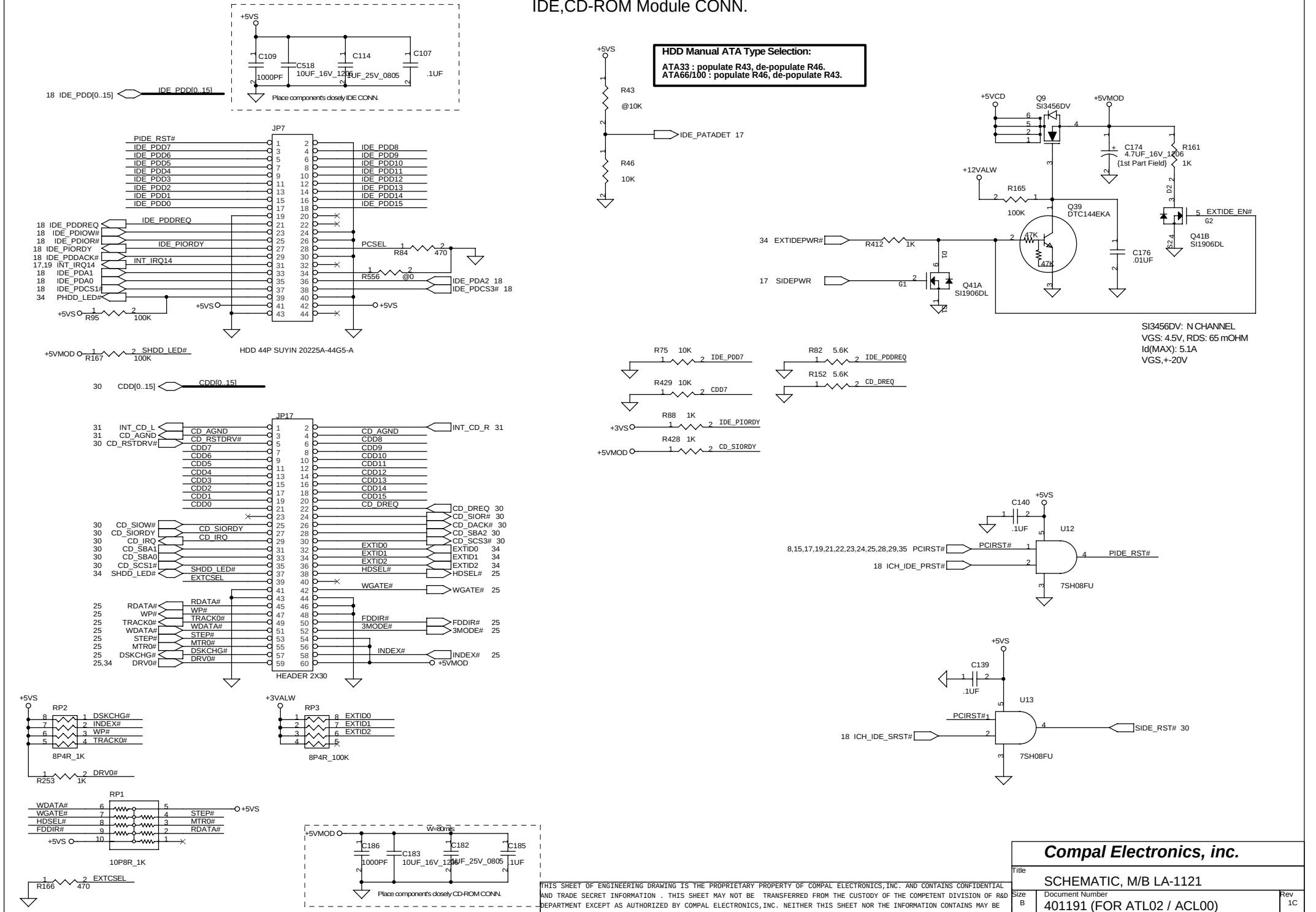
IDE,CD-ROM Module CONN.



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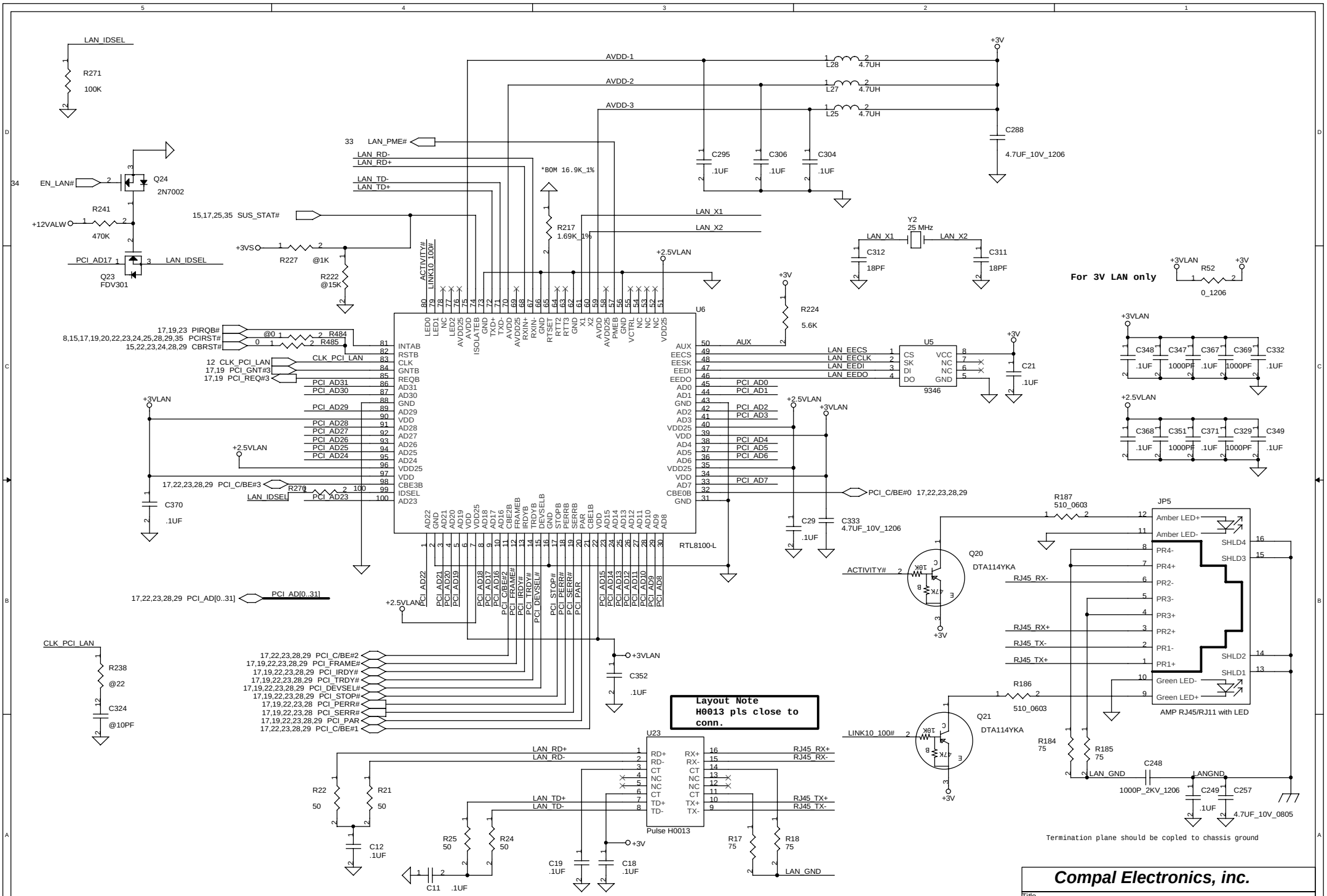

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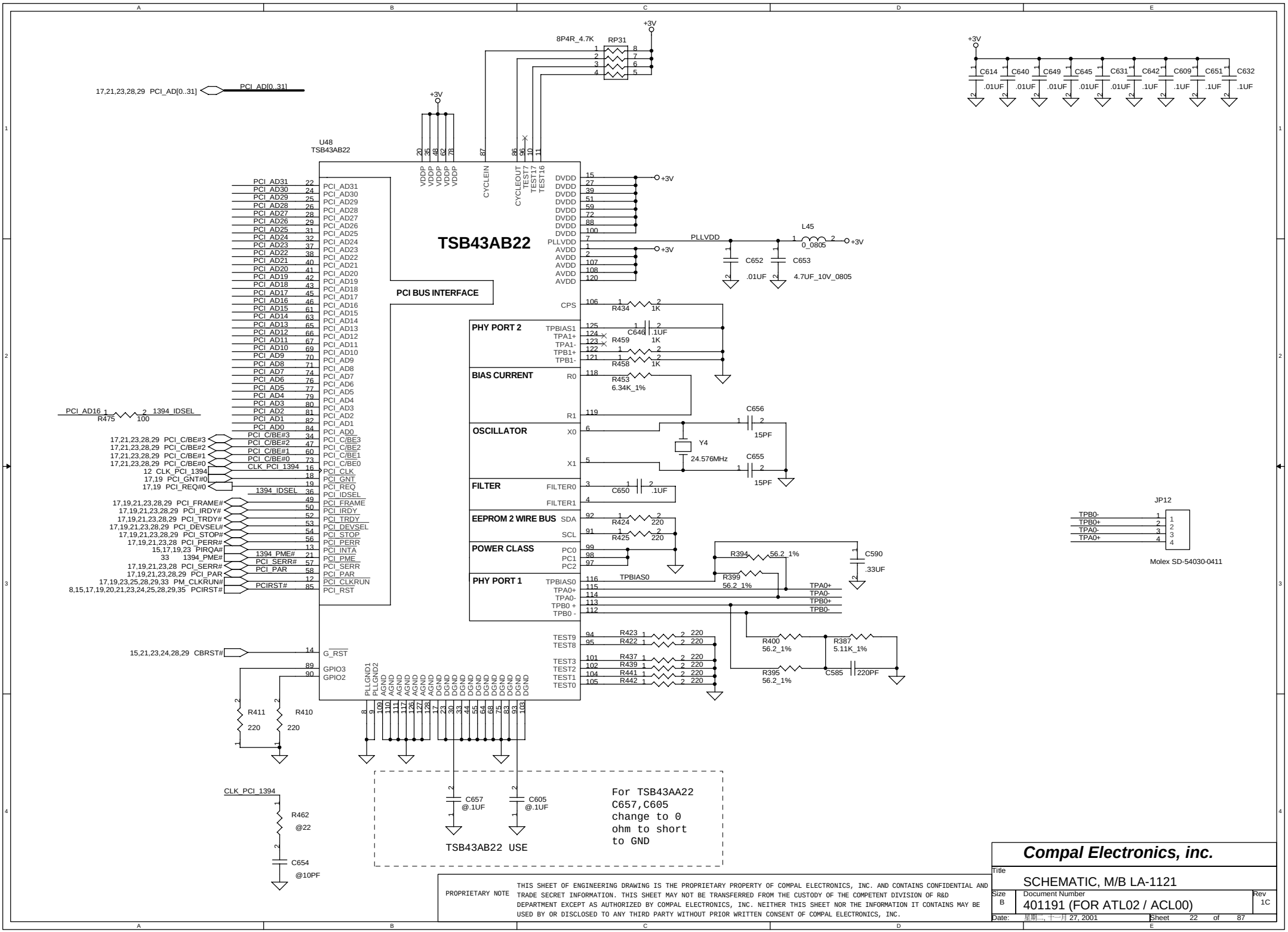

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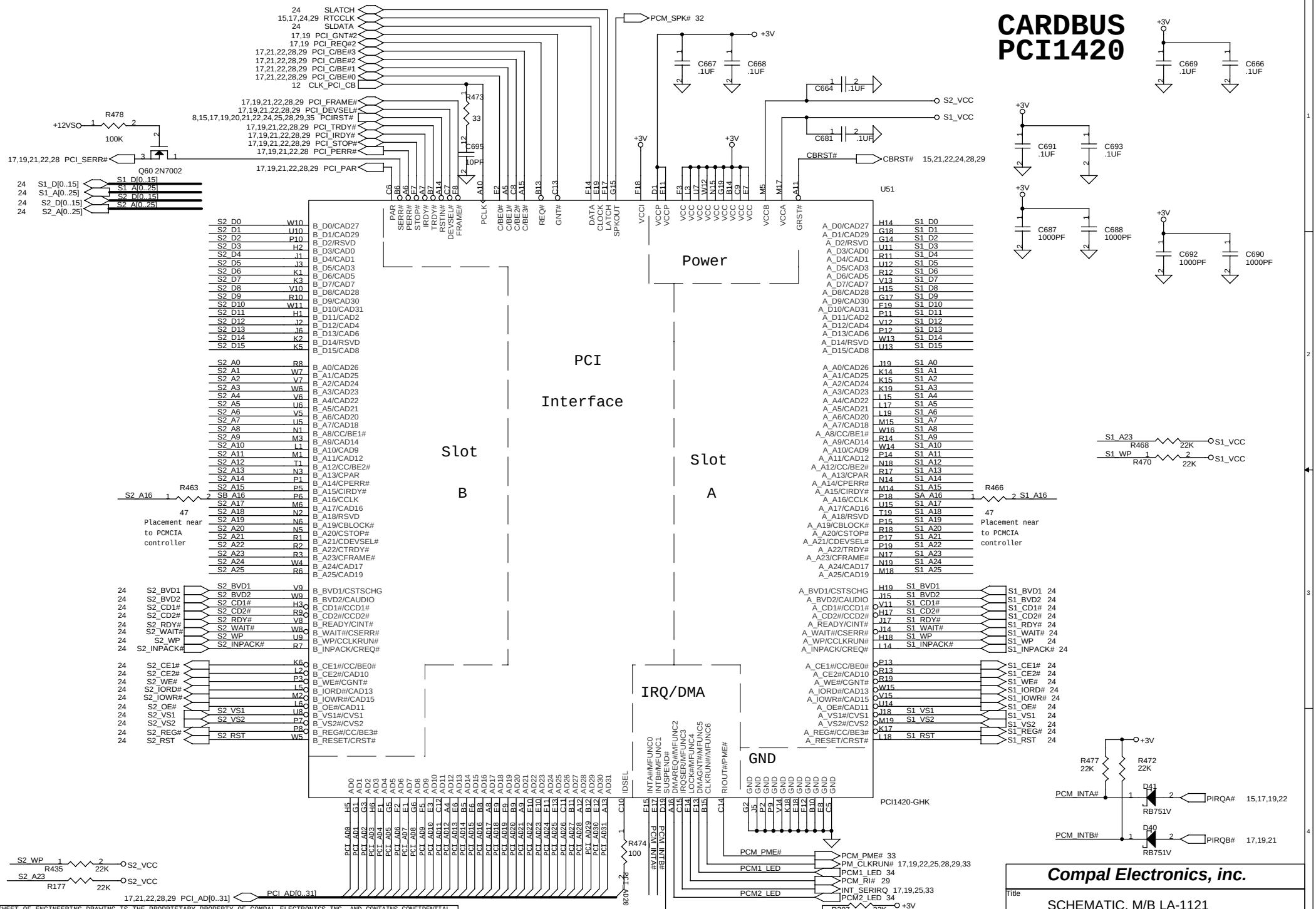
CARDBUS PCI1420



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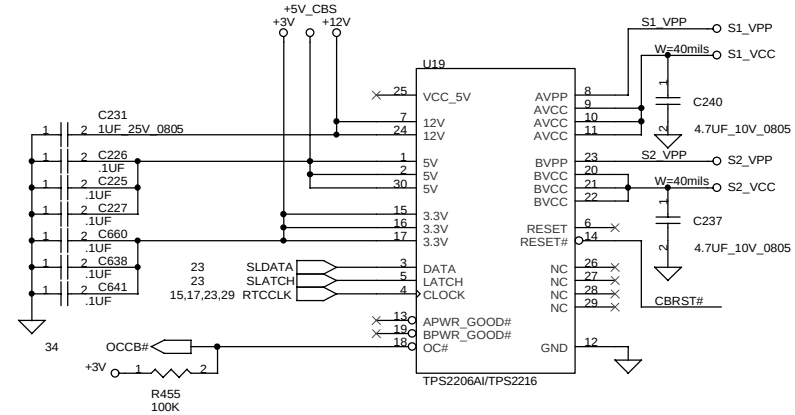
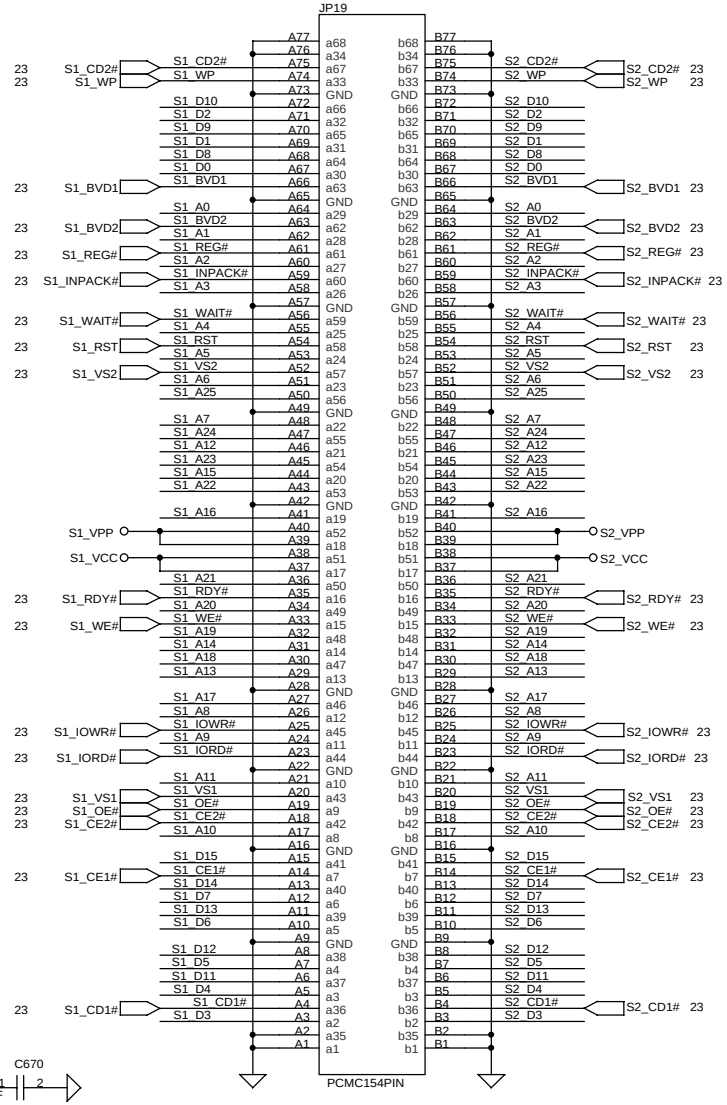
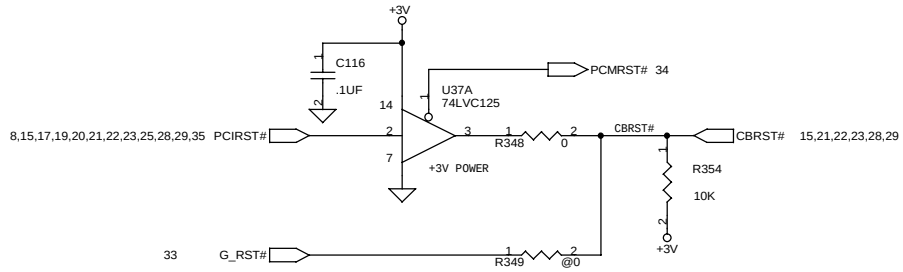
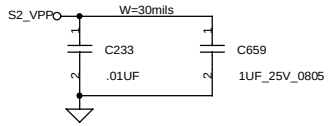
PCMCIA POWER CTRL.

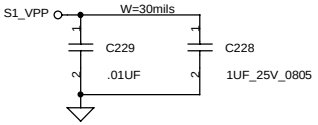


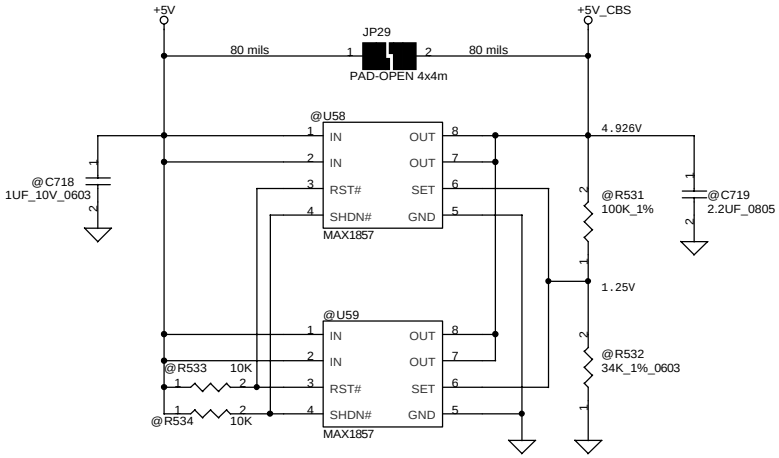
CARDBUS SOCKET

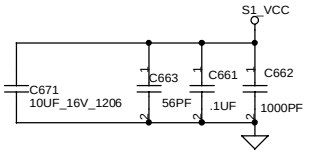


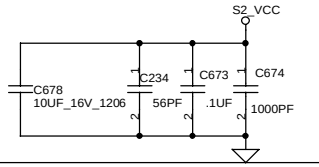












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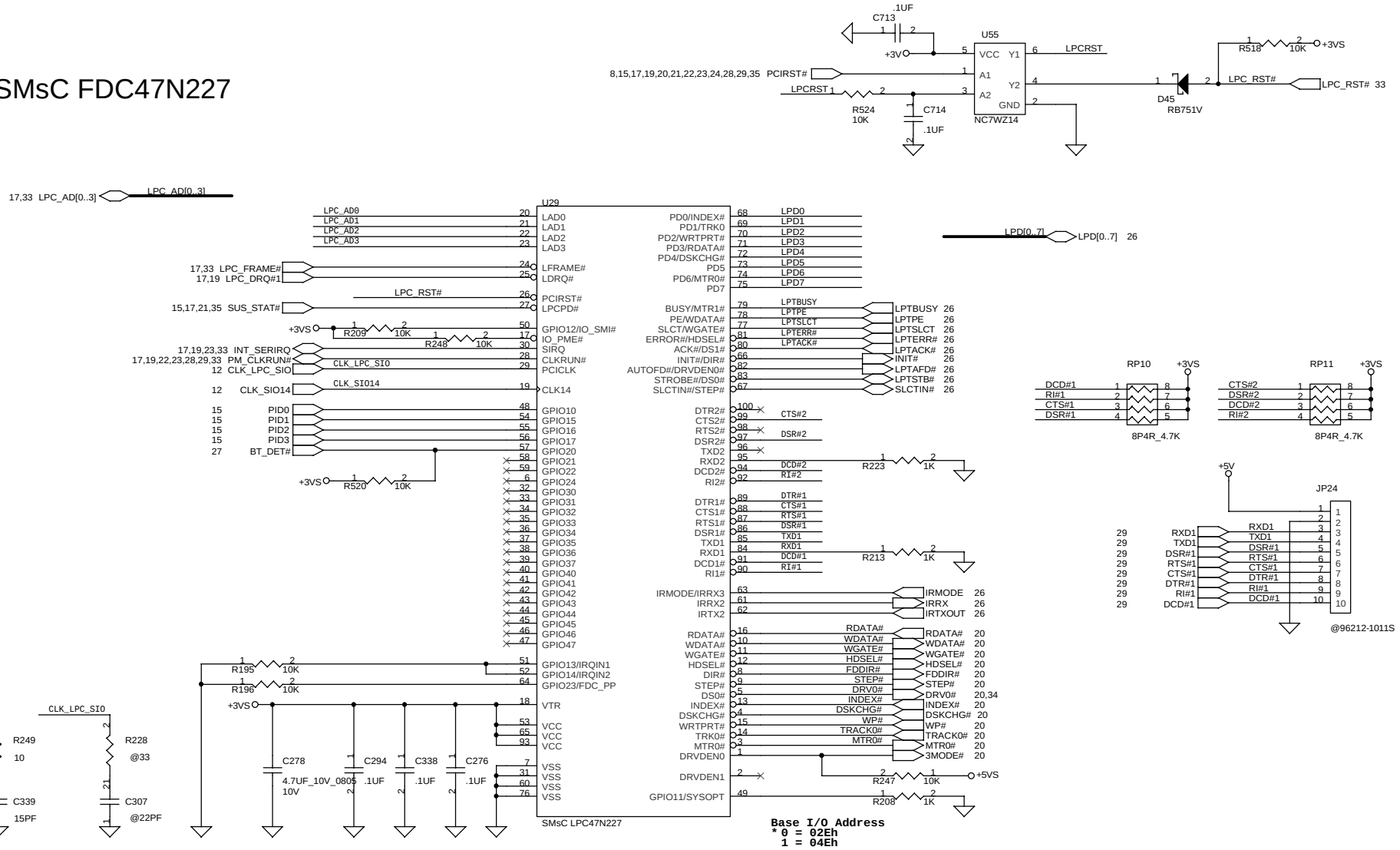
SUPER I/O SMsC FDC47N227



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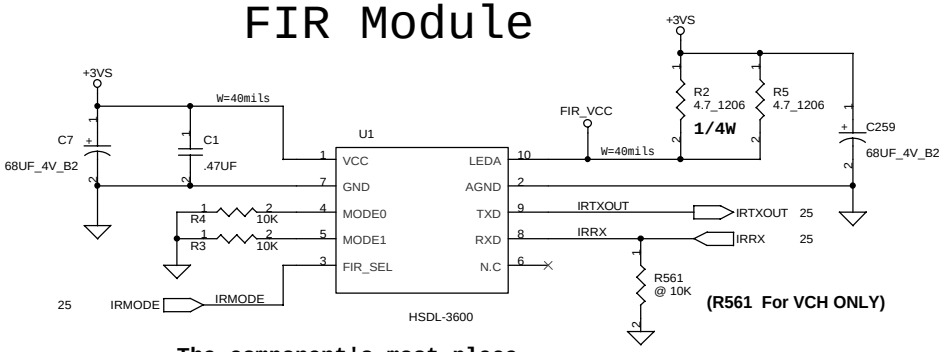
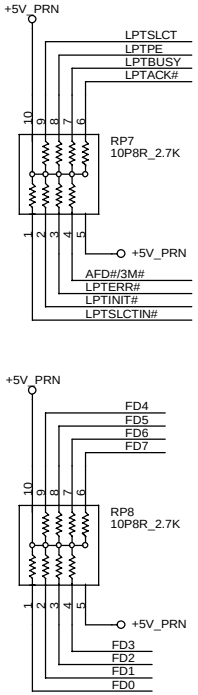
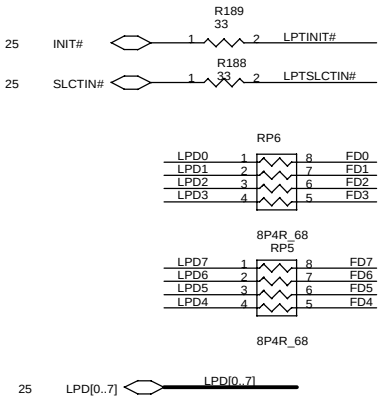
FIR Module

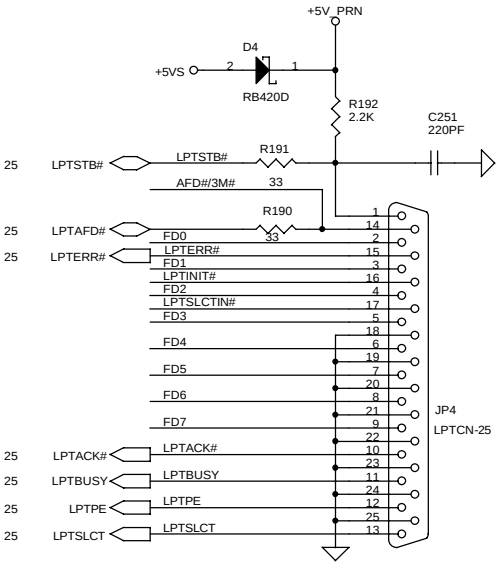


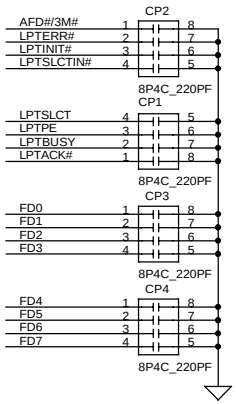
The component's most place cloely IRDA MODULE.

PARALLEL PORT









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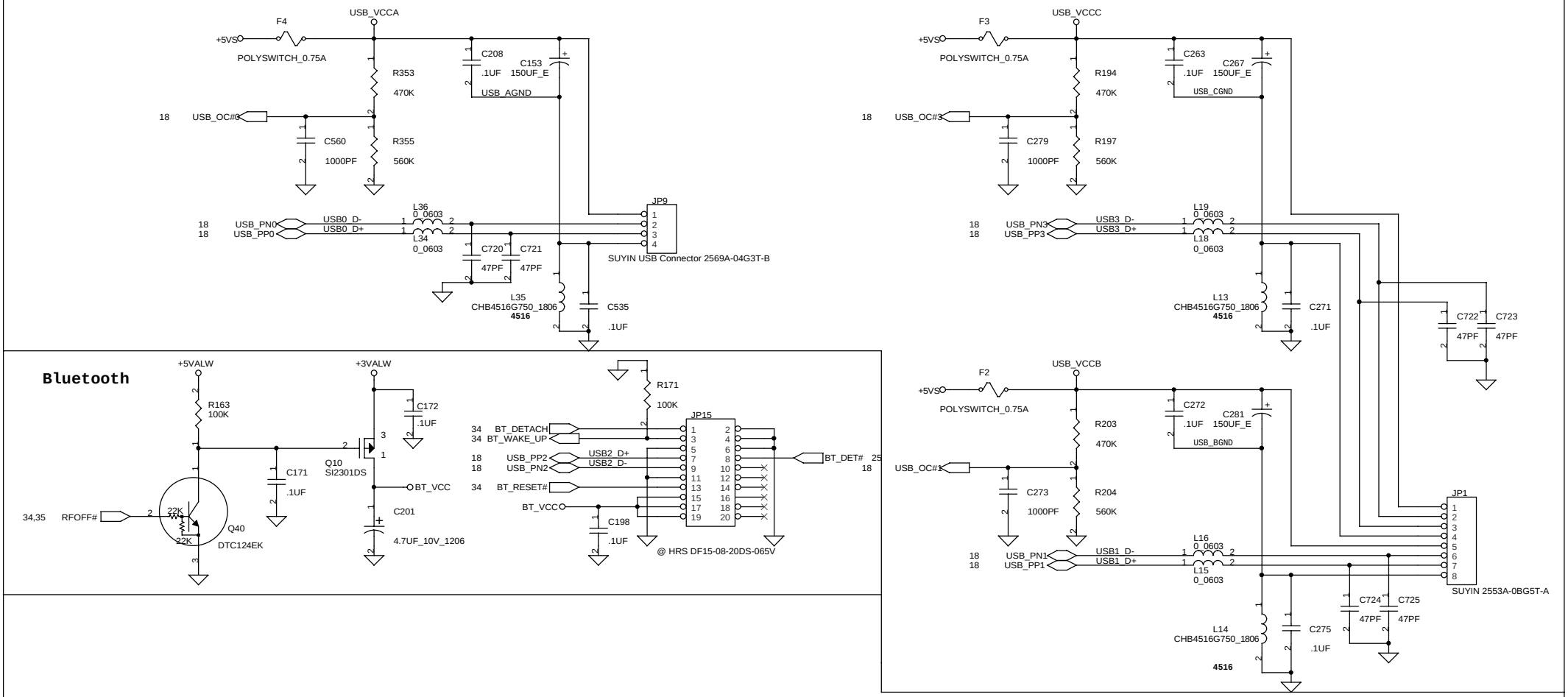
USB PORT



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Size: B | Document Number: 401191 (FOR ATL02 / ACL00) | Rev: 1C

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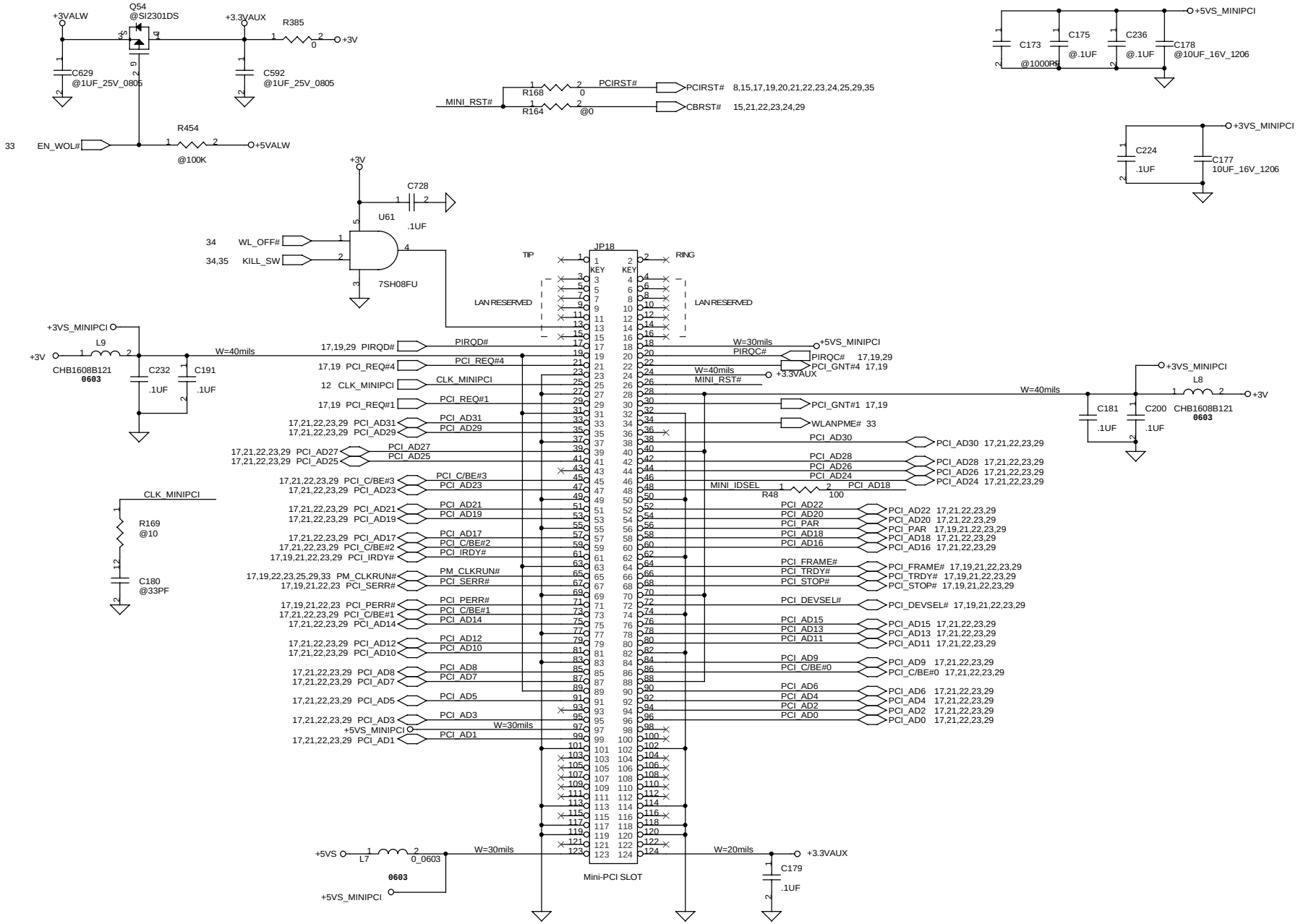

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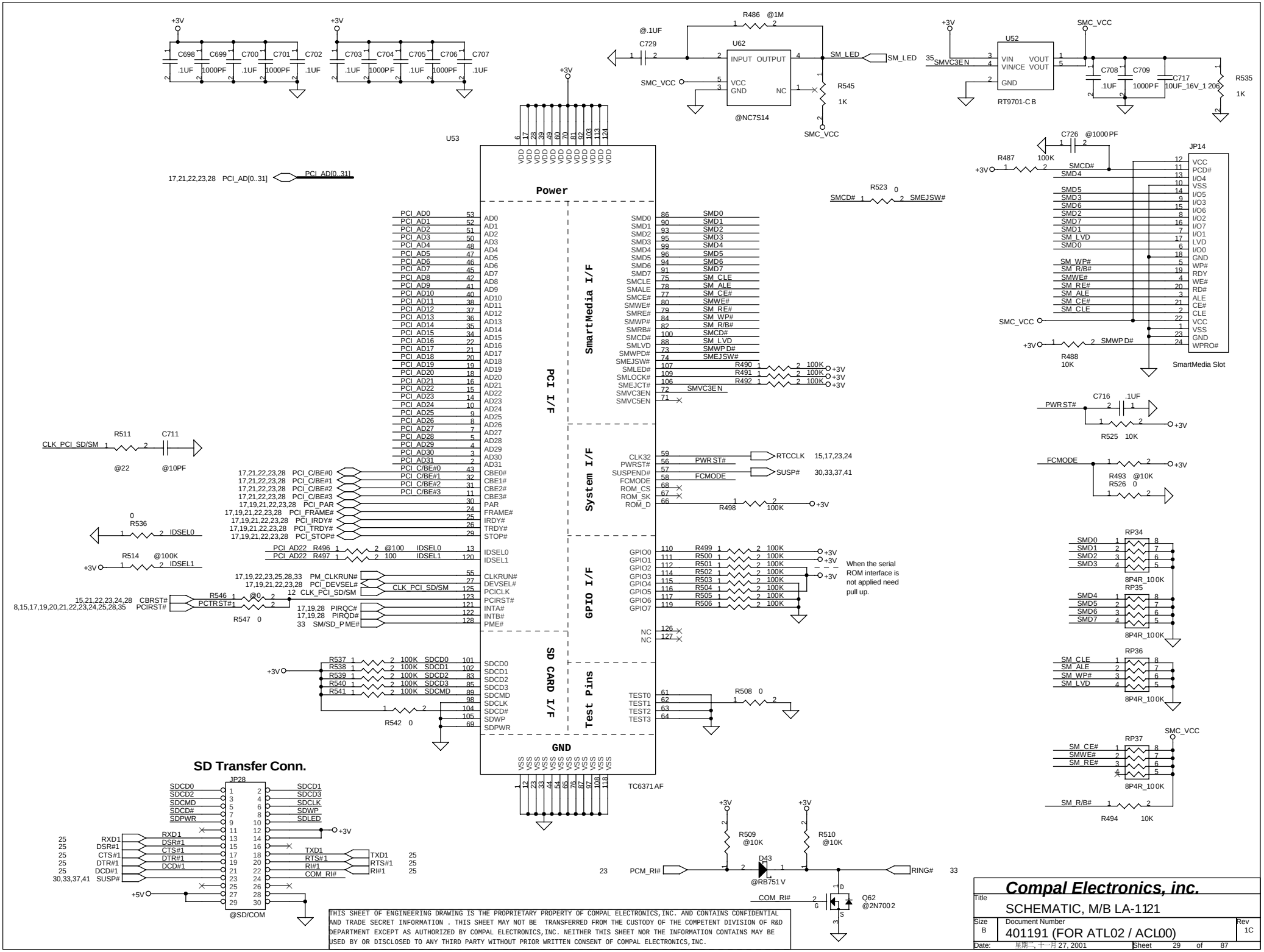

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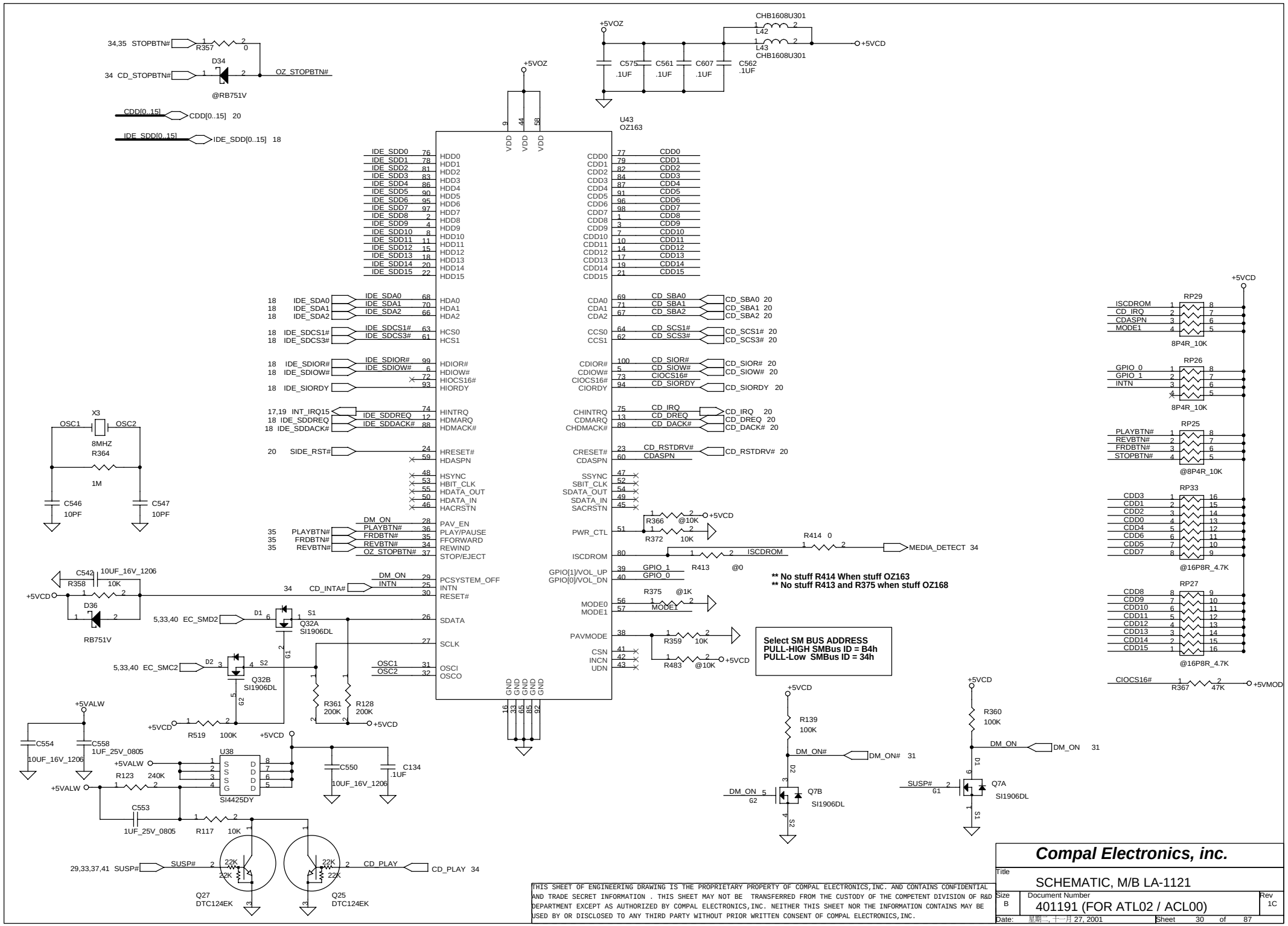

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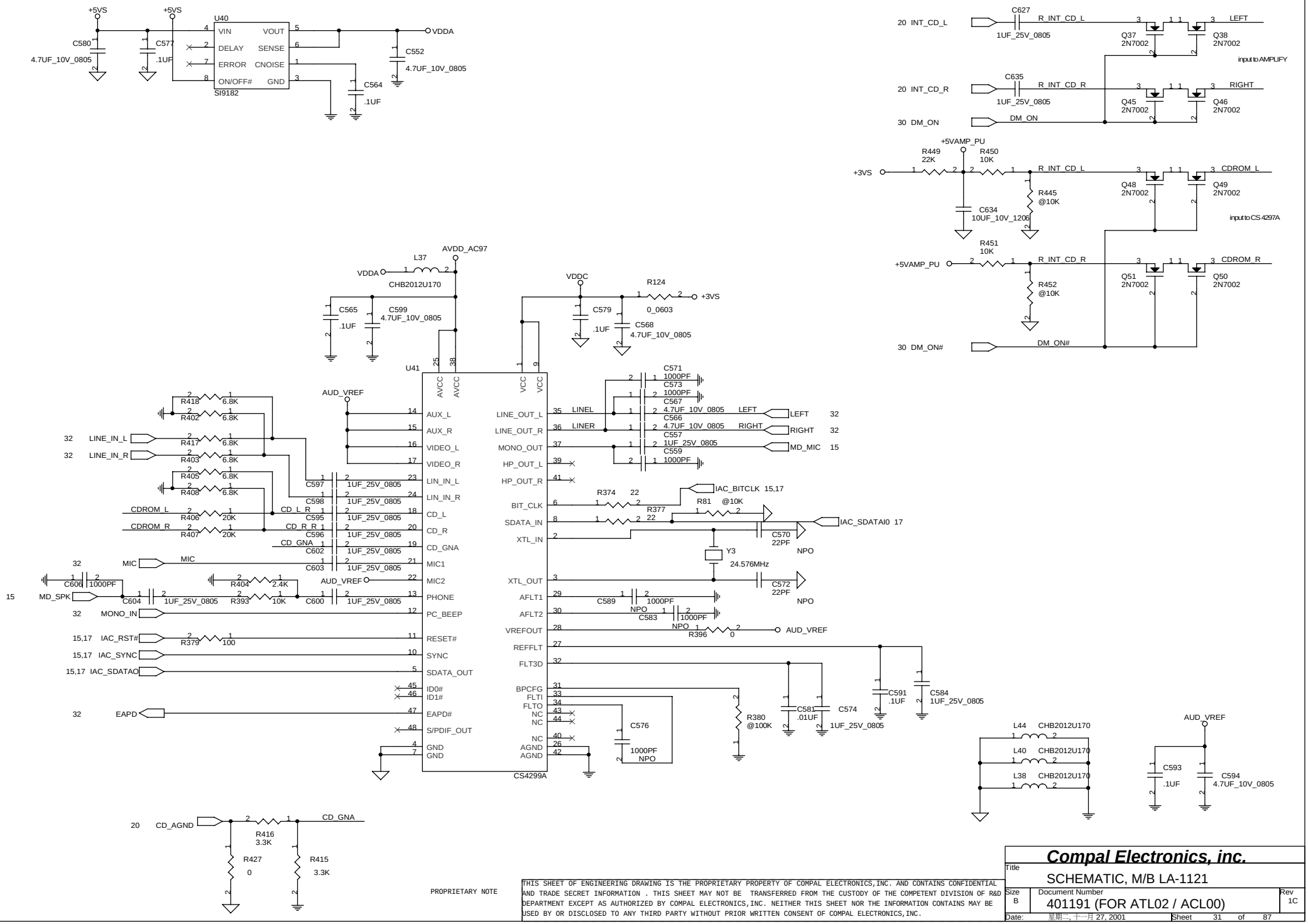
AC97 Codec



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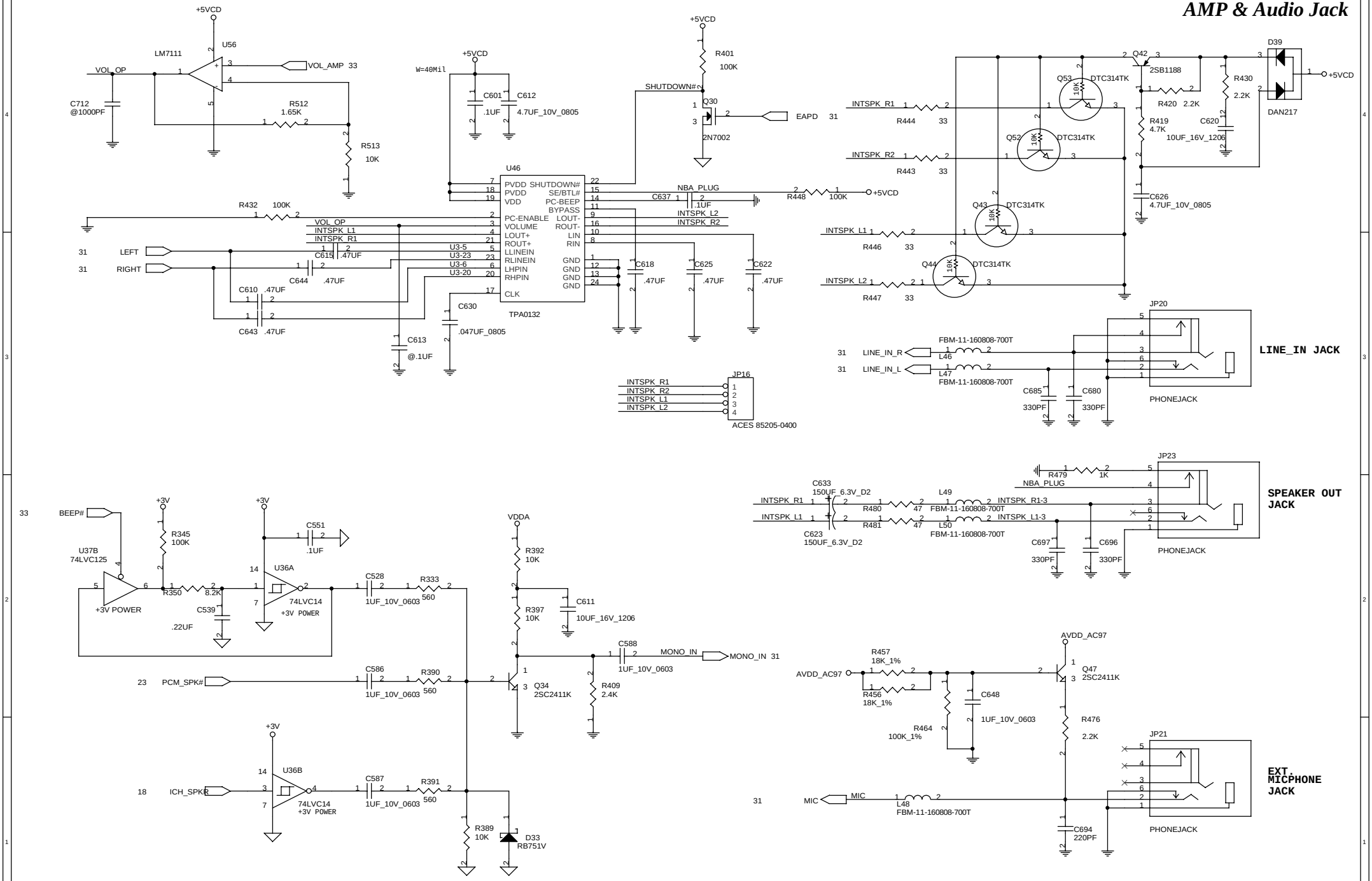
AMP & Audio Jack



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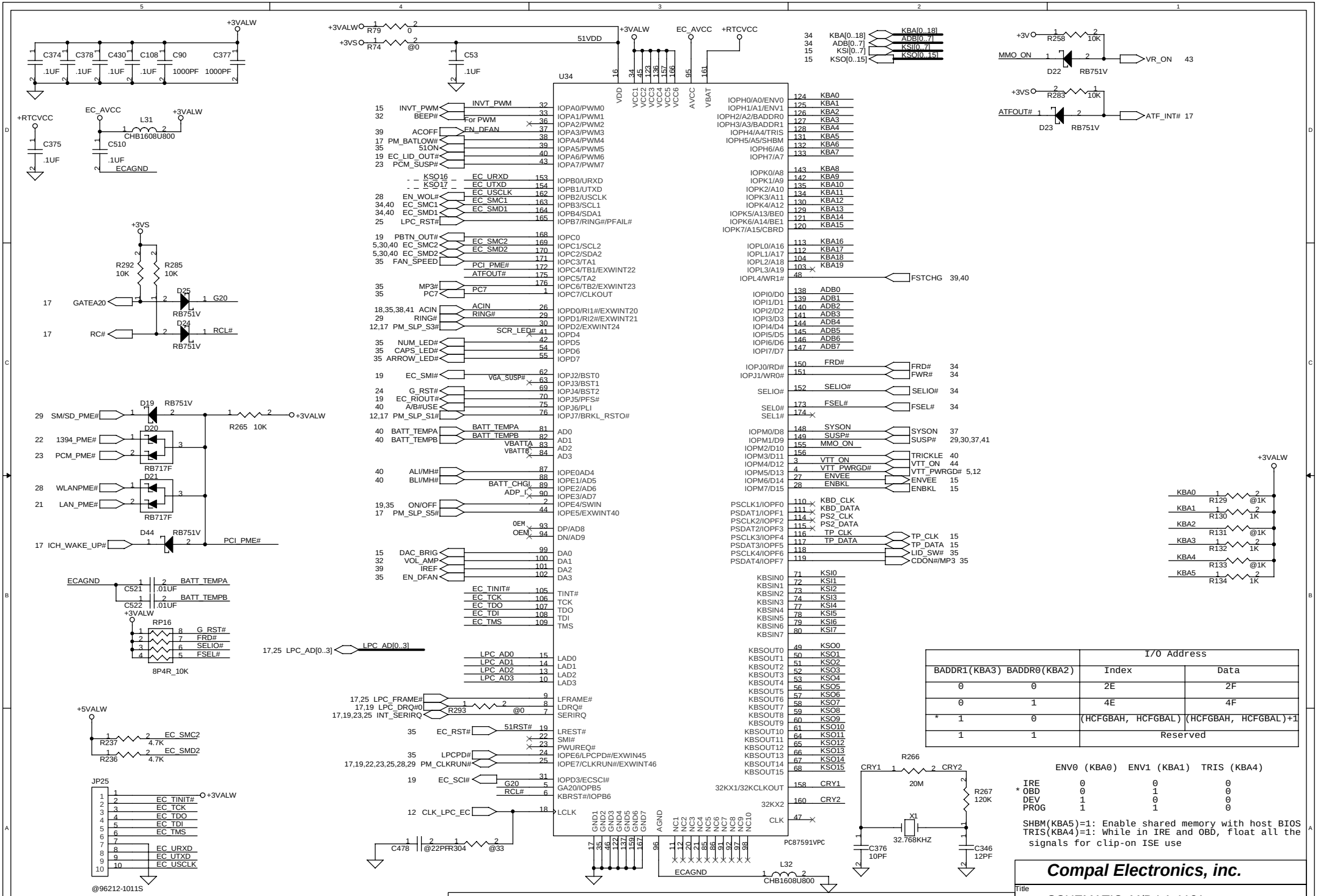

	I/O Address	
BADDR1(KBA3) BADDR0(KBA2)	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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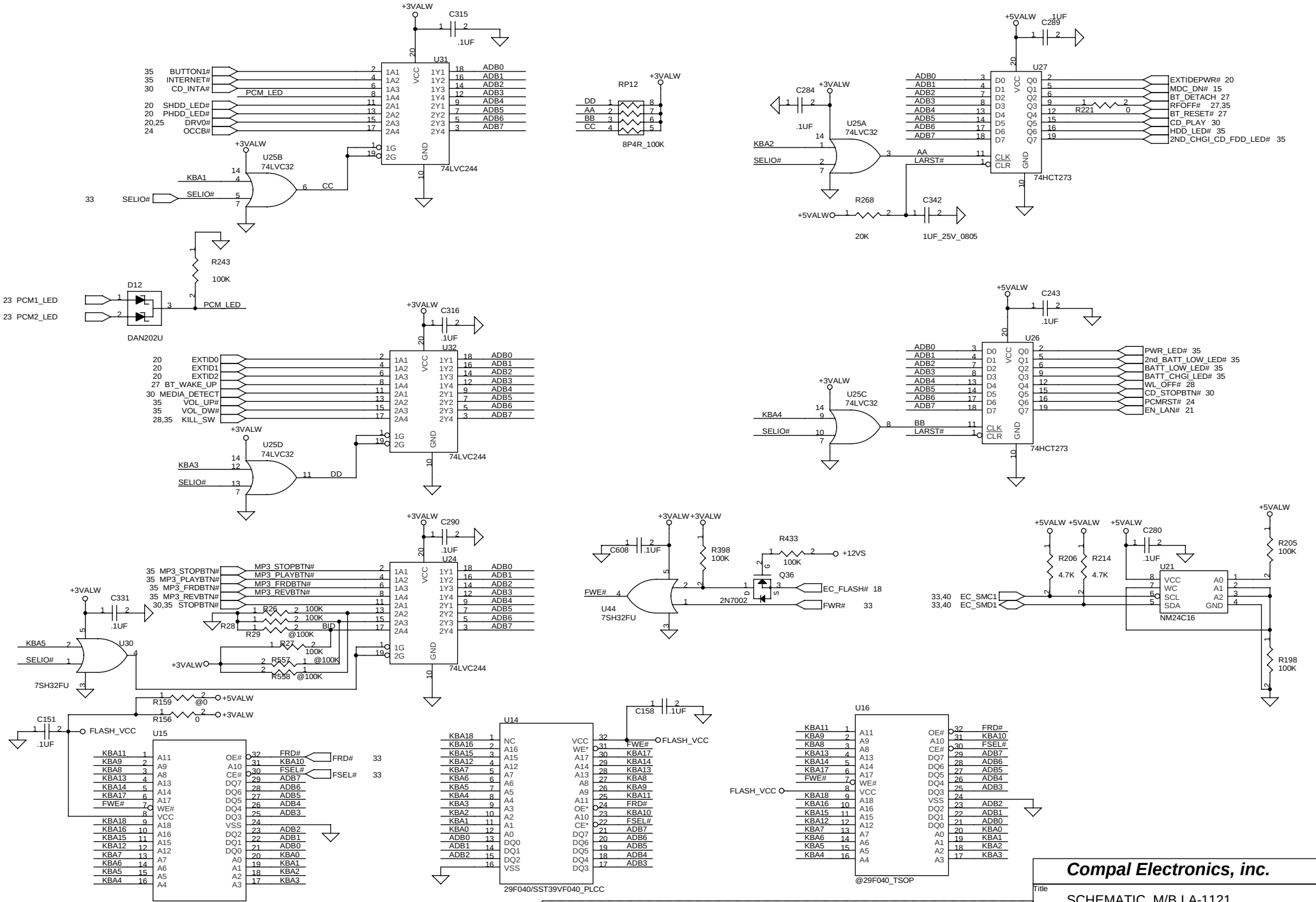

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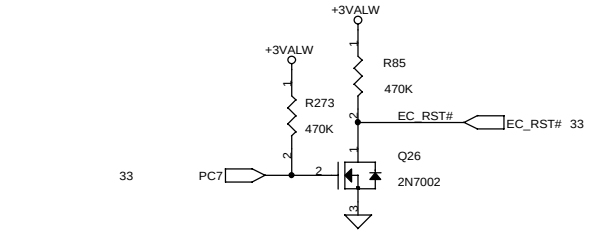
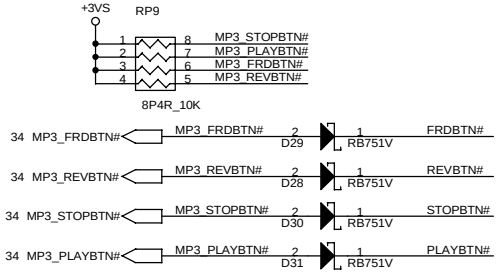
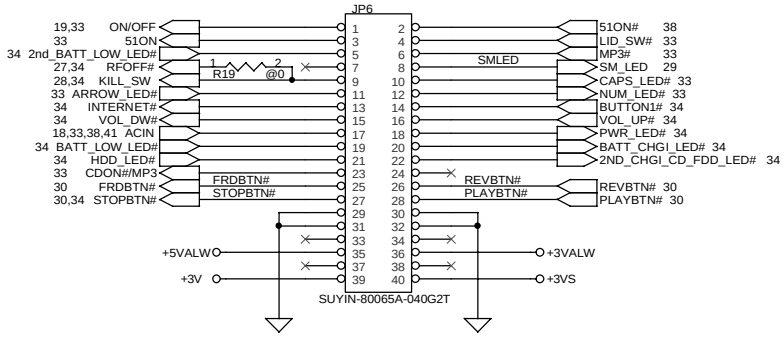
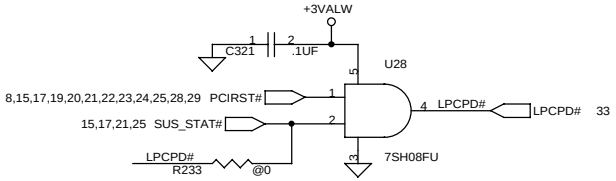


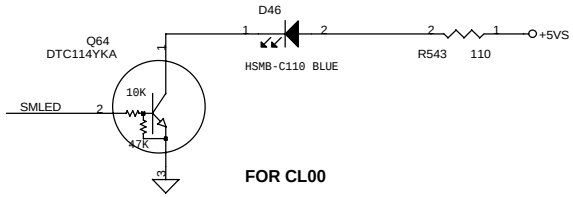






For PC87591 REV 0.A Only

FAN CONN.



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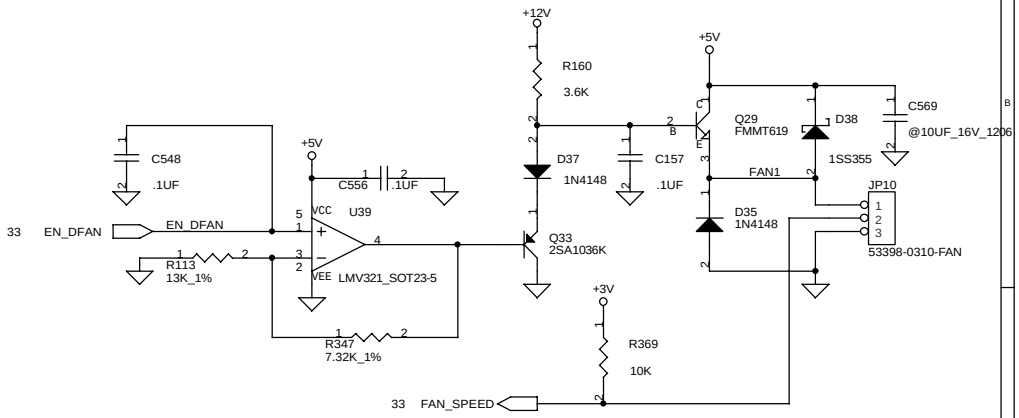

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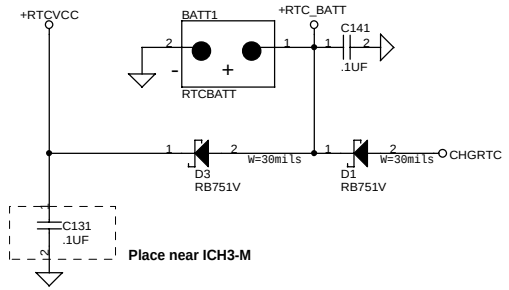
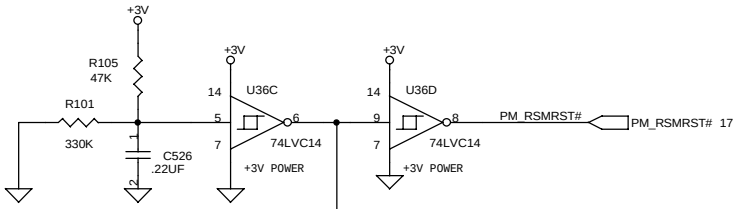
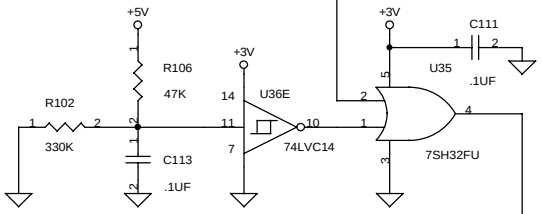
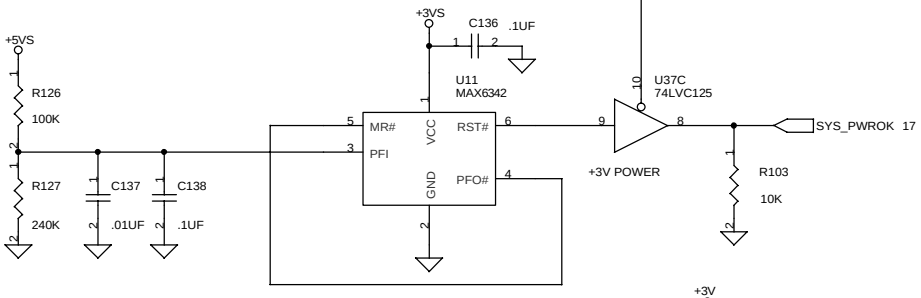
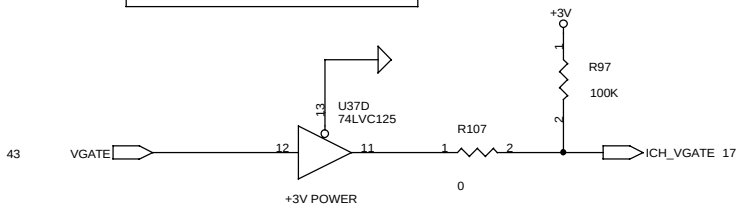
RTC Batt. Connector

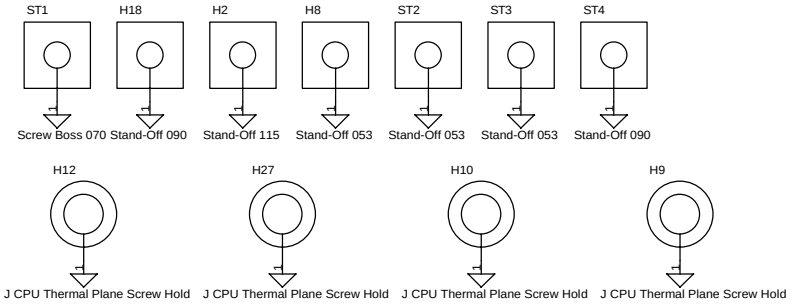


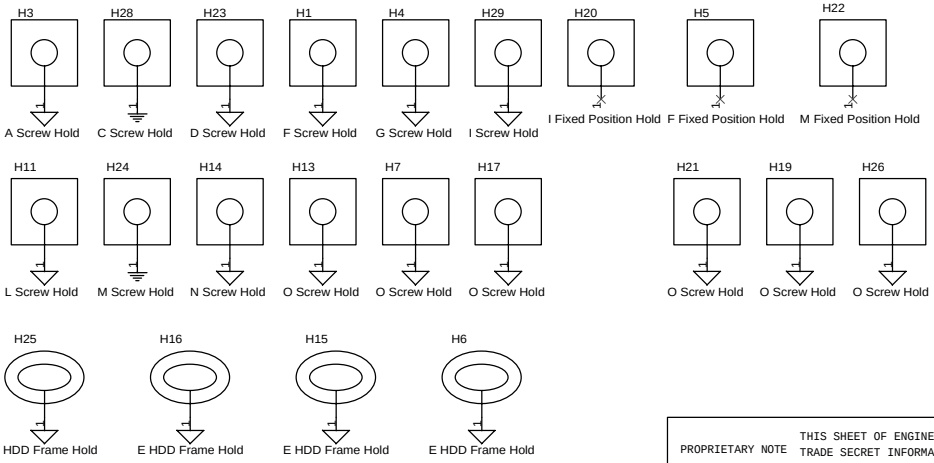


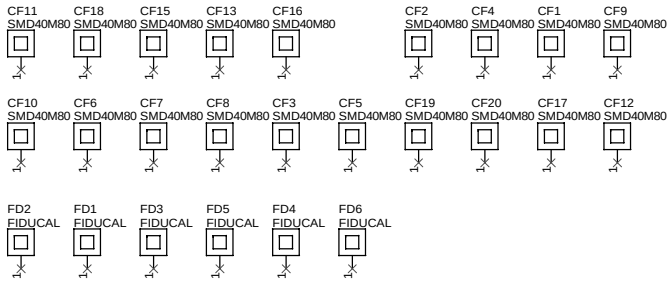












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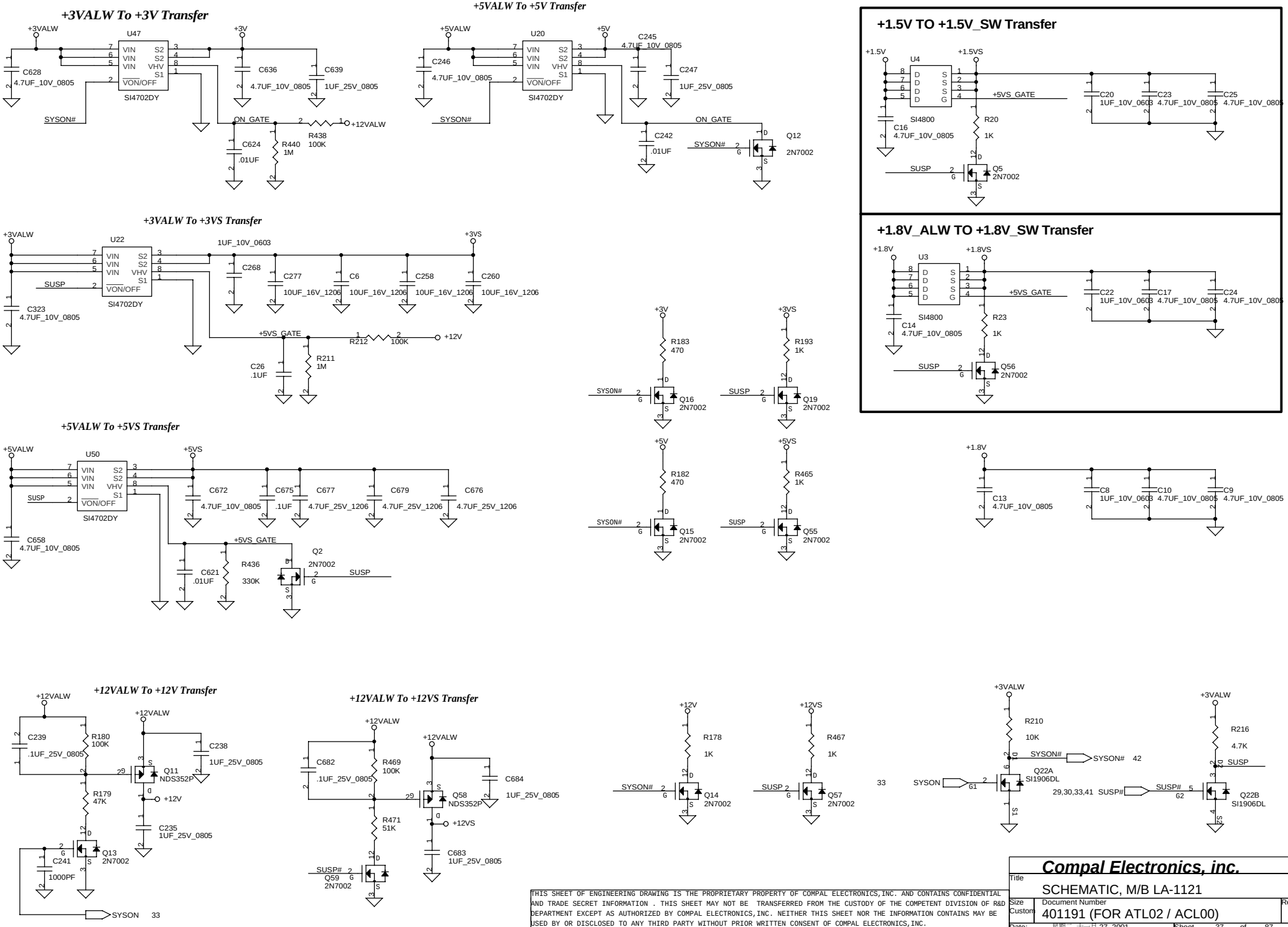
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U47
SI4702DY
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U20
SI4702DY
+1.5V TO +1.5V_SW Transfer
U4
SI4800
+1.8V_ALW TO +1.8V_SW Transfer
U3
SI4800
+3VALW To +3VS Transfer
U22
SI4702DY
+5VALW To +5VS Transfer
U50
SI4702DY
+12VALW To +12V Transfer
+12VALW To +12VS Transfer
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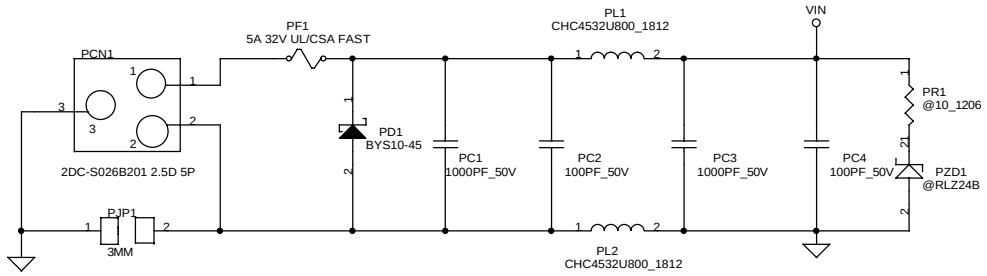
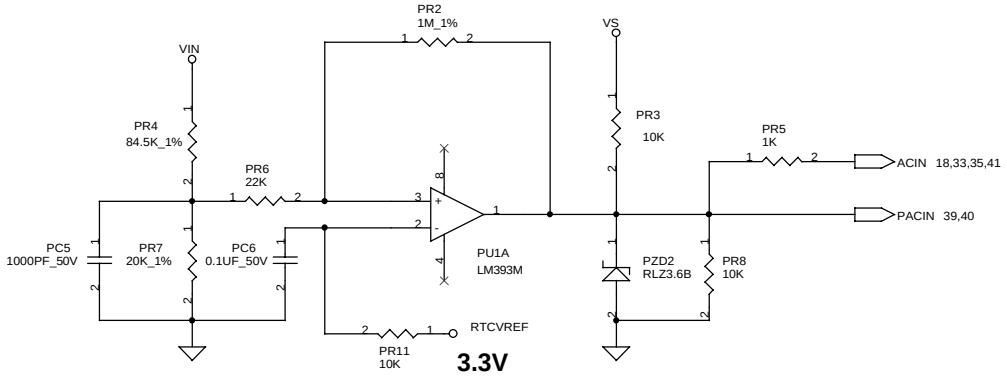
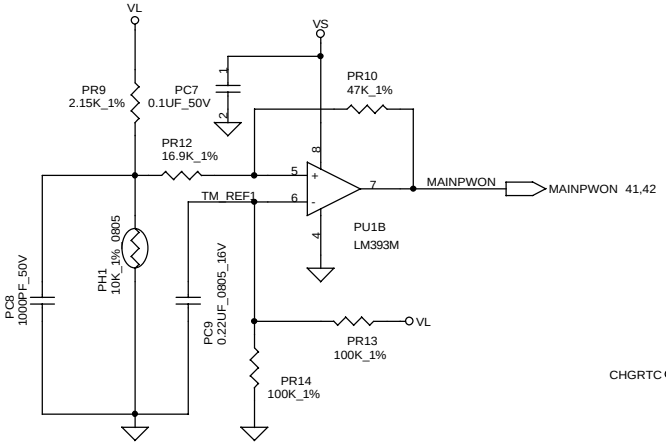
Vin Detector

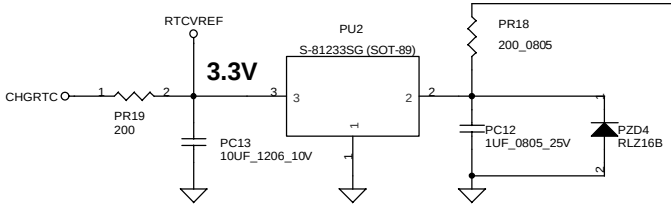
High	**18.764**	**17.901**	**17.063**
Low	**17.745**	**16.903**	**16.038**

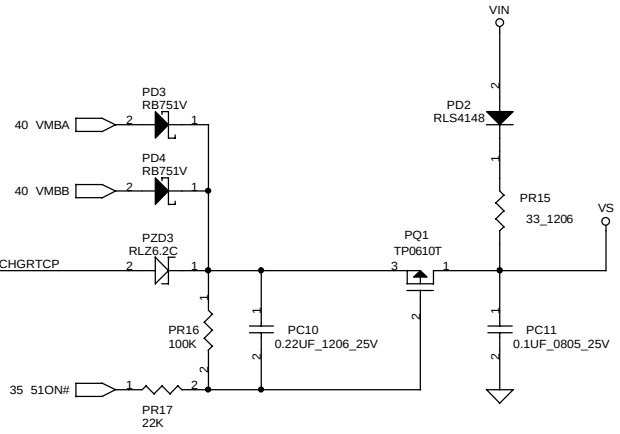


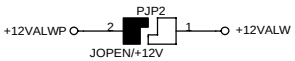


PH1 under CPU botten side :
CPU thermal protection at 81(82) degree C
Recovery at 50(51) degree C

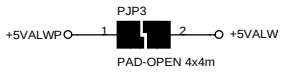








(120mA,20mils ,Via NO.= 1)



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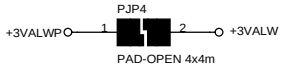

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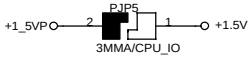
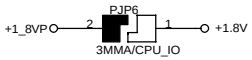


(1.5A,60mils ,Via NO.= 3)



(3A,120mils ,Via NO.= 6)

(6A,240mils ,Via NO.= 12)

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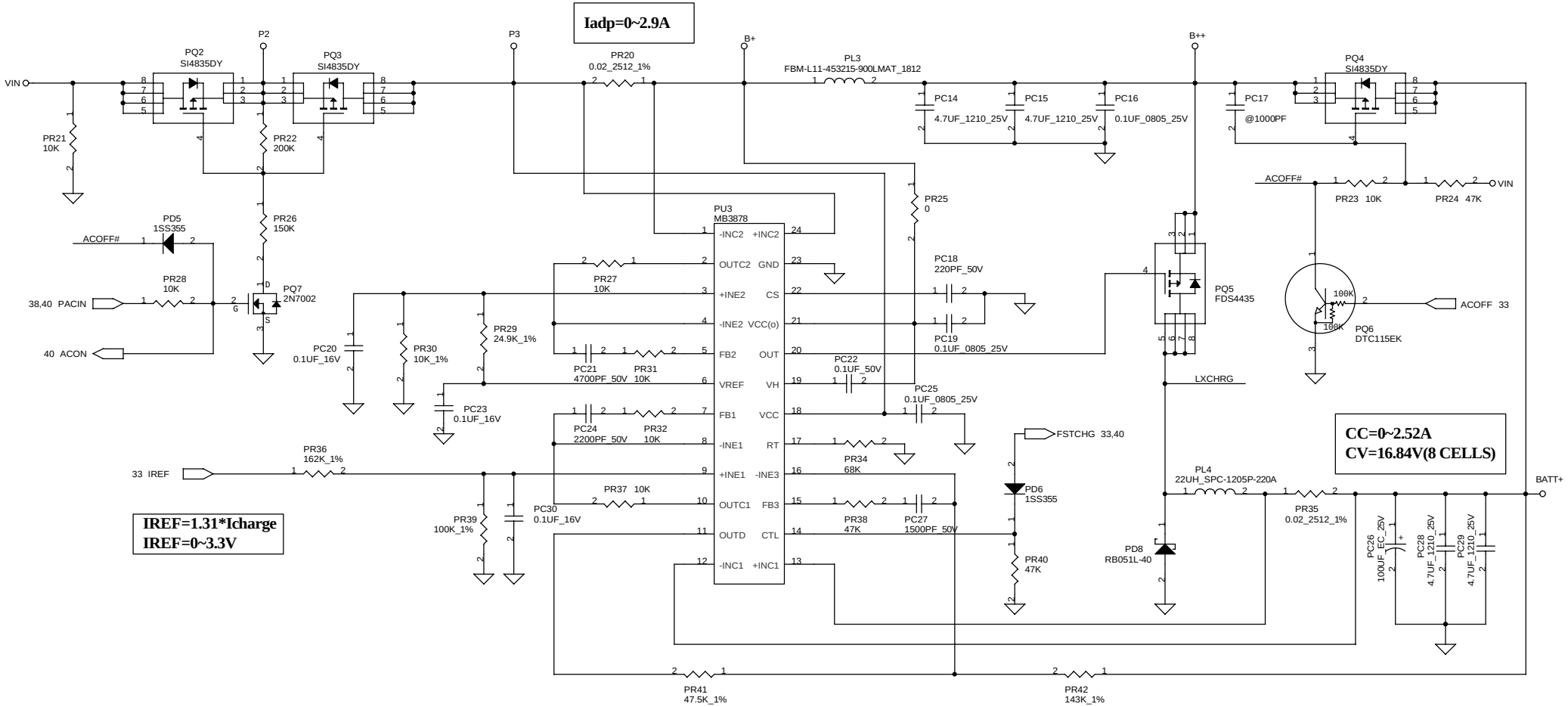

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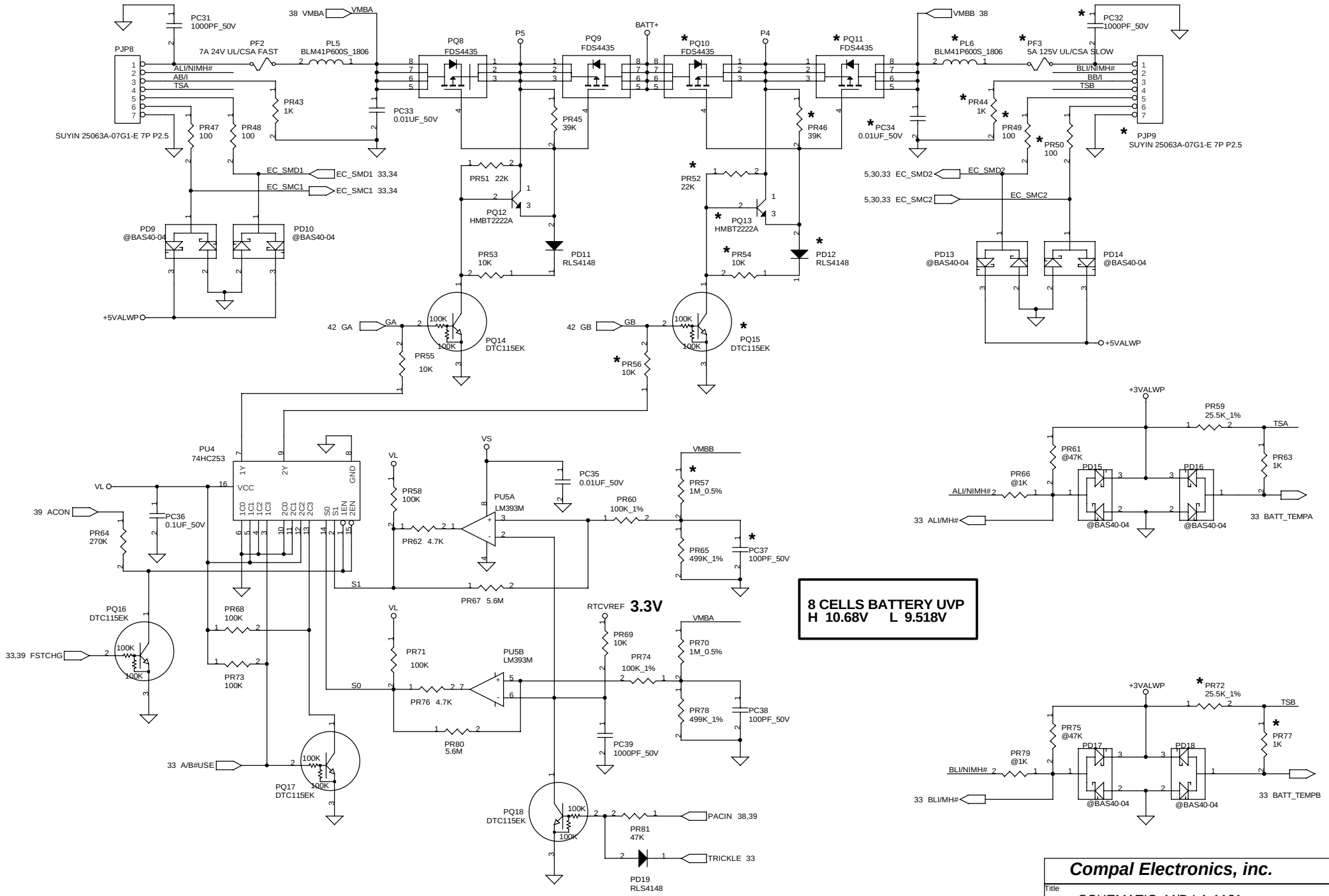

8 CELLS BATTERY UVP
H 10.68V L 9.518V

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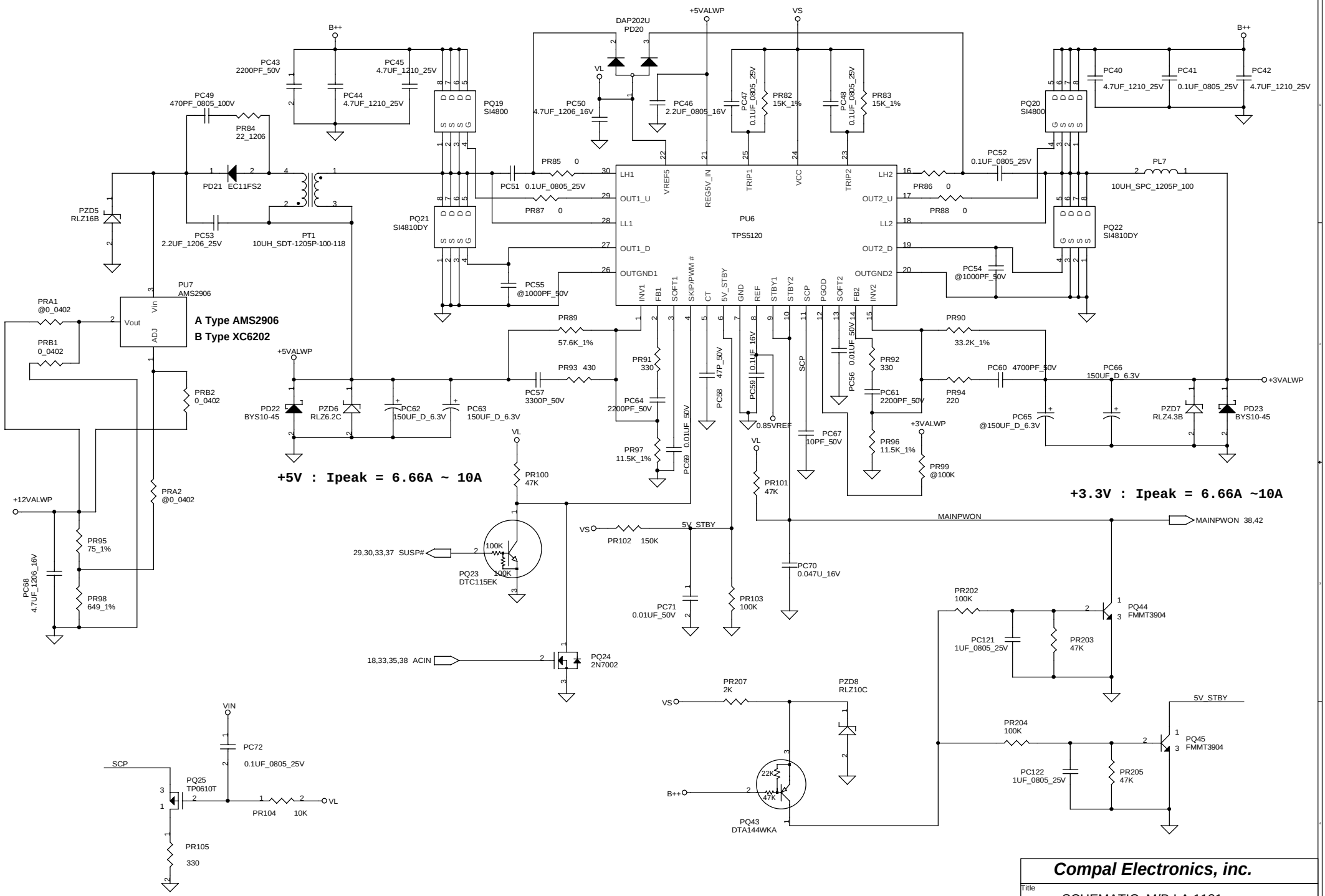

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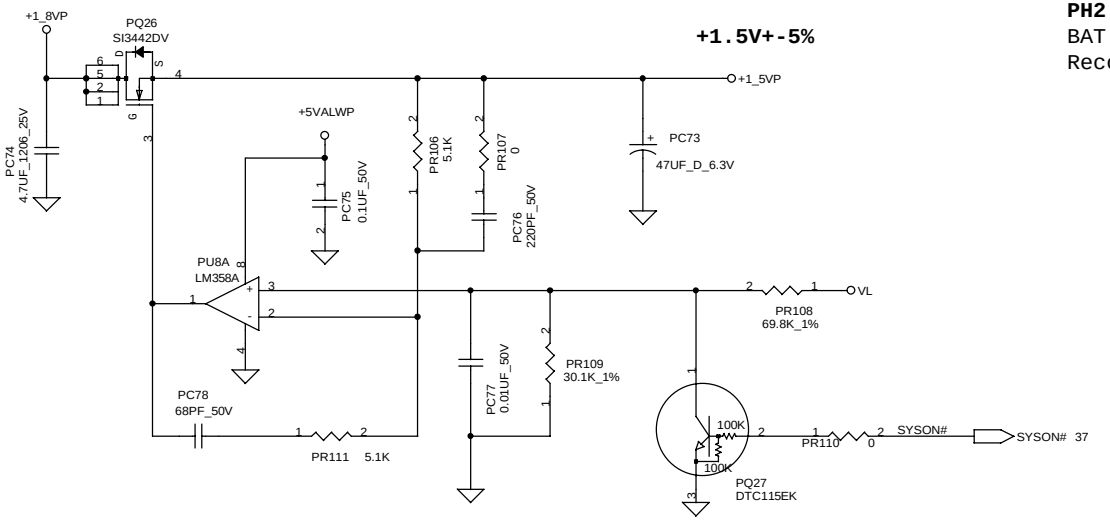
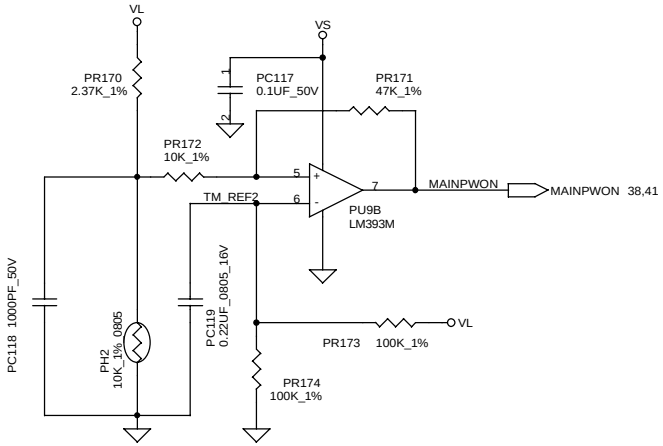
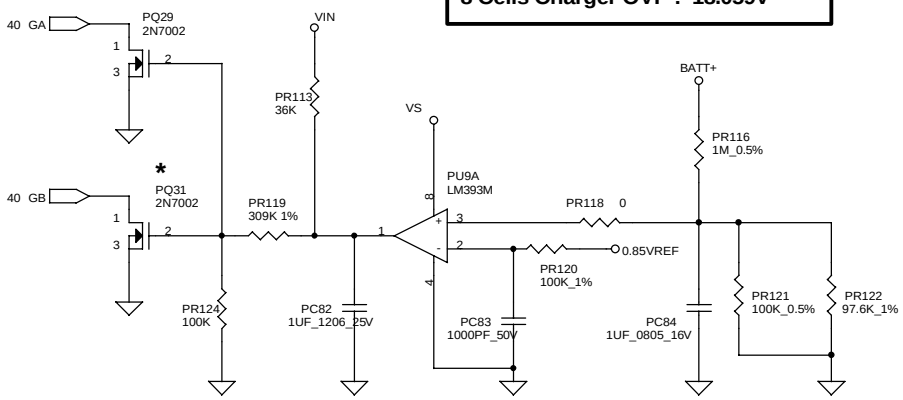


PH2 near main Battery CONN :
BAT. thermal protection at 73(74) degree C
Recovery at 50(51) degree C

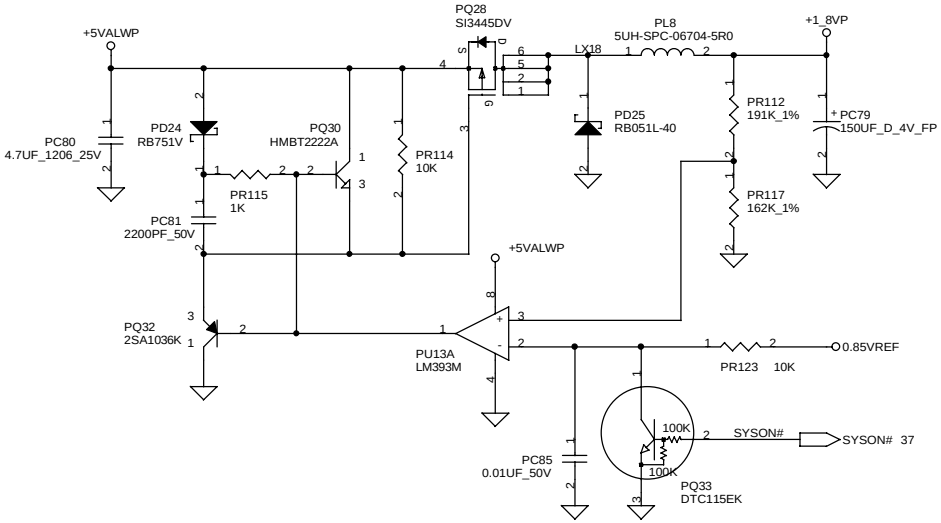


The * is DEL item only for ACL00

8 Cells Charger OVP : 18.059V



+1.8V+-5%



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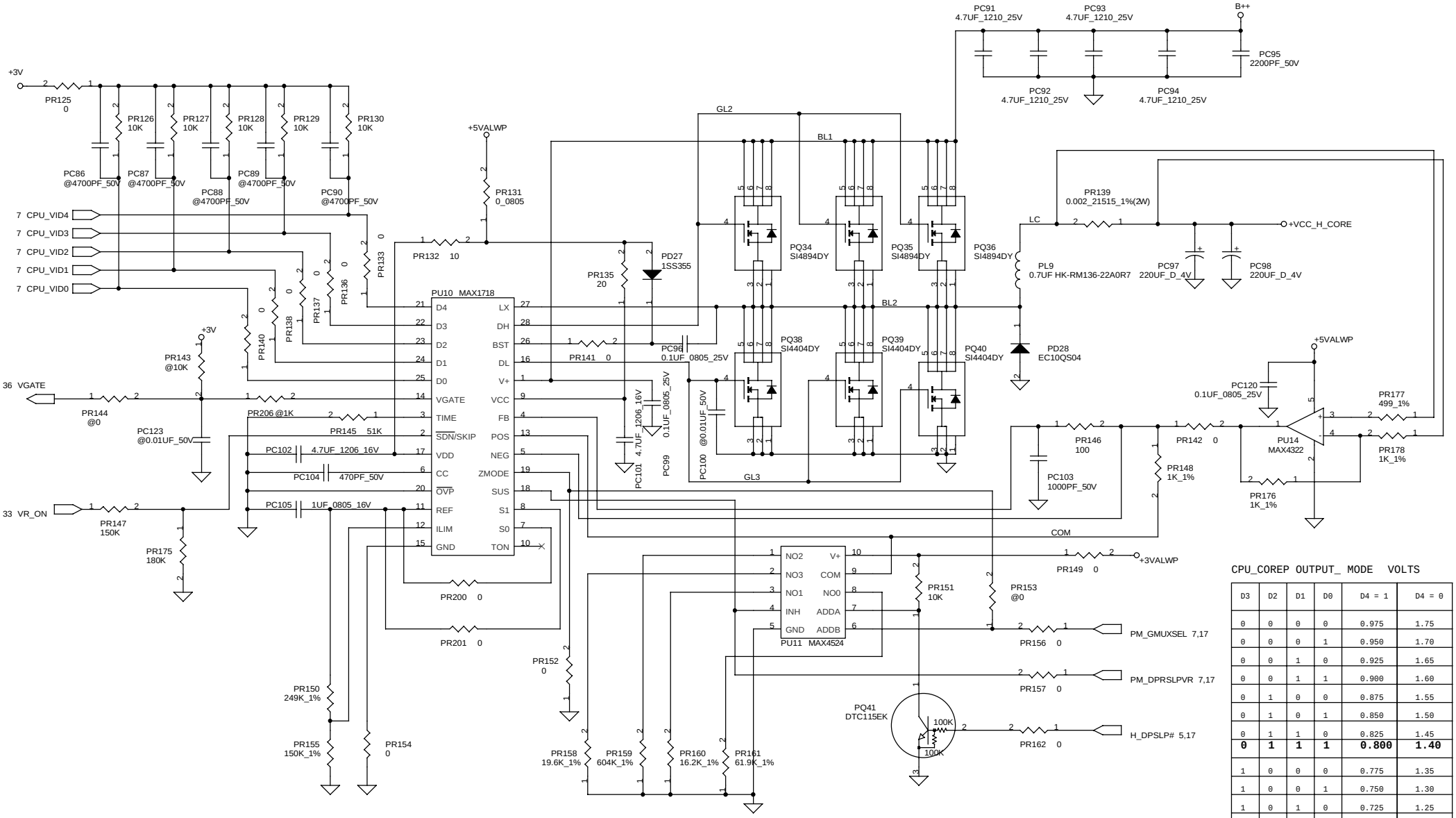

CPU CONTROL MODE

MODE	OFFSET	RBOTTOM	Vout(0A)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTEY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	-1.8mV	604K	1.248	0	1

CPU_COREP OUTPUT_ MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	0	0	1	0.950	1.70
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	**1**	**1**	**1**	**0.800**	**1.40**
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	**1**	**0**	**0**	**0.675**	**1.15**
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

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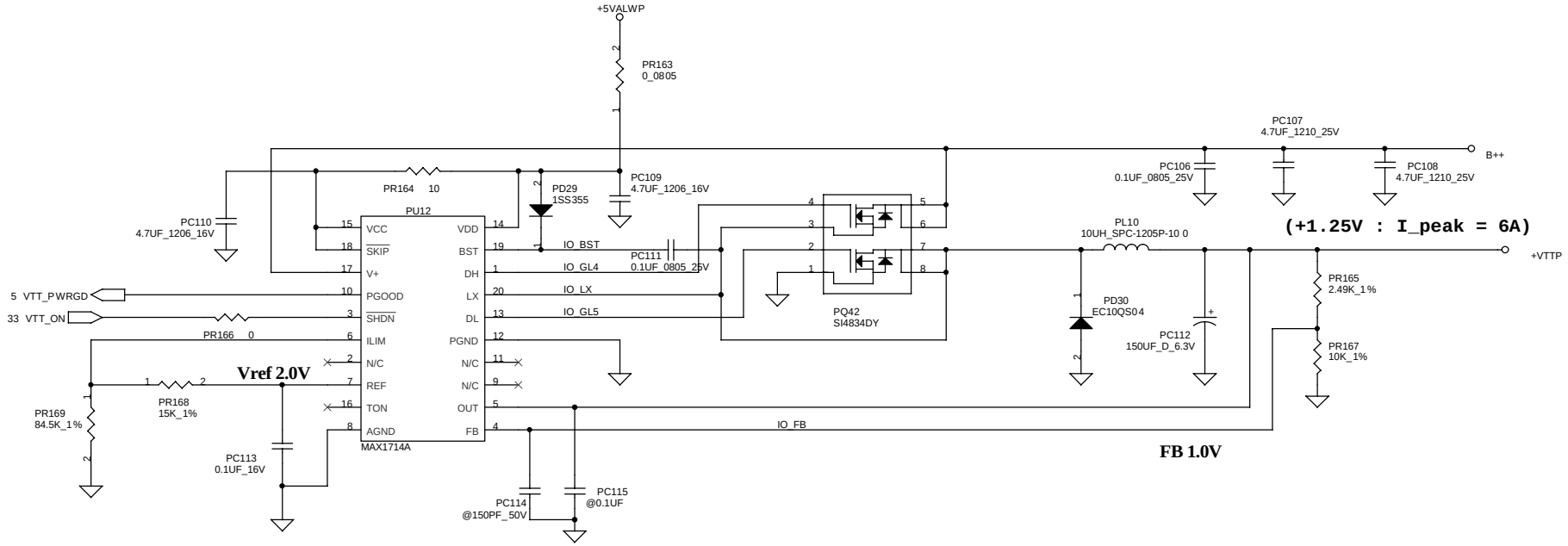

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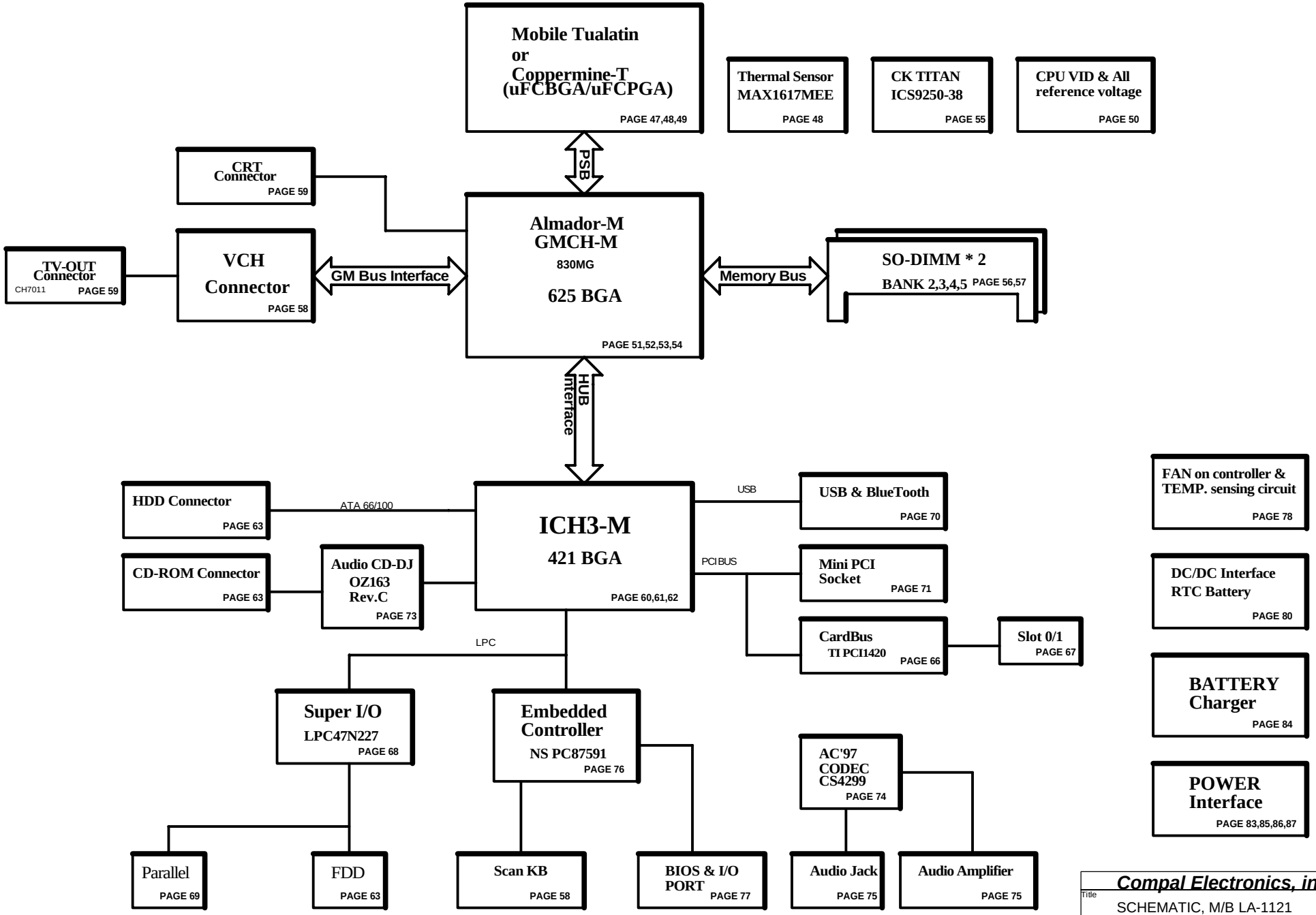
Model Name : ATW01

BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

PIR

REV 0.2

Date	Page	Description
9/6	12	

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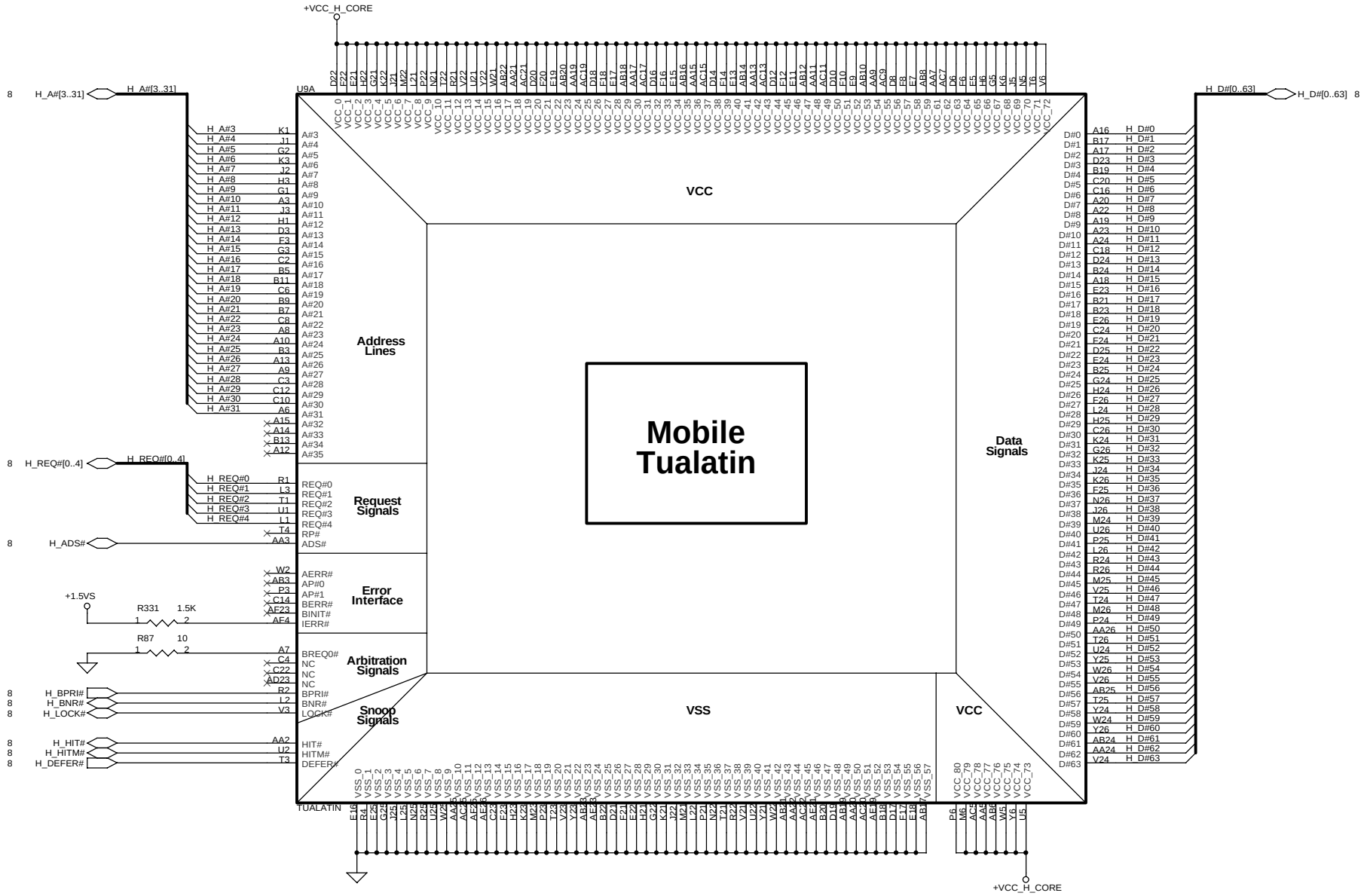

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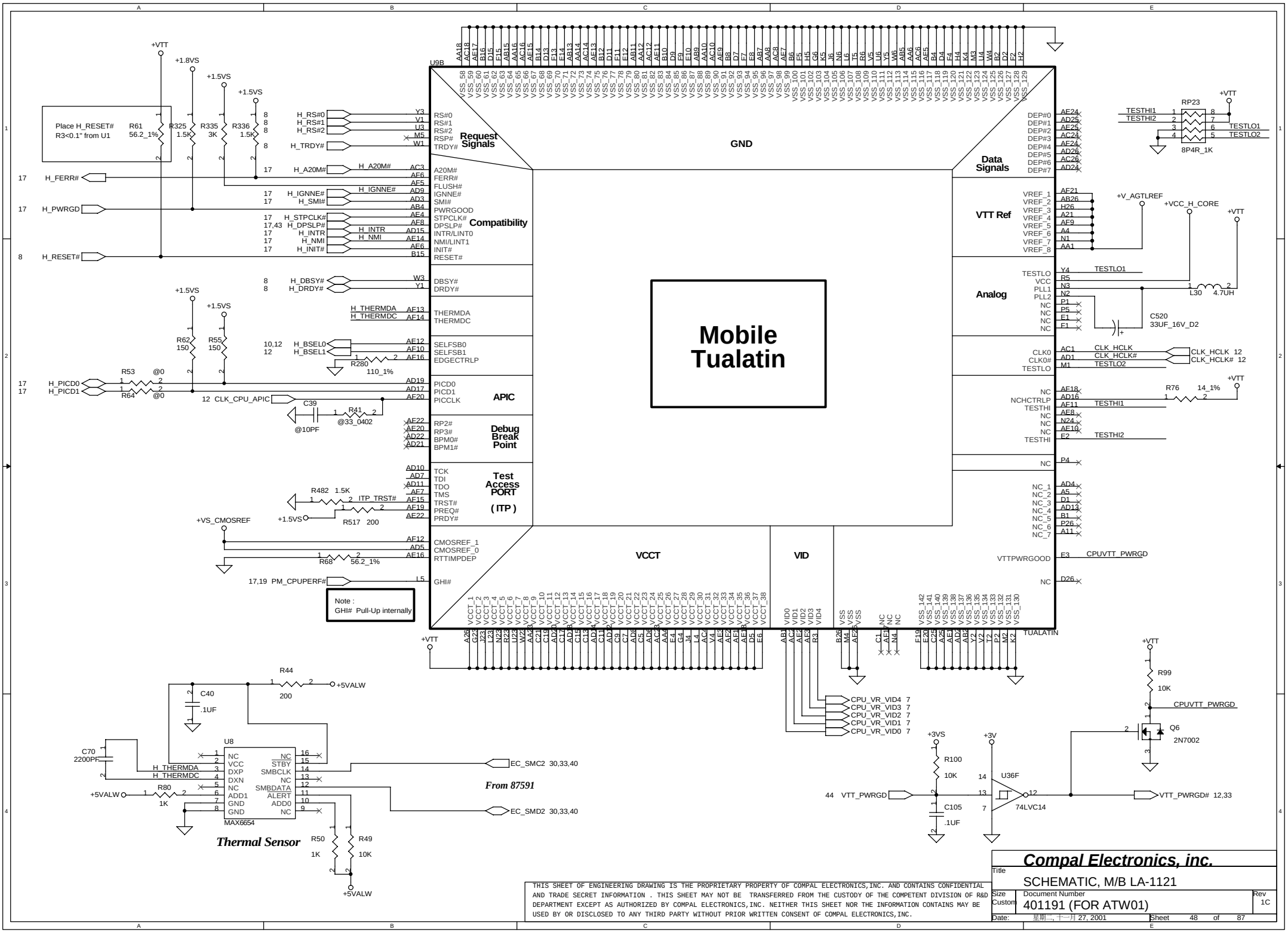

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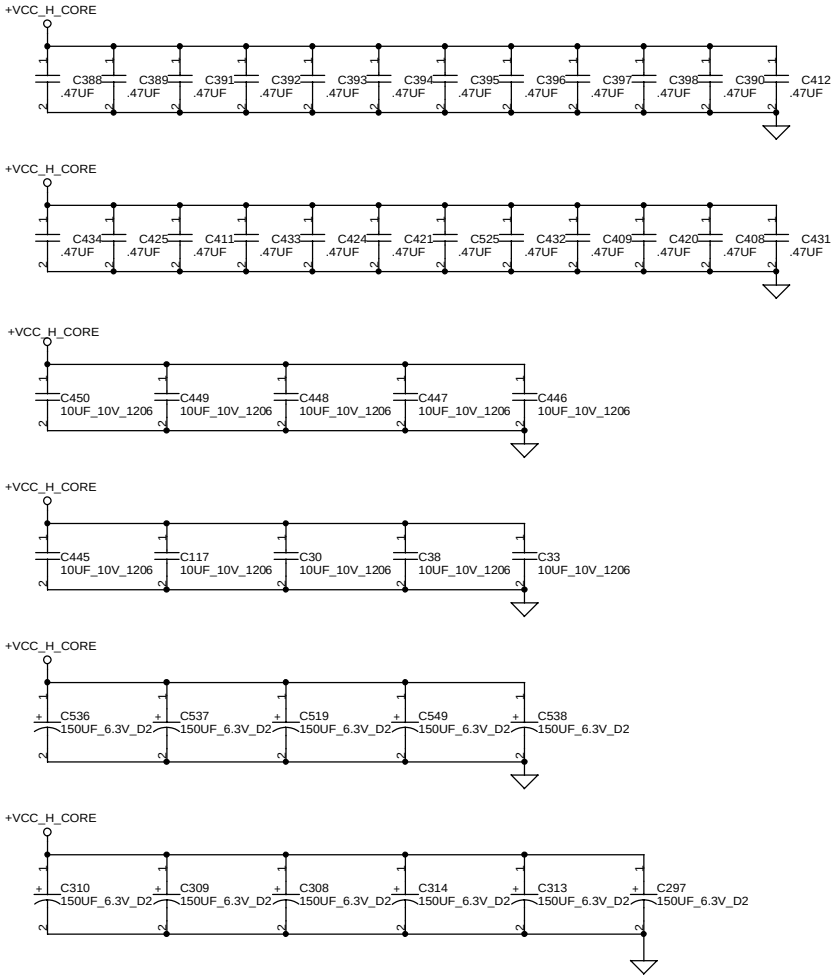
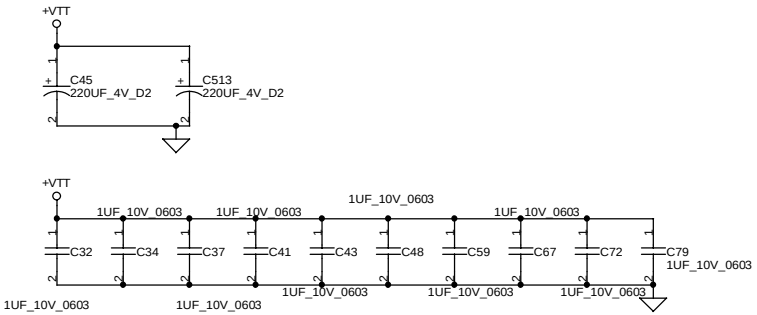
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.



Layout note :

Place close to CPU,
Use 2 vias per PAD.



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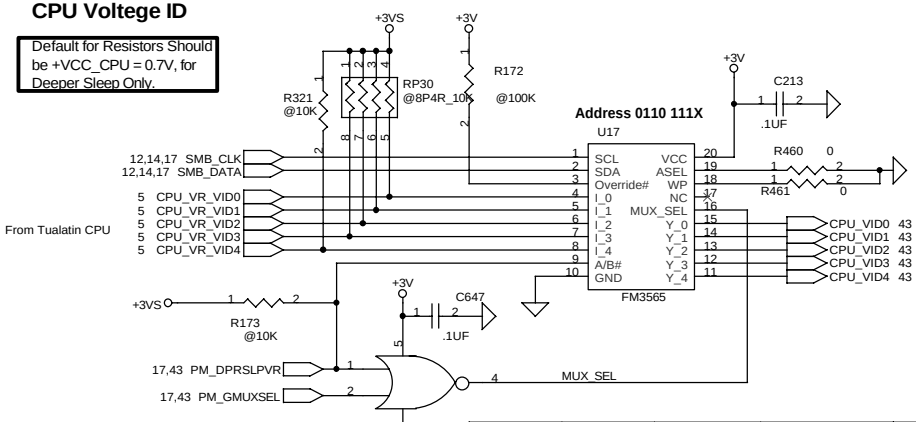
CPU Voltege ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1: for Deeper Sleep mode
0 : for Performance mode

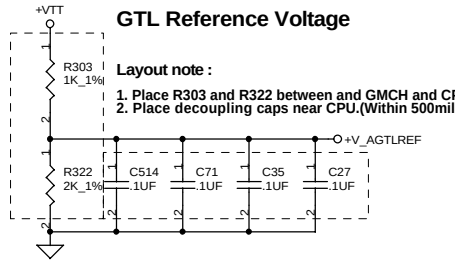
Override#	MUX_SEL	A/B#	MUX_outputs	Mode
1	1	X	MUX_inputs	Battery
1	0	0	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

```
D4  D3  D2  D1  D0  CPU_Core(V)  ES(before MP)
-----------------------------------------------------
0   0   1   0   1       1.50V (Performance)
0   1   1   0   0       1.15V (Battery)
1   0   1   0   1       0.85V (Deeper Sleep)


D4  D3  D2  D1  D0  CPU_Core(V)  QS( MP)
-----------------------------------------------------
0   0   1   1   1       1.40V (Performance)
0   1   1   0   0       1.15V (Battery)
1   0   1   0   1       0.85V (Deeper Sleep)
```

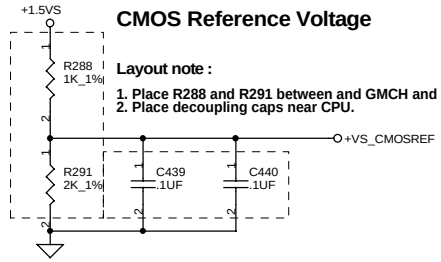
GTL Reference Voltage



Layout note :

1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)

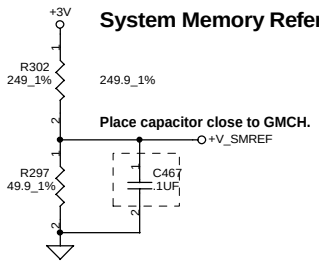
CMOS Reference Voltage



Layout note :

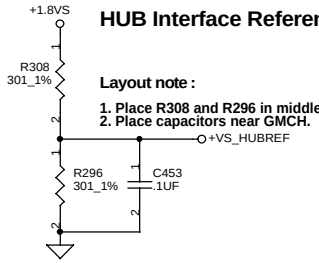
1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.

System Memory Reference



Place capacitor close to GMCH.

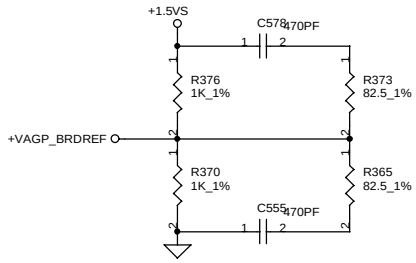
HUB Interface Reference



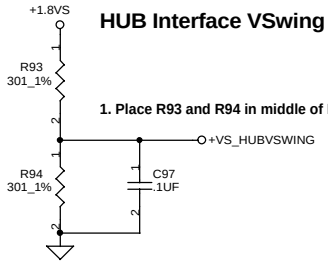
Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

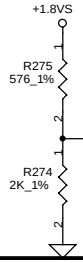
Place Reference Circuit near GMCH



HUB Interface VSwing Voltage



1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.

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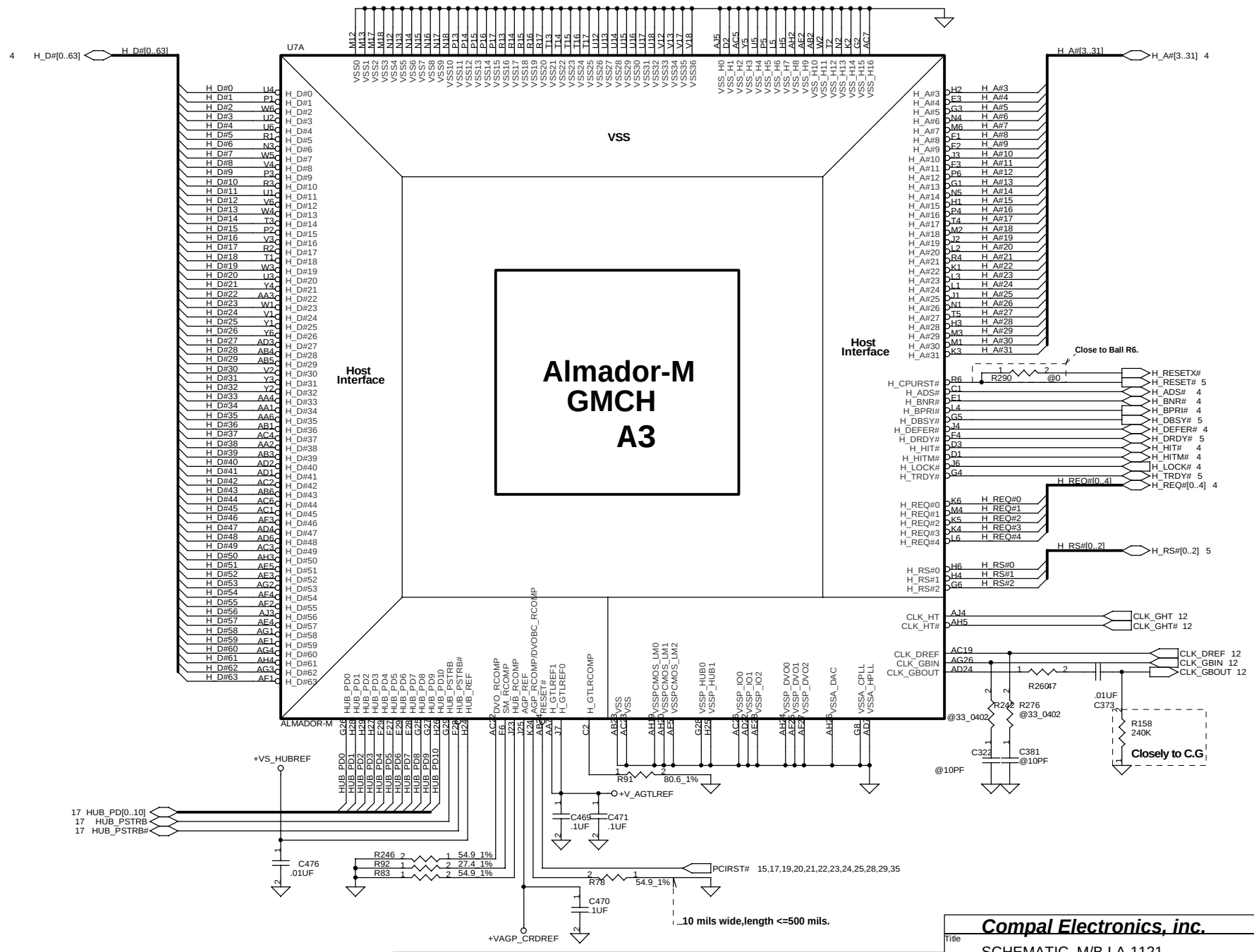

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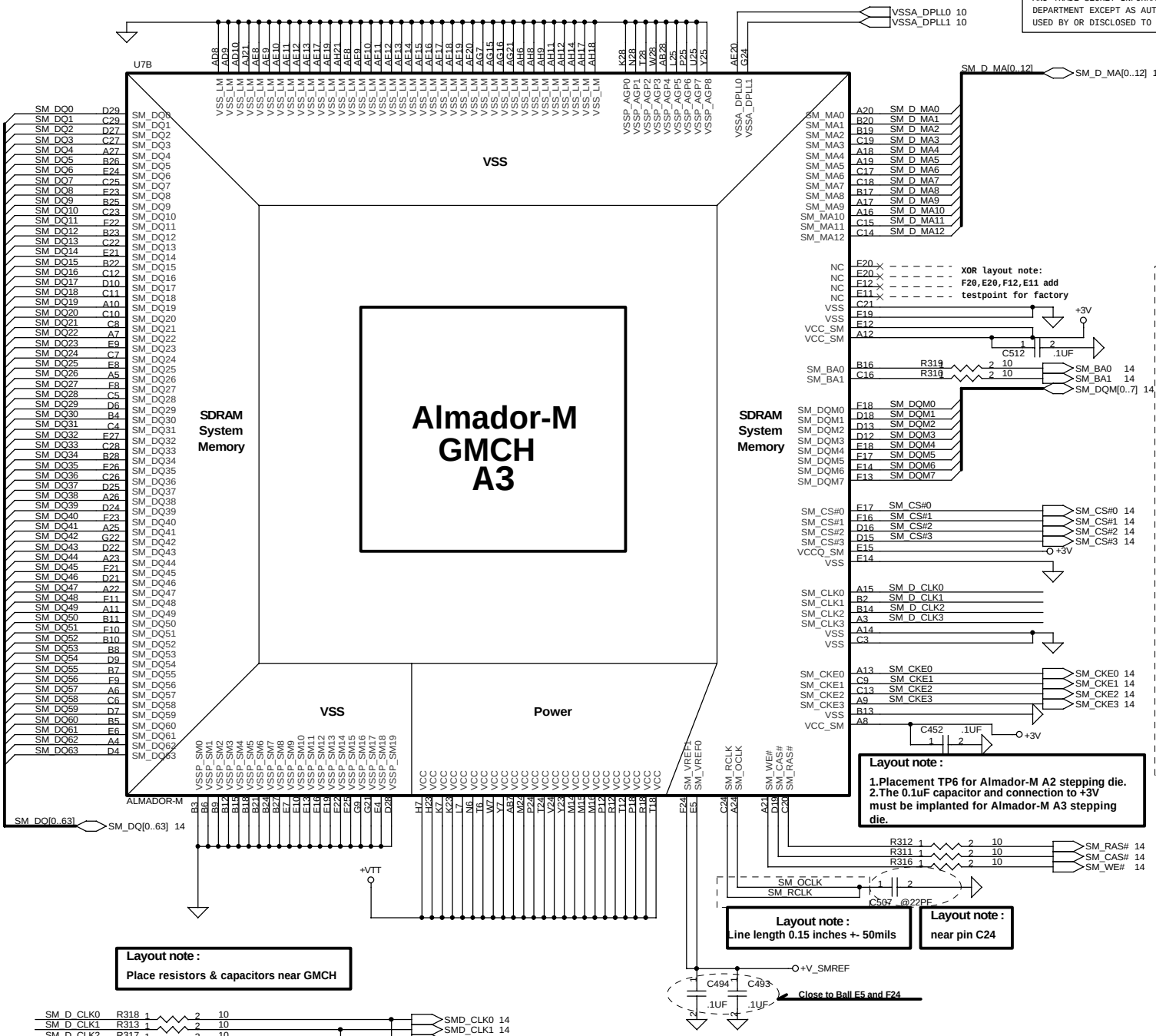

For Almador-M A3 stepping requirement.

The table below provides a summary of the ballout changes to the Almador-M chip

Table 4-1 Ballout Changes

Ball#	New Signal Name	Old Signal Name
A8	VCC_SM	SM_CKE5
A12	VCC_SM	SM_ECC7
E12	VCC_SM	SM_ECC6
G10	VCC_SM	VCCQ_SM
F7	VCCQ_SM	VCC_SM
G19	VCCQ_SM	VCC_SM
E15	VCCQ_SM	SM_CS4
F15	VCCQ_SM	VCC_SM
A14	VSS	SM_CLK4
B13	VSS	SM_CKE4
C3	VSS	SM_CLK5
C21	VSS	SM_ECC4
E14	VSS	SM_CS5
F19	VSS	SM_ECC5
E11	NC	SM_ECC3
E20	NC	SM_ECC1
F12	NC	SM_ECC2
F20	NC	SM_ECC0

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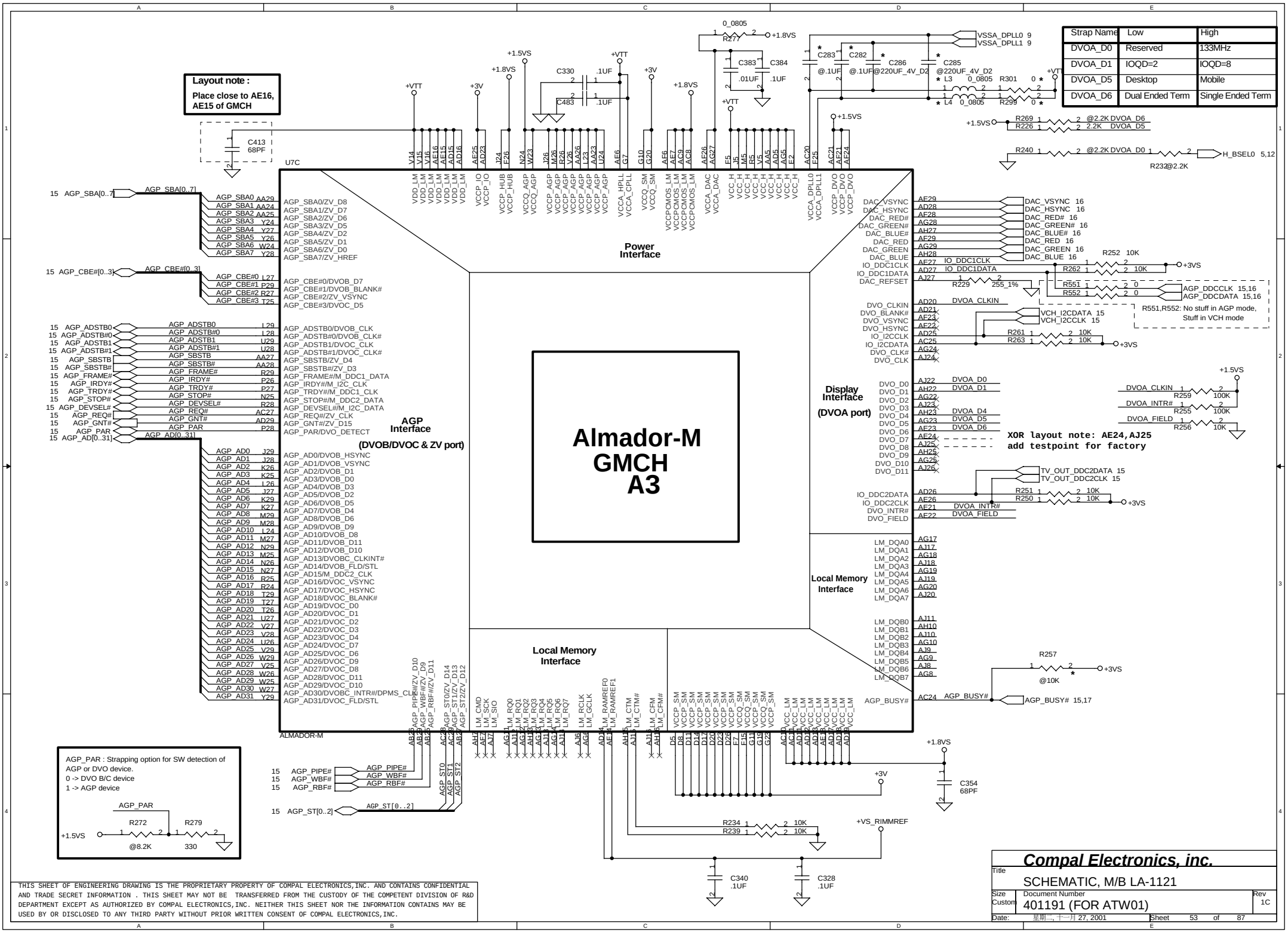

Strap Name	Low	High
DVOA_D0	Reserved	133MHz
DVOA_D1	IOQD=2	IOQD=8
DVOA_D5	Desktop	Mobile
DVOA_D6	Dual Ended Term	Single Ended Term

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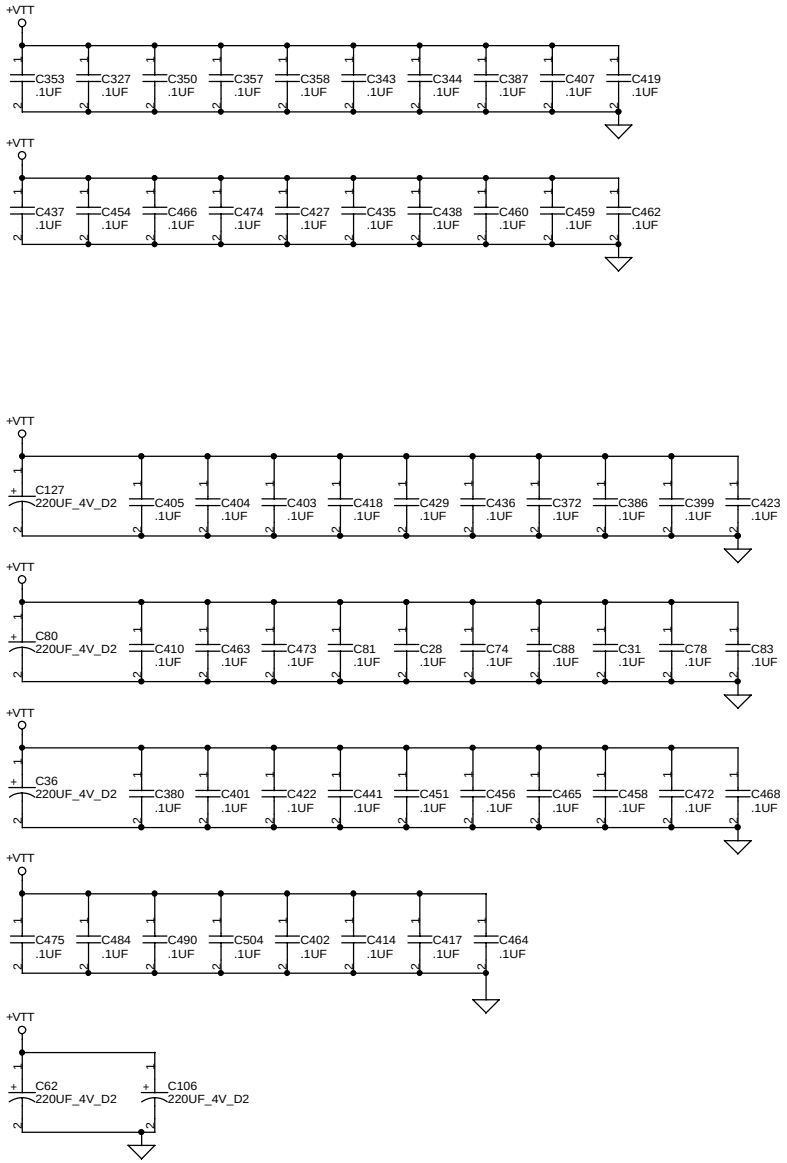
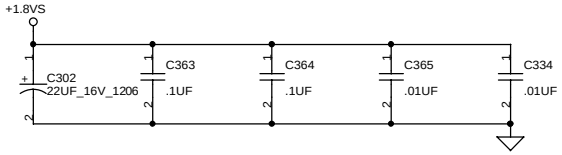
Layout note :

Distribute as close as possible to GMCH Processor Quadrant .



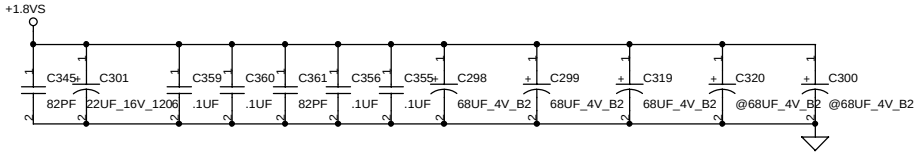
Layout note :

Distribute as close as possible to VCCPCMOS_LM .



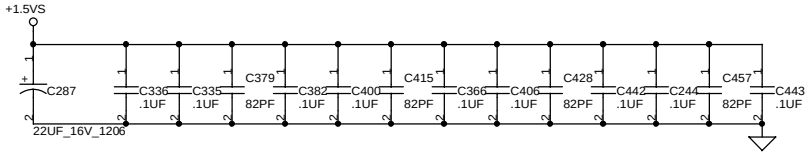
Layout note :

Distribute as close as possible to GMCH Local Memory Quadrant .



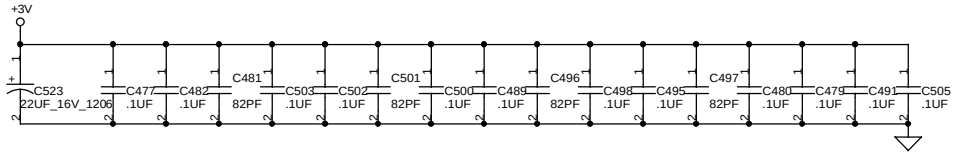
Layout note :

Distribute as close as possible to GMCH AGP/DVO Quadrant .



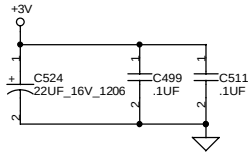
Layout note :

Distribute as close as possible to GMCH System Memory Quadrant .



Layout note :

Distribute as close as possible to IO Quadrant .



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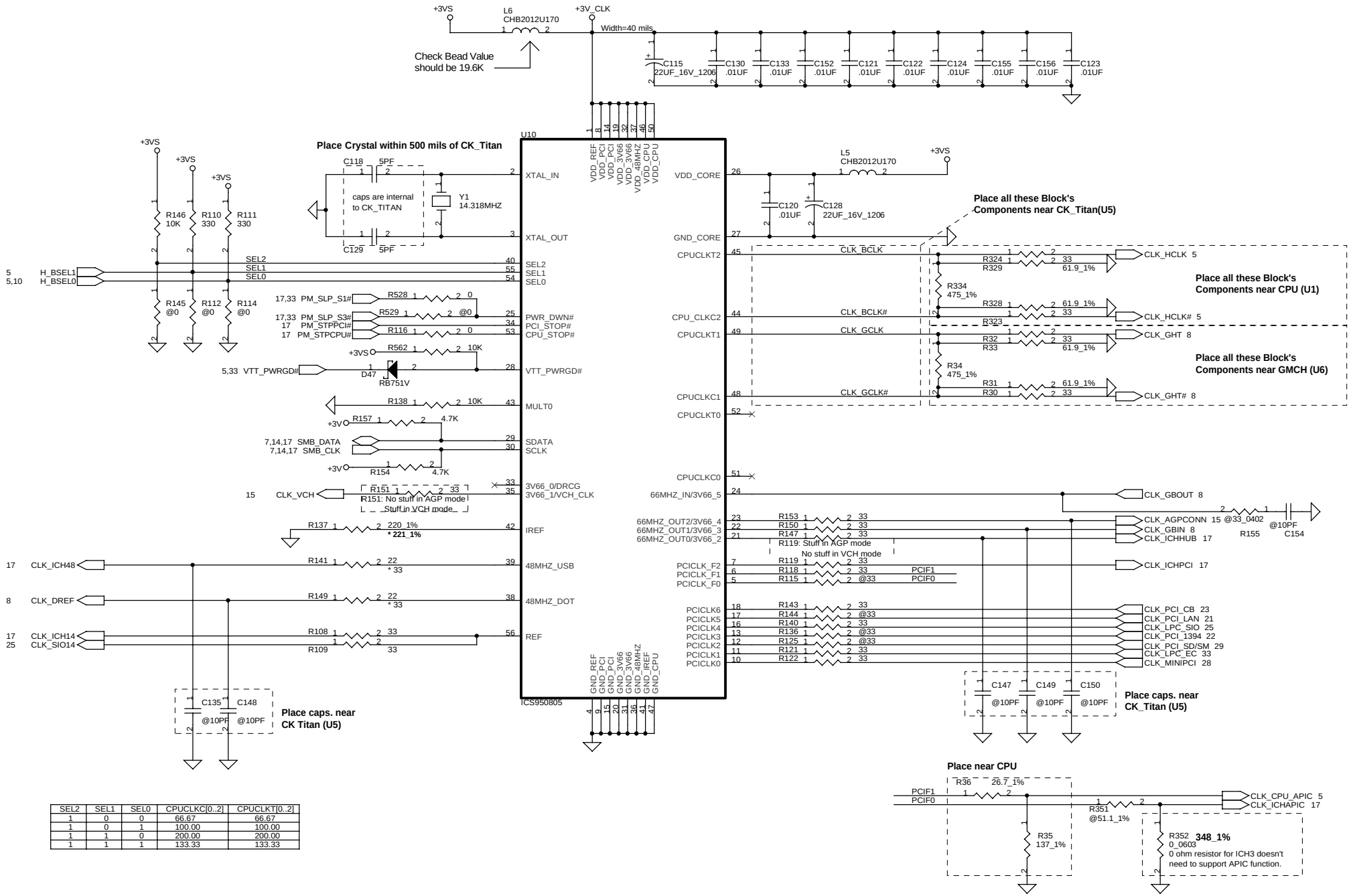

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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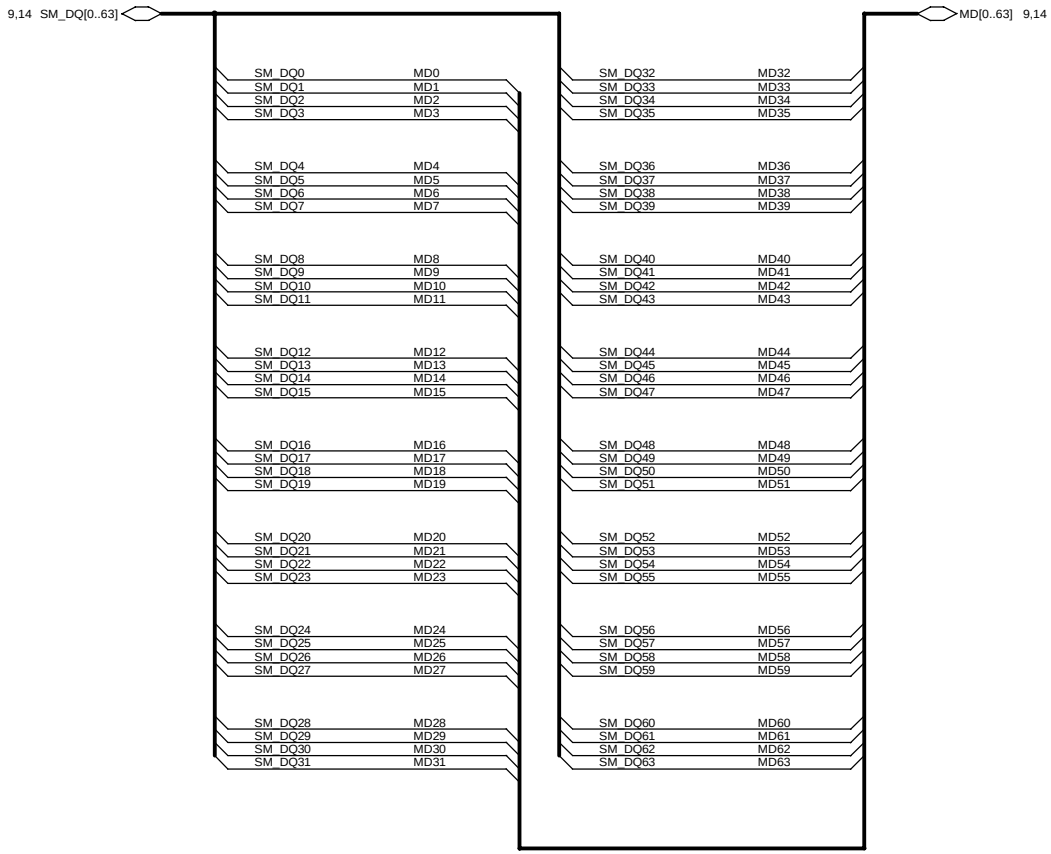
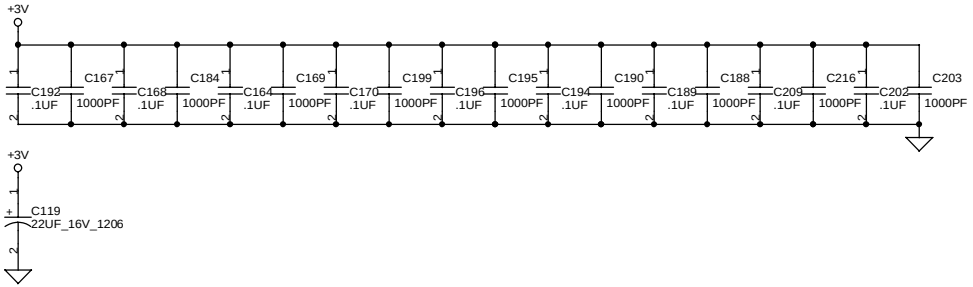


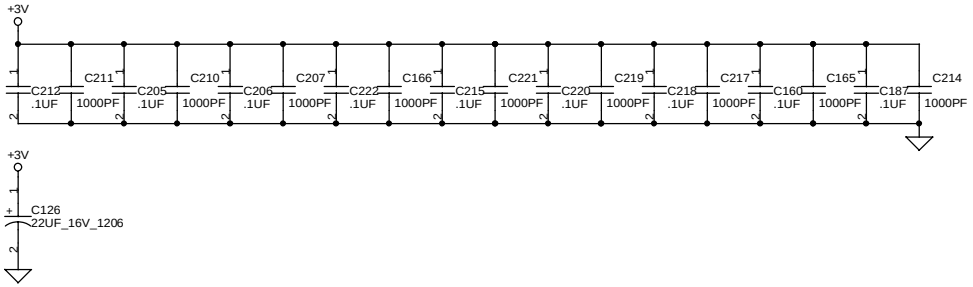
Layout note :

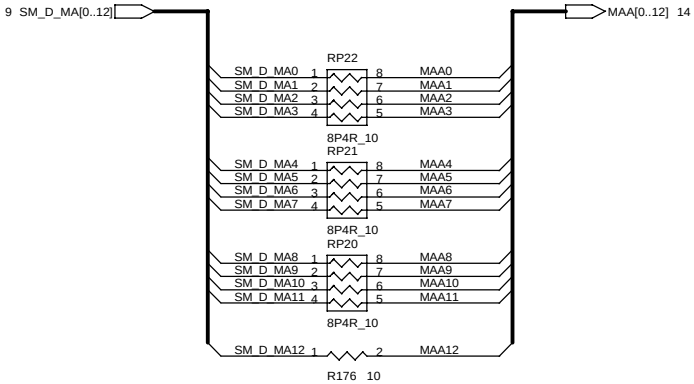
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :

One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .





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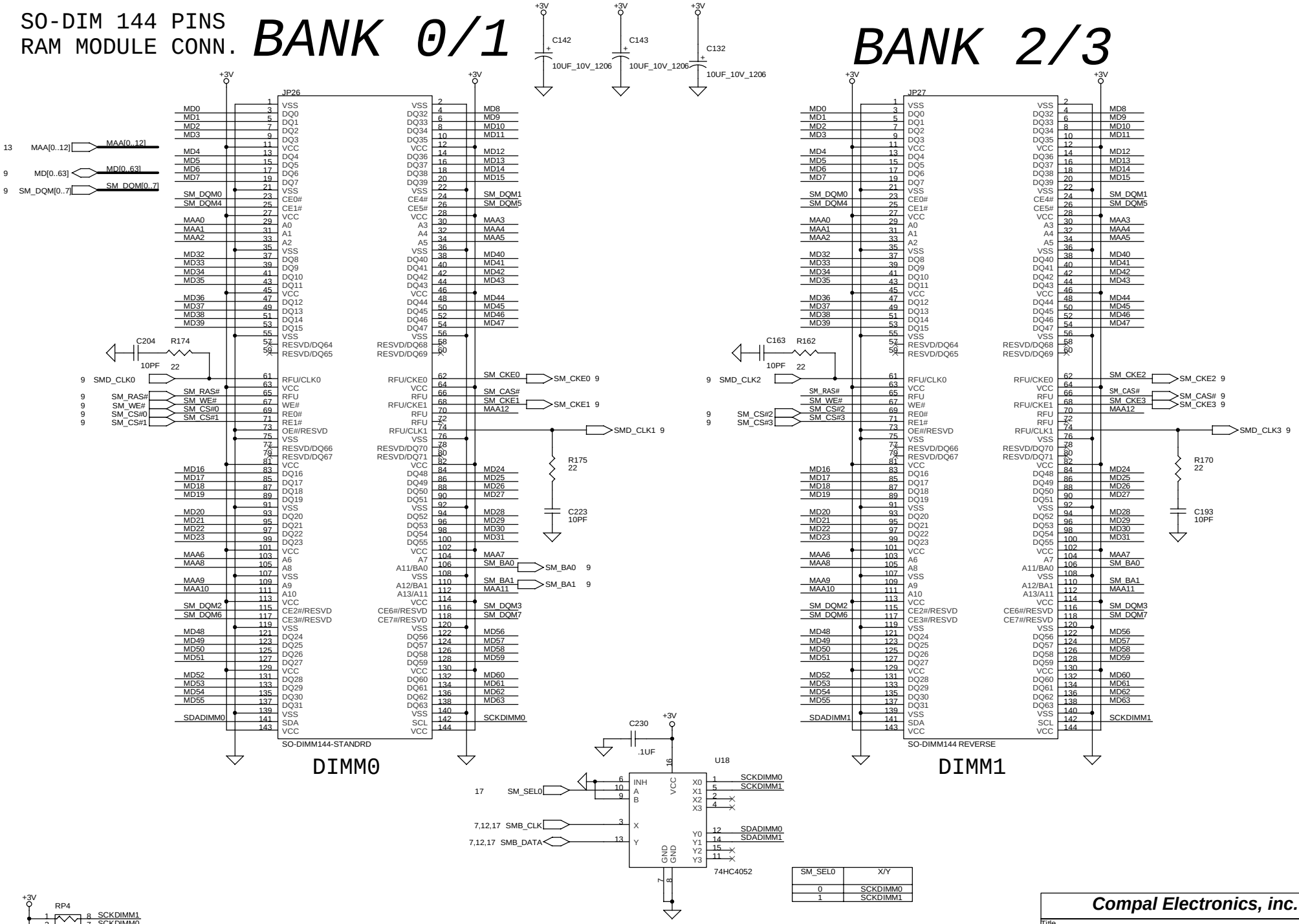
SO-DIM 144 PINS RAM MODULE CONN.

BANK 0/1

BANK 2/3



SM_SEL0	X/Y
0	SCKDIMM0
1	SCKDIMM1

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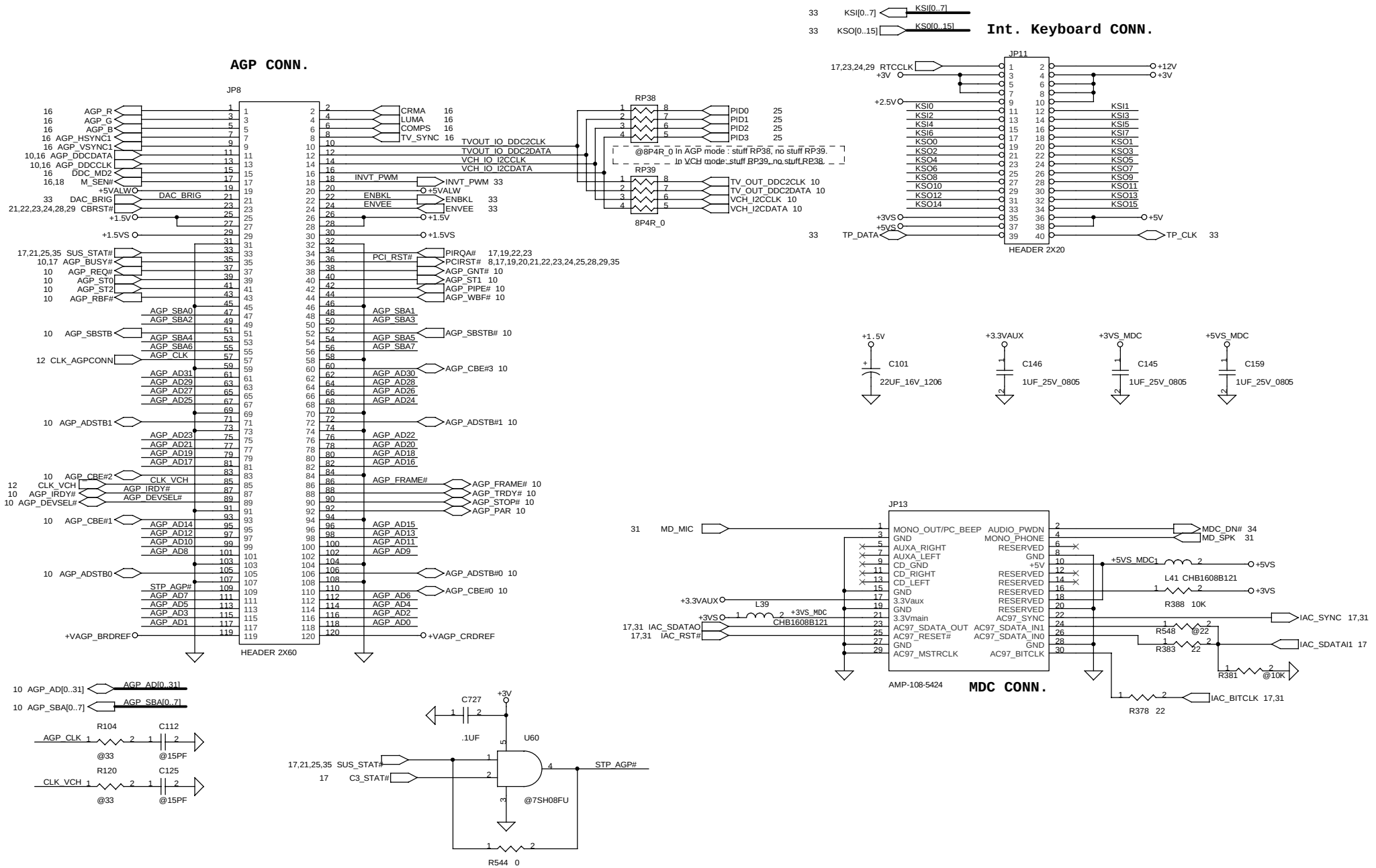

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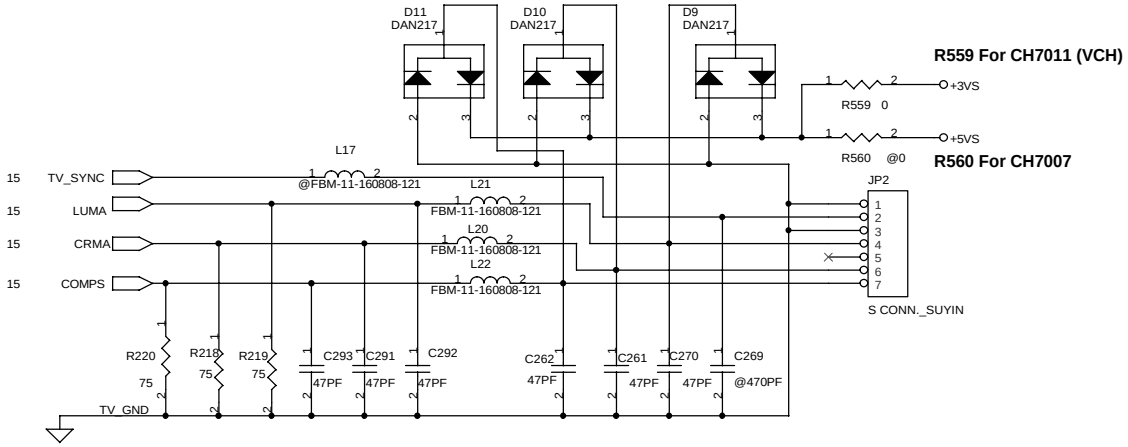
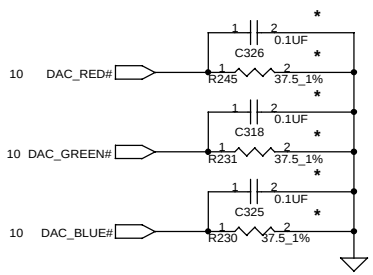
TV_OUT CONN.

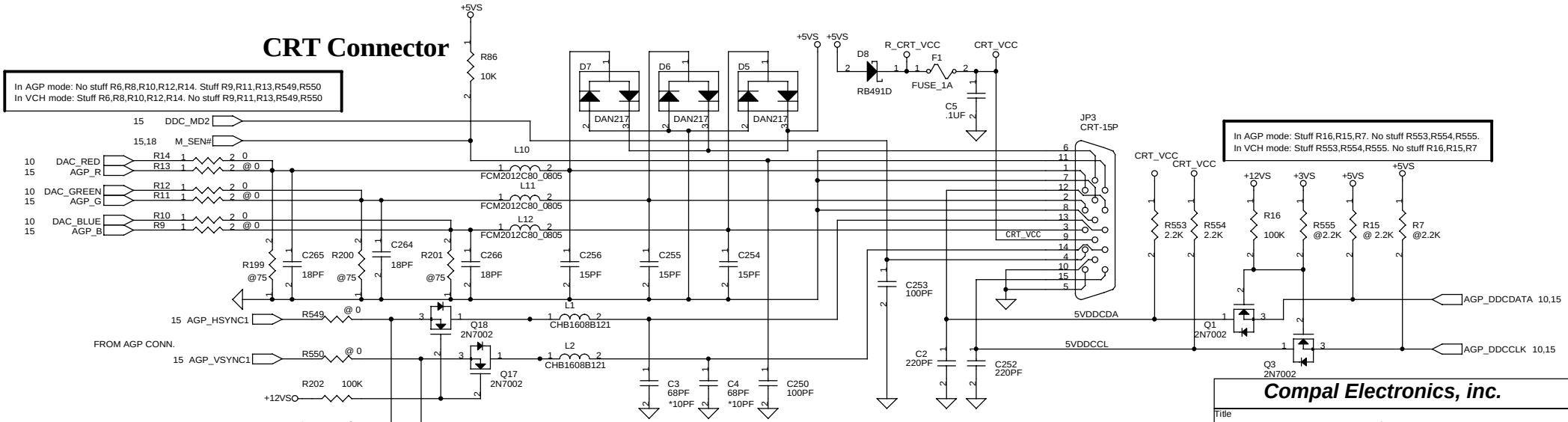


In AGP mode: No stuff C326,R245,C318,R231,C325,R230.
In VCH mode: Stuff C326,R245,C318,R231,C325,R230



CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550



In AGP mode: Stuff R16,R15,R7. No stuff R553,R554,R555.
In VCH mode: Stuff R553,R554,R555. No stuff R16,R15,R7

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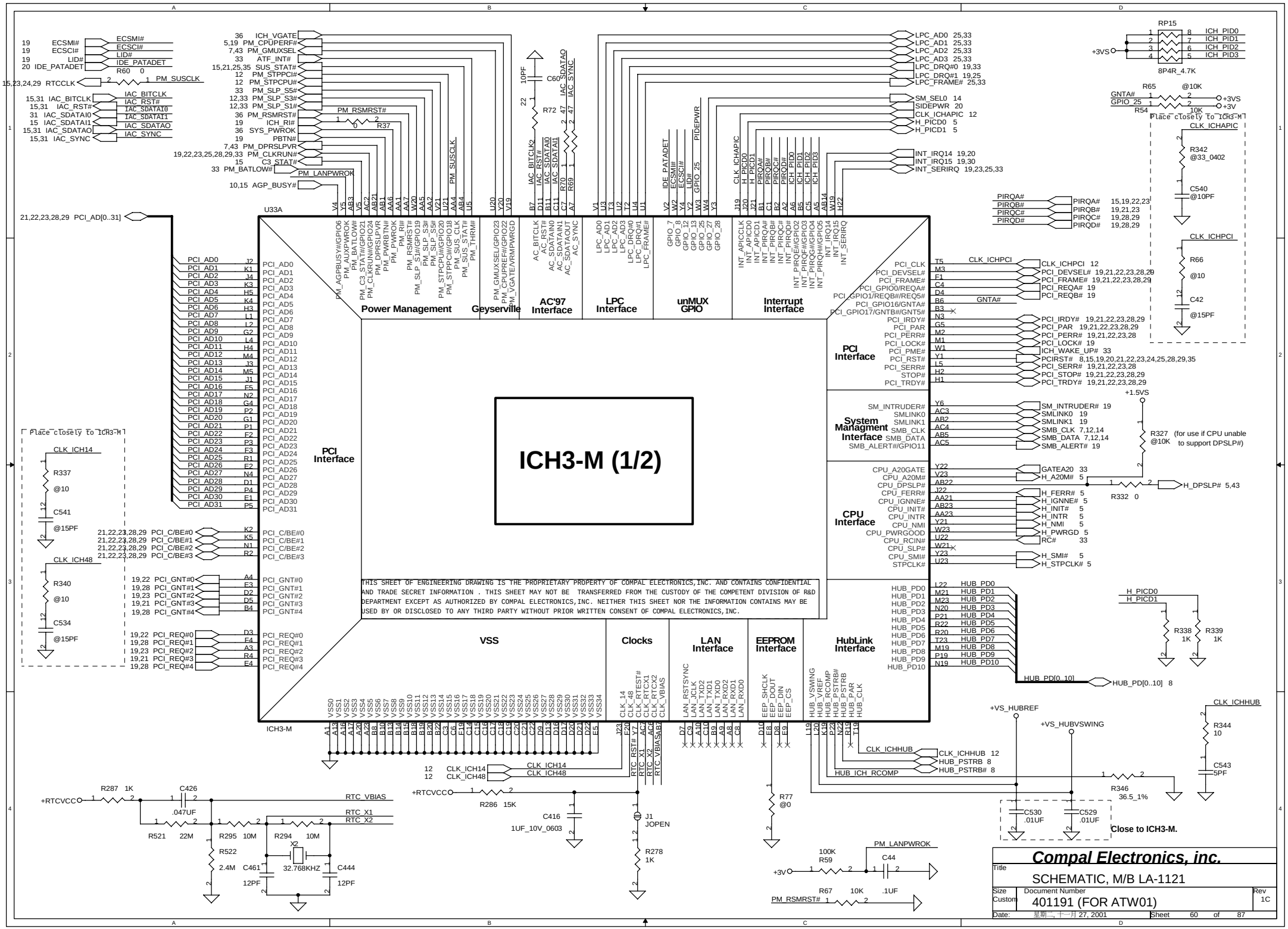
ICH3-M (1/2)
U33A
Power Management
Geyserville
AC'97 Interface
LPC Interface
unMUX GPIO
Interrupt Interface
PCI Interface
System Managment Interface
CPU Interface
VSS
Clocks
LAN Interface
EEPROM Interface
HubLink Interface
ICH3-M
Place closely to ICH3-M
Close to ICH3-M.
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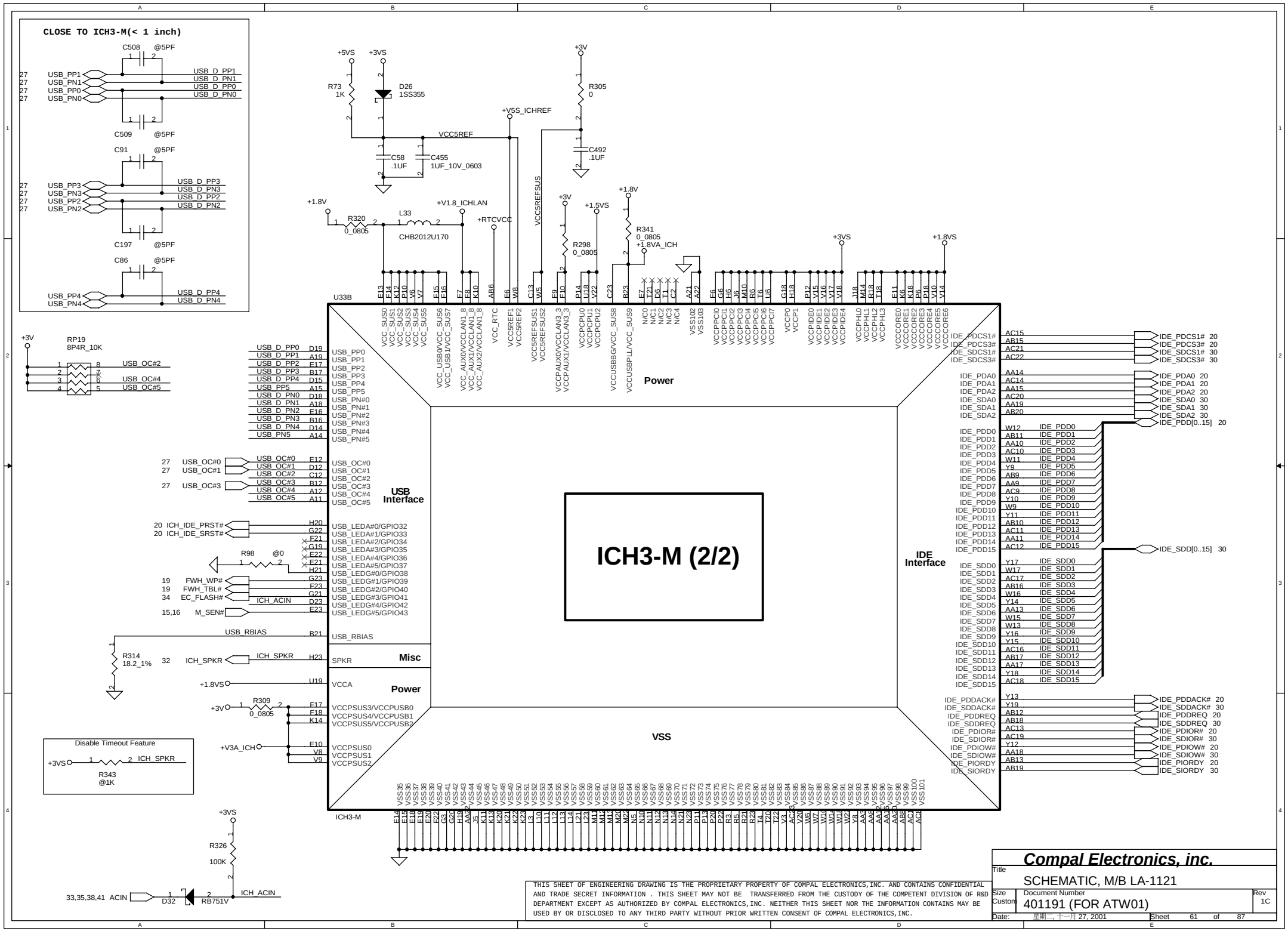
CLOSE TO ICH3-M(< 1 inch)
C508 @5PF
C509 @5PF
C91 @5PF
C197 @5PF
C86 @5PF
USB_PP1
USB_PN1
USB_PP0
USB_PN0
USB_D_PP1
USB_D_PN1
USB_D_PP0
USB_D_PN0
USB_PP3
USB_PN3
USB_PP2
USB_PN2
USB_D_PP3
USB_D_PN3
USB_D_PP2
USB_D_PN2
USB_PP4
USB_PN4
USB_D_PP4
USB_D_PN4
+5VS
+3VS
R73 1K
D26 1SS355
VCC5REF
C58 .1UF
C455 1UF_10V_0603
+V5S_ICHREF
+3V
R305 0
C492 .1UF
+1.8V
R320 0_0805
L33
CHB2012U170
+V1.8_ICHLAN
+RTCVCC
VCC5REFSUS
+1.5VS
R298 0_0805
R341 0_0805
+1.8VA_ICH
+3VS
+1.8VS
RP19 8P4R_10K
USB_OC#2
USB_OC#4
USB_OC#5
USB_D_PP0
USB_D_PP1
USB_D_PP2
USB_D_PP3
USB_D_PP4
USB_PP5
USB_D_PN0
USB_D_PN1
USB_D_PN2
USB_D_PN3
USB_D_PN4
USB_PN5
USB_OC#0
USB_OC#1
USB_OC#3
USB_OC#2
USB_OC#4
USB_OC#5
USB Interface
ICH_IDE_PRST#
ICH_IDE_SRST#
R98 @0
FWH_WP#
FWH_TBL#
EC_FLASH#
ICH_ACIN
M_SEN#
USB_RBIAS
R314 18.2_1%
ICH_SPKR
Misc
+1.8VS
Power
R309 0_0805
+V3A_ICH
Disable Timeout Feature
+3VS
ICH_SPKR
R343 @1K
ICH3-M (2/2)
Power
VSS
IDE Interface
IDE_PDCS1#
IDE_PDCS3#
IDE_SDCS1#
IDE_SDCS3#
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_SDA0
IDE_SDA1
IDE_SDA2
IDE_PDD[0..15]
IDE_SDD[0..15]
IDE_PDDACK#
IDE_SDDACK#
IDE_PDDREQ
IDE_SDDREQ
IDE_PDIOR#
IDE_SDIOR#
IDE_PDIOW#
IDE_SDIOW#
IDE_PIORDY
IDE_SIORDY
ICH3-M
+3VS
R326 100K
33,35,38,41 ACIN
D32 RB751V
ICH_ACIN
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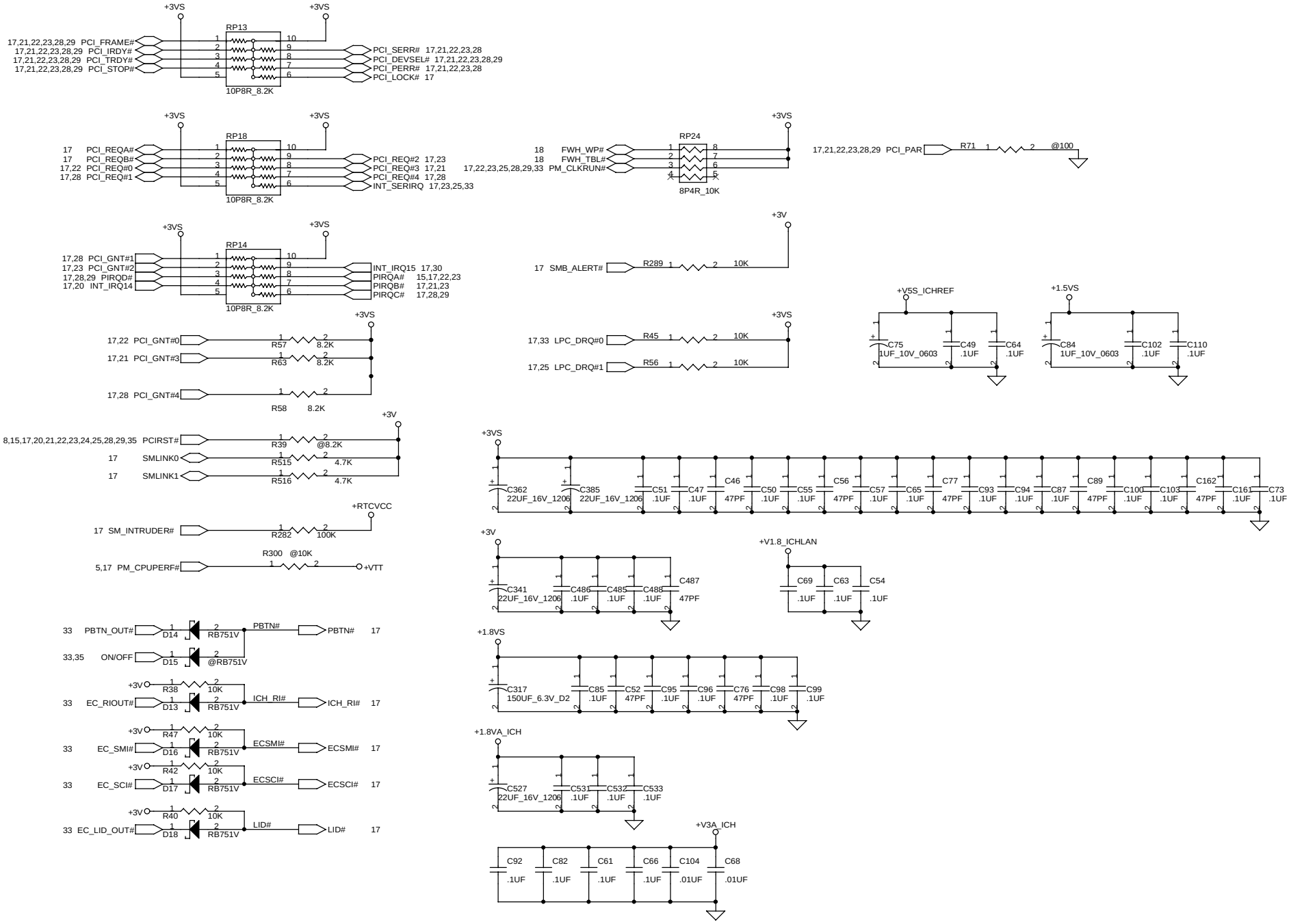

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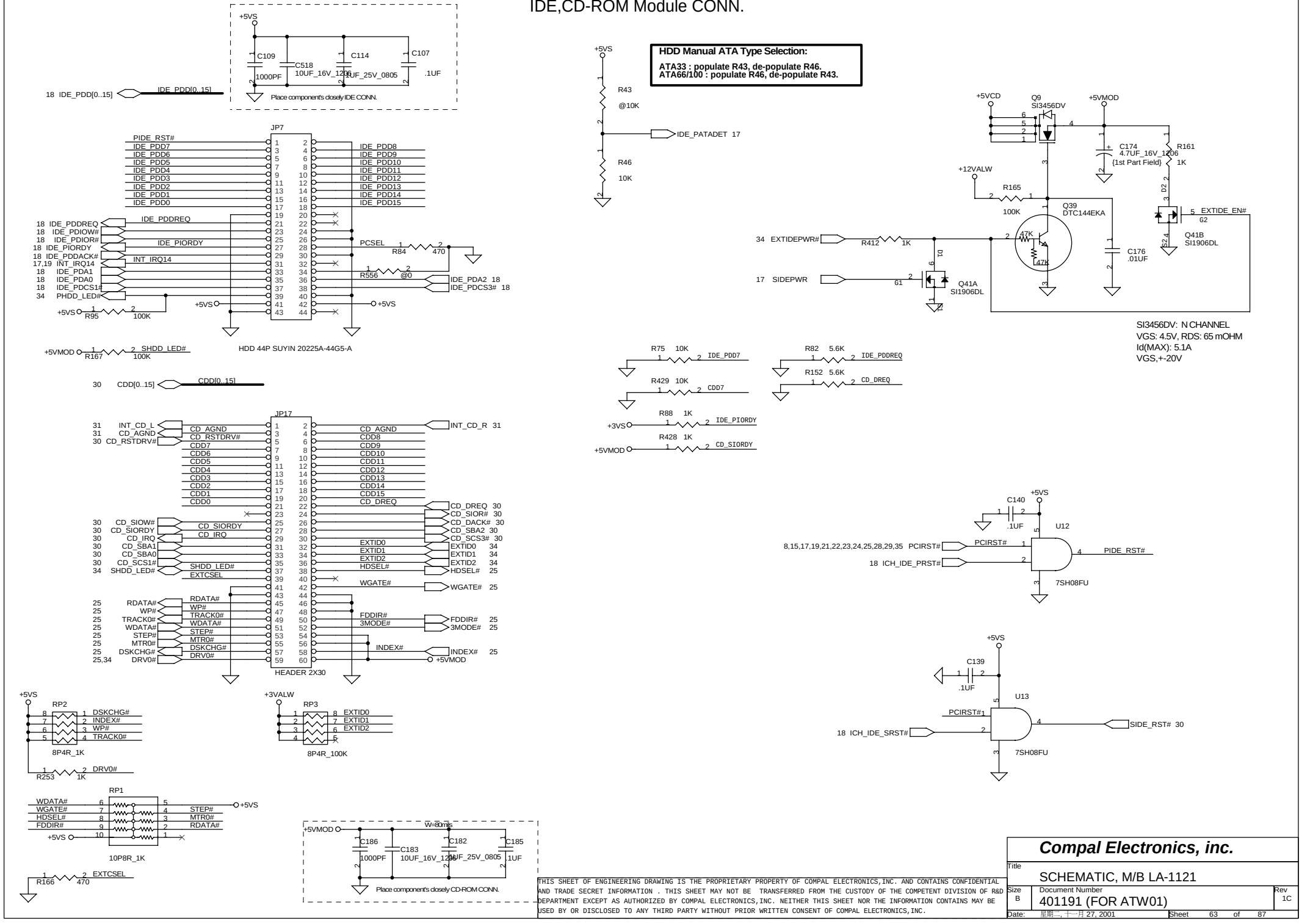
IDE,CD-ROM Module CONN.



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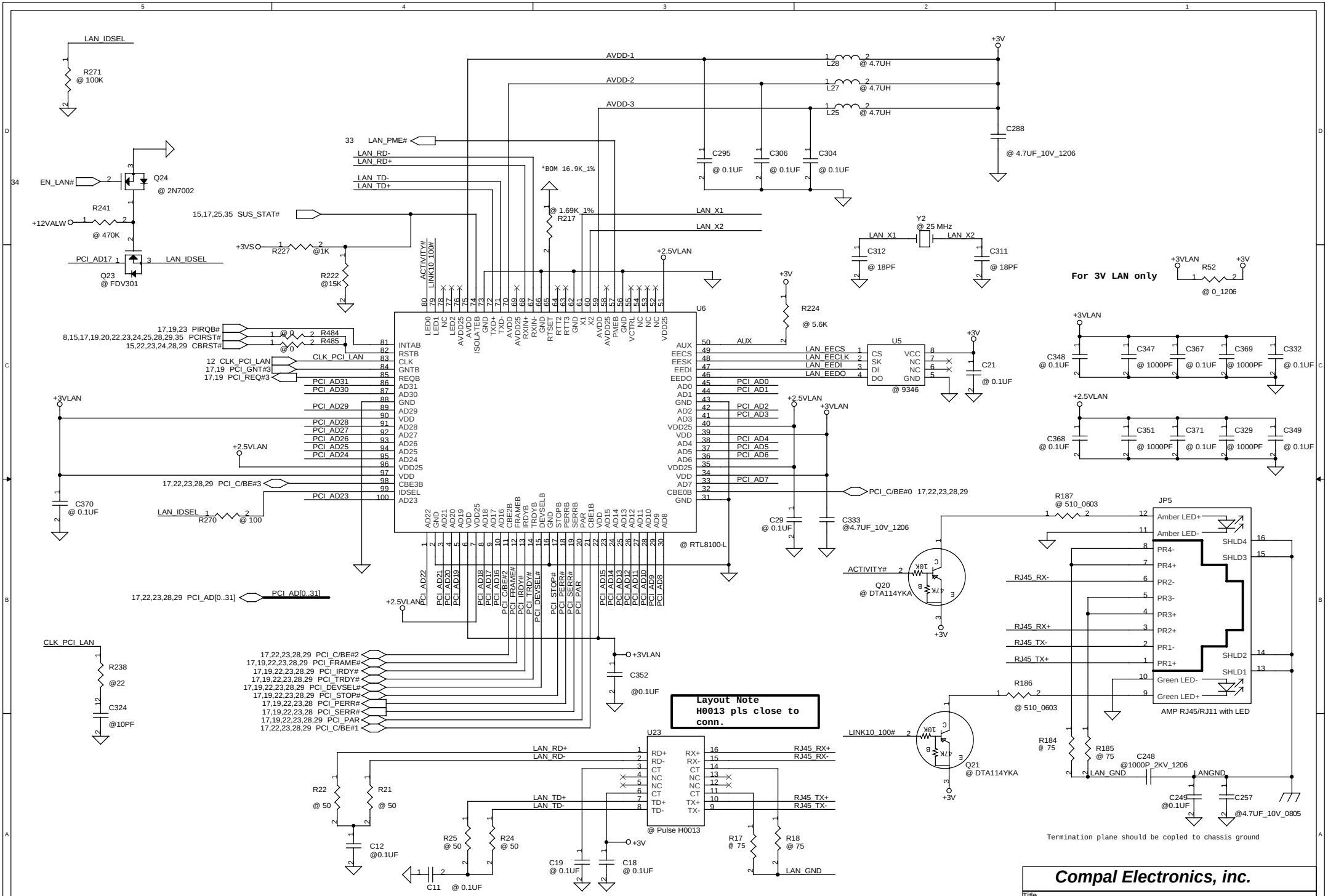

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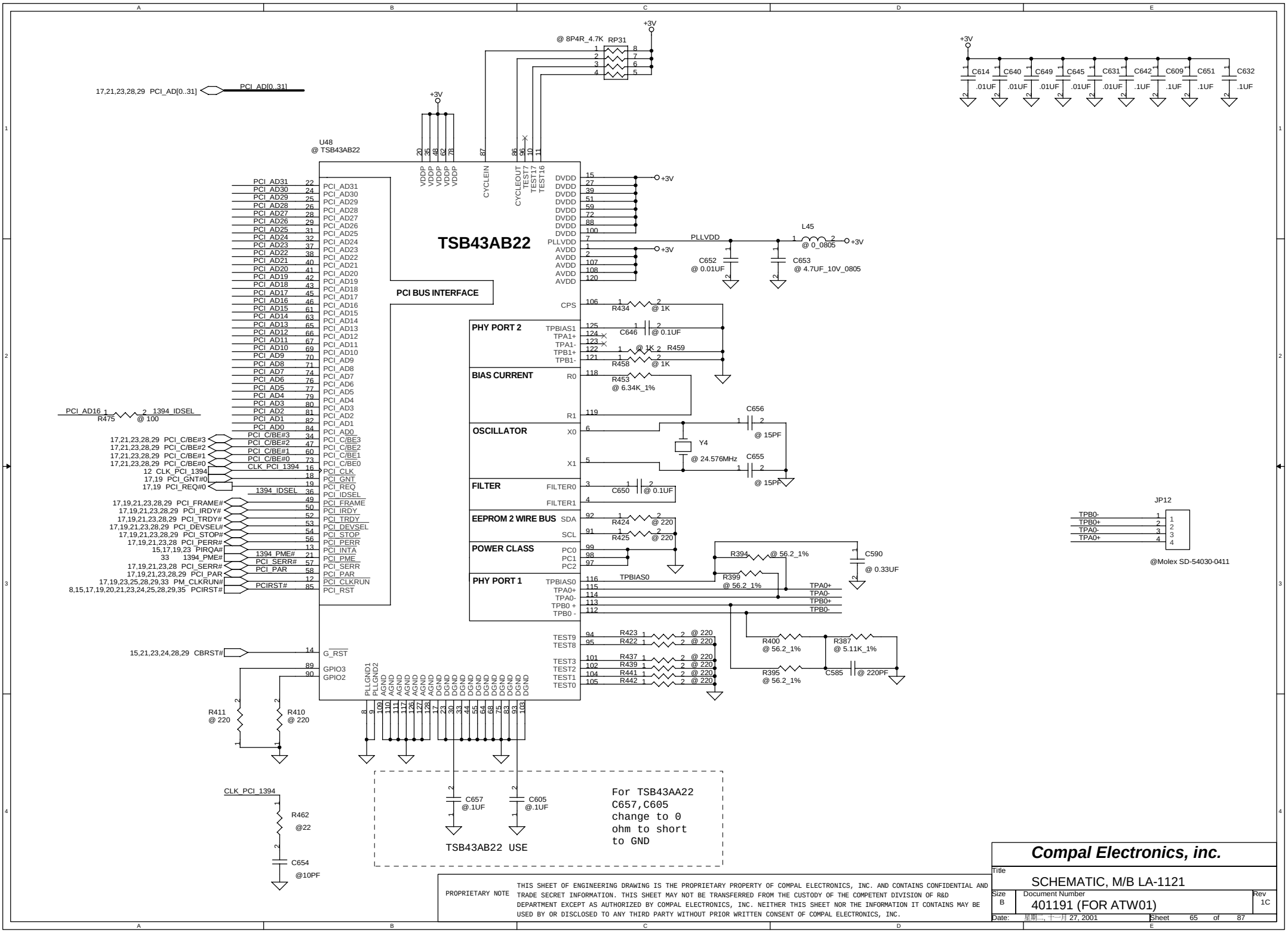

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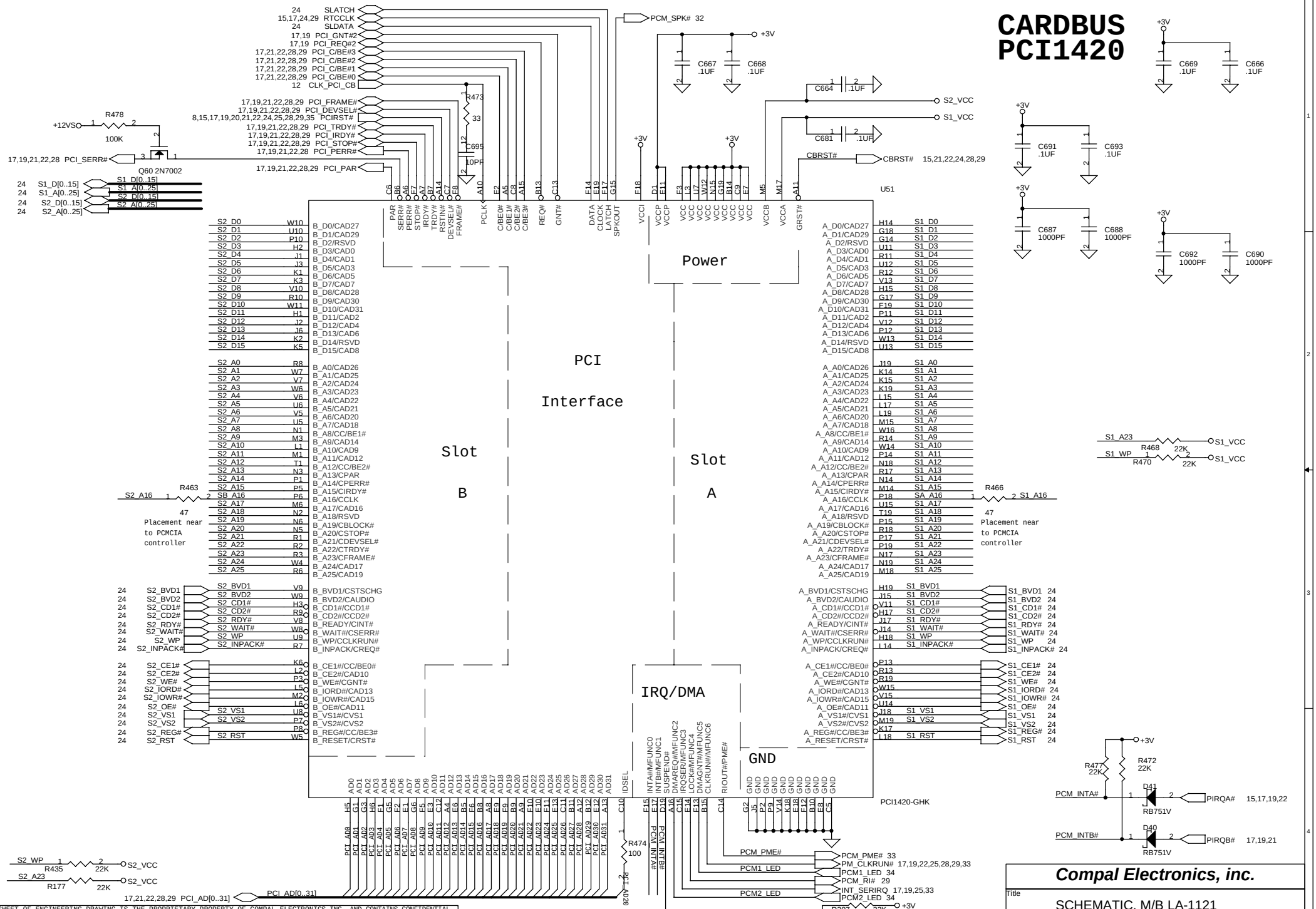
CARDBUS PCI1420



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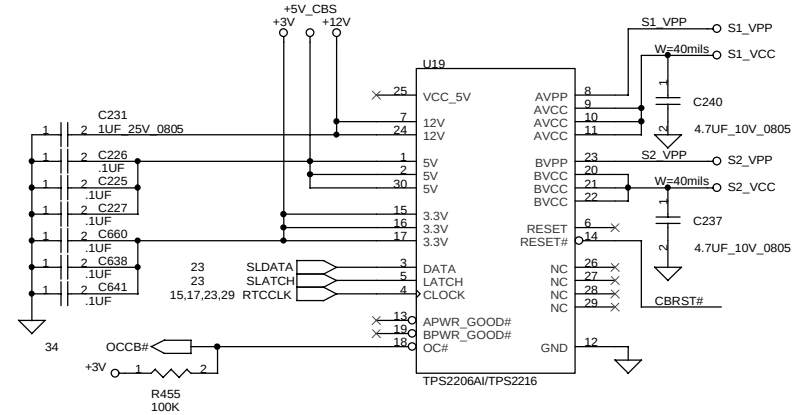
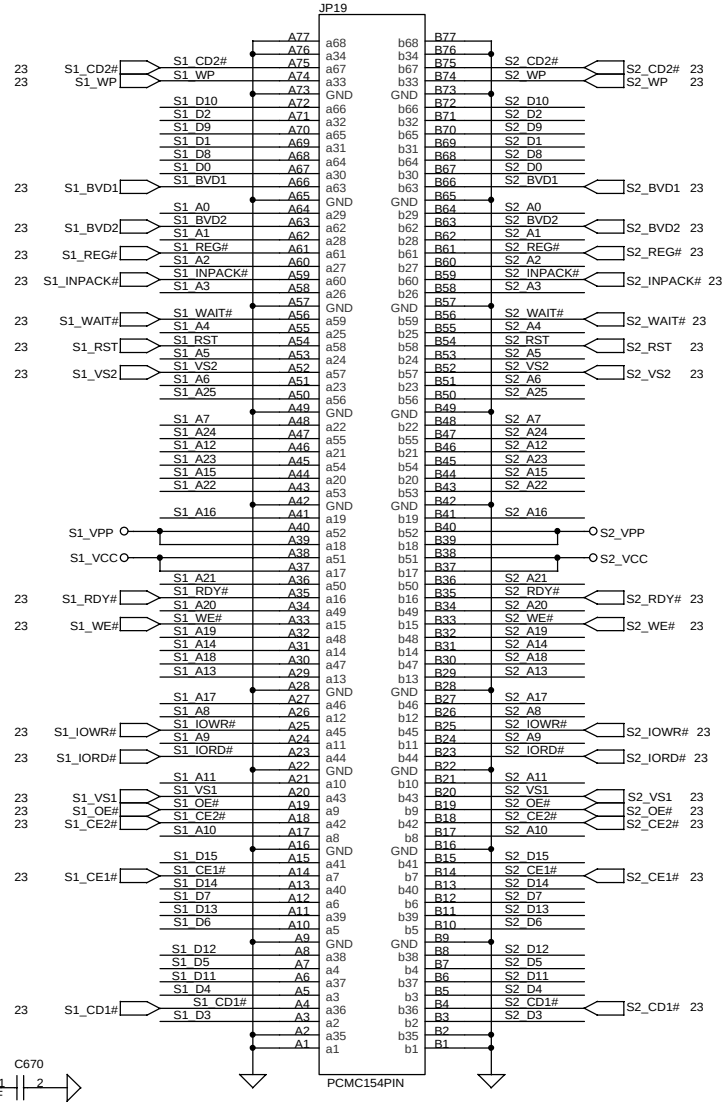
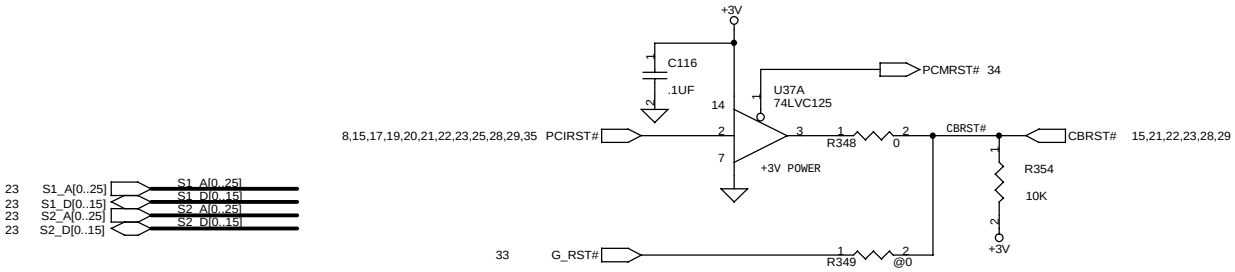
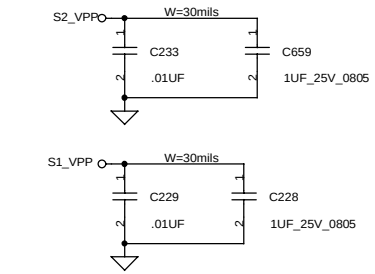
PCMCIA POWER CTRL.

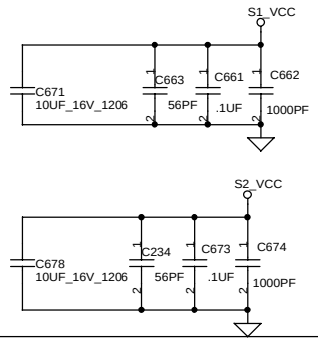


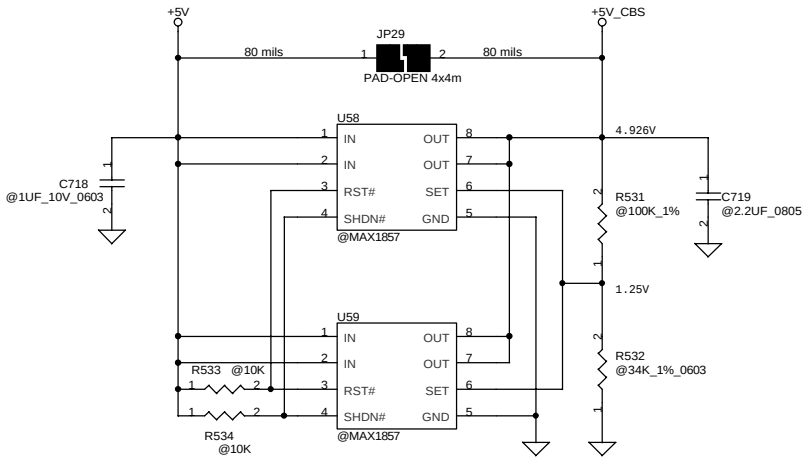
CARDBUS SOCKET











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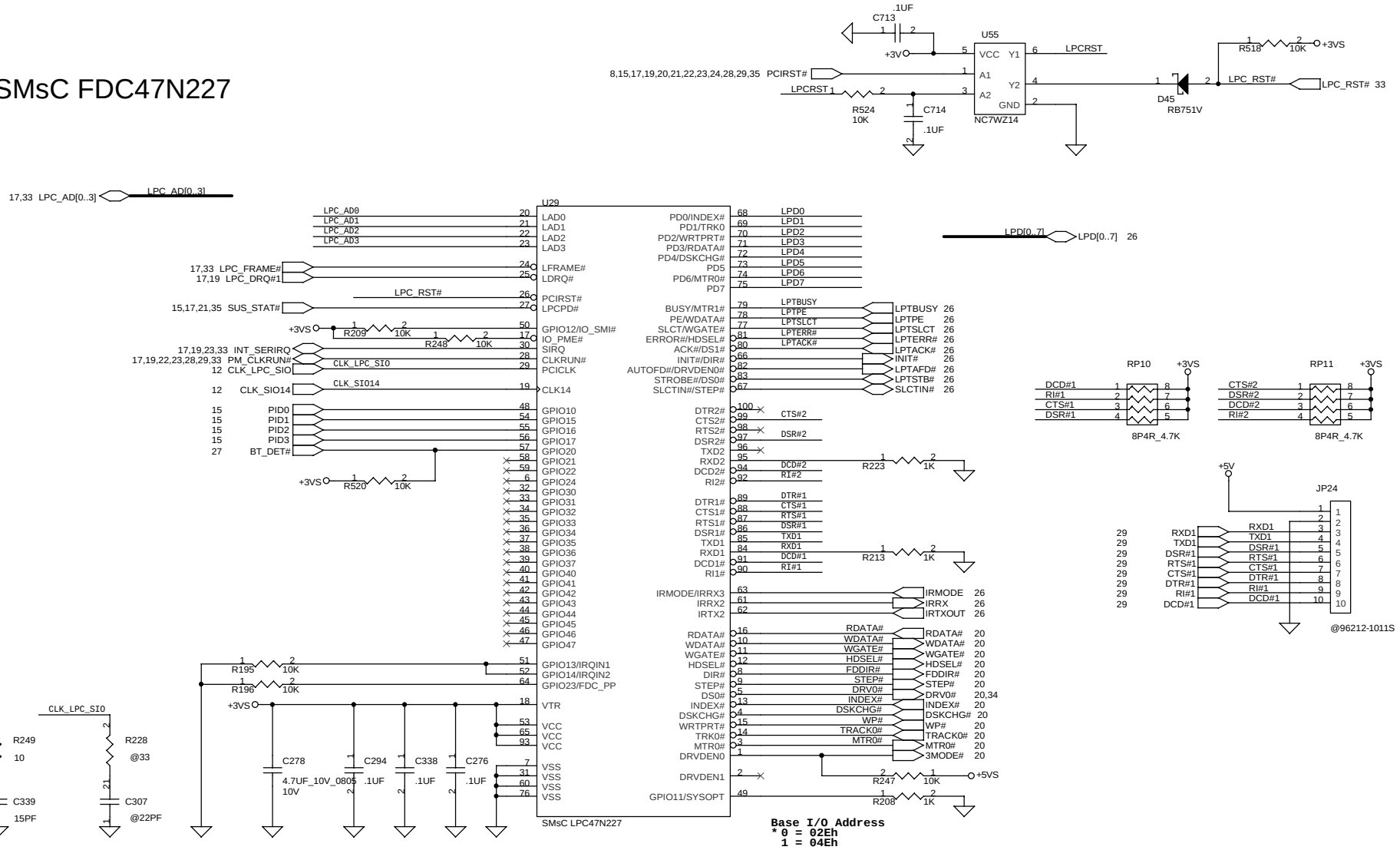
SUPER I/O SMsC FDC47N227



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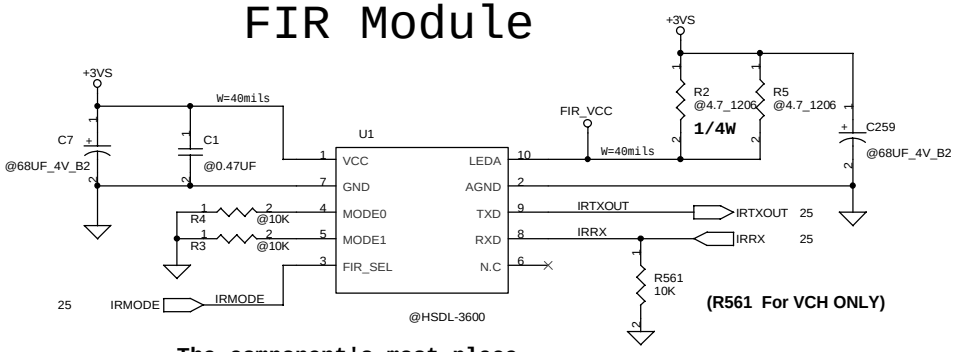
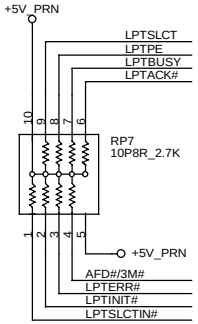
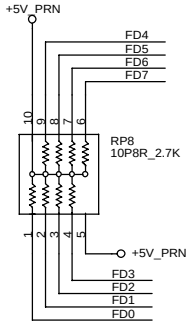
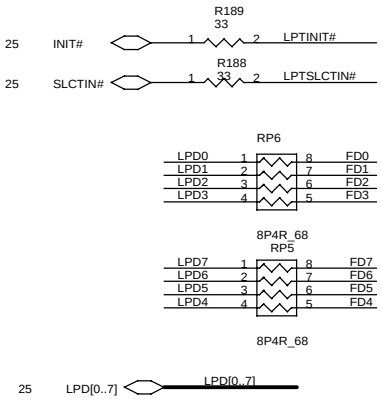
FIR Module



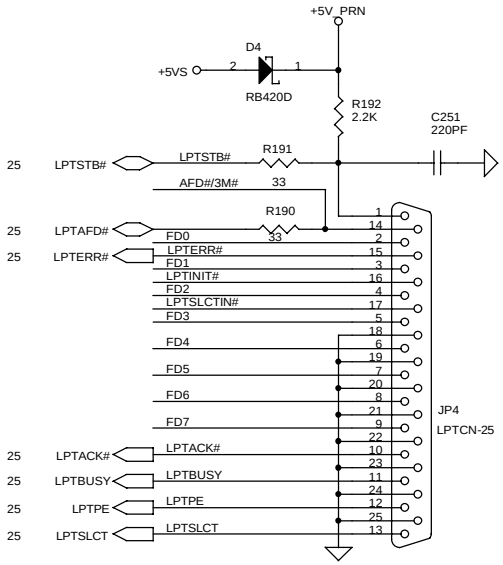
The component's most place cloely IRDA MODULE.

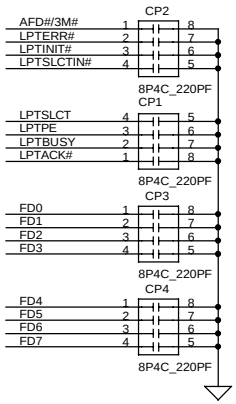






PARALLEL PORT





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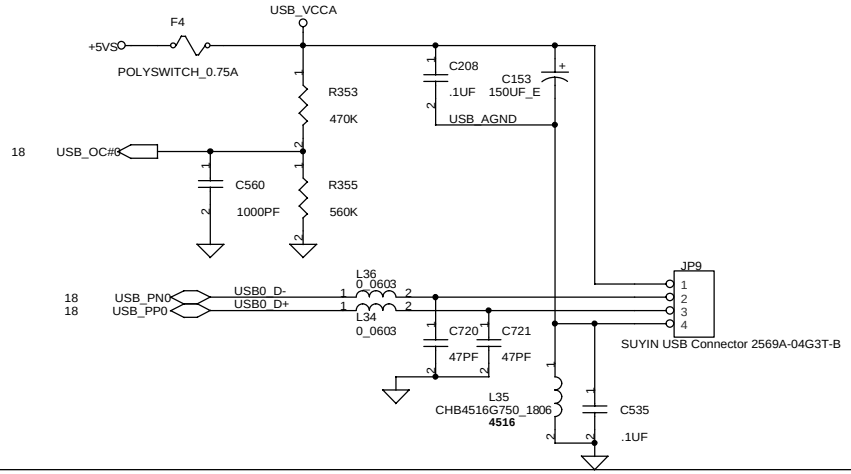
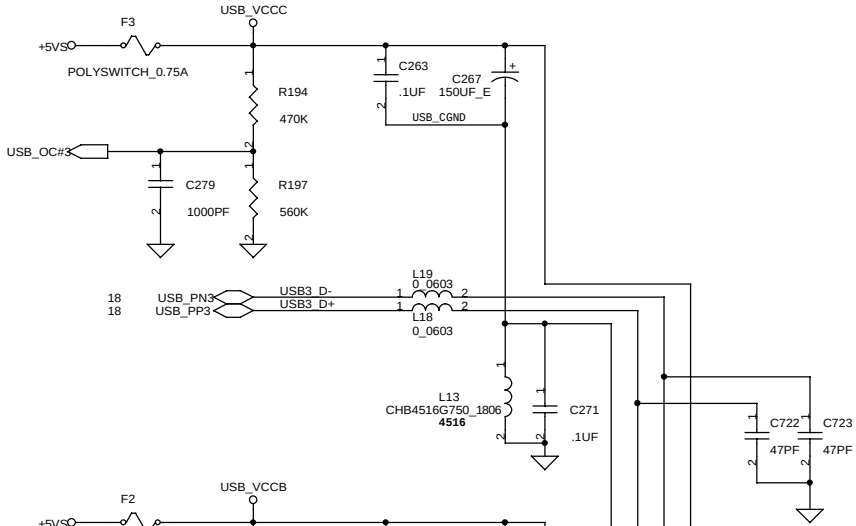
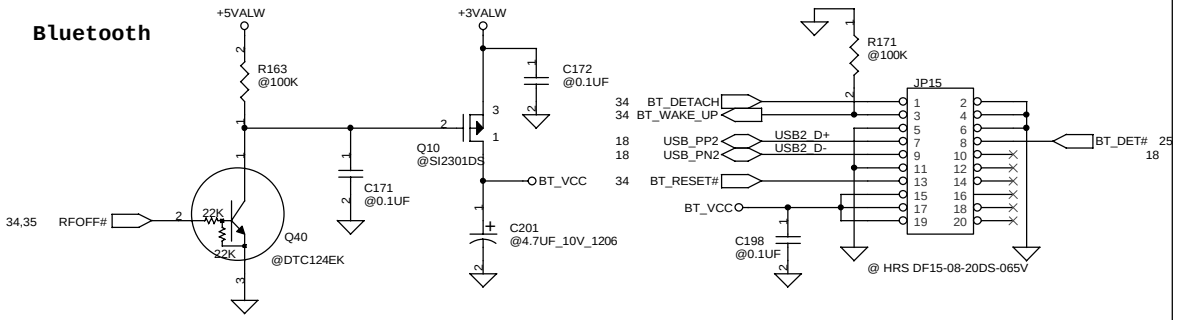
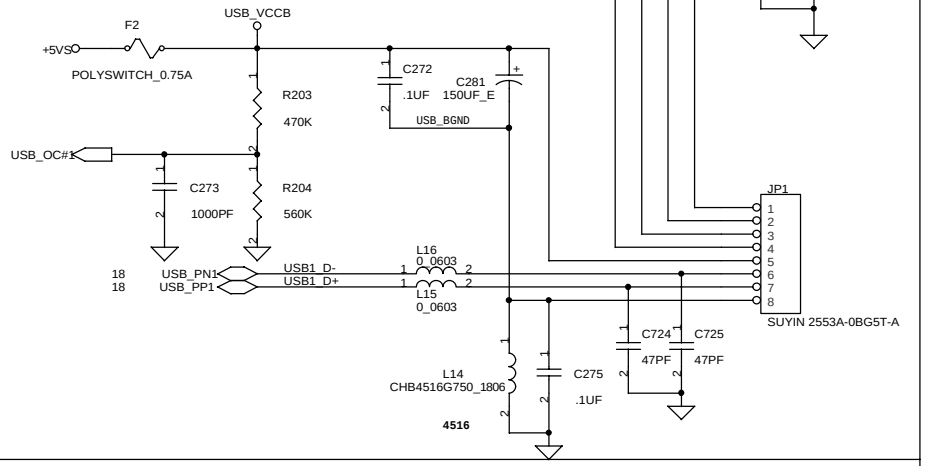
USB PORT





Bluetooth





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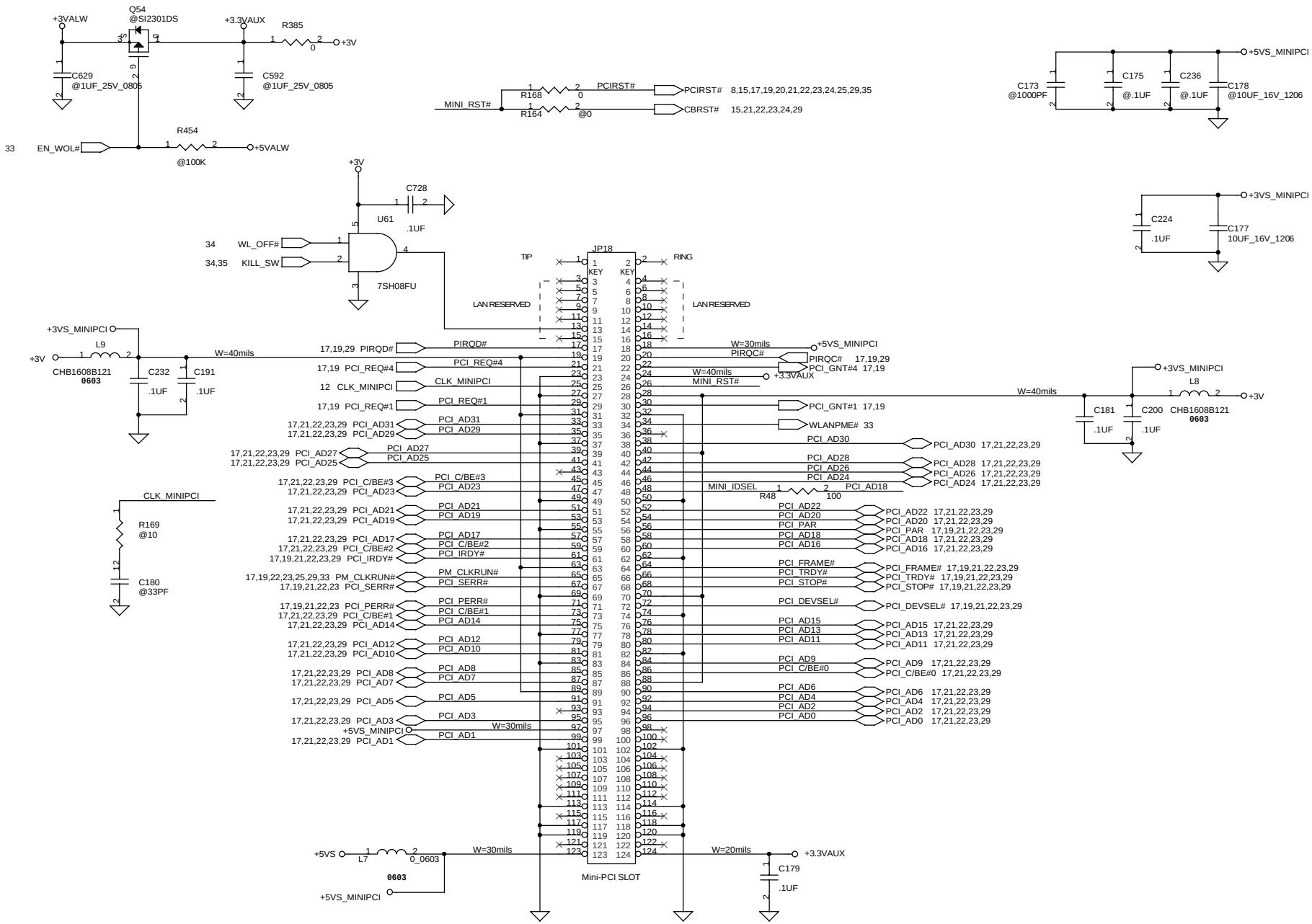

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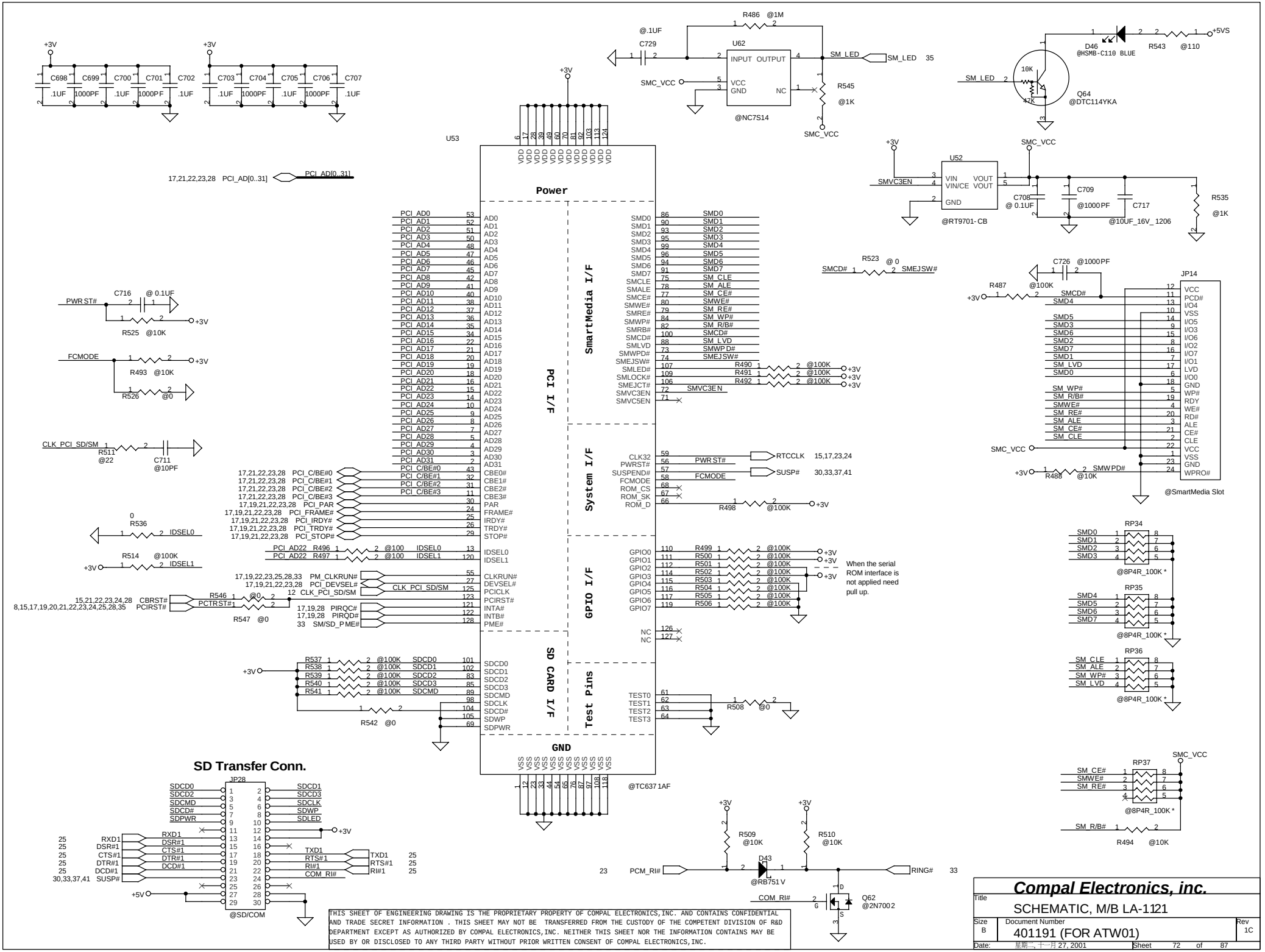

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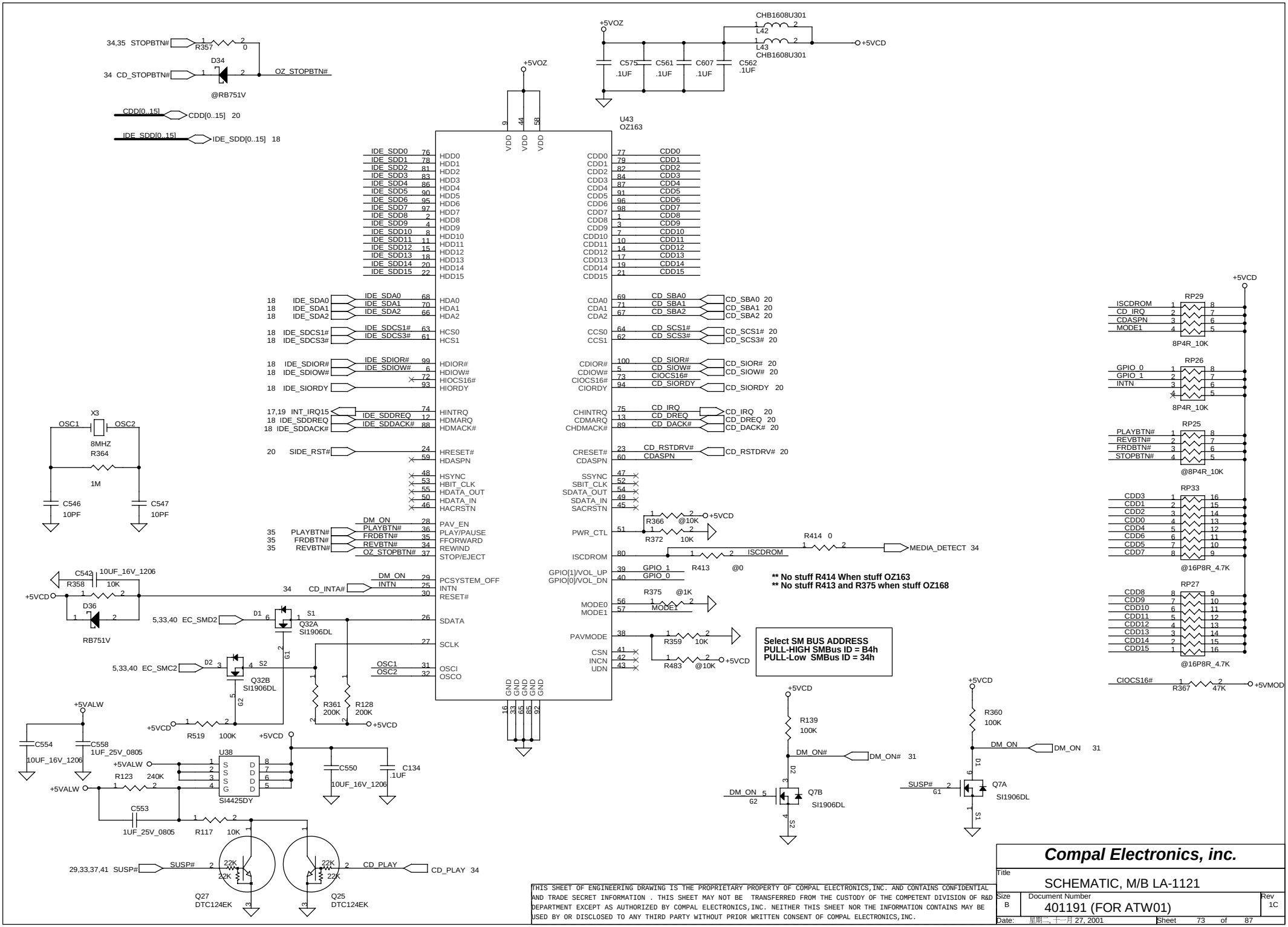

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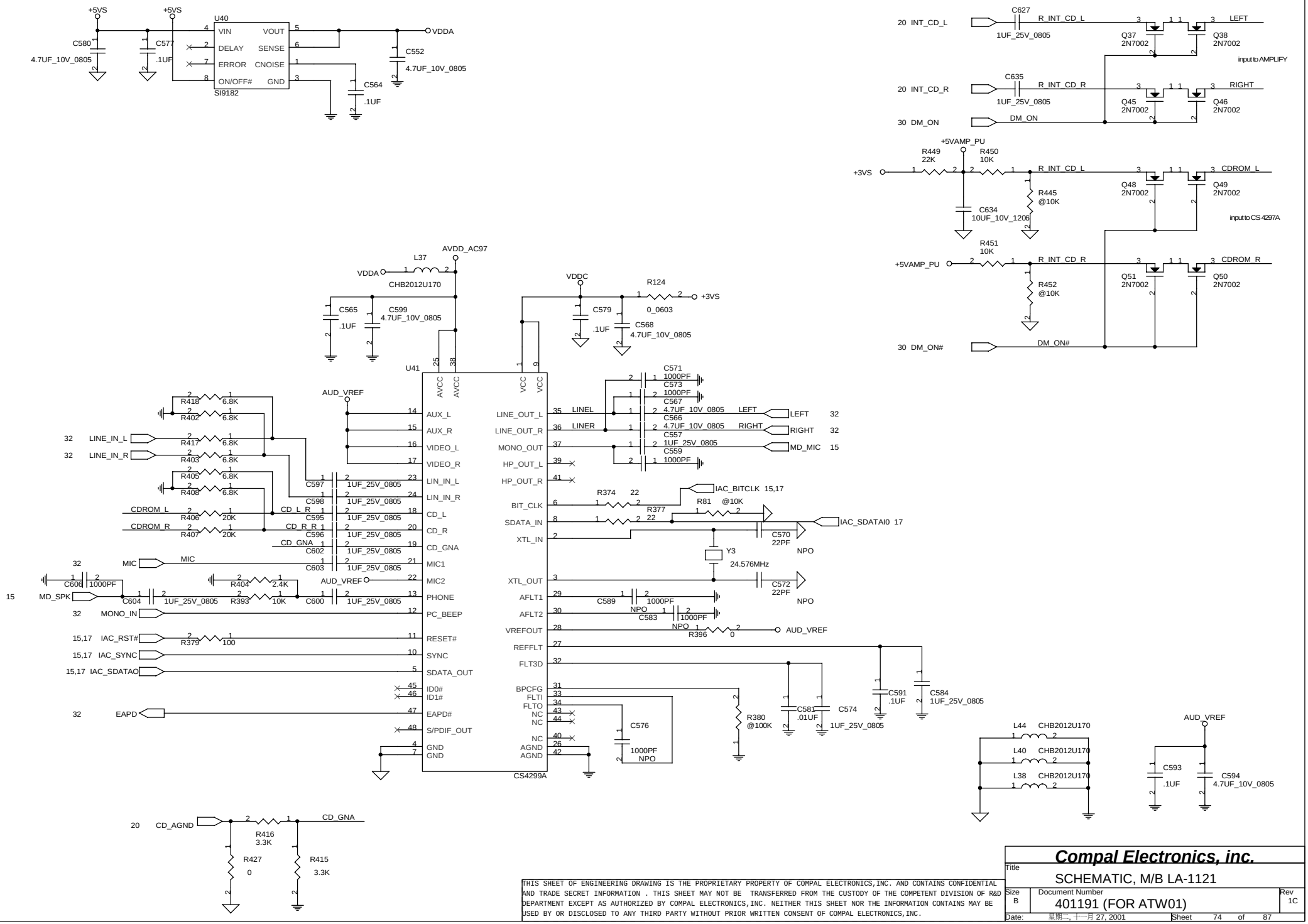
AC97 Codec



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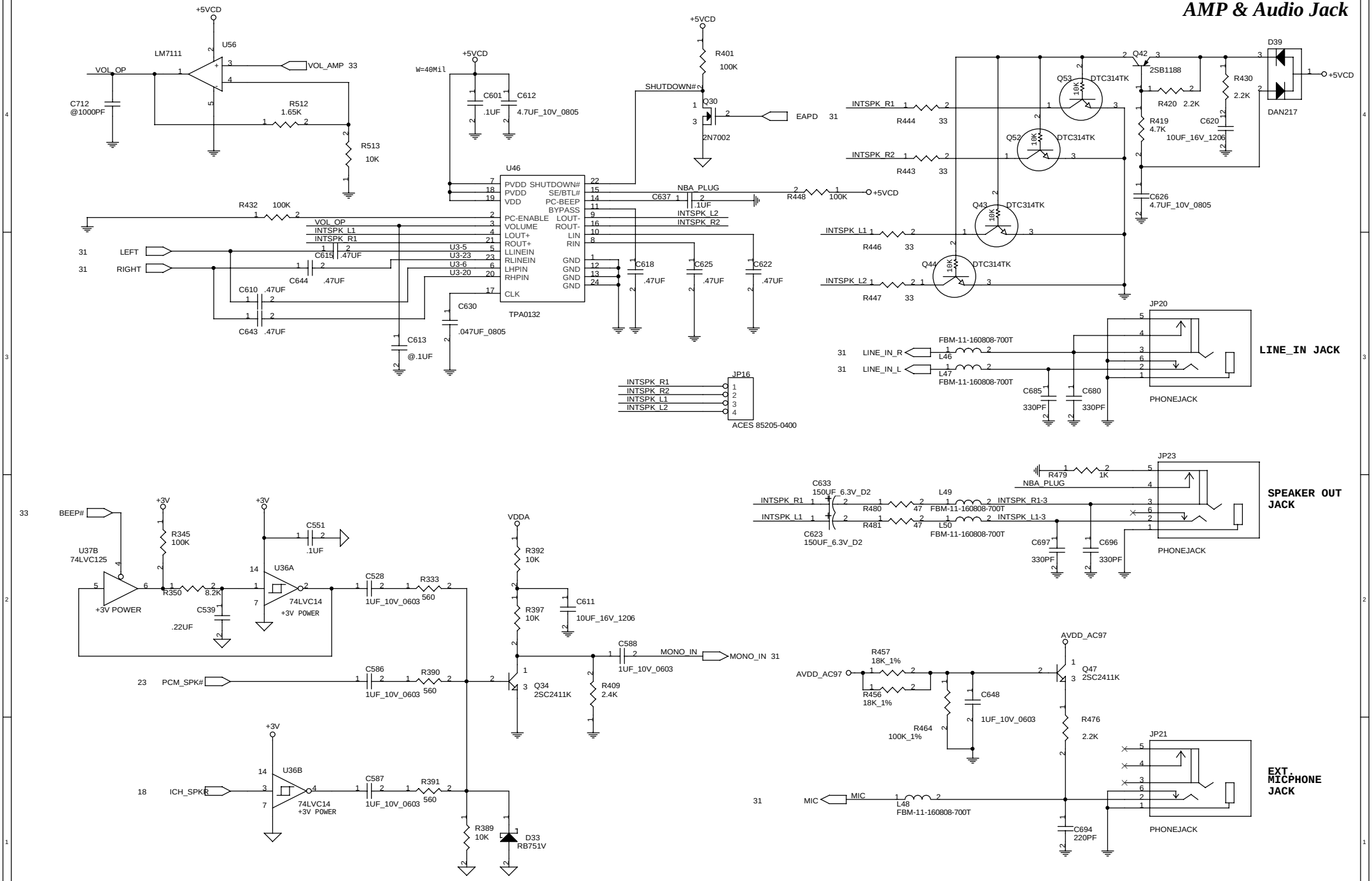
AMP & Audio Jack



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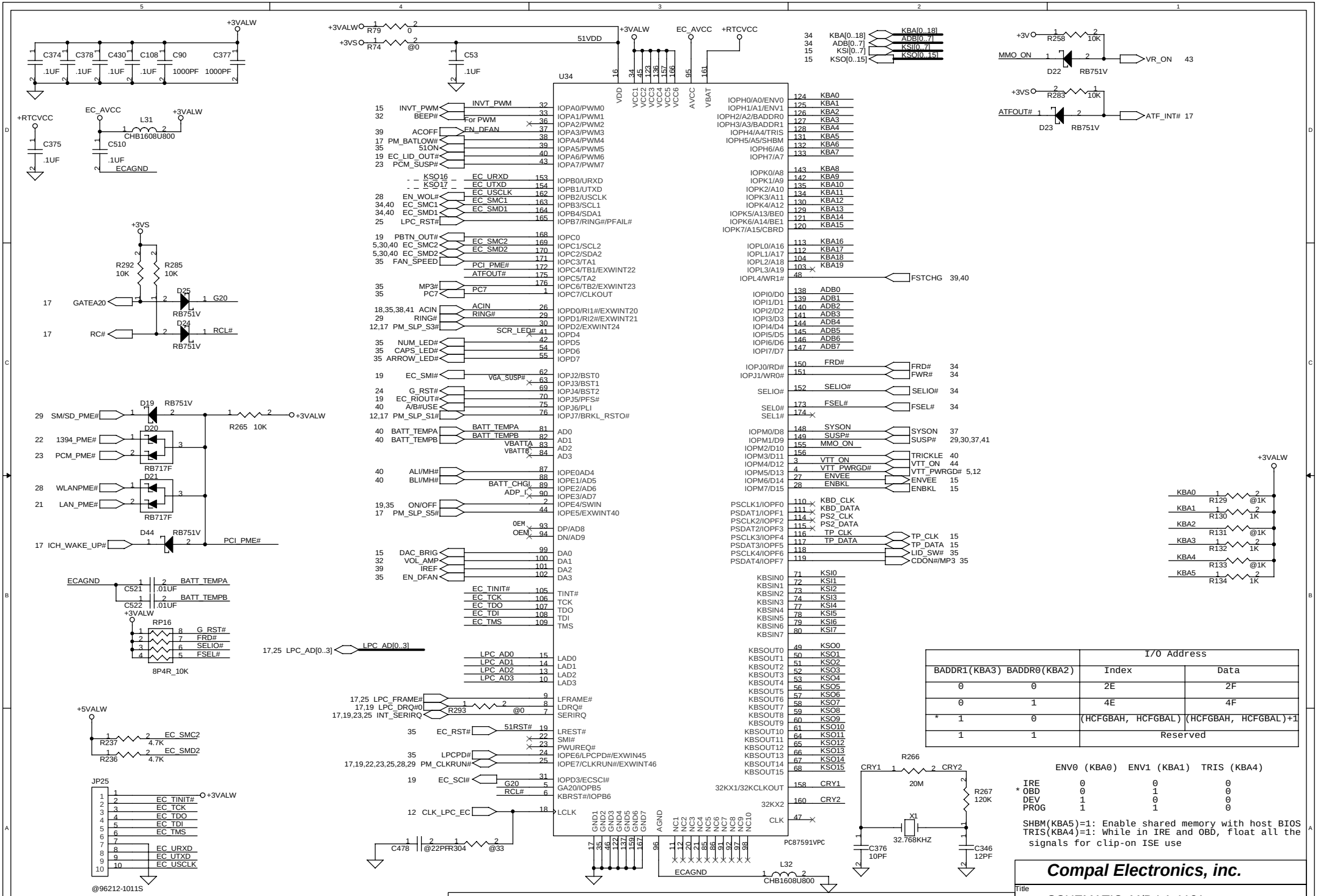

	I/O Address	
BADDR1(KBA3) BADDR0(KBA2)	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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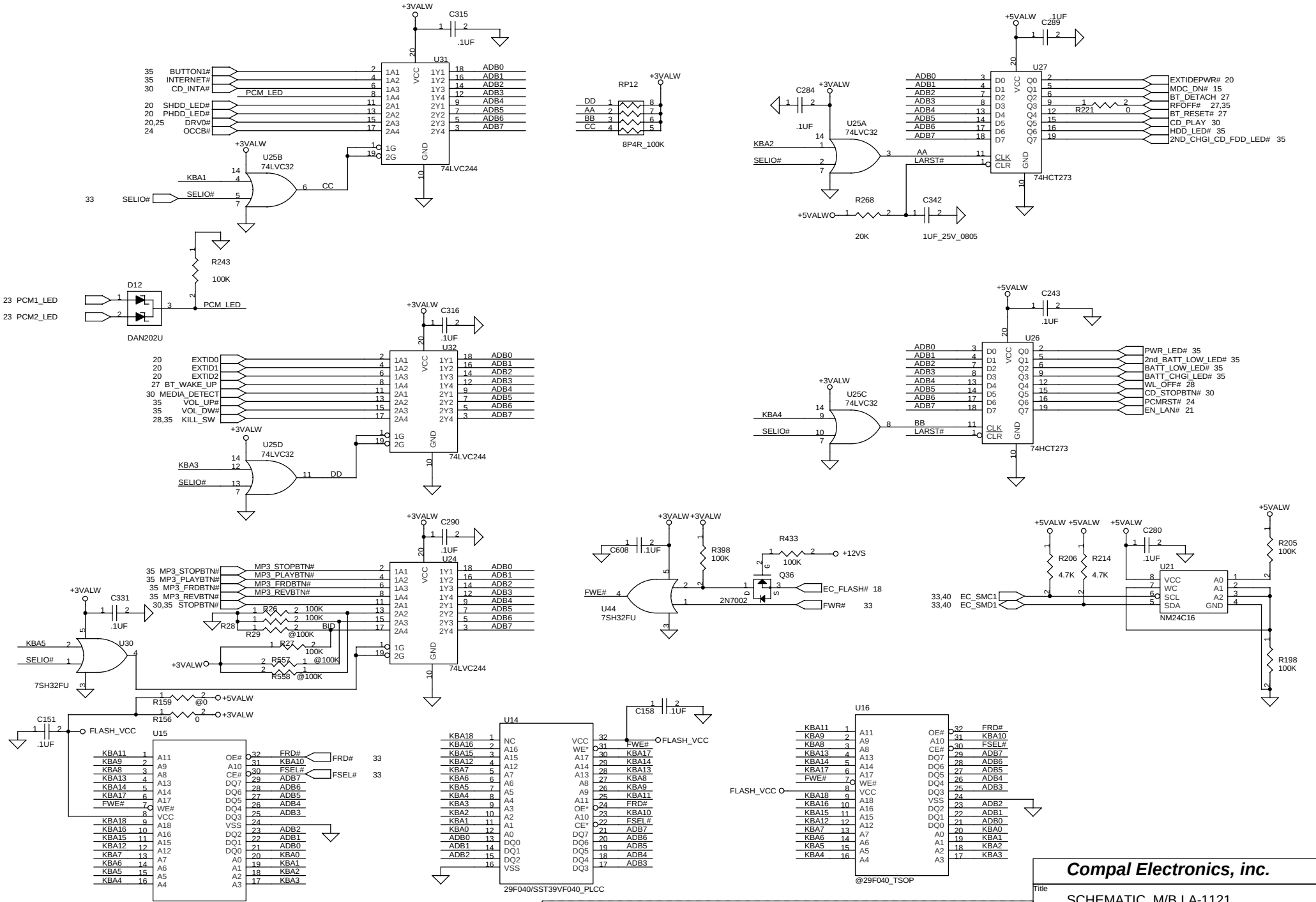

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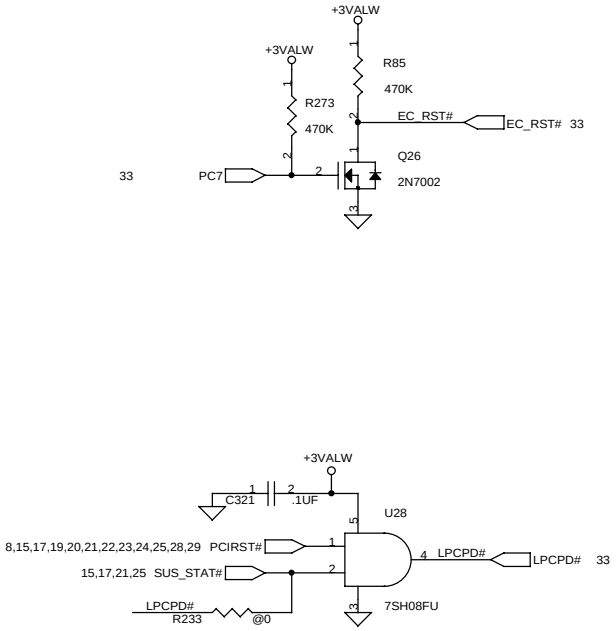
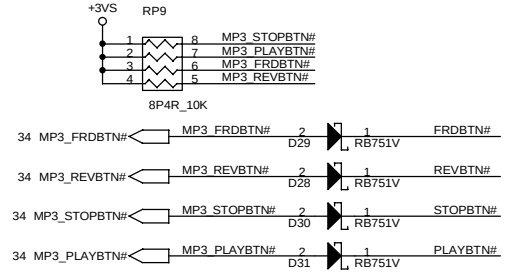
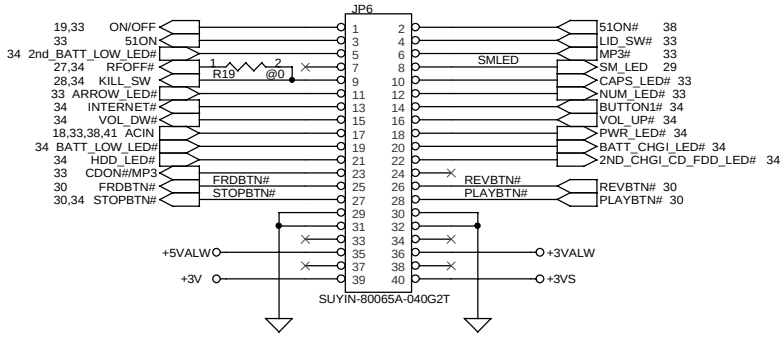


For PC87591 REV 0.A Only





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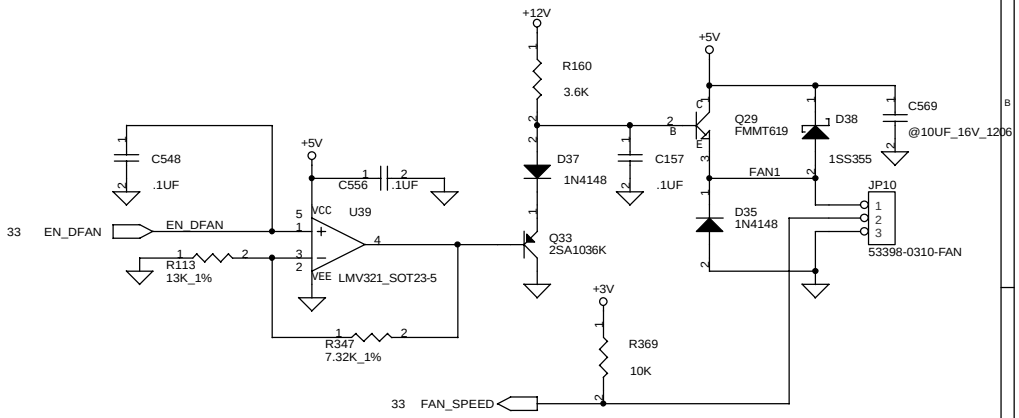

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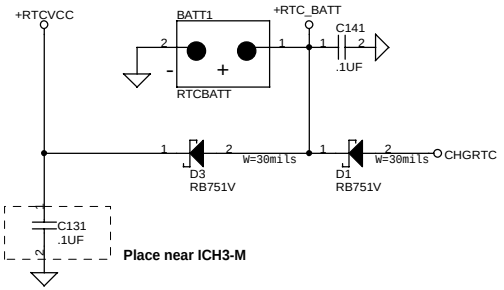
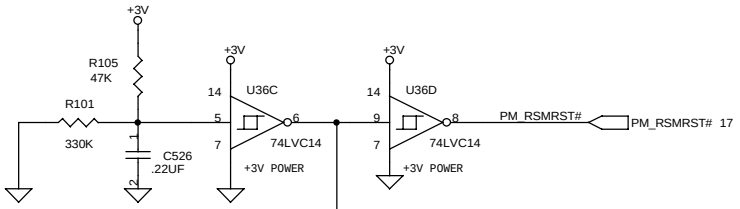
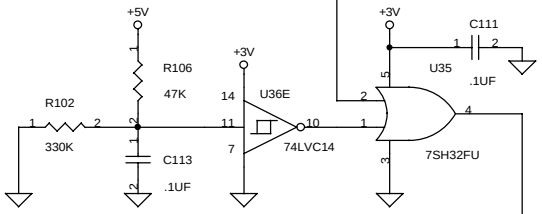
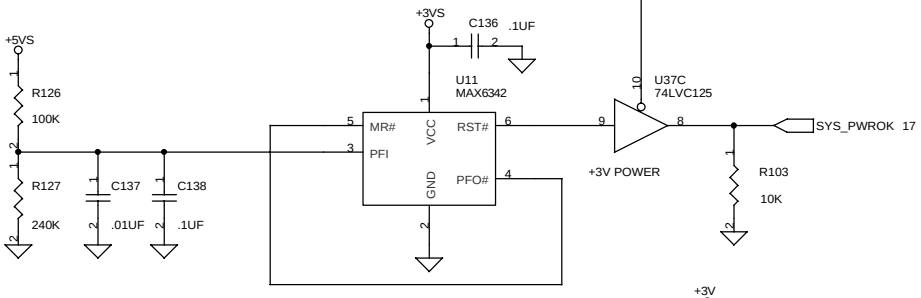
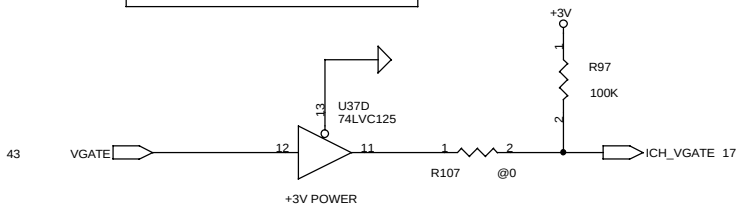
RTC Batt. Connector

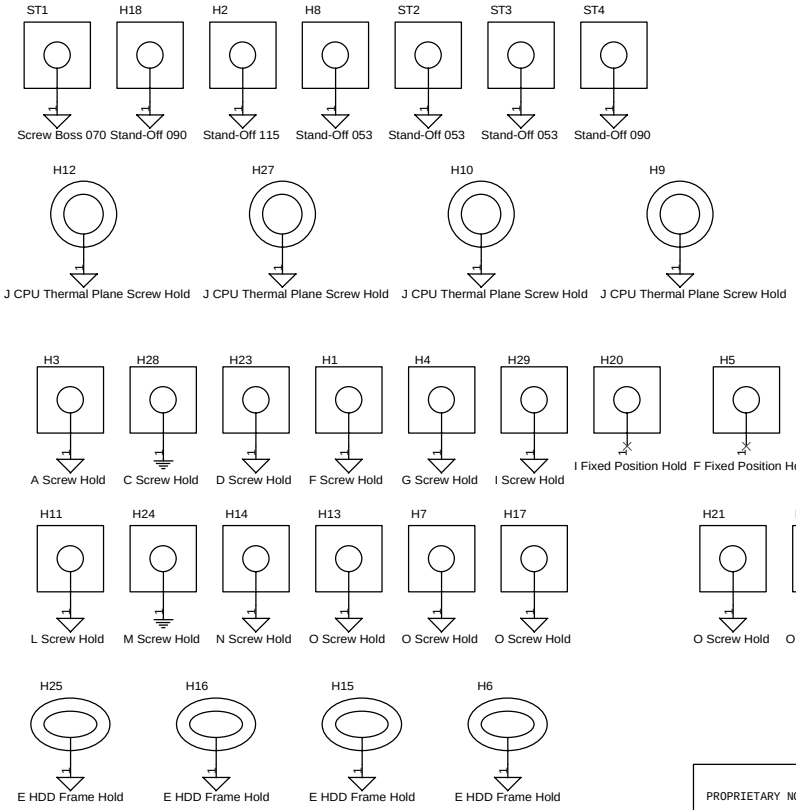


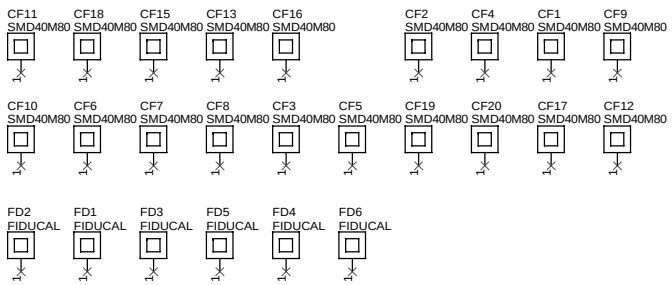












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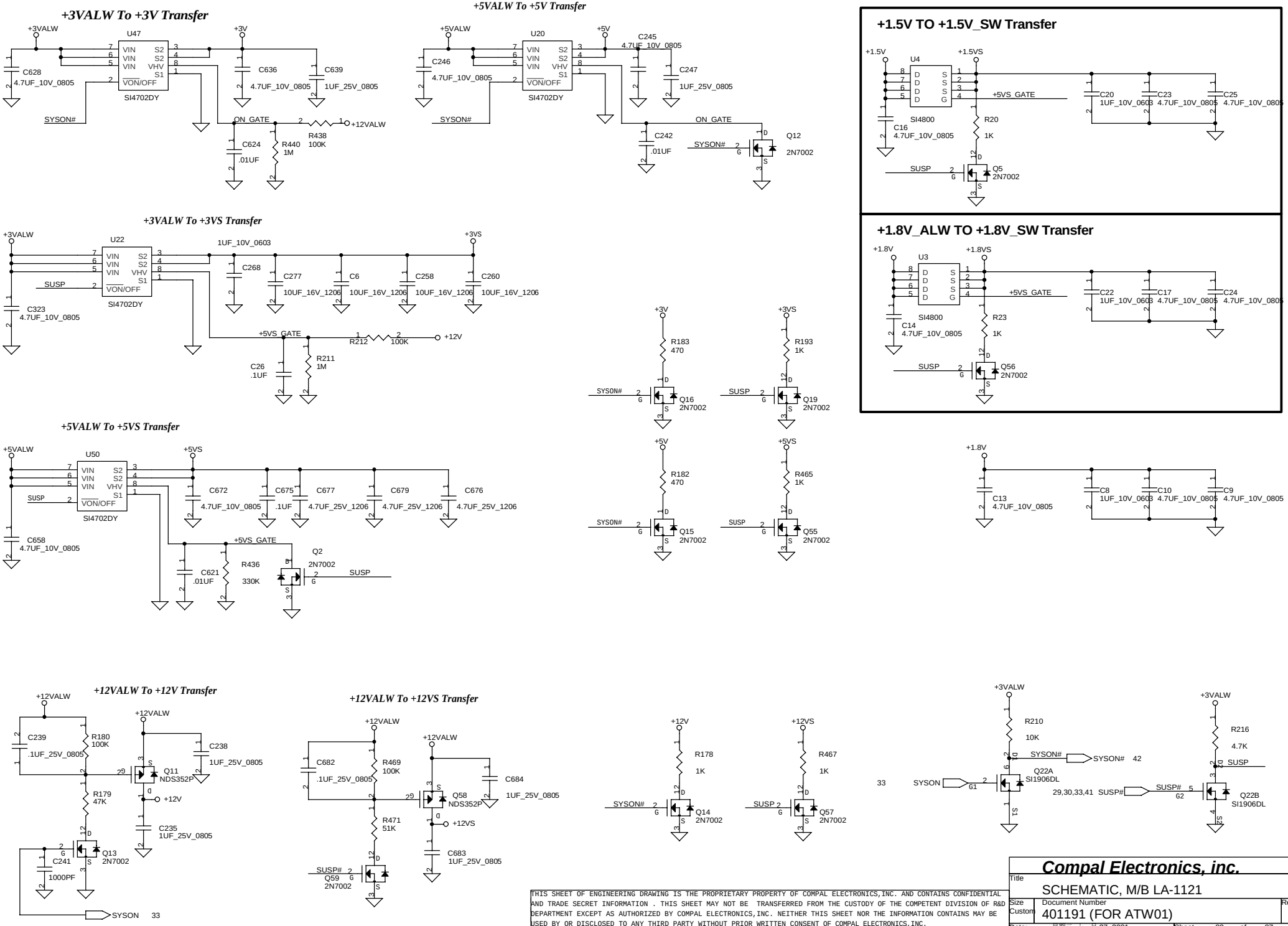
+3VALW To +3V Transfer
U47
SI4702DY
+5VALW To +5V Transfer
U20
SI4702DY
+1.5V TO +1.5V_SW Transfer
U4
SI4800
+1.8V_ALW TO +1.8V_SW Transfer
U3
SI4800
+3VALW To +3VS Transfer
U22
SI4702DY
+5VALW To +5VS Transfer
U50
SI4702DY
+12VALW To +12V Transfer
+12VALW To +12VS Transfer
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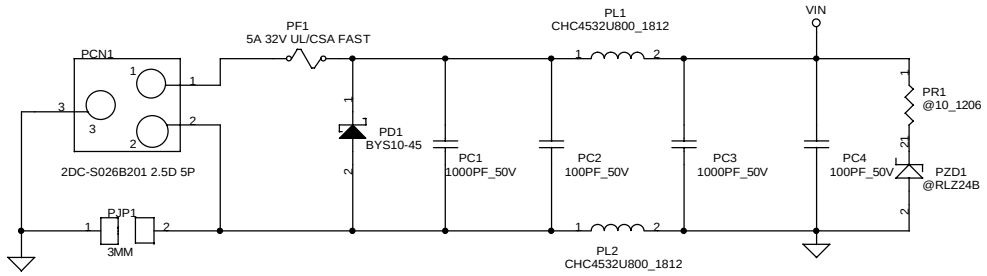
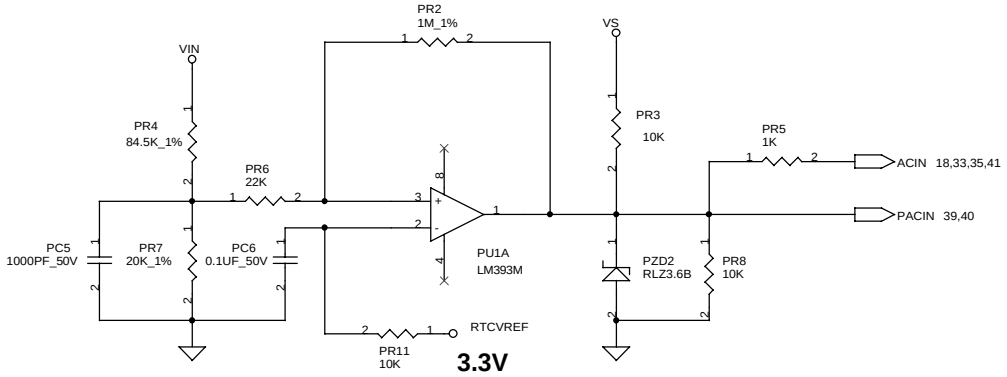
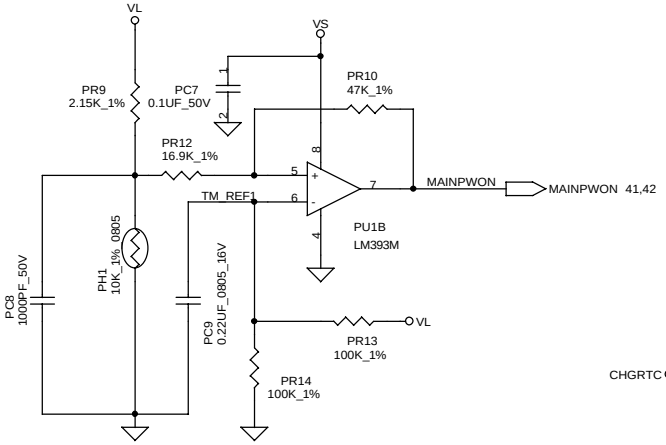
Vin Detector

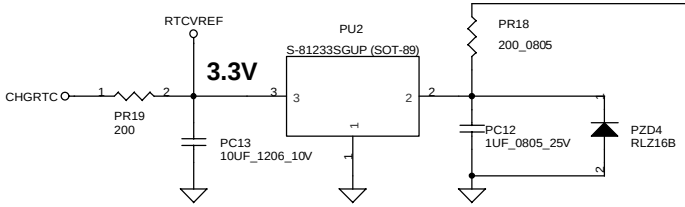
High	**18.764**	**17.901**	**17.063**
Low	**17.745**	**16.903**	**16.038**

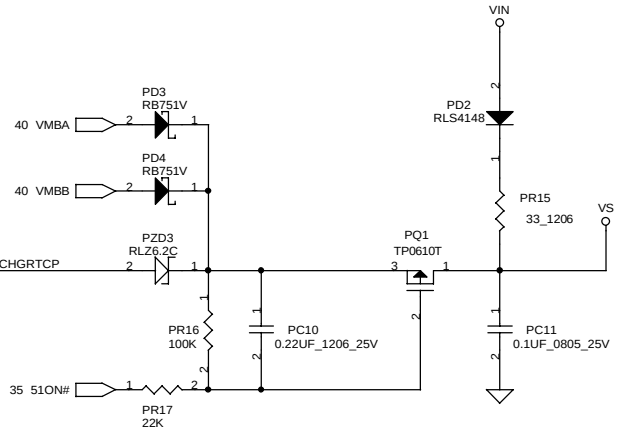


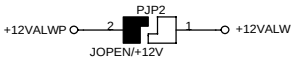


PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 50(51) degree C

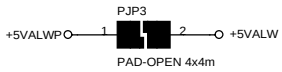




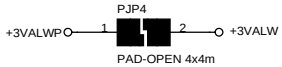




(120mA,20mils ,Via NO.= 1)



(5A,200mils ,Via NO.= 10)



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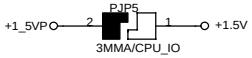
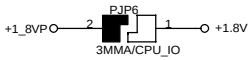


(1.5A,60mils ,Via NO.= 3)



(3A,120mils ,Via NO.= 6)

(6A,240mils ,Via NO.= 12)

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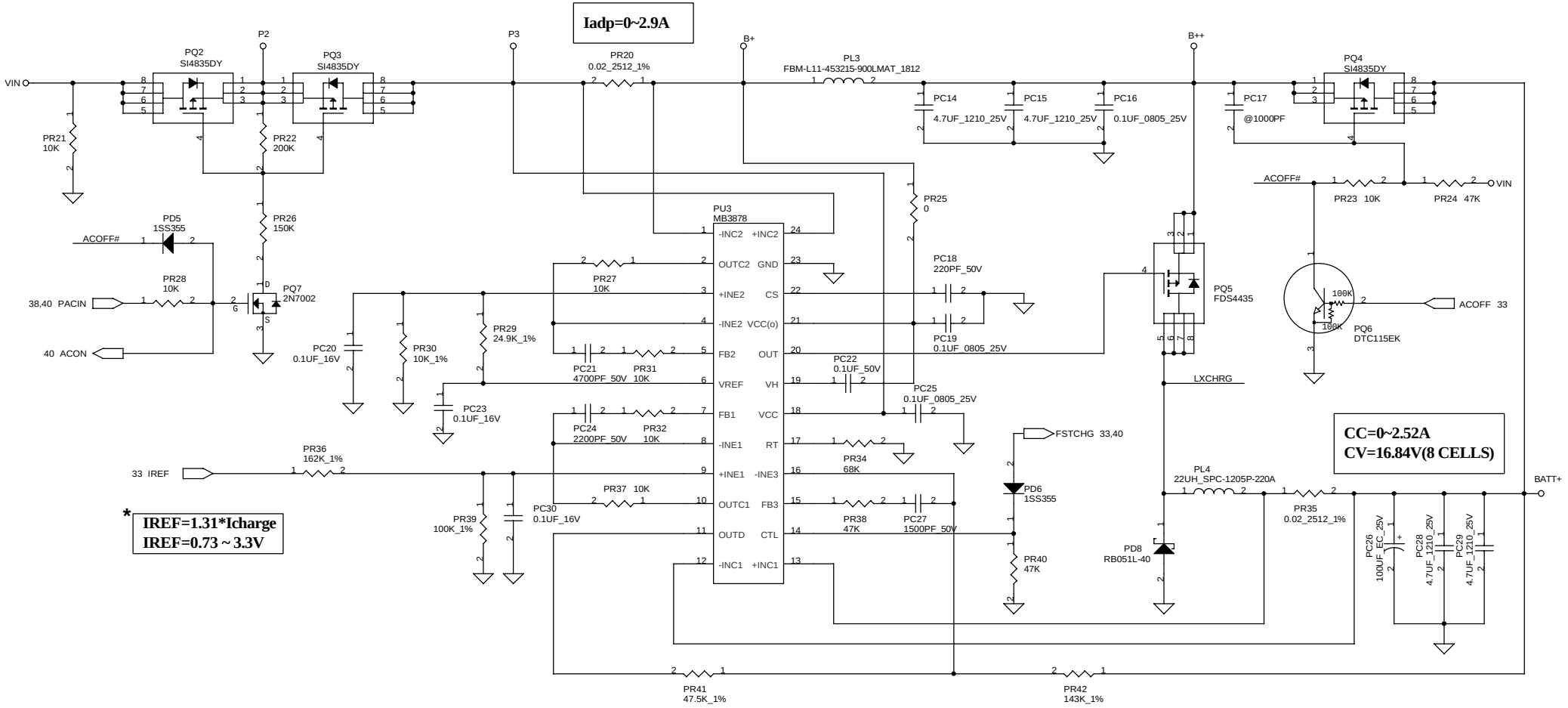

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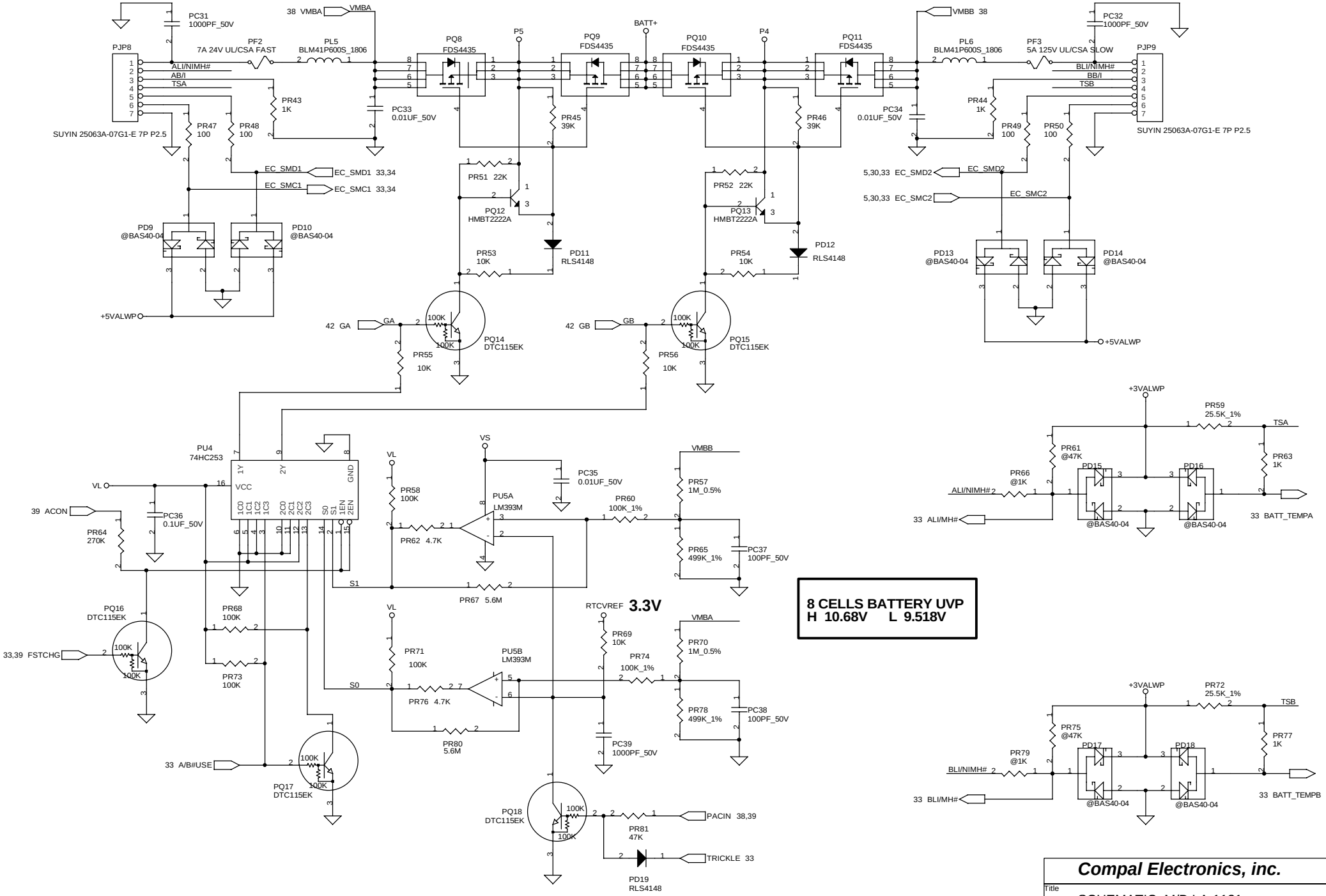

8 CELLS BATTERY UVP
H 10.68V L 9.518V

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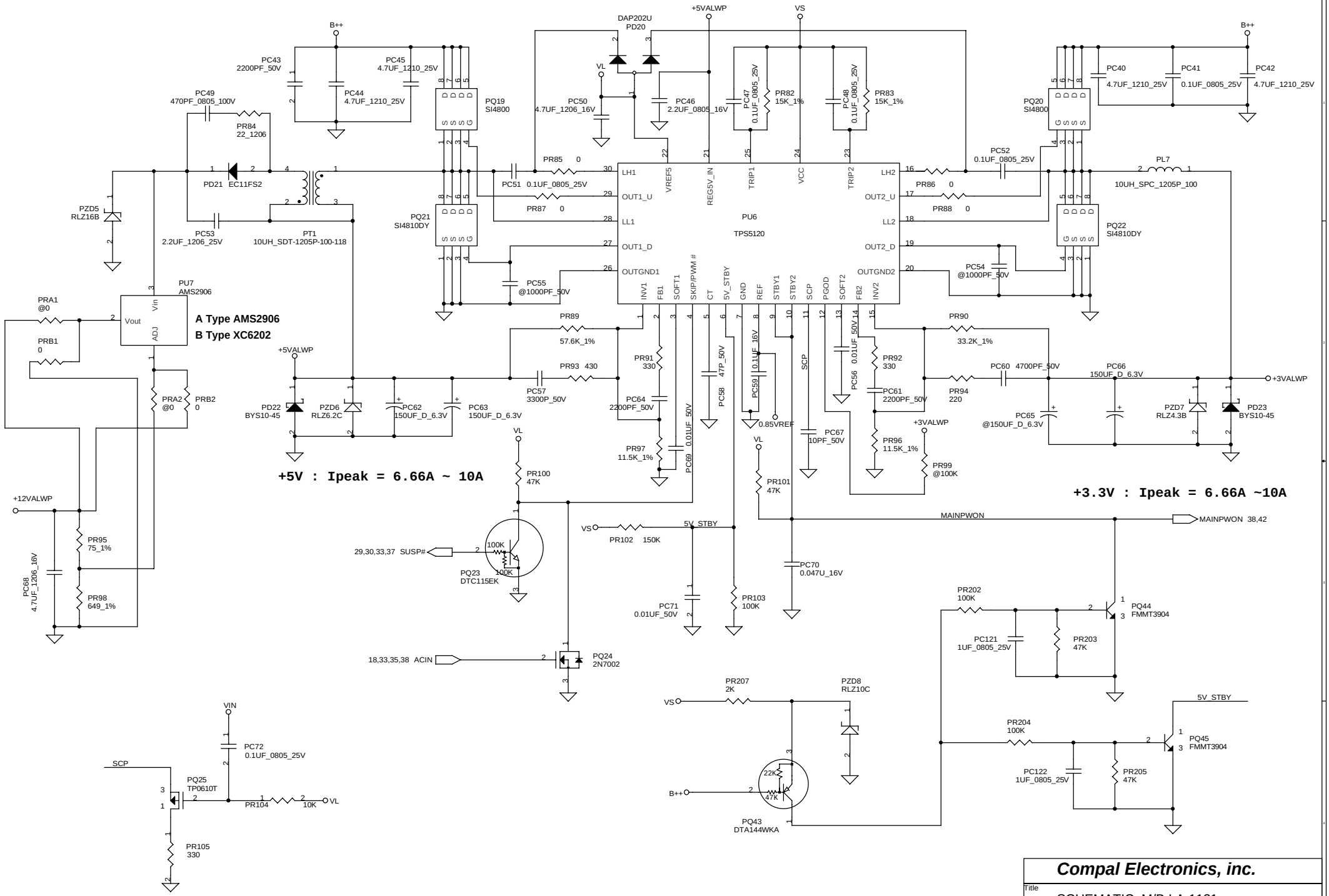

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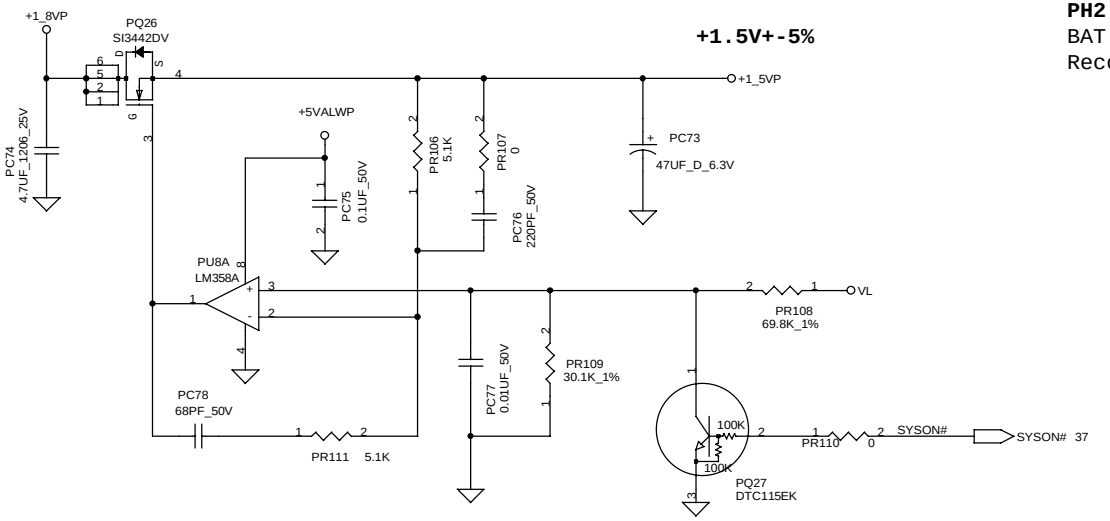
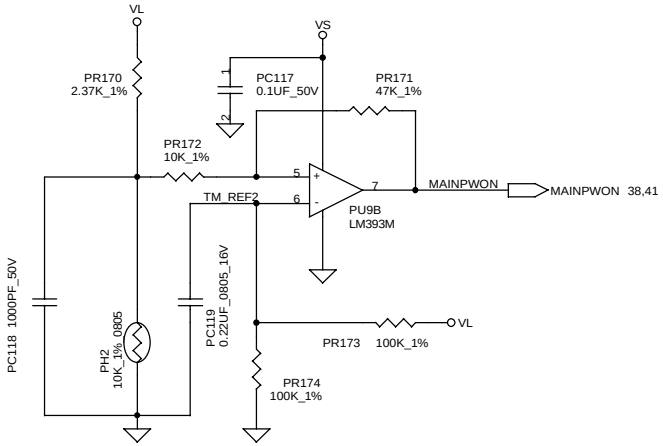
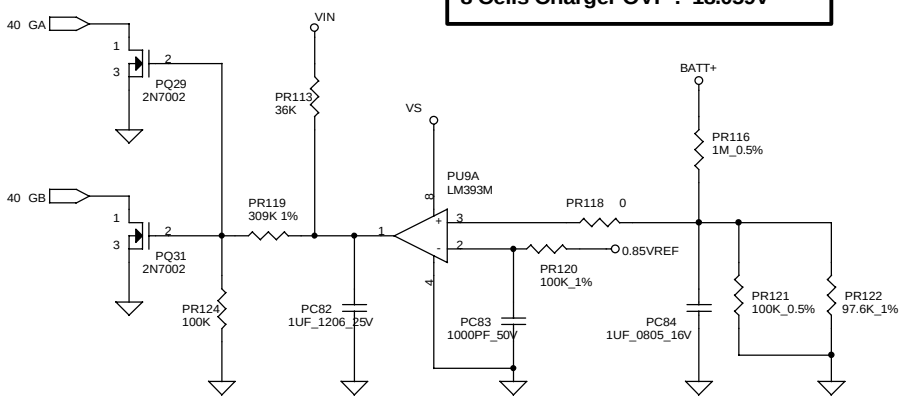


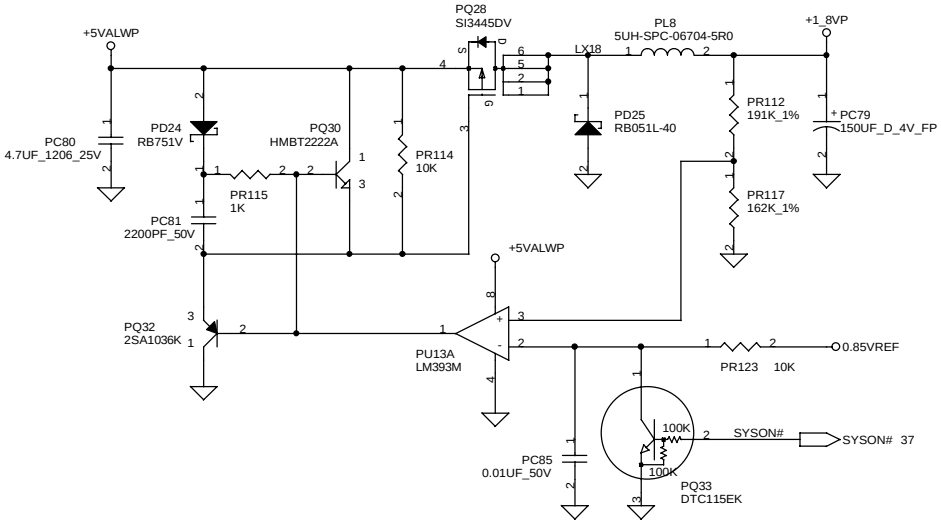
PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C



8 Cells Charger OVP : 18.059V



+1.8V+-5%



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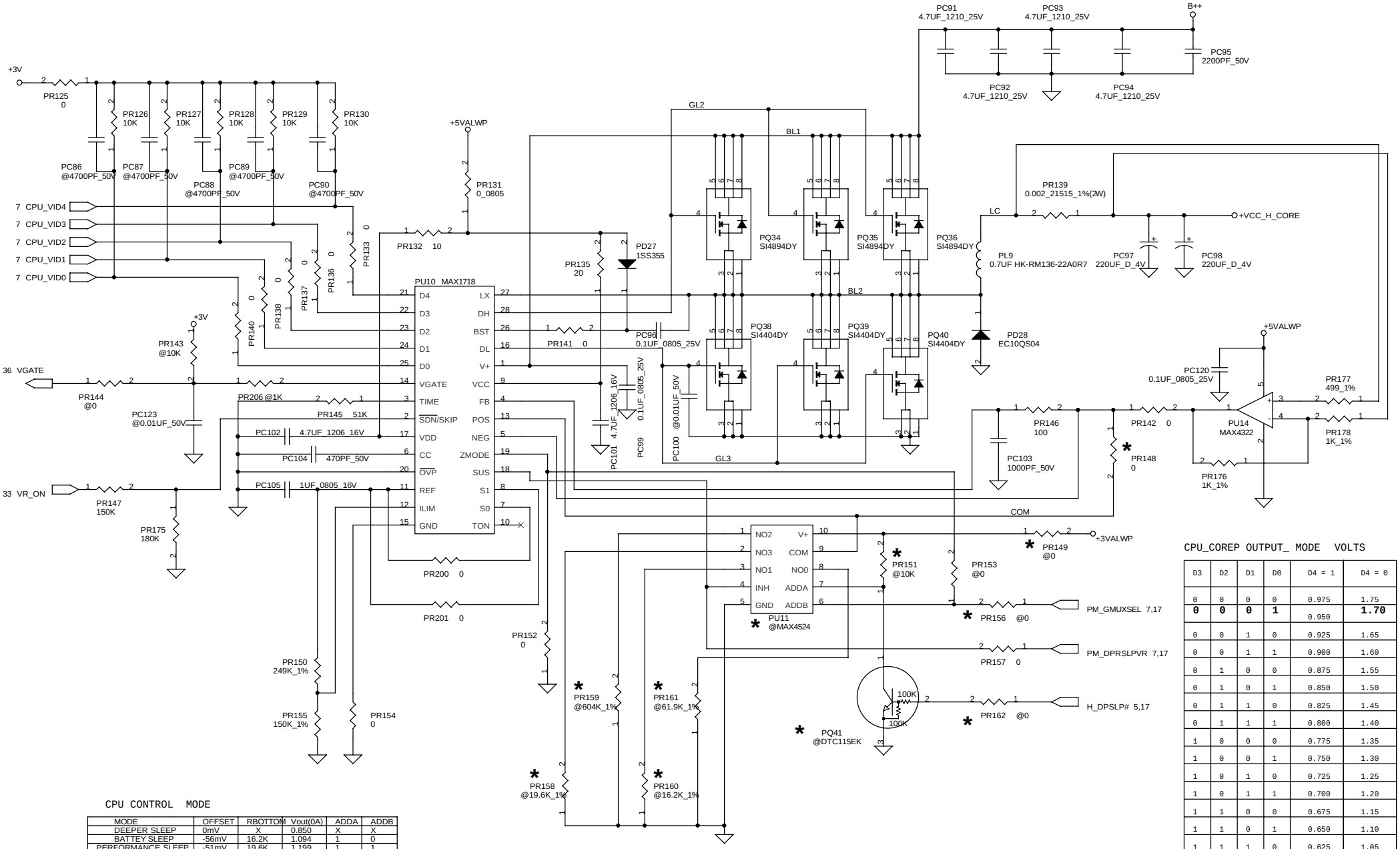

CPU CONTROL MODE

MODE	OFFSET	RBOTTOM	Vout(0A)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTEY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	-1.8mV	604K	1.248	0	1

CPU_COREP OUTPUT_ MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	**0**	**0**	**1**	0.950	**1.70**
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

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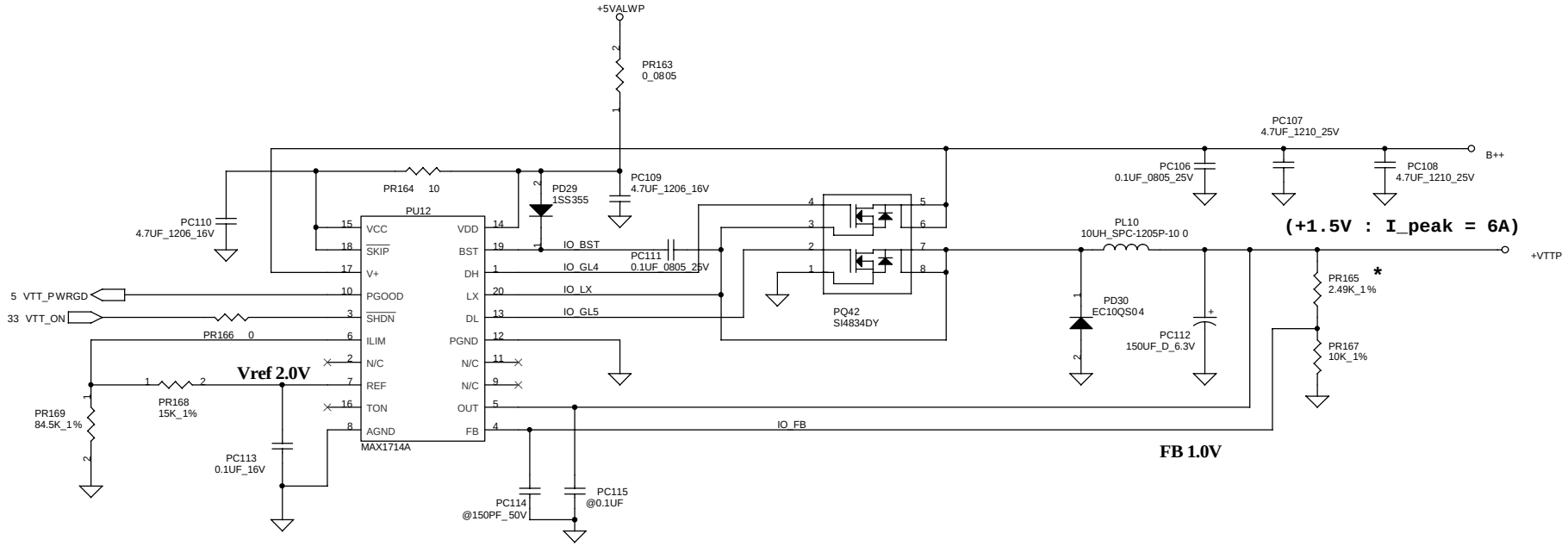

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