

ACL05 LA-1371 Schematics
Document
REV 1.0

INTEL Coppermine-T or Tualatin CPU uFCBGA/uFCPGA
Almador-M(830MG) + ICH3-M + VCH Chipset

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ACL05 BLOCK DIAGRAM

Mobile Tualatin
or
Coppermine-T
(uFCBGA/uFCPGA)
PAGE 4,5,6

Thermal Sensor
MAX1617MEE
PAGE 5

CK TITAN
ICS9250-38
PAGE12

CPU VID & All
reference voltage
PAGE 7

Almadore-M
GMCH-M
625 BGA
PAGE 8,9,10,11

CRT CONN.
PAGE 16

VCH/B
CONN.
PAGE 15

GM Bus Interface

Memory Bus

SO-DIMM * 2
BANK 2,3,4,5
PAGE 13,14

USB
PAGE 27

USB

HDD Connector
PAGE 20

ATA 66/100

Audio CD-DJ
OZ163
Rev.C
PAGE 30

AC'97 CODEC
CS4299
PAGE 31

Audio Amplifier
PAGE 32

Audio Jack
PAGE 32

ICH3-M
421 BGA
PAGE 17,18,19

Hub Interface

PCI BUS

IEEE 1394
TI TSB43AB22
PAGE 22

LAN
RTL8100-L
PAGE 21

Mini PCI
Socket
PAGE 28

CardBus
TI PCI1420
PAGE 23

Slot 0/1
PAGE 24

Super I/O
LPC47N227
PAGE 25

Embedded
Controller
NS PC87591
PAGE 33

Parallel
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FDD
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Scan KB
PAGE 15

BIOS & I/O
PORT
PAGE 34

FAN on controller &
TEMP. sensing circuit
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DC/DC Interface
RTC Battery
PAGE 37

BATTERY
Charger
PAGE 41

POWER
Interface
PAGE 40,42,43,44

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VCH CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM (RESERVE)	AD22		PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ163	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

EC SM Bus2 address

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

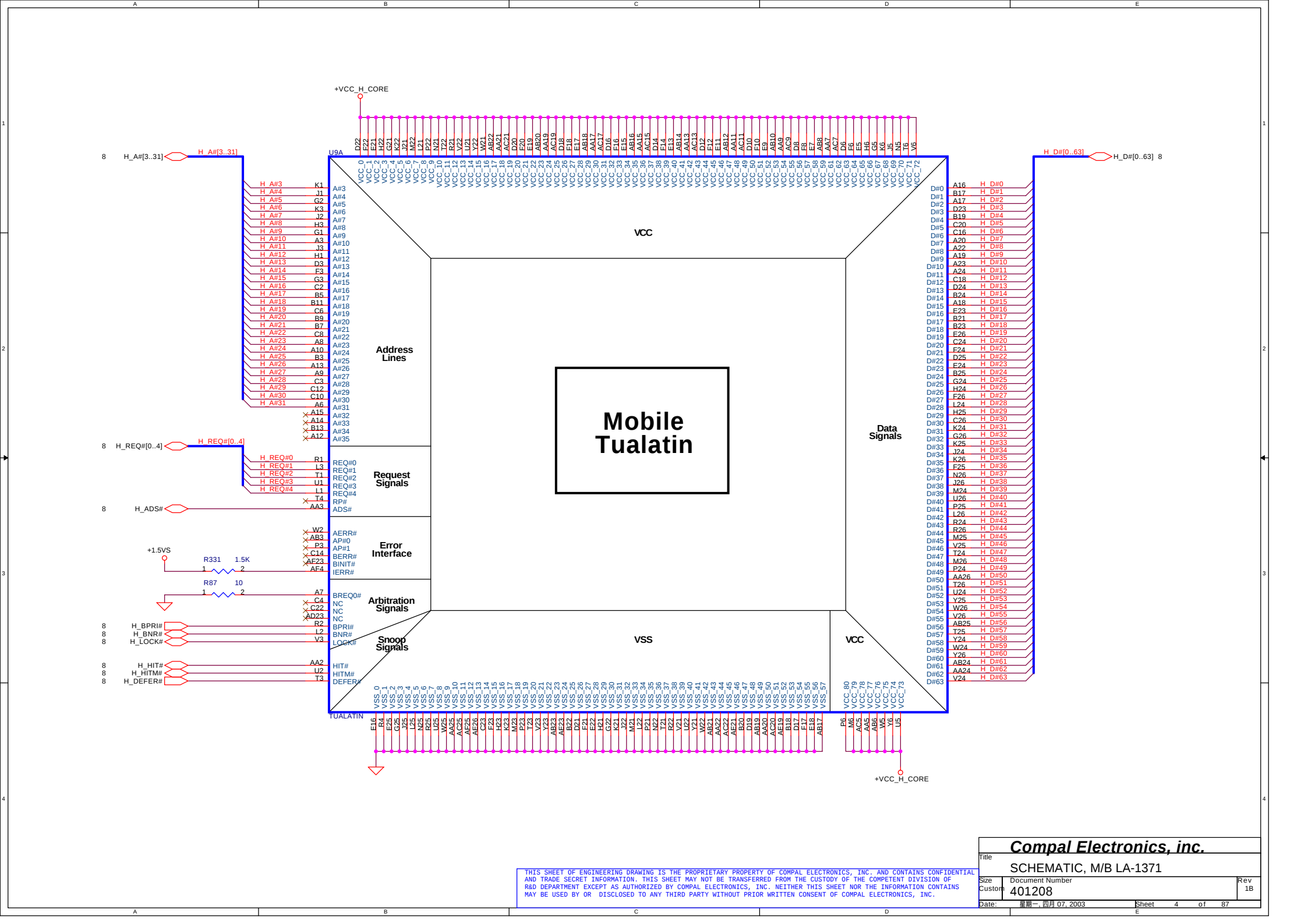
PIR

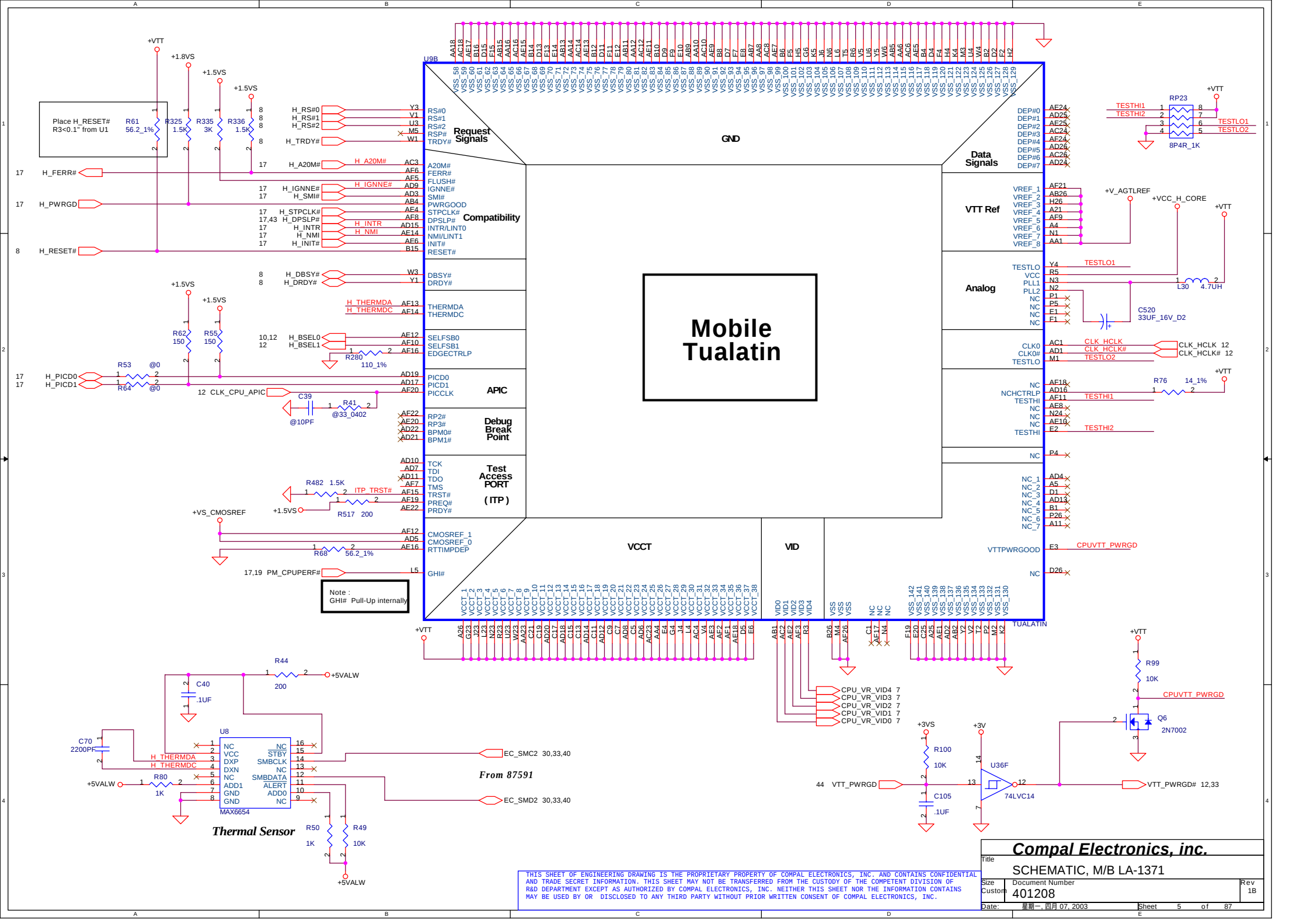
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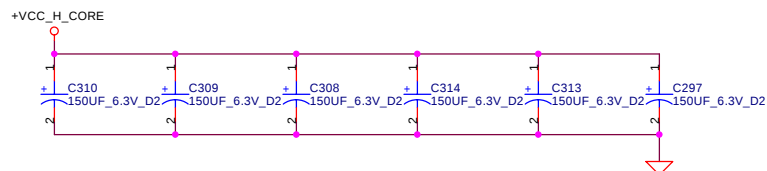
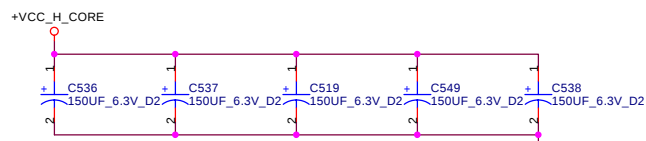
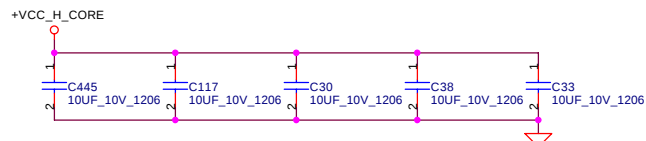
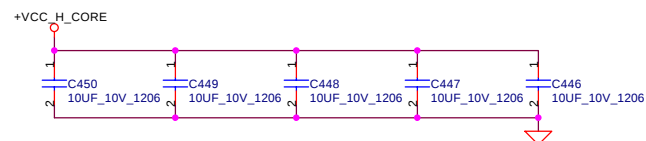
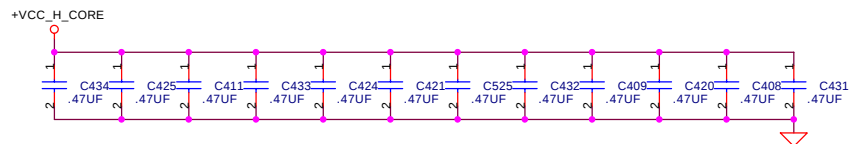
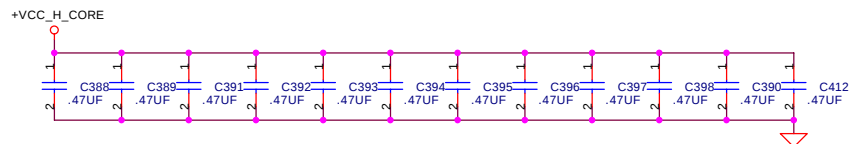
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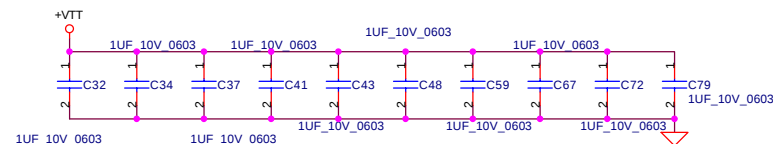
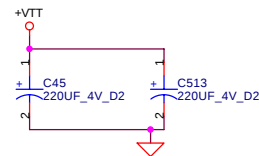
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.



Layout note :

Place close to CPU,
Use 2 vias per PAD.



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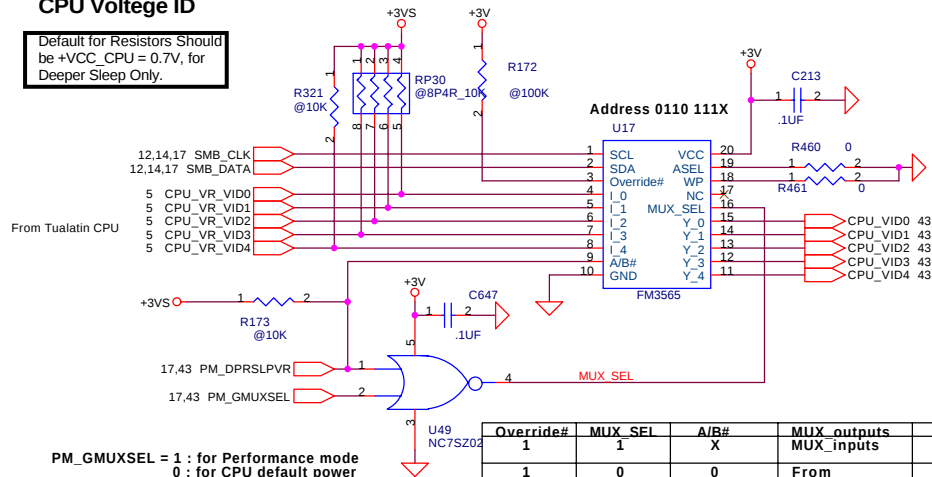
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CPU Voltage ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1 : for Deeper Sleep mode
0 : for Performance mode

Override#	MUX_SEL	A/B#	MUX_outputs MUX_inputs	Mode Battery
1	1	X		
1	0	0	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

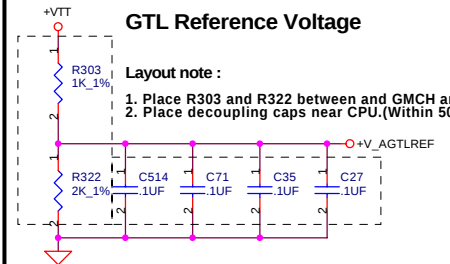
D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

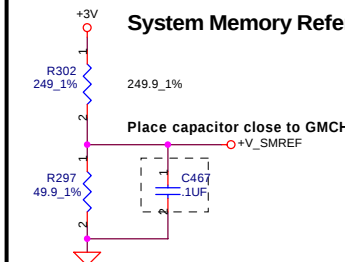
GTL Reference Voltage

Layout note :

1. Place R303 and R322 between and GMCH and CPU
2. Place decoupling caps near CPU.(Within 500mils)



System Memory Reference

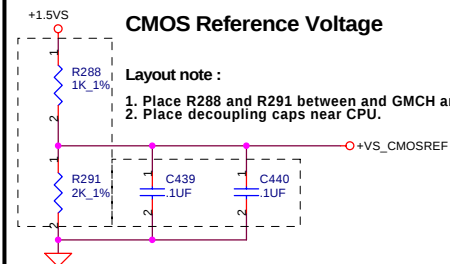


Place capacitor close to GMCH.

CMOS Reference Voltage

Layout note :

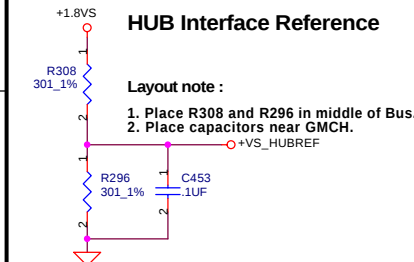
1. Place R288 and R291 between and GMCH and CPU
2. Place decoupling caps near CPU.



HUB Interface Reference

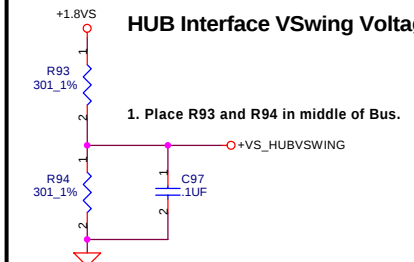
Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

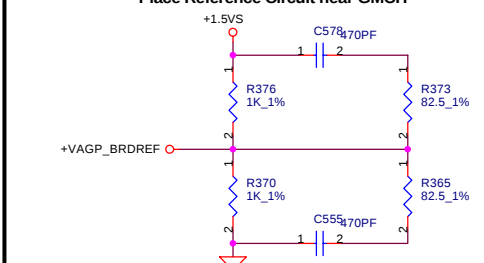


HUB Interface VSwing Voltage

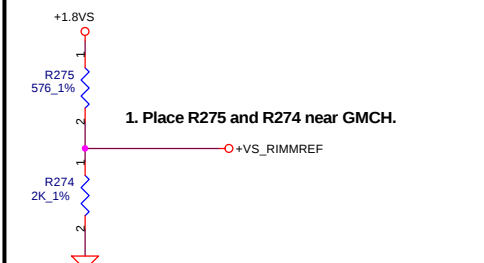
1. Place R93 and R94 in middle of Bus.



Place Reference Circuit near GMCH



1. Place R275 and R274 near GMCH.

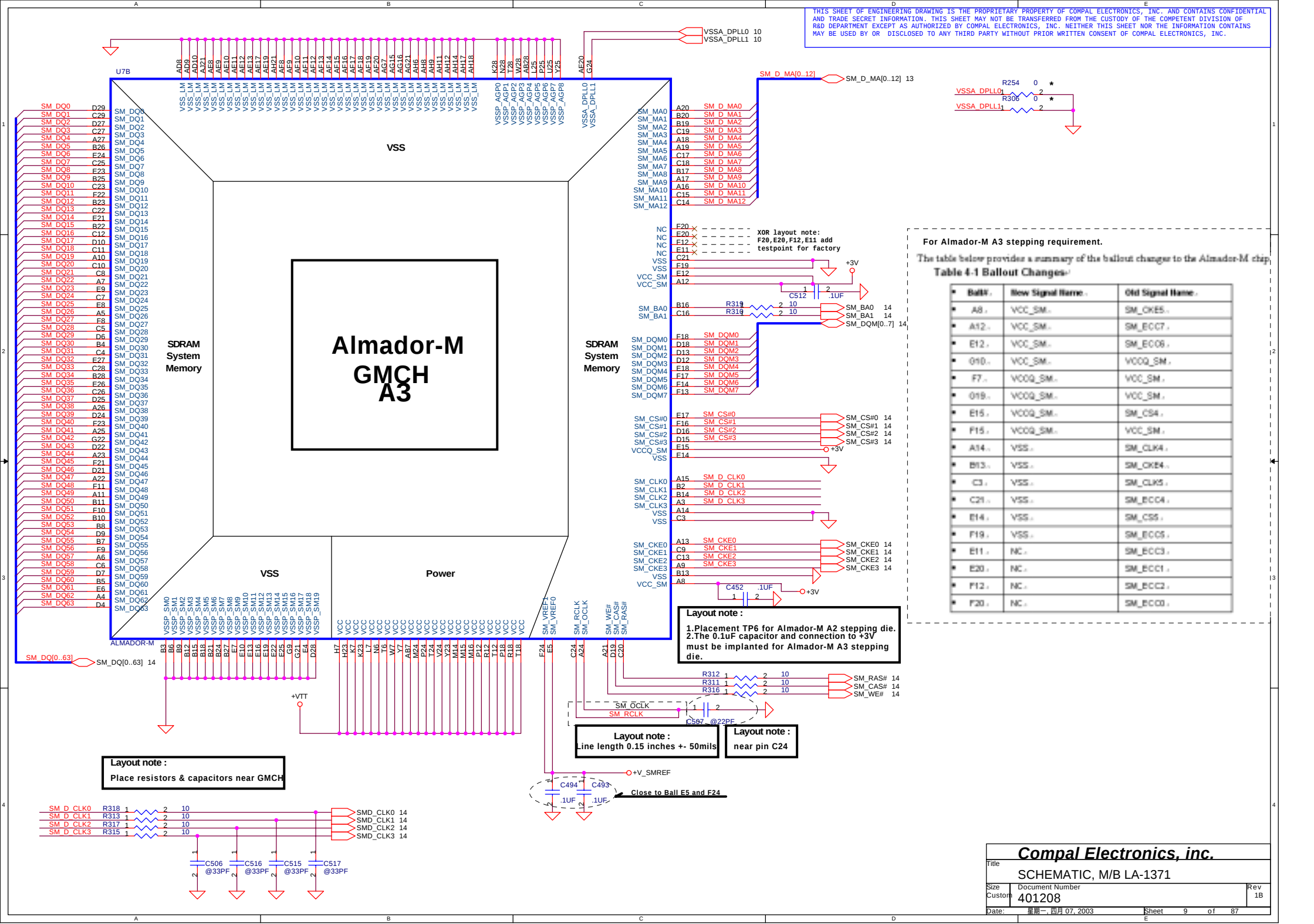


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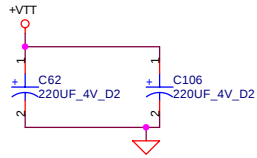
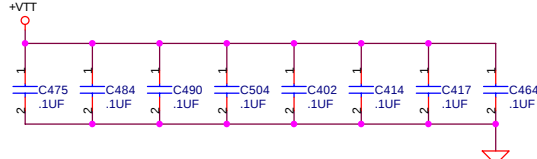
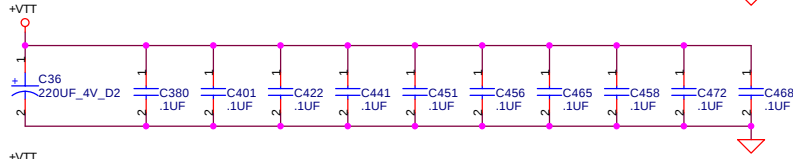
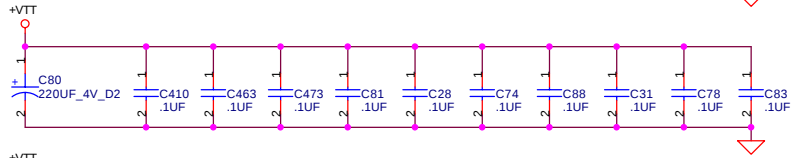
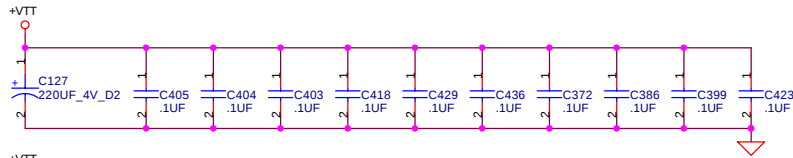
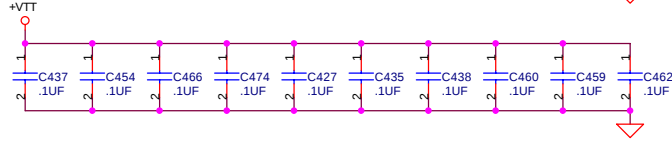
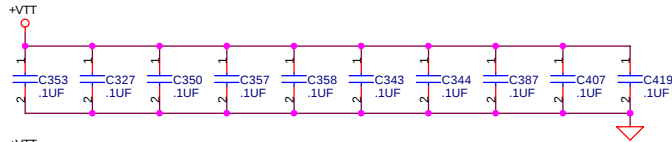
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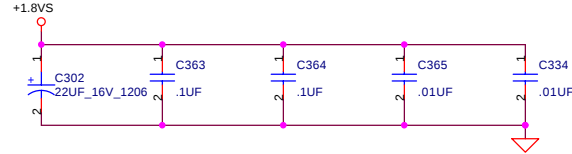
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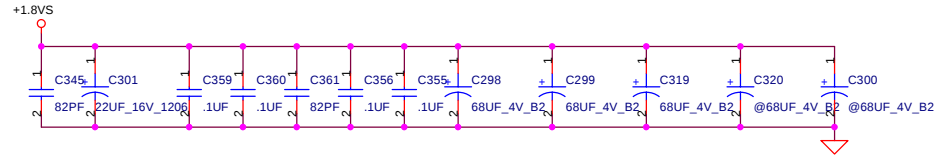
Layout note :
Distribute as close as possible
to GMCH Processor Quadrant .



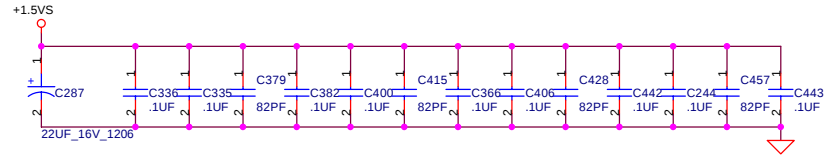
Layout note :
Distribute as close as possible
to VCCPCMOS_LM .



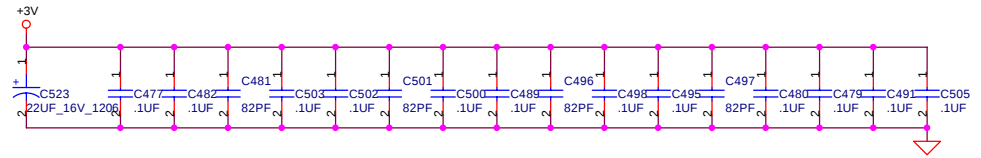
Layout note :
Distribute as close as possible
to GMCH Local Memory Quadrant .



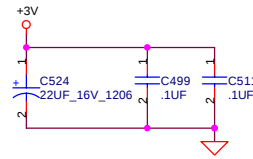
Layout note :
Distribute as close as possible
to GMCH AGP/DVO Quadrant .



Layout note :
Distribute as close as possible
to GMCH System Memory Quadrant .



Layout note :
Distribute as close as possible
to IO Quadrant .



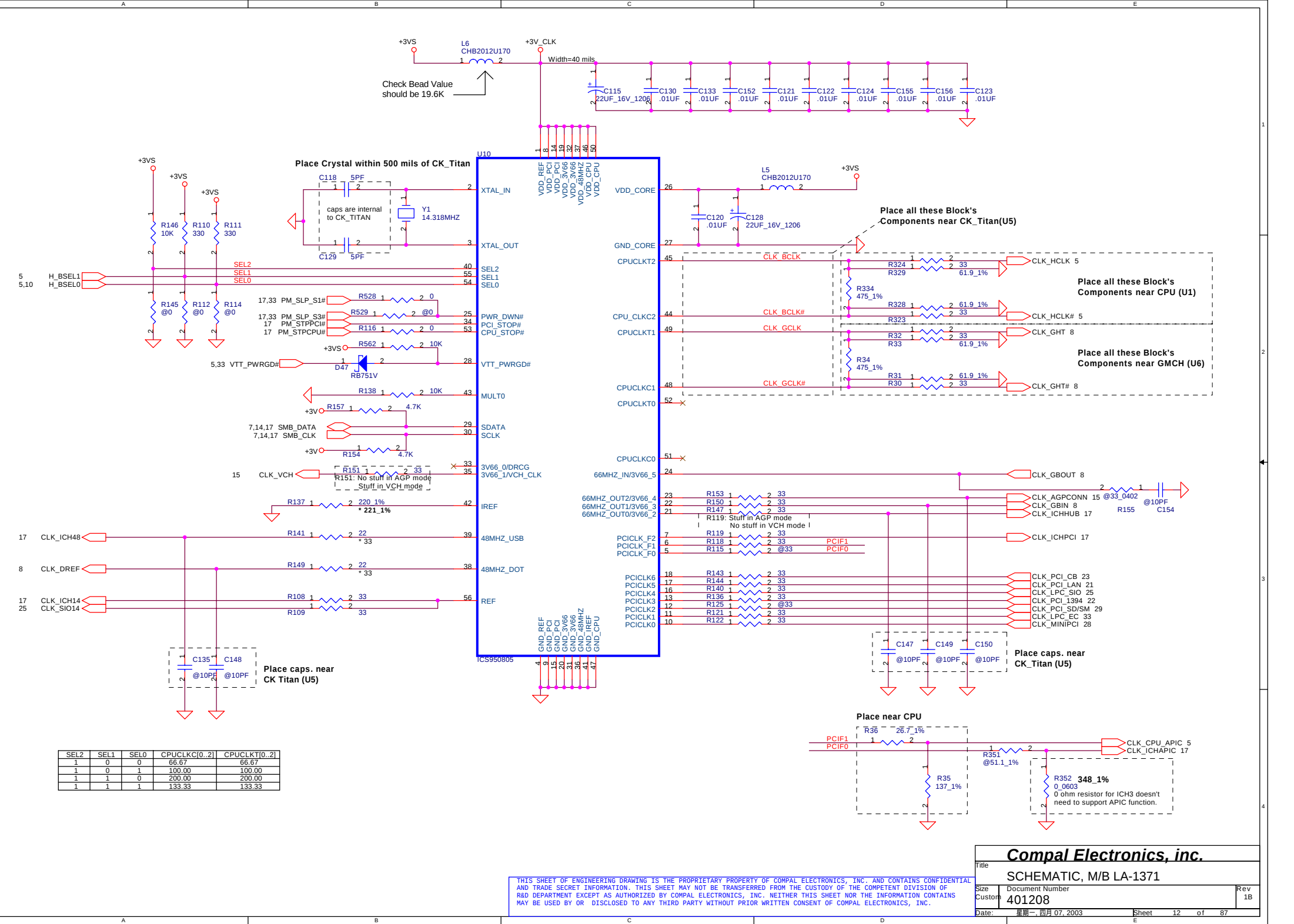
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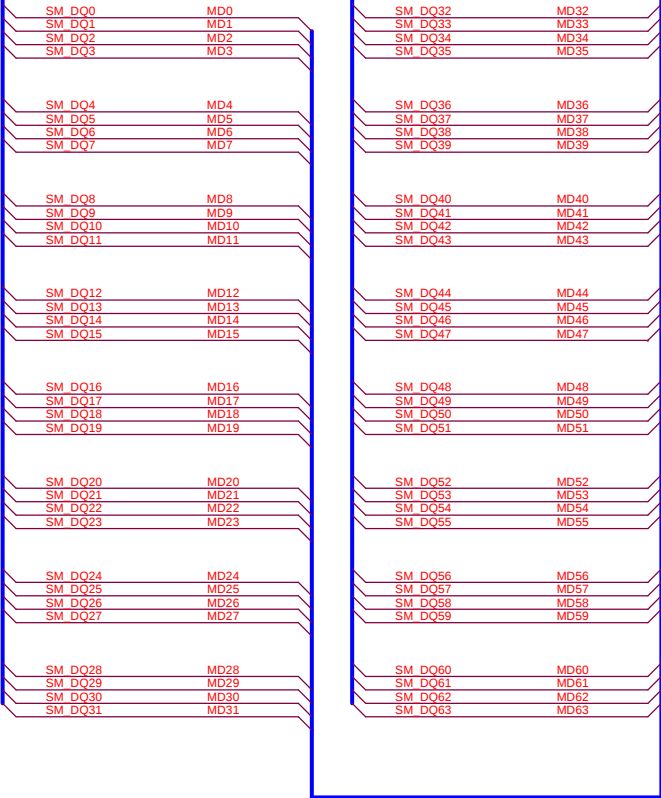
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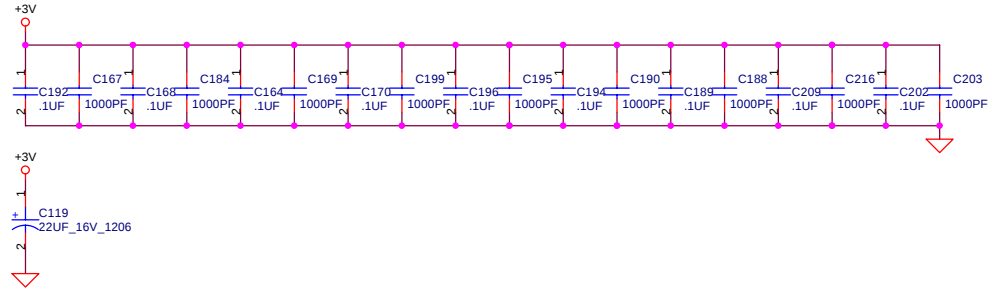
SEL2	SEL1	SEL0	CPUCCLK0[0..2]	CPUCCLK0[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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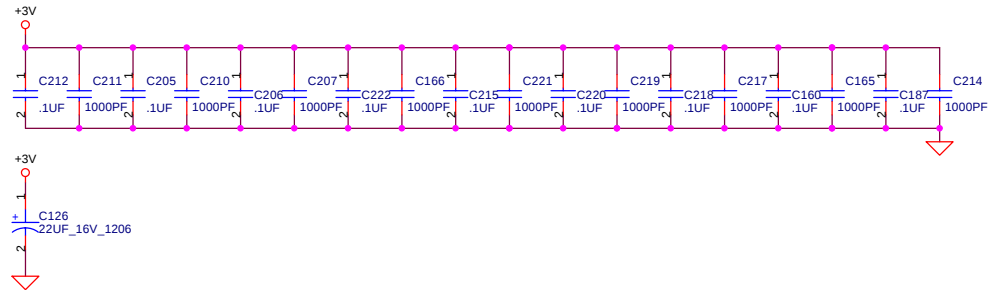
9,14 SM_DQ[0..63] MD[0..63] 9,14



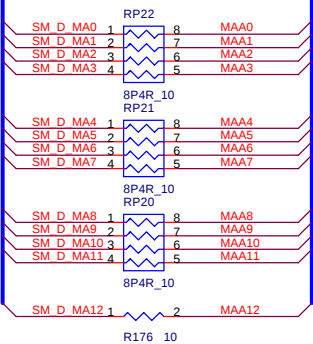
Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .



9 SM_D_MAA[0..12] MAA[0..12] 14

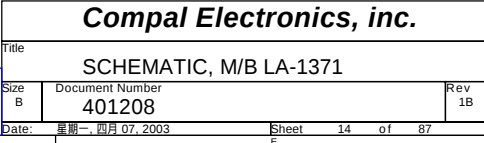


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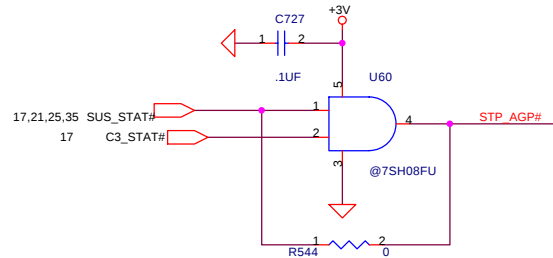
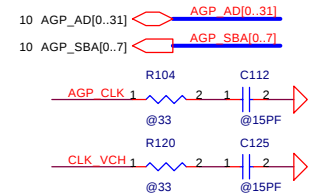
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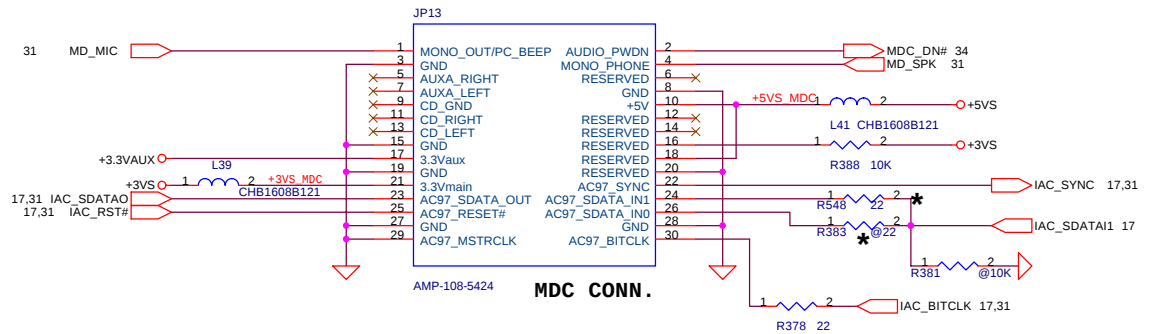
BANK 2/3



JP8



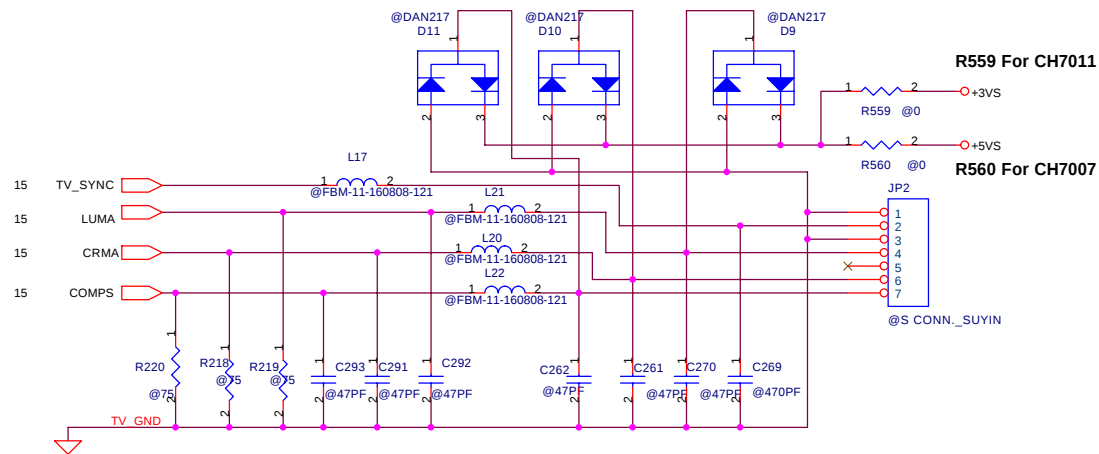
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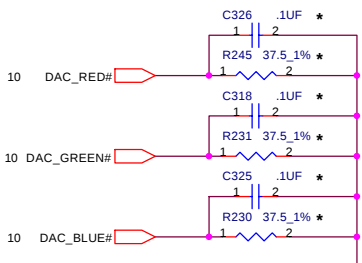
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TV_OUT CONN.

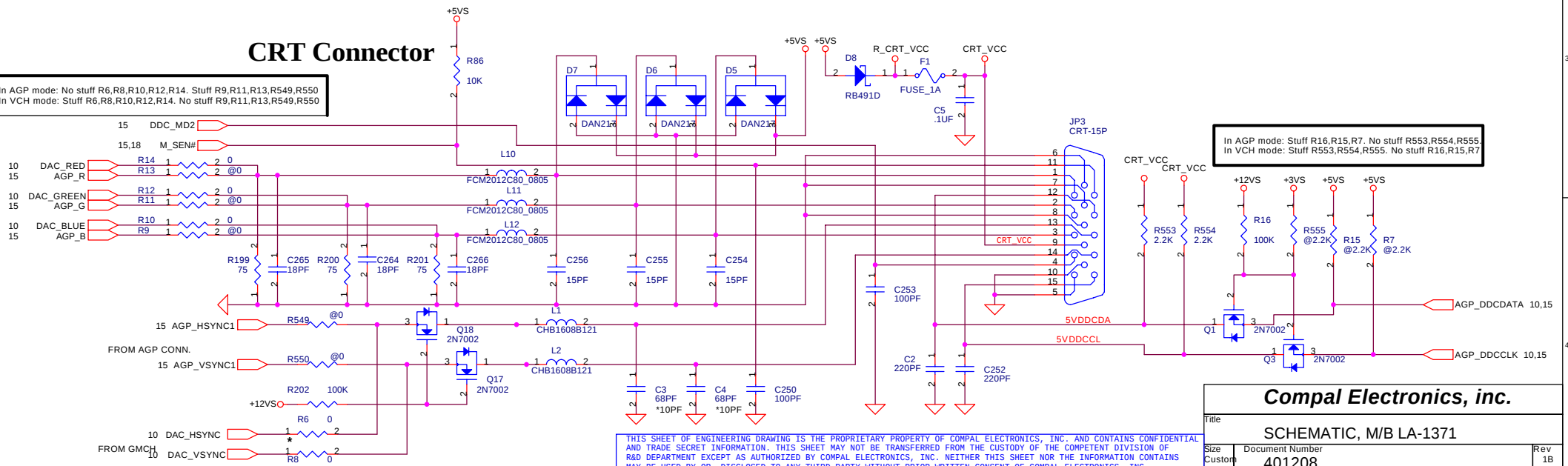


In AGP mode: No stuff C326,R245,C318,R231,C325,R230.
In VCH mode: Stuff C326,R245,C318,R231,C325,R230



CRT Connector

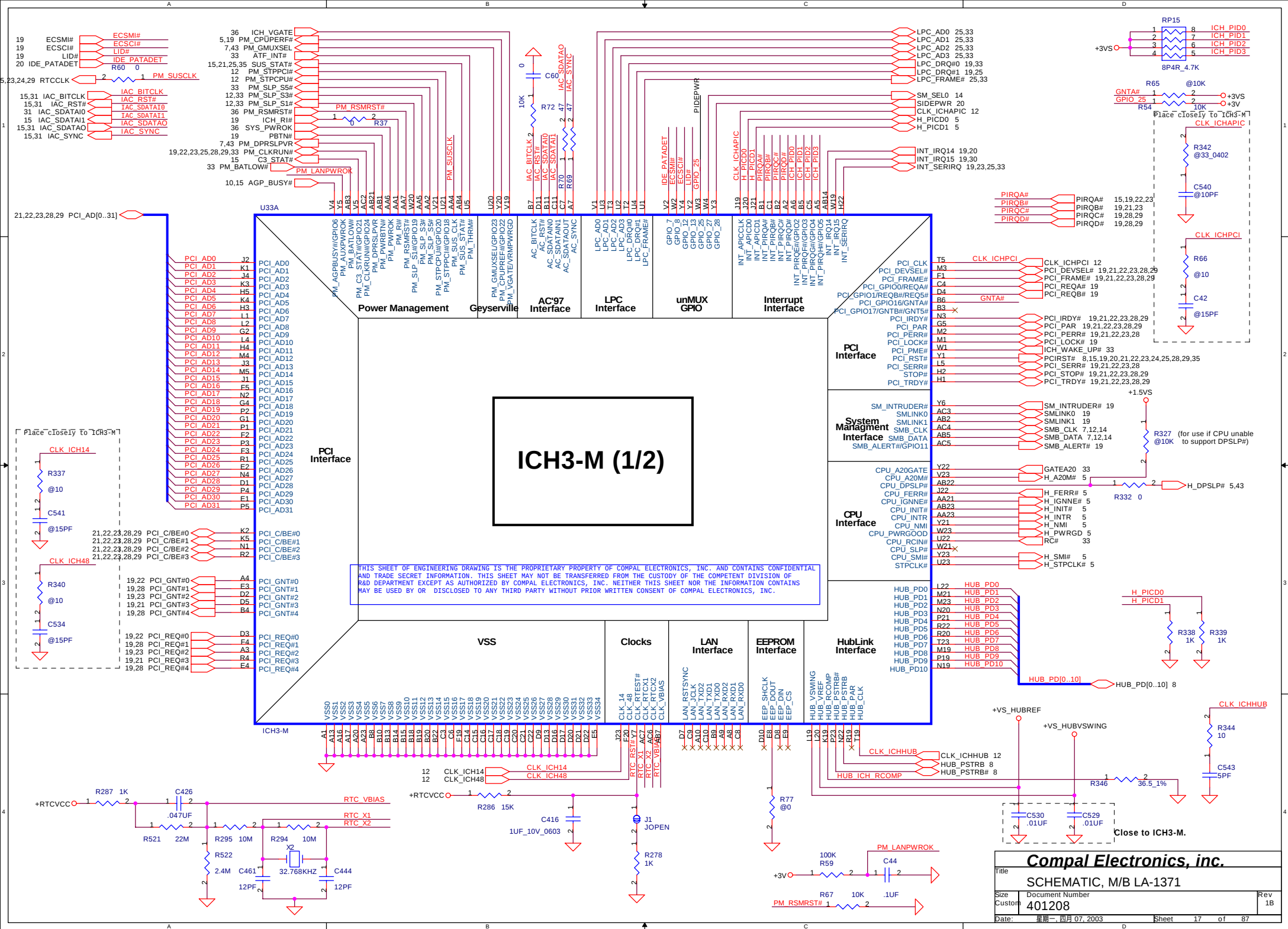
In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550

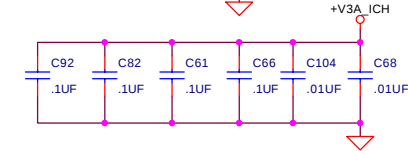
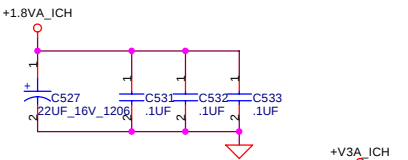
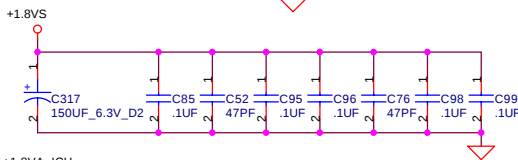
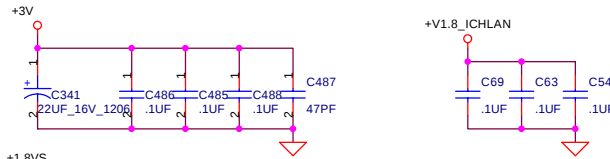
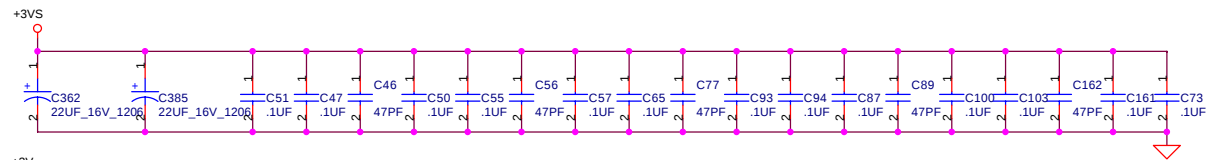
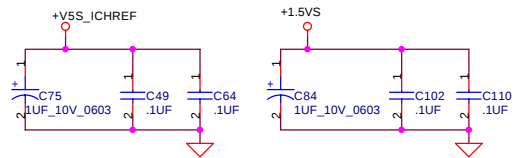
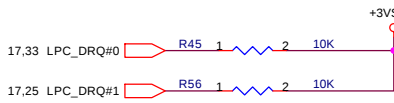
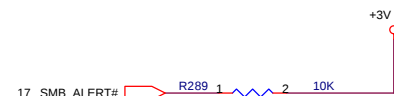
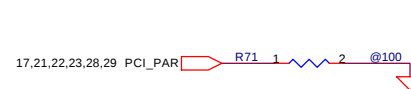
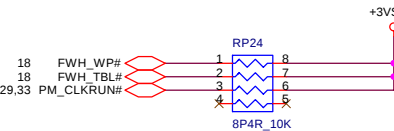
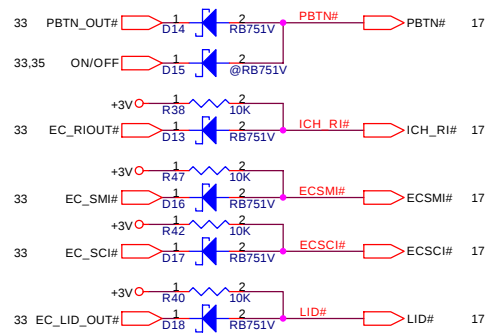
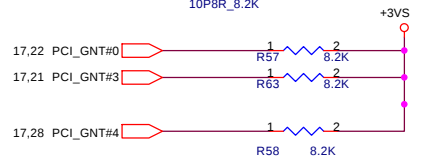
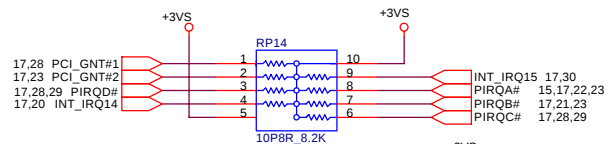
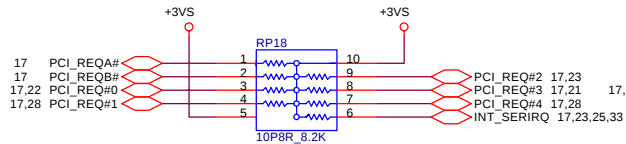
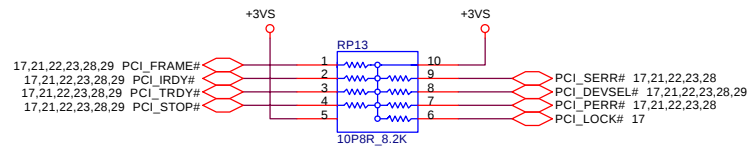


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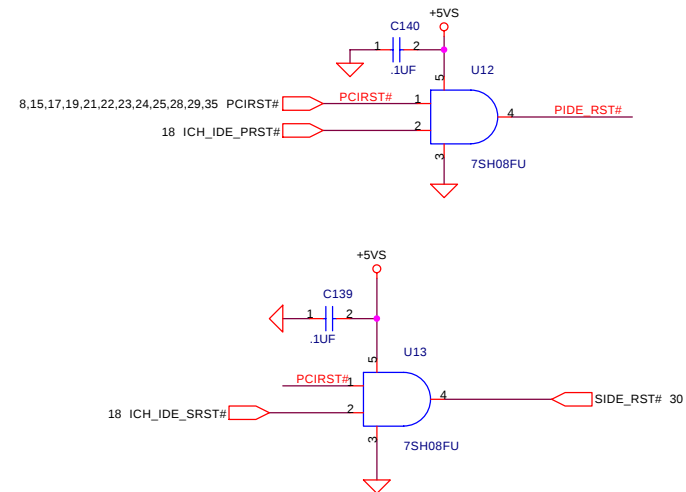
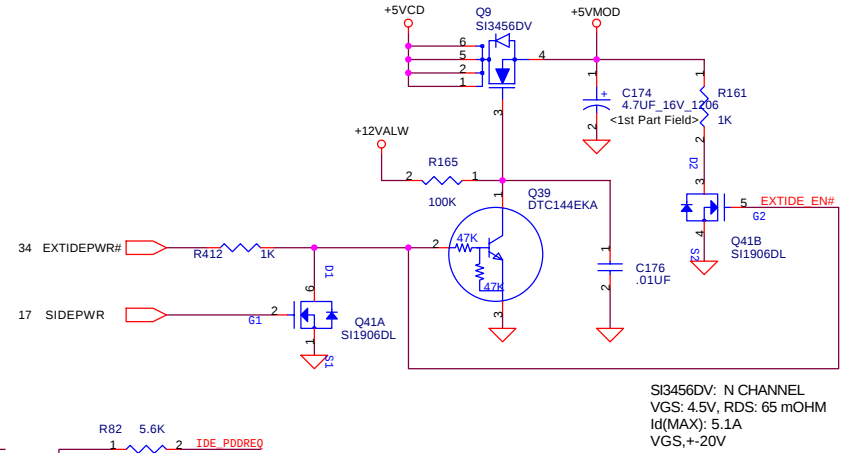
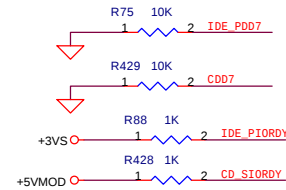
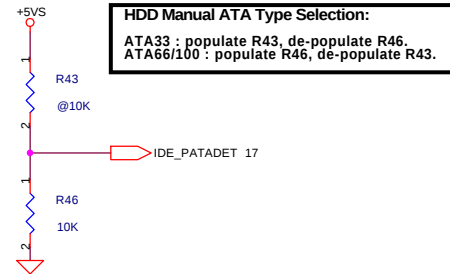
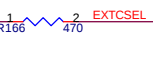
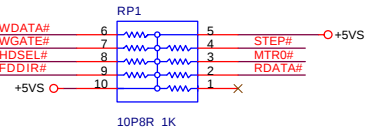
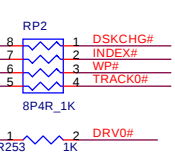
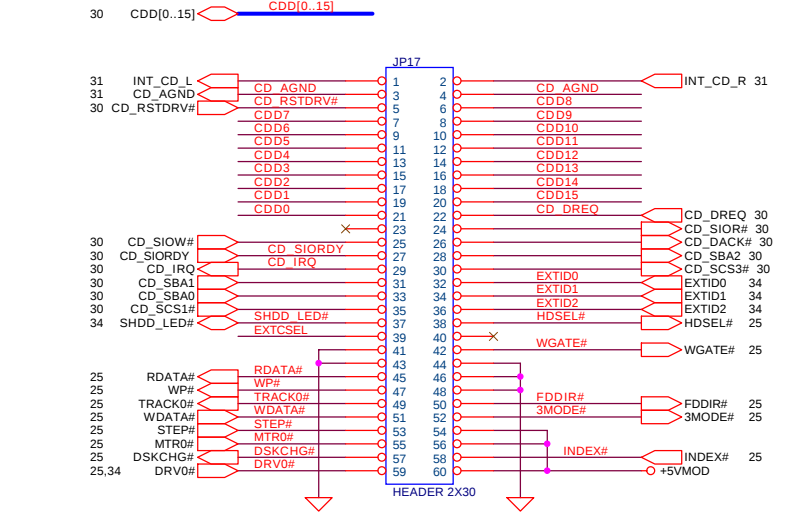
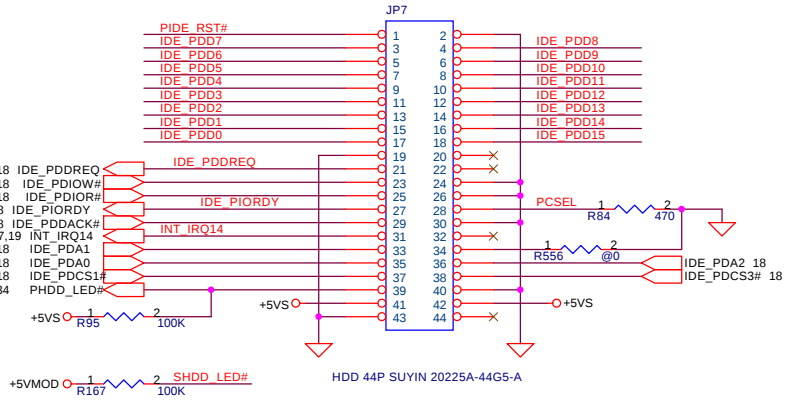
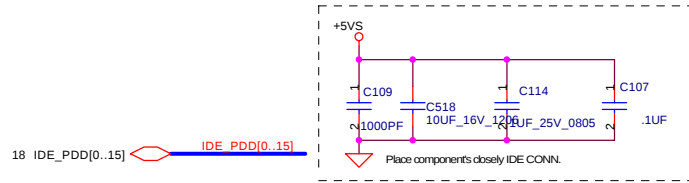




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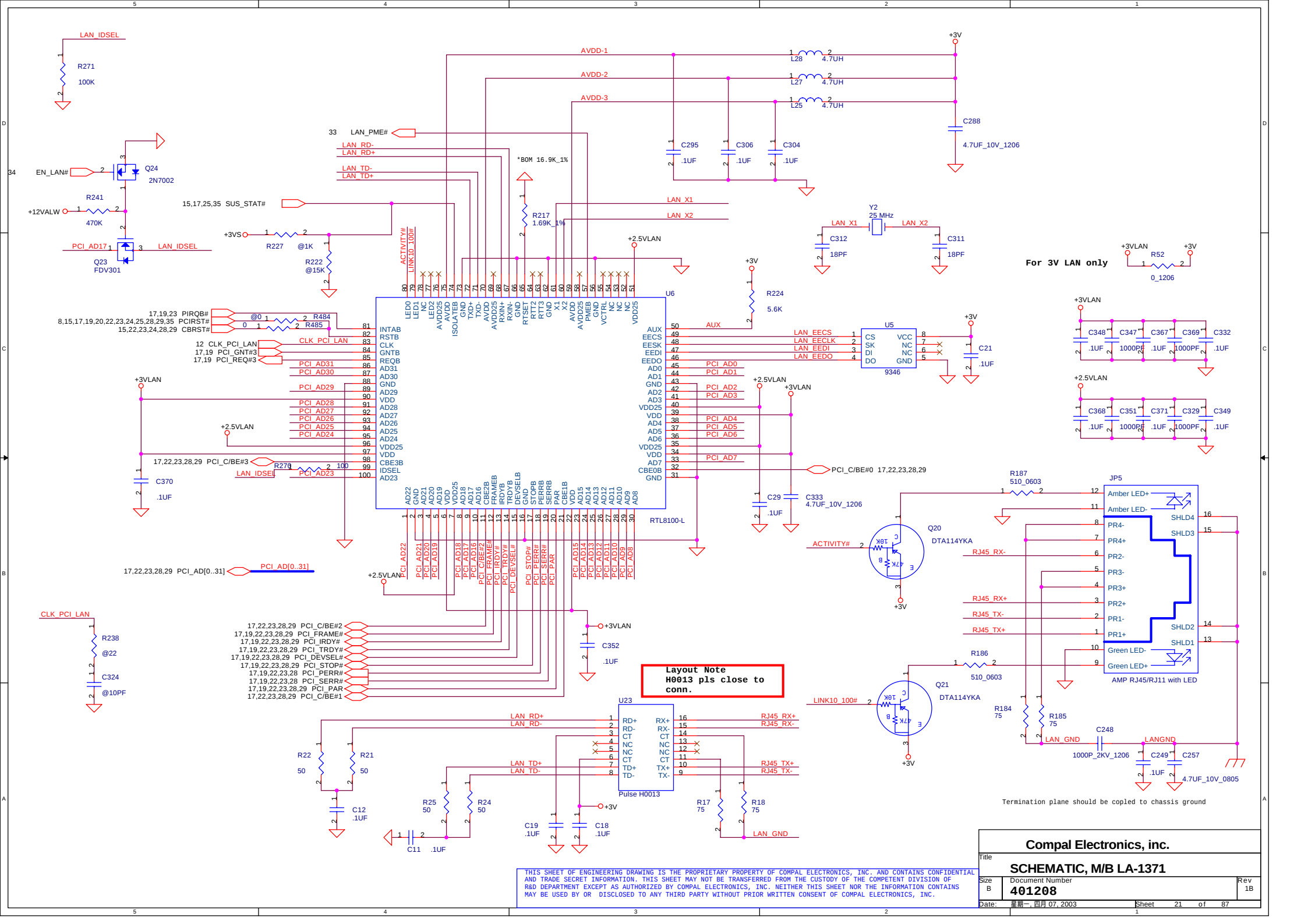
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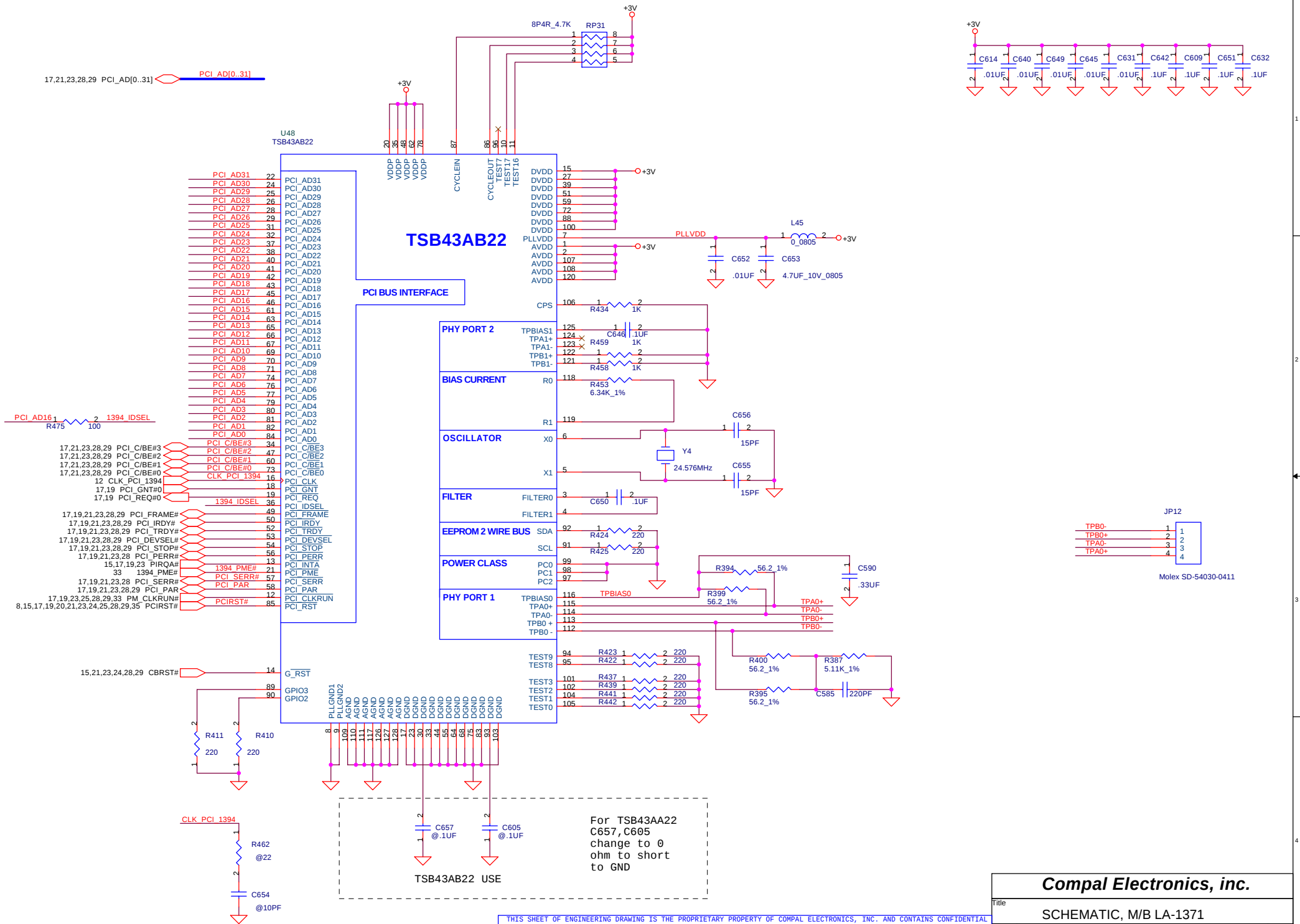
IDE,CD-ROM Module CONN.



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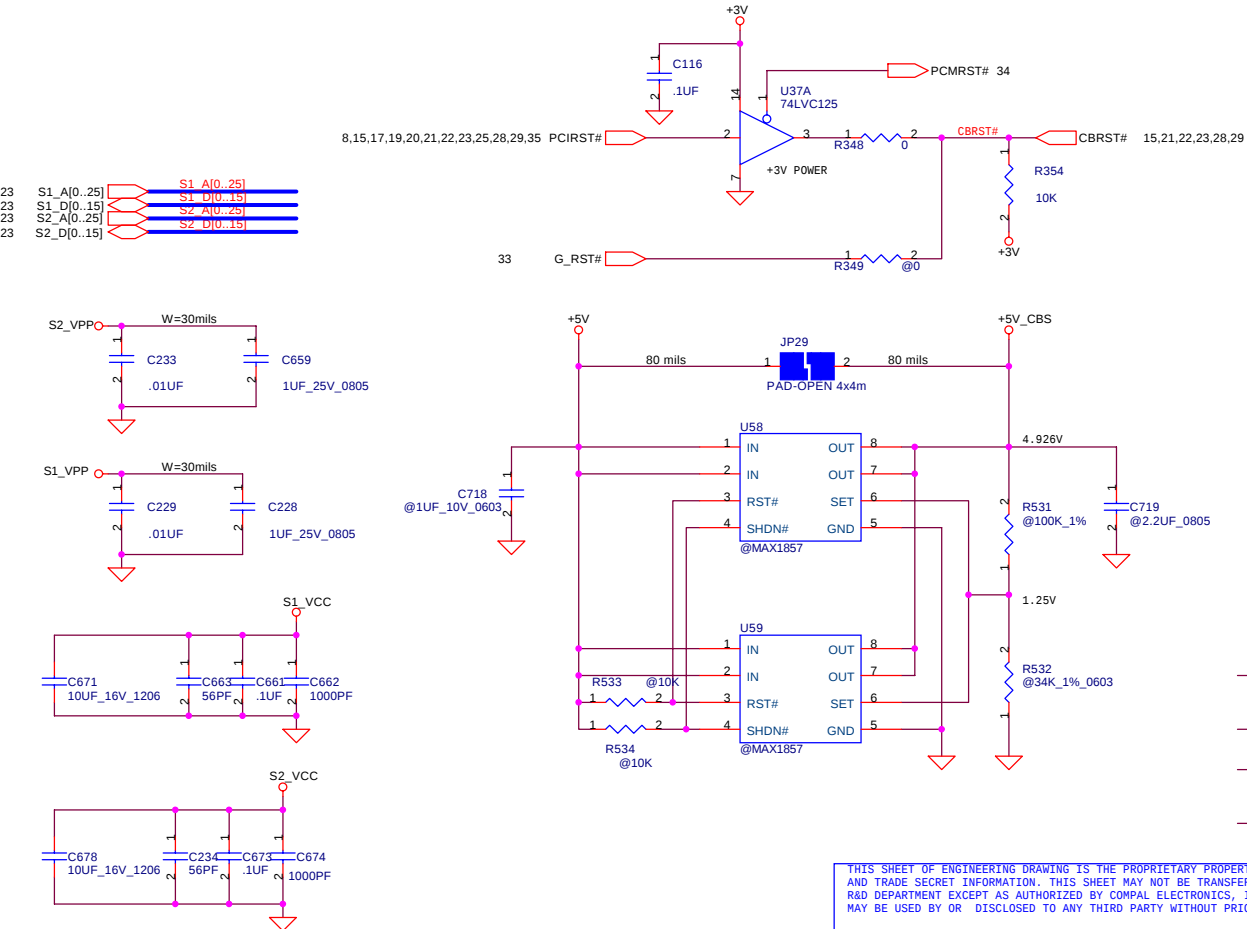
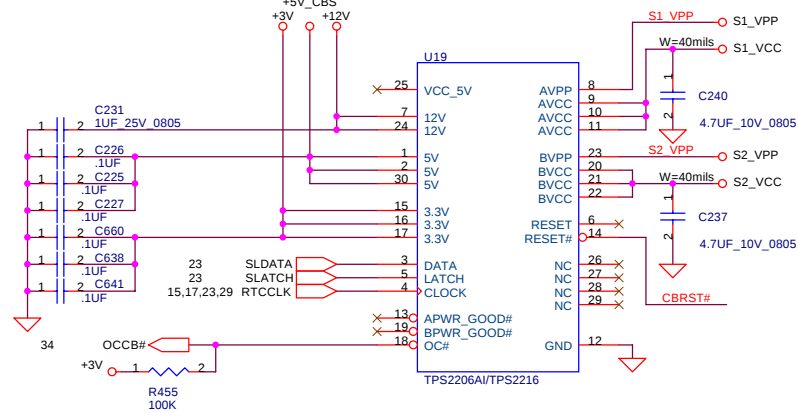
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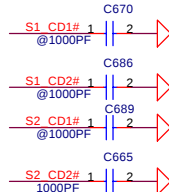
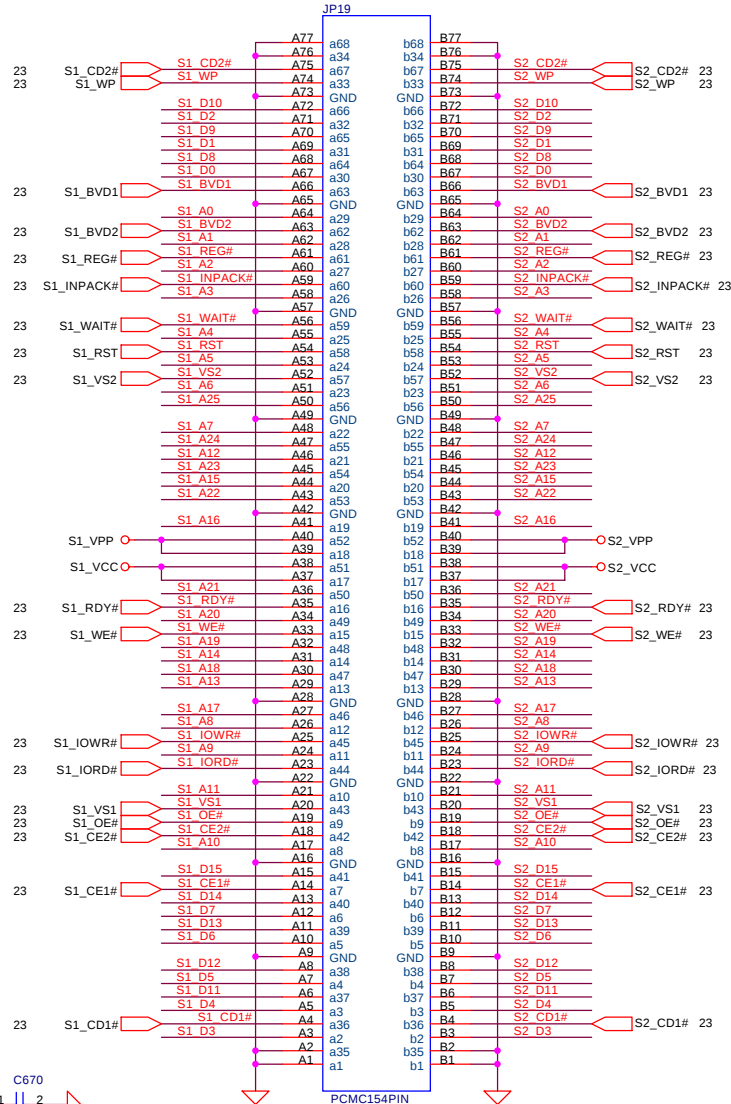




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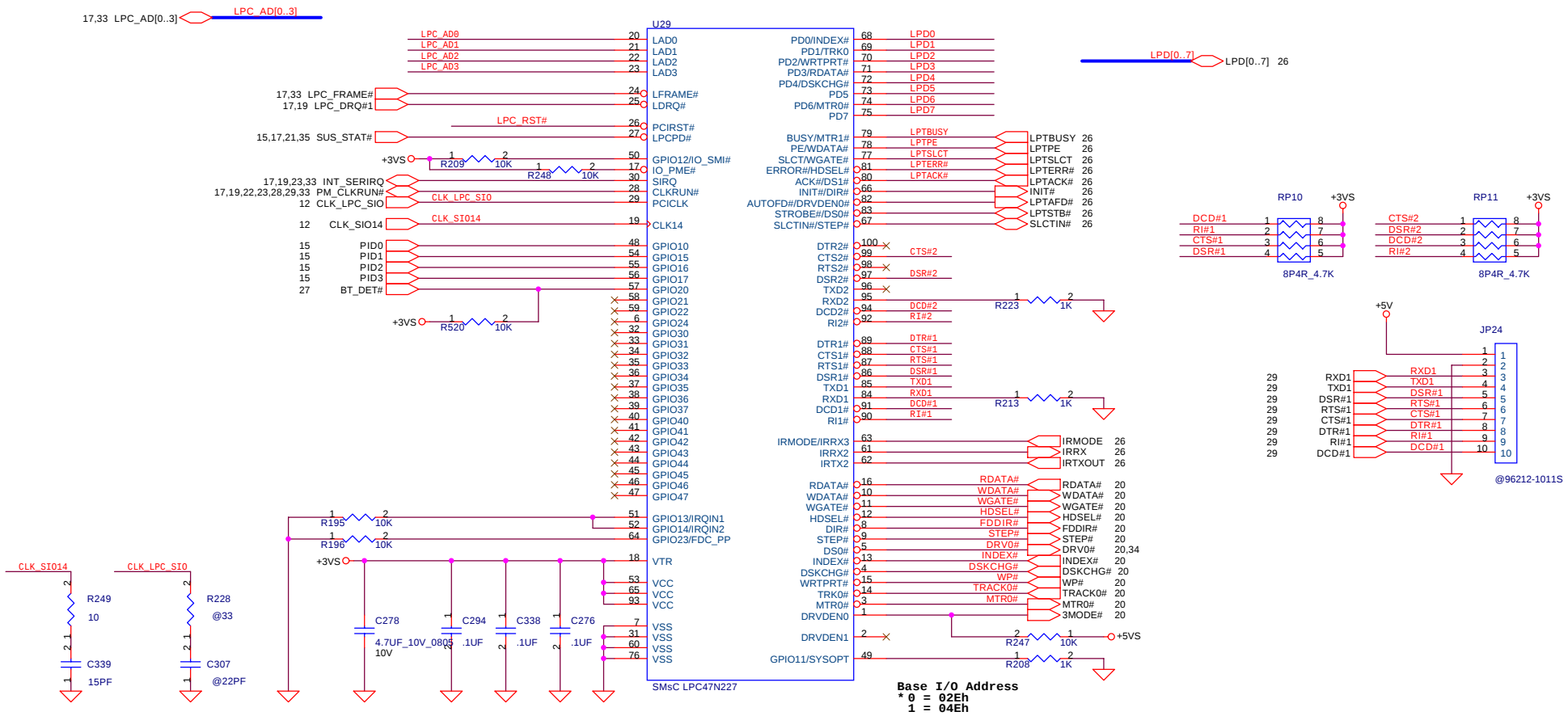


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SOCKET

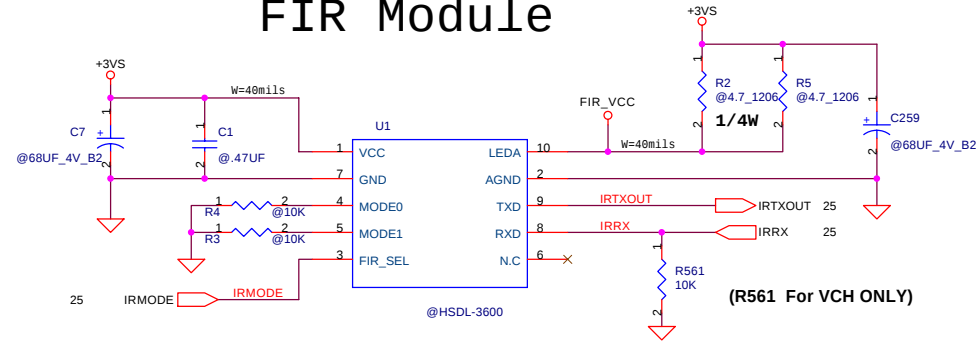


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SUPER I/O SMsC FDC47N227

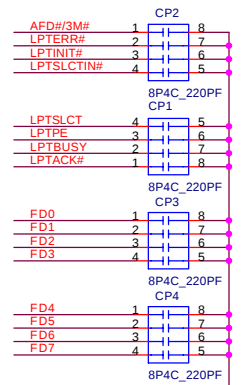
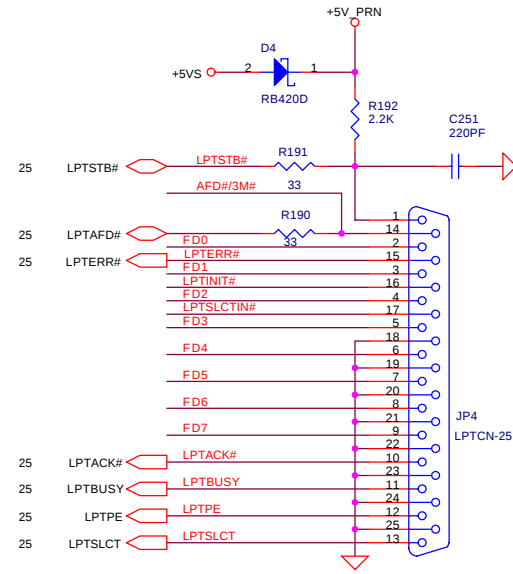
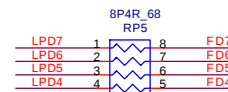
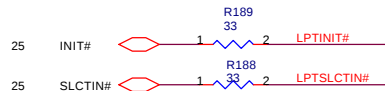
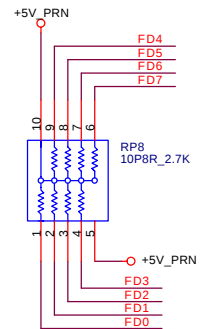
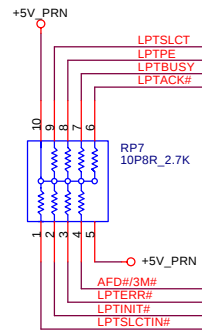


FIR Module



The component's most place
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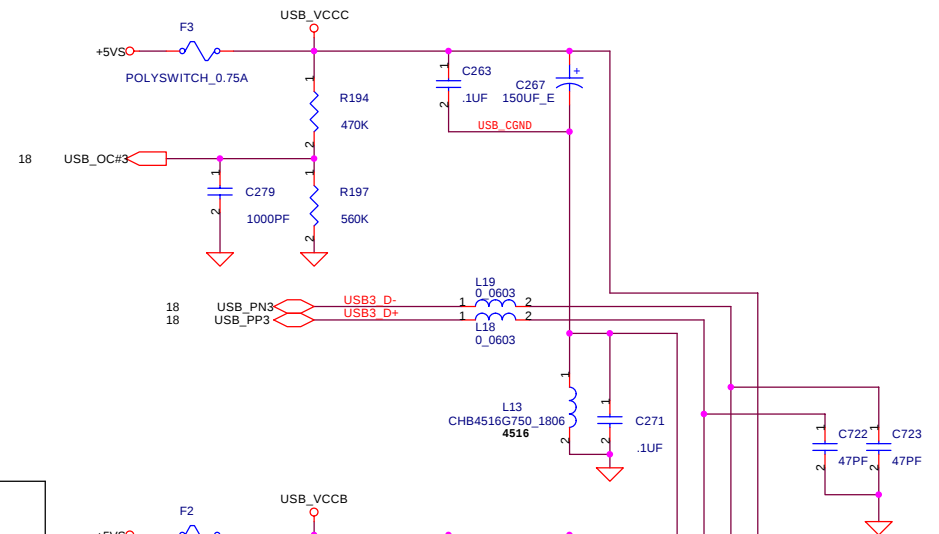
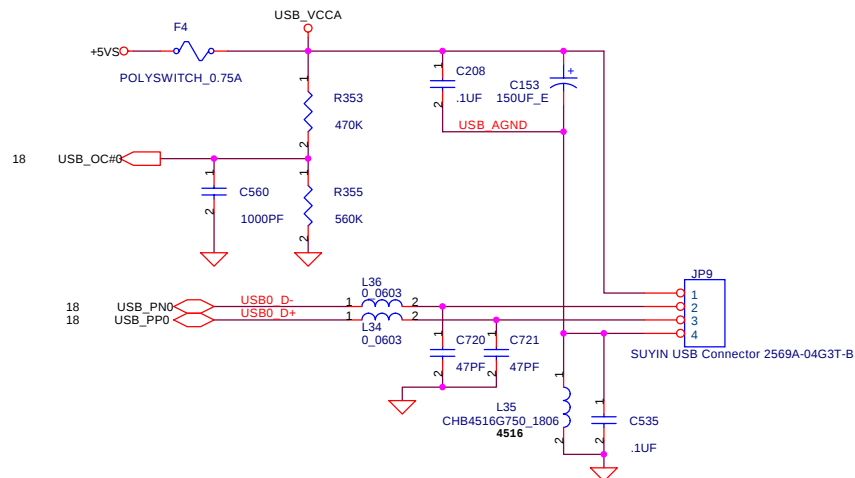
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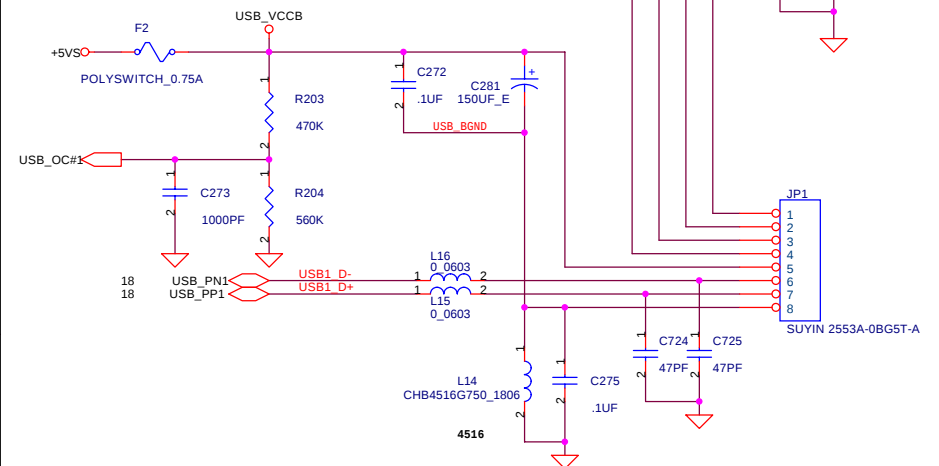
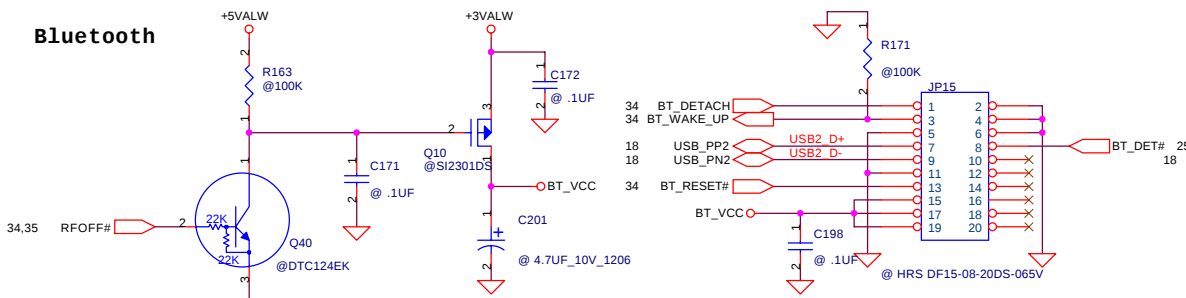
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USB PORT



Bluetooth

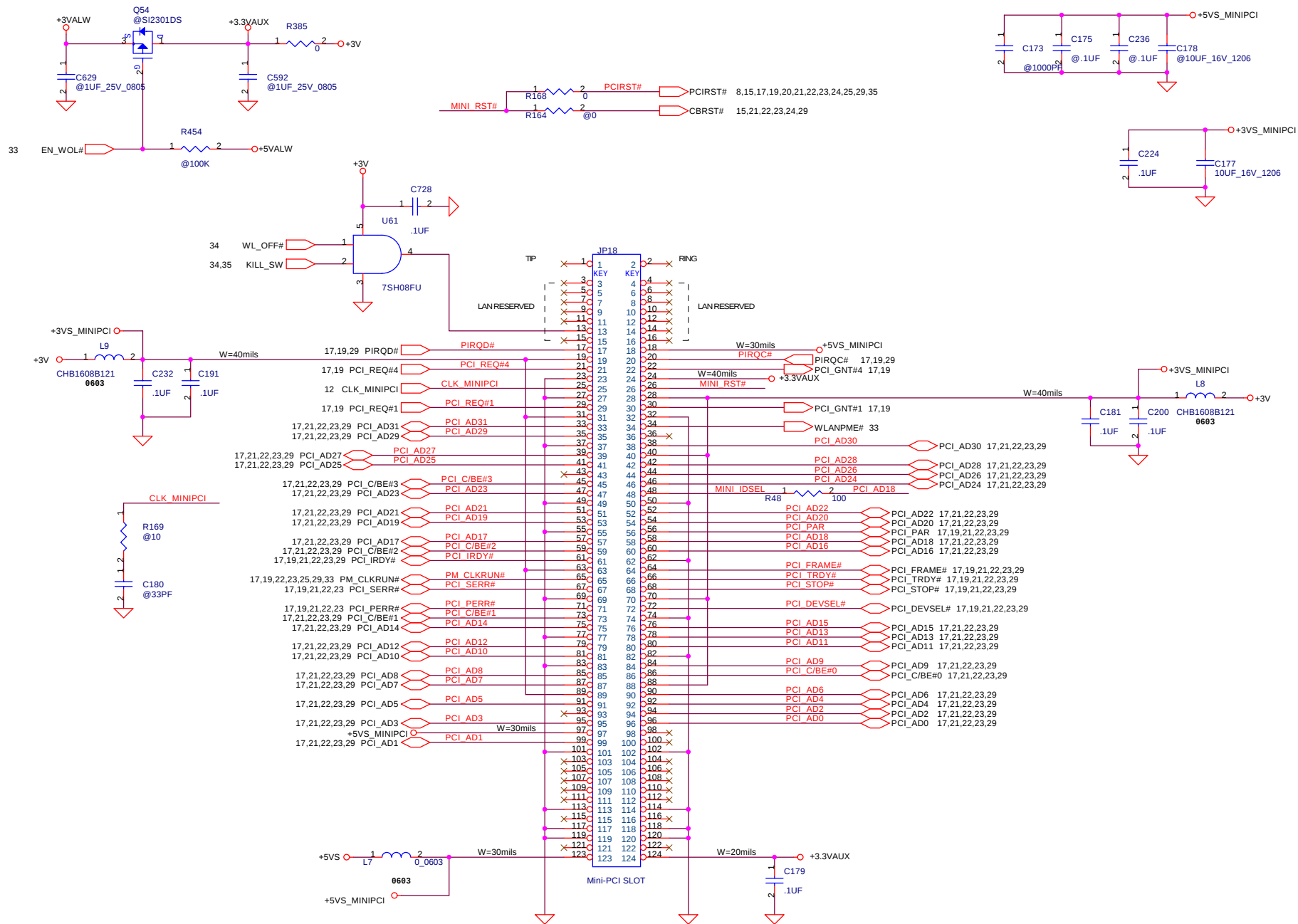


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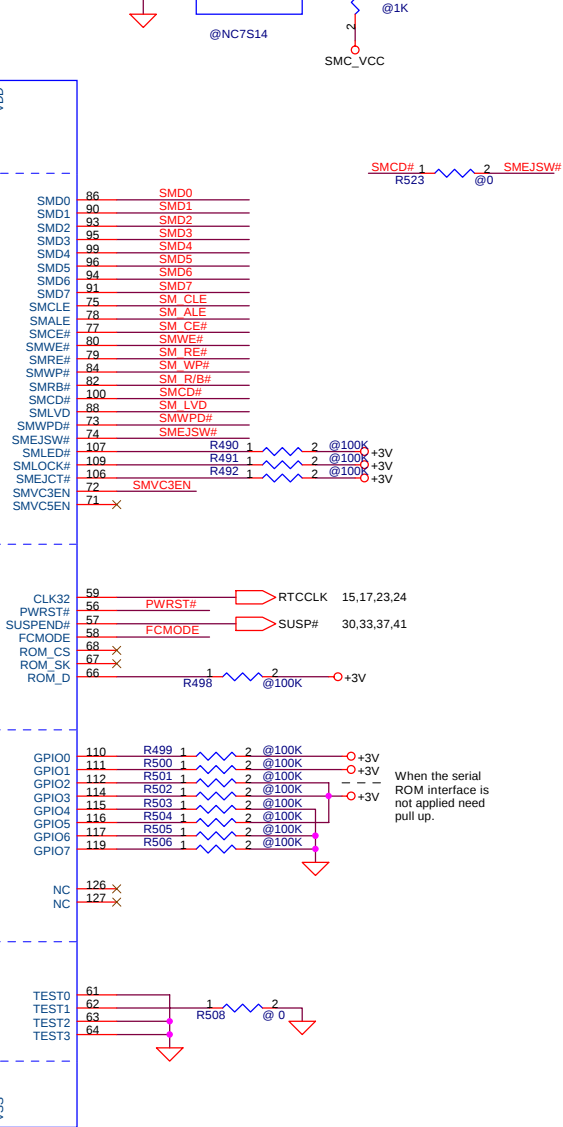
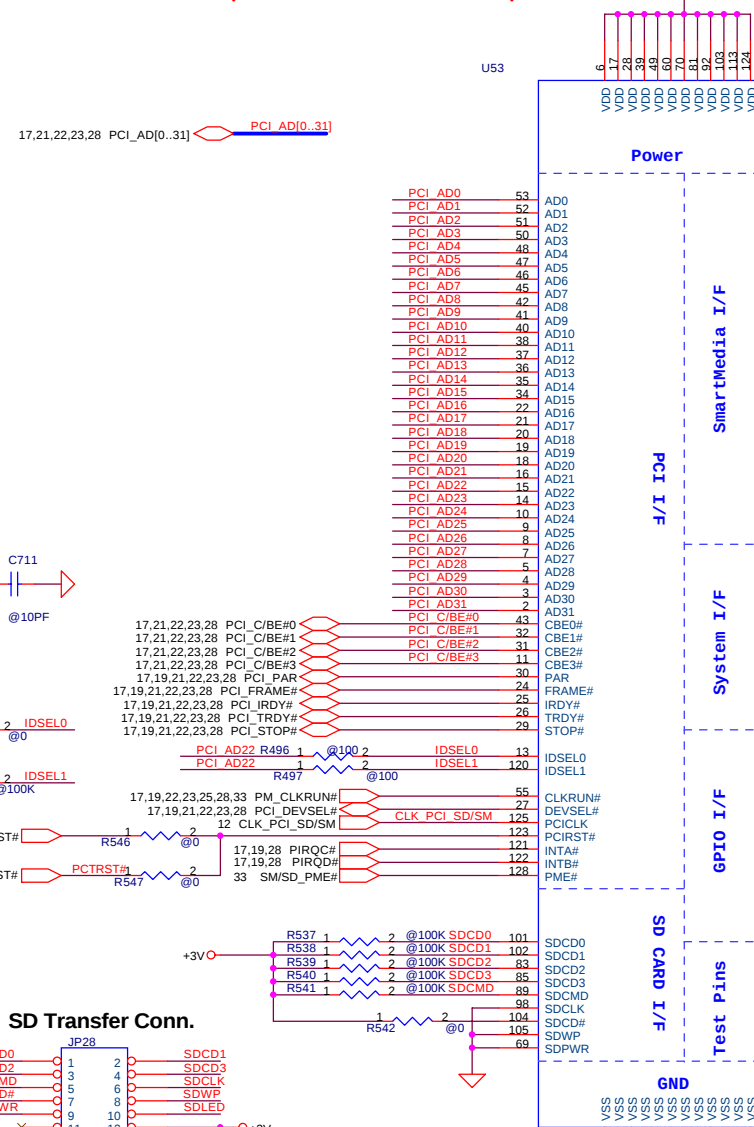
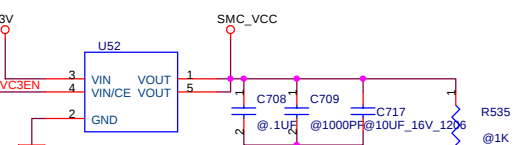
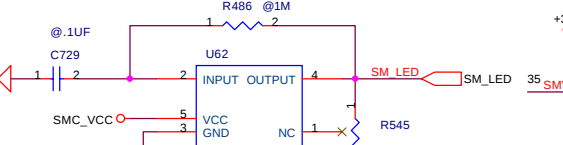
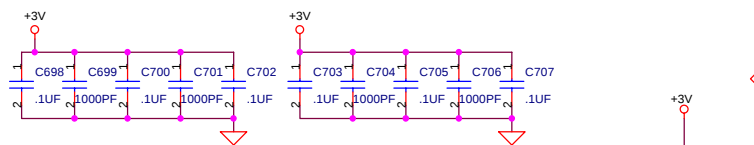
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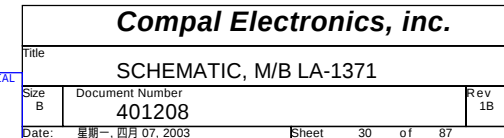
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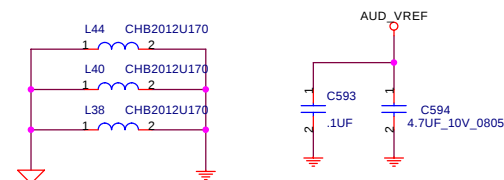
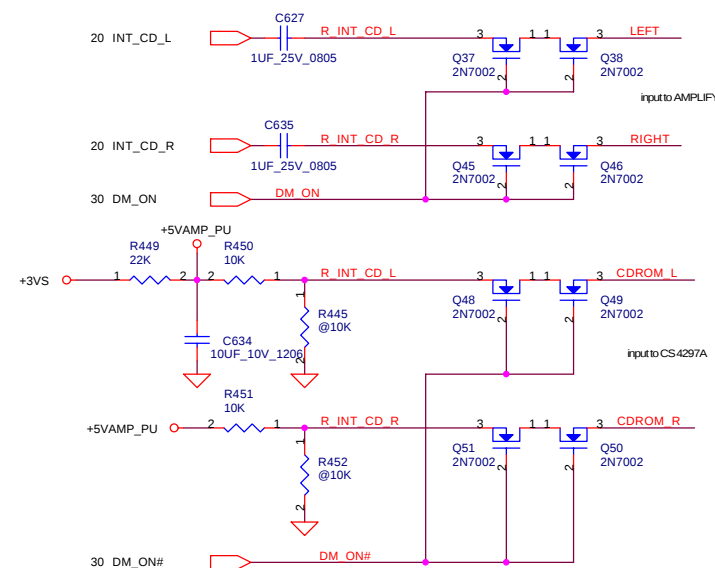
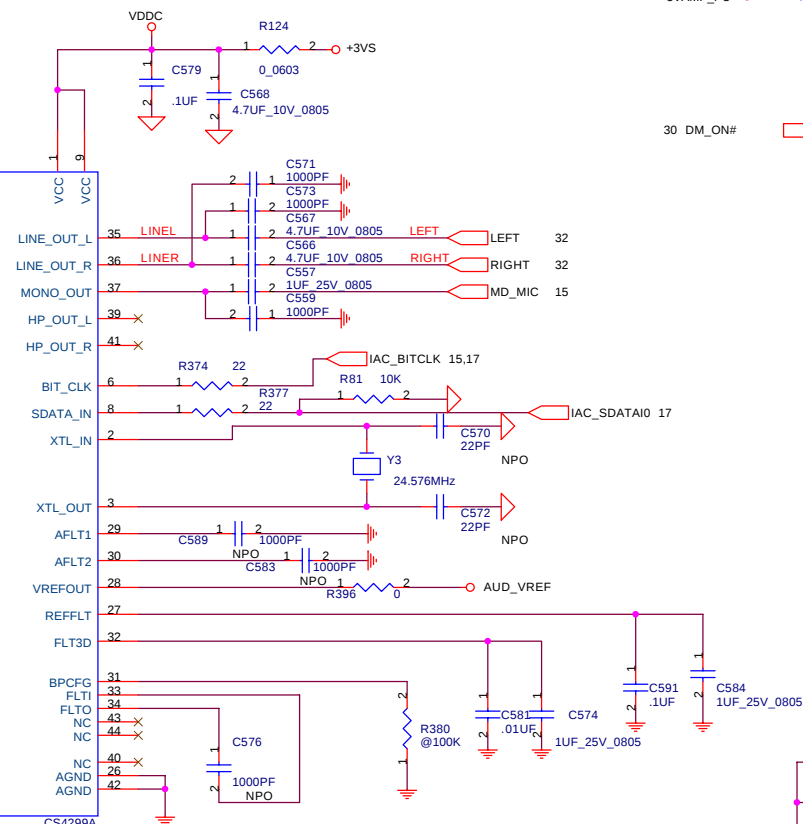
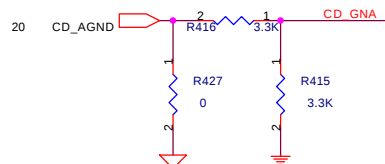
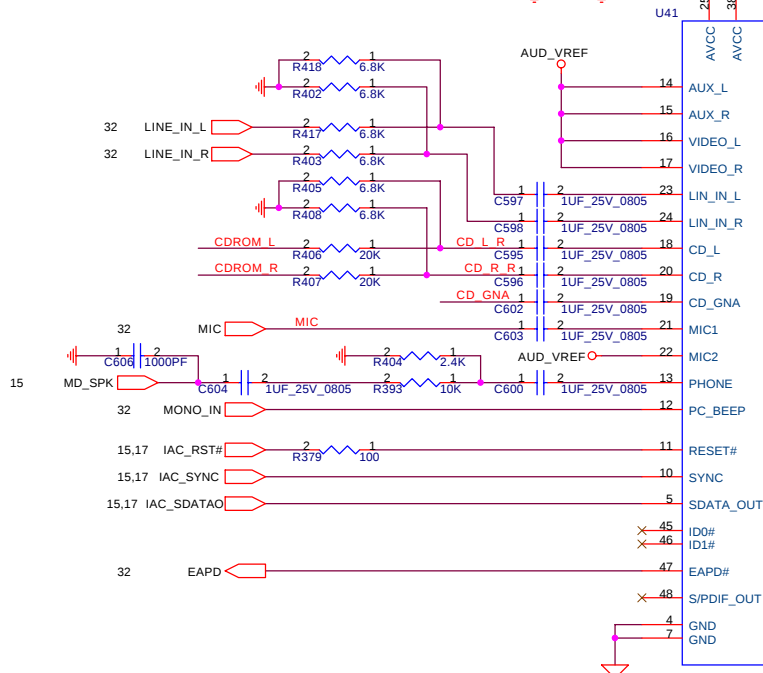
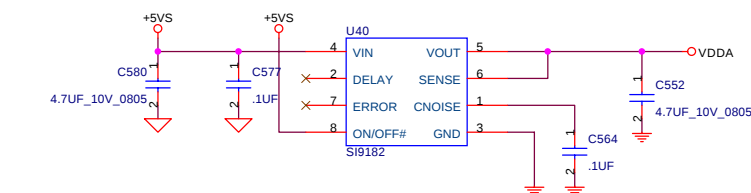
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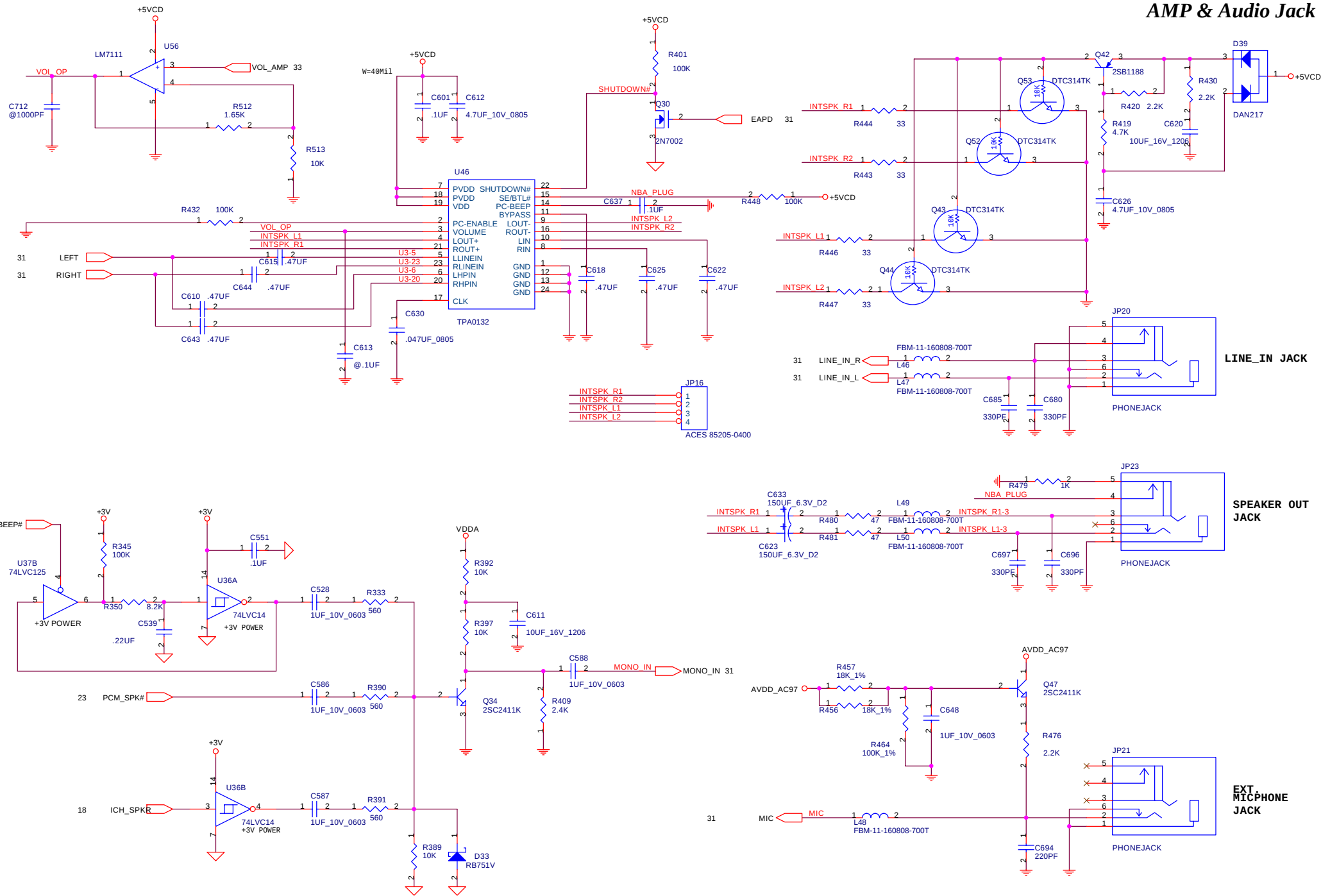


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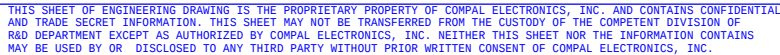
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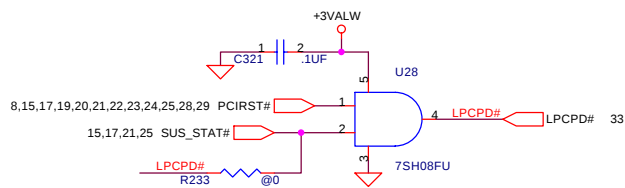
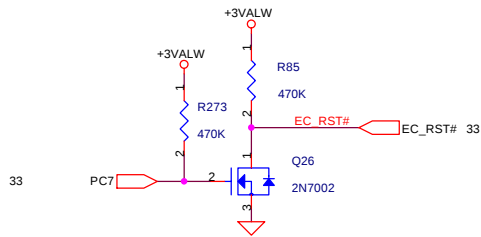
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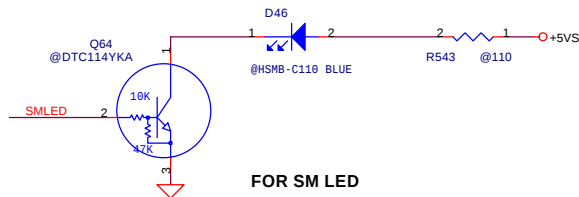
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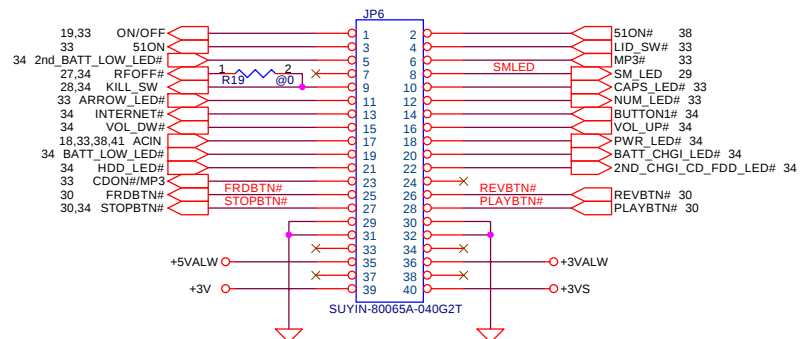
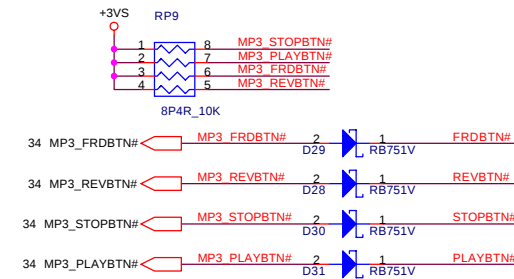




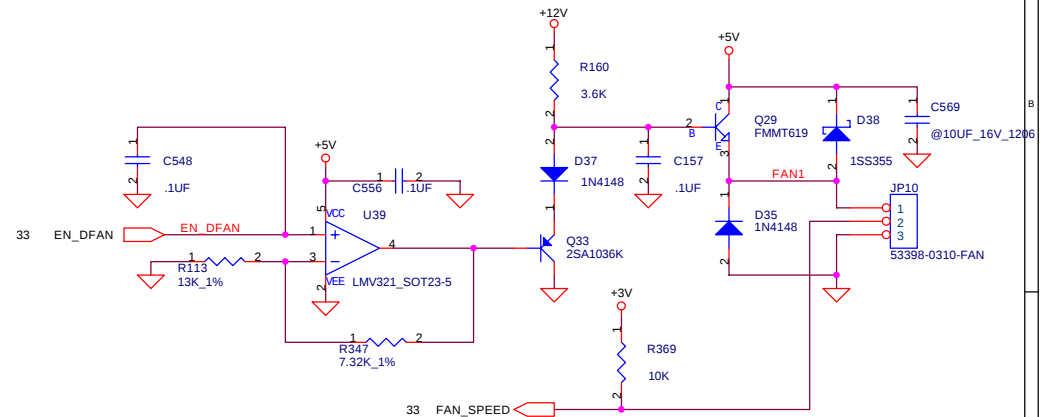
For PC87591 REV 0.A Only



FOR SM LED



FAN CONN.

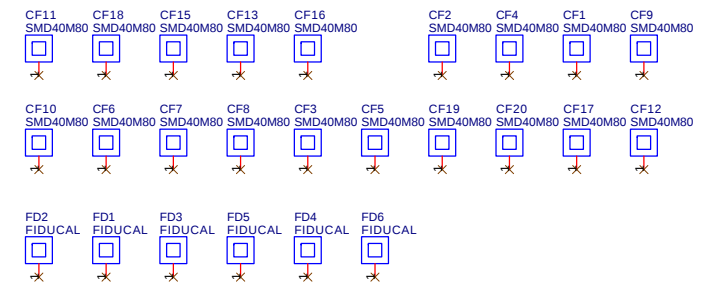
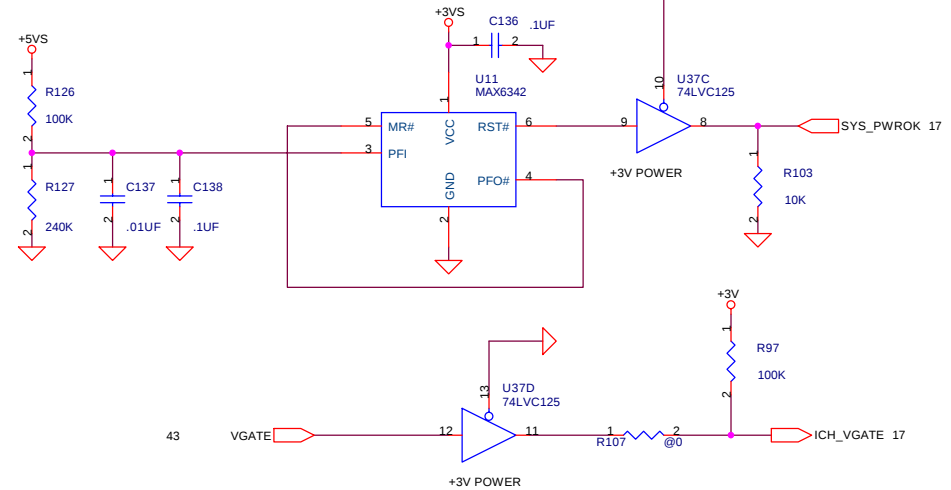
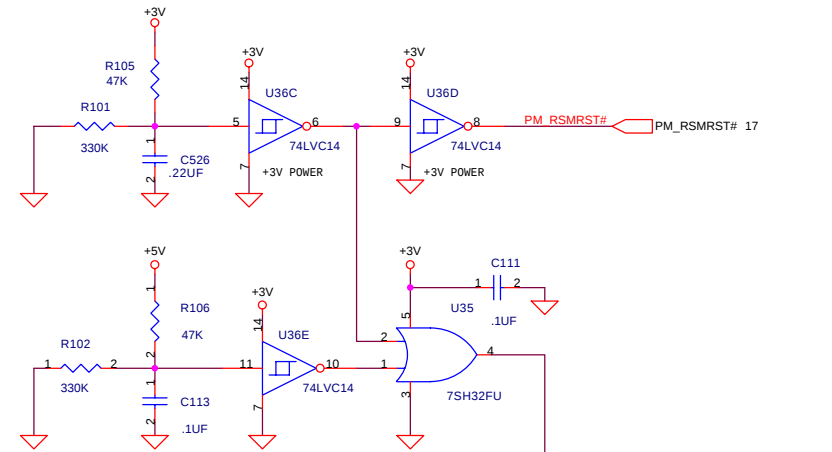
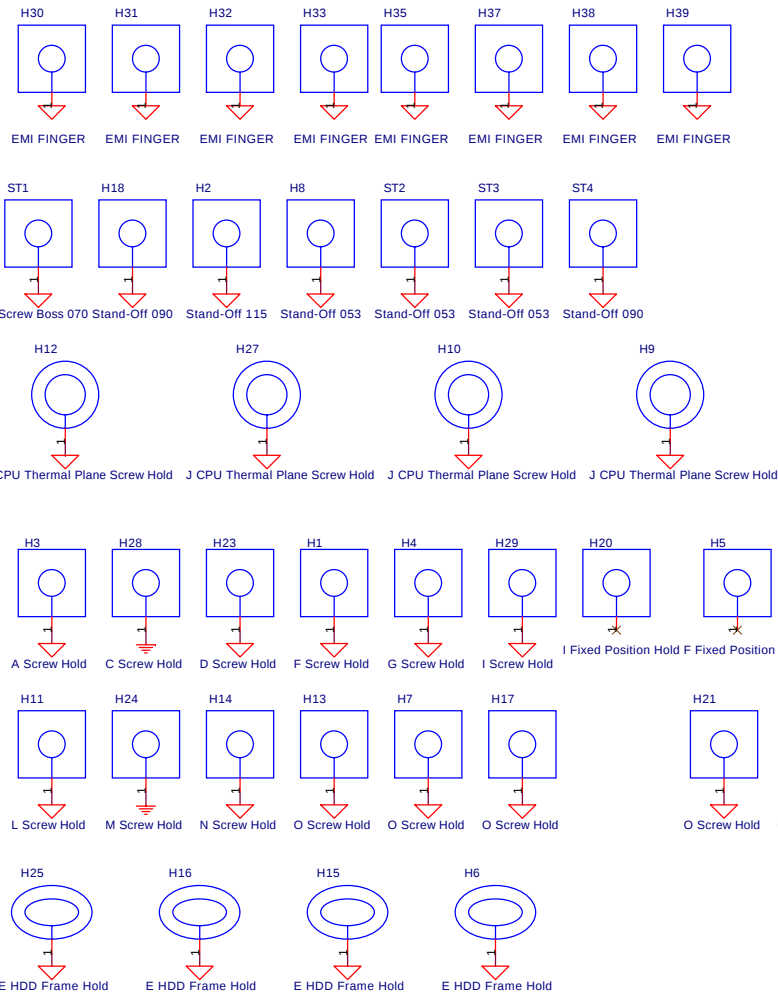
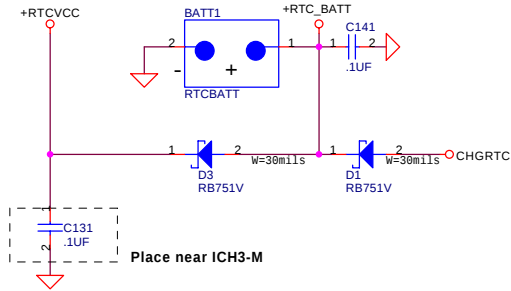


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RTC Batt. Connector

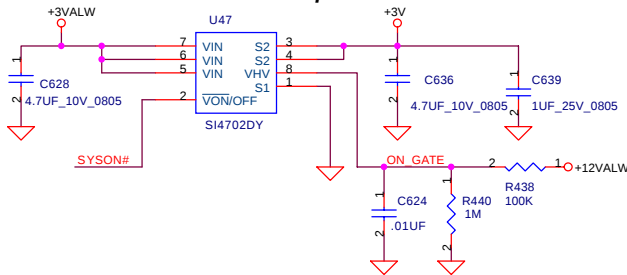


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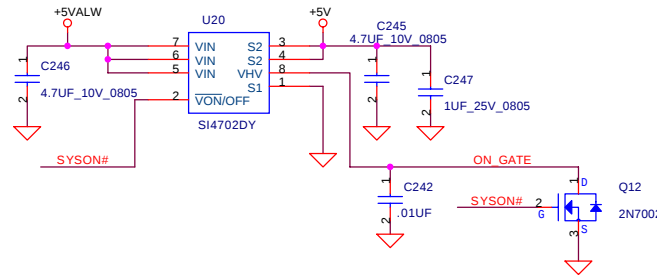
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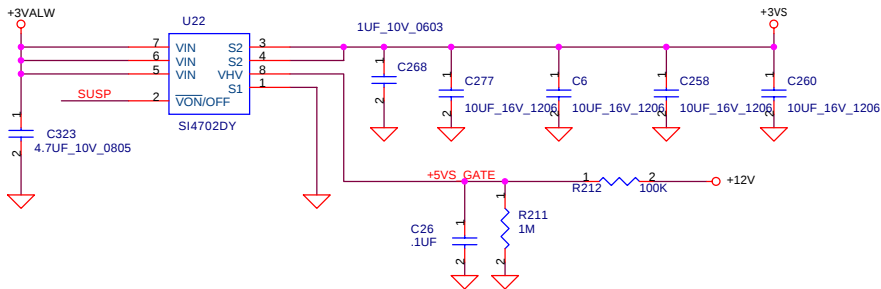
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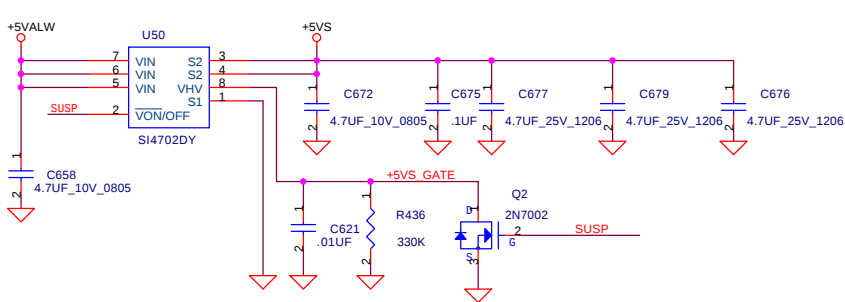
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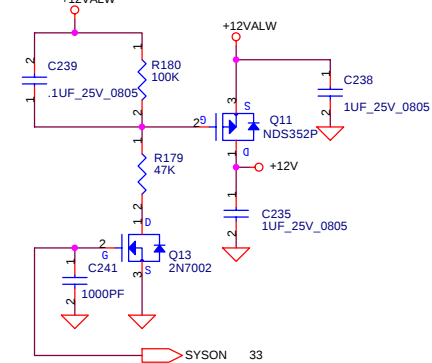
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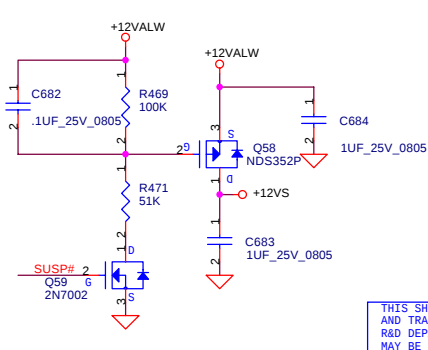
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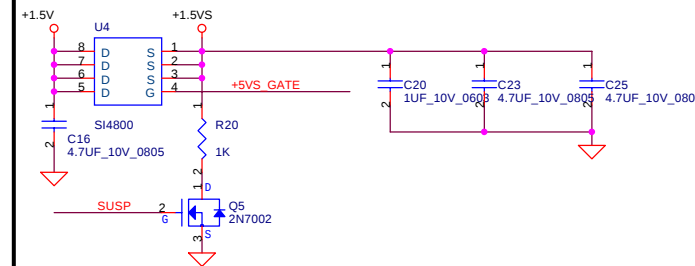
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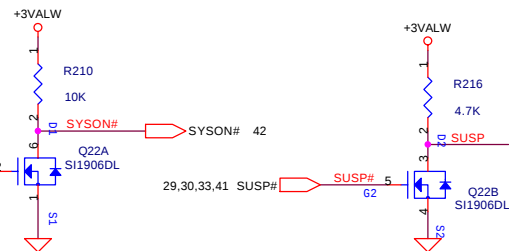
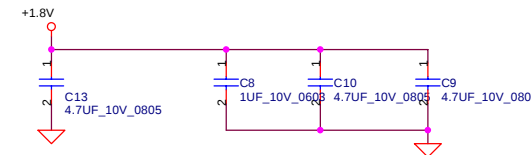
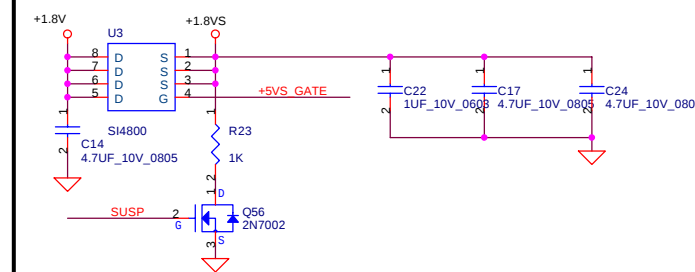
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+1.5V TO +1.5V_SW Transfer



+1.8V_ALW TO +1.8V_SW Transfer



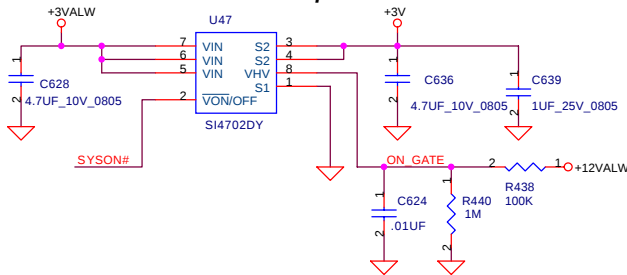
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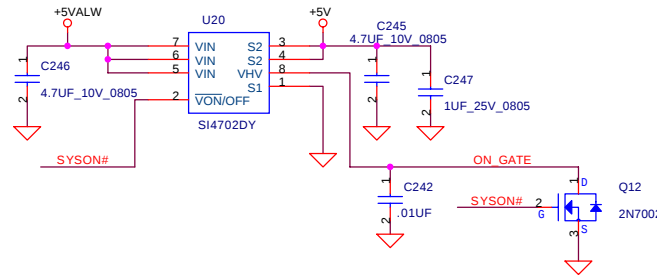
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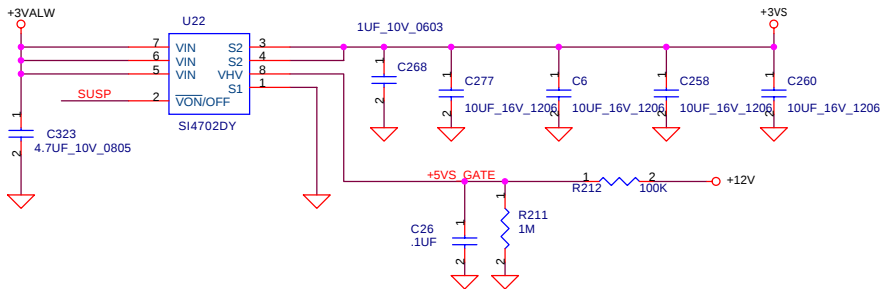
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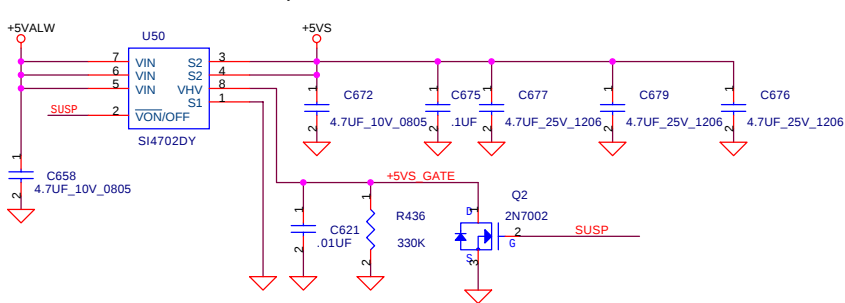
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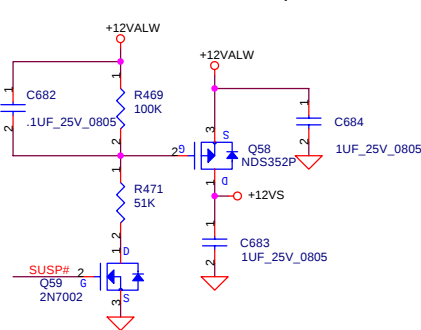
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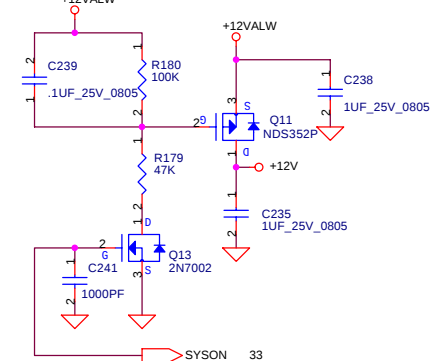
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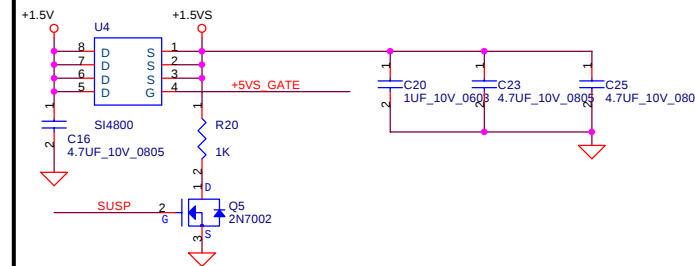
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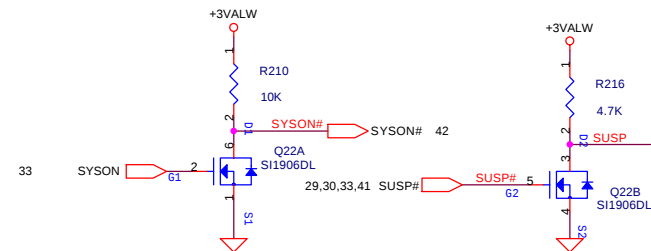
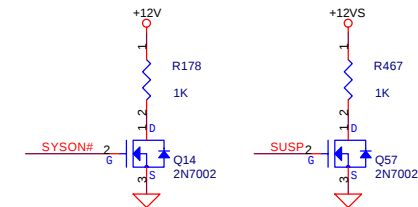
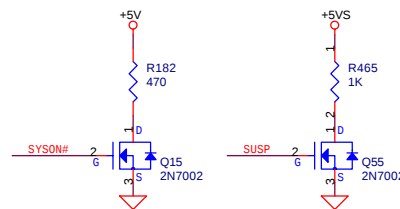
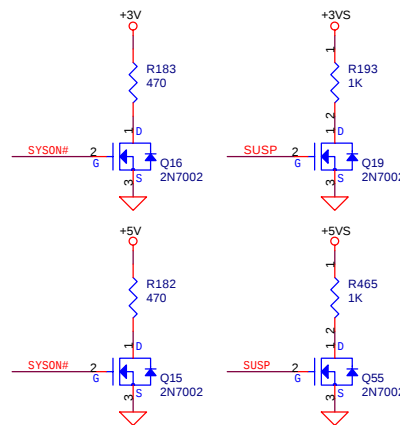
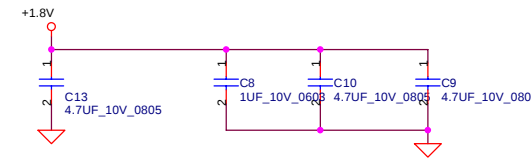
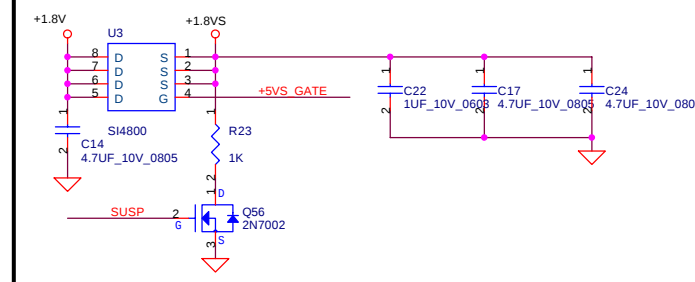
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+1.5V TO +1.5V_SW Transfer



+1.8V_ALW TO +1.8V_SW Transfer

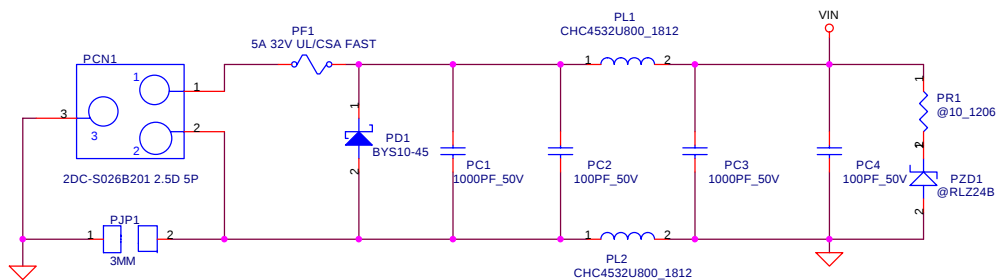


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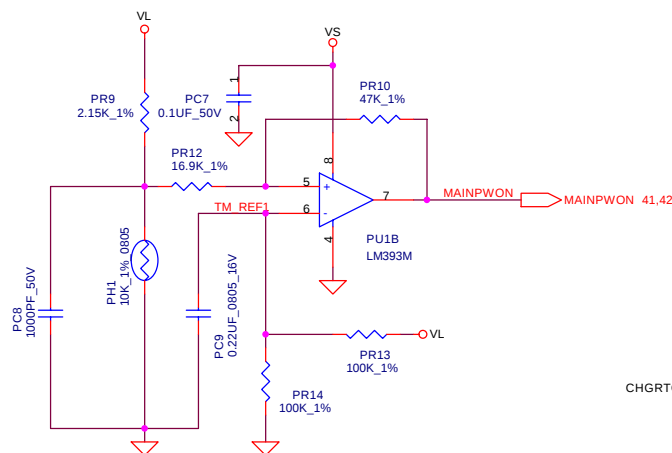
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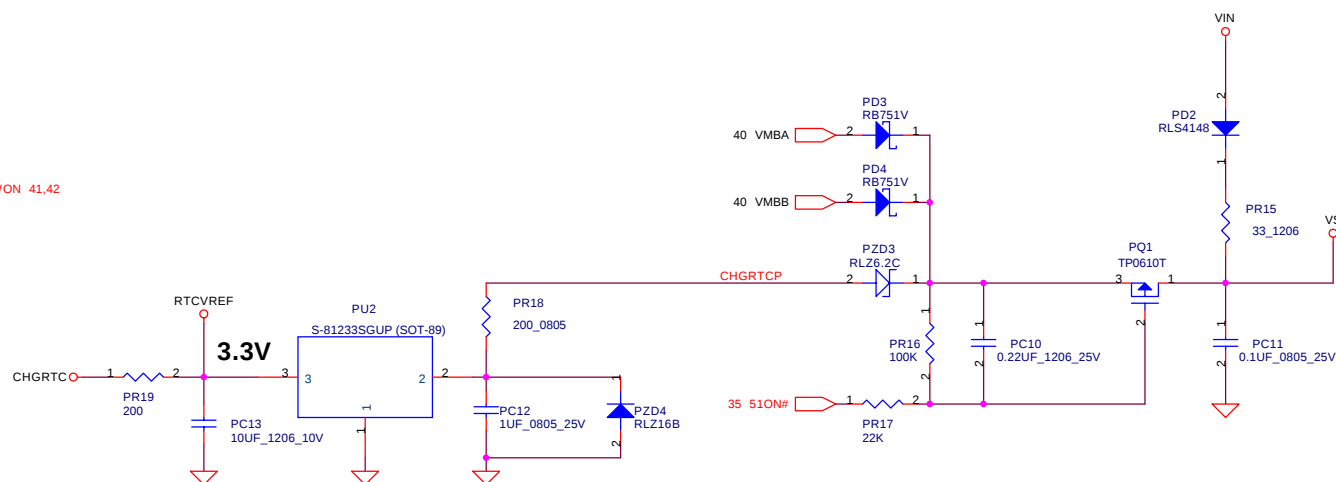
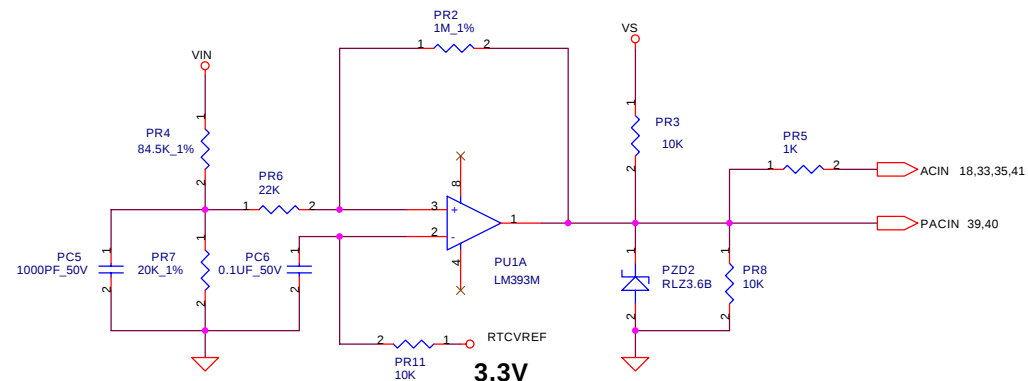


PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 50(51) degree C



Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038



+12VALWP 2 PJP2 1 +12VALW (120mA,20mils ,Via NO.= 1)
JOPEN/+12V

+5VALWP 1 PJP3 2 +5VALW (5A,200mils ,Via NO.= 10)
PAD-OPEN 4x4mm

+3VALWP 1 PJP4 2 +3VALW (5A,200mils ,Via NO.= 10)
PAD-OPEN 4x4mm

+1_5VP 2 PJP5 1 +1.5V (1.5A,60mils ,Via NO.= 3)
3MMA/CPU_IO

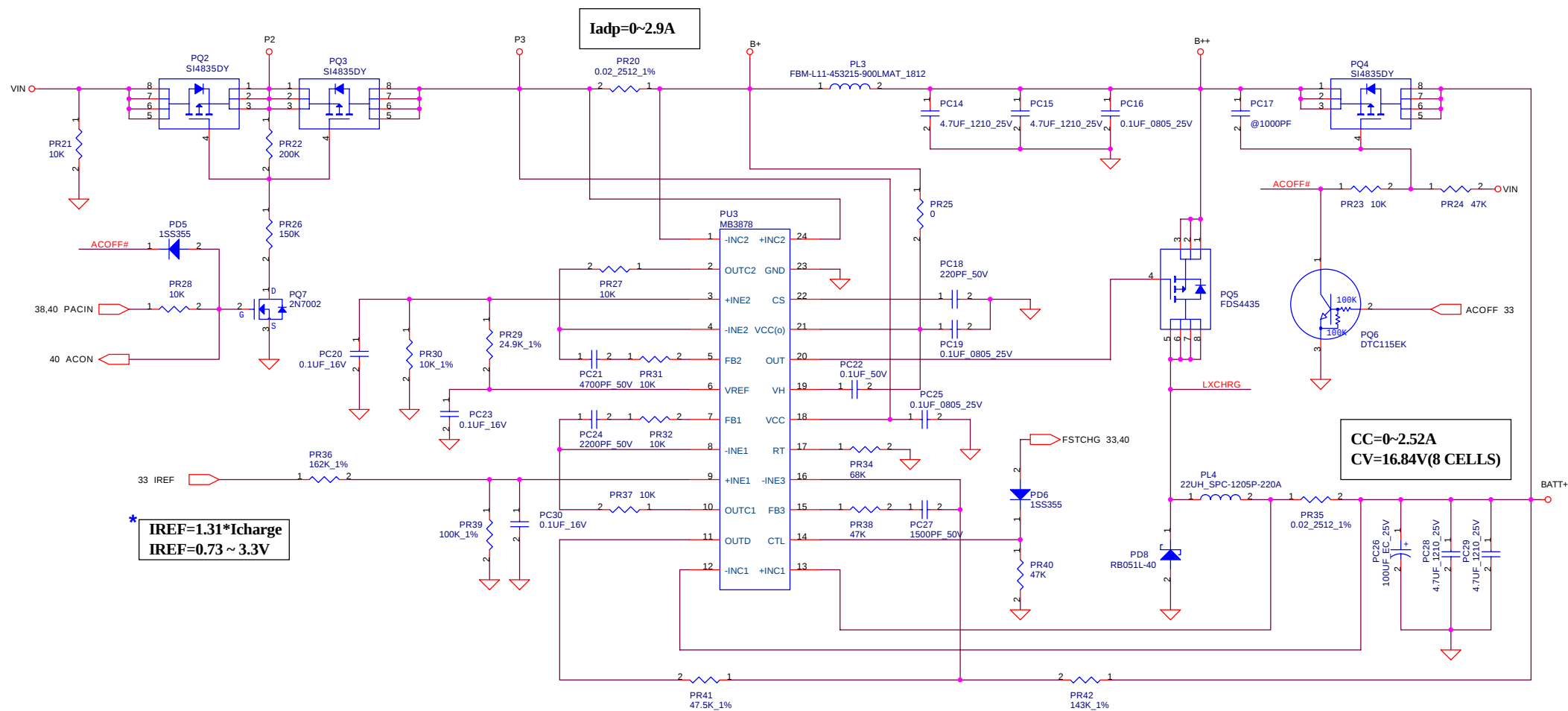
+1_8VP 2 PJP6 1 +1.8V (3A,120mils ,Via NO.= 6)
3MMA/CPU_IO

+VTP 1 PJP7 2 +VTT (6A,240mils ,Via NO.= 12)
PAD-OPEN 4x4mm

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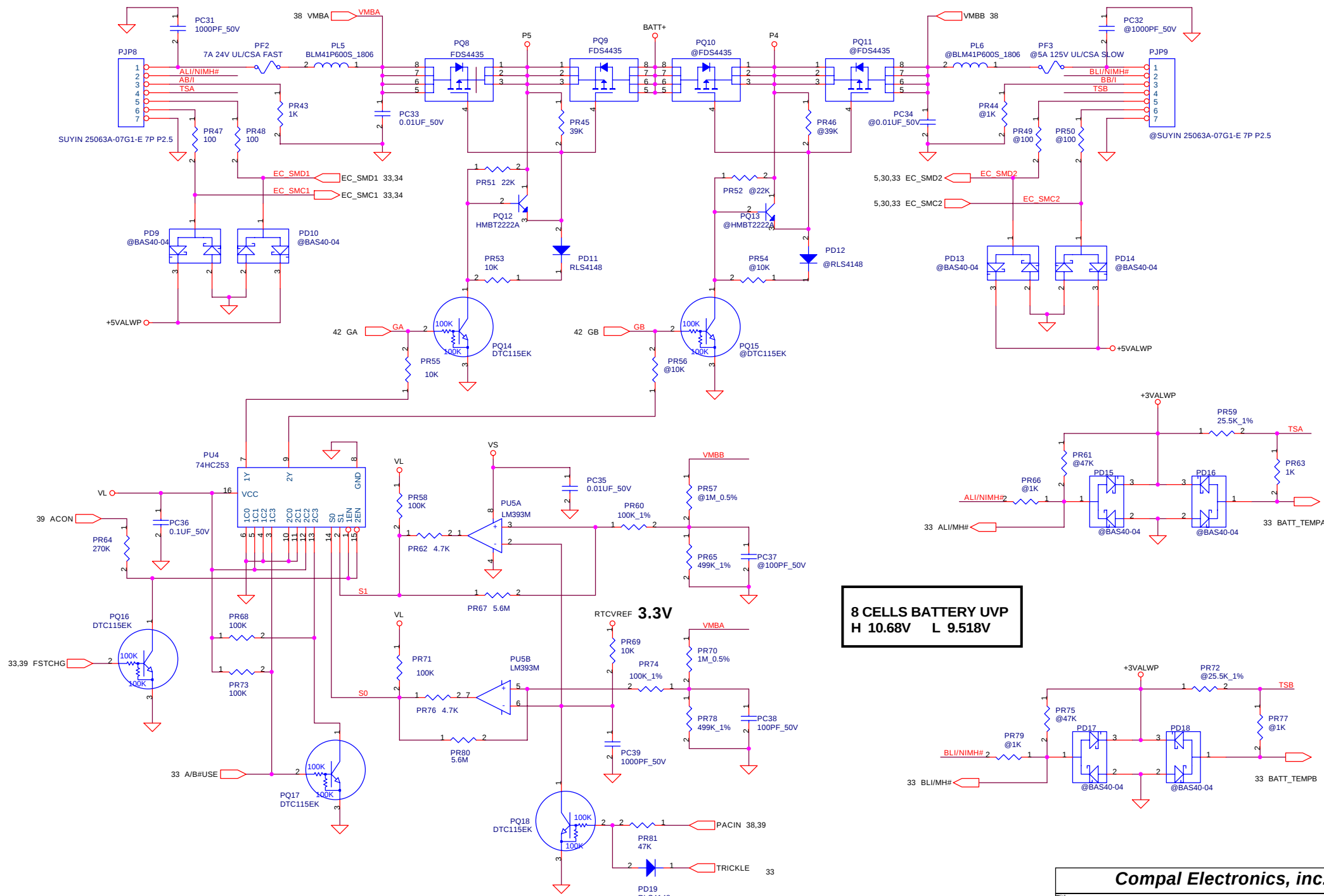
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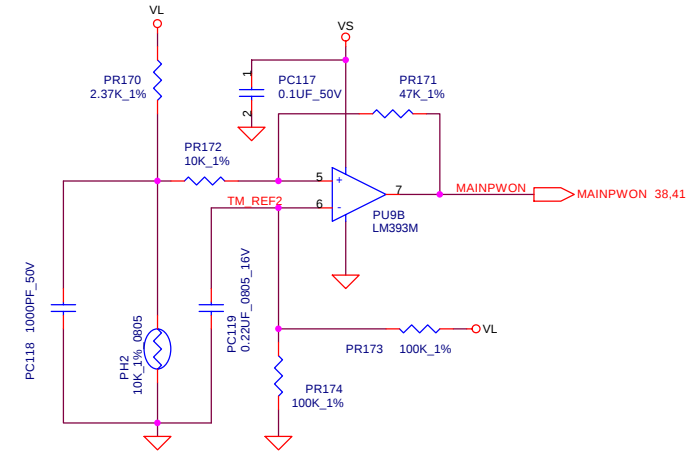
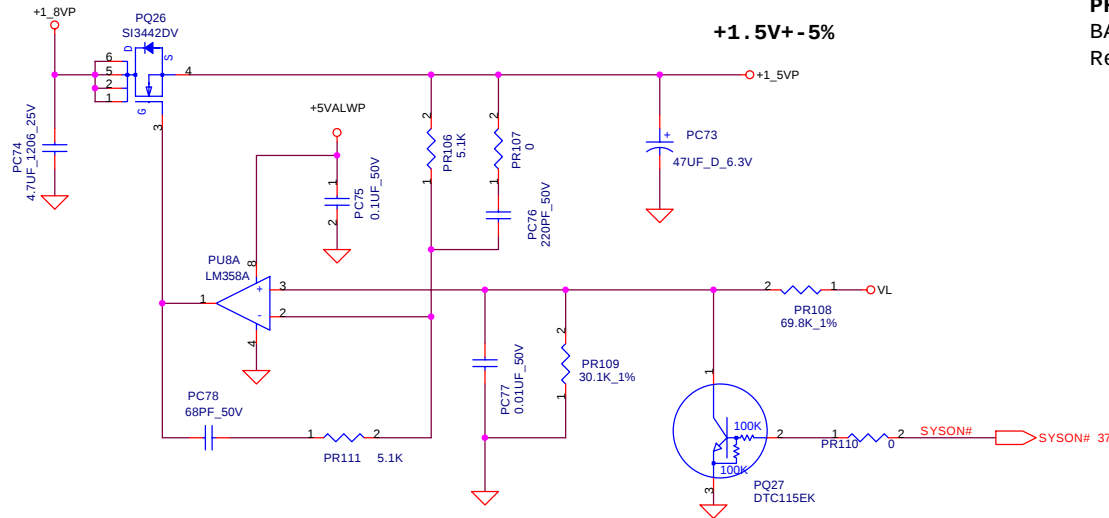


8 CELLS BATTERY UVP
H 10.68V L 9.518V

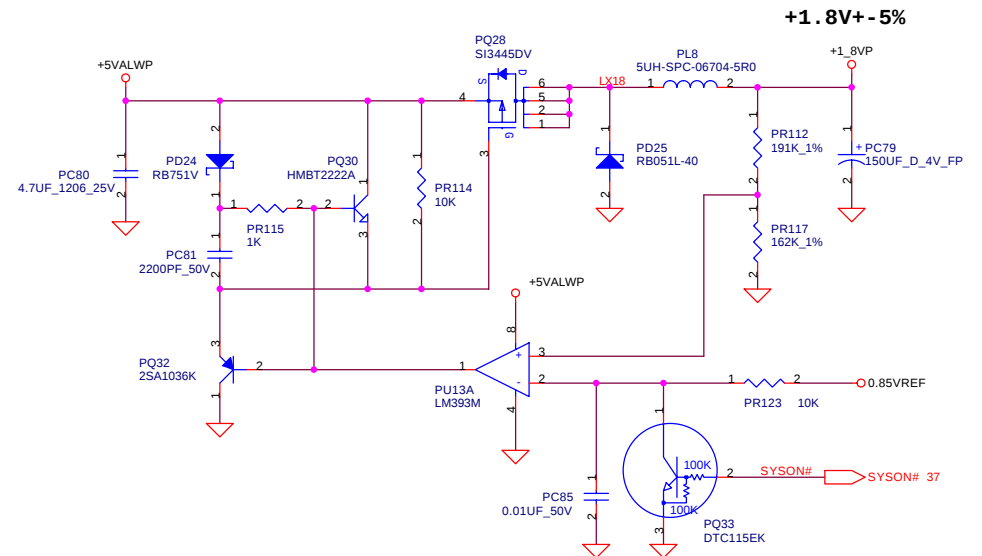
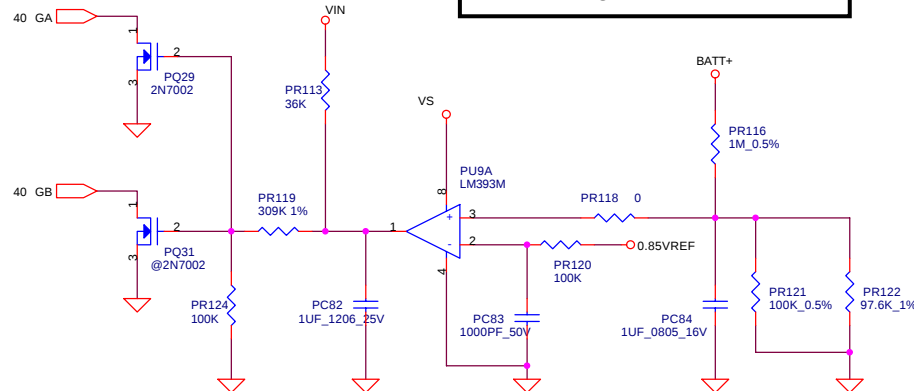
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PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50(51) degree C



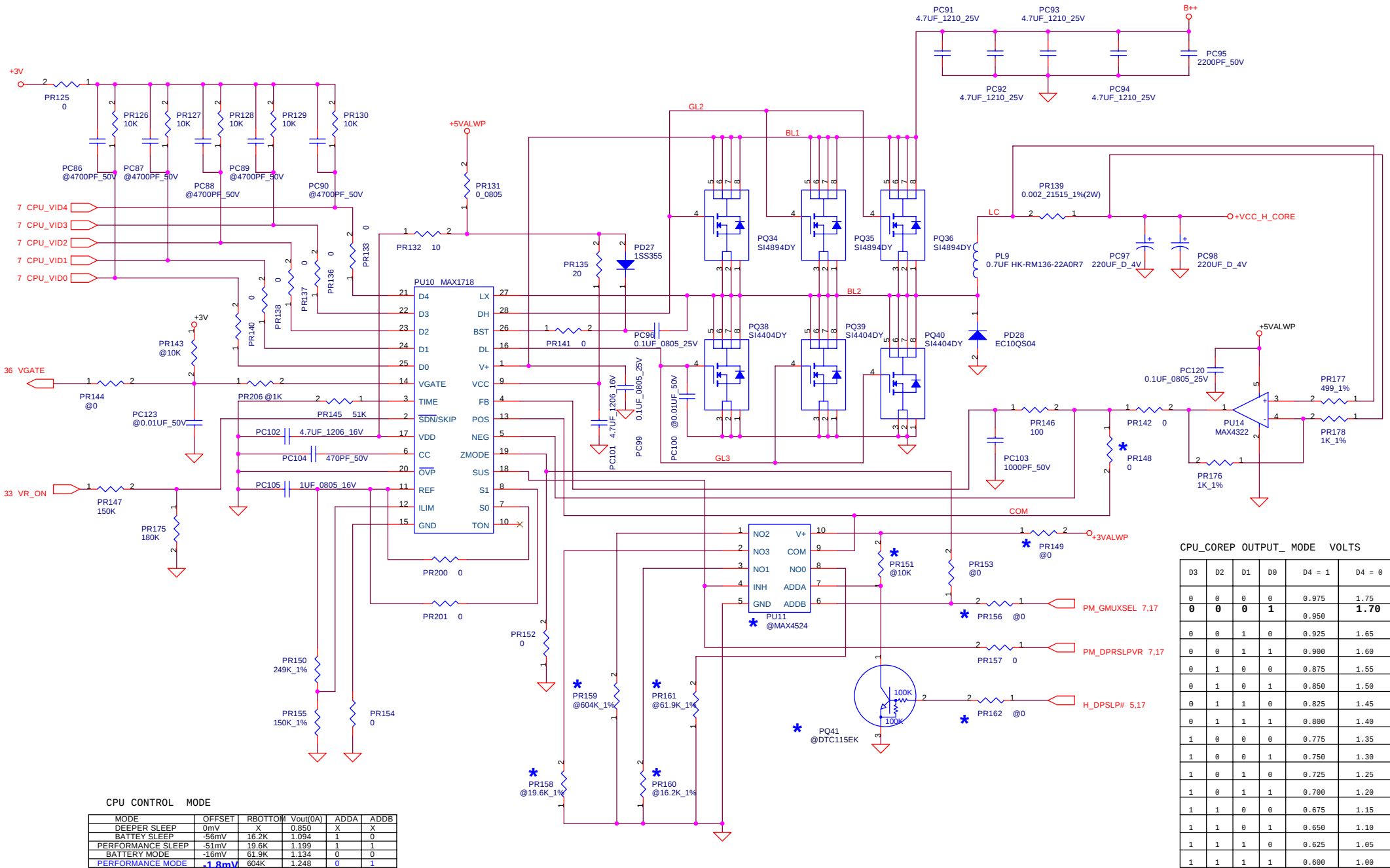
8 Cells Charger OVP : 18.059V



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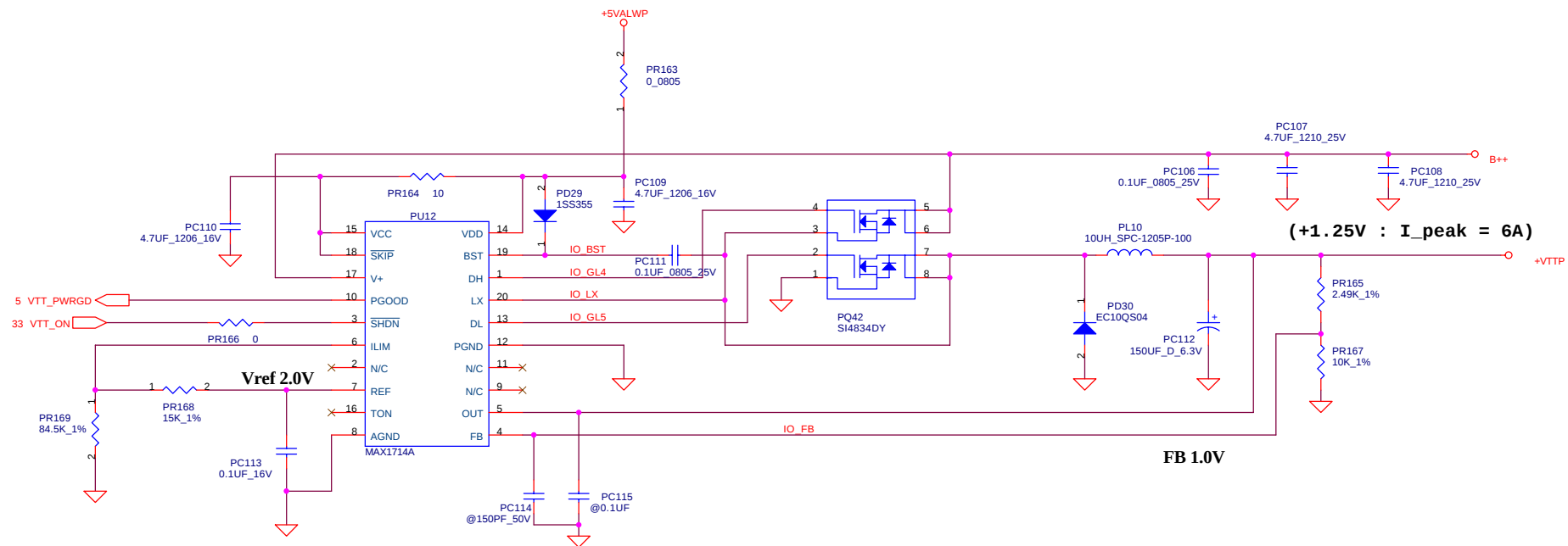
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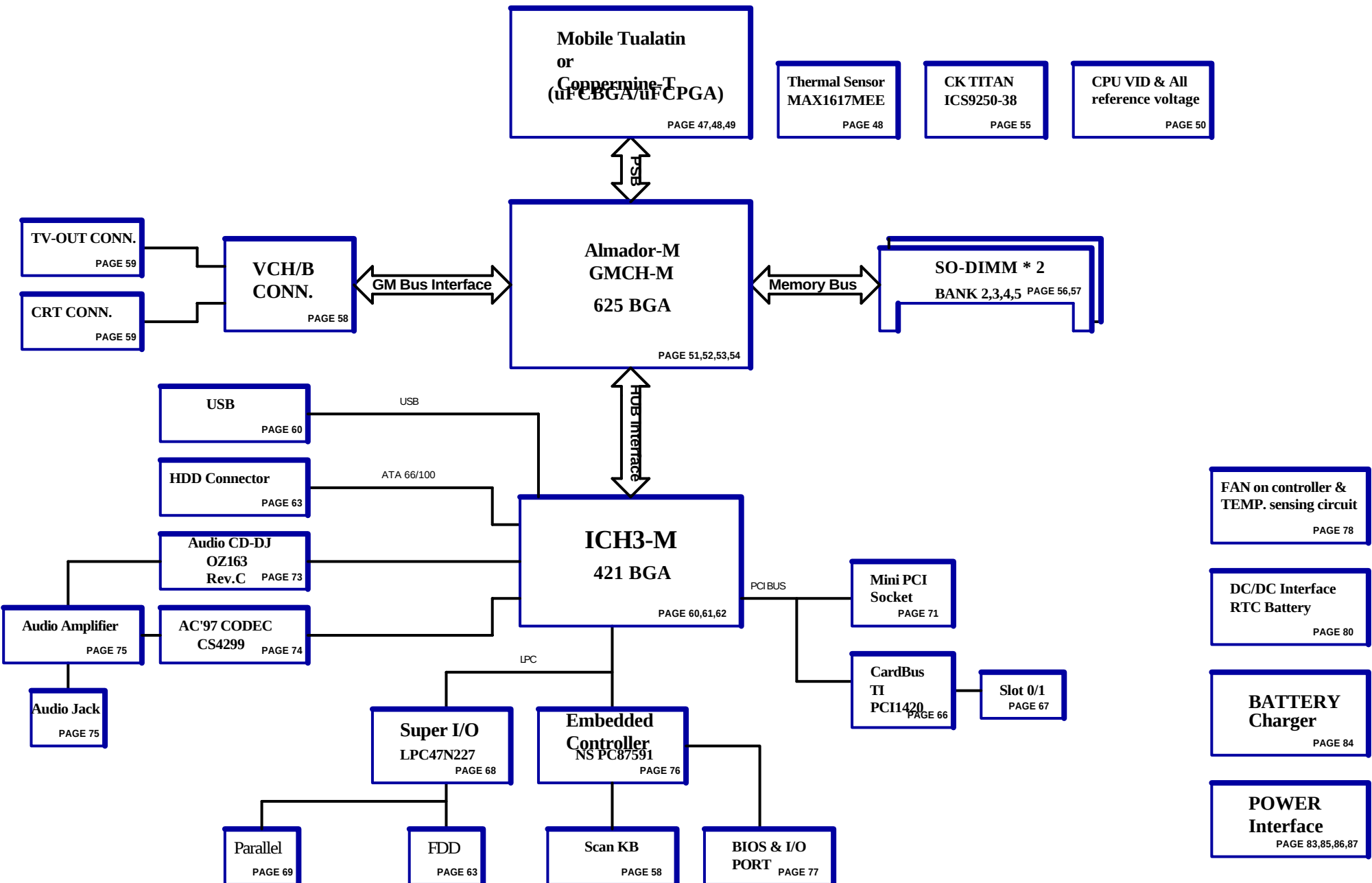
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ATW03 BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VCH CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM (RESERVE)	AD22		PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ163	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

EC SM Bus2 address

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

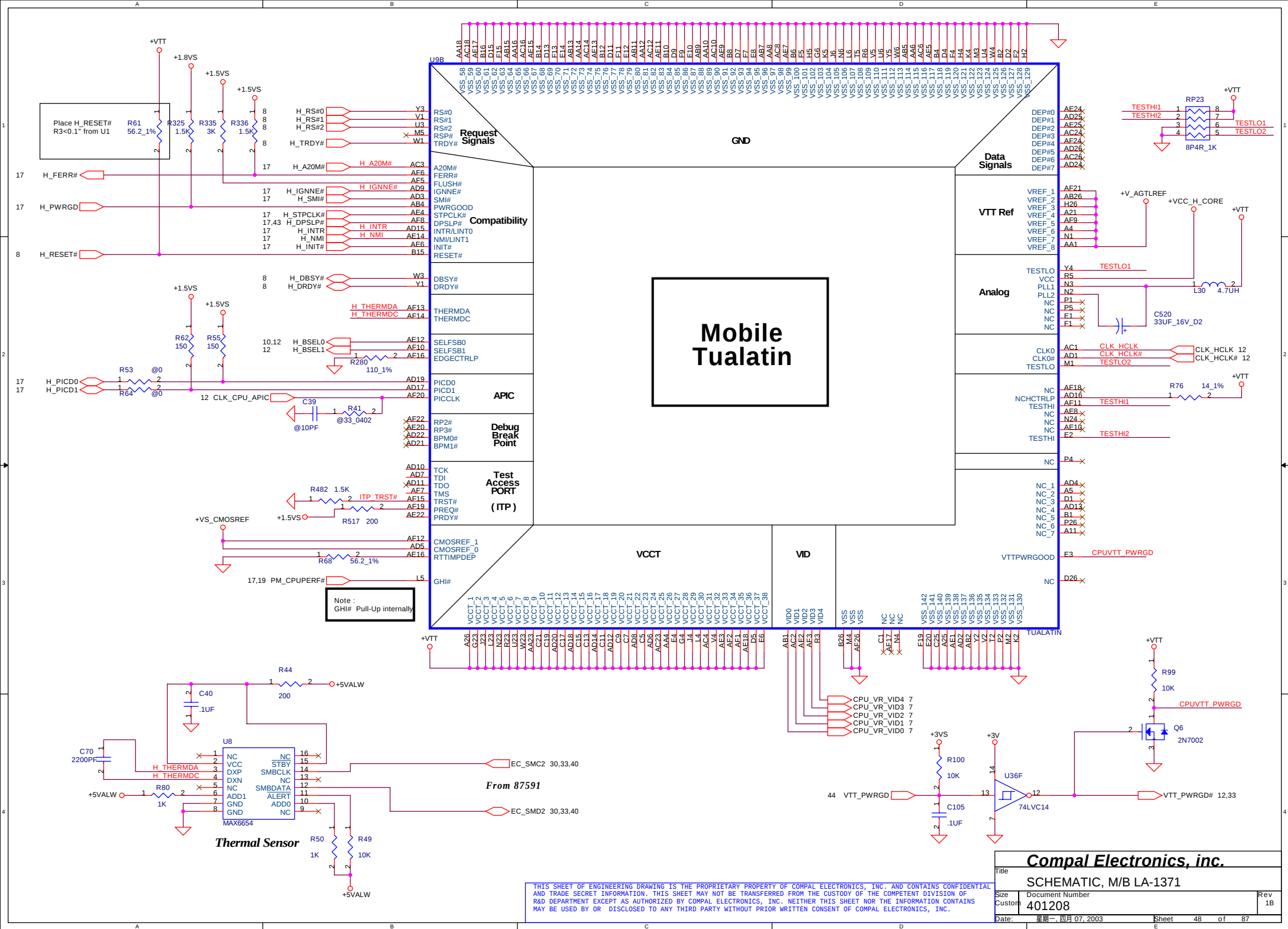
PIR

REV 0.1

Date	Page	Description
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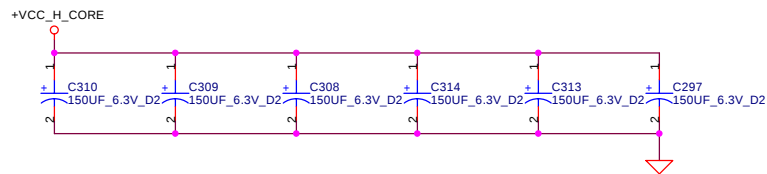
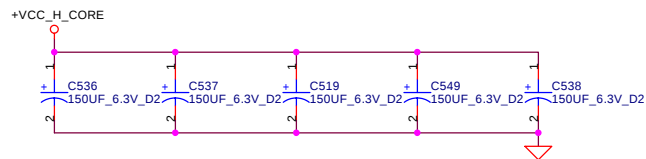
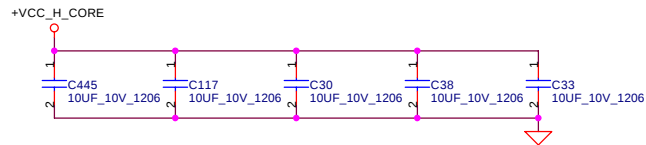
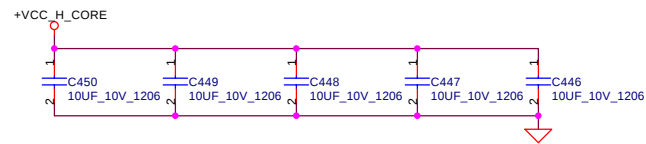
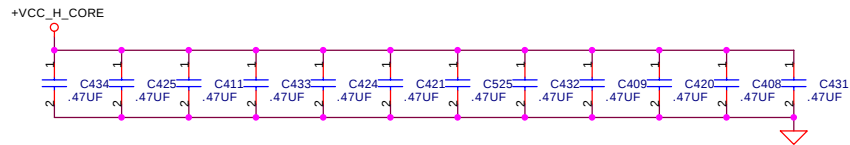
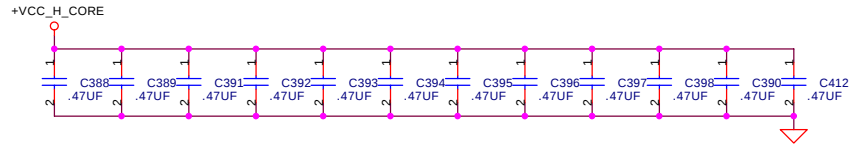
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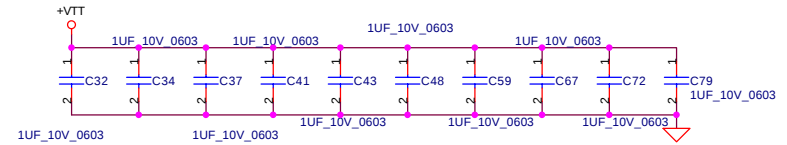
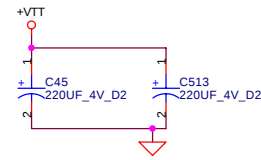
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.



Layout note :

Place close to CPU,
Use 2 vias per PAD.



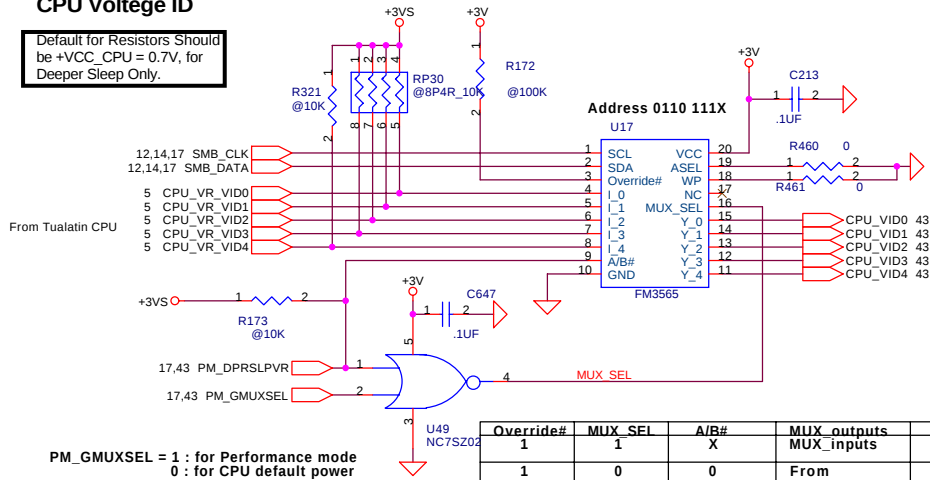
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CPU Voltage ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1 : for Deeper Sleep mode
0 : for Performance mode

Override#	MUX_SEL	A/B#	MUX_outputs MUX_inputs	Mode Battery
1	1	X	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

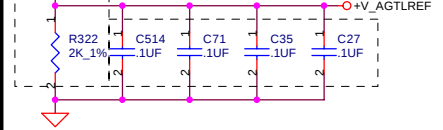
D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

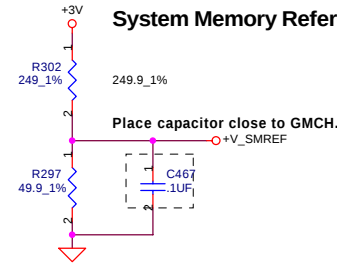
GTL Reference Voltage

Layout note :

1. Place R303 and R322 between and GMCH and CPU
2. Place decoupling caps near CPU.(Within 500mils)



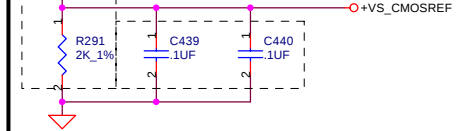
System Memory Reference



CMOS Reference Voltage

Layout note :

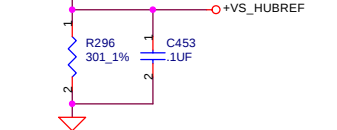
1. Place R288 and R291 between and GMCH and CPU
2. Place decoupling caps near CPU.



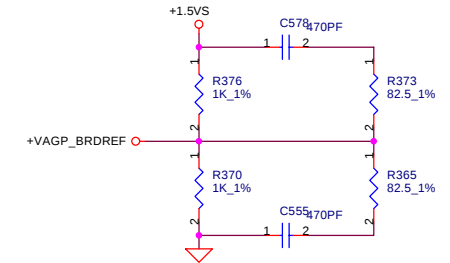
HUB Interface Reference

Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

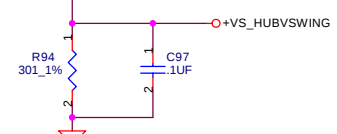


Place Reference Circuit near GMCH

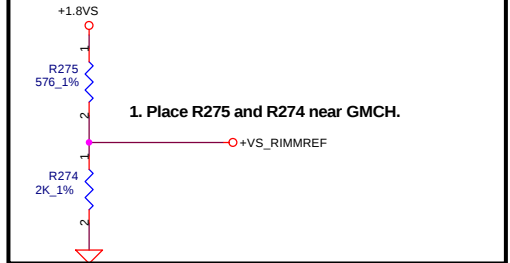


HUB Interface VSwing Voltage

1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.

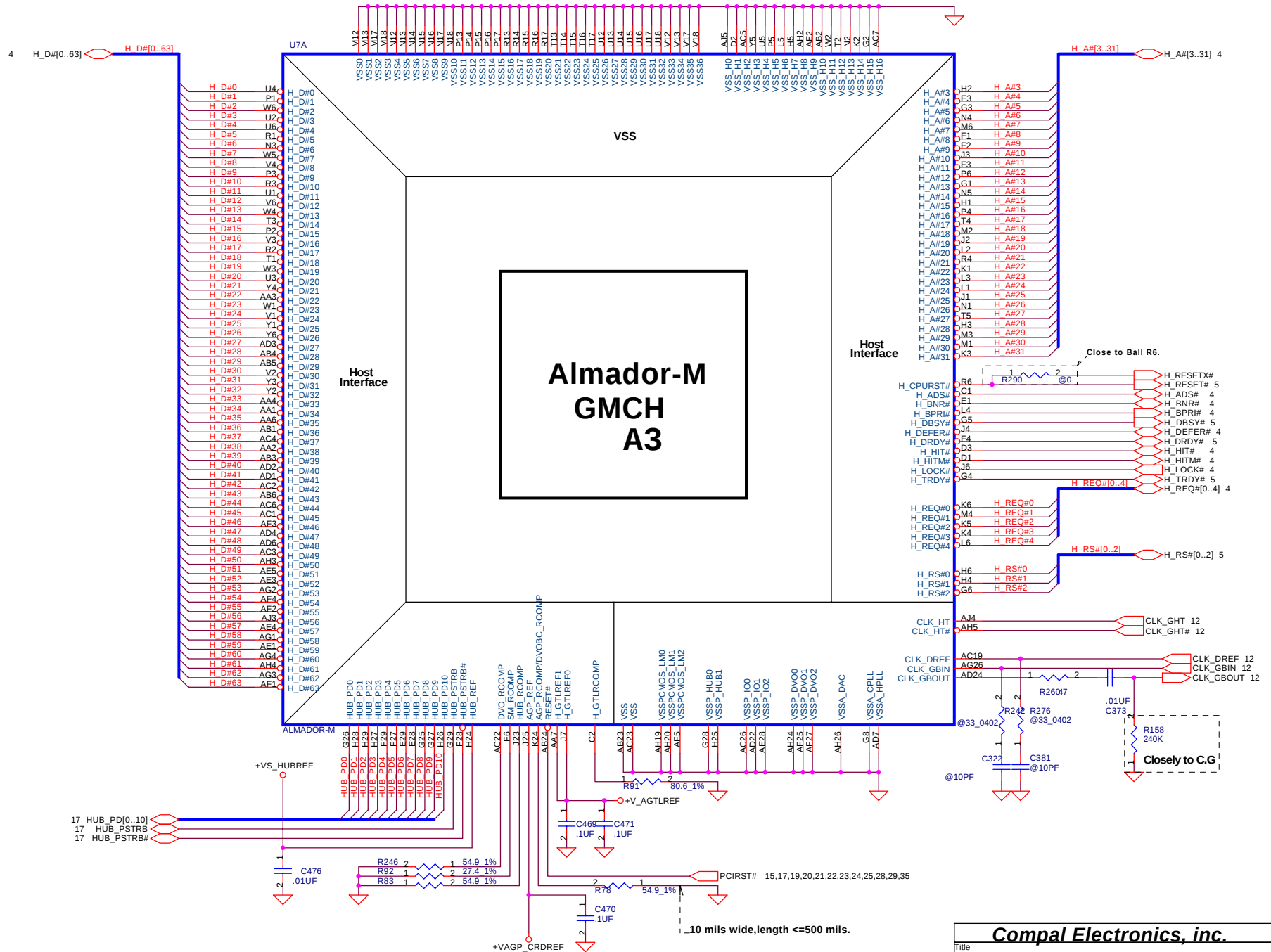


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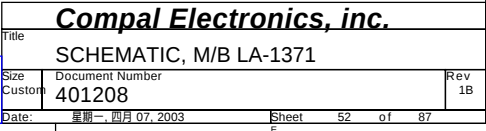


Compal Electronics, inc.

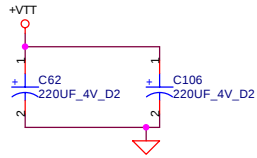
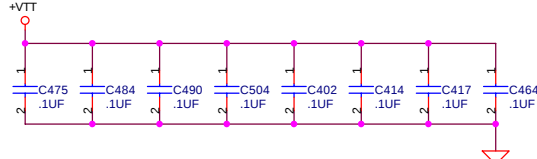
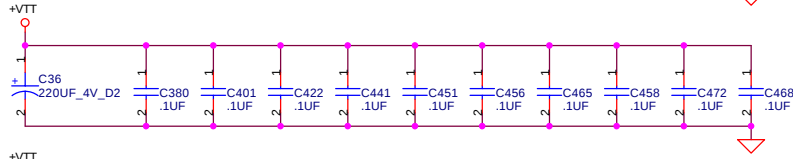
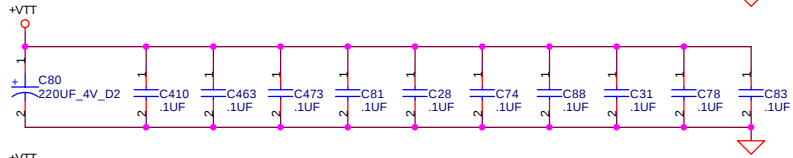
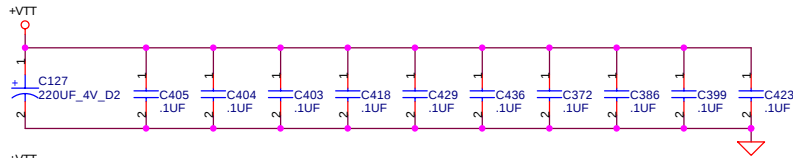
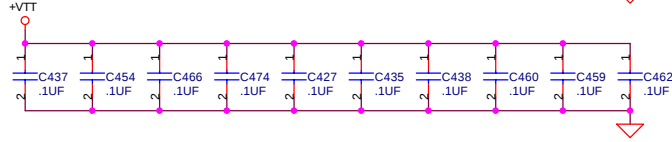
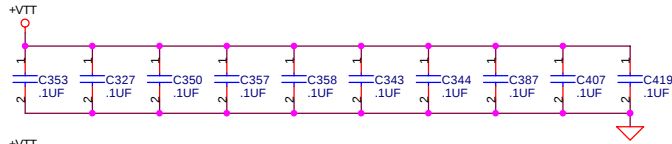
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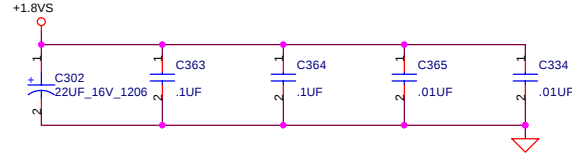
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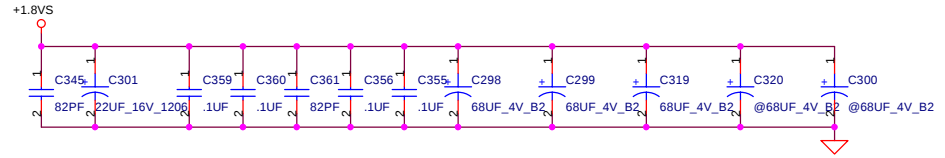
Layout note :
Distribute as close as possible
to GMCH Processor Quadrant .



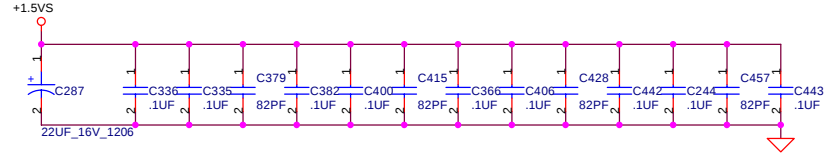
Layout note :
Distribute as close as possible
to VCCPCMOS_LM .



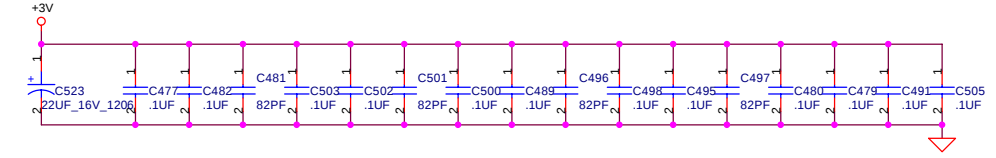
Layout note :
Distribute as close as possible
to GMCH Local Memory Quadrant .



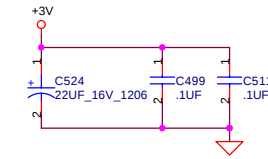
Layout note :
Distribute as close as possible
to GMCH AGP/DVO Quadrant .



Layout note :
Distribute as close as possible
to GMCH System Memory Quadrant .

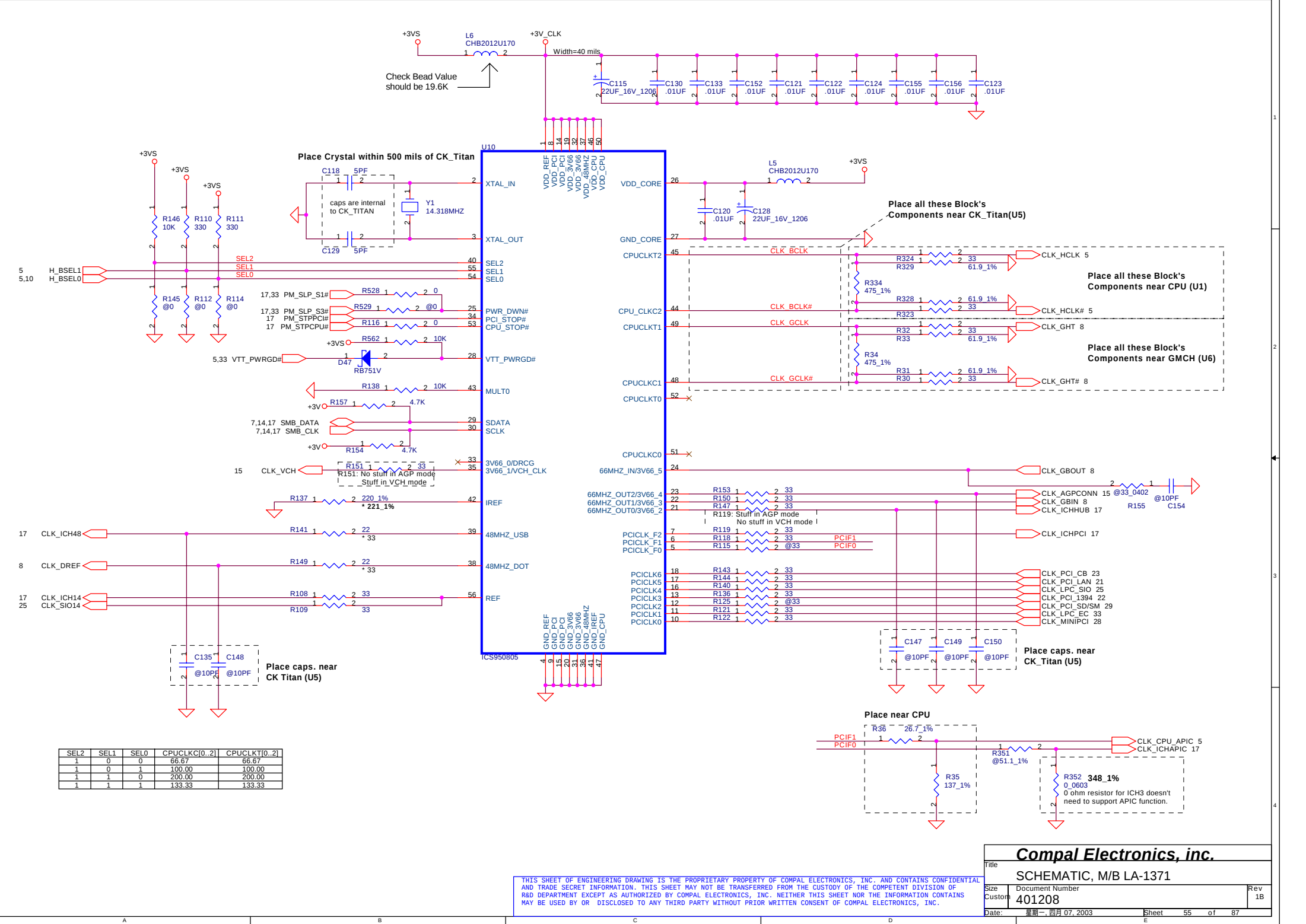


Layout note :
Distribute as close as possible
to IO Quadrant .



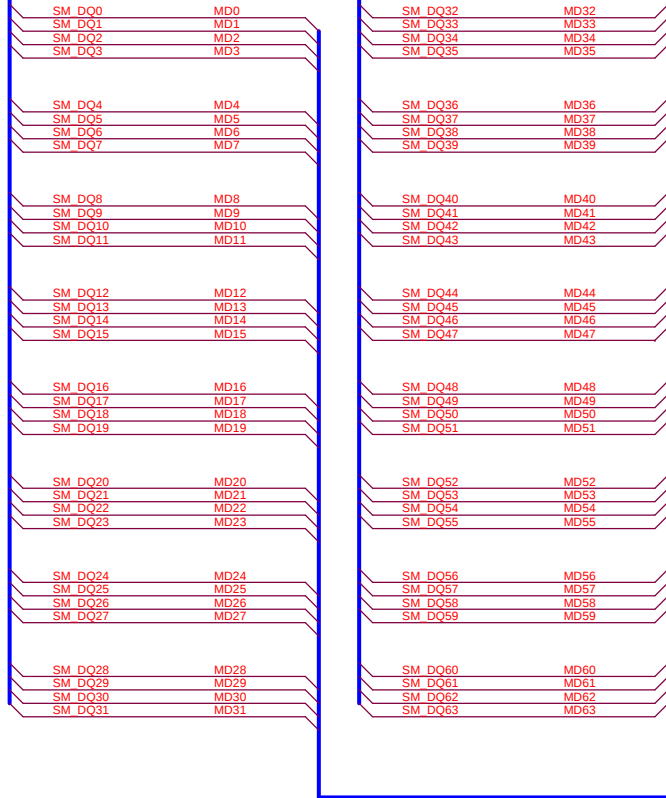
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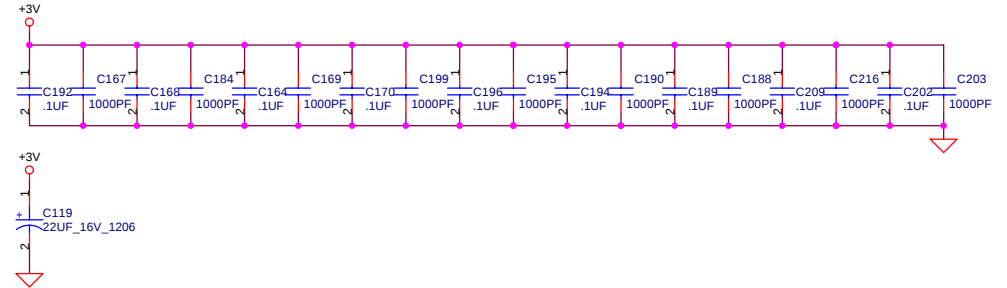


SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

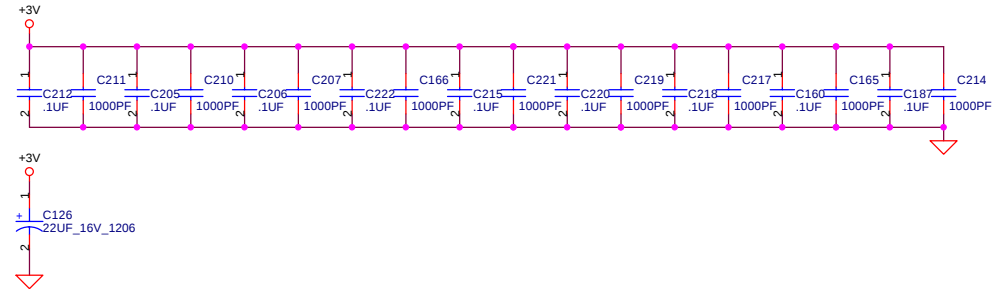
9,14 SM_DQ[0..63] MD[0..63] 9,14



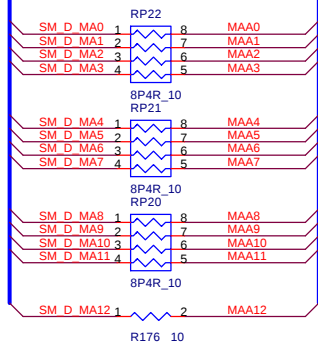
Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .



9 SM_D_MAA[0..12] MAA[0..12] 14

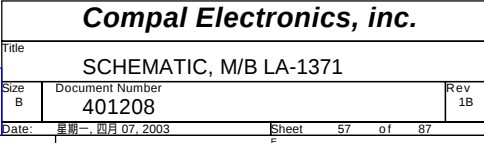


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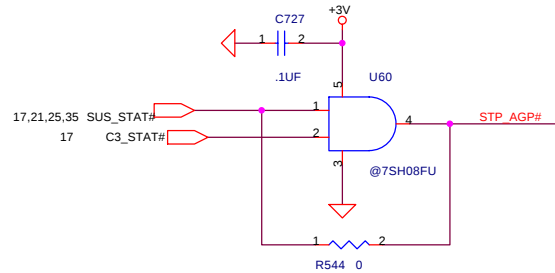
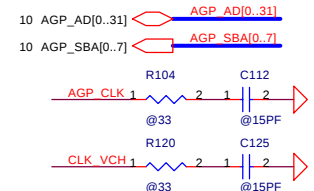
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BANK 0/1

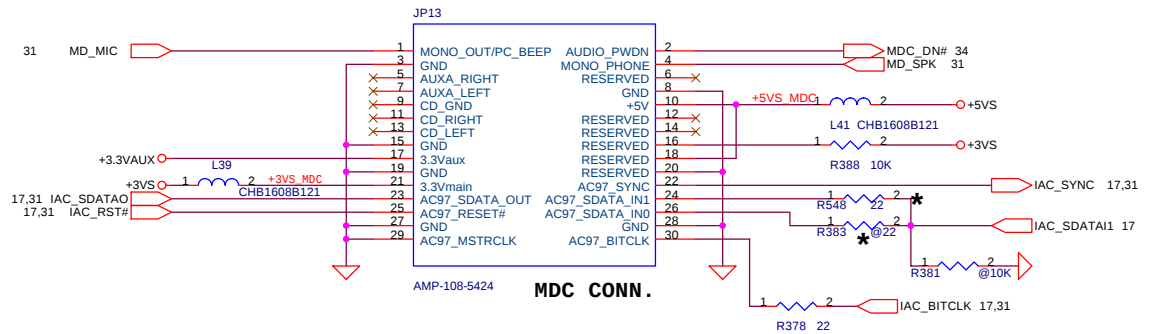
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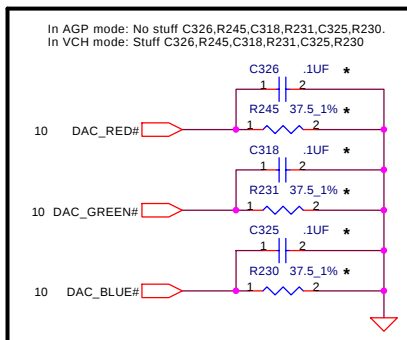
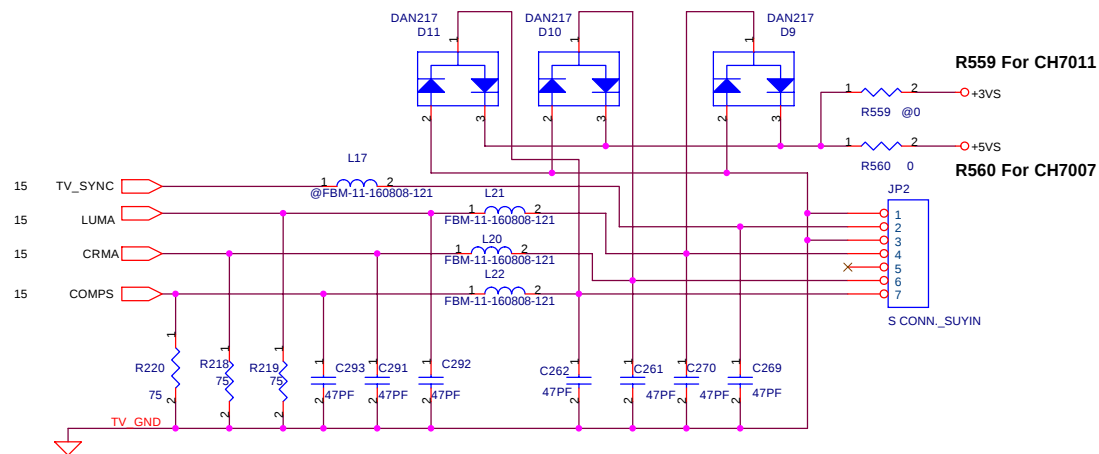
JP8



JP11

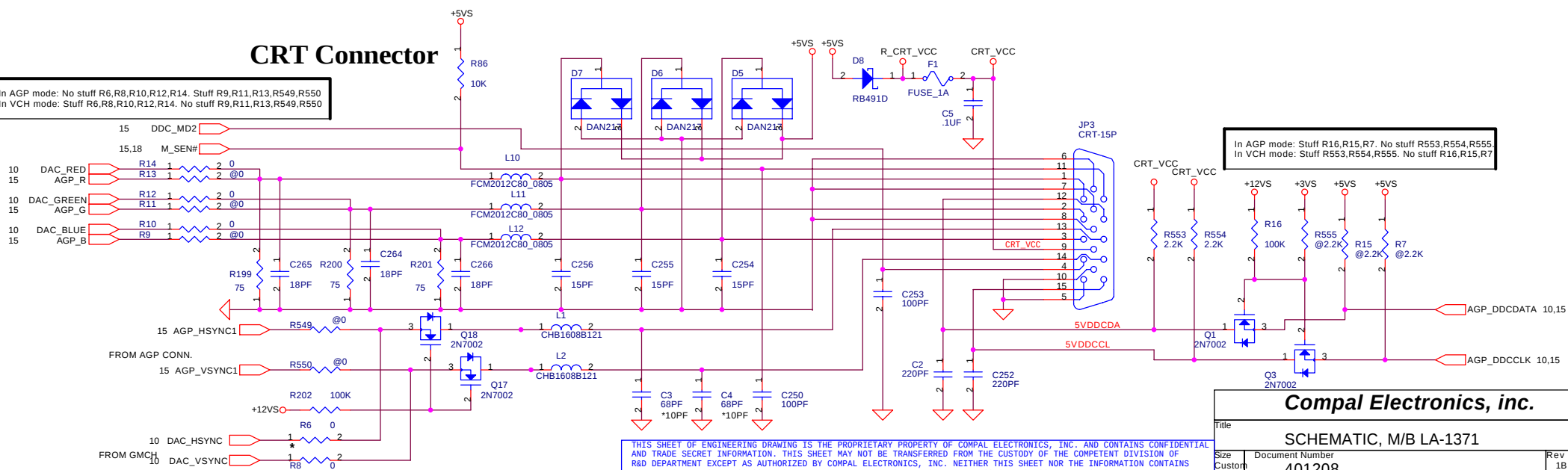


TV_OUT CONN.



CRT Connector

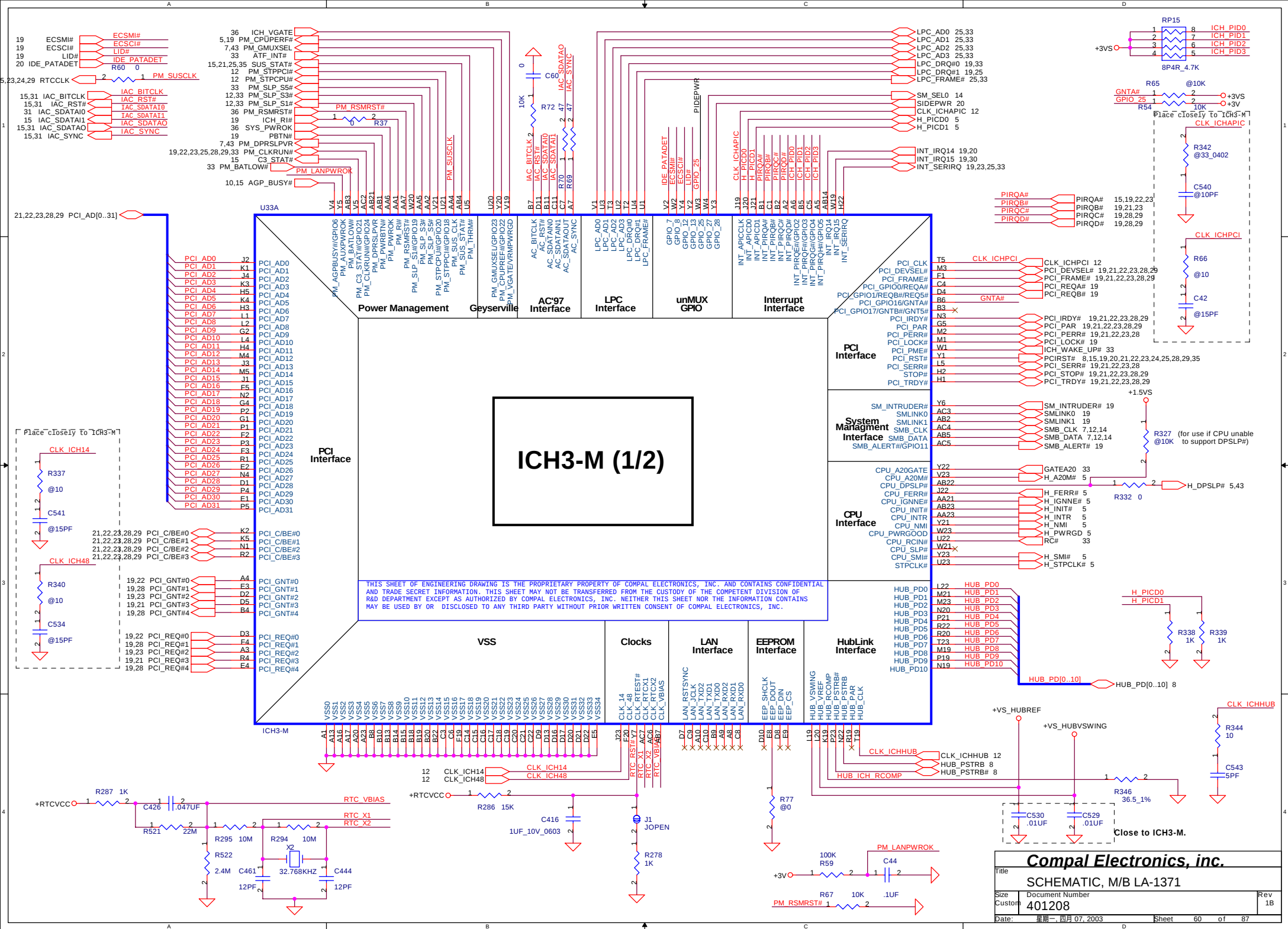
In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550

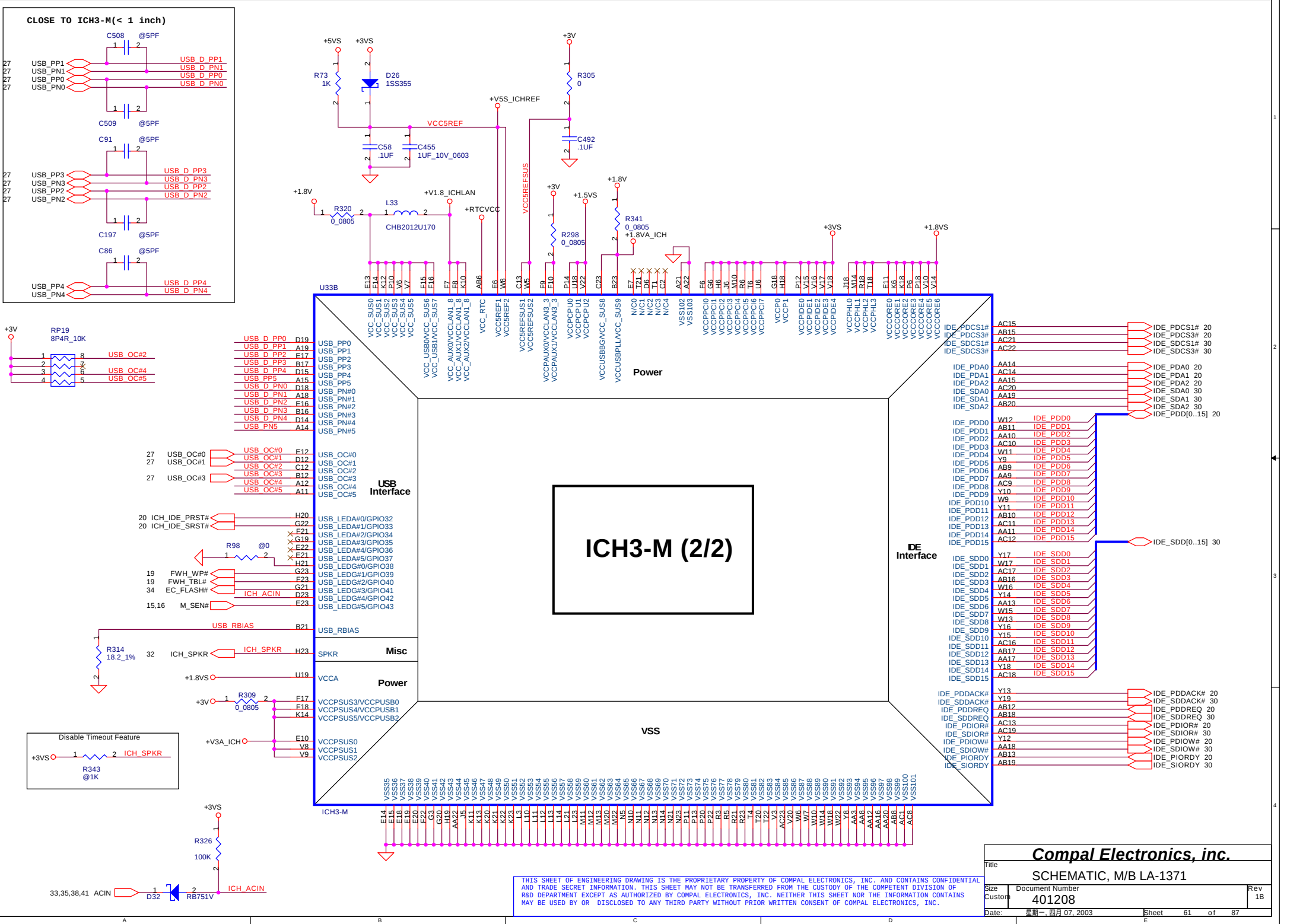


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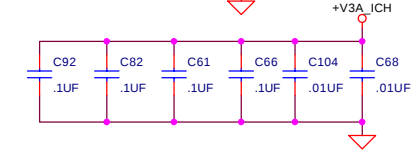
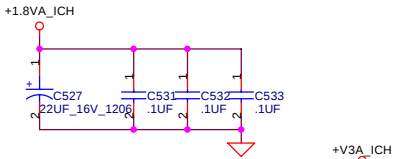
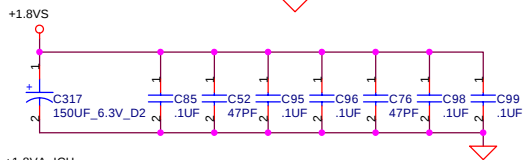
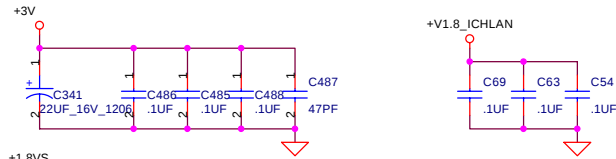
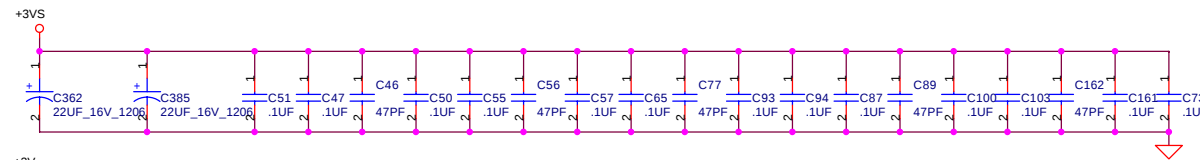
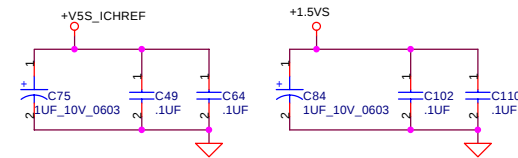
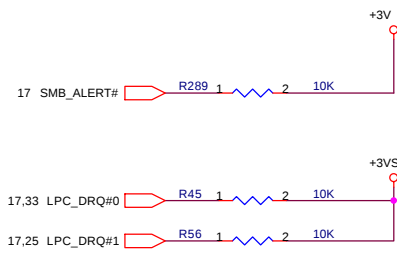
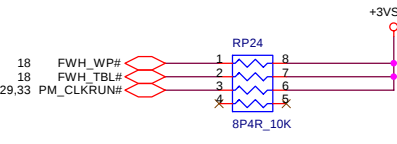
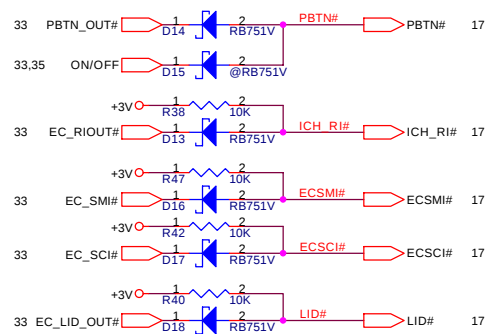
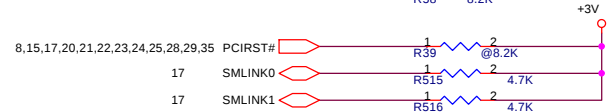
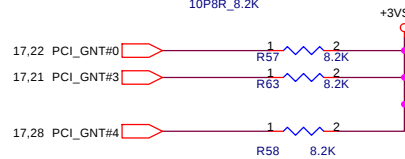
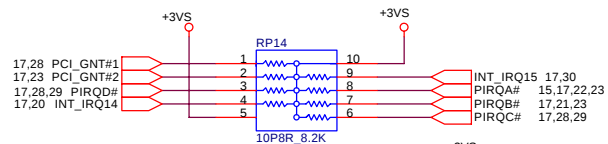
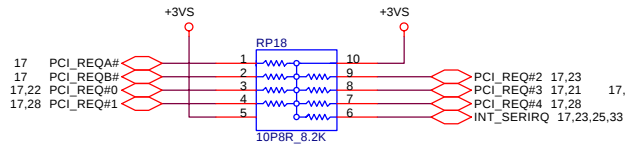
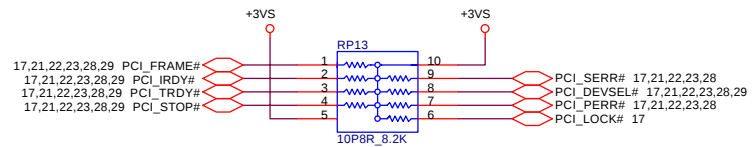
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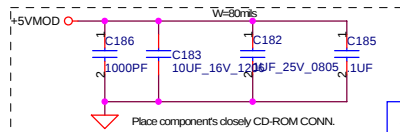
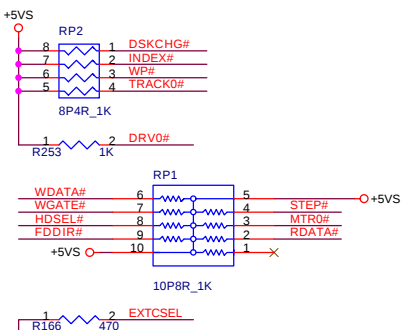
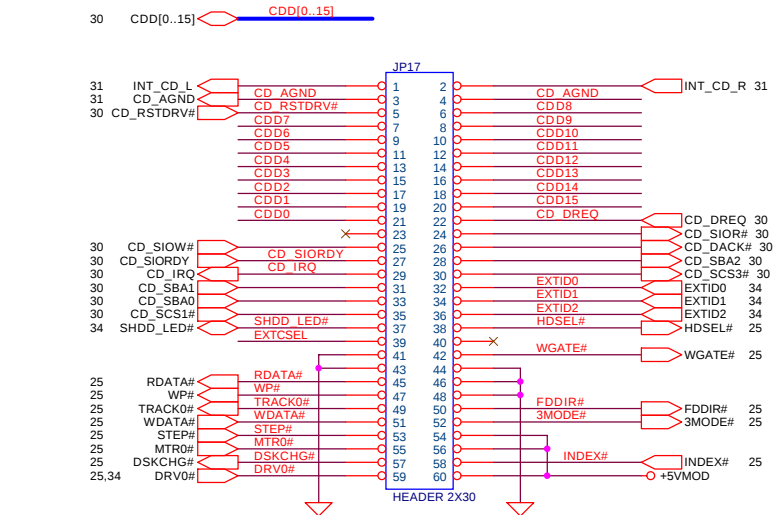
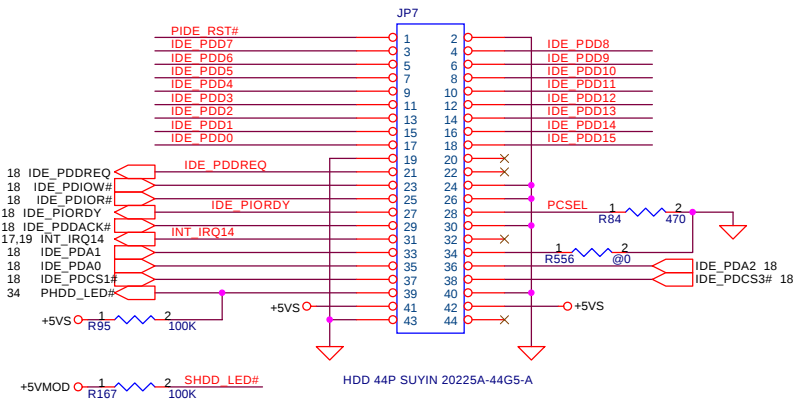
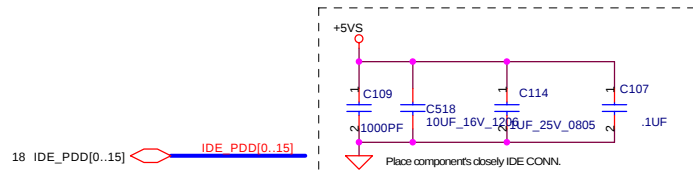
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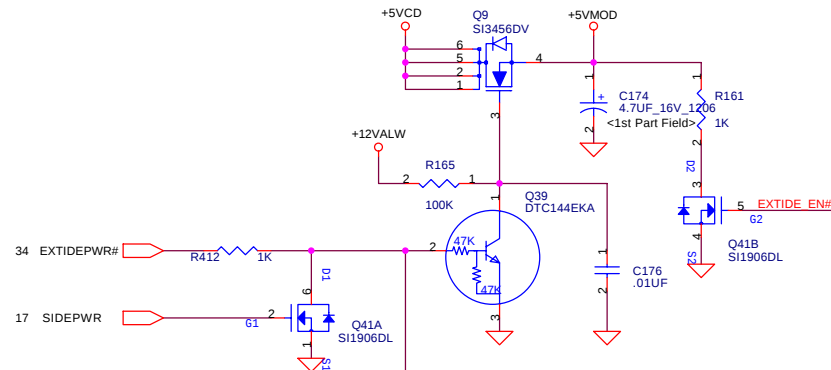
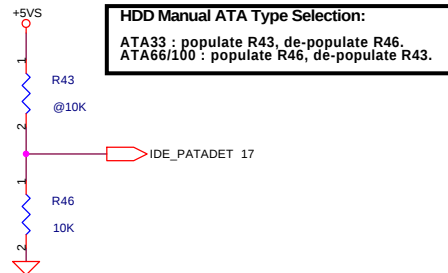
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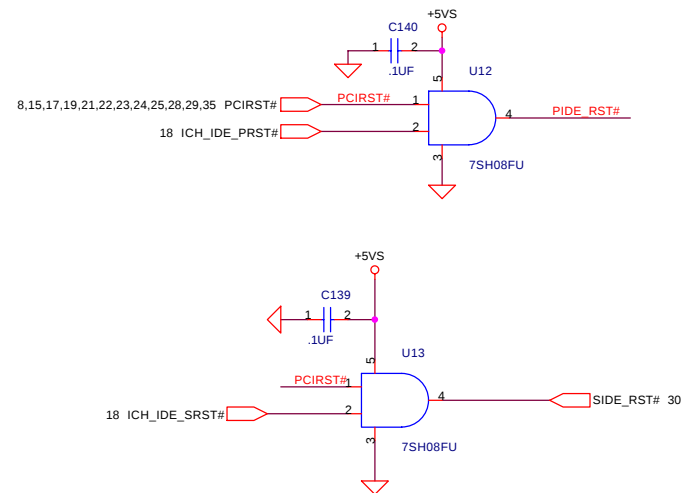
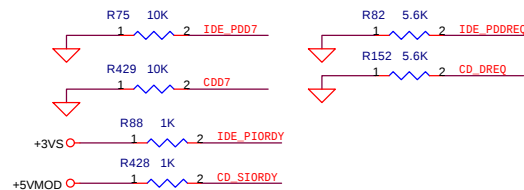
IDE,CD-ROM Module CONN.



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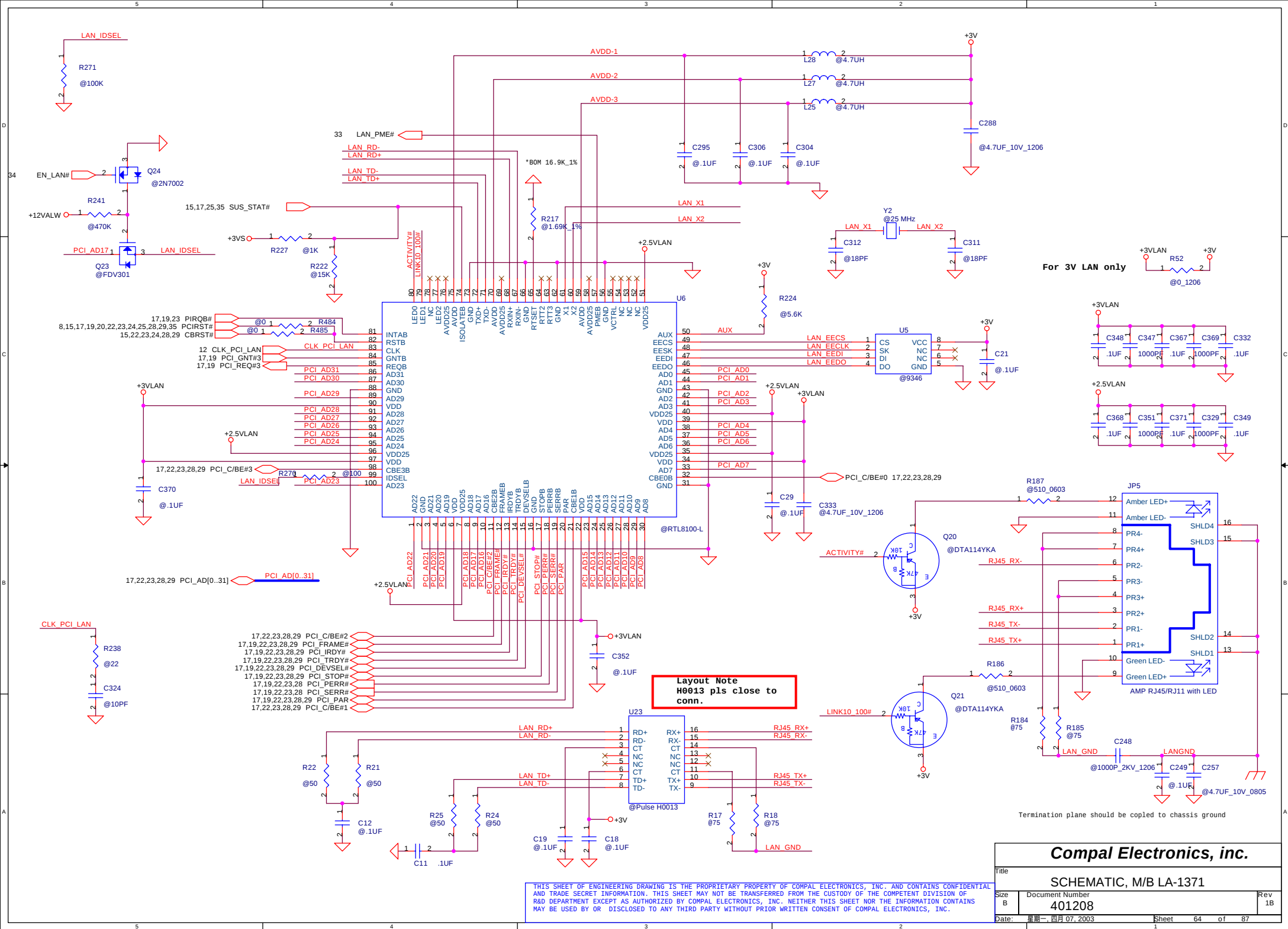
SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+-20V



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TSB43AB22

PCI BUS INTERFACE

PHY PORT 2

BIAS CURRENT

OSCILLATOR

FILTER

EEPROM 2 WIRE BUS

POWER CLASS

PHY PORT 1

For TSB43AA22
C657, C605
change to 0
ohm to short
to GND

TSB43AB22 USE

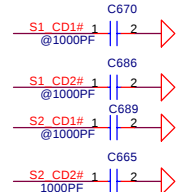
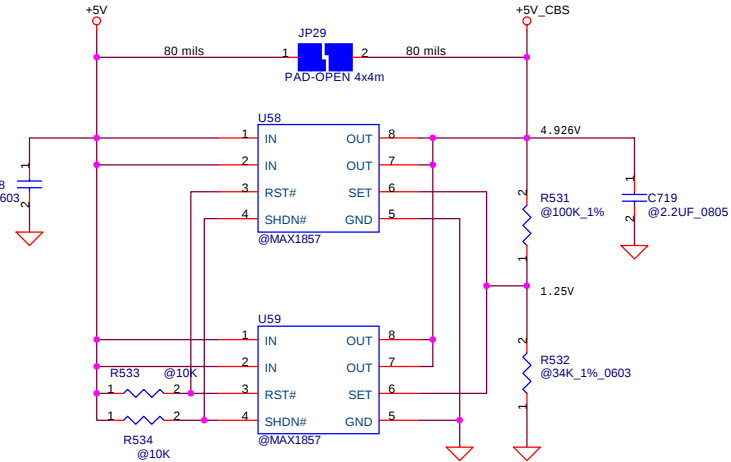
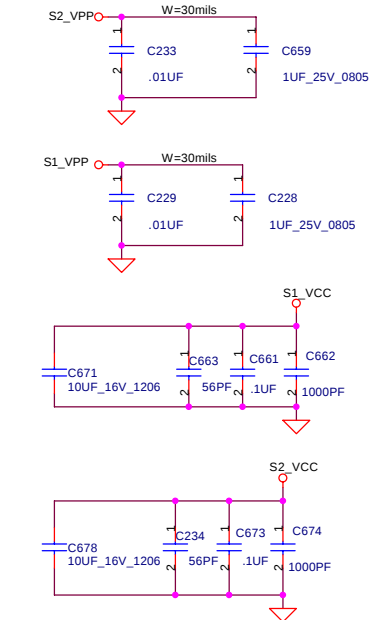
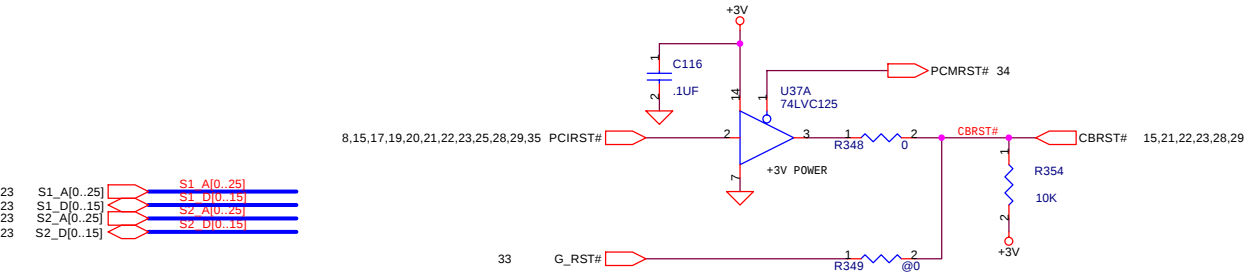
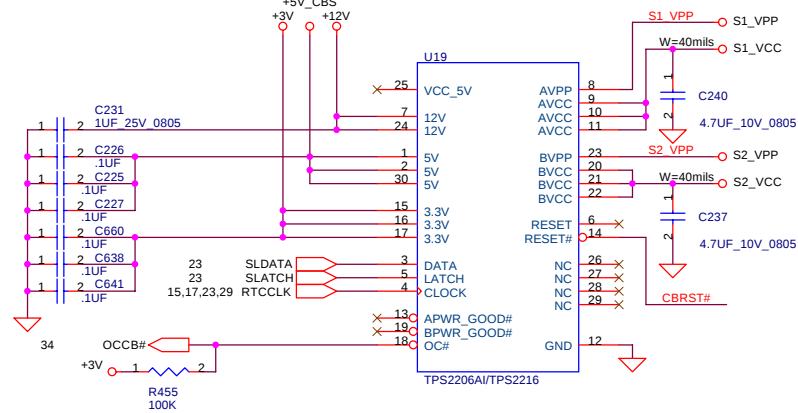
Compal Electronics, inc.

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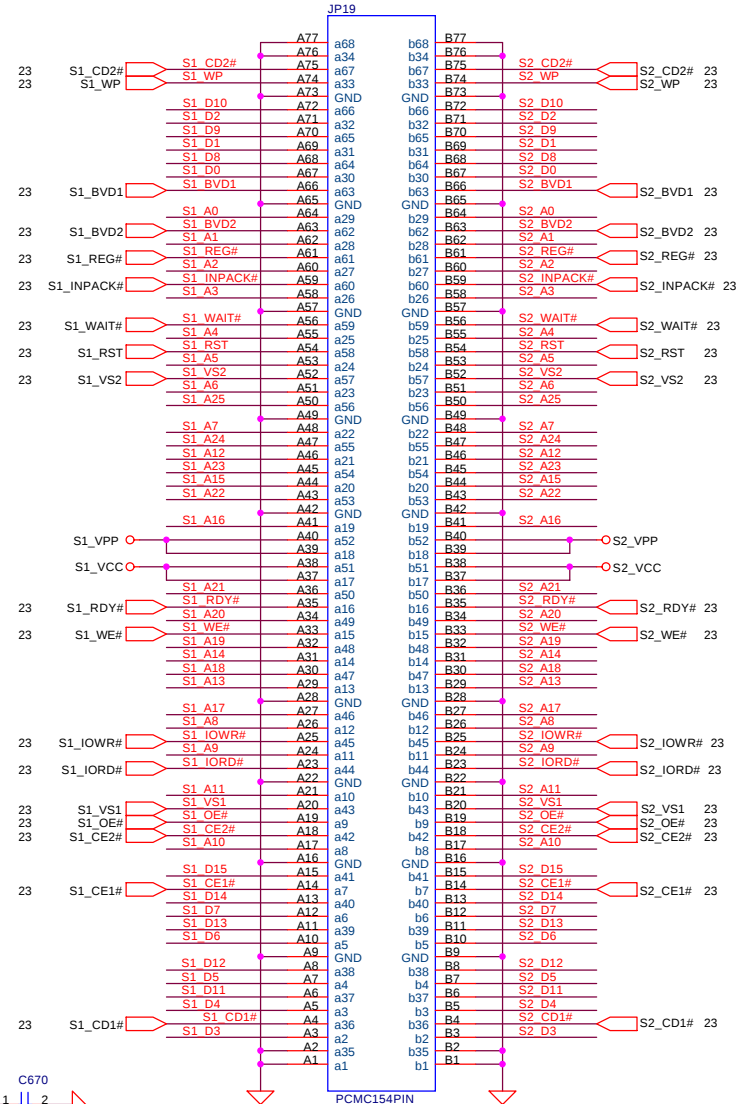
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PCMCIA POWER CTRL.



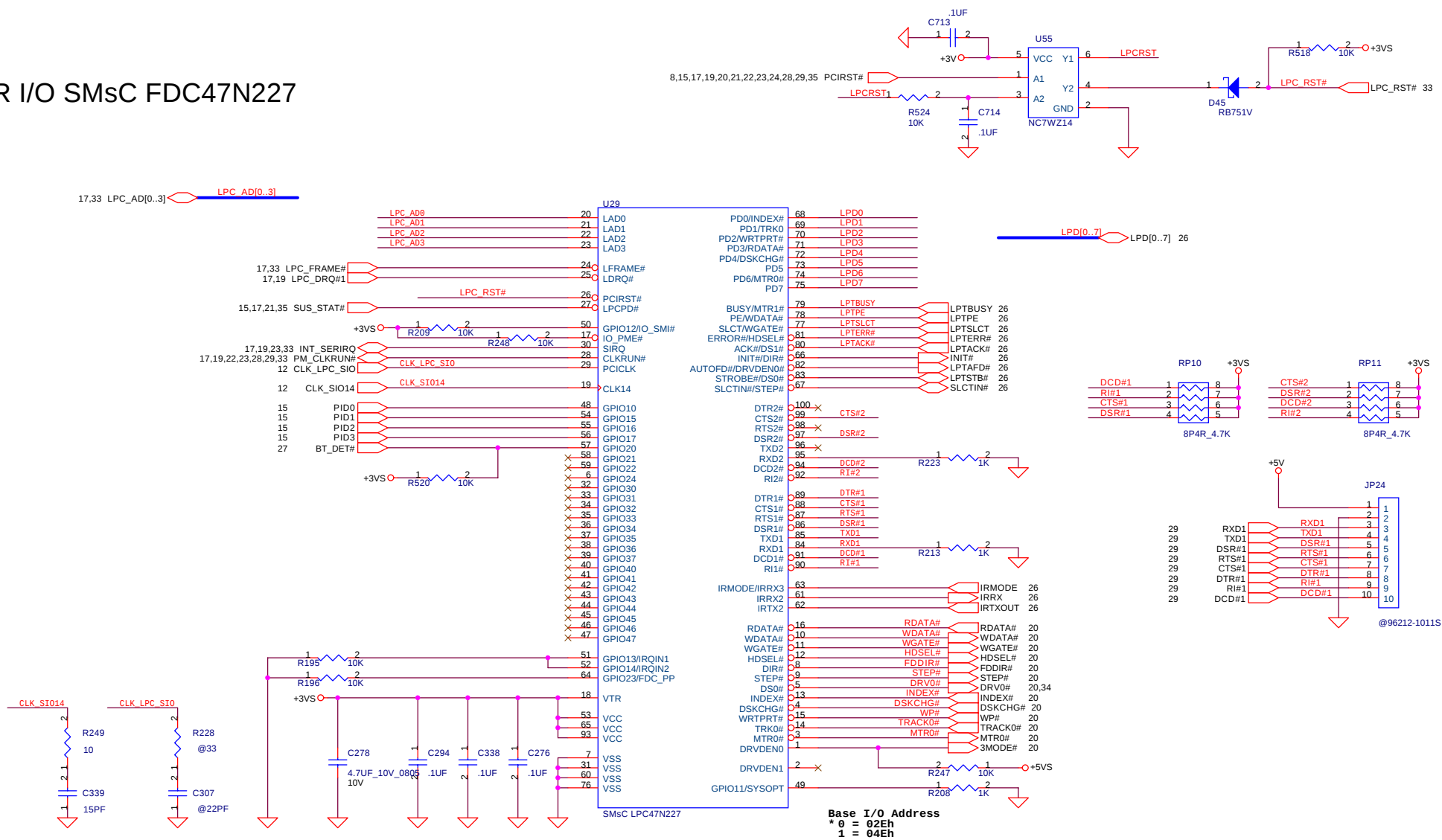
CARDBUS
SOCKET



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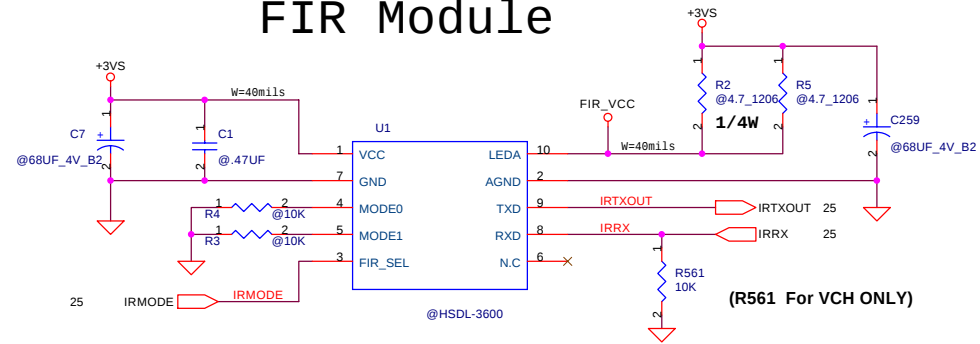
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SUPER I/O SMsC FDC47N227



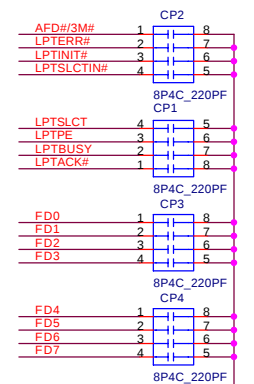
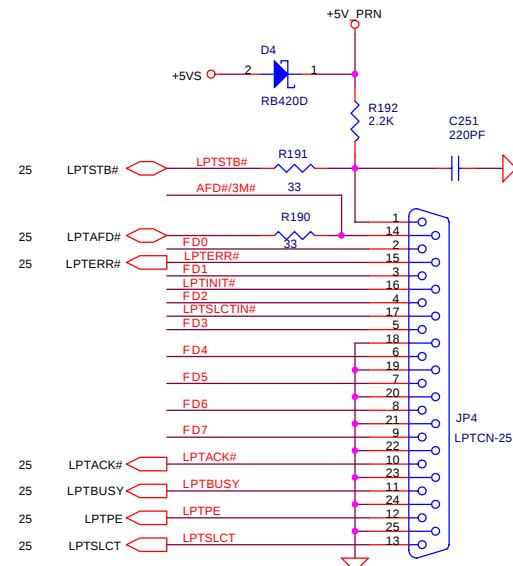
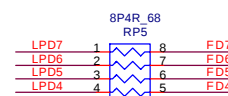
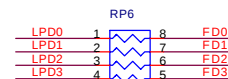
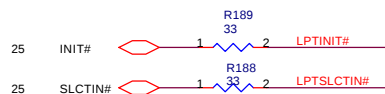
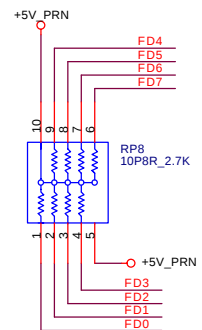
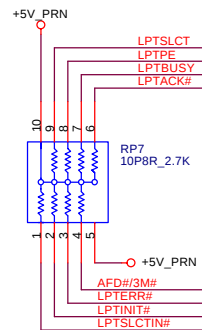
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FIR Module



The component's most place
cloely IRDA MODULE.

PARALLEL PORT



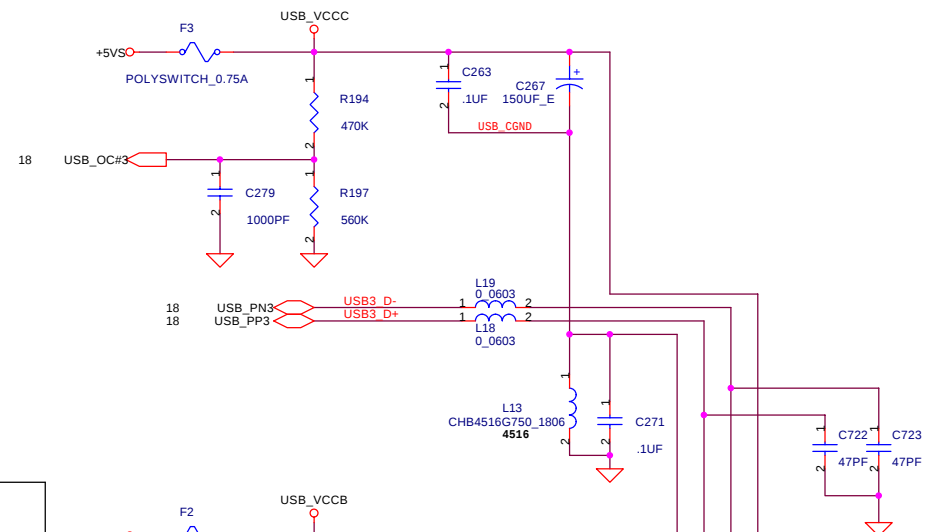
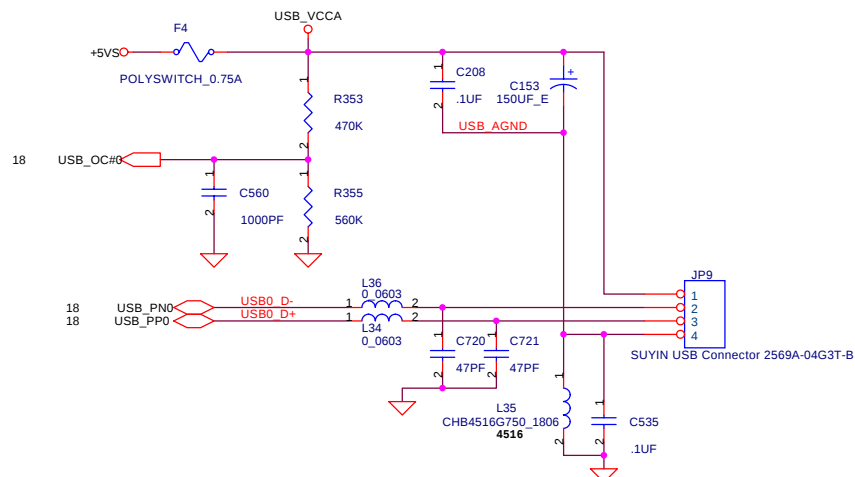
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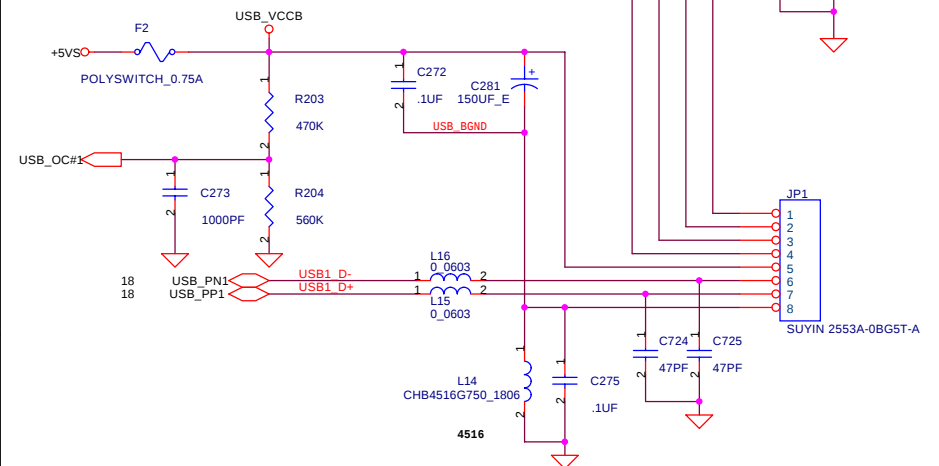
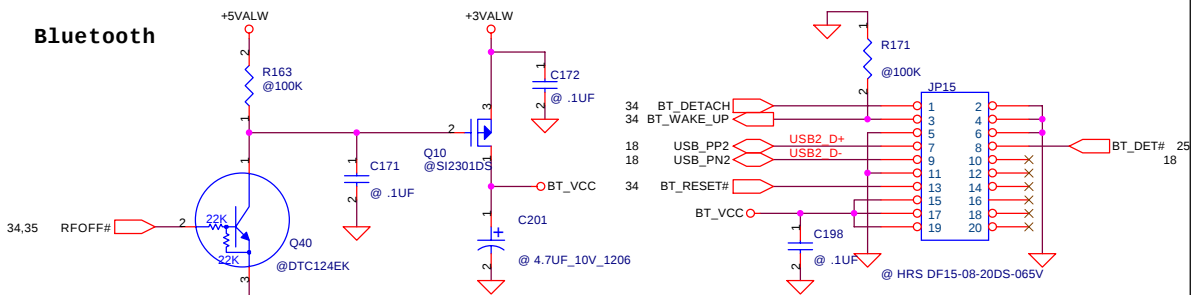
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USB PORT



Bluetooth

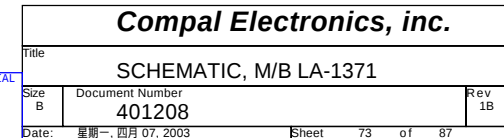


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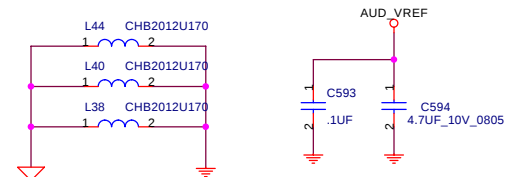
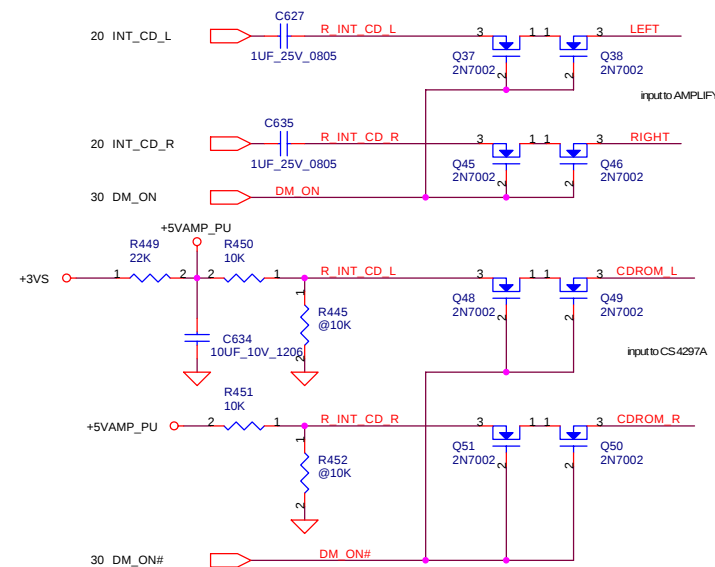
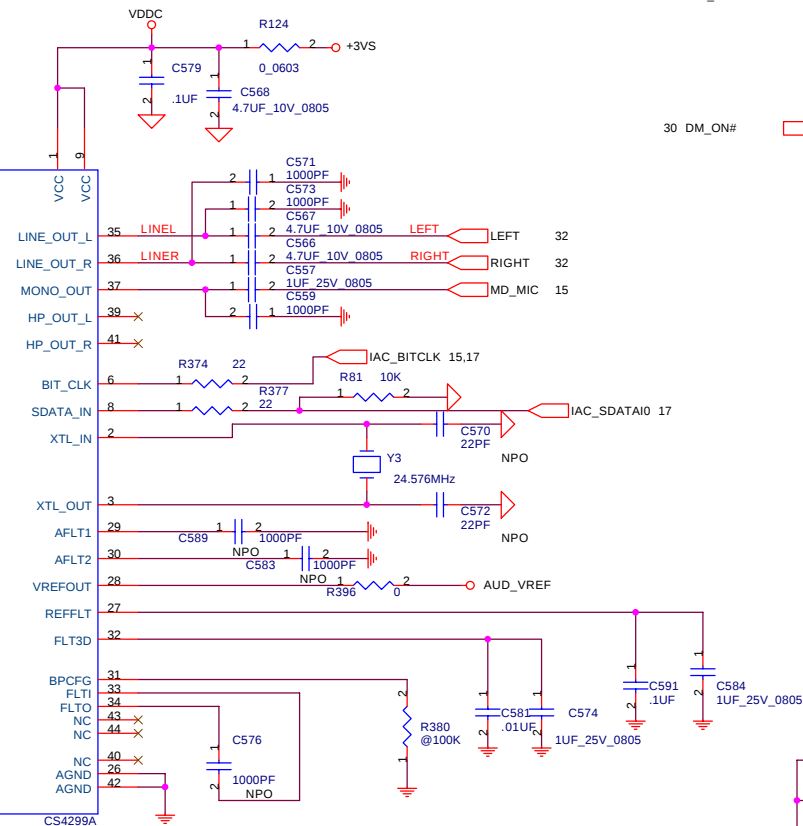
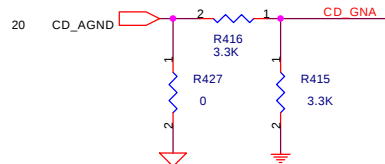
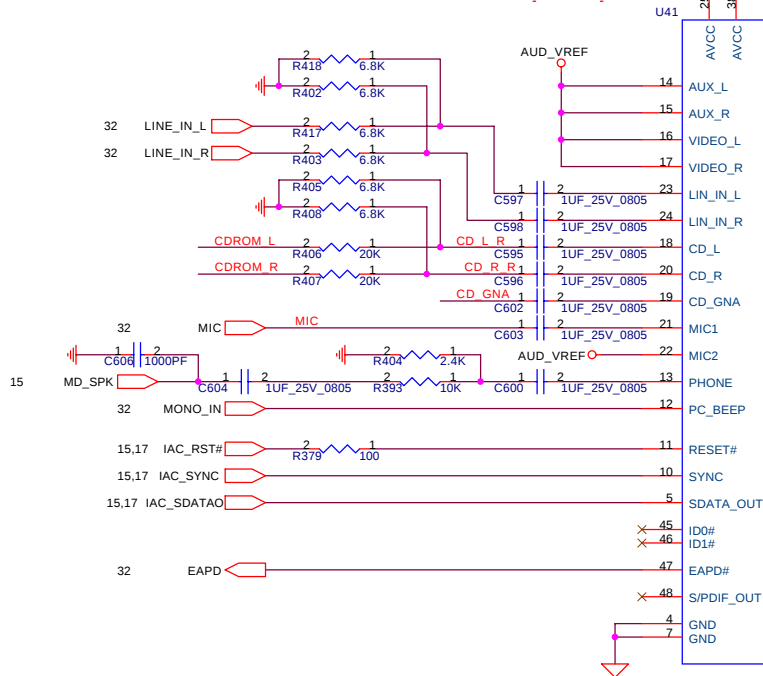
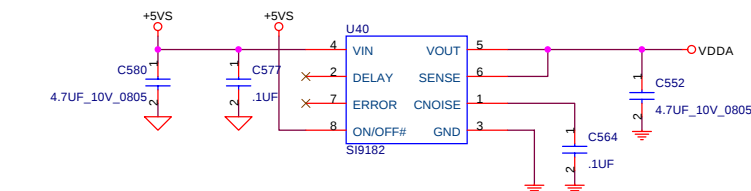
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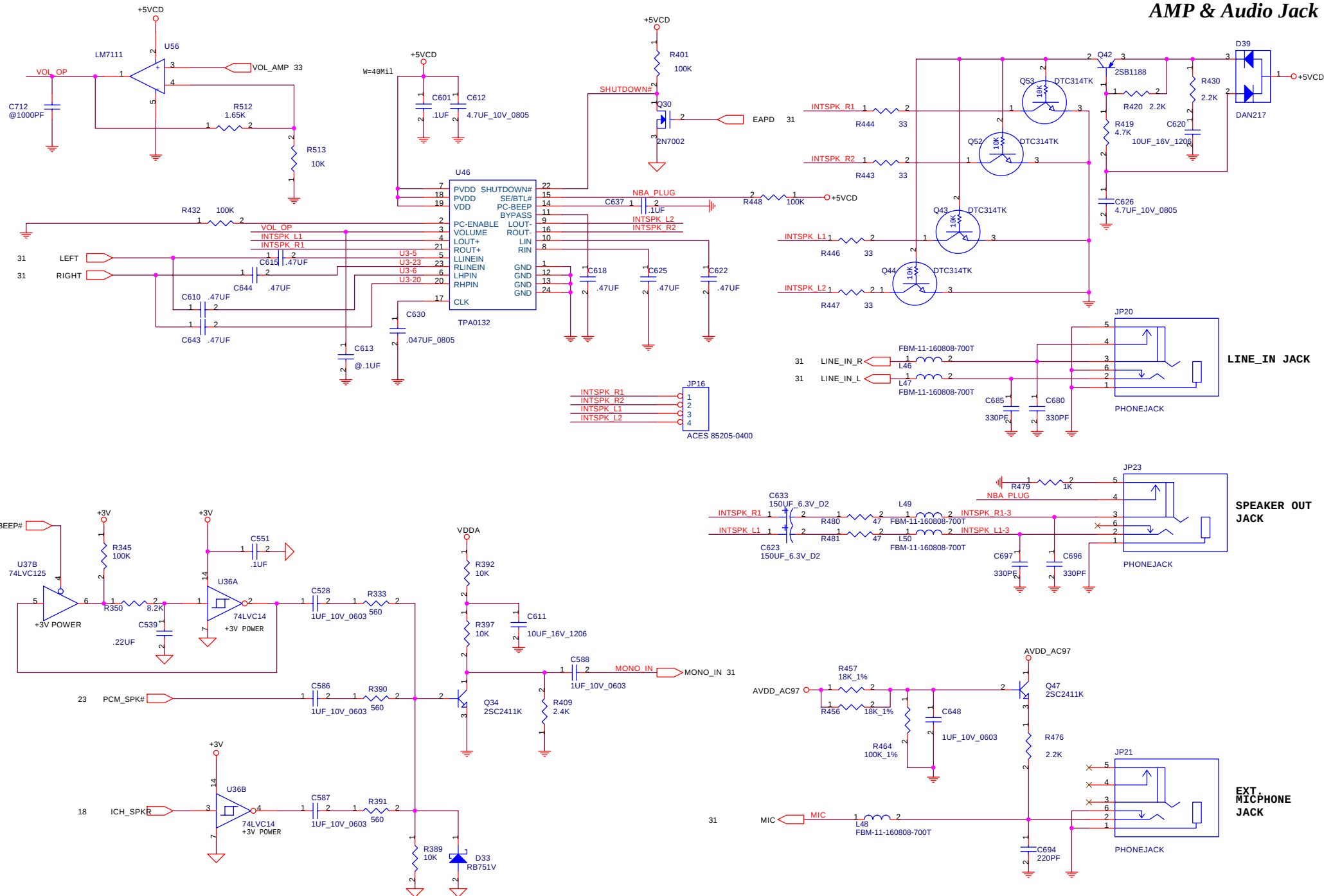
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AC97 Codec

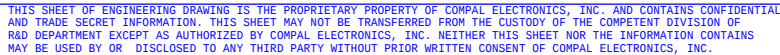


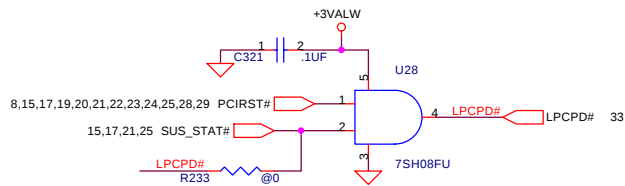
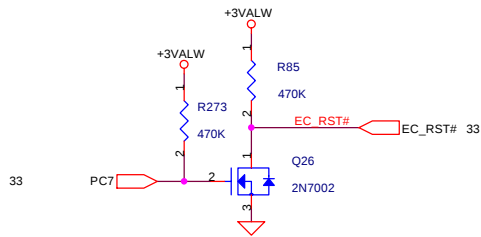
AMP & Audio Jack



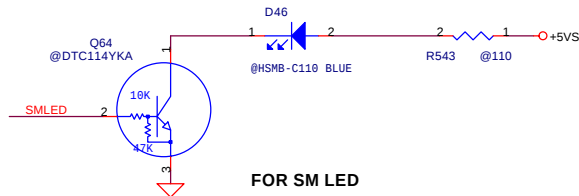
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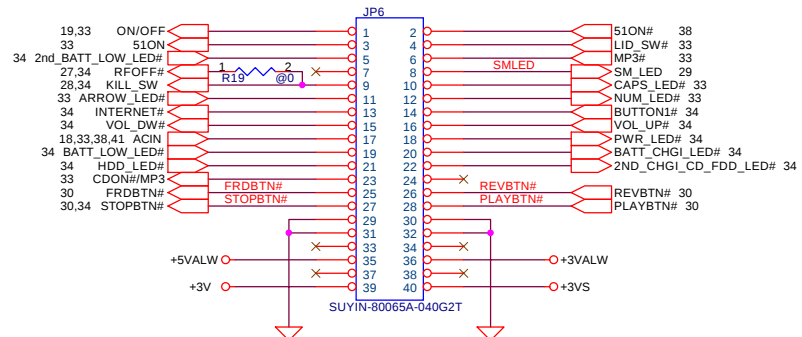
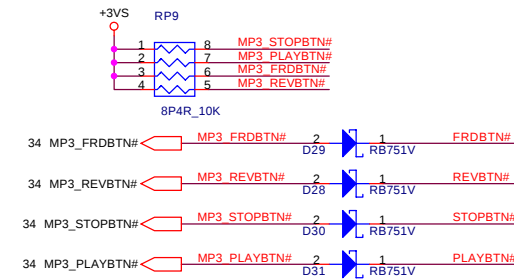




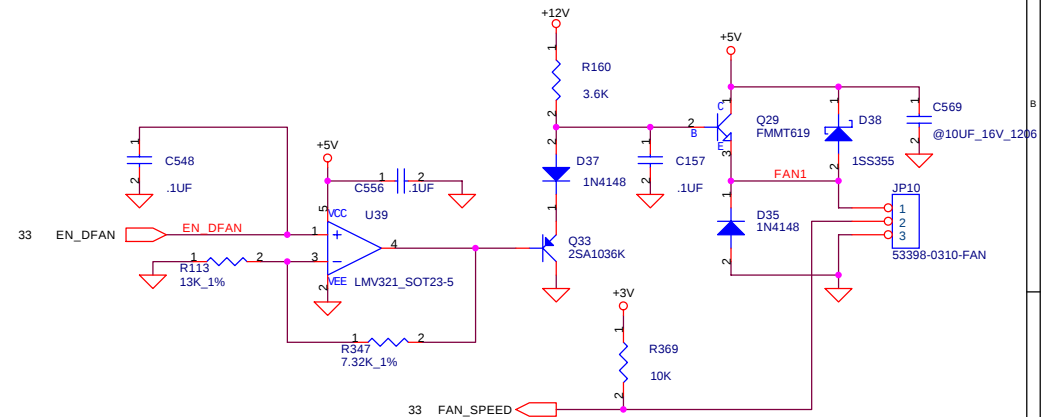
For PC87591 REV 0.A Only



FOR SM LED



FAN CONN.

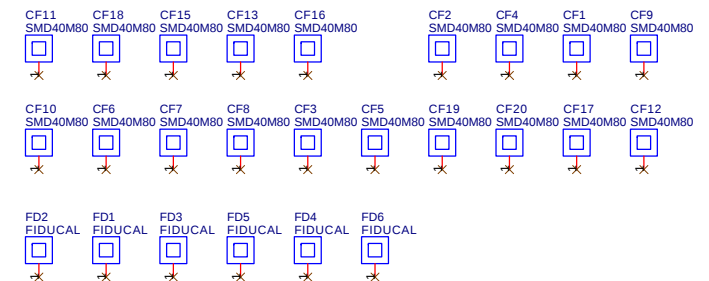
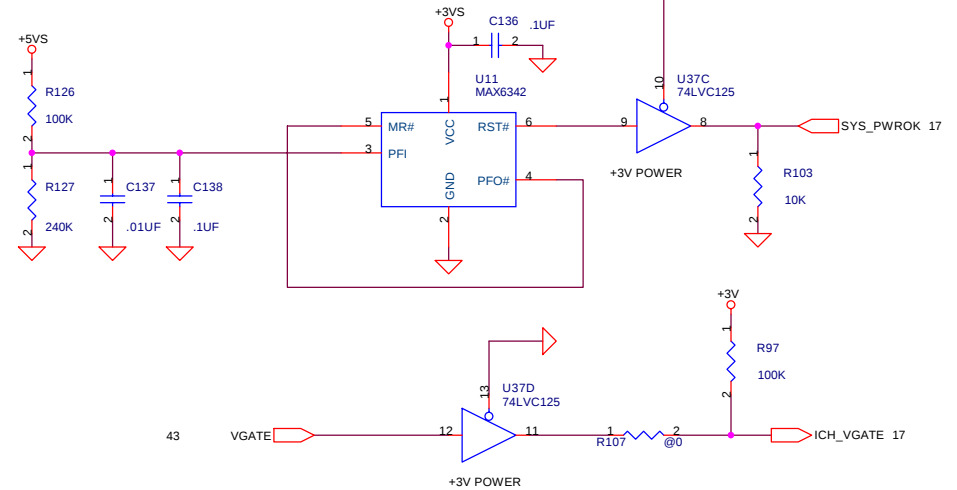
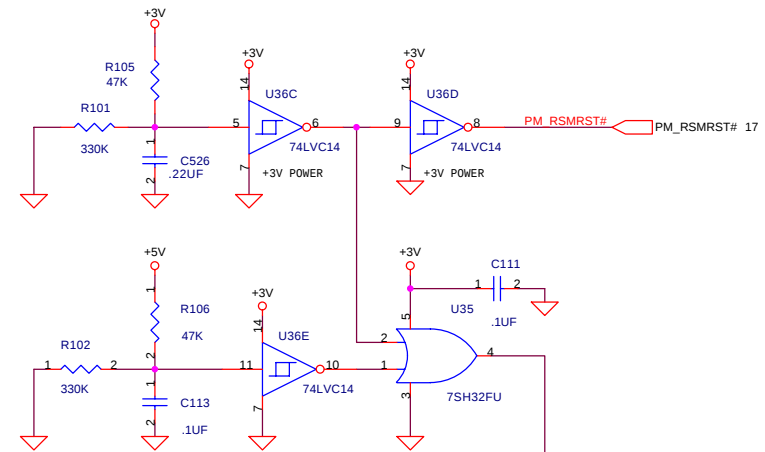


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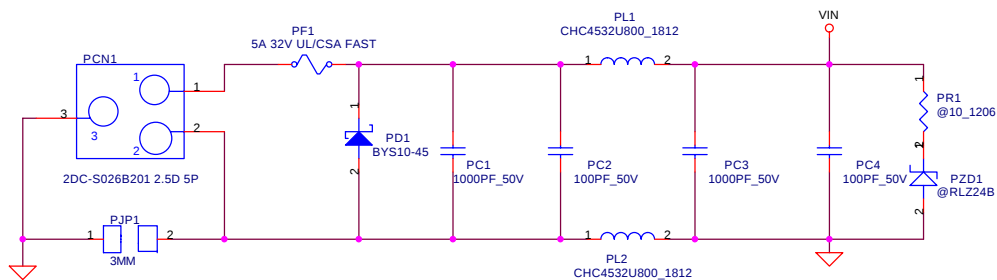
The schematic diagram illustrates the power supply for the Real Time Clock (RTC). It features a +RTCVCC input connected to a +RTC_BATT output through a BATT1 component. A capacitor C141 (1uF) is connected between +RTC_BATT and ground. Two diodes, D3 and D1 (RB751V), are connected in series between the +RTC_BATT line and the CHGRTC output. A capacitor C131 (1uF) is connected between the CHGRTC output and ground. A note indicates to place C131 near the ICH3-M component.



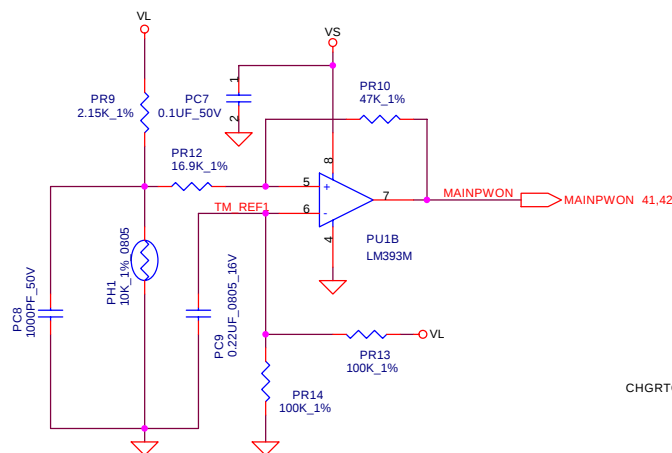
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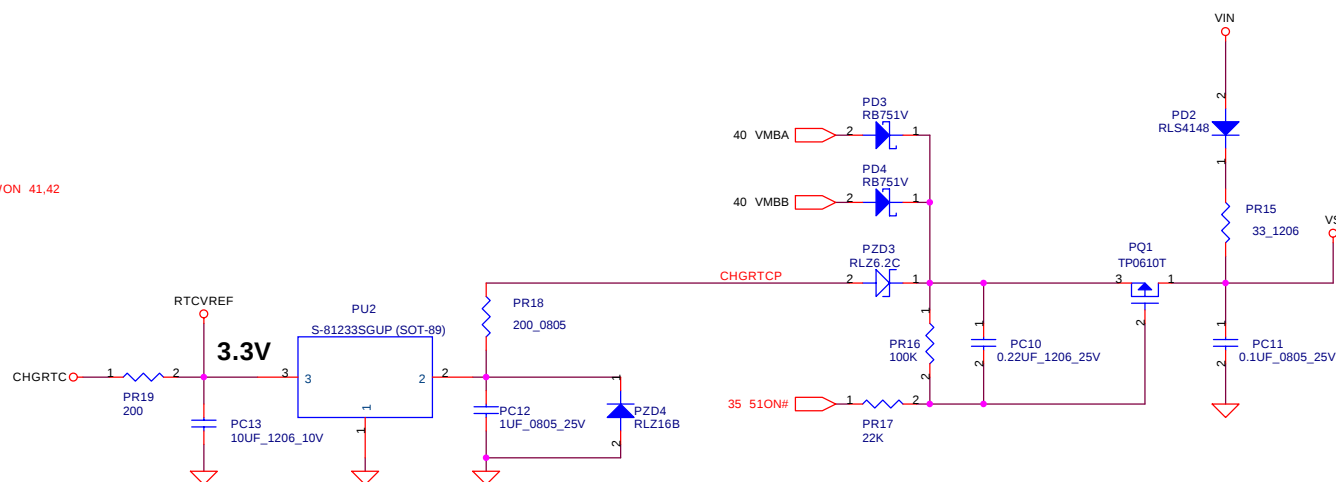
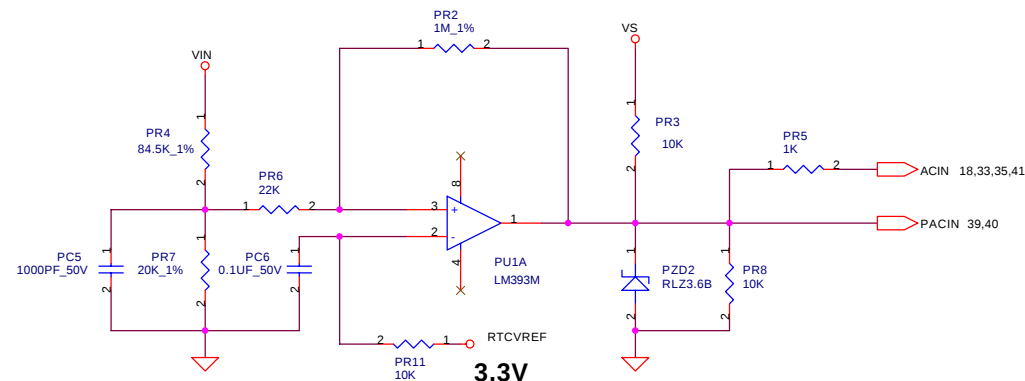


PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 50(51) degree C



Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038



+12VALWP 2 PJP2 1 +12VALW (120mA,20mils ,Via NO.= 1)
JOPEN/+12V

+5VALWP 1 PJP3 2 +5VALW (5A,200mils ,Via NO.= 10)
PAD-OPEN 4x4mm

+3VALWP 1 PJP4 2 +3VALW (5A,200mils ,Via NO.= 10)
PAD-OPEN 4x4mm

+1_5VP 2 PJP5 1 +1.5V (1.5A,60mils ,Via NO.= 3)
3MMA/CPU_IO

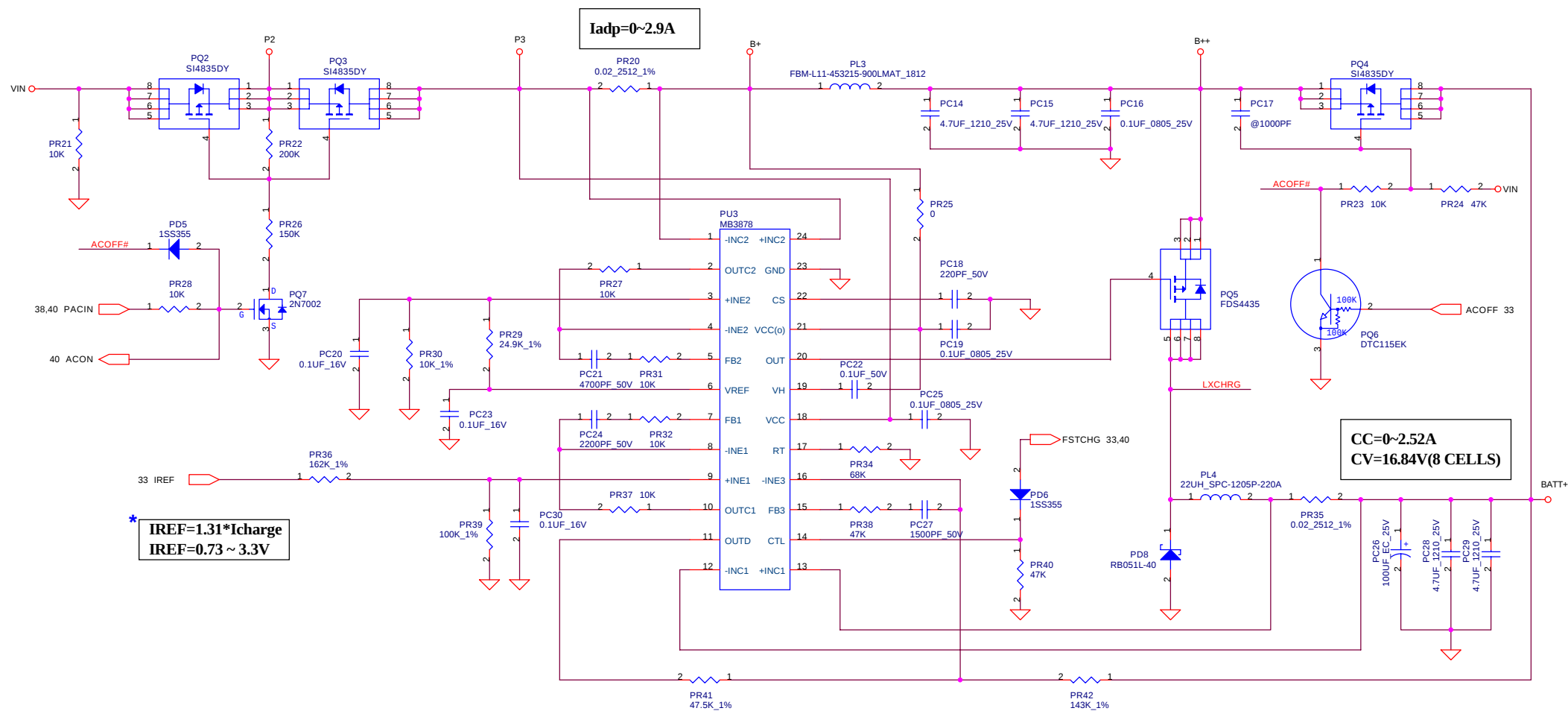
+1_8VP 2 PJP6 1 +1.8V (3A,120mils ,Via NO.= 6)
3MMA/CPU_IO

+VTP 1 PJP7 2 +VTT (6A,240mils ,Via NO.= 12)
PAD-OPEN 4x4mm

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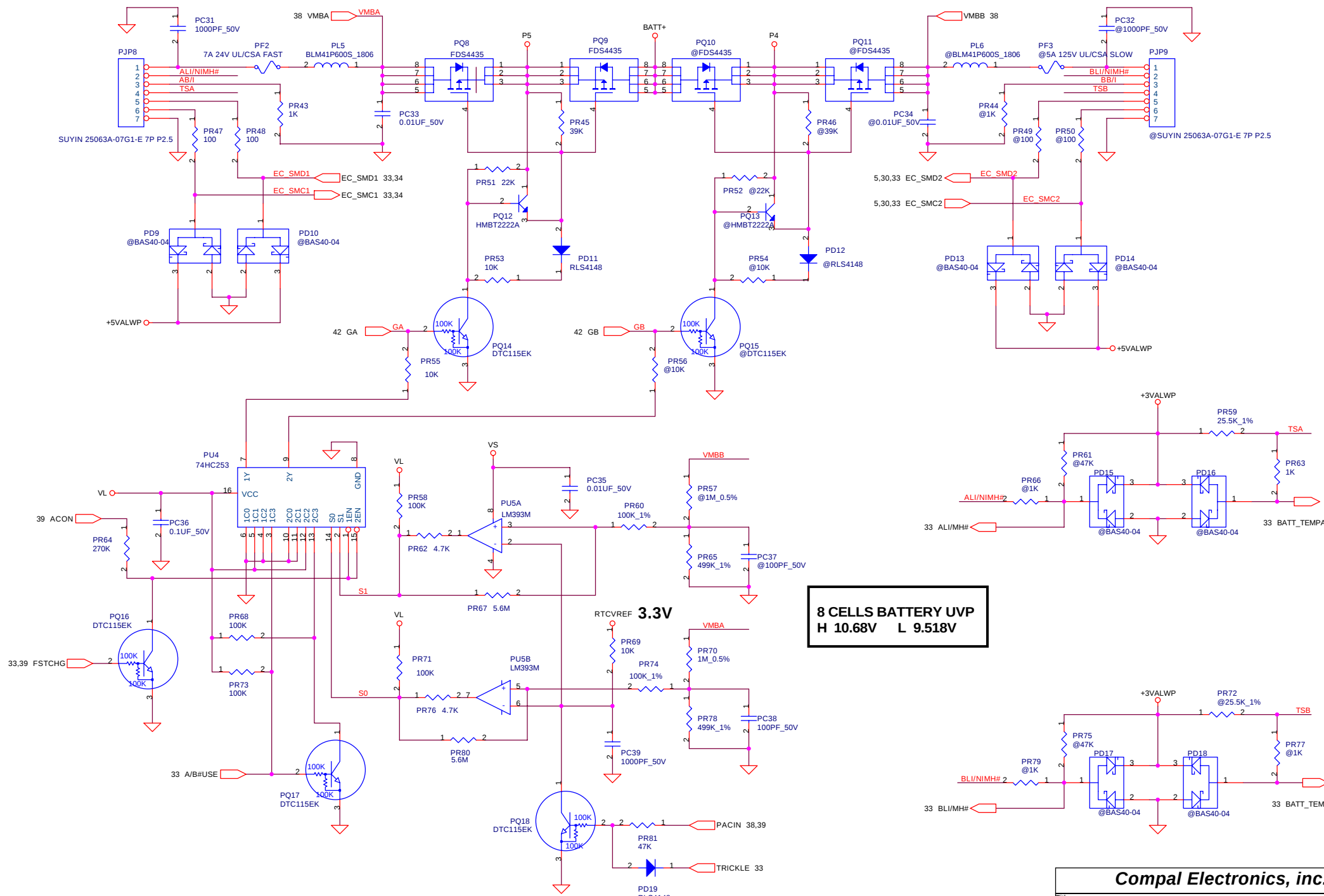
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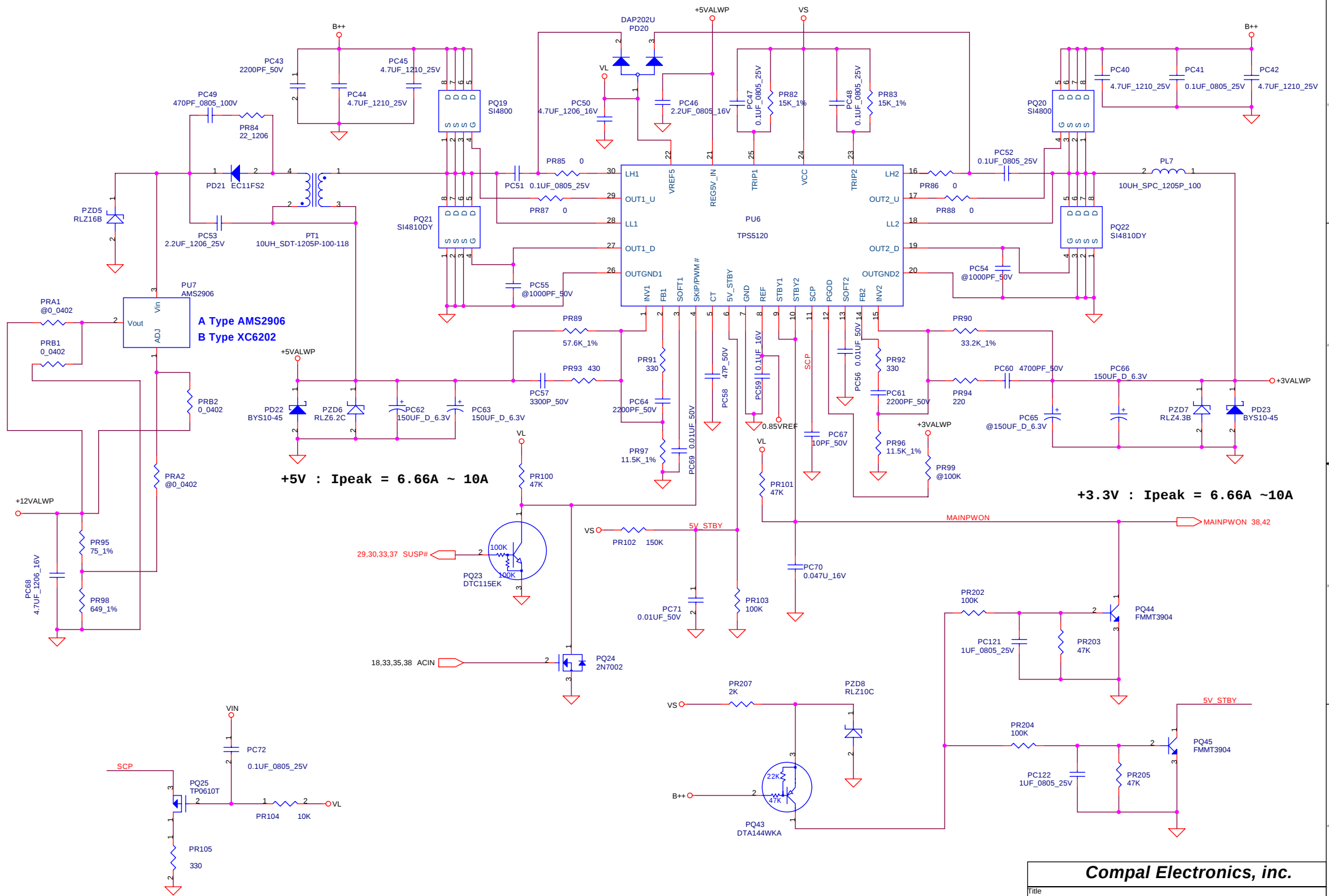
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8 CELLS BATTERY UVP
H 10.68V L 9.518V

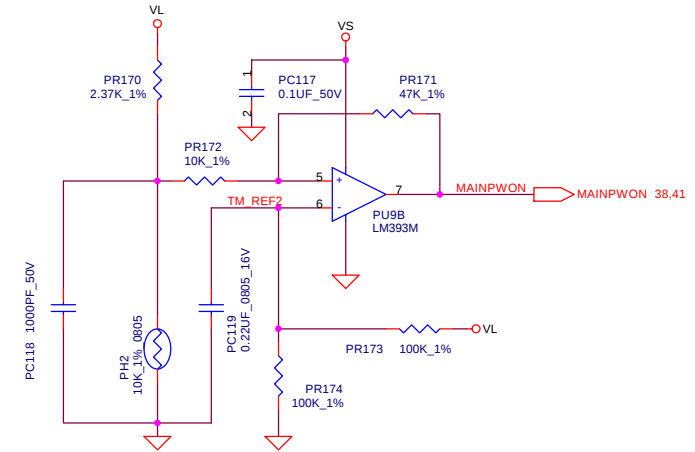
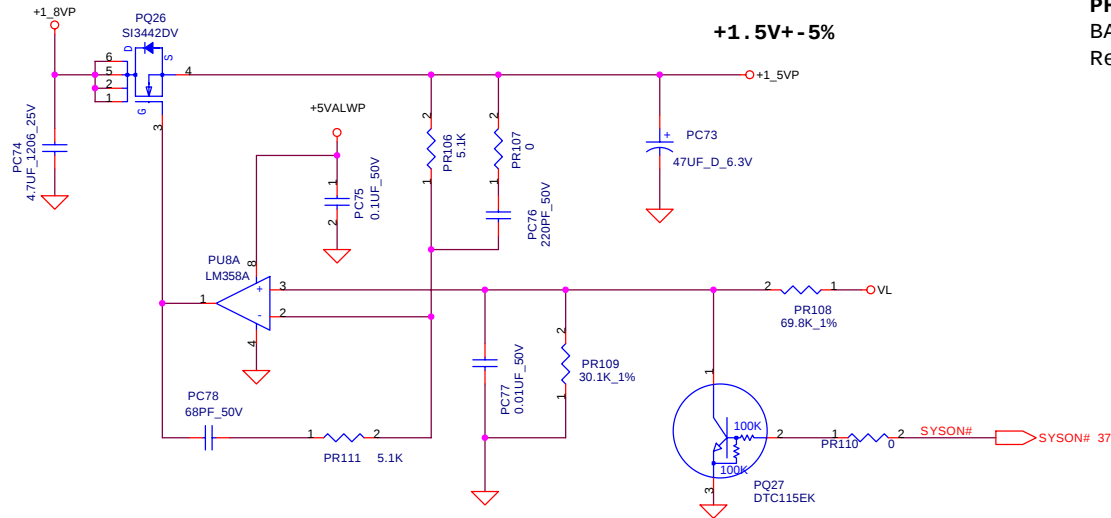
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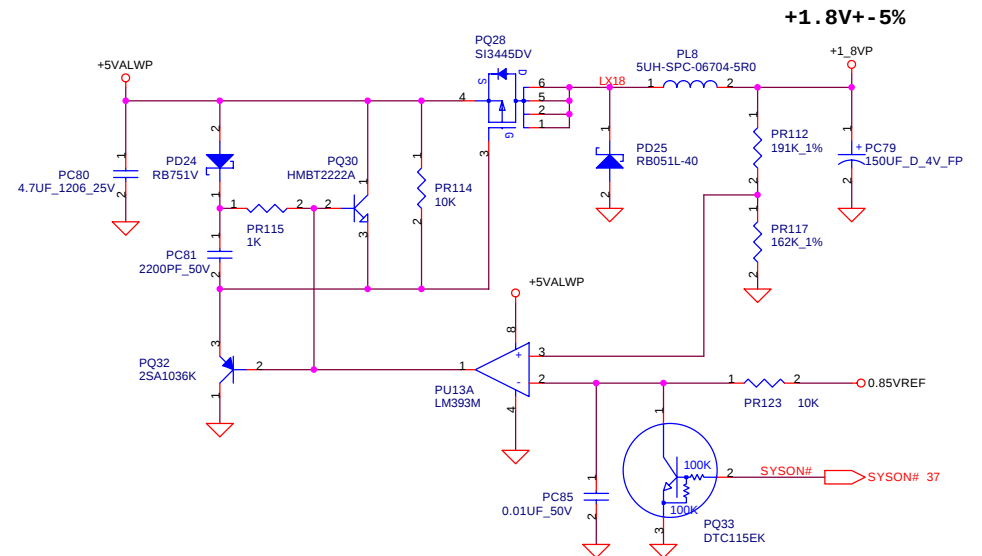
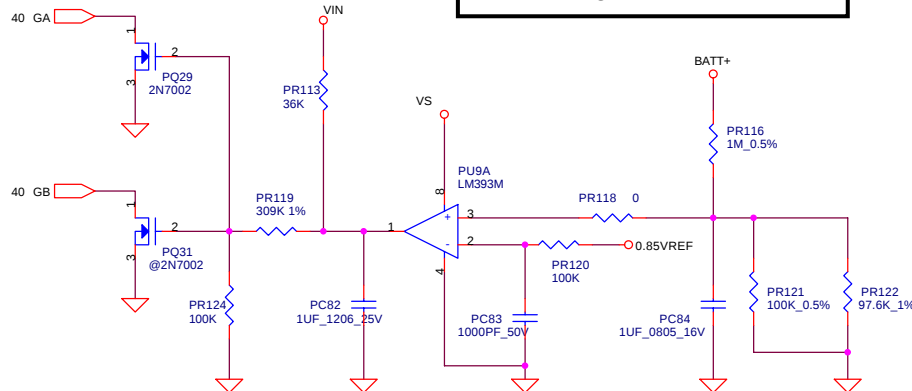
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PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50(51) degree C



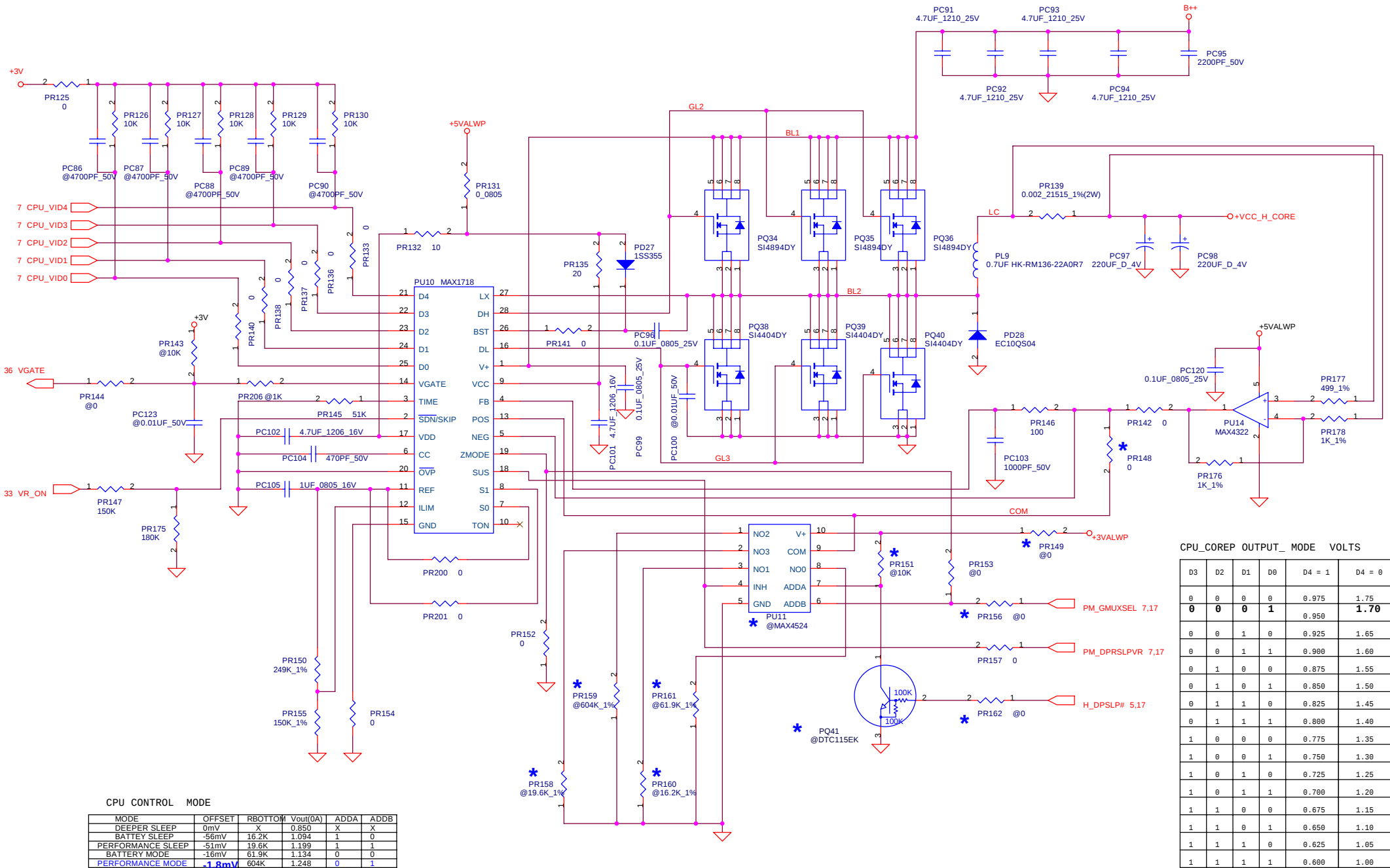
8 Cells Charger OVP : 18.059V



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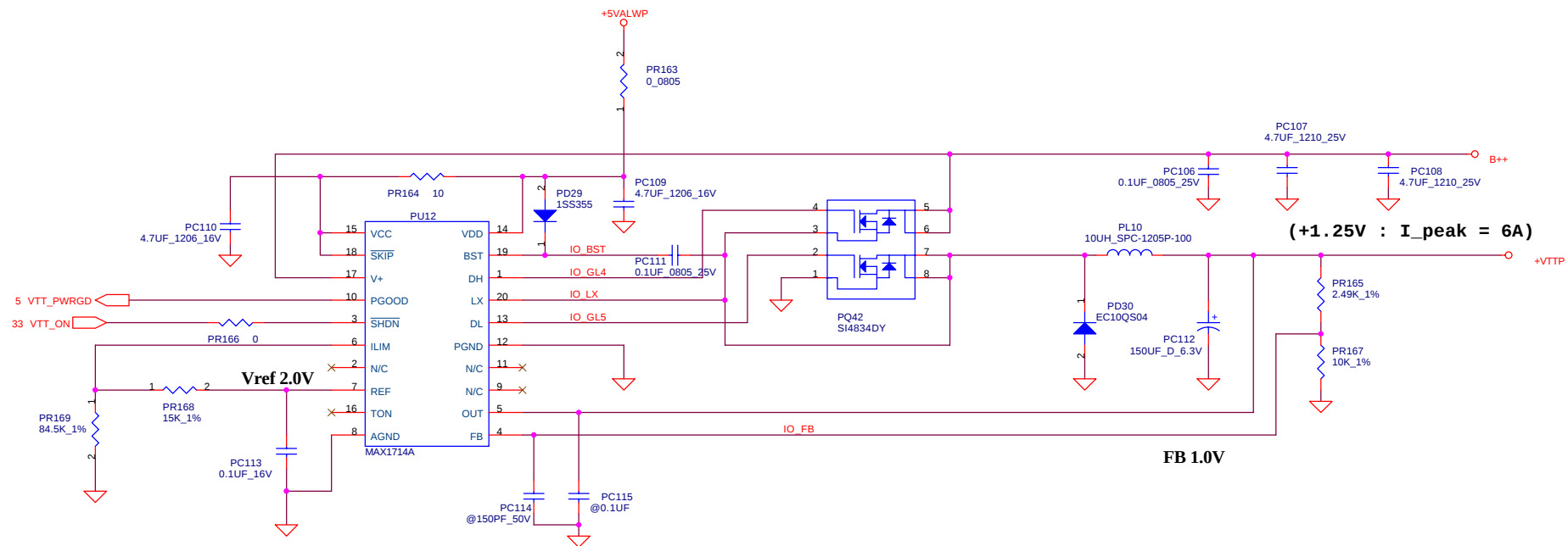
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