

Prescott & Springdale Schematic with Capture CIS and Function field

uFCPGA Prescott

2003-07-23

REV: X02-D

Cature library ball out check document

Prescott : Prescott processor Electrial,Mechanical and Thermal Specification Rev0.5 [Check by HW:Henry,Steve]

Springdale (GMCH): Springdale GMCH External Design Specification (EDS) REV1.0 [Check by HW: Henry,Rita]

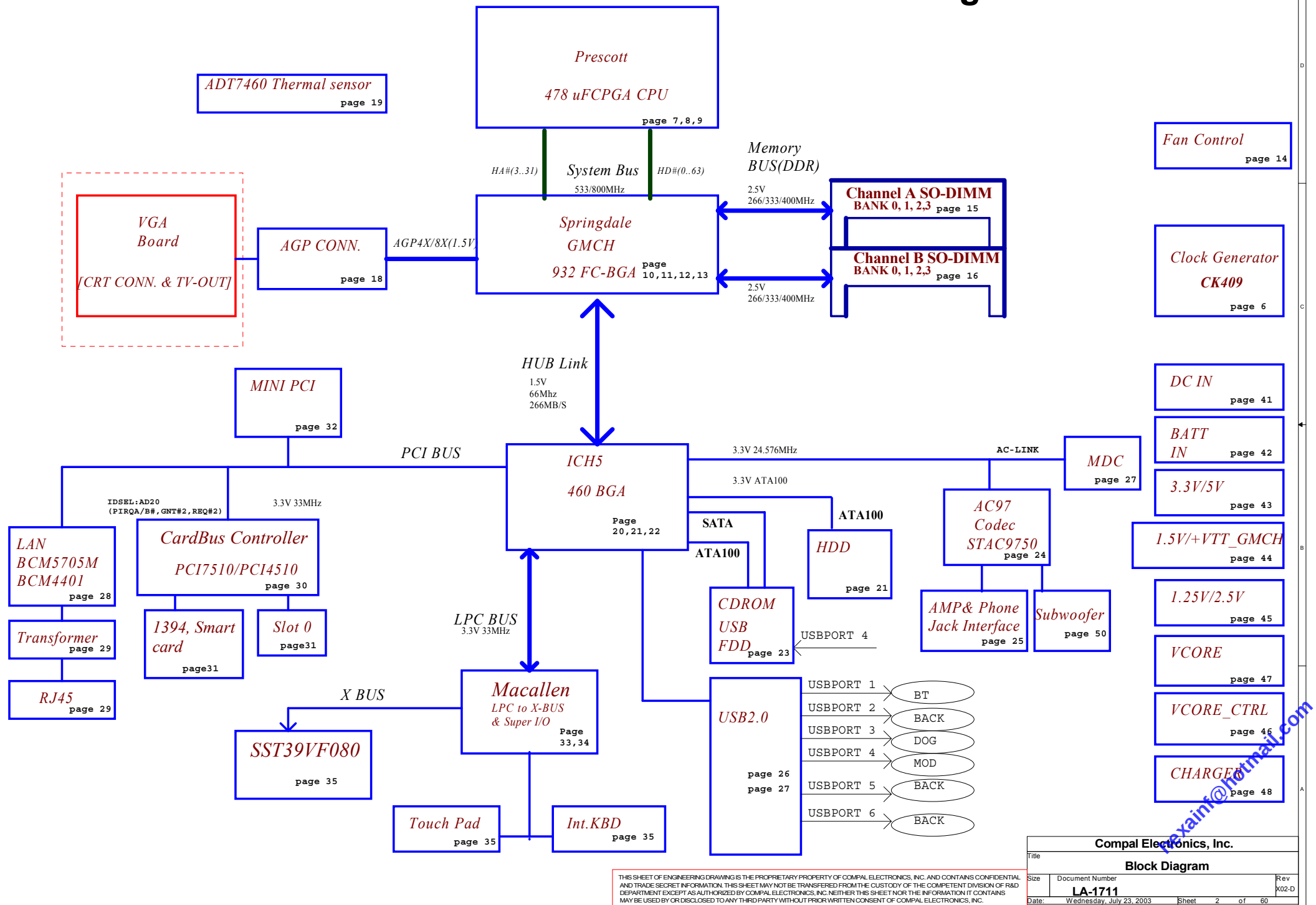
ICH5: N/A

@ : Depop Component
1@ : Depop on Nimitz (Inspiron)
2@ : Depop on Beijing (Precision)

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Block Diagram



PM TABLE

power plane State	+3VALW +5VALW	+3VSUS +5VSUS +2.5V_MEM +3.3VRTC +RTC_PWR	+3VRUN +5VRUN +1.5VRUN +VCC_CORE +12V +VCCVID V_1P25V_DDR_VTT
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D, C
LAN	AD16	4	C
MINI PCI	AD19	3	D, B (NP)
VGA			A, B (NP)

USB TABLE

USB PORT#	DESTINATION
0	Reserved
1	BT
2	BACK
3	DOG
4	MOD
5	BACK
6	BACK
7	Reserved

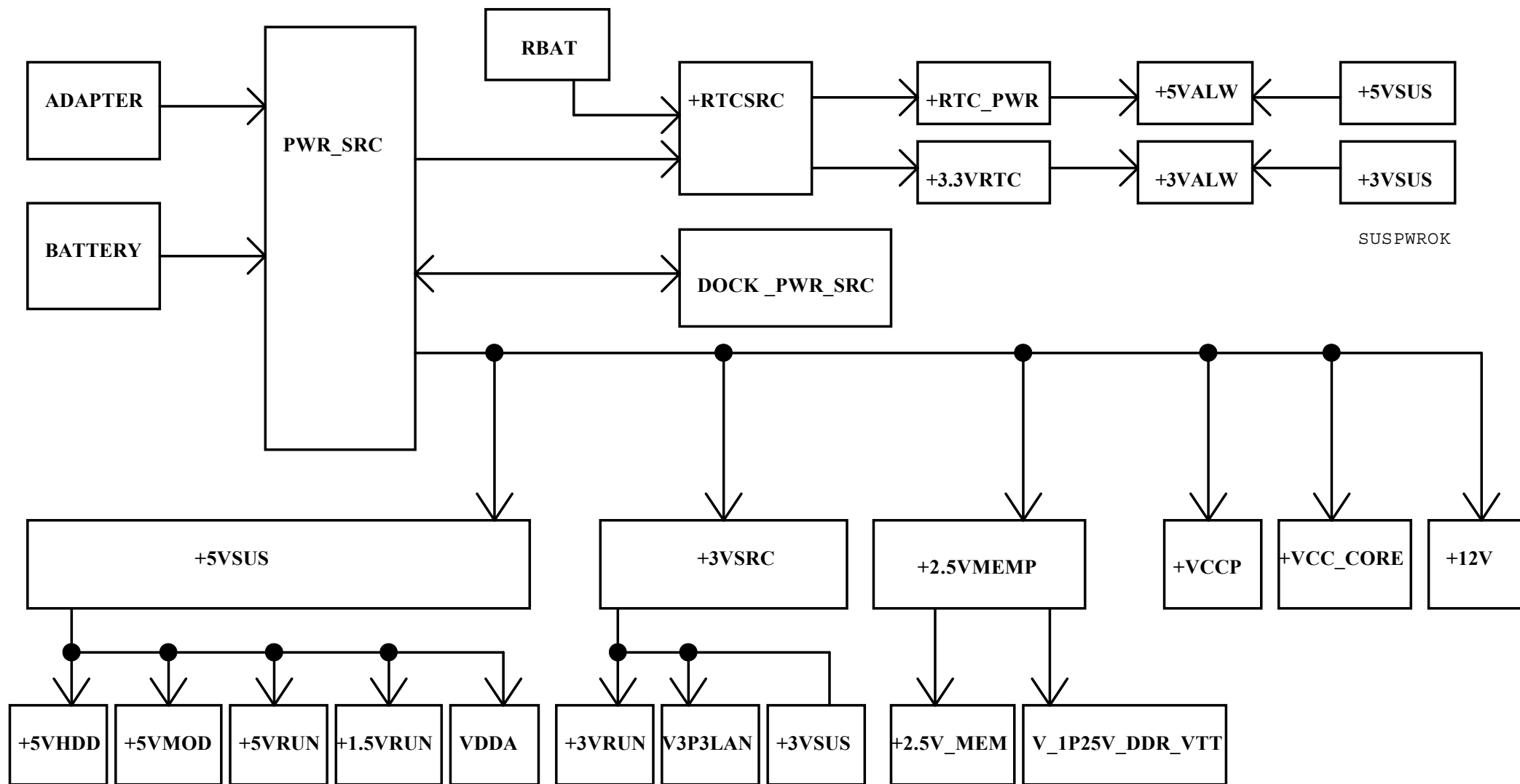
Note : "@" means all model depop
"1@" means Nimitz depoped only
"2@" means Beijing depoped only

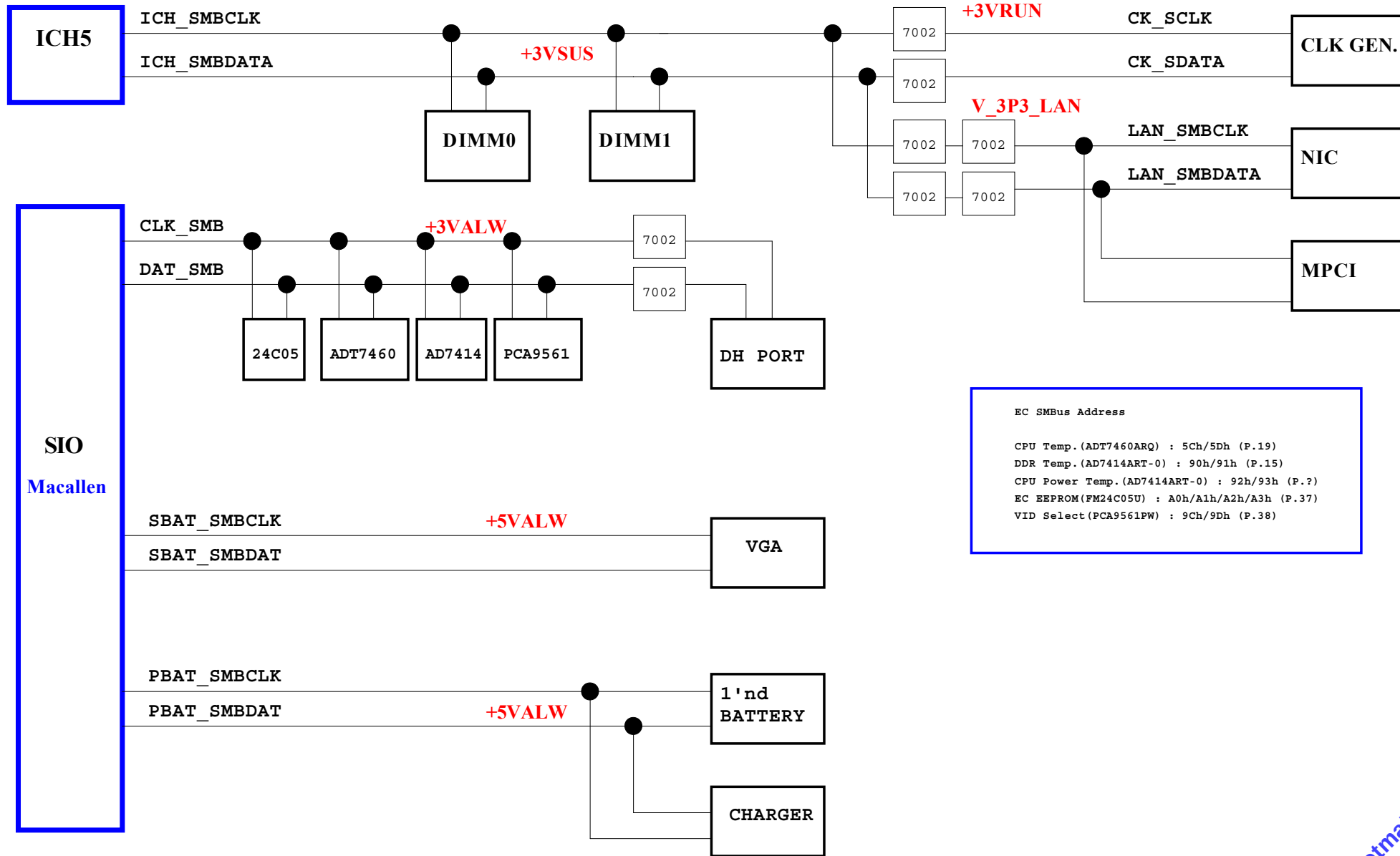
Model Function	Nimitz	Beijing
Smart Card	No	YES
LAN	10/100 (4401)	1000 (5705M)
Dog House	YES	YES

	MCH Rev.	ICH5 Rev.
Bring up	RG828SDGES A1 (QE18)	FW82801EB A1 (QE16ES)
SST-Build	RG828SDGP A2 (QE45)	FW82801EB A3 (QE51ES)
PT-Build		
ST-Build		
QT-Build		
Pilot-Build		

Configuration List

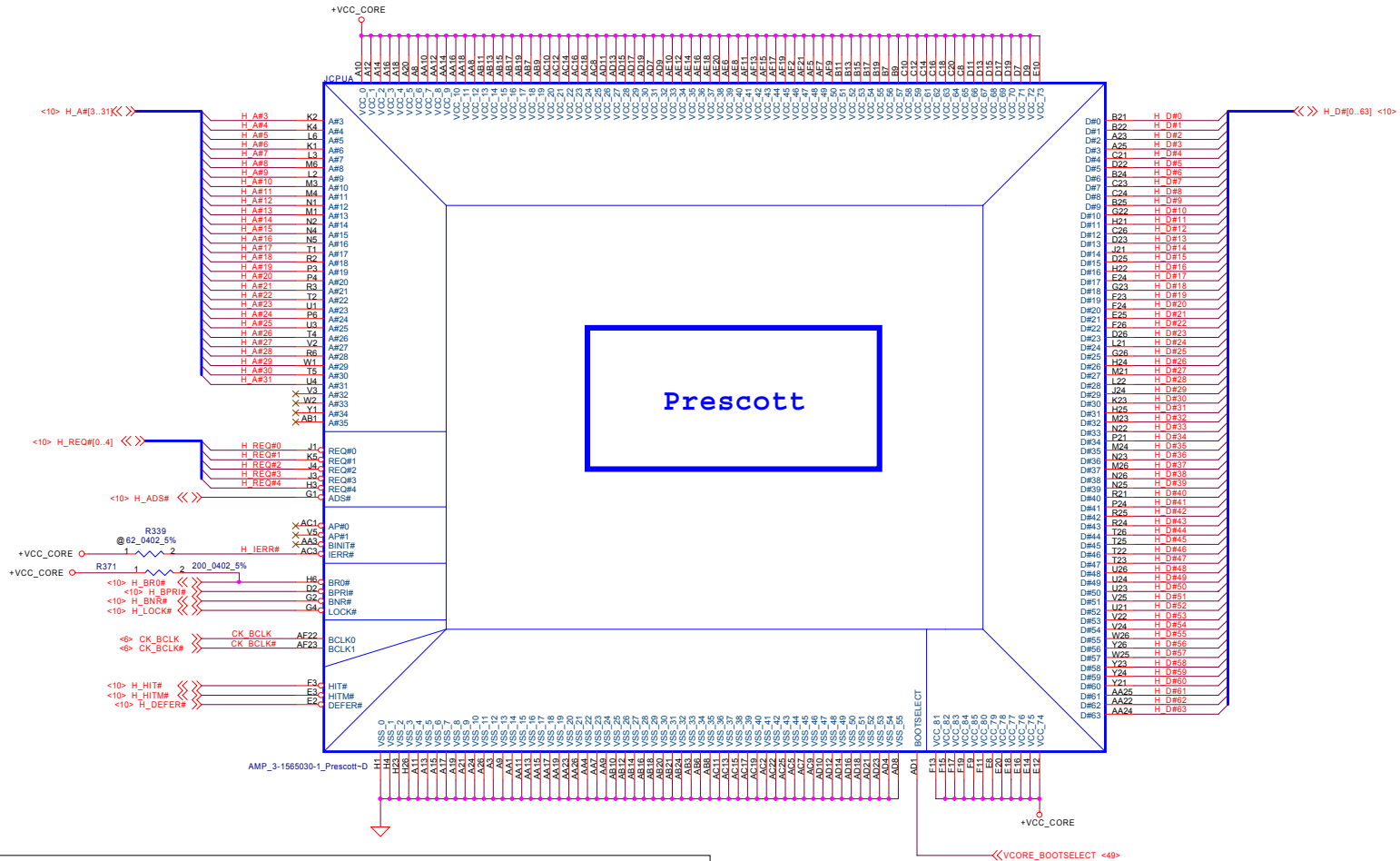
BOM Structure		
Function		





EC SMBus Address

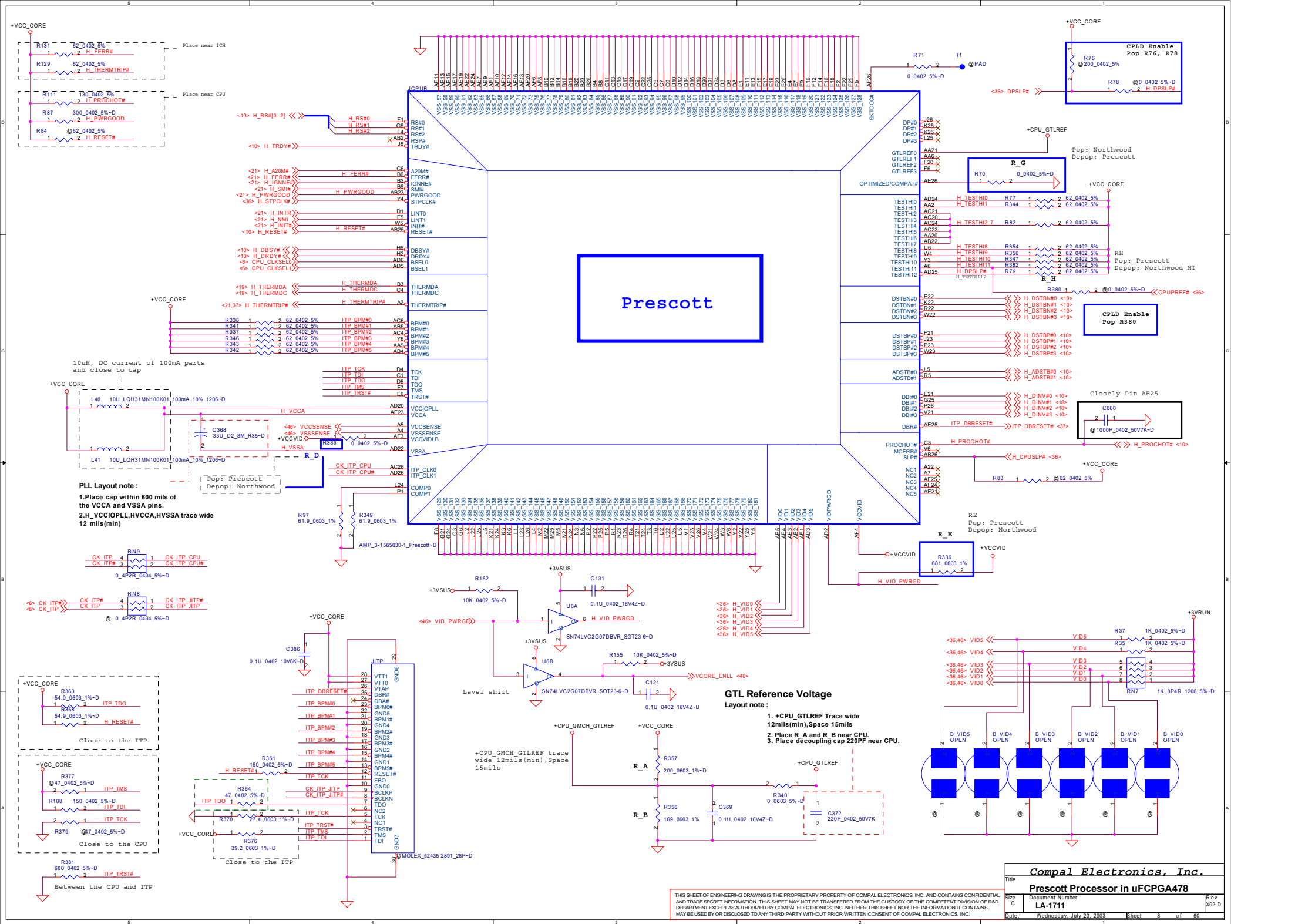
CPU Temp. (ADT7460ARQ) : 5Ch/5Dh (P.19)
DDR Temp. (AD7414ART-0) : 90h/91h (P.15)
CPU Power Temp. (AD7414ART-0) : 92h/93h (P.?)
EC EEPROM (FM24C05U) : A0h/A1h/A2h/A3h (P.37)
VID Select (PCA9561PW) : 9Ch/9Dh (P.38)

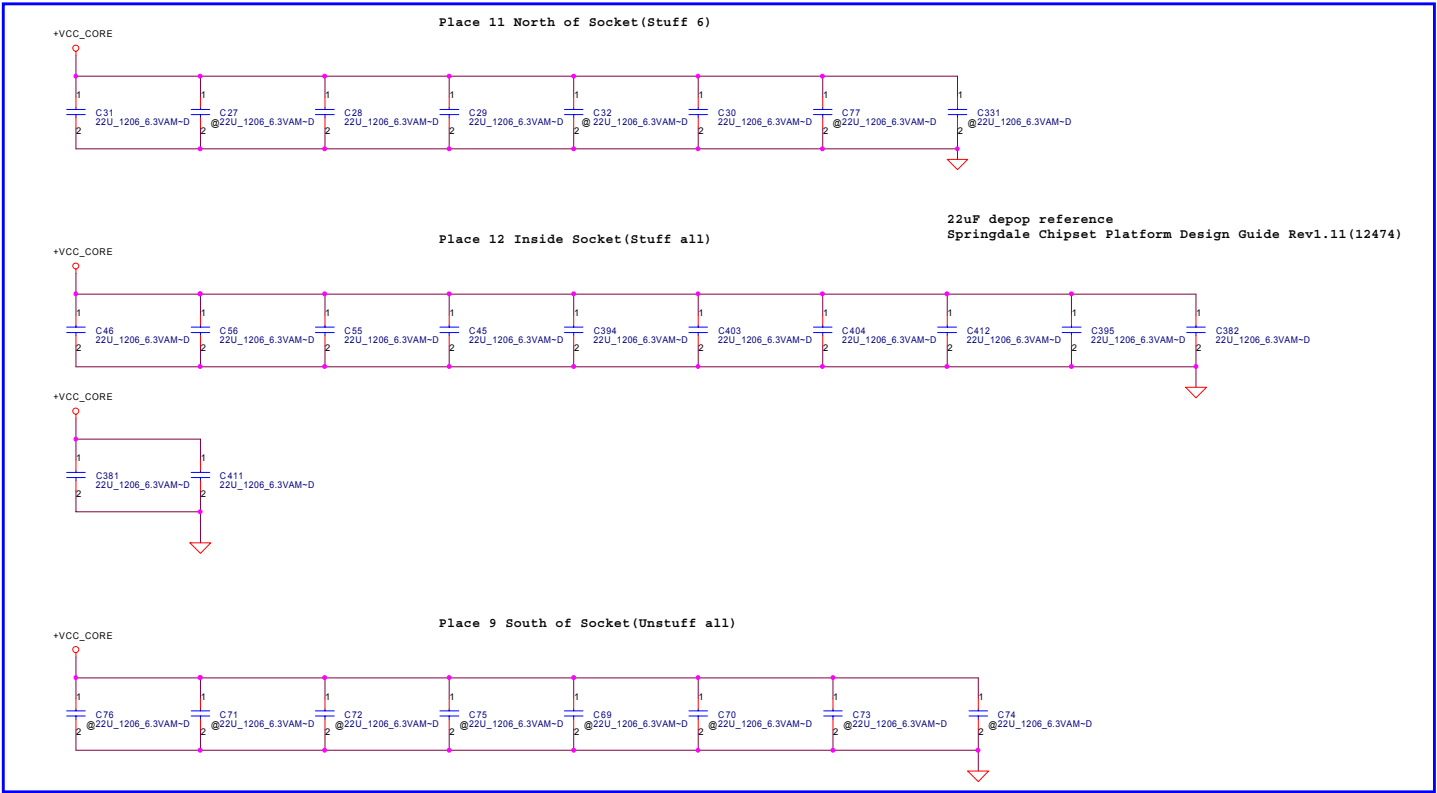


Reference Intel document						
Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0						
Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5						
Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood MT Pin name	Comment
A6	TESTHI11	Pull-up 200ohm to +VCC_CORE	TESTHI11	Pull-up 62ohm to +VCC_CORE	GHI	Connect to PLD CPU/PB/F through 0ohm
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBR#	Pull-up 62ohm to +VCC_CORE	FERR#	Pull-up 62ohm to +VCC_CORE
AA20	ITPCLKOUT0	Pull-up 56ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	ITPCLKOUT0	Pull-up 56ohm to +VCC_CORE
AB22	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	ITPCLKOUT1	Pull-up 56ohm to +VCC_CORE
AD2	NC	float	VIDPWRGD	Pull-up 2.43K ohm to +VCCVID	NC	float
AD3	NC	float	VID5	Pull-up 1Kohm to +3VRUN & connect to PWRIC	NC	float
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	NC	float
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	VSS	Connect to GND
AD25	TESTHI12	Pull-up 200ohm to +VCC_CORE	TESTHI12	Pull-up 62ohm to +VCC_CORE	DPSLP	Connect to PLD through 0ohm

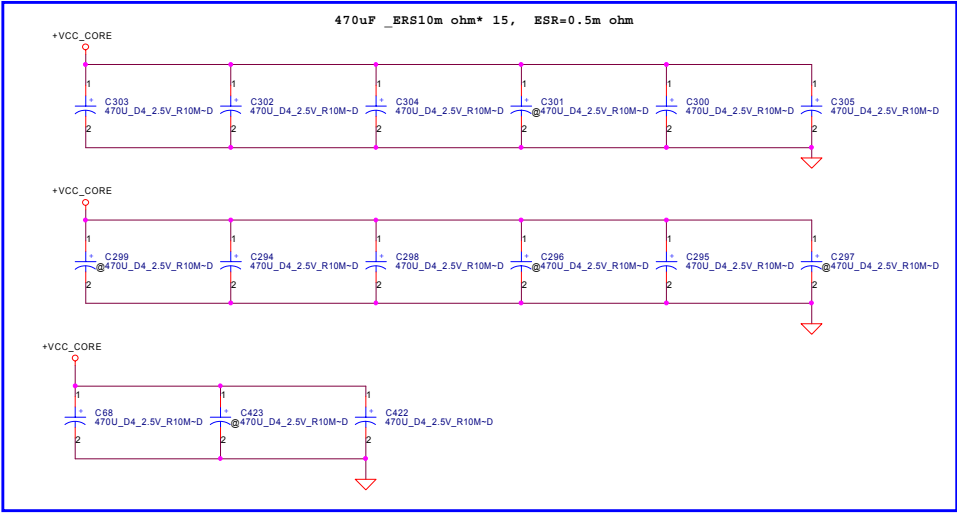
Note: AD2,AD3 pop(bring up)

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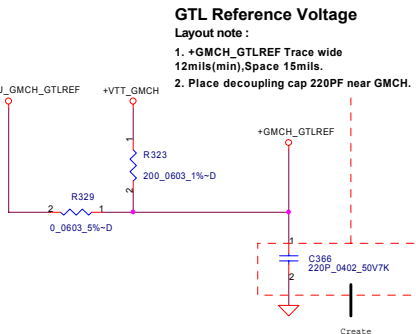
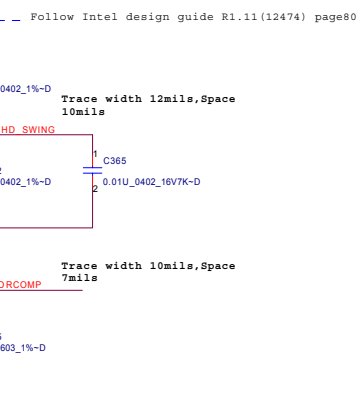
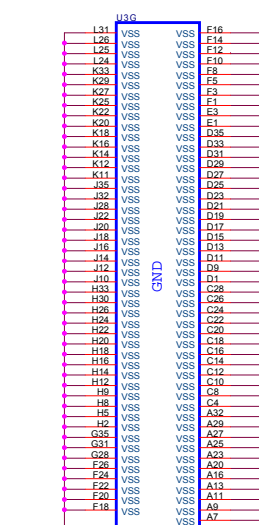
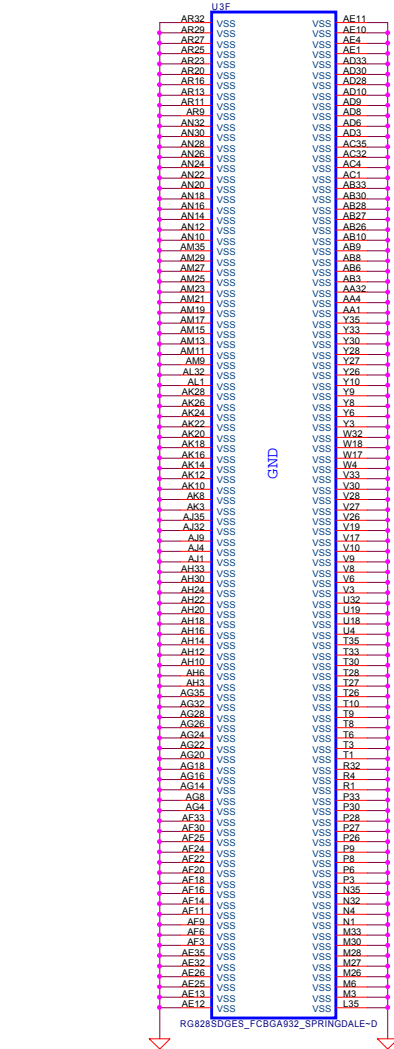
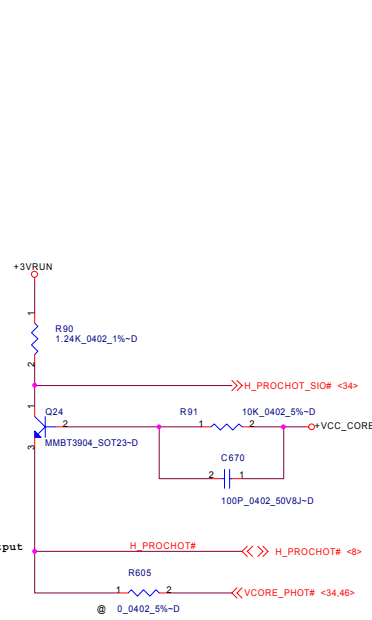
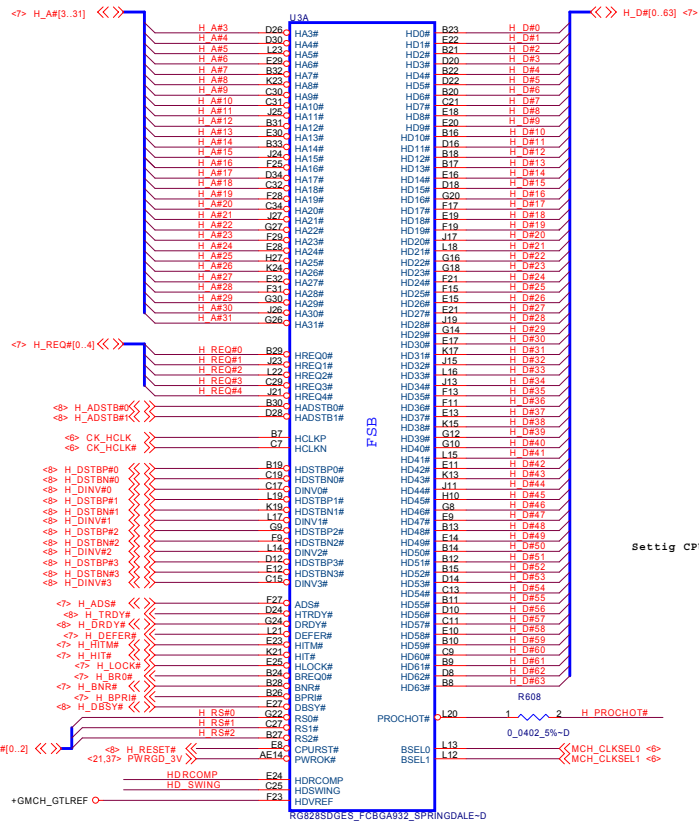


Note: For PT-phase
22uF depop reference
Springdale Chipset Platform Design Guide Rev1.2 (12837)
Inside the socket cavity 12 pcs (all stuffed)
North side 12pcs (4 sites stuffed)
Delete south side

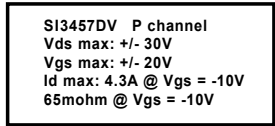


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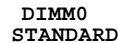
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CPU Decoupling		
Size C	Document Number LA-1711	Rev K02-D
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GTL Reference Voltage
 Layout note:
 1. +GMCH_GTLREF Trace wide 12mils(min),Space 15mils.
 2. Place decoupling cap 220PF near GMCH.



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Title			
FAN CONTROL			
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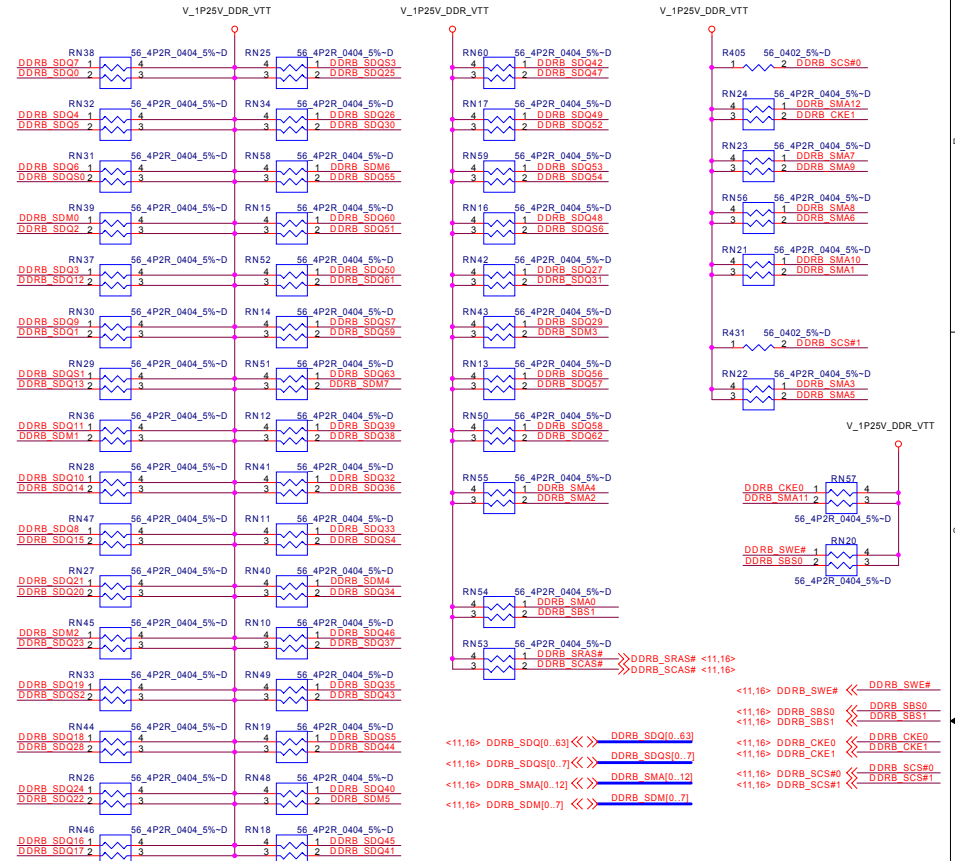


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Channel A(DIMM0) Termination
resistors & Decoupling caps

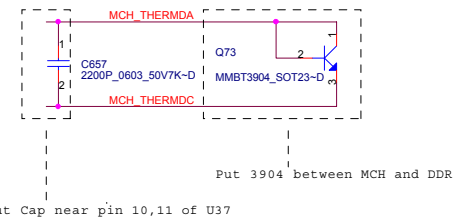
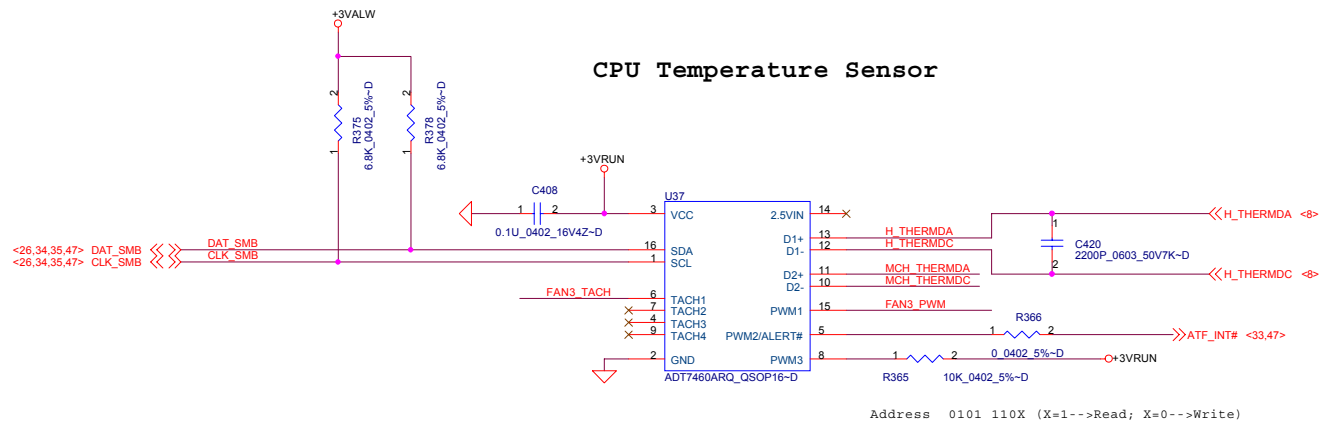


Channel B(DIMM1) Termination
resistors & Decoupling caps

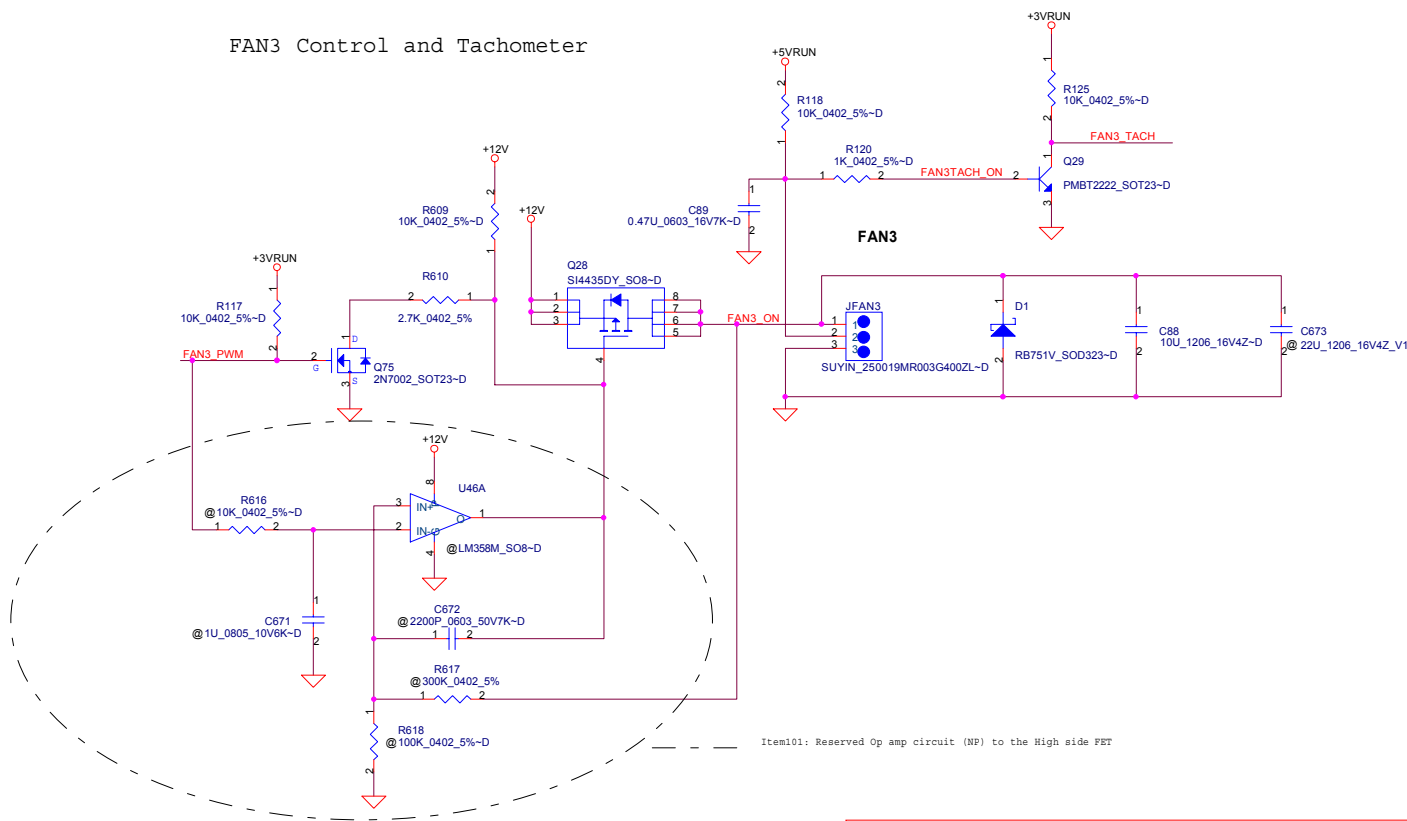


Decoupling Reference Document:
Springdale Customer Schematic R1.2 page26
each Channel(two DIMMs) requirement 4.7uF*2 ;
0.1uF*26

Title		DDR Termination Resistors	
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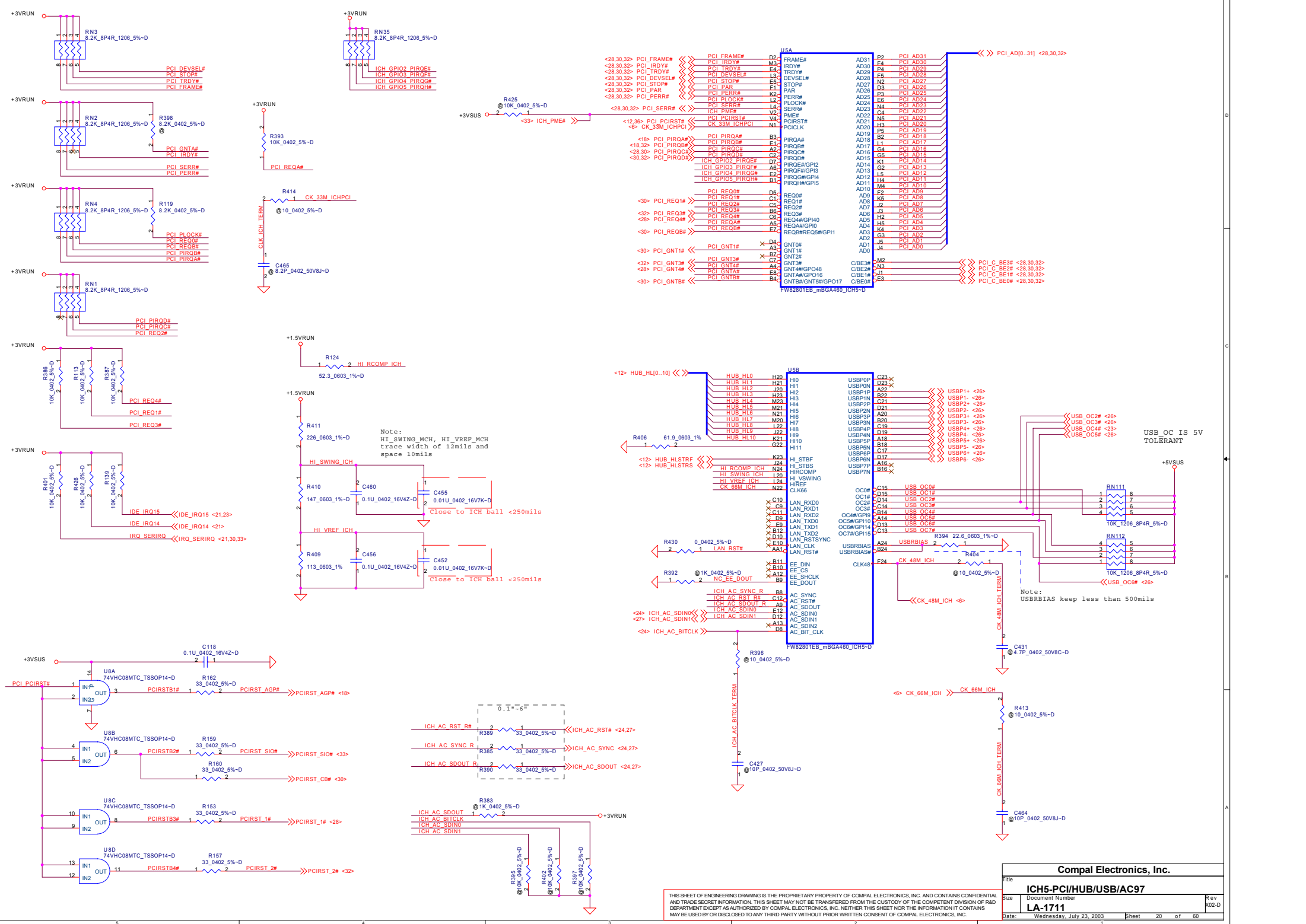


FAN3 Control and Tachometer

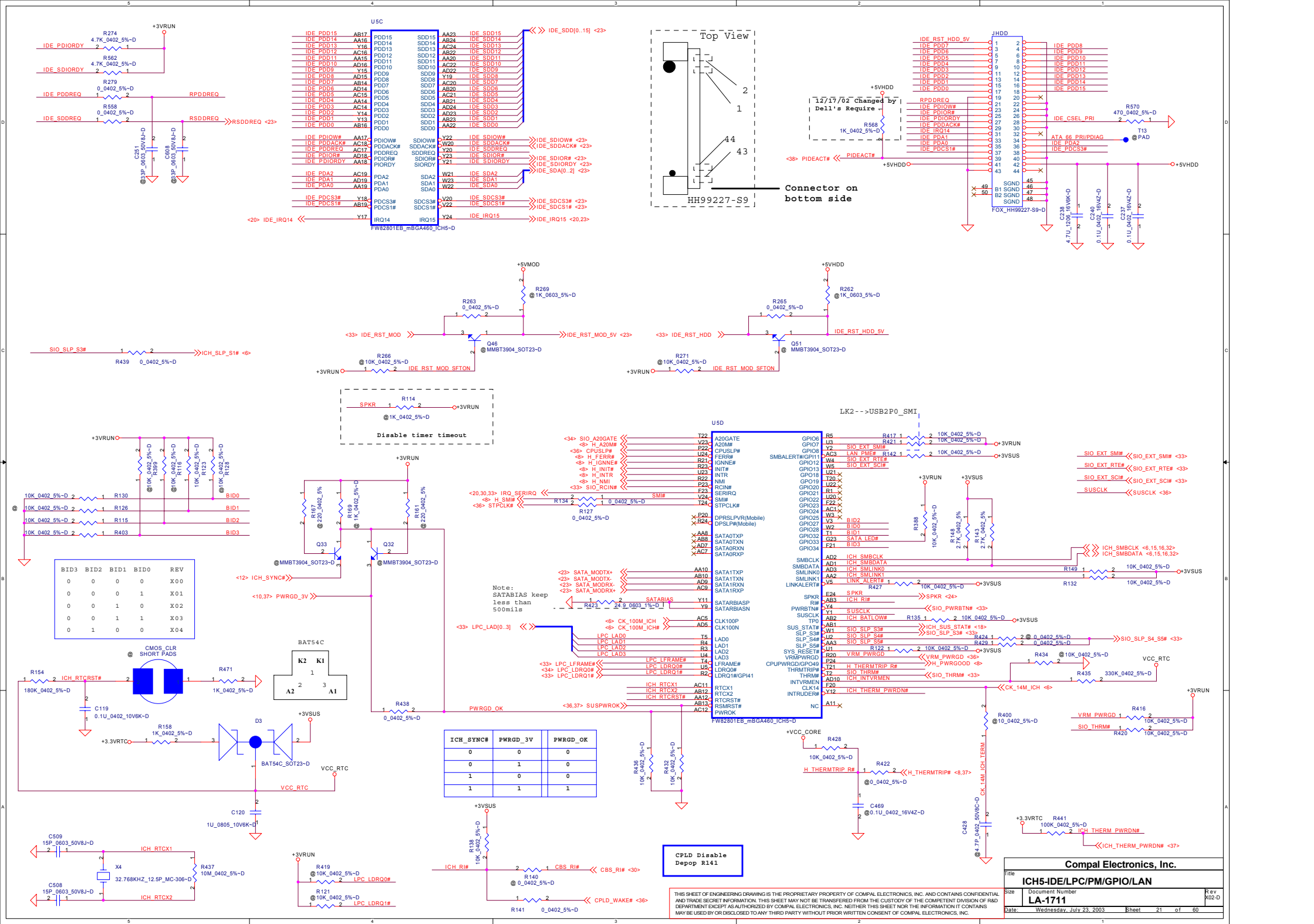


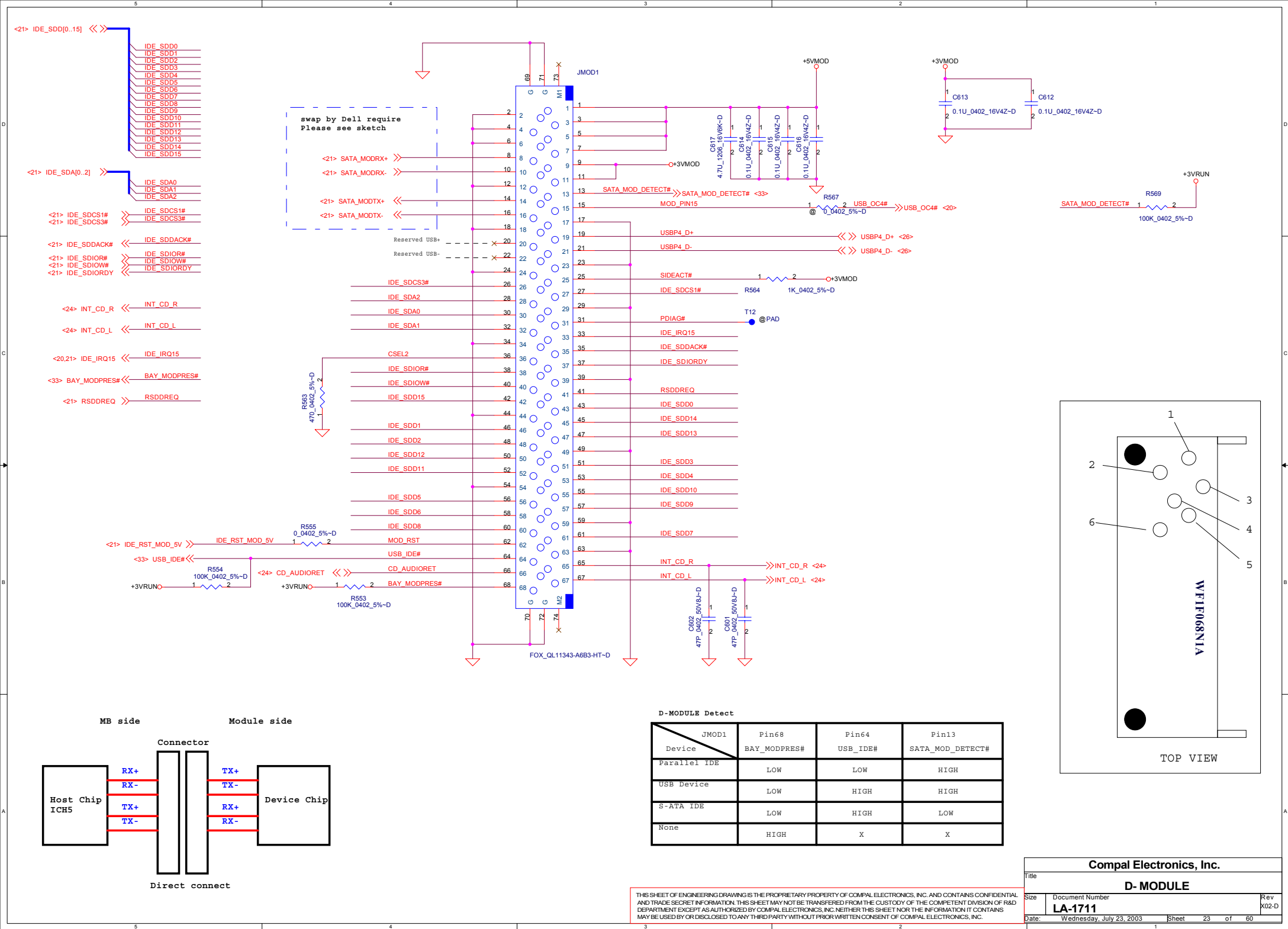
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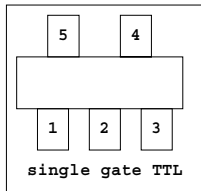
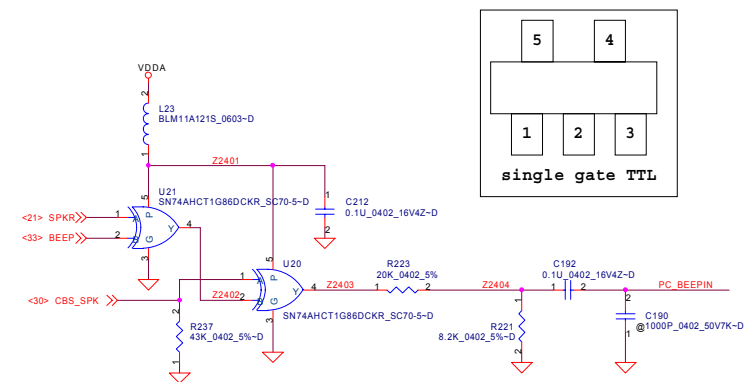
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Title	CPU Thermal Sensor & FAN Control		
Size	Document Number	Rev	
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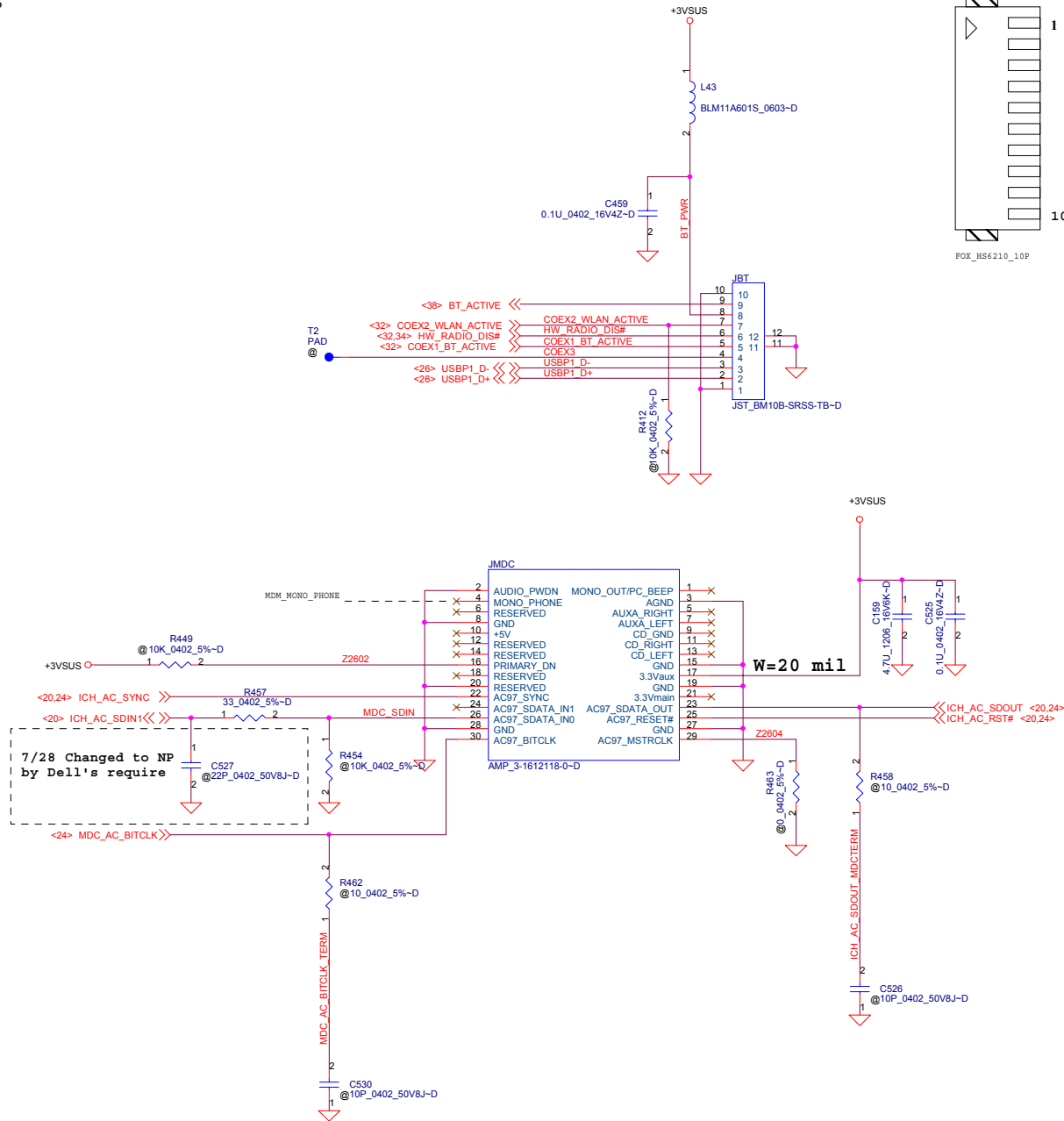






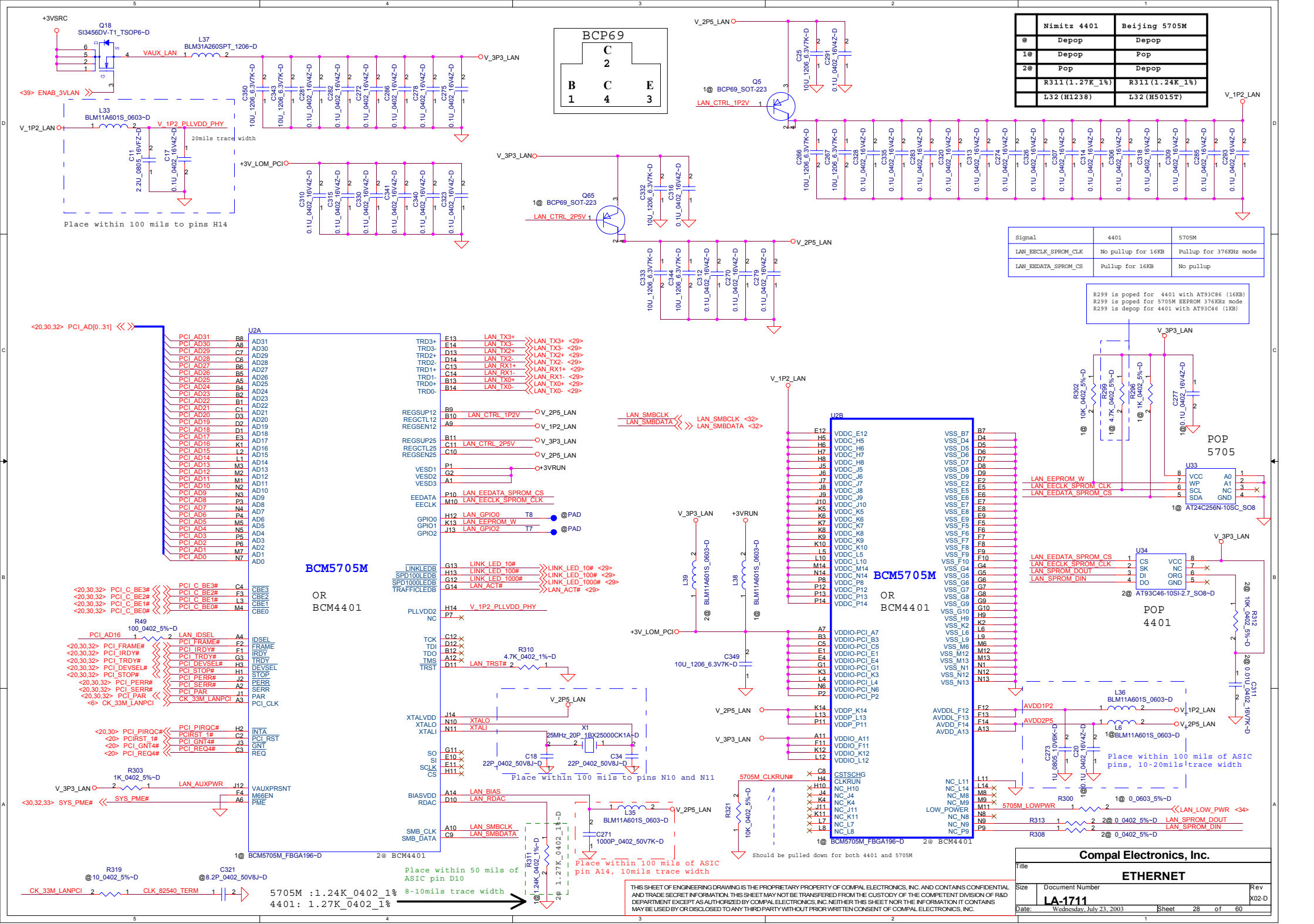
MDC cable wire clip

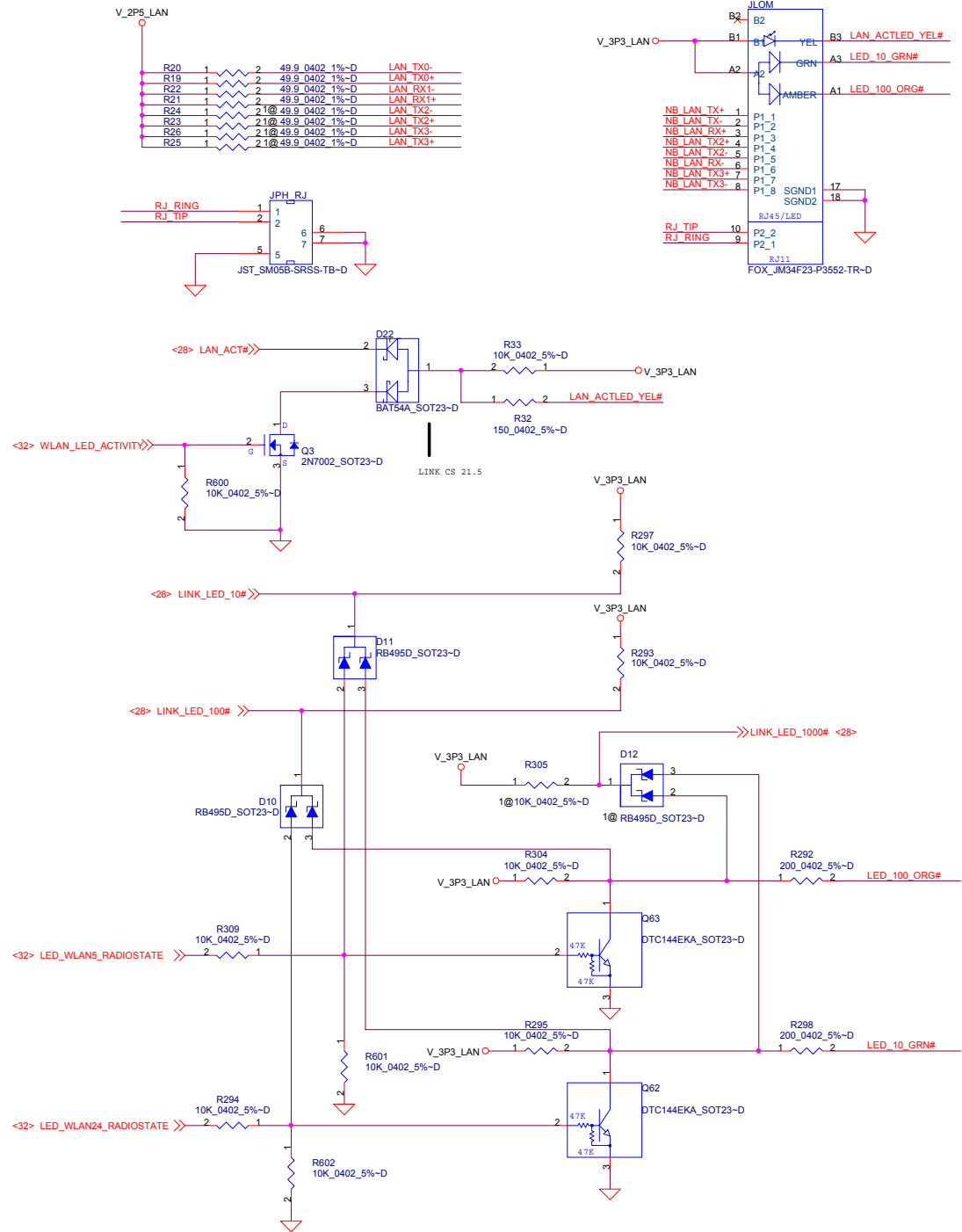
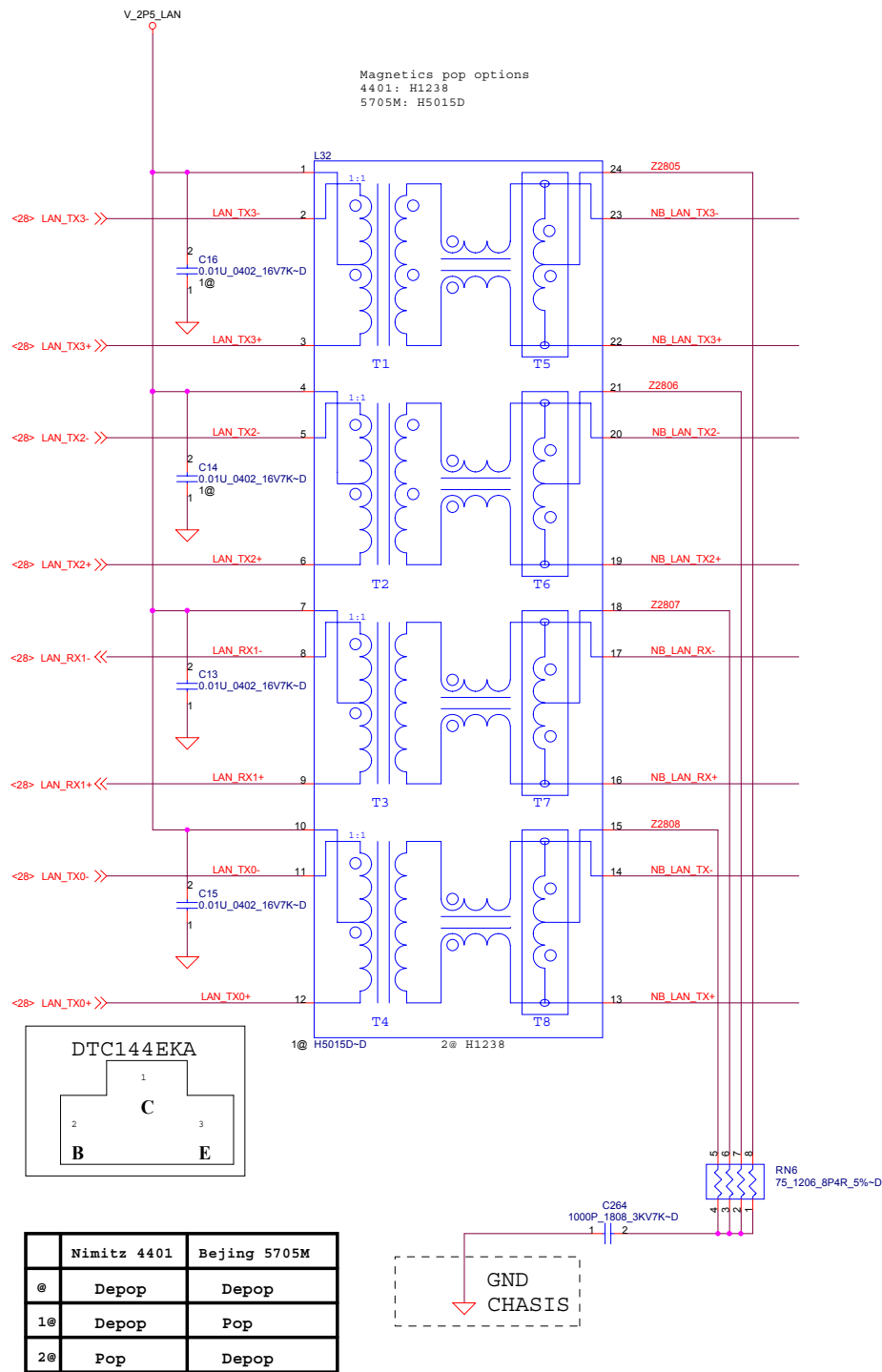
PAD2
MDC_CLIP
PAD3
MDC_CLIP

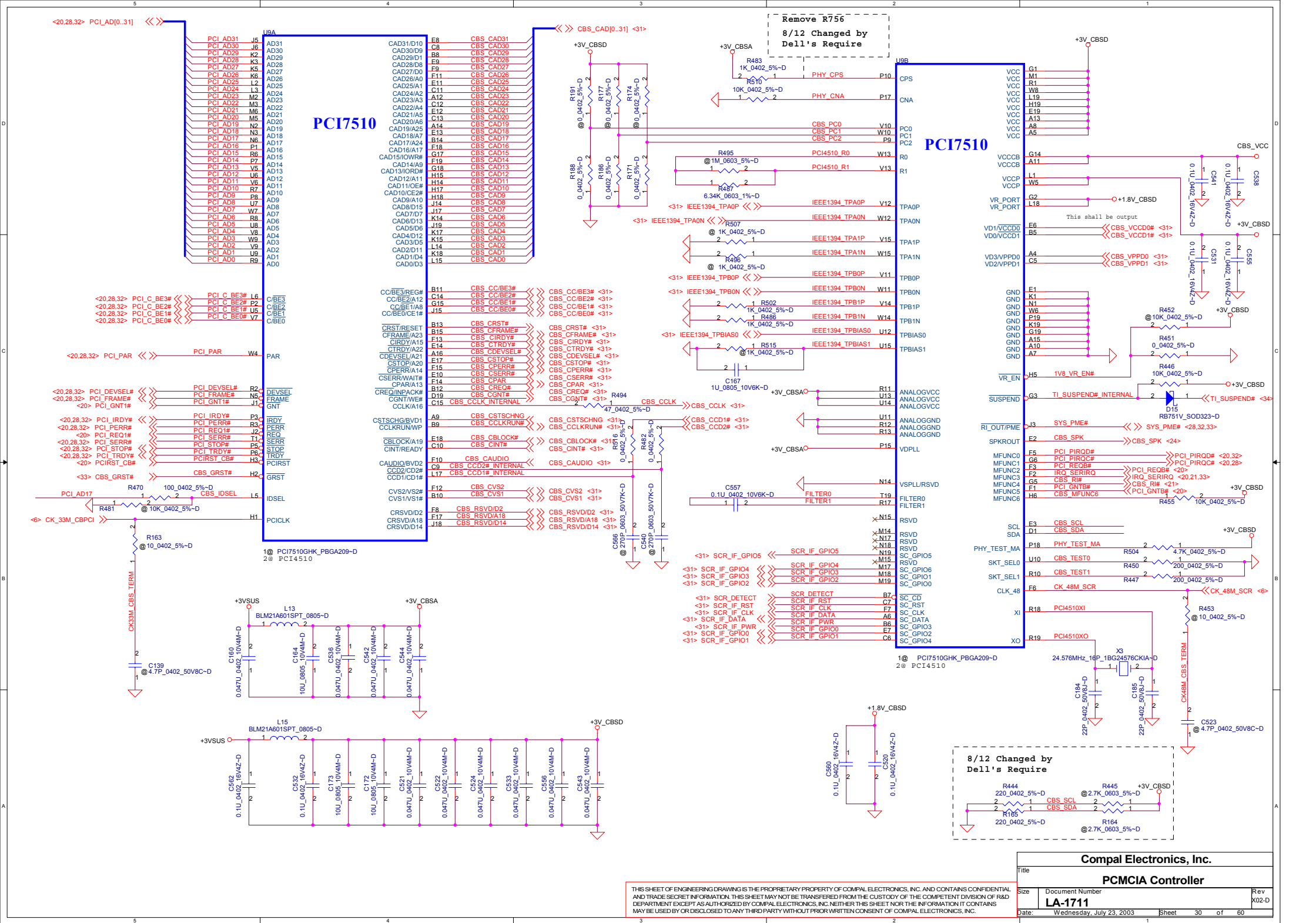


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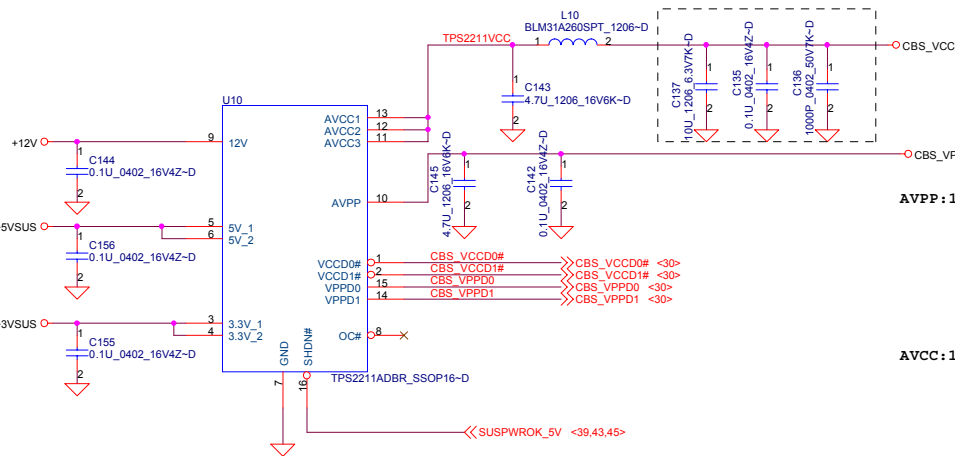
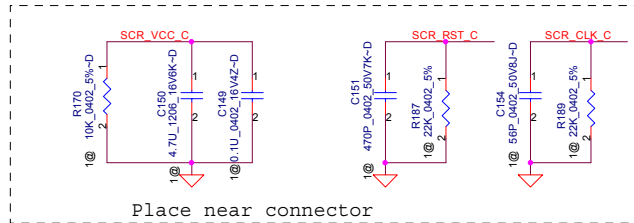
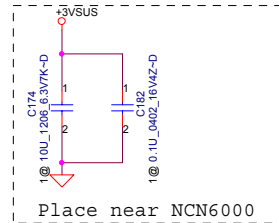
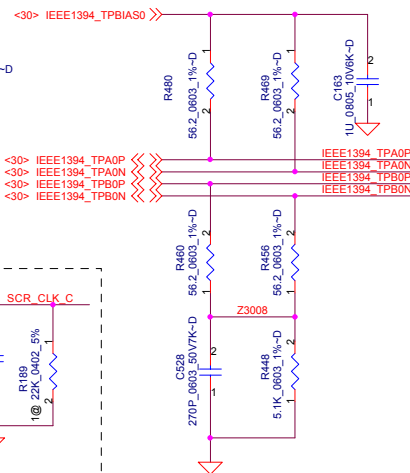
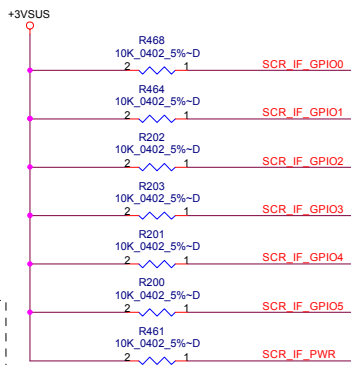
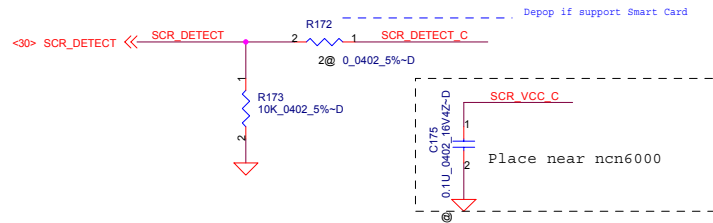
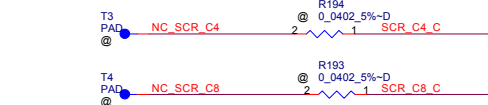
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Title			
BT PORT and MDC			
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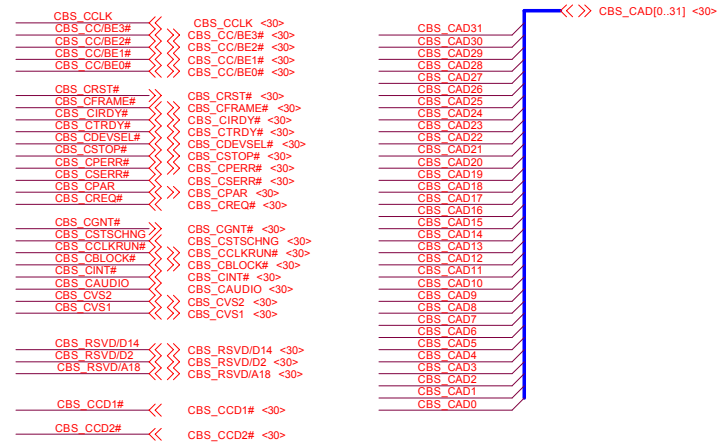
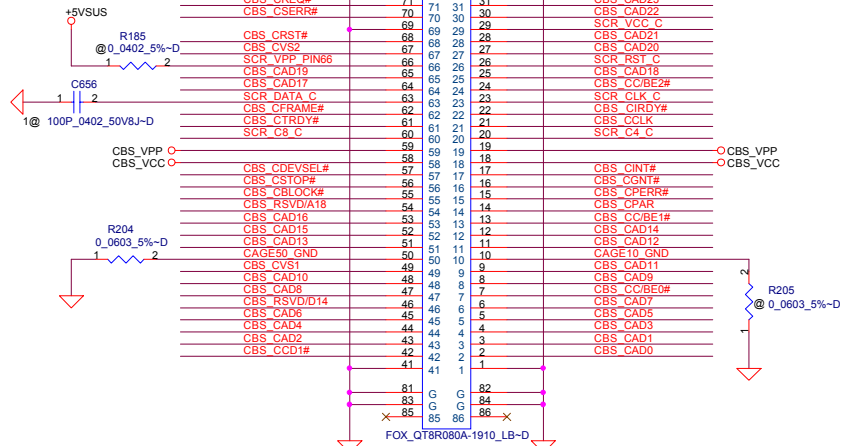


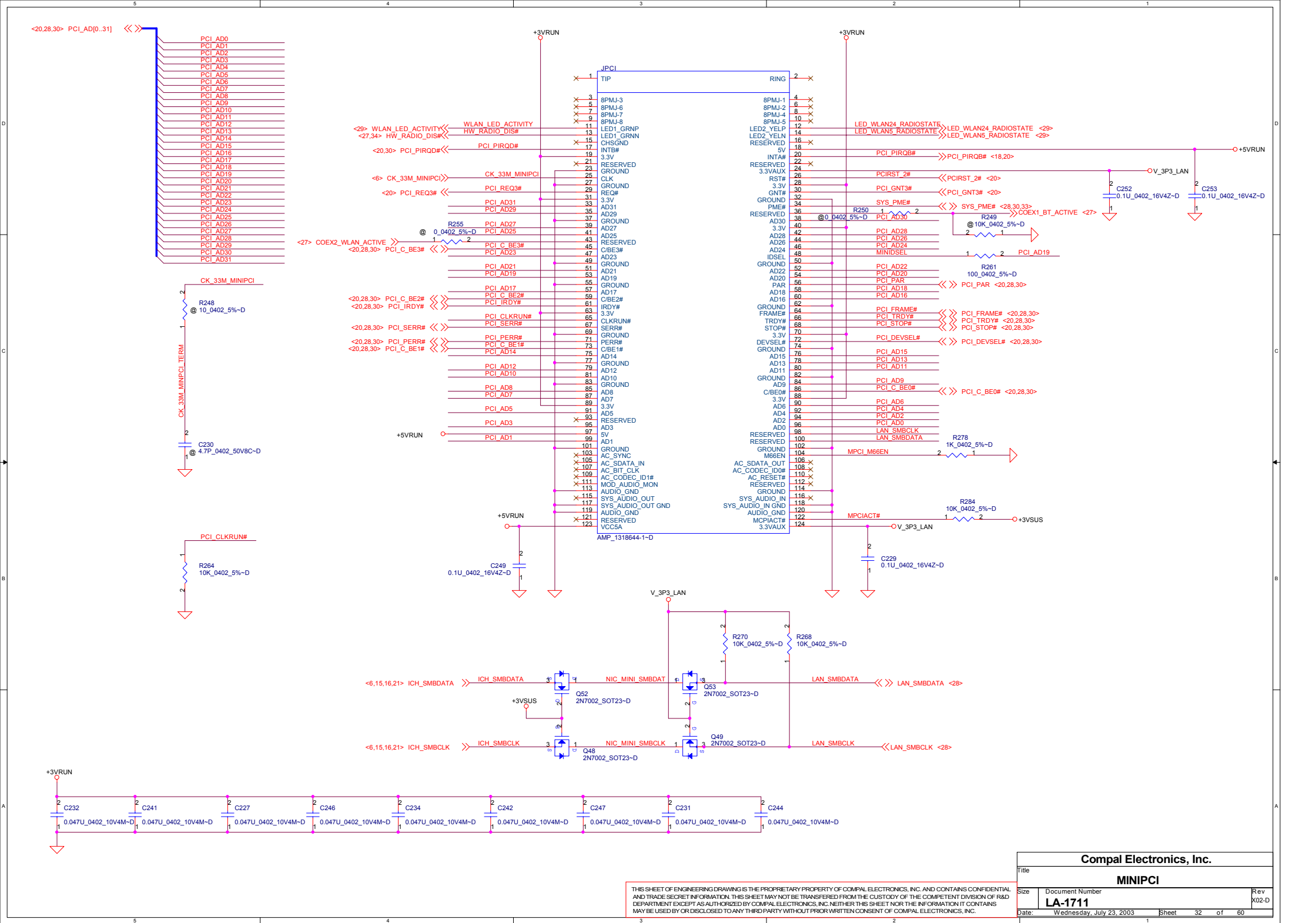
	Nimitz PCI4510	Beijing PCI7510
@	Depop	Depop
1@	Depop	Pop
2@	Pop	Depop

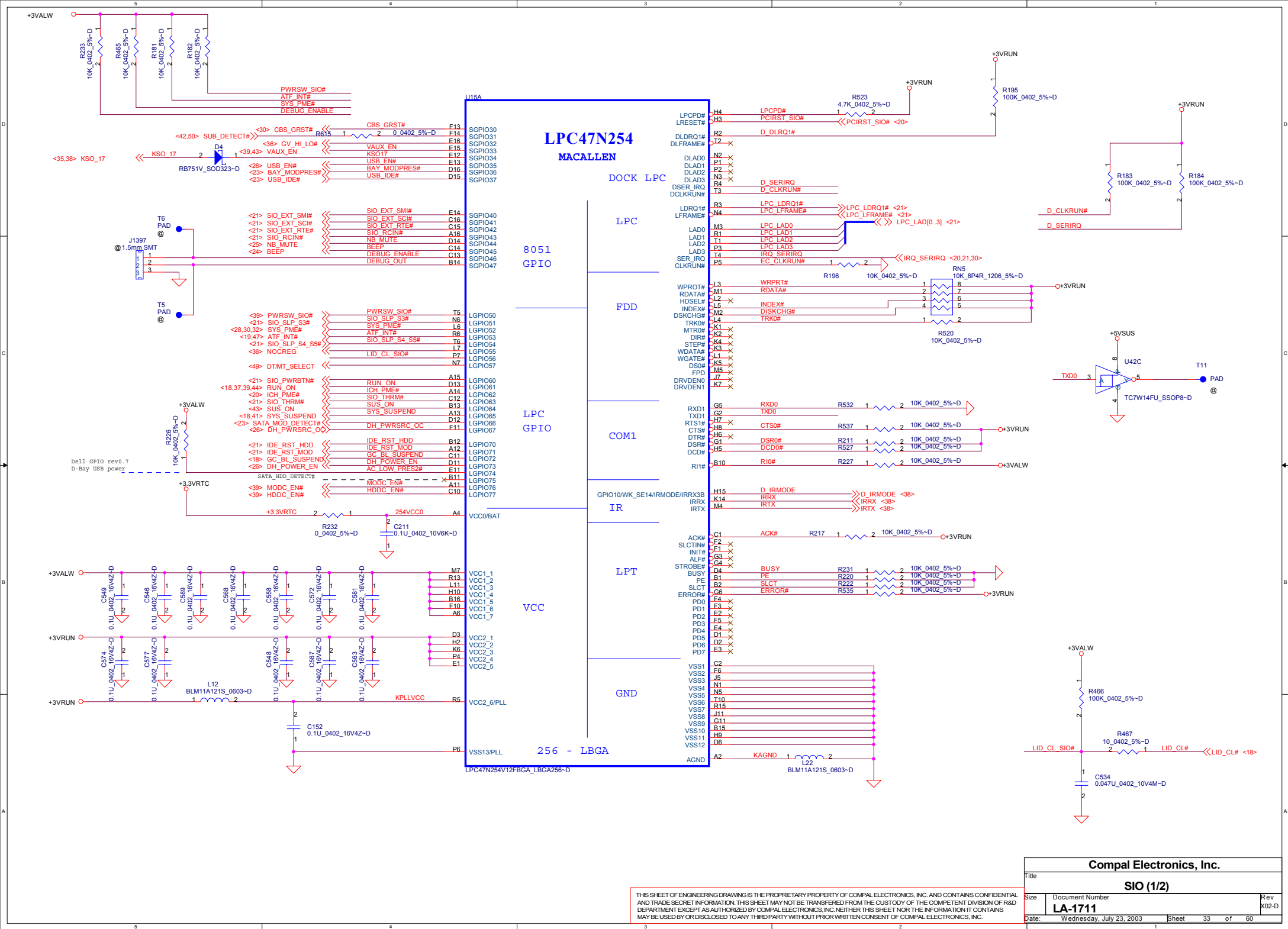


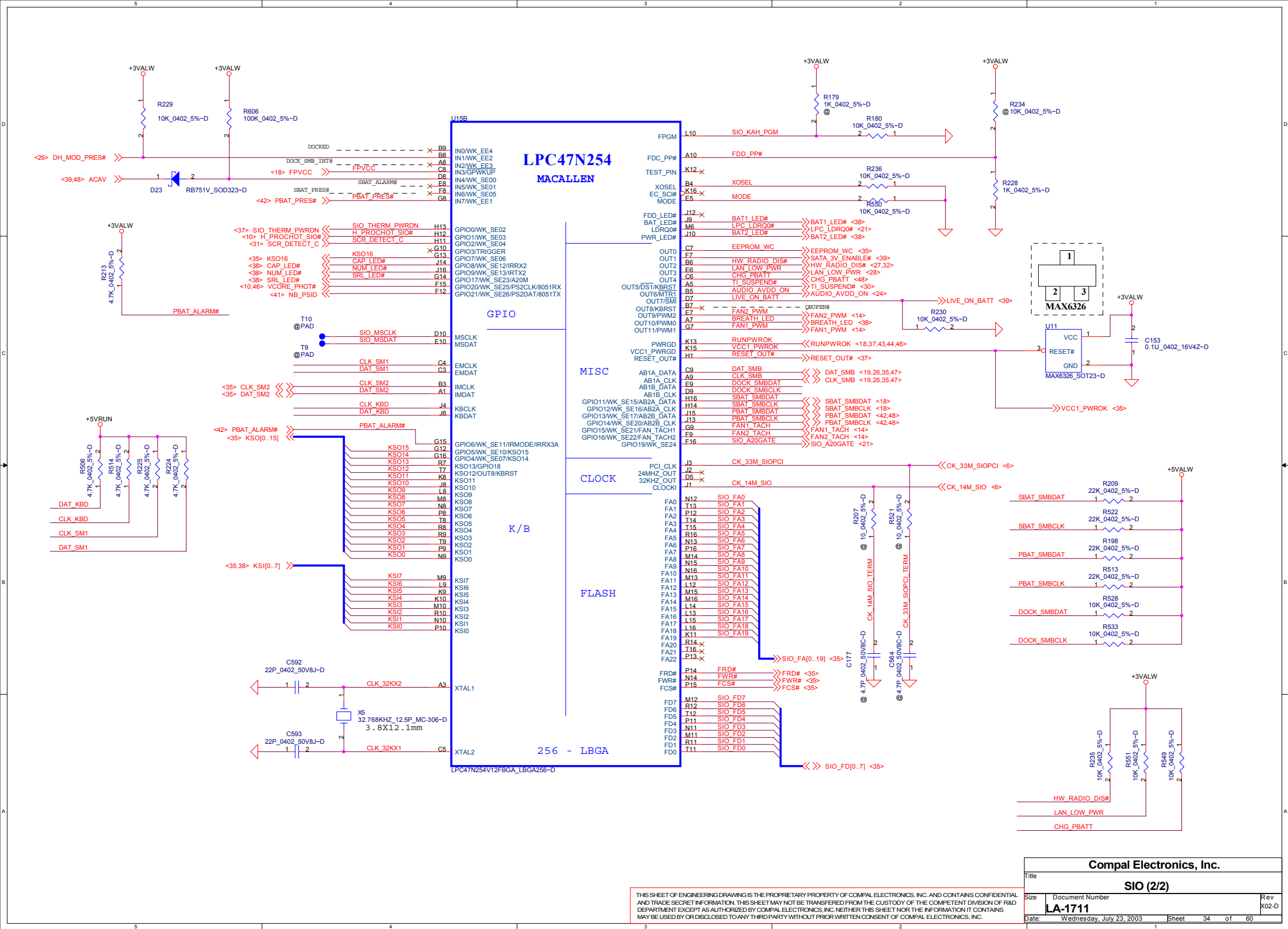
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1	0	1	
1	1	0	
1	1	1	
0	X	X	

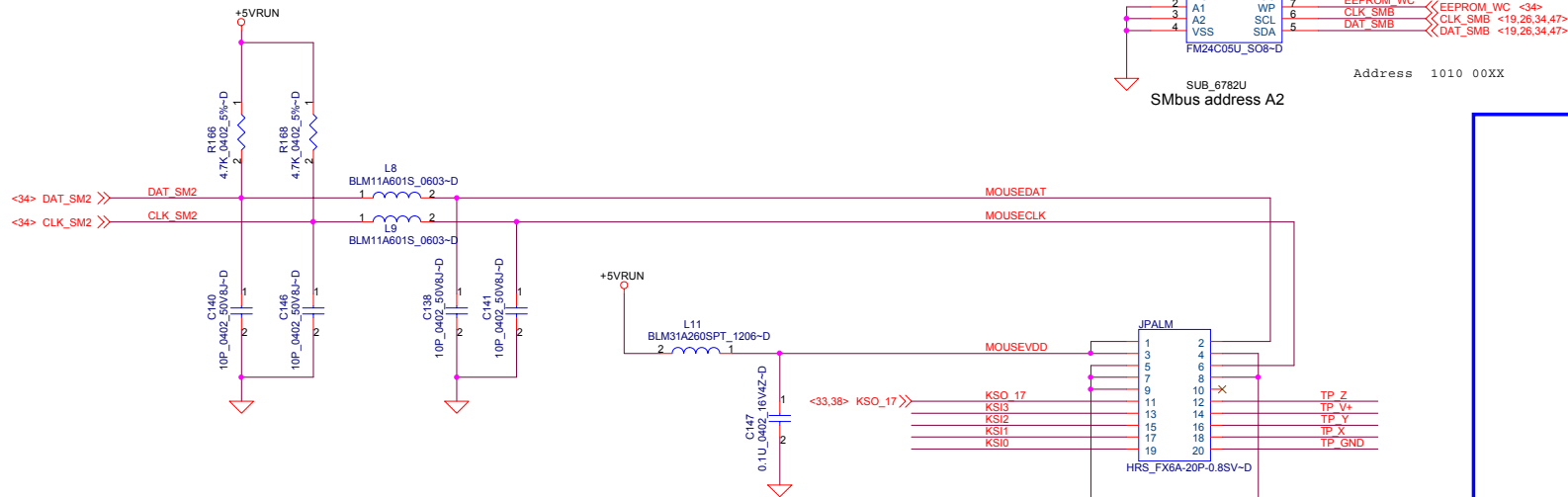
SHDN#	VCCD1#	VCCD0#	CBS_VCC
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1	1	1	
0	X	X	



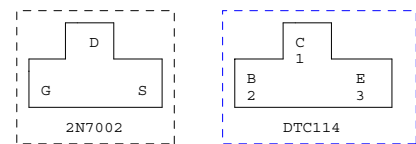
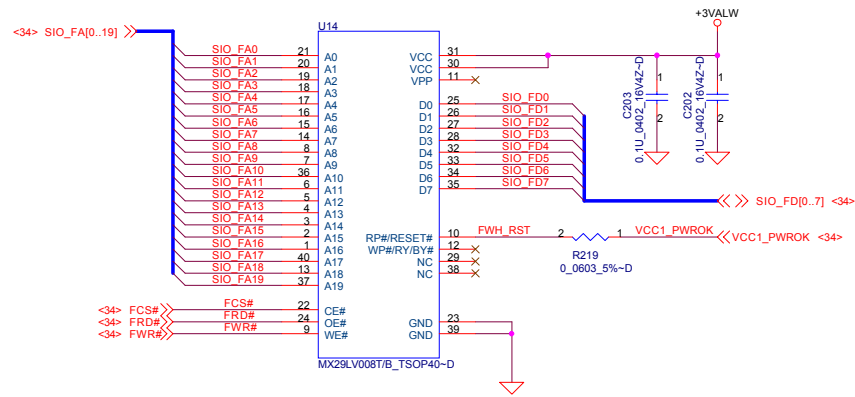
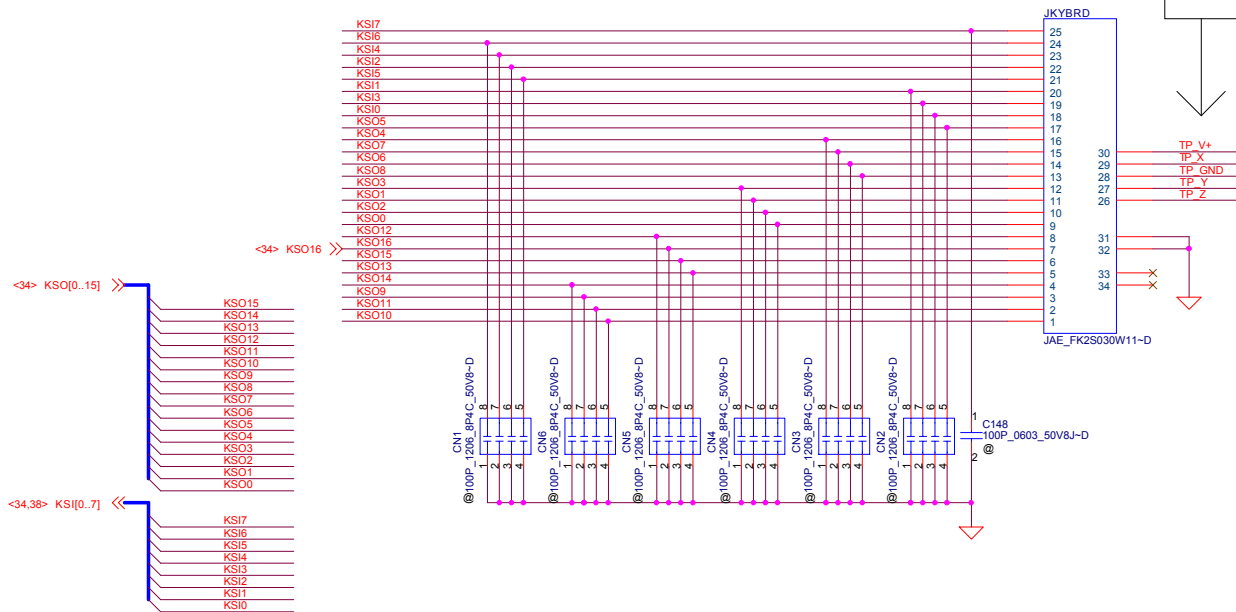
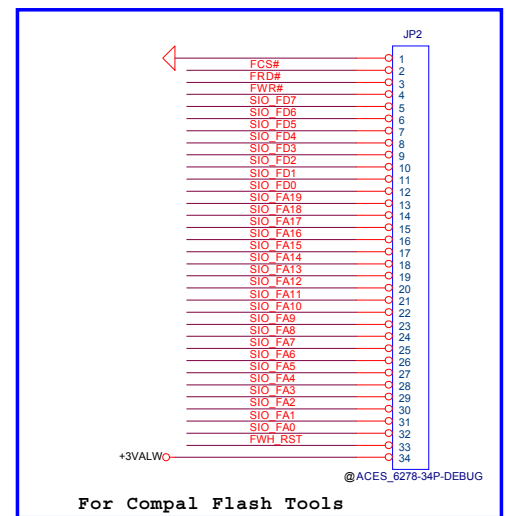








Keep no nosie coupled,
Especially the TP_GND

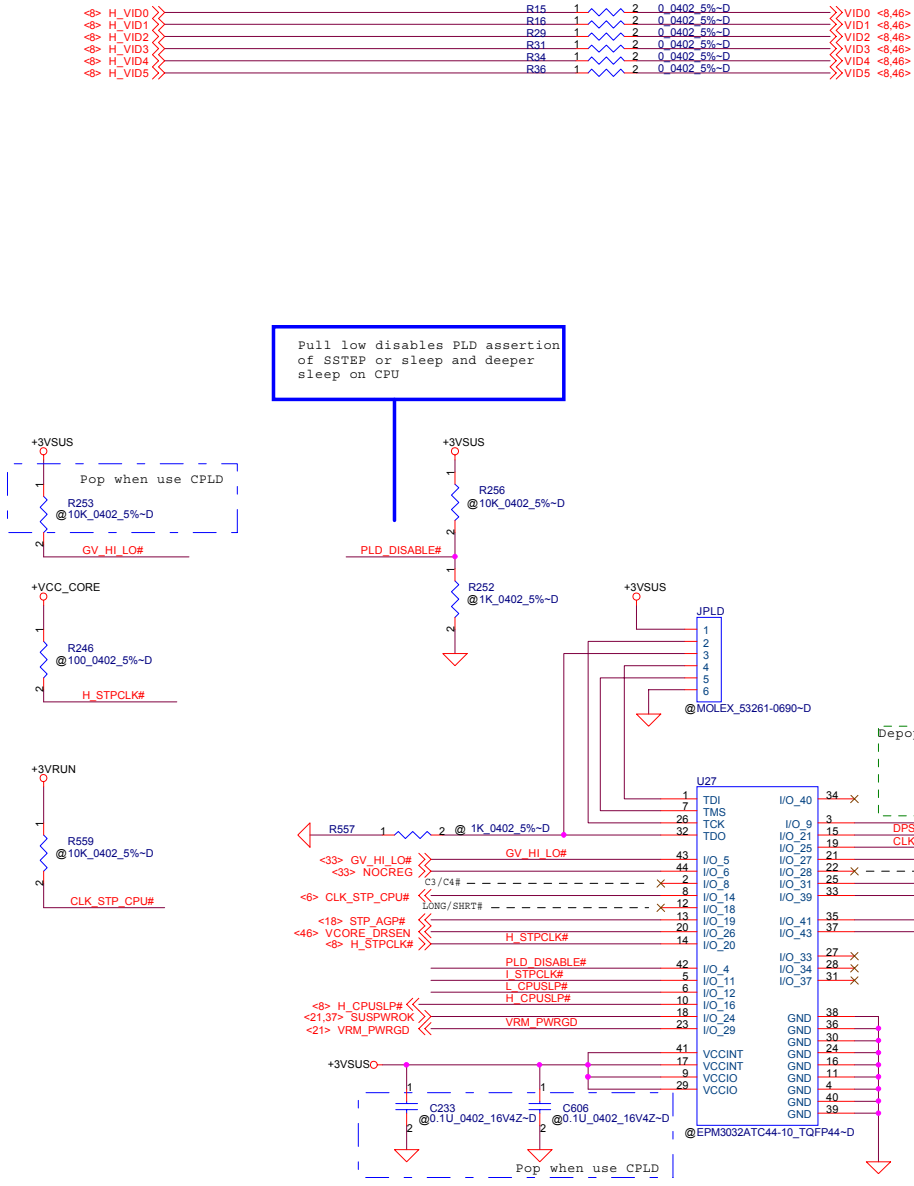


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INT KB & ROM			
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CPLD Function options Table

No.	Function	Speedstep enable	Speedstep disable
1	CPLD (U27)	Pop U27, C233, C606, R557,	Depop U27, JPLD, C233, C606, R557,
2	STPCLK# (From ICH to CPU)	Pop Q42, R254, Depop R259	Depop Q42, R254, Pop R259
3	CPUSLP# (From ICH to CPU)	Pop Q43, R561, Depop R251	Depop Q43, R561, Pop R251
4	VRMPWRGD (From Reset to ICH)	Depop R243	Pop R243
5	STP_AGP# (PLD to AGP)	Depop R96, Pop R98 (P.18)	Pop R96, Depop R98 (P.18)
6	CPUPREF# (From PLD to CPU)	Pop R380(P.8)	Depop R380 (P.8)
7	STPCPU_VR (From PLD to CPU Power)	Pop PR94, Depop PR95 (P.46)	Depop PR94, Pop PR95 (P.46)
8	DPRSLPVR (From PLD to CPU power)	Pop PR93, Depop PR92 (P.46)	Depop PR93, Pop PR92 (P.46)
9	PLD_WAKE# (From PLD to ICH)	Pop R141 (P.21)	Depop R141 (P.21)
10	PLD_DISABLE#	Pop R256, Depop R252	Depop R256, Pop R252
11	DPSLP#	Pop R76, R78(P.8)	Depop R76, R78(P.8)
12	PCI_PCIRST#(From ICH to PLD)	Pop R245	Depop R245
13	GV_HI_LO#	Pop R253	Depop R253

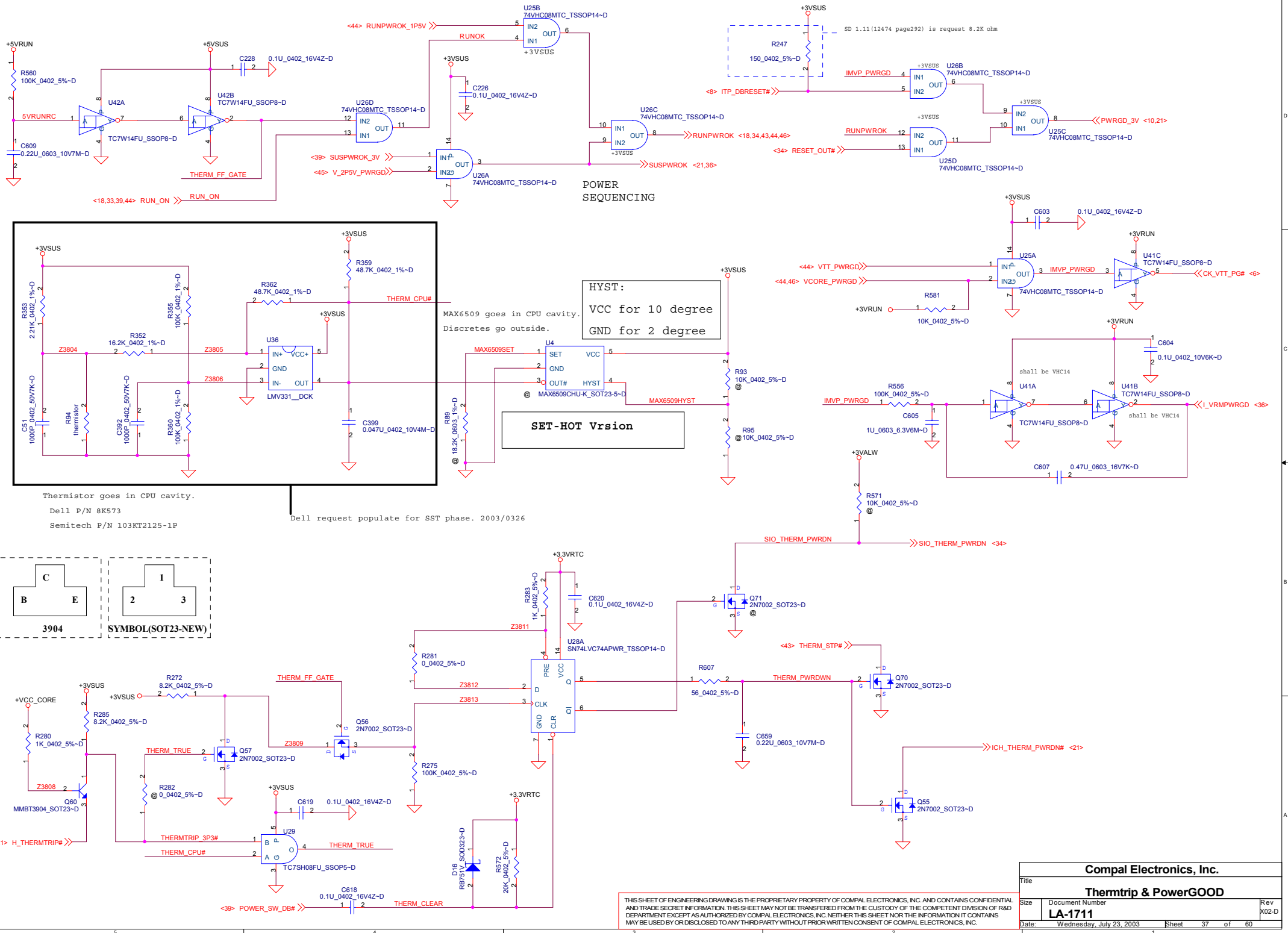


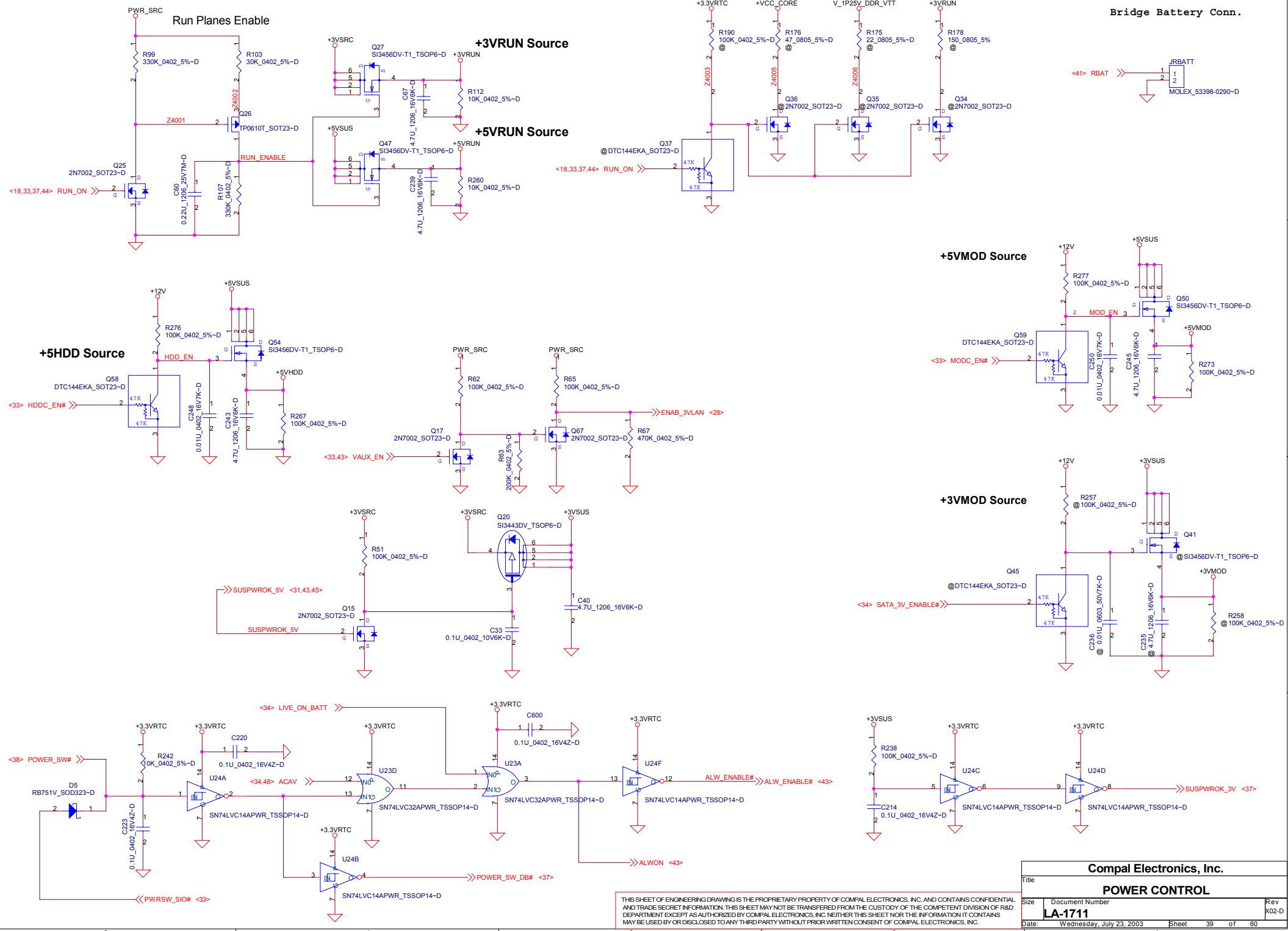
C
1
B 2 3 E

DTC114TKA

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PLD			
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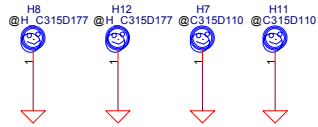
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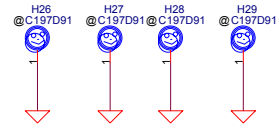


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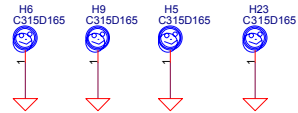
CPU screw hole



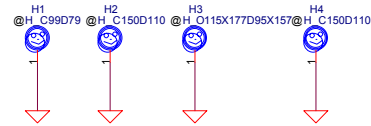
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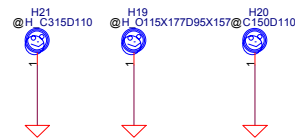
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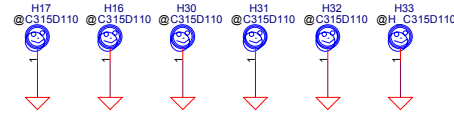
Others screw hole



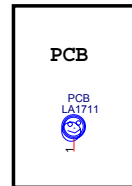
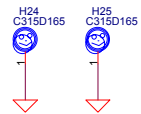
VGA Conn. screw hole



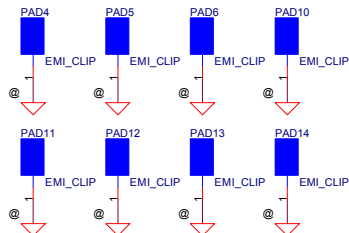
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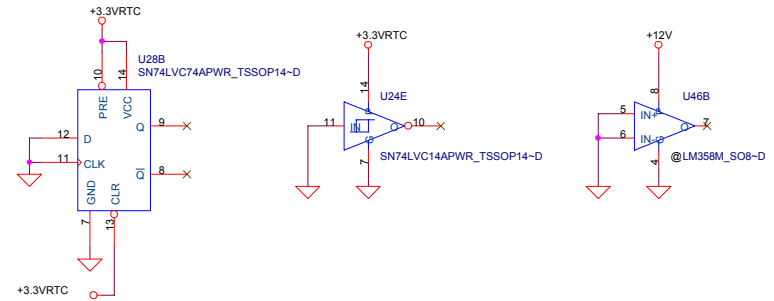
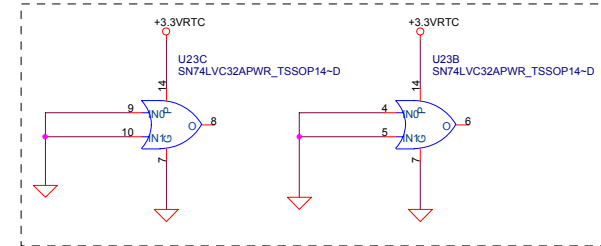
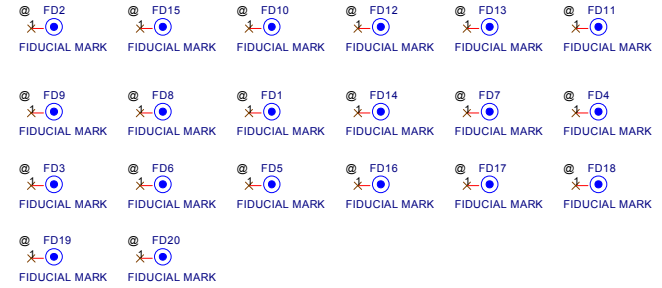
FAN Conn. screw hole

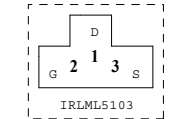
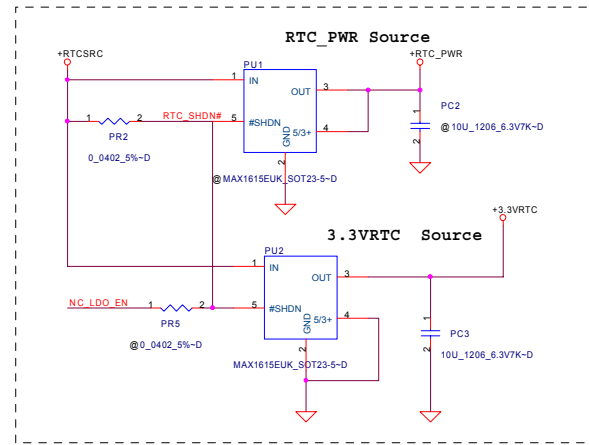
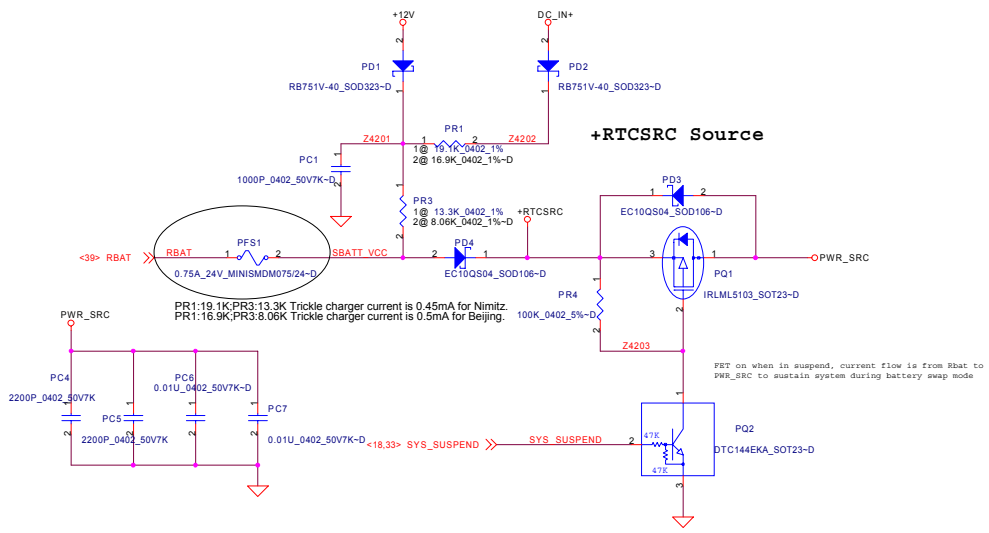


EMI Cilps

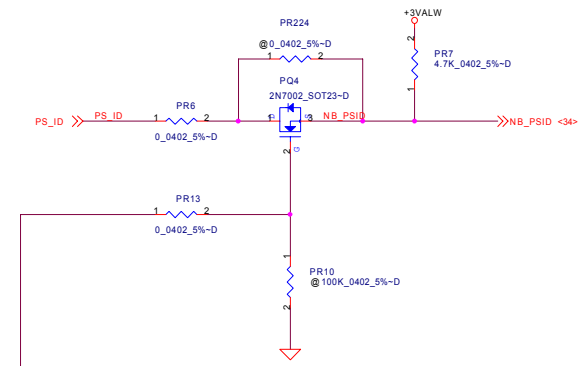
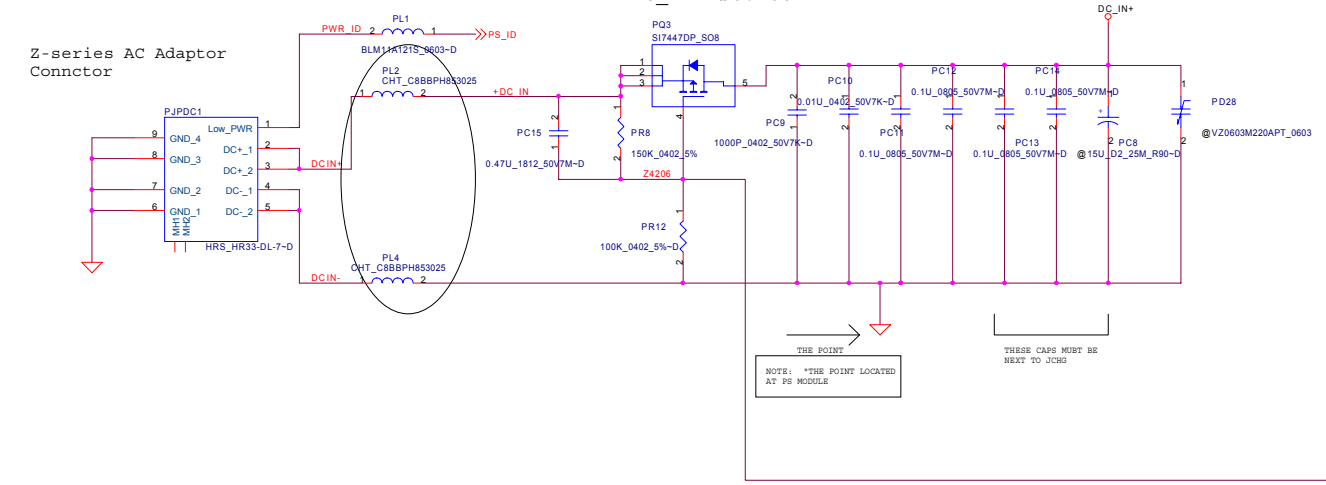


Fiducial Mark



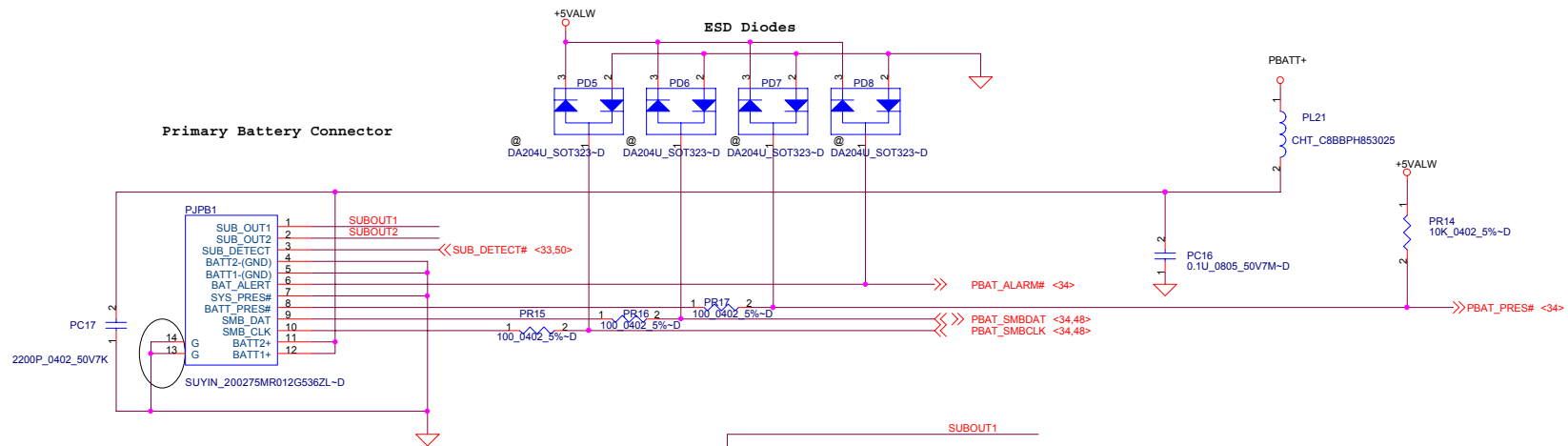


Z-series AC Adaptor Connector

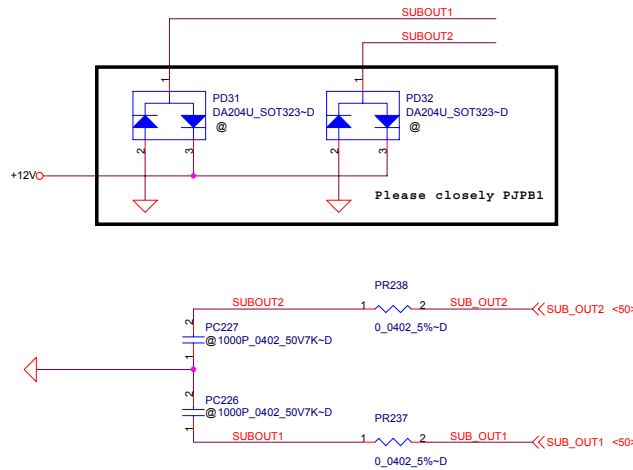
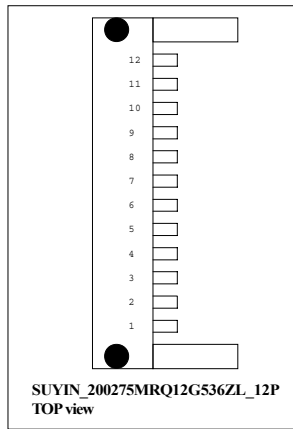


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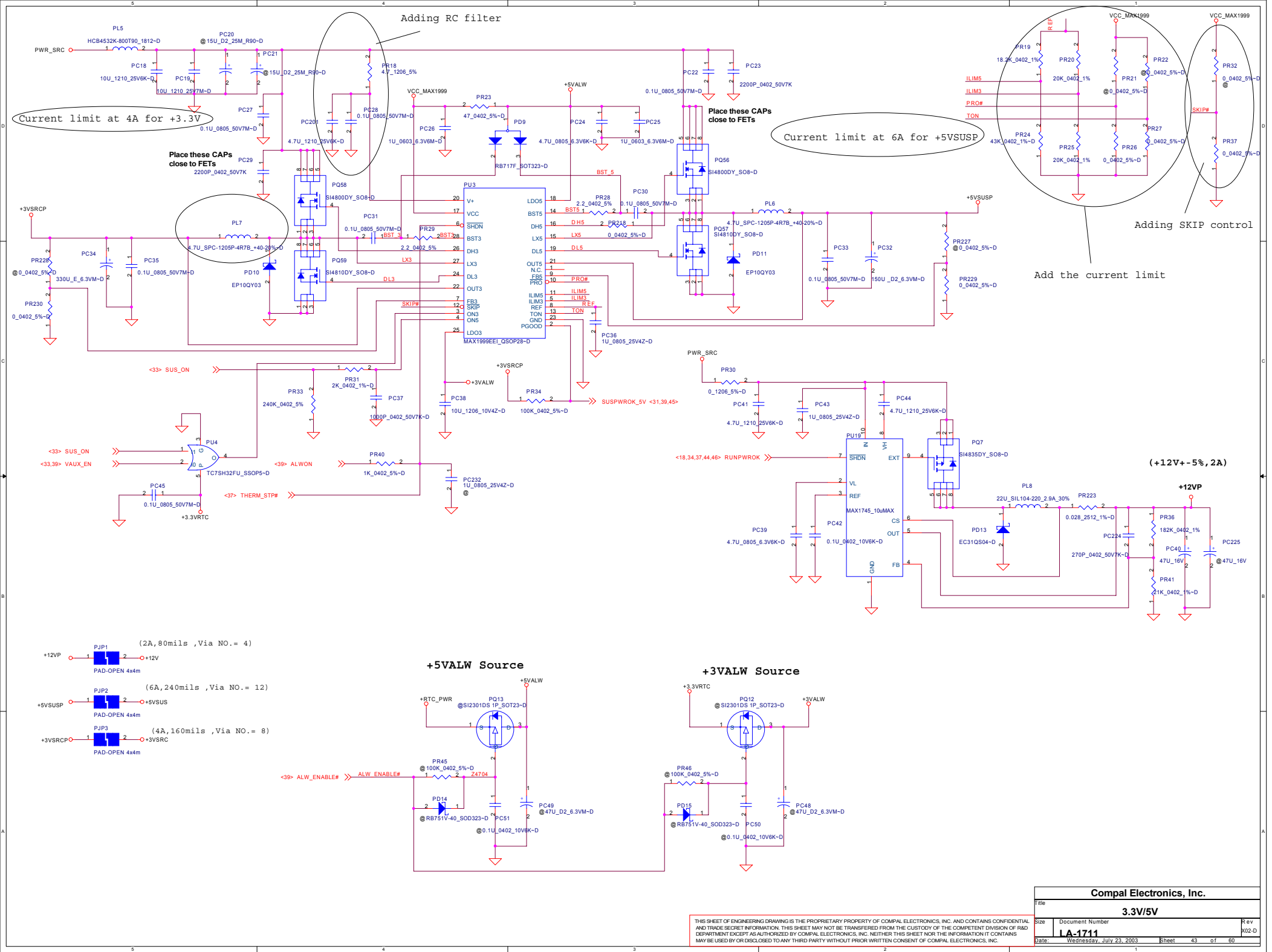


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THE POINT →

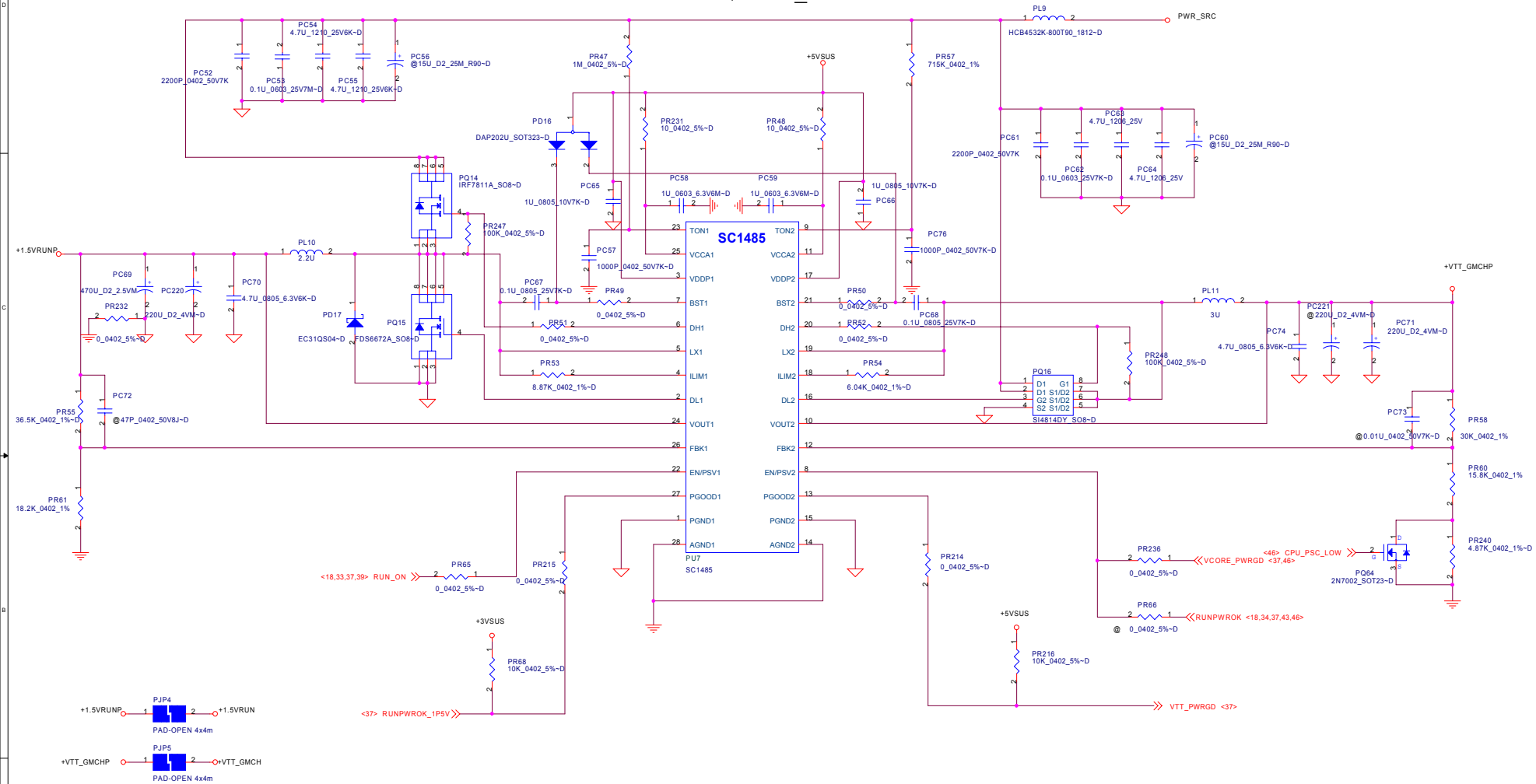


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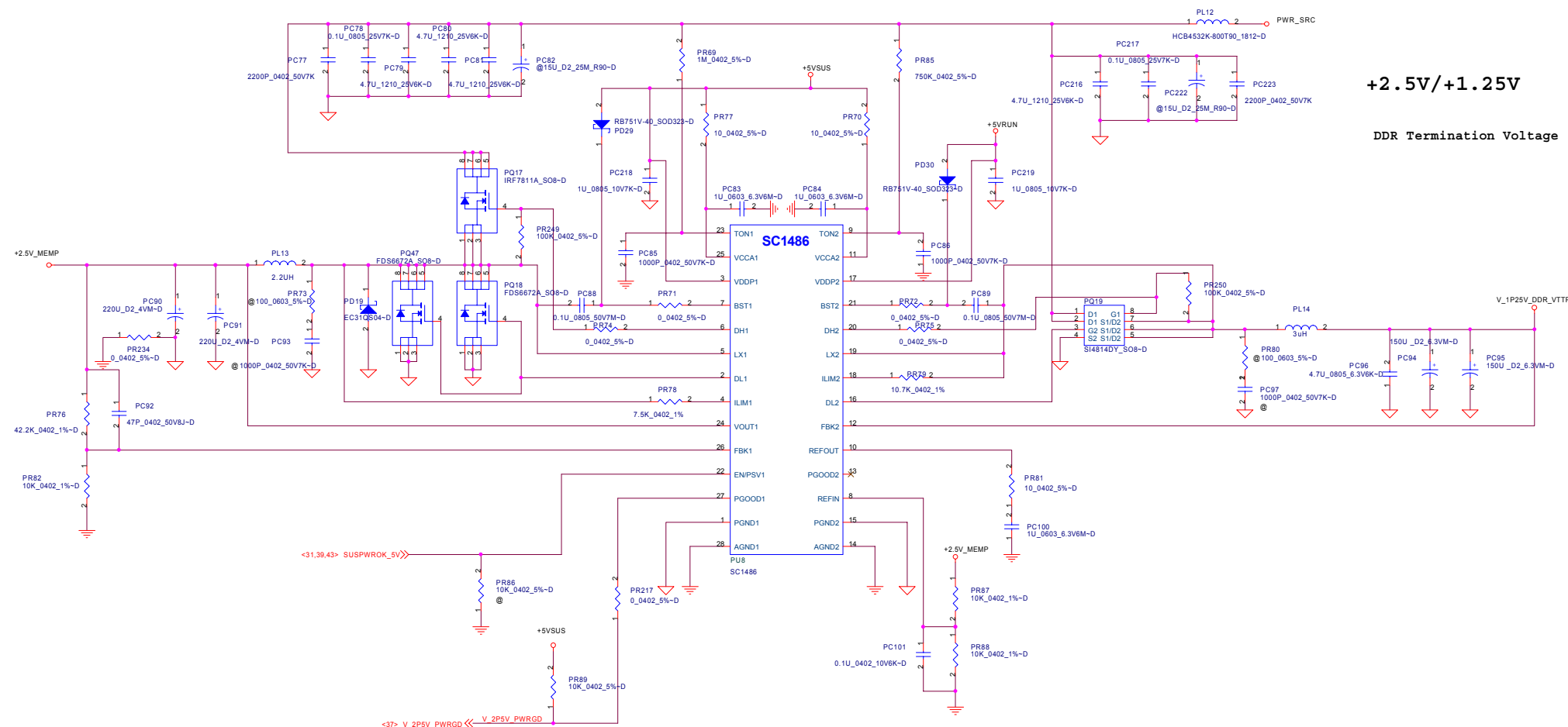
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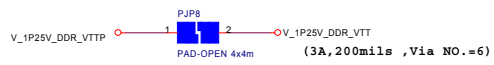
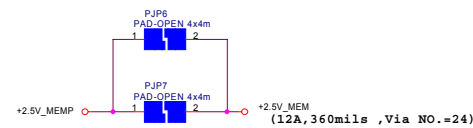
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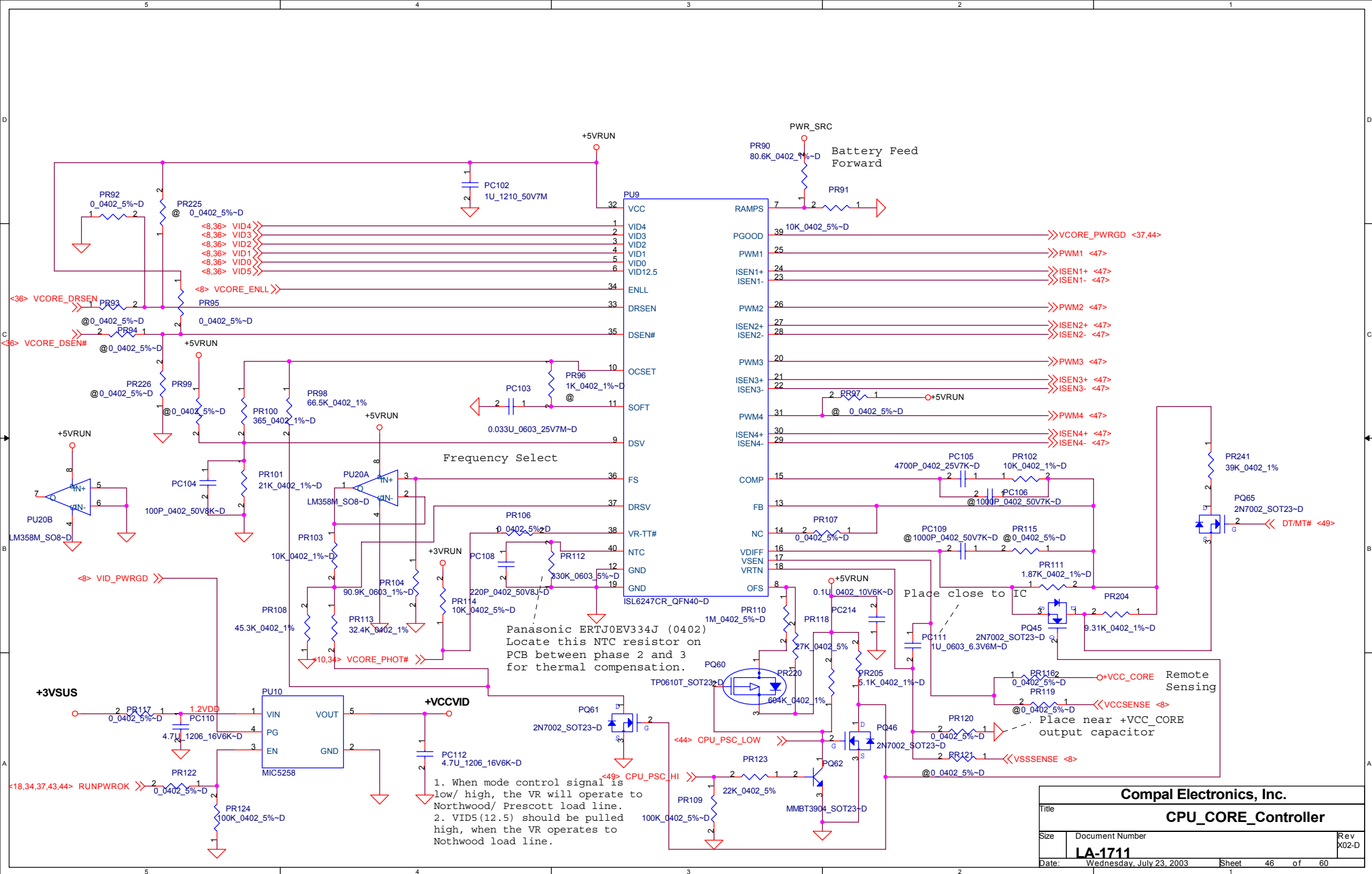


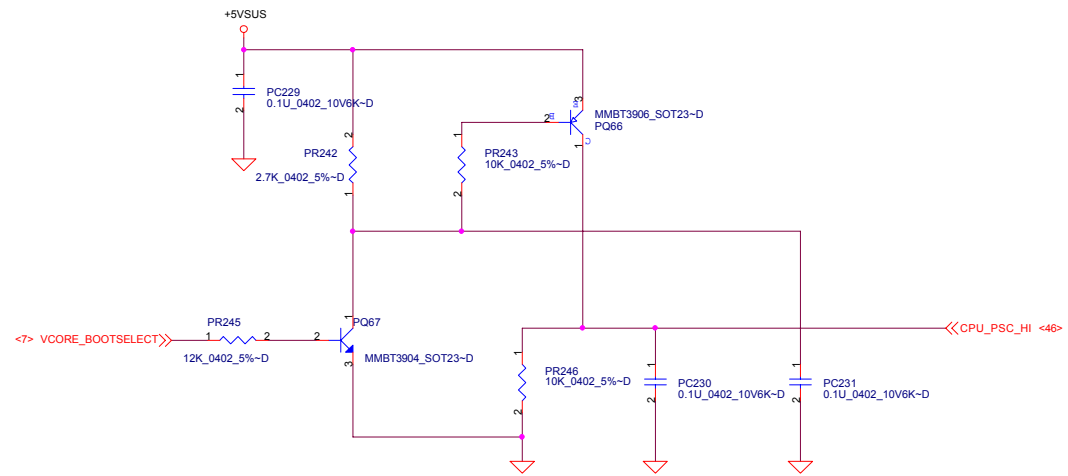
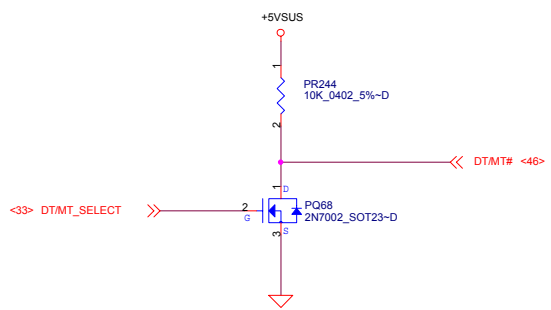
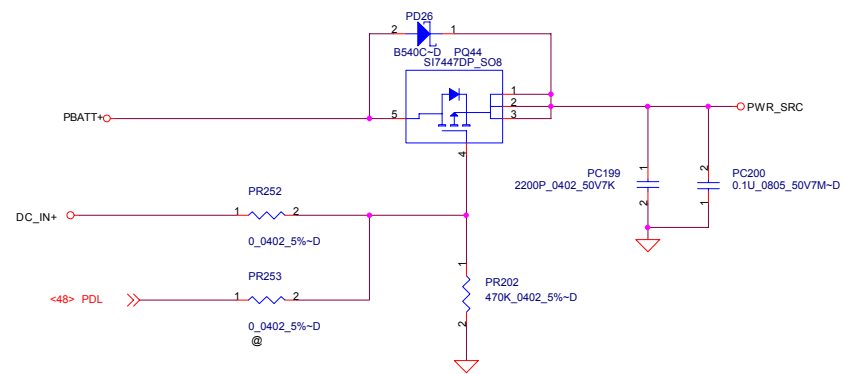
+2.5V/+1.25V
DDR Termination Voltage



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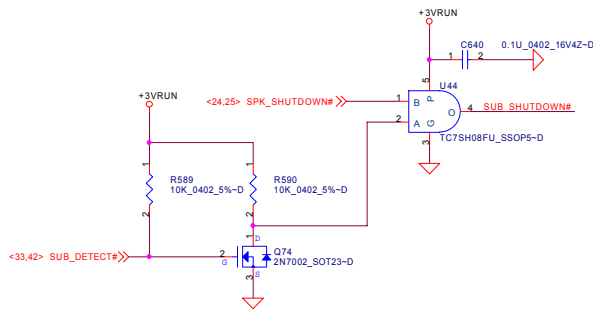
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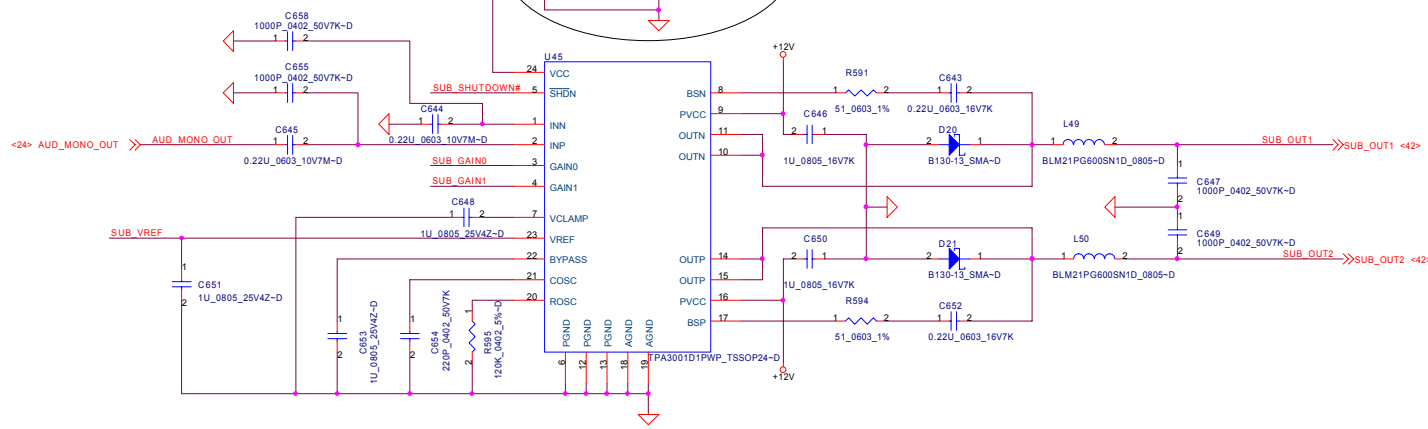
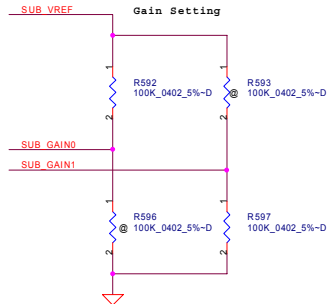
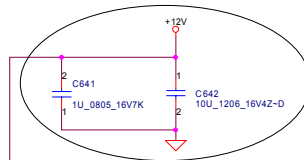


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