

Compal confidential

Schematics Document

ClawHammer AMD K8 with nVIDIA Chrush K8

2003-10-15

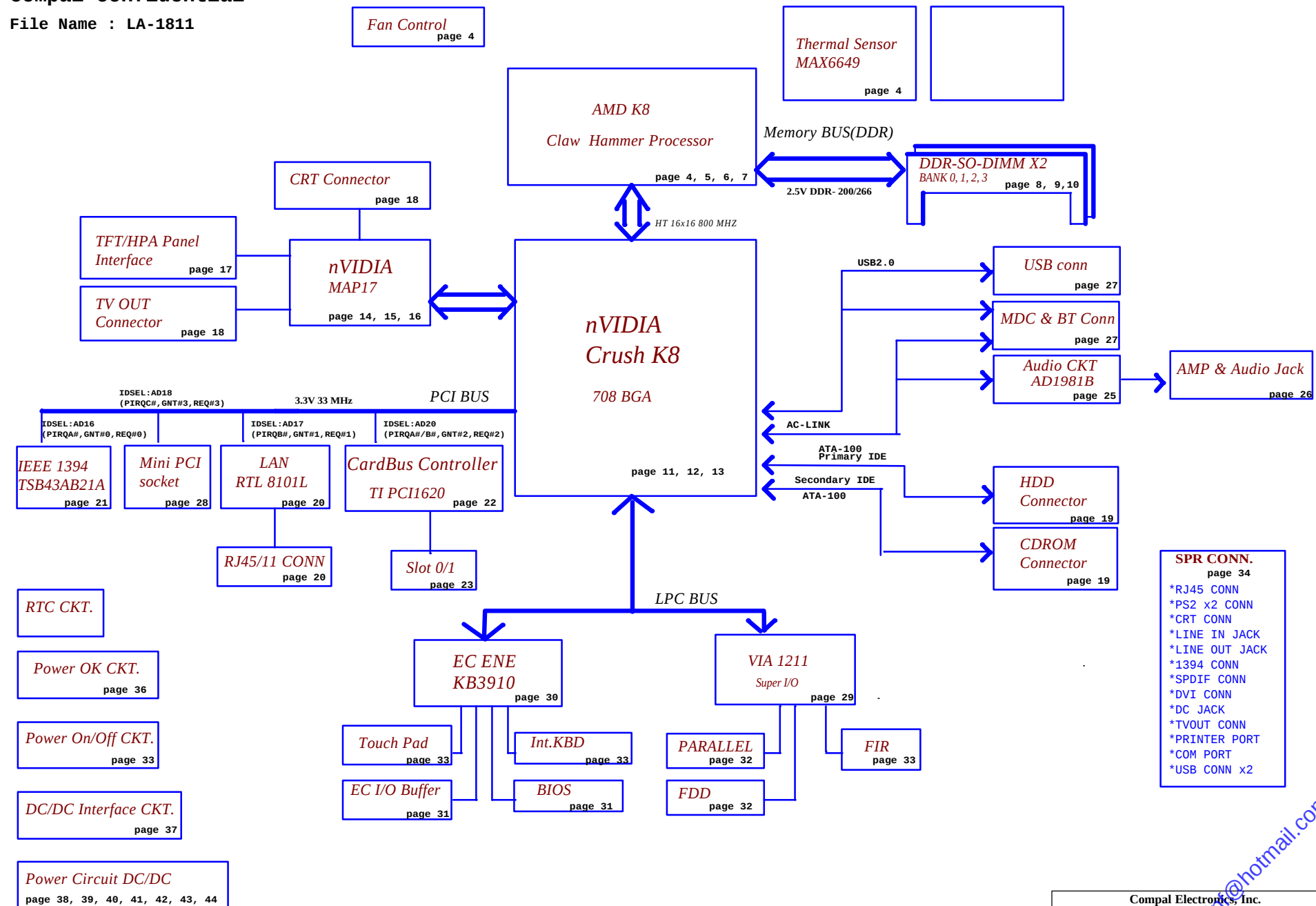
REV:0.5

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Title			
Cover Sheet			
Doc No	Document Number	Rev	
	LA-1851	0.5	
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he@mail@hotmail.com

File Name : LA-1811



Voltage Rails

power plane State	+1.2VALW +3VALW +5VALW 12VALW	+1.25V +2.5V +3V +5V	+1.2V_HT +1.2VS +1.5VS +2.5VS +3VS +5VS
S0	0	0	0
S1	0	0	0
S3	0	0	X
S5 S4/AC	0	X	X
S5 S4/AC don't exist	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
--------	---------------	---------	-----------	------

INTERNAL

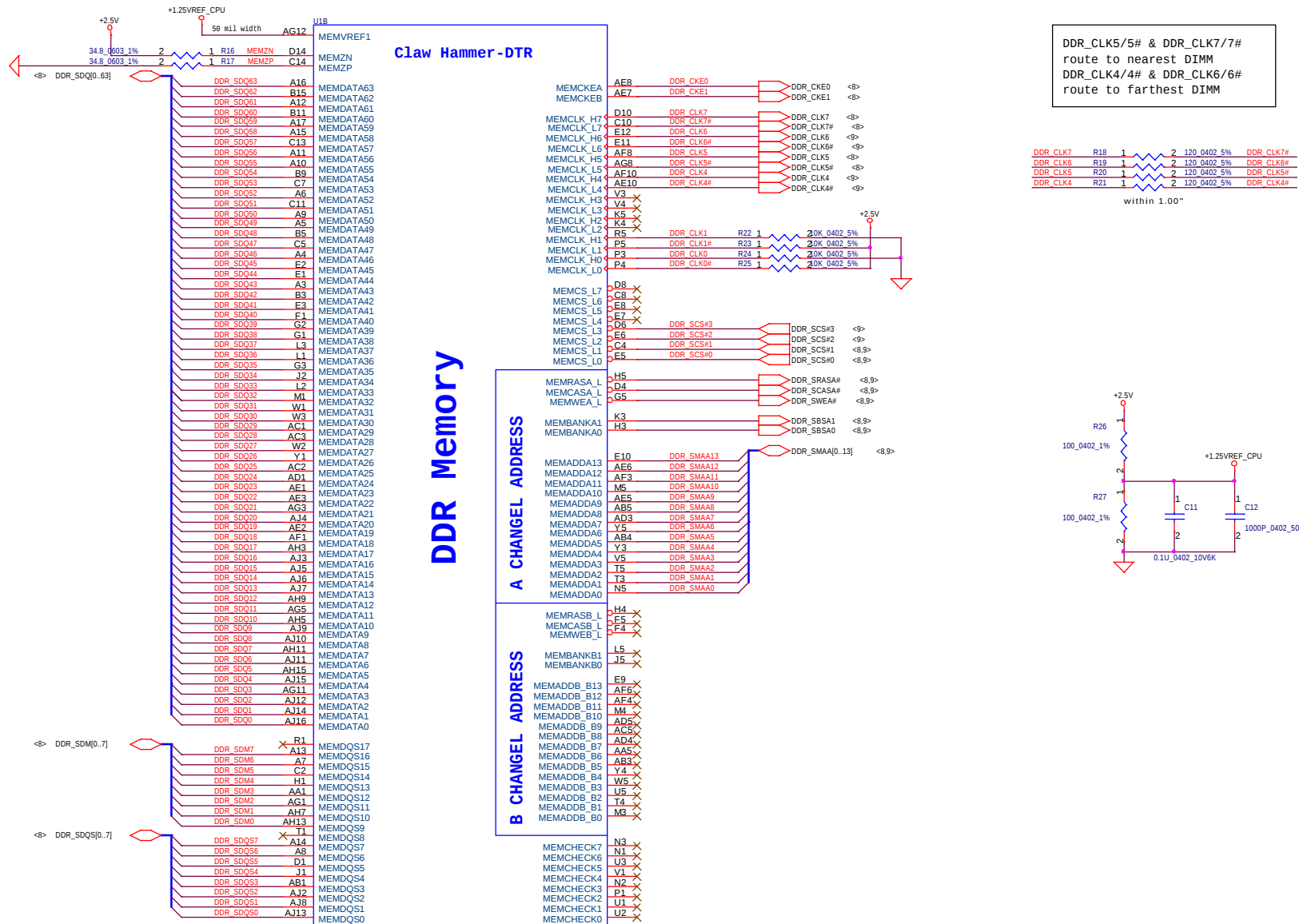
USB 2.0	2	AD13	N/A	G
AC97 MODEM	6	AD17	N/A	M
AC97	6	AD17	N/A	L
ATA 100	8	AD20	N/A	
ETHERNET	5	AD16	N/A	K
LPC I/F	1	AD12	N/A	
SMBUS	1	AD12	N/A	F

EXTERNAL

VGA	0	AD16	N/A	E
1394	0	AD16	0	A
LAN	1	AD17	1	B
CARD BUS	4	AD20	2	A, B
Wireless LAN	2	AD18	3	C
Mini-PCI (no use)	3	AD19	4	D

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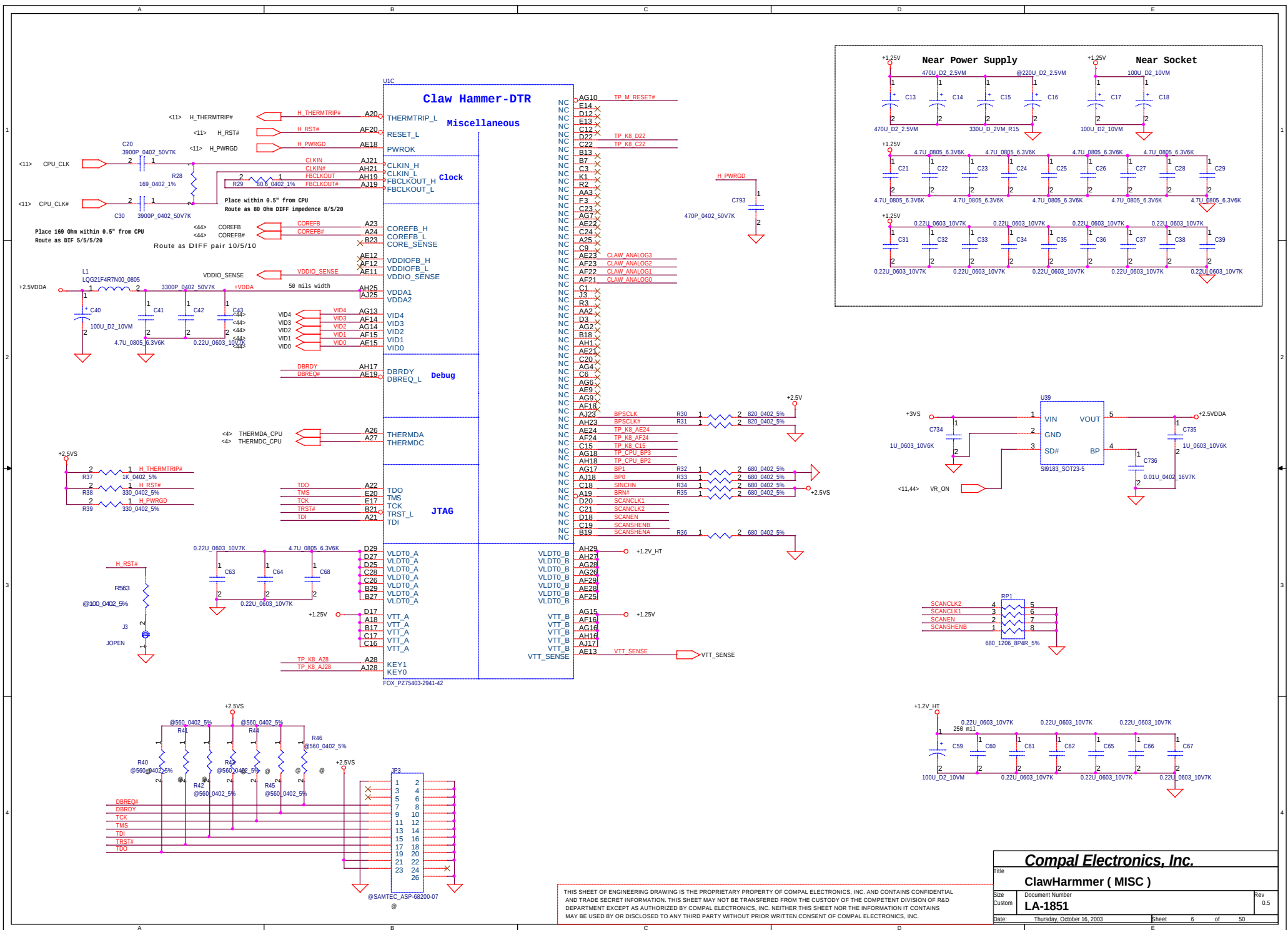
Compal Electronics, Inc.			
Title		Notes List	
Rev	Document Number	Rev	
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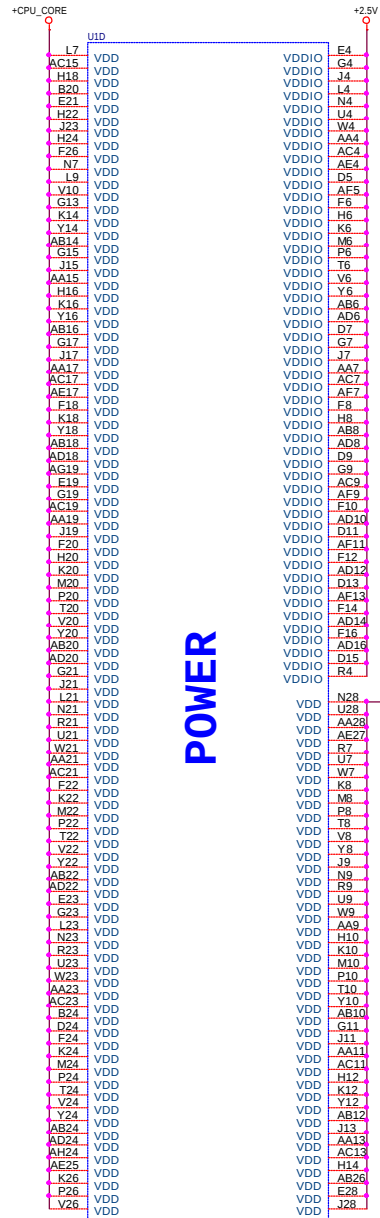
Compal Electronics, Inc.			
Claw Hammer (MEMORY BUS)			
Title	Document Number	Rev	
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POWER

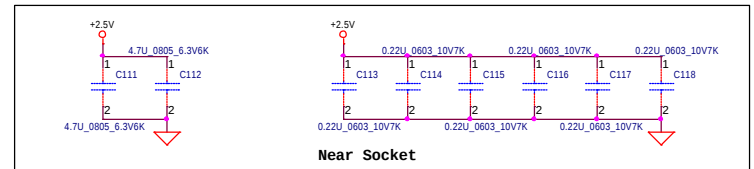
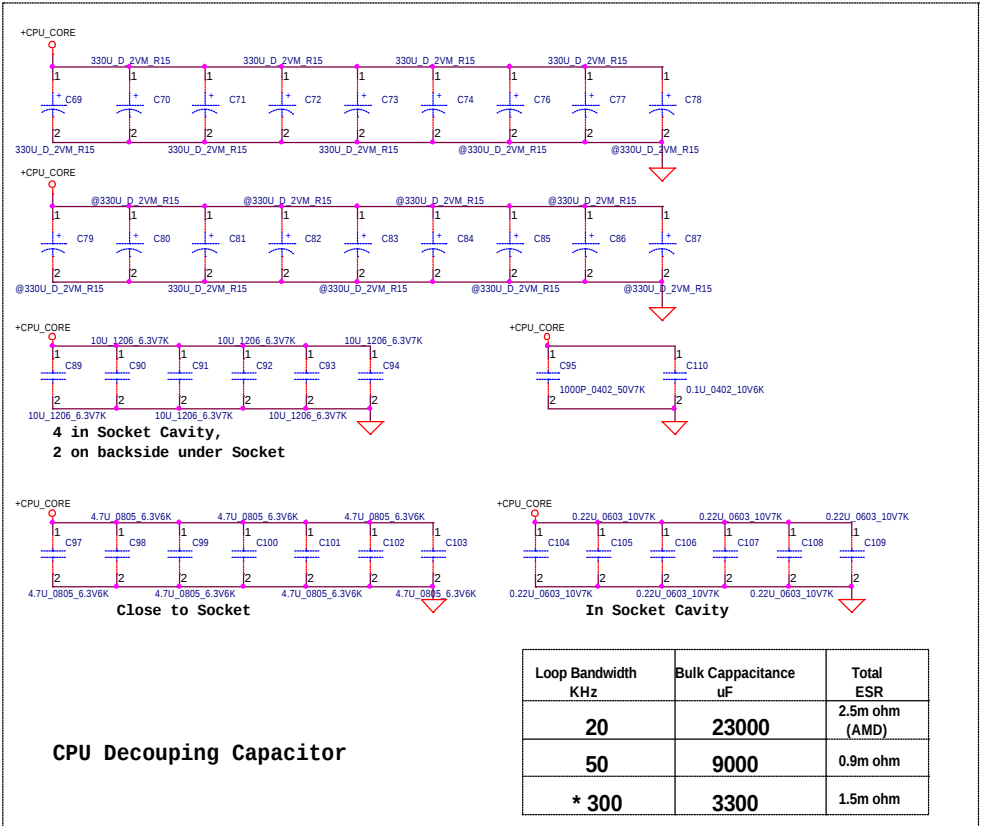
POWER



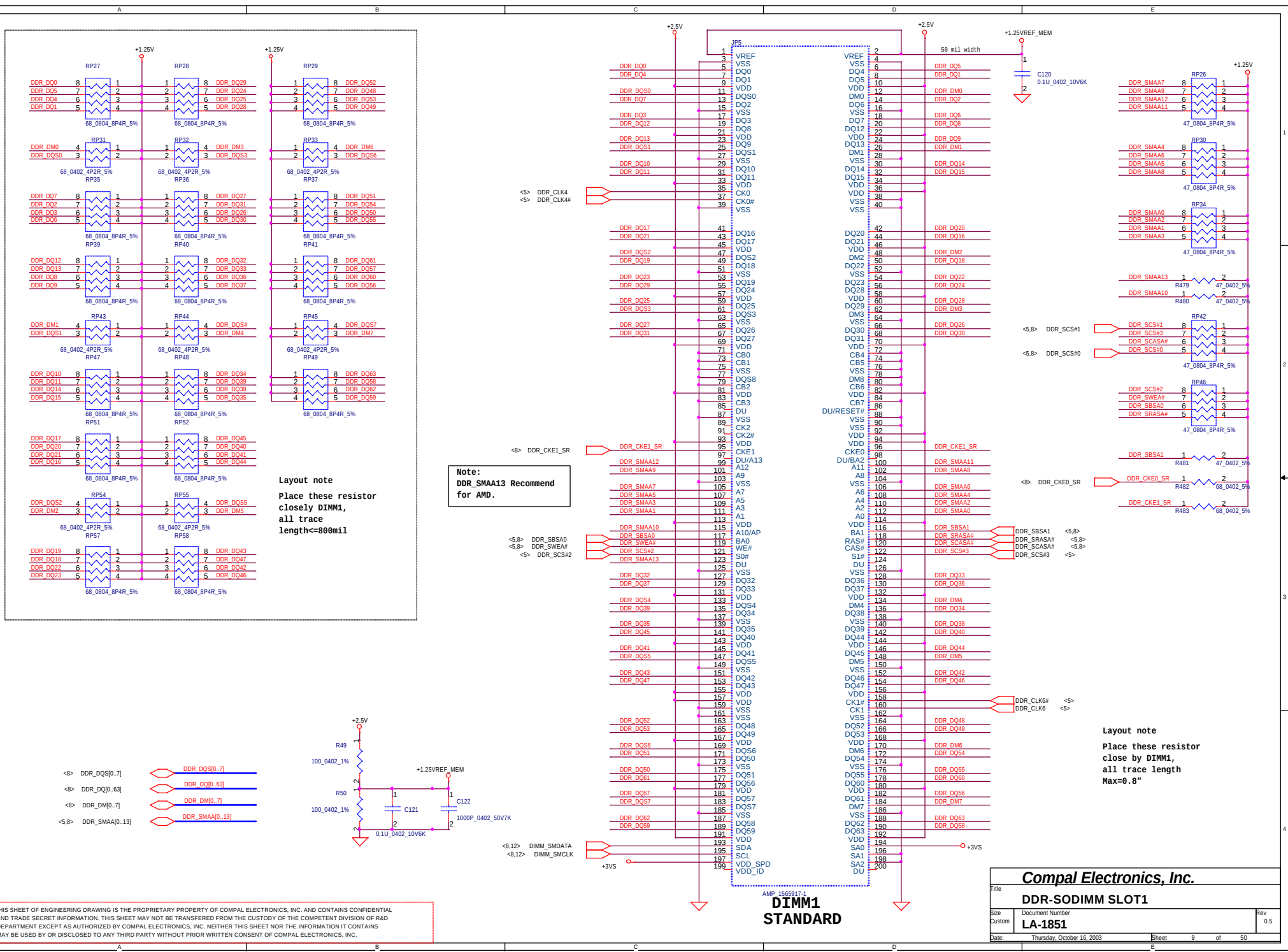
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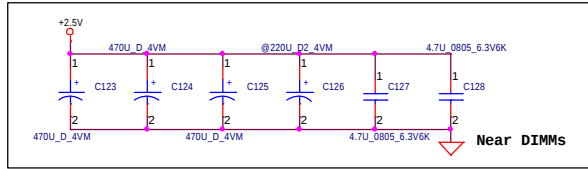


Compal Electronics, Inc.		
Claw Hammer (Power & Ground)		
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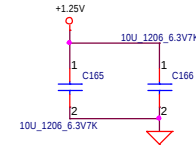
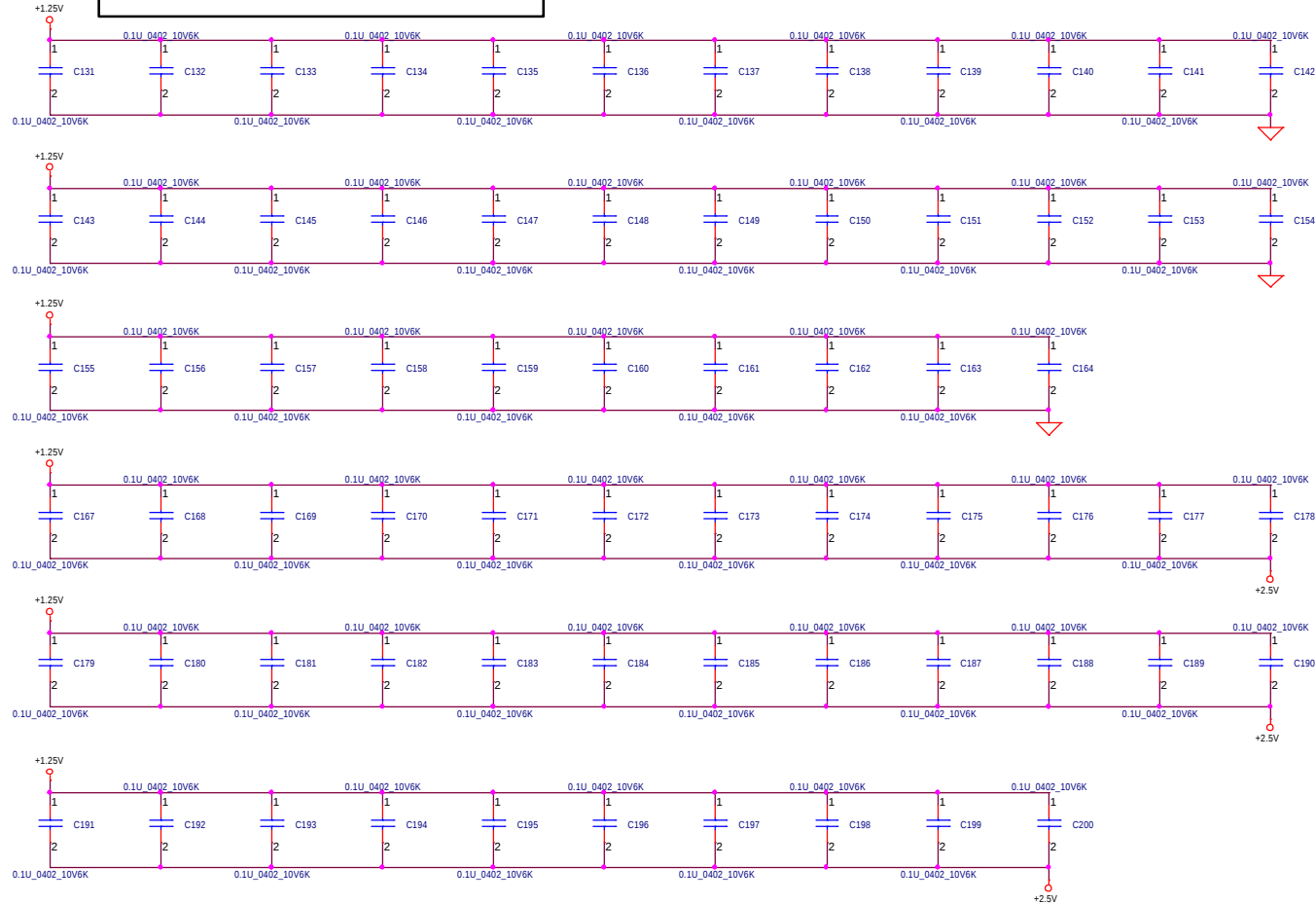


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Compal Electronics, Inc.			
DDR-SODIMM SLOT1			
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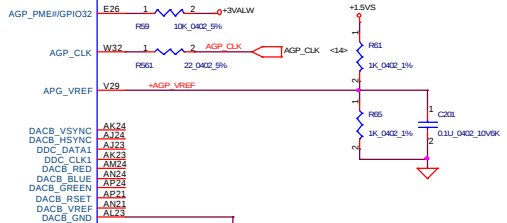
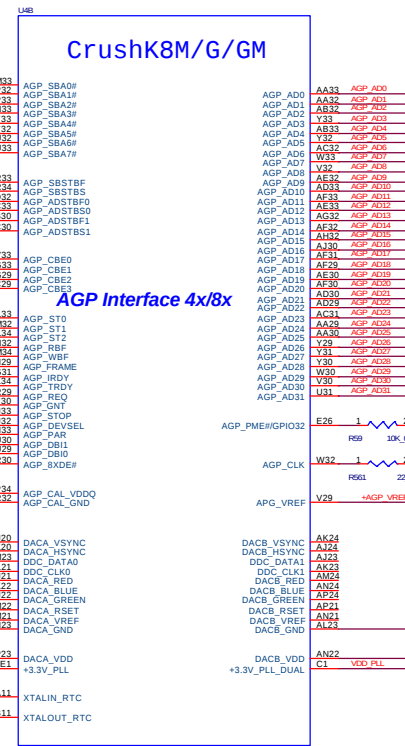
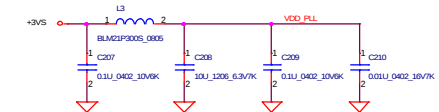
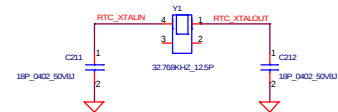


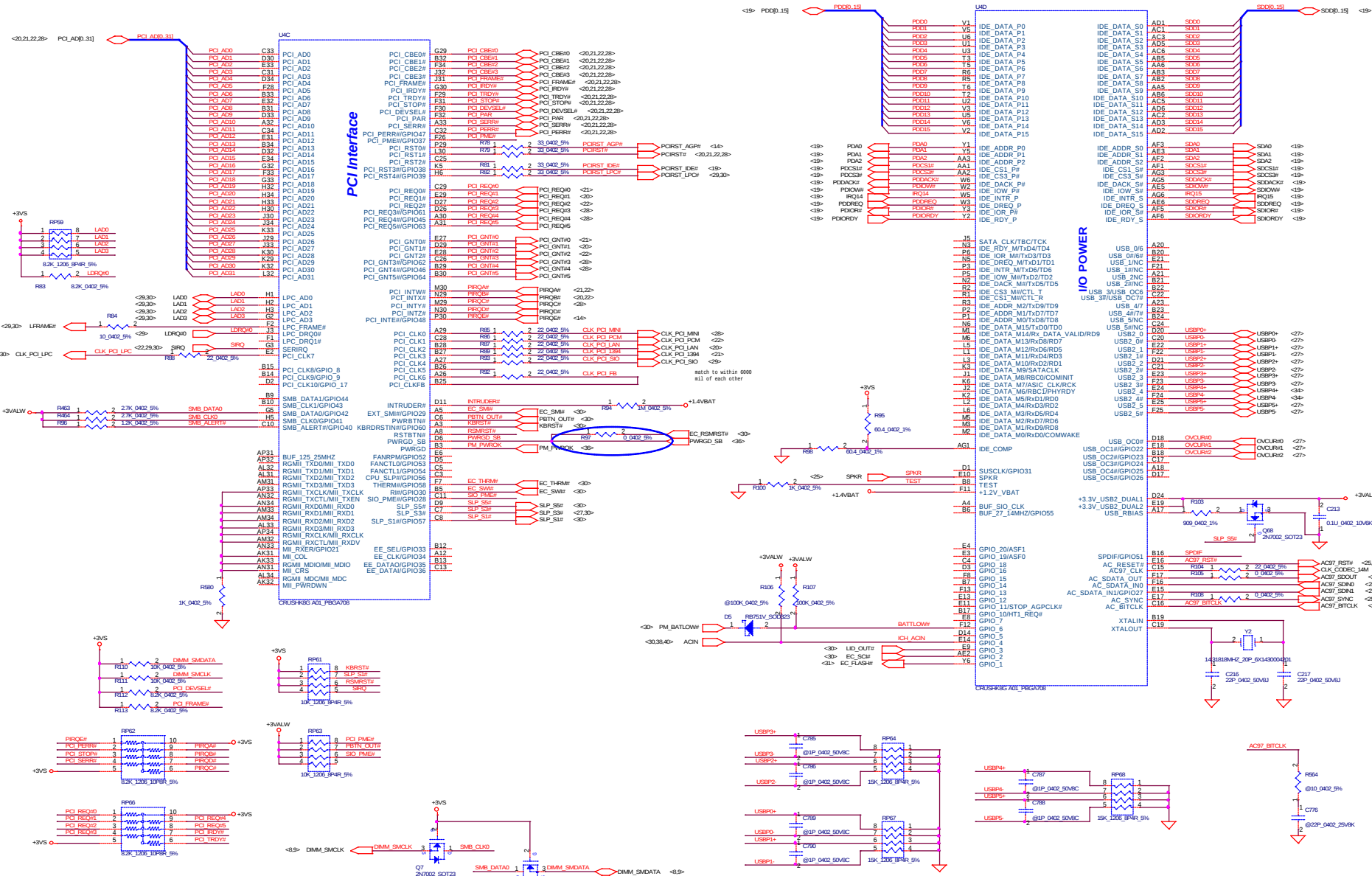
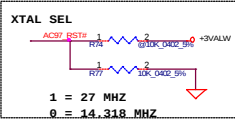
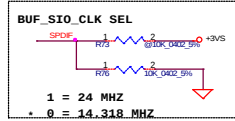
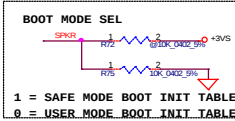
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS



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Title			
DDR SODIMM Decoupling			
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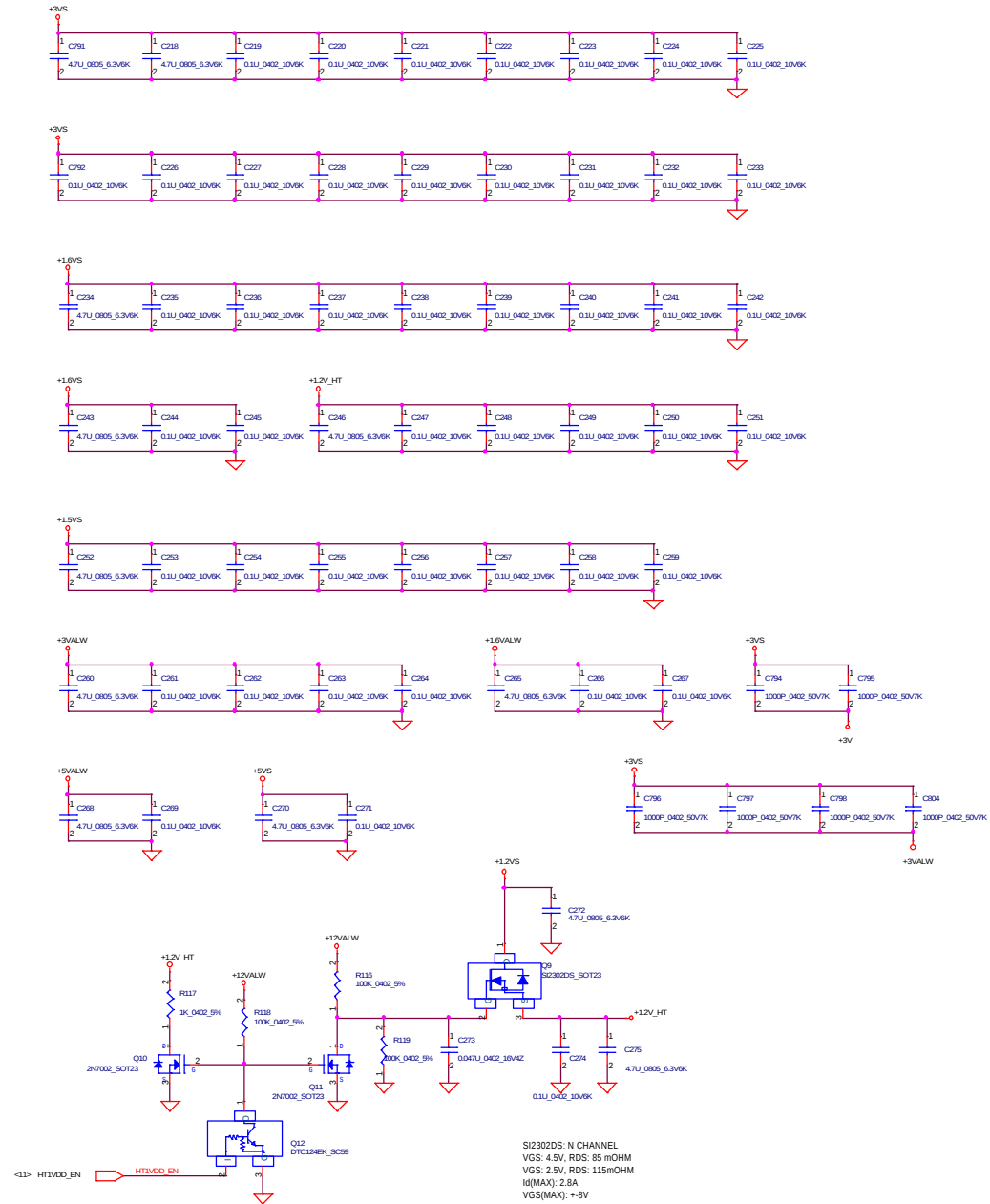
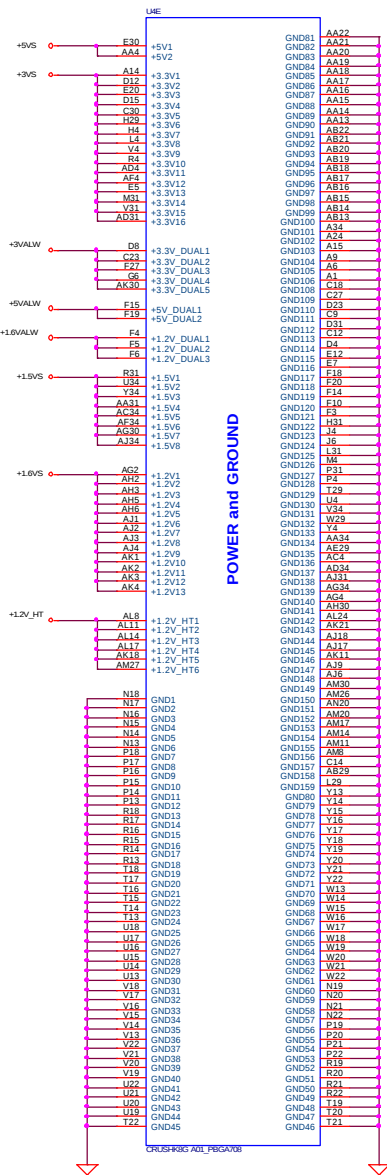




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nVIDIA CrushK8 (PCI & IDE & USB & MISC)
LA-1851

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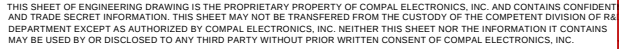
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nVIDIA CrushK8 (Power & Ground)

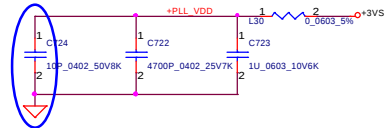
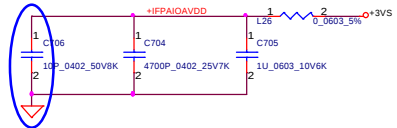
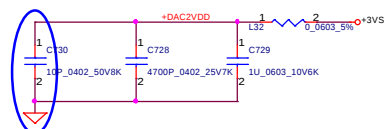
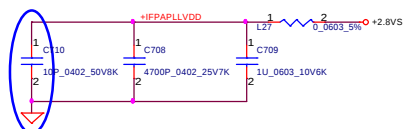
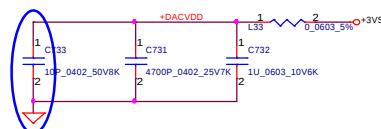
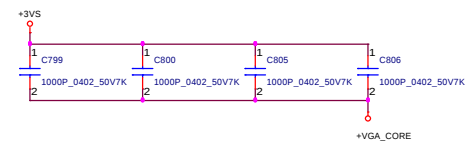
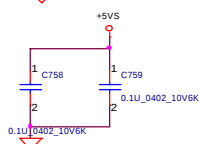
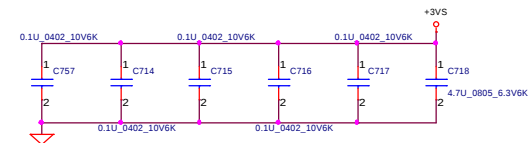
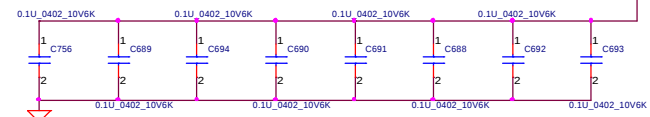
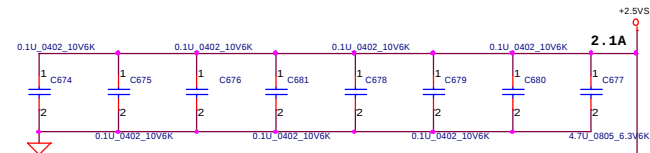
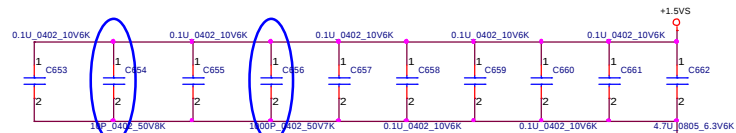
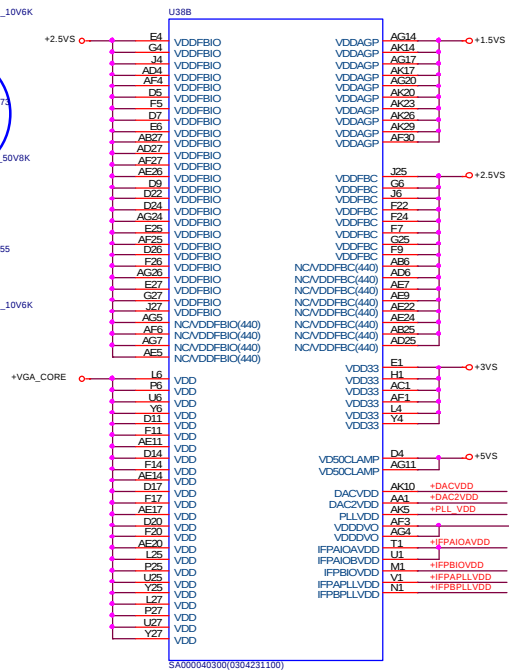
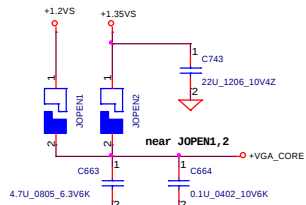
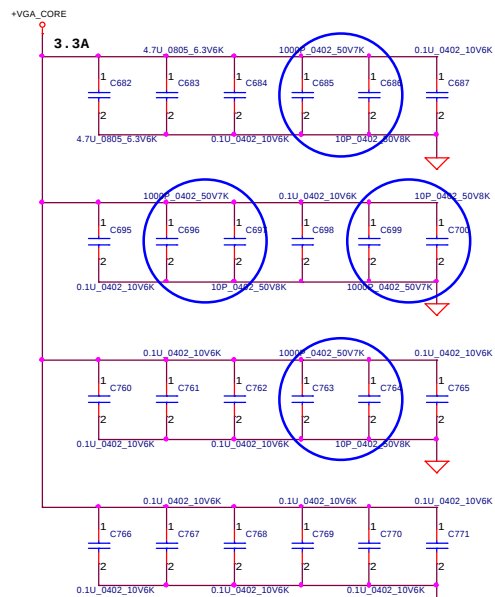
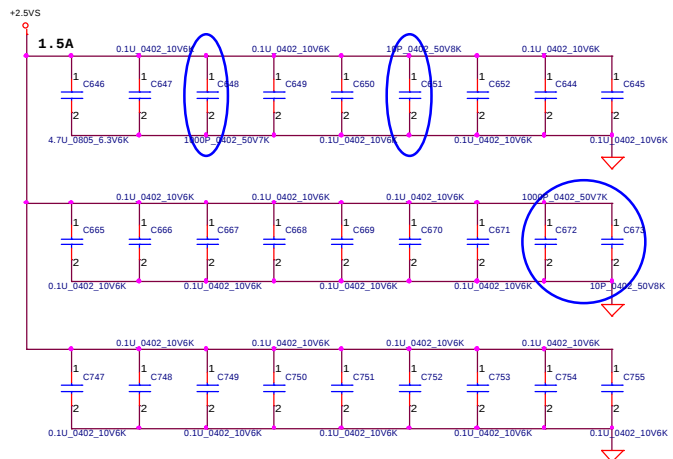
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	MAP17-116/232	MAP17-464
+VGA_CORE	* +1.2VS	+1.35VS

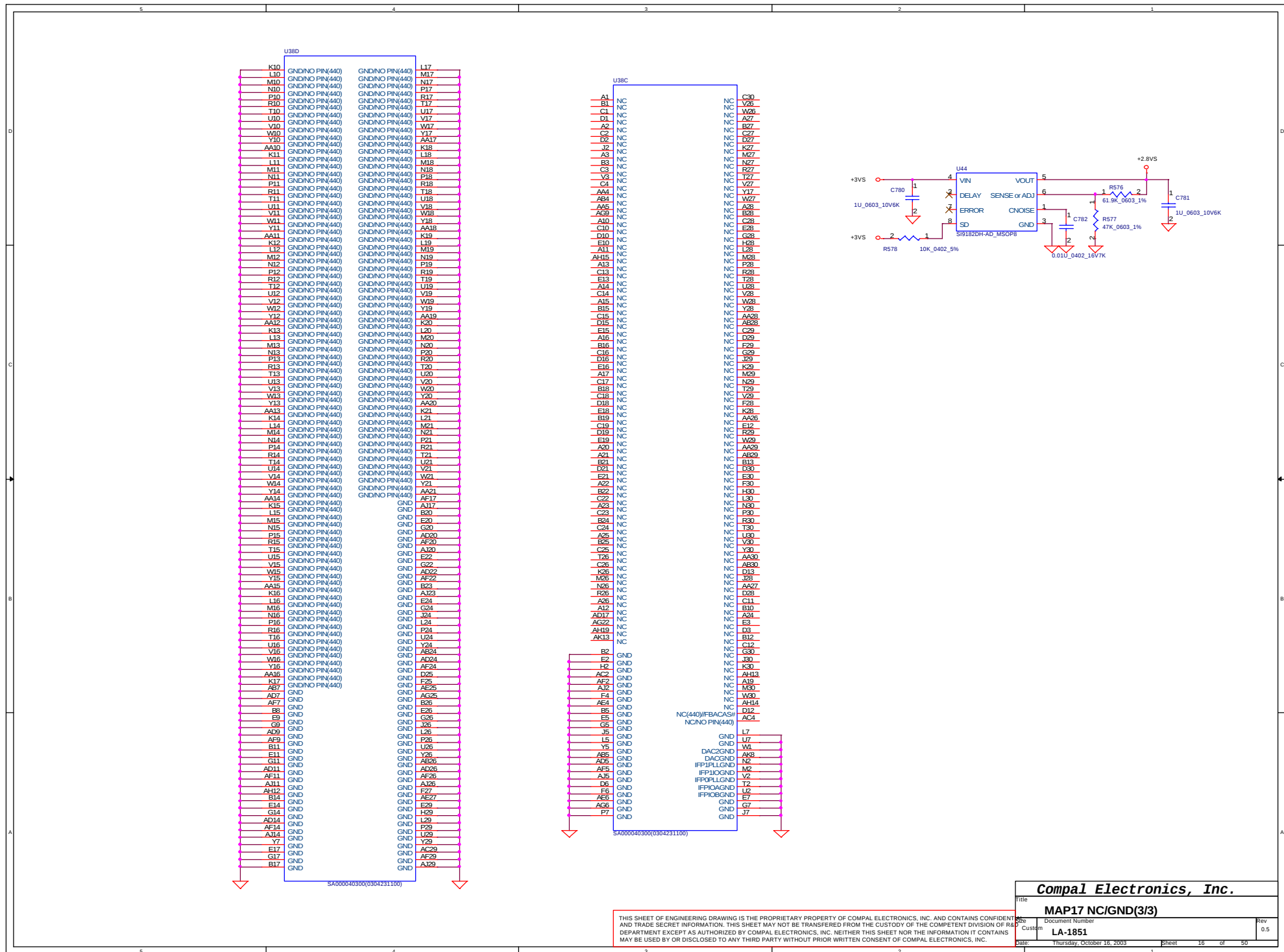


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MAP17 Power (2/3)

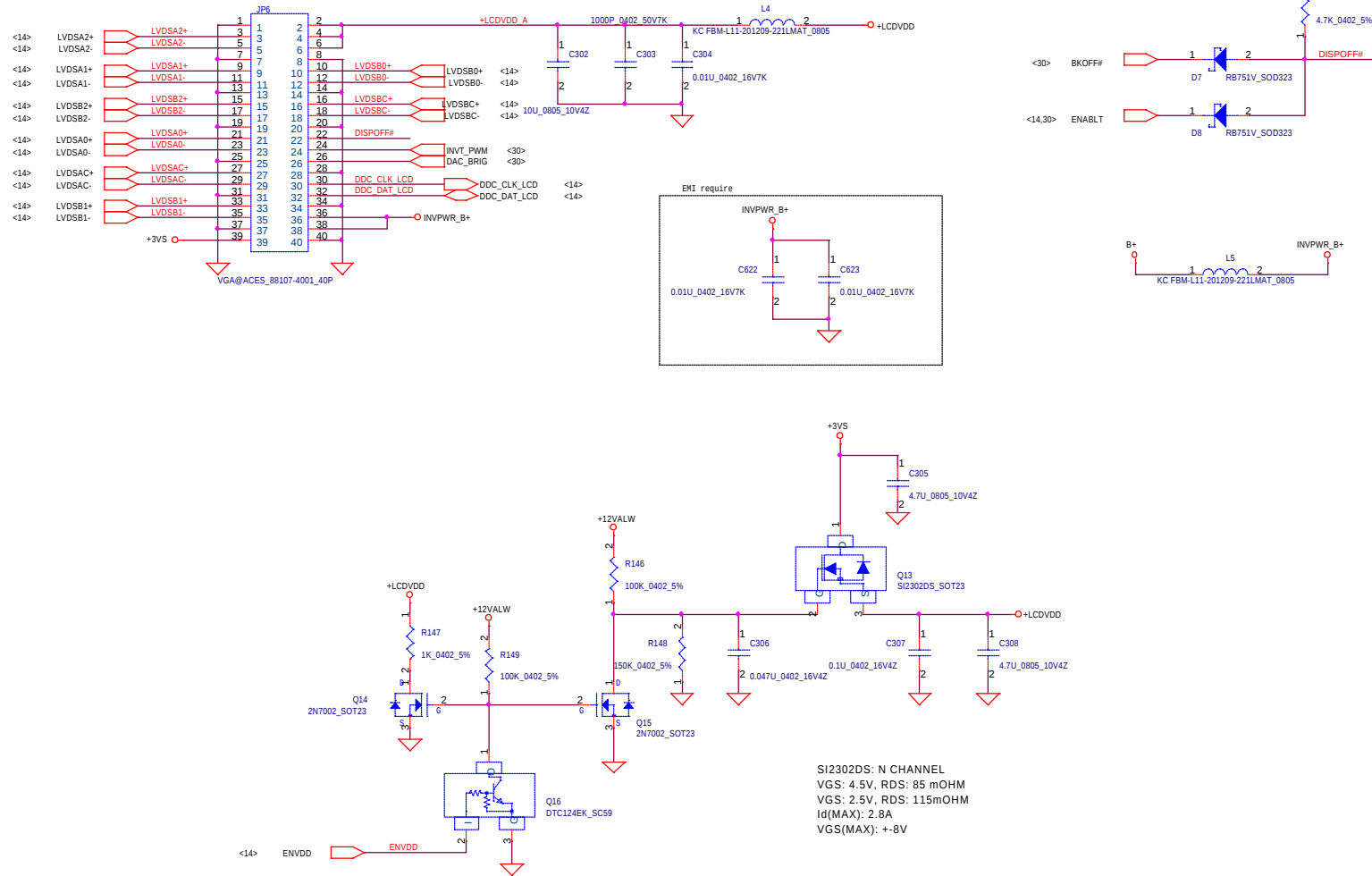
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LCD Panel Connector

The cap.'s colsely to LCD CONN.



SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

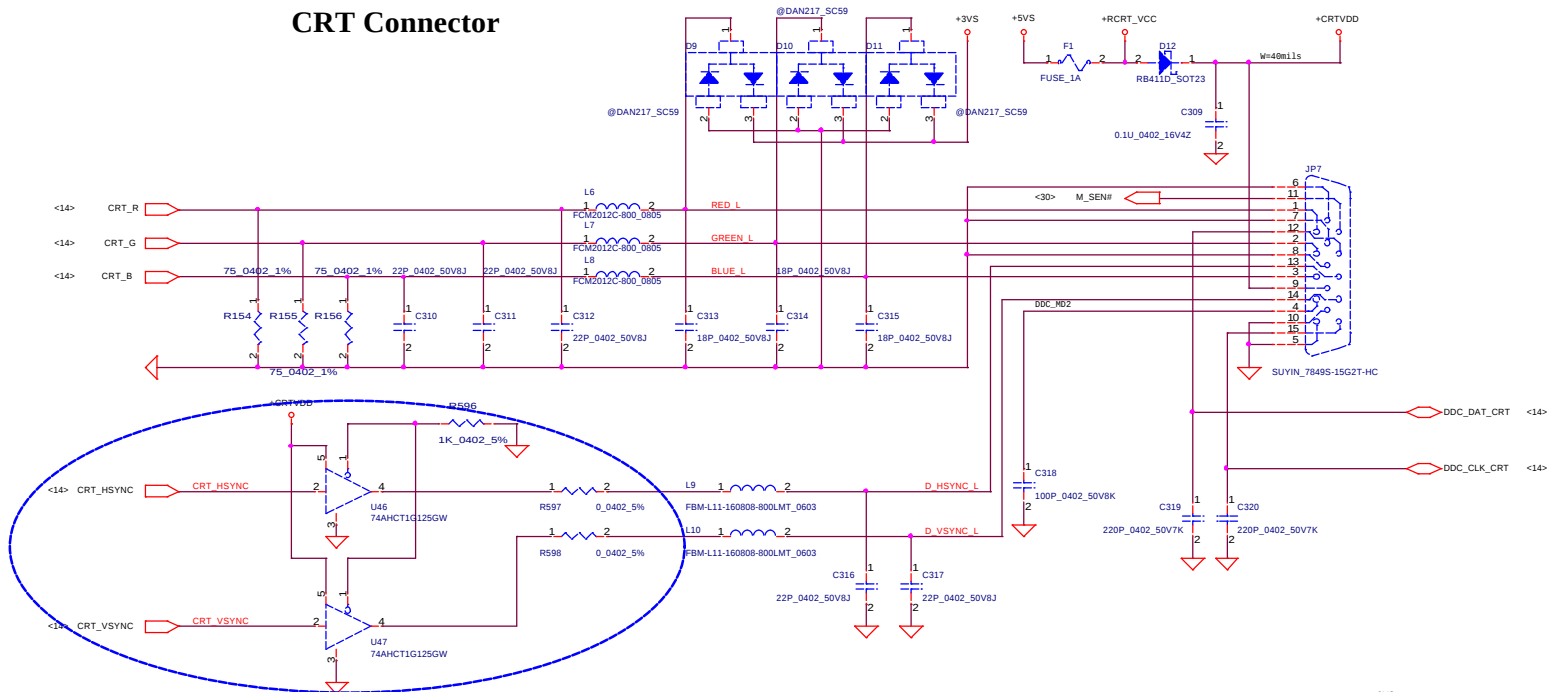
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LVDS Connector

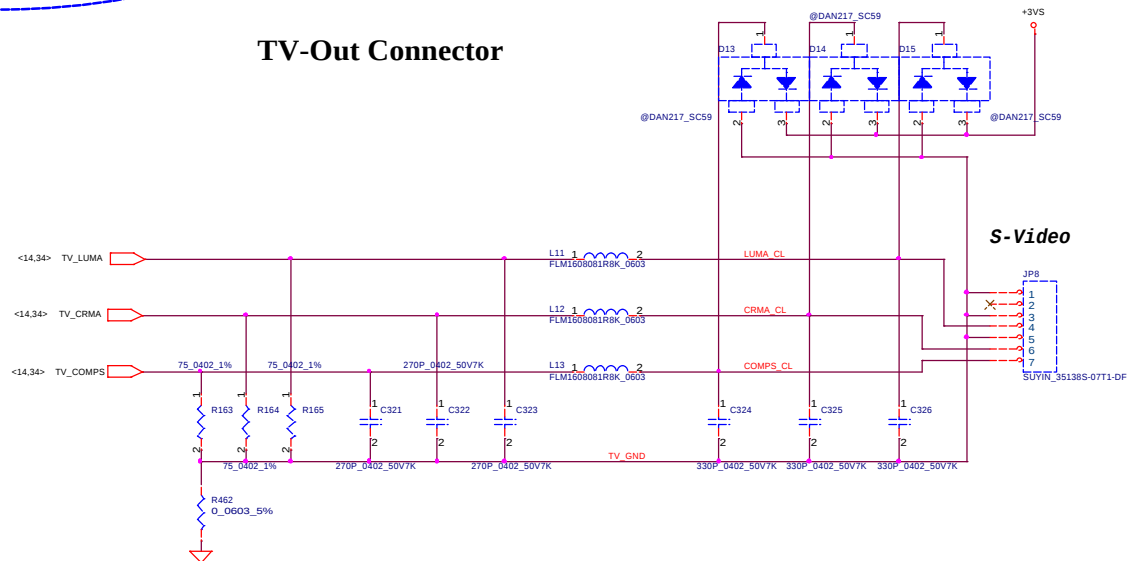
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CRT Connector



TV-Out Connector



S-Video

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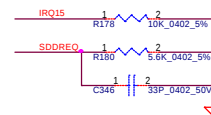
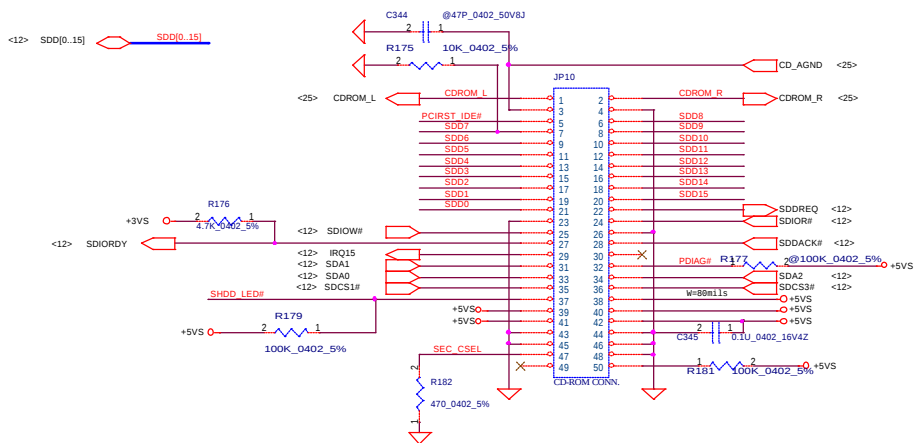
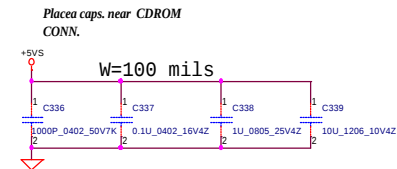
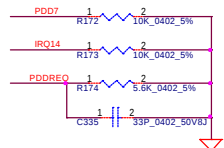
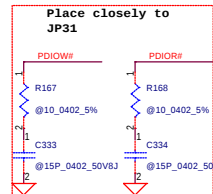
CRT & TVout Connector

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LA-1851

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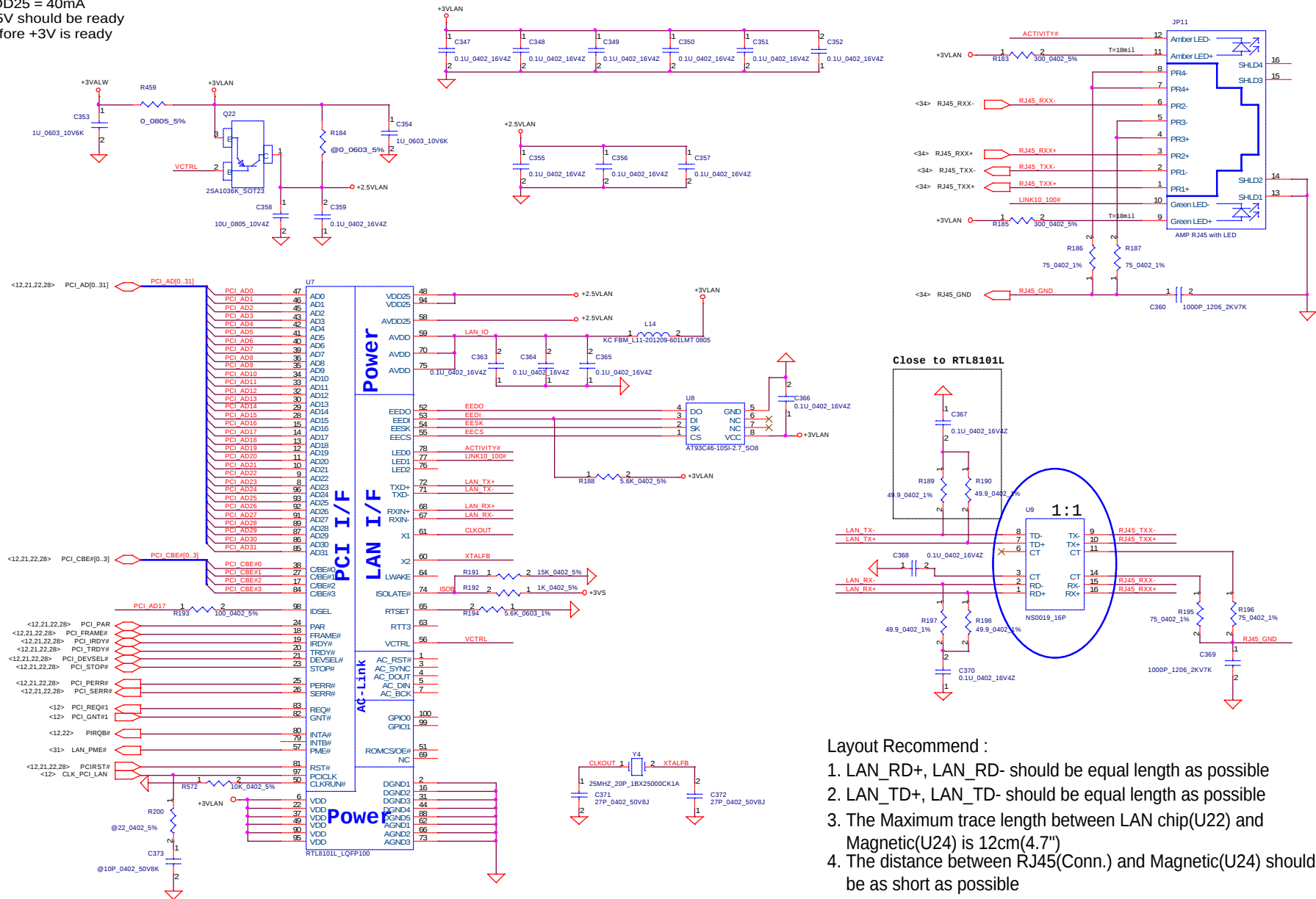
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IDE/FDD/CD-ROM Module

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Note : I_{max} for
VDD25 = 40mA
2.5V should be ready
before +3V is ready



Layout Recommend :

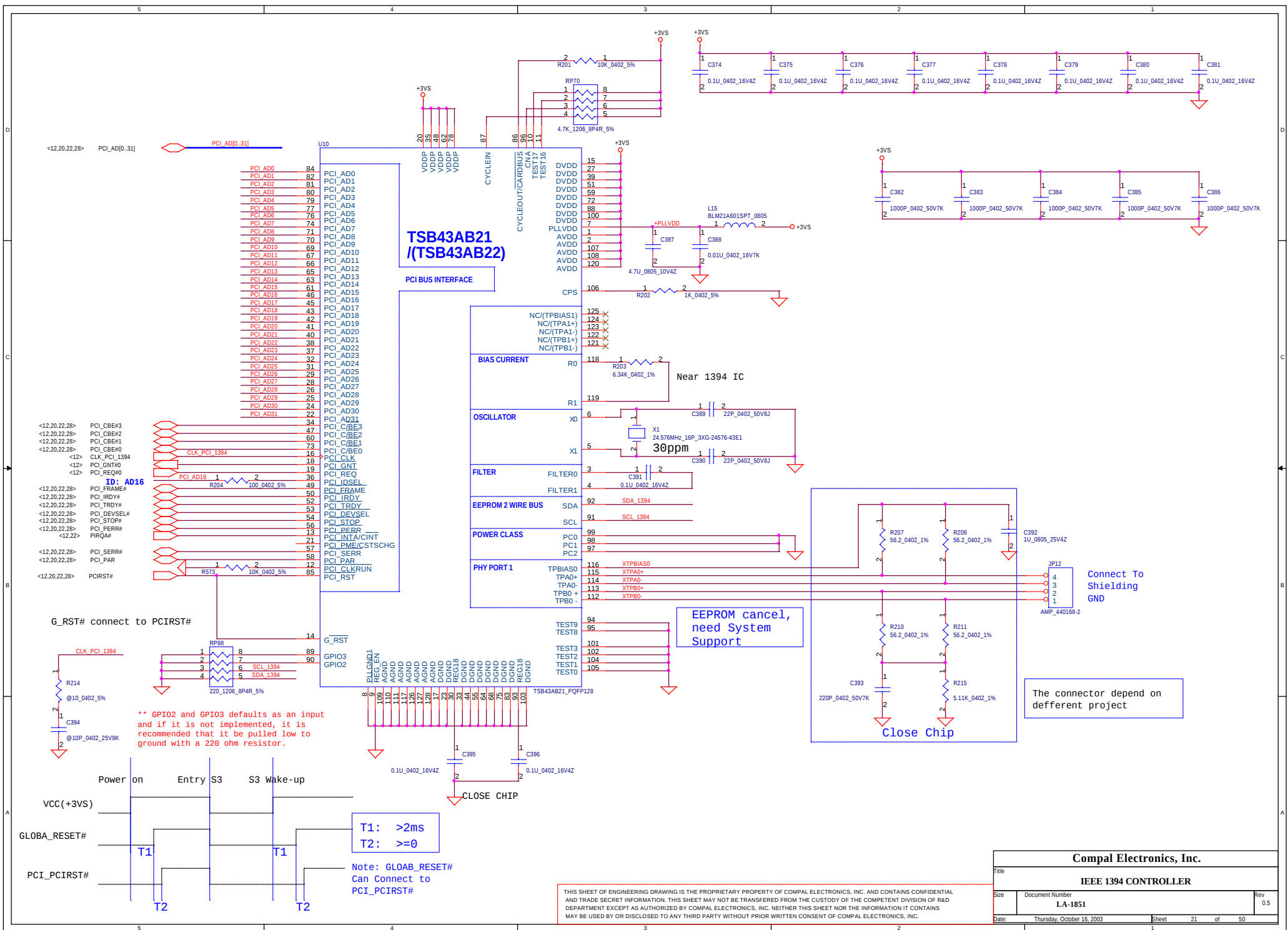
1. LAN_RD+, LAN_RD- should be equal length as possible
2. LAN_TD+, LAN_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

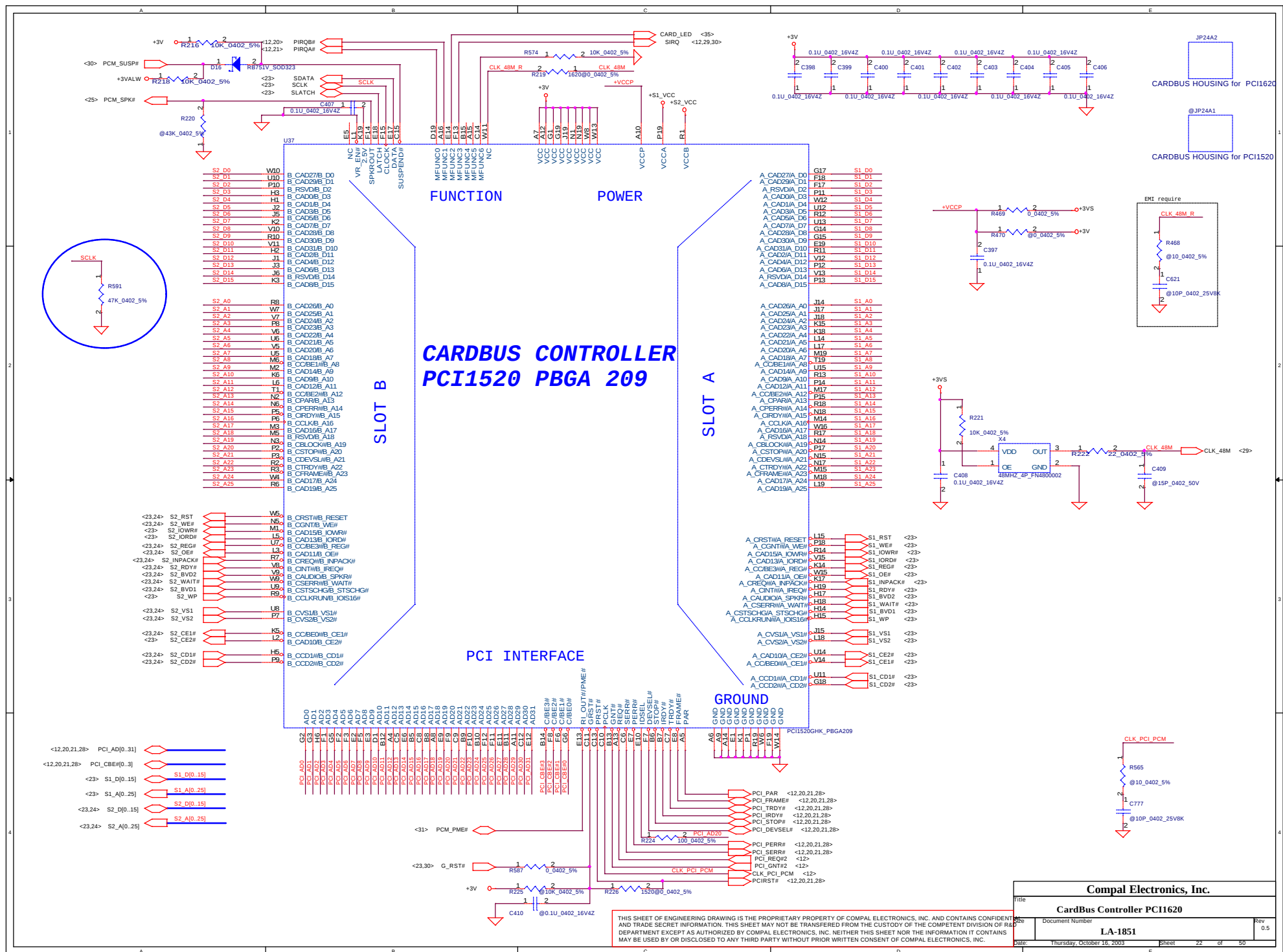
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LAN RealTech8100BL

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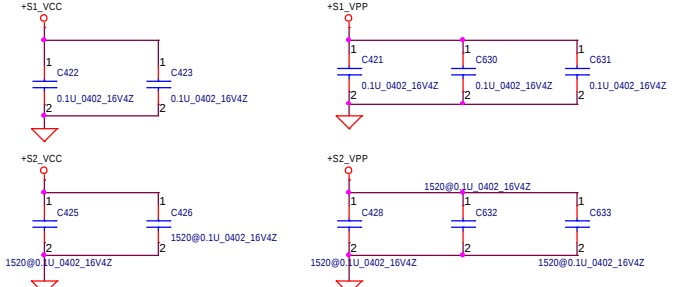
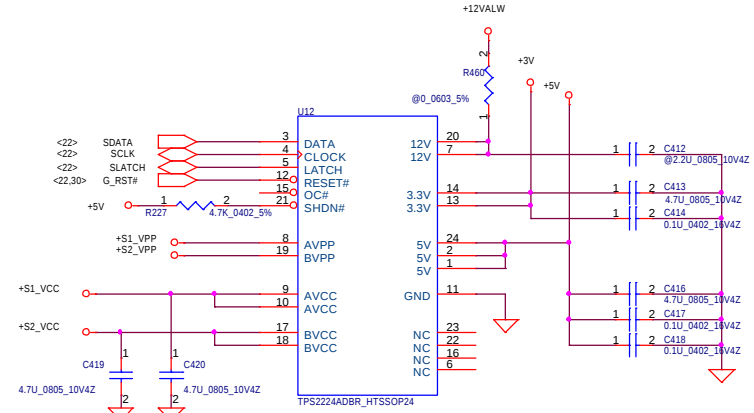
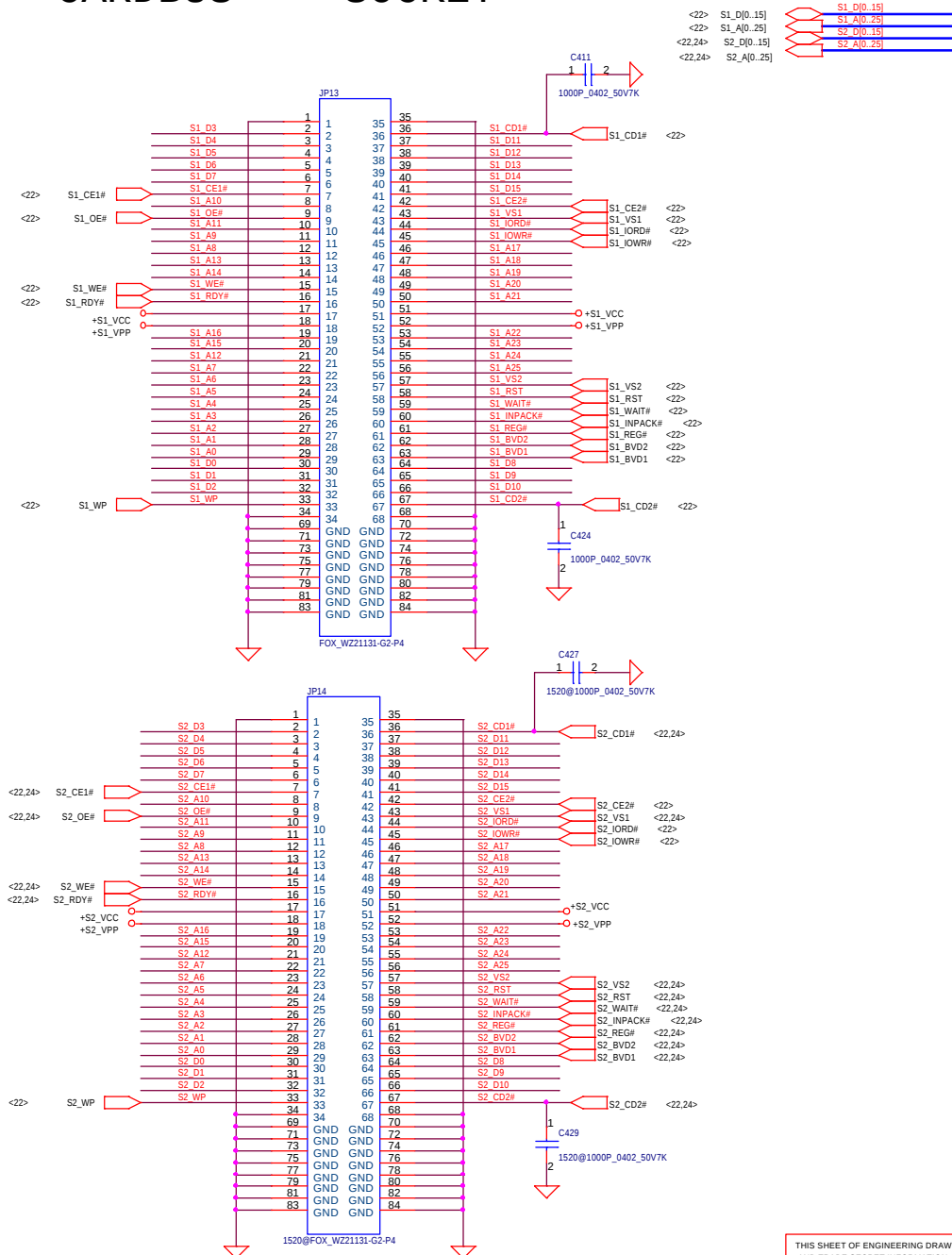




CARDBUS

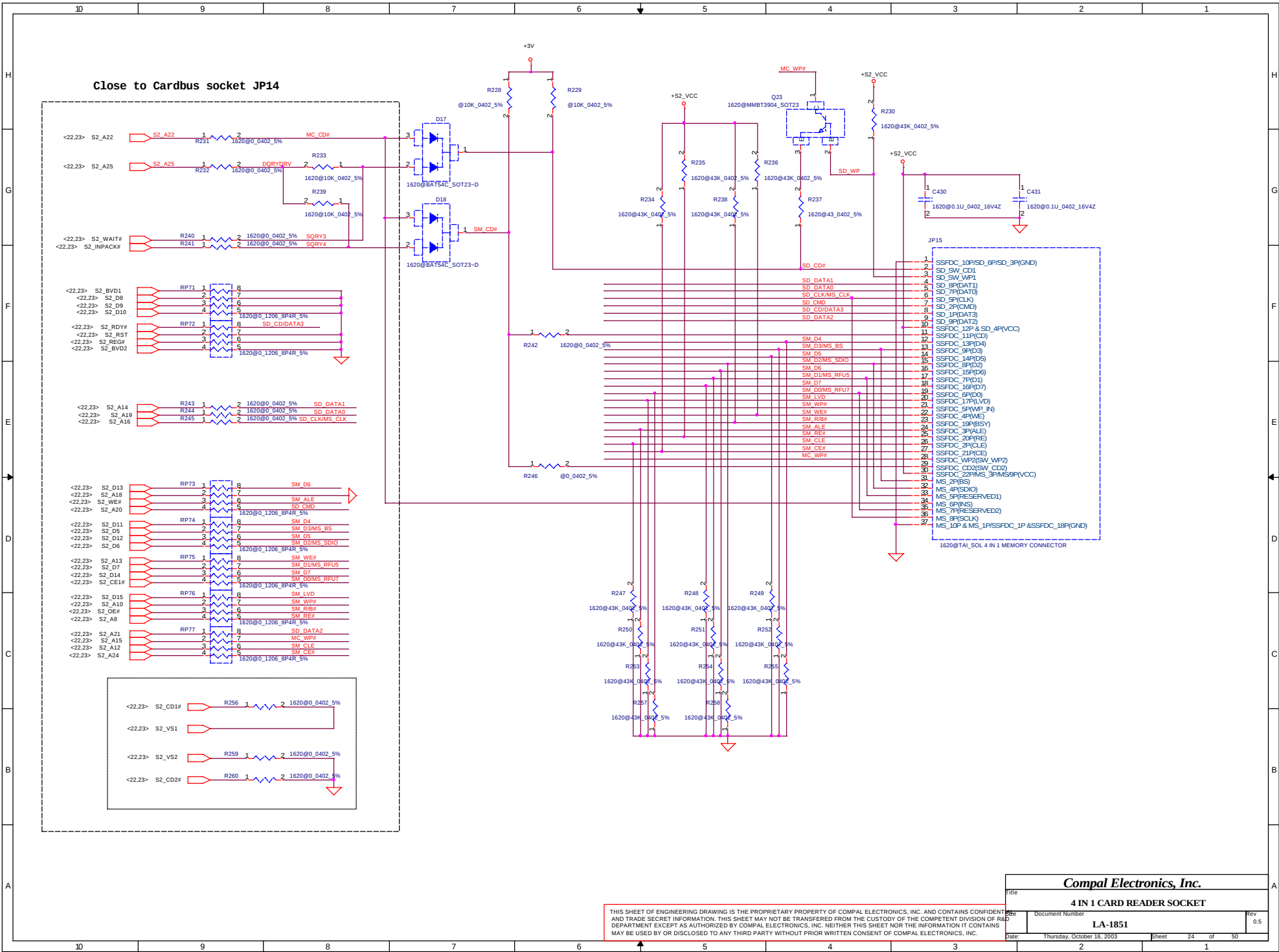
SOCKET

PCMCIA POWER CTRL.



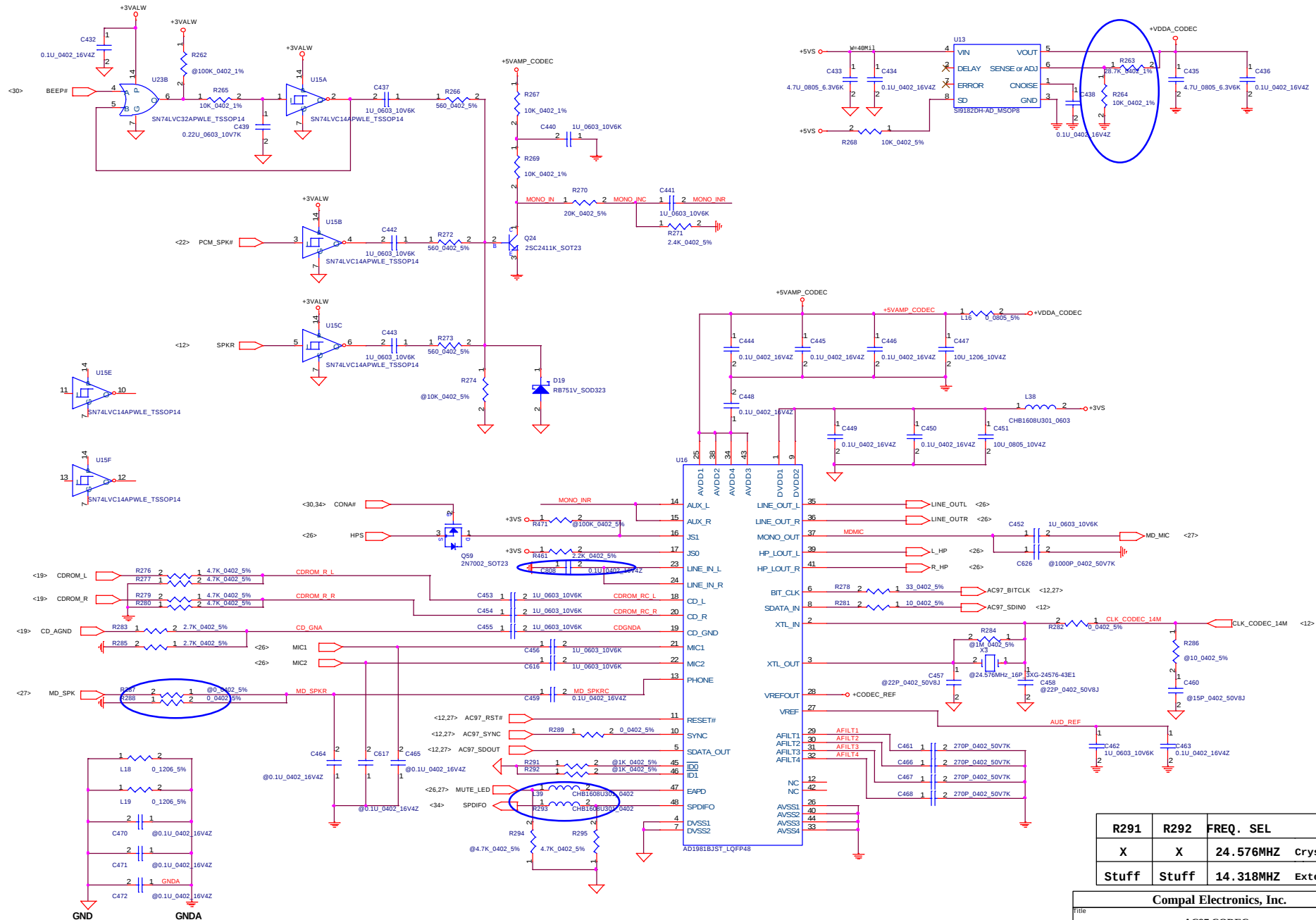
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Compal Electronics, Inc.		
File	CARD BUS SOCKET	
Size	Document Number	Rev
	LA-1851	0.5
Date	Thursday, October 16, 2003	Sheet 23 of 50



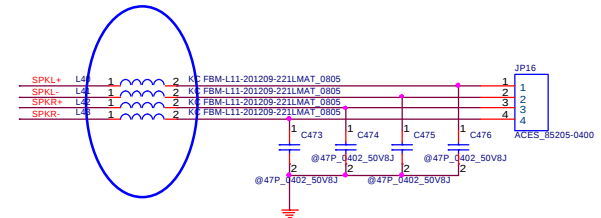
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Compal Electronics, Inc.			
4 IN 1 CARD READER SOCKET			
File	Document Number	Rev	
	LA-1851	0.5	
Date	Thursday, October 16, 2003	Sheet	24 of 50

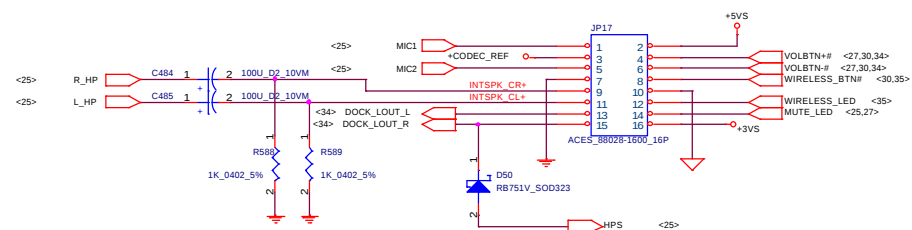


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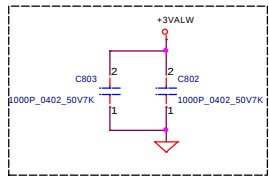
Compal Electronics, Inc.		
AC97 CODEC		
Title	Document Number	Rev
	LA-1851	0.5
Date	Thursday, October 16, 2003	Sheet 25 of 50



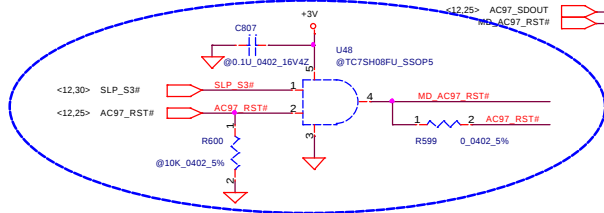
AUDIO CONNECTOR



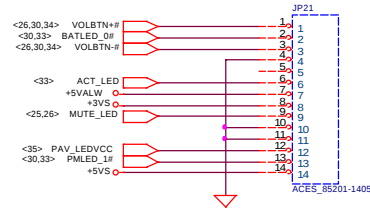
MDC Conn.



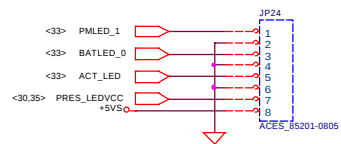
Stitched capacitor



Front Board CONNECTOR
Pavilion only

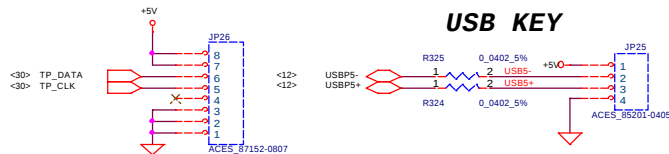


Front Board CONNECTOR
PRESARIO only



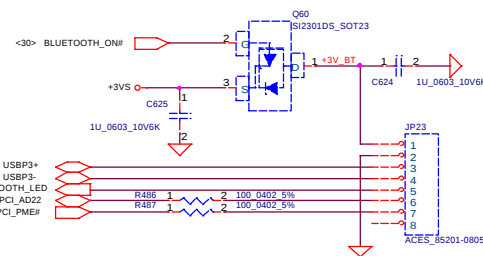
TP CONNECTOR

USB KEY

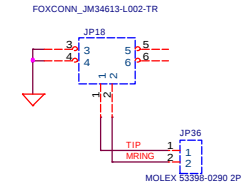


Note: PLACE CLOSE TO EACH USB PORT

BT CONNECTOR

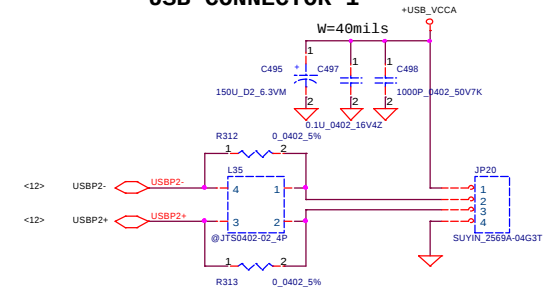


RJ11 CONN.

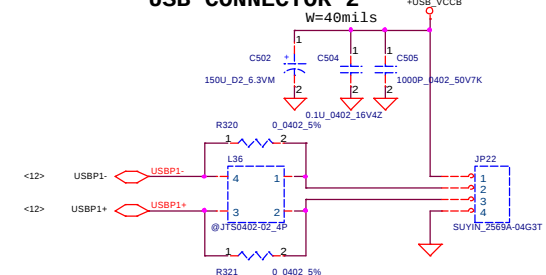


0: Have primary CODEC on mother board

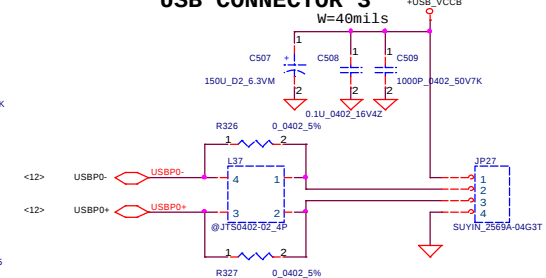
USB CONNECTOR 1



USB CONNECTOR 2



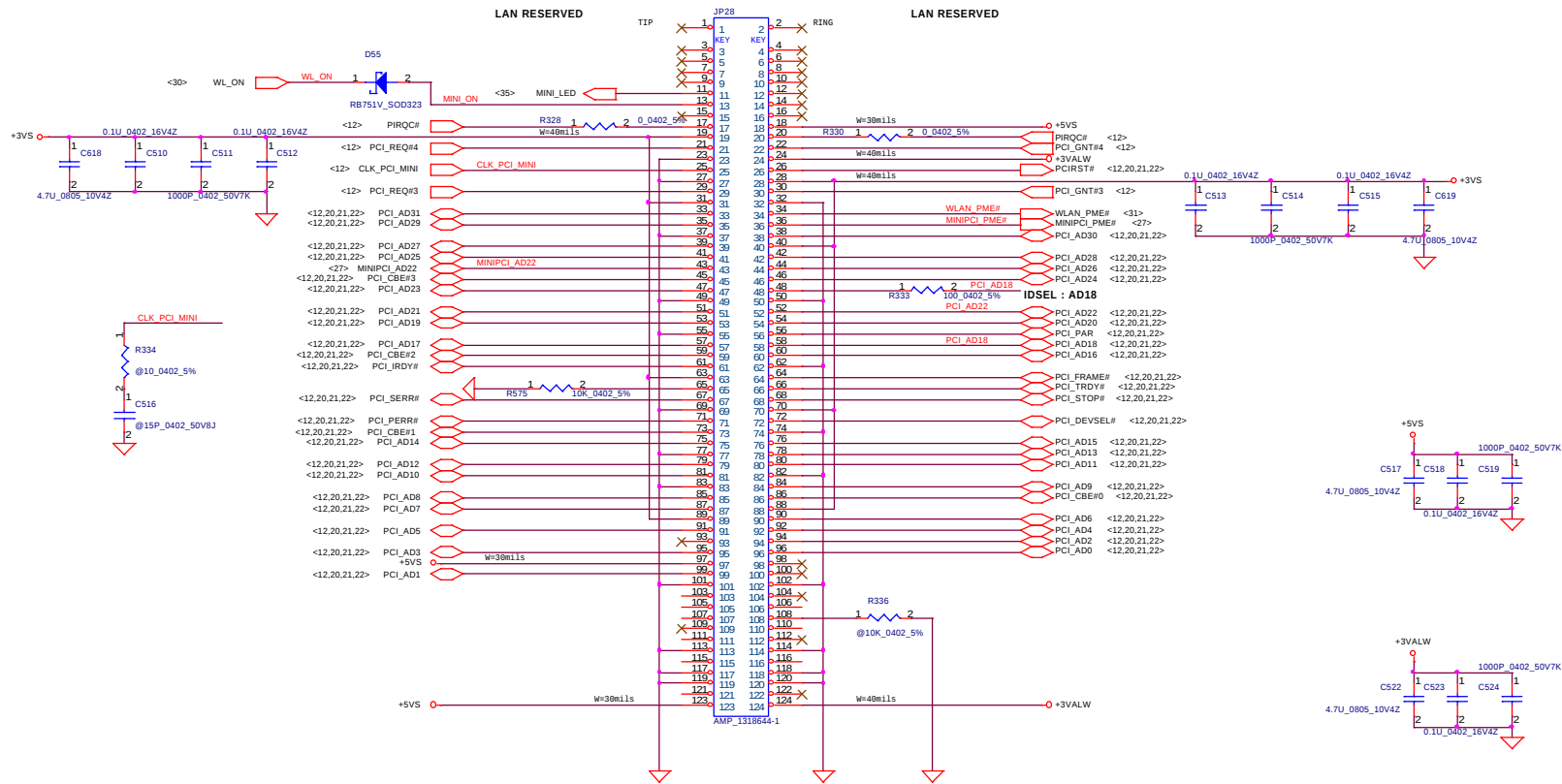
USB CONNECTOR 3



Compal Electronics, Inc.

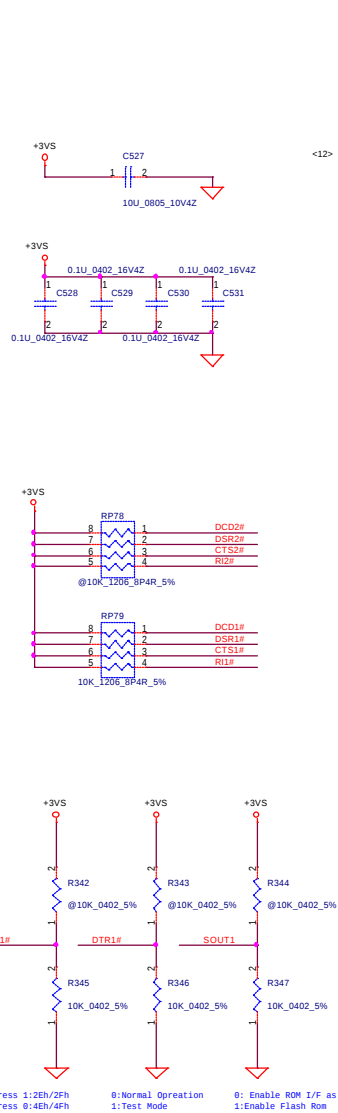
MDC , Bluetooth & USB CONN.

LA-1851

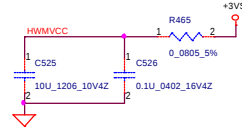
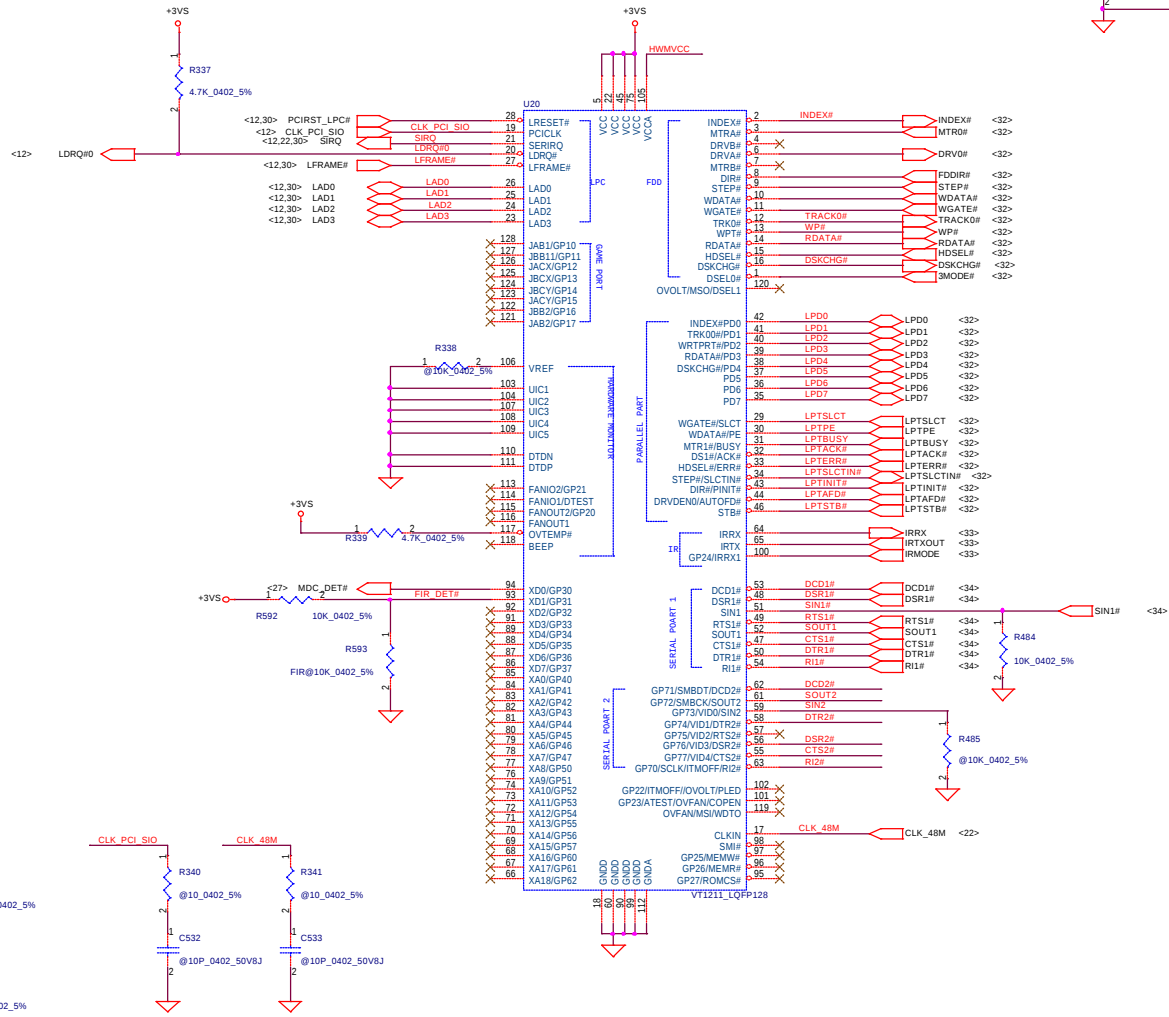
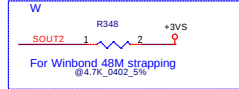


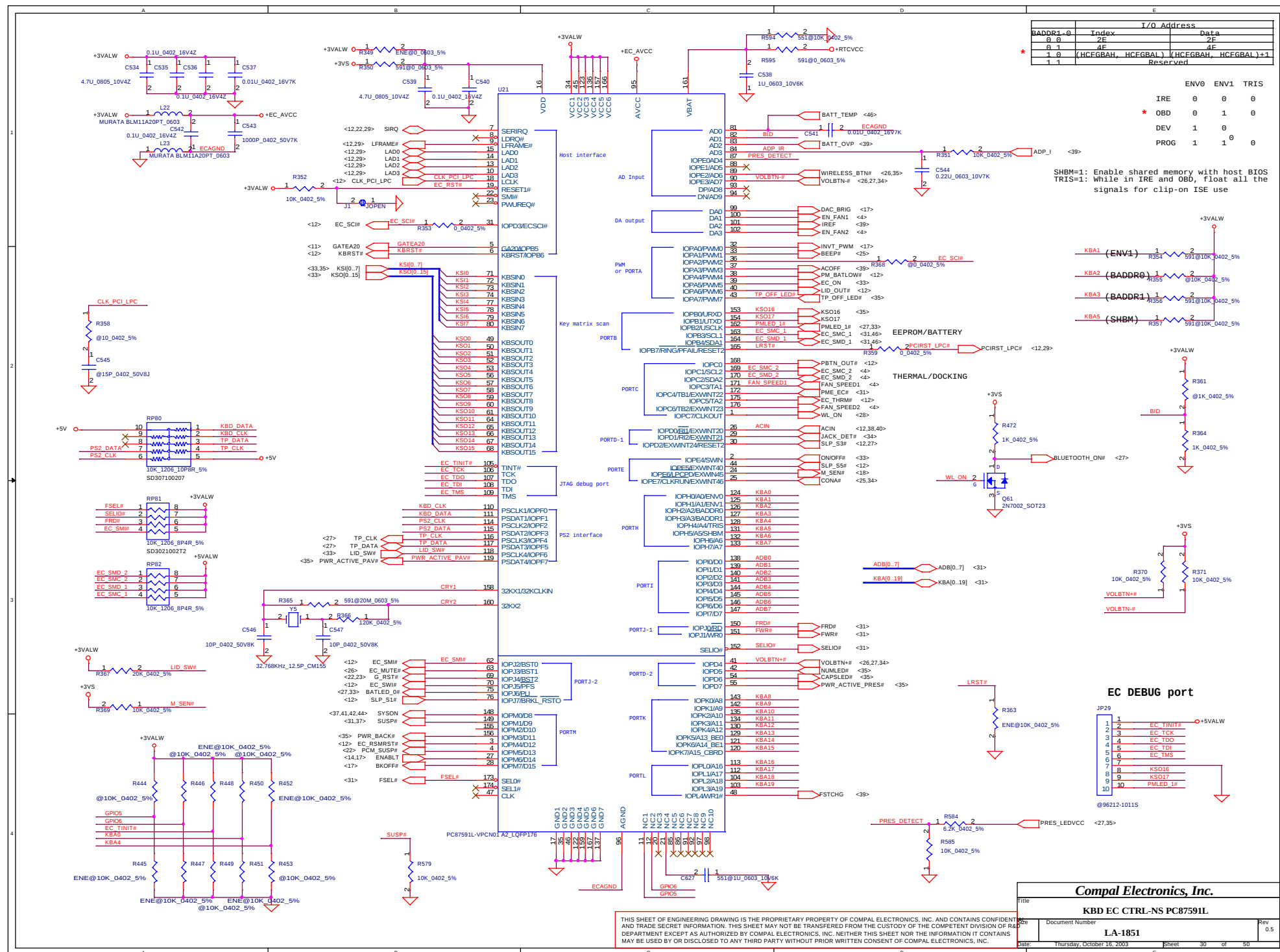
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Compal Electronics, Inc.			
Mini PCI Slot			
Doc No.	Document Number	Rev	0.5
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Super I/O strapping for VT1211

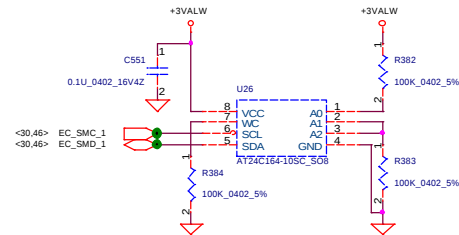
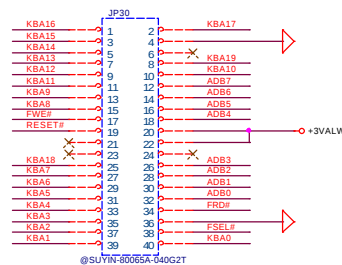
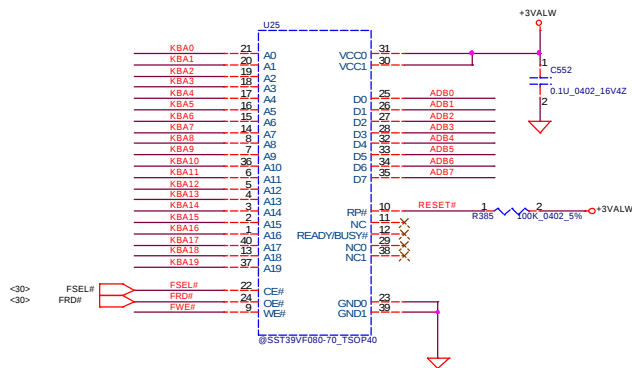
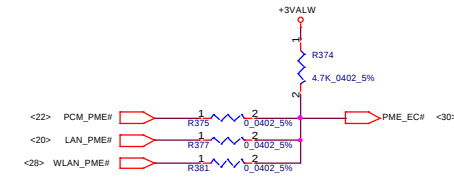
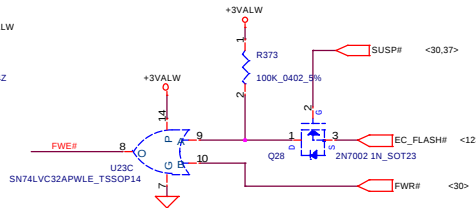
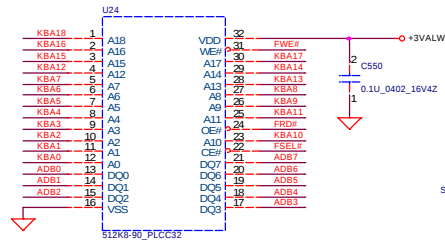
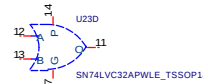
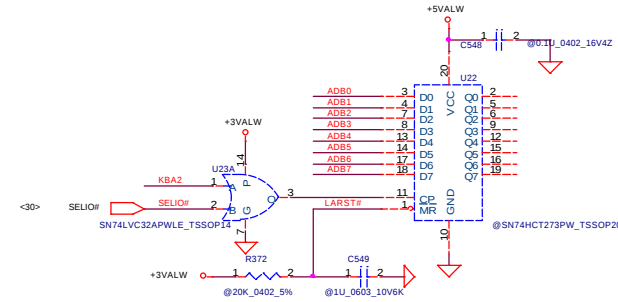




INPUT

<30> ADB[0..7] ADB[0..7]
<30> KBA[0..19] KBA[0..19]

OUTPUT



Compal Electronics, Inc.

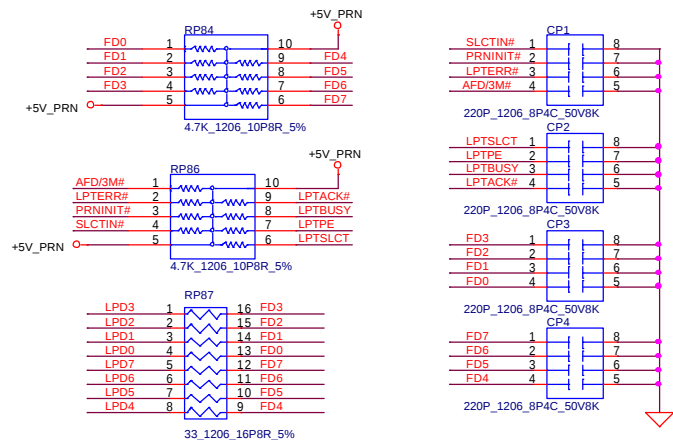
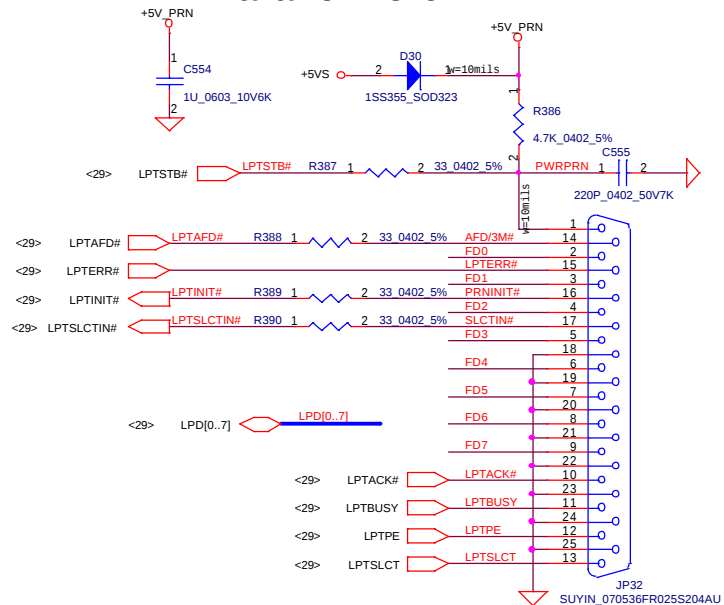
BIOS & EC I/O Port

L.A-1851

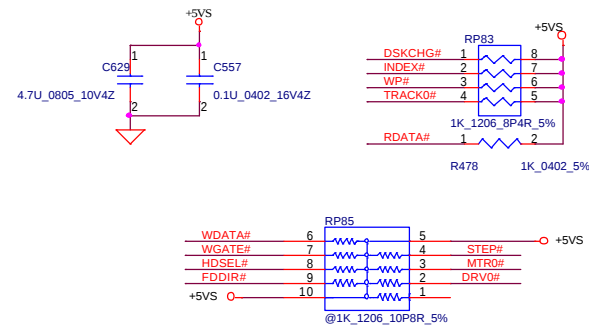
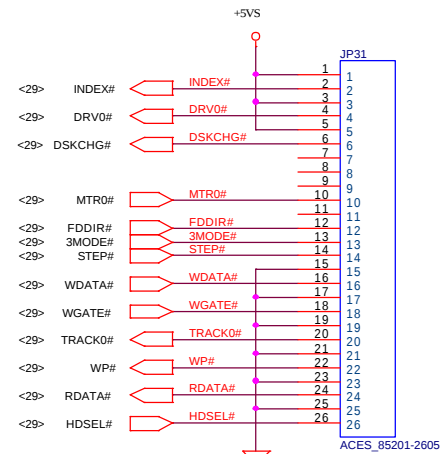
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		0.5
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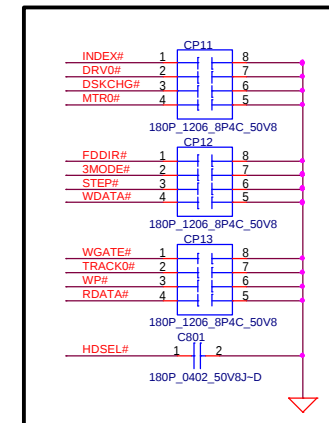
Parallel Port



FDD CONN.



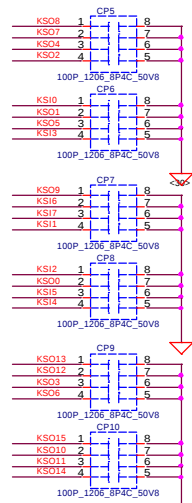
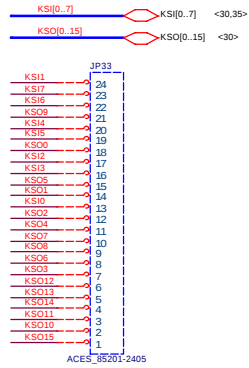
EMI Requirement



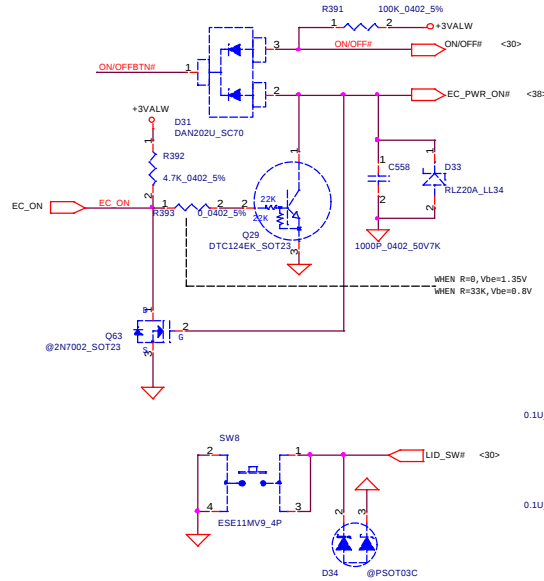
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Title		
Parallel port & FDD Connector		
Size B	Document Number LA-1851	Rev 0.5
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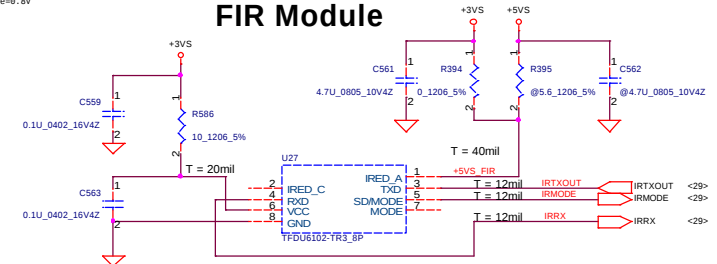
INT_KBD CONN.



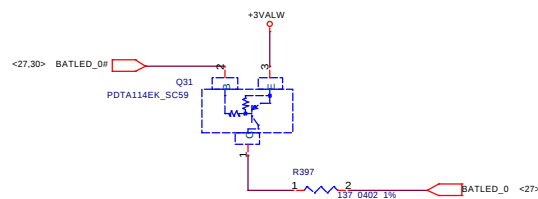
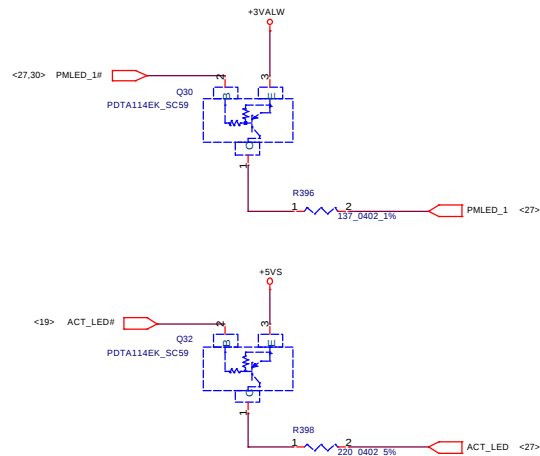
Power BTN



FIR Module



Touch Pad & Status LED Conn.



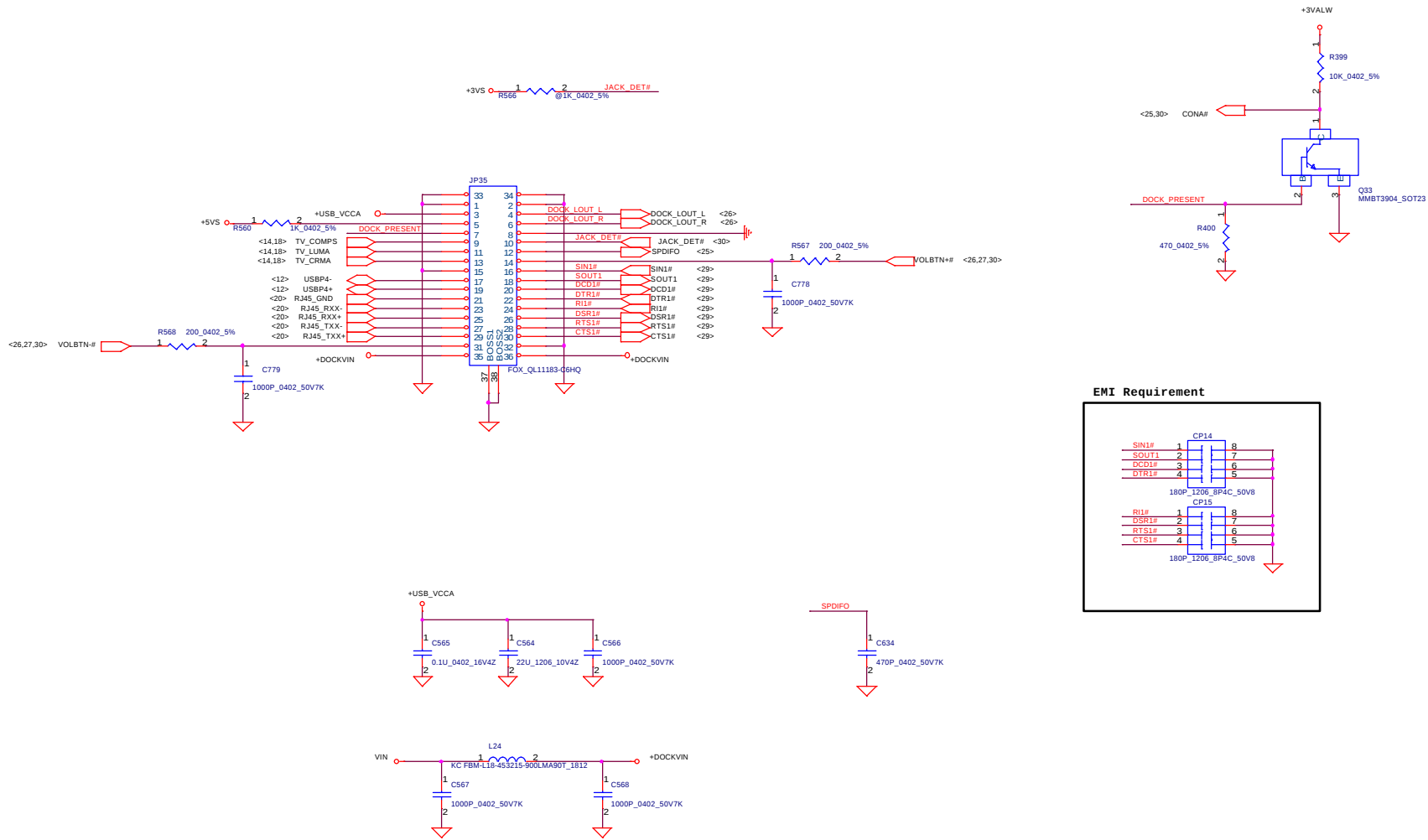
Compal Electronics, Inc.

KBD,ON/OFF,T/P,LED & FIR

LA-1851

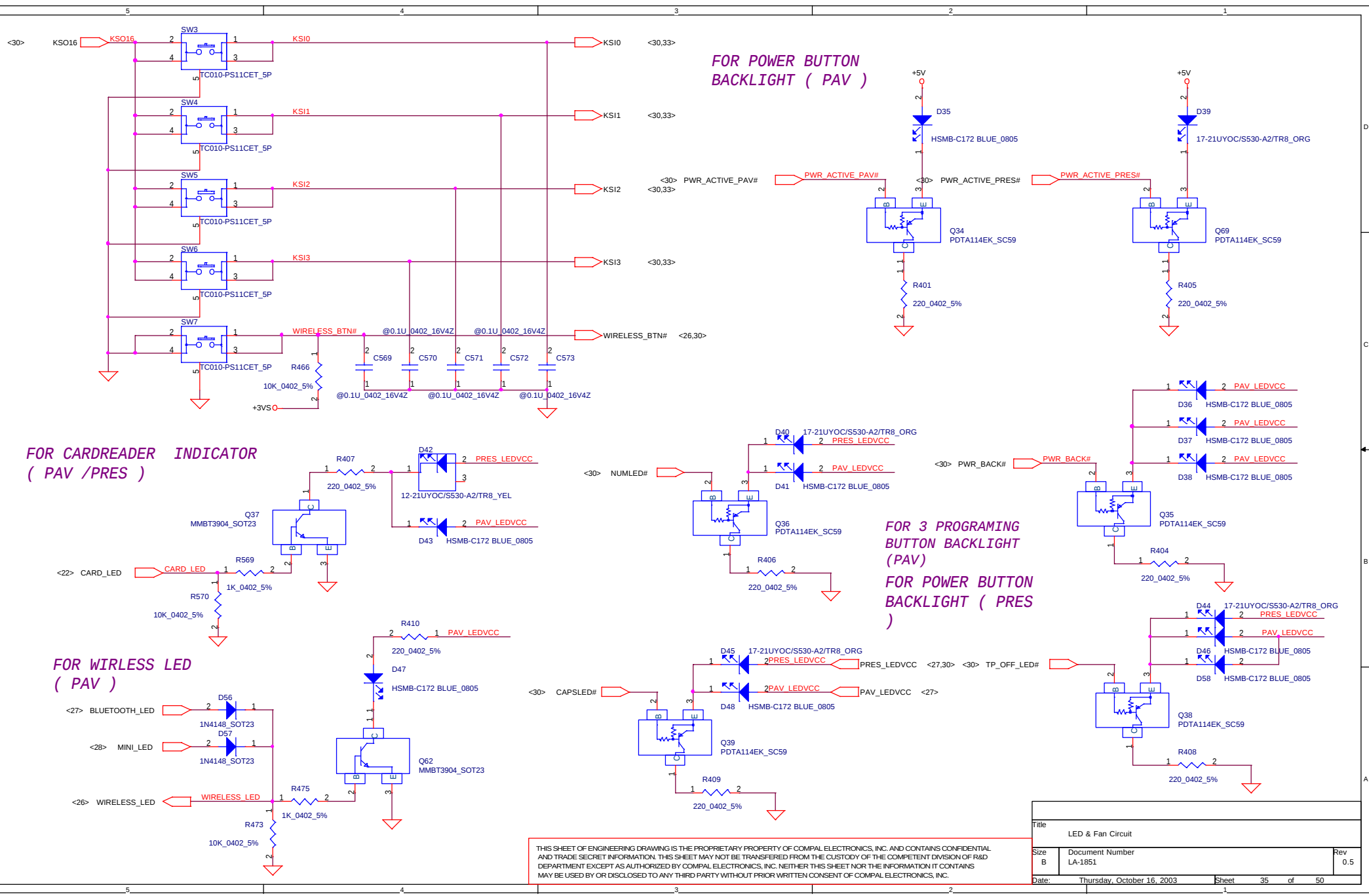
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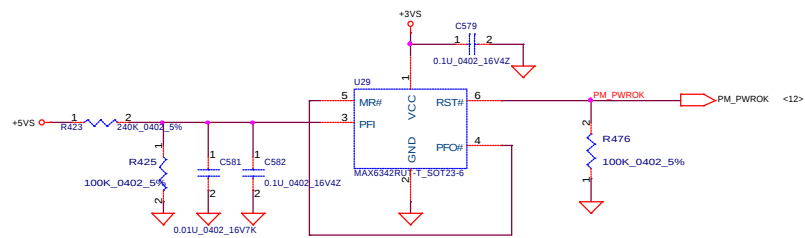
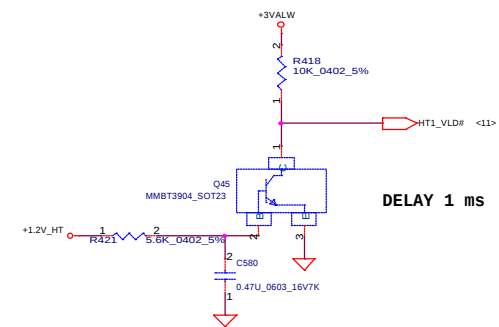
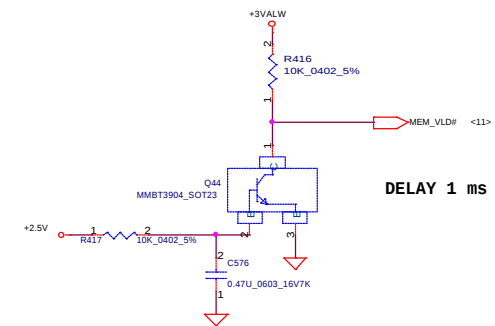
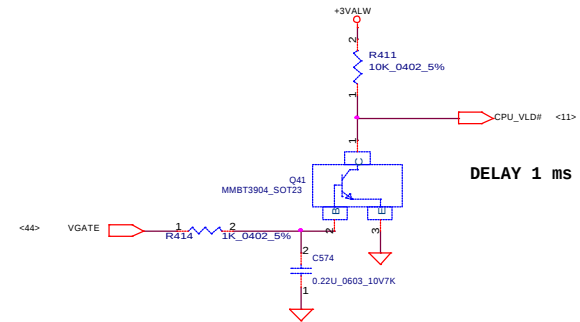
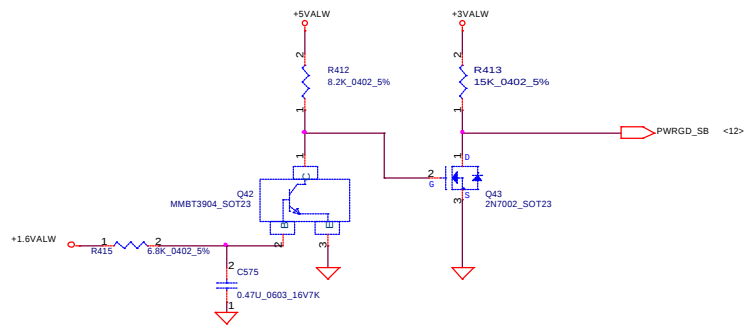
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Compal Electronics, Inc.			
Title			
SPR Connector			
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Title				
LED & Fan Circuit				
Size	Document Number			Rev
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Delay 100 ms

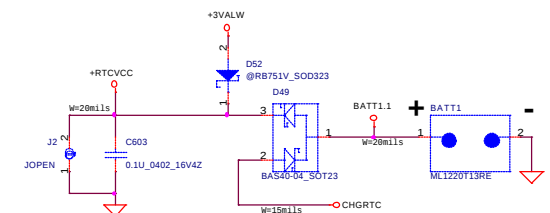
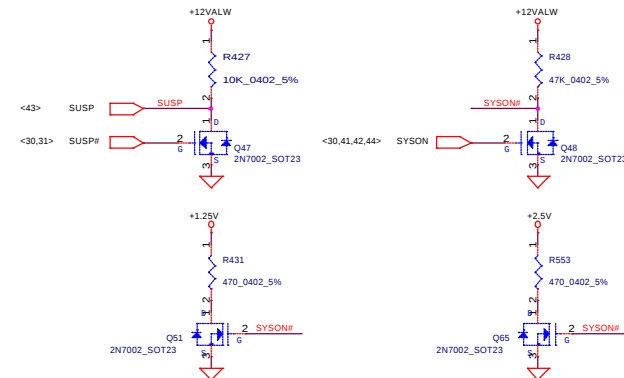
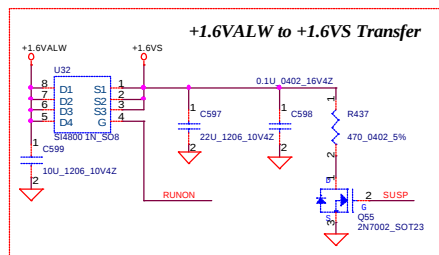
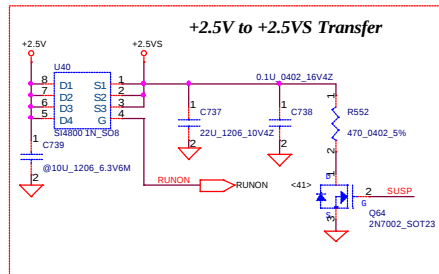
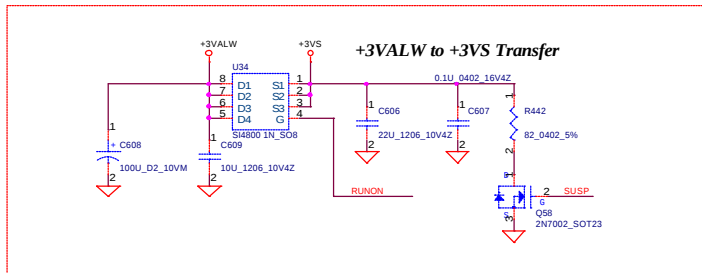
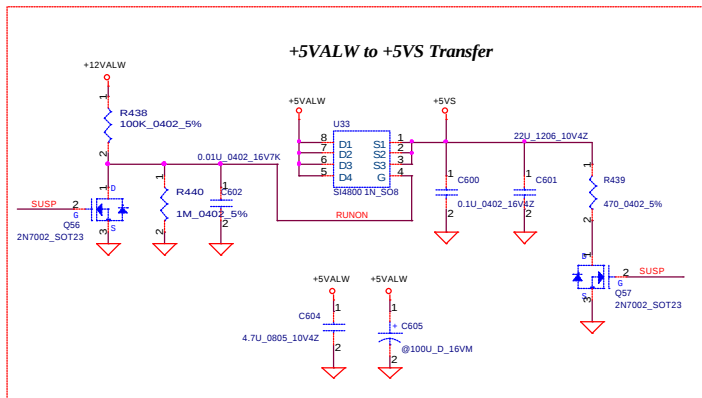
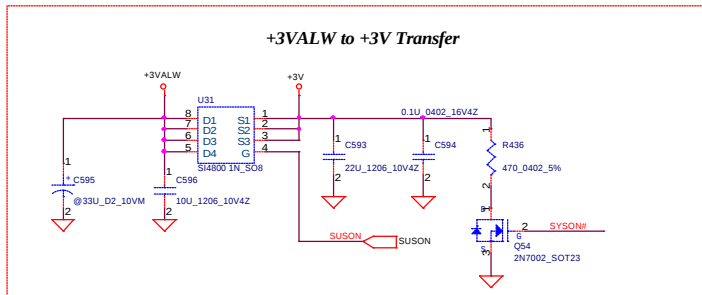
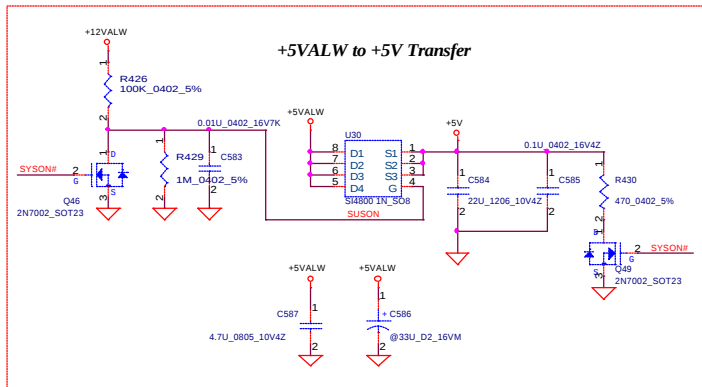
DELAY 1 ms

DELAY 1 ms

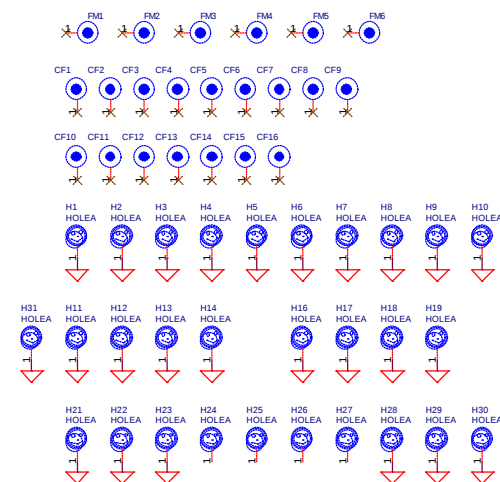
DELAY 1 ms

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Compal Electronics, Inc.			
Title		Power OK/Reset Conn.& MUTE Switch	
Rev	Document Number	Rev	
0.5	LA-1851	0.5	
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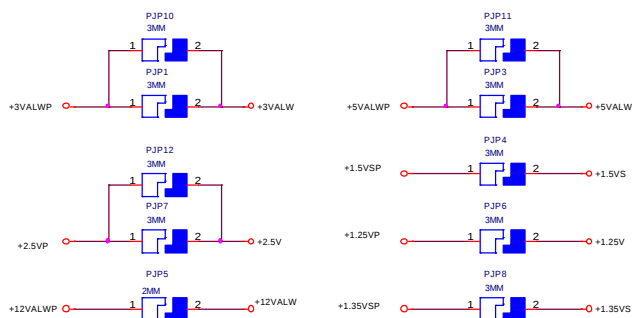
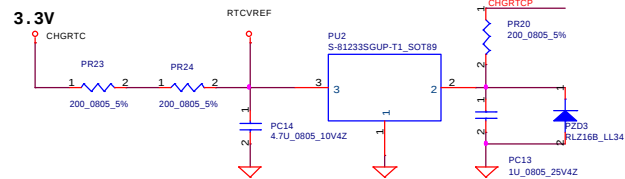
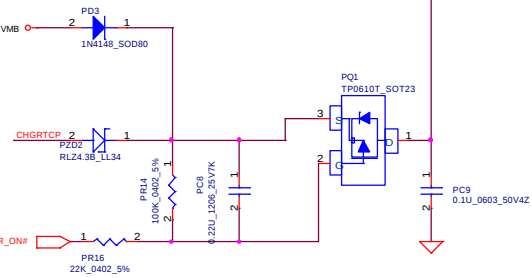
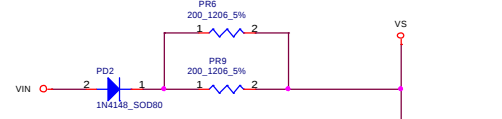
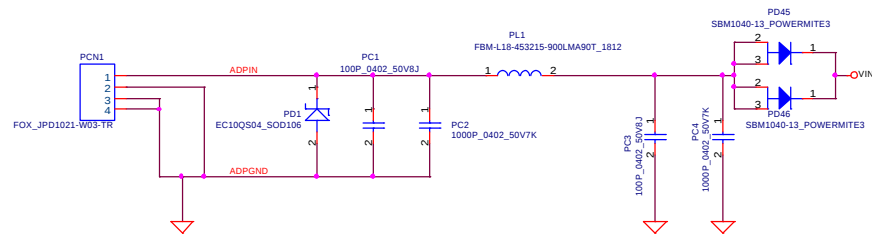
For customer request
they don't wanna
charge RTC



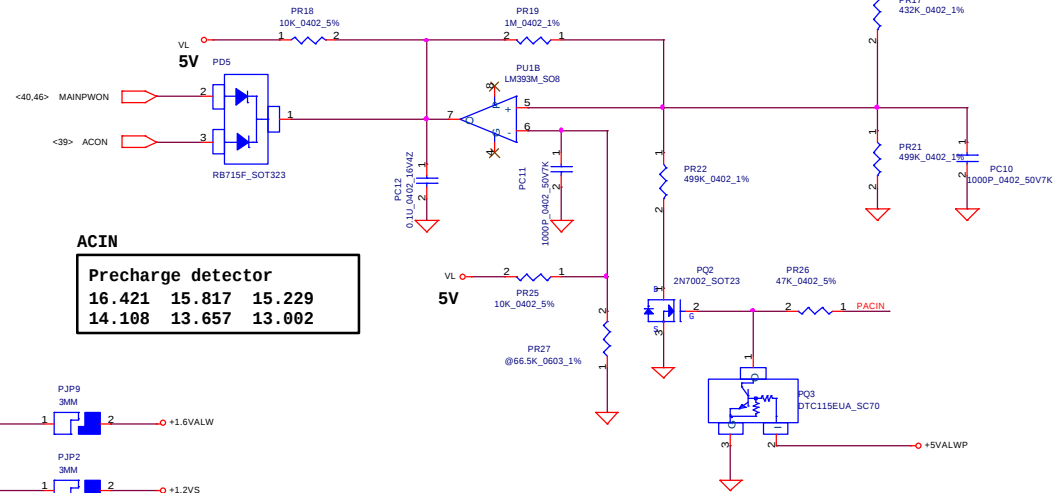
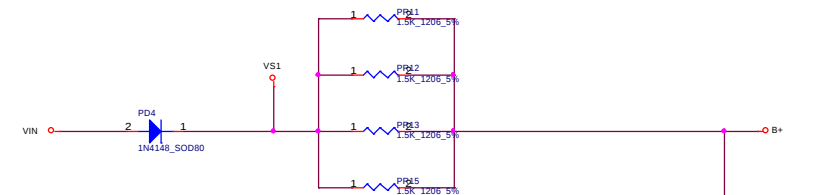
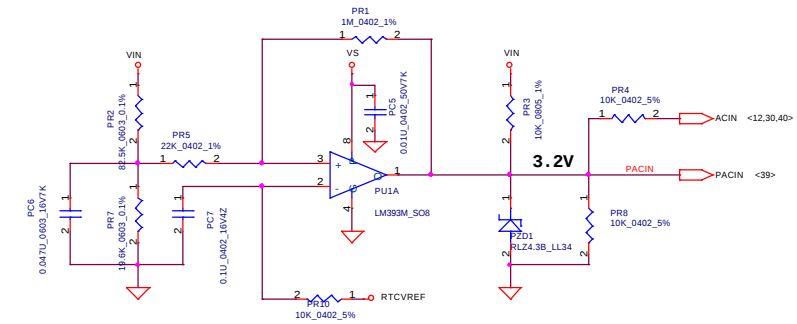
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Compal Electronics, Inc.			
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DC/DC Circuit		LA-1851	
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Detector



VIN detector			
17.945	17.343	16.757	
17.372	16.782	16.207	



ACIN			
Precharge detector			
16.421	15.817	15.229	
14.108	13.657	13.002	

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Charger

$I_{adp}=0\sim6.0A$

$I_{REF}=1.113 \cdot I_{charge}$
 $I_{REF}=0.373\sim3.3V$

OVP voltage : LI-MH 8 CELL(4S2P)
 BATT+ : 18.0V--> BATT_OVP : 2.0V
 (BATT_OVP voltage = $0.1109 \cdot BATT+$)

$CC=0(0.5A) \sim 3A$
 $CV=16.8V$ (12 CELLS)

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Compal Electronics, Inc.

Charger

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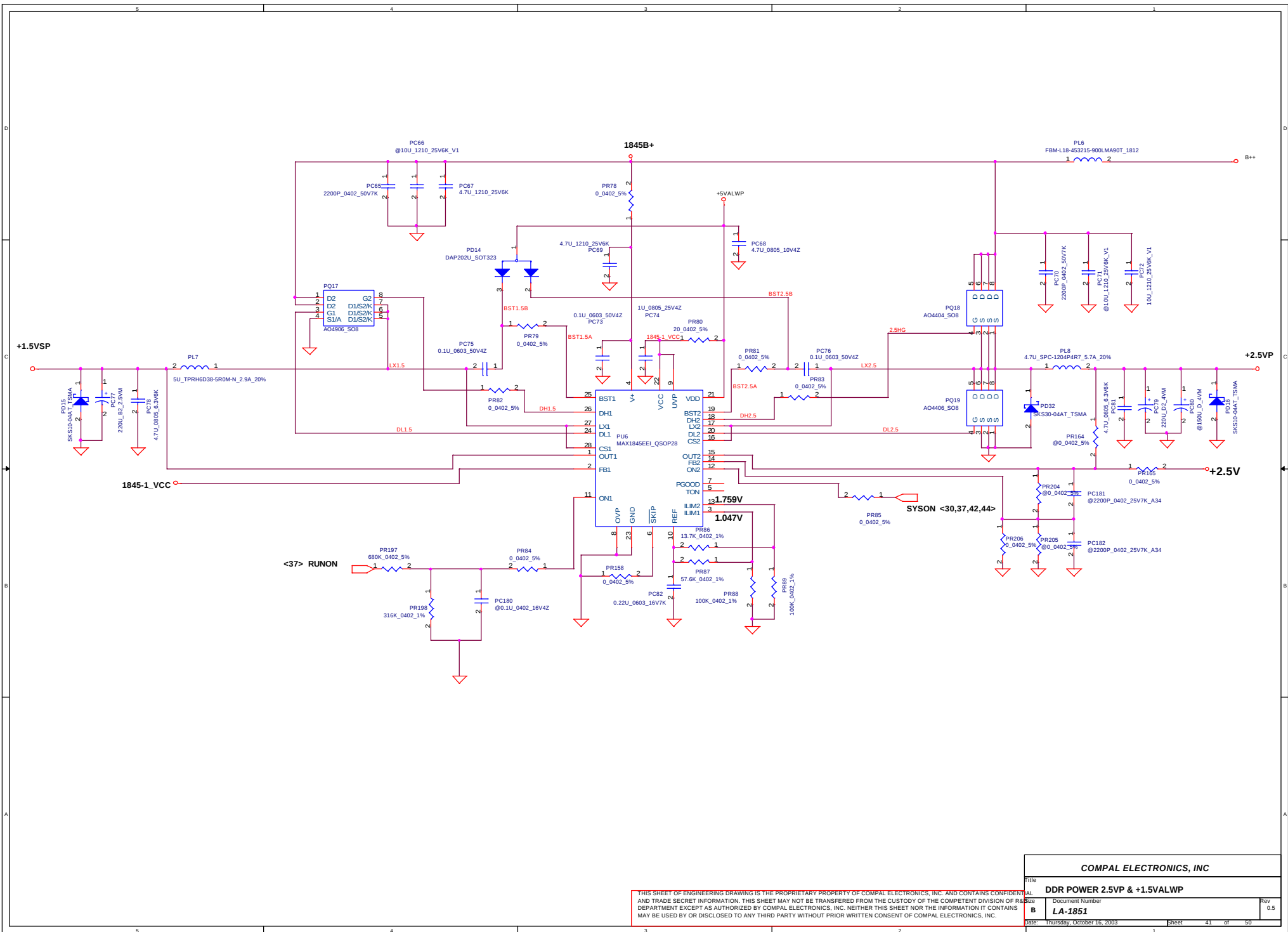
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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

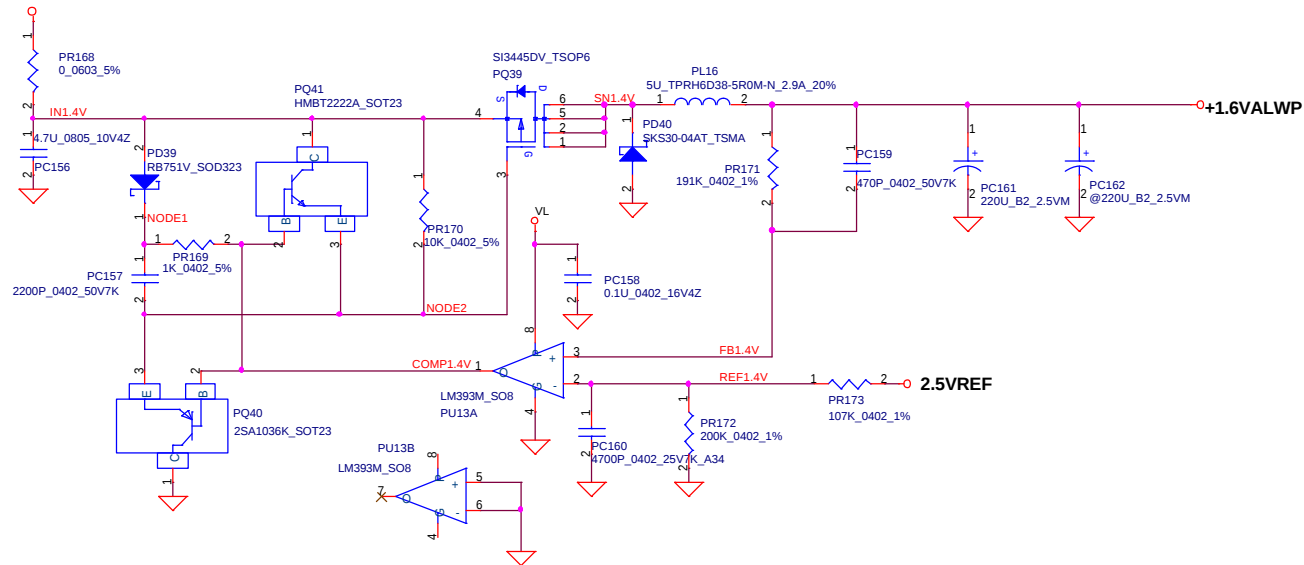
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Title			
3.3V / 5V / 12V			
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COMPAL ELECTRONICS, INC			
File			
DDR POWER 2.5VP & +1.5VALWP			
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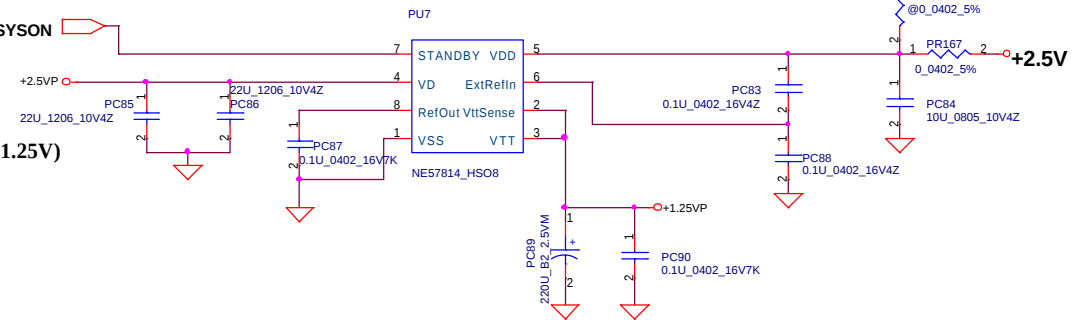
+5VALWP



+2.5VP

<30,37,41,44> SYSON

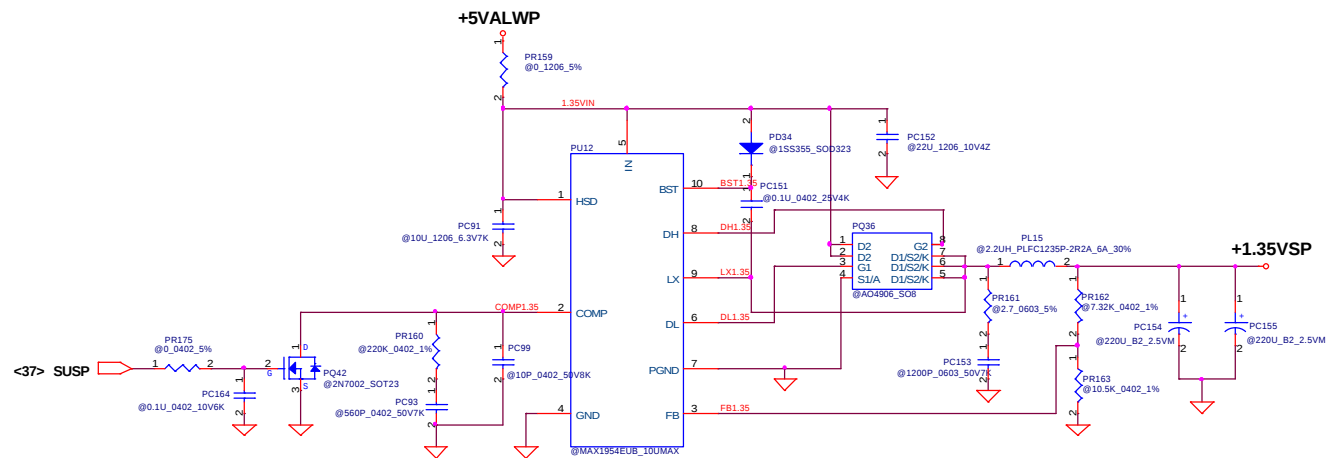
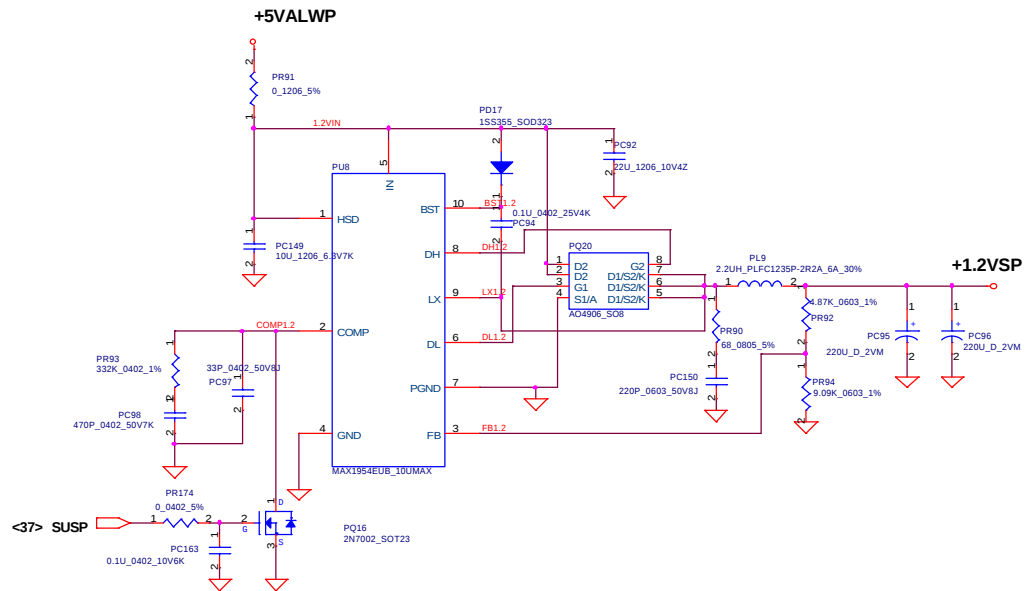
(1.25V)



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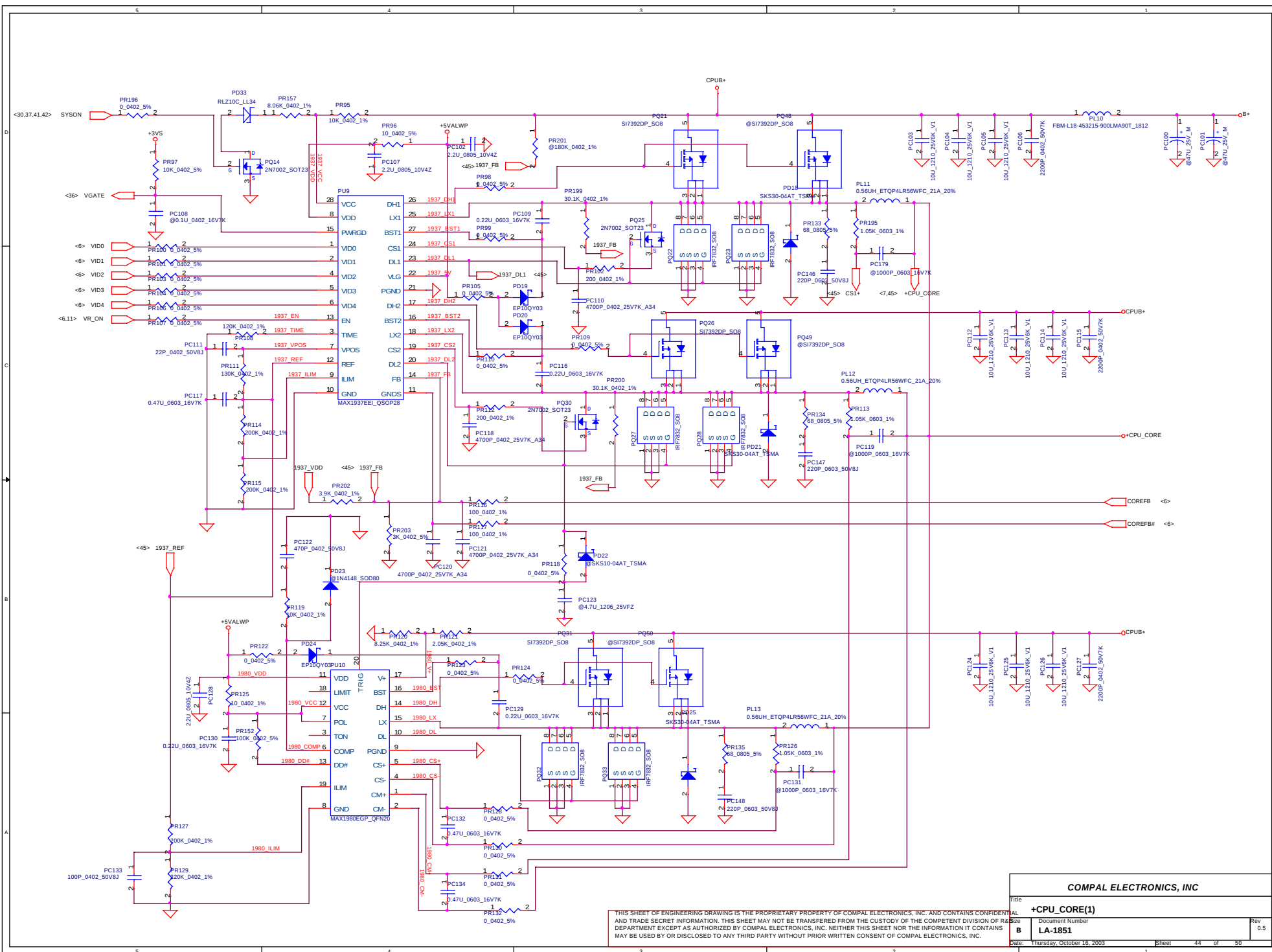
Title		
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Size	Document Number	Rev
B	LA-1581	0.5
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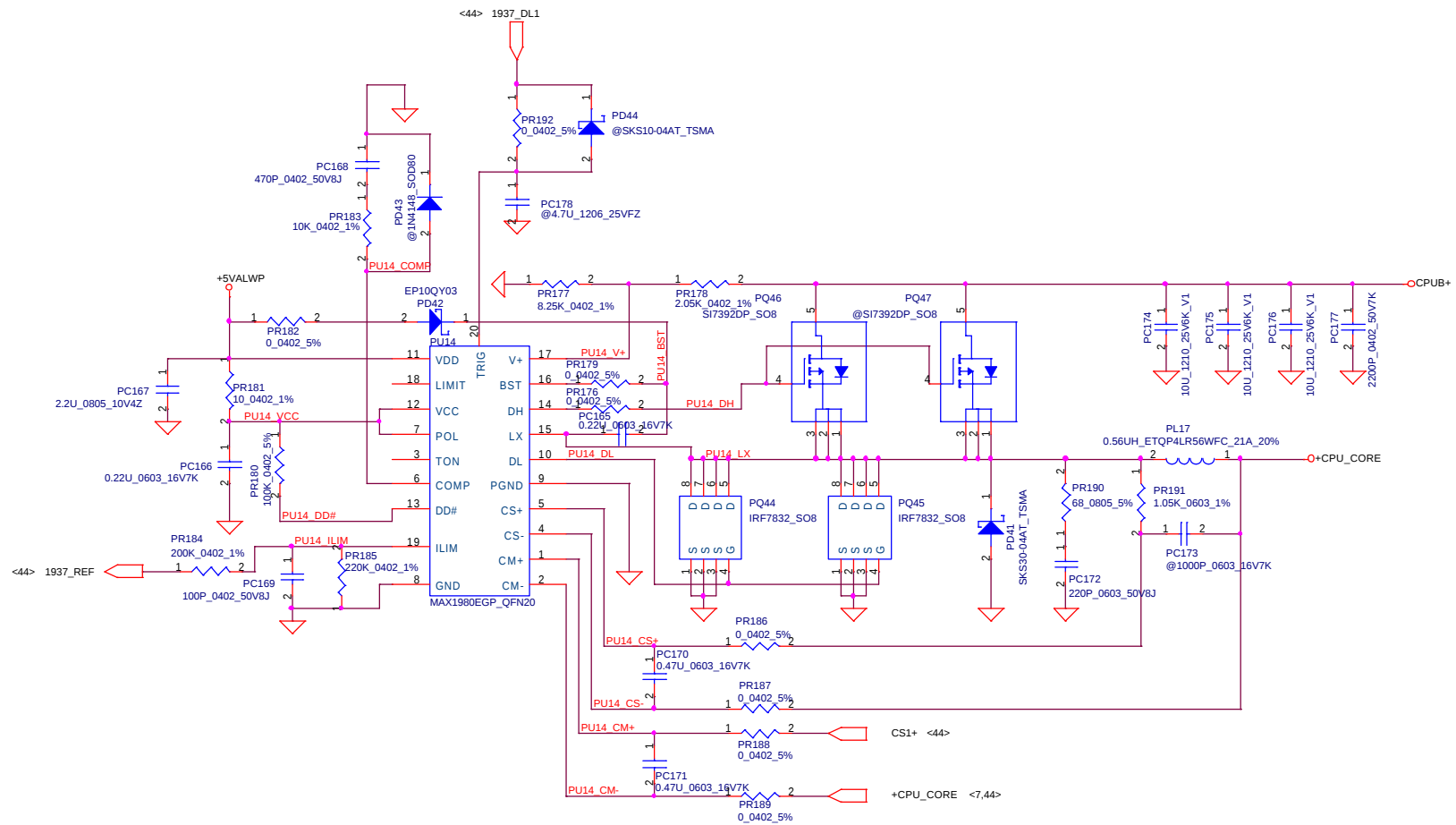
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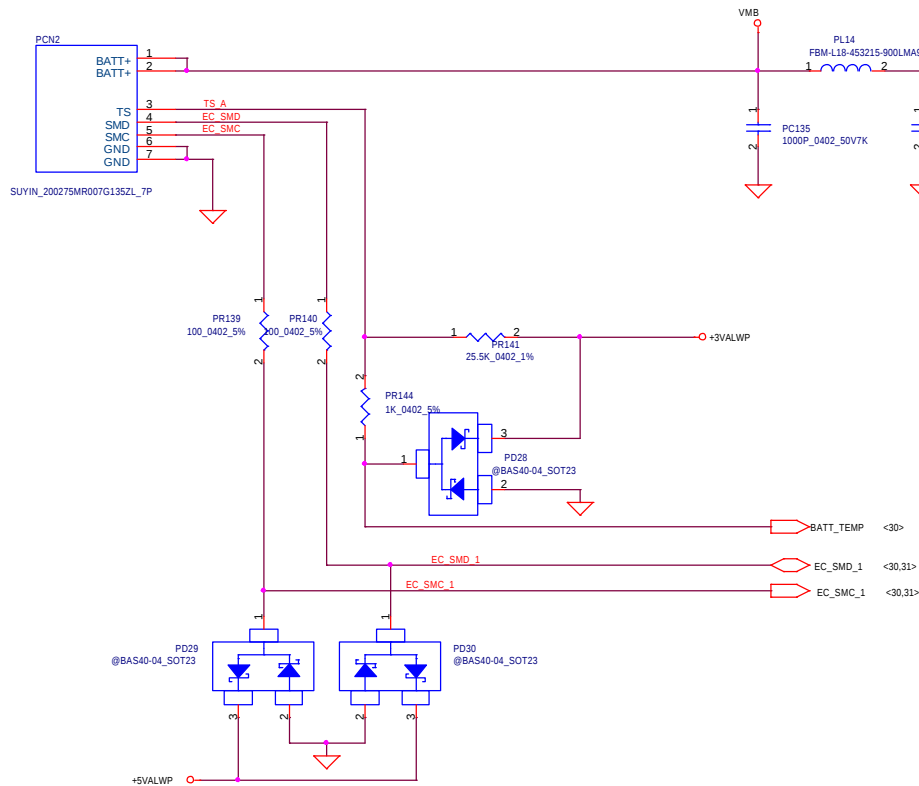
COMPAL ELECTRONICS, INC		
File	1.25V / VGA_CORE	
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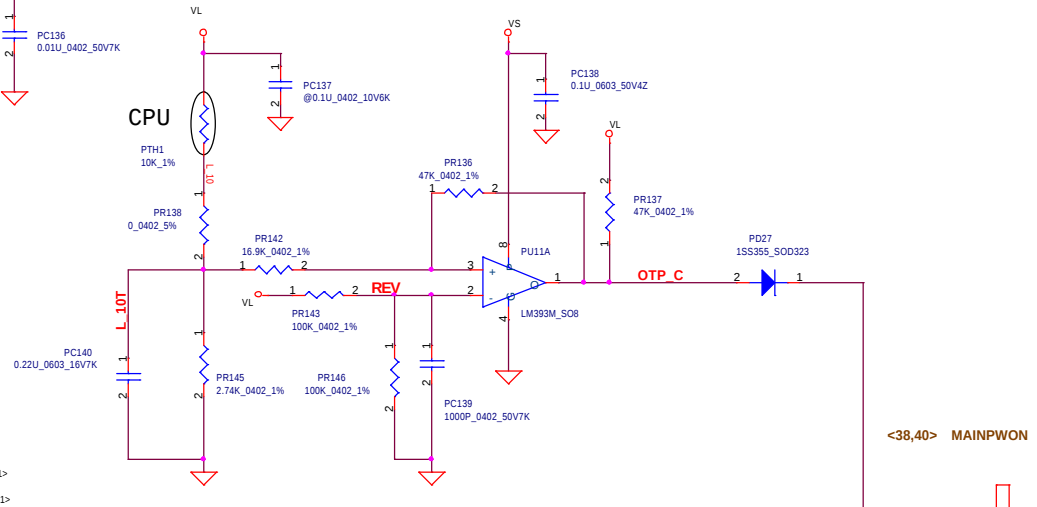


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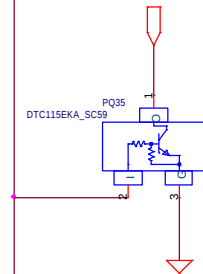
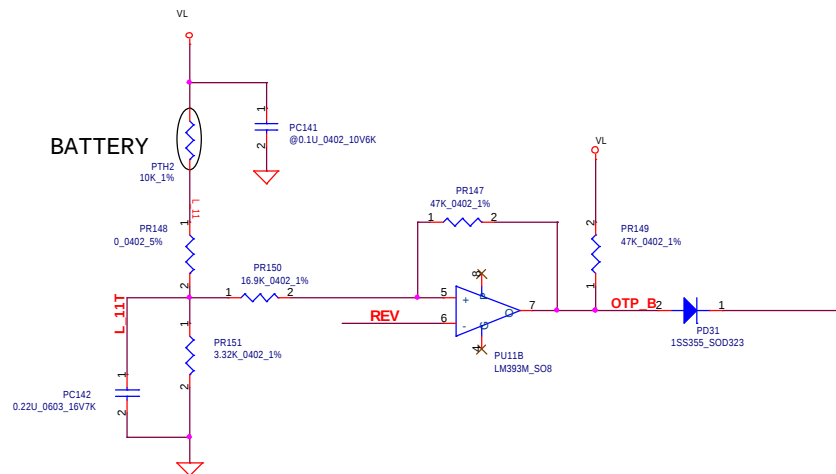
COMPAL ELECTRONICS, INC			
Title			
+CPU_CORE(2)			
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PH1 under CPU bottom side :
CPU thermal protection at 90 $\pm$ 3 degree C
Recovery at 50 $\pm$ 3 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 84 $\pm$ 3 degree C
Recovery at 45 $\pm$ 3 degree C



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COMPAL ELECTRONICS, INC			
File BATTERY CONN / OTP/1.8V			
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POWER PIR LIST

PHASE			
DB2	page	Reason for change	Modify list
	40	Modify 3V / 5V Vout and OCP	Change PR66 from 6.49K_0603_1% to 1.54K_0603_1% Change PR156 from 11.8K_0402_1% to 698_0402_1% Change PR154 from 4.12K_0603_1% to 0_0603_5% Change PC54, PC53 from 0.1U_0805_25V7K to 0.47U_0805_25V4Z Change PR62 from 5.76K_0603_1% to 1.27K_0603_1% Change PR155 from 27K_0603_1% to 1.24K_0603_1% Change PR153 from 4.7K_0402_1% to 619_0402_1%
	44,45	For CPU_CORE thermal issue	Change PQ21, PQ26, PQ31, PQ46 From IRLR7821 to SI7392DP Delete PD23, PD43, SC11N4148T8
	42	For 1.6V voltage accuracy	Change PR173 from 113K_0402_1% to 107K_0402_1%
	42	For layout pad issue	Change PC85, PC86 from 22U_1210_10V4Z to 22U_1206_10V4Z
	41	For power sequence setting	Add PR197, 680K_0603_1% Add PR198, 316K_0603_1%
	38	For solving cable dock shutdown issue	Add PD45, SKS80-04CT
SI	38	For thermal issue	Change PD45 from SKS80-04CT to SBM1040
	38	Change VIN detector sensing point because of DOCK issue	Change PR2 from 174K_0603_1% to 150K_0603_0.1% Change PR7 from 75k_0402_1% to 66.5k_0402_1%
	39	Improvment noise issue	
	41	Modify 2.5V / 1.5V OCP	Change PR87 from 24.9k_0402_1% to 57.6k_0402_1% Change PR88 from 0_0603_1% to 13.7k_0402_1% Add PR89, 100k_0402_1%
	43	VGA with 32M VRAM	Remove 1.35V regulator that is for VGA with 64M VRAM
	44,45	Modify CPU_CORE current balance issue	Change the connection of PC122 and PC168 from 14 pin of PU9 to ground. Remove PD22 and PD44.
PV	38	Improve the VIN detector accuracy.	Change PR1, PR2, PR5, PR7, PC6, and re-connect the reference voltage that is VL connected to PR10 to RTC charger output.
	39	Improve the accuracy of Constant Voltage mode of charger.	Change PR48, PR49
	41	reserve devices for the adjustment of 2.5V	Add PR204, PR205, PR206, PC181, PC182
	44	Improve the transient response	Add PR203, PC111, and remove PR202

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		AMD change Tdiode spec up to 127 degree	P4	Change U3 from MAX6649 to ADM1032	0.4
2		Support wake from Lan	P20	Populate R188	0.4
3		To avoid PCI1620 unknow action	P22	Reserve R591	0.4
4		To restrain audio noise	P25	Change R267 pull up to +5VAMP_CODEC, and delete C626	0.4
5		USB_OC# high should be between 2.5V to 5.5V	P27	Change R310 and R315 to 10K / R314 and R319 to 20K	0.4
6		To detect FIR	P29	Add R592 and R593	0.4
7		TP should be pull up to +5V	P30	RP80 pull up to +5V	0.4
8		In order to compatible with NS97551 -- changing pin87 ~ 90 to GPIO	P30	BID routed from pin88 to pin82	0.4
9		In order to compatible with NS97551 -- removing +RTCVCC	P30	Add R594 and R595	0.4
10		To prevent noise generated from FAN to +5VS cause audio noise while shut down	P4	Delete D1 and D3 / add C3, C8, C612, and C614	0.4
11		Solve for PCI1620 working abnormal -- fine tune G_RST# timing	P22	Populate R587, delete R225, C410	0.4
12		Double mount issue, already exist at audio board.	P30	Delete D28 and D29	0.4
13		Fast power on for battery only	P33	Change R392 from 100K to 4.7K	0.4
14		Presario LED color should be amber	P35	Change D39, D40, D42, D44, and D45 from XX_GRN to XX_ORG	0.4
15		To develop S19182 max effect	P25	Change C438 from 0.01UF to 0.1UF	0.4
16		For EMI	P26	Add L40, L41, L42, and L43 / delete C473, C474, C475, and C476	0.4
17		For VGA HSYNC/VSYNCR average peak to peak issue	P18	Add R159 and R160	0.4
18		For 512MB non-JEDEC module (16 chips)	P9	Change RP42, RP46, and R481 from 68 Ohm to 47 Ohm	0.4

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P.I.R HISTORY			
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		To use the same source as HR60	P4	Change U3 footprint to SOP8	0.5
2		To reset CK8 while boot up control by EC	P12	Add R97 to link EC_RSMRST# and PWRGD_SB	0.5
3		For EMI	P15	Change C648, C672, C685, C696, C699, C763, and C656 to 1000P Change C651, C673, C686, C697, C700, C764, C654, C733, C710, C730, C706, and C724 to 10P	0.5
4		To solve voltage level of HSYNC and VSYNC is over spec	P18	Add U46 and U47, and R596, R597, and R598 on CRT_HSYNC and CRT_VSYNC	0.5
5		Solve for data lost while transfer data from LAN	P20	Change U9 from NS0013 to NS0019	0.5
6		T1 recommendation --- avoid unknow state while initiate	P22	Populate R591	0.5
7		Mechanical restricted area	P25	R263 and R264 change footprint to R_0402	0.5
8		For EMI	P25	L39 and R293 change to CHB1608U301_0402	0.5
9		For EMI	P26	L40, L41, L42, and L43 change to KC FBM-L11-201209-221LMAT_0805	0.5
10		nVIDIA recommendation for WOR	P27	Add U48, C807, R599, and R600	0.5
11		Due to MD_SPK is no longer use, so prevent input pin floating.	P25	Delete R287 and change R288 to 0_0402_5%. Also add C808.	0.5

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P.I.R HISTORY			
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