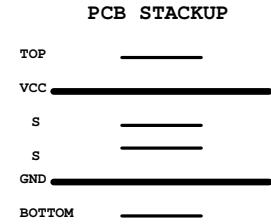
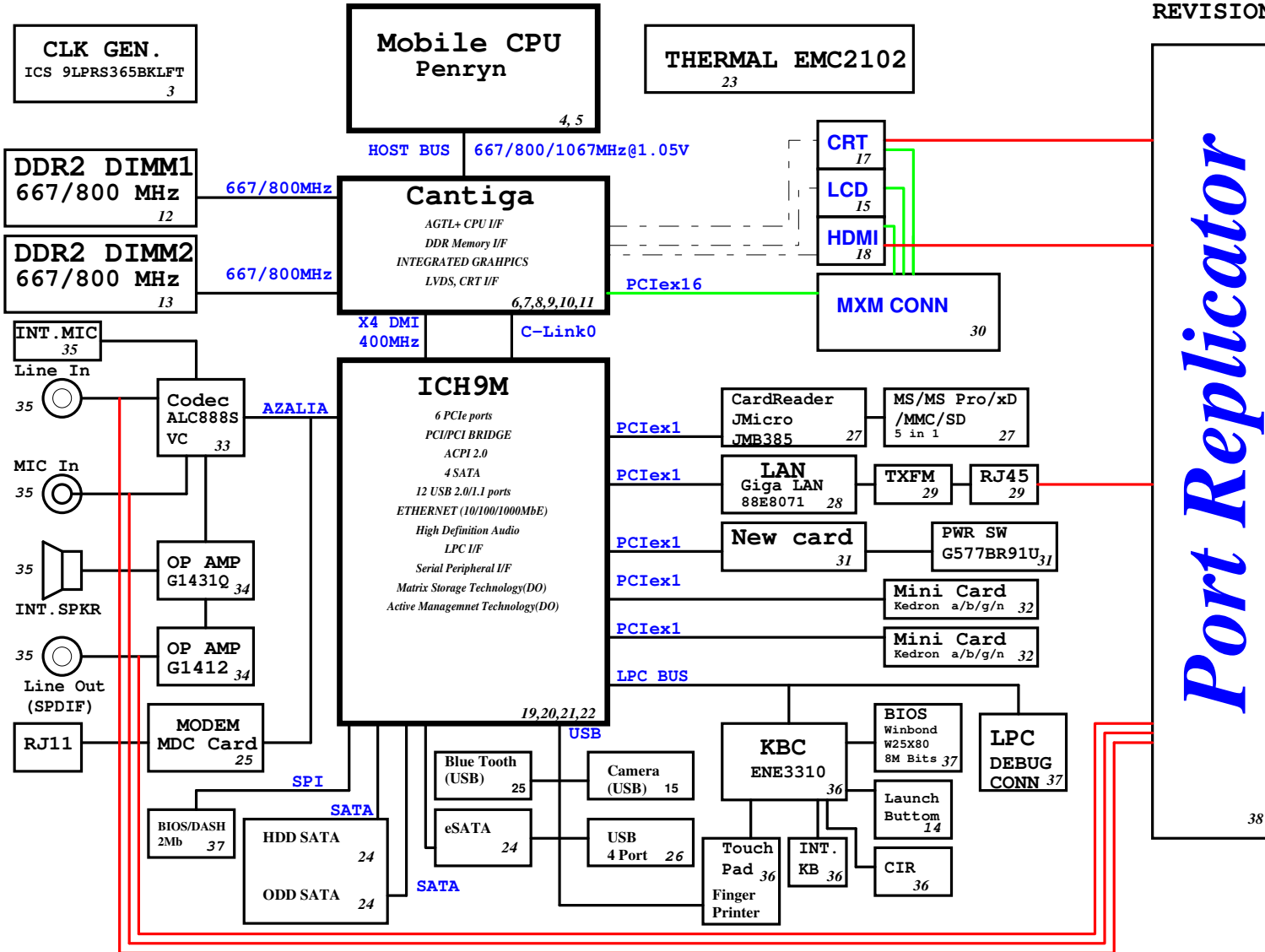


Eiger Block Diagram

Project code: 91.4Z501.001
 PCB P/N : 48.4Z501.001
 REVISION : 07246- -1



Port Replicator

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A 44	
1D8V_S3	1D5V_S0
G9131 44	
3D3V_S0	2D5V_S0
GFXCORE DC/DC ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V
CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V
CHARGER BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high, the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]: (3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]: (3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/IHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

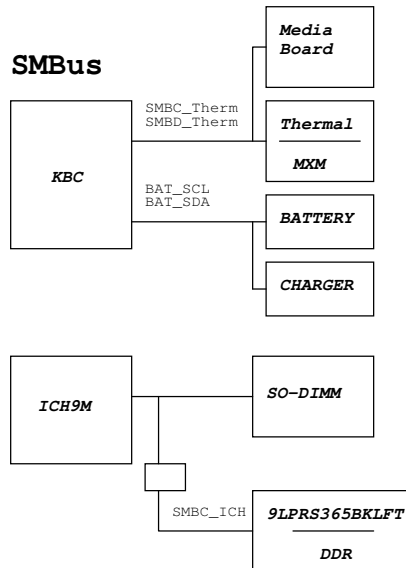
PCIe Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	NC

USB Table

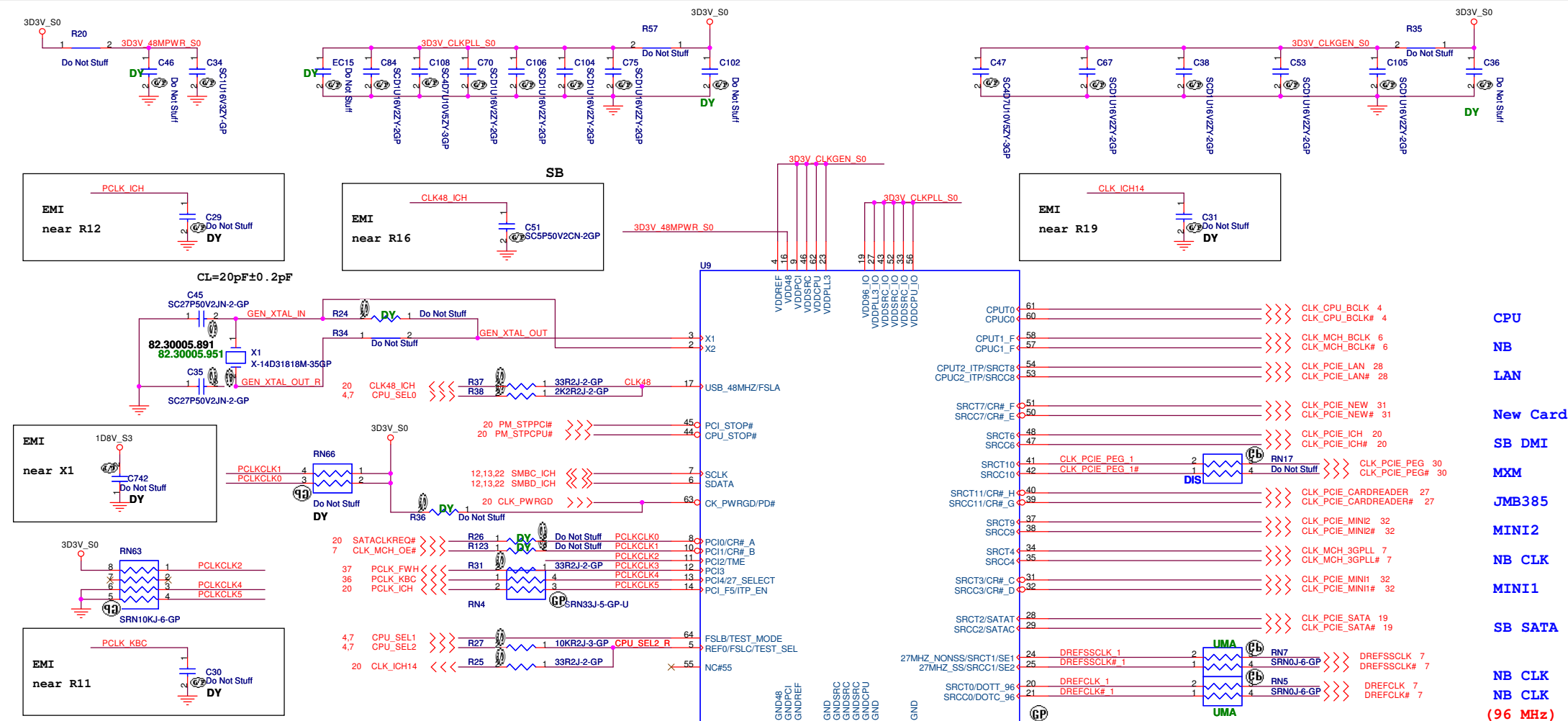
USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	USB5 (DOCK)
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Title	Document Number		Rev
Size A3	Eiger		-1
Date: Tuesday, April 01, 2008	Sheet 2	of	50



ICS9LPRS365BKLF1T setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 6 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

UMA

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

Size: Document Number: **Eiger** Rev: -1

Date: Tuesday, April 01, 2008 Sheet 3 of 50

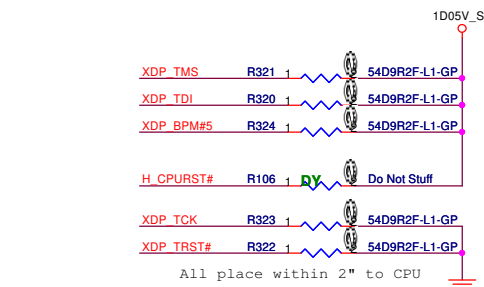
6 H_A#(35..3) <<< H_A#(35..3)

H_DINV#(3..0) <<< H_DINV#(3..0) 6
H_DSTBN#(3..0) <<< H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<< H_DSTBP#(3..0) 6
H_D#(63..0) <<< H_D#(63..0) 6

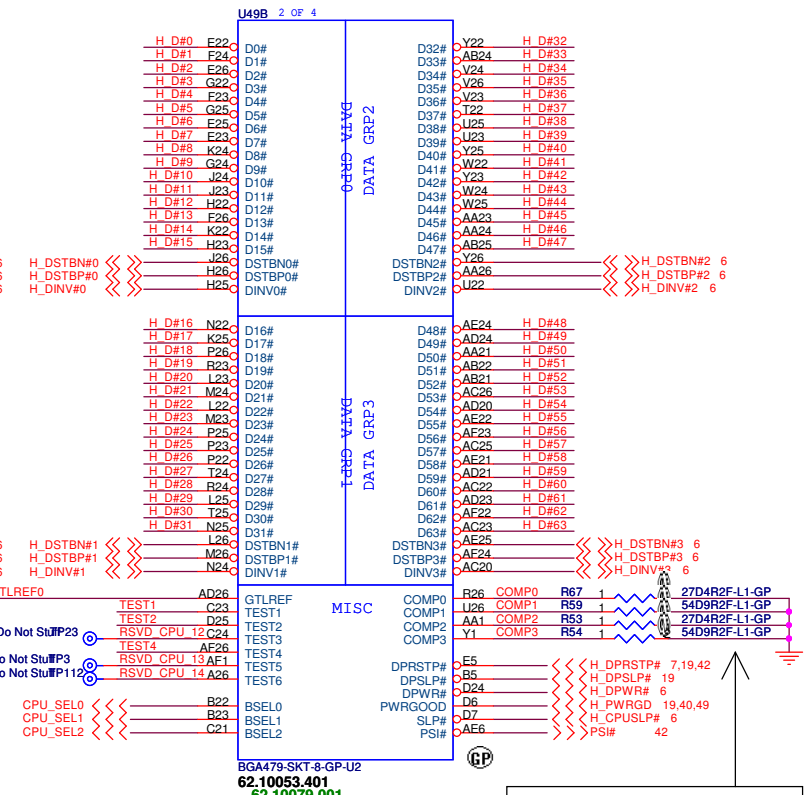
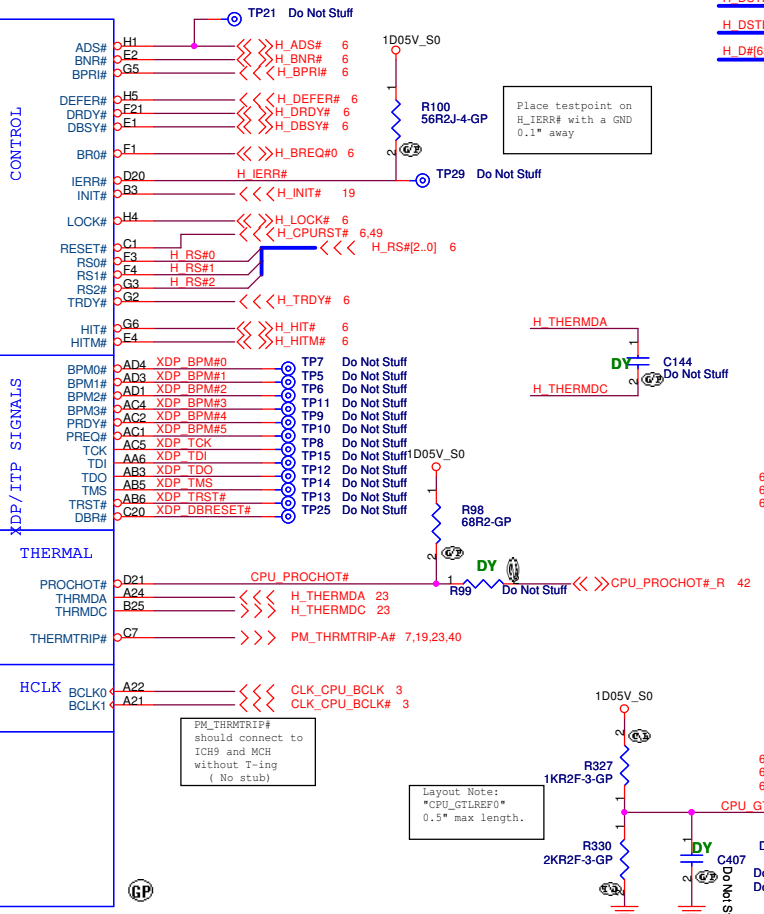
Side Band Non GTL

6 H_ADSTB#1 <<<
19 H_A20M# <<<
19 H_FERR# <<<
19 H_IGNNE# <<<
19 H_STPCLK# <<<
19 H_INTR <<<
19 H_NMI <<<
19 H_SMI# <<<

Do Not Stuff#19 RSVD CPU 1 M4
Do Not Stuff#18 RSVD CPU 2 N5
Do Not Stuff#17 RSVD CPU 3 T2
Do Not Stuff#16 RSVD CPU 4 V3
Do Not Stuff#27 RSVD CPU 5 V3
Do Not Stuff#31 RSVD CPU 6 C3
Do Not Stuff#24 RSVD#C3
Do Not Stuff#28 RSVD#D2
Do Not Stuff#26 RSVD#D3
Do Not Stuff#22 RSVD#F6
Do Not Stuff#32 RSVD CPU 11 B1



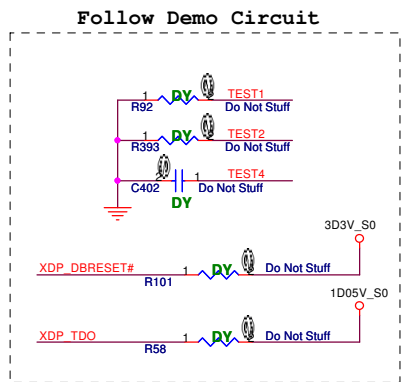
All place within 2" to CPU



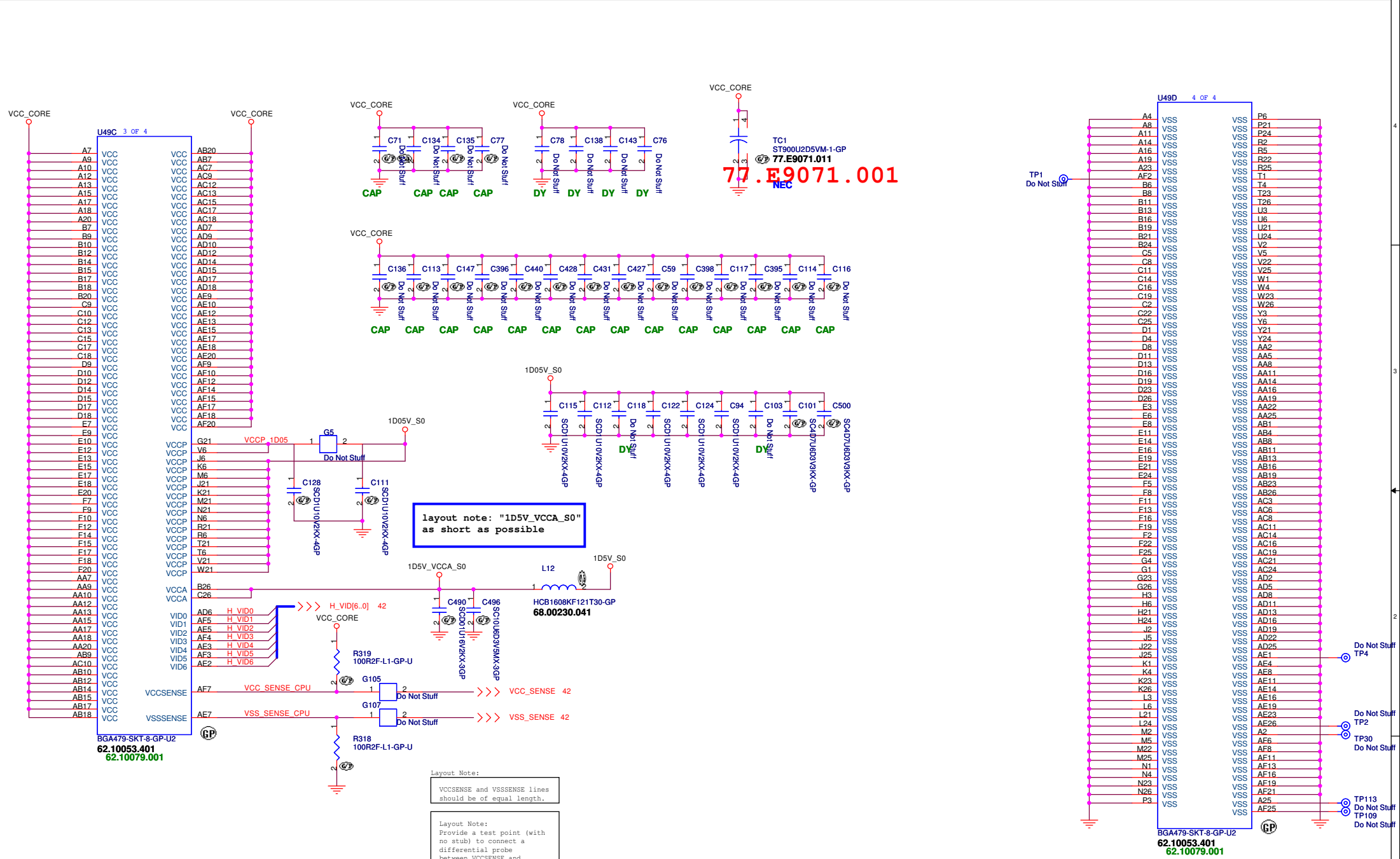
Layout Note: *CPU_GTLREF0* 0.5" max length.

Layout Note: Comp0, 2 connect with 20-27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with 20-55 ohm, make trace length shorter than 0.5".

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals



Wistron Corporation logo and contact information. Title: CPU (1 of 2). Date: Tuesday, April 01, 2008. Sheet 4 of 50.



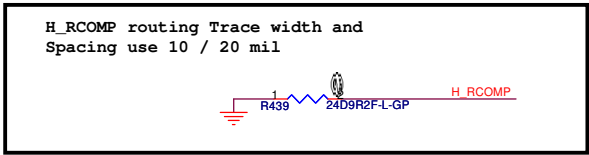
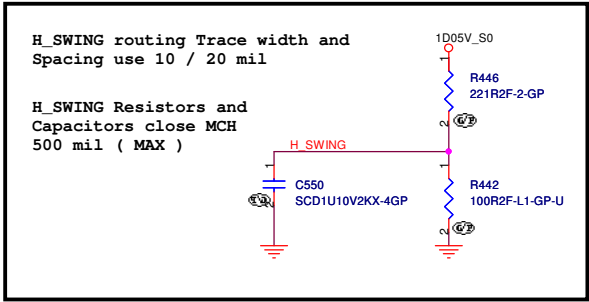
layout note: "1D5V_VCCA_S0"
as short as possible

Layout Note:
VCCSENSE and VSSSENSE lines
should be of equal length.

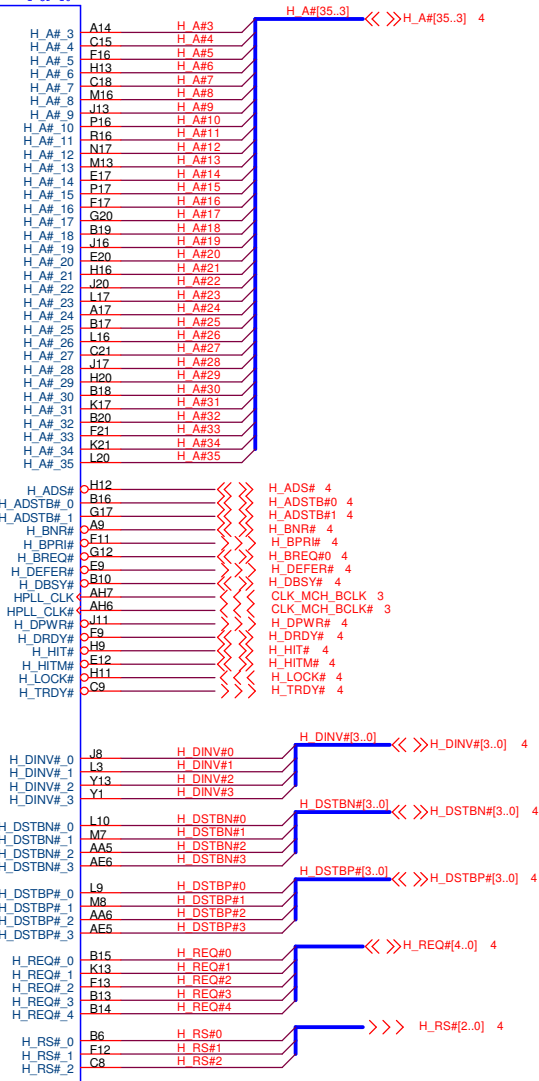
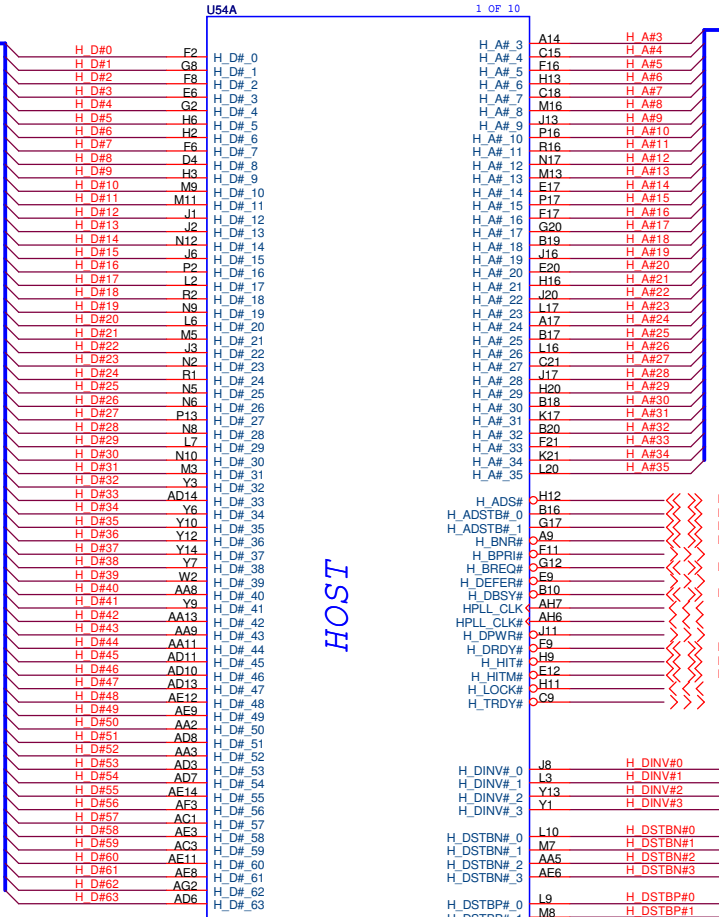
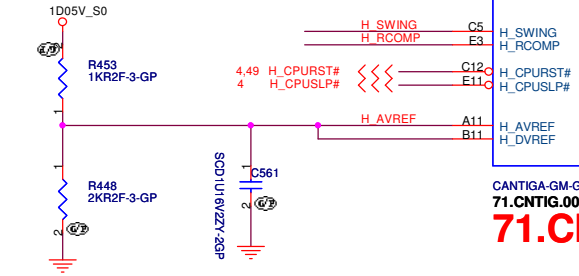
Layout Note:
Provide a test point (with
no stub) to connect a
differential probe
between VCCSENSE and
VSSSENSE at the location
where the two 54.9ohm
resistors terminate the
55 ohm transmission line.

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Taipei Hsien 221, Taiwan, R.O.C.

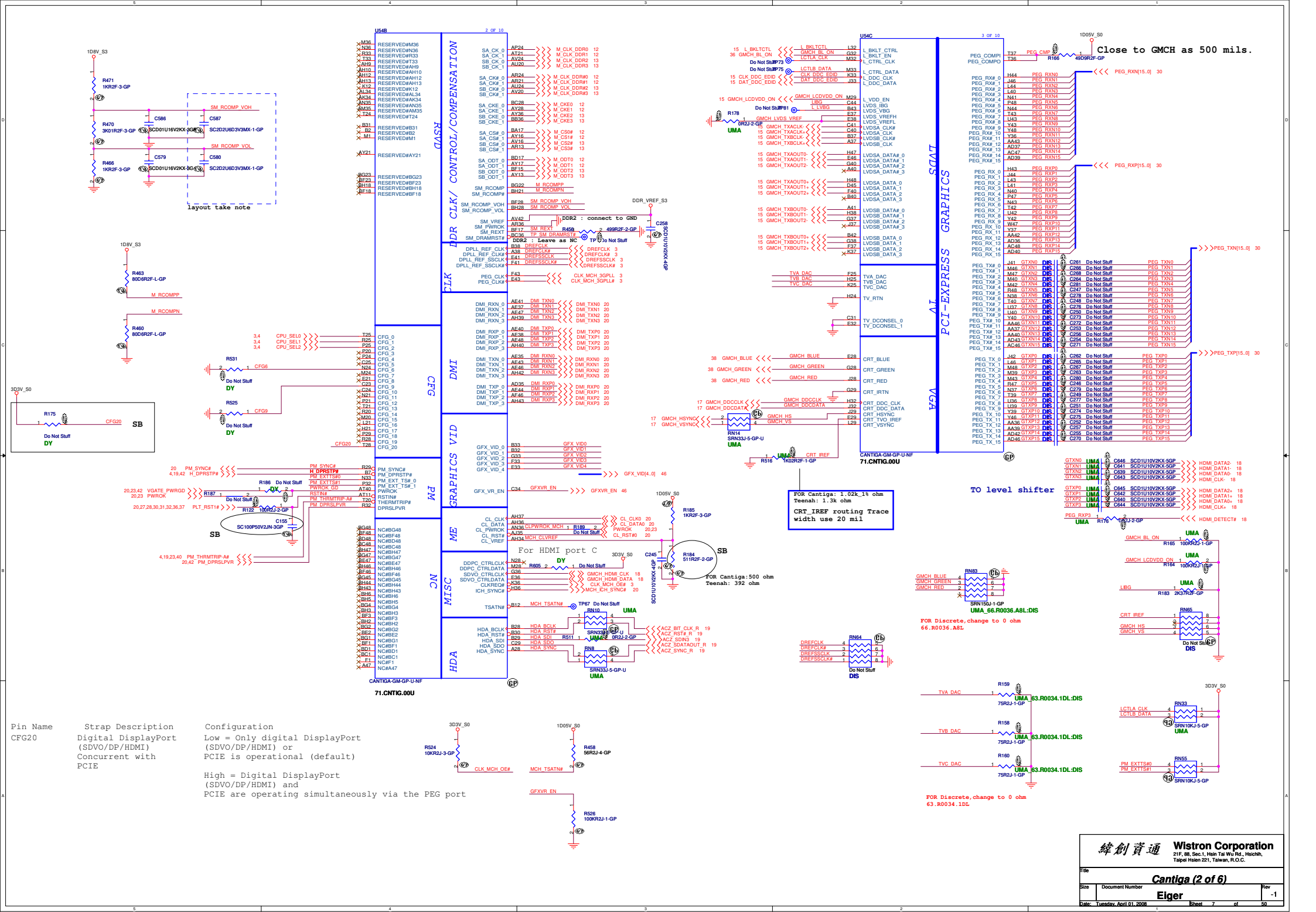
Title		
CPU (2 of 2)		
Size	Document Number	Rev
	Eiger	-1
Date: Tuesday, April 01, 2008	Sheet 5 of 50	



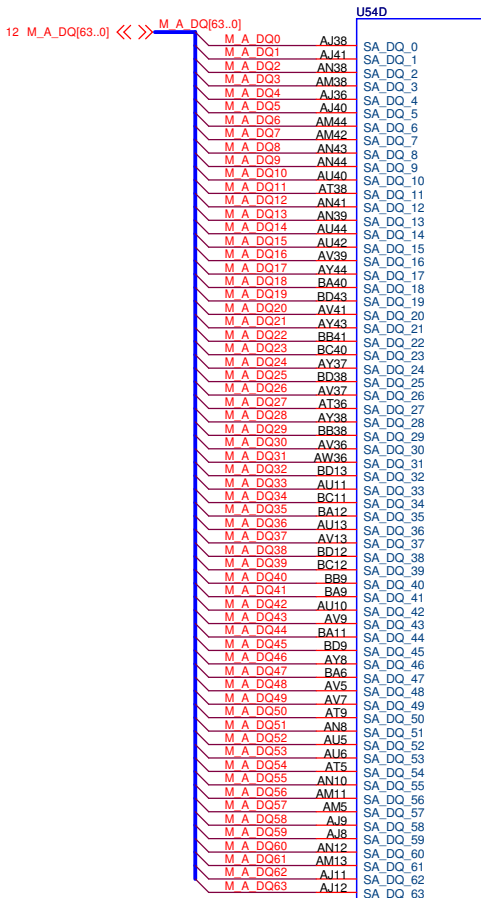
Place them near to the chip (< 0.5")



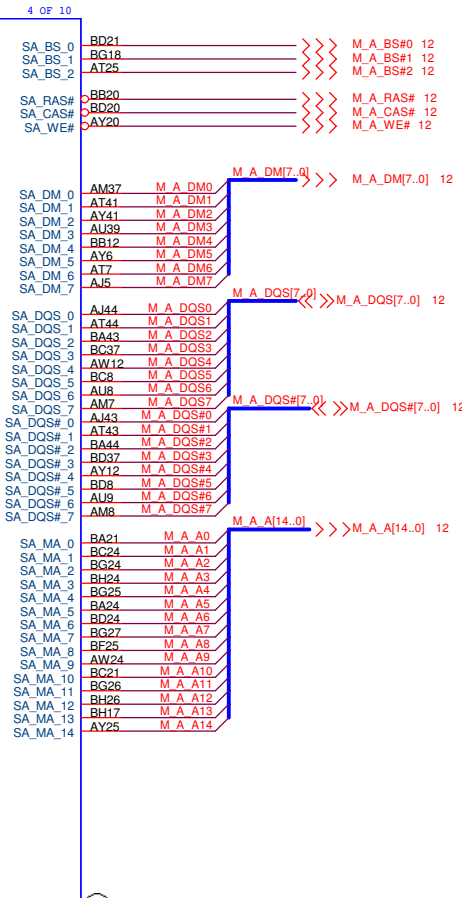
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71.CNTIG.00U
71.CNTIG.D1U



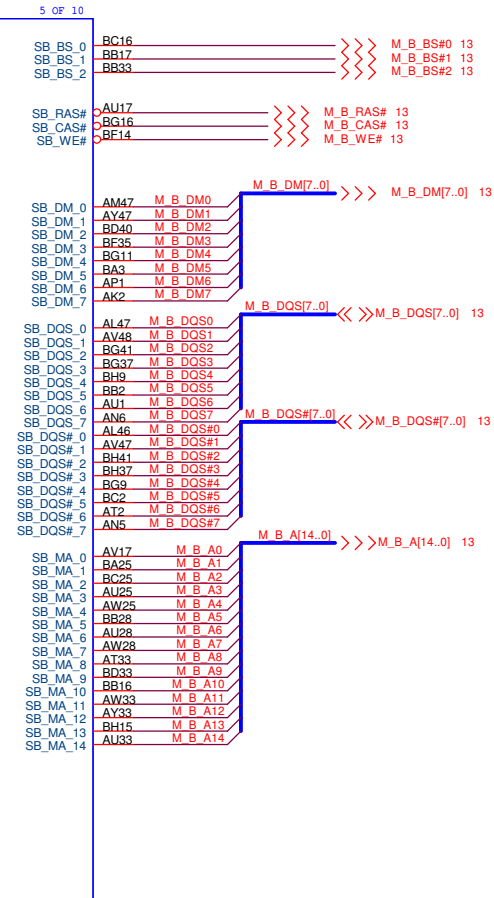
Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI)	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default)
	Concurrent with PCIE	High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG strap



DDR SYSTEM MEMORY A

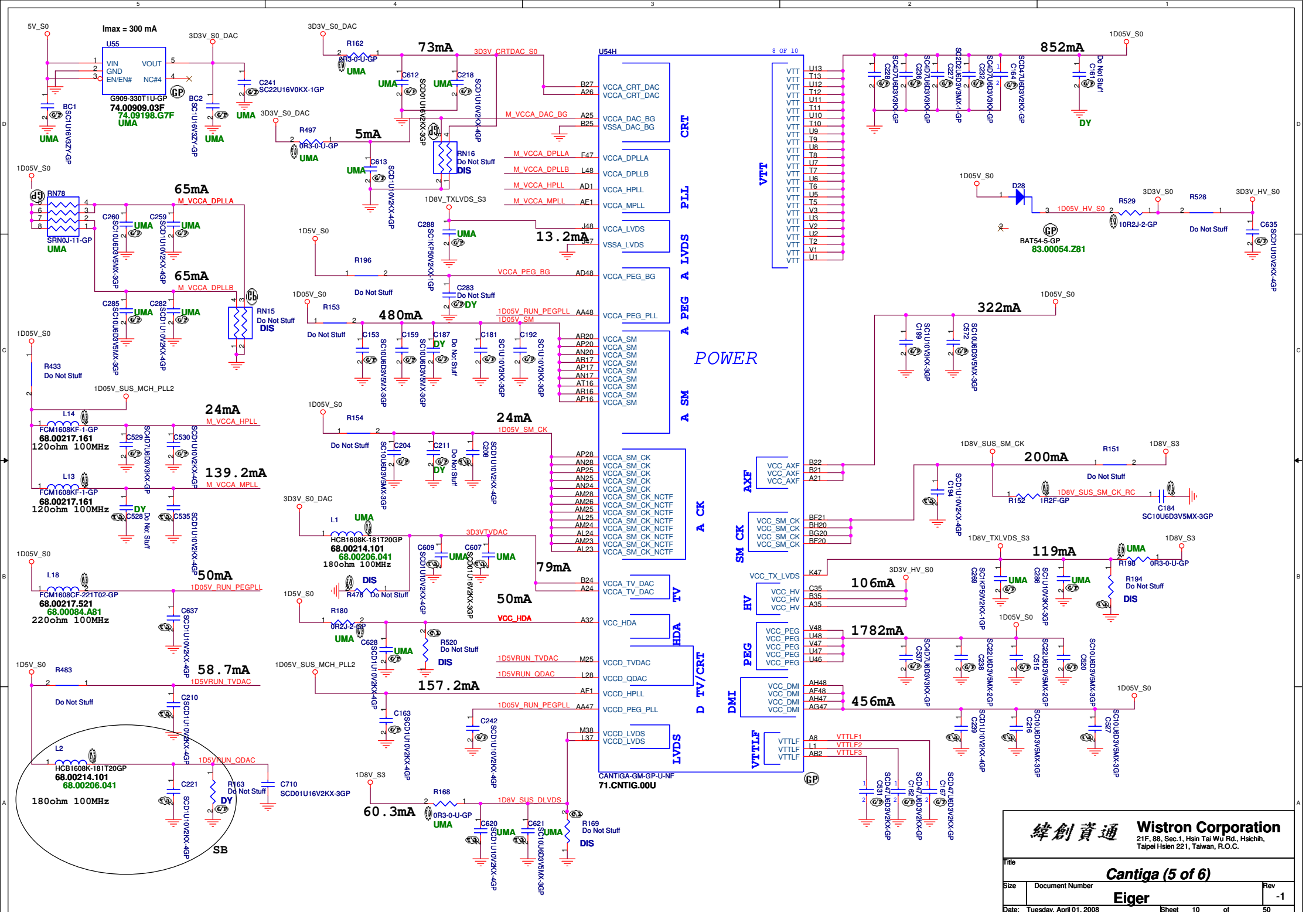


DDR SYSTEM MEMORY B



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

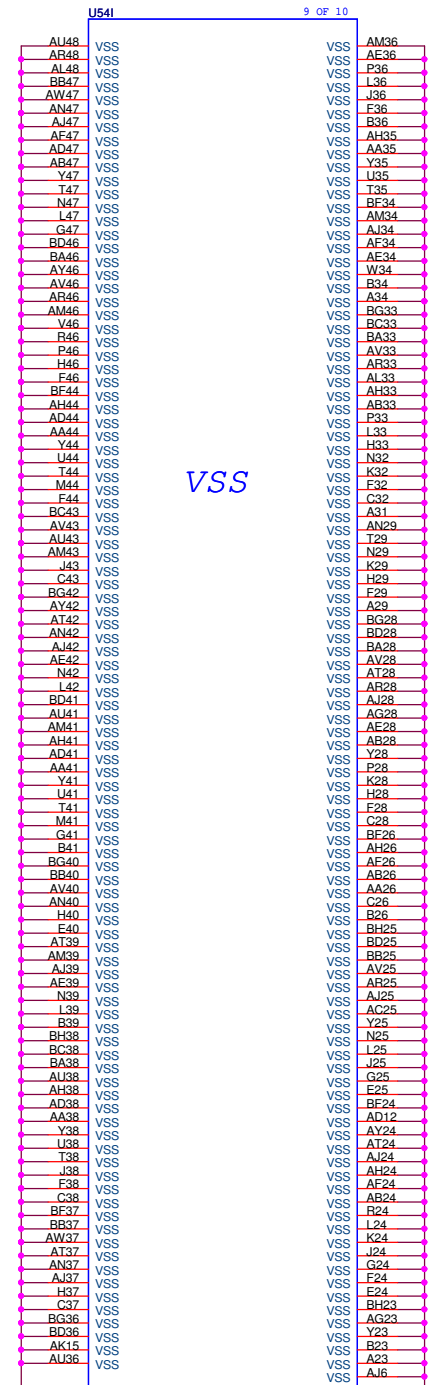
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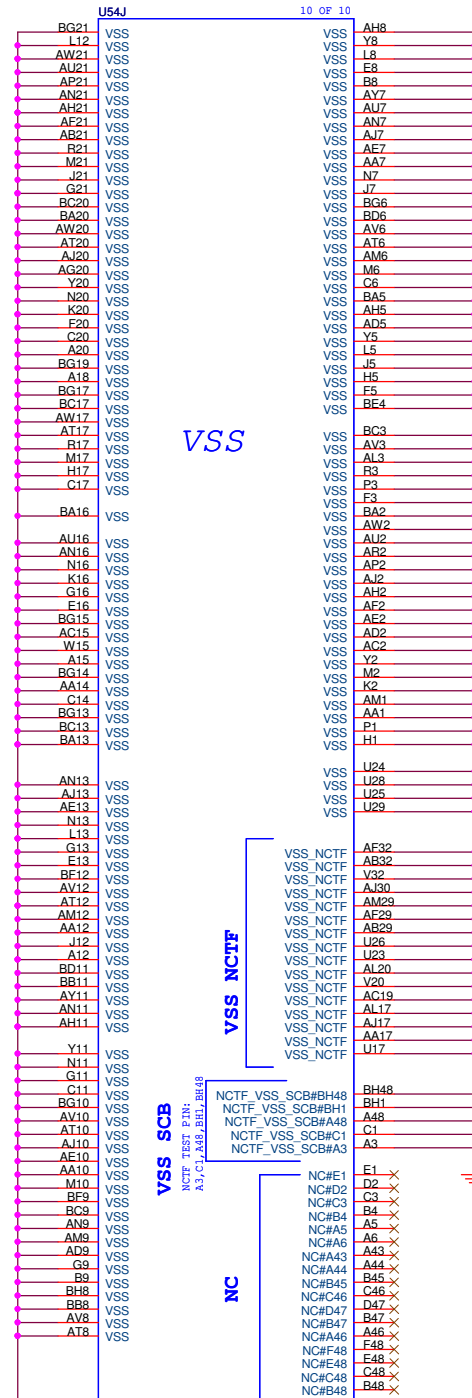
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Title		Cantiga (5 of 6)	
Size	Document Number	Rev	
Date: Tuesday, April 01, 2008		Sheet 10 of 50	

Eiger -1



CANTIGA-GM-GP-U-NF
71.CNTIG.00U



CANTIGA-GM-GP-U-NF
71.CNTIG.00U



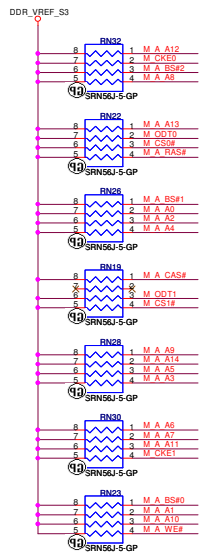
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
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Title: **Cantiga (6 of 6)**

Size: Document Number Rev: -1

Date: Tuesday, April 01, 2008 Sheet 11 of 50

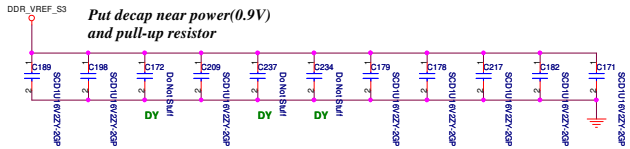
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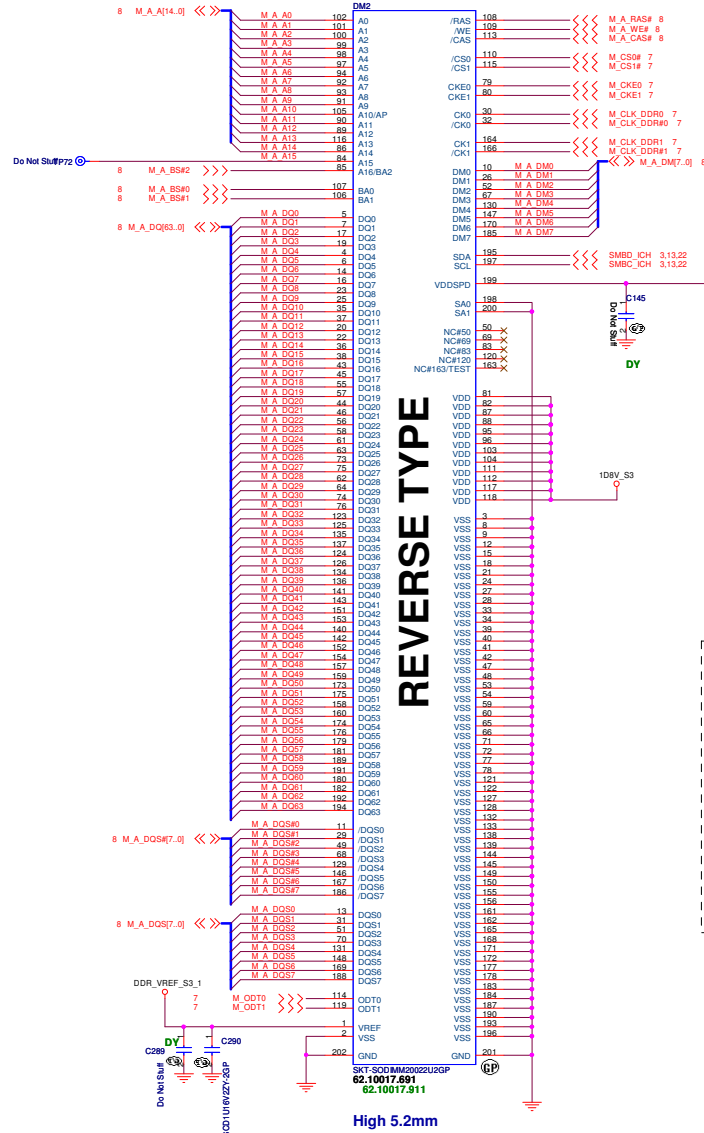
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

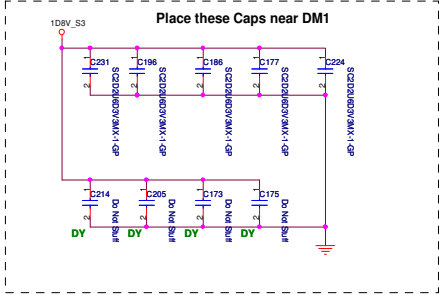
Decoupling Capacitor



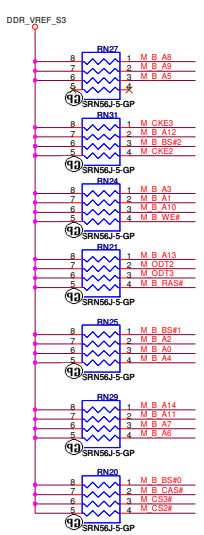
Put decap near power(0.9V) and pull-up resistor



REVERSE TYPE



High 5.2mm

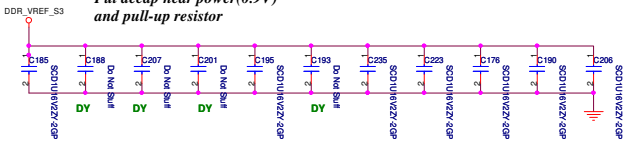


PARALLEL TERMINATION

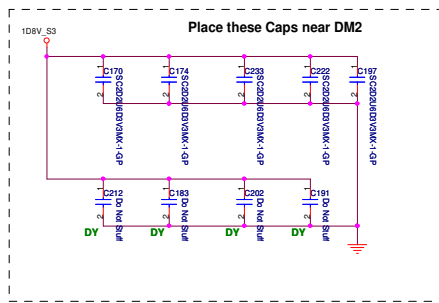
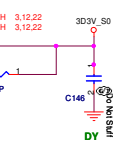
Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

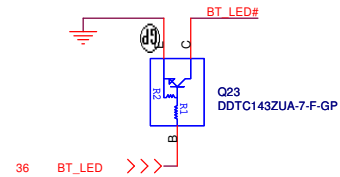
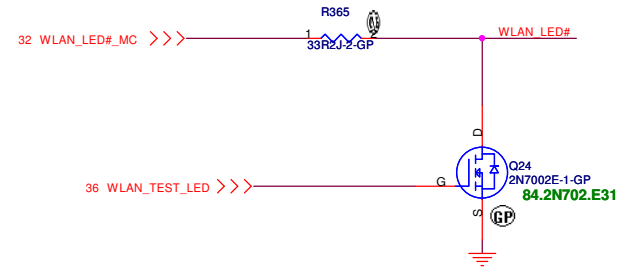
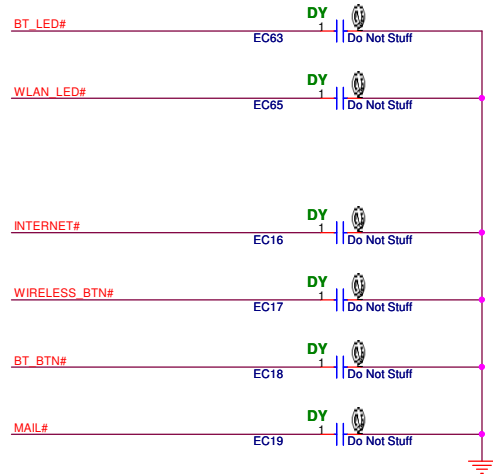
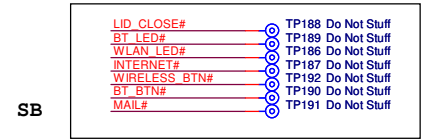
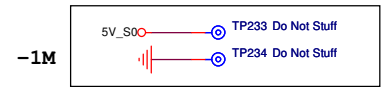
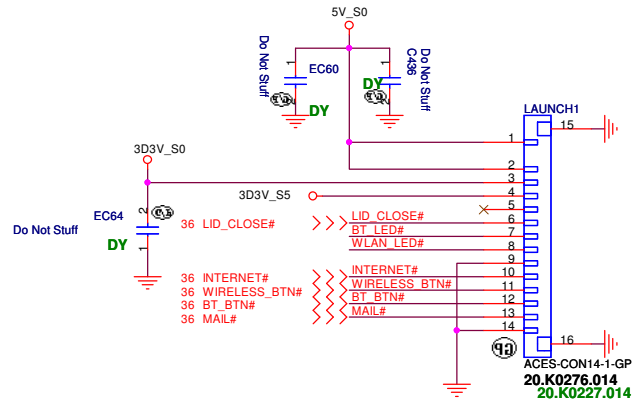
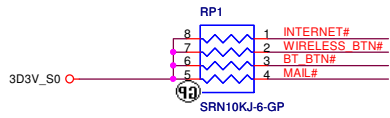
Put decap near power(0.9V) and pull-up resistor



REVERSE TYPE



High 9.2mm



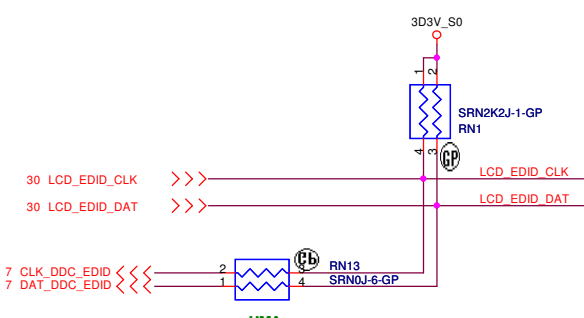
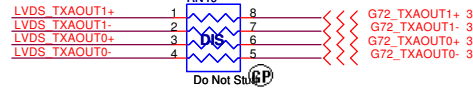
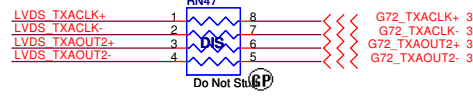
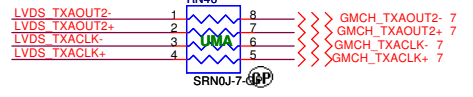
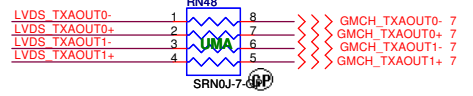
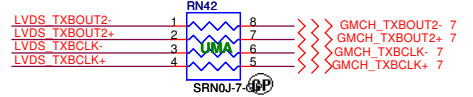
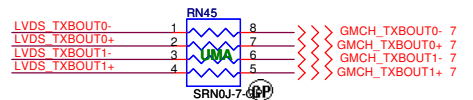
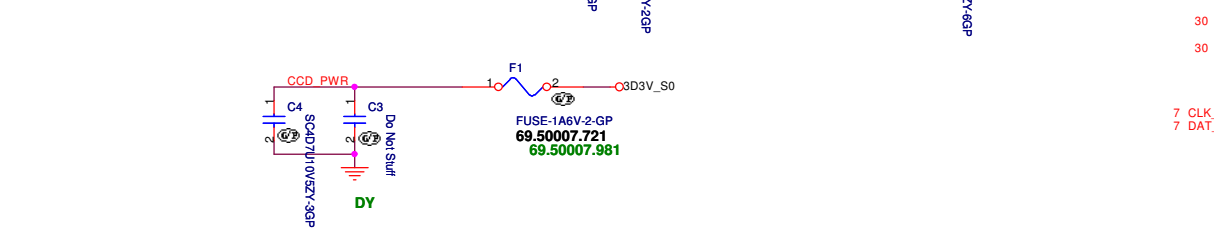
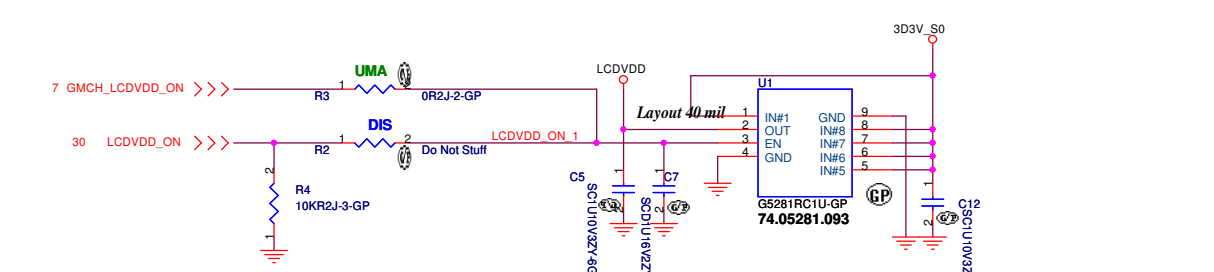
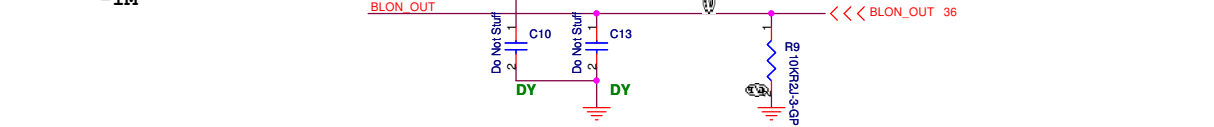
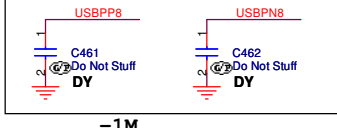
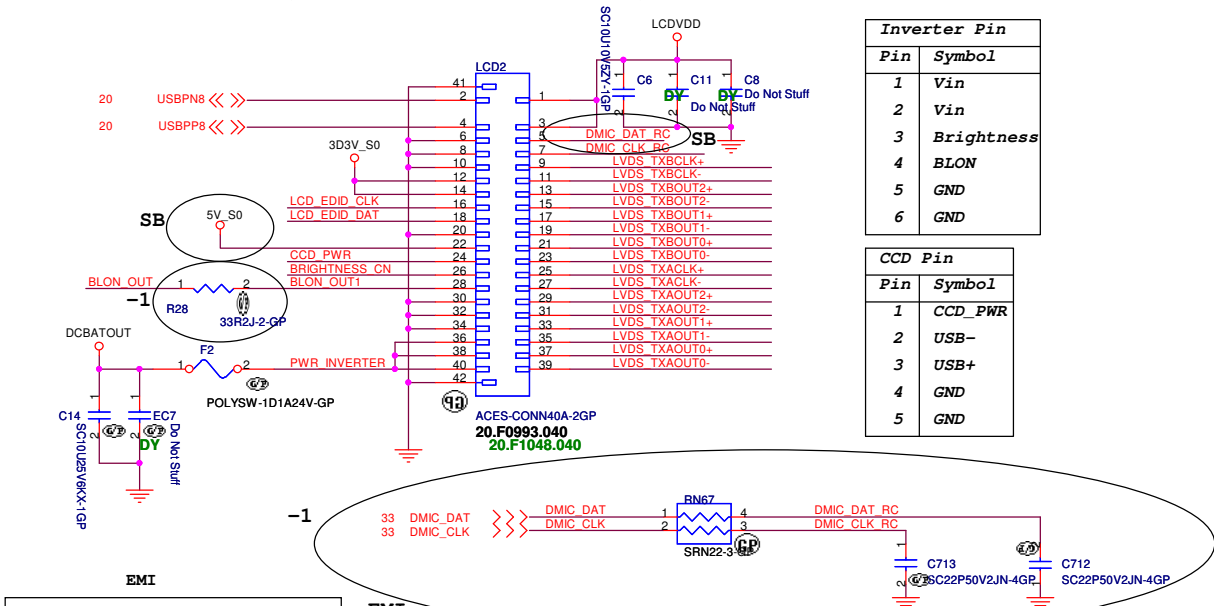
UMA

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LAUNCH	
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LCD/INVERTER/CCD CONN

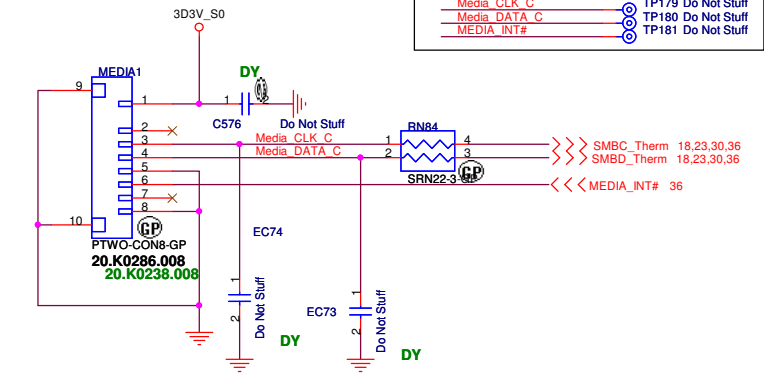
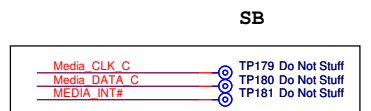
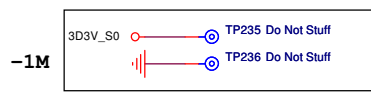
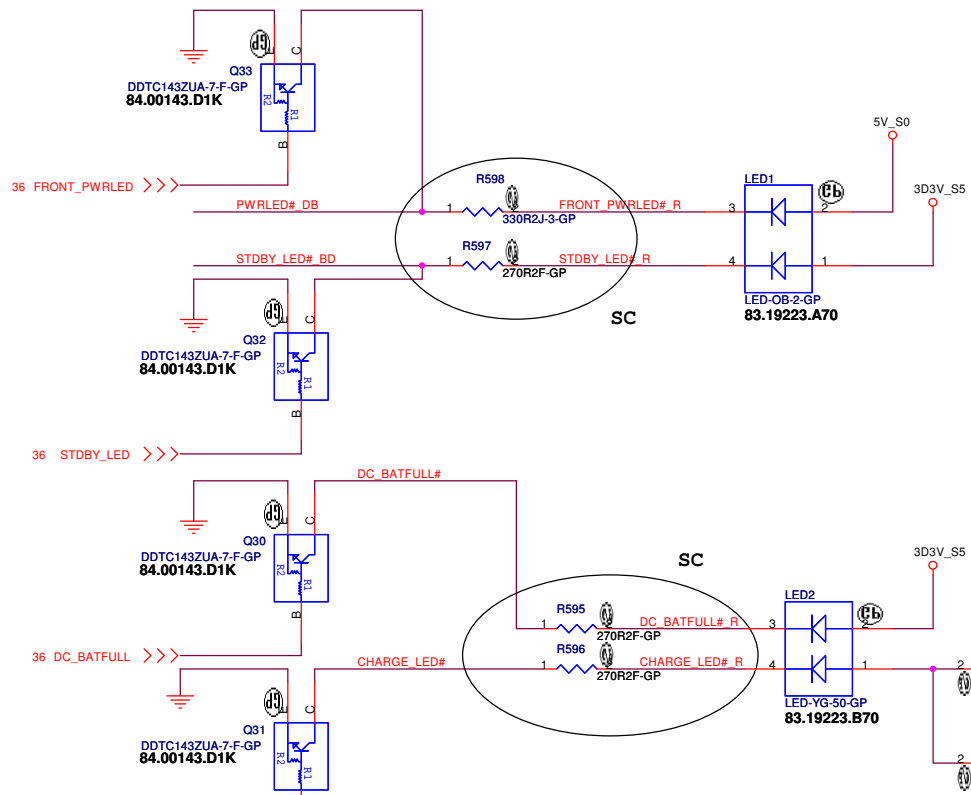
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

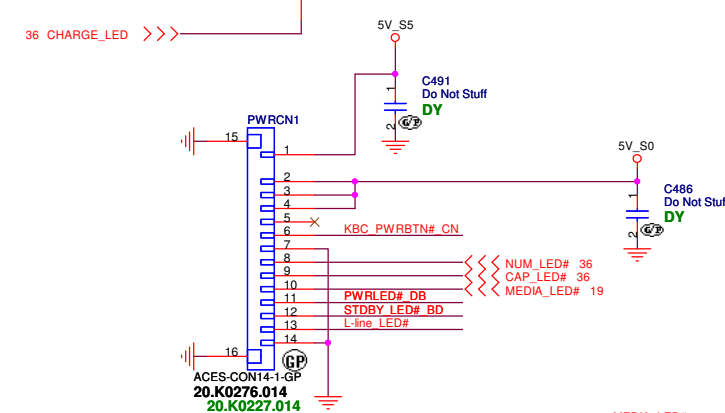


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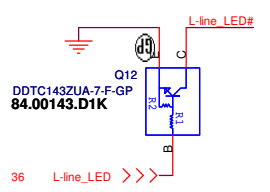
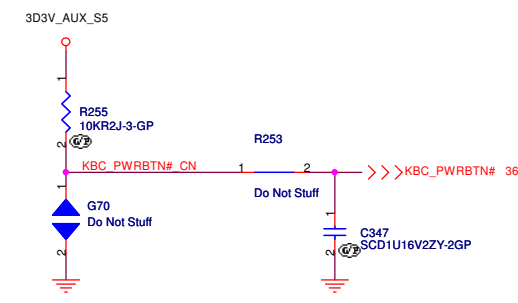
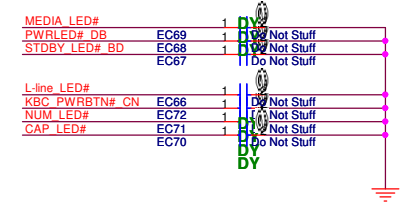
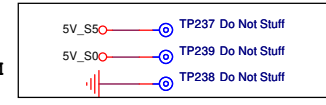
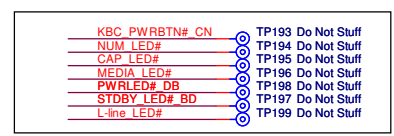
LCD CONN	
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MEDIA BOARD



SB



UMA

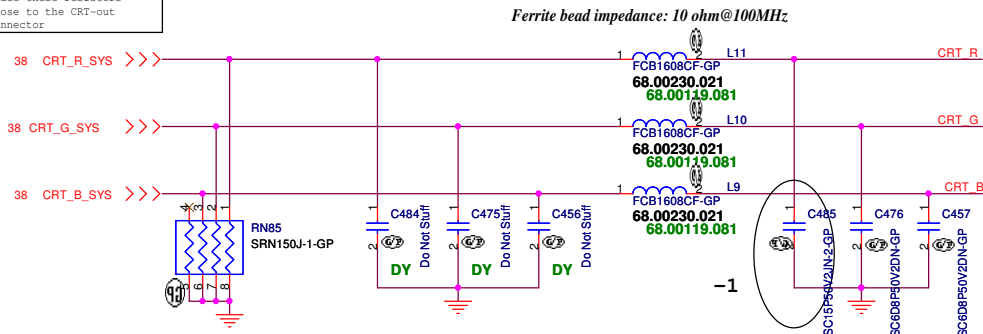
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Title: **Power & Media Board**

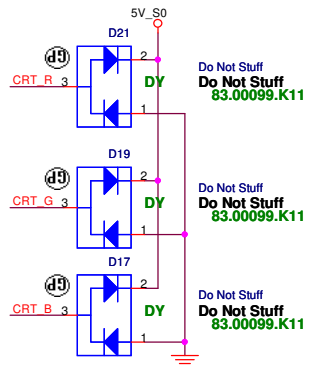
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Layout Note:
Place these resistors
close to the CRT-out
connector

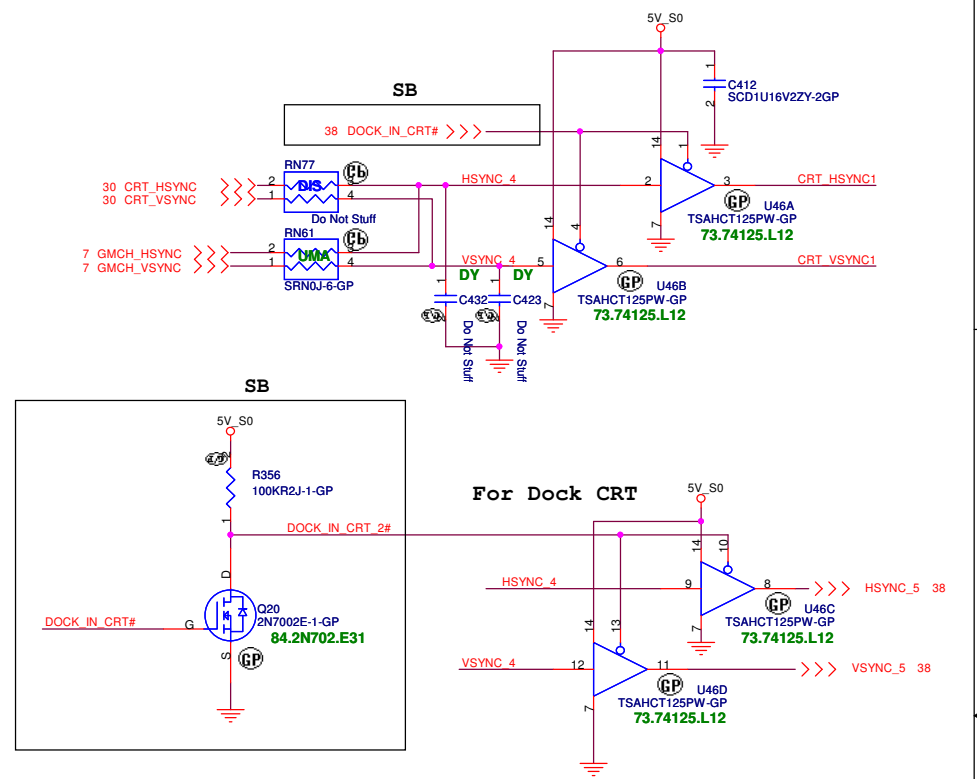


Ferrite bead impedance: 10 ohm@100MHz:

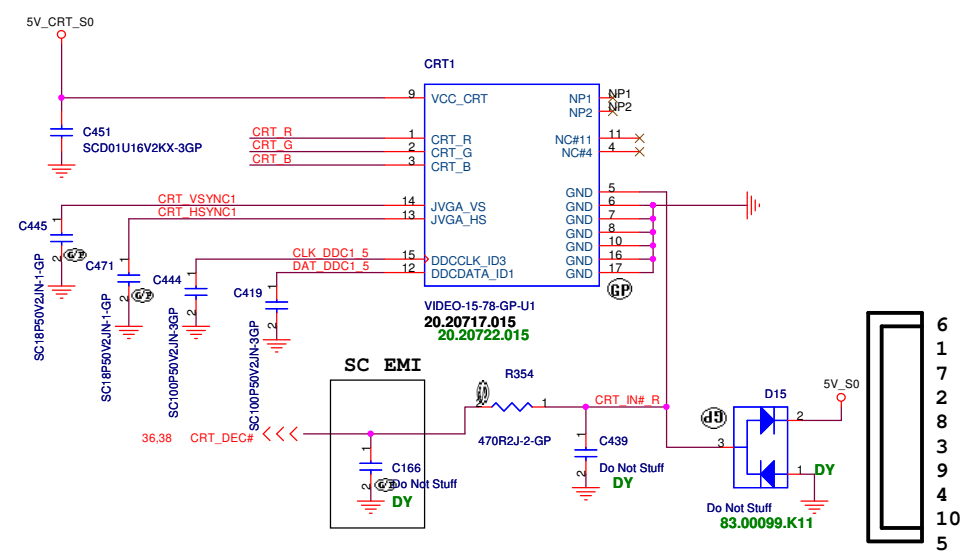


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

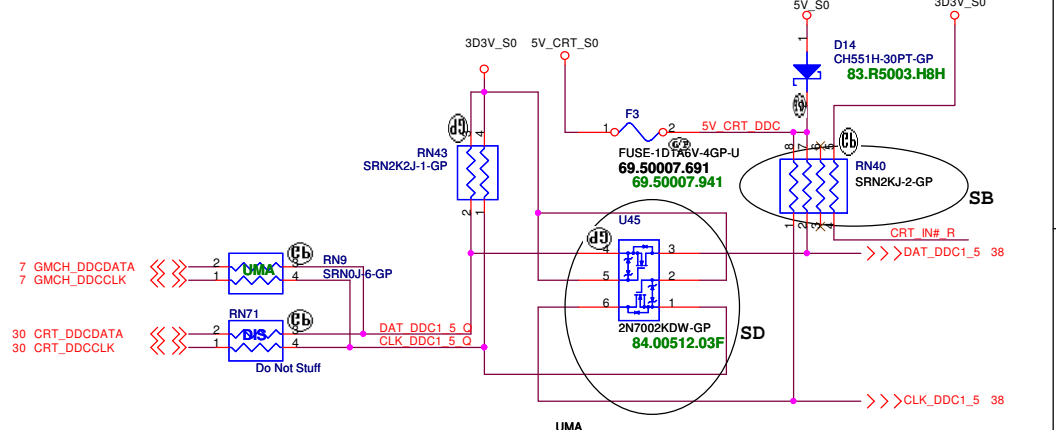
Hsync & Vsync level shift



CRT I/F & CONNECTOR



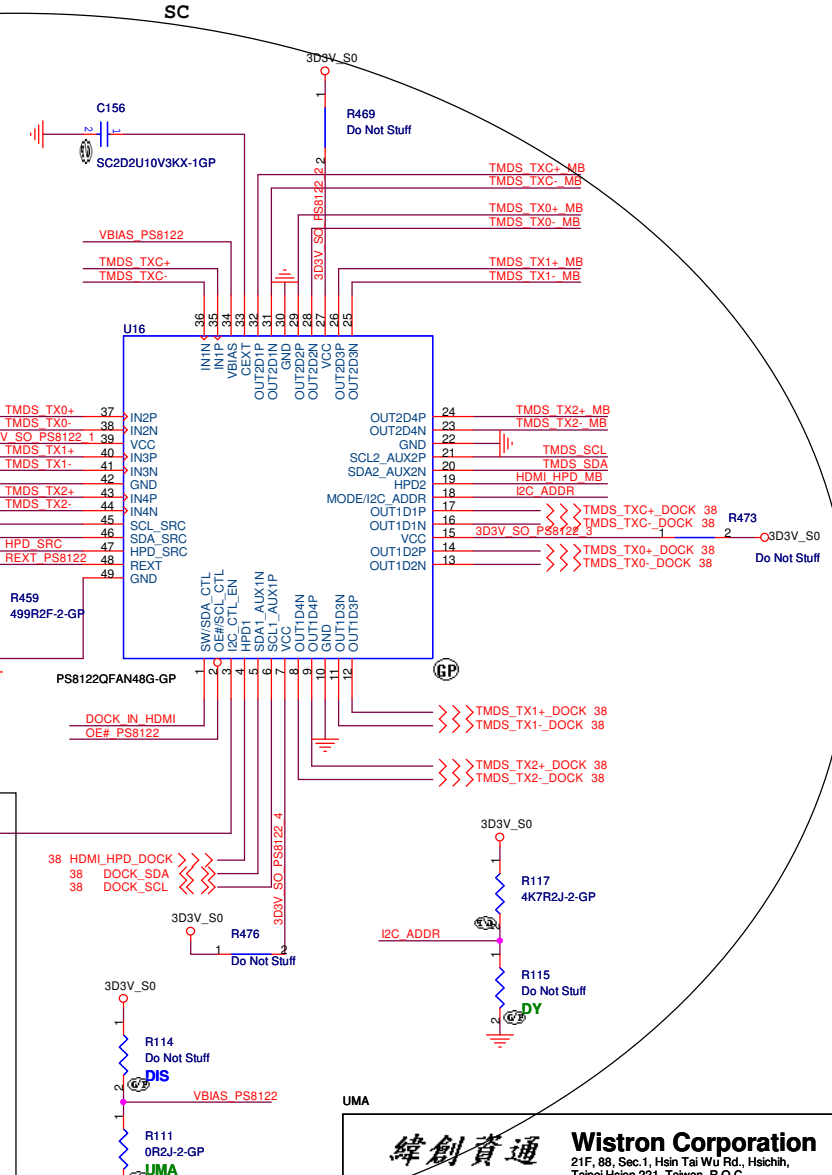
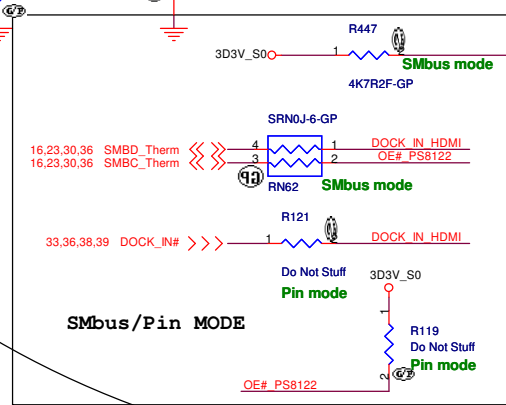
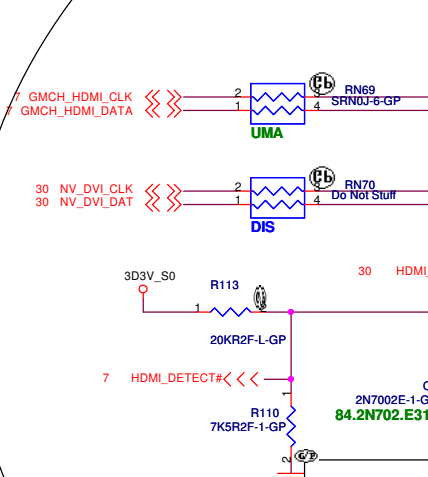
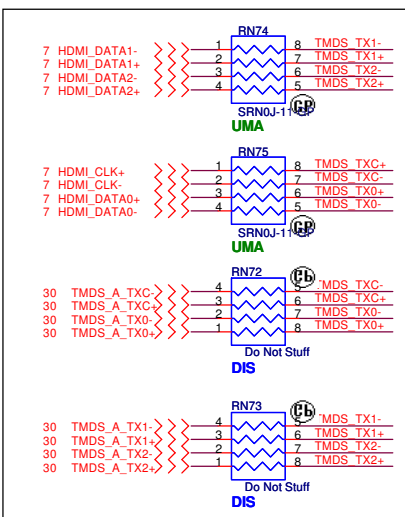
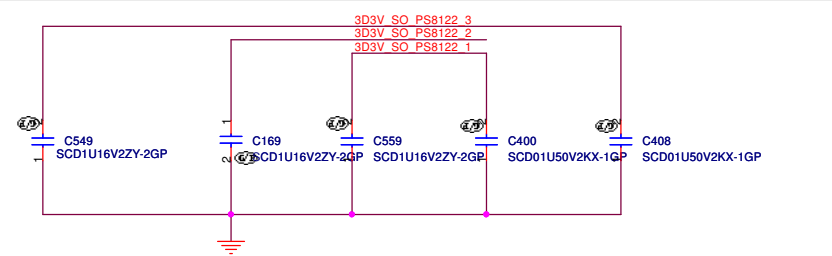
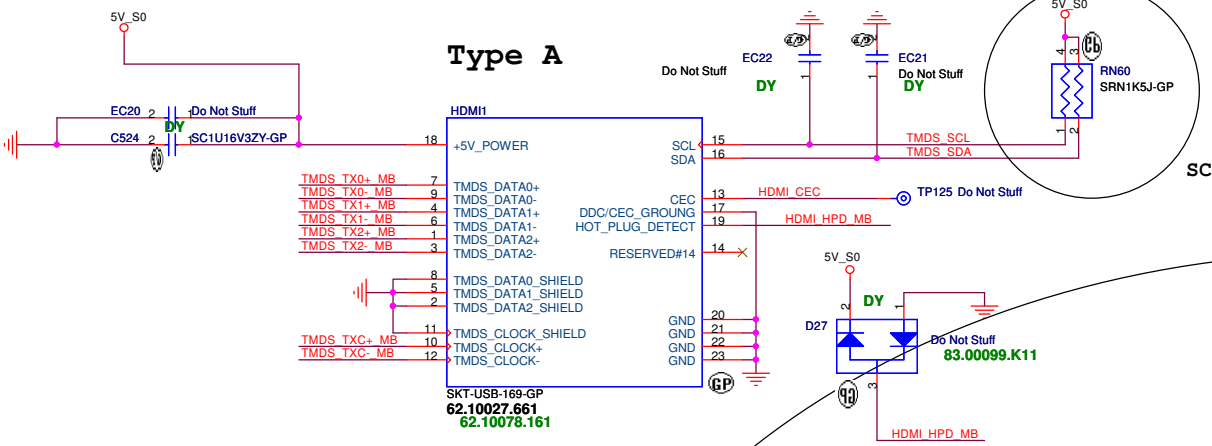
DDC_CLK & DATA level shift



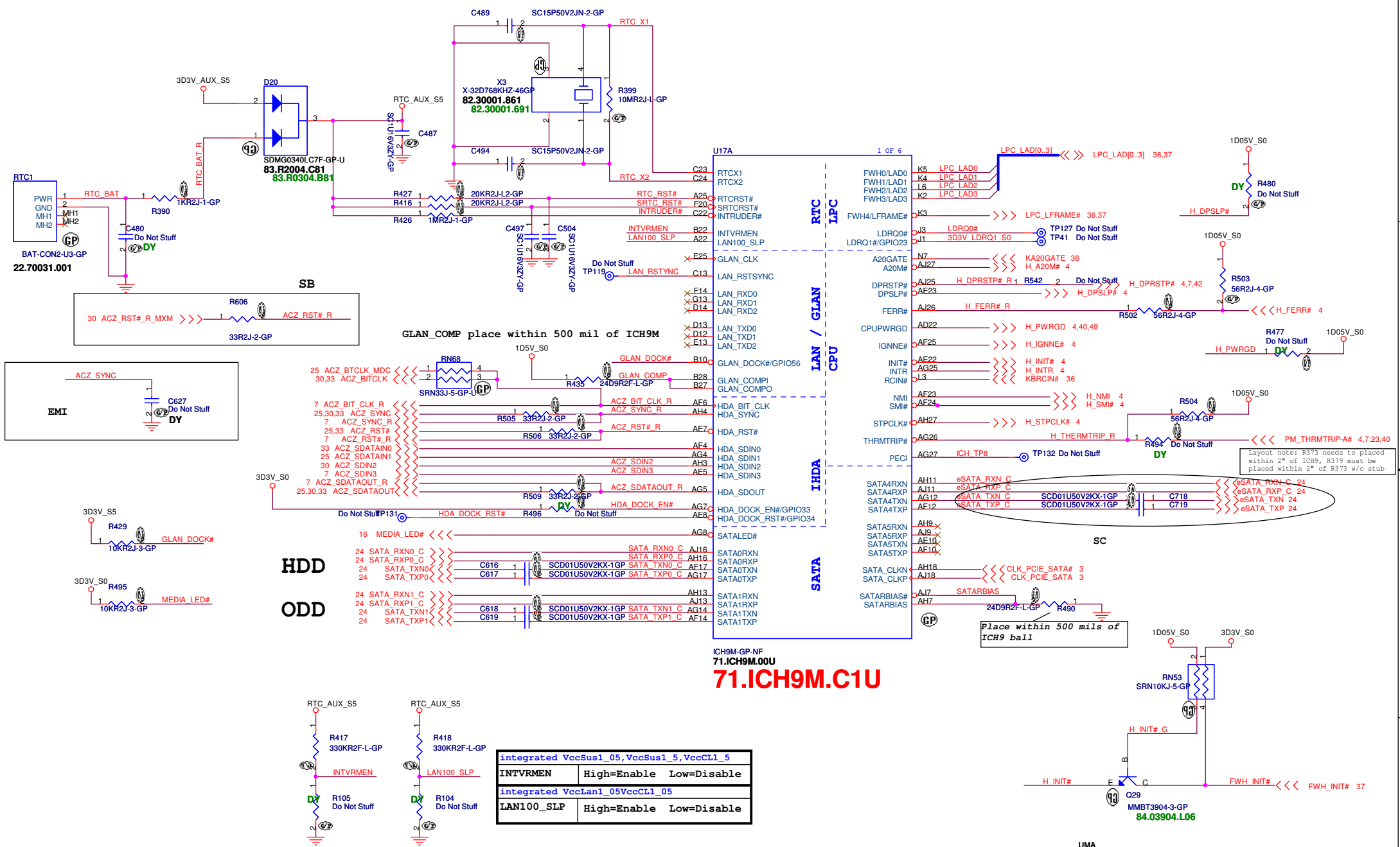
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Title		CRT Connector
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Type A

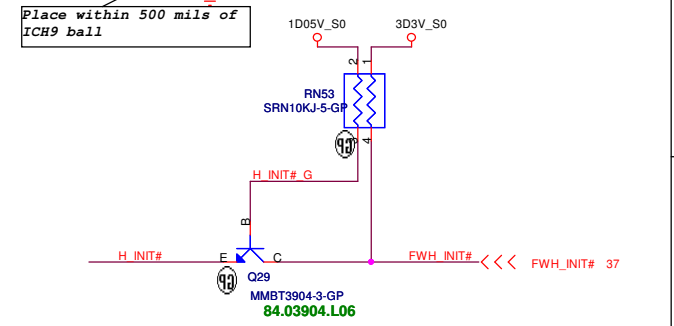
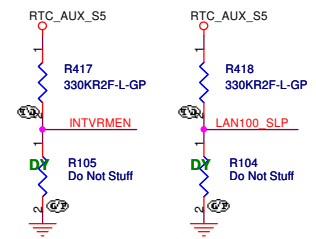


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71.ICH9M.C1U

integrated VccSus1_05, VccSus1_5, VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



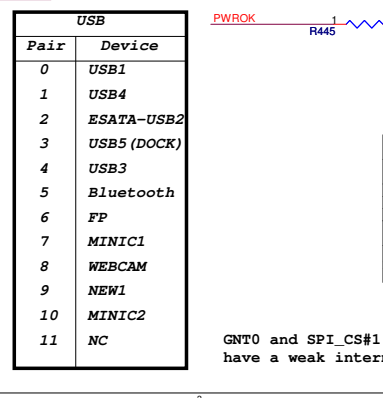
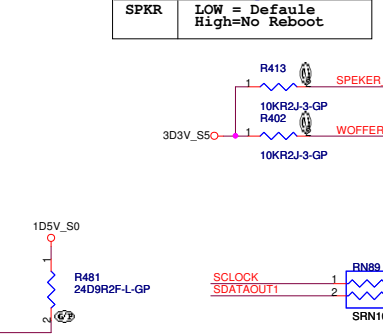
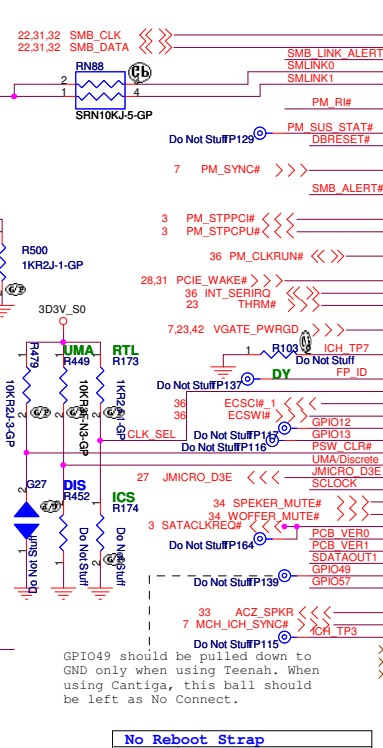
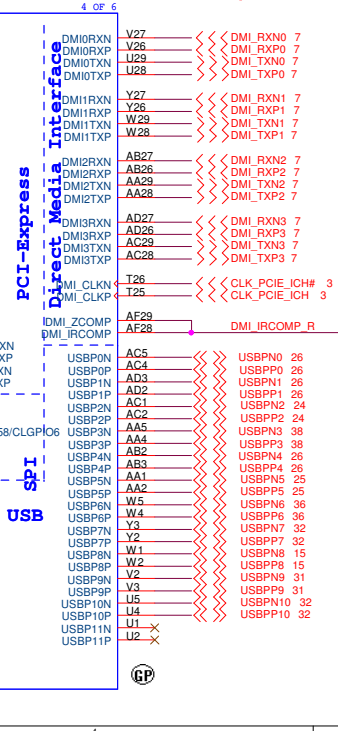
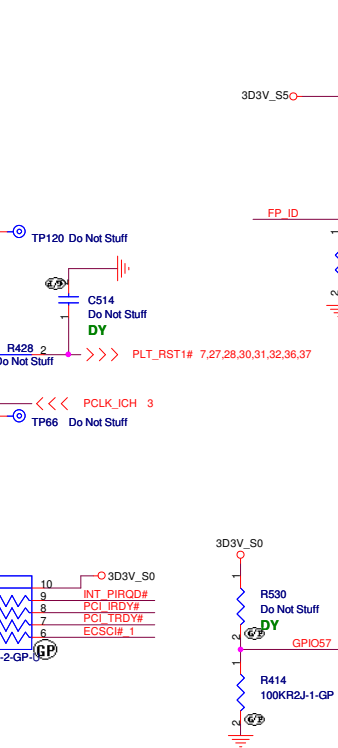
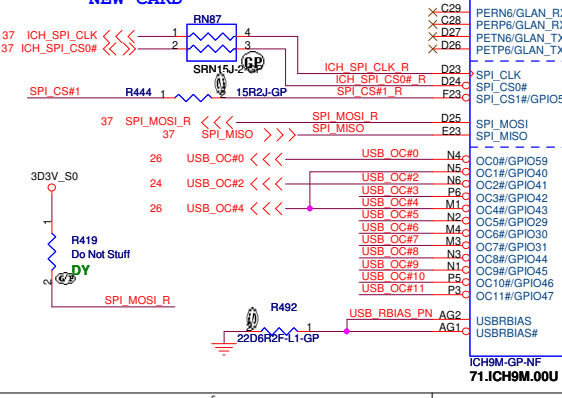
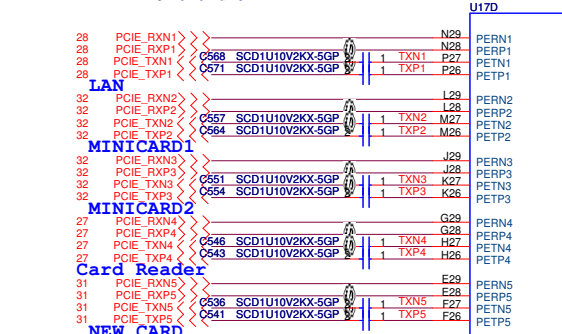
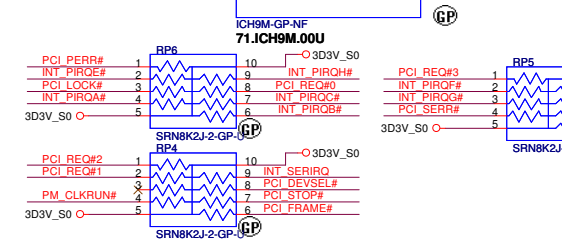
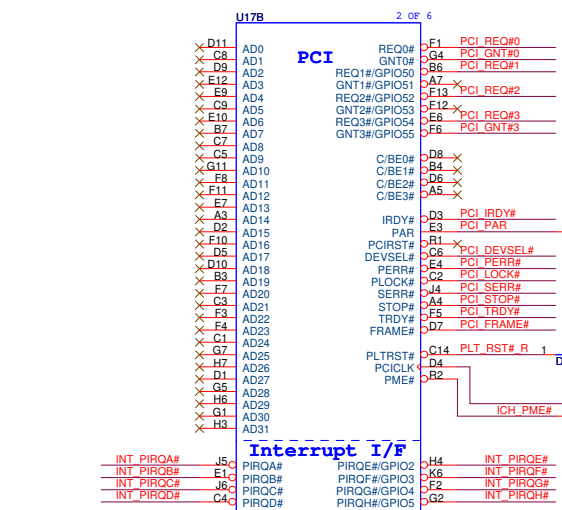
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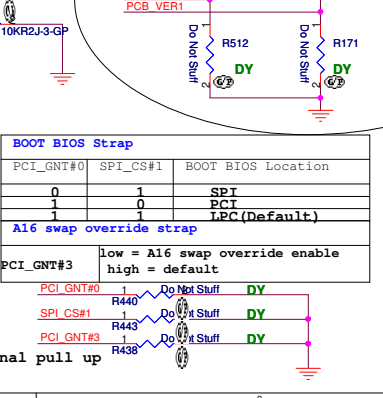
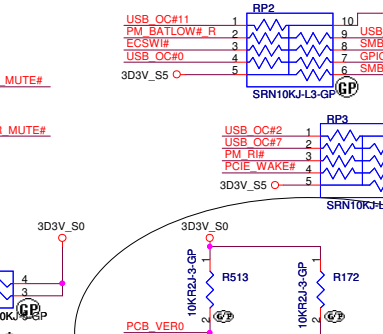
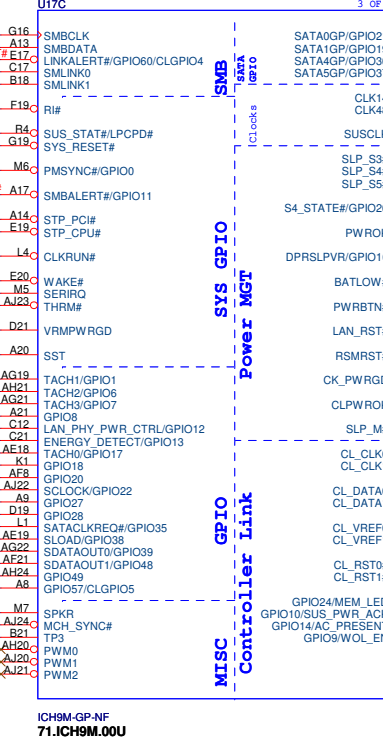
Title: **ICH9-M (1 of 4)**

Size: Document Number Rev: -1

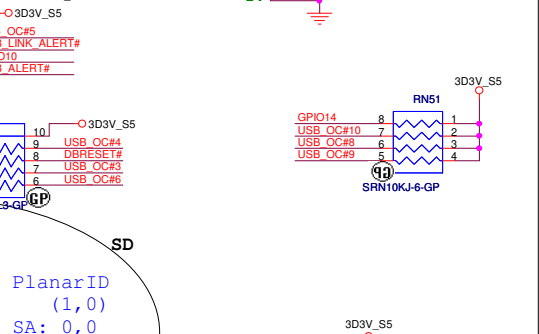
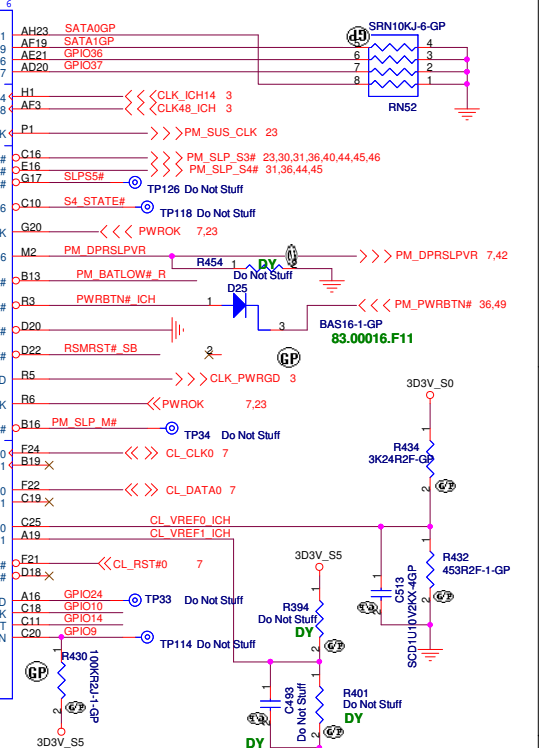
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Pair	Device
0	USB1
1	USB4
2	ESATA-(DOCK)
3	USB3
4	Bluetooth
5	MINIC1
6	FP
7	MINIC2
8	WEBCAM
9	NEW1
10	MINIC2
11	NC



PCI_GNT#	SPI_CS#	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)



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緯創資通

Title: **ICH9-M (2 of 4)**

Size: Document Number: Eiger

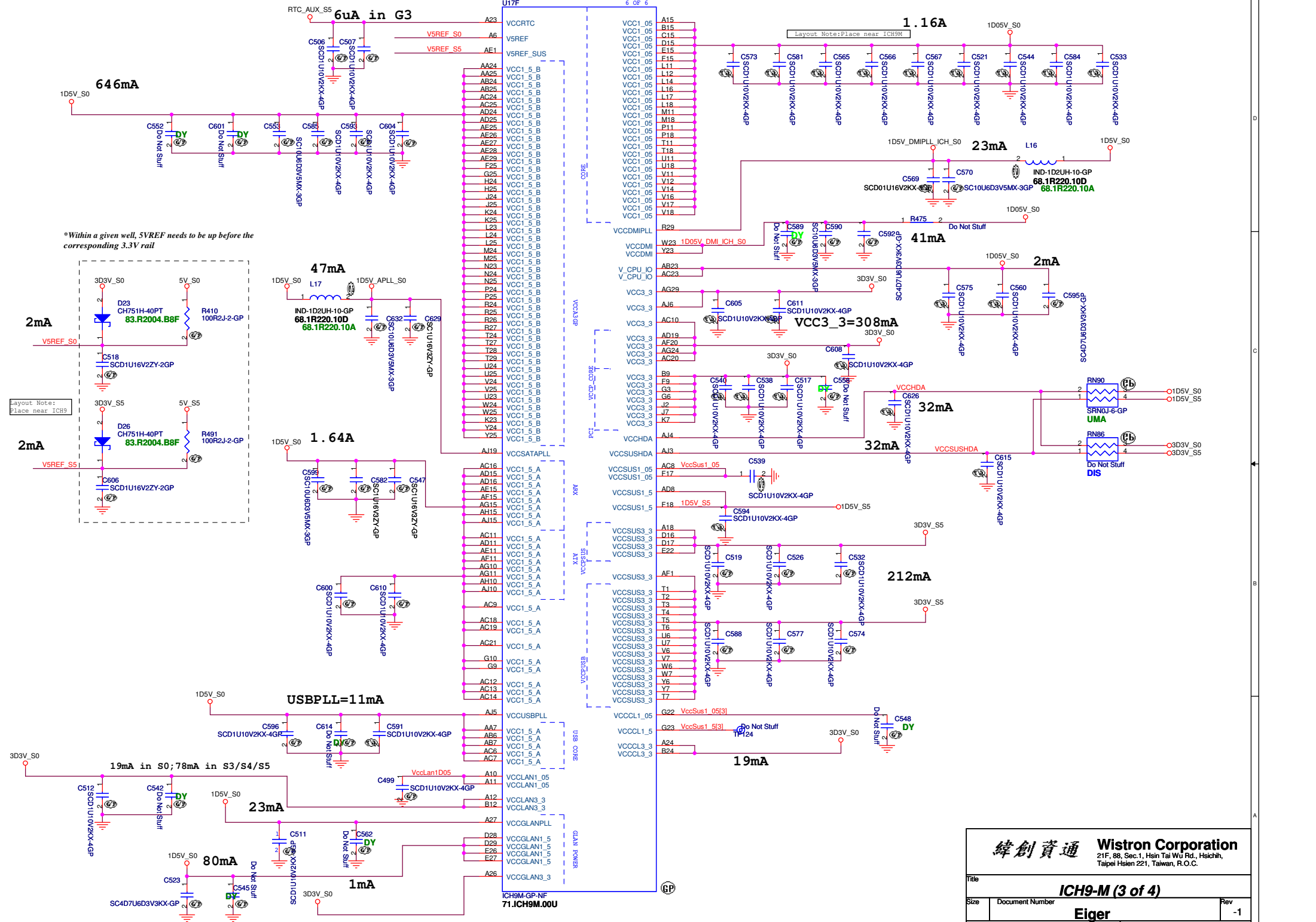
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GNT0 and SPI_CS#1 have a weak internal pull up

GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

No Reboot Strap
SPKR LOW = Default
High=No Reboot

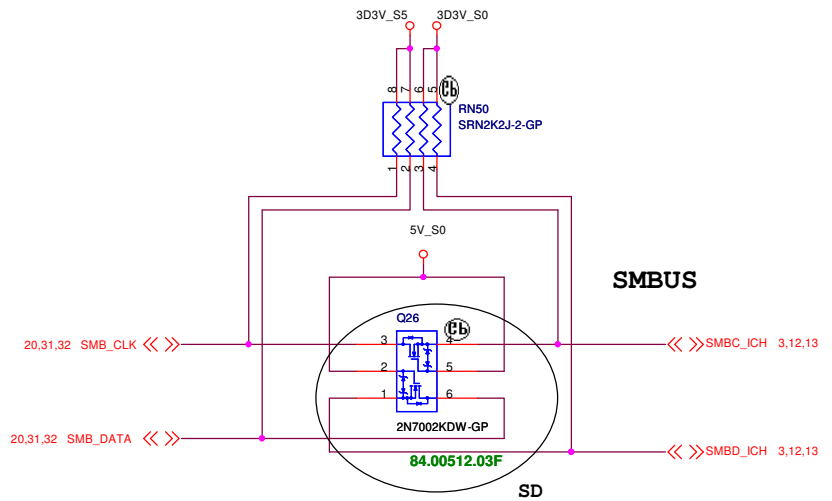
PlanarID (1,0)
SA: 0,0
SB: 1,0
SC: 0,1
SD: 1,1



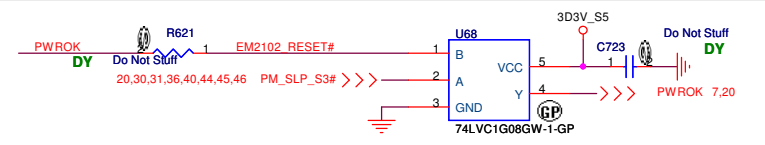
U17E 5 OF 6	
AA26	VSS
AA27	VSS
AA3	VSS
AA6	VSS
AB1	VSS
AA23	VSS
AB28	VSS
AE23	VSS
AB4	VSS
AB5	VSS
AC17	VSS
AC26	VSS
AC27	VSS
AC3	VSS
AD1	VSS
AD10	VSS
AD12	VSS
AD13	VSS
AD14	VSS
AD17	VSS
AD18	VSS
AD21	VSS
AD28	VSS
AD29	VSS
AD4	VSS
AD5	VSS
AD6	VSS
AD7	VSS
AD9	VSS
AE12	VSS
AE13	VSS
AE14	VSS
AE16	VSS
AE17	VSS
AE2	VSS
AE20	VSS
AE24	VSS
AE3	VSS
AE4	VSS
AE6	VSS
AE9	VSS
AE13	VSS
AF16	VSS
AF18	VSS
AF22	VSS
AH26	VSS
AF26	VSS
AF27	VSS
AF5	VSS
AF7	VSS
AF9	VSS
AG13	VSS
AG16	VSS
AG18	VSS
AG20	VSS
AG23	VSS
AG3	VSS
AG6	VSS
AG9	VSS
AH12	VSS
AH14	VSS
AH17	VSS
AH19	VSS
AH2	VSS
AH22	VSS
AH25	VSS
AH28	VSS
AH5	VSS
AH8	VSS
AJ12	VSS
AJ14	VSS
AJ17	VSS
AJ8	VSS
B11	VSS
B14	VSS
B17	VSS
B2	VSS
B20	VSS
B23	VSS
B5	VSS
B8	VSS
C26	VSS
C27	VSS
E11	VSS
E14	VSS
E18	VSS
E2	VSS
E21	VSS
E24	VSS
E5	VSS
E8	VSS
F16	VSS
F28	VSS
F29	VSS
G12	VSS
G14	VSS
G18	VSS
G21	VSS
G24	VSS
G26	VSS
G27	VSS
G28	VSS
G8	VSS
H2	VSS
H23	VSS
H28	VSS
H29	VSS
H5	VSS
J23	VSS
J26	VSS
J27	VSS
AC22	VSS
K28	VSS
K29	VSS
L13	VSS
L15	VSS
L2	VSS
L26	VSS
L27	VSS
L5	VSS
L7	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS
M16	VSS
M17	VSS
M23	VSS
M28	VSS
M29	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
N17	VSS
N18	VSS
N26	VSS
N27	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
P17	VSS
P2	VSS
P23	VSS
P28	VSS
P29	VSS
P4	VSS
P7	VSS
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R16	VSS
R17	VSS
R18	VSS
R28	VSS
T12	VSS
T13	VSS
T14	VSS
T15	VSS
T16	VSS
T17	VSS
T23	VSS
B26	VSS
U12	VSS
U13	VSS
U14	VSS
U15	VSS
U16	VSS
U17	VSS
AD23	VSS
U26	VSS
U27	VSS
U3	VSS
V1	VSS
V13	VSS
V15	VSS
V23	VSS
V28	VSS
V29	VSS
V4	VSS
V5	VSS
W26	VSS
W27	VSS
W3	VSS
Y1	VSS
Y28	VSS
Y29	VSS
Y4	VSS
Y5	VSS
AG28	VSS
AH6	VSS
AF2	VSS
B25	VSS

NCTF TEST PIN:			
A1, A2, B1, A29, B29	NCTF_VSS#A1	A1	TP37 Do Not Stuff
AH1, B1, A21, A25, A28, A28	NCTF_VSS#A2	A2	TP35 Do Not Stuff
	NCTF_VSS#B1	B1	TP39 Do Not Stuff
	NCTF_VSS#A29	A29	TP36 Do Not Stuff
	NCTF_VSS#A28	A28	TP38 Do Not Stuff
	NCTF_VSS#B29	B29	TP40 Do Not Stuff
	NCTF_VSS#B29	B29	TP77 Do Not Stuff
	NCTF_VSS#AJ1	AJ1	TP80 Do Not Stuff
	NCTF_VSS#AJ2	AJ2	TP80 Do Not Stuff
	NCTF_VSS#AH1	AH1	TP78 Do Not Stuff
	NCTF_VSS#AJ28	AJ28	TP71 Do Not Stuff
	NCTF_VSS#AJ29	AJ29	TP68 Do Not Stuff
	NCTF_VSS#AH29	AH29	TP69 Do Not Stuff

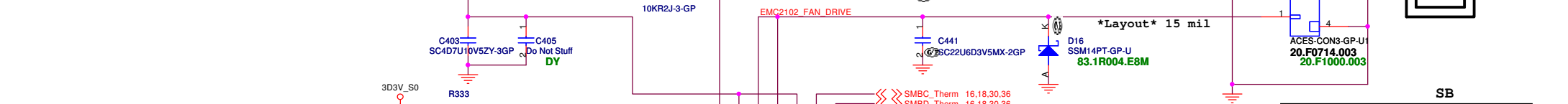
ICH9M-GP-NF
71.ICH9M.00U



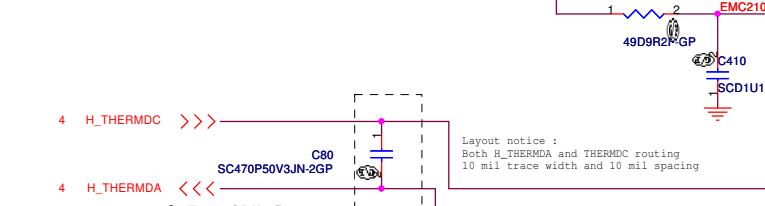
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH9-M (4 of 4)
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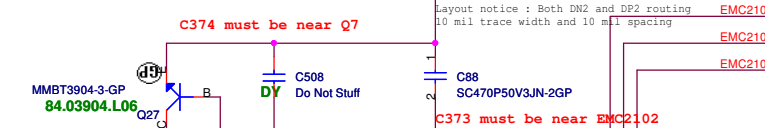
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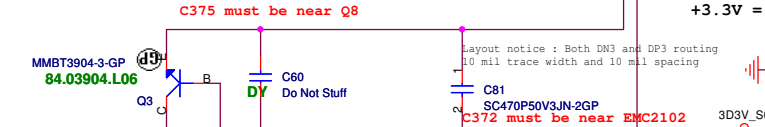
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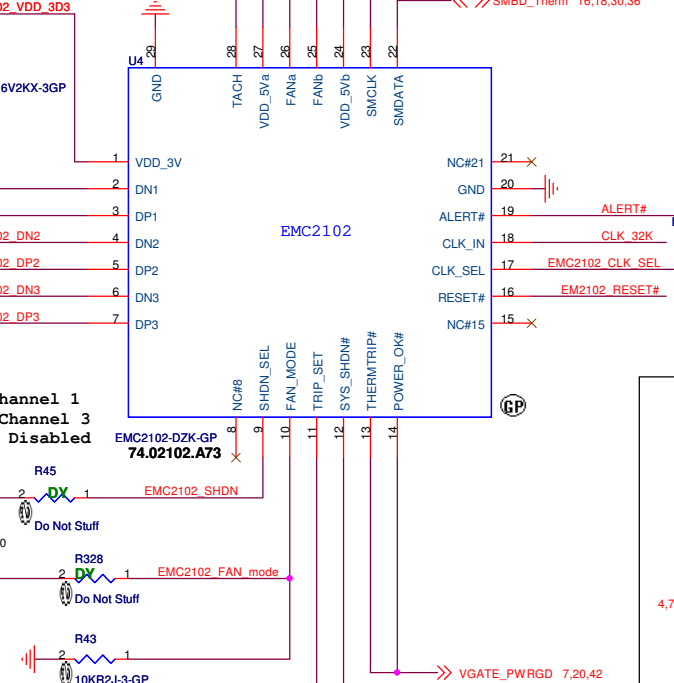
1. For CPU Sensor



2. System Sensor, Put between CPU and NB.

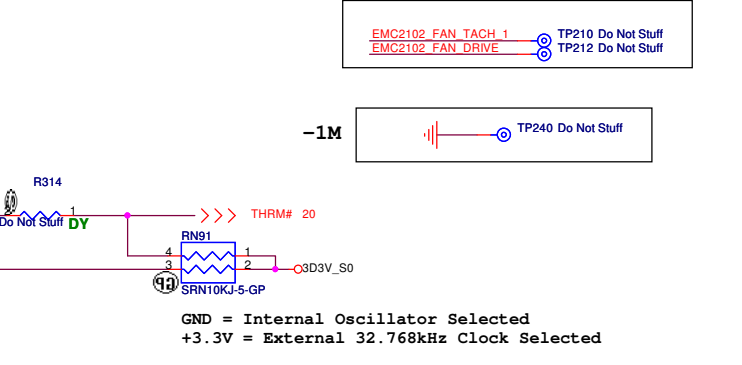


3. HW T8 sensor

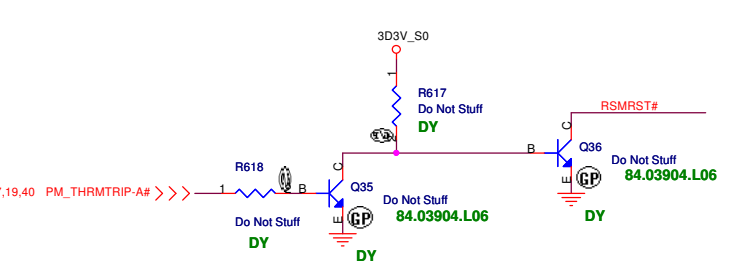


GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

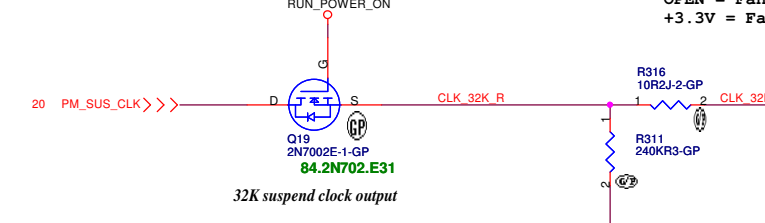
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale



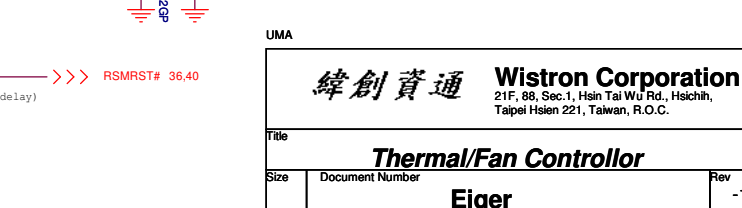
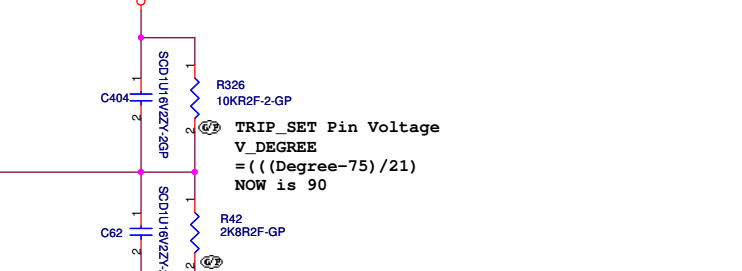
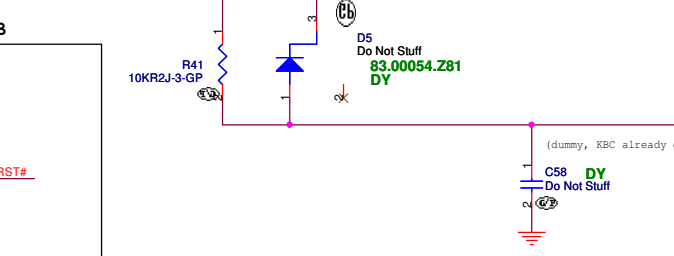
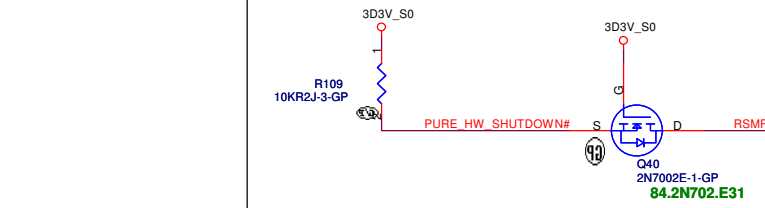
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected



TRIP_SET Pin Voltage
V_DEGREE
= ((Degree-75)/21)
NOW is 90



32K suspend clock output



UMA

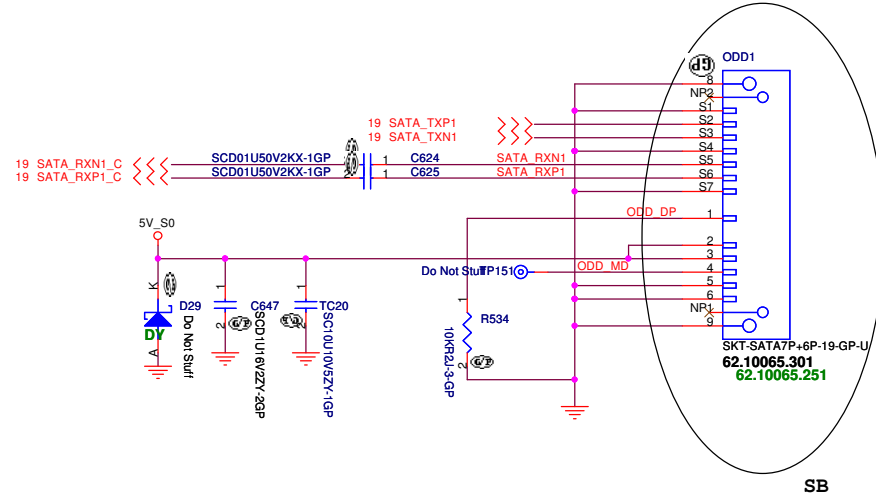
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controller**

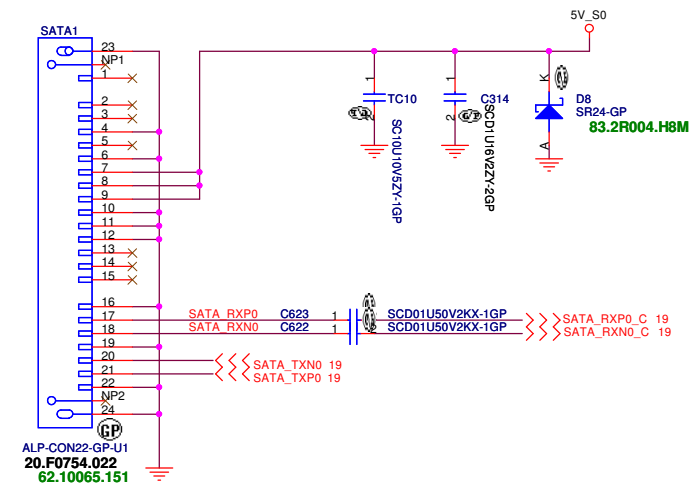
Size: Document Number **Eiger** Rev: -1

Date: Tuesday, April 01, 2008 Sheet 23 of 50

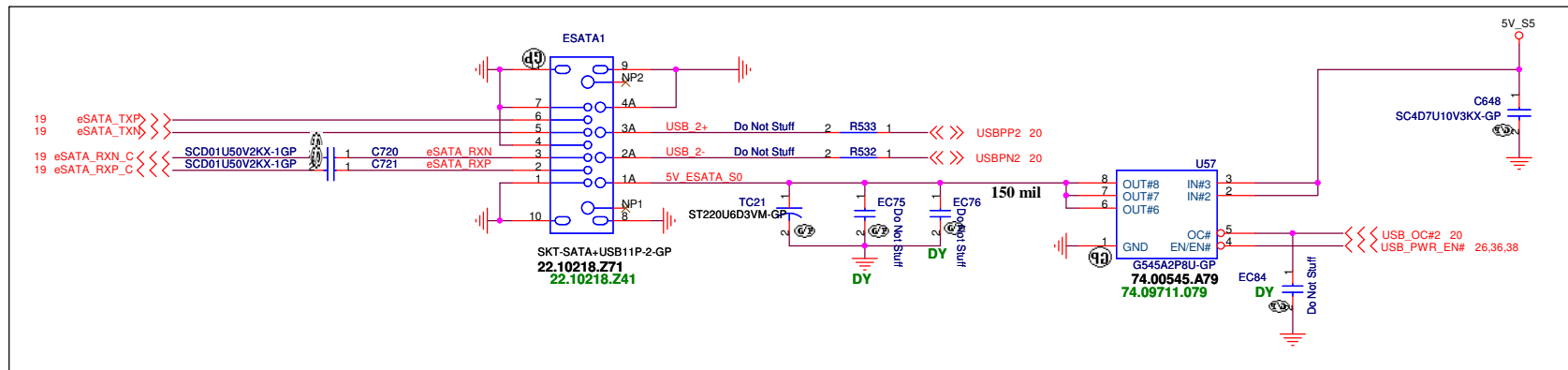
SATA ODD Connector



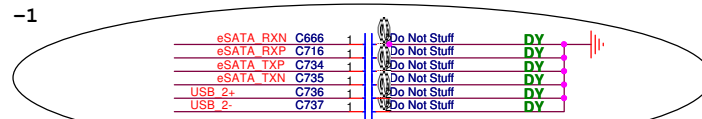
SATA Connector



SC



-1



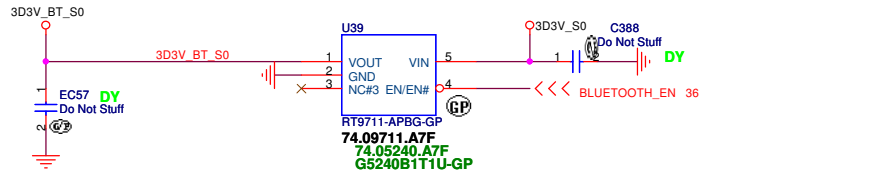
EMI

UMA

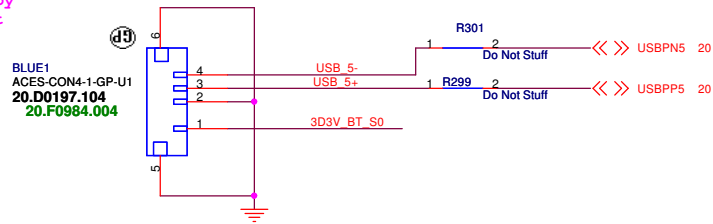
Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
HDD & CDROM & ESATA	
Size	Document Number
Eiger	
Date: Tuesday, April 01, 2008	Sheet 24 of 50

BLUETOOTH MODULE

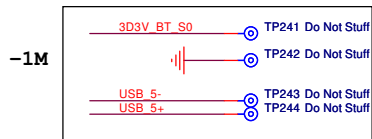
1.5A / High Active Voltage 2V



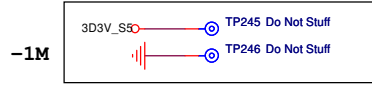
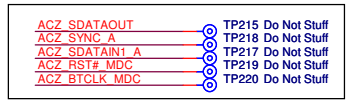
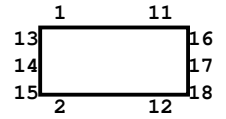
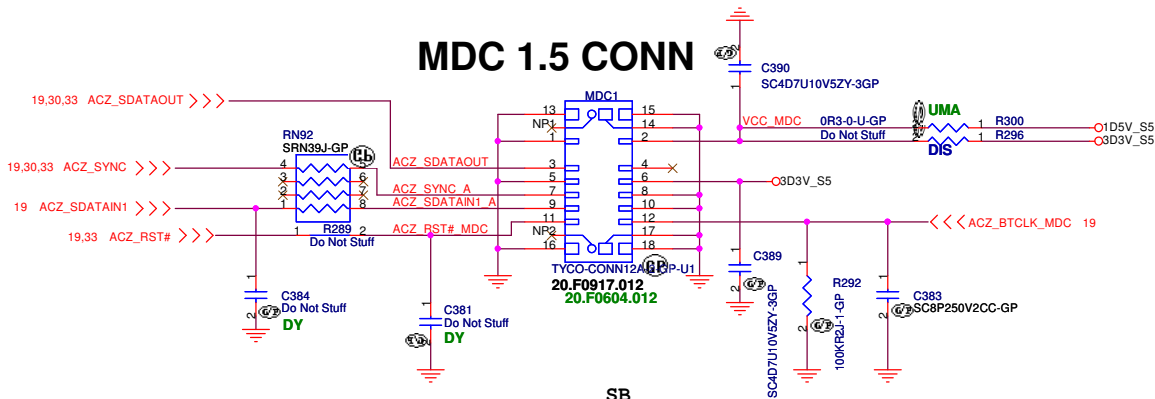
EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



BLUE1
ACES-CON4-1-GP-U1
20.D0197.104
20.F0984.004



MDC 1.5 CONN



Finger printer

MOVE TO Page 36

UMA

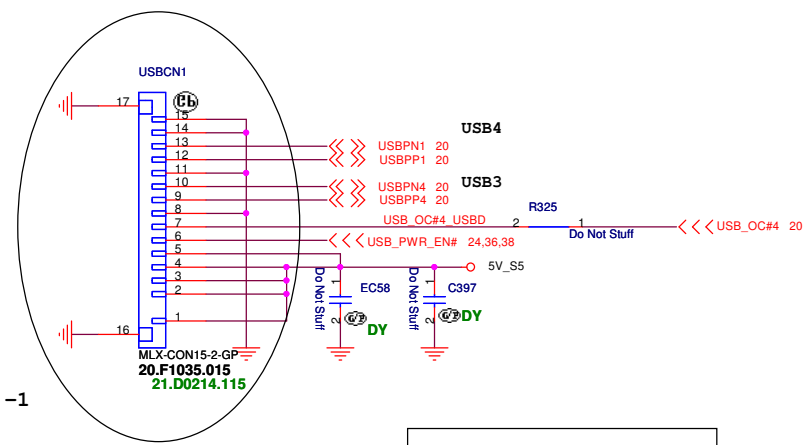
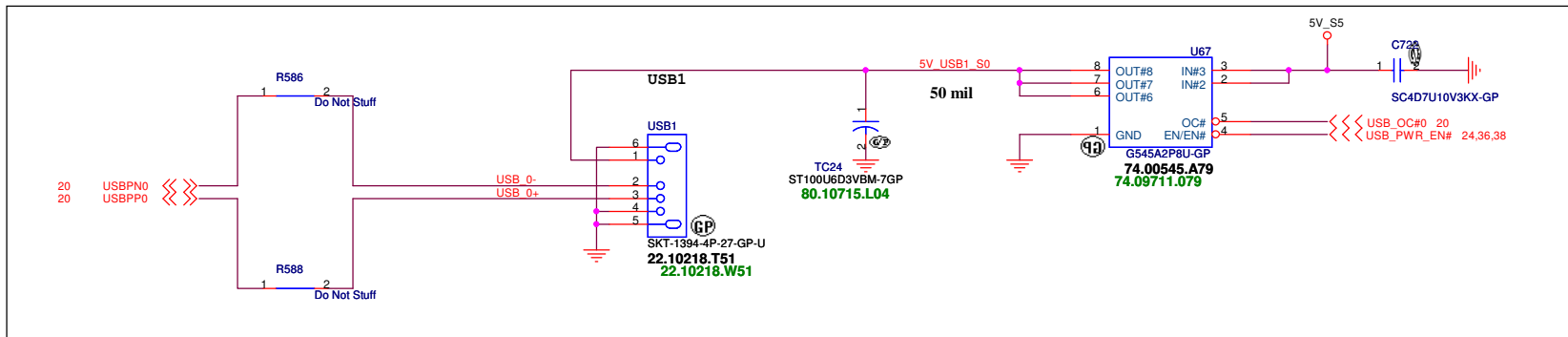
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLUETOOTH MDC Finger printer**

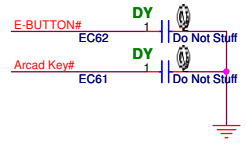
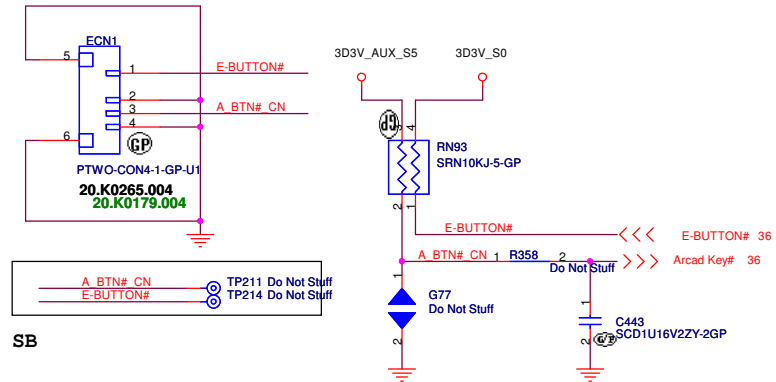
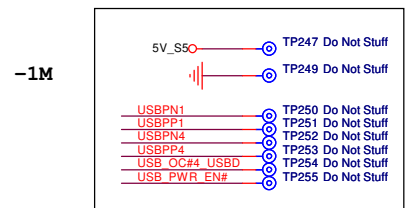
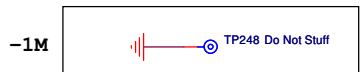
Size: Document Number Rev: -1

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SC



ECN BOARD



UMA

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

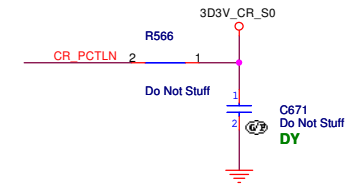
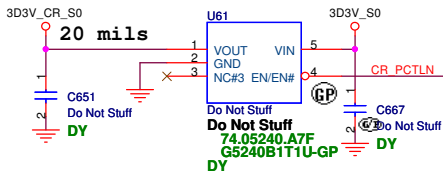
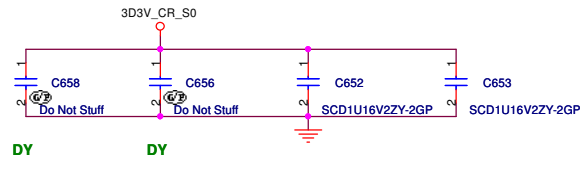
Title: **USB & ECN**

Size	Document Number	Rev
		-1

Date: Tuesday, April 01, 2008 Sheet 26 of 50

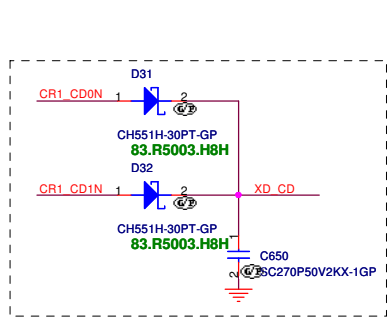
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

1.5A / High Active Voltage 2V

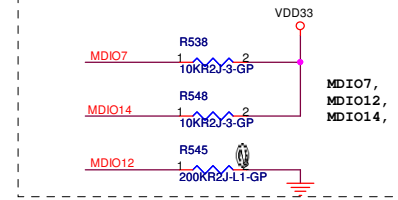
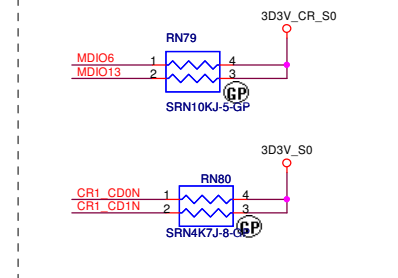
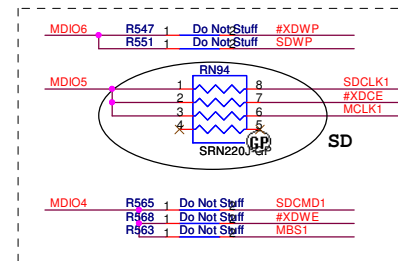
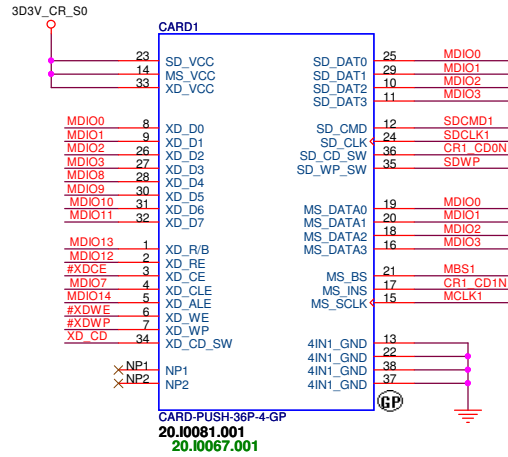


SC
EMI

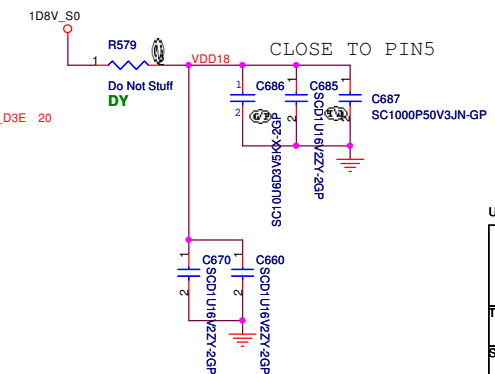
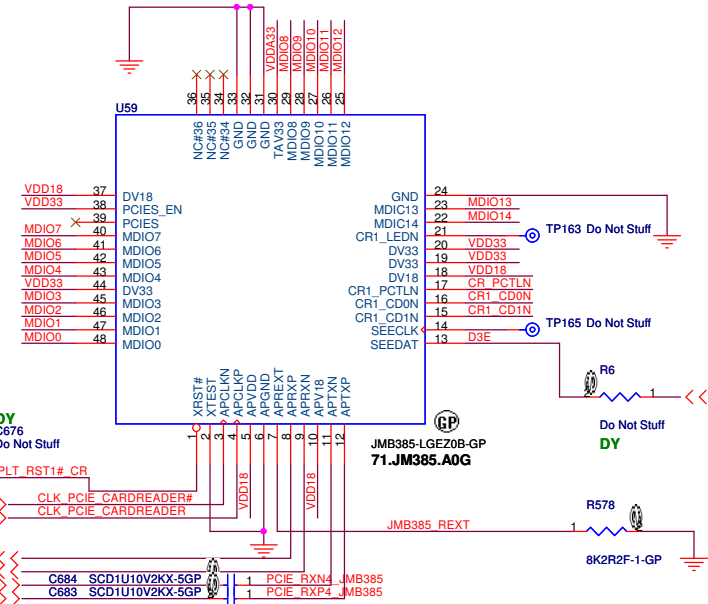
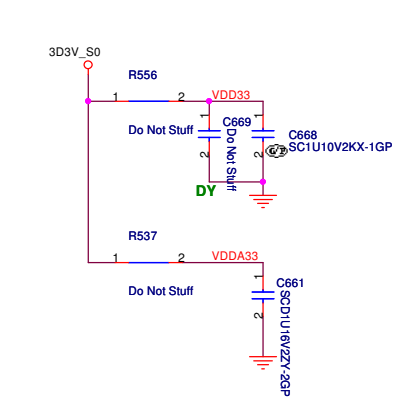
Signal	Part	Value	Notes	Label
MDIO0	C555	1	2 Do Not Stuff	DY
MDIO1	C556	1	2 Do Not Stuff	DY
MDIO2	C597	1	2 Do Not Stuff	DY
MDIO3	C598	1	2 Do Not Stuff	DY
SDCMD1	C602	1	2 Do Not Stuff	DY
SDCLK1	C603	1	2 Do Not Stuff	DY
CR1_CD0N	C714	1	2 Do Not Stuff	DY
SDWP	C715	1	2 Do Not Stuff	DY



SD/XD/MS/MS PRO/MMC



MDIO7, H on-board, L : on Add-in card or Express card
 MDIO12, H CR1_LEDN high active, L : CR1_LEDN low active
 MDIO14, H CR1_PCTLN high active, L : CR1_PCTLN low active



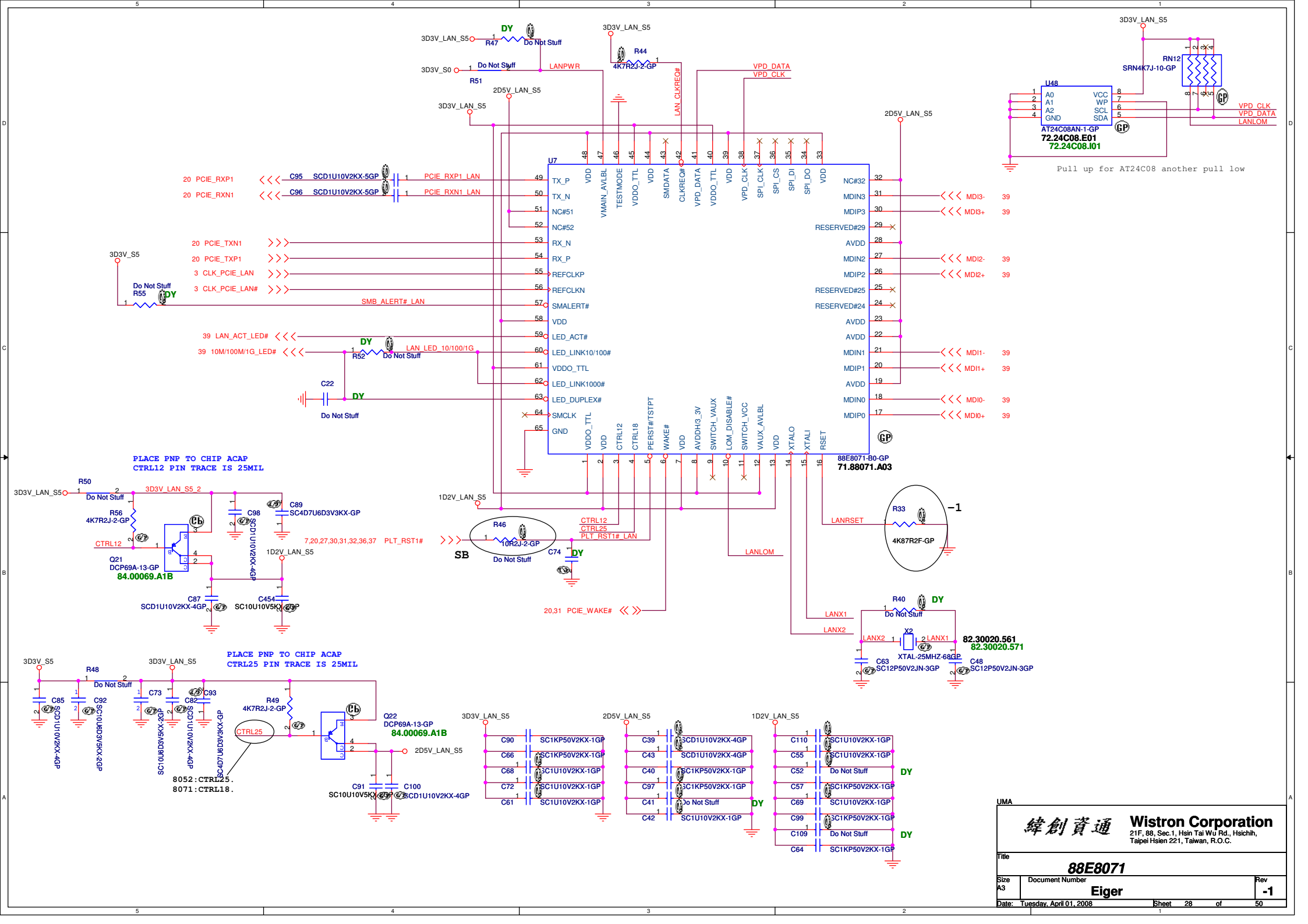
UMA

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **JMB385 Card Reader**

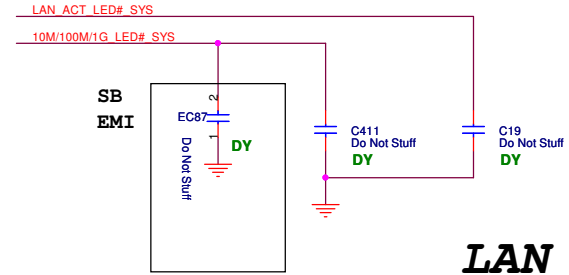
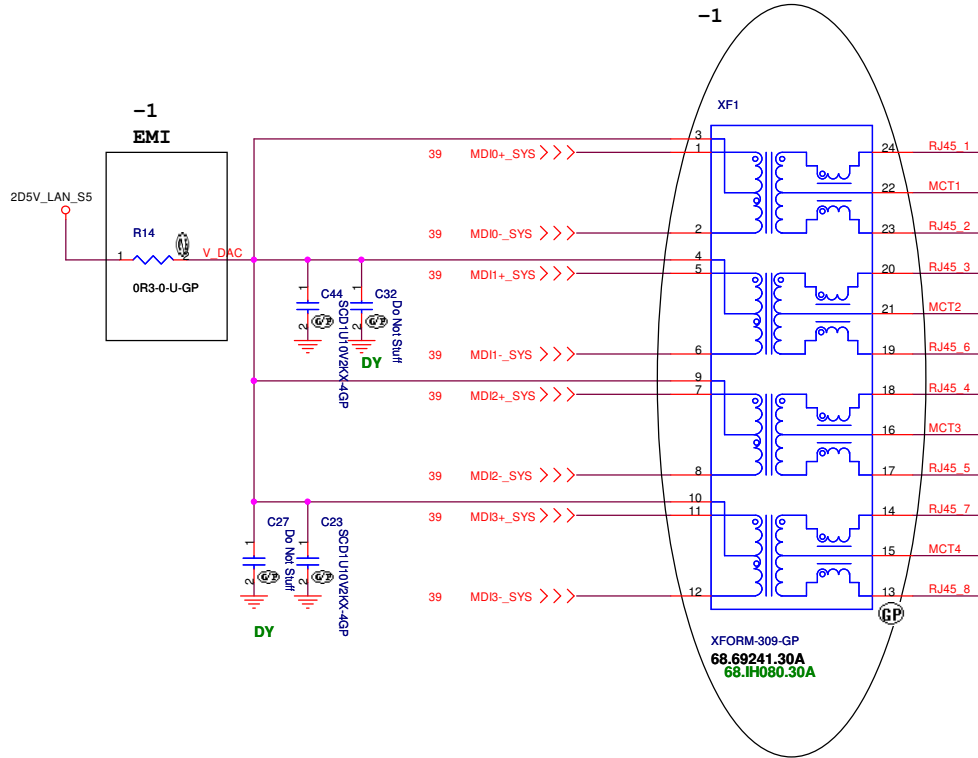
Size: Document Number Rev: -1

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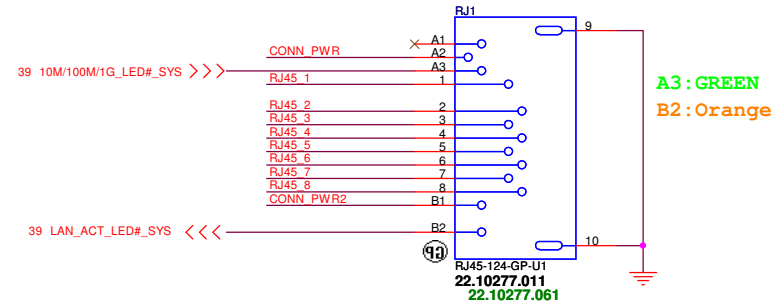


LAN Connector

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

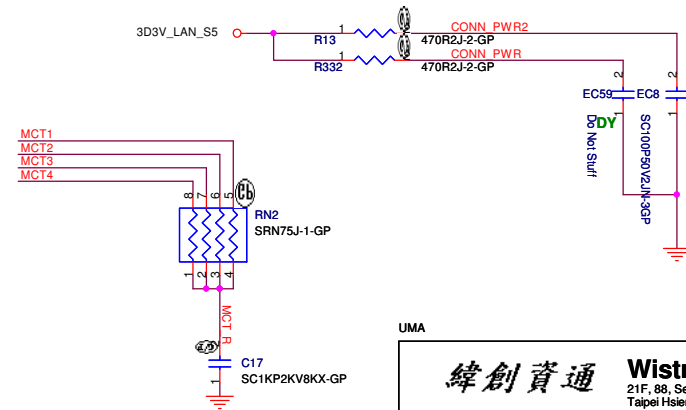


LAN Connector

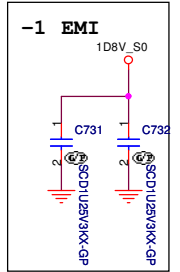


LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
 LAN Data: Yellow(B2), when LAN is transferring data.

DOC_TIP,DOC_RING,TIP,RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers

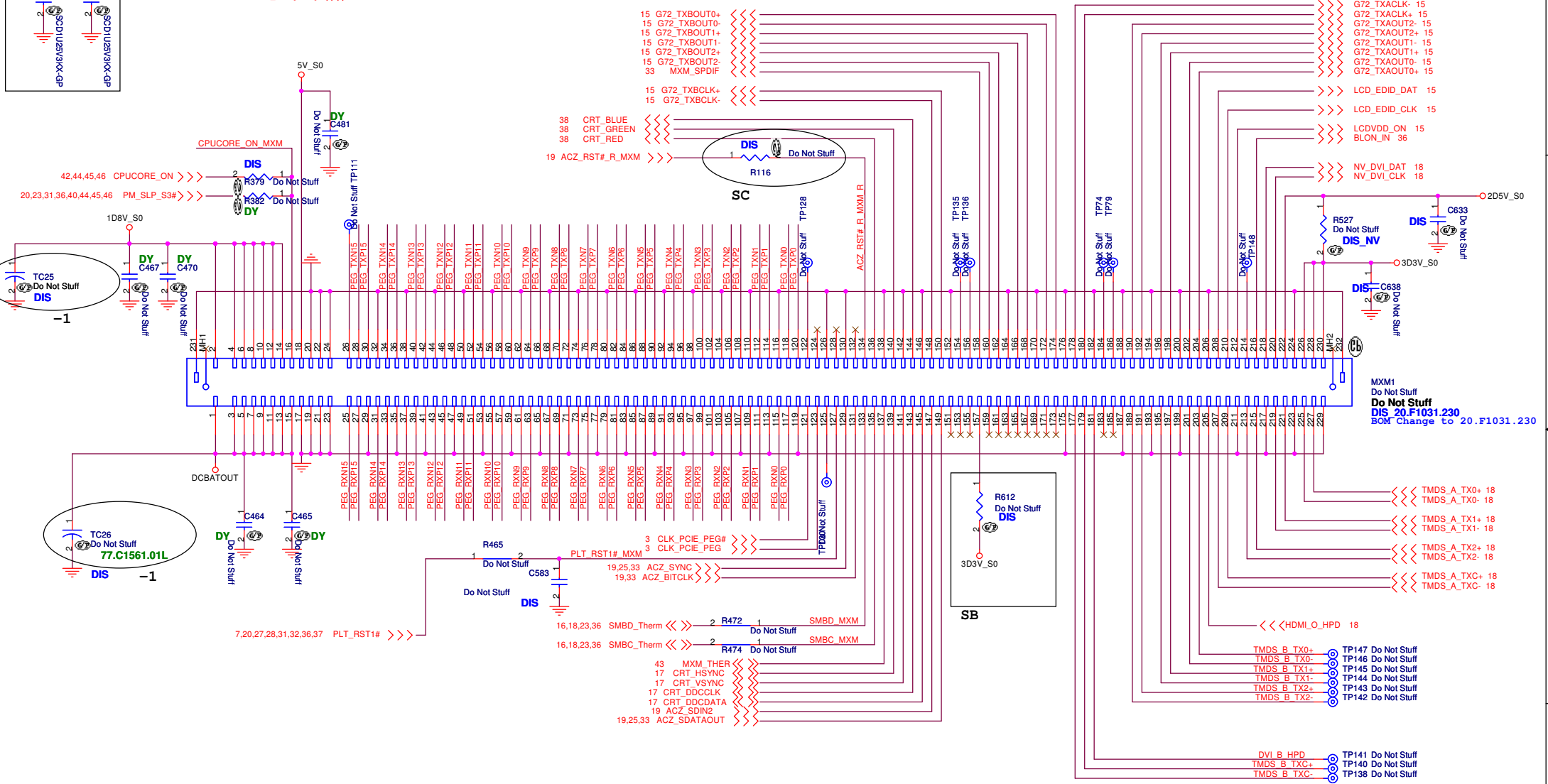


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LAN CONN	
Title	
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- 7 PEG_TXP[15.0] <<>>
- 7 PEG_TXN[15.0] <<>>
- 7 PEG_RXP[15.0] <<>>
- 7 PEG_RXN[15.0] <<>>

NV SMBus
 A(pin143&145) : VGA(CRT) / DOCK
 B(pin218&220) : DVI
 C(pin208&210) : HDMI / TPI / LVDS



- 15 G72_TXBOUT+ <<>>
- 15 G72_TXBOUT0- <<>>
- 15 G72_TXBOUT1+ <<>>
- 15 G72_TXBOUT1- <<>>
- 15 G72_TXBOUT2+ <<>>
- 15 G72_TXBOUT2- <<>>
- 33 MXM_SPDIF <<>>
- 15 G72_TXBCLK+ <<>>
- 15 G72_TXBCLK- <<>>

- 38 CRT_BLUE <<>>
- 38 CRT_GREEN <<>>
- 38 CRT_RED <<>>
- 19 ACZ_RST#_R_MXM <<>>

- G72_TXACLK- 15 <<>>
- G72_TXACLK+ 15 <<>>
- G72_TXAOUT2- 15 <<>>
- G72_TXAOUT2+ 15 <<>>
- G72_TXAOUT1- 15 <<>>
- G72_TXAOUT1+ 15 <<>>
- G72_TXAOUT0- 15 <<>>
- G72_TXAOUT0+ 15 <<>>
- LCD_EDID_DAT 15 <<>>
- LCD_EDID_CLK 15 <<>>
- LCDVDD_ON 15 <<>>
- BLON_IN_36 <<>>
- NV_DVI_DAT 18 <<>>
- NV_DVI_CLK 18 <<>>

2D5V_S0
 3D3V_S0
 MXM1 Do Not Stuff
DIS 20.F1031.230
 BOM Change to 20.F1031.230

- TMDS_A_TX0+ 18 <<>>
- TMDS_A_TX0- 18 <<>>
- TMDS_A_TX1+ 18 <<>>
- TMDS_A_TX1- 18 <<>>
- TMDS_A_TX2+ 18 <<>>
- TMDS_A_TX2- 18 <<>>
- TMDS_A_TXC+ 18 <<>>
- TMDS_A_TXC- 18 <<>>

- TP147 Do Not Stuff
- TP146 Do Not Stuff
- TP145 Do Not Stuff
- TP144 Do Not Stuff
- TMDS_B_TX2+ <<>>
- TMDS_B_TX2- <<>>
- TP142 Do Not Stuff

- DVI B HPD <<>>
- TP141 Do Not Stuff
- TMDS_B_TXC+ <<>>
- TP140 Do Not Stuff
- TMDS_B_TXC- <<>>
- TP138 Do Not Stuff

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

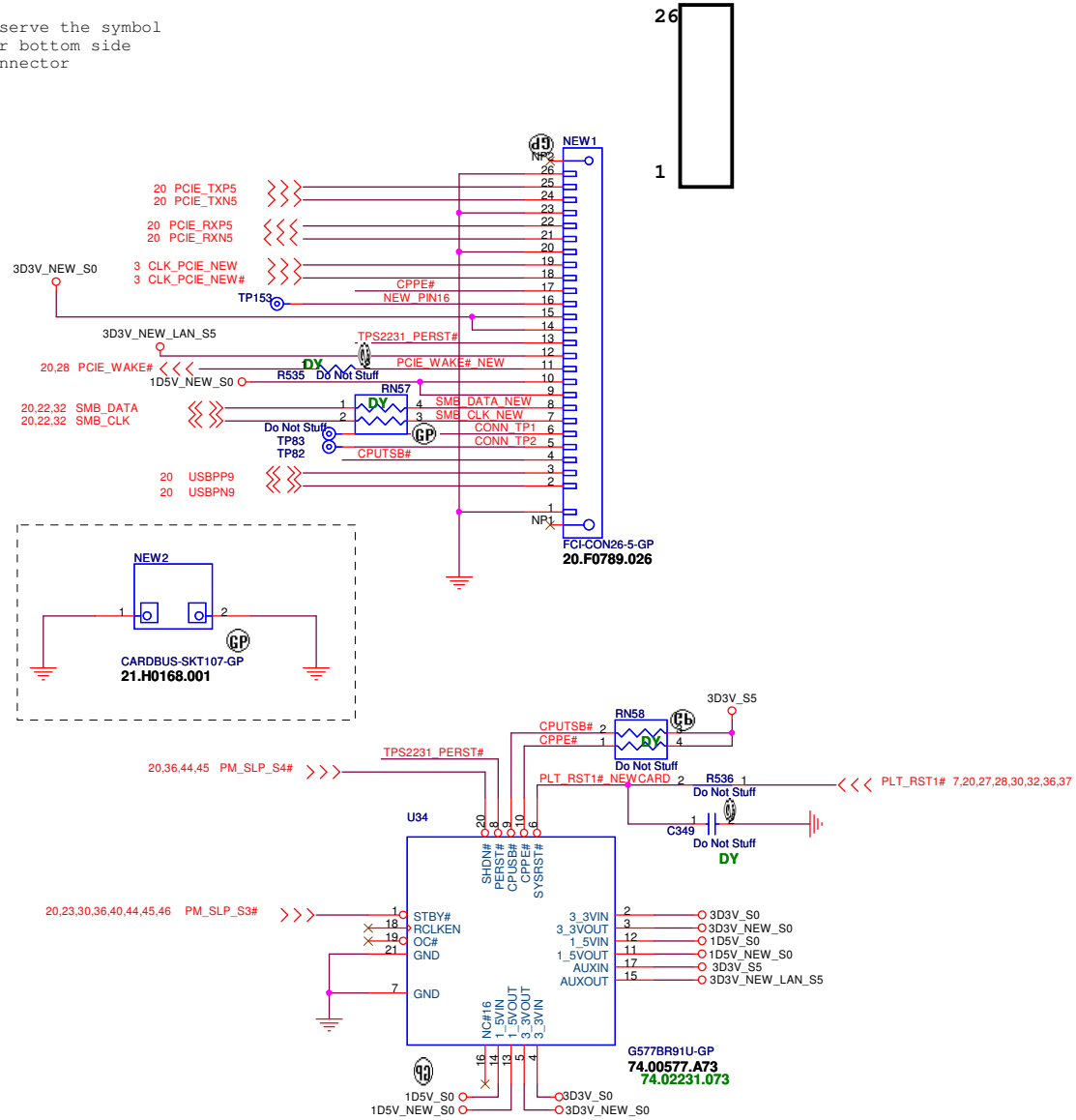
Size: A3 Document Number: **Eiger** Rev: -1

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NEWCARD Connector

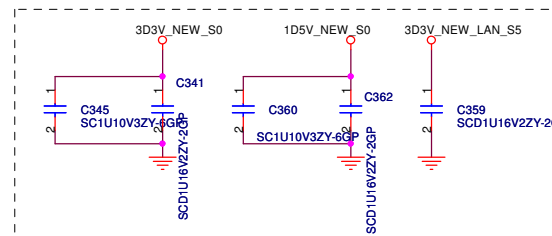
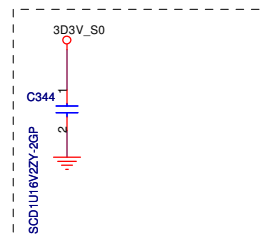
Reserve the symbol for bottom side connector

TOP VIEW



Place them Near to Chip

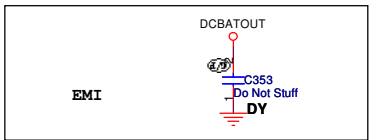
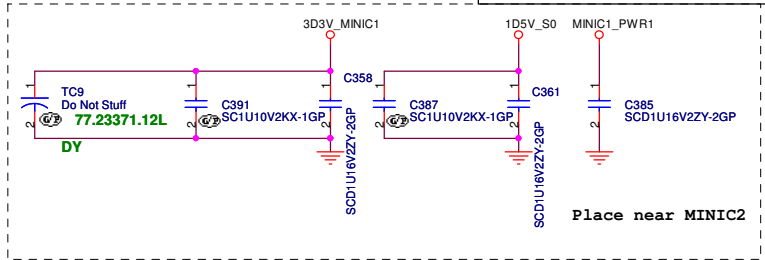
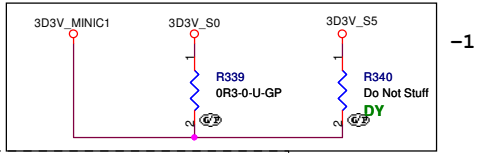
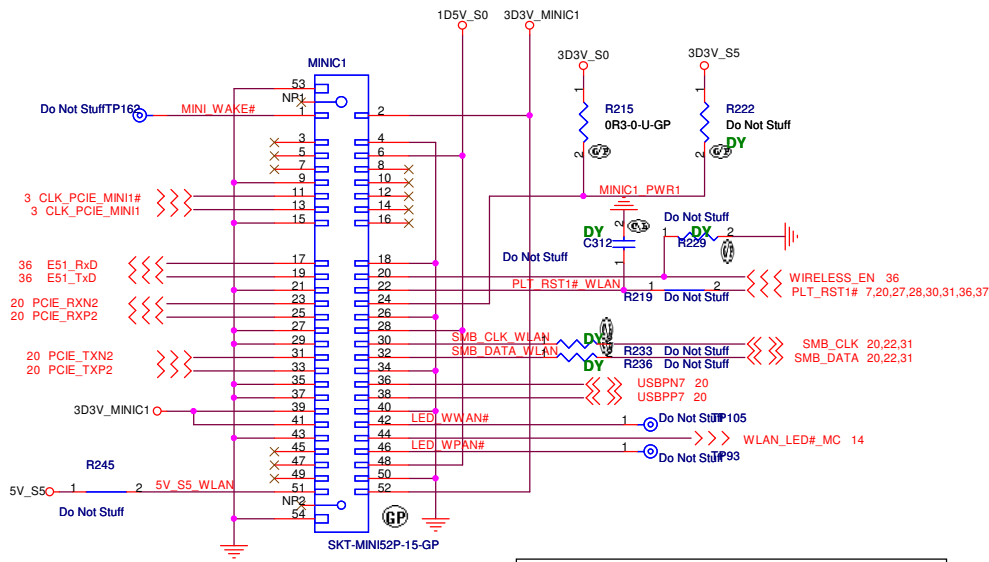
Place them Near to Connector



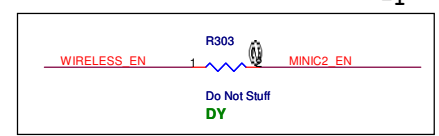
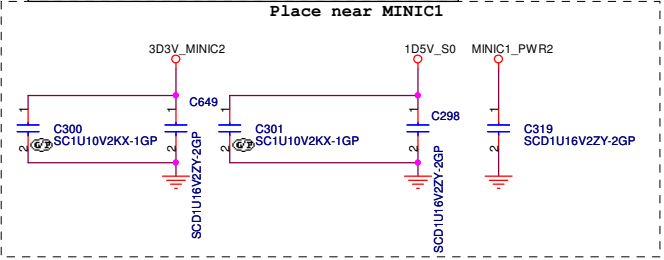
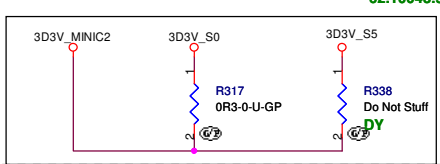
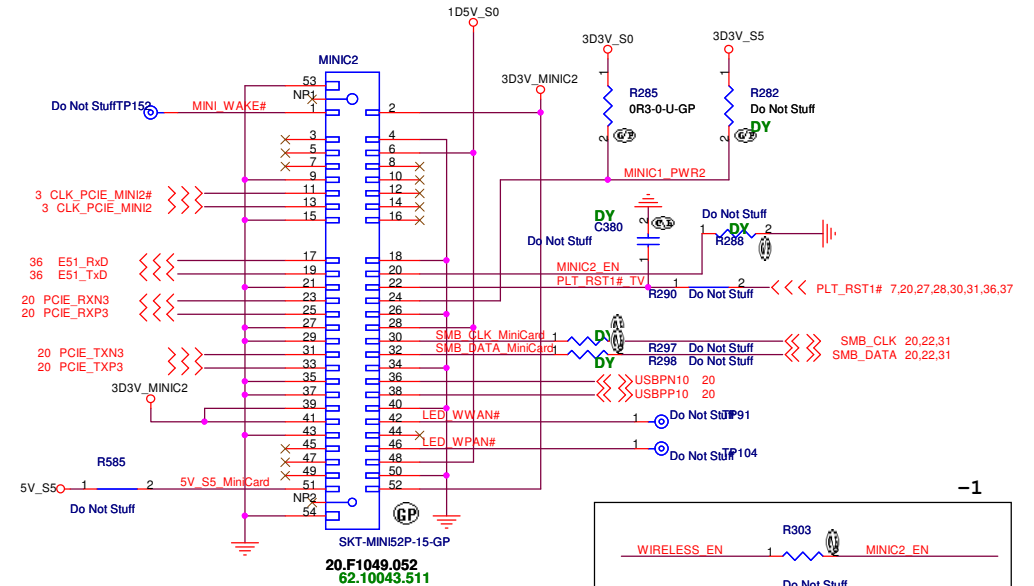
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
NEW CARD			
Title	Document Number		Rev
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Date: Tuesday, April 01, 2008	Sheet	31 of	50

Mini Card Connector(WLAN)



Mini Card Connector(TV)



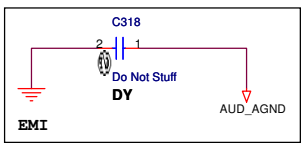
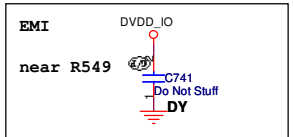
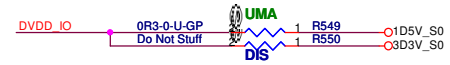
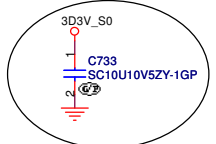
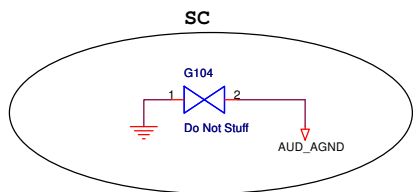
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

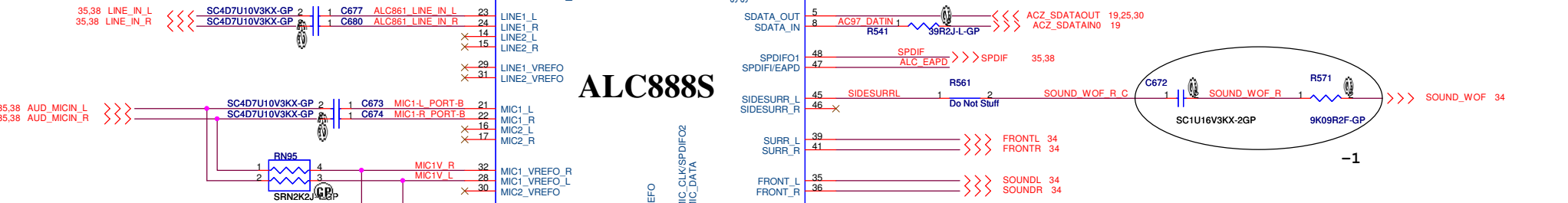
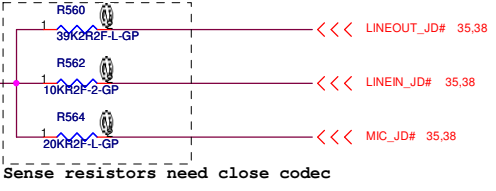
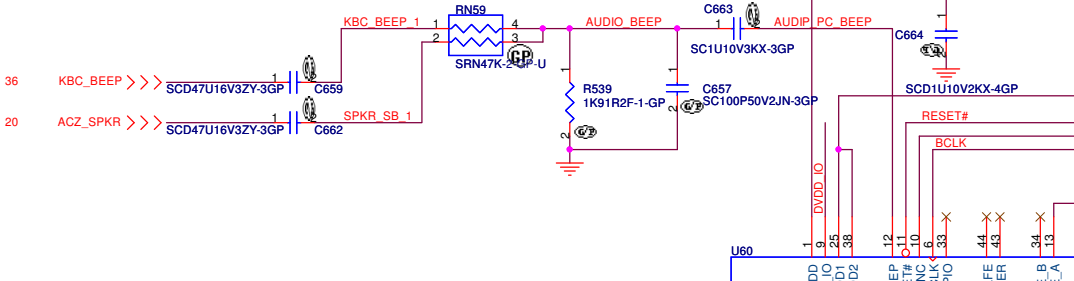
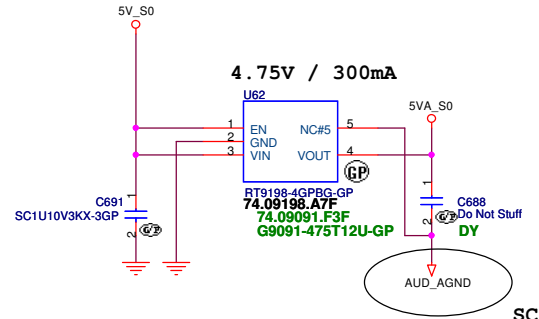
Title: **MINI CARD**

Size A3 | Document Number: **Eiger** | Rev: **-1**

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5VA_S0 "VAUX" Pull high to enable standby mode



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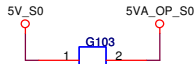
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title Azalia codec ALC268

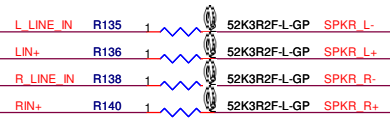
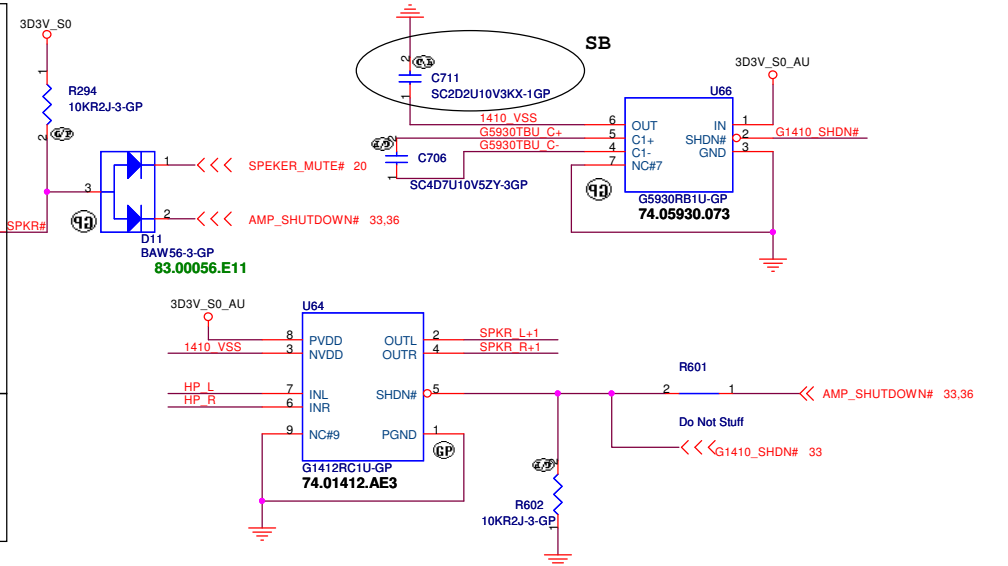
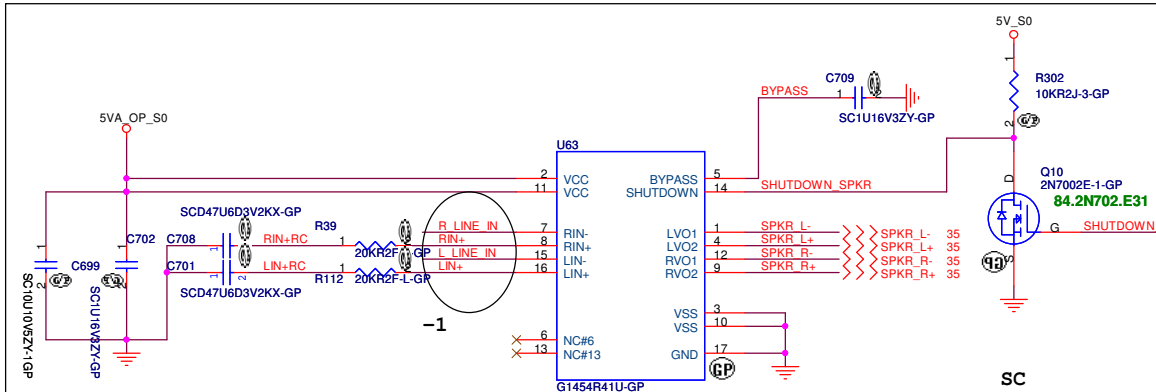
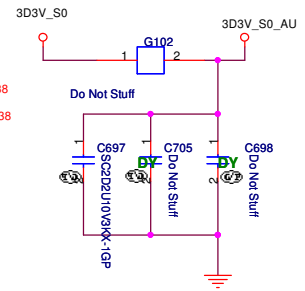
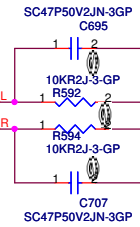
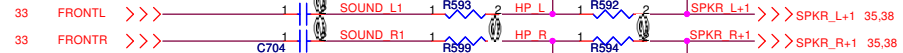
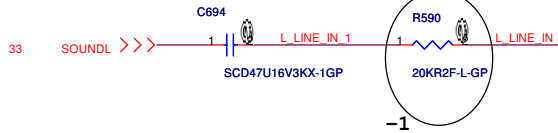
Size A3	Document Number Eiger	Rev -1
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Date: Tuesday, April 01, 2008 Sheet 33 of 50

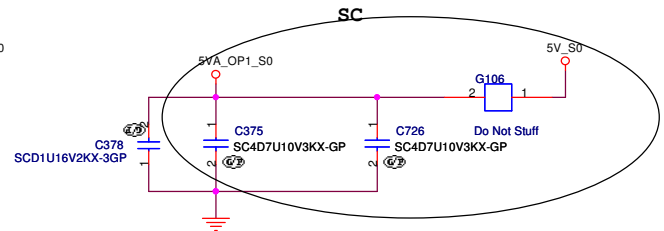
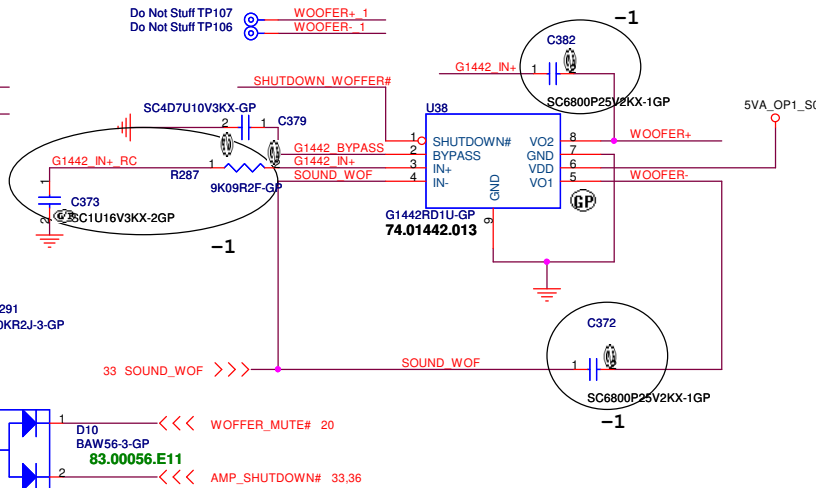
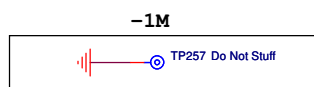
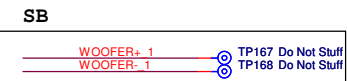
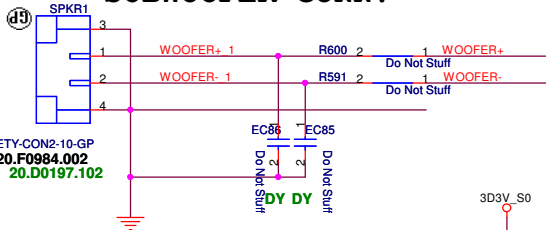
AUDIO OP AMPLIFIER



Do Not Stuff



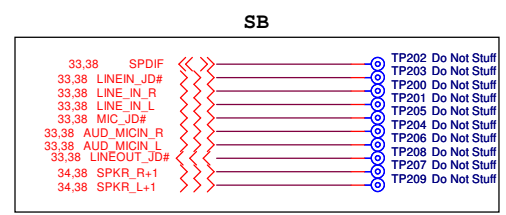
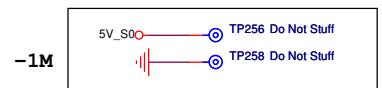
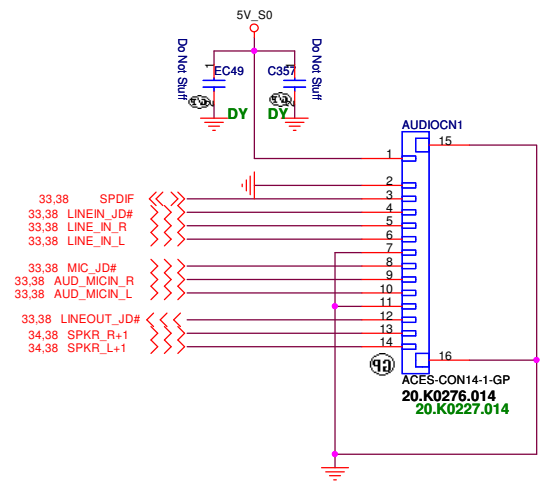
SUBWOOFER CONN.



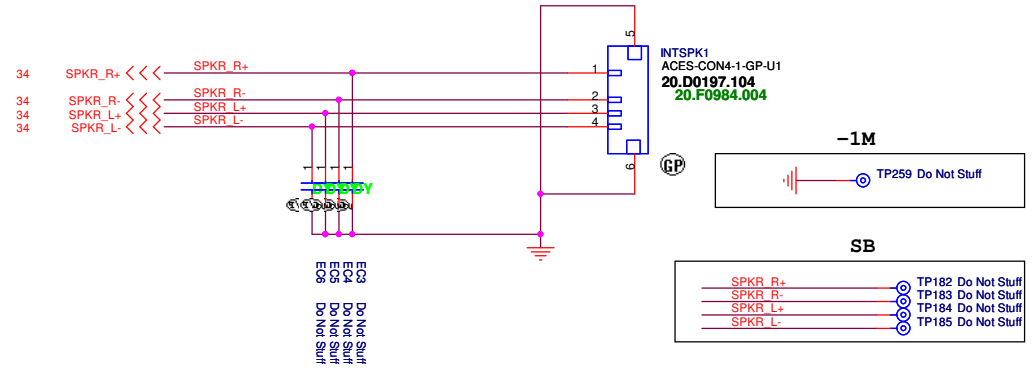
UMA

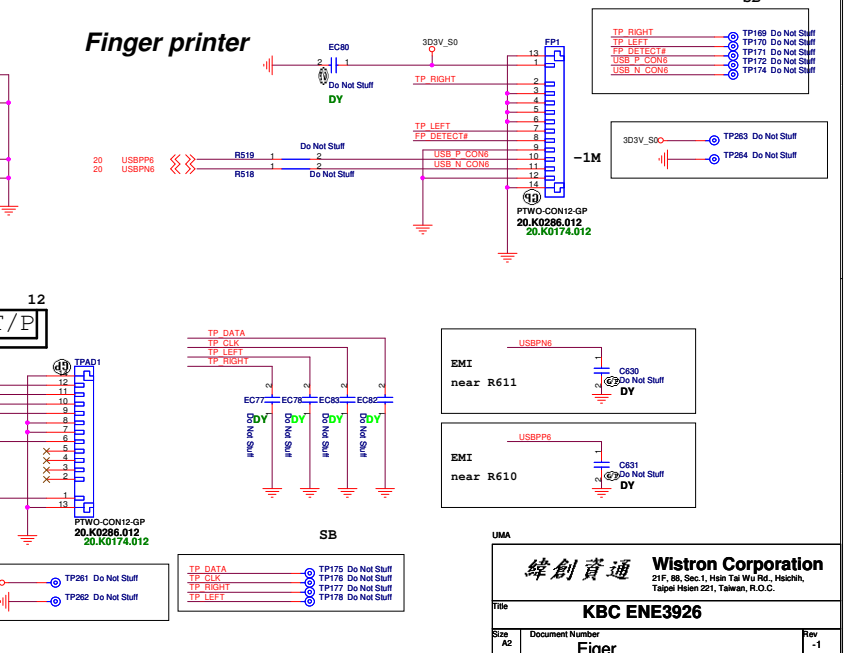
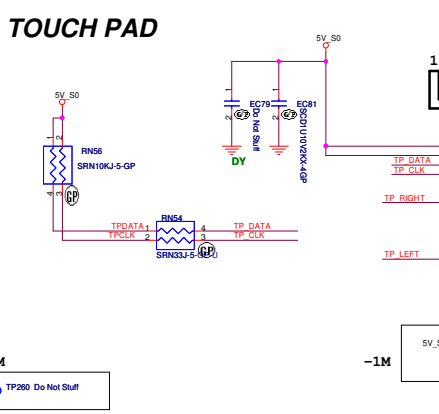
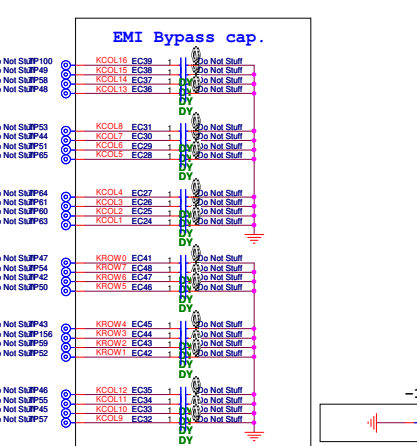
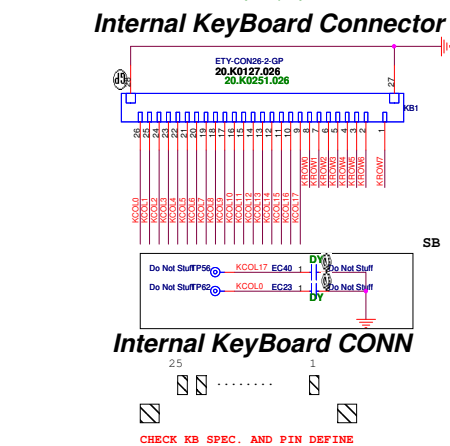
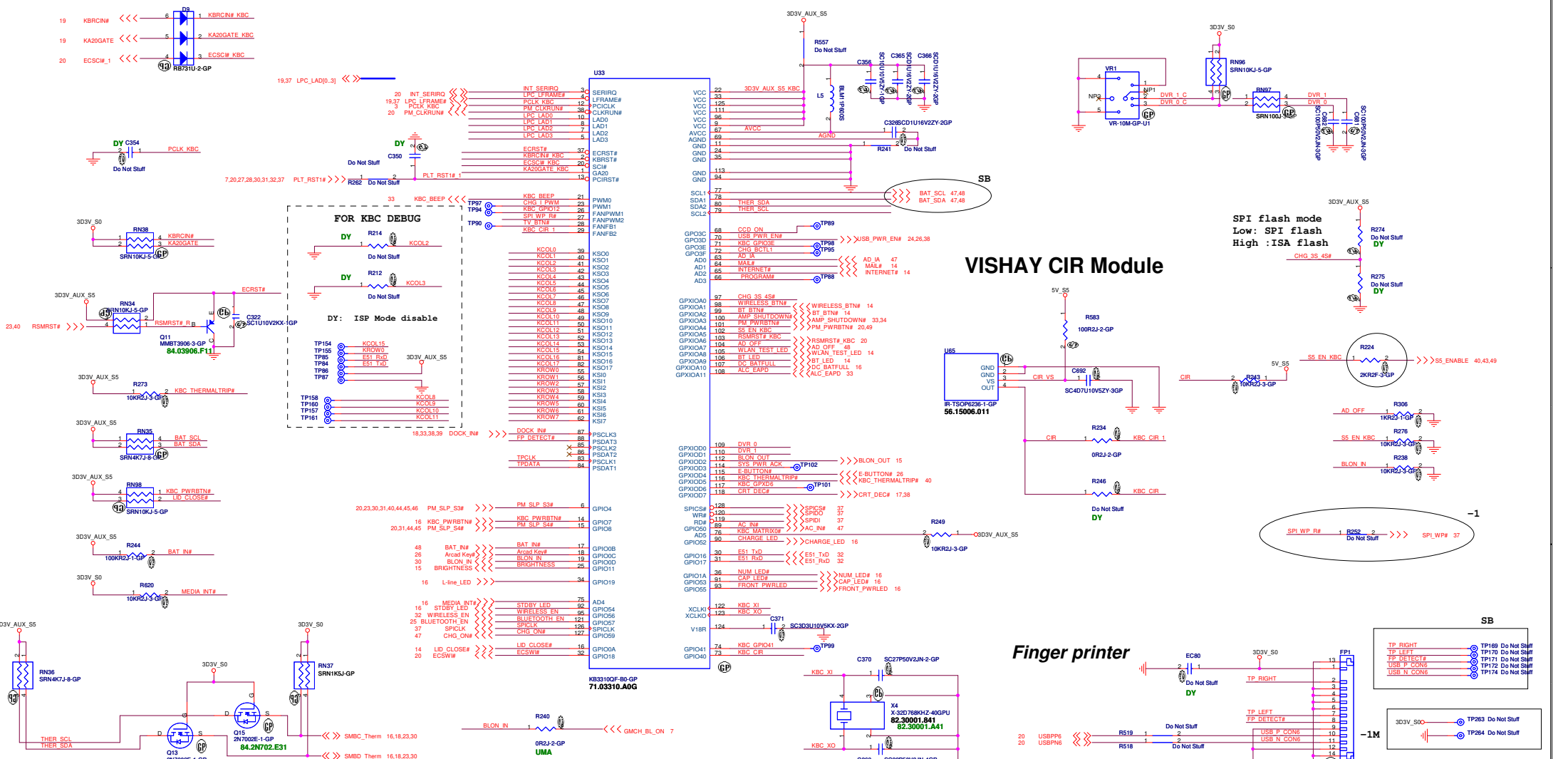
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Title		AUDIO AMP AND JACK	
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Eiger		-1	
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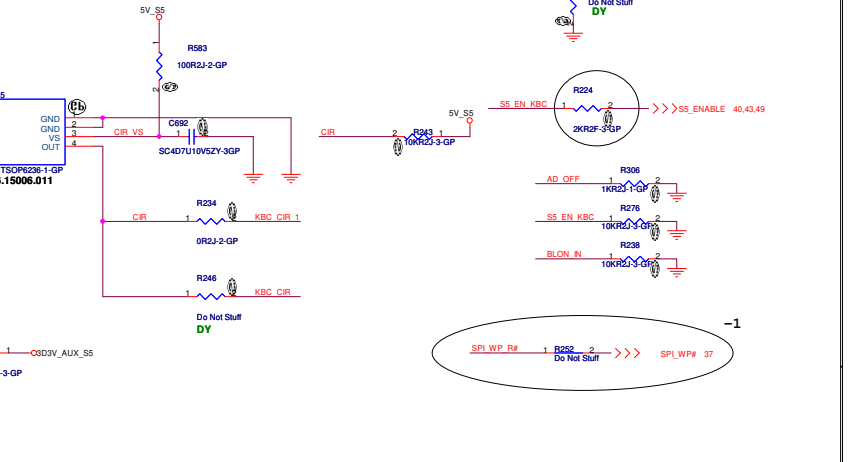


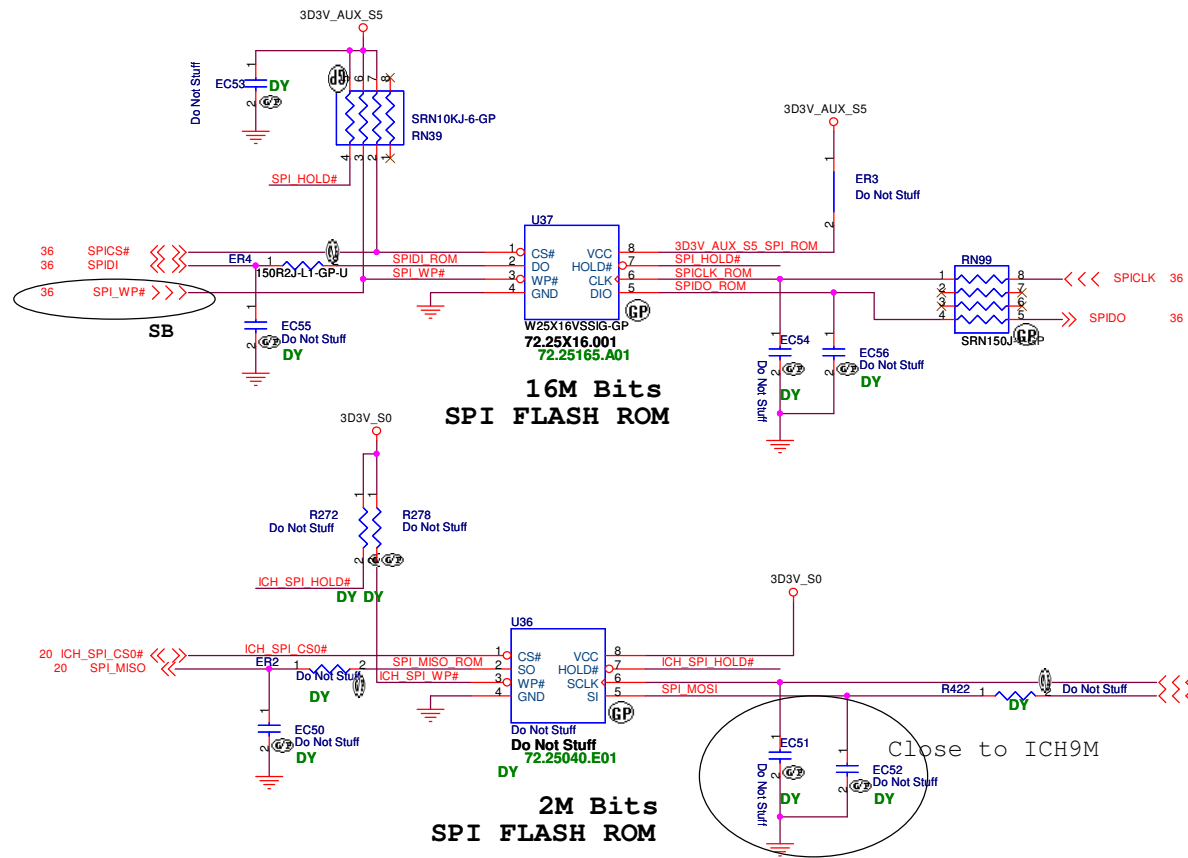
Internal Speaker



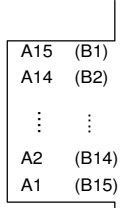


VISHAY CIR Module

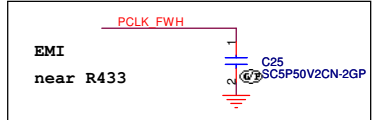




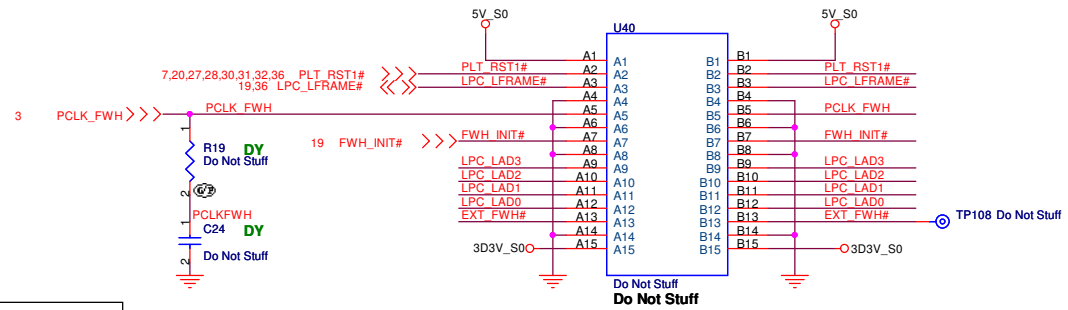
TOP VIEW



(BOTTOM VIEW)



GOLDEN FINGER FOR DEBUG BOARD



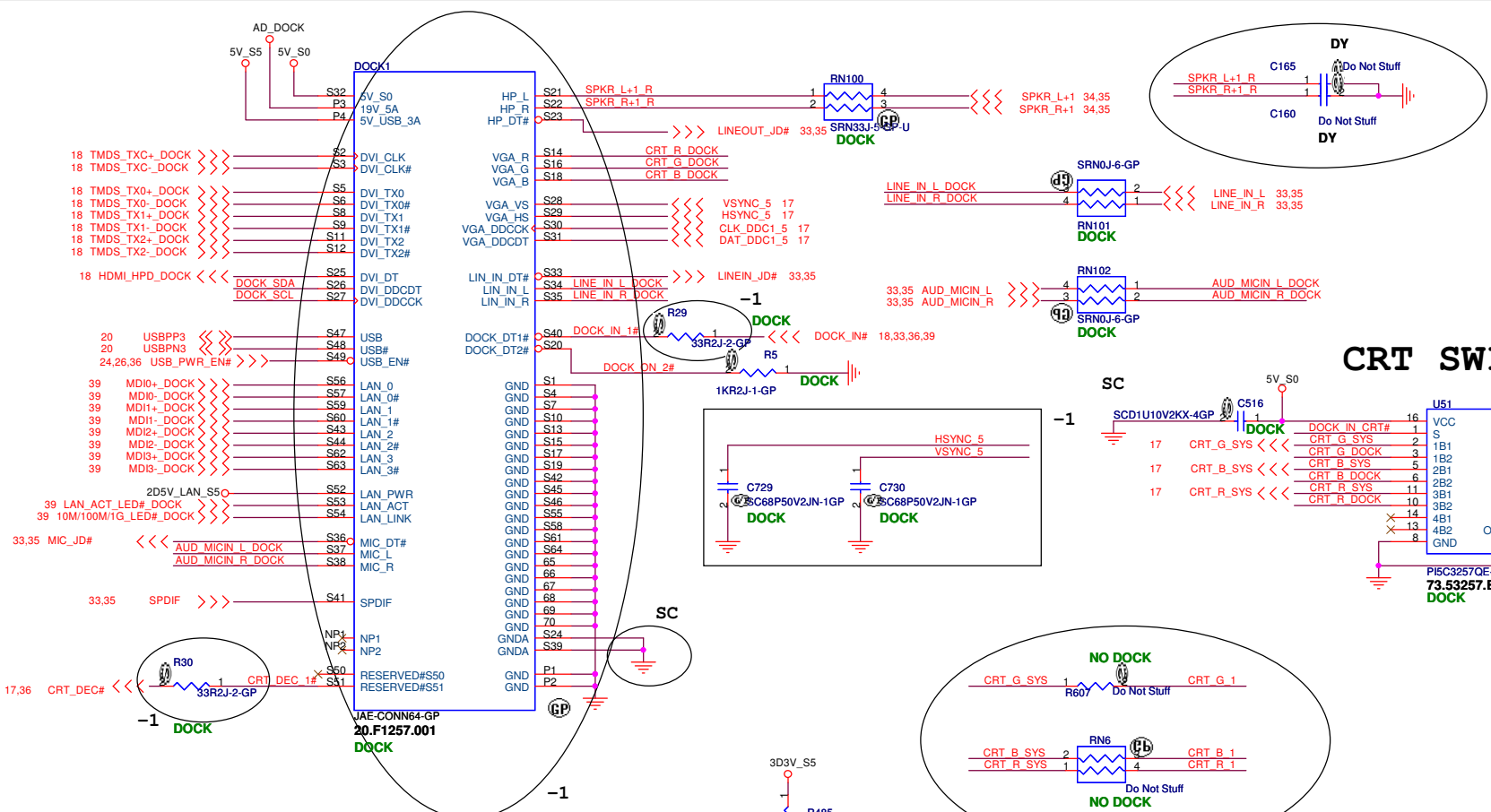
UMA

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Title: **BIOS**

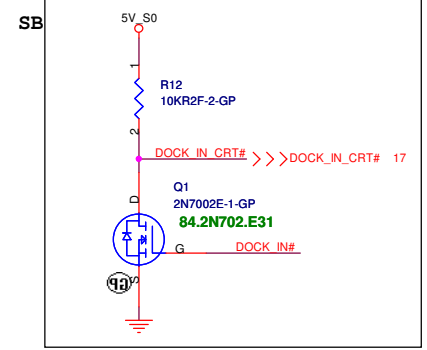
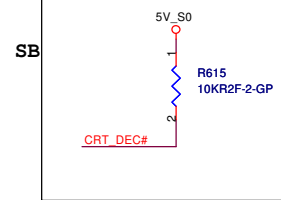
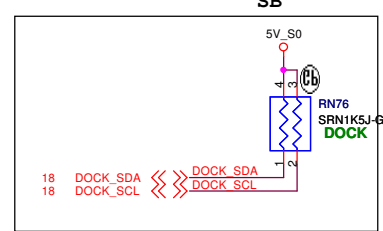
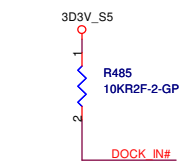
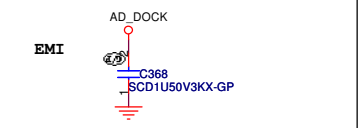
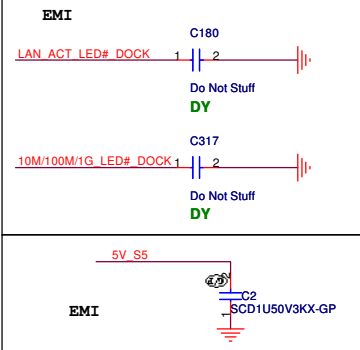
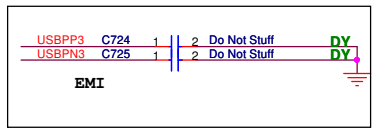
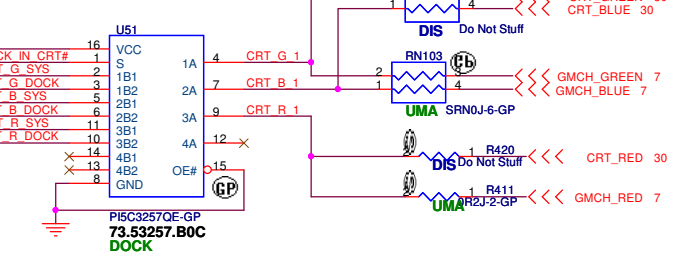
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Function	SEL	SYSTEM
A to 1	L	SYSTEM
A to 2	H	DOCK

CRT SWITCH



UMA

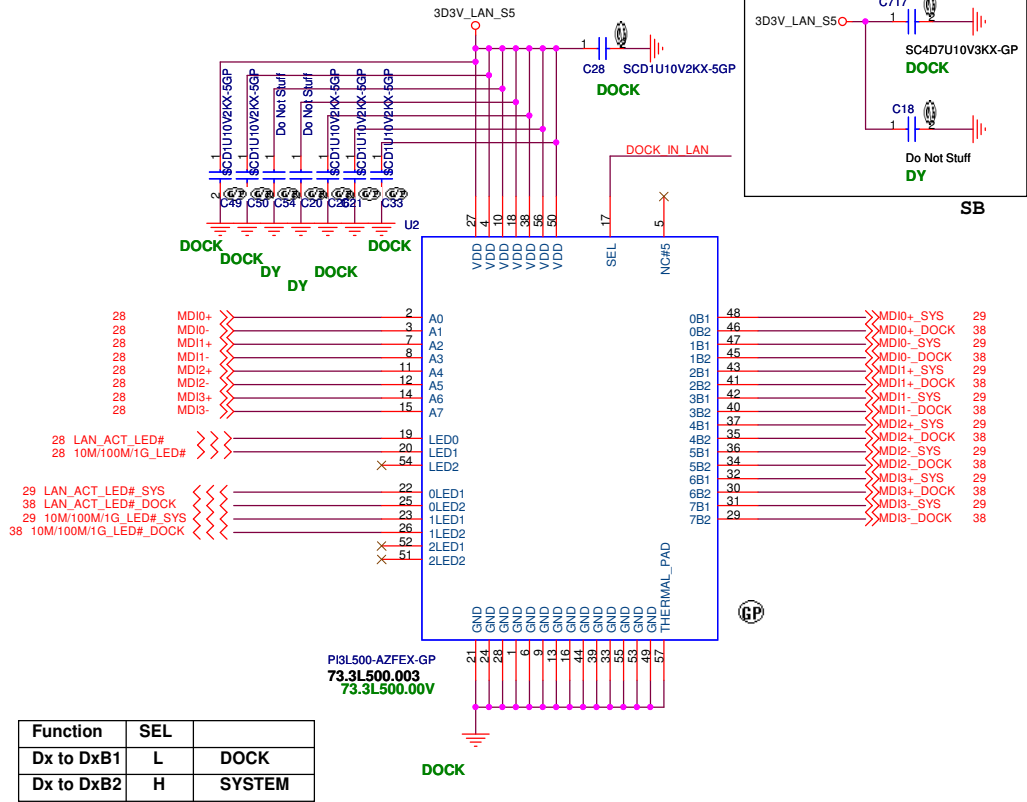
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Title: **EASY PORT4 (1/2)**

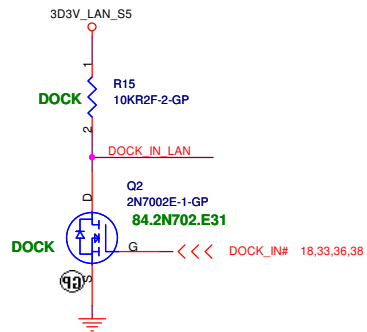
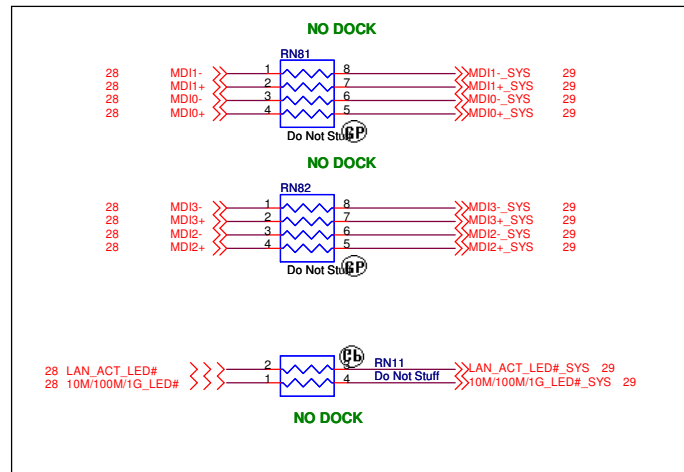
Size A3 Document Number: **Eiger** Rev: **-1**

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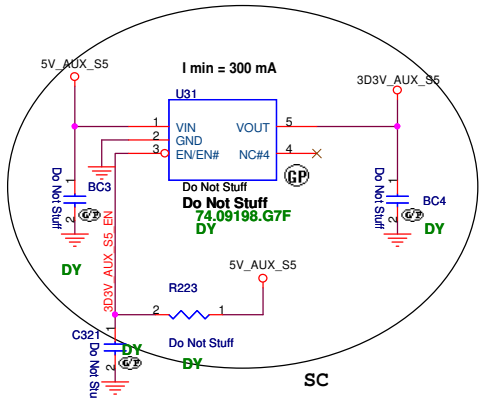
LAN switch



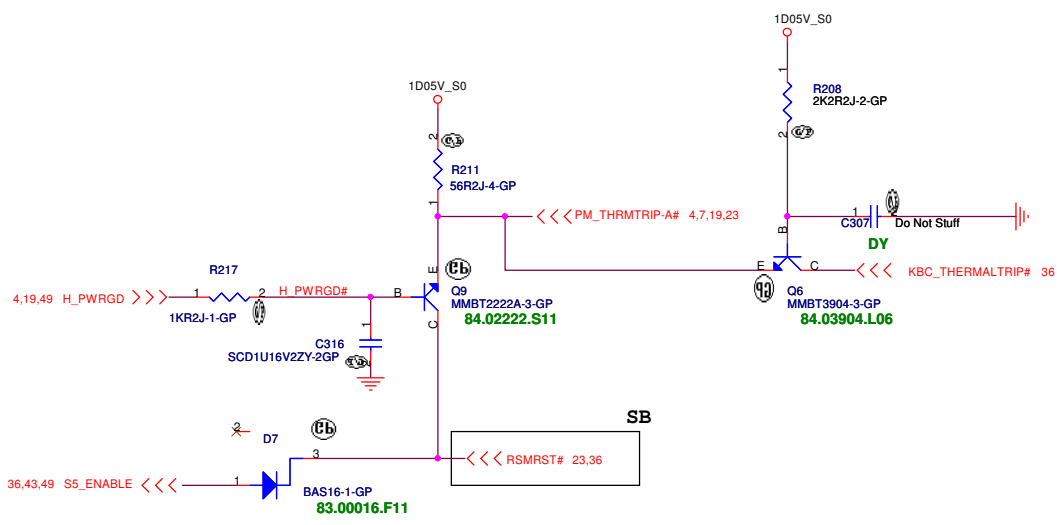
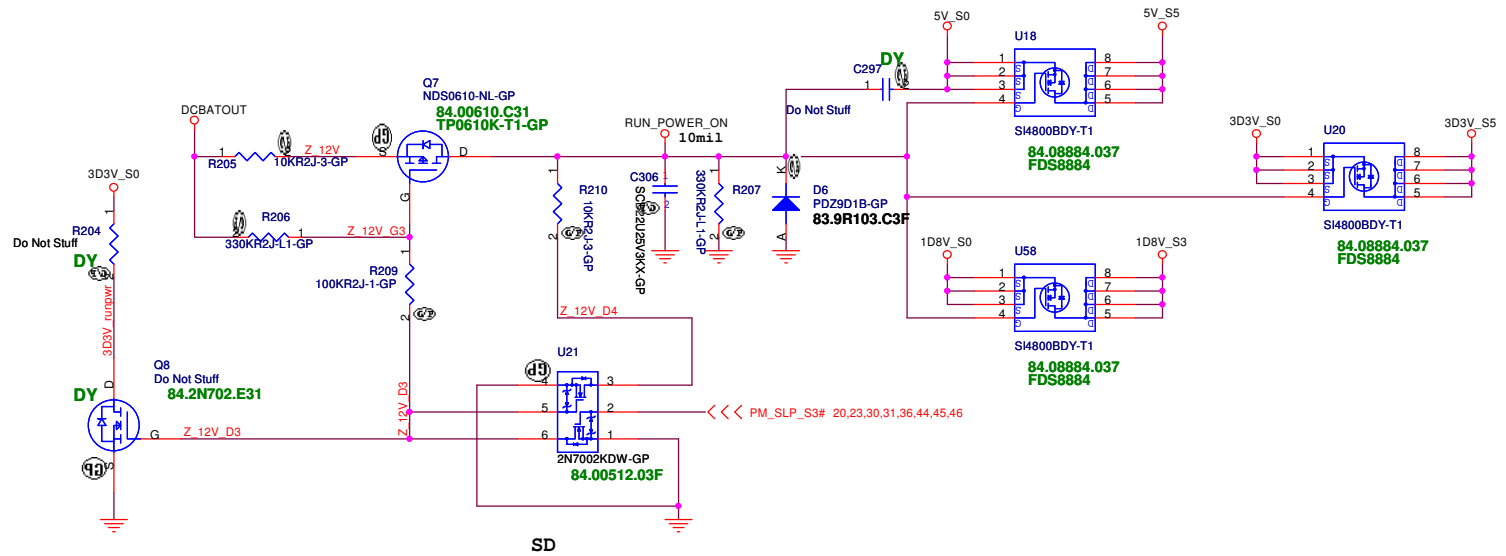
SB



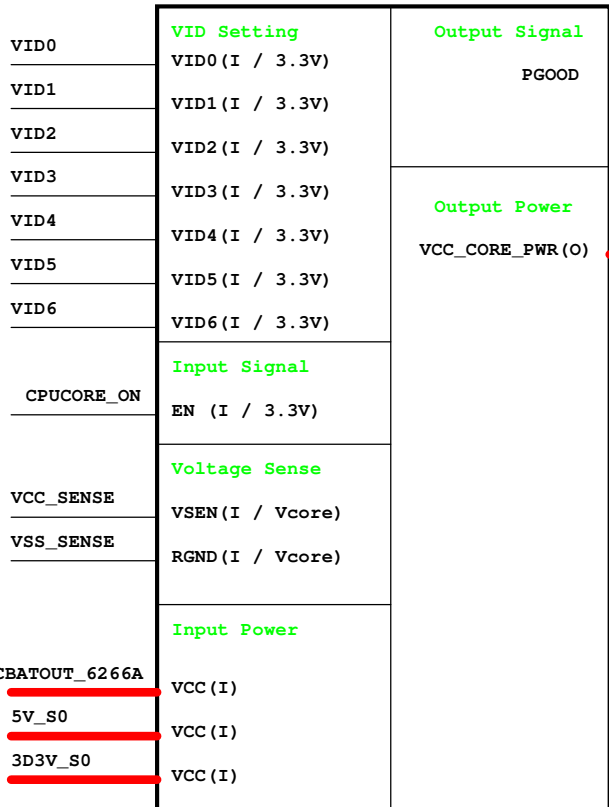
UMA



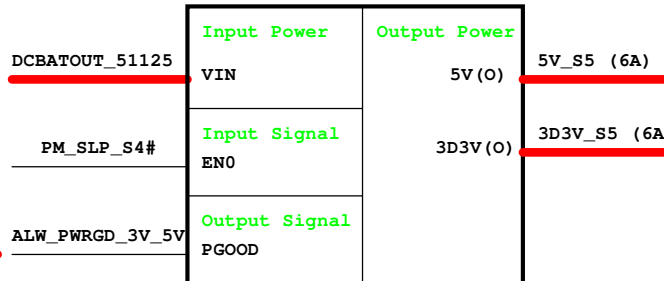
Run Power



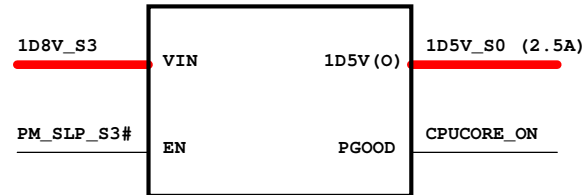
CPU_CORE
ISL6266A



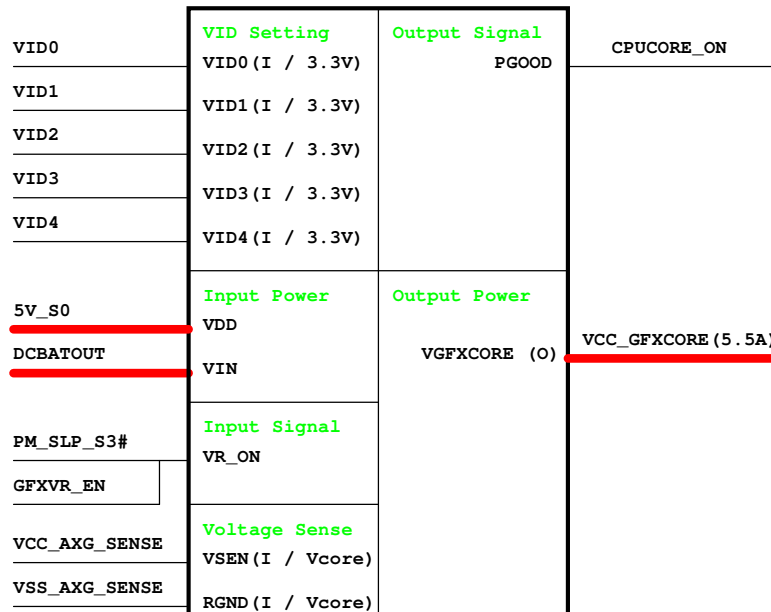
TPS51125
5V/3D3V



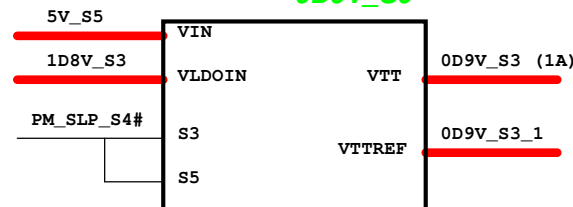
RT9018A
1D5V_S0



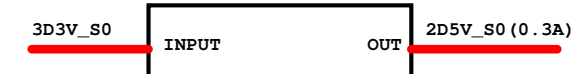
GFX_CORE
ISL6263A



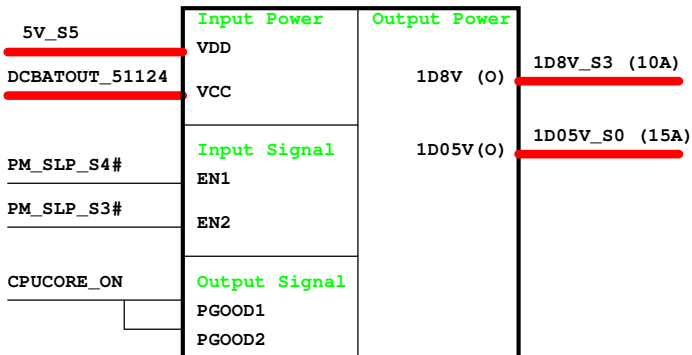
RT9026 0D9V_S0



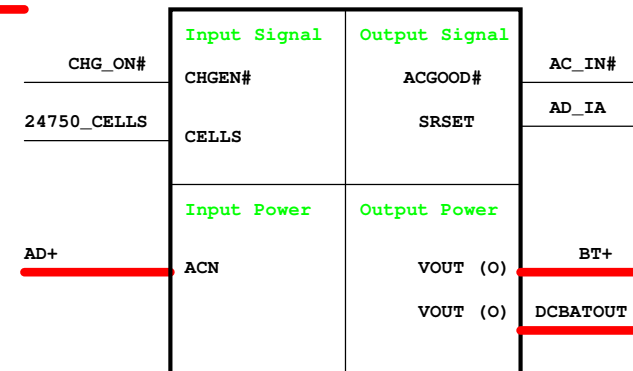
G9131 2D5V_S0



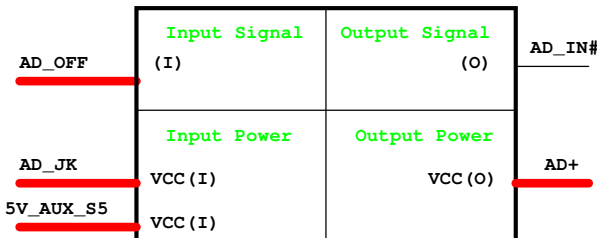
TPS51124
1D8V/1D05V



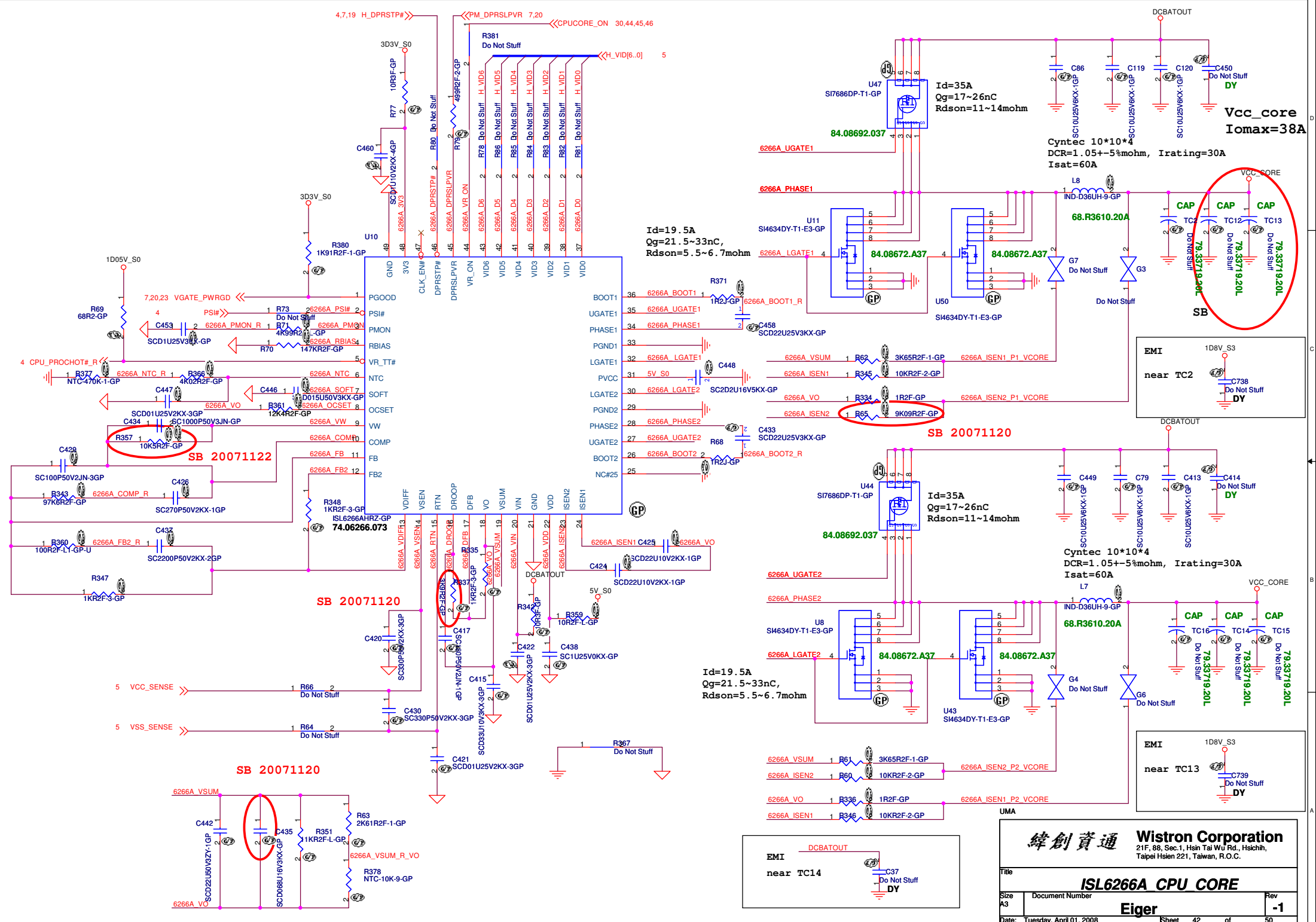
Charger BQ24750



Adapter



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Title: **ISL6266A CPU CORE**

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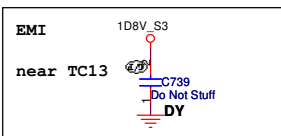
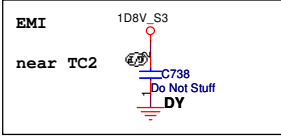
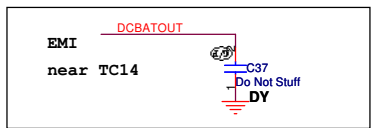
Vcc_core
Iomax=38A

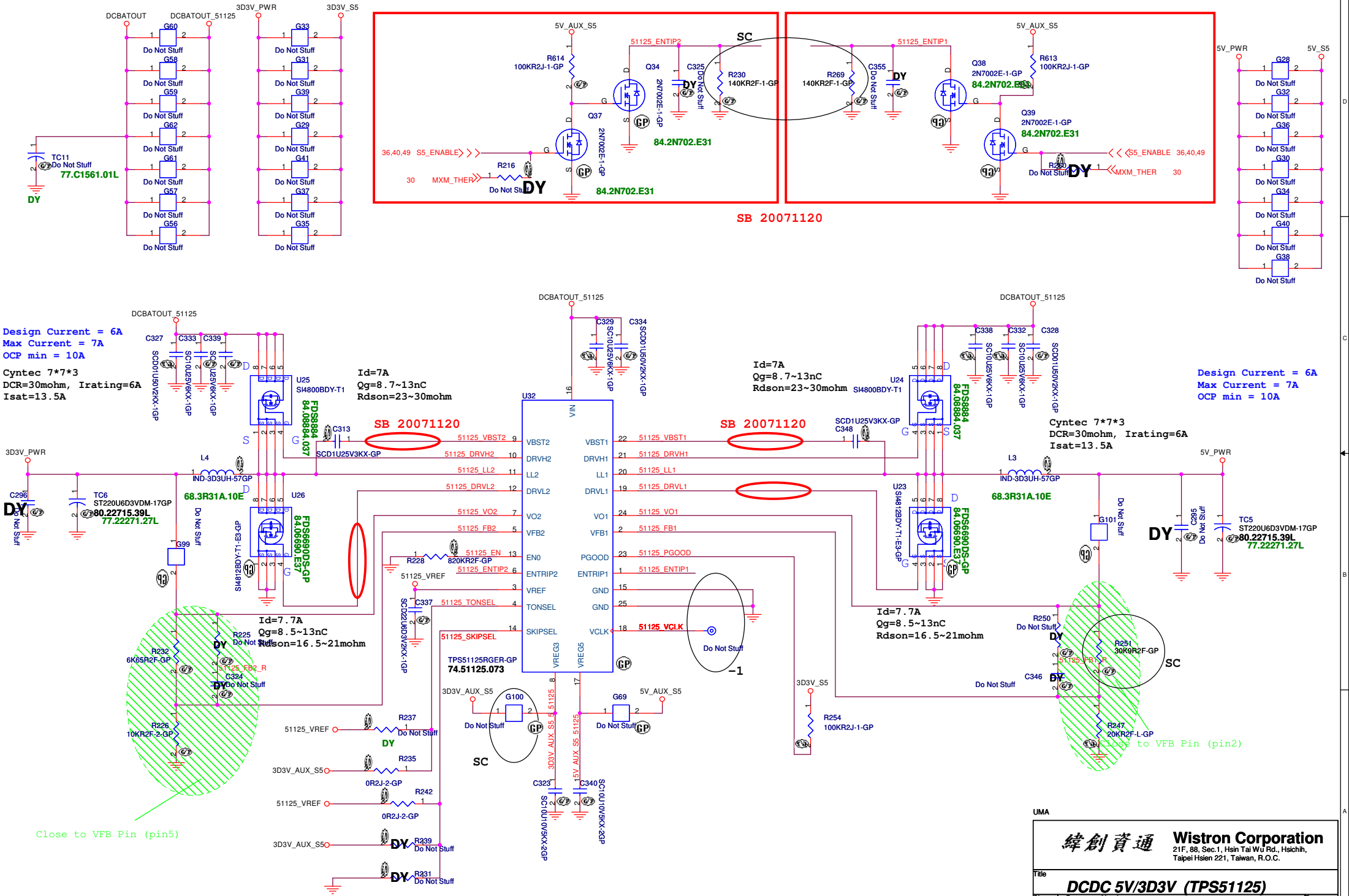
Cyntec 10*10*4
DCR=1.05+-5% mohm, Irating=30A
Isat=60A

SB 20071120

SB 20071120

SB 20071120





Design Current = 6A
 Max Current = 7A
 OCP min = 10A
 Cynotec 7*7*3
 DCR=30mohm, Irating=6A
 Isat=13.5A

Design Current = 6A
 Max Current = 7A
 OCP min = 10A

Close to VFB Pin (pin5)

UMA

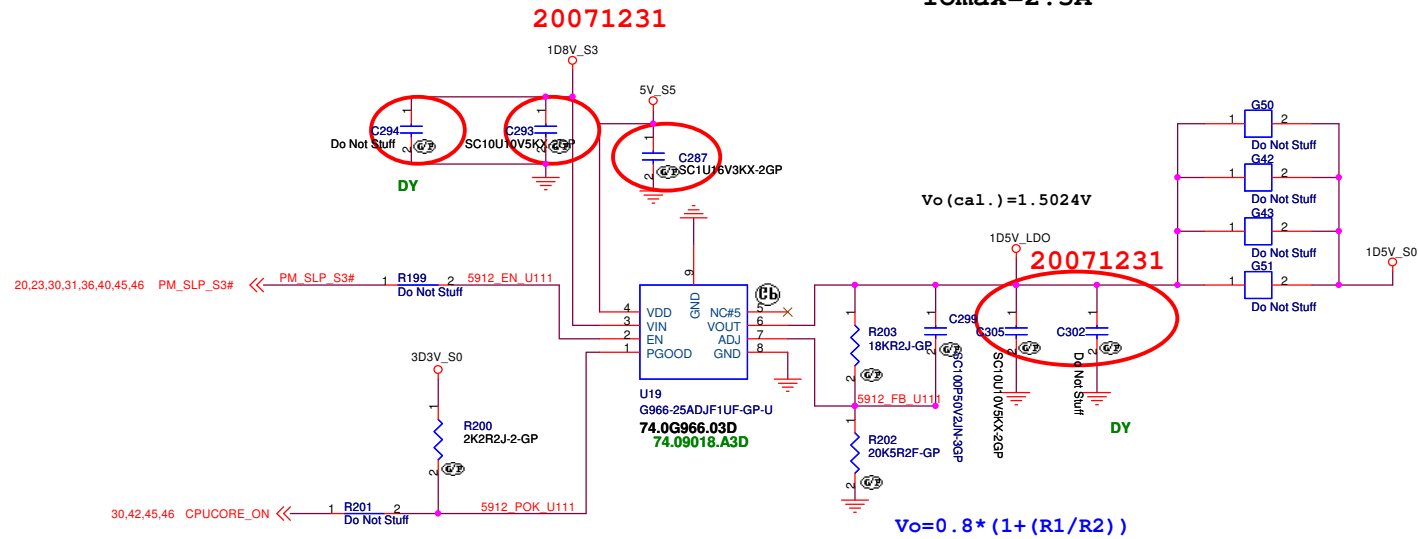
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC 5V/3D3V (TPS51125)**

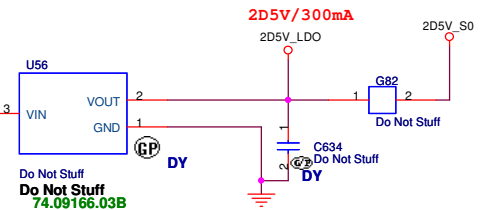
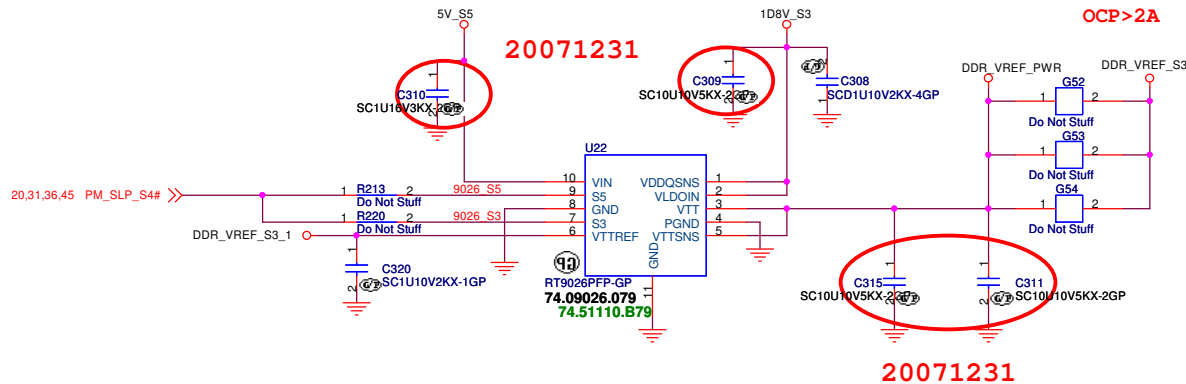
Size A3 Document Number: **Eiger** Rev: **-1**

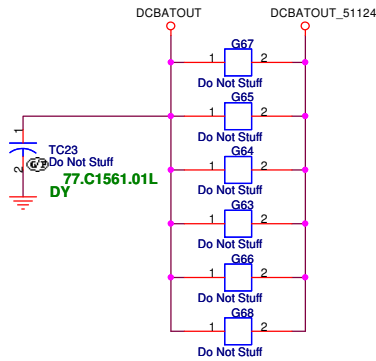
Date: Tuesday, April 01, 2008 Sheet 43 of 50

1D5V_S0
I_{omax}=2.5A

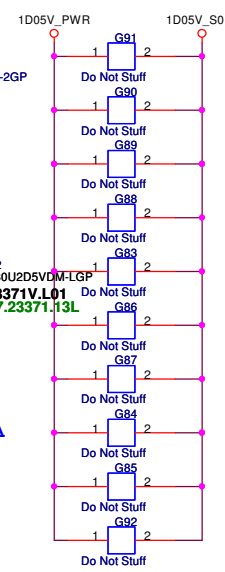
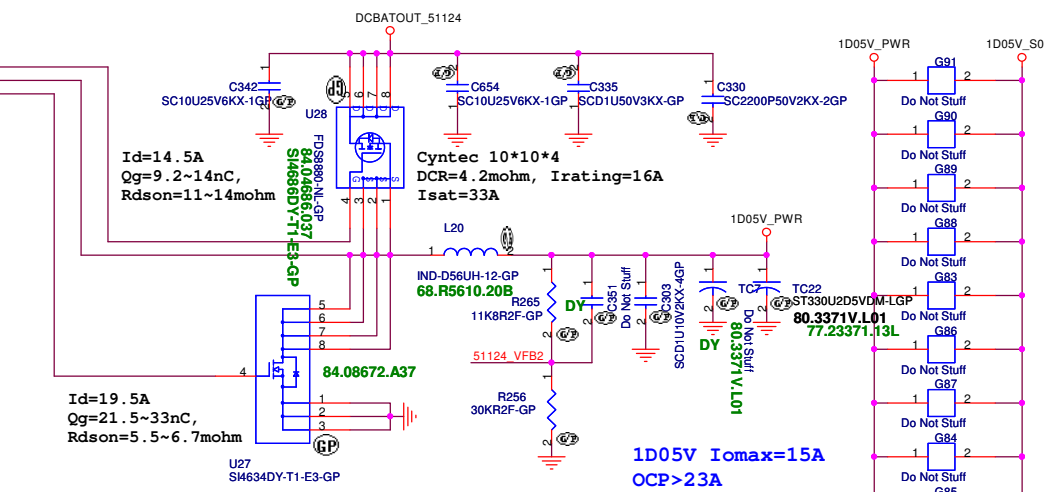
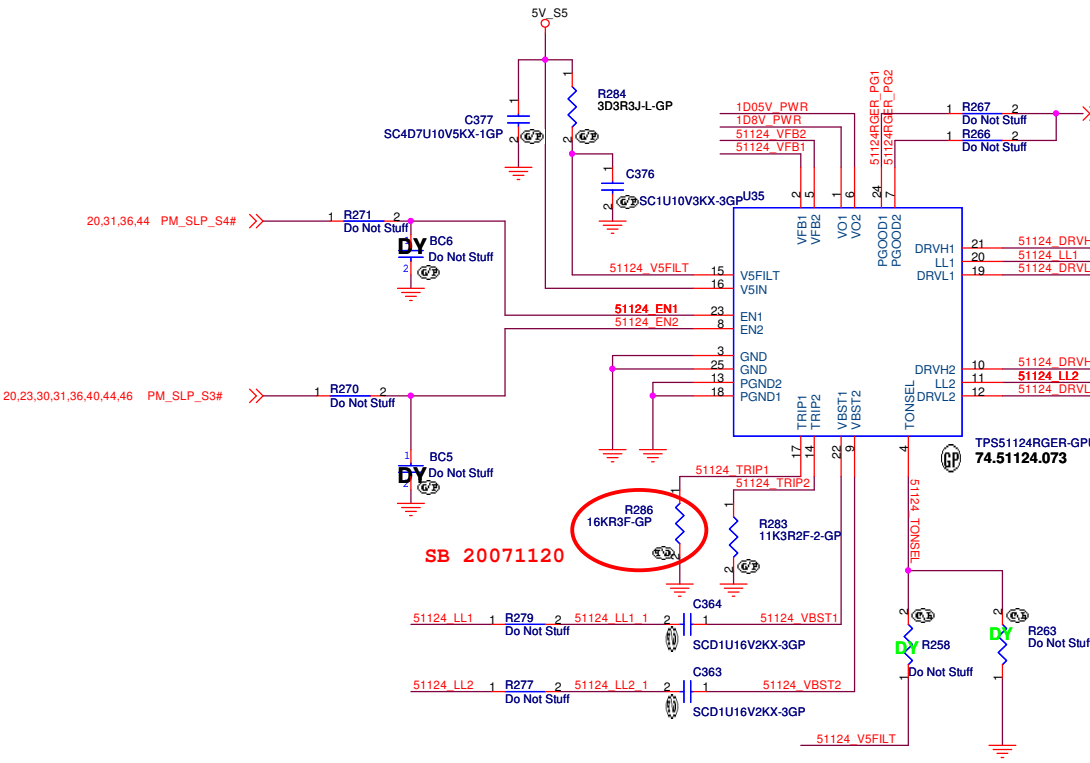
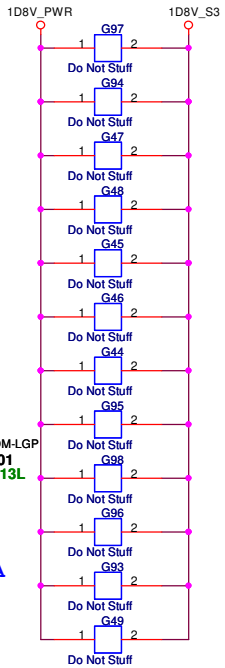
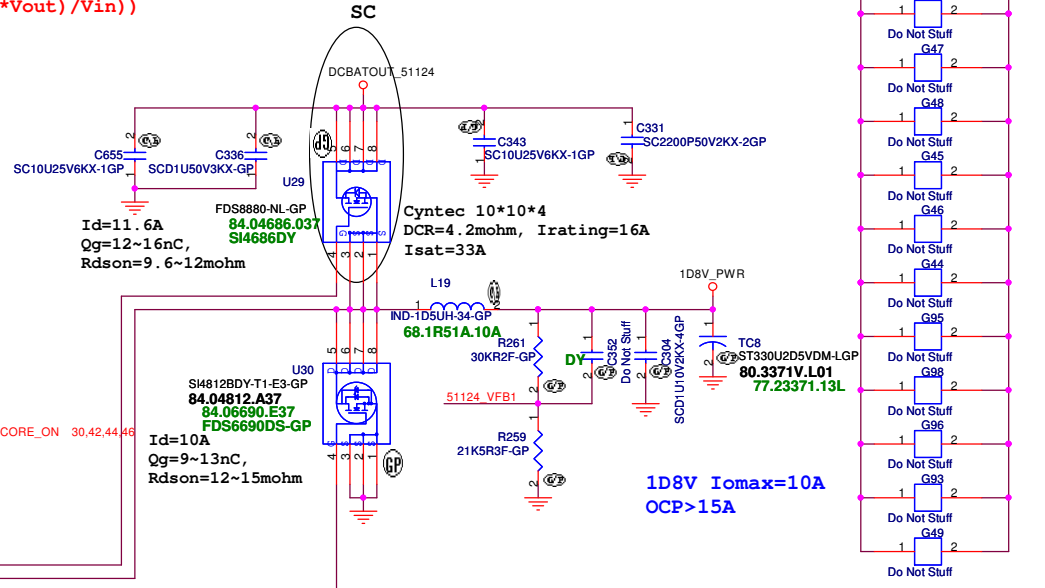


2D5V_S0
I_{omax}=1A
OCP>2A





$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$
 $I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

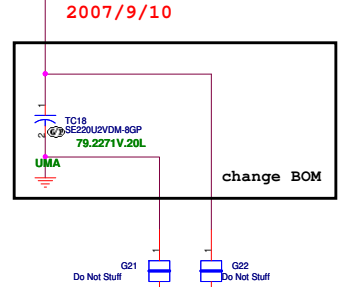
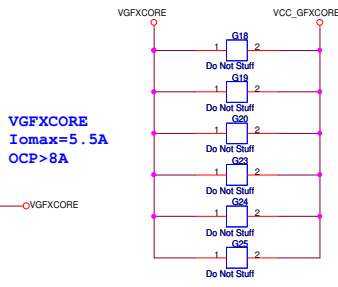
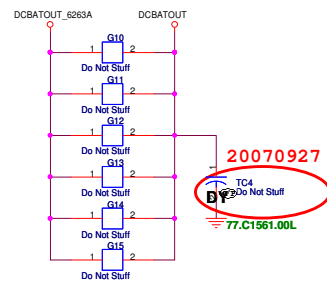
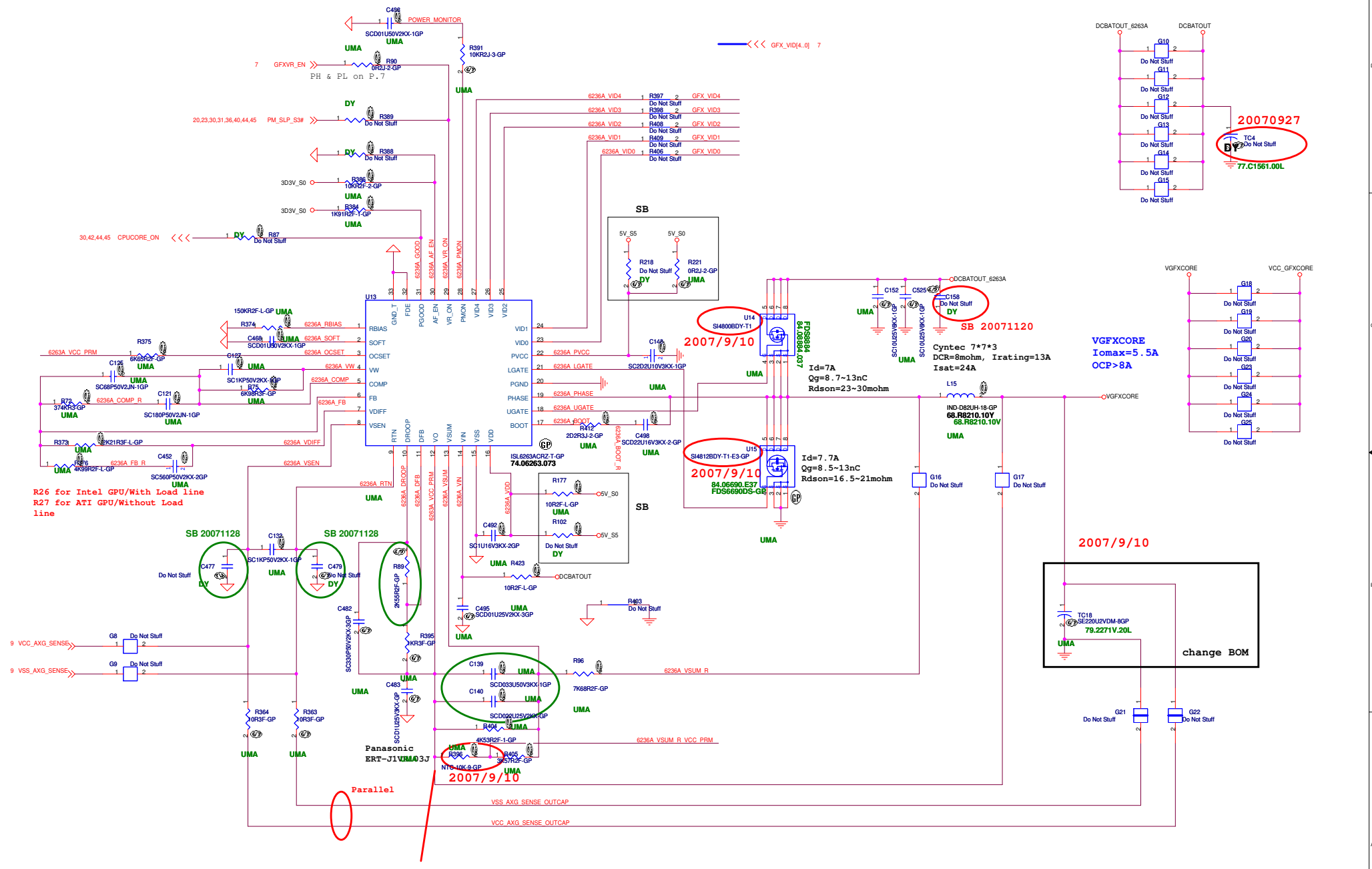


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

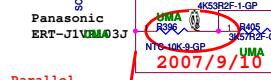
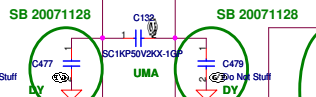
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

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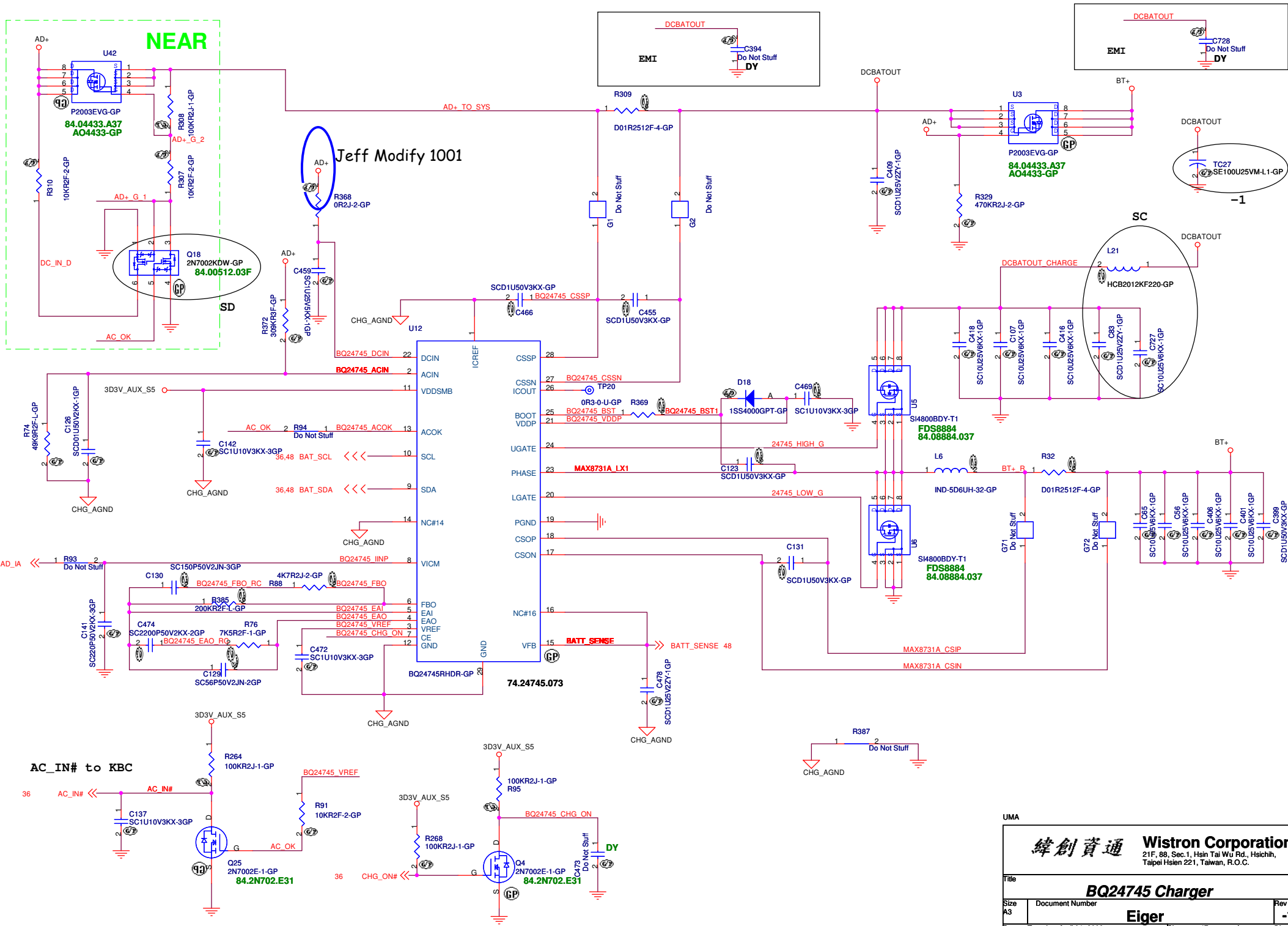
TPS51124 1D8V 1D05V
 Eiger
 Date: Tuesday, April 01, 2008 Sheet 45 of 50



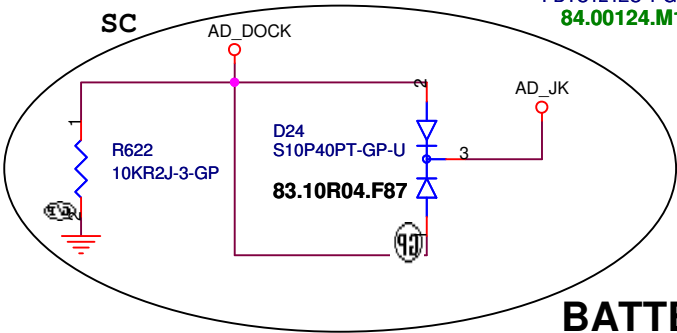
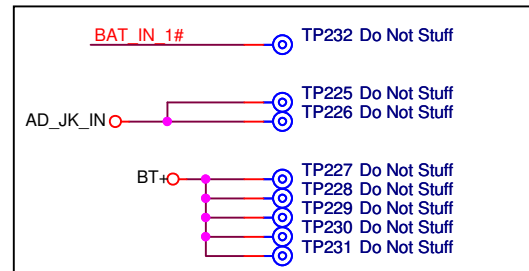
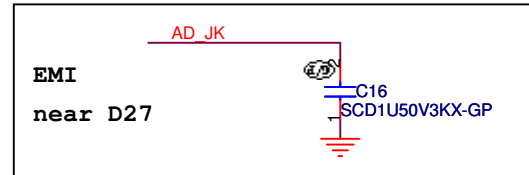
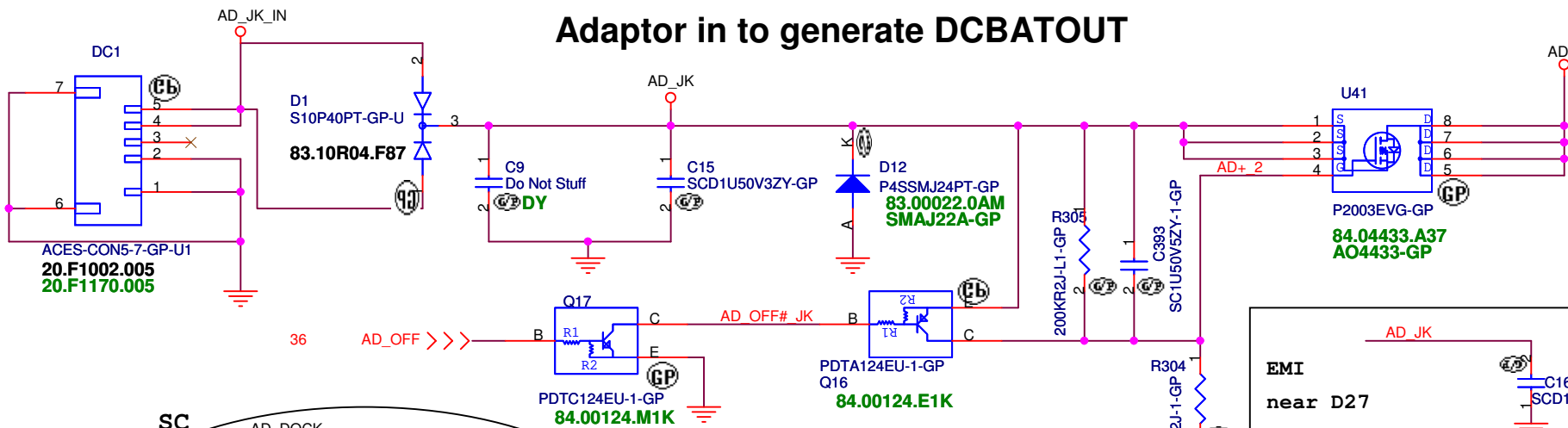
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line



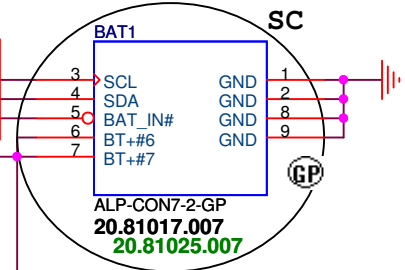
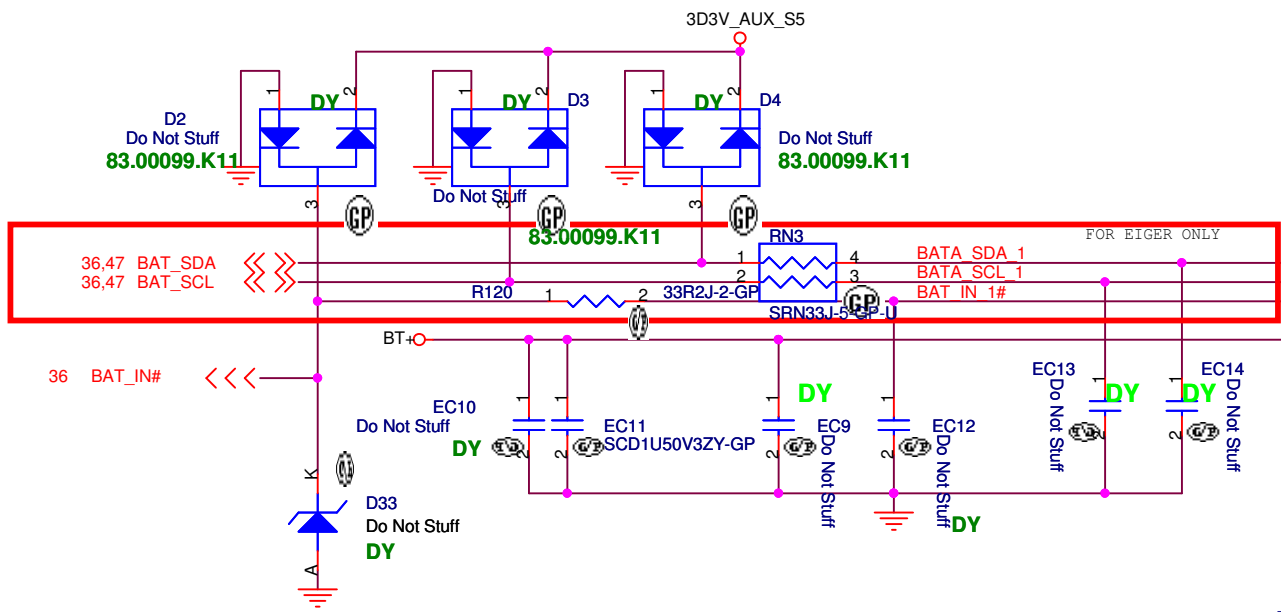
Place close to L1



Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



-1M

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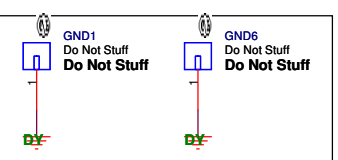
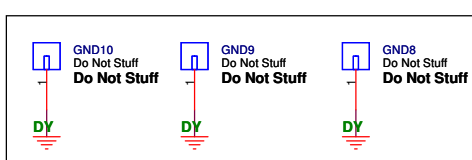
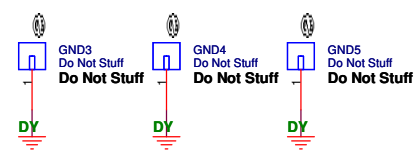
Title: **AD/BATT CONN**

Date: Tuesday, April 01, 2008

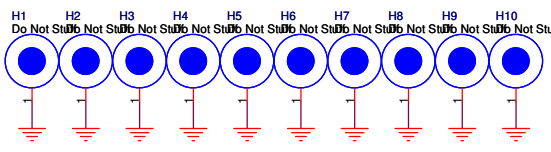
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Eiger

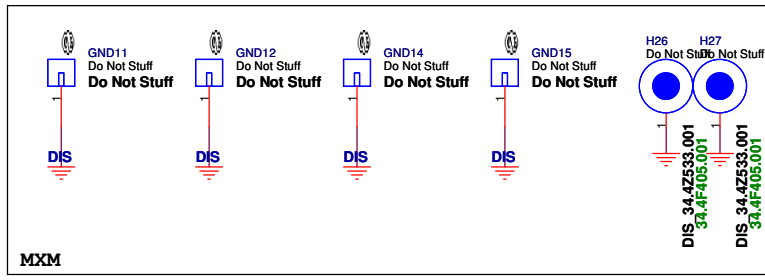
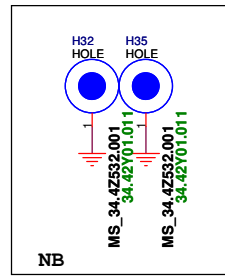
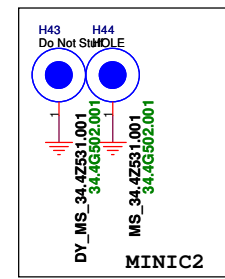
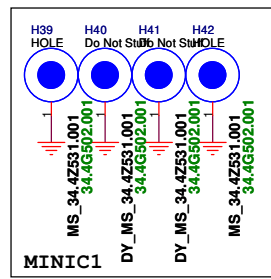
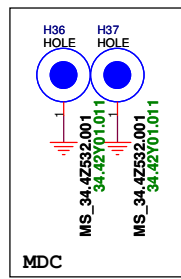
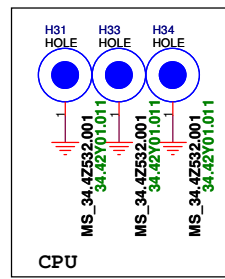
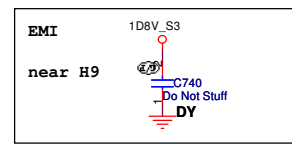
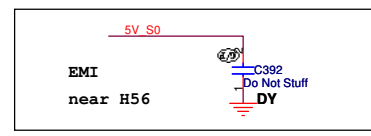
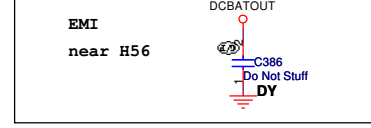
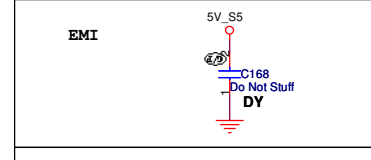
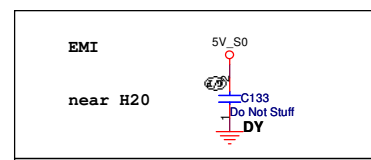
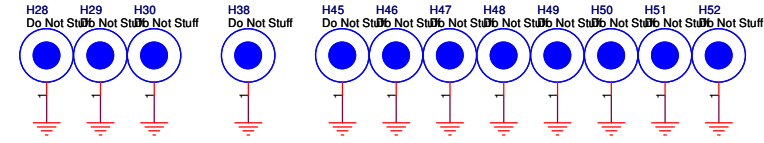
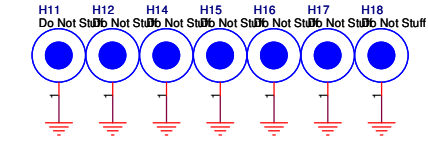
Rev -1



SB



HDD



SB

Check test point


- 3D3V_S0 TP92 Do Not Stuff
- 3D3V_AUX_S5 TP223 Do Not Stuff
- 3D3V_S5 TP173 Do Not Stuff
- 5V_S5 TP224 Do Not Stuff
- 20,36 PM_PWRBTN# <<< TP222 Do Not Stuff
- 4,19,40 H_PWRGD <<< TP221 Do Not Stuff
- 36,40,43 S5_ENABLE <<< TP166 Do Not Stuff
- 4,6 H_CPURST# <<< TP183 Do Not Stuff

Test Point 放在 Dimm Door 打開可量測處

UMA

- EC SB01/07/ DY R175 (fix can not boot)
- EC SB02/07/ change R184 (intel spec change)
- EC SB03/10/ mount L2,C221 (intel spec change)
- EC SB04/15/ modify LCD2 pin define(add dig-MIC,backlight)
- EC SB05/17/ DOCK_IN_CRT# logic change
- EC SB06/18/ change HDMI level shift IC setting
- EC SB07/19/ change R606(meet HDA SPEC)
- EC SB08/23/ change PURE_HW_SHUTDOWN# ,PM_THRMTRIP-A# schematic
- EC SB09/26/ change C648 ,deltree poly switch
- EC SB10/27/ change R555,R557,R559 (vendor request)
- EC SB11/30/ change R612 (vendor request)
- EC SB12/34/ add C711 (fix audio noise)
- EC SB13/36/ add SPL_WP# (BIOS write protect)
- EC SB14/38/ add CRT_DEC# (Acer change spec)
- EC SB15/38/ add dock/no dock option schematic
- EC SB16/40/ D7(power sequencing)
- EC SC01/16/ R595,R596,R597,R598(LED)
- EC SC02/18/ HEMI level shift & switch solution change
- EC SC03/19/ ESATA function
- EC SC04/23/ H/W Thermal shut down,power off Sequence
- EC SC05/24/ Add ESATA circuit
- EC SC06/30/ Add R116(MXM acrst# Acer request)
- EC SC07/33/ Add audio ground
- EC SC08/34/ Change audio AMP circuit
- EC SC09/38/ Add RC circuit to reduce audio noise
- EC SC10/40/ 3D3V_AUX_S5 from U32 internal LDO
- EC SC11/43/ Change 5V to 5.1V
- EC SC12/47/ Isolate Change IC switching high side MOS input power
- EC SC13/48/ Isolate AD19V in and Dock19V in

UMA

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Title EC Tracking Record		
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