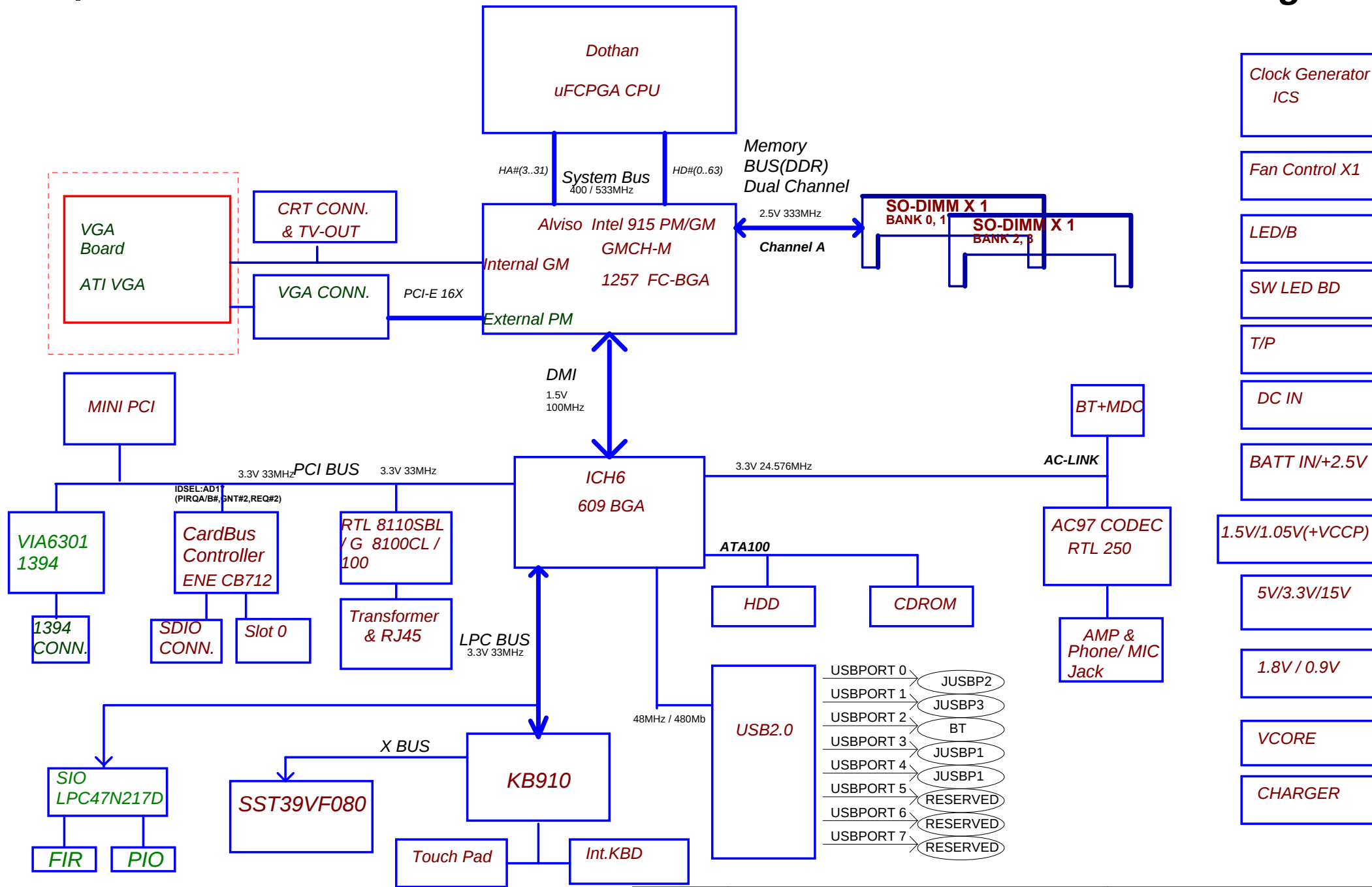


Sonoma Dothan EAL50_1
LA2362 Schematic

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				Date:	Friday, March 11, 2005
				Sheet	1 of 52



I2C / SMBUS ADDRESSING

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	F
CARD BUS	AD20	1	A
Cardreader			B
1394	AD16	2	E
Wireless LAN(MINI PCI)	AD18	3	G,H

@ Depop
1@ EAL51
2@ EAL50
1@ EAL51 VALUE (DELETE SIO/1394)

Power Managment table

Signal State	+12VALW +3VALW +5VALW	+2.5V +3V +5V +12V	+CPU_CORE +VCCP +5VS +3VS +2.5VS +1.8VS +1.25VS +1.5VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Ceramic Capacitor Spec
Guide:

Temperature Characteristics:								
Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+-.05PF	+-.0.1PF	+-.0.25PF	+-.0.5PF	+-.1PF	+-.2%	+-.3%	+5%

K	M	N	P	Q	V	X	Z	
+-.10%	+-.20%	+-.30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

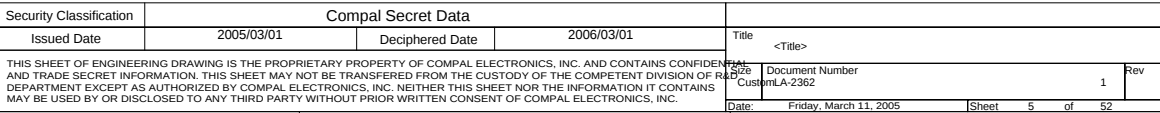
	PCB Rev	Data
Bringup-Build SST-Build	0.1	
PT-Build		
ST-Build		
QT-Build		

SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK
0.0A		First Release

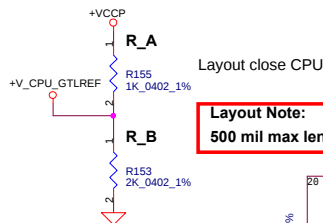
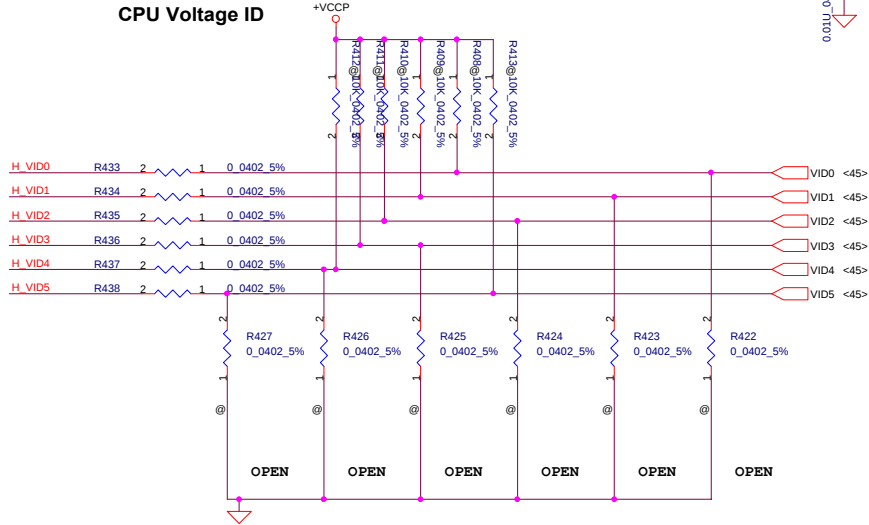
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	THERMAL SENSOR (LM75)	SODIMM	CLK CHIP	MINI PCI	LCD	VGA Thermal ADM1032
SMB_EC_CK1 SMB_EC_DA1	PC87591L	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	PC87591L	✗	✗	✗	✓	✓	✗	✗	✗	✗	✓
ICH_SMBCLK ICH_SMBDATA	ICH6-M	✗	✗	✗	✗	✗	✓	✓	✗	✗	✗
LCD_DDCCLK LCD_DDCDATA	ALVISO GM-GP	✗	✗	✗	✗	✗	✗	✗	✗	✓	✗



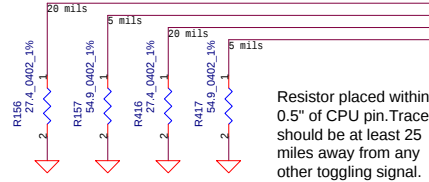
For test only ,Cmos output

CPU Voltage ID

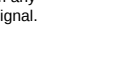
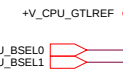
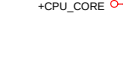
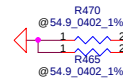
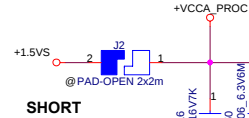


Layout close CPU

Layout Note:
500 mil max length



Resistor placed within
0.5" of CPU pin.Trace
should be at least 25
mils away from any
other toggling signal.



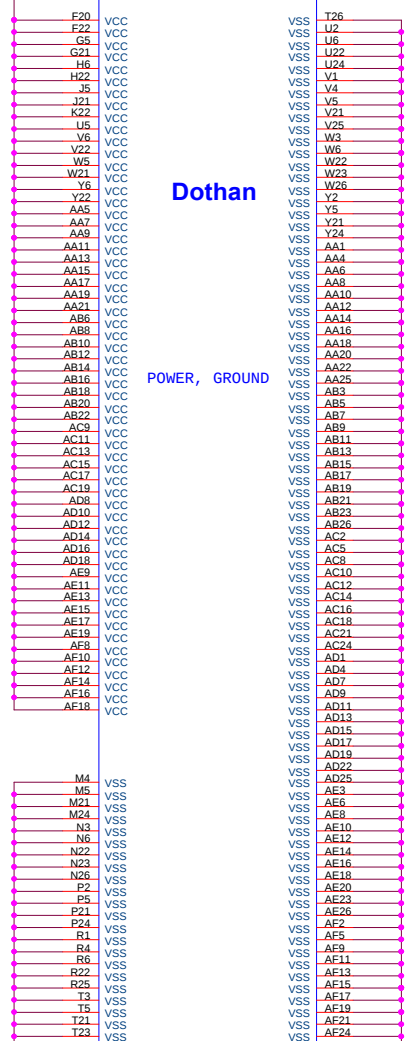
Dothan

POWER, GROUND, RESERVED SIGNALS AND NC

TYCO_1612365-1_Dothan

+CPU_CORE

JCPU1C

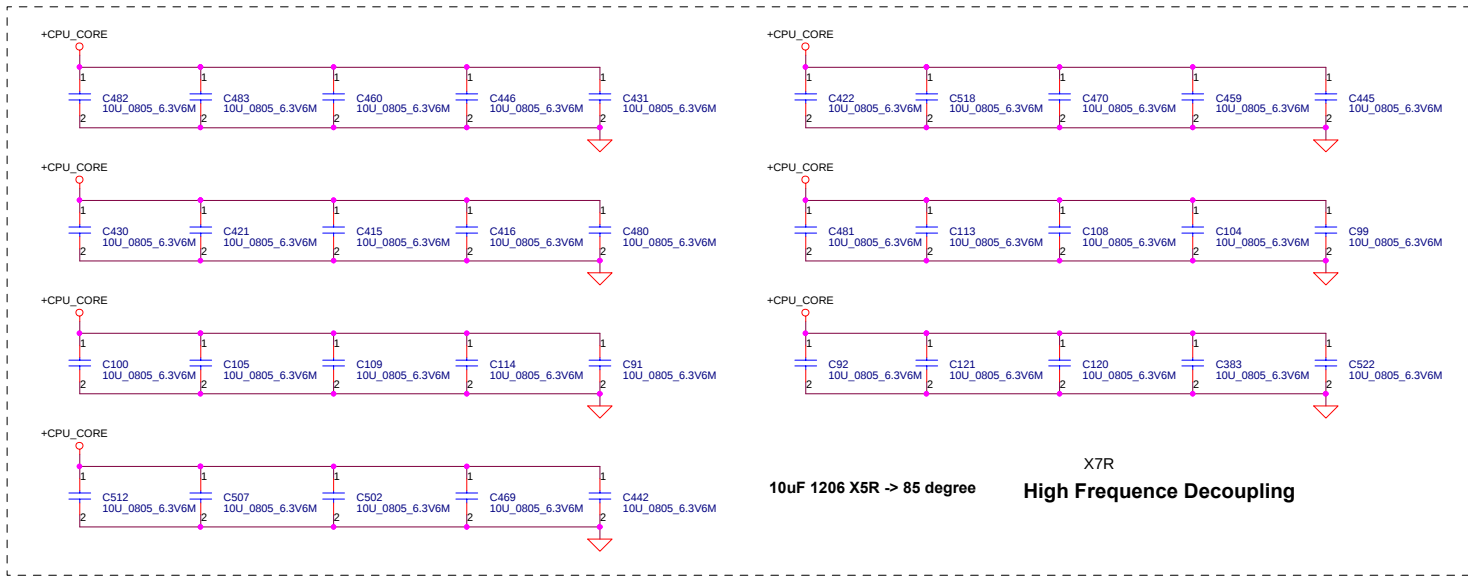


Dothan

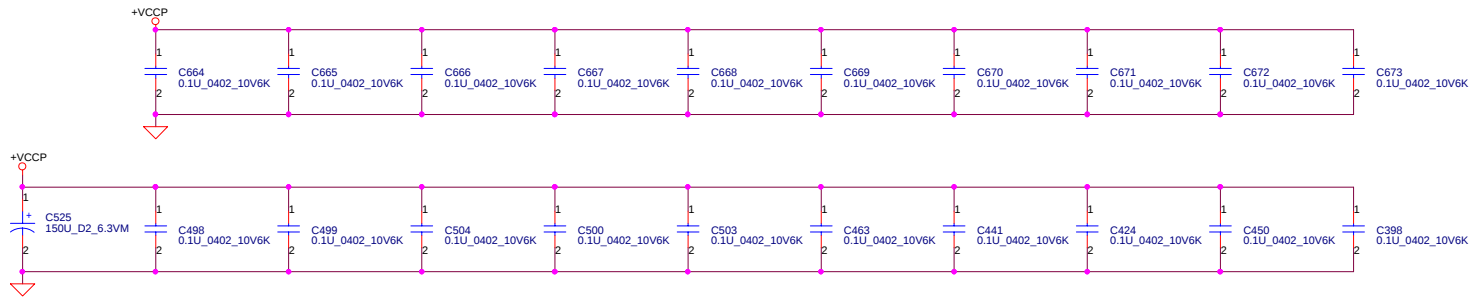
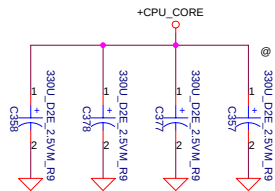
POWER, GROUND

TYCO_1612365-1_Dothan

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				CustomerLA-2362	1
				Date: Friday, March 11, 2005	Sheet 6 of 52



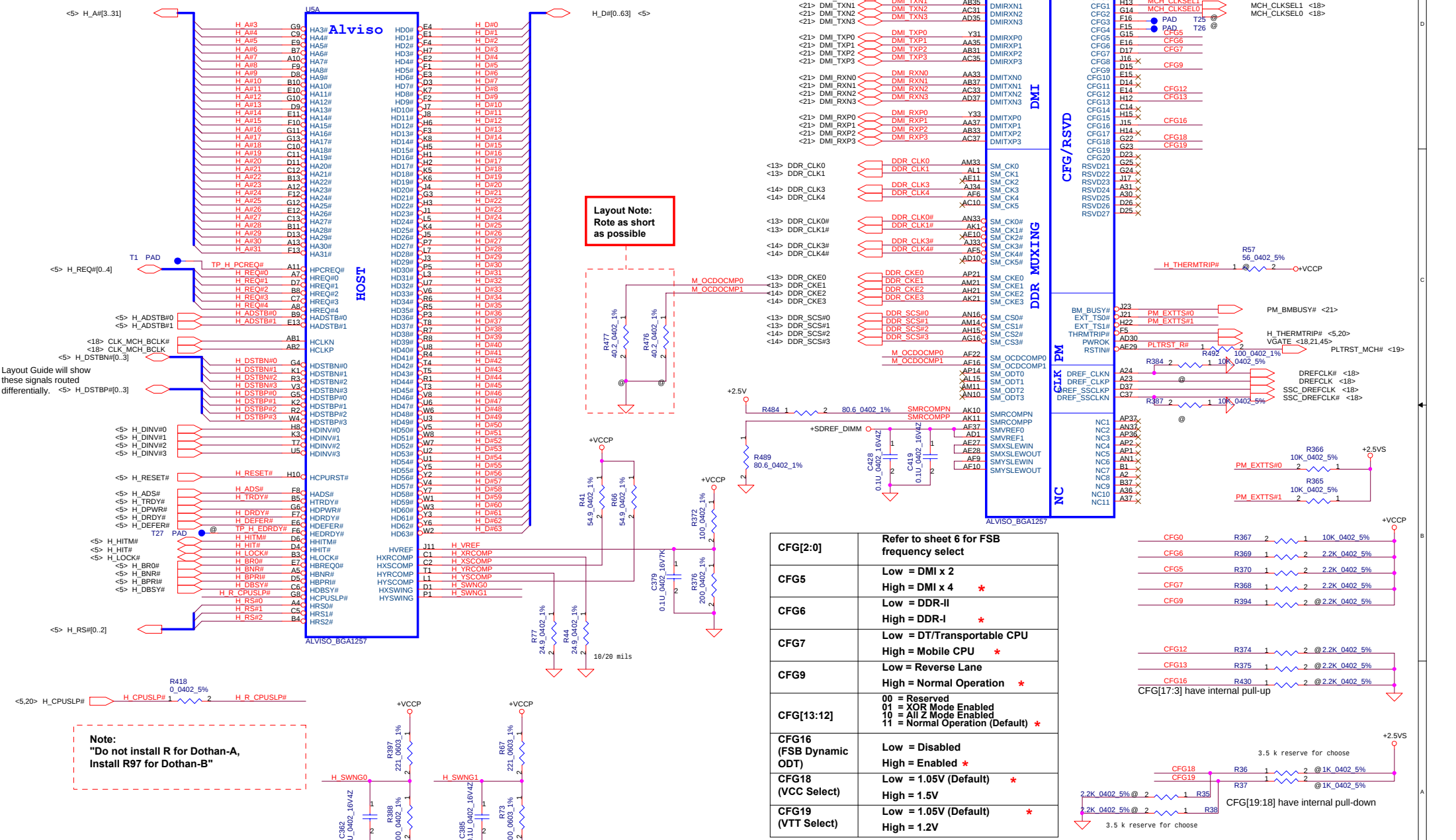
Near VCORE regulator.

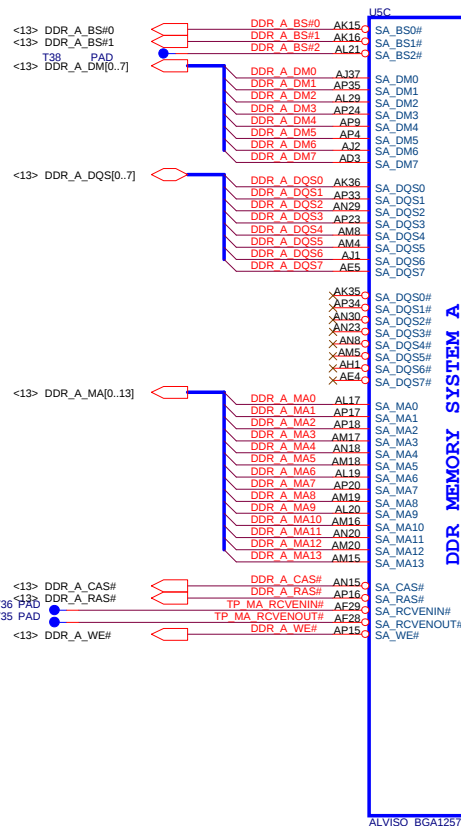


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						Rev		1	
Date:						Friday, March 11, 2005		Sheet 7 of 52	

Layout Guide will show these signals routed differentially.

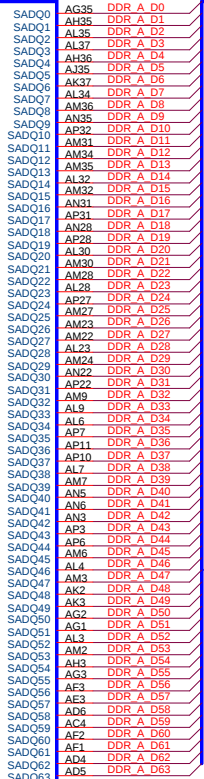
Alviso CFG[17:3] has internal pull-up



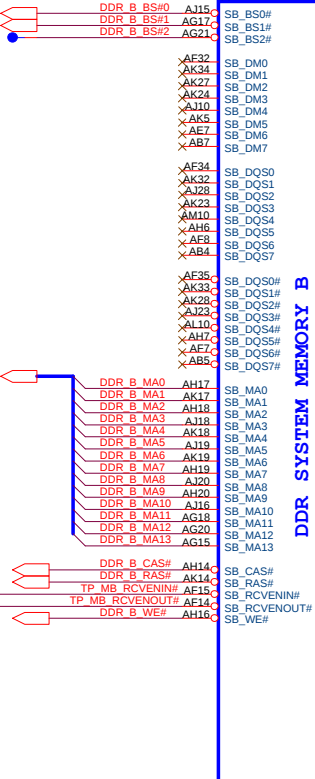
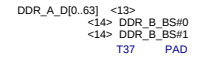


DDR MEMORY SYSTEM A

ALVISO_BGA1257

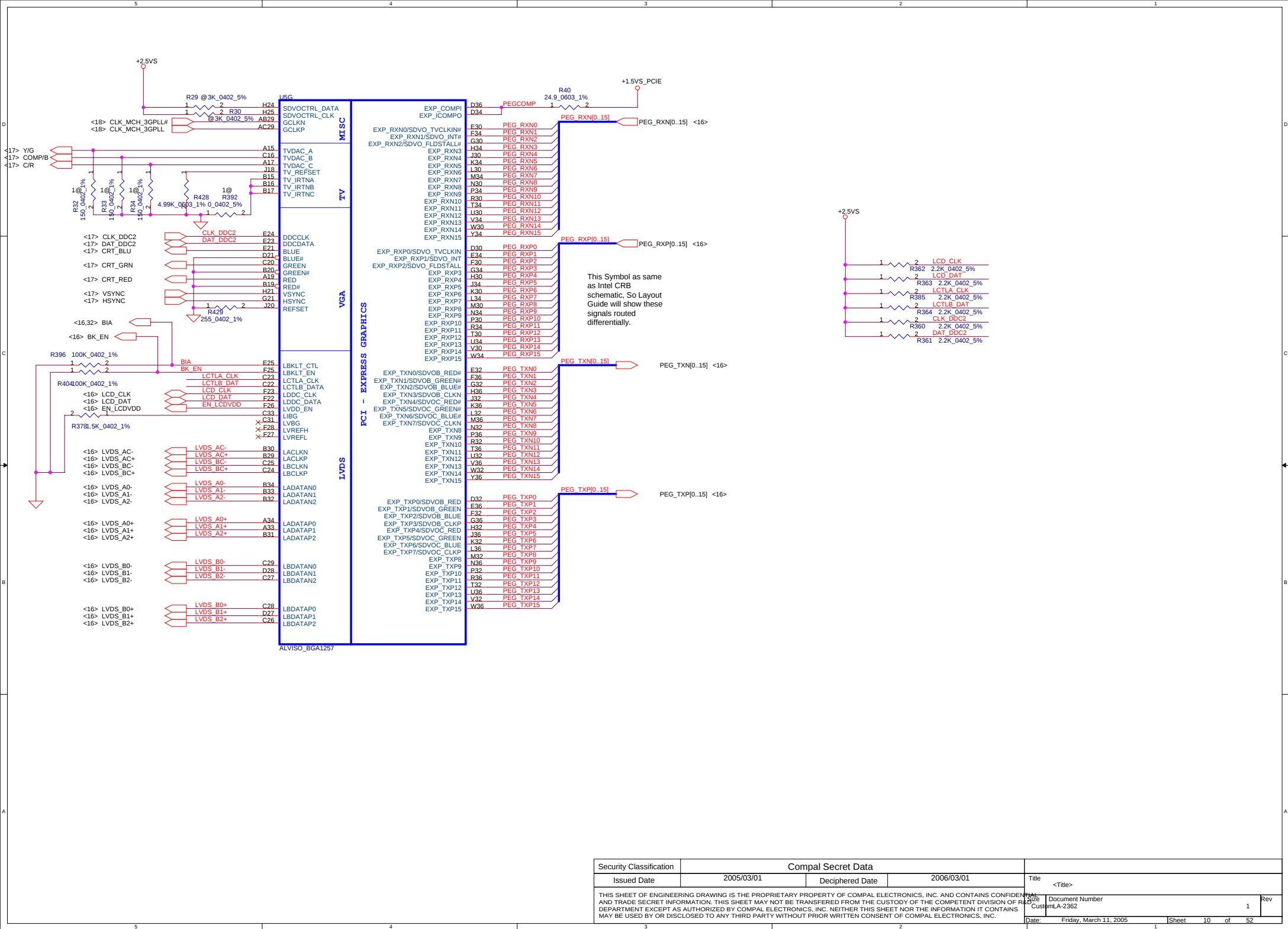


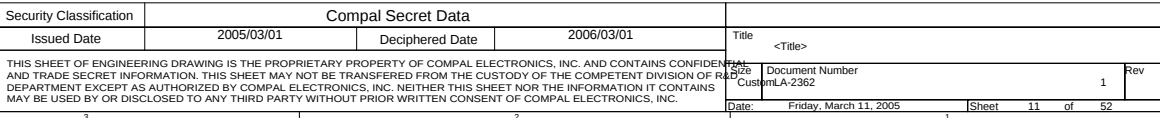
This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.

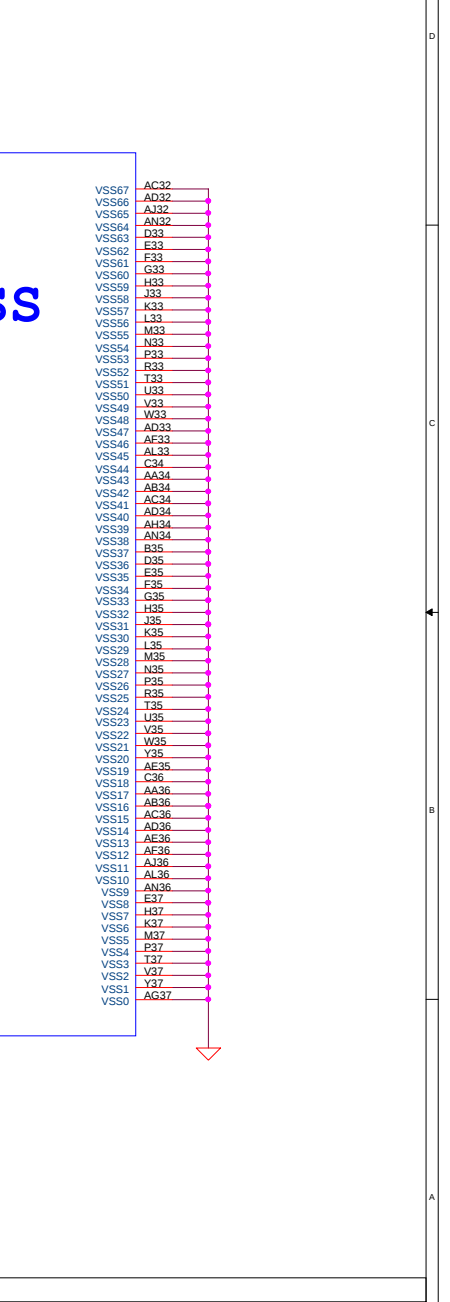
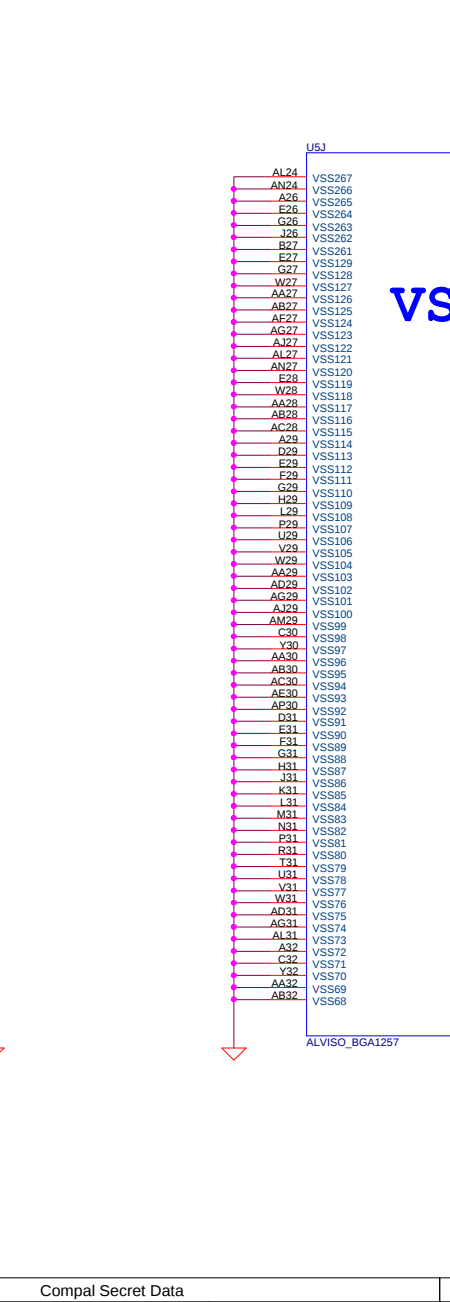
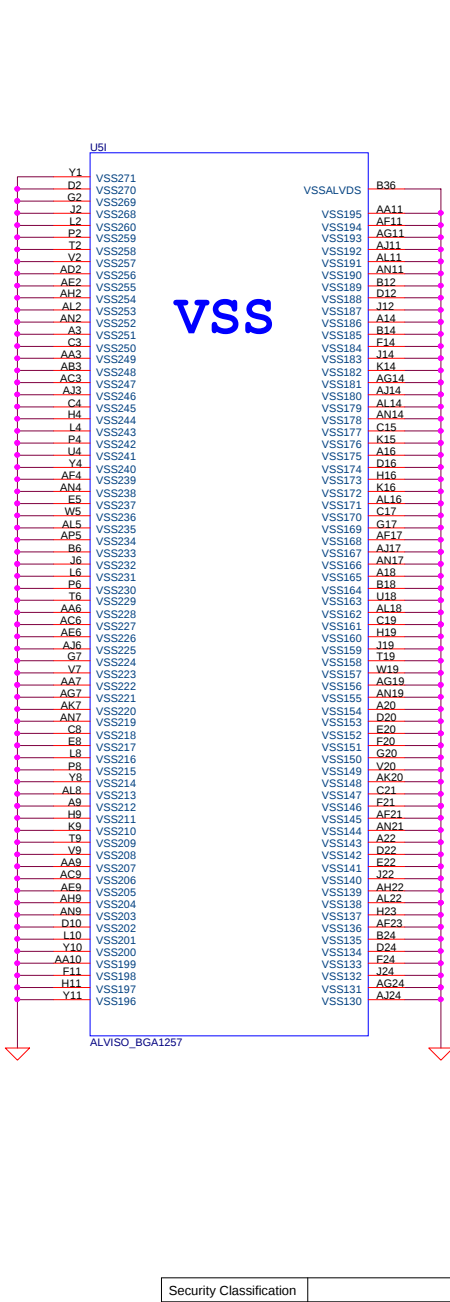
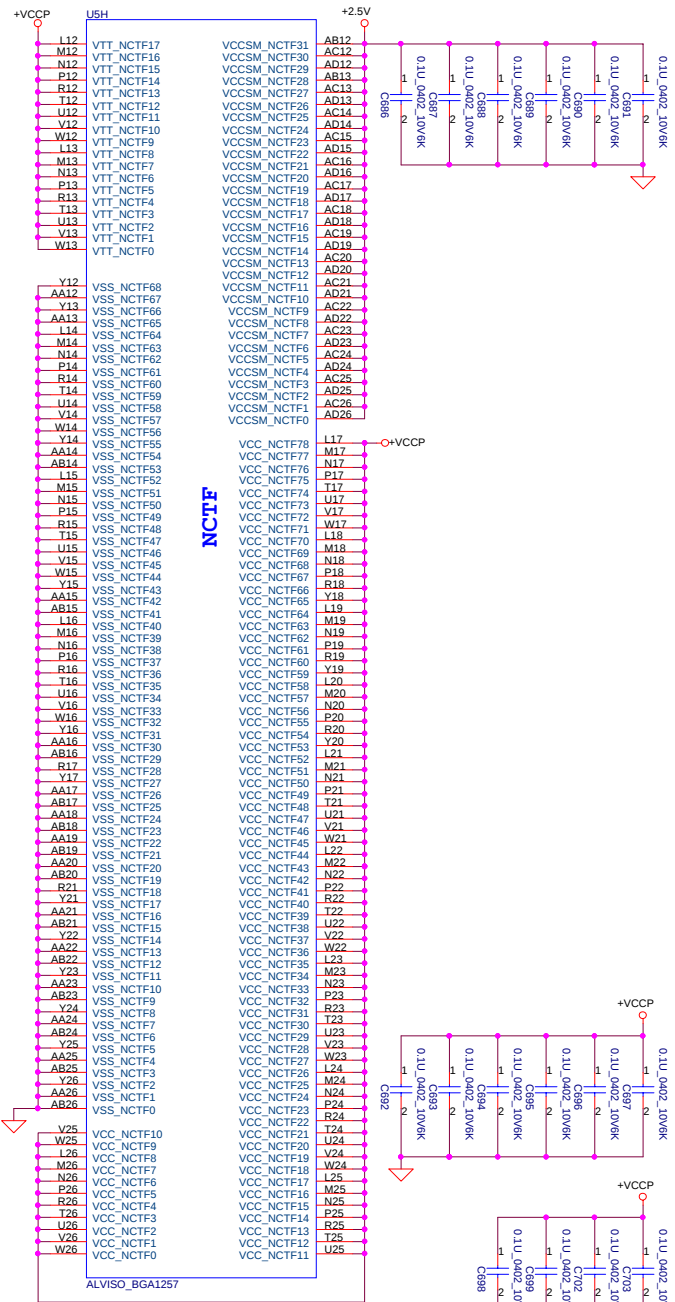


DDR MEMORY SYSTEM B

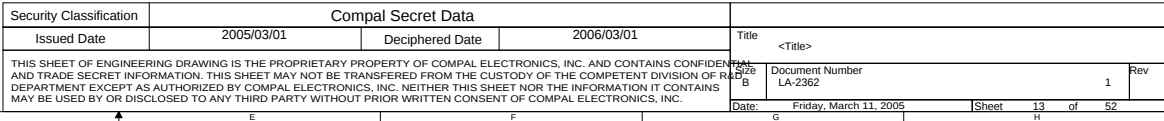
ALVISO_BGA1257

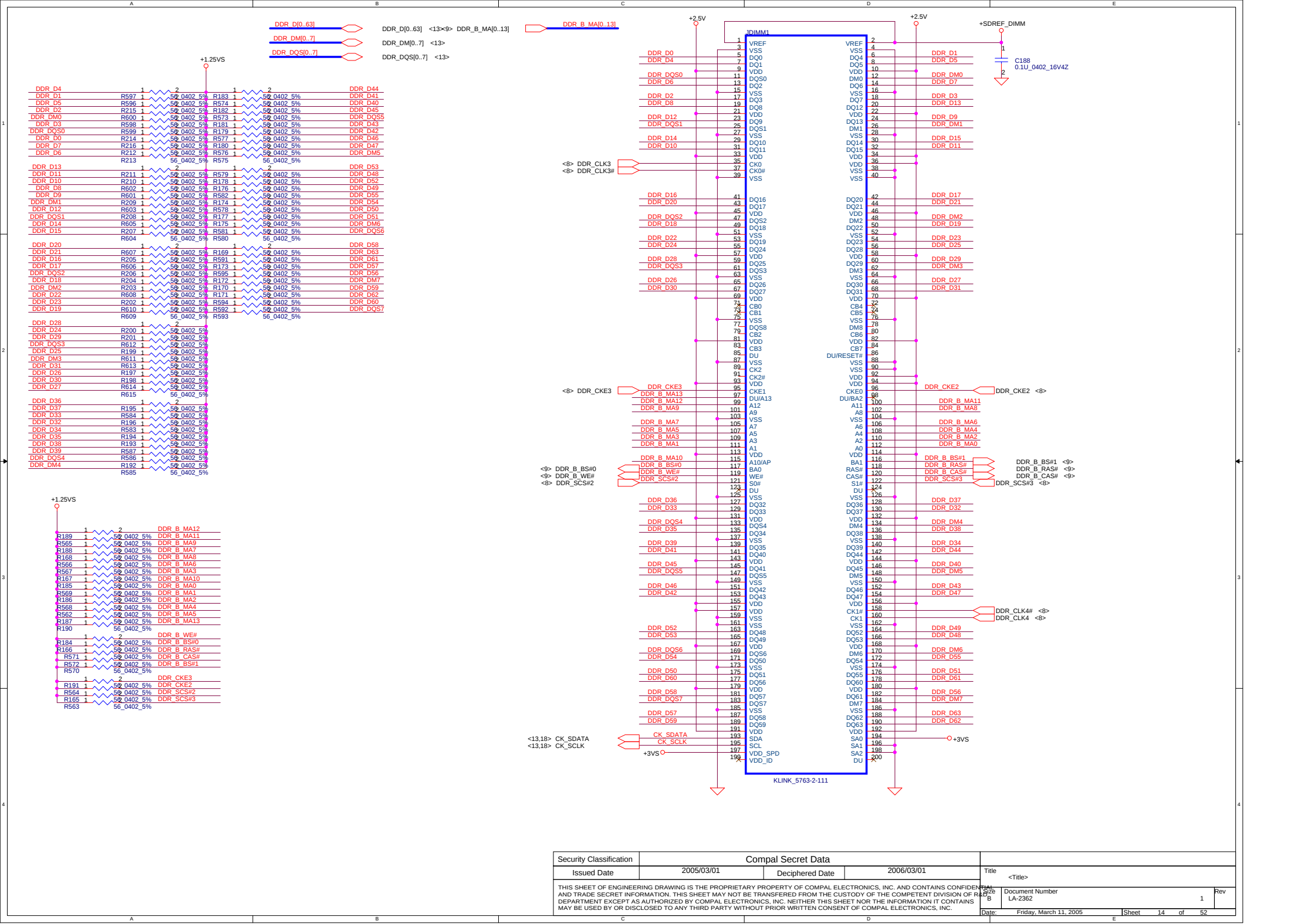






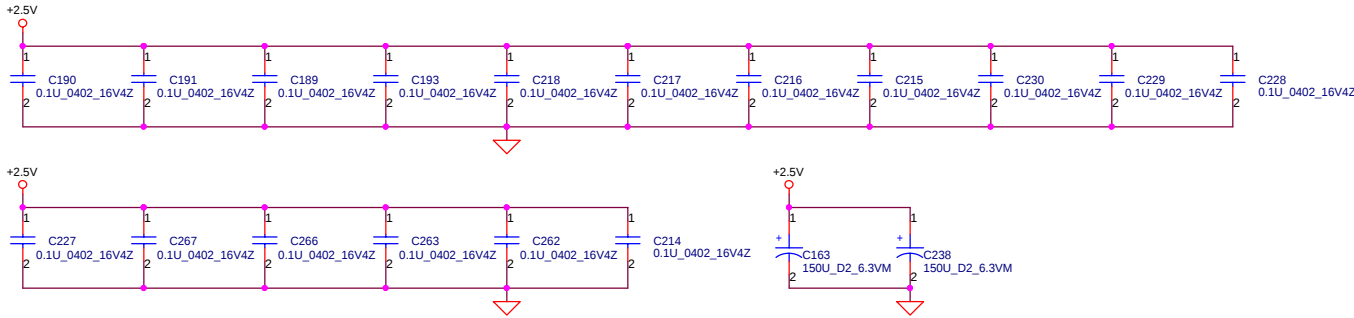
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Date:						Friday, March 11, 2005		Sheet 12 of 52	





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						1
				Date:	Friday, March 11, 2005	Sheet 14 of 52

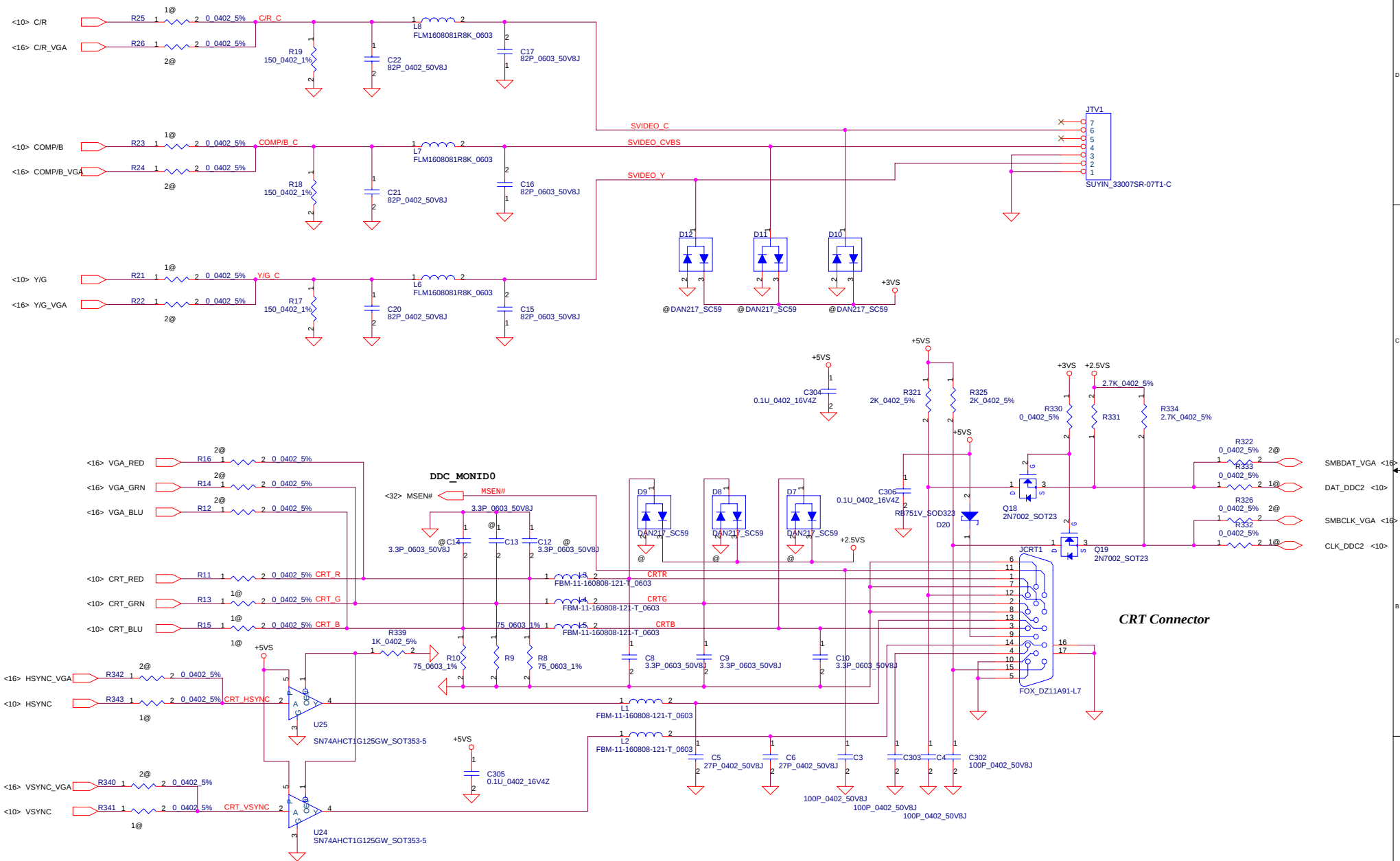
Layout note :
Distribute as close as possible
to DDR-SODIMM.



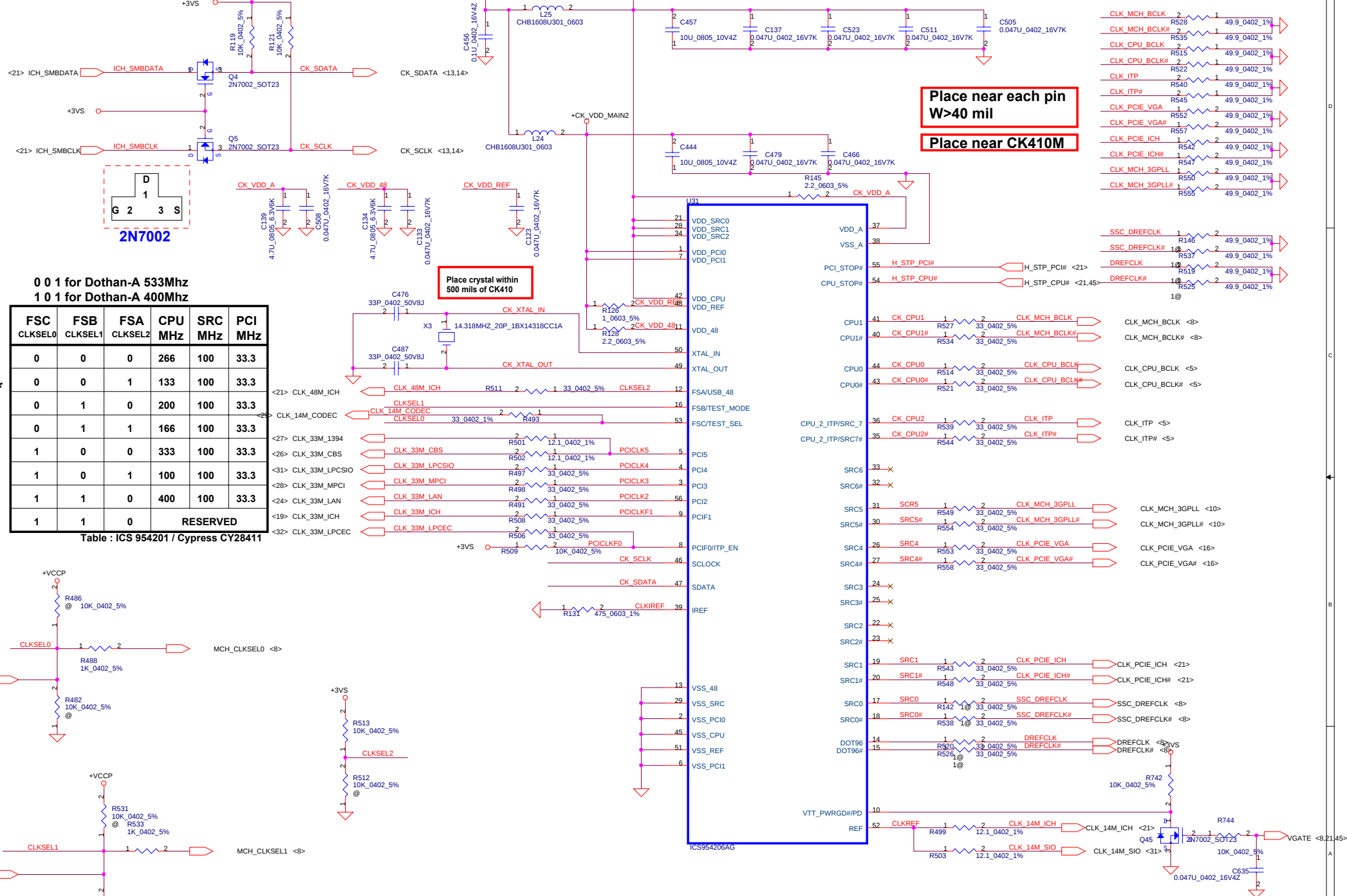
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



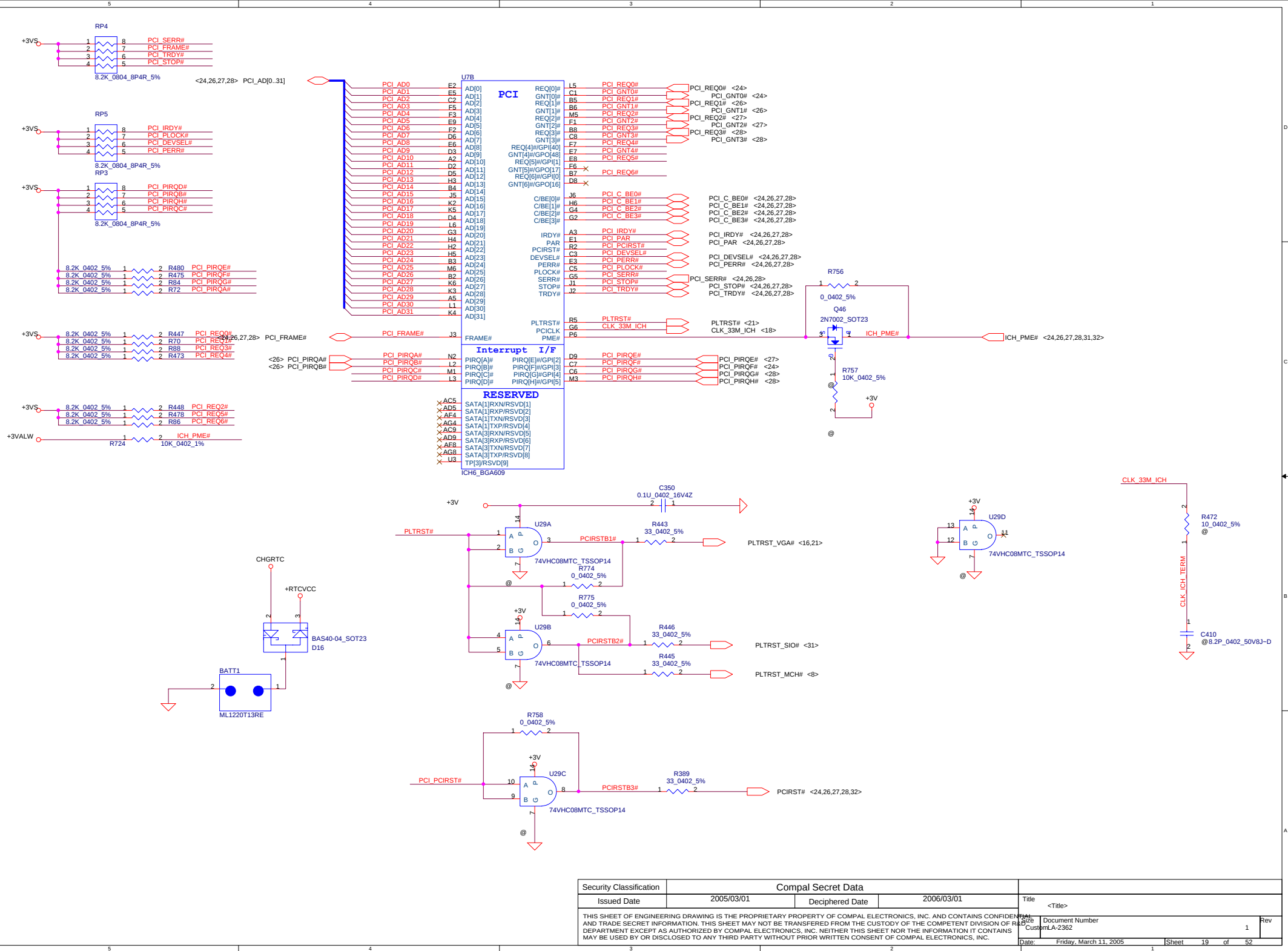
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						Customer		LA-2362									
						Date:		Friday, March 11, 2005				Sheet		15		of 52	



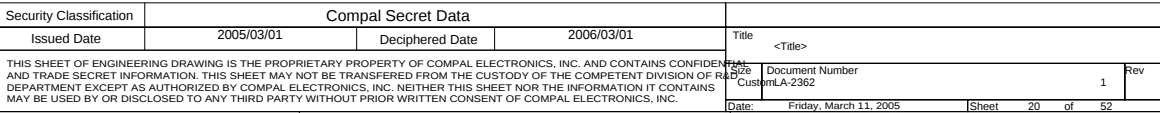
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Date: Friday, March 11, 2005				Sheet	17 of 52

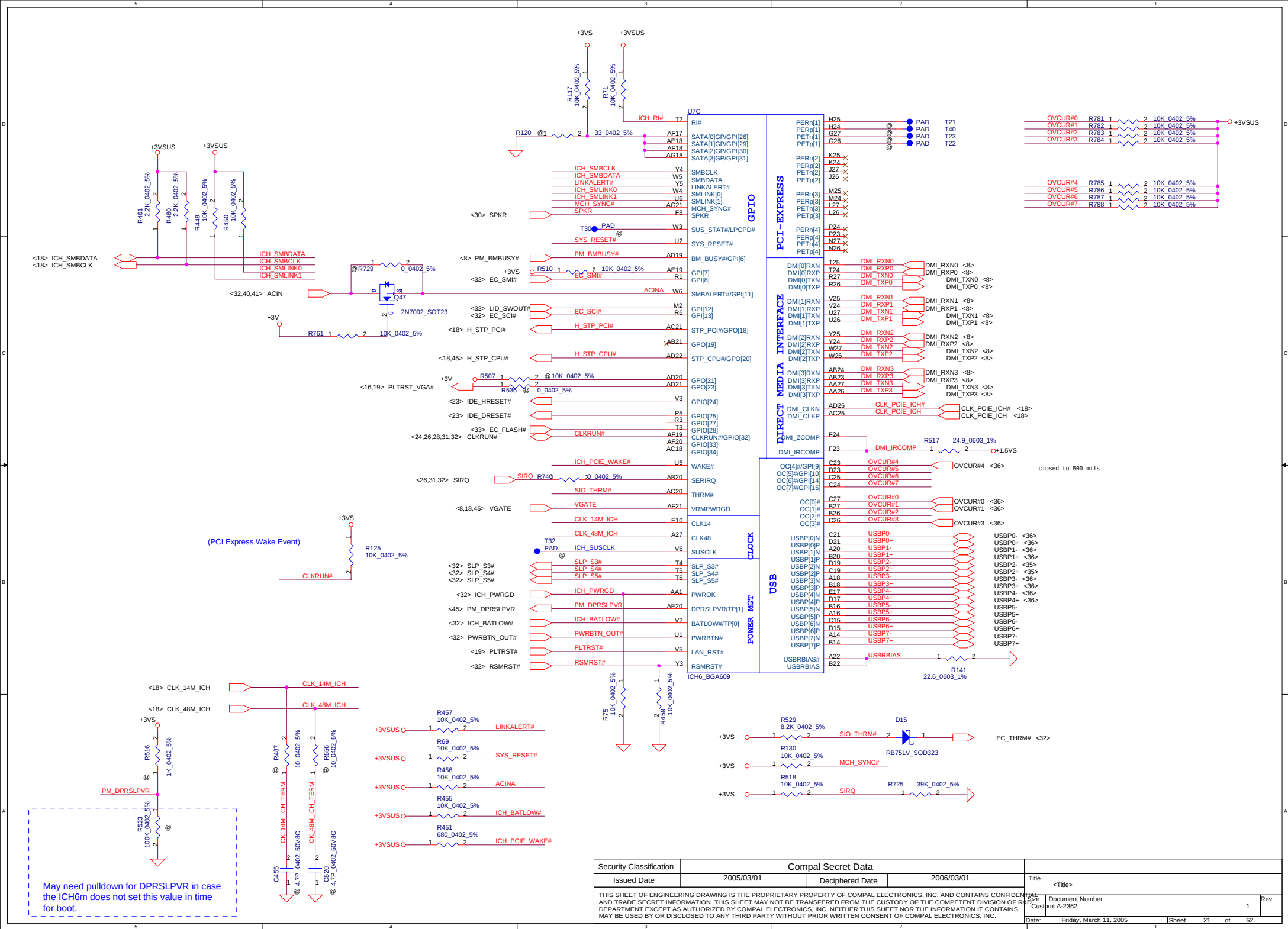


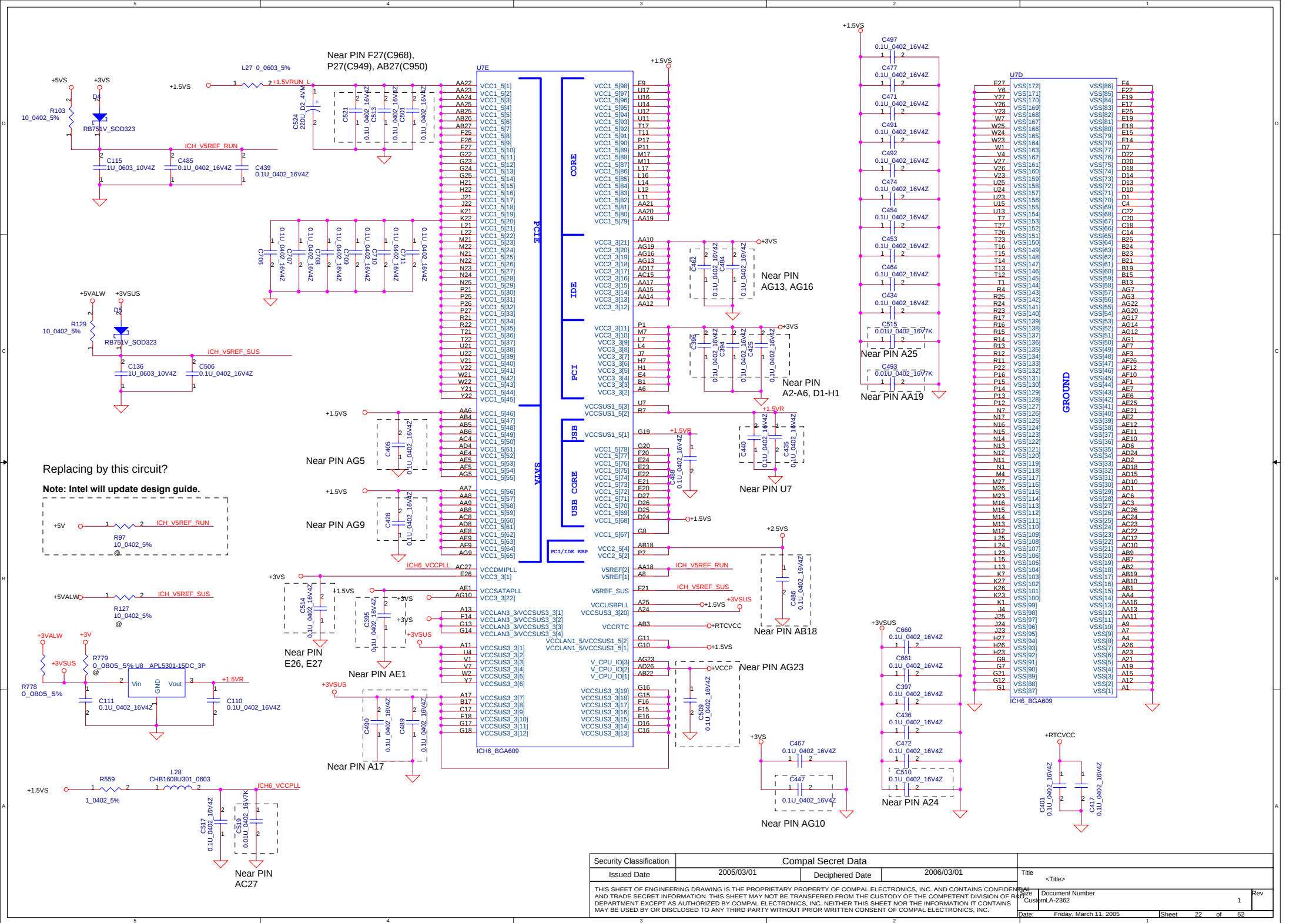
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Date:	Friday, March 11, 2005	Sheet	18	of 52

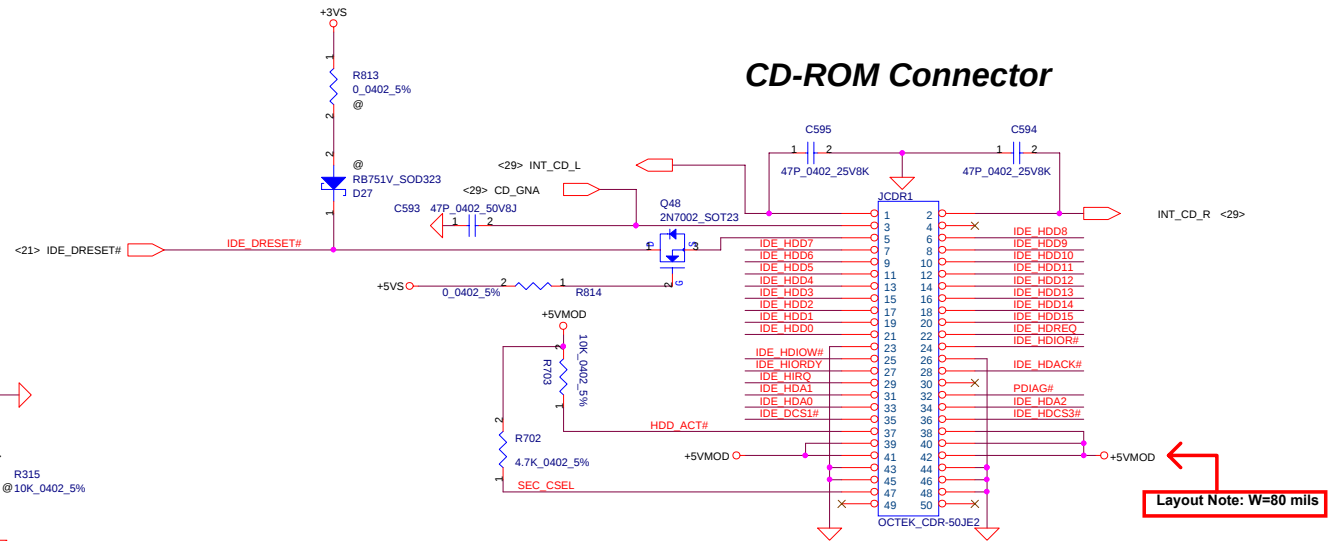
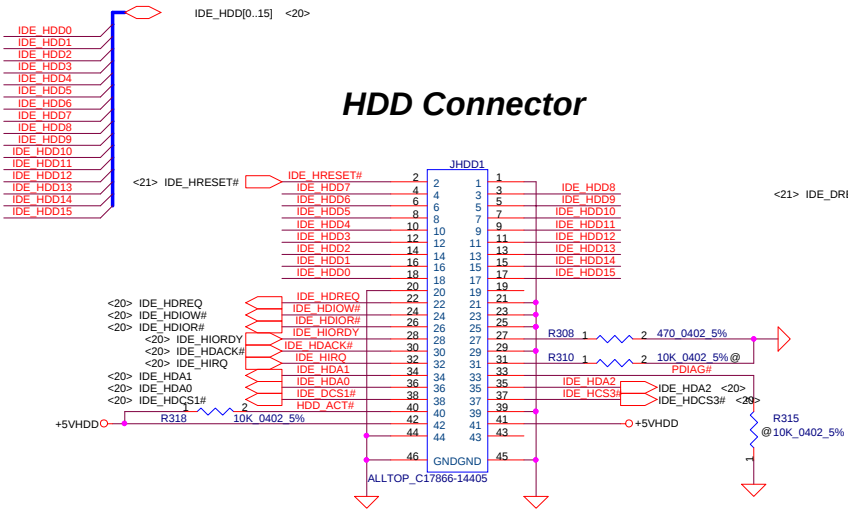


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				Sheet	19	of 52

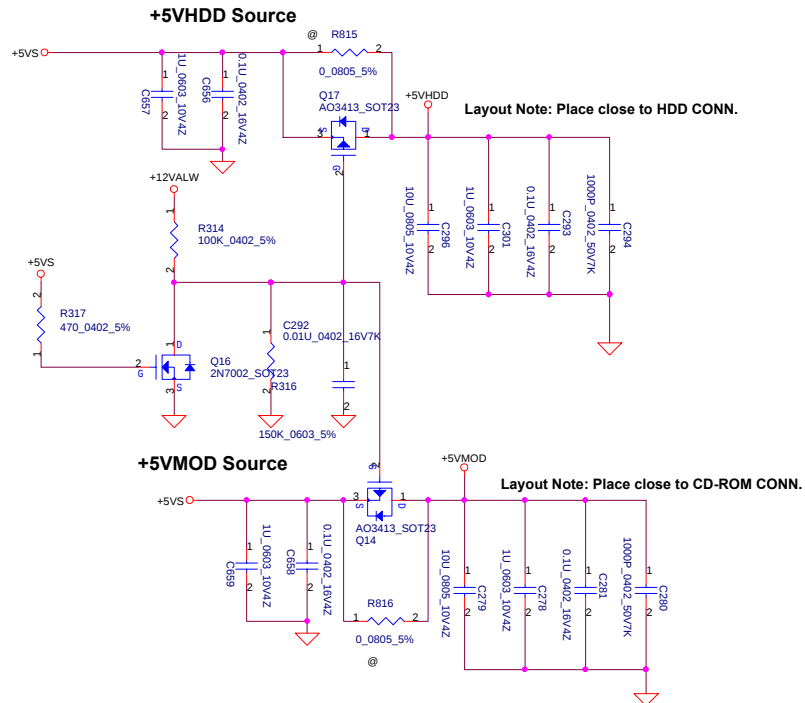




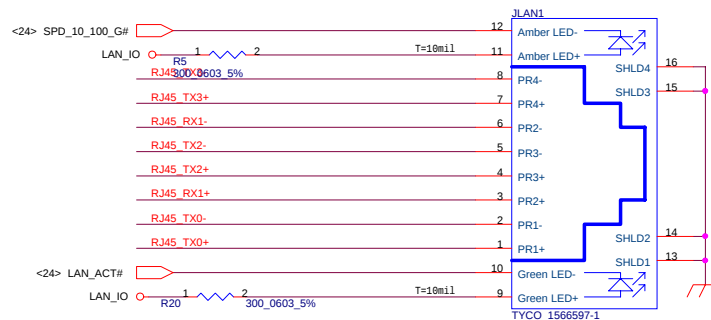
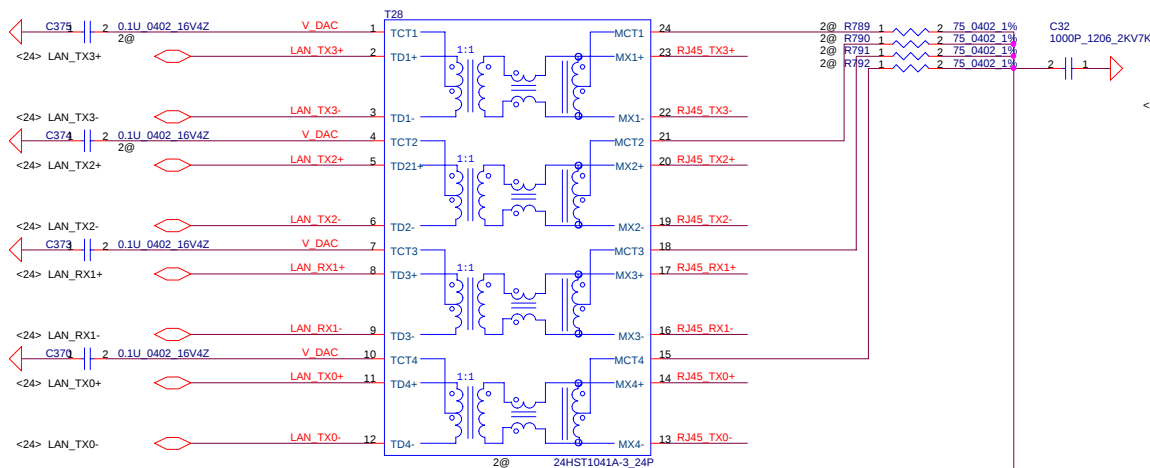




IRQ how to assign



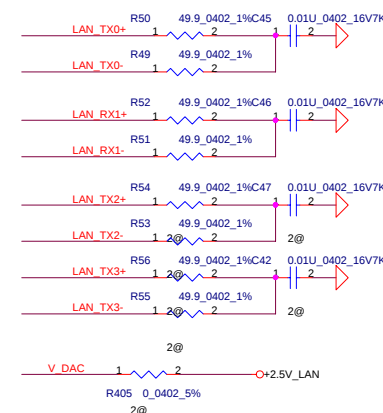
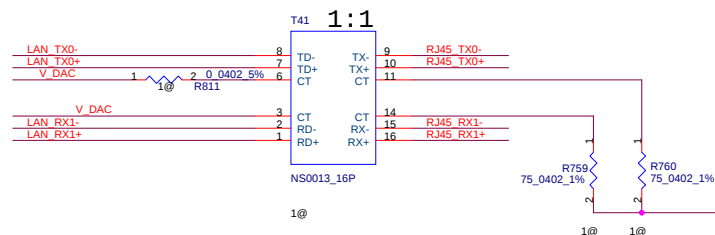
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					CustomerLA-2362	1			
				Date:	Friday, March 11, 2005	Sheet	23	of	52



RTL8110SBL used the 24HST1041A-3_24P
RTL8100CL used the 24ST0023-3_24P

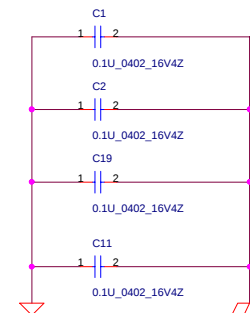
Layout Note
24HST1041A-3 pls close to conn.

Termination plane should be copied to chassis ground
and also depends on safety concern

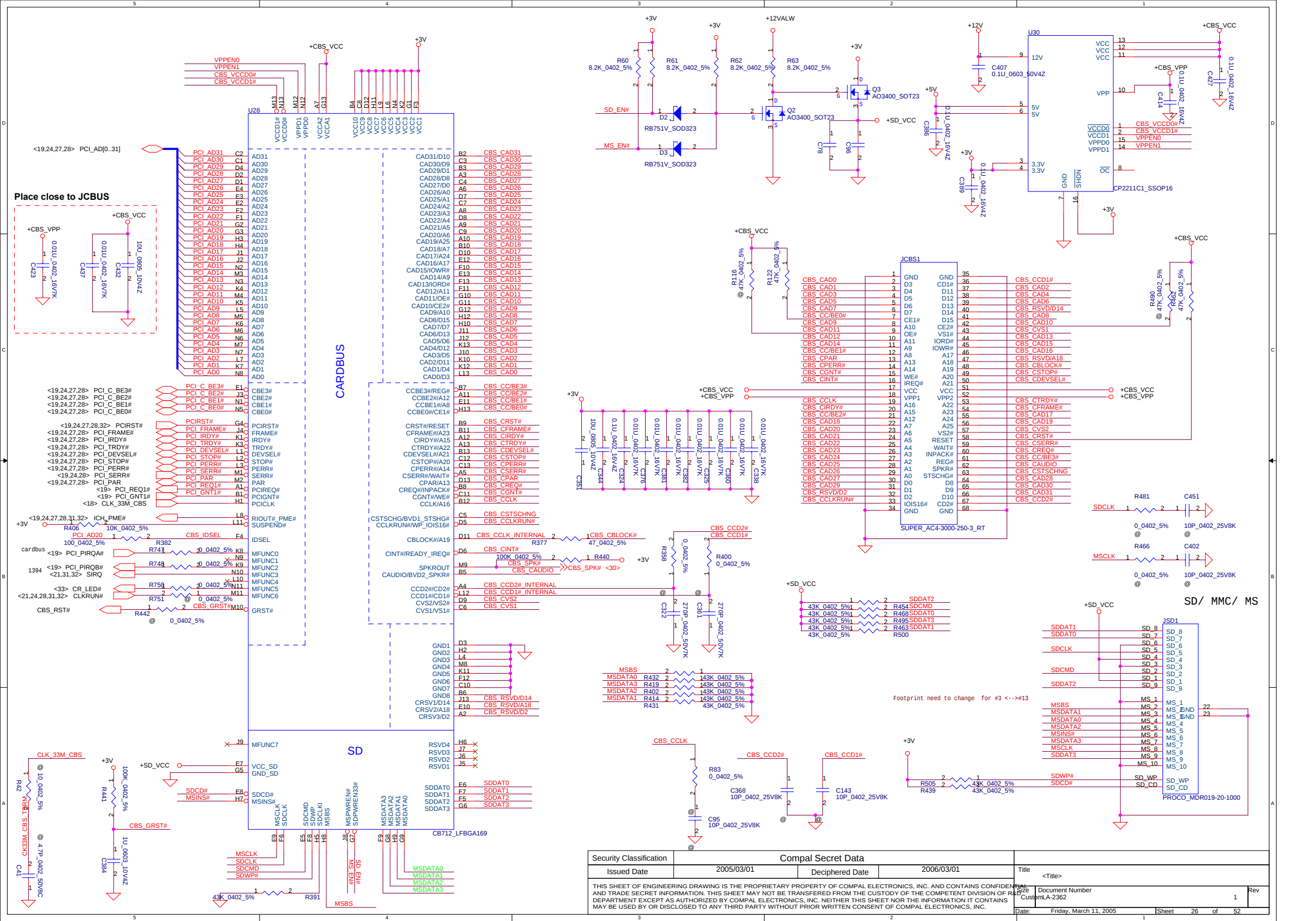


Termination plane should be copied
to chassis ground and also depends
on safety concern

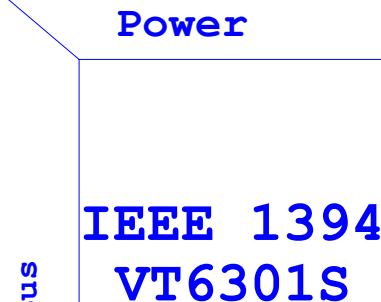
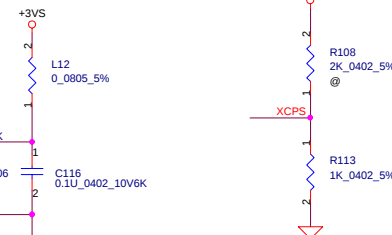
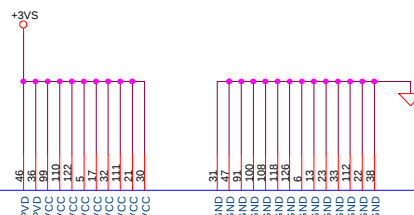
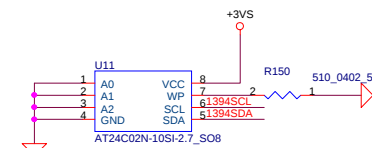
Please close to LAN IC

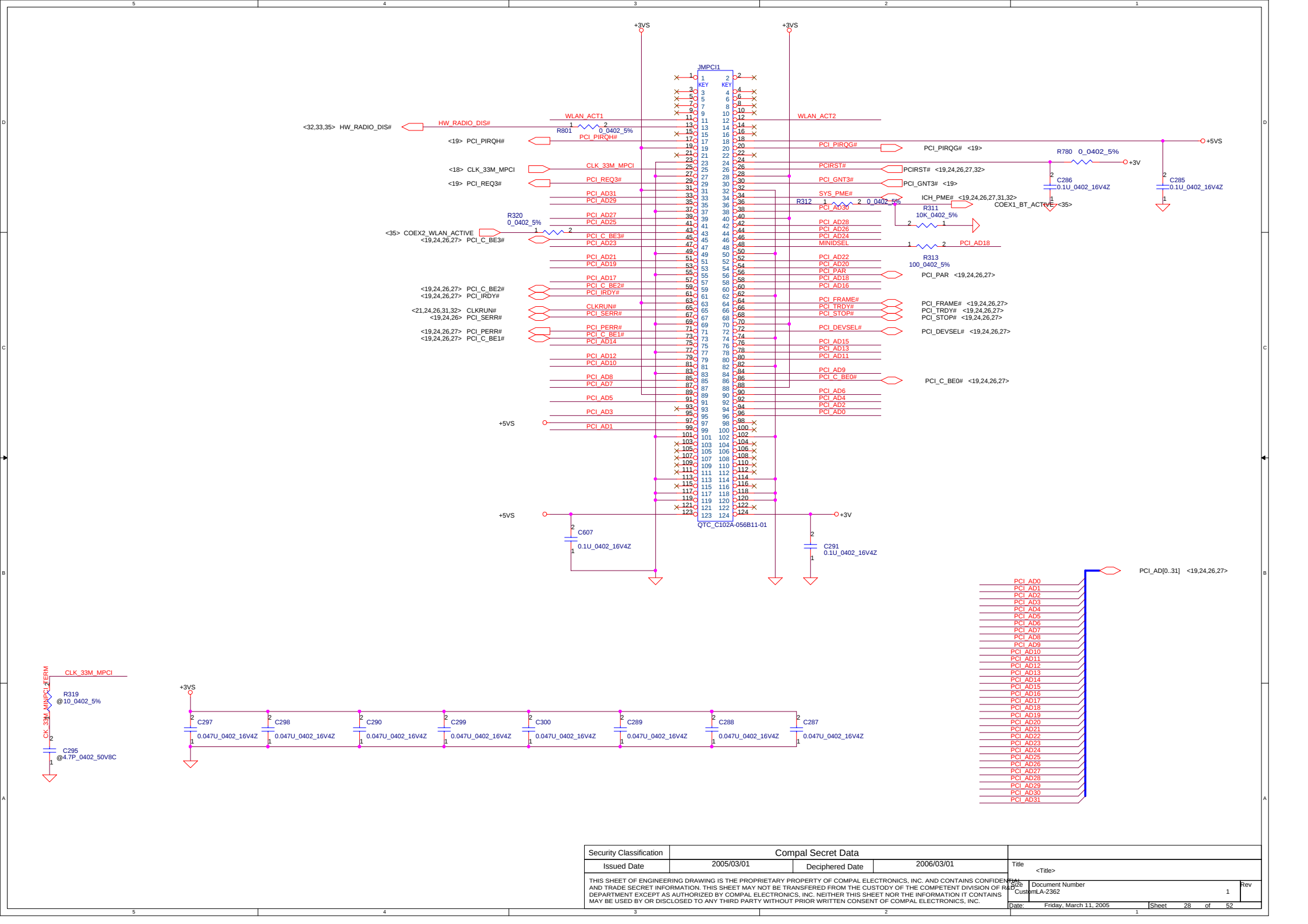


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Date:	Friday, March 11, 2005	Sheet	25 of 52	Rev 1



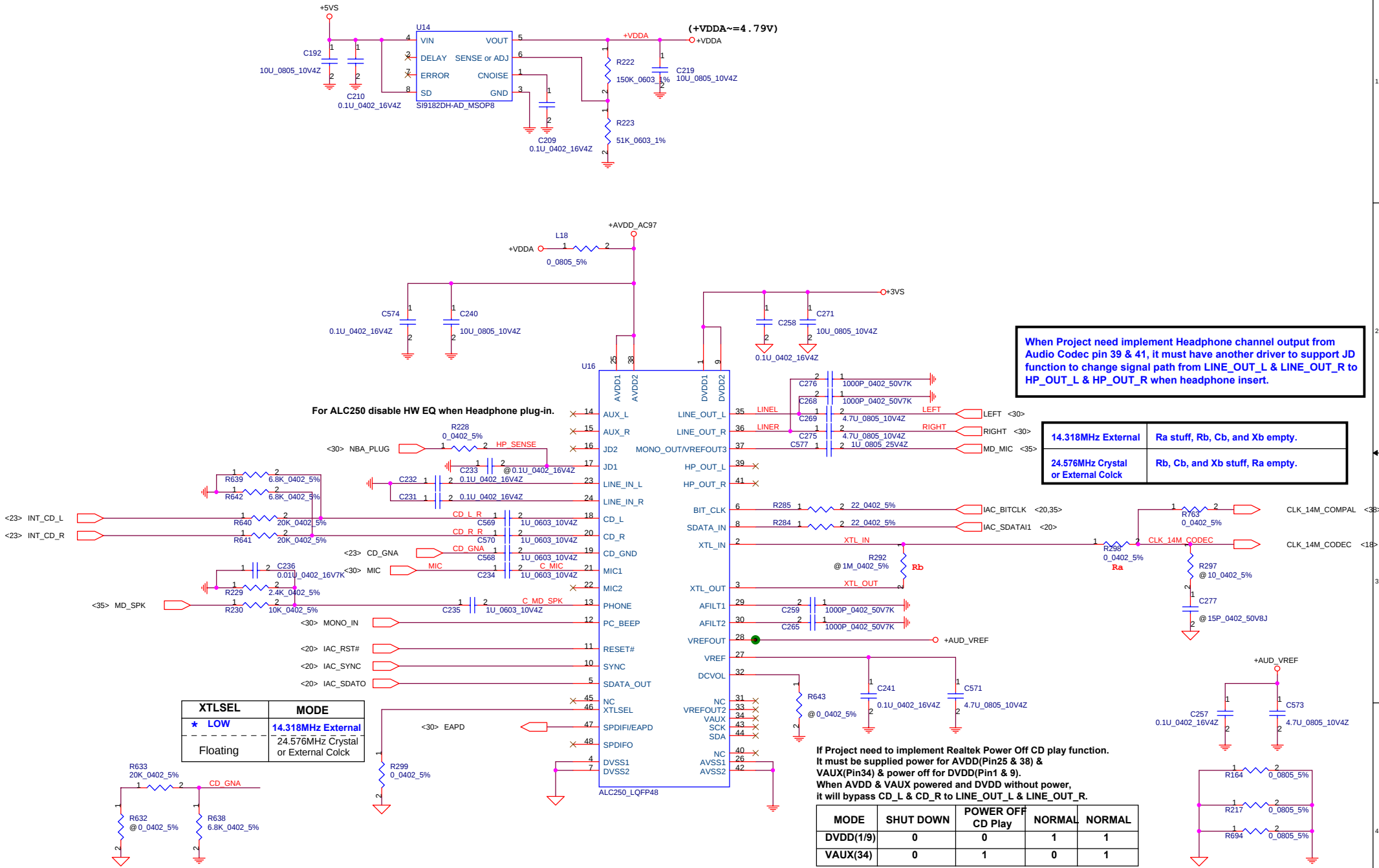
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Date		Friday, March 11, 2005	Sheet 26 of 52

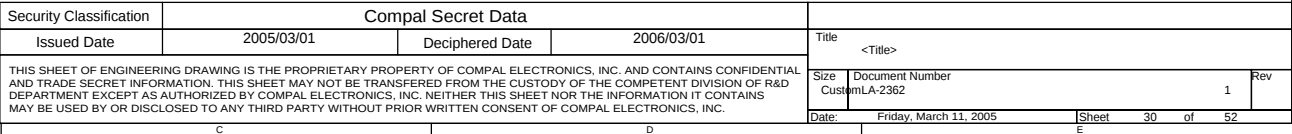




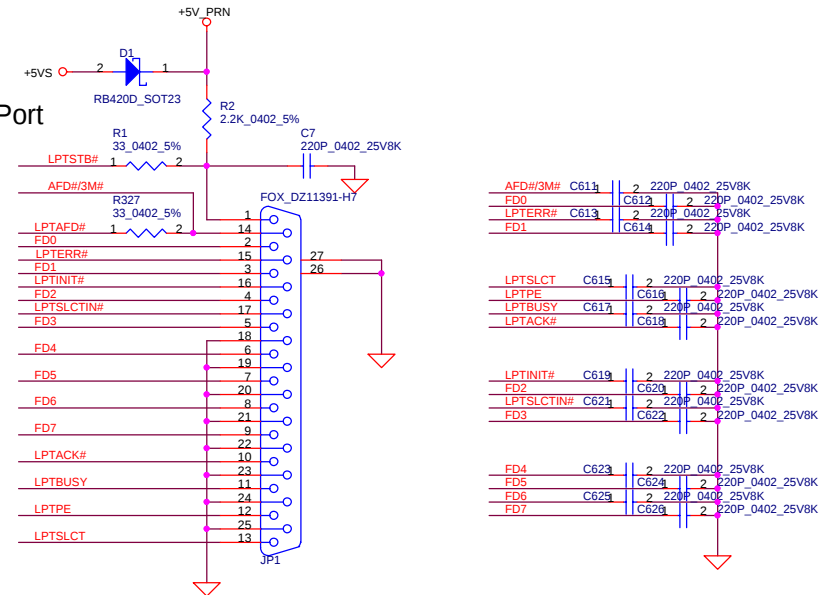
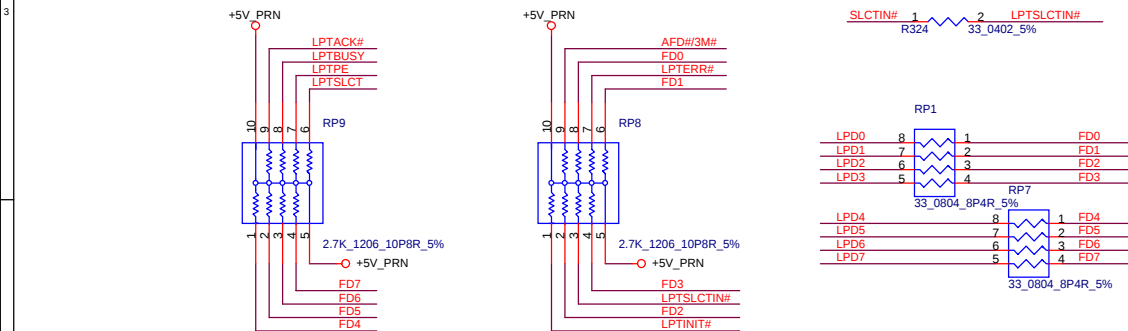
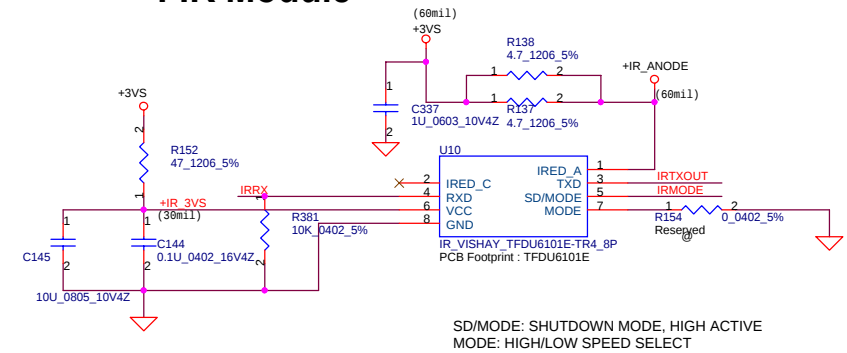
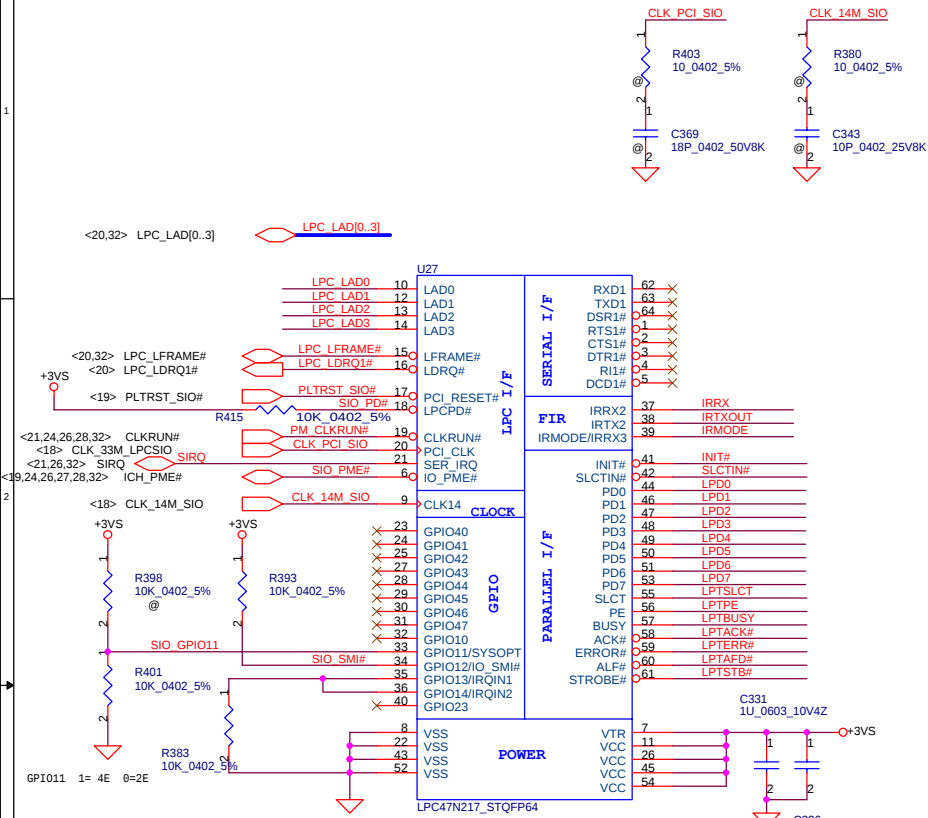
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				CustomLA-2362	1
Date: Friday, March 11, 2005				Sheet	28 of 52

AC97 Codec

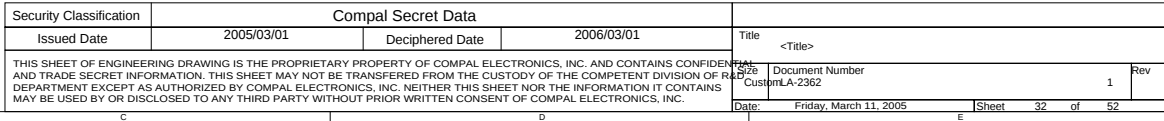


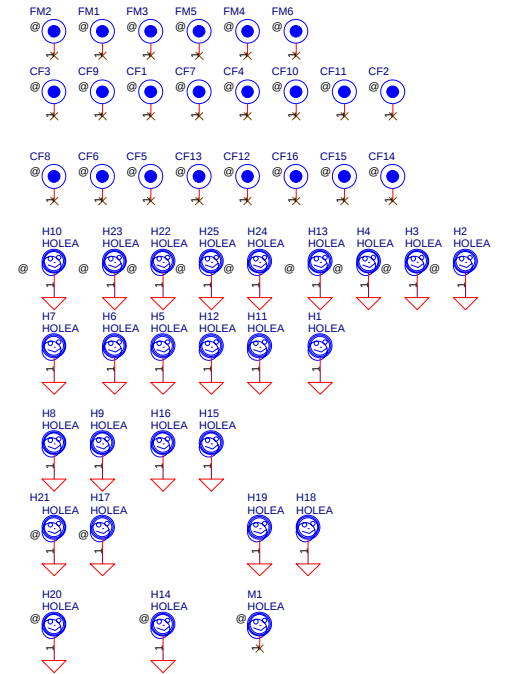
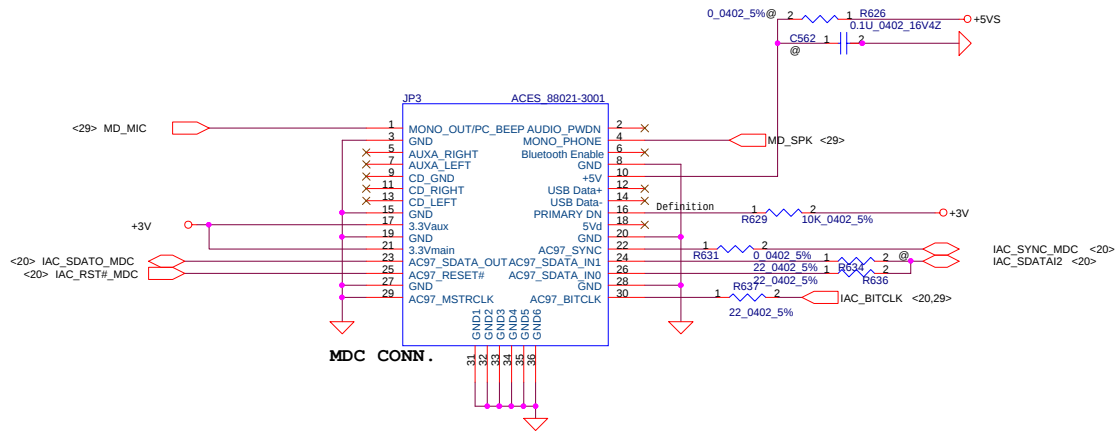
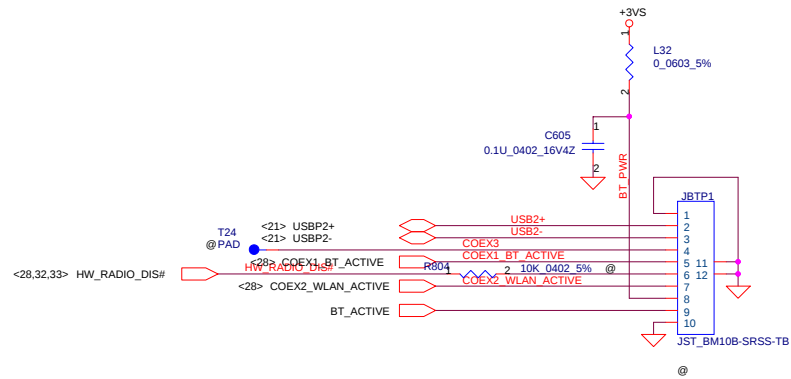


FIR Module

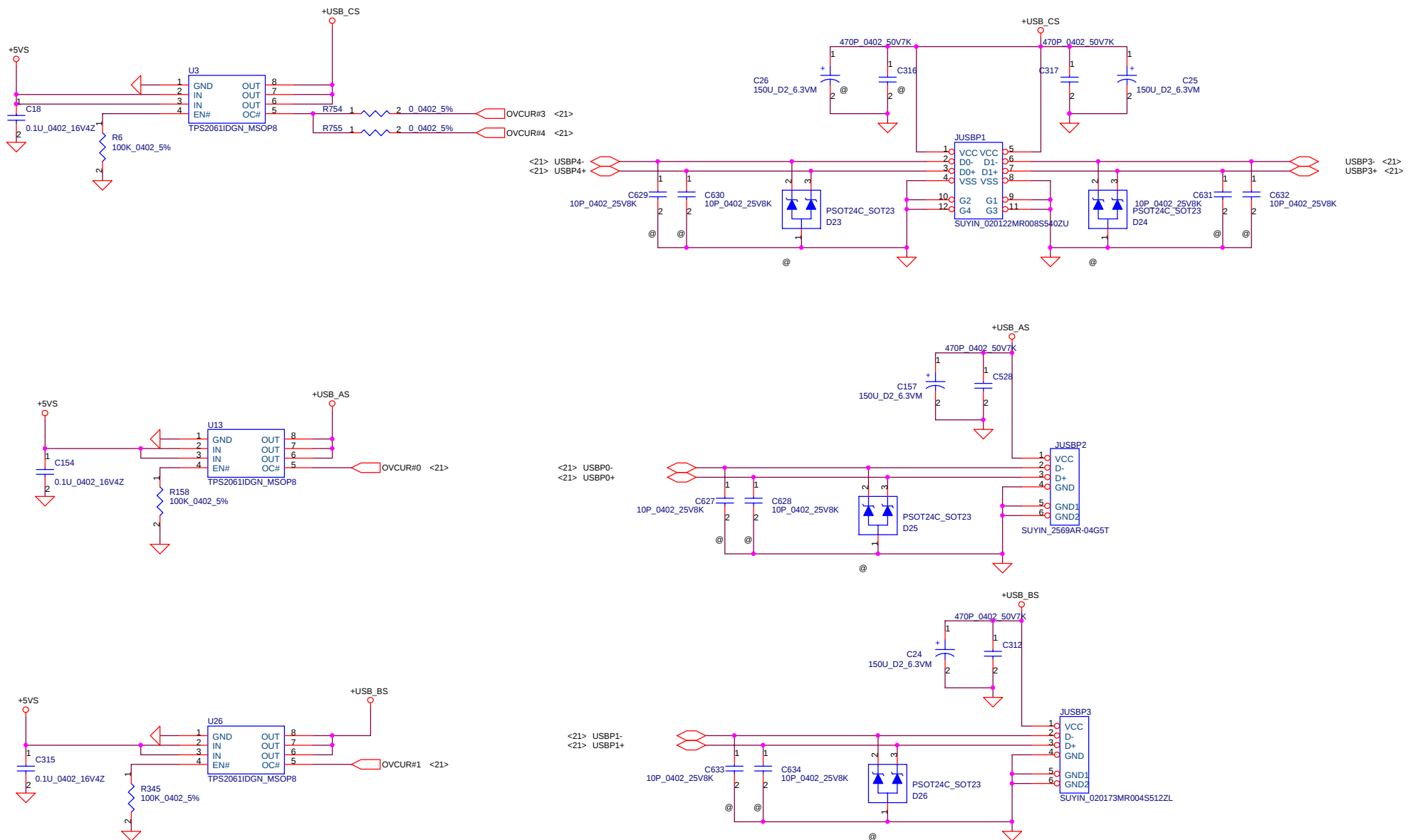


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					CustomLA-2362	1	
				Date:	Friday, March 11, 2005	Sheet 31 of 52	

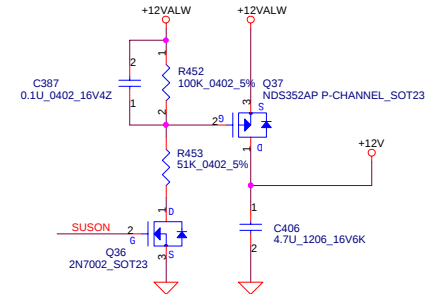
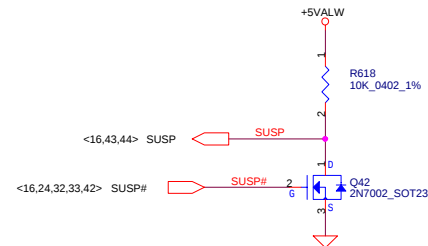
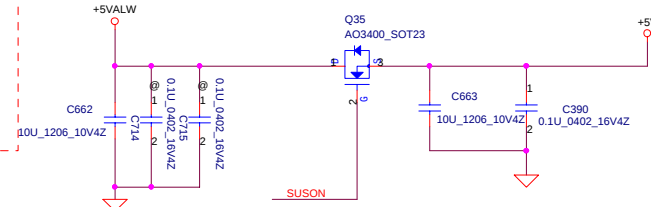
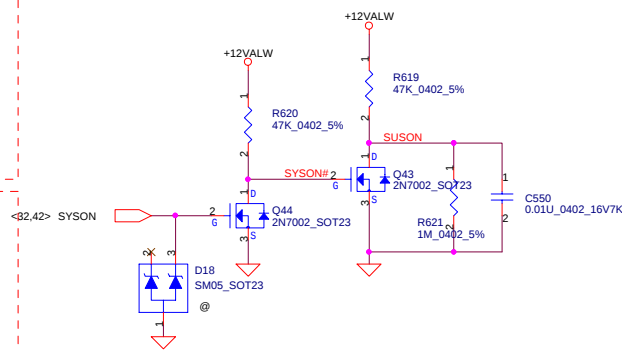
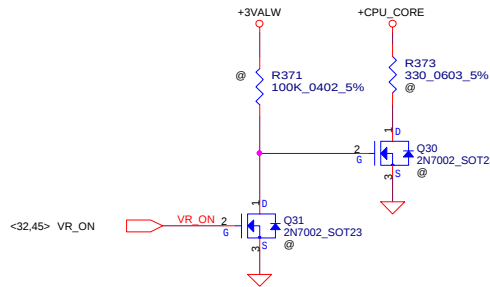
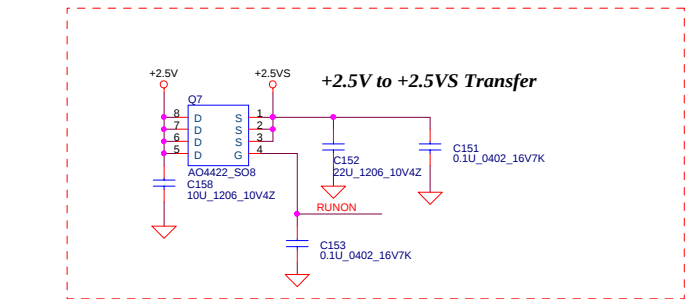
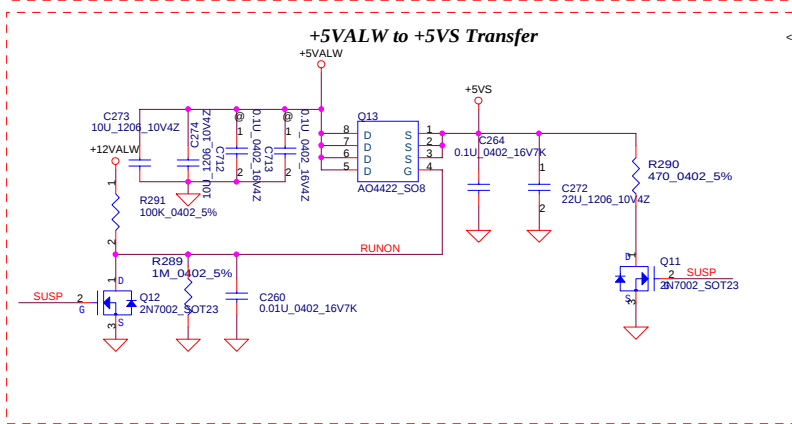
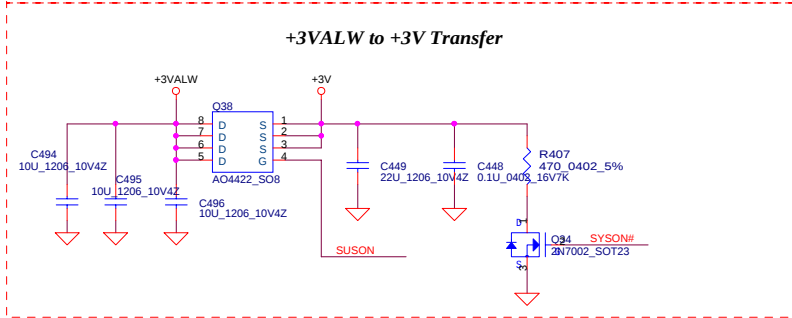
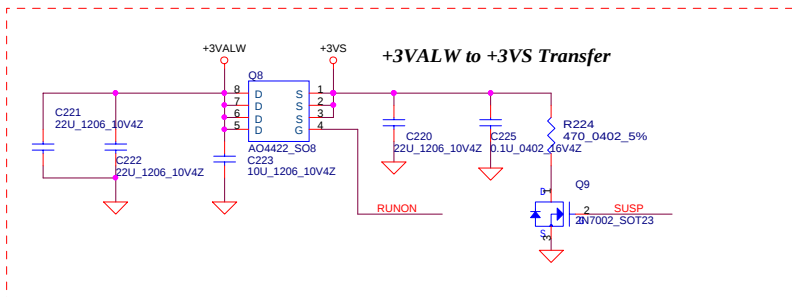




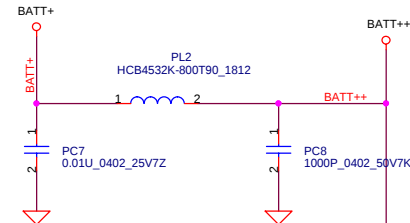
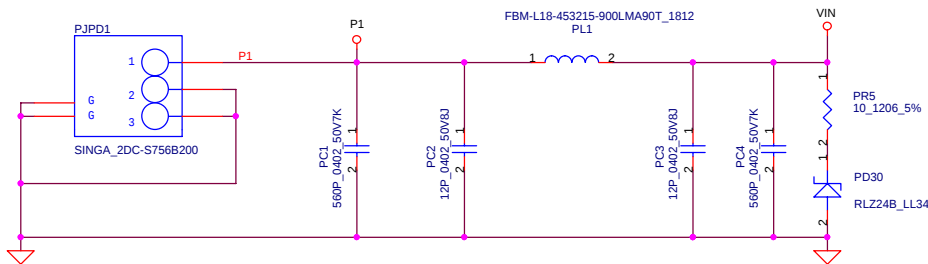
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						Document Number CustomLA-2362		Rev 1	
Date:						Friday, March 11, 2005		Sheet 35 of 52	



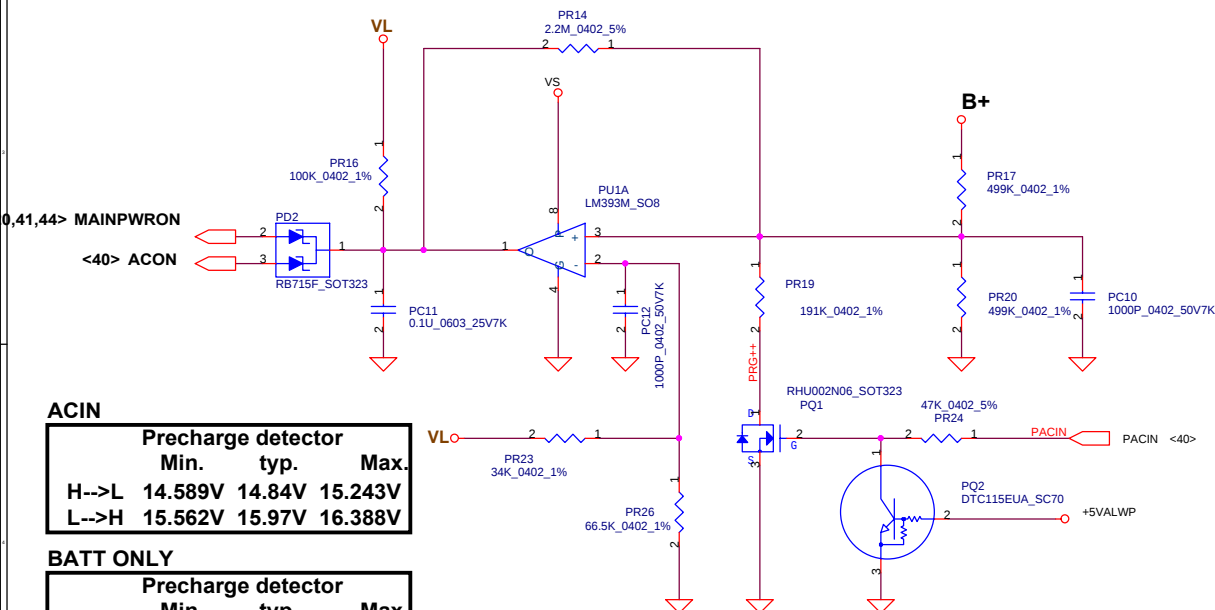
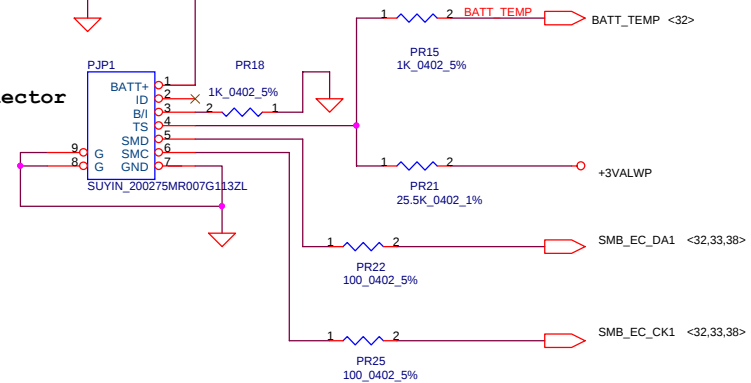
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								Cust		mLA-2362					
Date:		Friday, March 11, 2005				Sheet		36		of		52			



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Issued Date	2005/03/01	Deciphered Date	2006/03/01	<Title>	
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				CustomLA-2362	1
Date:				Friday, March 11, 2005	Sheet 37 of 52



PJPB1 battery connector
SMART
Battery:
1.BAT+
2.ID
3.B/I
4.TS
5.SMD
6.SMC
7.GND



ACIN

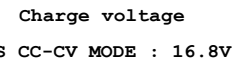
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Compal Electronics, Inc.			
Title	DCIN & DETECTOR & Precharge		
Size	Document Number	Rev	
B	LA-2362	1	
Date:	Friday, March 11, 2005	Sheet	39 of 52



2P4S:4300mAH/cell
0.7C=3.0A

OVP voltage :

LI-3S :17.8V---BATT-OVP=1.9758V

$$\text{BATT-OVP}=0.111*\text{BATT}+$$

Compal Electronics, Inc.

Charger

Size B	Document Number LA-2362
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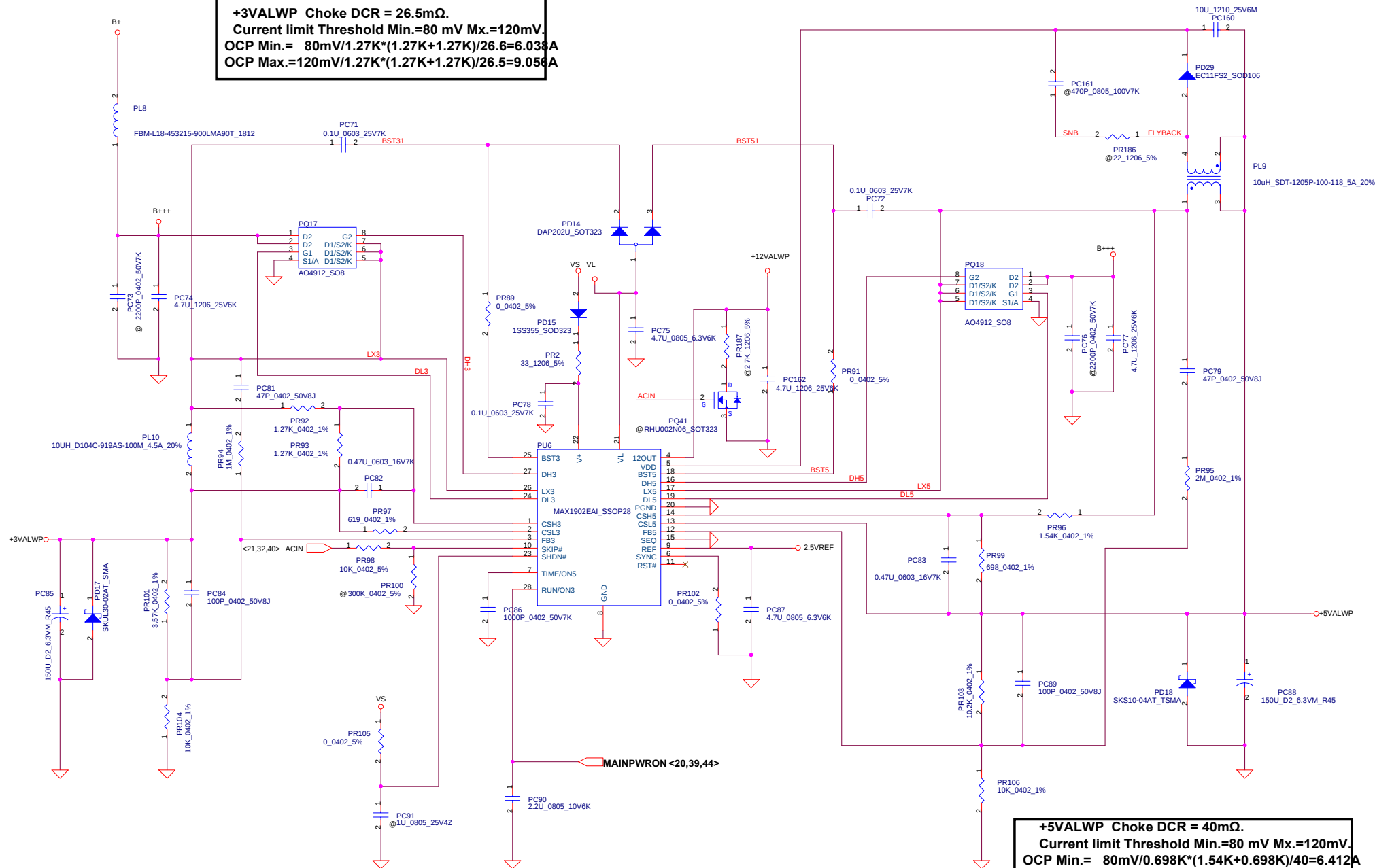
Rev	
1	

Date: Friday, March 11, 2005

Sheet 40 of 52

+3.3V/+5V/+12V

+3VALWP Choke DCR = 26.5mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/1.27K*(1.27K+1.27K)/26.6=6.03A
OCP Max.=120mV/1.27K*(1.27K+1.27K)/26.5=9.05A



$$RS2(PR64)=RS1(PR58)*RS3(PR61)/(RS1+RS3)$$

$$L/RL(DCR)=RS1*RS3(PR61)/(RS1+RS3)*Cs(PC56)$$

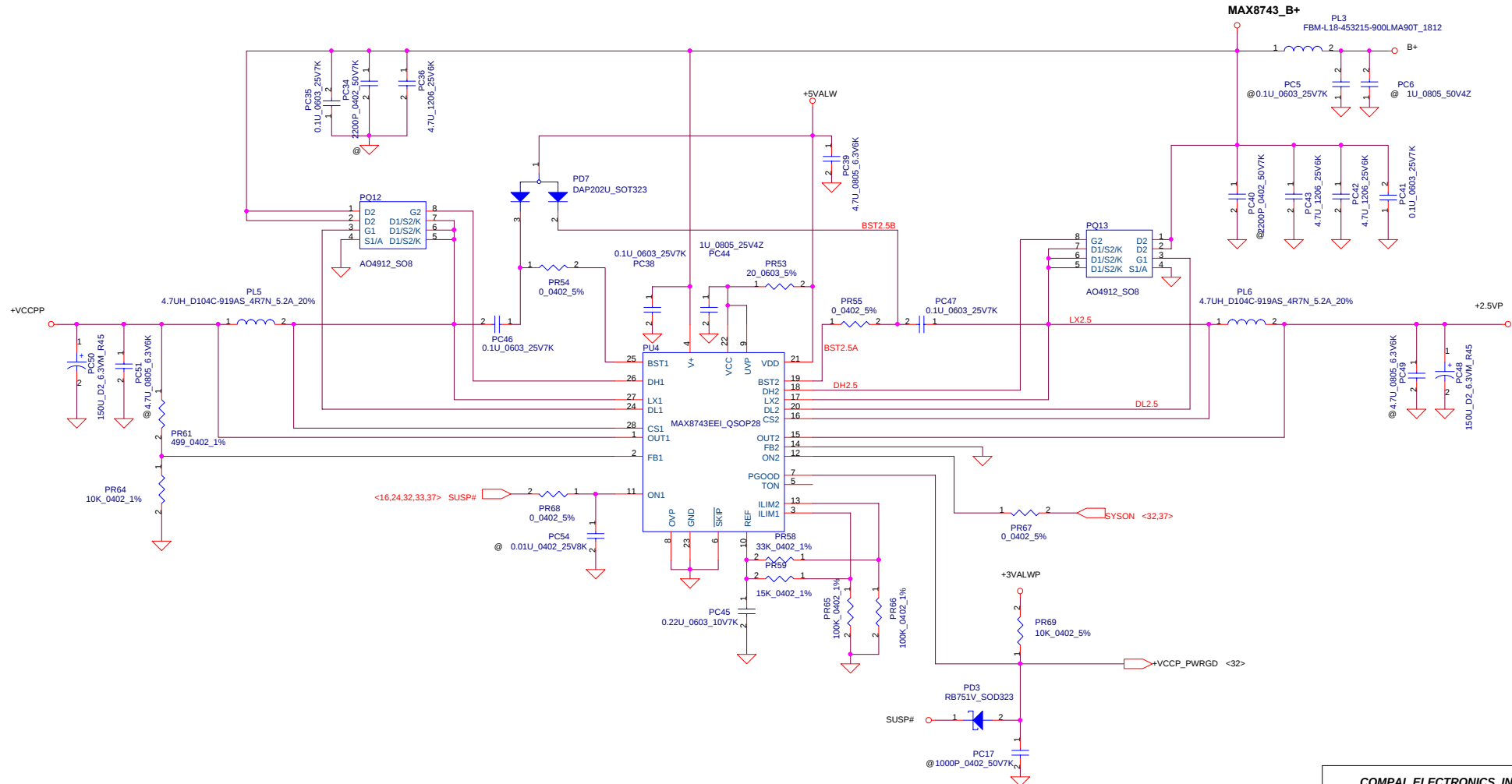
+5VALWP Choke DCR = 40mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/0.698K*(1.54K+0.698K)/40=6.412A
OCP Max.=120mV/0.698K*(0.698K+1.54K)/40=9.593A

Compal Electronics, Inc.			
Title	3.3V / 5V / 12V		
Document Number	402362		
Rev	0.1		
Date	Friday, March 11, 2005	Sheet	41 of 52

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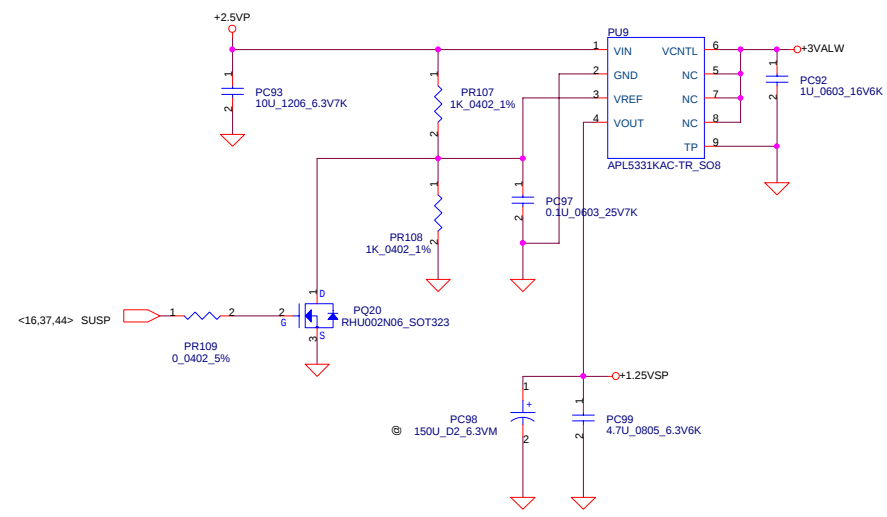
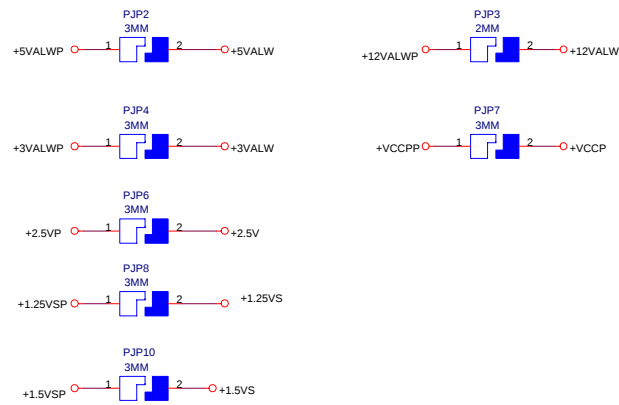
$V_{in}=19V, V_o=2.5V, I_o=4.5A, F_s=345KHZ, L=4.7UH$
 $Mosfet\ Rds(ON)\ tpy.=19.7m\Omega\ Max=24m\Omega, \Delta I = 0.6118A$
 $I_{limit}=ILIM(V)/10/Rds(ON)+1/2\ \Delta I$
 $I_{limit\ Min}=1.98V*100K/(100K+15K)/10/31.2m\Omega+0.3059=5.824A$
 $I_{limit\ Max}=2.02V*100K/(100K+15K)/10/19.7m\Omega+0.3059=9.821A$
 $+VCCPP = 5.824A \sim 9.821A$

$V_{in}=19V, V_o=2.5V, I_o=4.5A, F_s=255KHZ, L=4.7UH$
 $Mosfet\ Rds(ON)\ tpy.=19.7m\Omega\ Max=24m\Omega, \Delta I = 1.8115A$
 $I_{limit}=ILIM(V)/10/Rds(ON)+1/2\ \Delta I$
 $I_{limit\ Min}=1.98V*100K/(100K+33K)/10/31.2m\Omega+0.905=5.6765A$
 $I_{limit\ Max}=2.02V*100K/(100K+33K)/10/19.7m\Omega+0.905=8.614A$
 $+2.5VP = 5.6765A \sim 8.614A$



COMPAL ELECTRONICS, INC			
Title	+2.5VP & +VCCPP		
Document Number	LA-2362		
Rev	1		
Date	Friday, March 11, 2005	Sheet	42 of 52

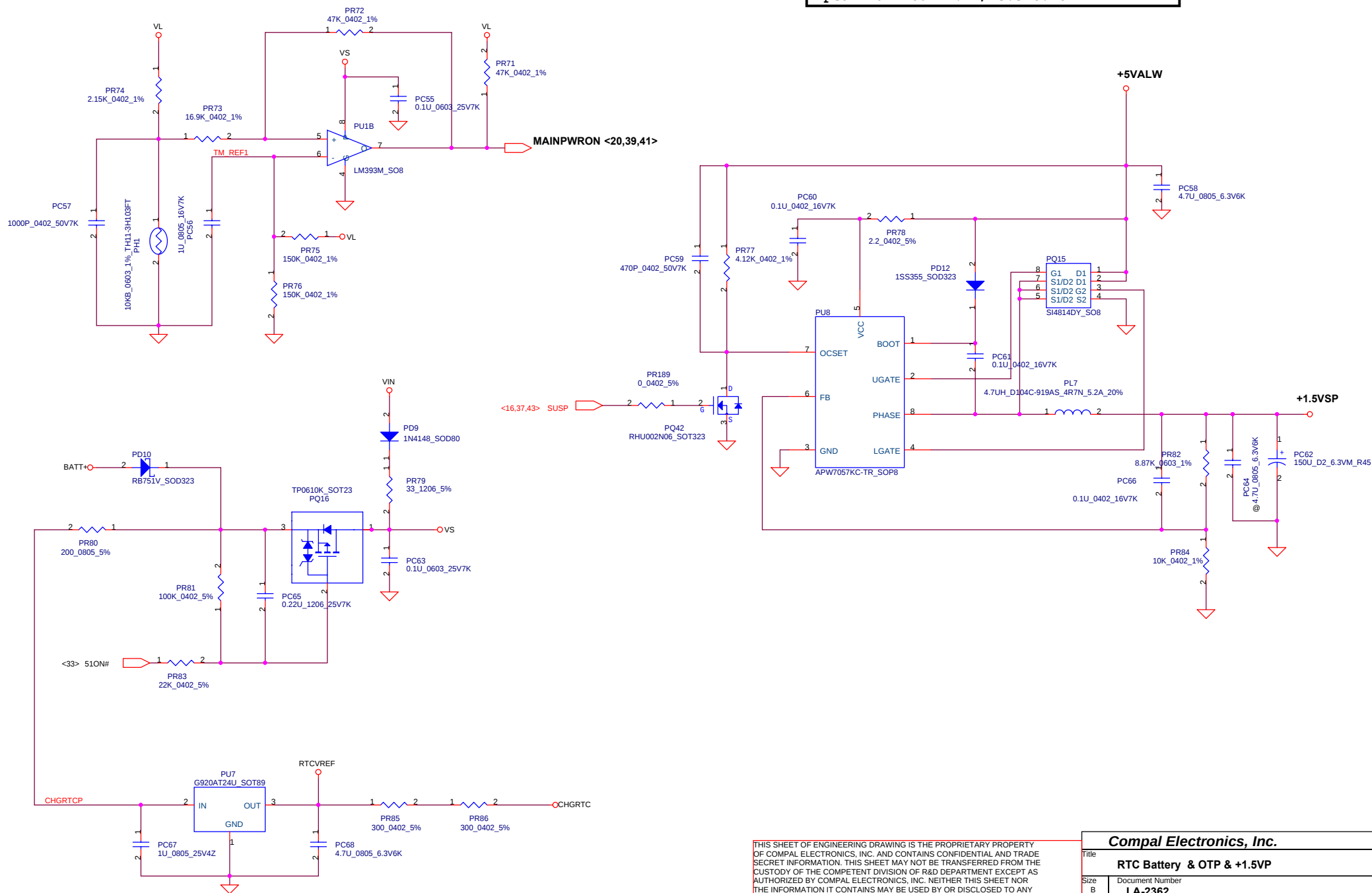
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PH2 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C

$I_{peak} = I_{ocset} * R_{ocset} / R_{DS(ON)} \text{ high side}$
 $I_{ocset} = 40\mu A$, $R_{ocset} = 4.12K$ $R_{DS(on)} = 25.5m\Omega$
 $I_{peak \text{ min}} = 40\mu A * 4.12 / (25.5 * 1.3) = 4.97A$
 $I_{peak \text{ max}} = 40\mu A * 4.12 / 25.5 = 6.46A$



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Compal Electronics, Inc.			
Title		RTC Battery & OTP & +1.5VP	
Size		Document Number	
B		LA-2362	
Date:		Friday, March 11, 2005	Sheet 44 of 52
		Rev	1

Vin=19V,Vo=1.484V,Io=12.5A,Fs=300KHZ,L=0.56UH
Current sense tpy.=1mΩ Max=1.1mΩ,Delta I =8.12A
Iimit=ILIM(V)/20/DCR+1/2 delta I
Iimit Min={1.99V*78.7K/(78.7K+470K)/20/1.01mΩ+4.22A}*2=36.69A
Iimit Max={2.01V*78.7K/(78.7K+470K)/20/0.99mΩ+4.22A}*2=37.56A

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Compal Electronics, Inc.

+CPU_CORE

Document Number

LA-2362

Date: Friday, March 11, 2005

Sheet 45 of 52

Rev 1

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1					ICH_PME# pull up +3VALW add R 10K	0.2	DVT
2					LID_SW# pull up +3VALW add R 10K	0.2	DVT
3					SB +1.5V regulator footprint error	0.2	DVT
4					SB +1.5V regulator footprint error U8 need to reverse	0.2	DVT
5					R76 take off	0.2	DVT
6					PR191 power plane 2.5vref change to +2.5V	0.2	DVT
7					R398 remove to R401	0.2	DVT
8					H_DPRS LP# add pull up to +vccp power plane POP R546	0.2	DVT
9					POP U9 for lose and foot print error	0.2	DVT
10					U3 pin6 & pin 7 need to swap	0.2	DVT
11					Add R476/7 40.2 Ohm for memory	0.2	DVT
12					R259 short	0.2	DVT
13					PR122 chang power plane to +3V for EC voltage leakage	0.2	DVT
14					Add R224/R290/R407 470ohm and Q34/9/11 2N7002	0.1	DVT-2
15					ADD R 39K//220p to GND at R518 for modify SIRQ	0.1	DVT-2
16					Reverse the JHP1 & JMIC1 Symble error	0.1	DVT-2
17					Modify NB FSB speed select for Dothan	0.1	DVT-2
18					Modify ACIN for SB	0.1	DVT-2
19					CardReader pin swap for flash memory	0.1	DVT-2
20					Reverse the JHP1 & JMIC1 Symbl	0.1	DVT-2
21					Add VCCP noise cap. at CPU C664/5/6/7/8/9 C670/1/2	0.2	DVT-3
22					Change R362/3 2.2K to 10K for Panel select	0.2	DVT-3

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Compal Electronics, Inc.			
Title			
PIR			
Drawing Number			
LA-2362			
Date	Friday, March 11, 2005	Sheet	46 of 52
Rev	1		

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
23					Add C674/5/6/7/8 C680/1/2/3/4/5 C686/7/8/9 C690/1/2/3/4/5/6/7/8/9 C702/3 for NB VCCP noise cap.	0.2	DVT-3
24					ADD C646/7/8/9 C650/1/2/3/4/5 for DDR RAM 1.25V noise cap	0.2	DVT-3
25					ADD C704/5 for JVGAP1 2.5V for noise	0.2	DVT-3
26					Change R17/8/9 from 75 to 150 OHM for TV-out signal	0.2	DVT-3
27					ADD R774/5 for cost down U29 parts	0.2	DVT-3
28					Change SB(U5) sus power from V plane to Always power plane and R457 R69 R456 R455 R456 R451 U7.T2 +1.5VR	0.2	DVT-3
29					R154 remove for FIR function	0.2	DVT-3
30					ADD C656/7 C659/8 for +5VS HDD CDROM power noise	0.2	DVT-3
31					U9 replace the new package to RM8 and remove to TOP	0.2	DVT-3
32					ADD C706/7/8/9/10/11 for SB 1.5Vrun noise	0.2	DVT-3
33					R129 change to +5VALW	0.2	DVT-3
34					Q3 cahnge to AO3400 for current rating not enough	0.2	DVT-3
35					JMPC11 P.24 change to +3V for wireless power	0.2	DVT-3
36					Remove KB910 & 39VF080 ROM	0.2	DVT-3
37					R705 change to 13K for MB ID	0.2	DVT-3
38					Change the Killer switch circuit for EC detect method then light on the LED	0.2	DVT-3
39					Move U32 to near NB	0.2	DVT-3
40					ADD 5VALW noise cap. C714/5/2/3,	0.2	DVT-3
41							
42							
43							
44							

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Compal Electronics, Inc.			
Title			
PIR			
Revision Number		Rev	
LA-2362		1	
Date	Friday, March 11, 2005	Sheet	47 of 52

Version change list (P.I.R. List)

Page 1 of 2

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Delete the charge circuit.	Delete the charge circuit.	0.2	38	1.Delete the PU5 IC LM393M (SM). 2.Delete PD1 S DIO 1N4148 (SM). 3.Delete PR10,PR11,PR12,PR13 S RES 1/4W 1.5K +-5% 1206.	0.2	DVT
2	Change the CPU OTP circuit from active H to active L.	Change the CPU OTP circuit from active H to active L.	0.2	43	1.Delete PQ14 S TR DTC115EUA NPN (UMT3). 2..Delete PD8 S DIO 1SS355. 3.Change PR75 and PR76 from S RES 1/16W 100K +-1% 0402 to S RES 1/16W 150K +-1% 0402. 4.Change PR73 from S RES 1/16W 15K +-1% 0402 to S RES 1/16W 16.9K +-1% 0402. 5.Change PC56 from S CER CAP .22U 16V K X7R 0603 to S CER CAP 1U 16V K X7R 0805 6.Change PR74 from S RES 1/16W 3.4K +-1% 0402 to S RES 1/16W 2.15K +-1% 0402.	0.2	DVT
3	For cost down solution.	To cost down for +1.5VP.	0.2	43	1.Change the PD12 from DIO 1N4148 (SM) to DIO 1SS355.	0.2	DVT
4	For cost down solution.	To cost down for RTC charge circuit..	0.2	43	1.Delete the PD33 S ZEN DIO RLZ4.3B (LL-34).	0.2	DVT
5	To prevent the KB-910 damag.	To prevent the KB-910 damag.	0.2	40	1.Change the PD17 from SCH DIO SKS10-04AT TSMA to SCH DIO SKUL30-02AT THIN SMA.	0.2	DVT
6	For cost down solution.	To cost down for +1.5VP for +12VALWP circuit.	0.2	40	1.Delete PR187 S RES 1/8W 2.7K +-5% 1206 S7.	0.2	DVT
7	For cost down solution.	To cost down for DDR 2.5V.	0.2	41	1.Delete PR62 S RES 1/16W 0 +-5% 0402.	0.2	DVT
8	For cost down solution.	To cost down for CPU_CORE.	0.2	44	1.Delete PR127 and PR152 S RES 1/16W 0 +-5% 0402.	0.2	DVT
9	For cost down solution.	To cost down for snubber circuit.	0.2	40	1.Deete PR127 and PR152 S RES 1/16W 0 +-5% 0402. 2.Delete the PC161 S CER CAP 470P 100V K X7R 0805.	0.2	DVT
10	For cost down solution.	To cost down for EMI capacitor.	0.2	39 40 41	1.Delete PC41,PC158 and PC159 S CER CAP .1U 25V K X7R 0603. 2.Delete PC40,PC73 and PC76 CER CAP 2200P 50V K X7R 0402.	0.2	DVT
10	Don't has pull high resister on VGATE pin.	Add pull high resister on VGATE pin.	0.2	44	1.Add the S RES 1/16W 100K +-5% 0402.	0.2	DVT
10	VCCPP output voltage has error.	Adjustment resistor divider.	0.2	41	1.Change the PR60 from S RES 1/16W 681 +-1% 0402 to S RES 1/16W 1.69K +-1% 0603.	0.2	DVT
11.	Choke Rating not enough for +1.5VP.	Choke Rating not enough for +1.5VP.	0.2	43	1.Change PL7 from 4.7UH_FDV0630-4.7UH_5.5A_20% to 4.7UH_D104C-919AS_4R7N_5.2A_20%.	0.2	DVT

Compal Electronics, Inc.

Title	PIR	Rev	1
Document Number	LA-2362	Date	Friday, March 11, 2005
Sheet	48	of	52

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Version change list (P.I.R. List)

Page 2 of 4

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Don't has pull down resister on SHDN# pin for charger.	Add pull down resister on SHDN# pin.	0.2	39	1.Add PR193 the S RES 1/16W 100K +-5% 0402.	0.2	DVT
2	Change the Vin Detector from LM393 to charger ACOK#.	Change the Vin Detector from LM393 to charger ACOK#.	0.2	38,39	1.Add the PQ40 S TR DTC115EUA NPN (UMT3). 2.Delete the PR3,PR4,PR8 and PR9 RES 1/16W 10K +-1% 0402. 3.Add the PR193,PR172 and PR173 RES 1/16W 100K +-5% 0402. 4.Delete PR6 the S RES 1/16W 22K +-1% 0402. 5.Delete PR1 the S RES 1/16W 1M +-1% 0402. 6.Change PR182 from S RES 1/16W 150K +-1% 0402 to S RES 1/16W 20K +-1% 0402. 7.Delete the PR7 S RES 1/16W 20K +-1% 0402. 8.Delete the PR2 S RES 1/16W 84.5K +-1% 0402. 9.Add the PR175 S RES 1/16W 158K +-1% 0402. 10.Add the PR175 S RES 1/16W 681K +-1% 0402. 11.Delete PC6 from S CER CAP .1U 25V K X7R 0603. 12..Delete PC5 from S CER CAP 1000P 50V +-10% X7R 0402.	0.2	DVT
3	For ACIN pin,	ACIN pin don't have connect to system.	0.2	39	1.Add PR4 the 10K +-5% 0402	0.2	DVT
4	+1.8VSP power rating not enough.	+1.8VSP power rating isnot enough.	0.2	42	1.Change PU10 from S IC 6965-18P1U SOP-8L REG to S IC APW7057KC-TR SOP-8 PWM. 2.Add PR197 S RES 1/16W 12.7K +-1% 0402. 3.Add the PQ44 S TR RHU002N06 1N SOT323 4.Delete PQ43 the S TR A04912 2N S08 W/D 5.Add PD33 the S DIO 1SS355. 6.Add PR195 the S RES 1/16W 2.2 +-5% 0402 7.Add PR198 the S RES 1/16W 10K +-1% 0402. 8.Add PR196 the S RES 1/16W 4.12K +-1% 0402 9.Add the PC167 the S CER CAP 4.7U 10V Z Y5V 0805. 10.Add the PC164 S CER CAP 470P 50V +-10% X7R 0402. 11.Add the PC163,PC165 and PC168 S CER CAP .1U 16V +-10% X7R 0402 12.Delete PC96 the S CER CAP 10U 6.3V K X7R 1206. 13.Add the PC166 S POLY CAP 150U 6.3V M V(D2) T520 LESR. 14.Add PL18 the S COIL 5.0UH +-20% TPRH6D38-5R0M-N 2.9A.	0.2	DVT
5	VCCP's transients cannot meet spec.	VCCP's transients cannot meet spec.	0.2	41	1.Change PC50 from S POLY CAP 150U 6.3V M V(D2) T520 LESR to S POLY C 220U 4V M V(D2) T520 LESR. 2.Change PL6 from S COIL 4.7UH +-20% D104C-919AS-4R7M 5.2A to S COIL 1.8UH +-30% D104C-919AS-1R8N 9.5A.	0.2	DVT
6	For CPU_CORE's EMI,	For CPU_CORE's EMI,	0.2	44	1.Change the PR125 and PR148 from S RES 1/16W 0 +-5% 0402S to RES 1/16W 2 +-5% 0402.	0.2	DVT

Compal Electronics, Inc.

Title	PIR	Rev	1
Document Number	LA-2362	Date	Friday, March 11, 2005
Sheet	49	of	52

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Version change list (P.I.R. List)

Page 3 of 3

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1.	CPU's transients cannot meet spec.	Add one current sense on phase 2.	0.2	44	1.Delete PC124 and PC137 the S CER CAP 0.47U 16V +-10% X7R 0603. 2.Delete PR134,PR141,PR155 and PR156 the S RES 1/16W 909+-1% 0402. 3.Add PR134 S RES 1W 0.01 +-1%2512.	0.2	DVT
2.	PACIN pin's high level is only 2.3V.	To adjust PACIN pin's level.	0.2	39	1.Delete PR175 the S RES 1/16W 158K+-1% 0402. 2.Change the PR172 from S RES 1/16W 100K +-1% 0402 S to RES 1/16W 10K +-1% 0402.	0.2	DVT
3.	The 5VALWP rising time is faster than PACIN's.	To delay timer of 5VALWP.	0.3	40	1.Change the PR105 from S RES 1/16W 47K +-1% 0402 S to RES 1/16W 100K +-1% 0402. 2.Change the PC91 from S CER CAP .047U 25V M X7R 0603 to CAP 1U 25V Z F Y5V 0805..	0.3	DVT2
4.	The charge has error on change mode.	To adjust input and output current regulation loop compensation.	0.3	39	1.Change PC152 and PC153 from the S CER CAP 0.01U 16V +-10% X7R to CER CAP 0.001U 16V +-10% X7R.	0.3	DVT2
5.	For cost down solution.	For cost down solution.	0.3	42 43	1.Change PC58,PC68,PC95 and PC99 from the S CER CAP 4.7U 25V K X5R 1206 to CAP 4.7U 10V K X7R 0805.	0.3	DVT2
6.	The charger has EMI issue.	Add a resistor on charger's boost for EMI.	0.3	39	1.Add the PR1 S RES 1/16W 0 +-5% 0402.	0.3	DVT2
7.	Change the current limit's from sense DRC to resister.	To adjust current limit point for CPU_CORE.	0.3	44	1.Change the PR142 from S RES 1/16W 200K +-5% 0402 to S RES 1/16W 470K +-5% 0402.	0.3	DVT2
8.	To preven in-rush current for B+ of MAX1902.	To preven in-rush current for B+ of MAX1902.	0.3	40	1.Add PR2 S RES 1/8W 33 +-5% 1206.	0.3	DVT2
9.	The CPU's dual choke will shortage.	Change to single choke.	0.3	44	1.Add PQ26 SB502060000 S TR RHU002N06 1N SOT323. 2.Add PR134,PR141,PR155,PR156 S RES 1/16W 909 +-1% 0402. 3.Delete PL14 S COIL .5UH +-30% CXZT1050-R50 28A. 4.Add the PL14,PL15 S COIL .56UH +-20% ETQP4LR56 WFC 21A. 5.Add the PC124,PC137 0.47U 16V +-10% X7R 0603 S8. 4.Add the PL14,PL15 S COIL .56UH +-20% ETQP4LR56 WFC 21A.	0.3	DVT2
10.	Delete the +1.8VSP on M/B.	Delete the +1.8VSP on M/B.	0.3	42	1.Delete the PU10 S IC APW7057KC-TR SOP-8 PWM. 2.Delete the PQ43 S TR A04912 2N S08 W/D. 3.Delete the PR188 S RES 1/16W 0 +-5% 0402. 4.Delete the PR195 S RES 1/16W 2.2 +-5% 0402 5.Delete the PR196 S RES 1/16W 4.12K +-1% 0402 6.Delete the PR198 S RES 1/16W 10K +-1% 0402 7.Delete the PR197 S RES 1/16W 12.7K +-1% 0402. 8.Delete the PL18 S COIL 5.0UH +-20% TPRH6D38-5R0M-N 2.9A. 9.Delete the PC166 S POLY CAP 150U 6.3V M V(D2) T520 LESR. 10.Change the PC75 and PC87 from S CER CAP 4.7U 10V Z Y5V 0805 to S CER CAP 4.7U 6.3V +-10% X5R 0805 11.Delete PC95 S CER CAP 4.7U 10V Z Y5V 0805. 12.Delete PC163,PC165,PC168 .1U 16V +-10% X7R 0402. 13.Delete PC164 S CER CAP 470P 50V +-10% X7R 0402. 14.Delete PD33 S DIO 1SS355.	0.3	DVT2

Compal Electronics, Inc.

Title	PIR	Rev	1
Document Number	LA-2362	Date	Friday, March 11, 2005
Sheet	50	of	52

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Compal Electronics, Inc.				
Title				
PIR				
CONFIDENTIAL SECTION OF R&D CONTAINS C.				Rev 1
Document Number LA-2362				
Date:	Friday, March 11, 2005	Sheet	51	of 52

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Document Number	Rev
LA-2362	1
Date	Sheet
Friday, March 11 2005	52 of 52