

HAWAA

LA-3142PREV 1.0

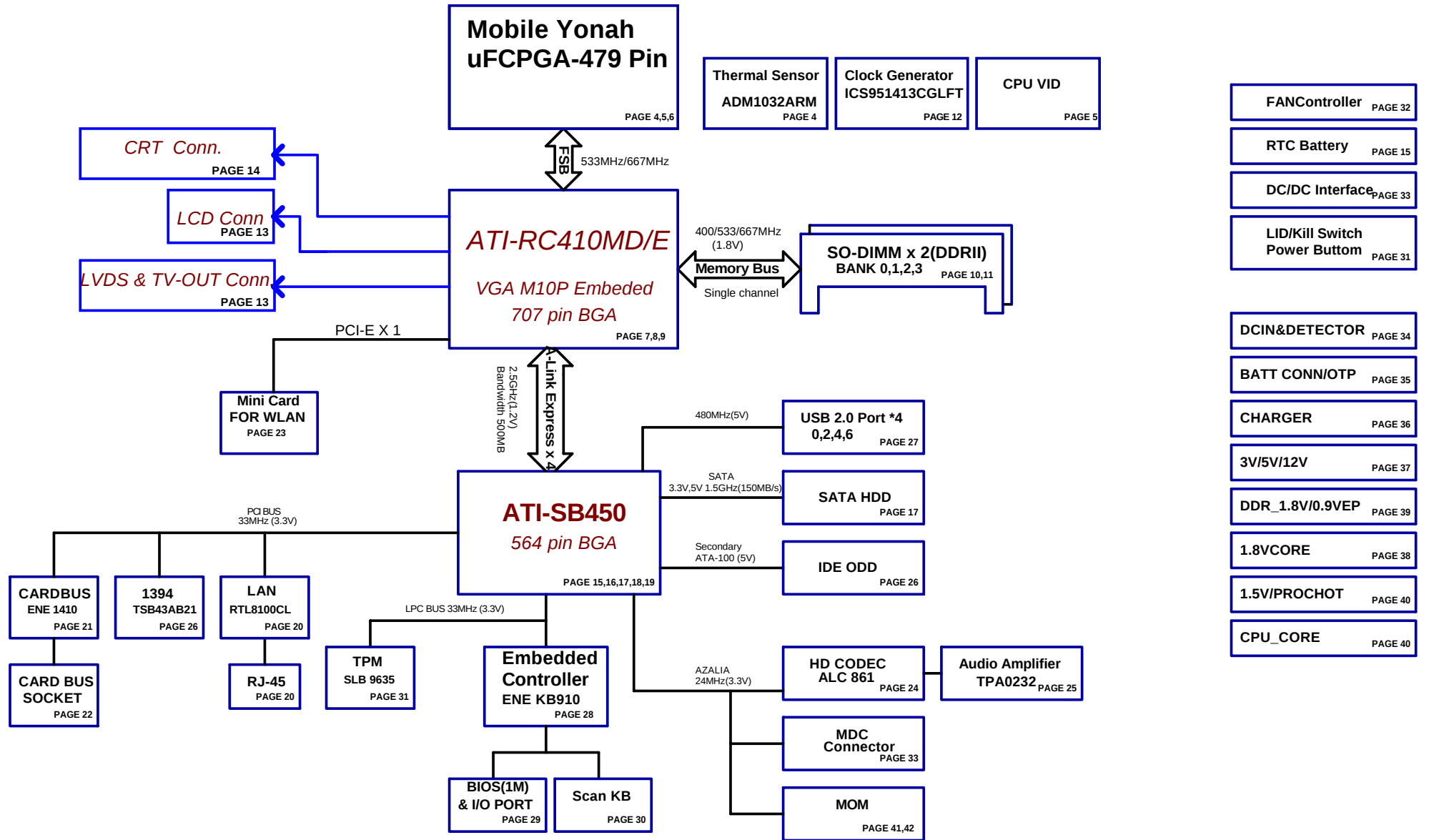
Schematic

uFCPGA Yonah/ ATi-RC410MD(A12)/ ATi-SB450(A13)

2006-03-08 Rev. 1.0

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HAWAA LA-3141 FUNCTION BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	Yonah	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
ENE 1410	AD20	2	PIRQB
LAN	AD22	1	PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b

EC SM Bus2 address

SB450 SM Bus address

Device	Address
Clock Generator (ICS951413BGLFT)	1101 001Xb
DDRII DIMM0	1010 0100b A4
DDRII DIMM1	1010 0110b A6

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

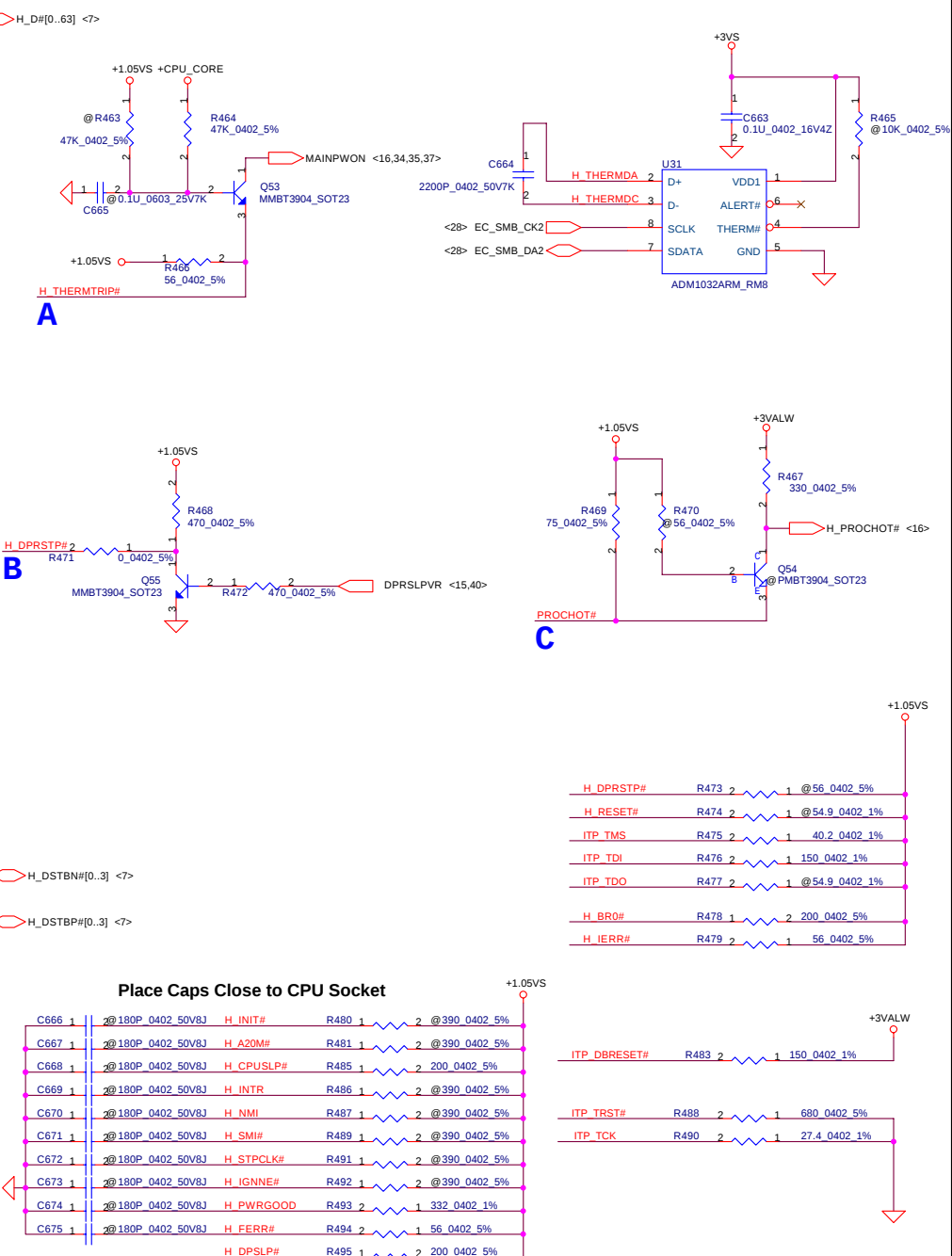
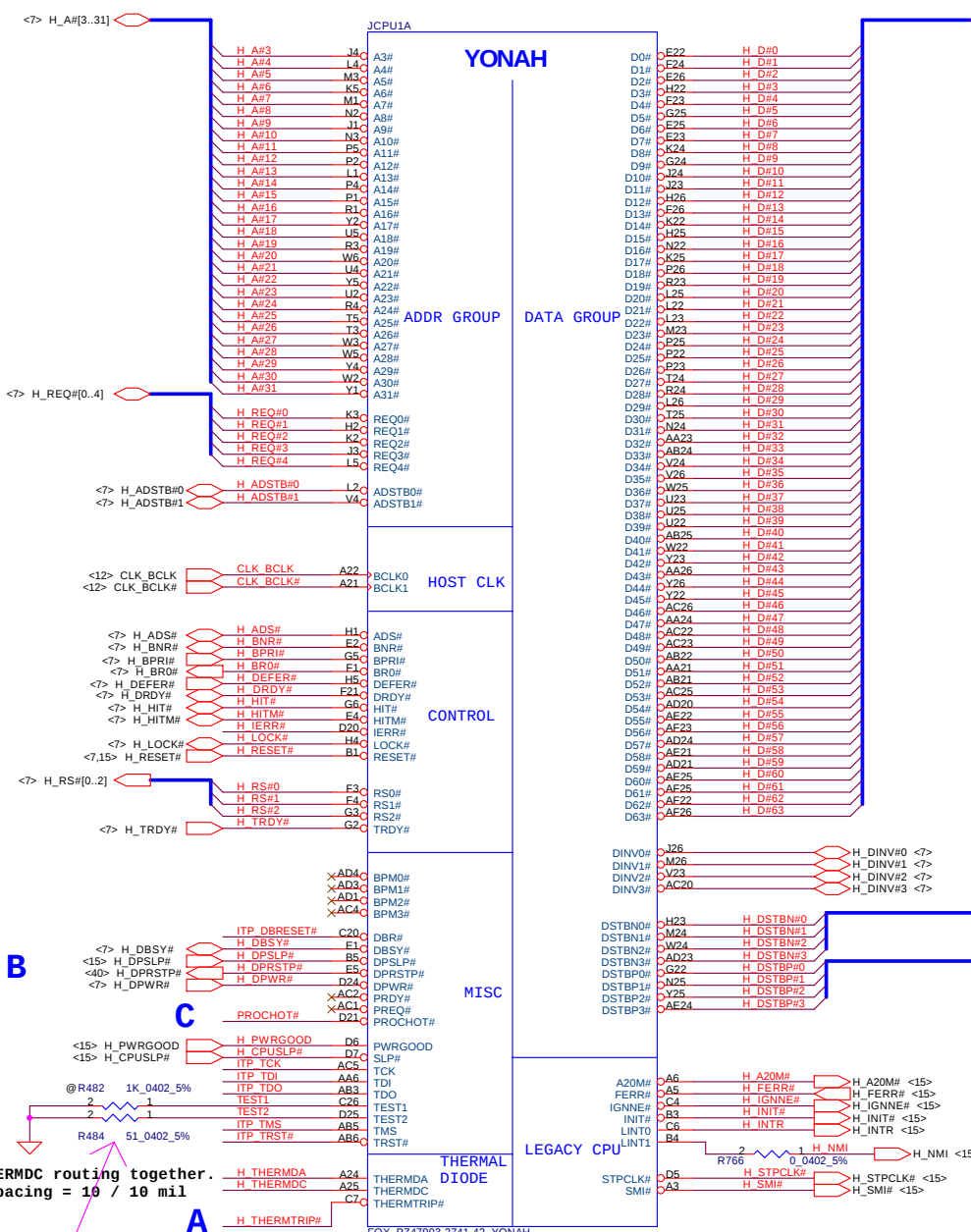
Vcc	3.3V +/- 5%			
Ra/Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

SKU ID	PCB Revision
0	All
1	
2	
3	
4	JP
5	
6	
7	

BTN ID	BTN Status
0	1 Buttons
1	
2	
3	
4	6 Buttons
5	
6	
7	

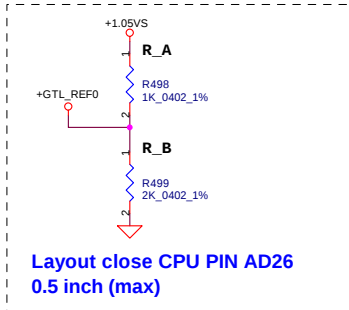
BTO Function	BOM structure
1394	1394@
Wireless LAN	WLAN@
TV-OUT	TVOUT@
TPM	TPM@



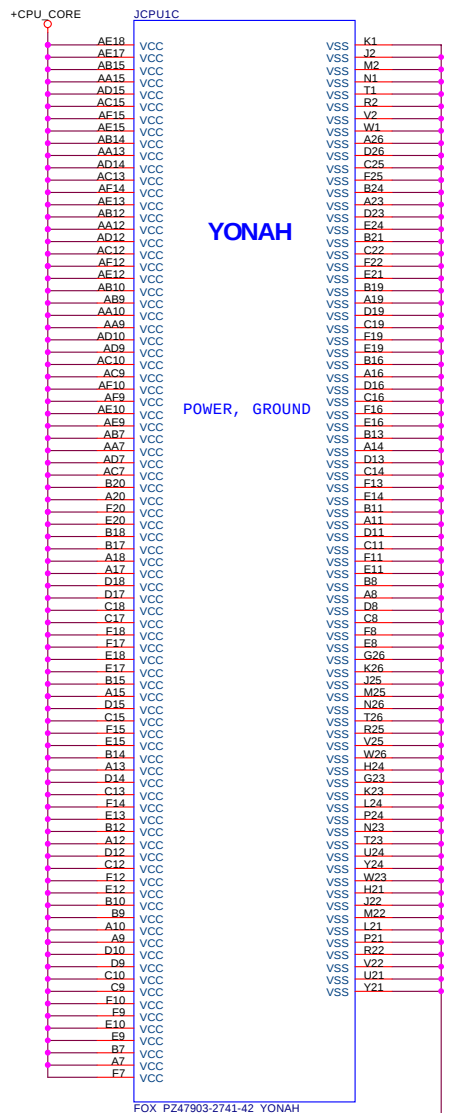
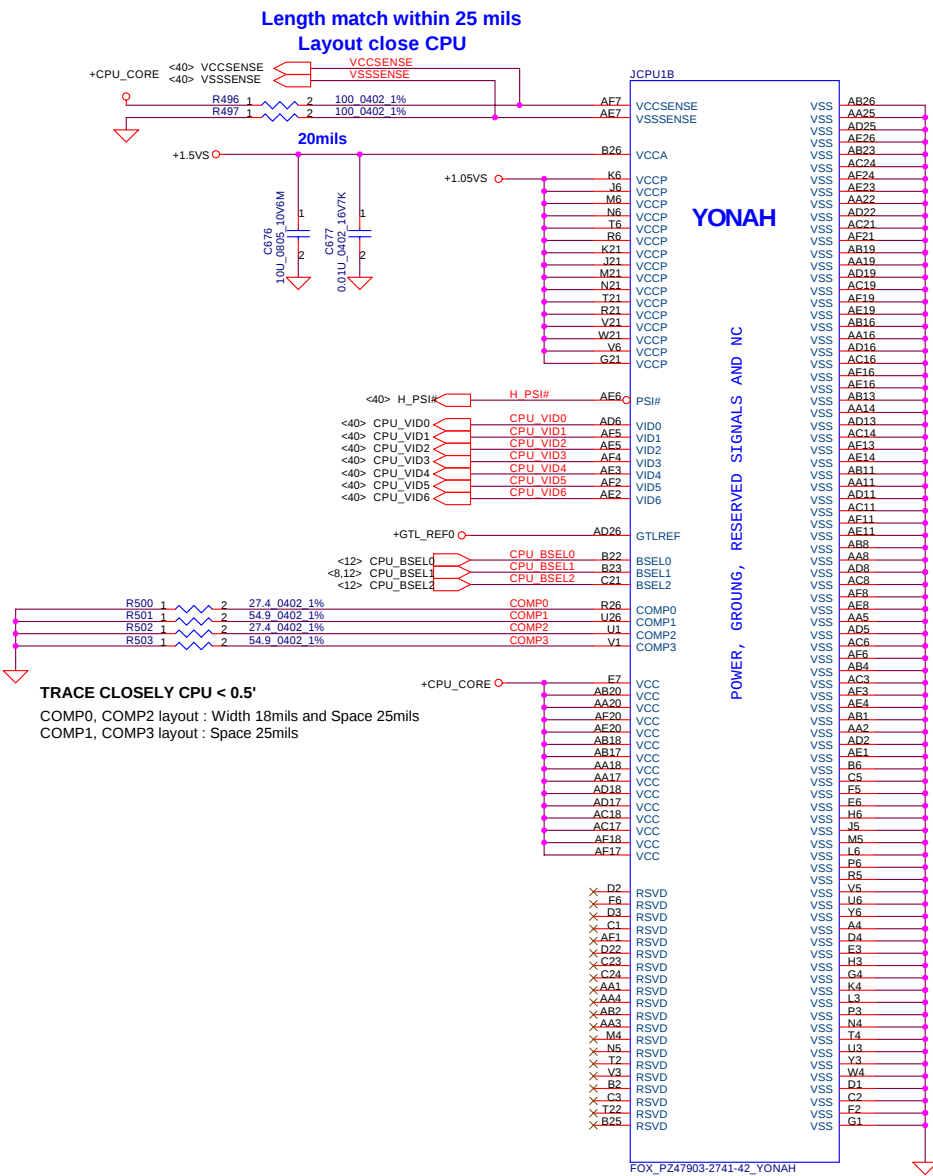
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

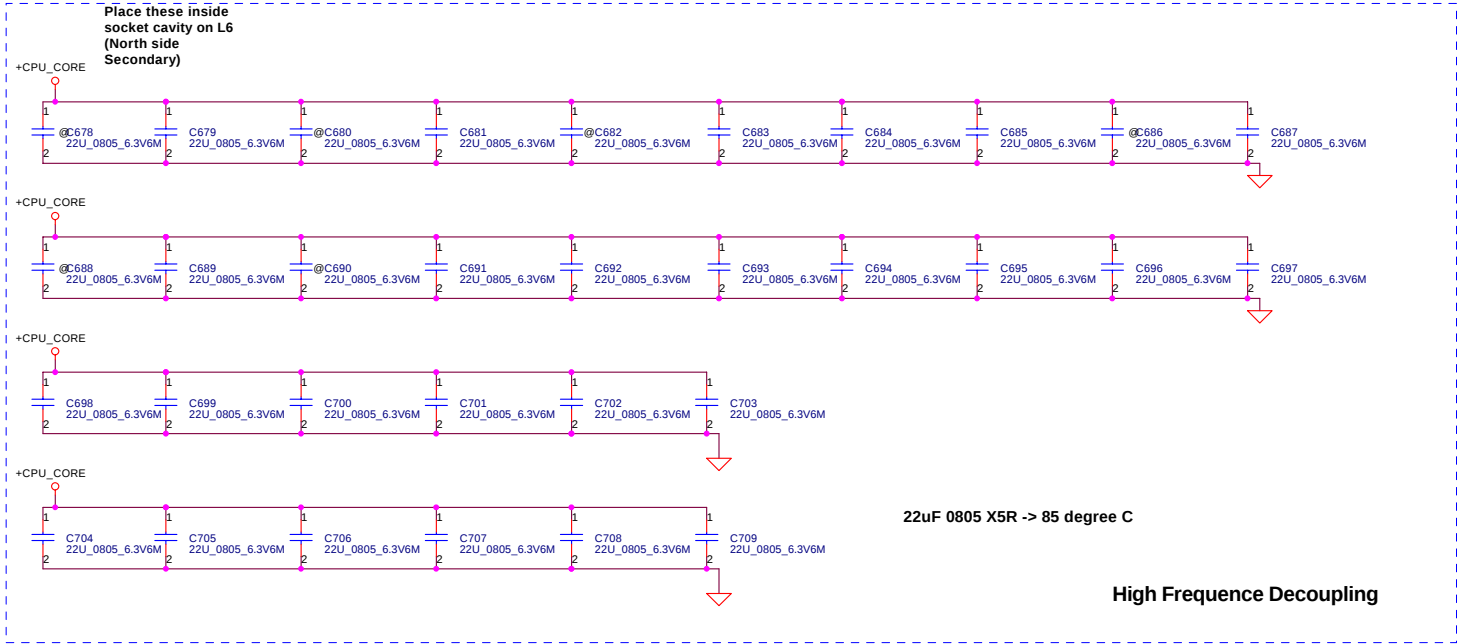
For B-0 stepping engineering samples (ES) of Celeron M processor need to pop this 51 ohm resistor.

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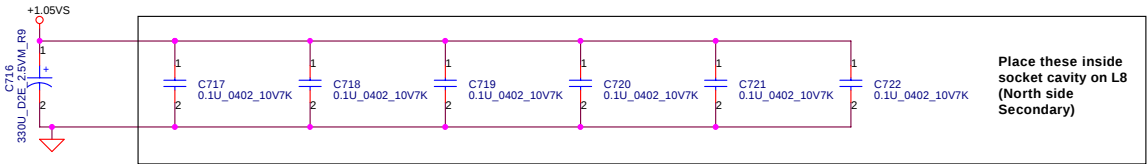
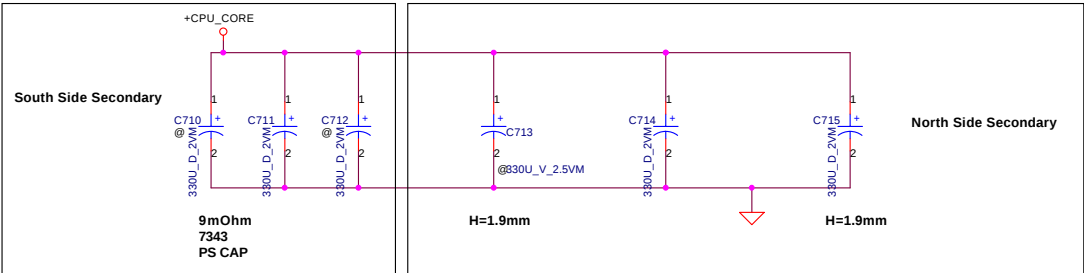


CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
133	0	0	1
166	0	1	1

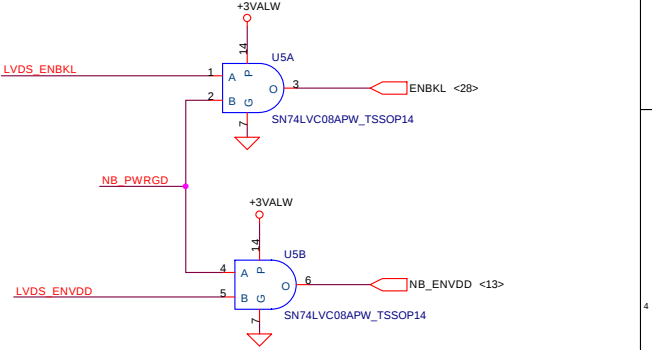
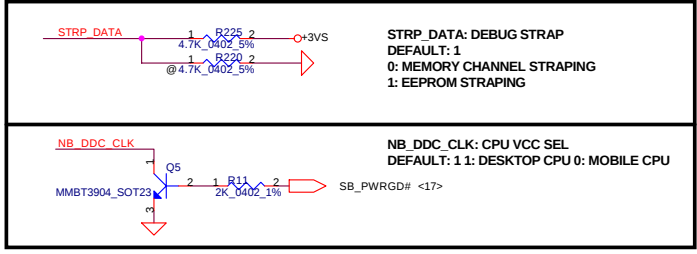
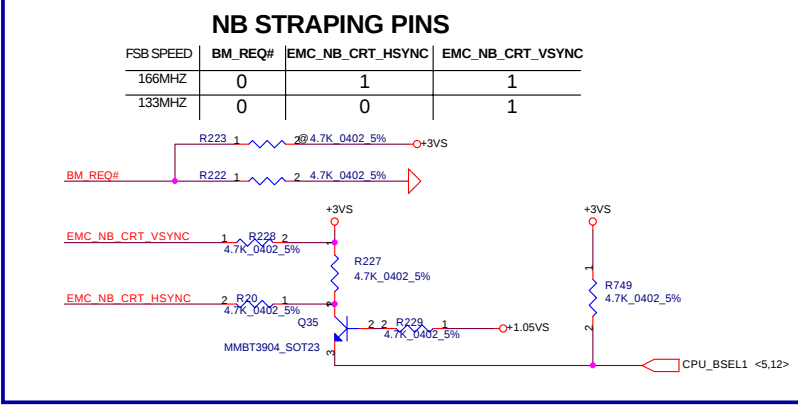
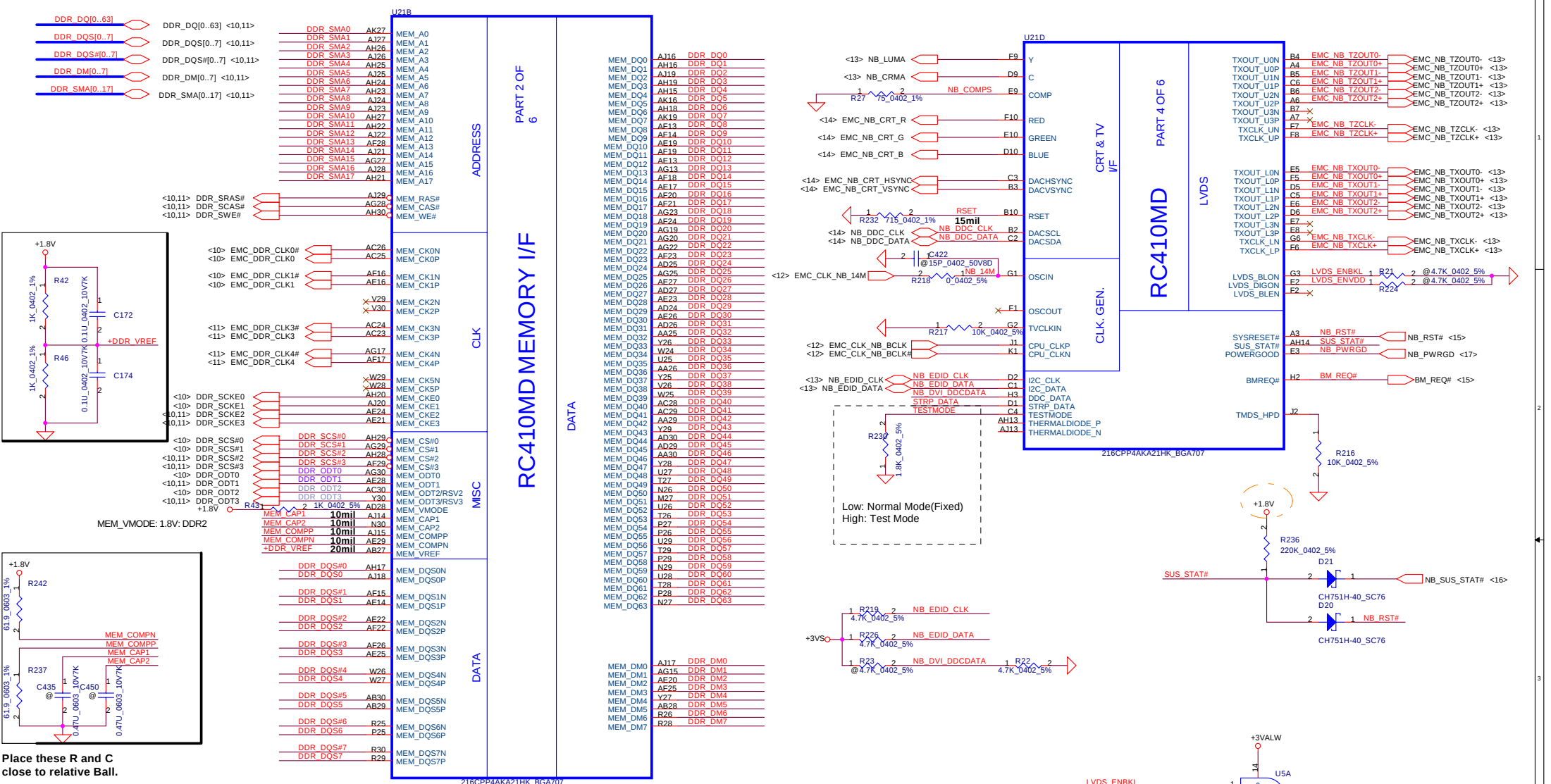


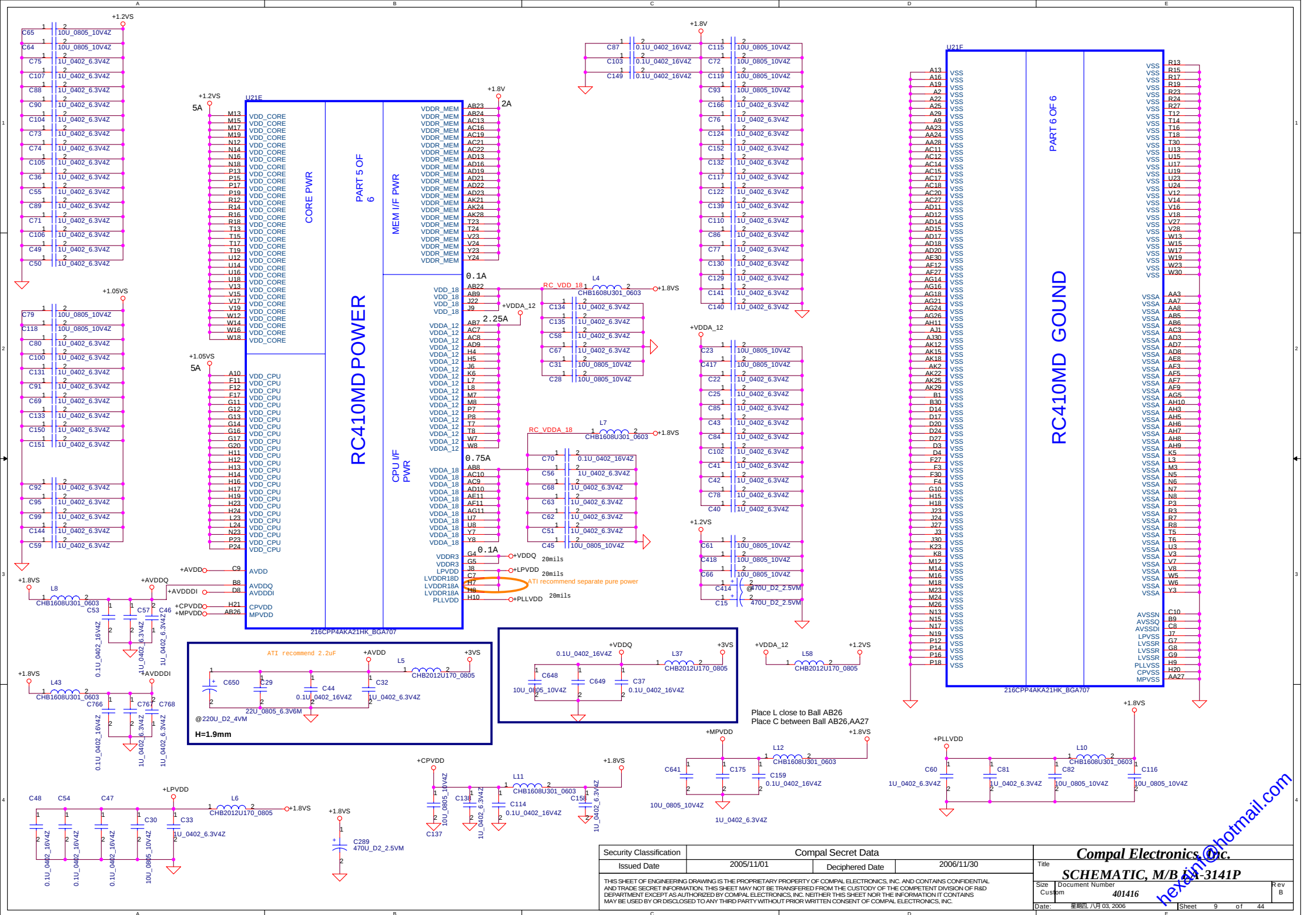


Near VCORE regulator.



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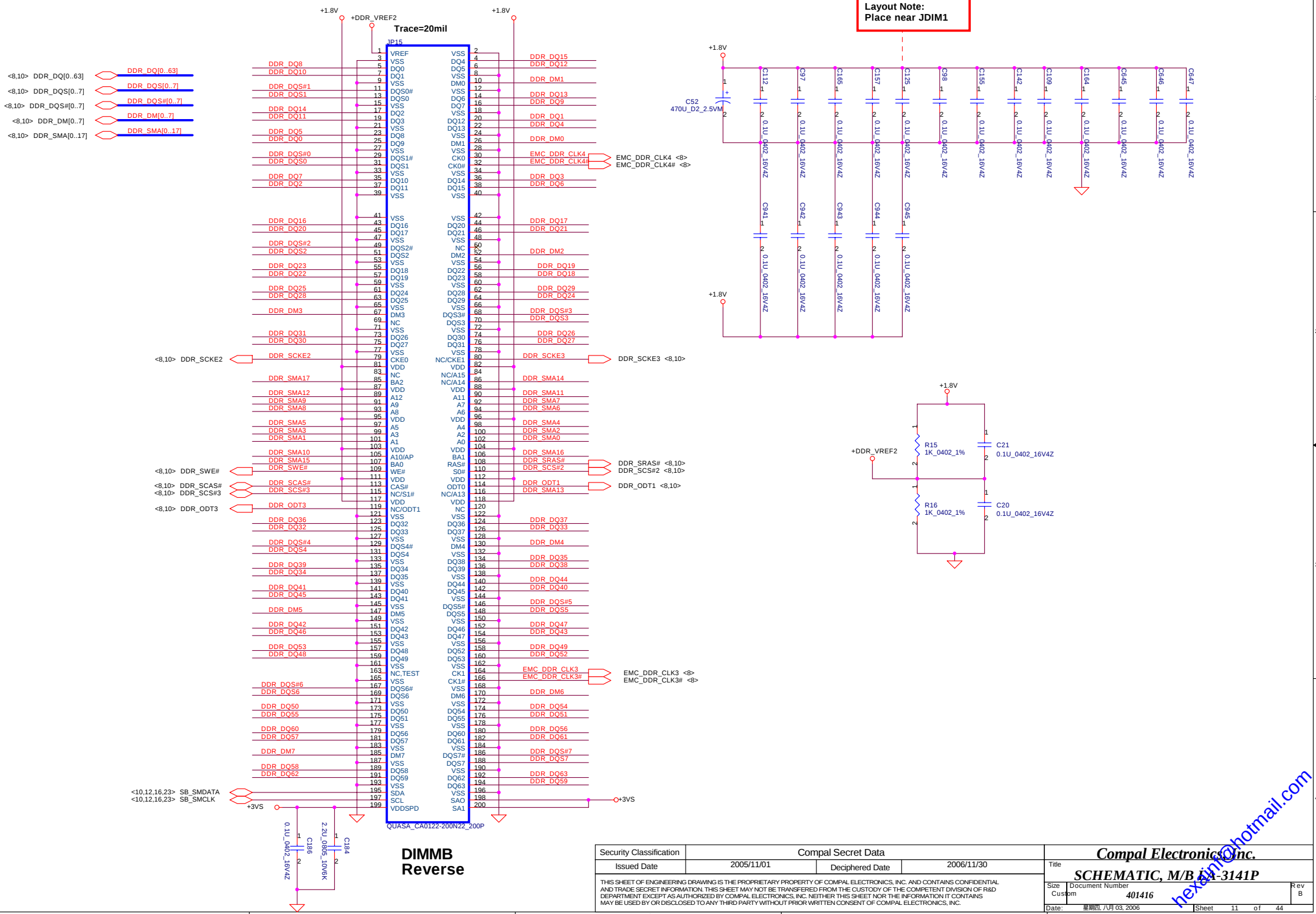




Layout Note:
Place near JDIM1

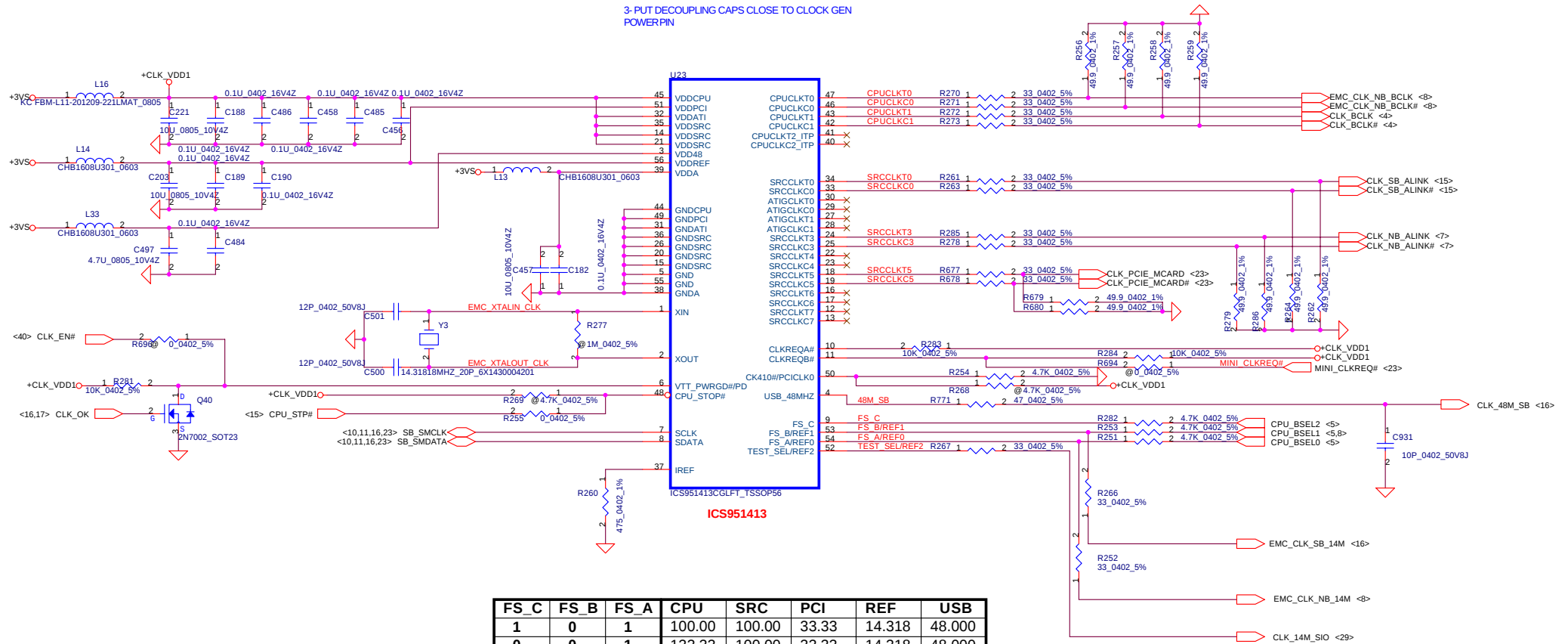
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to V_DDR_MCH_REF

Layout Note:
Every four parallel termination resistors with two caps,
one is connected to ground, the other one is connected
between +1.8V and +0.9VS. Need to place each parallel
resistor with one cap to GND and one cap between
+1.8V and +0.9VS



Clock Generator

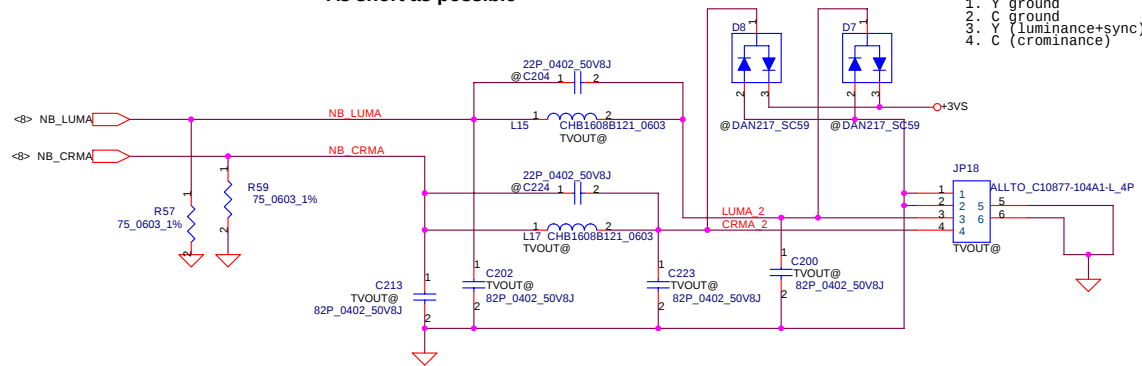
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK##, NBCLK##, ITPCLK## AND SCR## ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWERPIN



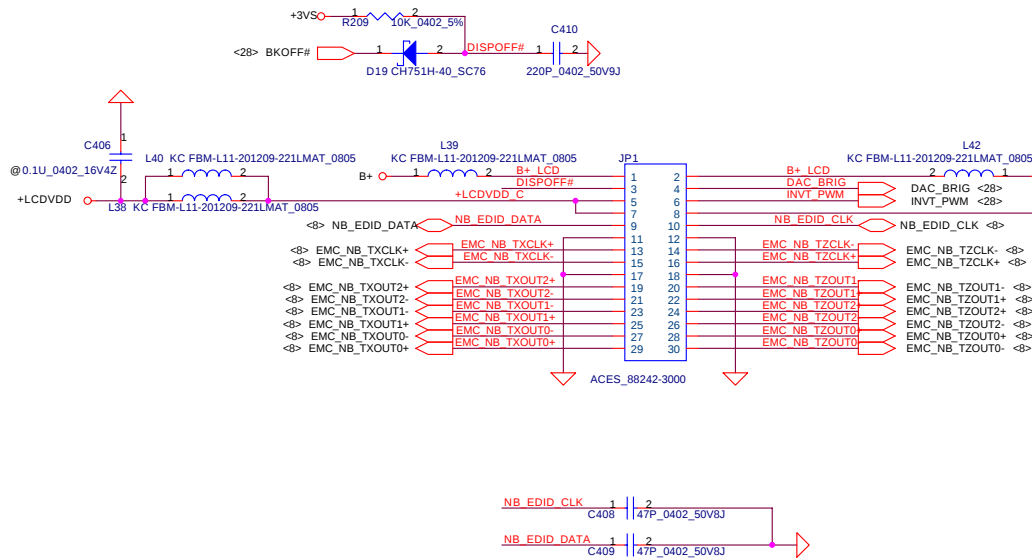
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

TV-OUT CONNECTOR

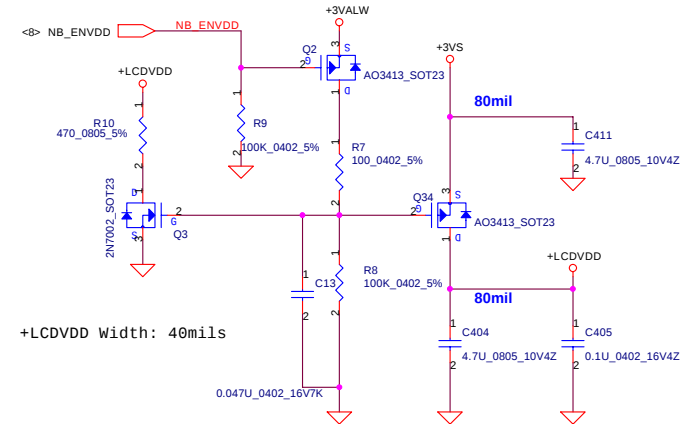
Reduce LUMA_1 and CRMA_1 length
As short as possible



LCD/PANEL BD. Conn.

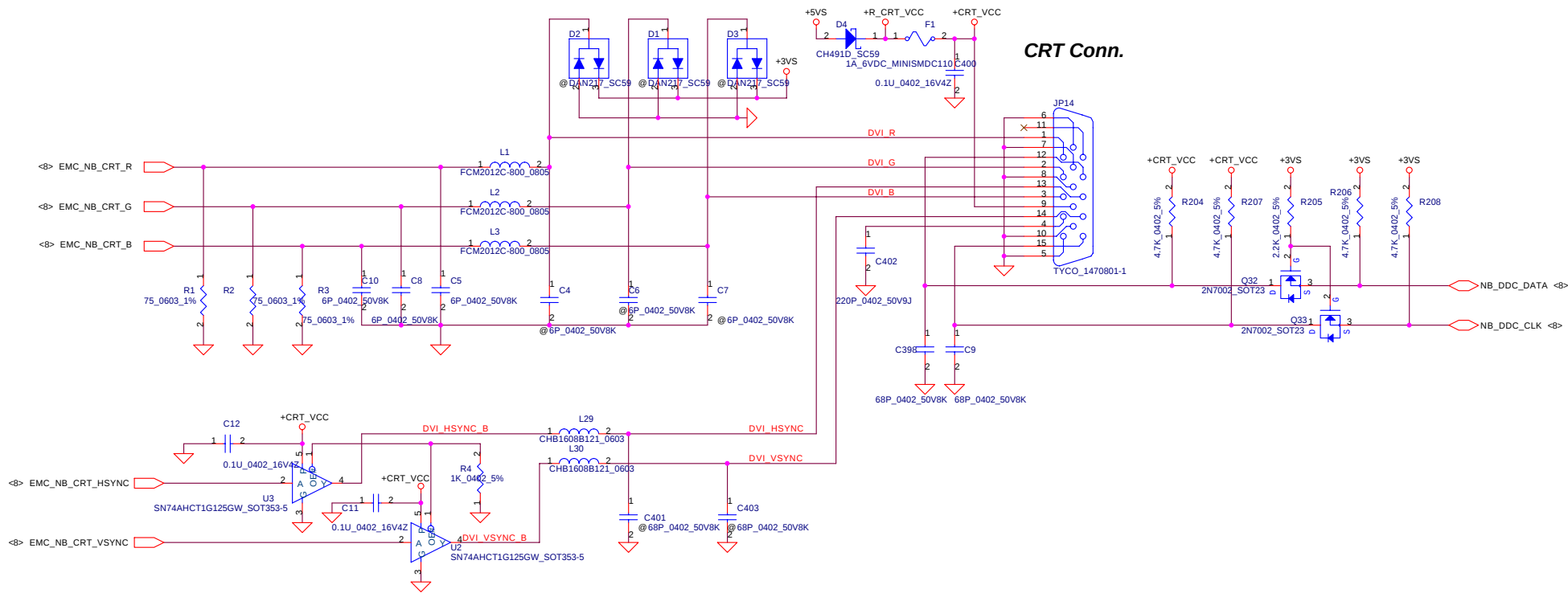


PANEL +LCDVDD CTRL CKT

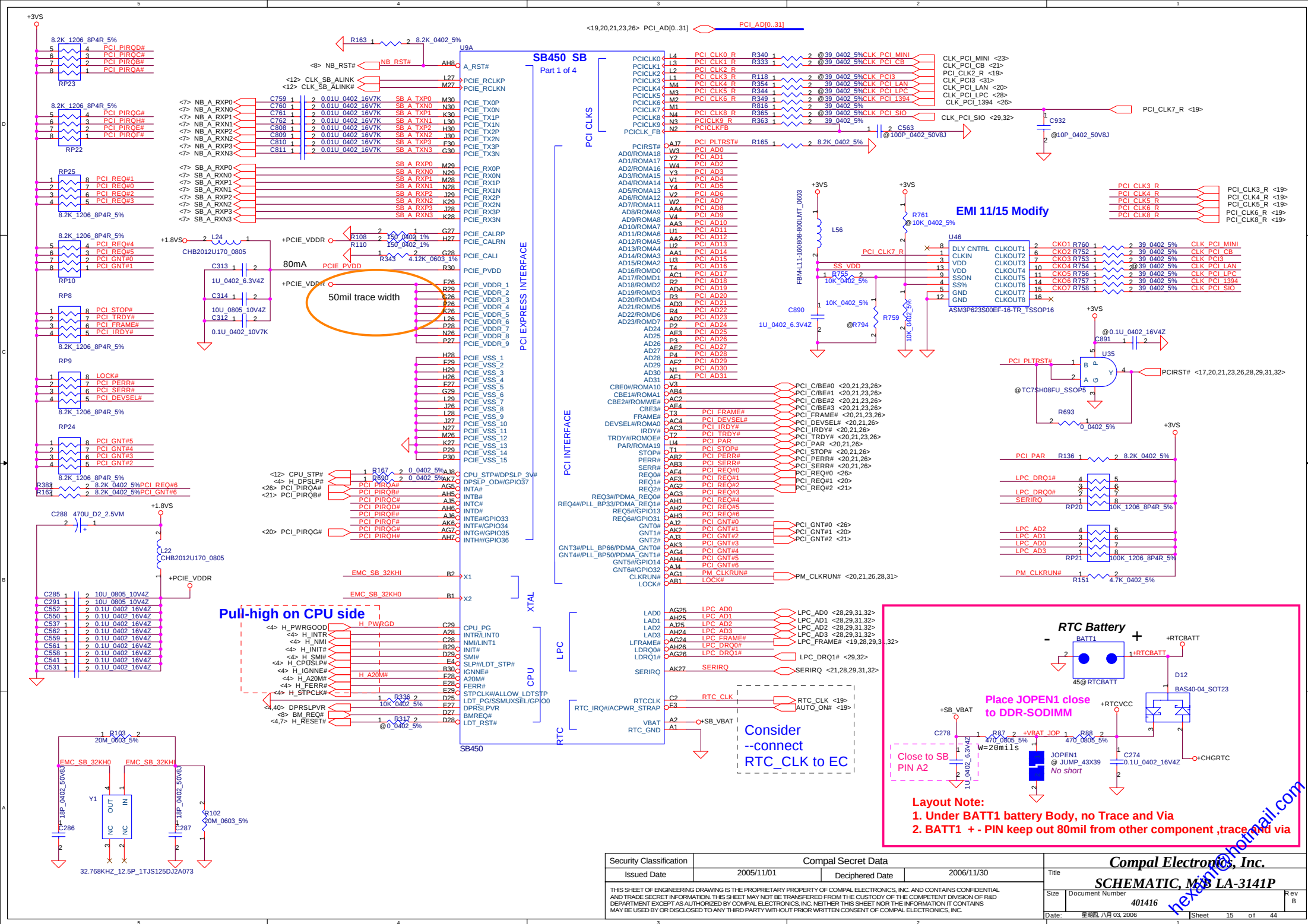


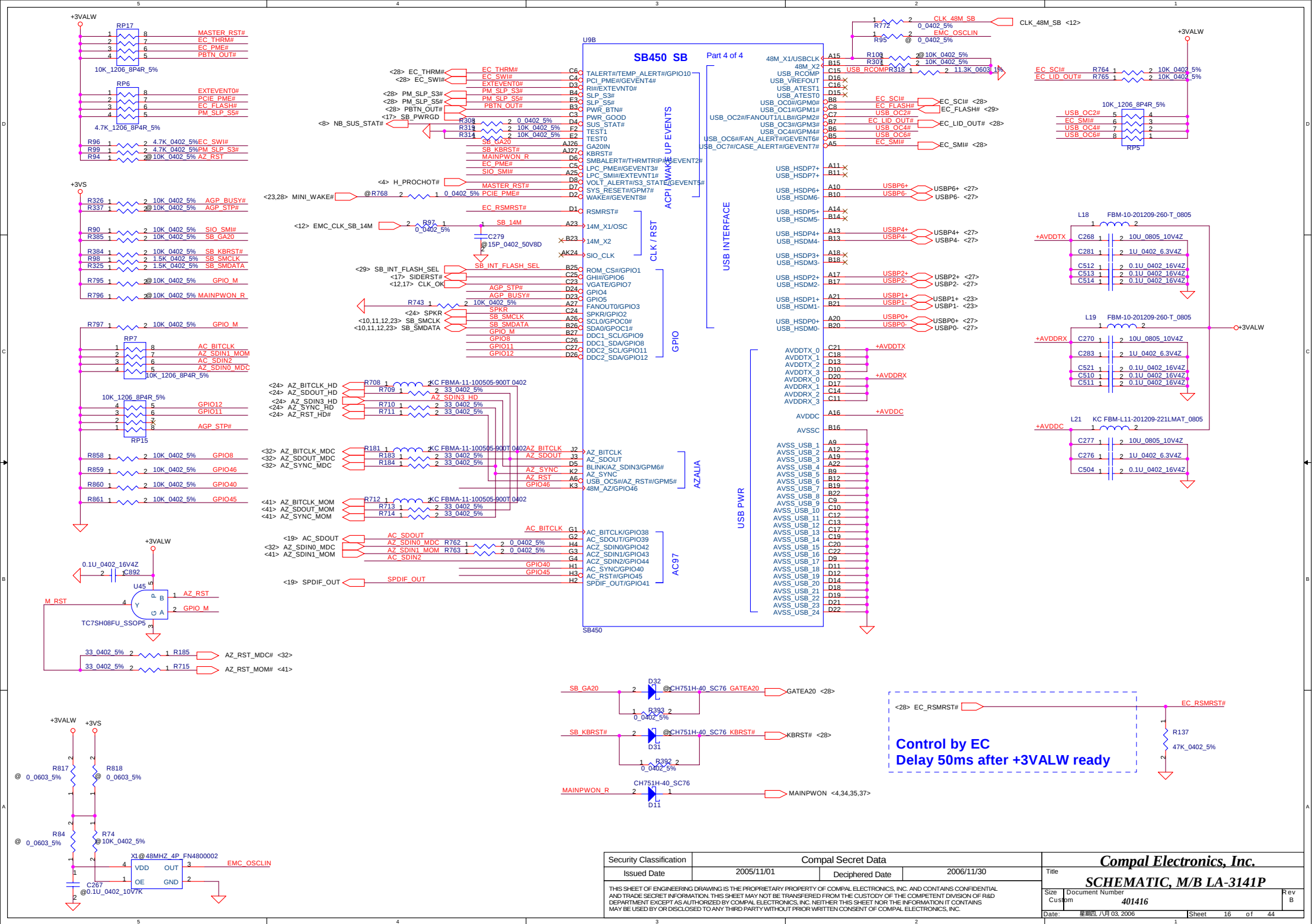
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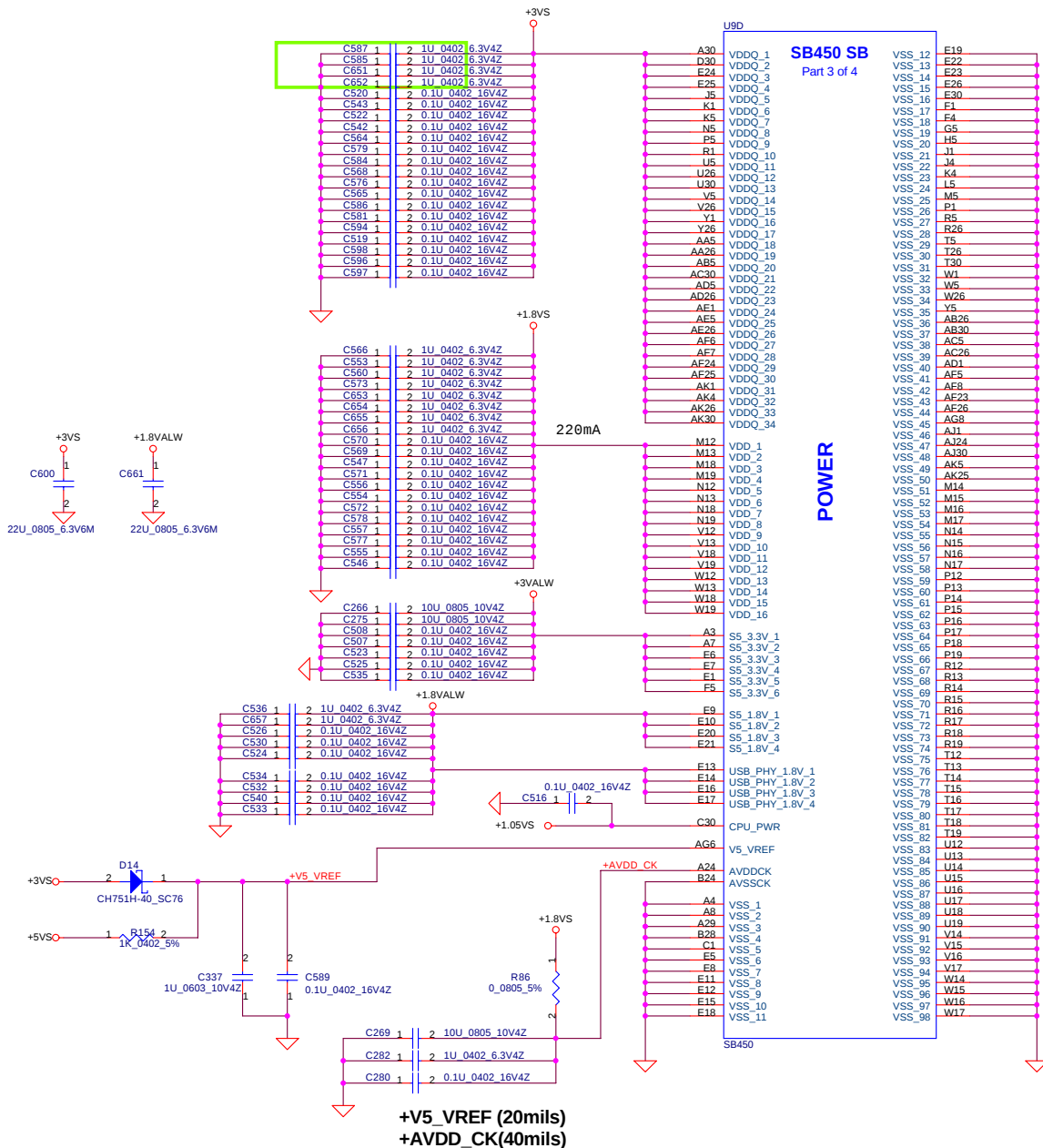
CRT CONNECTOR



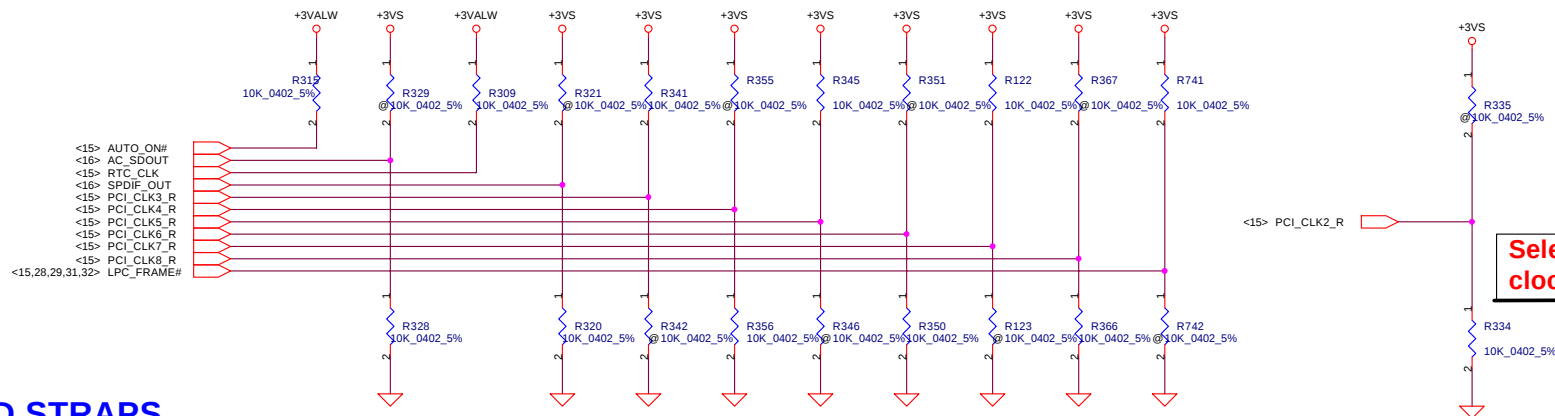
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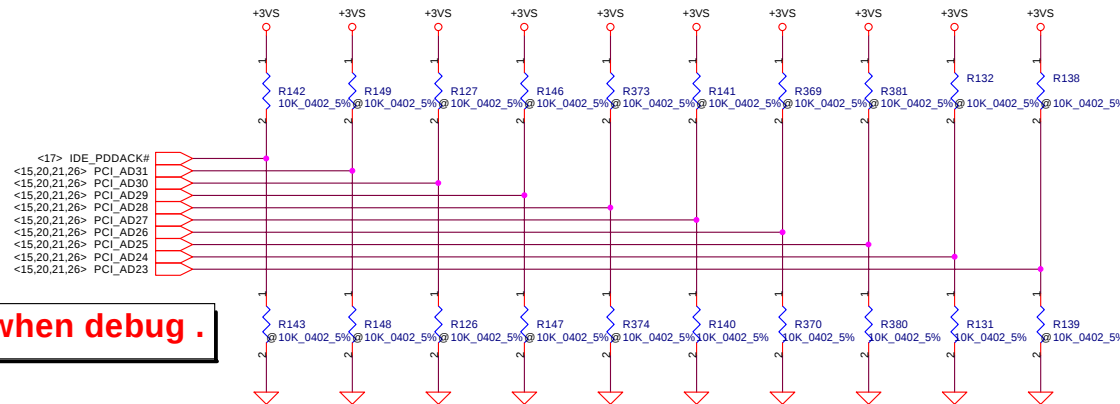
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REQUIRED STRAPS

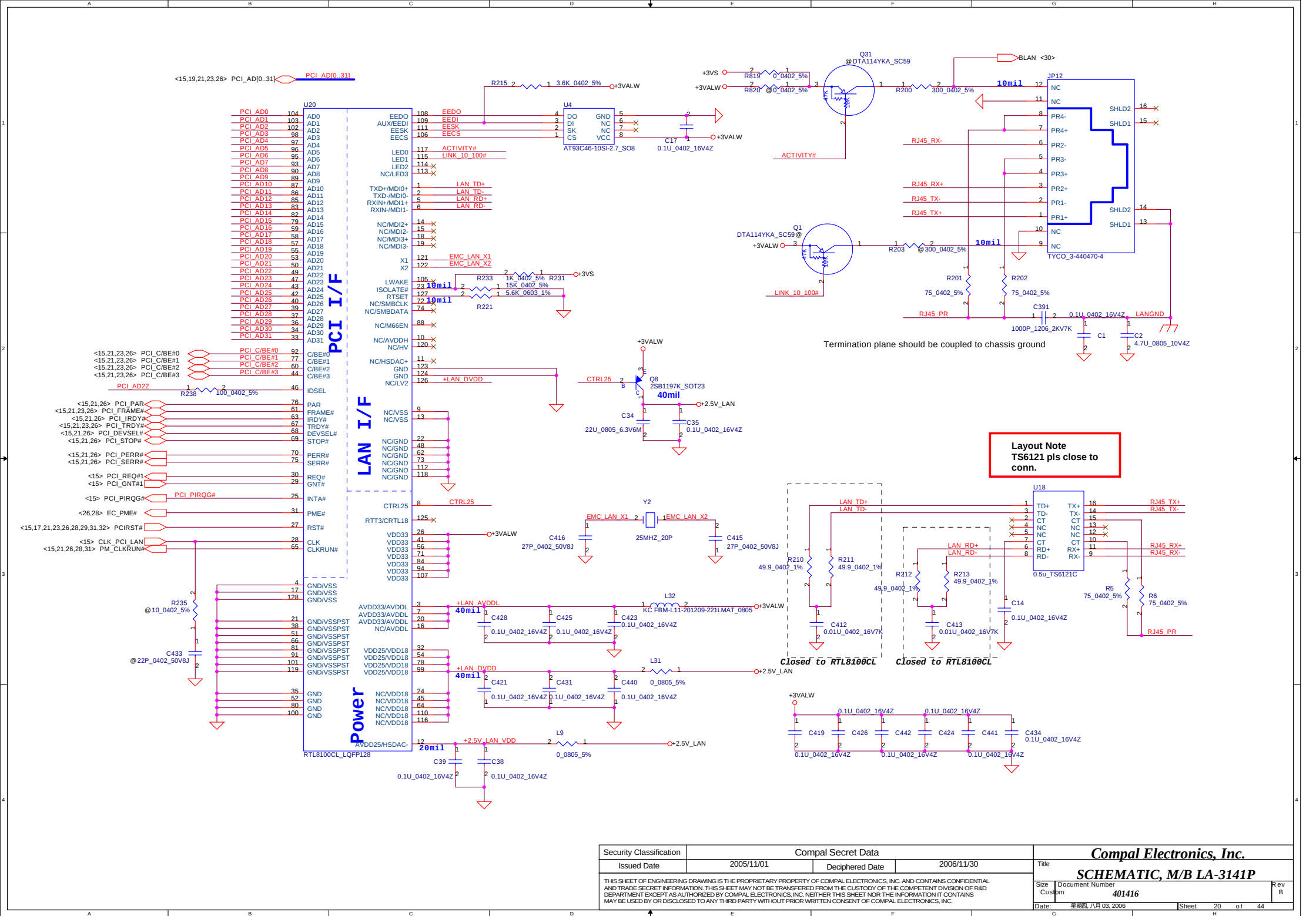


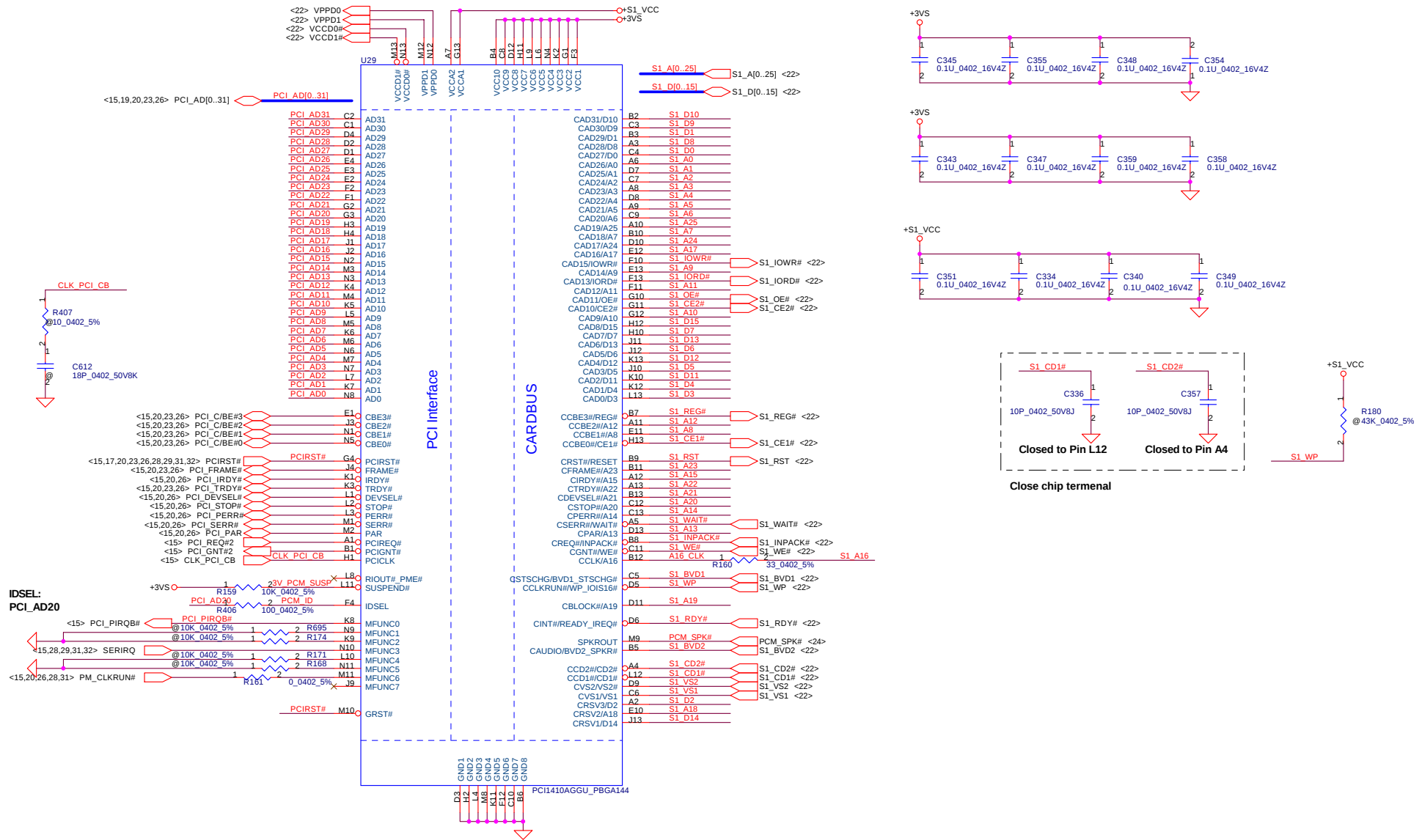
	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI4	CLK_PCI5	PCI_CLK6	PCI_CLK7	PCI_CLK8	LFRAME#	CLK_PCI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL	PCIE AUTO detect DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		THERMTRIP# ENABLE DEFAULT	Crystal Pad
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE	External Clock DEFAULT	Forcing PCIE to 2 lanes (debug only)	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		THERMTRIP# DISABLE	Clock input buffer DEFAULT



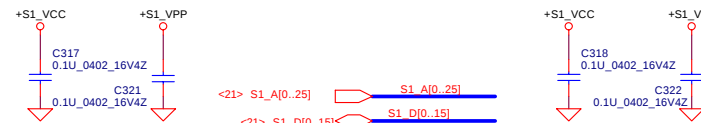
DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS	

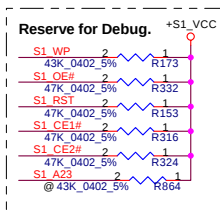
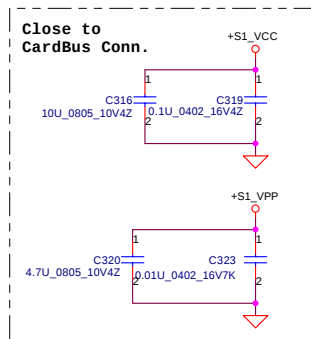
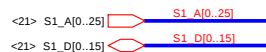
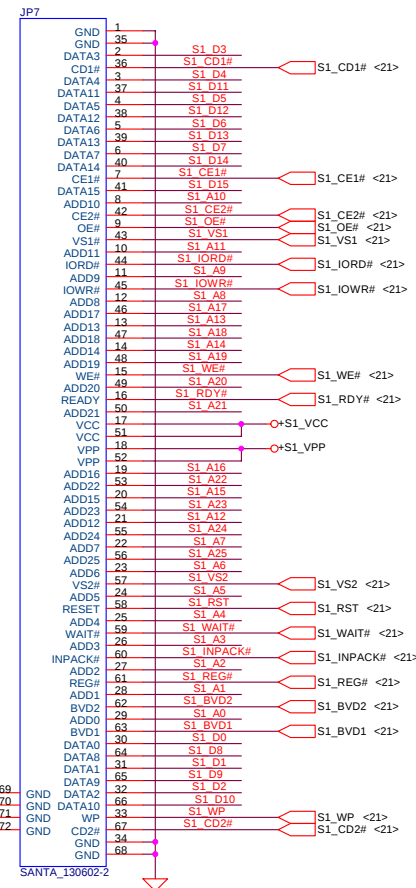


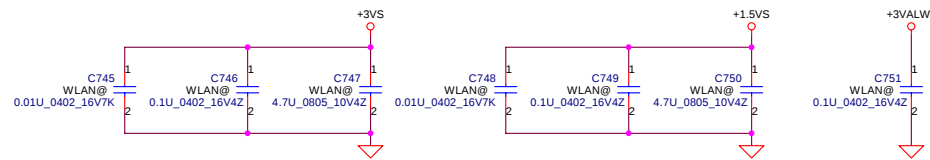


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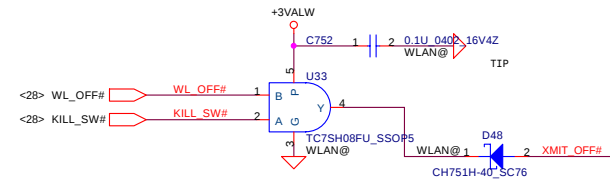
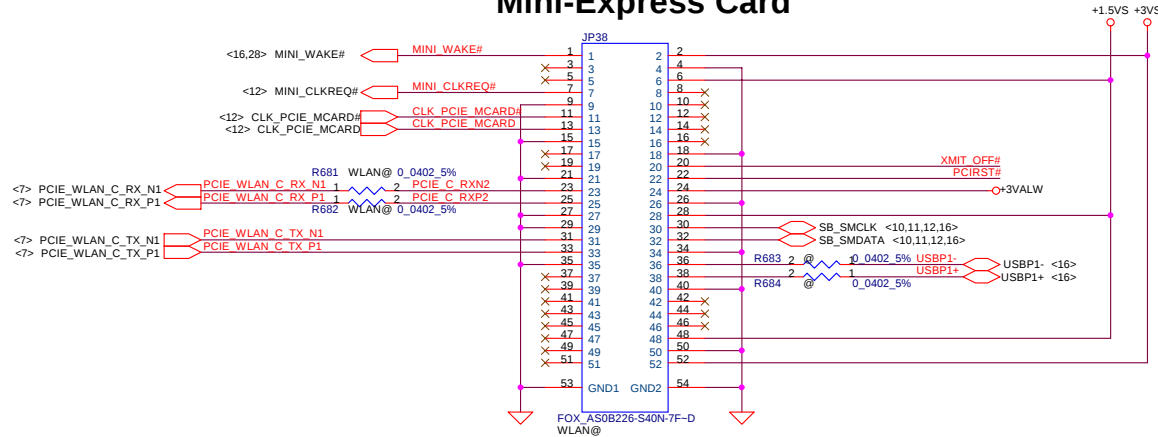


CardBus Socket

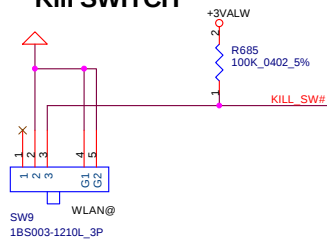




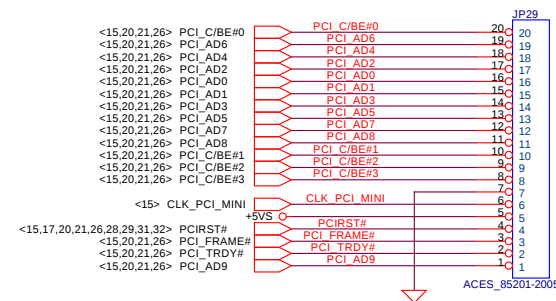
Mini-Express Card



Kill SWITCH

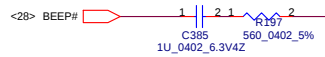


Port 80 Debug Card Connector



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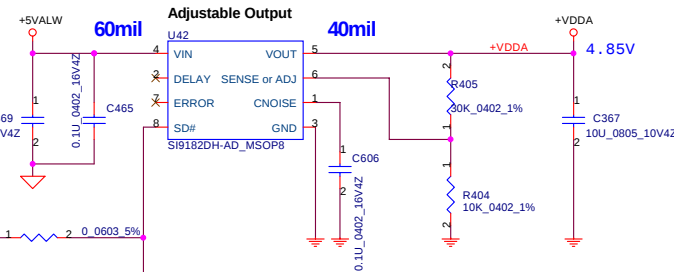
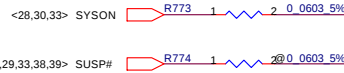
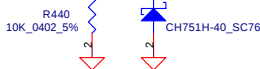
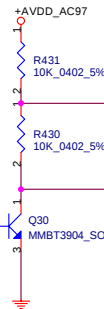
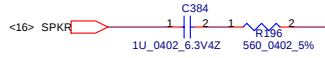
EC Bleep



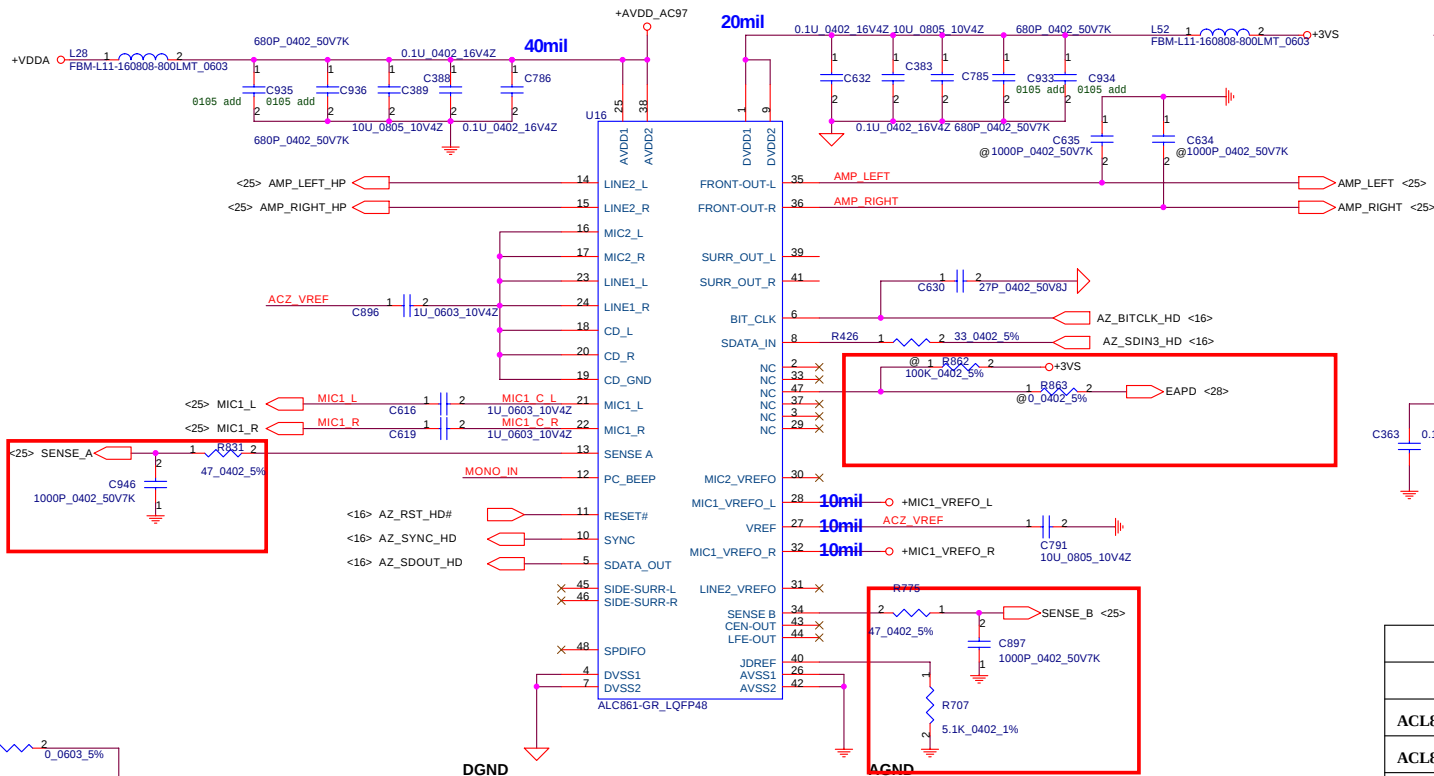
CardBus Bleep



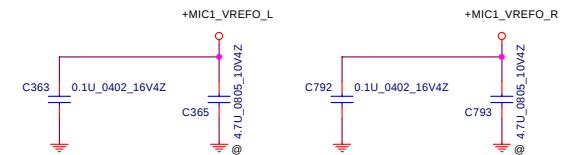
PCI Bleep



HD Audio Codec

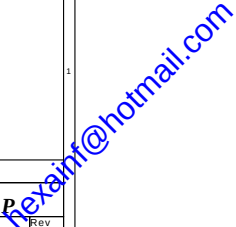


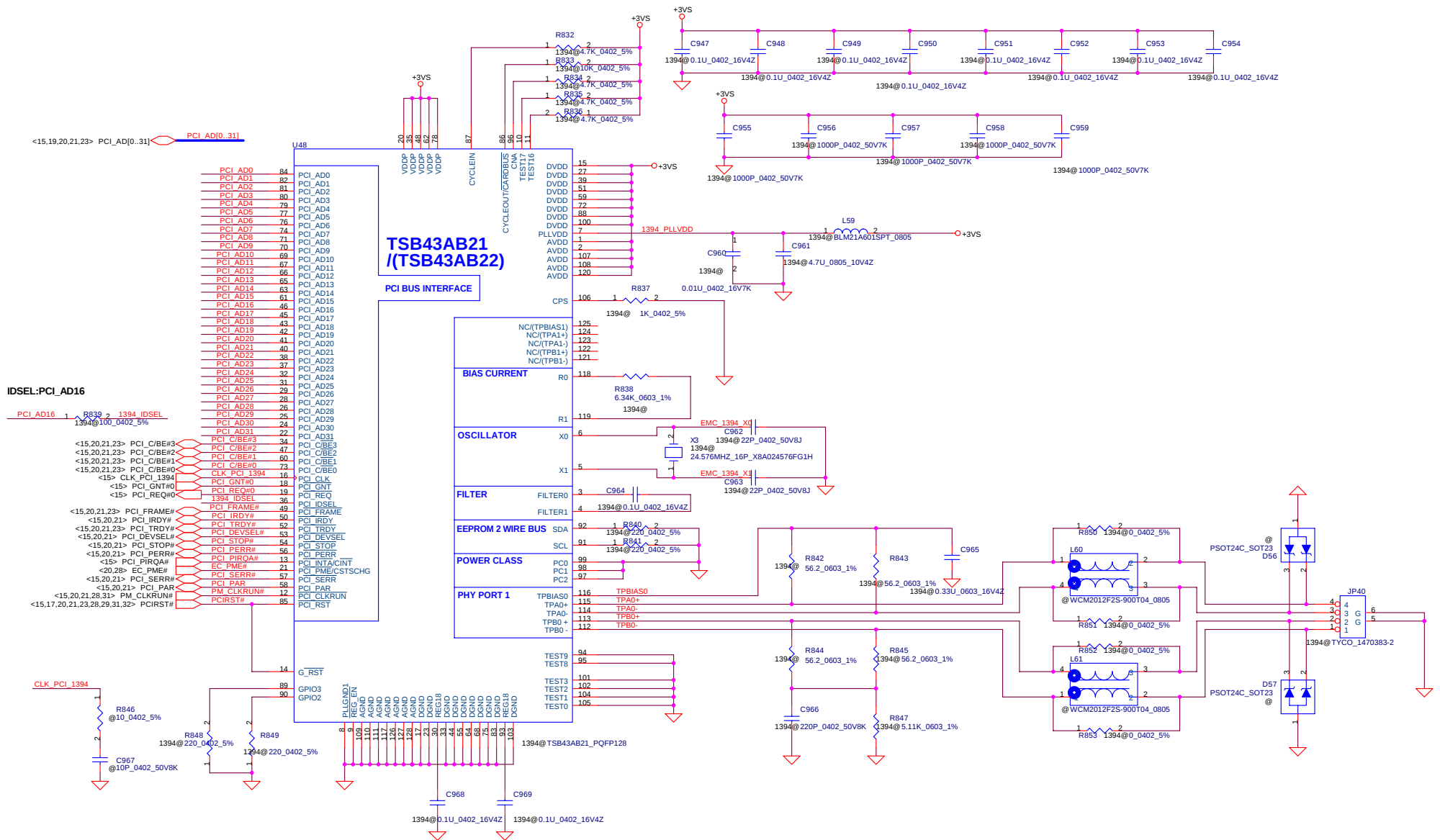
Analog Reference V



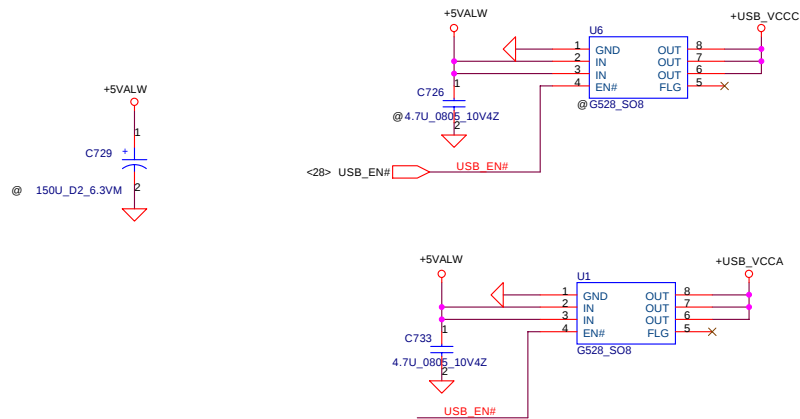
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	R813	C946	R775
ACL861 ver C	47 ohm	1000p F	47 ohm
ACL861 ver D	0 ohm	NC	0 ohm
ACL883	0 ohm	NC	0 ohm

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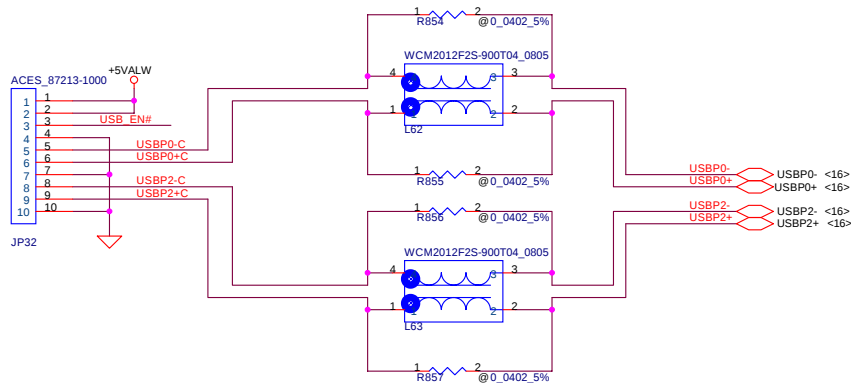




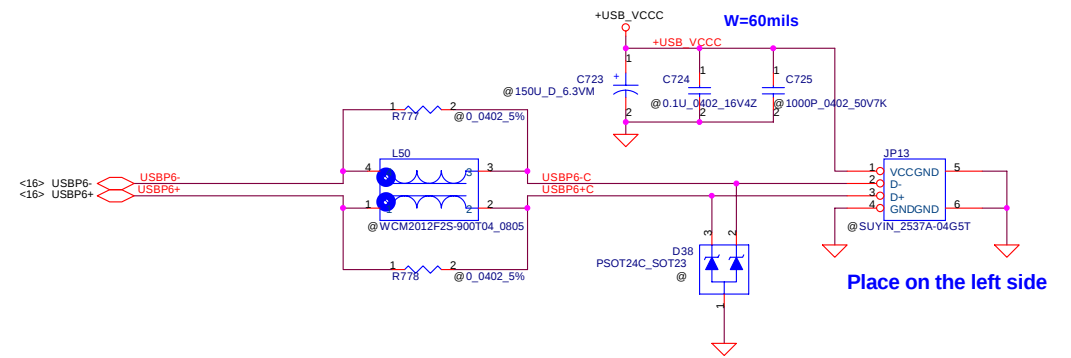
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2 port in right side

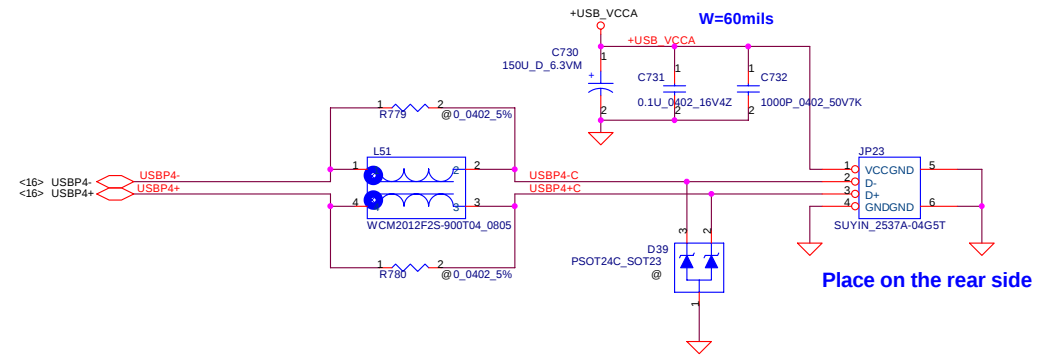


USB CONN. 1

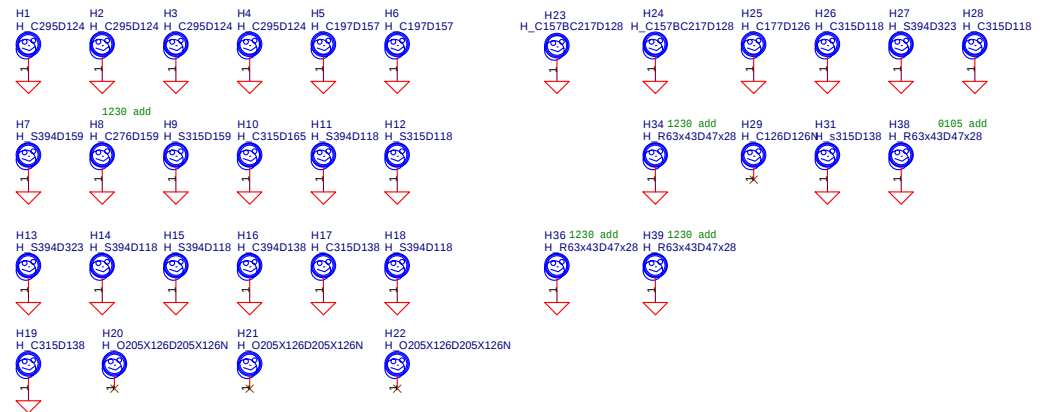
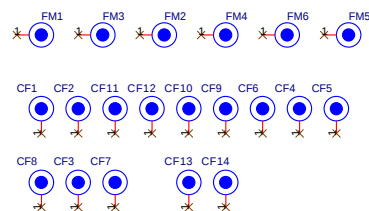


Place on the left side

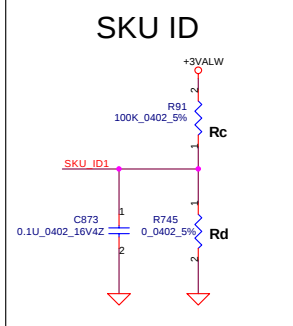
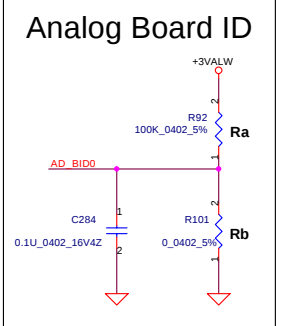
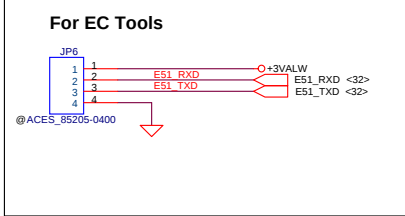
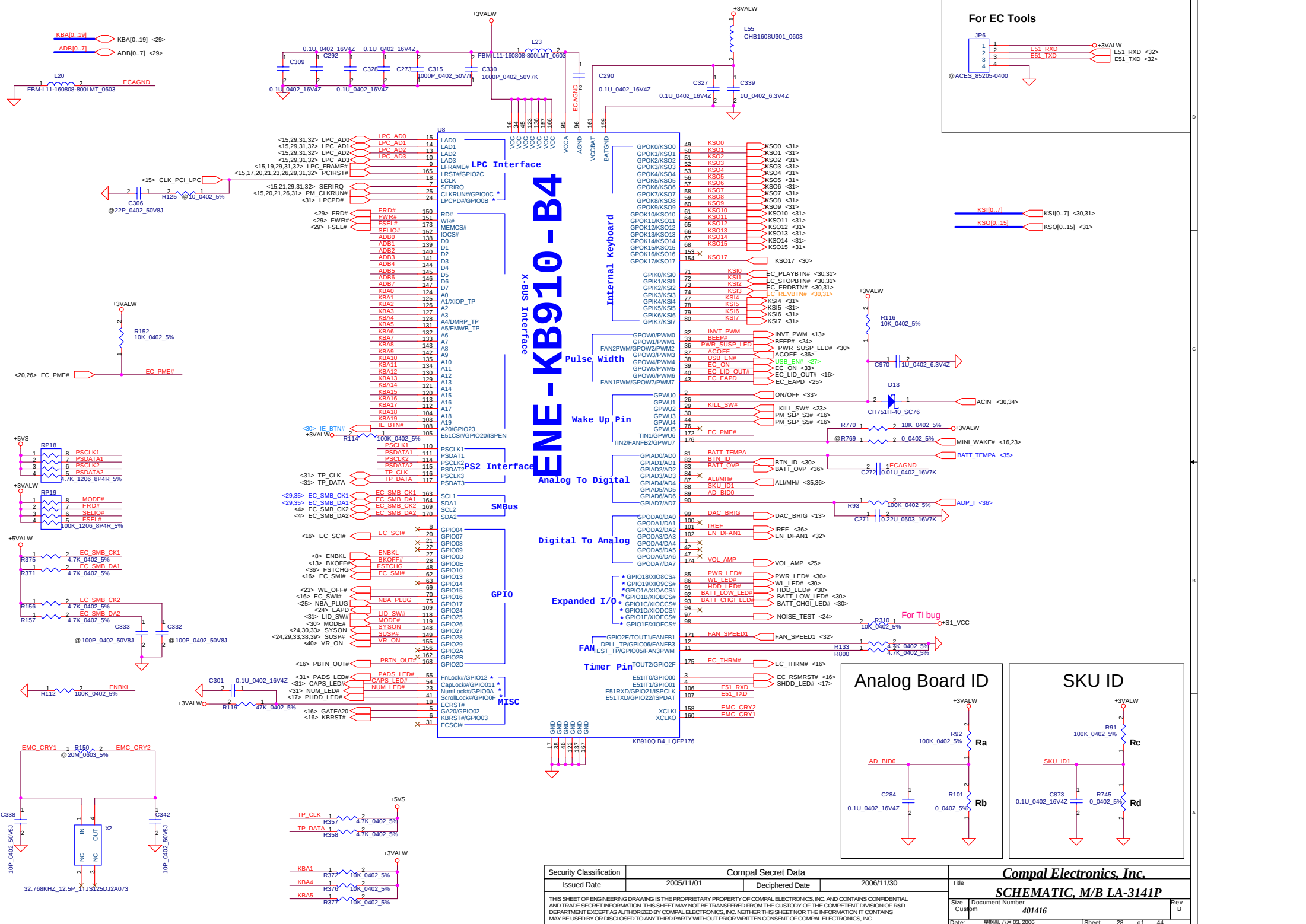
USB CONN.2



Place on the rear side

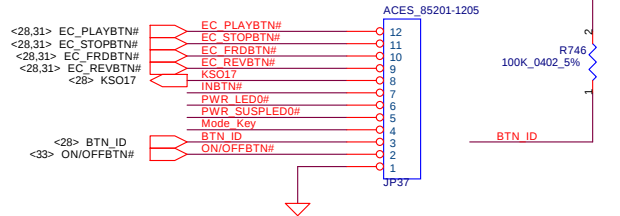


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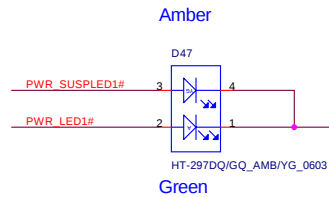
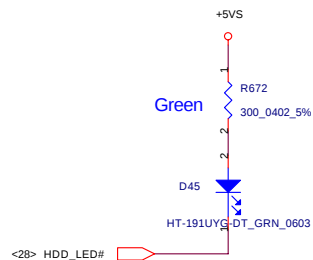
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PWR BTN/B

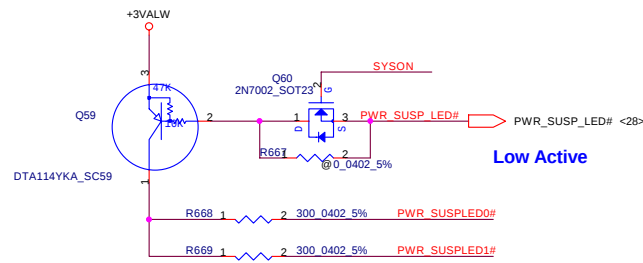
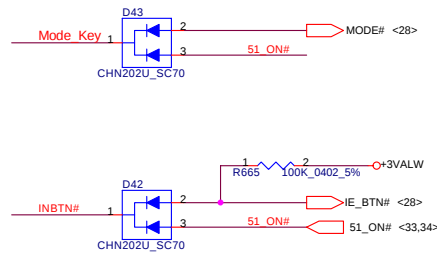


EC_PLAYBTN#	C874	100P_0402_25V8K
EC_STOPBTN#	C875	100P_0402_25V8K
EC_FRDBTN#	C876	100P_0402_25V8K
EC_REVBTN#	C877	100P_0402_25V8K
KSO17	C878	100P_0402_25V8K
INBTN#	C879	100P_0402_25V8K
PWR_LED0#	C880	100P_0402_25V8K
PWR_SUSPLED0#	C881	100P_0402_25V8K
Mode_Key	C882	100P_0402_25V8K
BTN_ID	C883	120P_0402_25V8K
ON/OFFBTN#	C884	120P_0402_25V8K

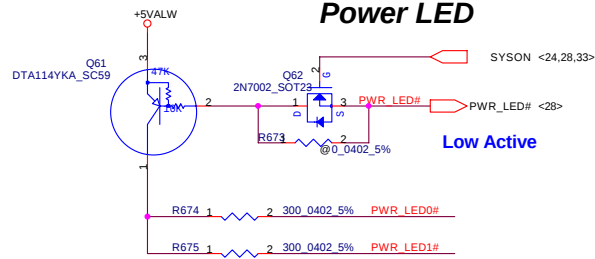
HDD LED



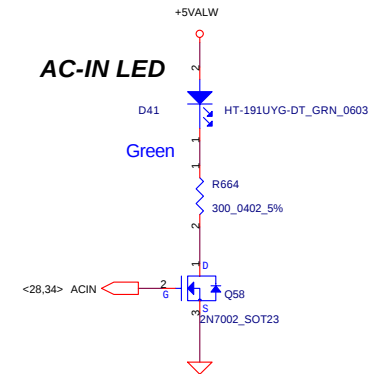
Vivace Button



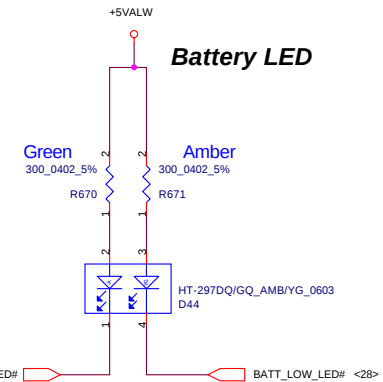
Power LED



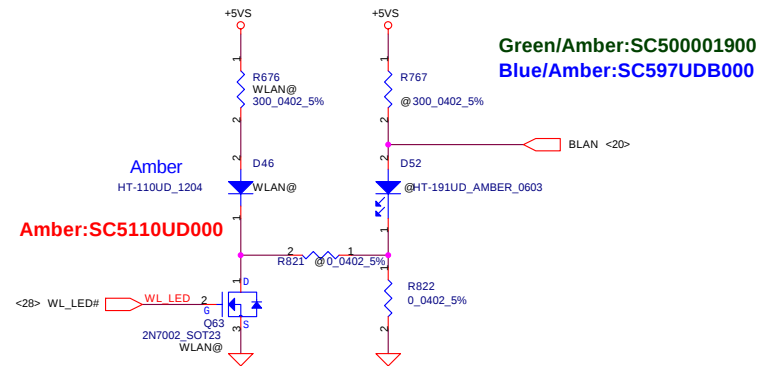
AC-IN LED



Battery LED

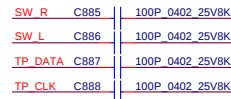
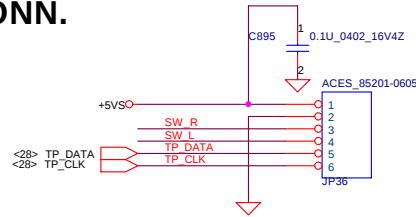


Wireless Lan LED

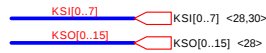
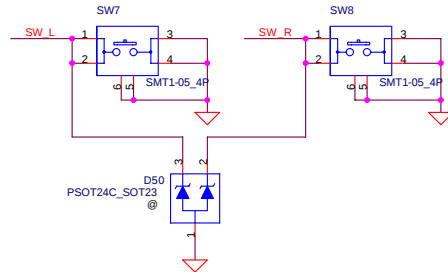


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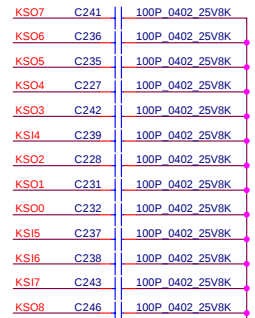
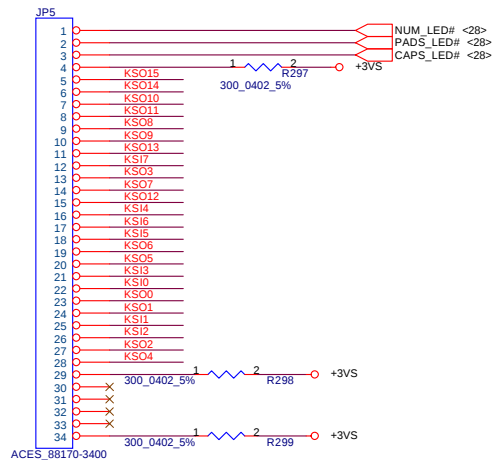
TP CONN.



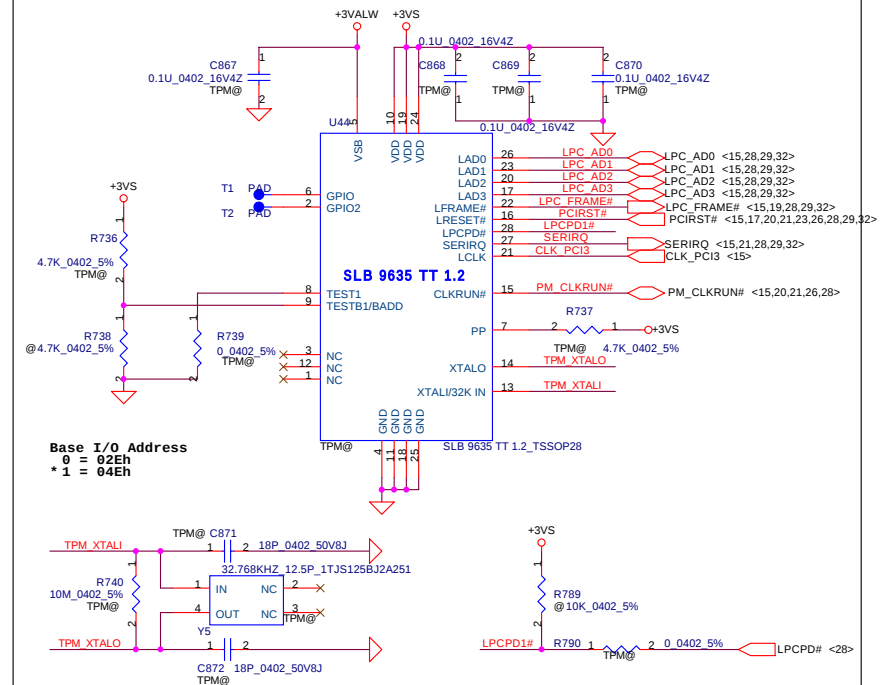
TP Button



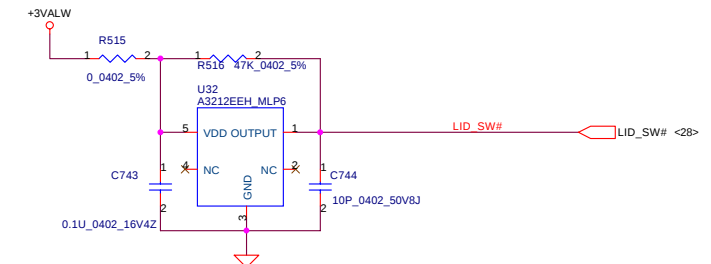
INT_KBD CONN.



TPM1.2 on board

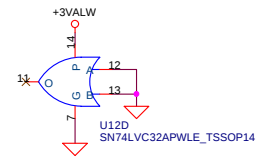
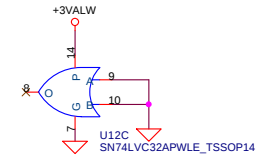
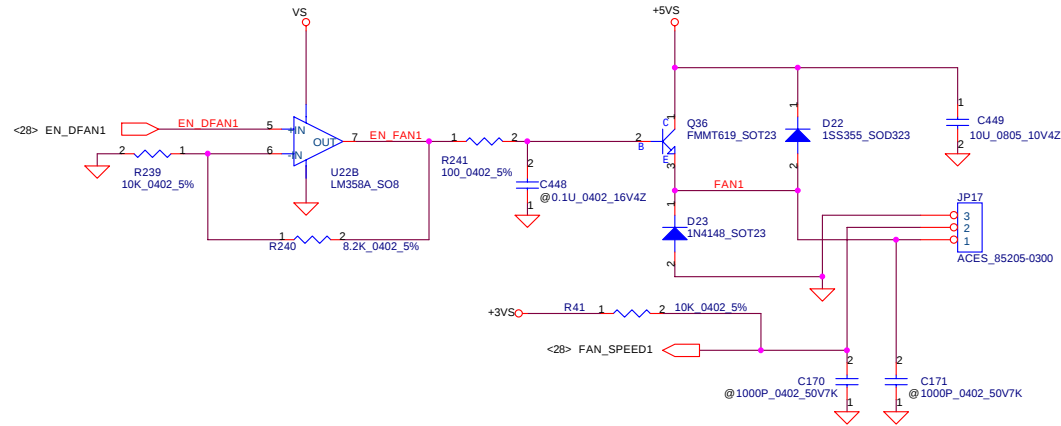


Lid Switch



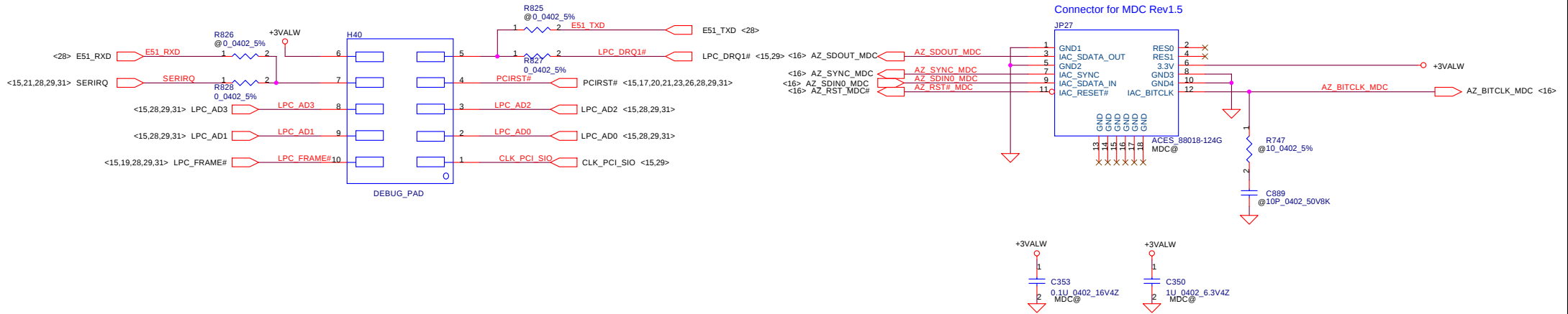
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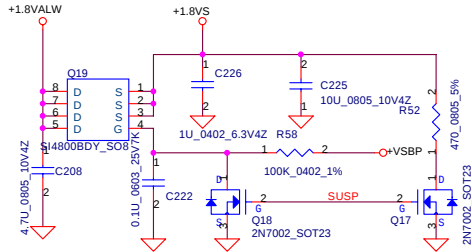
MDC CONN.

Connector for MDC Rev1.5

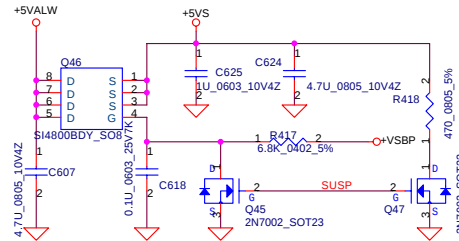


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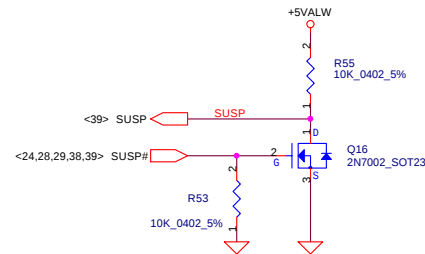
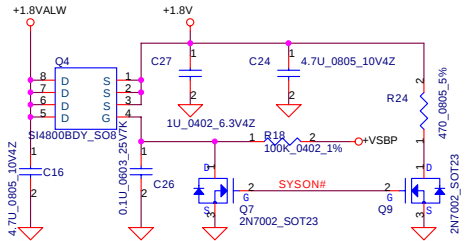
+1.8VALW TO +1.8VS



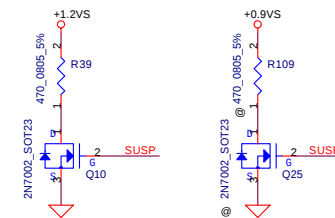
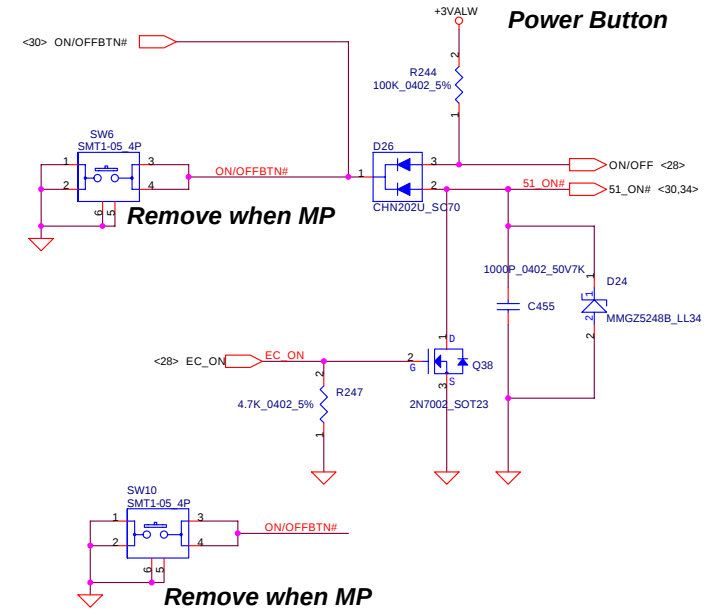
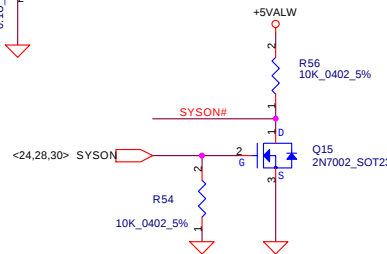
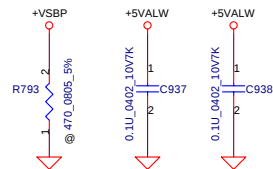
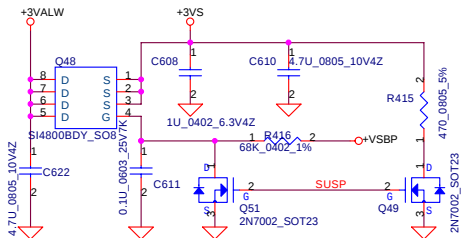
+5VALW TO +5VS



+1.8VALW TO +1.8V

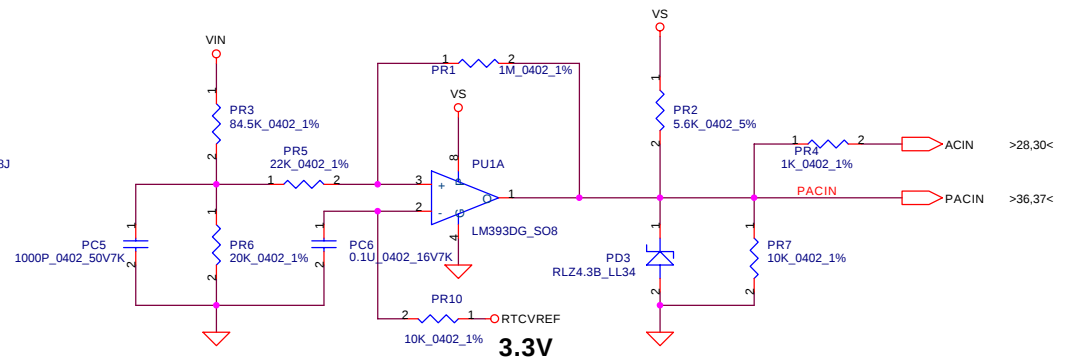
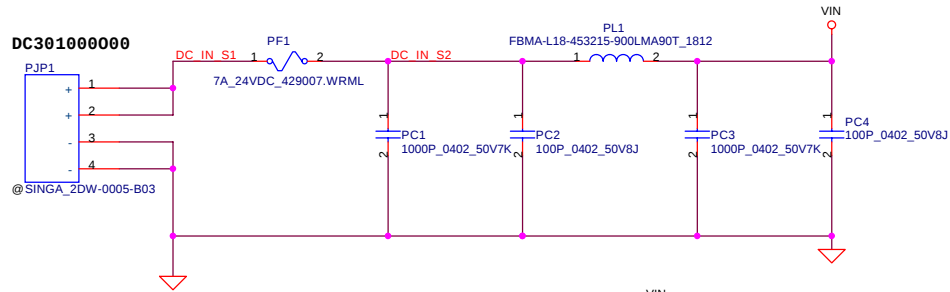


+3VALW TO +3VS

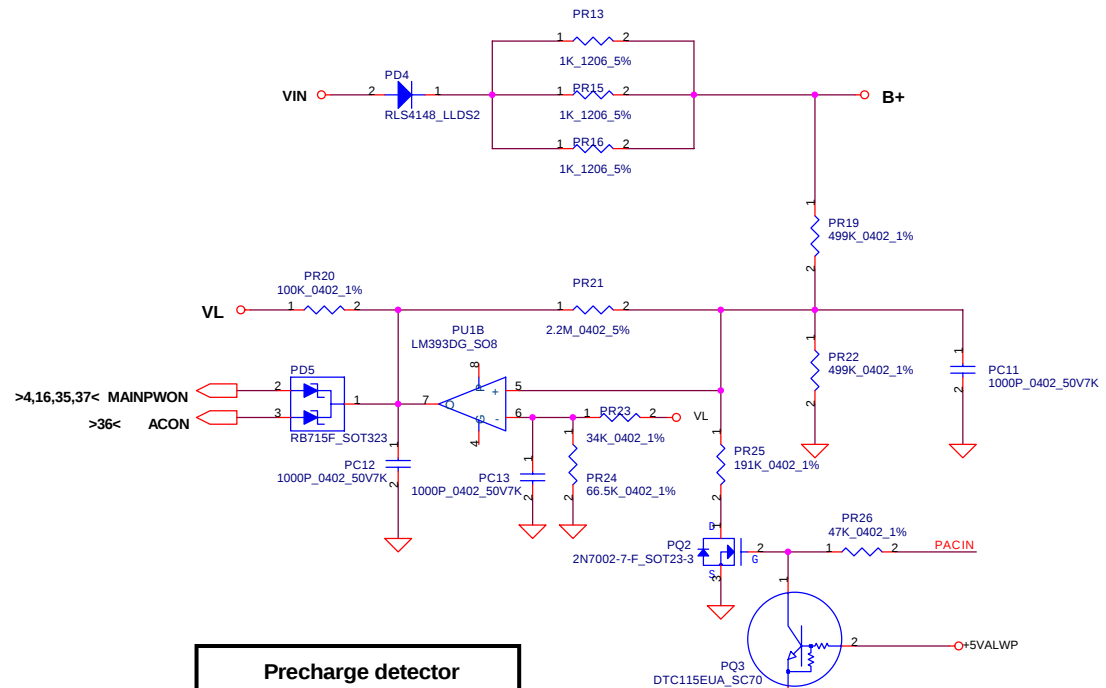
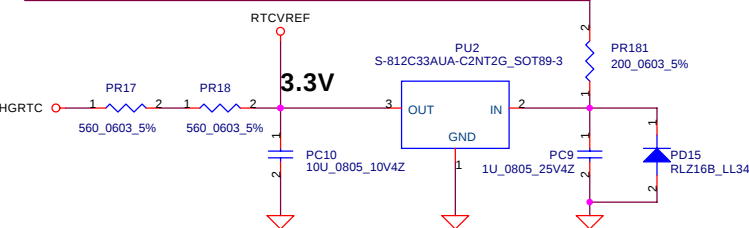
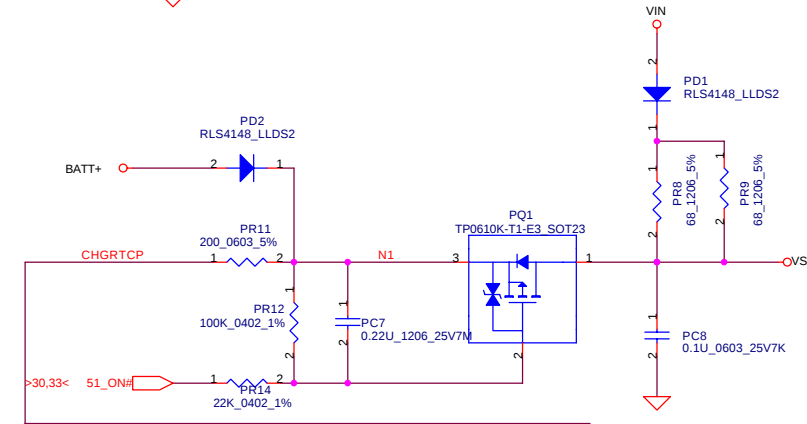


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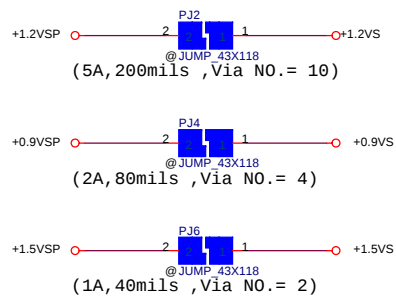
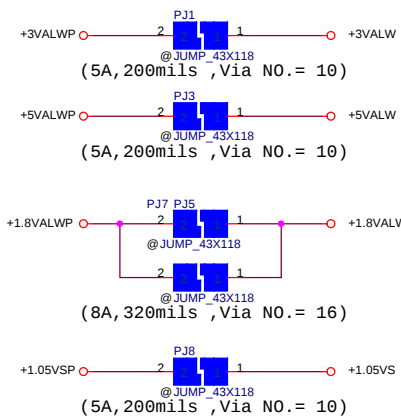
DC301000000



Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976

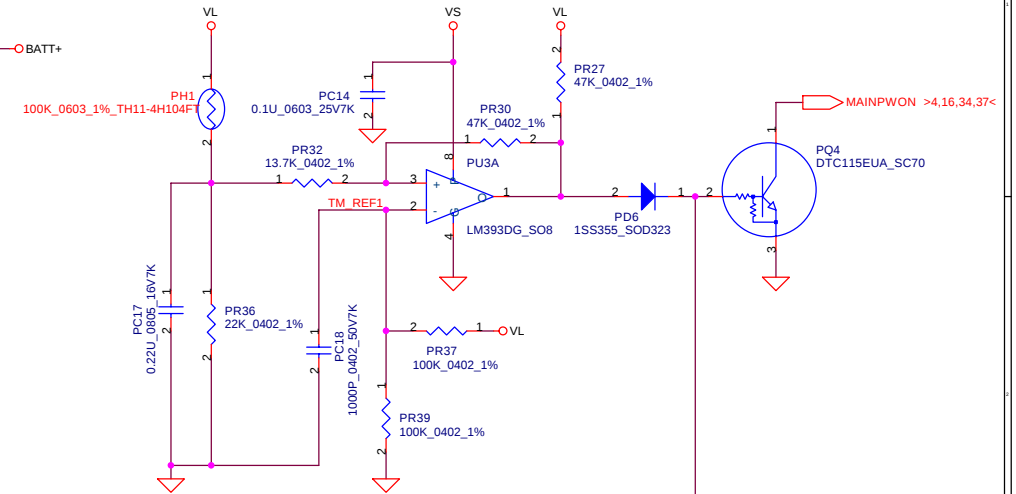
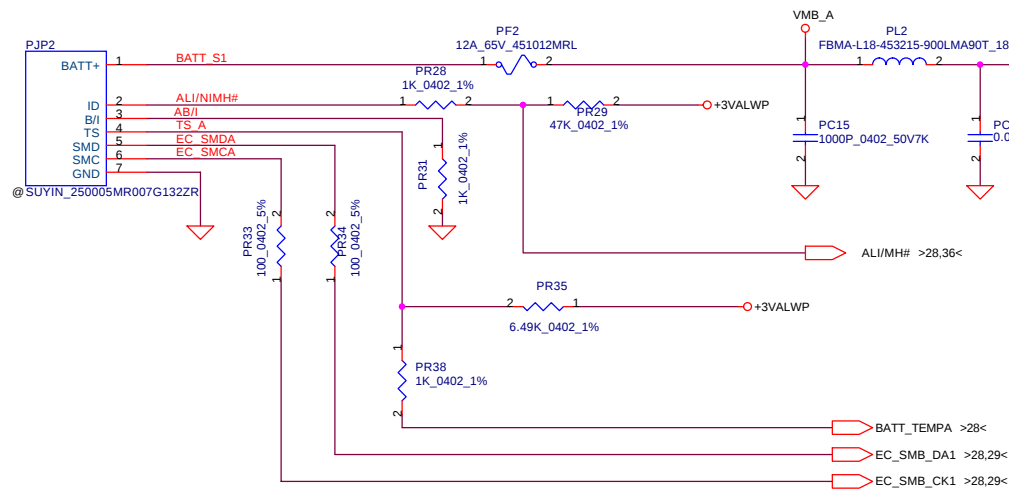


Precharge detector
 15.97V/14.84V FOR
 ADAPTOR

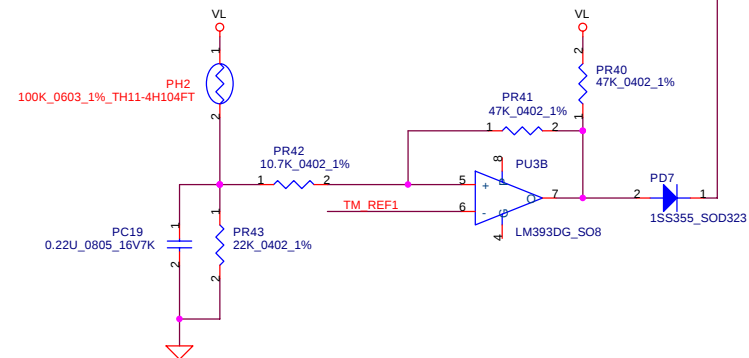
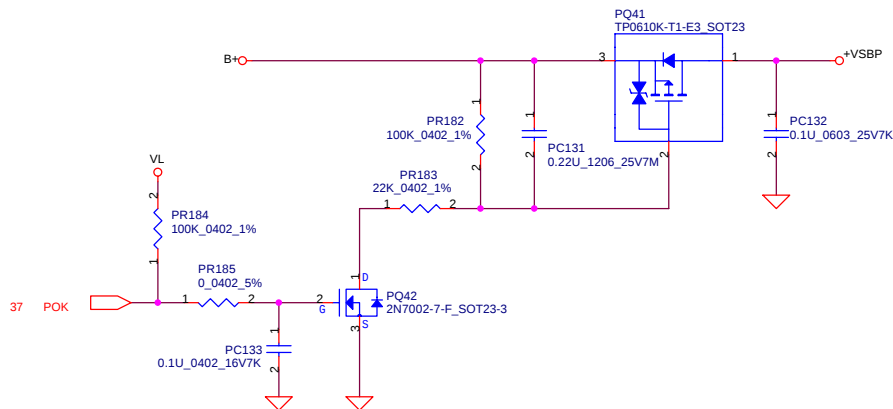


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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

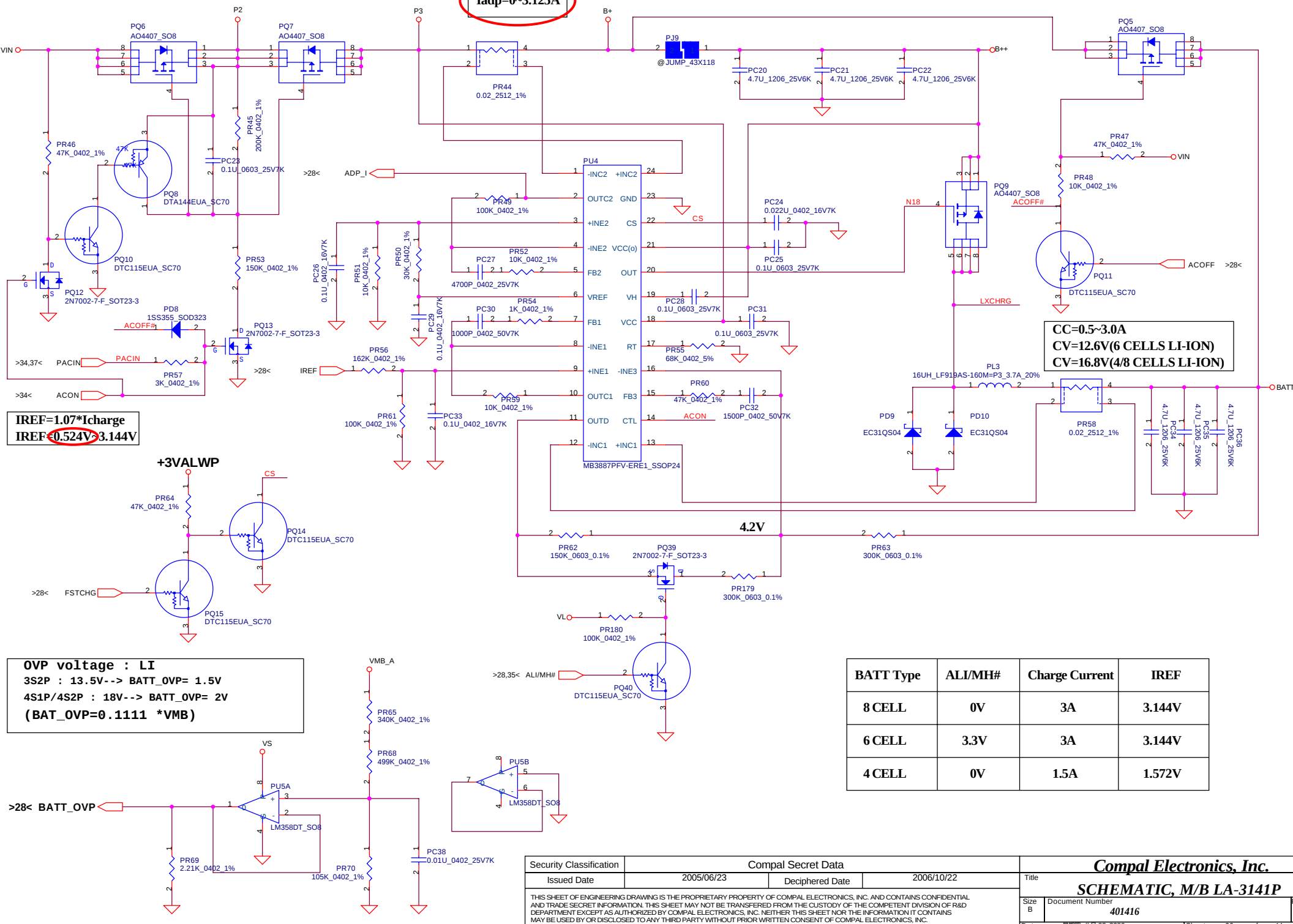


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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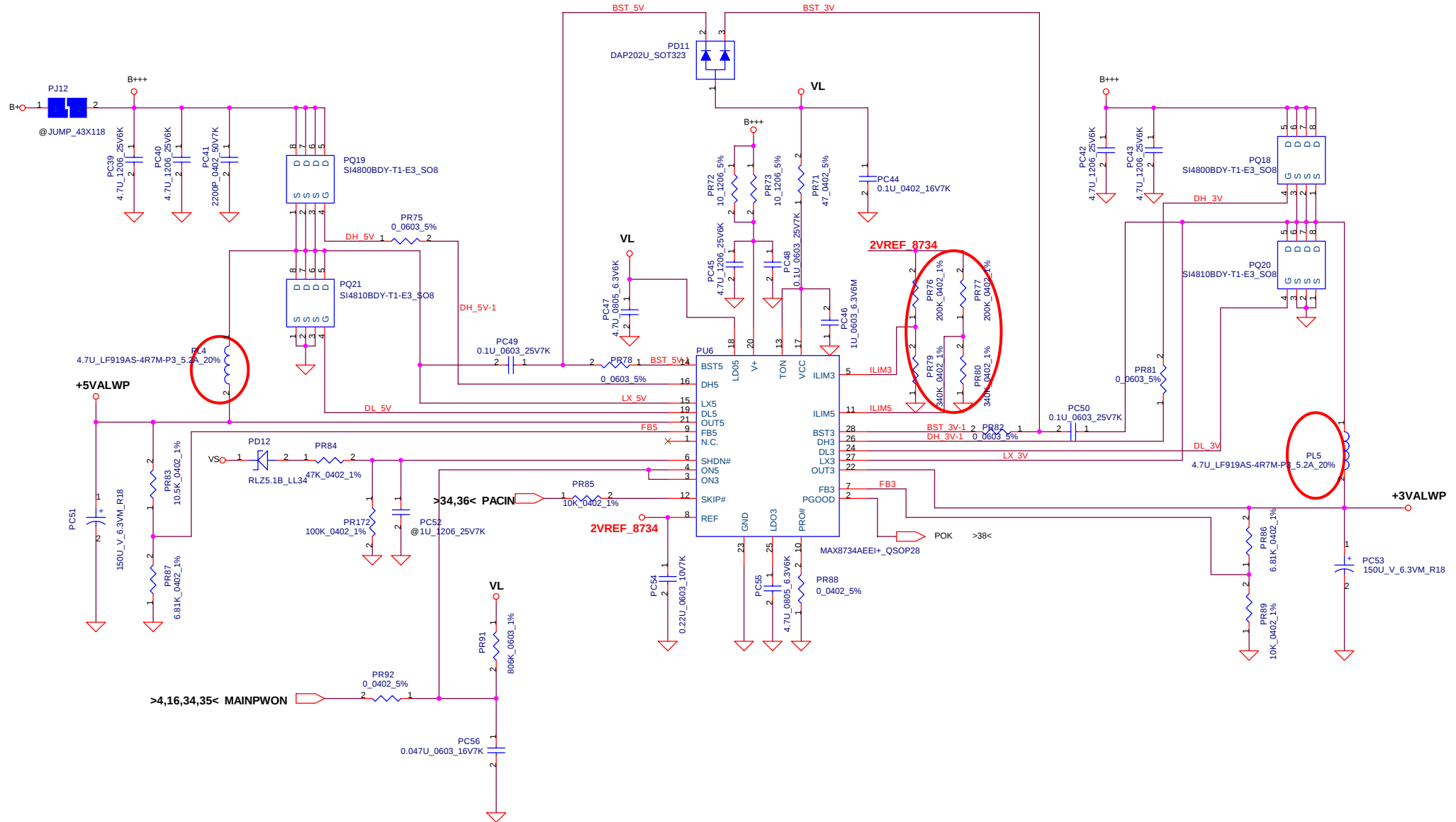


IREF=1.07*Icharge
IREF=0.524V>3.144V

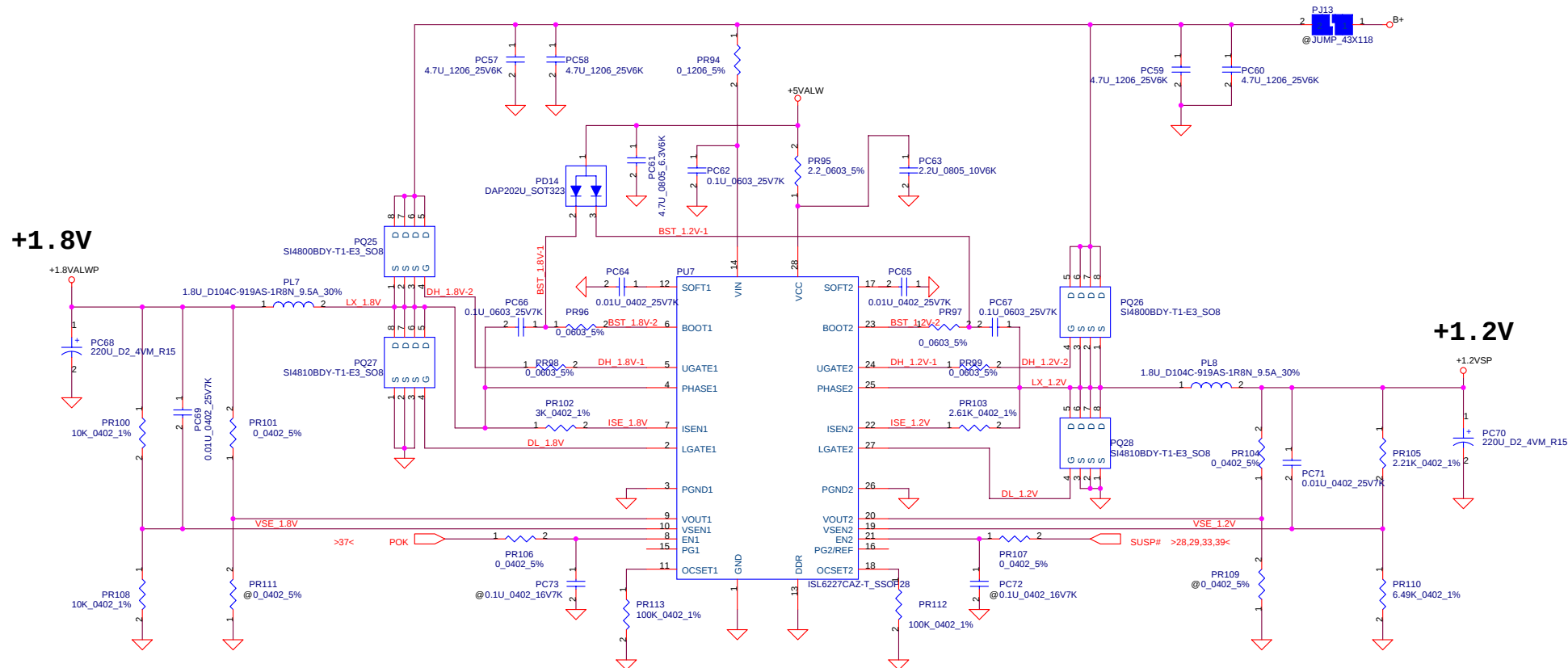
OVP voltage : LI
3S2P : 13.5V--> BATT_OVP= 1.5V
4S1P/4S2P : 18V--> BATT_OVP= 2V
(BATT_OVP=0.1111 *VMB)

BATT Type	ALI/MH#	Charge Current	IREF
8 CELL	0V	3A	3.144V
6 CELL	3.3V	3A	3.144V
4 CELL	0V	1.5A	1.572V

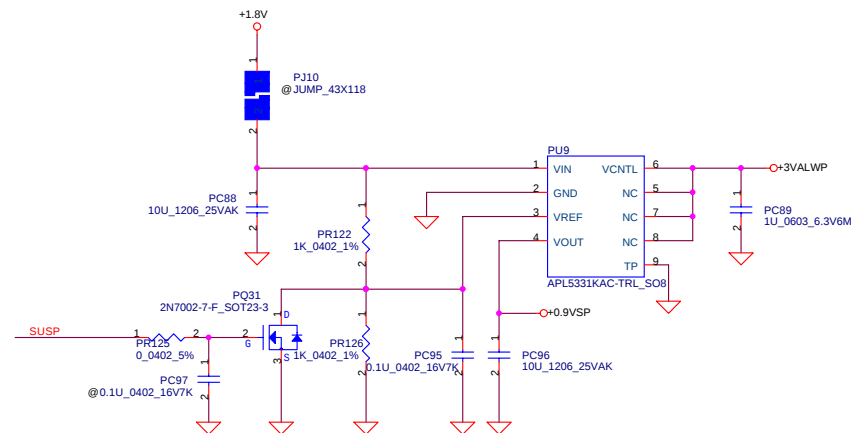
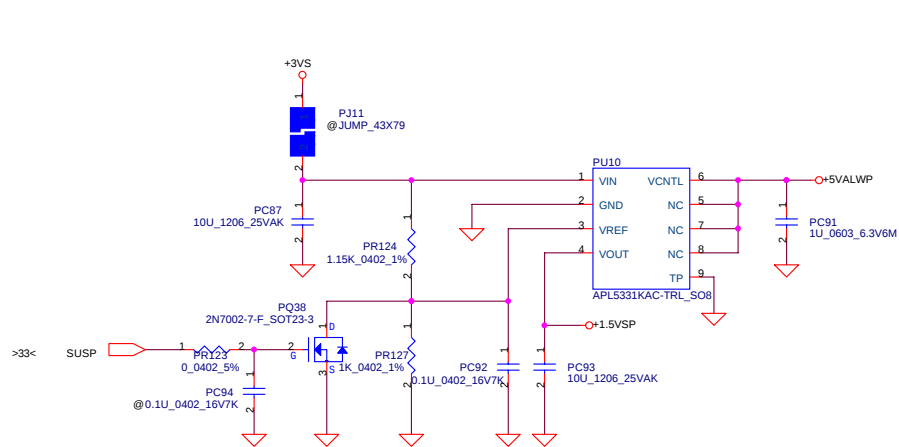
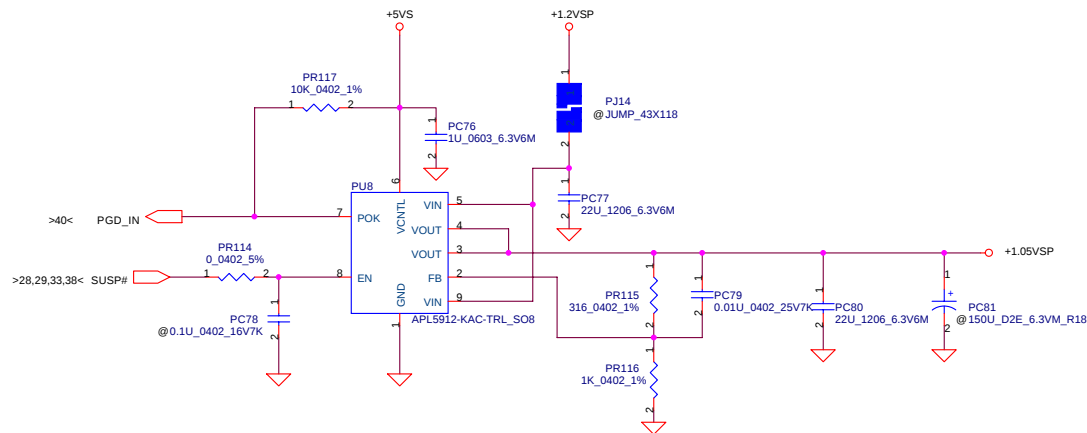
+3.3VALWP/+5VALWP



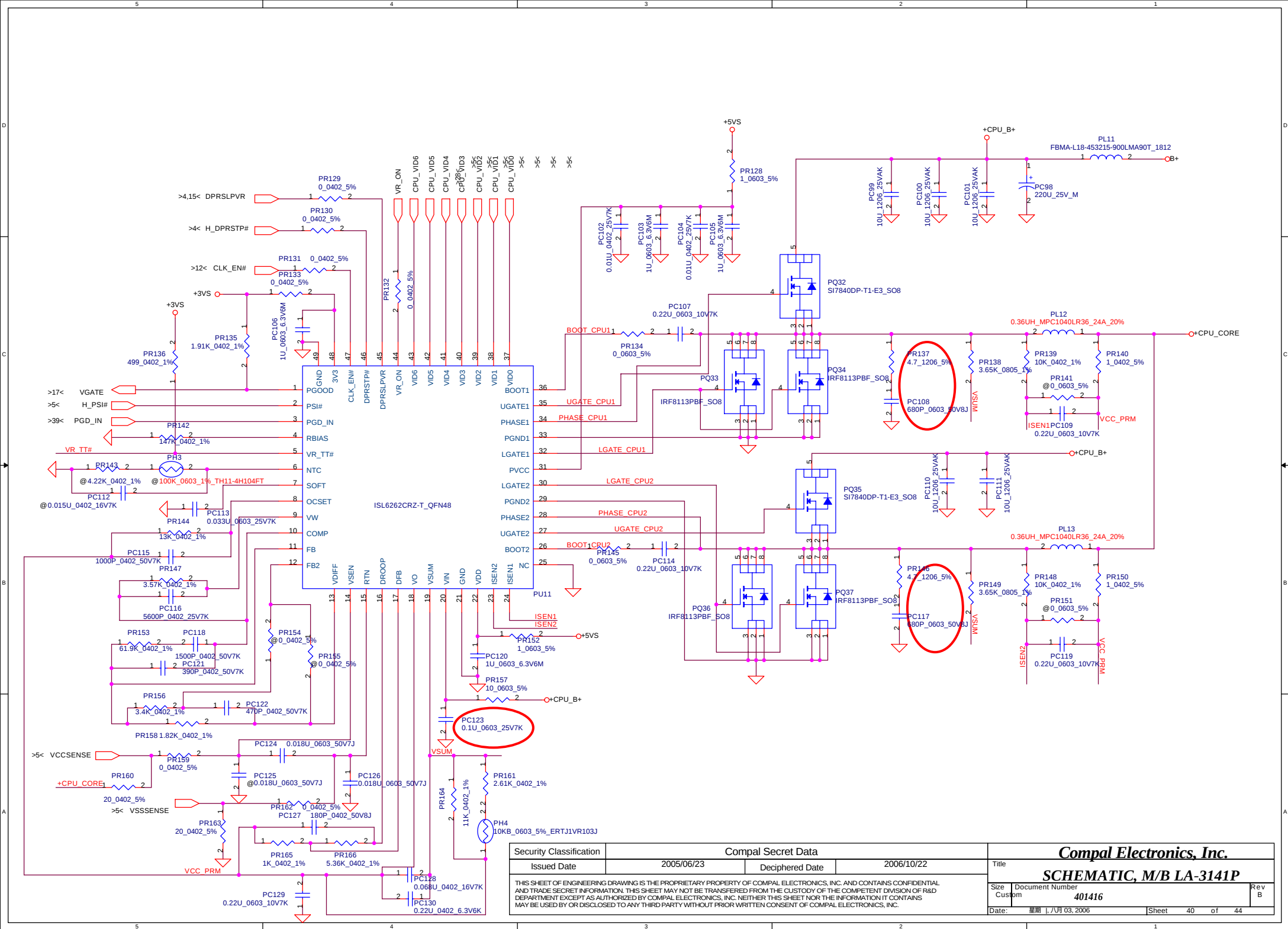
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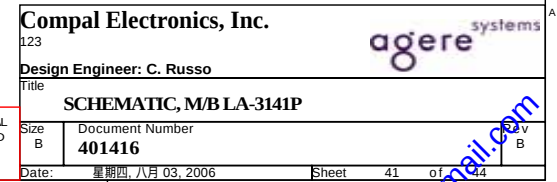


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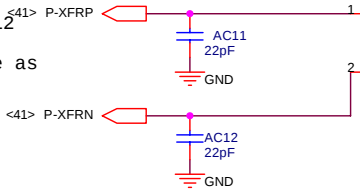




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Locate C11, C12^{<41>} as close to digital device as possible.



FUSE Note:
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.

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Design Engineer: R. Trevino		
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HW4 Product Improvement Record (P.I.R.)

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POWER PIR LIST

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Reason for change

Modify list

PVT

37	Change 3V/5V OCP point and choke	Change PR76,PR77 to 200K; PR79,PR80 to 340K; PL4,PL5 to 4.7U
40	For EMI request to reduce CPU power board band	Add snuber PR137,PR146(4.7ohm), PC108,PC117(680p)

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