

Compal Confidential

Everest Schematics Document

Intel Merom Processor with Calistoga + DDRII + ICH7M

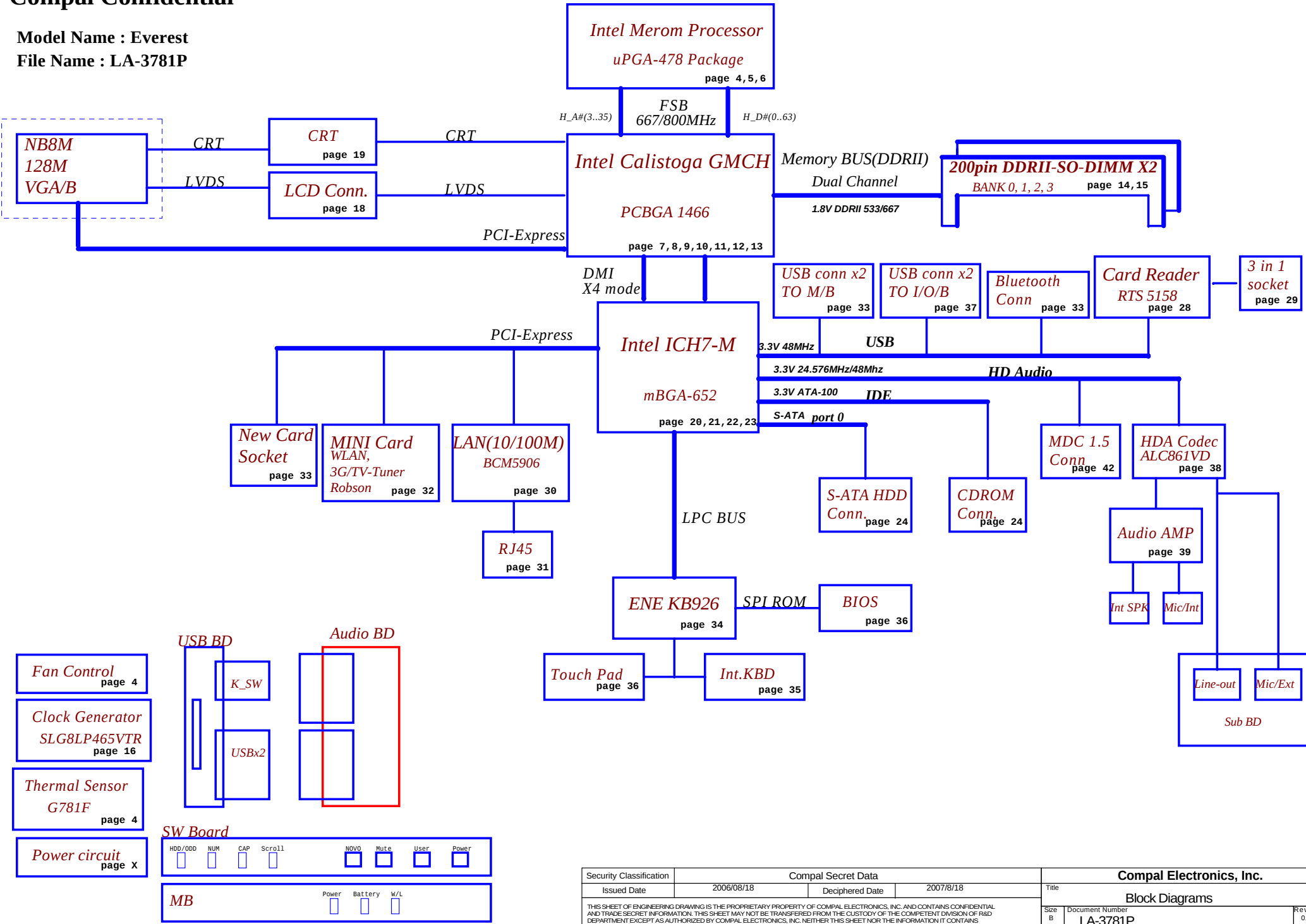
2007 - 05 - 15

REV: 1.0

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Model Name : Everest
File Name : LA-3781P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	CLock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

	ID	BRD ID	R54/42(Rb)	Vab
IHL00	0	R01 (EVT)	0	0V
	1	R02 (DVT)	8.2K	0.25V
	2	R03 (PVT)	18K	0.50V
	3	R10A (MP)	33K	0.82V
IGT30	4	R01 (EVT)	56K	1.19V
	5	R02 (DVT)	100K	1.65V
	6	R03 (PVT)	200K	2.20V
	7	R10A (MP)	NC	3.30V

PANEL ID Table

ID	UMA_DES	Vab
0	IHL00/IGT30 UMA	3.30V
1	IHLV3 UMA	2.20V
2		
3		
4		
5		
6	IHLV2 VGA	0.25V
7	IHL00/IGT30 VGA	0V

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

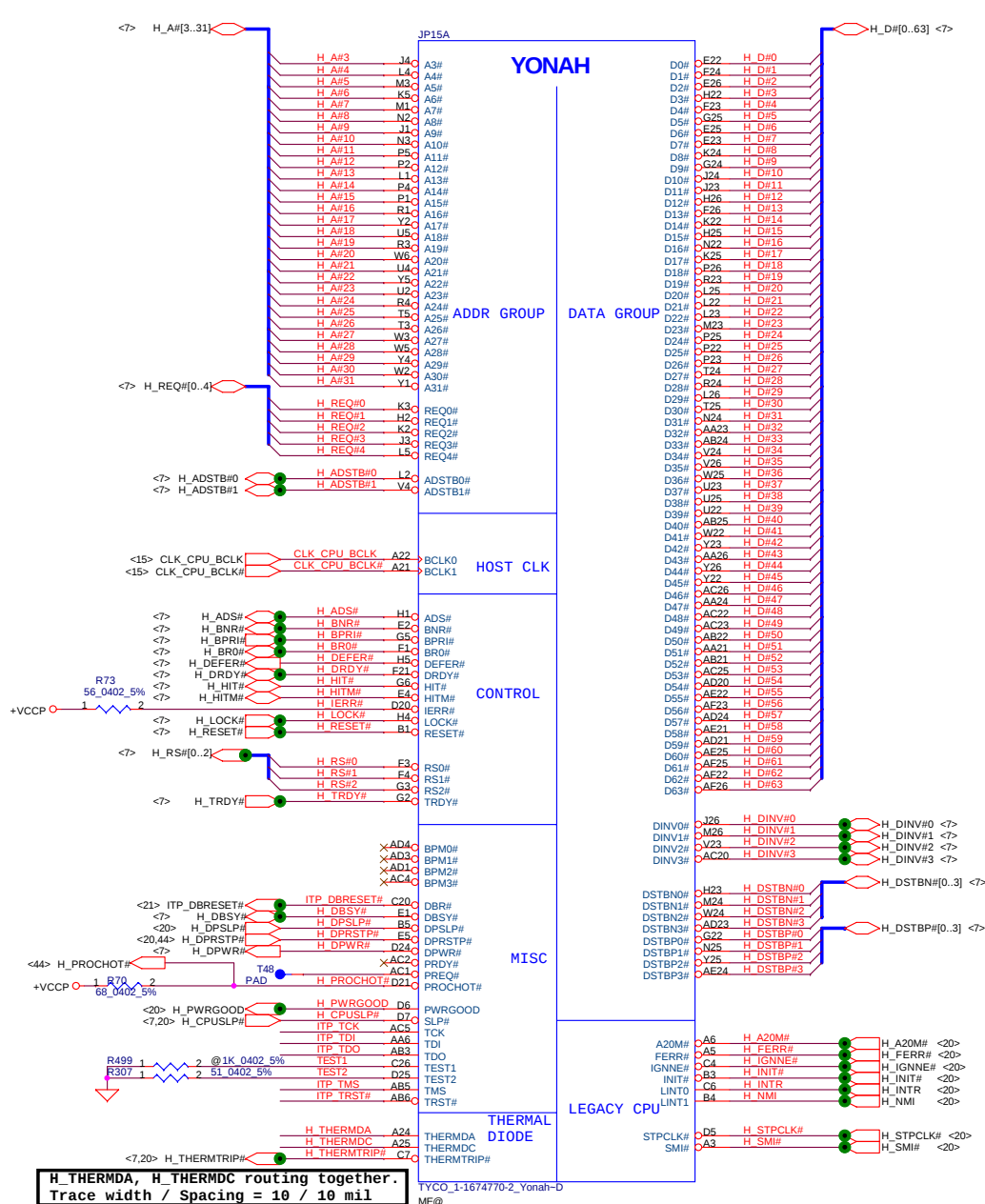
Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

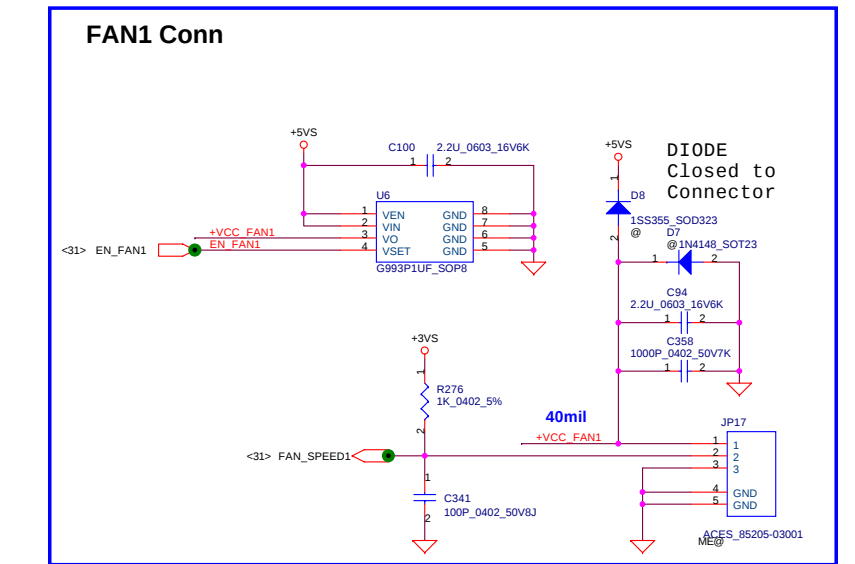
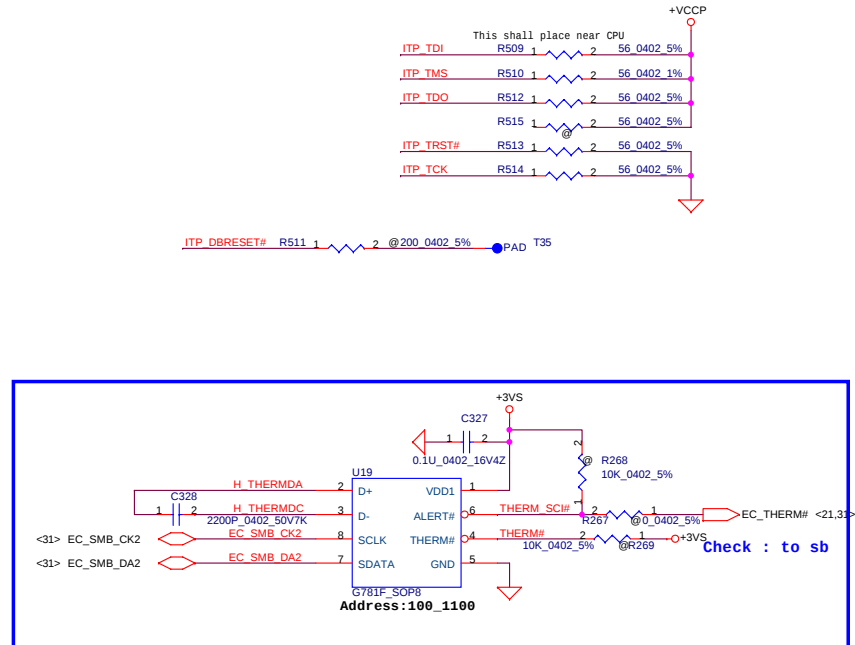
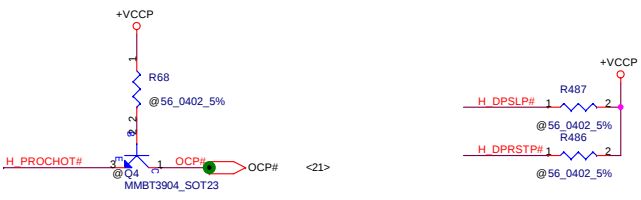
Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

ICH7M SM Bus address

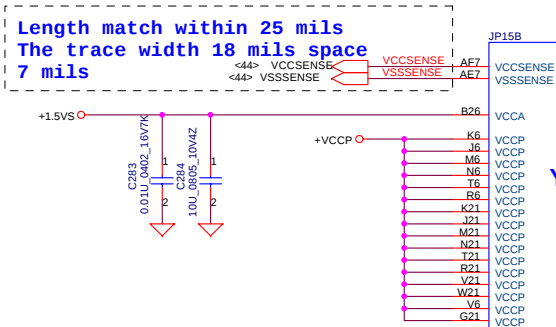
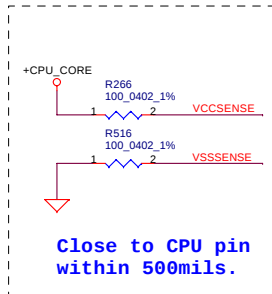
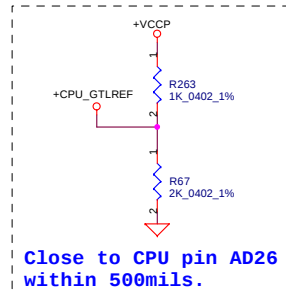
Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb
Wireless	
NewCard	
LAN	



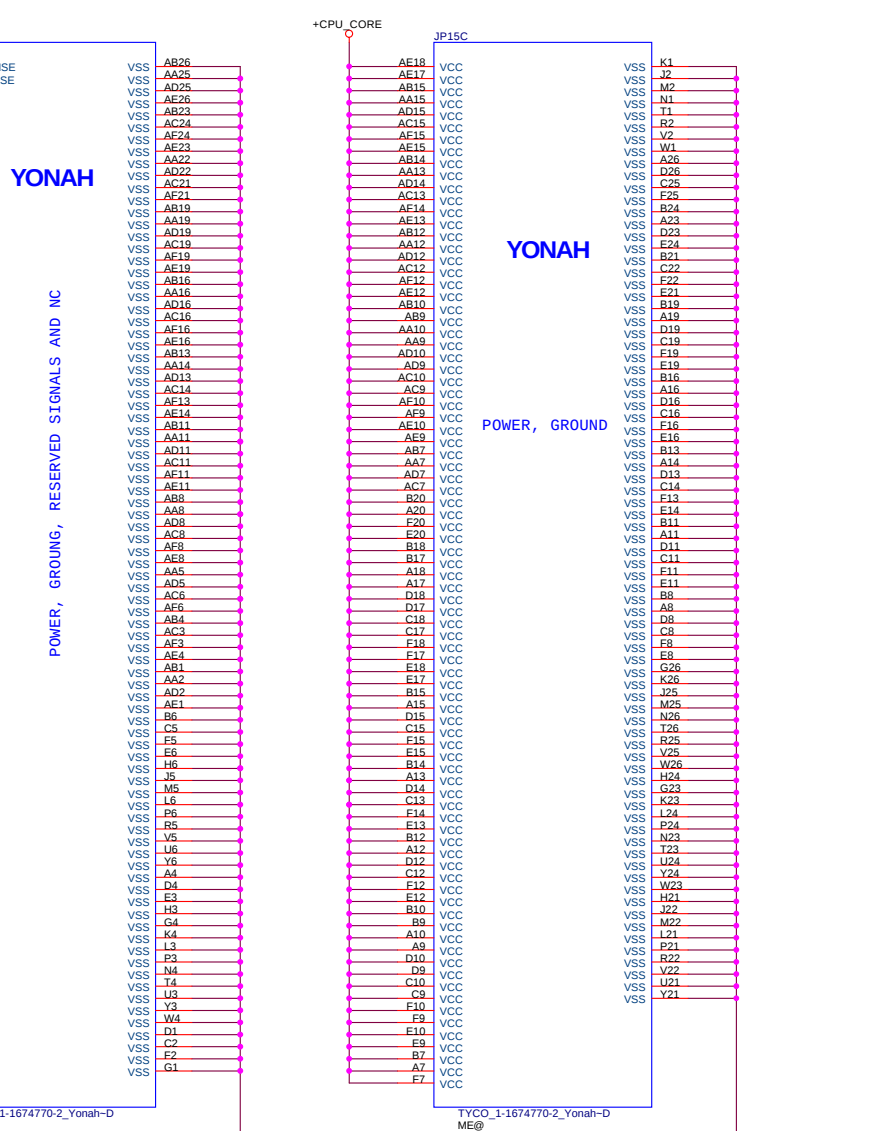
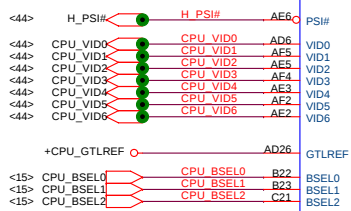
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

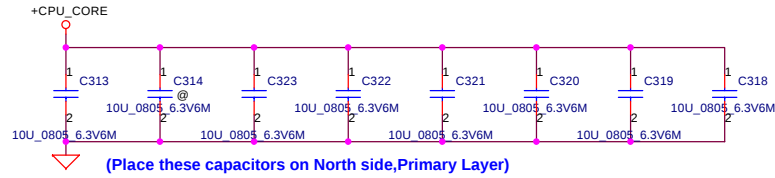
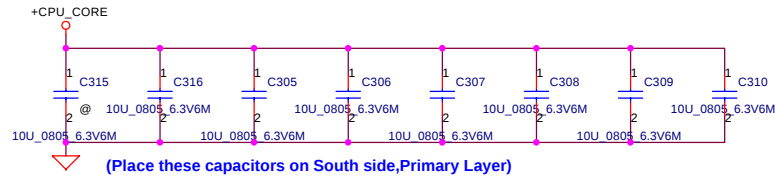
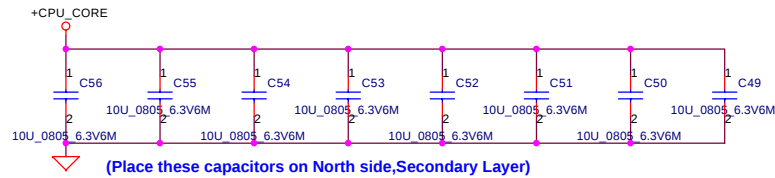
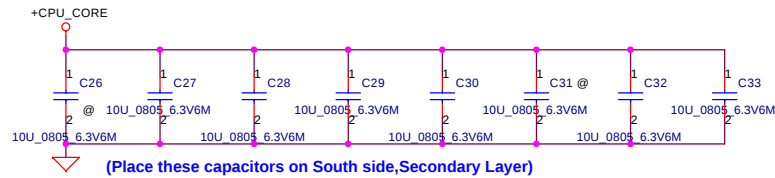
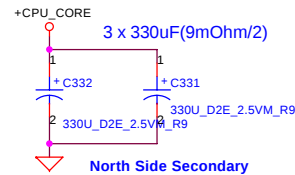
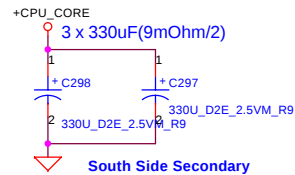


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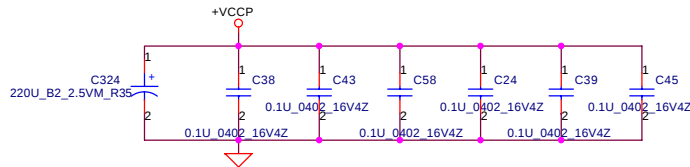
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

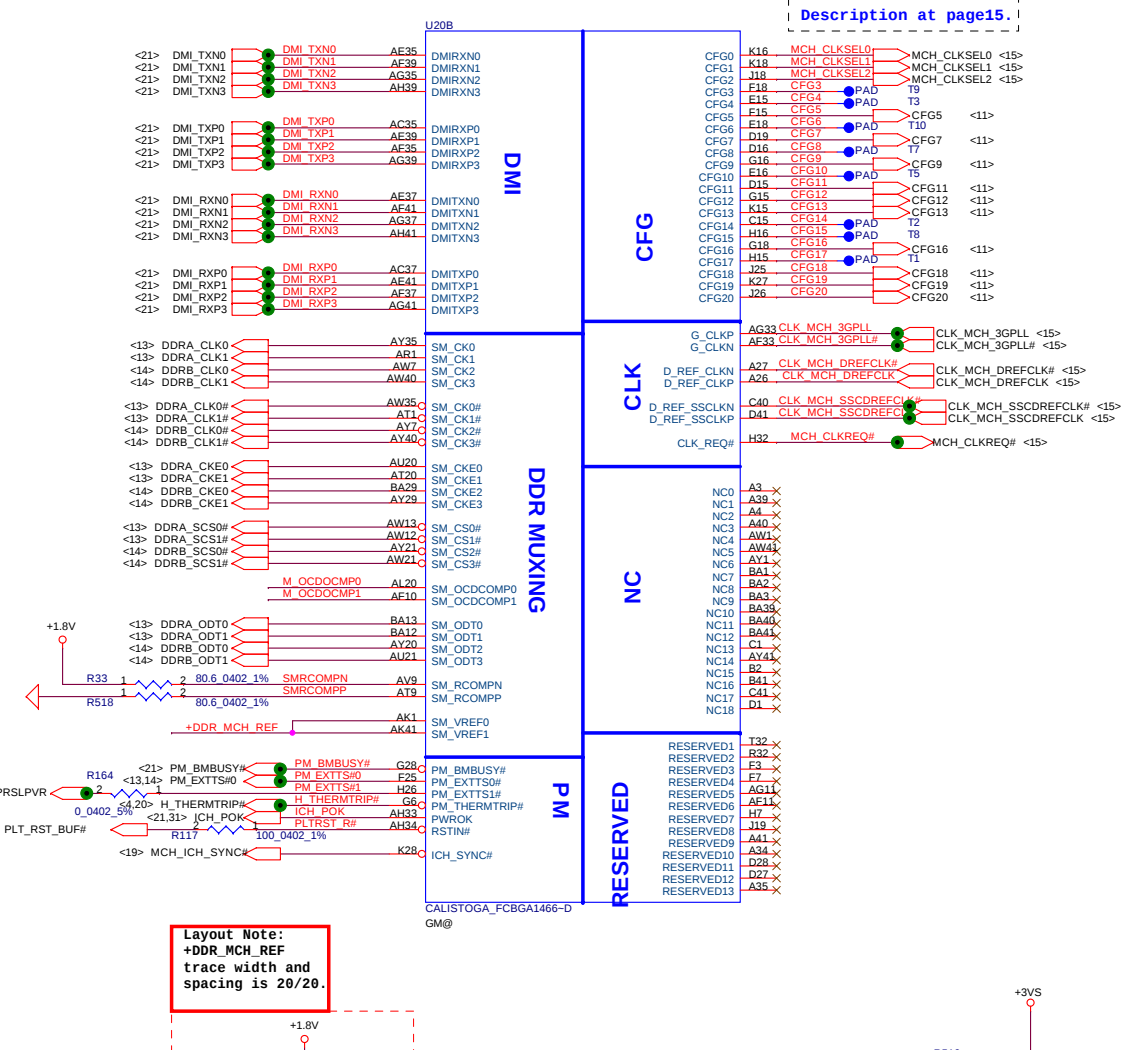




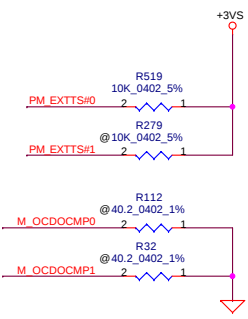
9/25 10U checked. OK for use!

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32





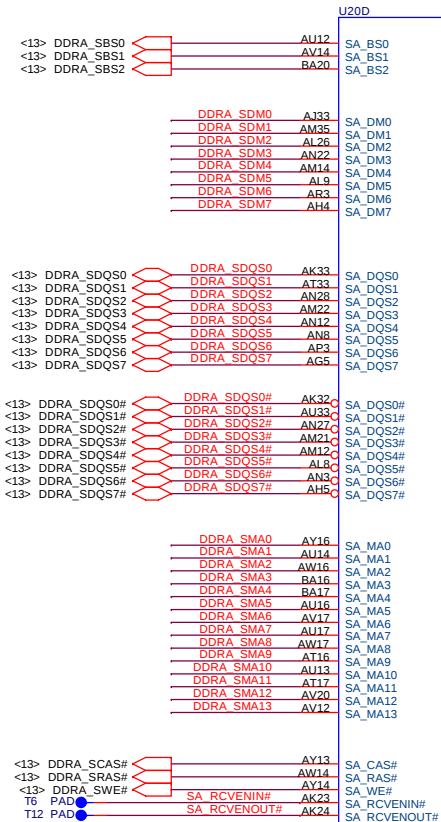
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 /
H_SWNG1 trace width and spacing is 10/20.



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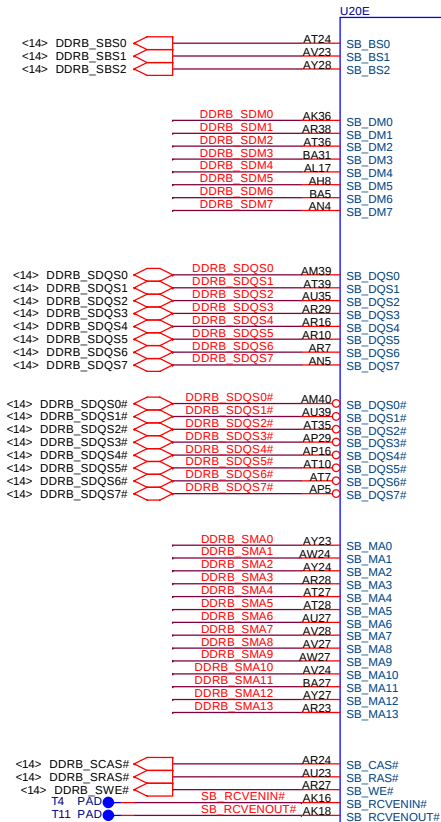
<13> DDRA_SDQ[0..63]  DDRA_SDQ[0..63]
<13> DDRA_SDM[0..7]  DDRA_SDM[0..7]
<13> DDRA_SMA[0..13]  DDRA_SMA[0..13]

<14> DDRB_SDQ[0..63]  DDRB_SDQ[0..63]
<14> DDRB_SDM[0..7]  DDRB_SDM[0..7]
<14> DDRB_SMA[0..13]  DDRB_SMA[0..13]



DDR SYS MEMORY A

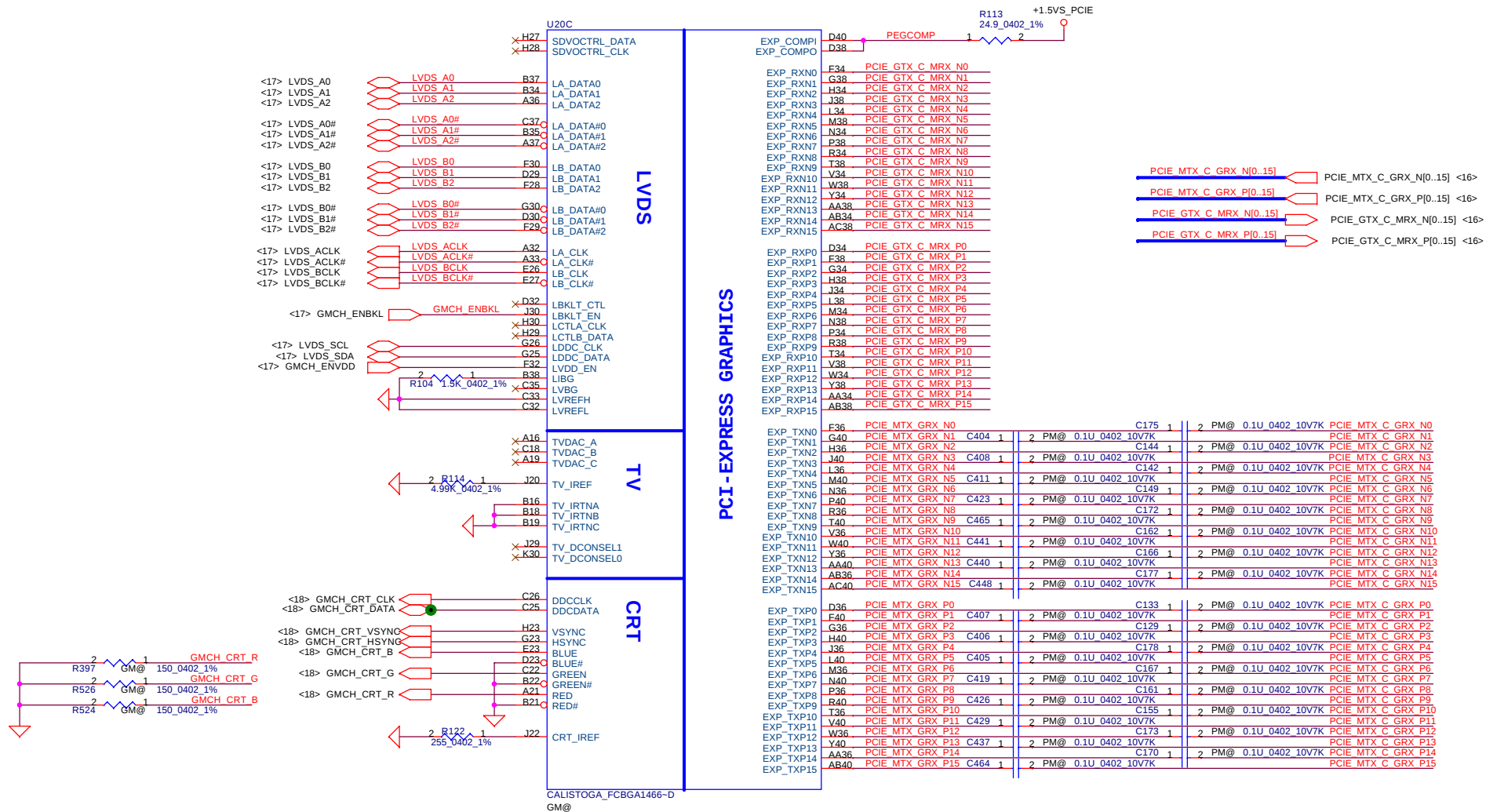
CALISTOGA_FCBGA1466-D
GM@



DDR SYS MEMORY B

CALISTOGA_FCBGA1466-D
GM@

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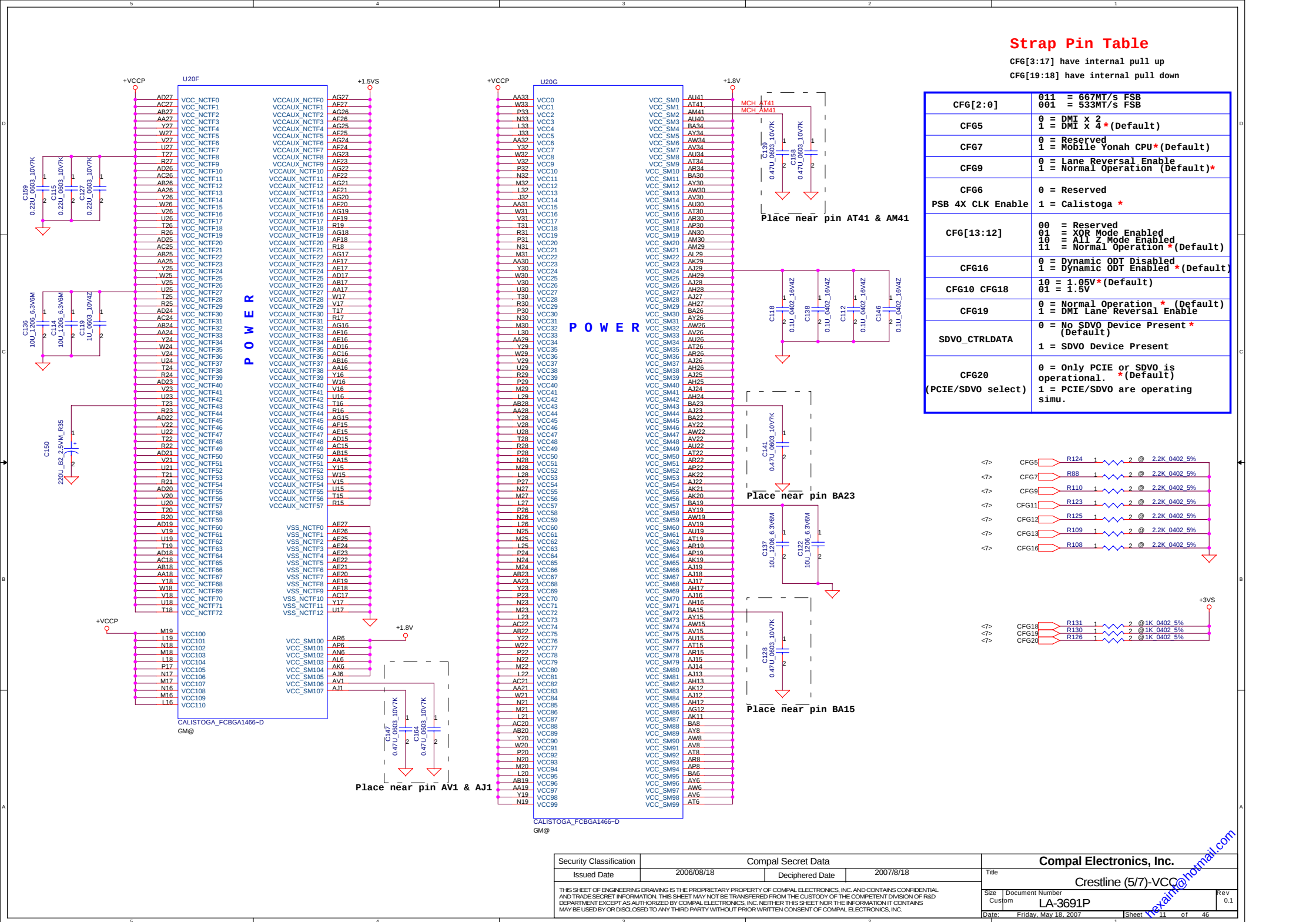
Strap Pin Table

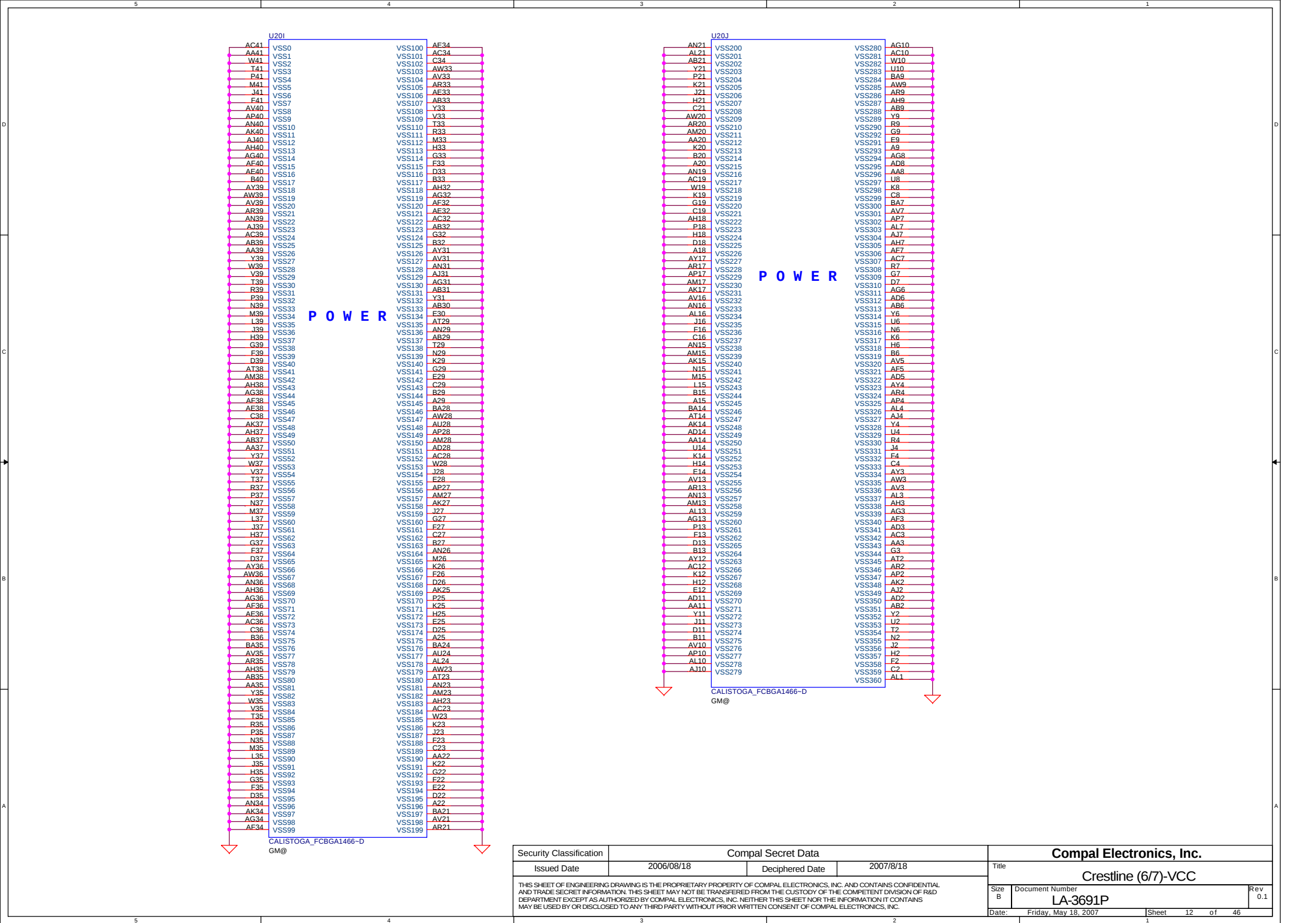
CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

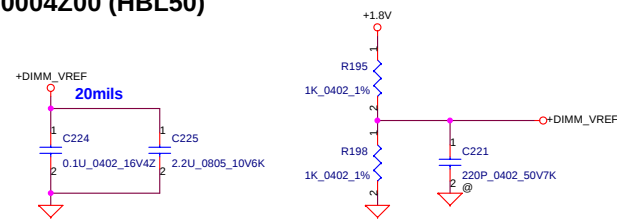
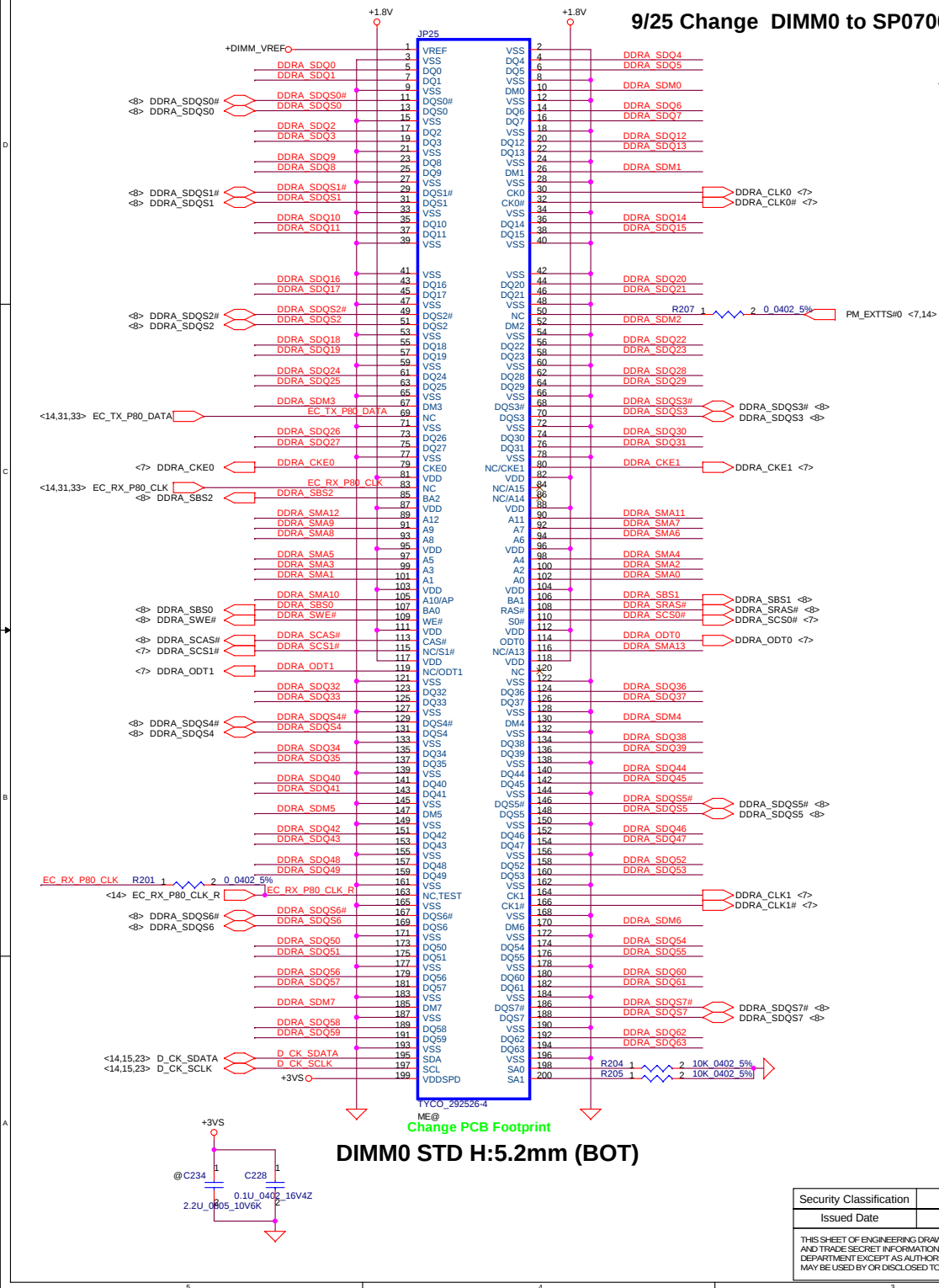
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU* (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved 1 = Calistoga *
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V* (Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.

<7>	CFG5	R124	1	2	@ 2.2K 0402 5%
<7>	CFG7	R88	1	2	@ 2.2K 0402 5%
<7>	CFG9	R110	1	2	@ 2.2K 0402 5%
<7>	CFG11	R123	1	2	@ 2.2K 0402 5%
<7>	CFG12	R125	1	2	@ 2.2K 0402 5%
<7>	CFG13	R109	1	2	@ 2.2K 0402 5%
<7>	CFG16	R108	1	2	@ 2.2K 0402 5%
<7>	CFG18	R131	1	2	@ 1K 0402 5%
<7>	CFG19	R130	1	2	@ 1K 0402 5%
<7>	CFG20	R126	1	2	@ 1K 0402 5%

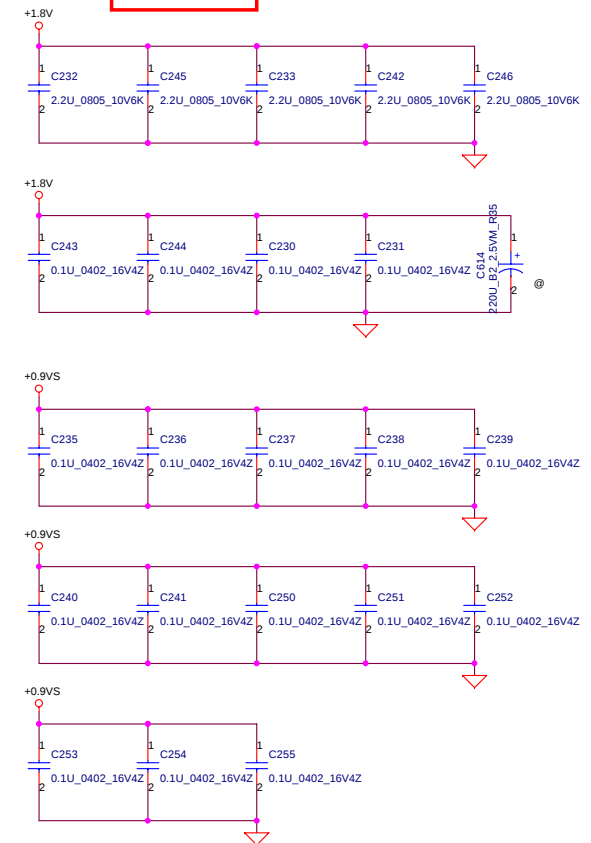




9/25 Change DIMM0 to SP070004Z00 (HBL50)



Layout Note:
Place near JP35

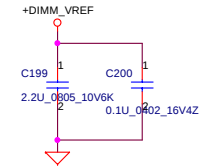
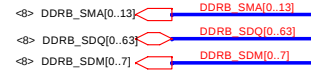
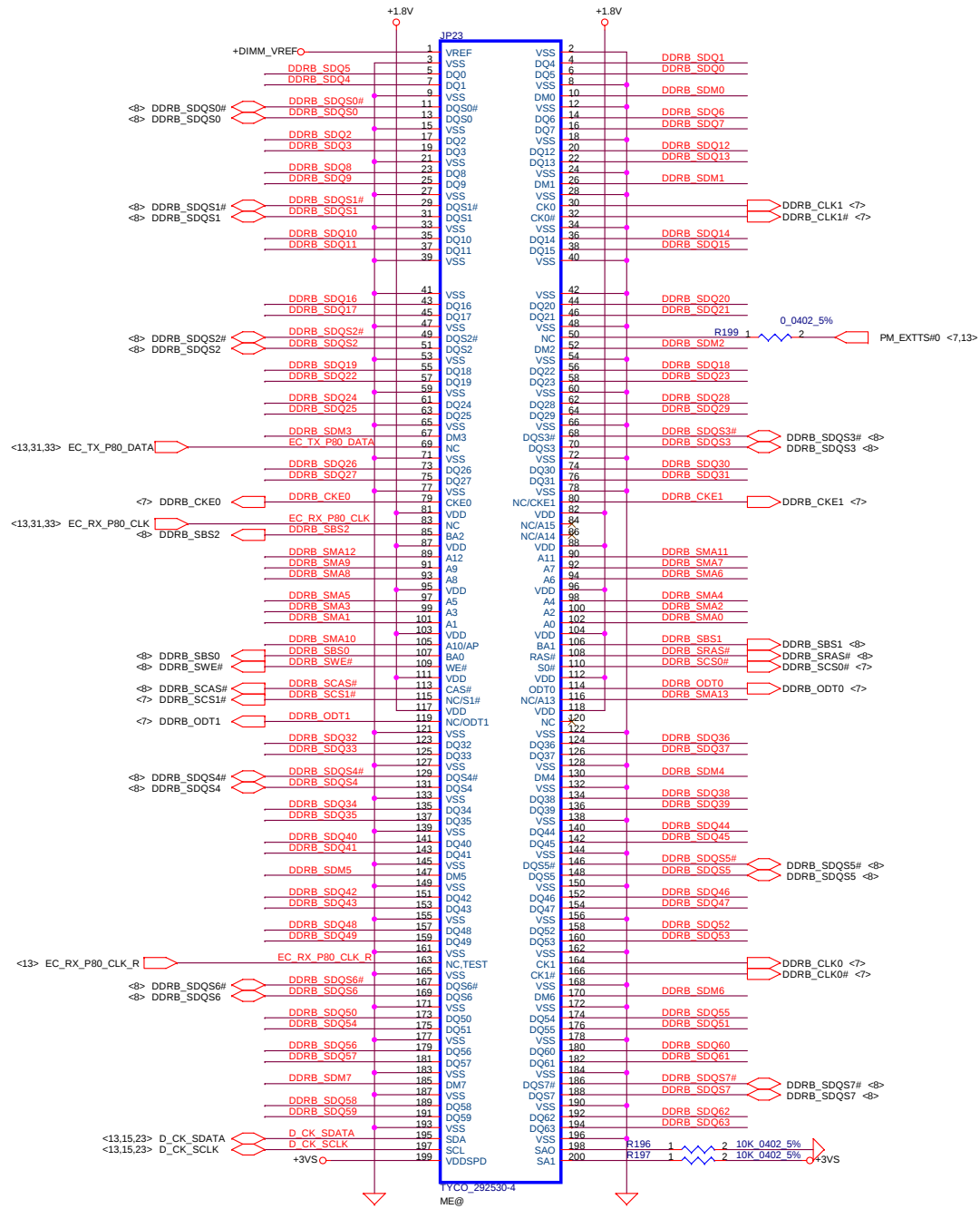


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

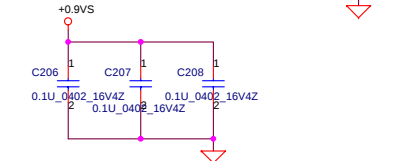
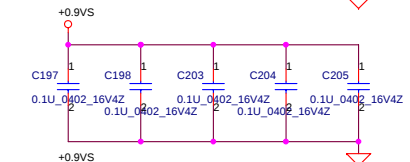
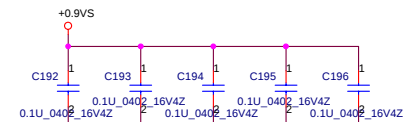
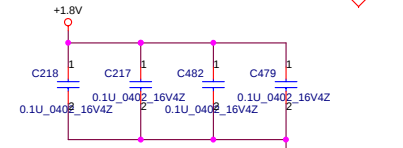
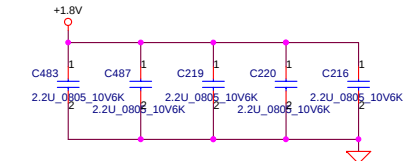
Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5

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9/25 Change DIMM1 to SP070006F00



Layout Note:
Place near JP34



Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

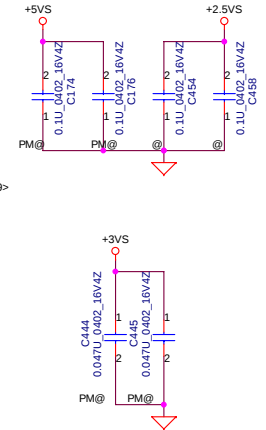
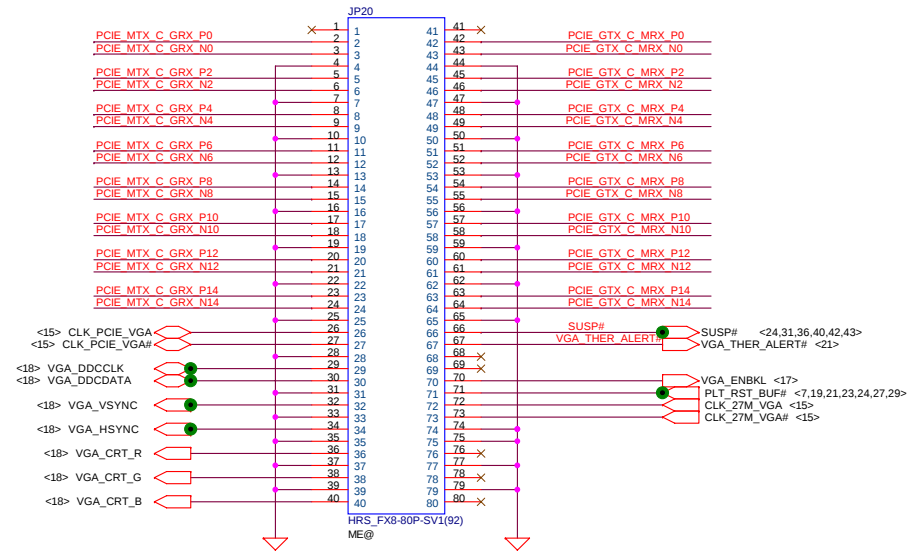
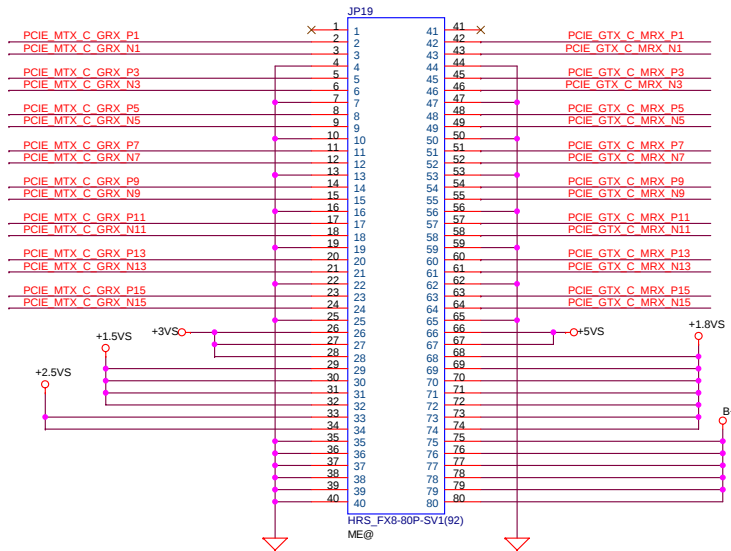
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MAX. 4.06A @ 1.8V

MAX. 130mA @ 2.5V

MAX. 655mA @ 3.3V

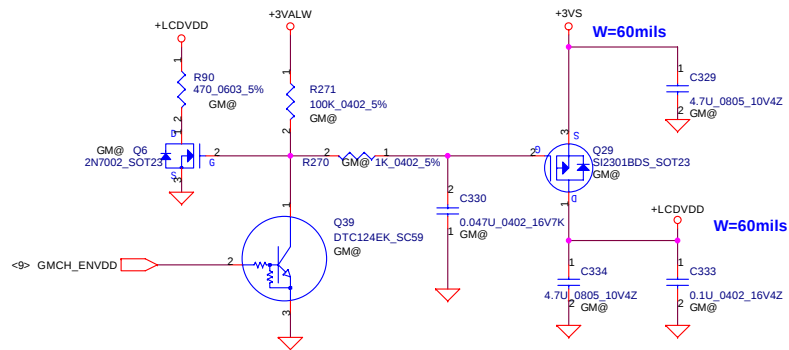
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<9> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N0..15
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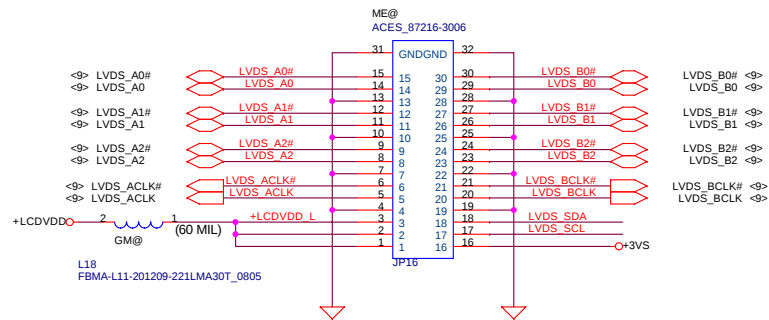
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VGA/B connector			
Title	Size	Document Number	Rev
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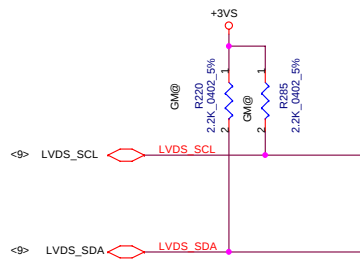
LCD POWER CIRCUIT



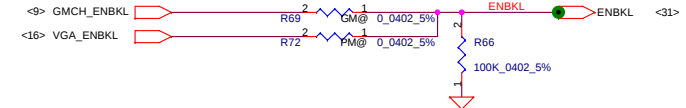
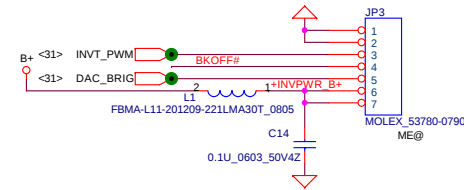
LCD/PANEL BD. Conn.



Follow HEL80's pin definition
Except pin 29



INVERTER Conn.

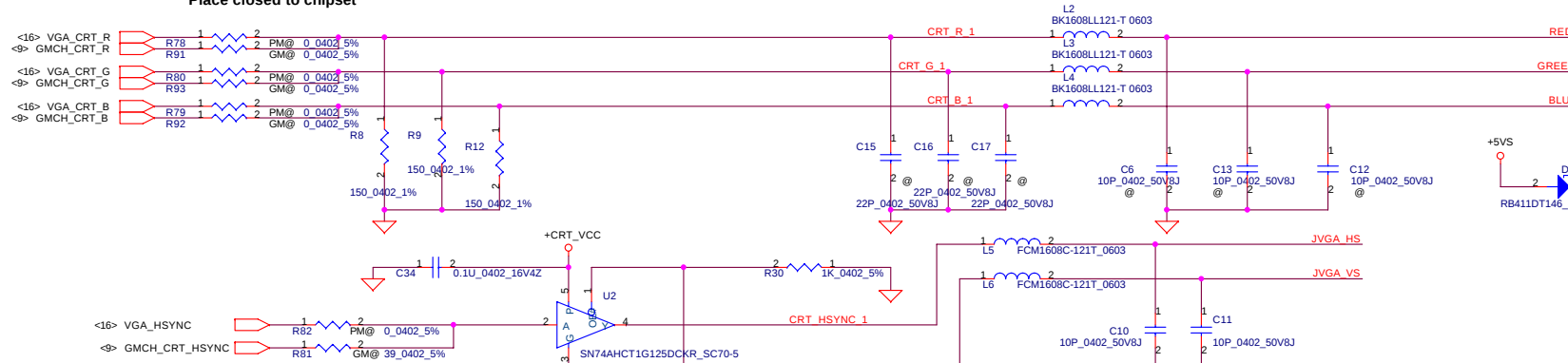


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				B	LA-3691P
				Date:	Friday, May 18, 2007
				Sheet	17 of 46

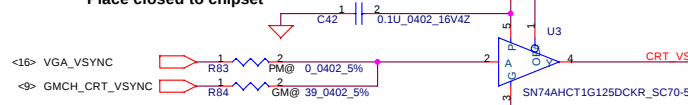
Revain@hotmail.com

CRT Connector

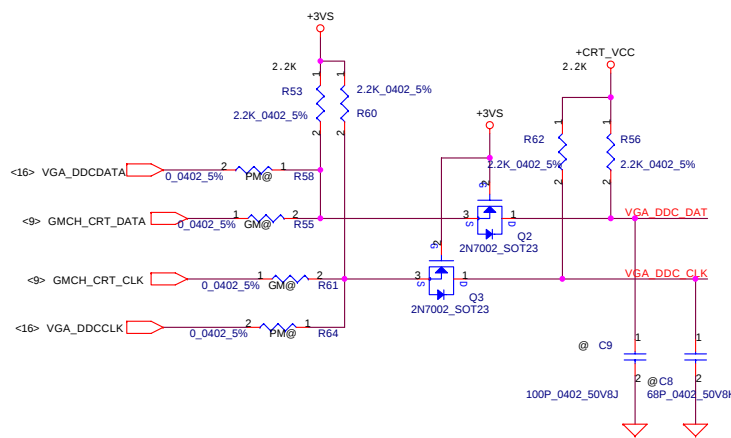
Place closed to chipset



Place closed to chipset

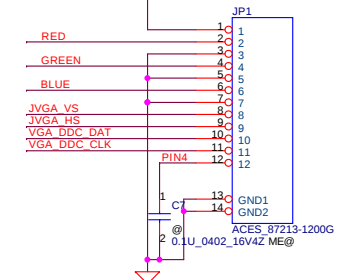


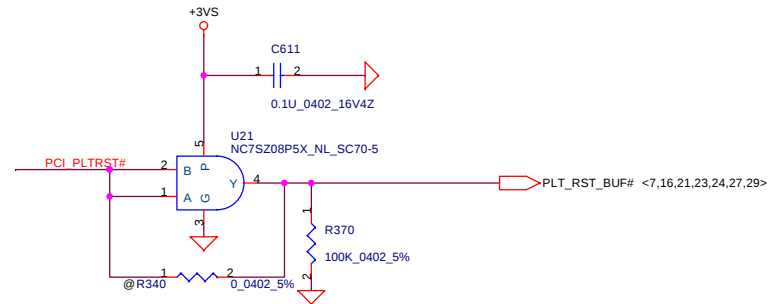
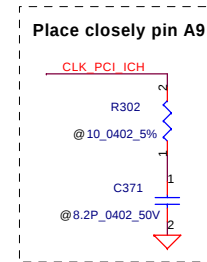
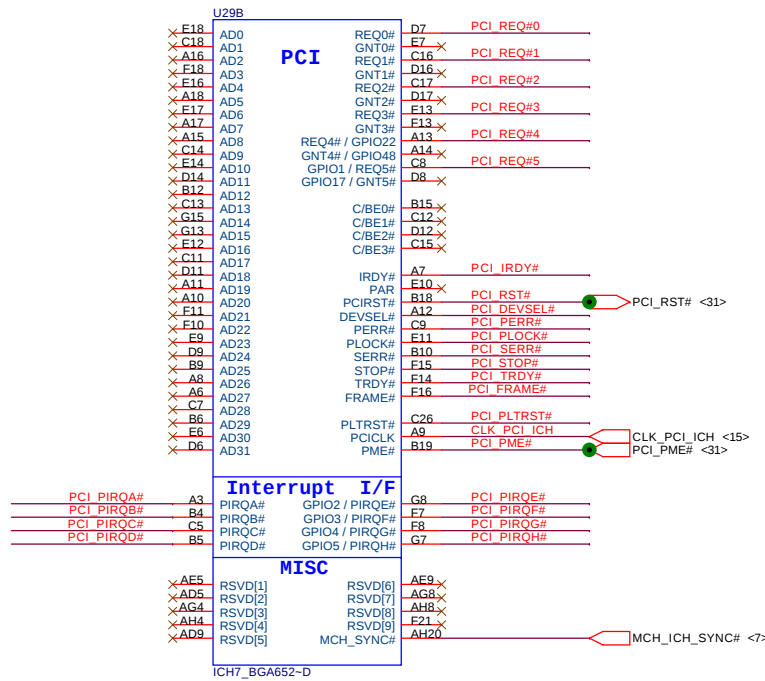
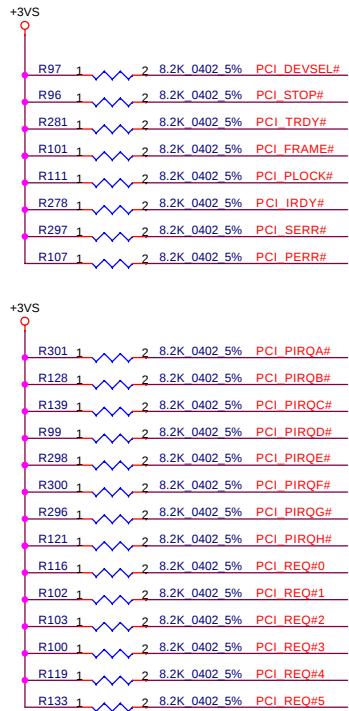
Update Footprint



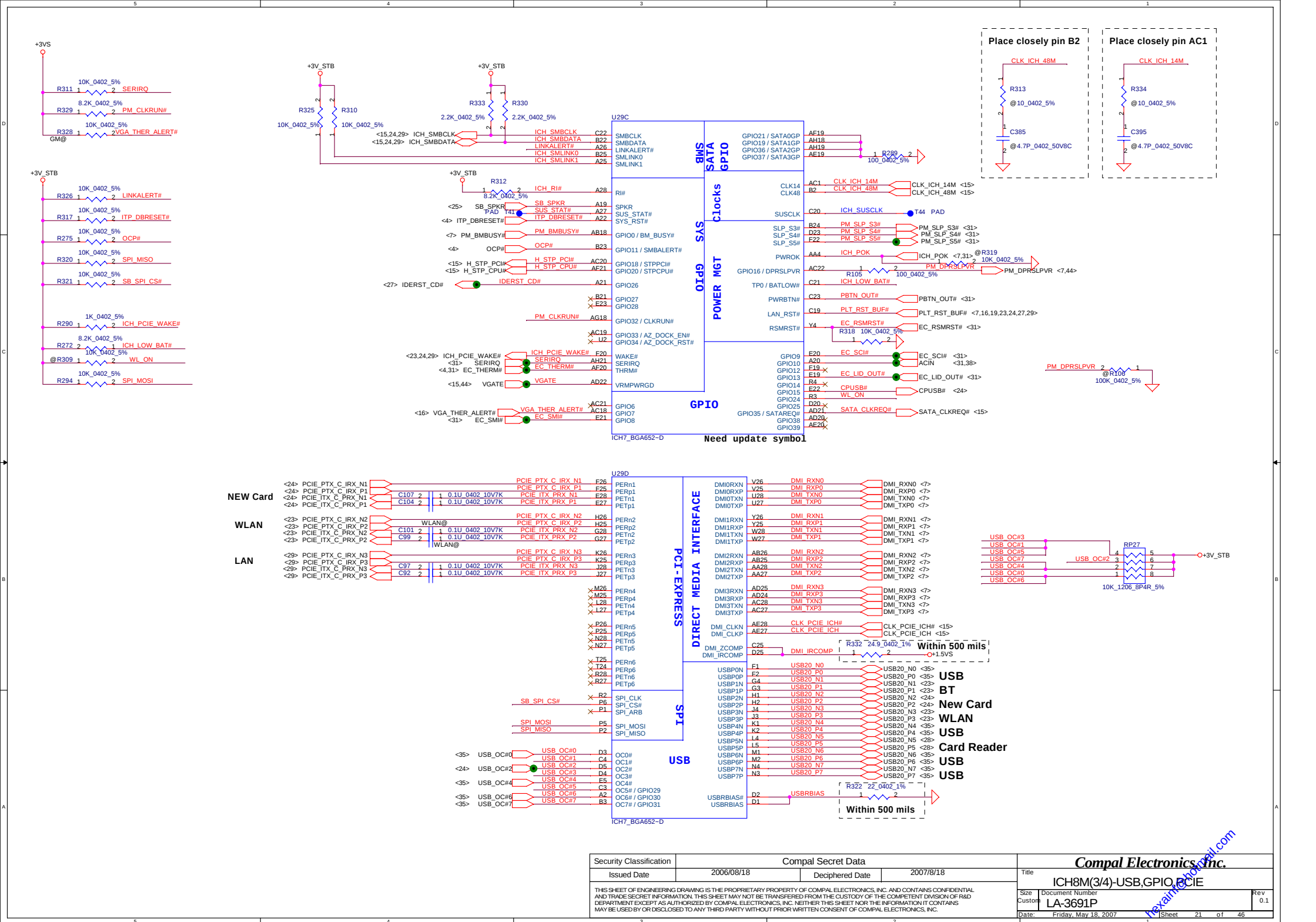
PIN ASSIGMENT

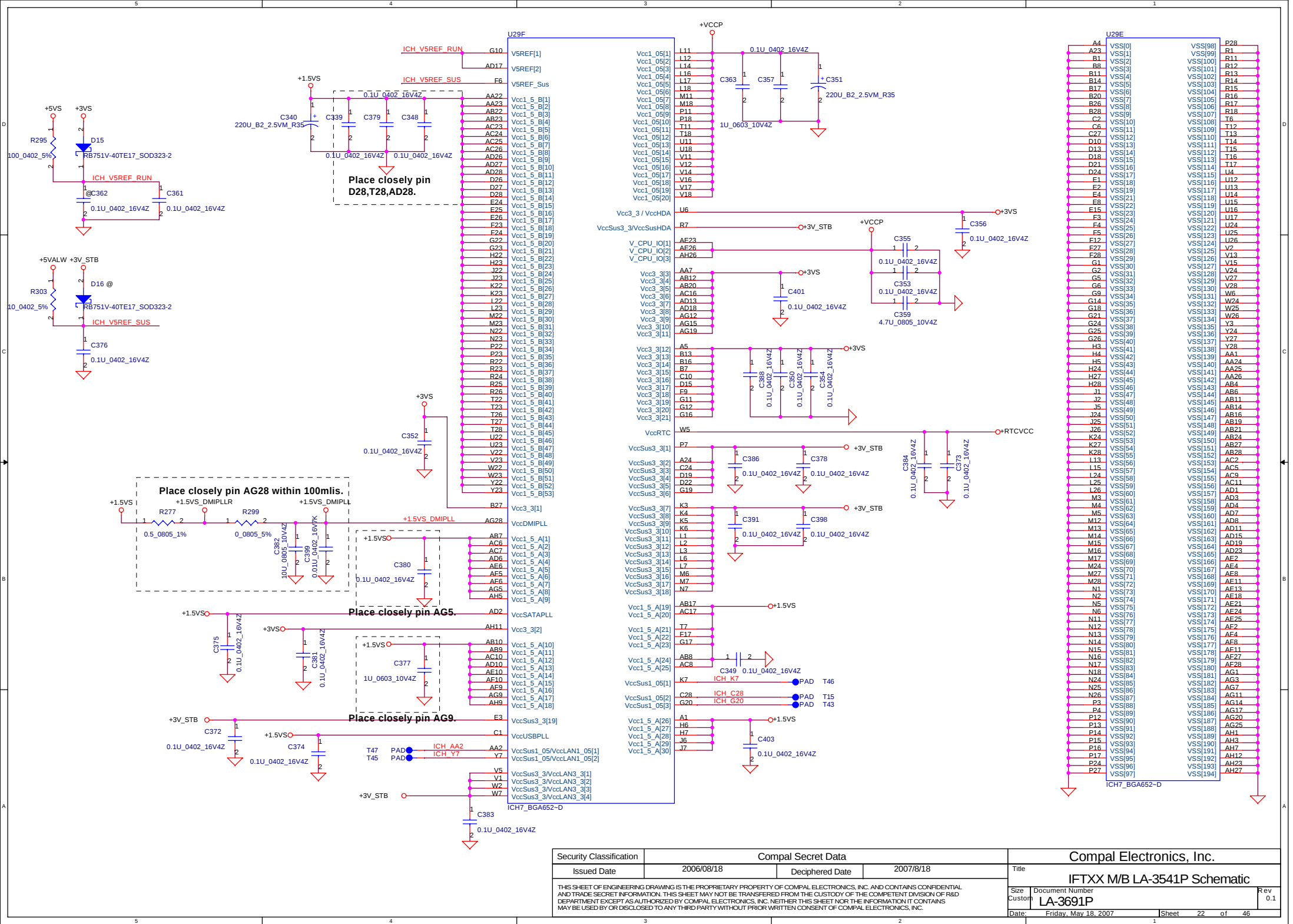
PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
	10	GND
9	13	HSYNC
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
12		
	5	GND
	4	





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				Date:	Friday, May 18, 2007
				Sheet	19 of 46
				Rev	0.1

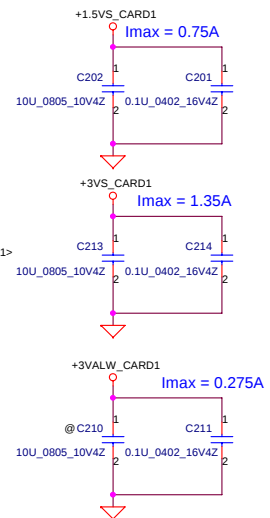
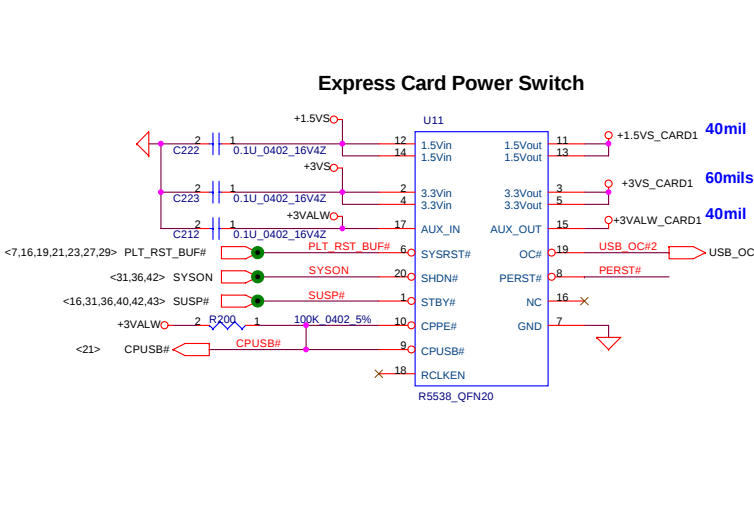




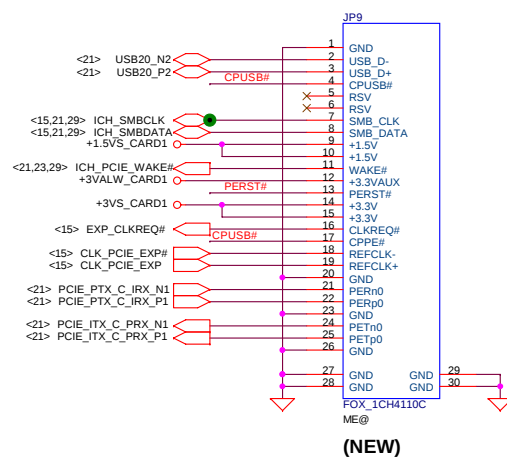
Mini-Express Card for 3G Or TV Tuner

Mini-Express Card for WLAN

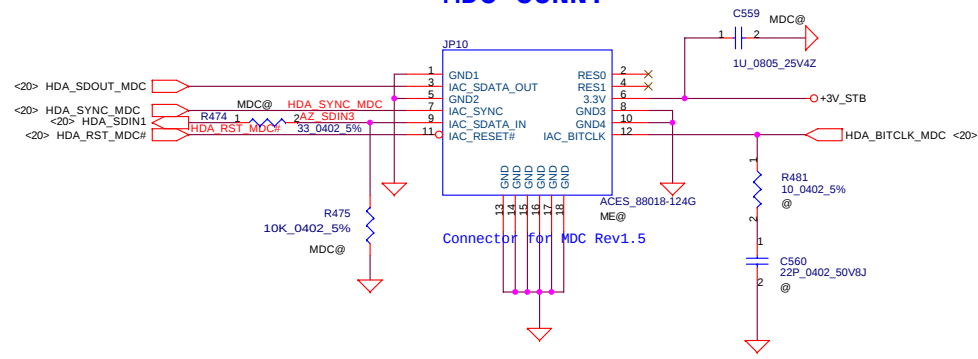




New Card Socket (Left/TOP)



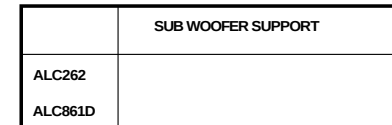
MDC CONN.



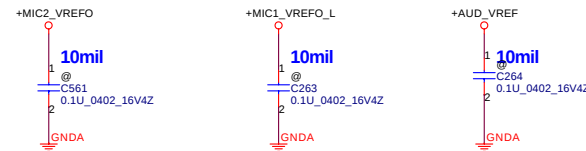
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Size B	Rev 0.1
Date: Friday, May 18, 2007		Sheet 24 of 46			

28.7K for Module Design (VDDA = 4.702)

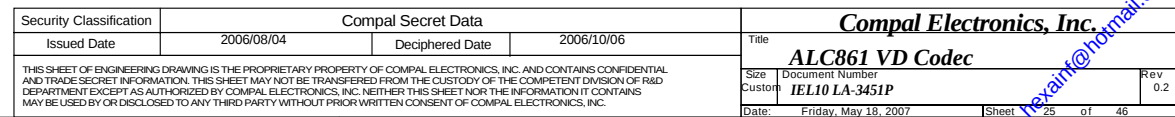
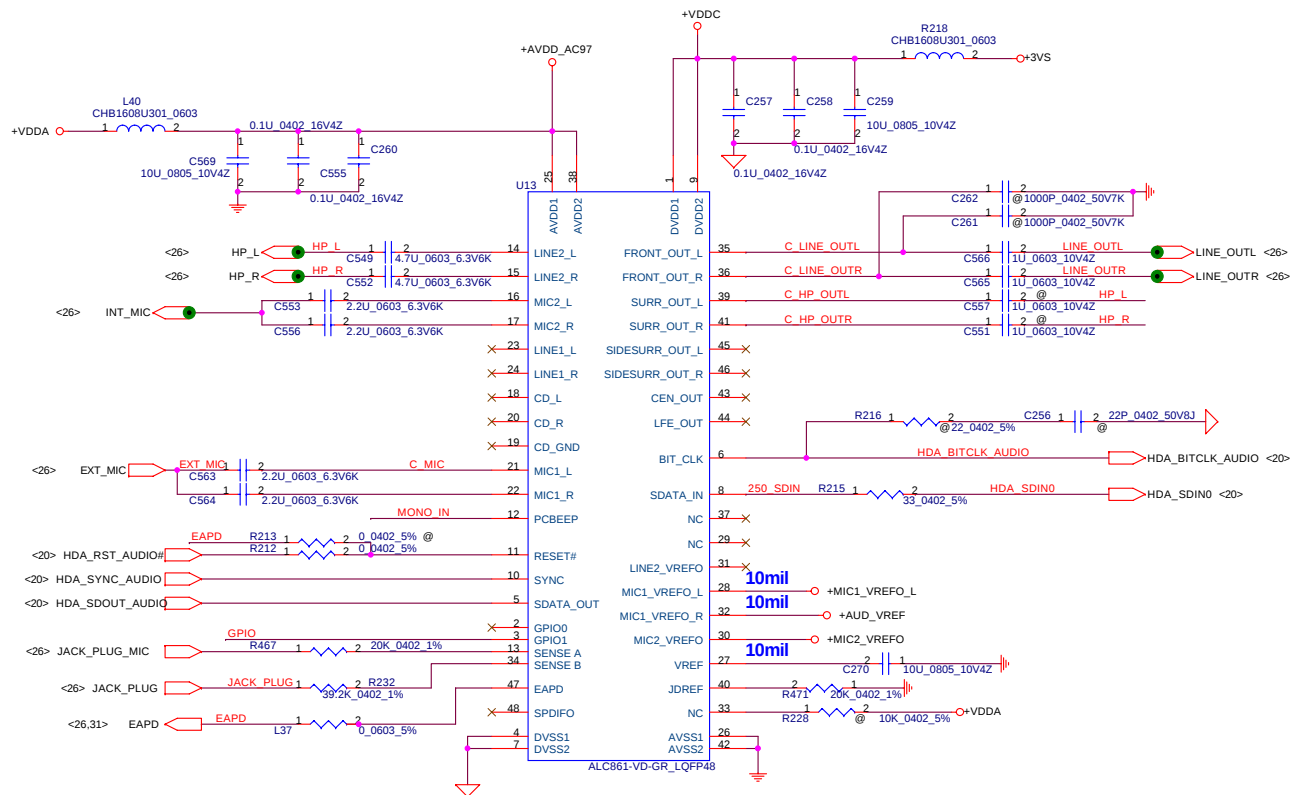
4.85V



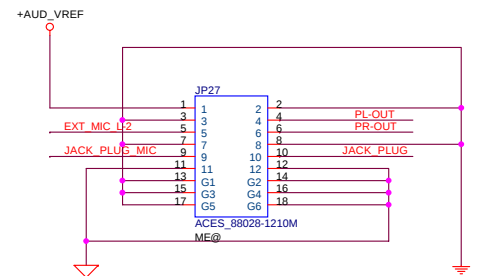
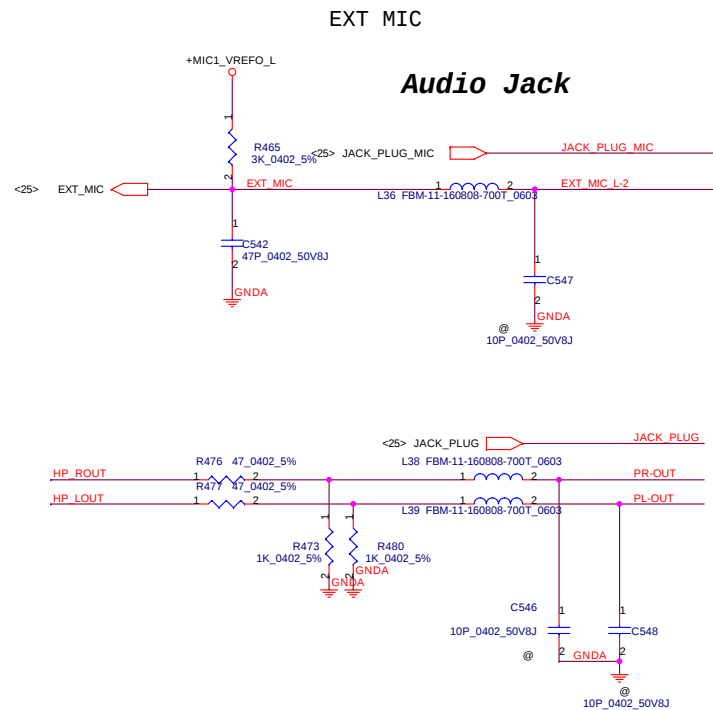
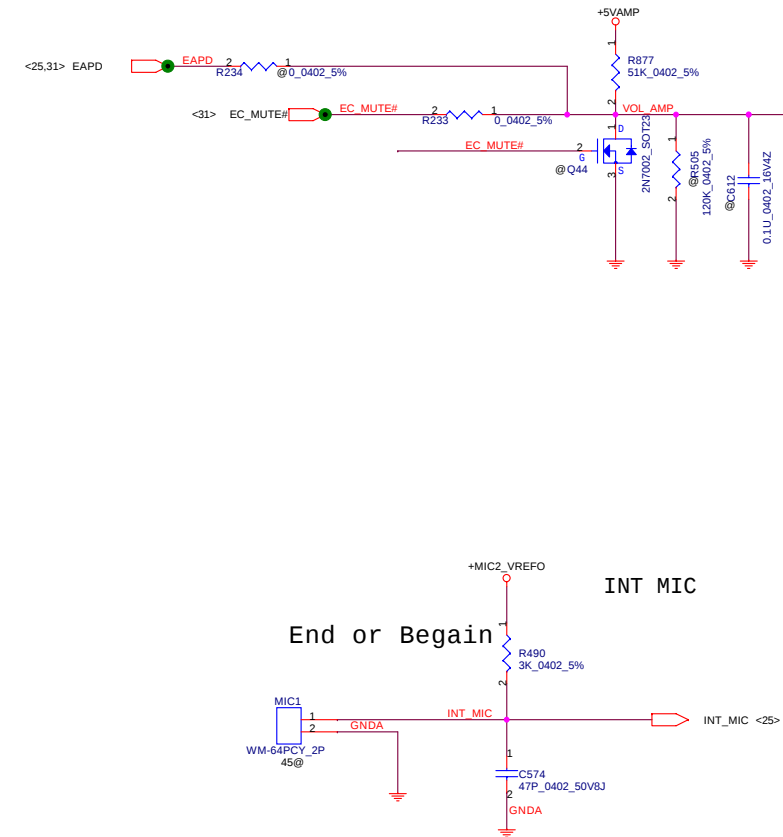
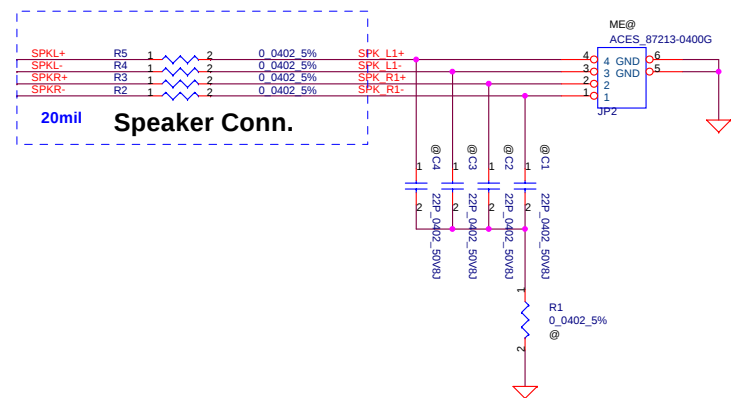
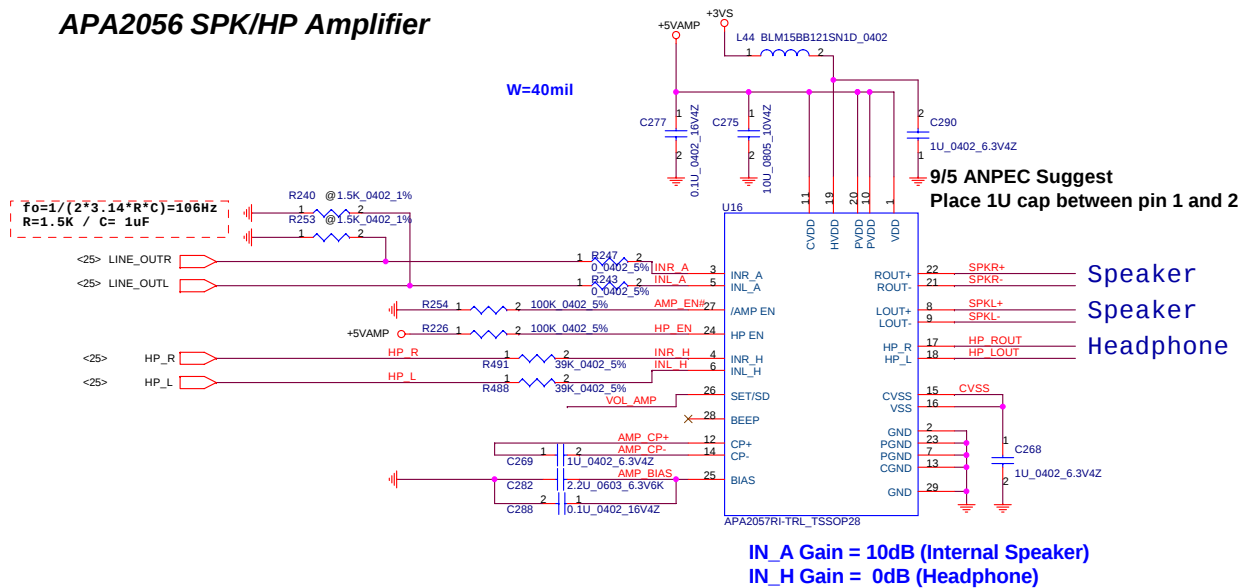
Driver initial



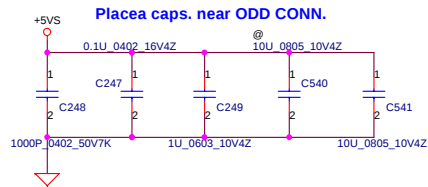
DOS mode



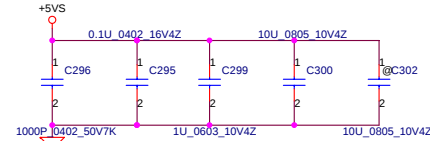
APA2056 SPK/HP Amplifier



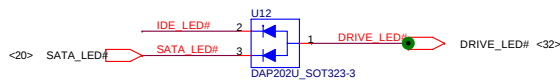
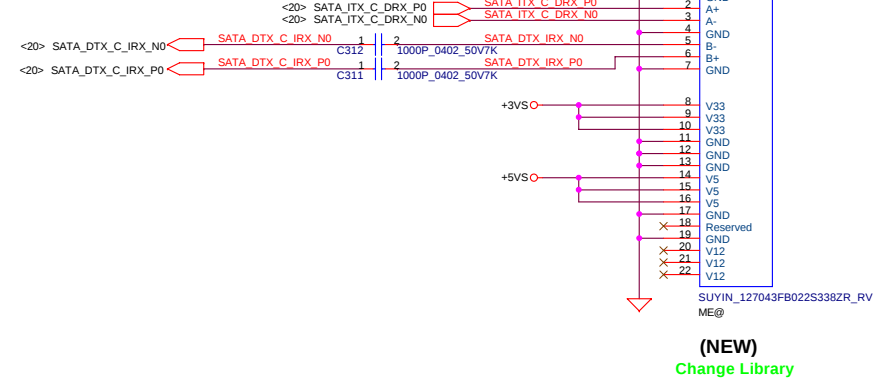
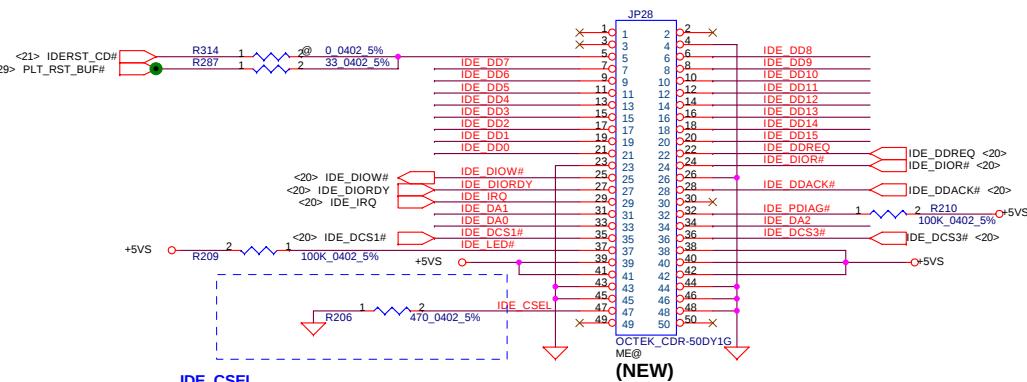
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title AMP/VR/Audio Jack/MIC		
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				Date: Monday, May 21, 2007 Sheet 26 of 46		



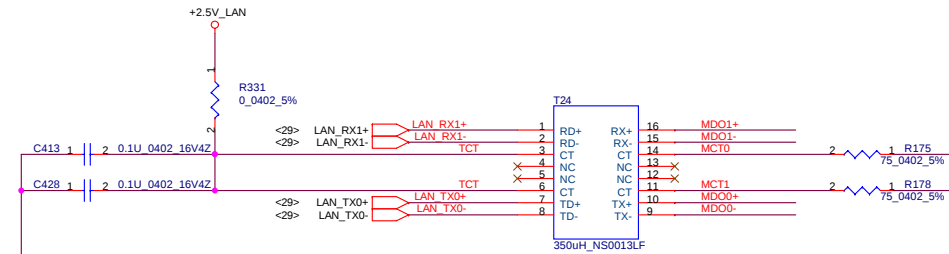
<20> IDE_DD[0..15] IDE_DD[0..15]
 <20> IDE_DA[0..2] IDE_DA[0..2]



SATA HDD Conn.

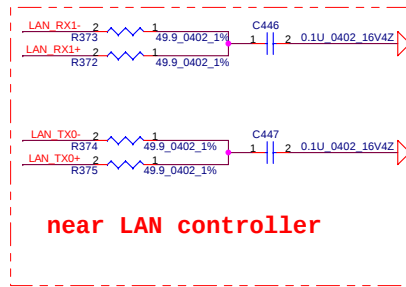


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	B	Document Number	LA-3691P	Rev	0.1
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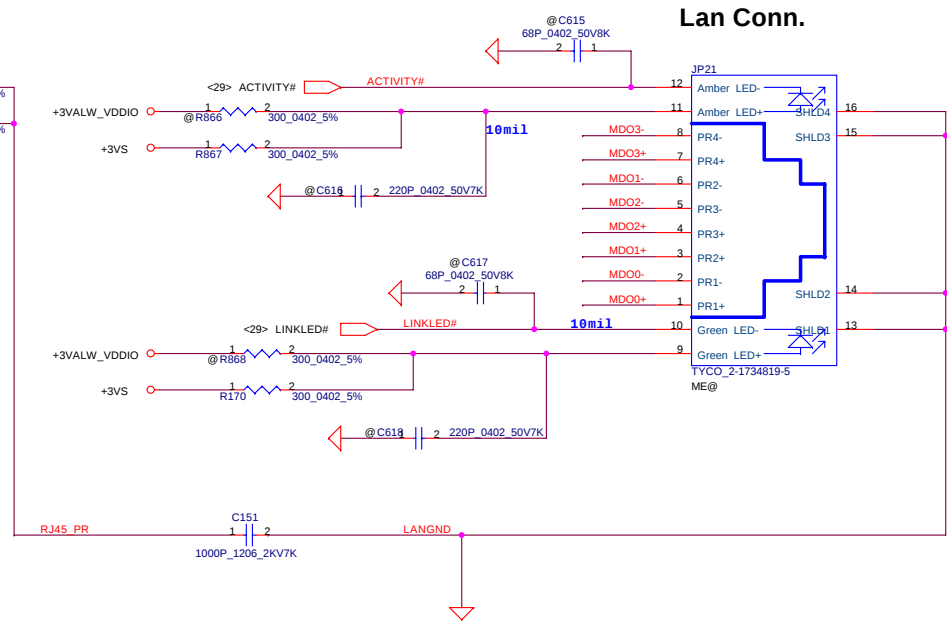


Change T1 from SP050001210 to SP050001210

Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



near LAN controller



Lan Conn.

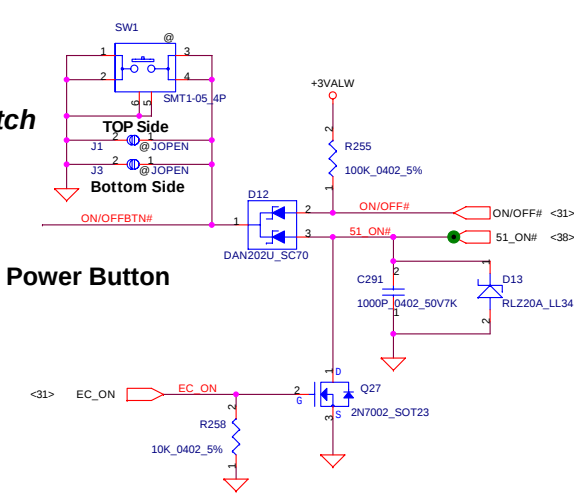
Security Classification	Compal Secret Data			Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	LAN CONTROLLER	
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				Custom	0.1
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LAN CONTROLLER

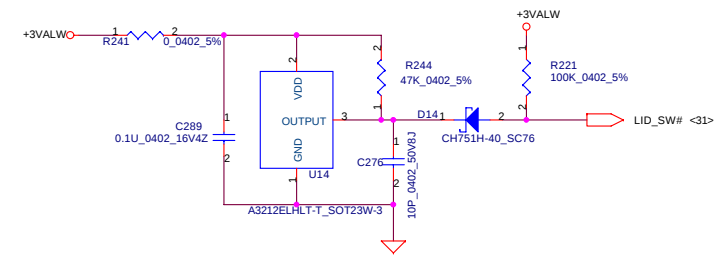
Document Number
LA-3691P
Rev
0.1

ON/OFF switch

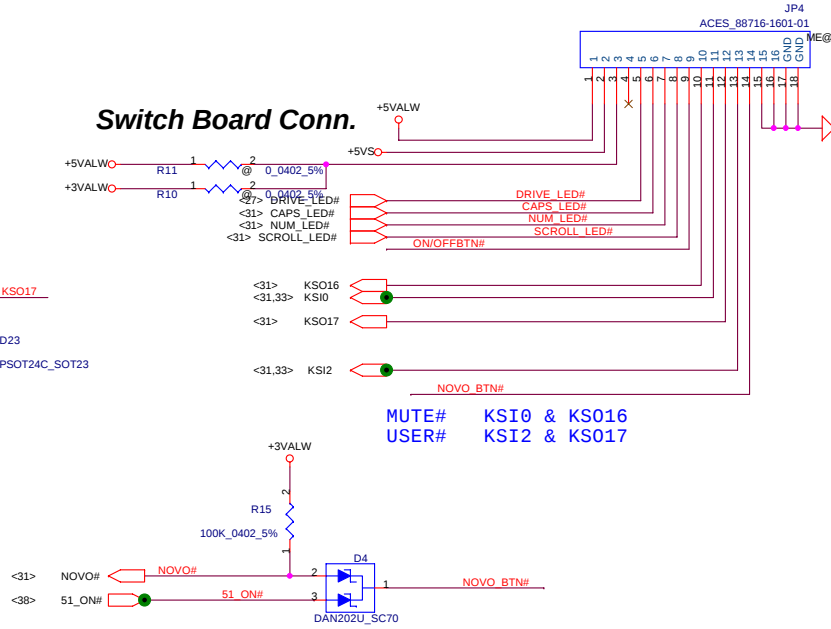


Power Button

LID Switch

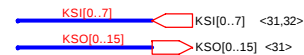


Switch Board Conn.

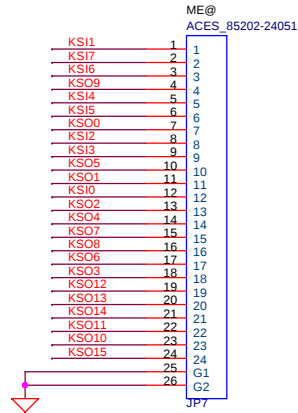
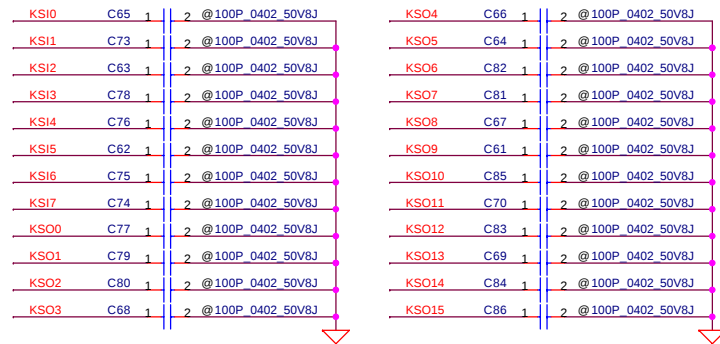


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2007/8/18		Title		BIOS, I/O Port & K/B Connector	
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B		Document Number		0.1	
LA-3691P		Date:		Friday, May 18, 2007	
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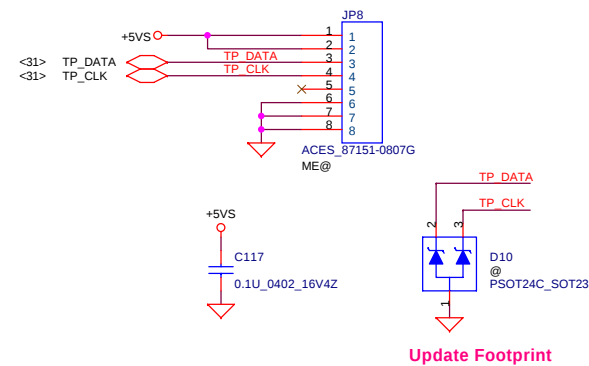
INT_KBD Conn.



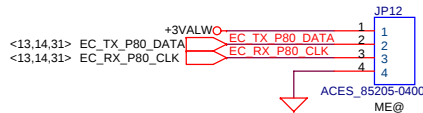
For IHL00



To TP/B Conn.

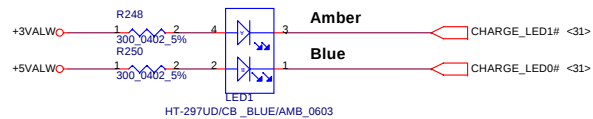
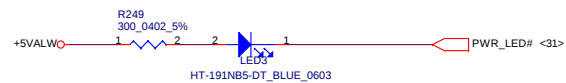


EC DEBUG PORT

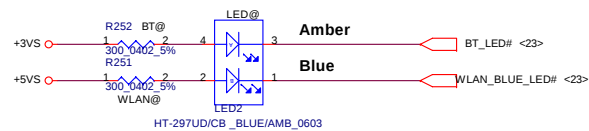


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LED



Blue&Amber

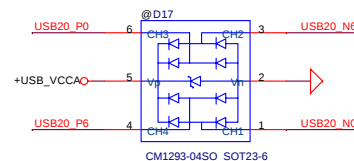
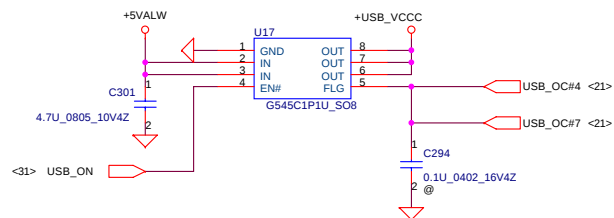
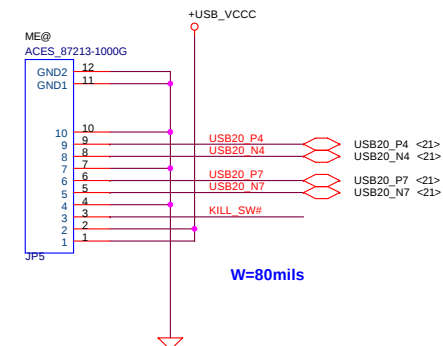
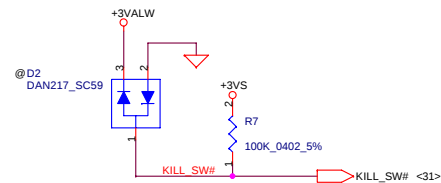


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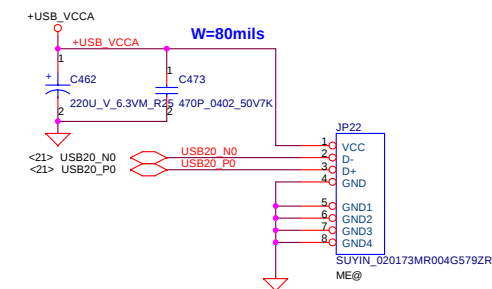
USB Conn.

W=80mils

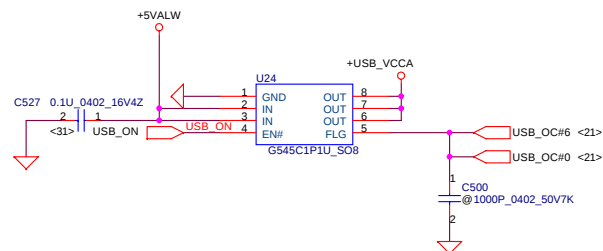
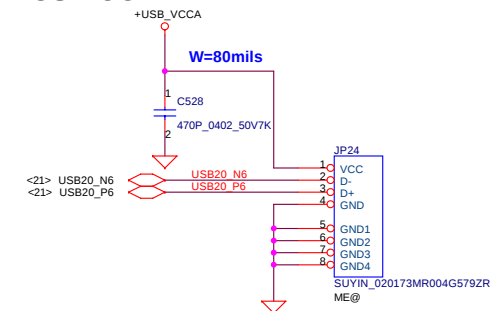
Kill SWITCH



USB CONN. 1

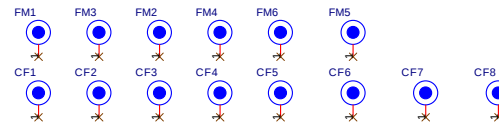


USB CONN. 2



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
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Date: Friday, May 18, 2007		Sheet 27		of 46	

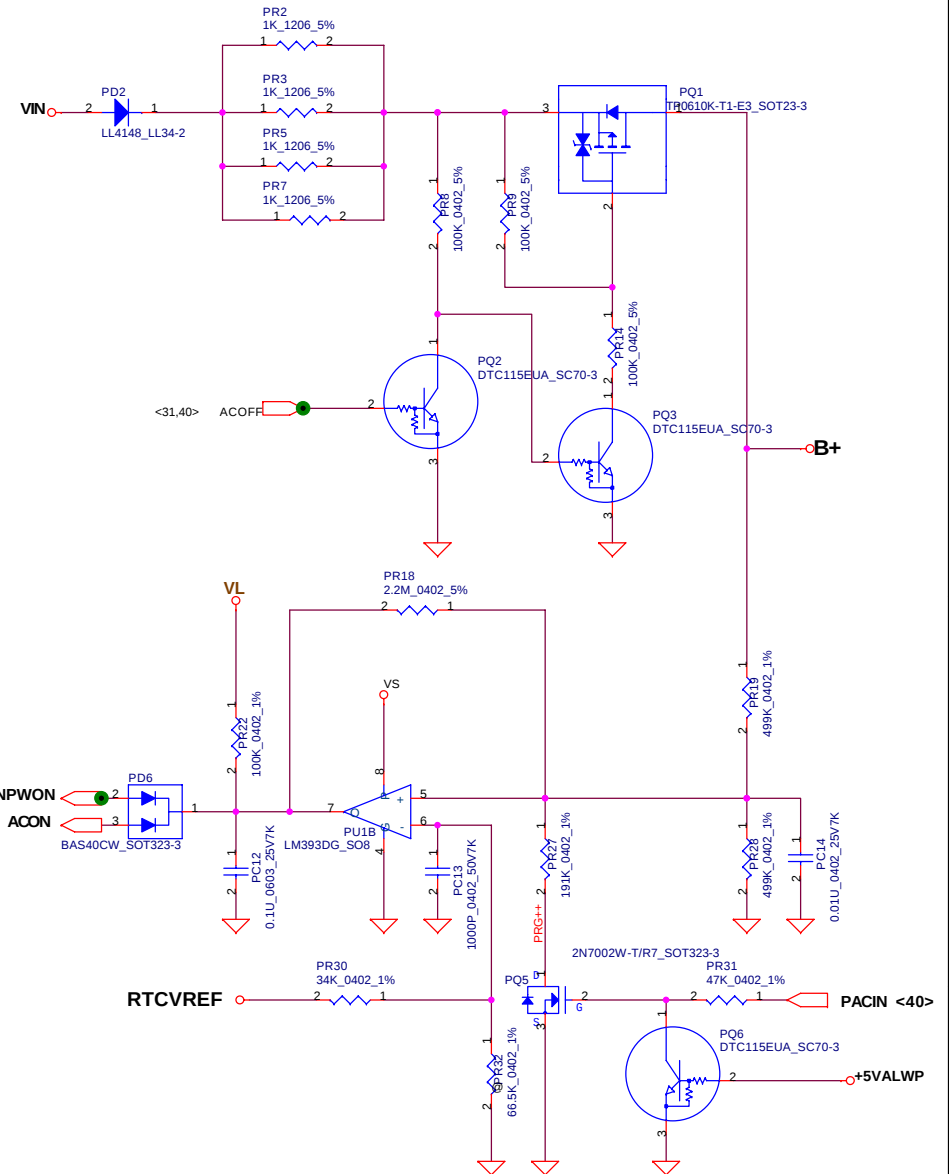
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High	18.764	17.901	17.063
Low	17.745	16.9	16.03

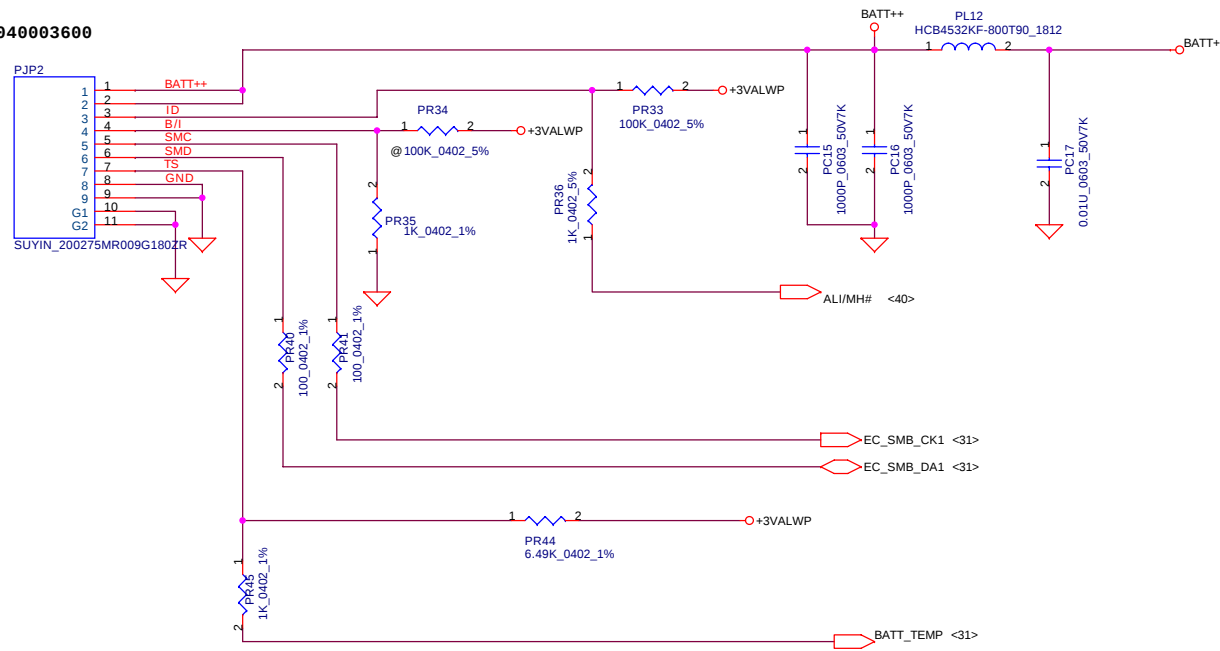
[illegible]

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

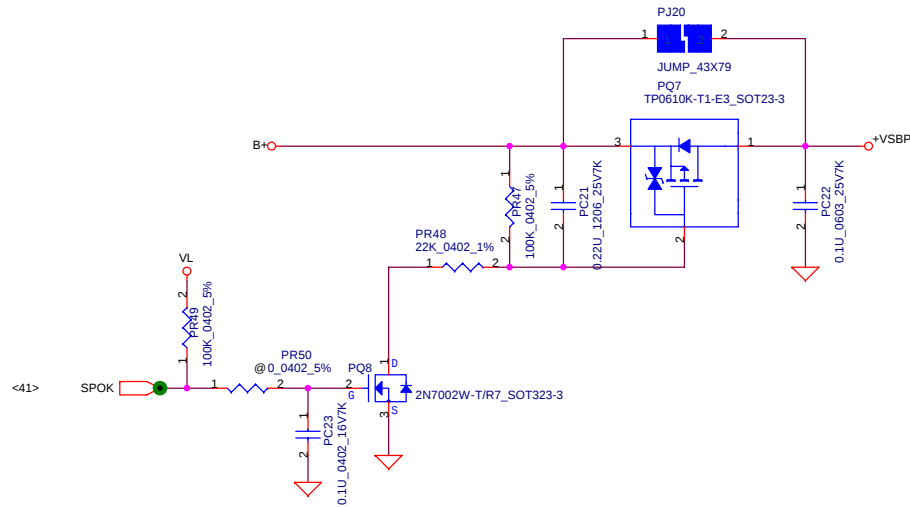
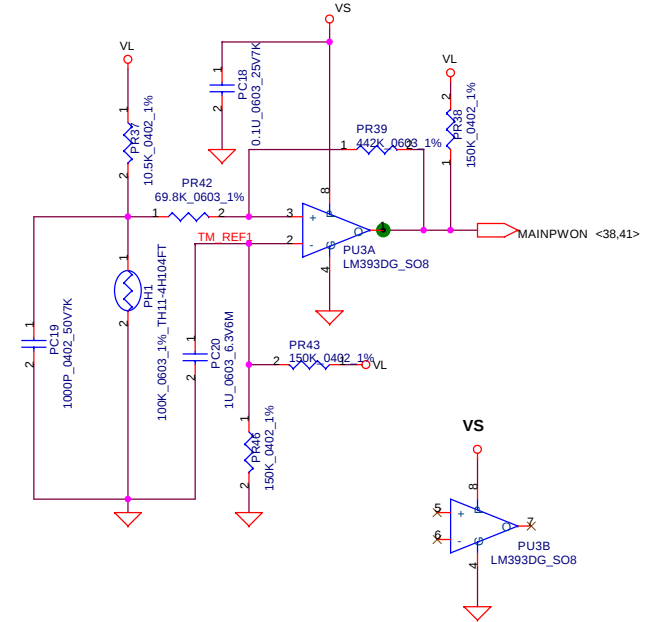
	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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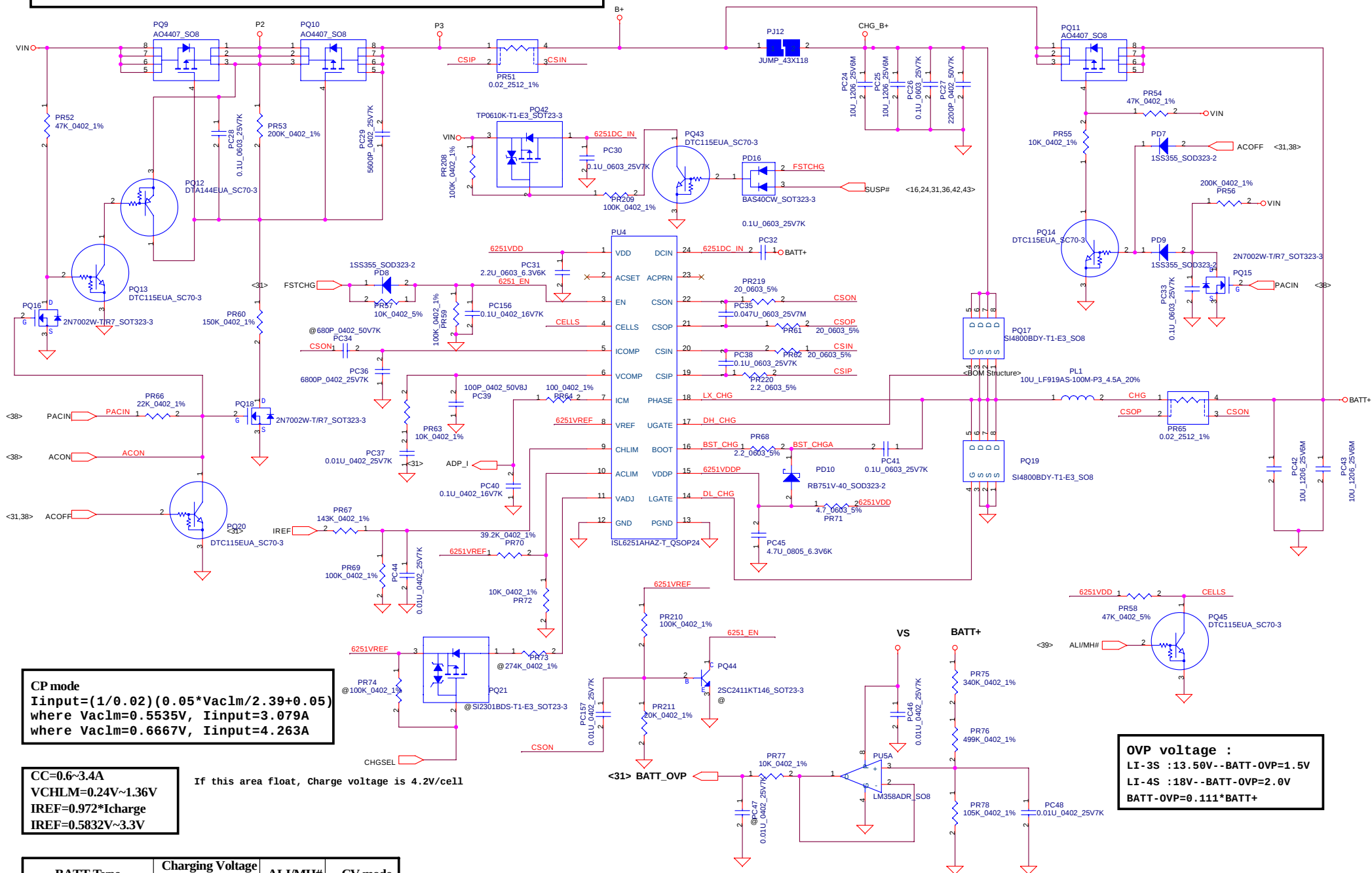
PH1 under CPU bottom side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A

ADP_I = 19.9*Iadapter*Rsense



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 * I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

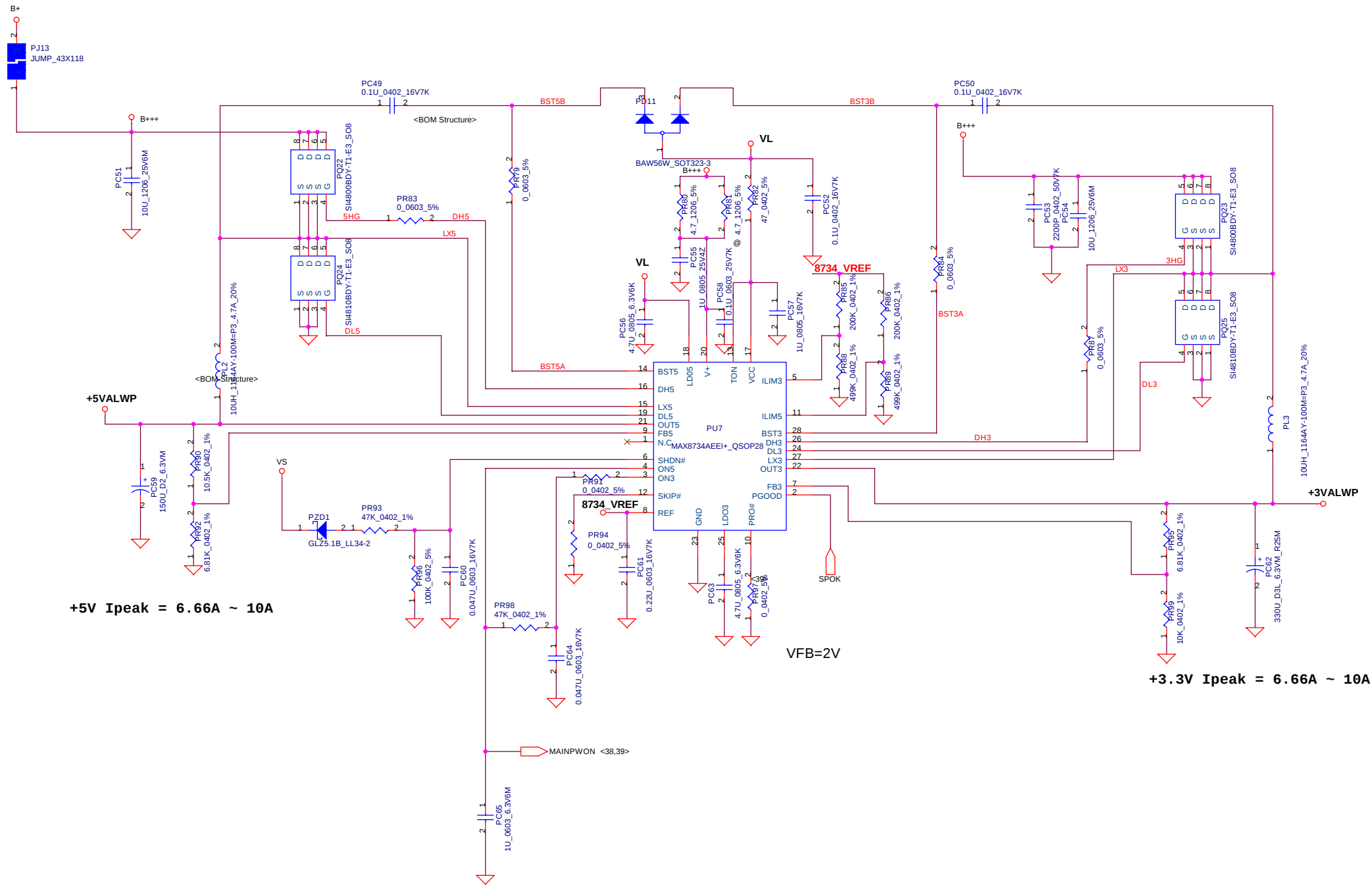
If this area float, Charge voltage is 4.2V/cell

OVP voltage :
 LI-3S : 13.50V -- BATT-OVP=1.5V
 LI-4S : 18V -- BATT-OVP=2.0V
 $BATT-OVP = 0.111 * BATT+$

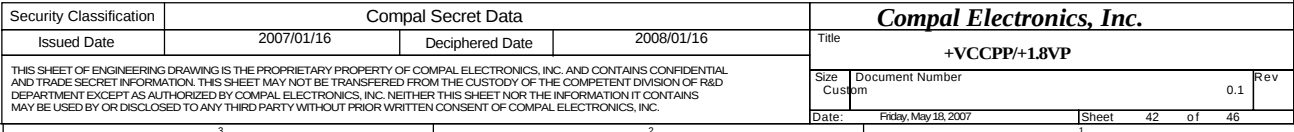
BATT Type	Charging Voltage (0x15)	ALI/MH#	CV mode
4800mAH 3S pack	16800mV	LOW	16.8V
2400mAH 4S pack	12600mV	HIGH	12.60V

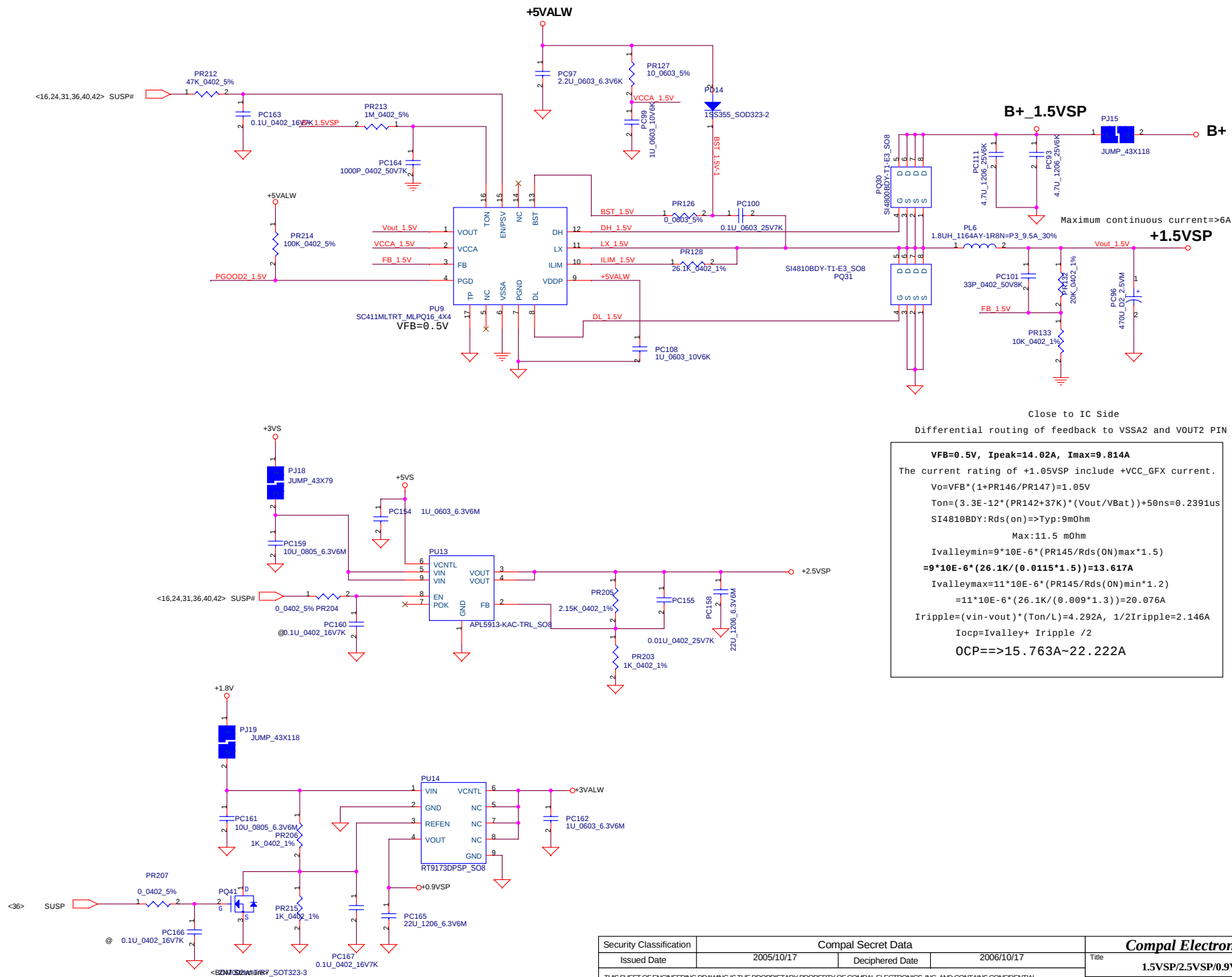
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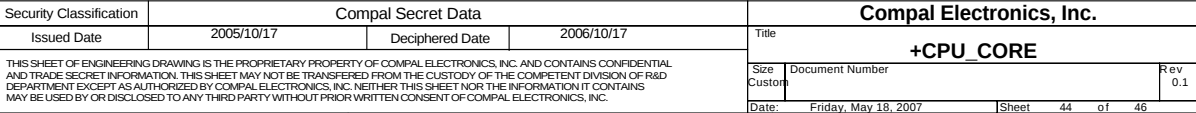


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Version change list (P.I.R. List)

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Item	Fixed Issue	Rev.	PG#	Modify List
1	USB port 2 and 4 can't work	0.2	P.35	Change U17 P/N SA005280110 to SA00001H600
2	Change symbol	0.2	P.20.31	Change Y4 and X1 to SJ132P7K220
3	CRT wave	0.2	P.10	Change L41 to R878 and reserve C619
4	To meet INTEL SPEC	0.2		Change C148.C442.C171.C400.C606.C607 from 2200P to 22N
5	Delete reserve	0.2	P.17	Delete R71,74 Delete C171
6	FACTORY REQUEST	0.2	P.35	Delete JP5 PIN3
7	To meet CRT SPEC	0.2	P.18	Remove C7
8	Tune frequency	0.2	P.28	Change C511;515 from 27p to 18p
9	EMI Request	0.2		change C632 to 2.2nF Remove R441,R145,C6,12,13, change L2,3,4 to SM01000AL00
10	EMI Request	0.2	P.30	LAN RX TX change
11	EMI Request	0.2	P.32	ADD D22;23;24
12	EMI Request	0.2	P.4	Delete ITP_BPM0-5 and R515
13	FAN issue	0.2	P.4	Change R276 from 10k to 1k ohm C341 from 1000p to 100p
14	USB issue	1.0	P.21	Change USB port 2 to NEW card port 7 to USB Change R322 to 22 ohm
15	Remove LPC debug connect	1.0	P.33	Remove JP13,R265,R441,R145
16	ESD Request and reserve	1.0		ADD T48 AND R515 AND JP9 29,30 pin to GND
17	Power improve	1.0	P.6	RemoveC26, 31, 314, 315
18		0.2		
19		0.2		
20		0.2		

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