

12/21 Add PJP1 for DCIN Cable on 45 Level
One for 14W DCIN , PN: DC301001Y00
Another for 15W DCIN , PN: DC301001V00

05/20 Add DAZ PCB Panel P/N

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JHXXX Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

(With nVIDIA MXM/B)

2008-06-03

REV: 1.0

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File Name : LA-4241P

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	ID1	ID0
JHT00 (00@)	R361	R357
JHT01 (01@)	R361	R355
JHL90 (10@)	R360	R357
JHL91 (11@)	R360	R355

MIC ID Table

R	Structure
R585 Single MIC	SINGLE@
R583 Array MIC	DUAL@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH9M SM Bus address

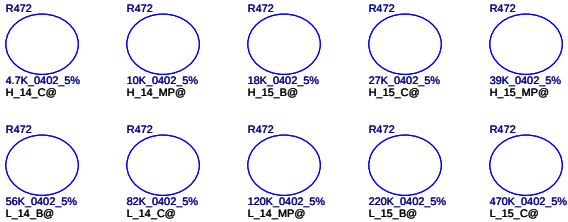
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%
Rb	47K +/- 5%

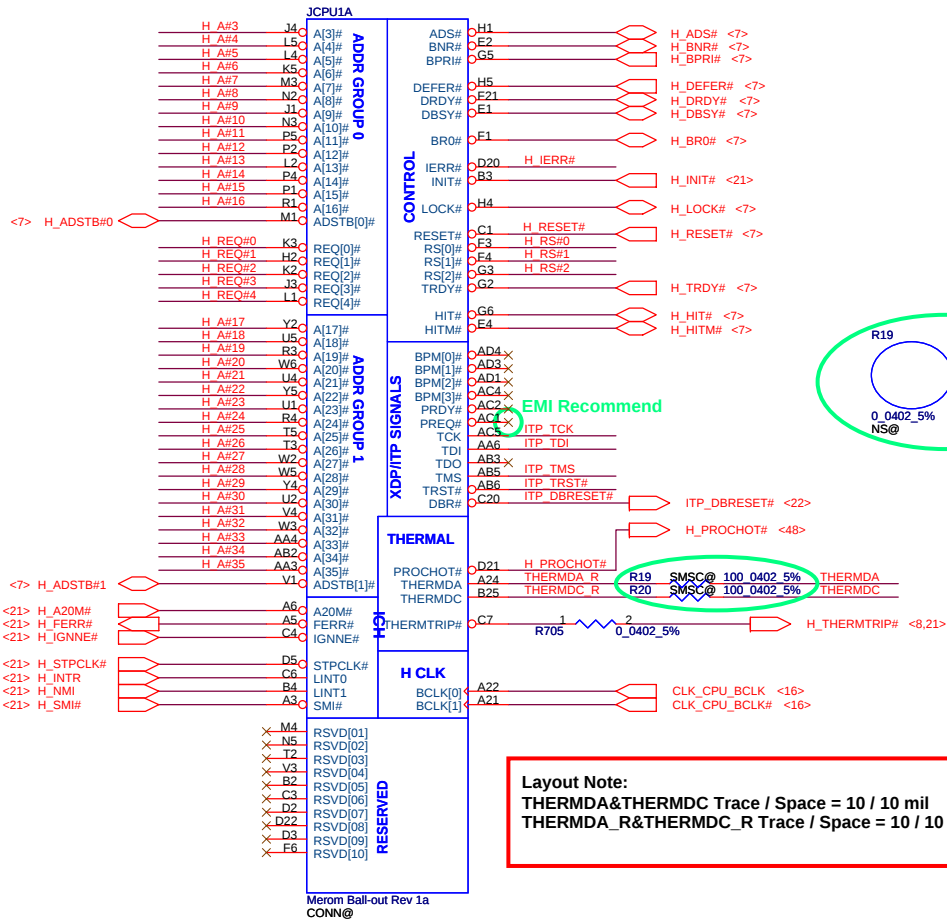
Rb~ R470

Ra~ R472



Board ID	Rb	Ra	VAD_BID min	VAD_BID typ	VAD_BID max	Ra BOM Structure
1	NA	4.7K +/- 5%	0 V	0 V	0 V	H_14_B@
2	47K(RB@)	4.7K +/- 5%	0.274 V	0.300 V	0.328 V	H_14_C@ ✓
3	47K(RB@)	10K +/- 5%	0.553V	0.578 V	0.628 V	H_14_MP@
4	47K(RB@)	18K +/- 5%	0.849V	0.913V	0.981 V	H_15_B@
5	47K(RB@)	27K +/- 5%	1.129 V	1.204 V	1.282 V	H_15_C@ ✓
6	47K(RB@)	39K +/- 5%	1.415 V	1.496 V	1.579 V	H_15_MP@
7	47K(RB@)	56K +/- 5%	1.712 V	1.794 V	1.876 V	L_14_B@
8	47K(RB@)	82K +/- 5%	2.020V	2.097 V	2.173 V	L_14_C@ ✓
9	47K(RB@)	120K +/- 5%	2.303 V	2.371 V	2.437 V	L_14_MP@
10	47K(RB@)	220K +/- 5%	2.670 V	2.719 V	2.765 V	L_15_B@
11	47K(RB@)	470K +/- 5%	2.972 V	3.000 V	3.026 V	L_15_C@ ✓
12	47K(RB@)	NA	3.135 V	3.300 V	3.465 V	NA for L_15_MP

<7> H_A# [3..35]
 <7> H_REQ# [0..4]
 <7> H_RS# [0..2]

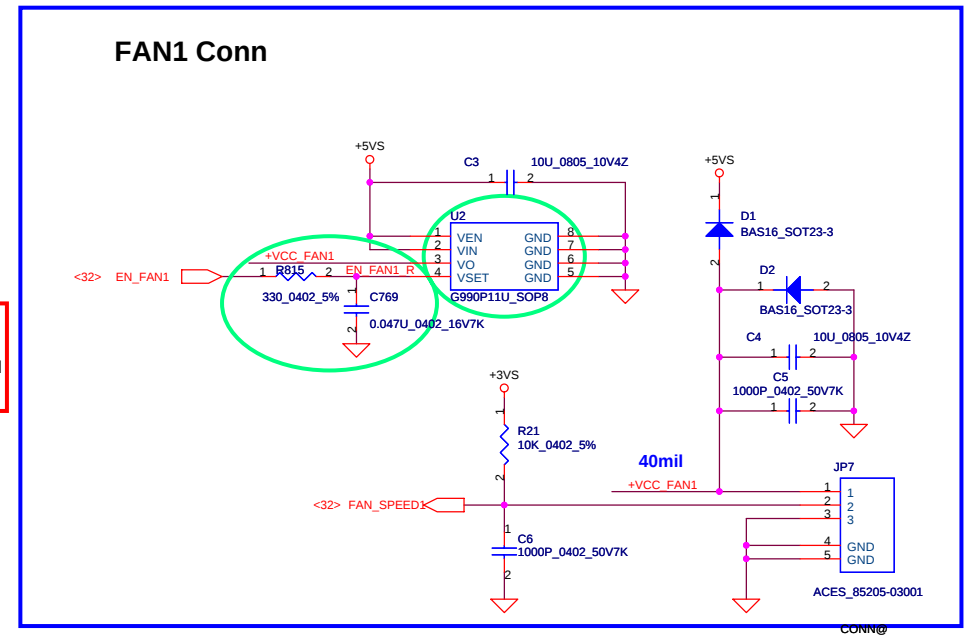
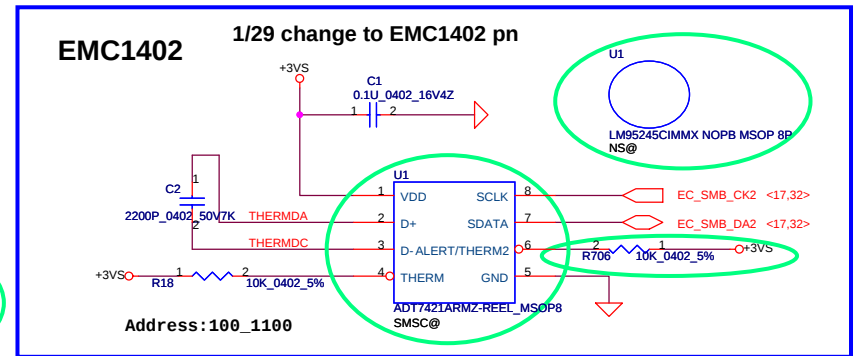


Which to follow?

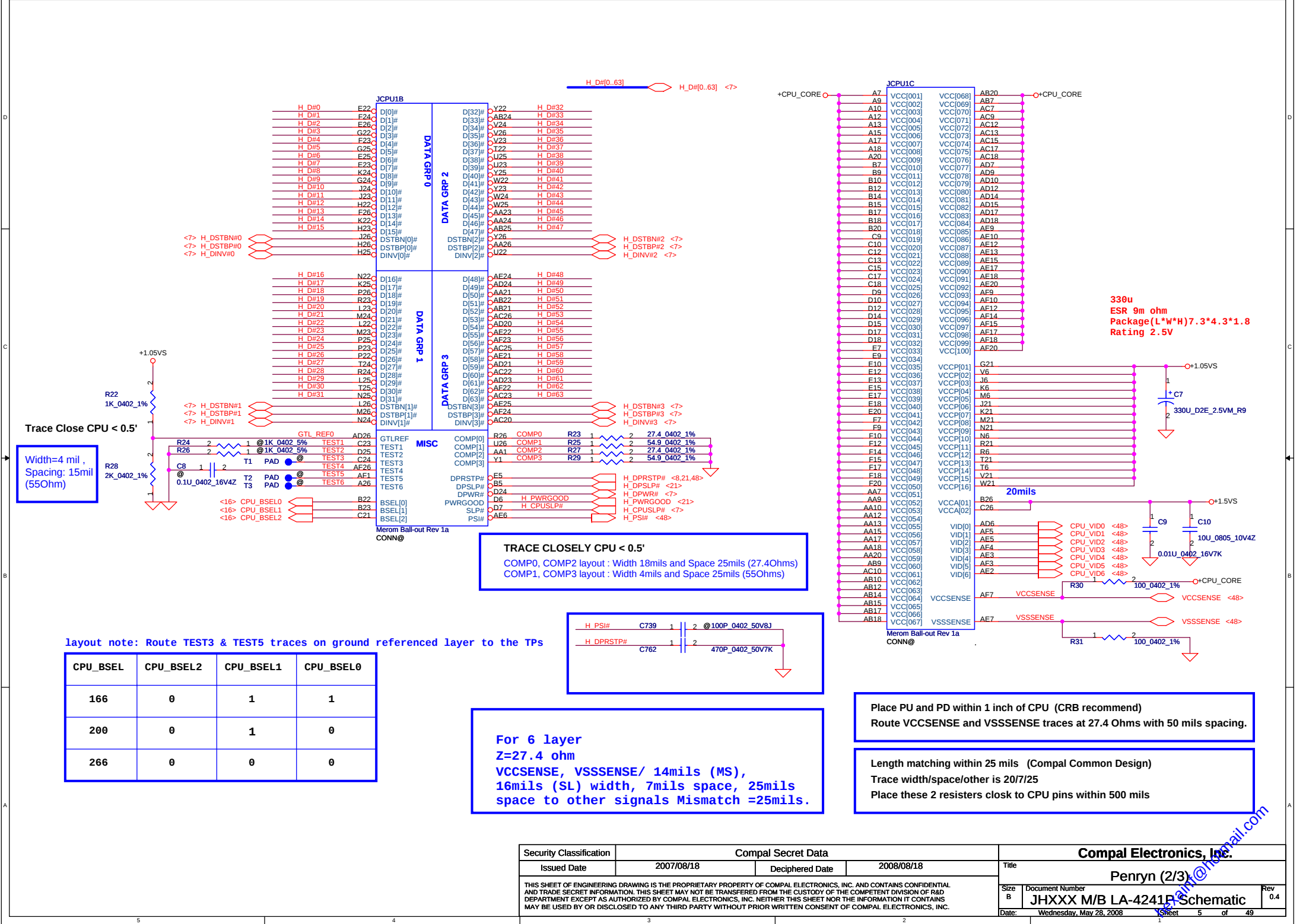
	Checklist	CRB
TCK	55.5%	54.9 1%
TDI	55.5%	54.9 1%
TMS	55.1%	54.9 1%
TRST#	55.5%	54.9 1%
PREQ#	X	54.9 1%

EMI Recommend

H_IERR#	R12	1	2	56.0402 5%
ITP_TMS	R13	1	2	54.9 0402 1%
ITP_TDI	R14	1	2	54.9 0402 1%
H_PROCHOT#	R15	1	2	56.0402 5%
ITP_TCK	R16	1	2	54.9 0402 1%
ITP_TRST#	R17	1	2	54.9 0402 1%



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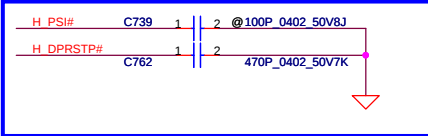


Width=4 mil ,
Spacing: 15mil
(55Ohm)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

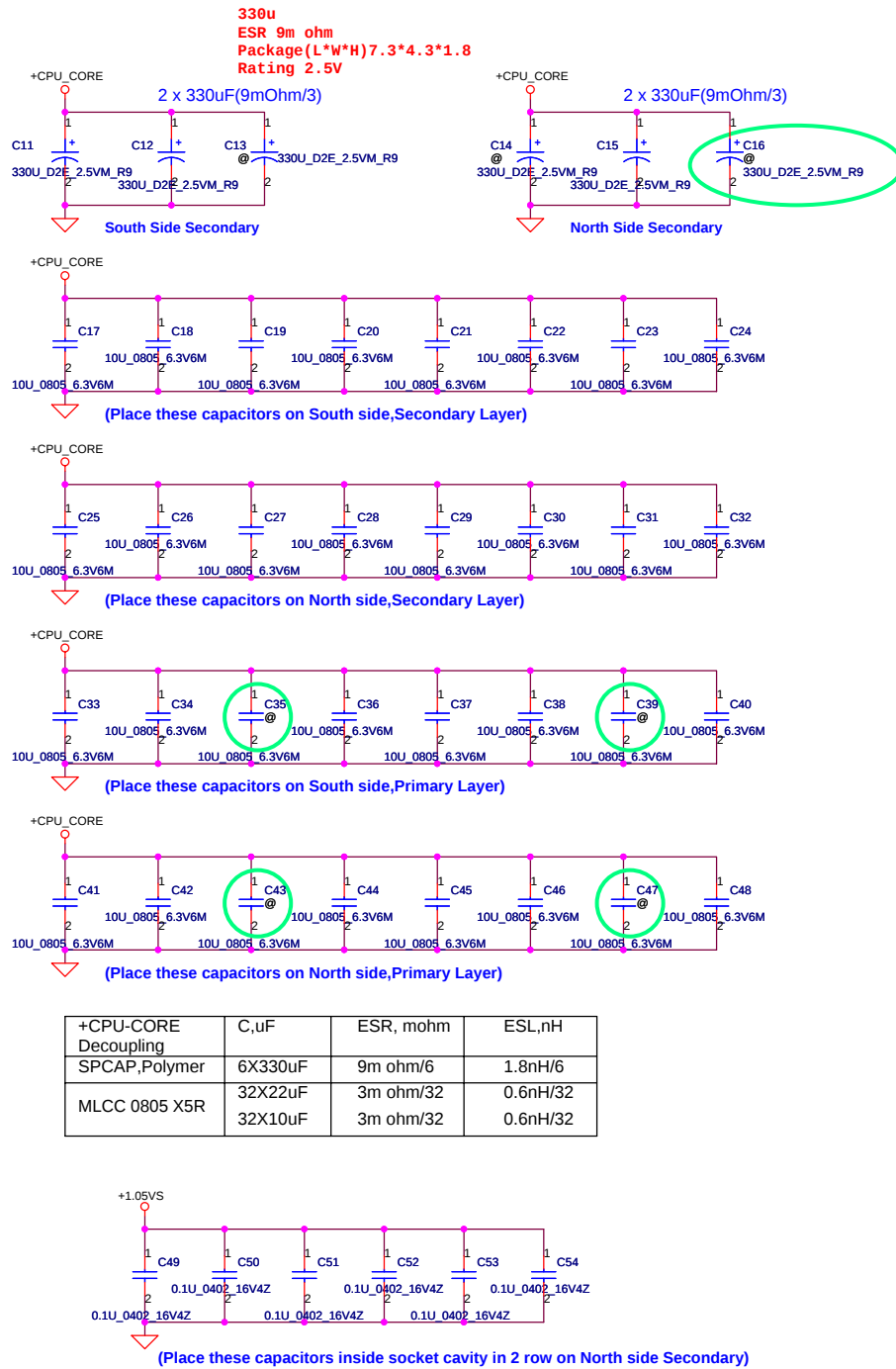
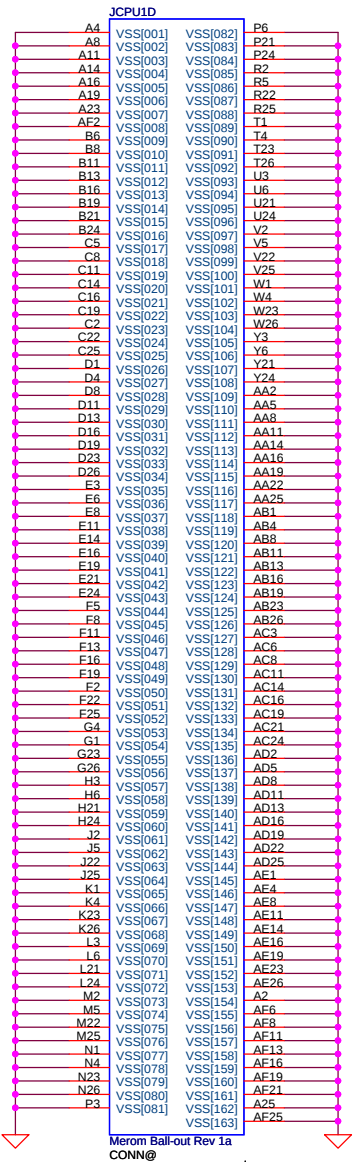


For 6 layer
Z=27.4 ohm
VCCSENSE, VSSSENSE/ 14mils (MS),
16mils (SL) width, 7mils space, 25mils
space to other signals Mismatch =25mils.

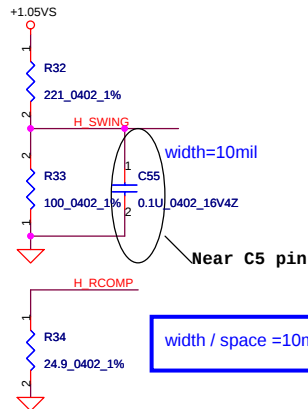
Place PU and PD within 1 inch of CPU (CRB recommend)
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mils spacing.

Length matching within 25 mils (Compal Common Design)
Trace width/space/other is 20/7/25
Place these 2 resistors close to CPU pins within 500 mils

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								3		2		1			

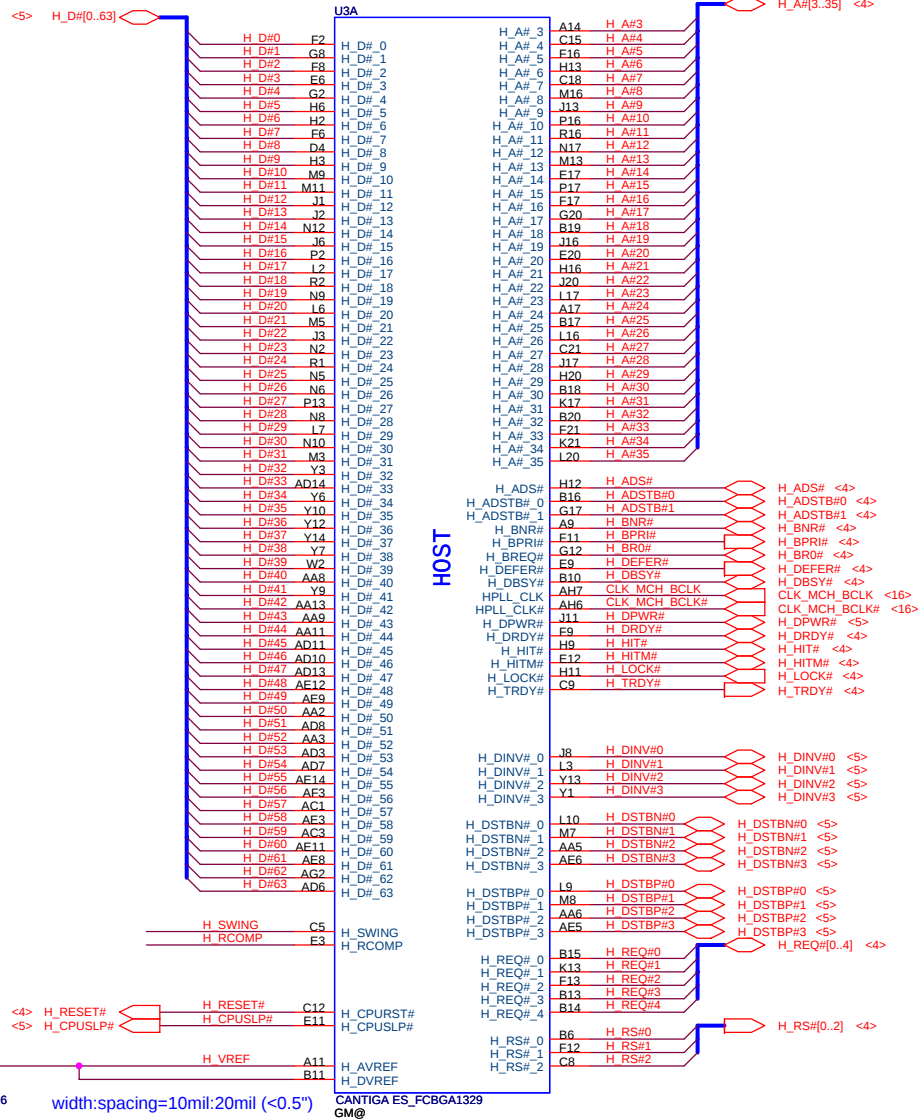
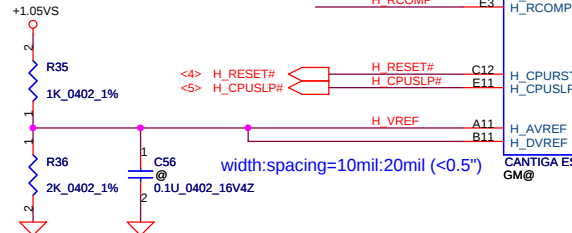


Change U3 from SA00001P900 to SA00001P930
3/4 Change U3 from SA00001P930 to SA00002JT10 (B0 to B2)



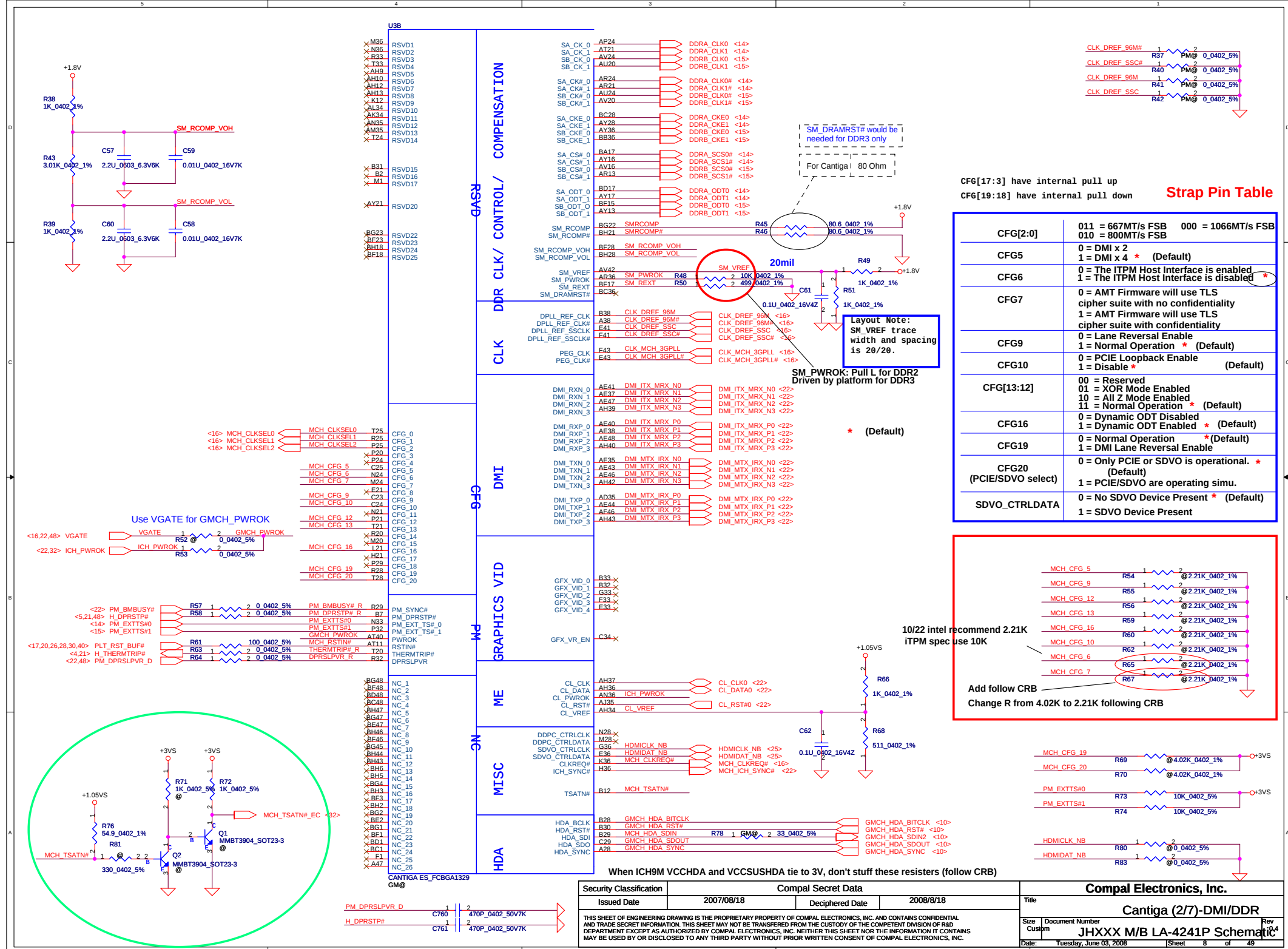
width / space = 10mil / 20mil

Layout Note:
H_RCOMP / H_VREF / H_SWING
trace width and spacing is 10/20



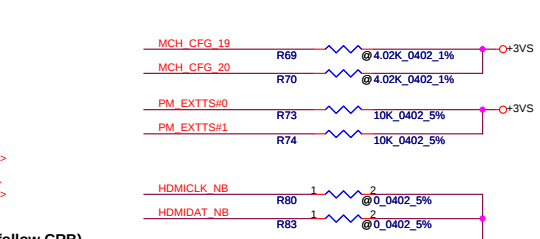
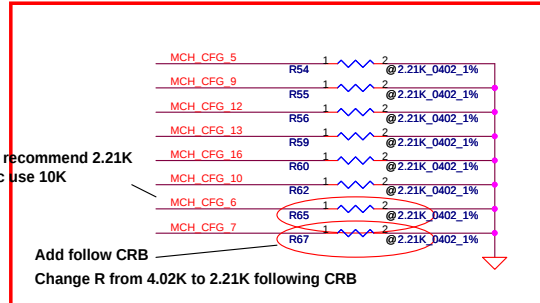
3/4 Change U3 PM@ from SA00001Z030
to SA00002JJ00 (B0 to B2)

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Strap Pin Table

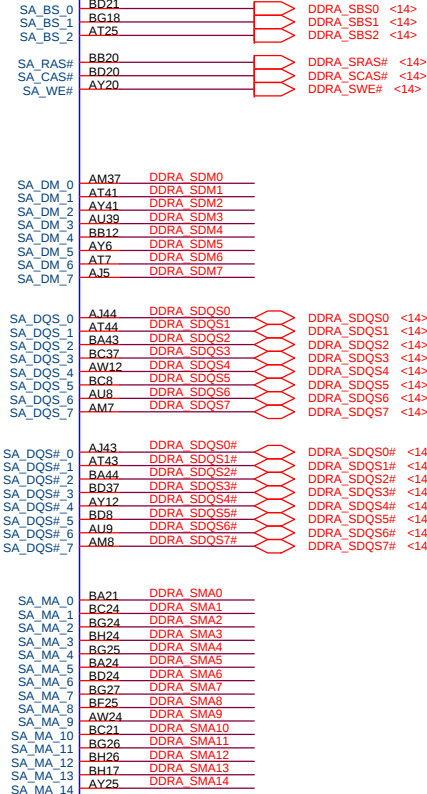
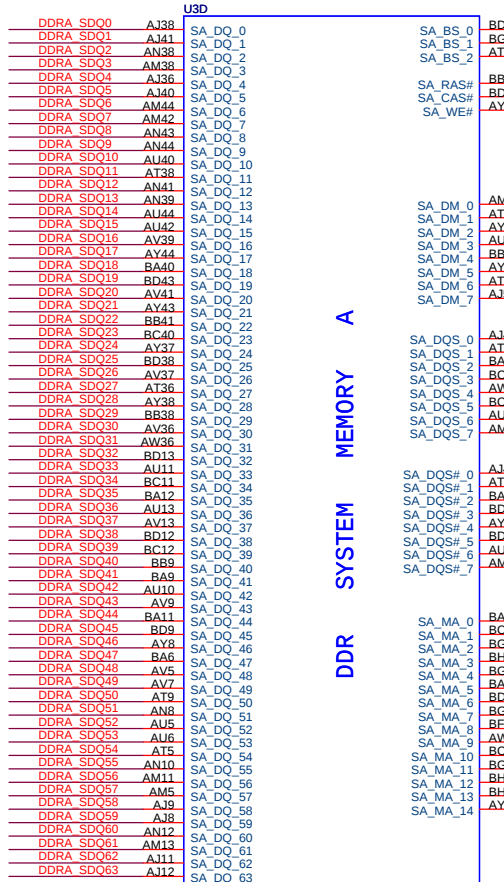
CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB 0 = DMI x 2 1 = DMI x 4 * (Default)
CFG5	0 = The ITPM Host Interface is enabled 1 = The ITPM Host Interface is disabled *
CFG6	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality
CFG7	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG9	0 = PCIE Loopback Enable 1 = Disable * (Default)
CFG10	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG13:12	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG16	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG19	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
CFG20 (PCIE/SDVO select)	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
SDVO_CTRLDATA	



Title		Cantiga (2/7)-DMI/DDR	
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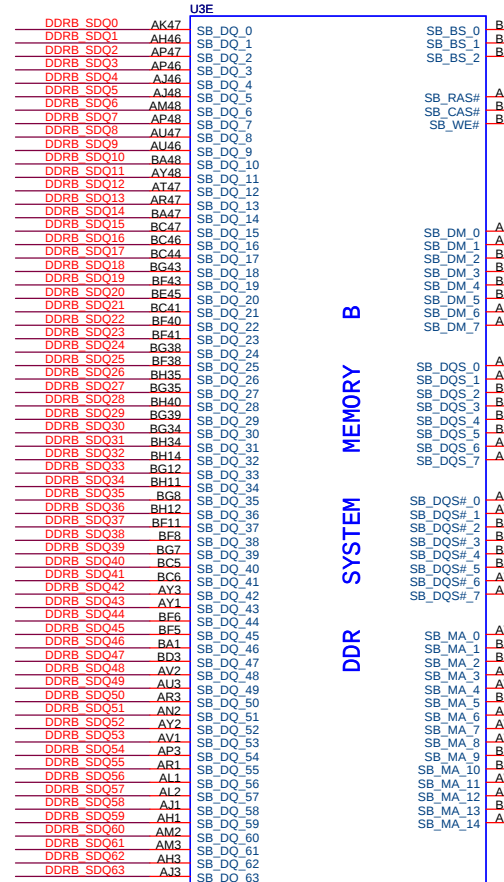
<14> DDRA_SDQ[0..63] <14> DDRA_SDM[0..7] <14> DDRA_SMA[0..14]

<15> DDRB_SDQ[0..63] <15> DDRB_SDM[0..7] <15> DDRB_SMA[0..14]



DDR SYSTEM MEMORY A

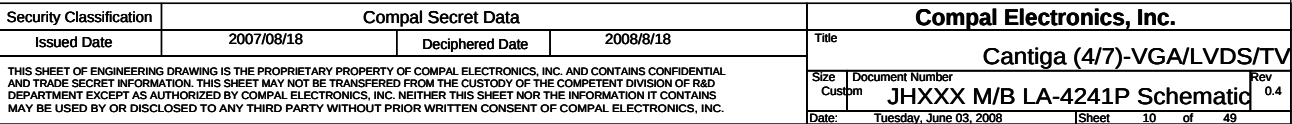
GM@ CANTIGA ES_FCBGA1329

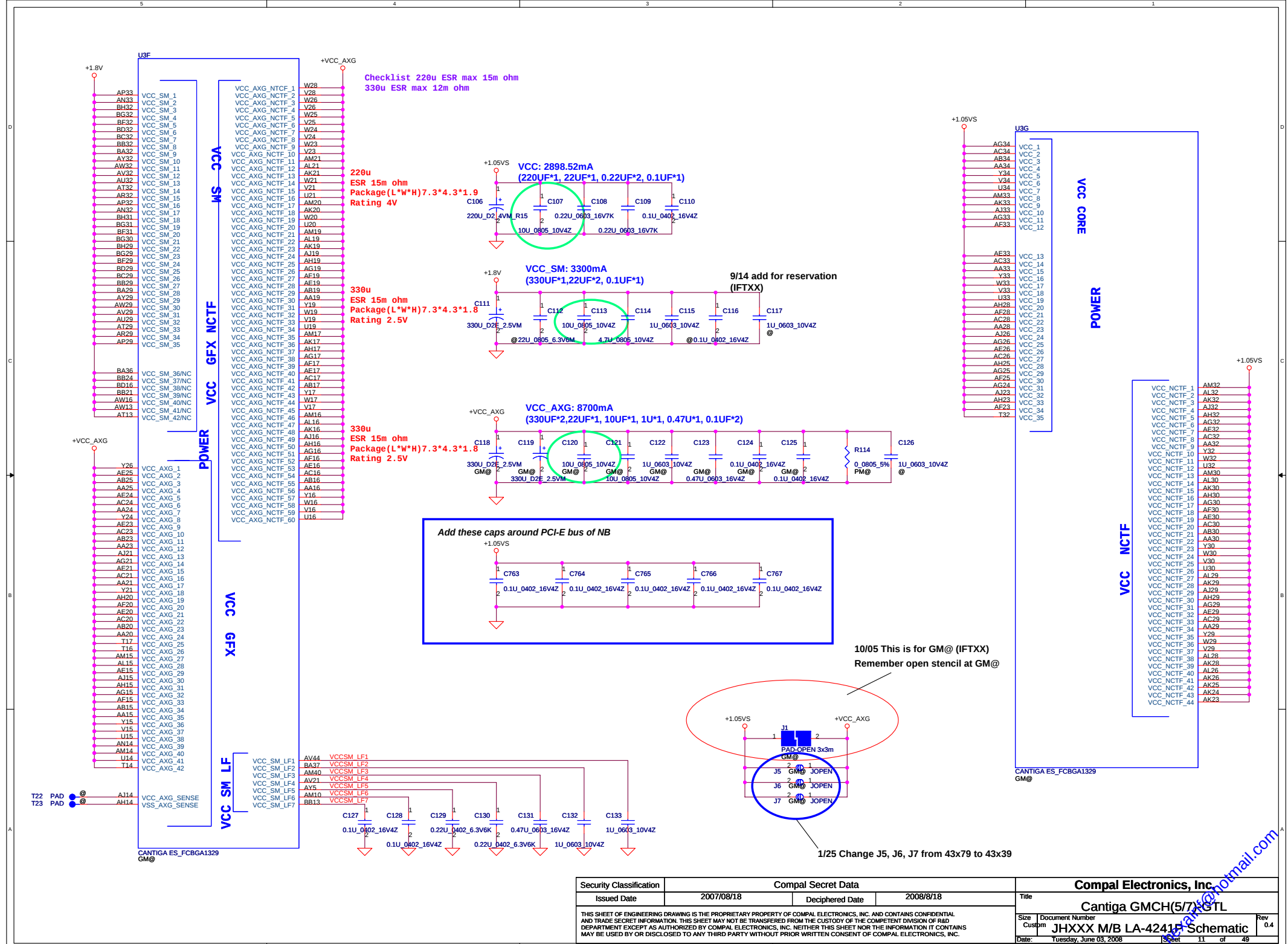


DDR SYSTEM MEMORY B

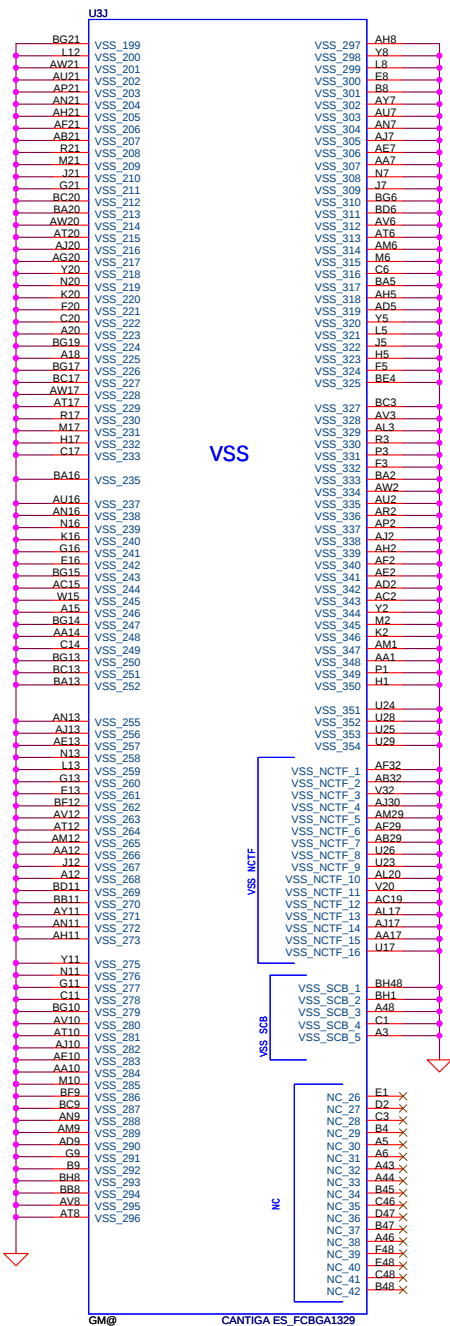
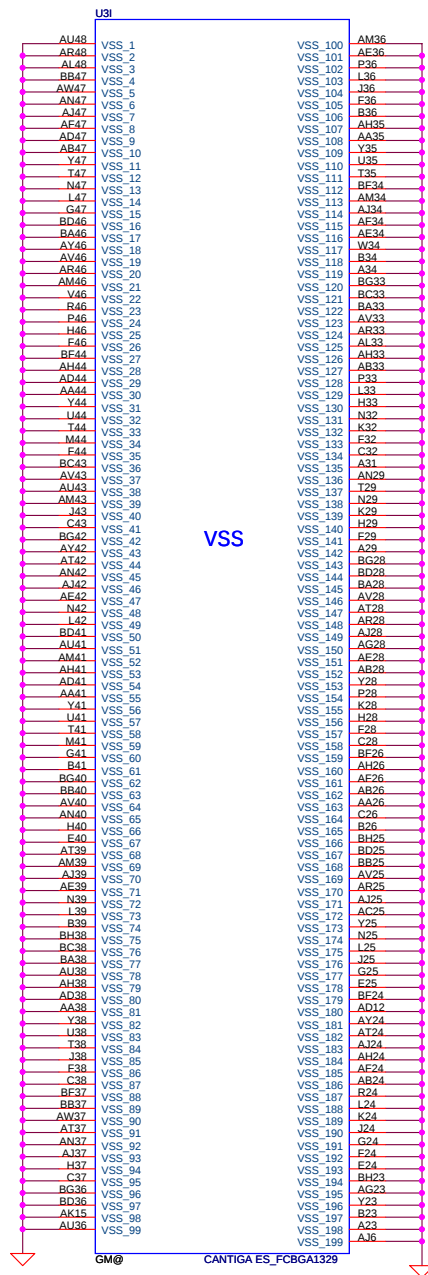
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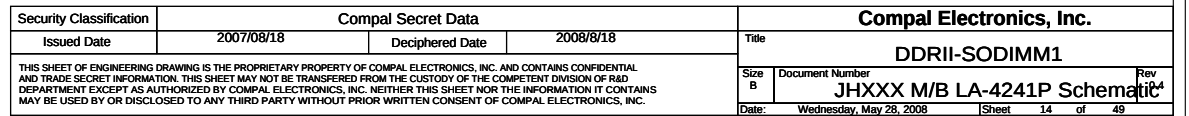


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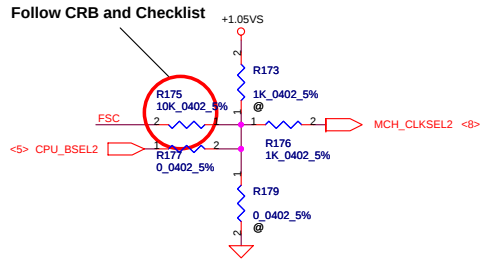
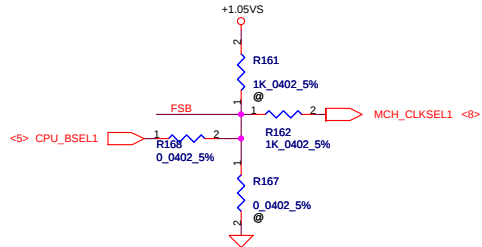
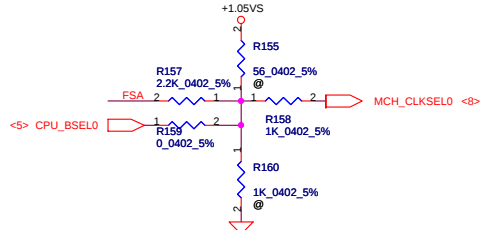
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DIMM1 STD H:5.2mm (BOT)



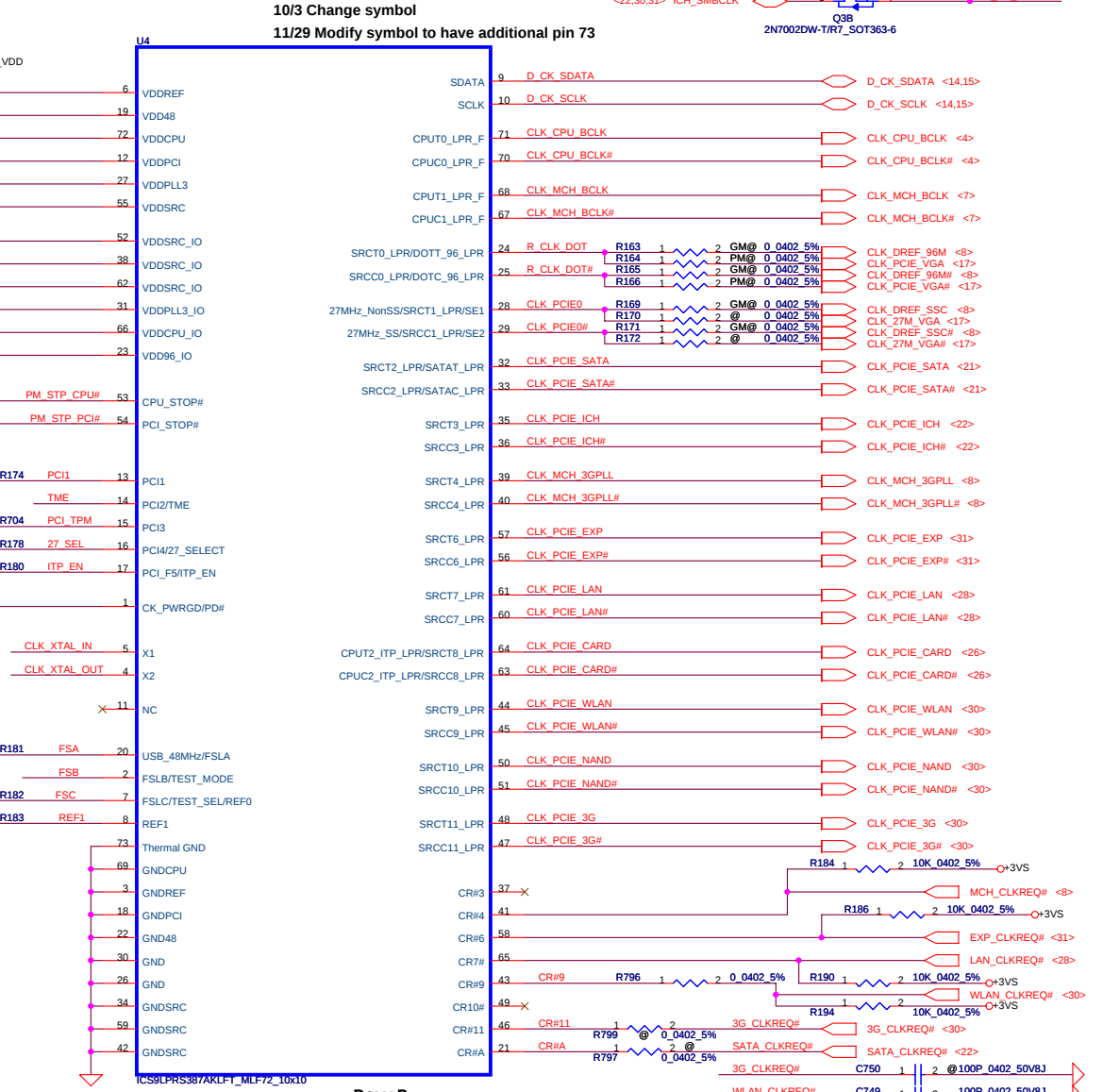
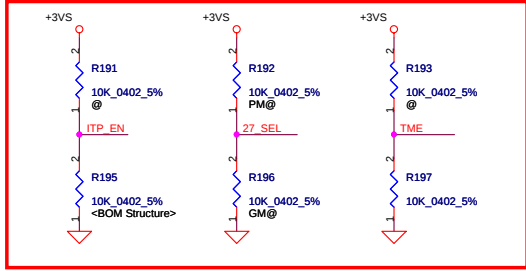
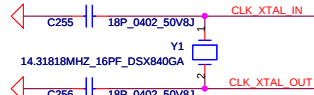
DIMM2 STD H:9.2mm (BOT)

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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ
0	1	1	166.6	100	33.3
0	1	0	200	100	33.3
0	0	0	266.6	100	33.3

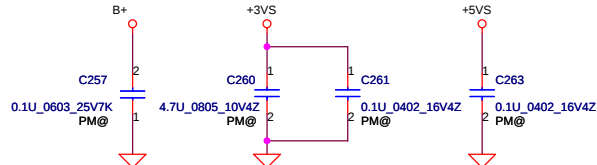
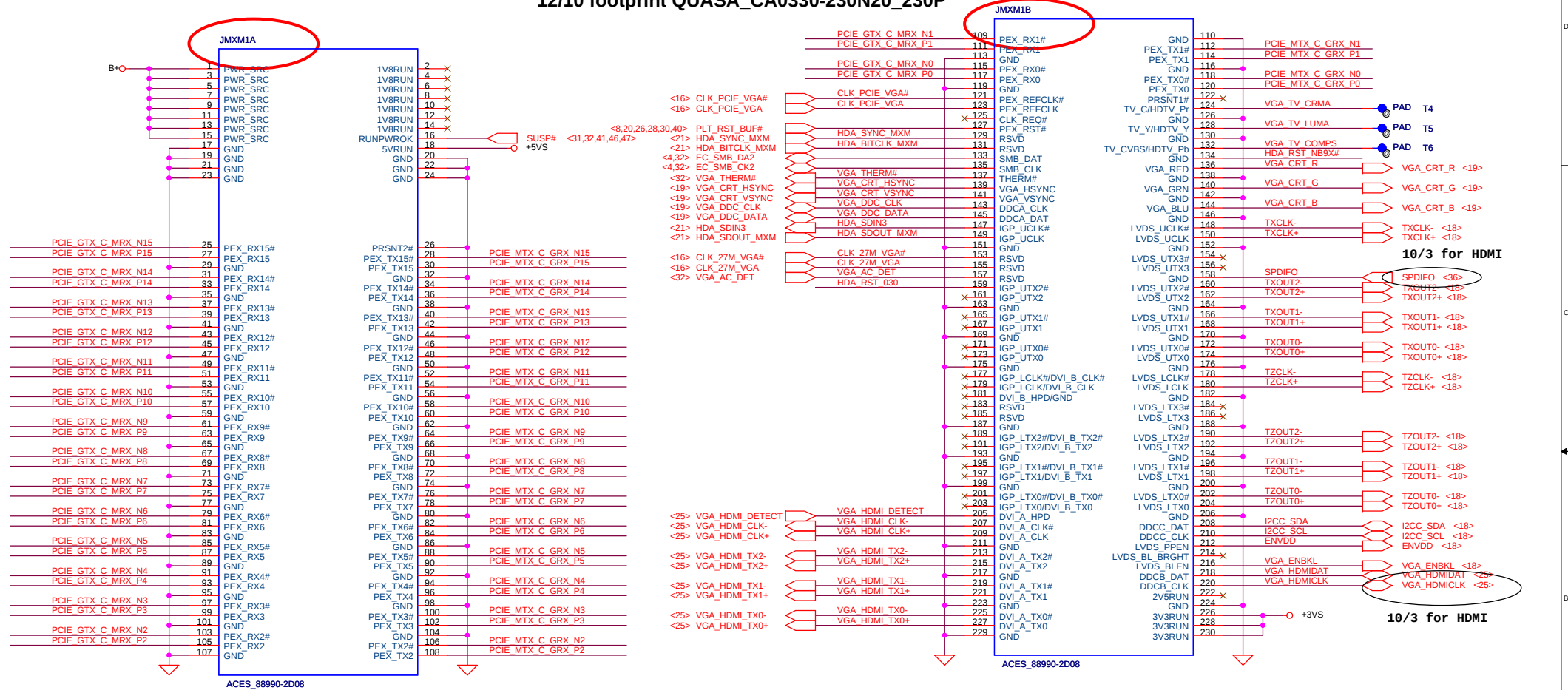
For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For TME, 0 = Overclocking of CPU and SRC allowed
1 = Overclocking of CPU and SRC NOT allowed



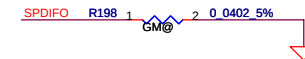
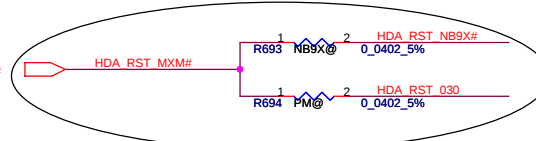
Security Classification	Compal Secret Data	Deciphered Date	2008/8/18
Issued Date	2007/08/18	Deciphered Date	2008/8/18
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Rev: B			
Title			
Size			
Document Number			
JHXXX M/B LA-4241P Schematic			
Date			
Wednesday, May 28, 2008			
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16 of 49			

<10,25> PCIE_MTX_C_GRX_N[0..15]  PCIE_MTX_C_GRX_N[0..15]
<10,25> PCIE_MTX_C_GRX_P[0..15]  PCIE_MTX_C_GRX_P[0..15]
<10> PCIE_GTX_C_MRX_N[0..15]  PCIE_GTX_C_MRX_N[0..15]
<10> PCIE_GTX_C_MRX_P[0..15]  PCIE_GTX_C_MRX_P[0..15]

9/13 modify this footprint from ACES_88990-2D08_230P to ACES_88990-2D28_230P
12/19 modify this footprint from ACES_88990-2D28_230P to QUASA_CA0330-230N20_230P
0208 : Modify this footprint from QUASA_CA0330-230N20_230P to QUASA_CA0330-230N20_230P-S
12/10 footprint QUASA_CA0330-230N20_230P



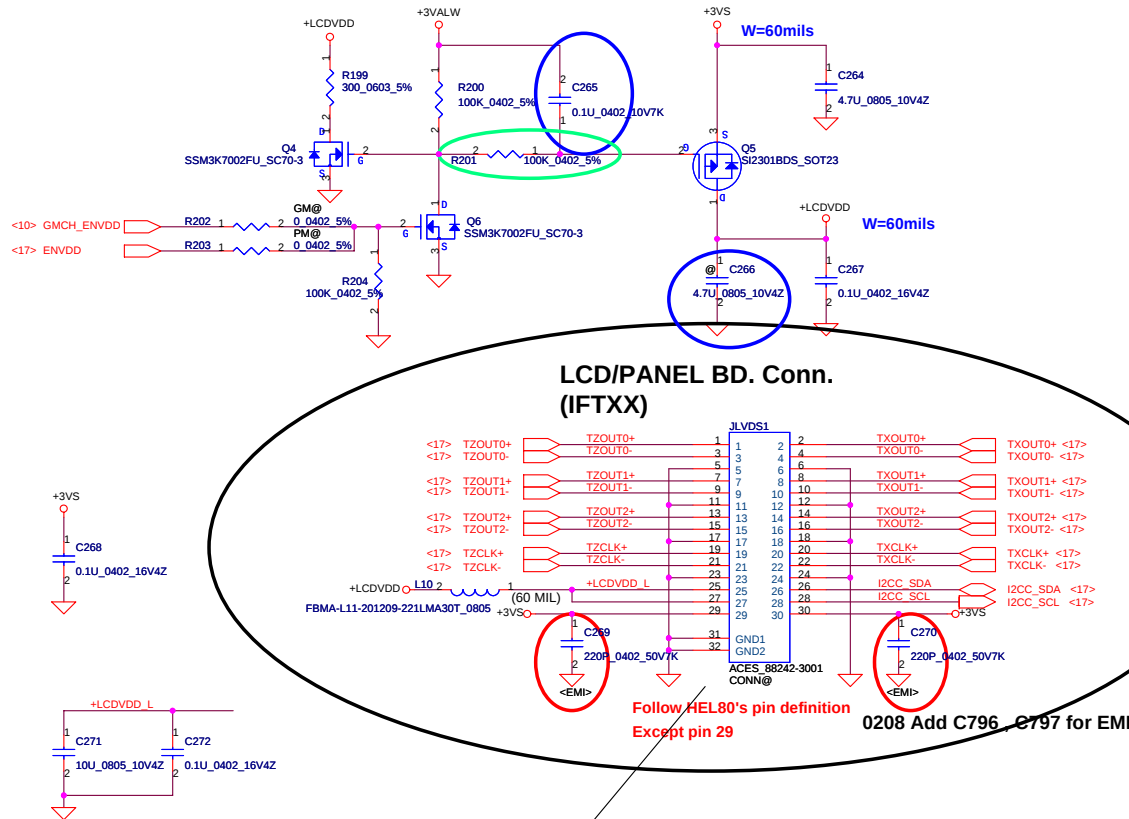
<21> HDA_RST_MXM#



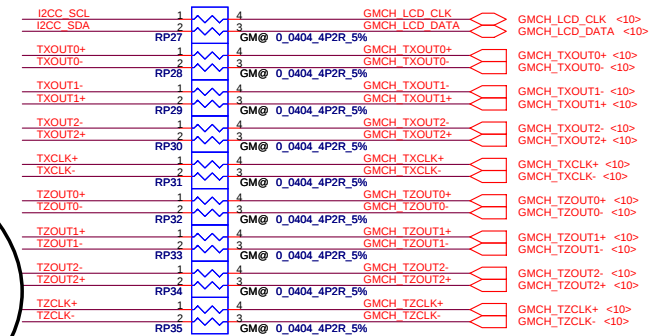
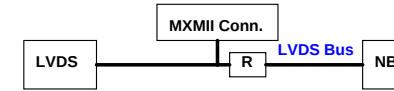
	R693	R694
NB9X	Mount	No stuff
030 NB9X	No stuff	Mount
NB8X	No stuff	No stuff

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2007/08/18	Deciphered Date	2008/8/18	MXM Connector			
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				Size	Document Number	Rev	
				Custom	JHXXX M/B LA-4241P Schematic		
				Date:	Wednesday, May 28, 2008	Sheet	17 of 49

LCD POWER CIRCUIT

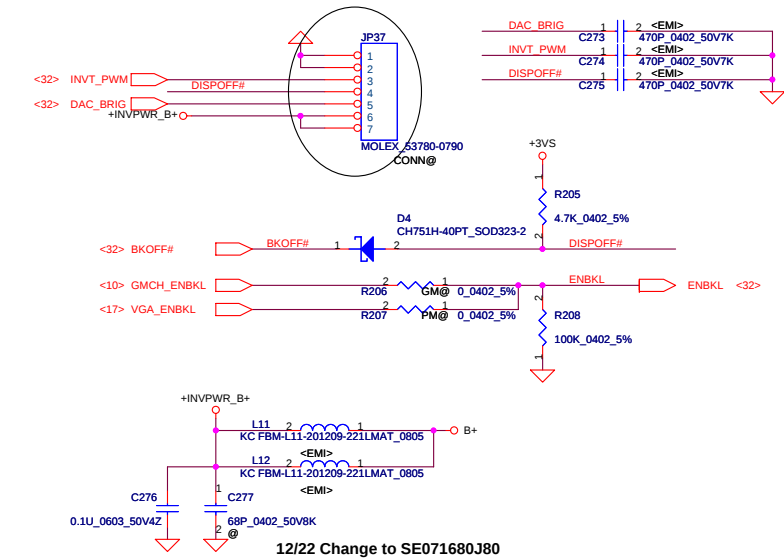


Routing Diagram



INVERTER Conn.

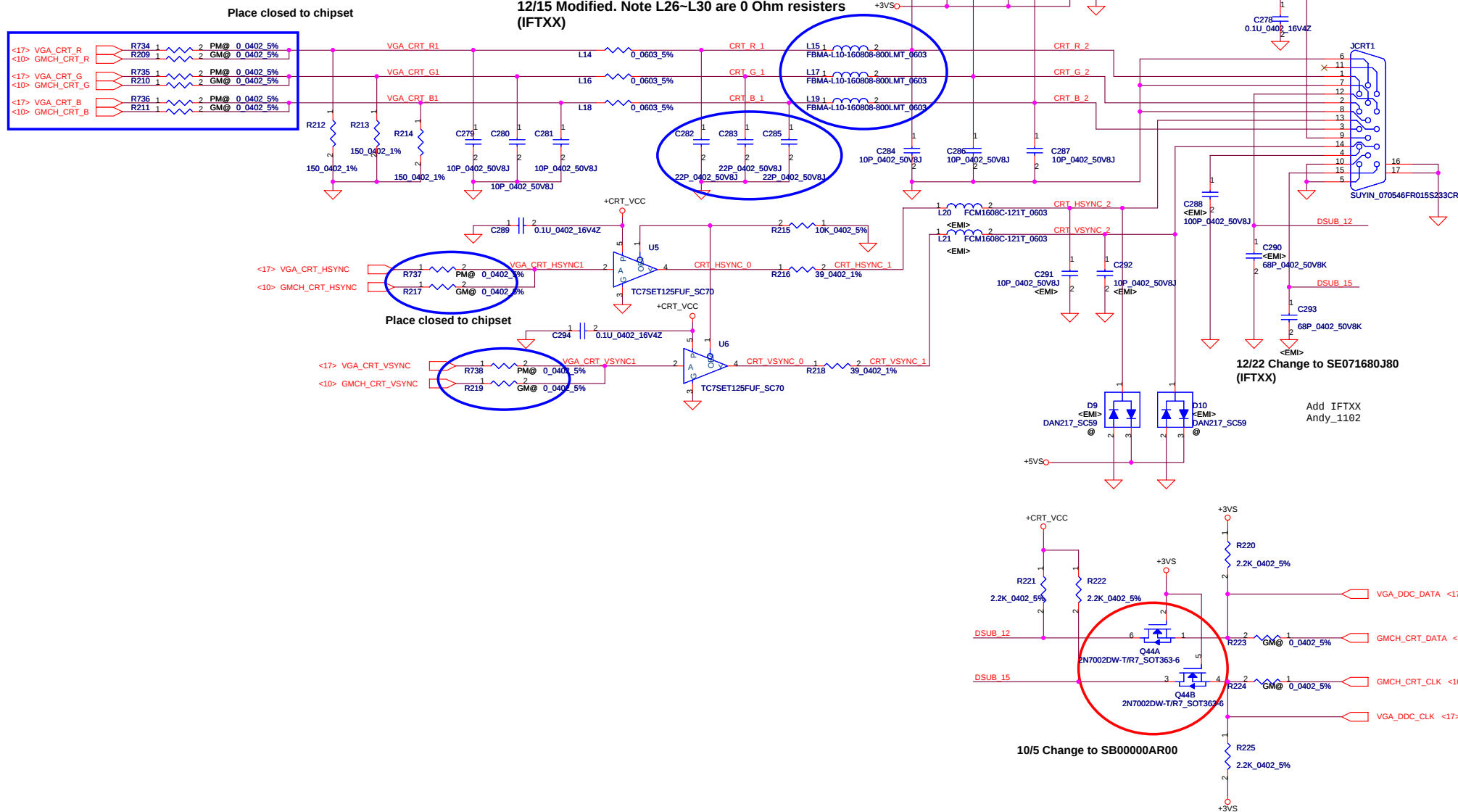
12/18 modified from 220p @ to 470p mount by EMI request



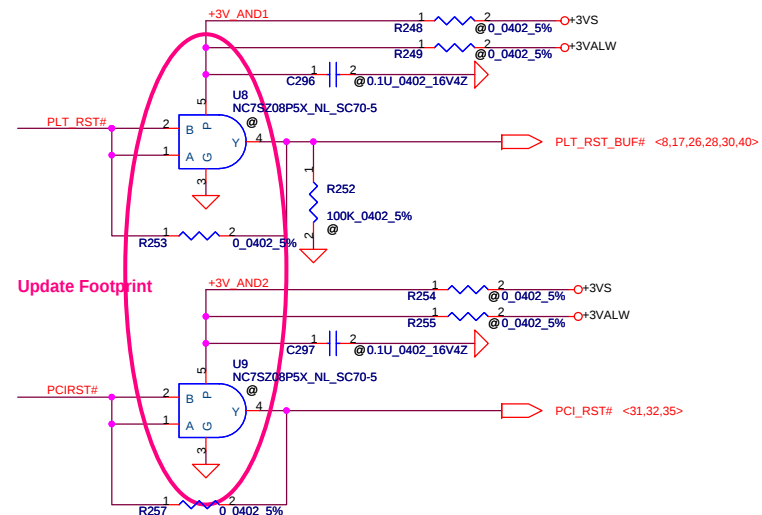
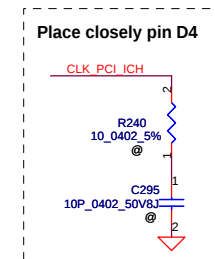
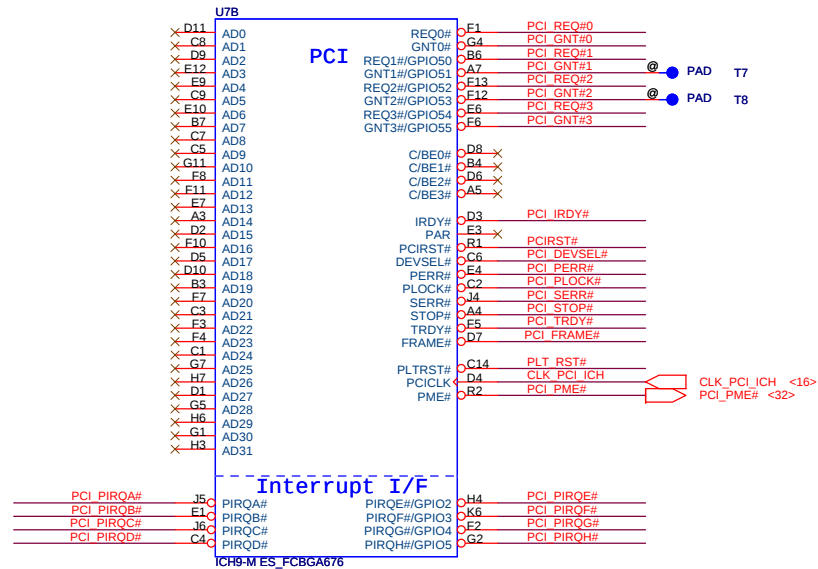
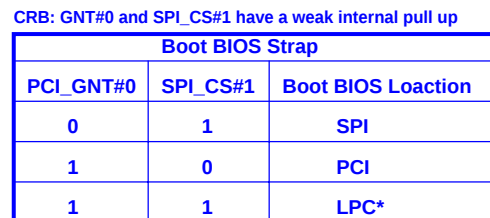
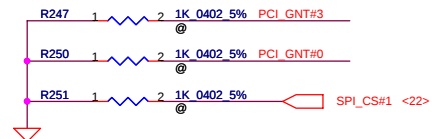
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/18	Deciphered Date	2008/08/18	LVDS & DVI Connector	
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				JHXXX M/B LA-4241P Schematic	
				Date:	Wednesday, May 28, 2008
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CRT Connector

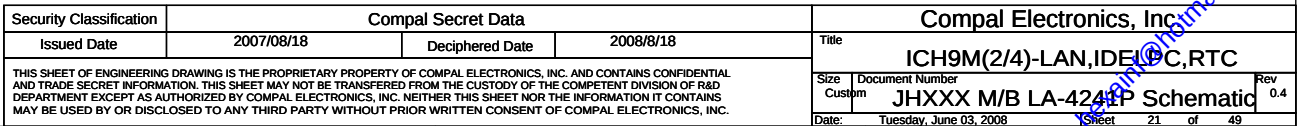
Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

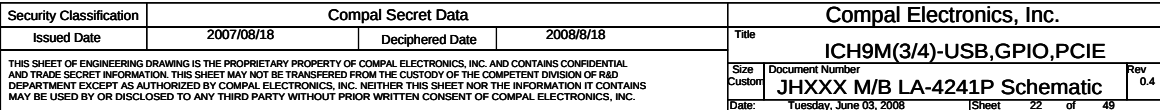


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Issued Date		2007/08/18		Deciphered Date		2008/8/18		Title							
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								Size B	Document Number			JHXXX M/B LA-4241P Schematic			Rev 04
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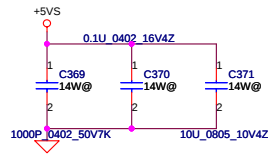


Security Classification	Compal Secret Data			Compal Electronics, Inc.				
Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title ICH9M(1/4)-PCI				
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				JHXXX M/B LA-4241P Schematic			0.4	
				Date:	Tuesday, June 03, 2008	Sheet	20	of





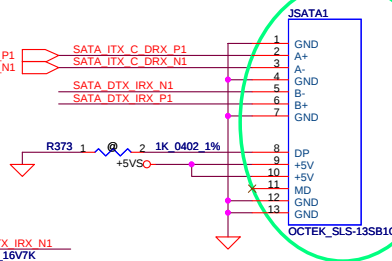
14W SATA ODD Conn.



SATA ODD Conn.

Copy JIWA2 Symbol

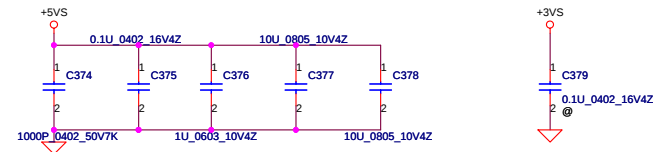
<21> SATA_ITX_C_DRX_P1
<21> SATA_ITX_C_DRX_N1
SATA_ITX_C_DRX_P1
SATA_ITX_C_DRX_N1
SATA_DTX_IRX_N1
SATA_DTX_IRX_P1



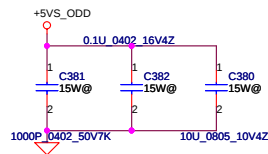
Update FootPrint from
OCTEK_SLS-13SB1G_13P-T to
OCTEK_SLS-13SB1G_13P_RV-T

<21> SATA_DTX_C_IRX_N1
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SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_DTX_IRX_N1
SATA_DTX_IRX_P1

SATA HDD Conn.



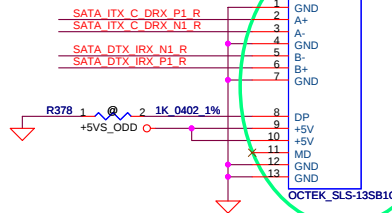
15W SATA ODD Conn.



SATA ODD Conn.

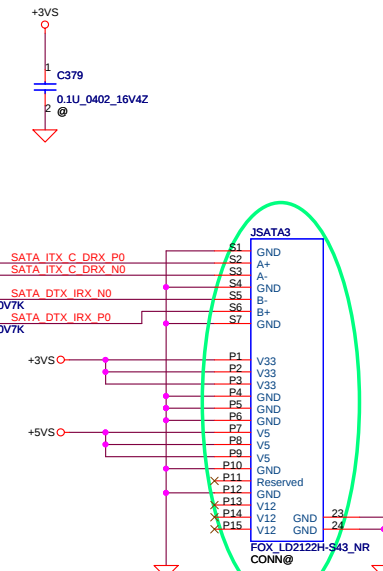
Copy JIWA2 Symbol

SATA_ITX_C_DRX_P1
SATA_ITX_C_DRX_N1
SATA_DTX_IRX_N1
SATA_DTX_IRX_P1
R374
R375
R376
R377
0.0402_5%
0.0402_5%
0.0402_5%
0.0402_5%



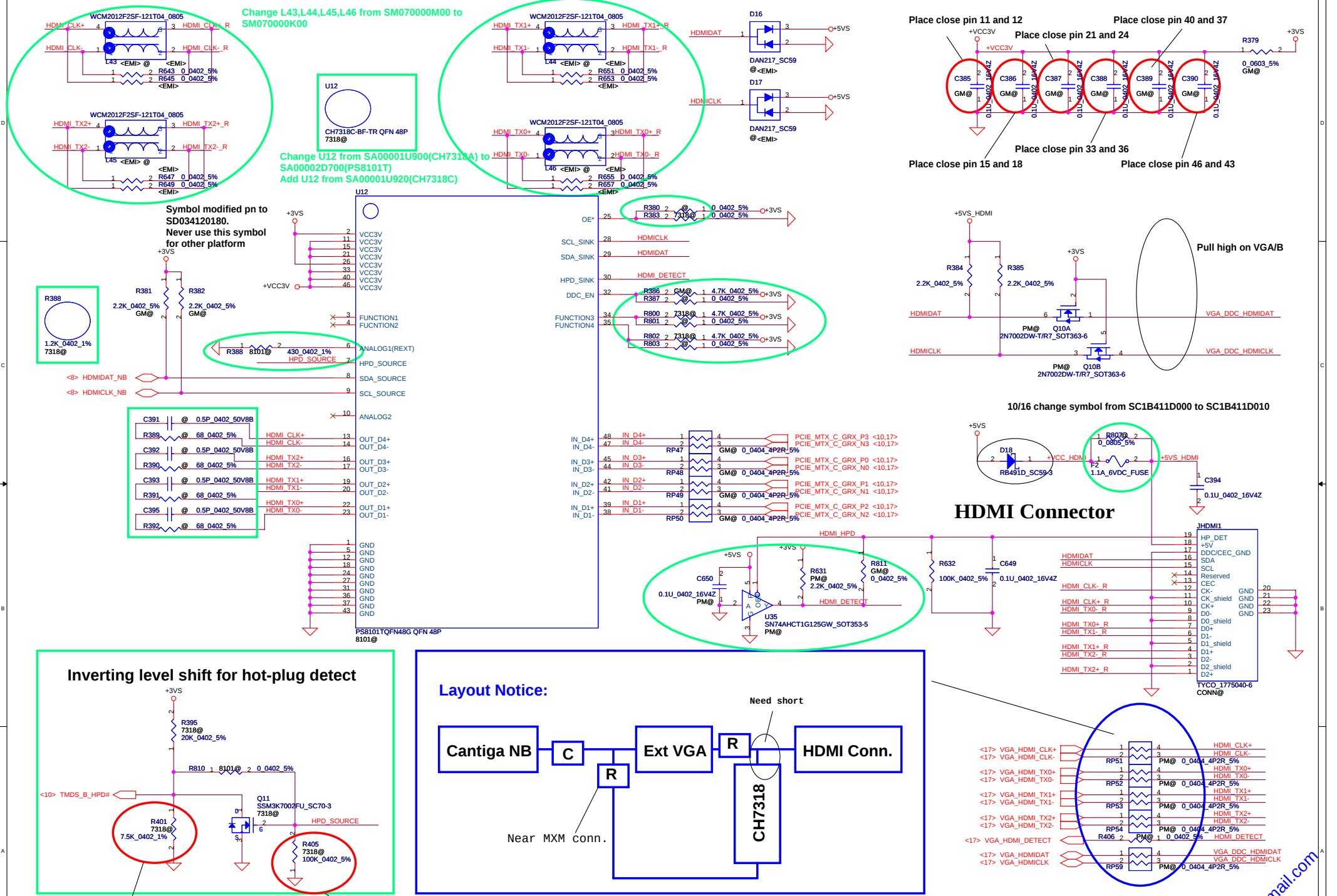
Update FootPrint from
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OCTEK_SLS-13SB1G_13P_RV-T

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SATA_ITX_C_DRX_P0
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SATA_DTX_IRX_N0
SATA_DTX_IRX_P0



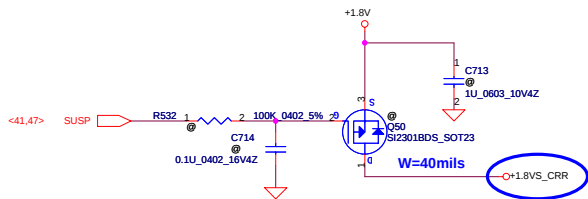
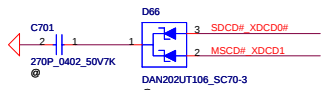
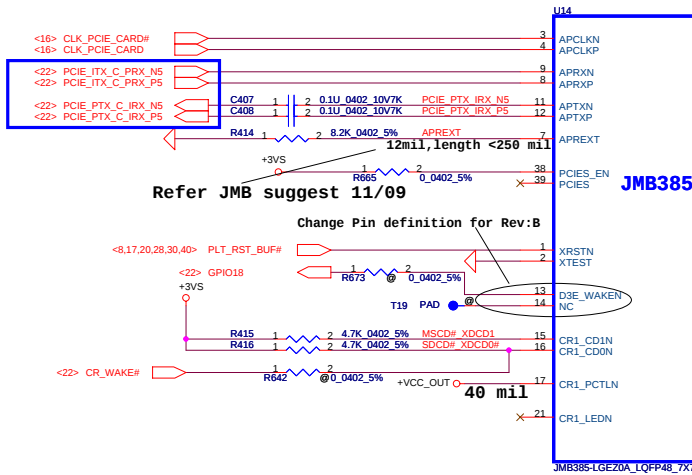
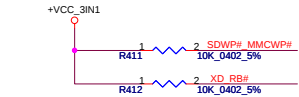
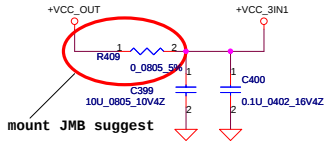
Update Symbol
SP01000G800
FOX_LD2122H-S43_NR
Manually update pin number

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Issued Date	2007/08/18	Deciphered Date	2008/8/18
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Title		Compal Electronics, Inc.	
HDD & ODD Connector		JHXXX M/B LA-4241P Schematic	
Size B	Document Number	Rev	4
Date: Wednesday, May 28, 2008	Sheet 24	of 49	

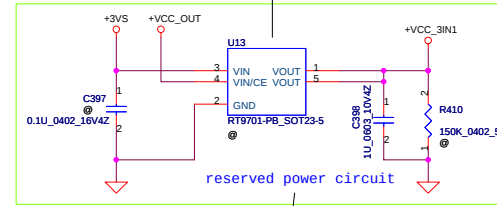


Security Classification		Compal Secret Data	
Issued Date	2007/08/18	Deciphered Date	2008/8/18
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Title		Compal Electronics, Inc.	
Size		CH7318A&HDMI Connector	
Custpm		JHXXX M/B LA-4241P Schematic	
Date:		Tuesday, June 03, 2008	
Sheet		25 of 49	

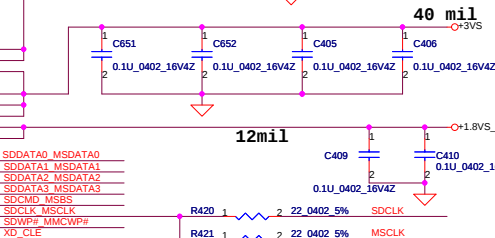
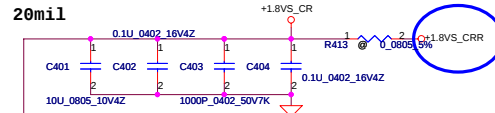
Use 0805 type and over 20 mils trace width on both side



Active High EN
11/24 Andy

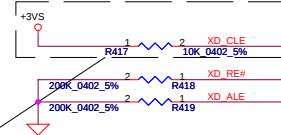


Refer JMB suggest 11/14



Damping need to close to IC

Strap pin for JMicro

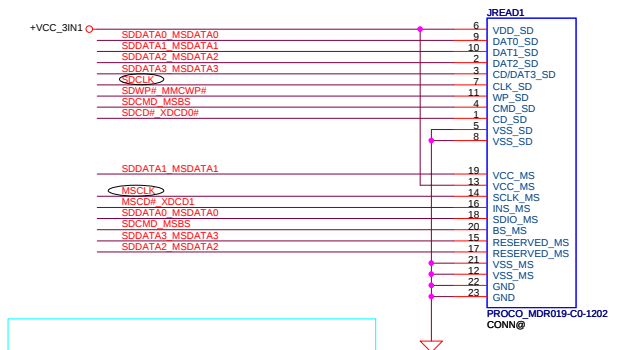


Refer JMB suggest 11/09

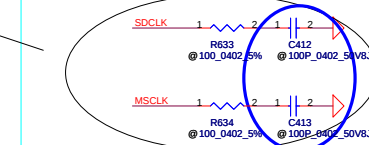
Rev :B

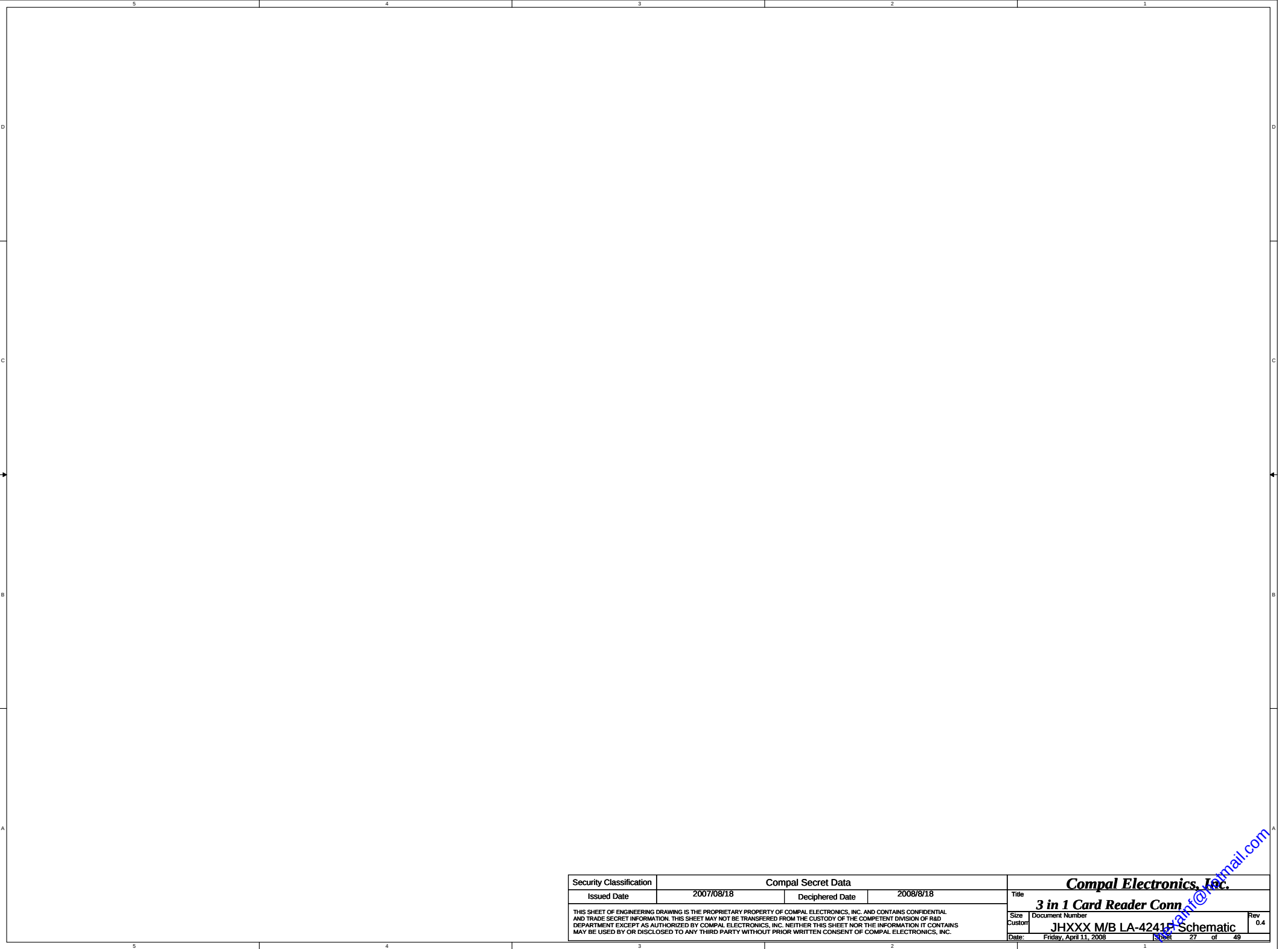
SD,MMC,MS muti-function pin define		
MDIO PIN Name	SD/MMC Card PIN Name	MS Card PIN Name
MDIO00	SD1_DAT0	MS1_DAT0
MDIO01	SD1_DAT1	MS1_DAT1
MDIO02	SD1_DAT2	MS1_DAT2
MDIO03	SD1_DAT3	MS1_DAT3
MDIO04	SD1_CMD	MS1_BS
MDIO05	SD1_CLK	MS1_CLK
MDIO06	SD1_WP	
MDIO07		
MDIO08	MMC_DAT4	MS1_DAT4
MDIO09	MMC_DAT5	MS1_DAT5
MDIO10	MMC_DAT6	MS1_DAT6
MDIO11	MMC_DAT7	MS1_DAT7
MDIO12		
MDIO13		
MDIO14		
CR1_LEDN	SD1_LED#	MS1_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#
CR1_CD0	SD1_CD#	
CR1_CD1		MS1_CD#

3 in 1 Card Reader

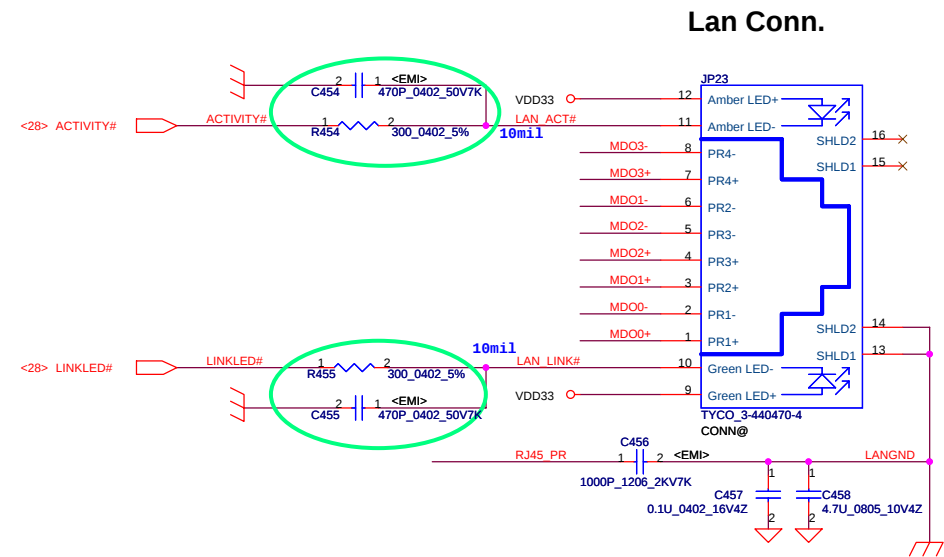
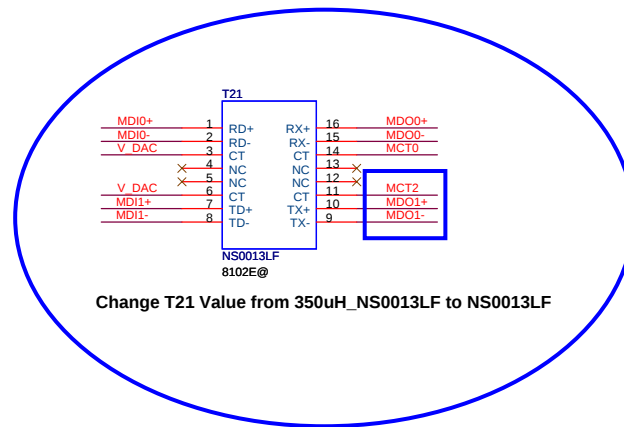
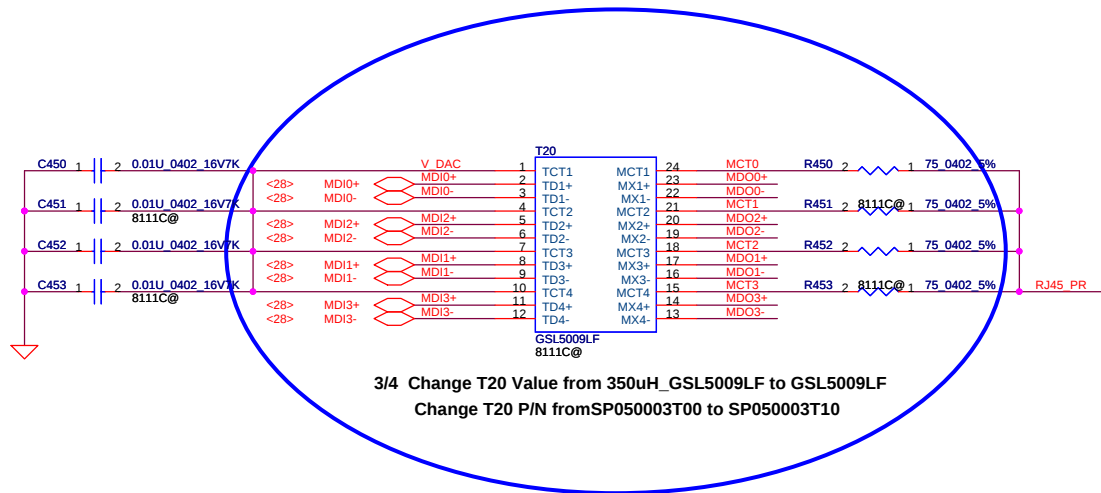


10/17 add for
JMB380

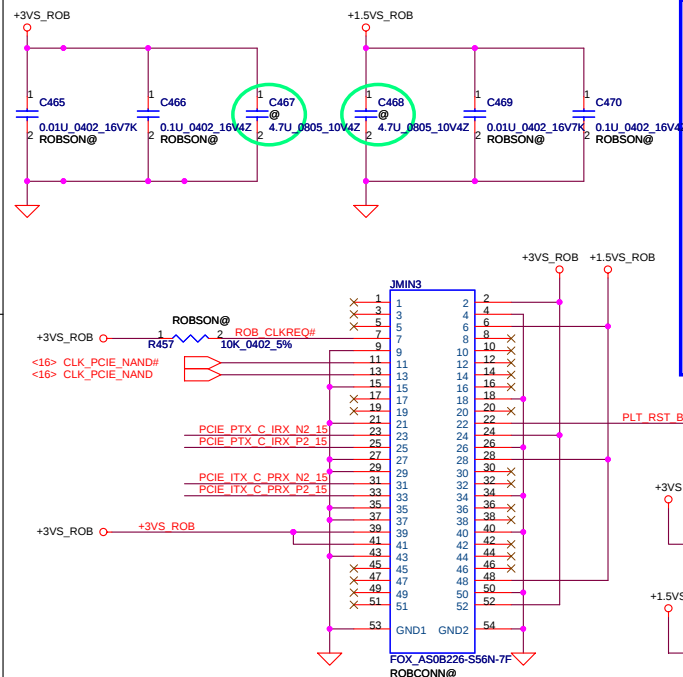




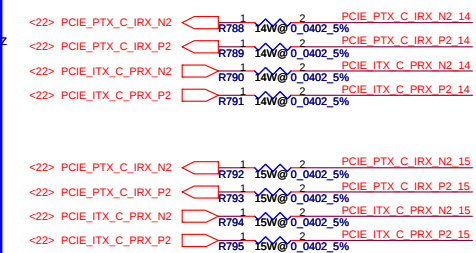
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	
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				Size	Document Number
				Custom	JHXXX M/B LA-4241H Schematic
				Date:	Friday, April 11, 2008
				Sheet	27 of 49



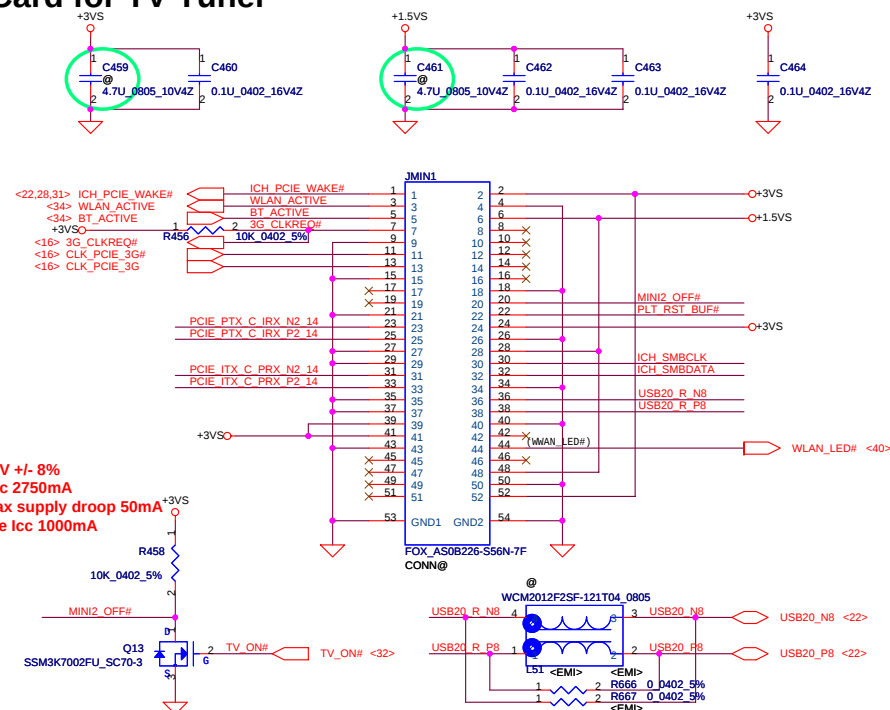
NAND mini Card(Robson support)



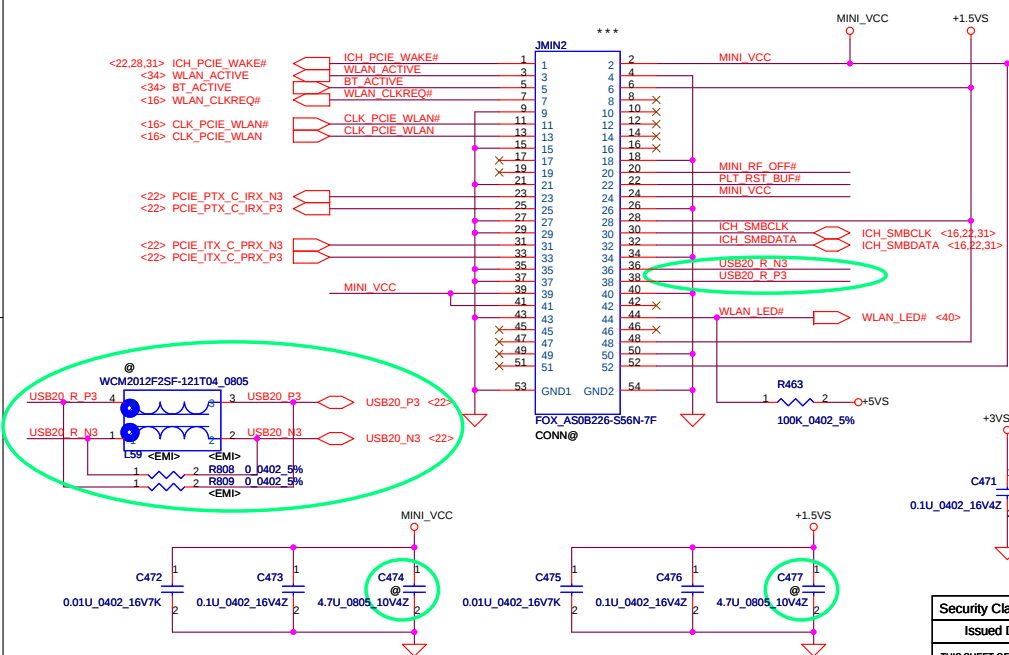
Use Y topology to place these resistors between JMIN2 and JMIN1



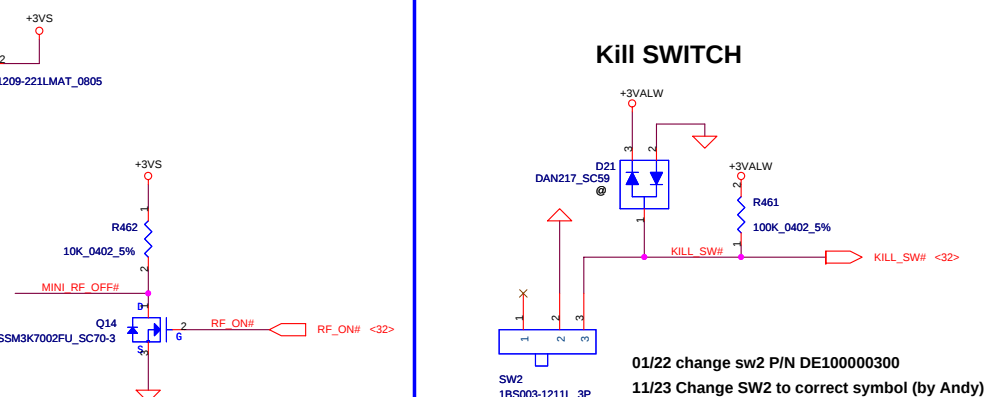
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply dro
Average Icc 1000mA



Mini-Express Card for WLAN



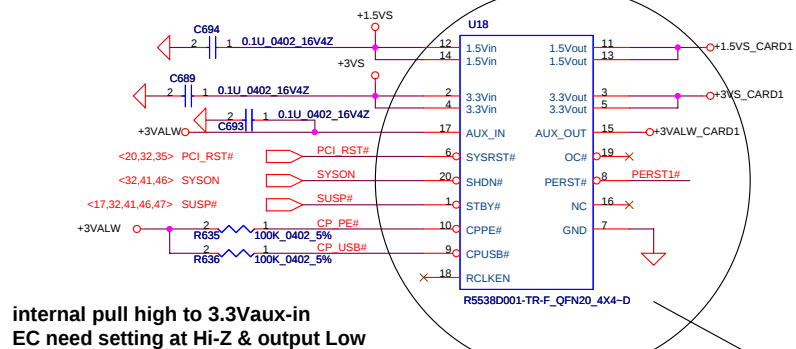
Please place these caps between JMIN1 and JMIN2



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Issued Date		2007/06/18	Deciphered Date		2008/6/18	Title					
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						Size	Document Number				Rev
						JHXXX M/B LA-4241P Schematic					0.4
Date:		Wednesday, May 28, 2008		Sheet	30	of 49					

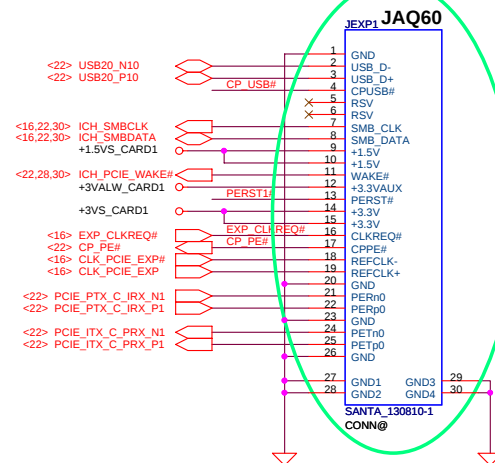
New Card Power Switch

New Card



Change to GMT PartNumber

New Card Socket (Left/TOP)



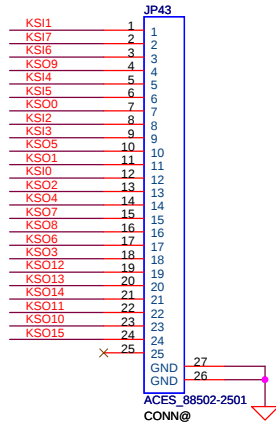
Update FootPrint from
SANTA_13181060-5_26P-T to
SANTA_130810-1_26P

Update FootPrint from
SANTA_130810-1_26P to
SANTA_130810-1_26P-S

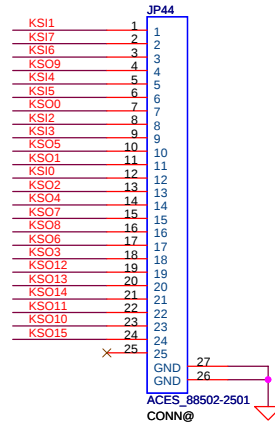
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	NEW CARD
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				Date: Wednesday, May 28, 2008	Rev 0.4
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INT_KBD Conn.

For JHL90

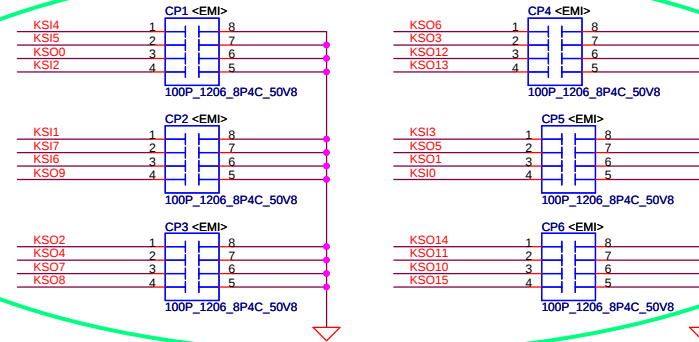


For JHT00

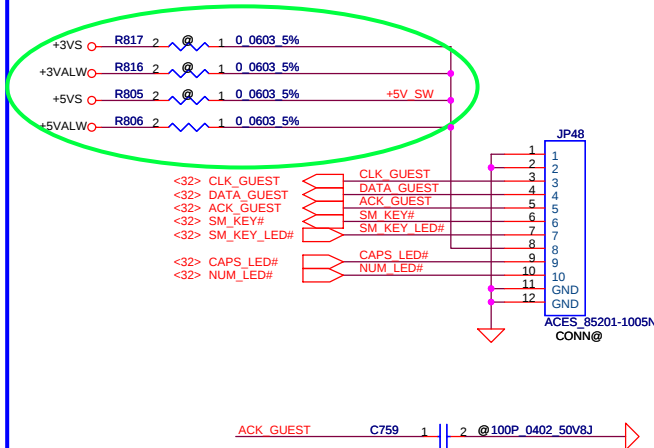


KSI[0..7] <32>
KSO[0..15] <32>

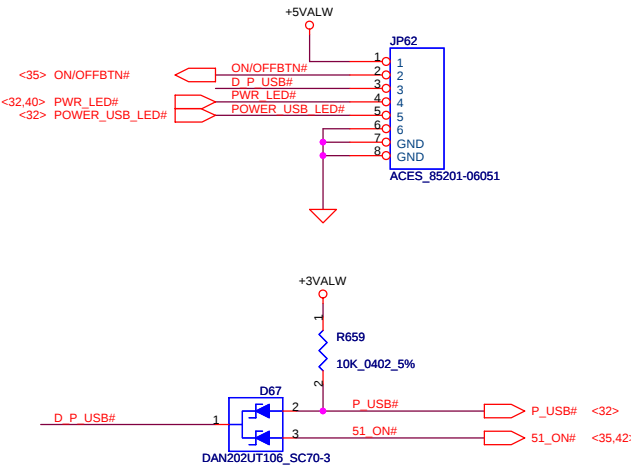
Delete C525-C548 SE071101J80 (100pF)
Add SI102101K80 (CP : 100pF)
(EMI Recommend)



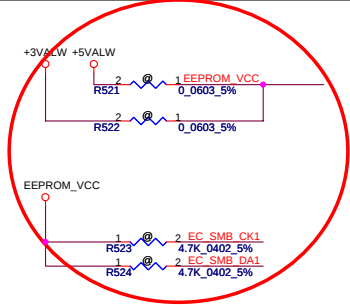
Function Board Conn.



Power USB Board Conn.



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Size	Document Number	JHXXX M/B LA-4241P Schematic		Rev	
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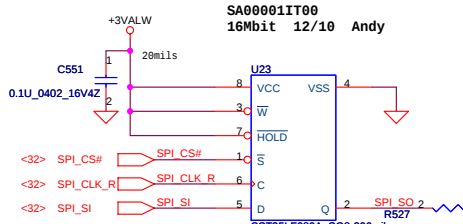


12/28 Add

0206 => change PN to SA00001N800
 12/19 change pn to SA00001MP00 (original part EOL)
 12/25 change back to SA024160140 (Samples can not on time)

16M SPI ROM

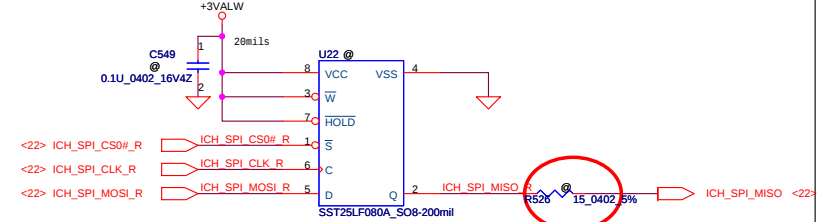
For EC+BIOS+VBIOS



12/15 change from 15 to 0 ohm'

8M SPI ROM

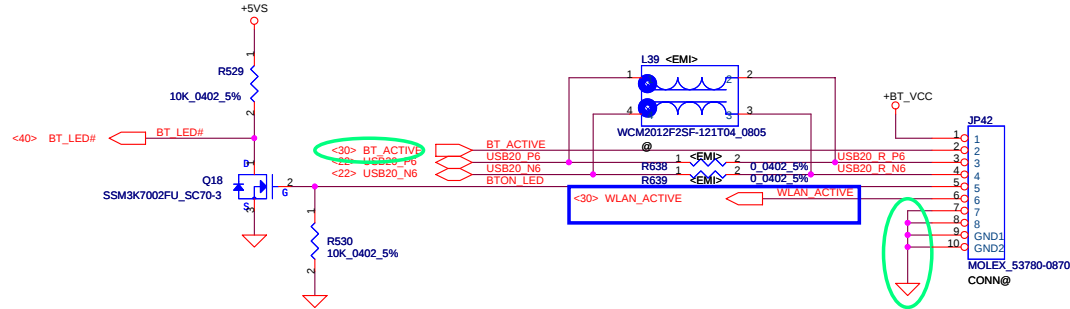
For iTPM+HDCP



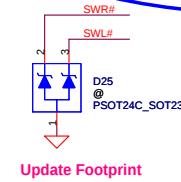
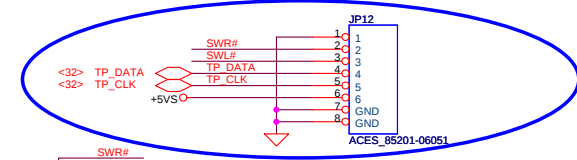
follow CRB Check
 SD028150A80

Bluetooth Conn.

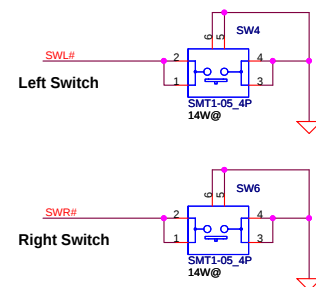
Need to check BT pin definition again!
 9/20 modified this block



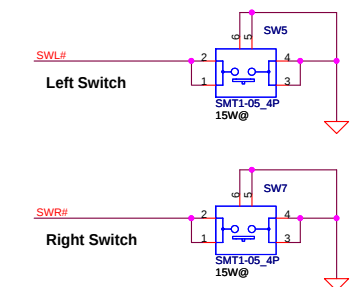
To TP/B Conn.



14W Use

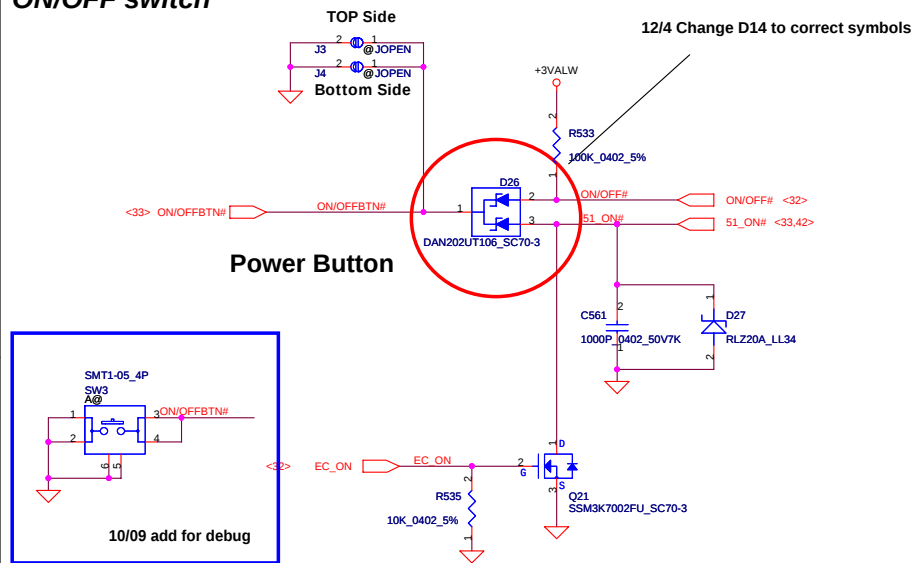


15W Use

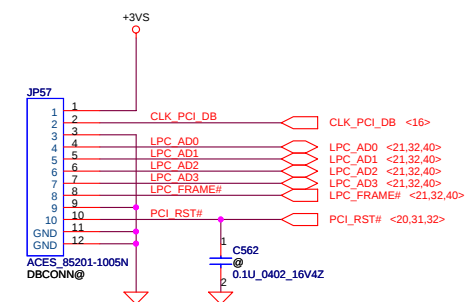


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								Size B		Document Number				JHXXXX M/B LA-4241P Schematic				Rev 0.4	
								Date:		Wednesday, May 28, 2008				Sheet		34		of 49	

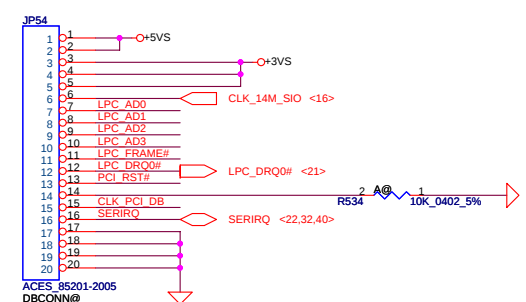
ON/OFF switch



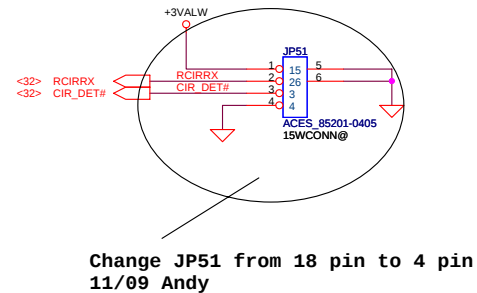
FOR LPC DEBUG PORT



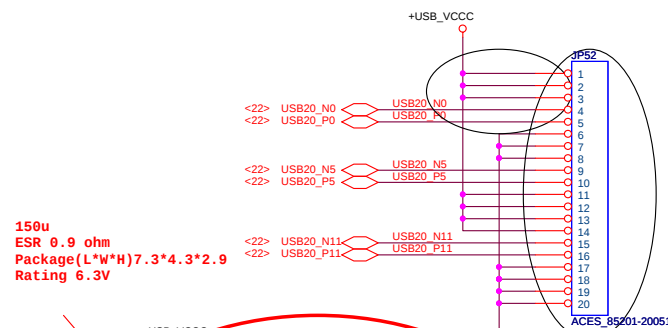
FOR LPC SIO DEBUG PORT



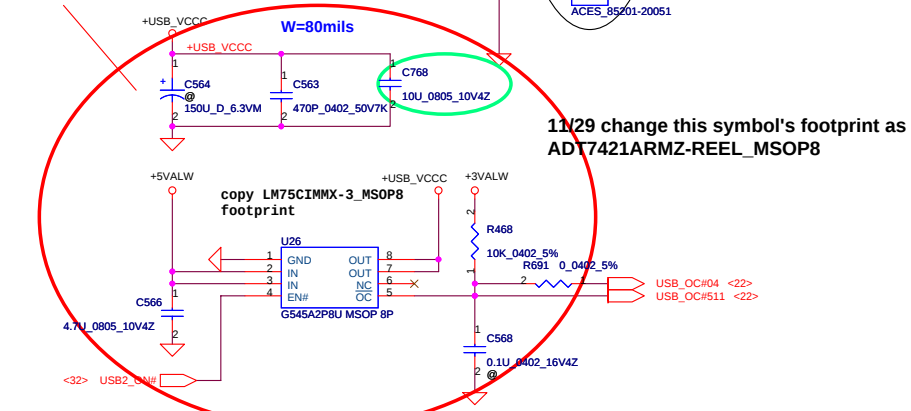
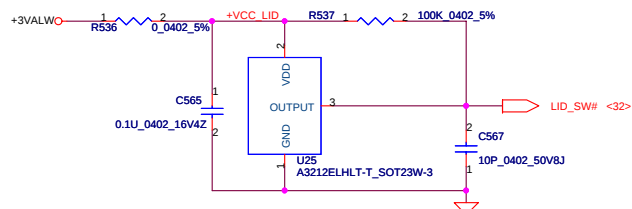
CIR



USB IO Conn.

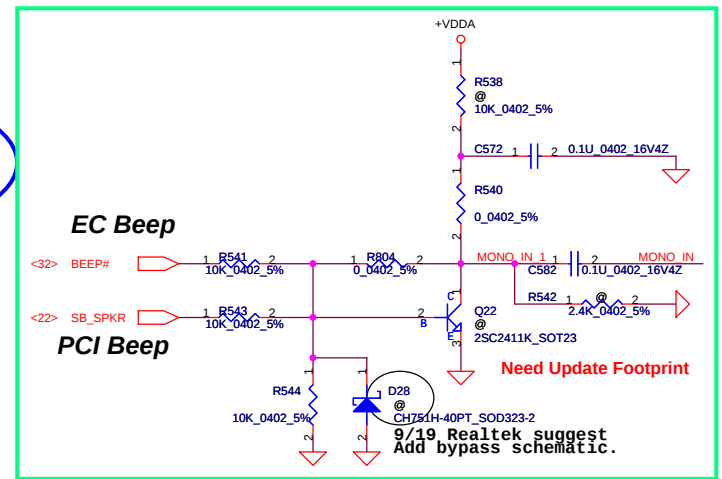
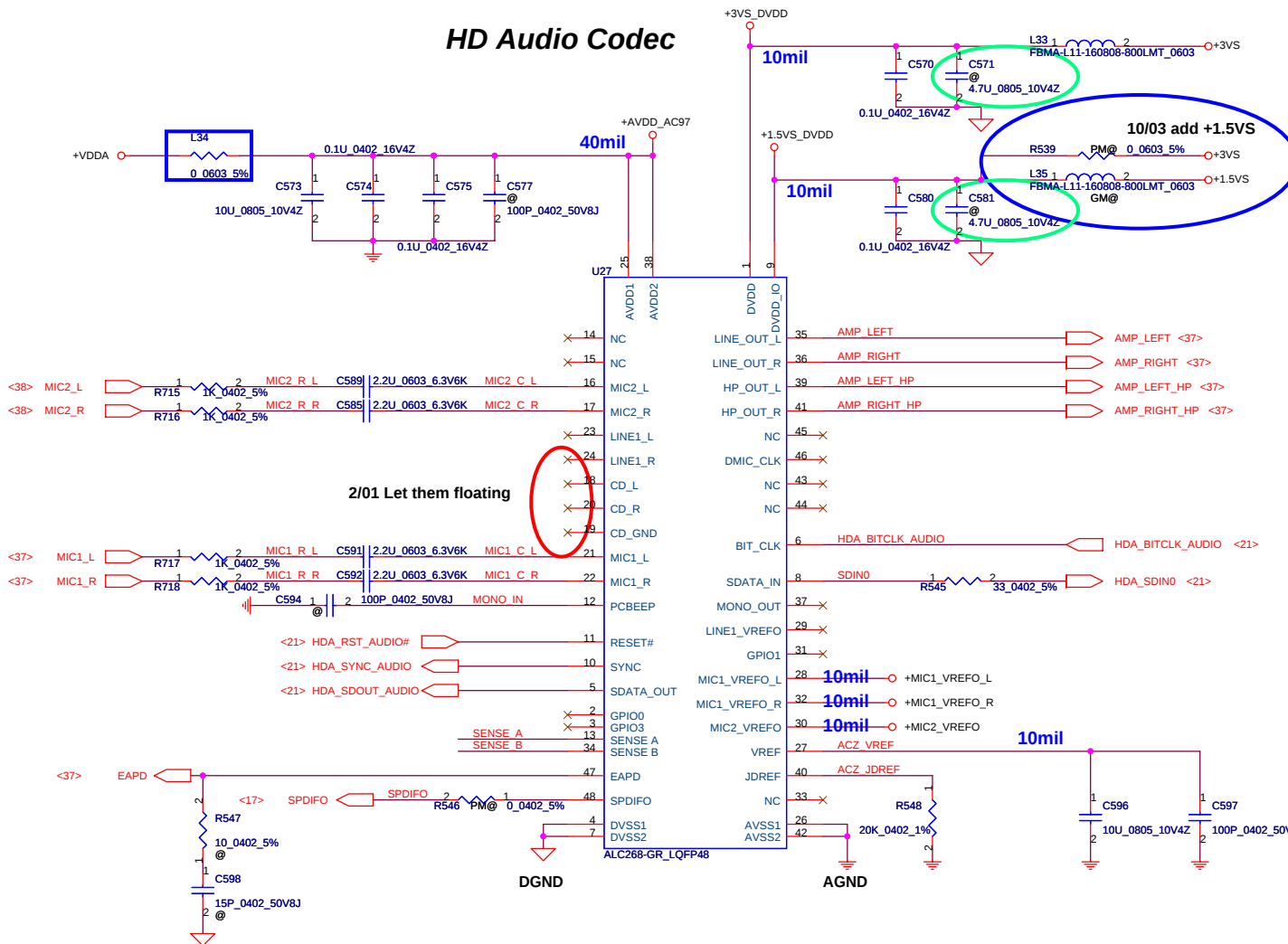


Lid Switch



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HD Audio Codec

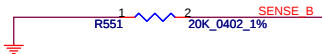


Sense Pin	Impedance	Codec Signals	Funnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE OUT
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE OUT

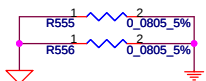
SENSE FOR Ext. Mic.



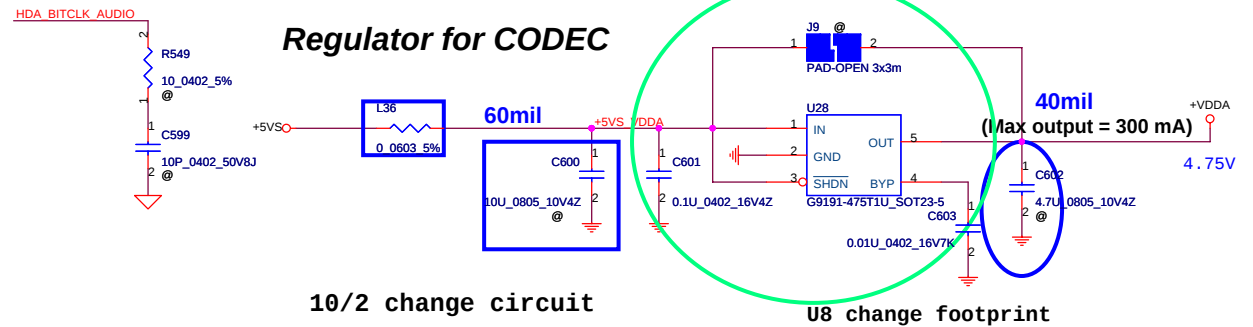
SENSE FOR Solo Int. Mic.



SENSE FOR HP



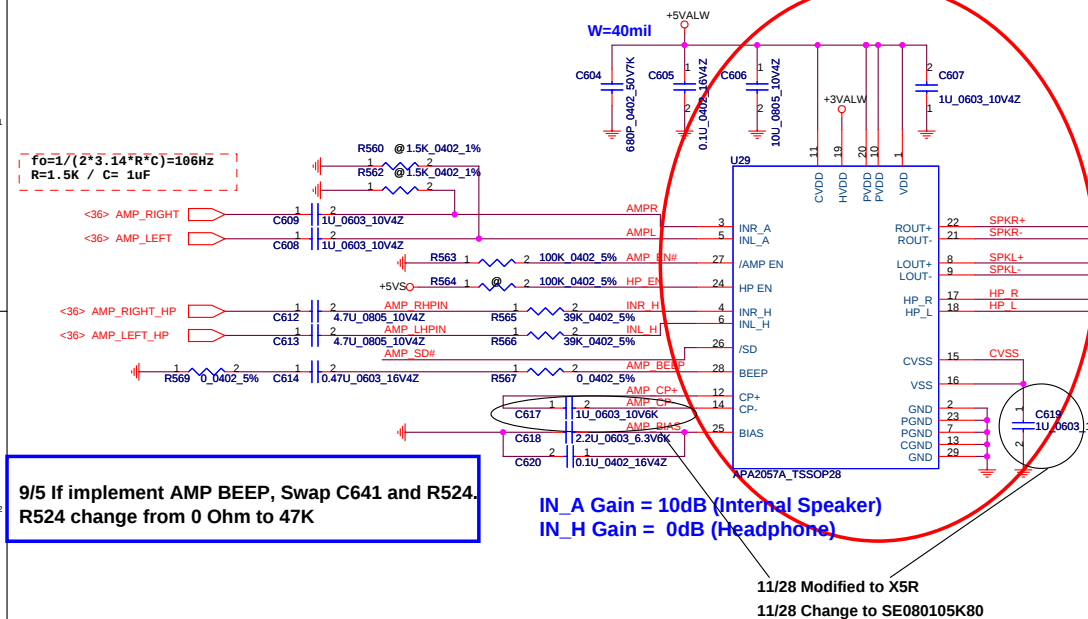
Regulator for CODEC



Security Classification		Compal Secret Data		Compal Electronics, Inc. Title <Title> HD Audio Codec ALC268		
Issued Date	2007/08/18	Deciphered Date	2008/8/18	Size Custom	Document Number JHXXX M/B LA-4241P Schematic	Rev 0.4
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APA2057 SPK/HP Amplifier

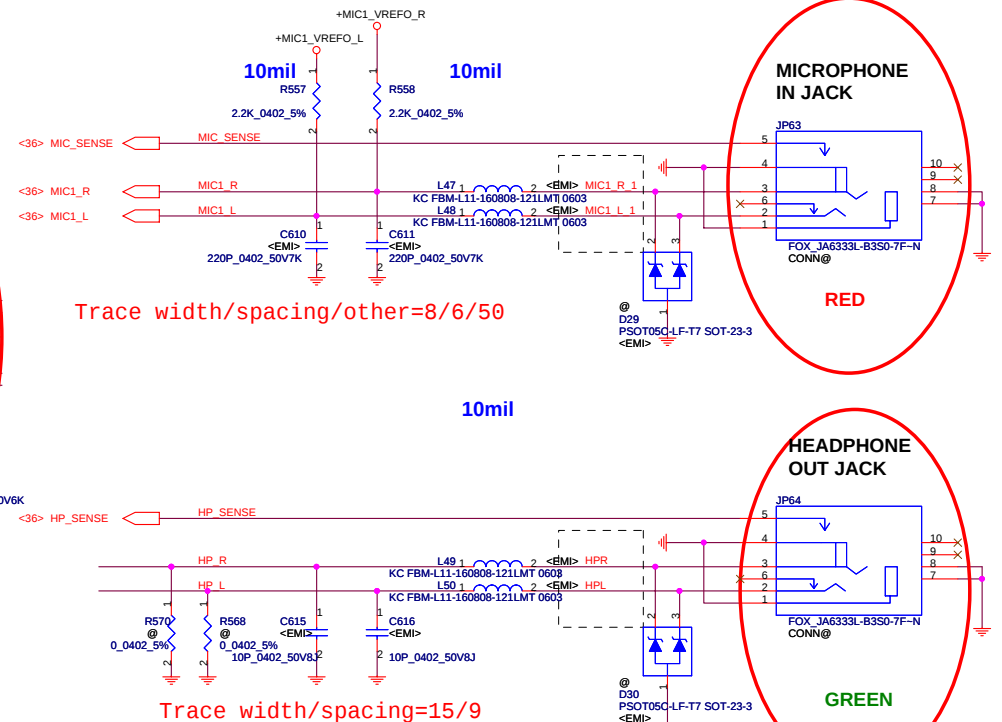
10/2 U6 APA2057A P/N:SA00001QD00



9/5 If implement AMP BEEP, Swap C641 and R524.
R524 change from 0 Ohm to 47K

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

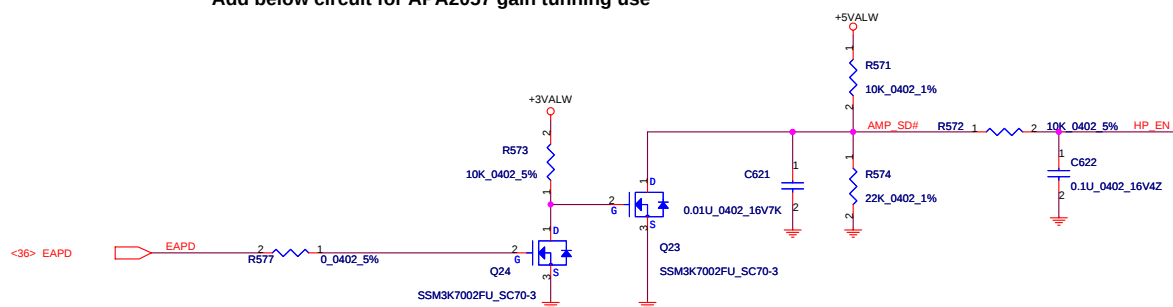
11/28 Modified to X5R
11/28 Change to SE080105K80



Trace width/spacing/other=8/6/50

Trace width/spacing=15/9

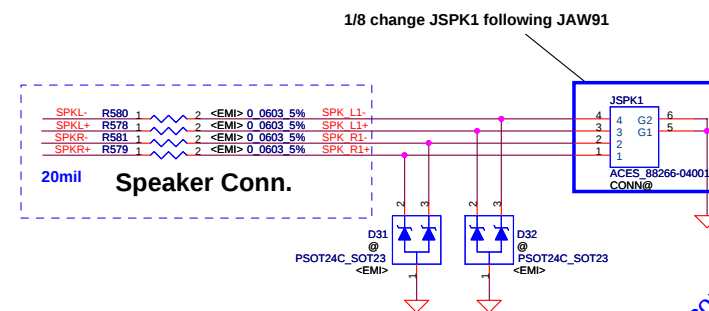
Add below circuit for APA2057 gain tuning use



Gain= 10dB

Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

+5VALW assume equal 5.1V
10 dB ---> $5.1 \times 220 / 320 = 3.5$

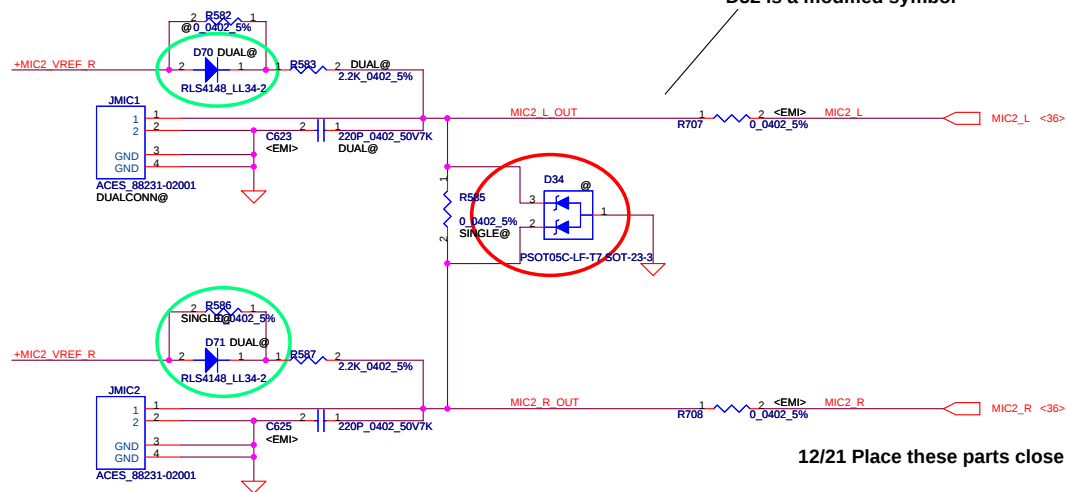


1/8 change JSPK1 following JAW91

Speaker Conn.

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				AMP/VR/Audio Jack			
				Size Custom		Document Number	
				JHXXX M/B LA-4241P Schematic			
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D52 is a modified symbol



12/21 Place these parts close to CODEC (U7)

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				JHXXX M/B LA-4241P Schematic		
				Date: Wednesday, May 28, 2008	Sheet 38	of 49

11/27 Add screw for layout request

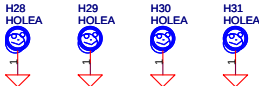
H_3P0



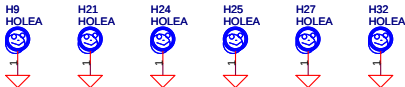
H_3P7



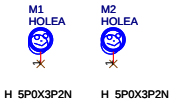
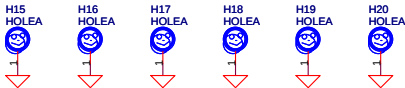
H_4P2



2/22 change these from H_3P7 to H_3P8



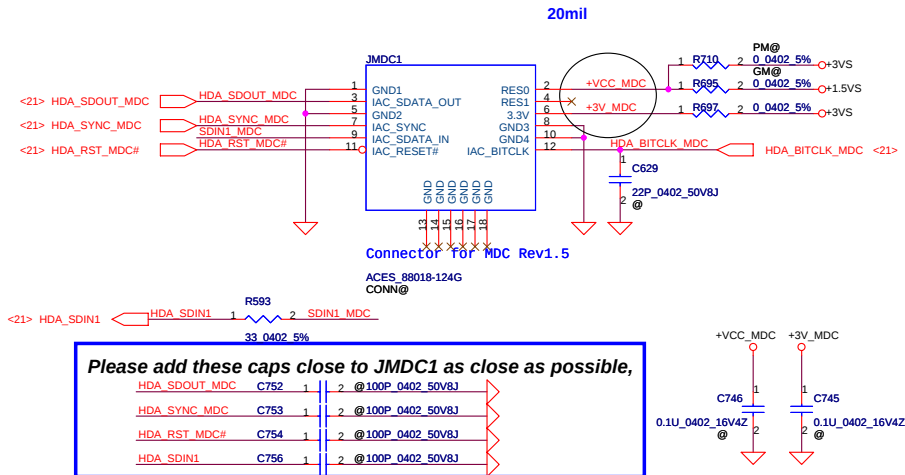
2/22 change these from H_3P2 to H_3P3



11/27 Add screw for layout request

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				JHXXX M/B LA-4241P Schematic	
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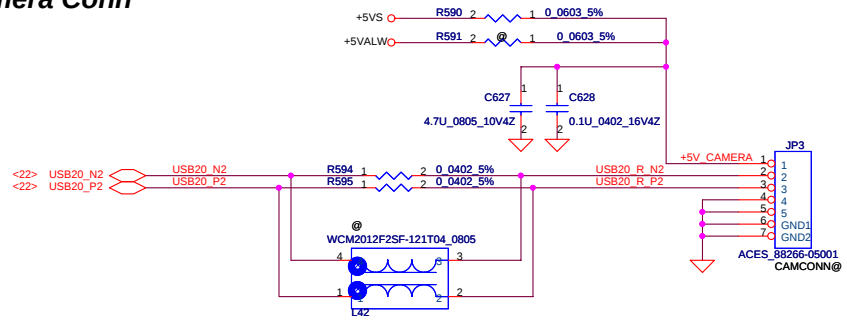
MDC Conn.



TPM X76 Information

X76 P/N	Vendor	Location	Bom Structure
X7611630L07	Infineon	C717,C718,R698,R702,R703,U32,X3	IN_TPM@
X7611630L08	Winbond	C724,U32	WB_TPM@

Camera Conn

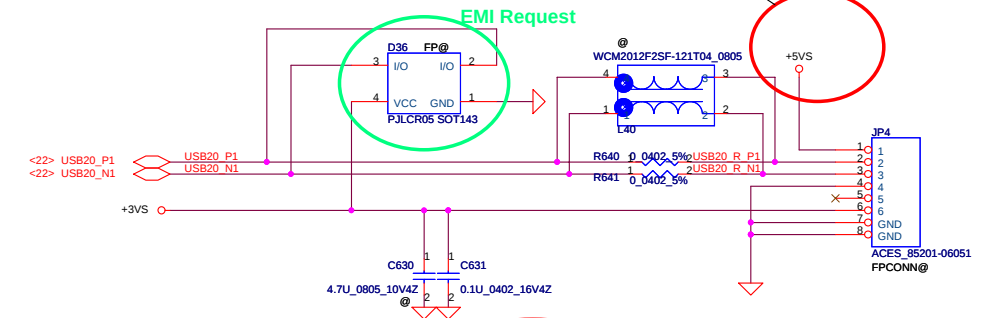


Finger Print board

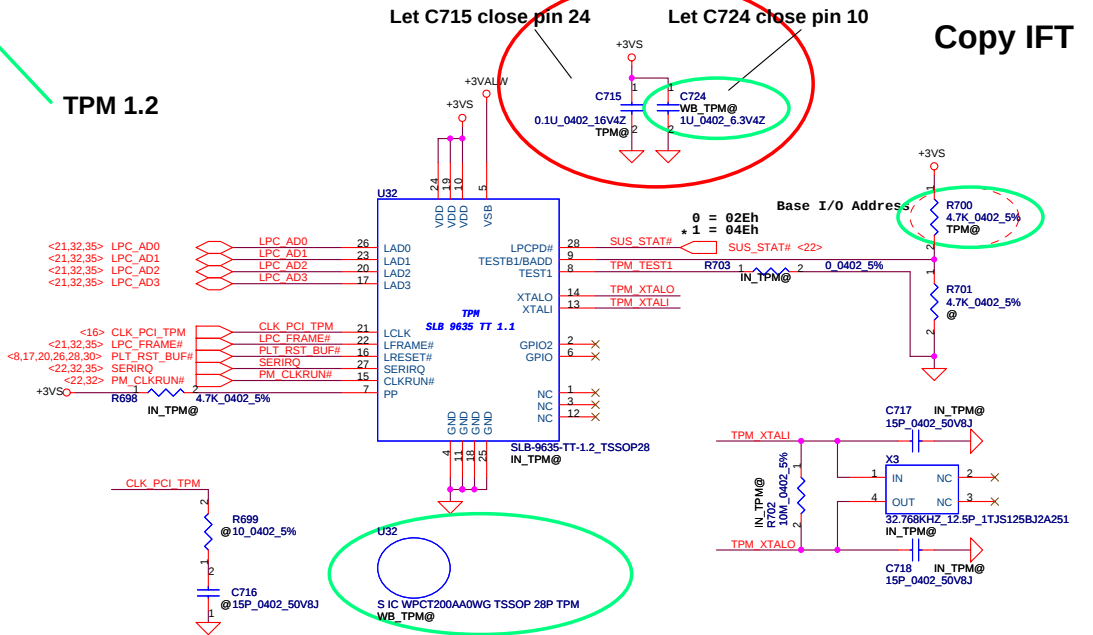
05/26 Change D36 from SC300000X00 to SC300000K00

1/05 Modified D3 to SCA00000A00 For EMI 2/1 change JP4 pin 6 to +5VS for LTT FP use

0208 Remove D3, Add D55 (SC300000G00)

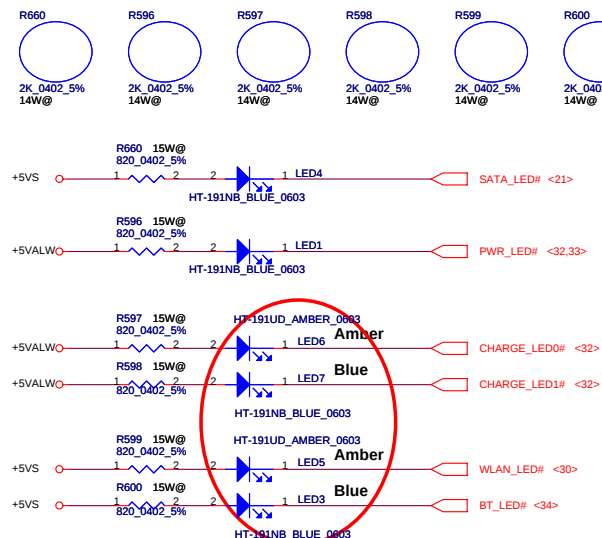


TPM 1.2



LED

05/28 Change R660,R596,R597,R598,R599,R600 to 820ohm for 15W@
05/28 Add R660,R596,R597,R598,R599,R600 to 2kohm for 14W@

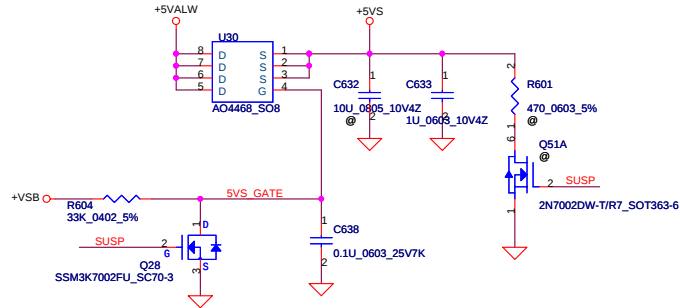


12/7 Modified LED footprint to LED_HT-297UD-CB_4P

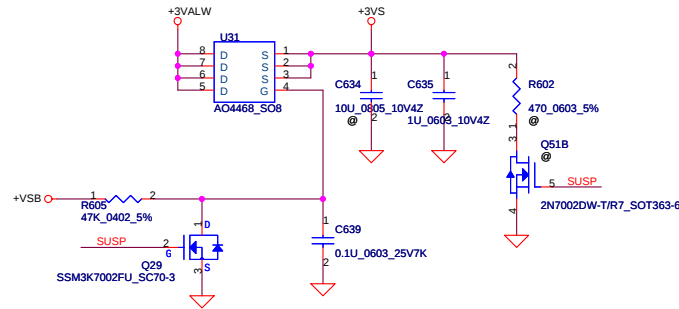
12/15 Modified to correct LED symbol!

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								2008/8/18			
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Title				MDC/LED/Camera/FP				Rev			
Size				JHXXX M/B LA-4241P Schematic				0.4			
Date:				Tuesday, June 03, 2008				Sheet 40 of 49			

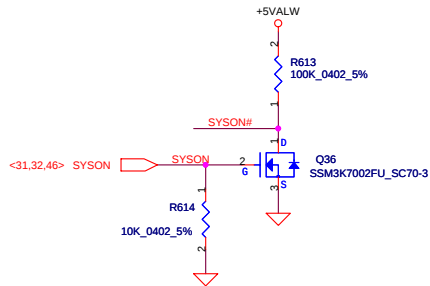
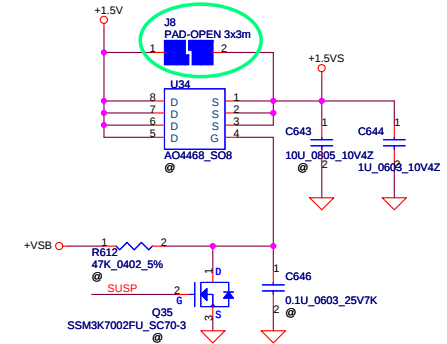
+5VALW TO +5VS



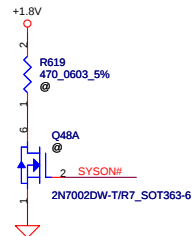
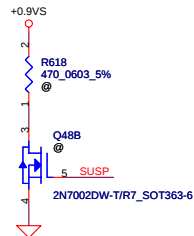
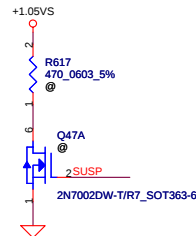
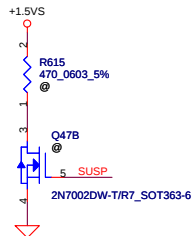
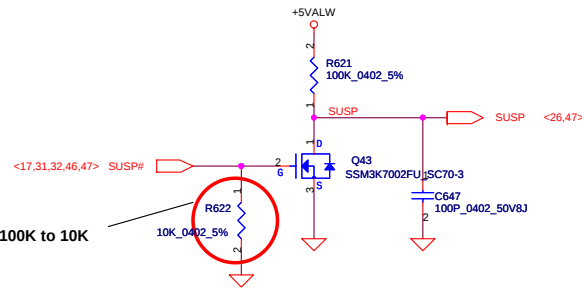
+3VALW TO +3VS



+1.5V TO +1.5VS

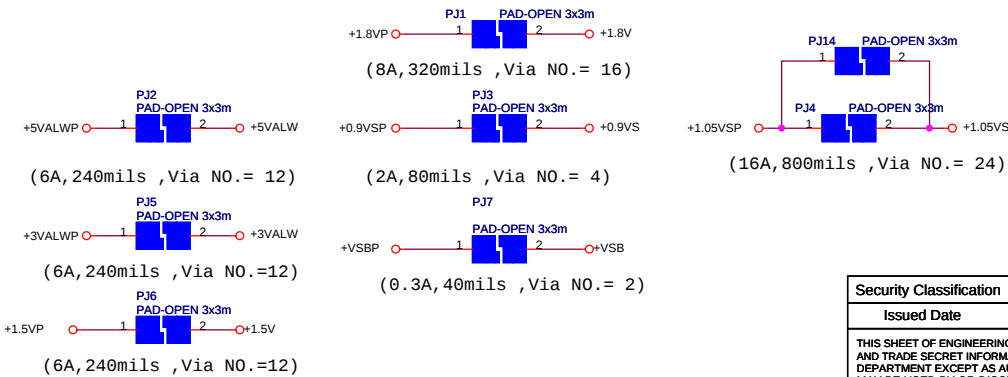
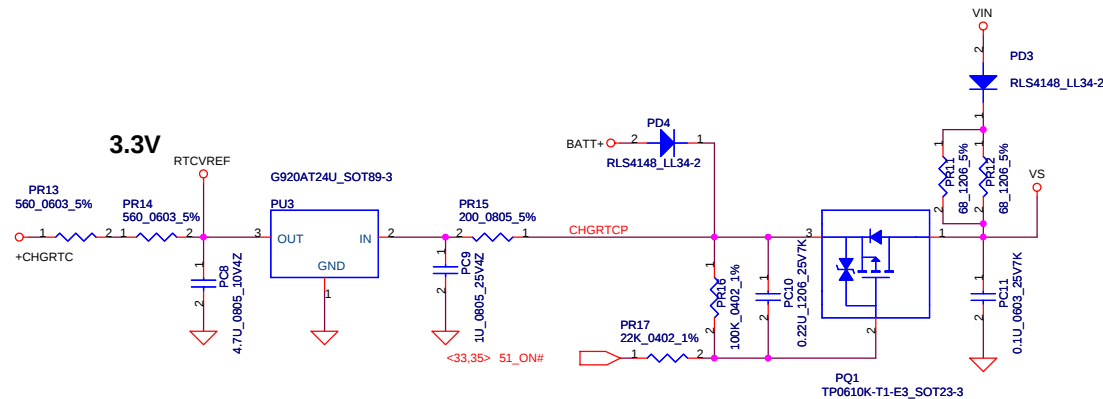
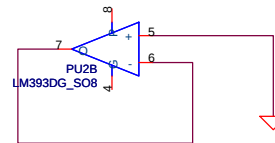
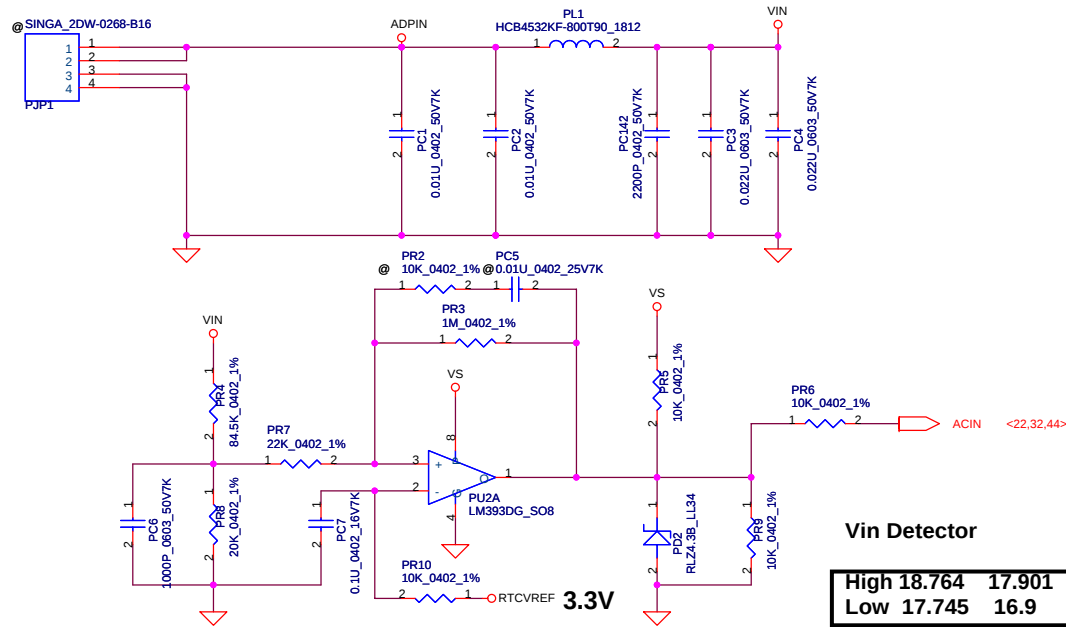


3/14 Change R16 from 100K to 10K



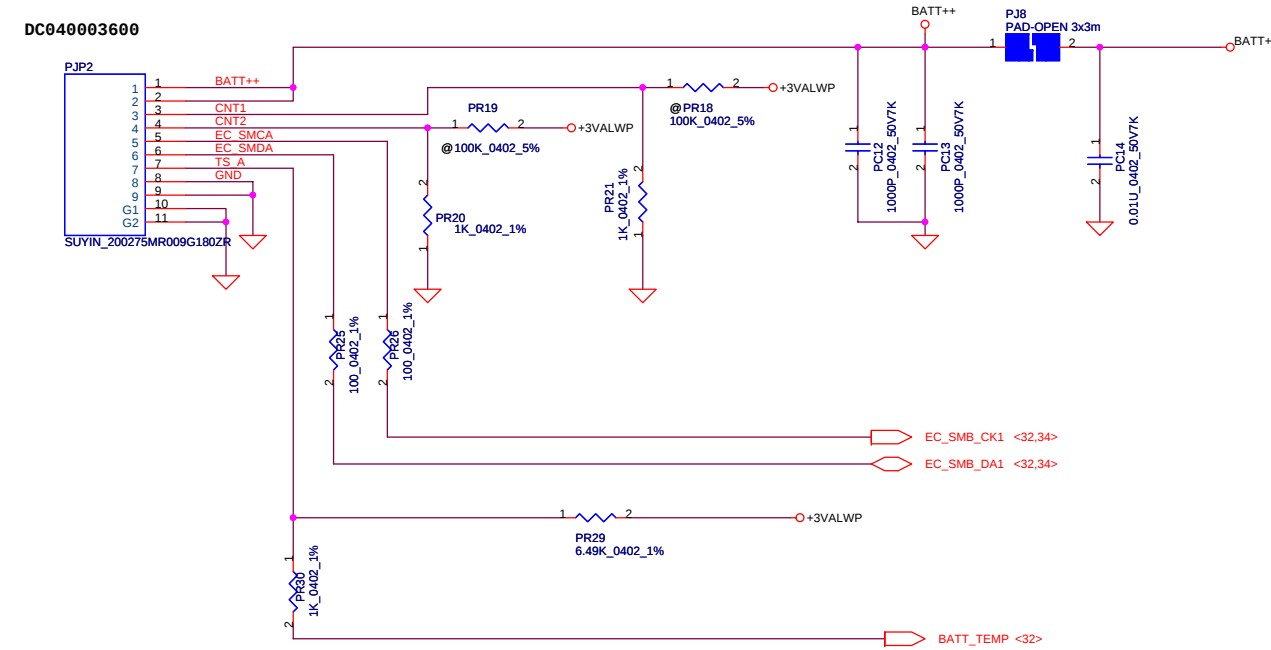
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DC301001Y00

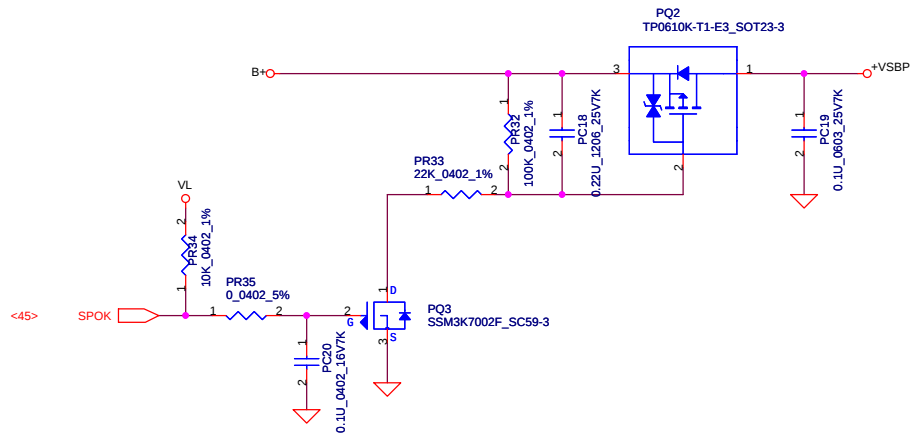
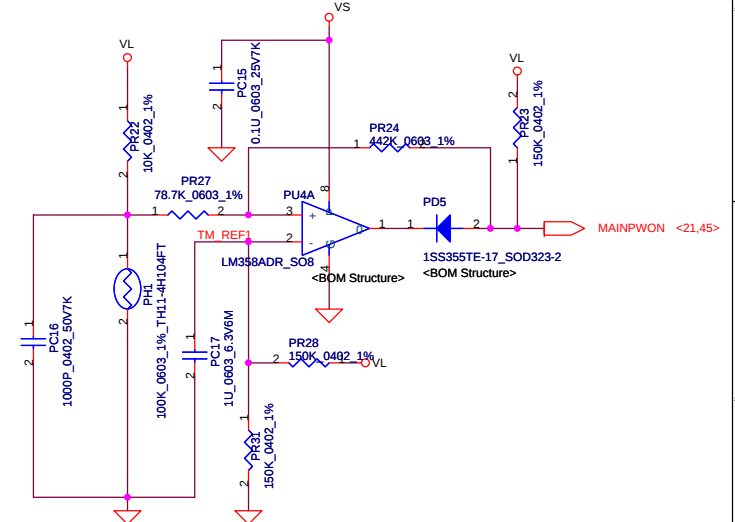


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DC040003600

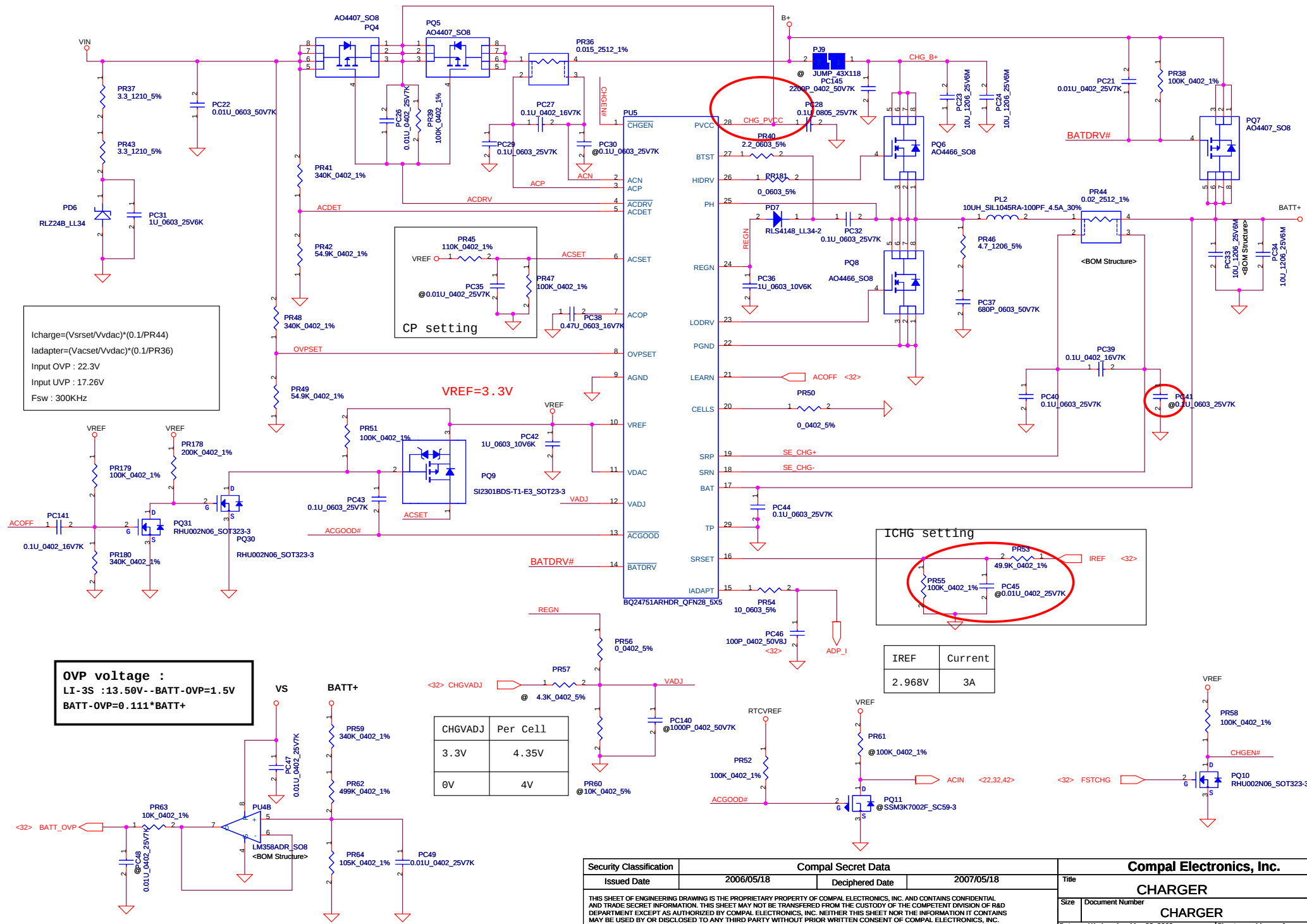


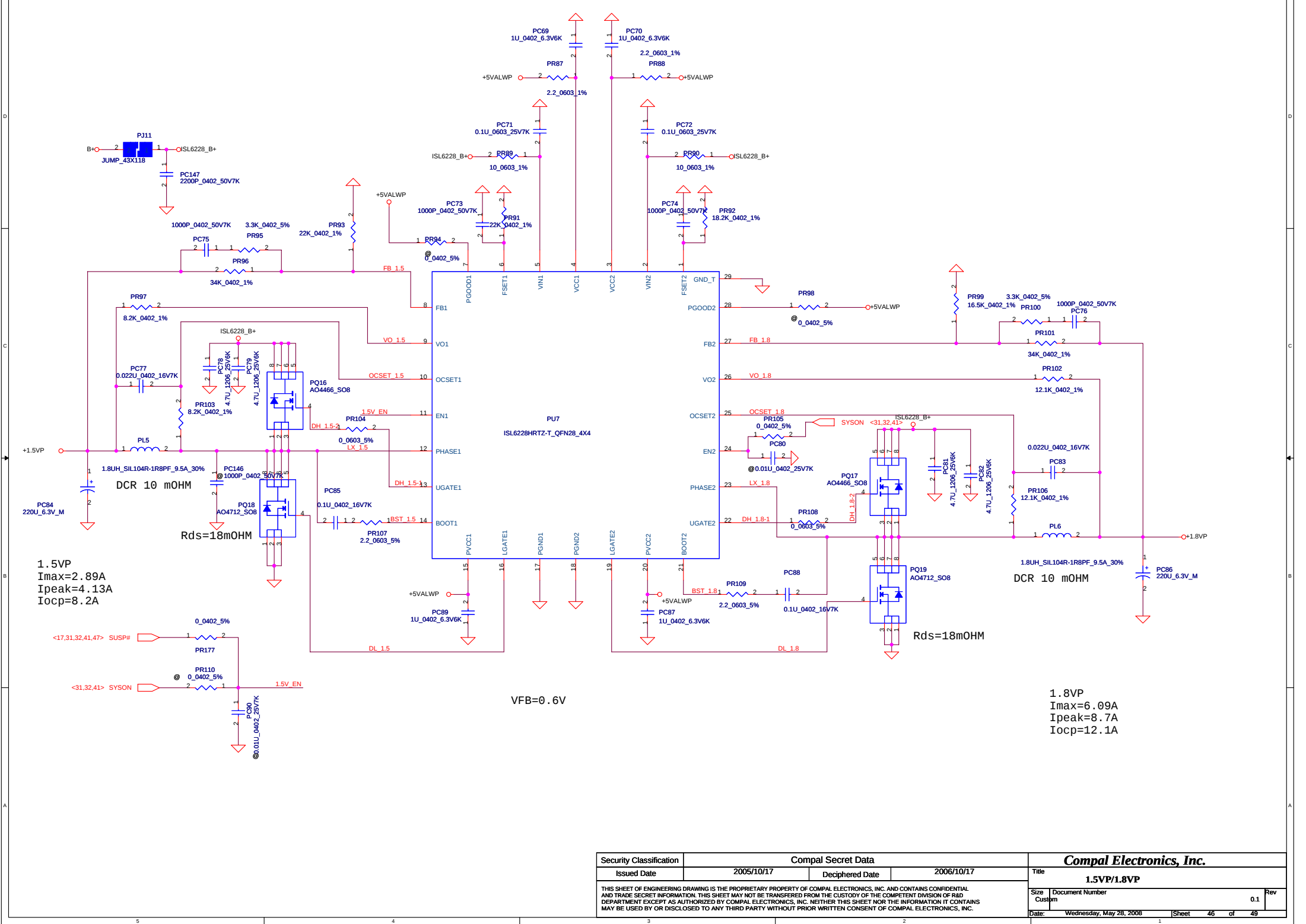
PH1 under CPU bottom side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C



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				BATTERY CONN. IOTP	
				Size B	Document Number
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65W, Iadapter=0~3.42A, Current sense=0.015ohm, PR45=110K, CP=3.175A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR45=54.9K, CP=4.303A



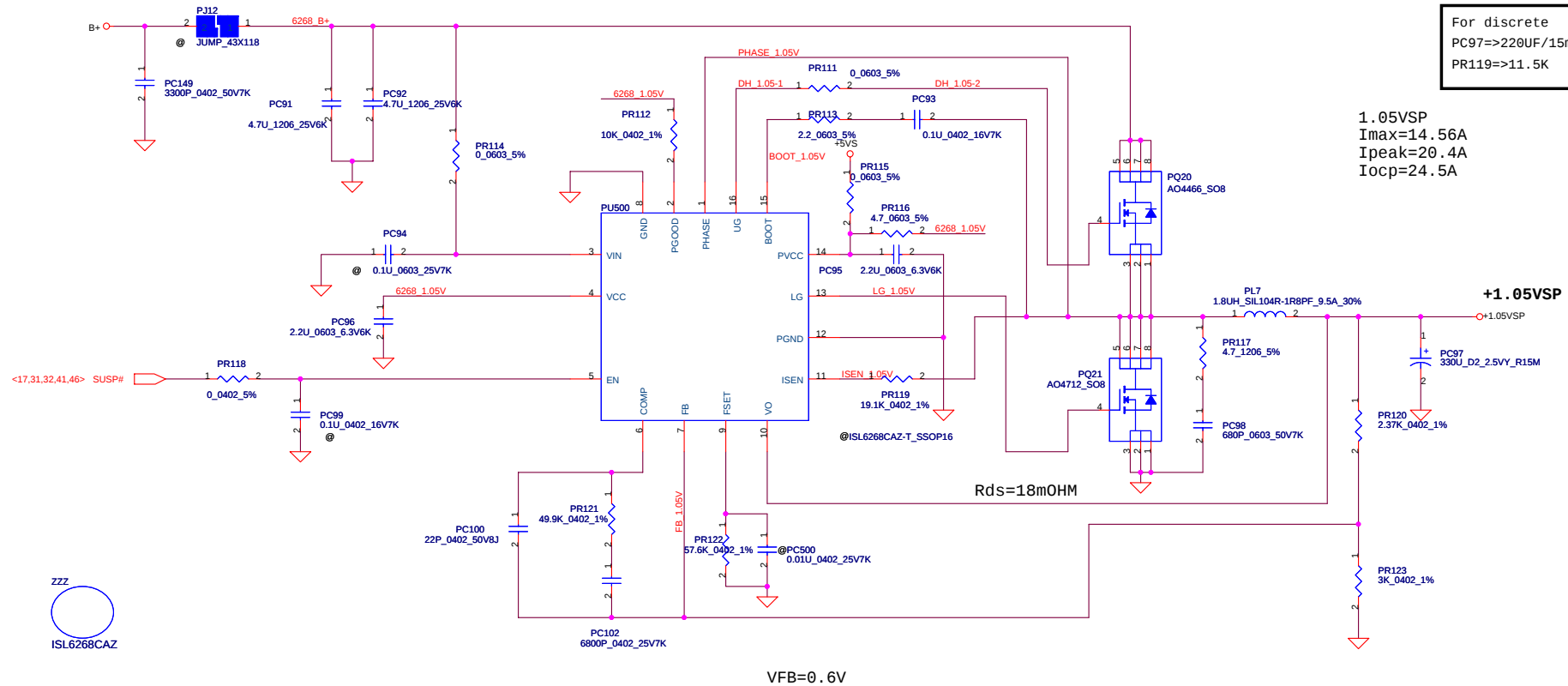


1.5VP
Imax=2.89A
Ipeak=4.13A
Iocp=8.2A

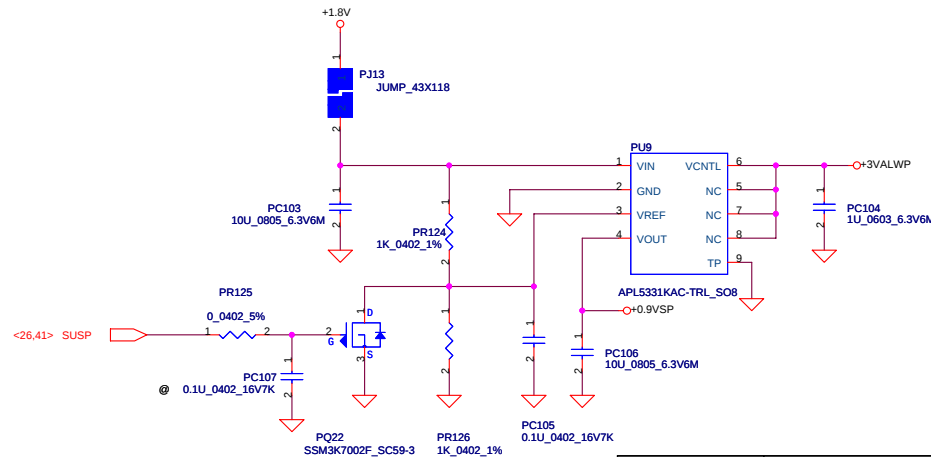
1.8VP
Imax=6.09A
Ipeak=8.7A
Iocp=12.1A

VFB=0.6V

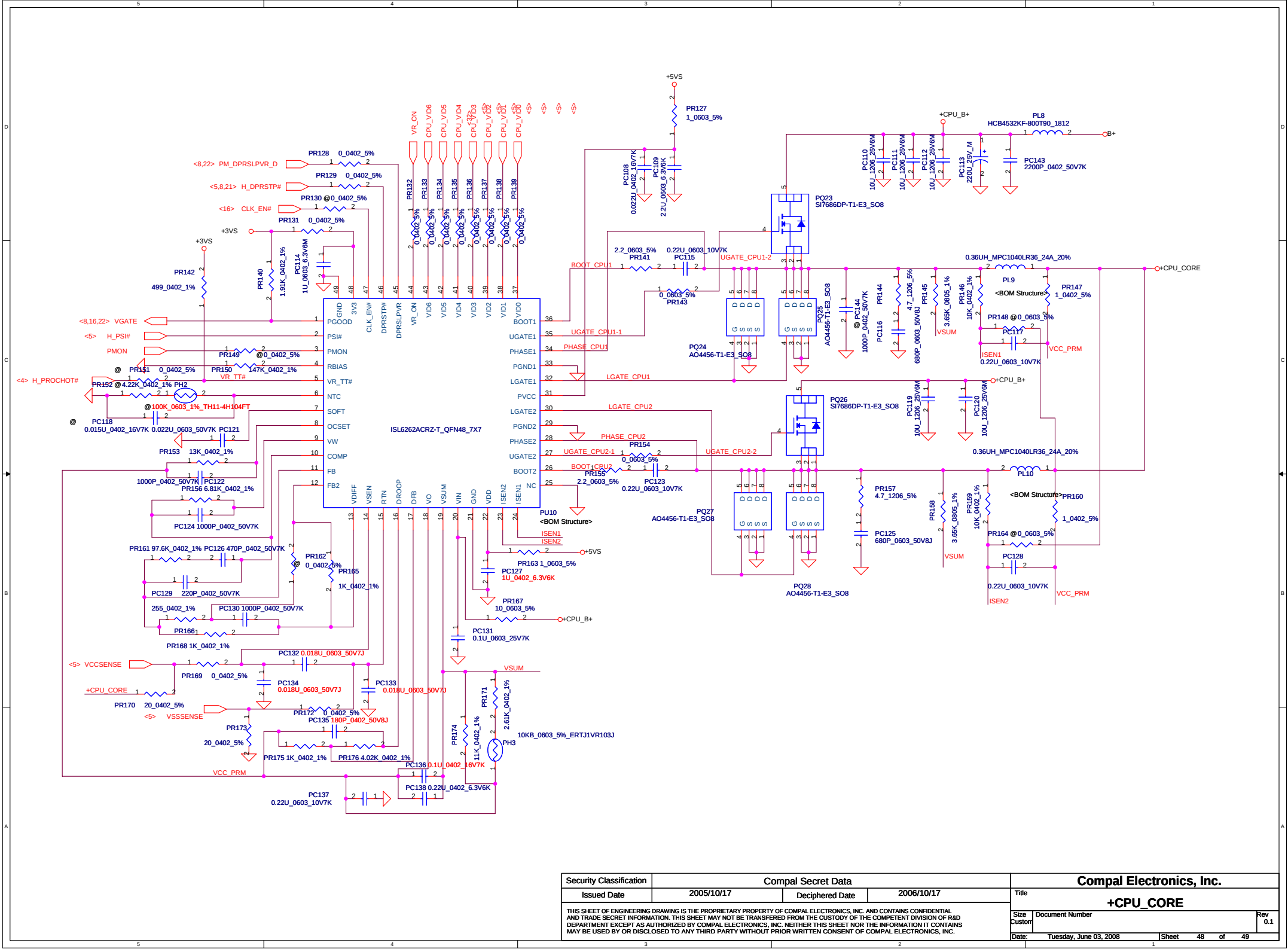
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					Size	Document Number		0.1	Rev
					Custom				
					Date:	Wednesday, May 28, 2008		Sheet	46



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page	Reason for change	Modify list
	Add original ACIN detector fun,and del TI fun.	ADD PR6, Del PQ11, PR61
	Change PC28 to 0.1U for common design	PC28
	Change PR16,PR32 & PR77 to 1% for common part	PR16 & PR32 & PR77
	Change PC55 to 0.1U_0603 for common design	PC55
	Add PC139 for 3/5V 2nd source	PC139
	Change PQ21 to A04712 and PL7 to 1.8UH for cost	PQ21 & PL7
	Change PC12 and PC13 to 0402 for source suggest	PC12 & PC13
	Change PR176 to 4.02K for load line	PR176
	Change 1.05V VIN from 5valwp to 5VS. reduce S3 power loss	
	Del PR83 for extra pull-high R	
	Add cpu_core boost and sunnber for EMI request	Add PR141,PR144,PC116,PR155,PR157 &PC125
	Add 1.05VSP boost and sunnber for EMI request	Add PR113,PR117 &PC98
	Fixed CV mode	Add PR56,Del PR57&PR60
	Adjust 1.05V to 1.074 for HW request	Modify PR120 to 2.37K
	Adjust 1.5V to 1.527 for HW request	Modify PR93 to 22K
DVT	Del PR73 for fix 3V in 2nd source	
	Add PQ30,PQ31, PR178,PR179,PR180,PC141	Prevent ACOP protection by charger
	Modify PQ10 to SOT322	Layout limit
	Modify 1.5V to susp#	Add PR177, Del PR170
	Modify PR36 to 0.015 for rating & change PR45 to 100K	
	Modify PL9 & PL10 form NEC to TOKO	
	Modify PR108 to 2.2 for EMI request	
PVT	Fix 5valwp, so del PR71, change PR72 to 0	
	Change PC8 to Y5V type for costdown	
	Change PU6 & PC101 to PU500 &PC500 for BOM	
	Add PC142,PC143,PC144,PC145,PC146,PC147,PC149,PC150 for EMI request	
	Add PR40,PR181,PR107,PR109,PR46,PC37 & Del PR108 for EMI request	
	Change PQ24,PQ25,PQ27,PQ28 to A04456 for EOL	
PVT-1	Move PC500 & PU500 to X76 group.	
Pre-MP	Del PC144 & PC146 for EMI request	

Title		<Title>	
Size	Document Number	Rev	
Custom	<Doc>	<Rev Code>	
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