Compal Confidential

G470/G570 DIS+UMA+Muxless M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Robson/PX3.0,PX4.0

2010-07-22

LA-6758P

REV:0.1

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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: Cover Page

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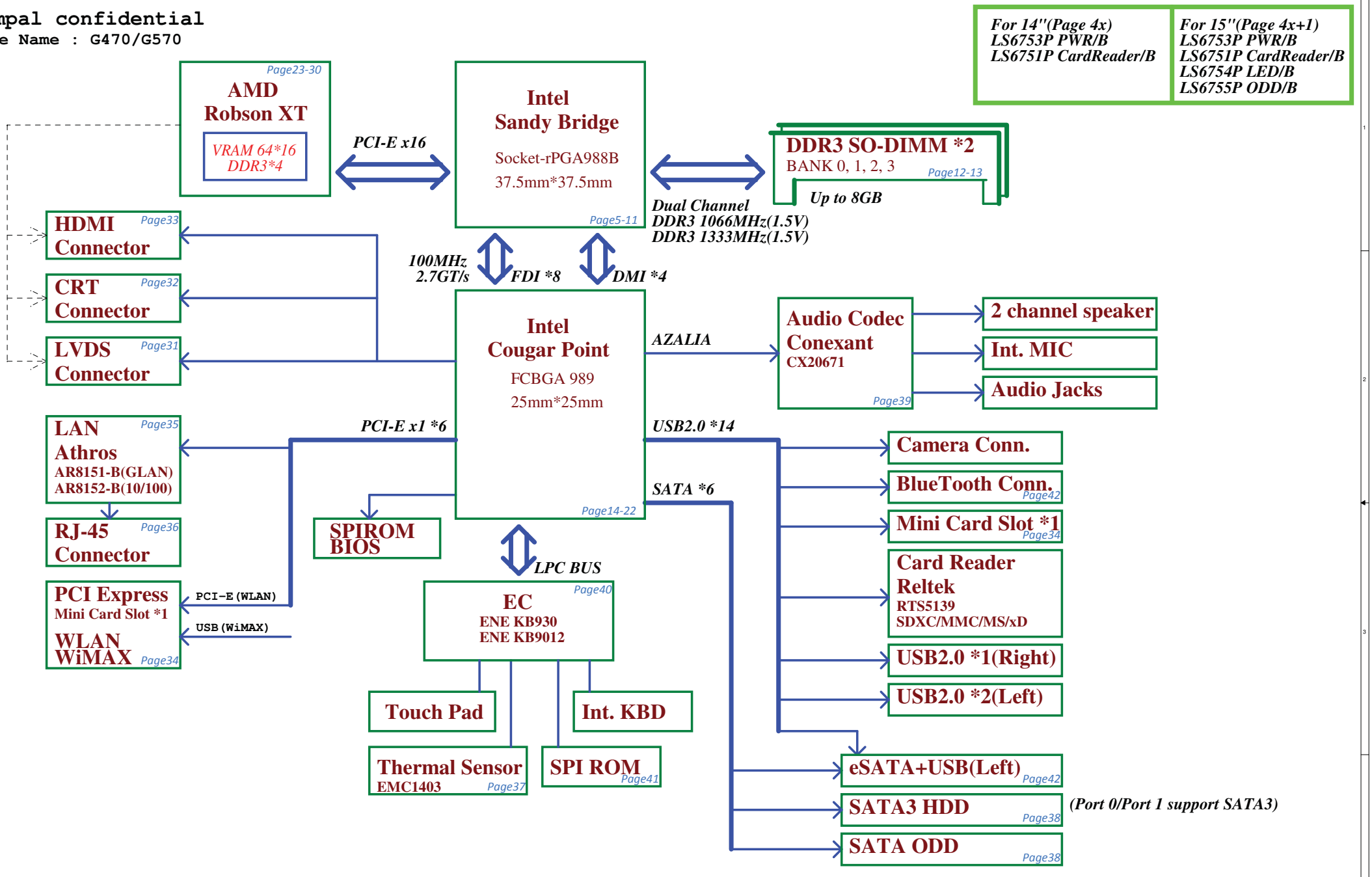
File Name : G470/G570



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Issued Date	2010/07/12	Deciphered Date 2012/07/11	Title: Block Diagram
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			Date: Tuesday, August 17, 2010; Sheet 2 of 57

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Thermal Sensor EMC1402-1	100_1100 b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
UMA only	PX@
Muxless	PX@+VGA@
Discrete Only	DIS@+VGA@
PX3.0 only, not for BACO	PX3@
BACO	BACO@
COMMON HDMI	HDMI@
UMA HDMI	UMA_HDMI@
Discrete HDMI	VGA_HDMI@
eSATA	ESATA@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Cameara	CMOS@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Power-Up/Down Sequence

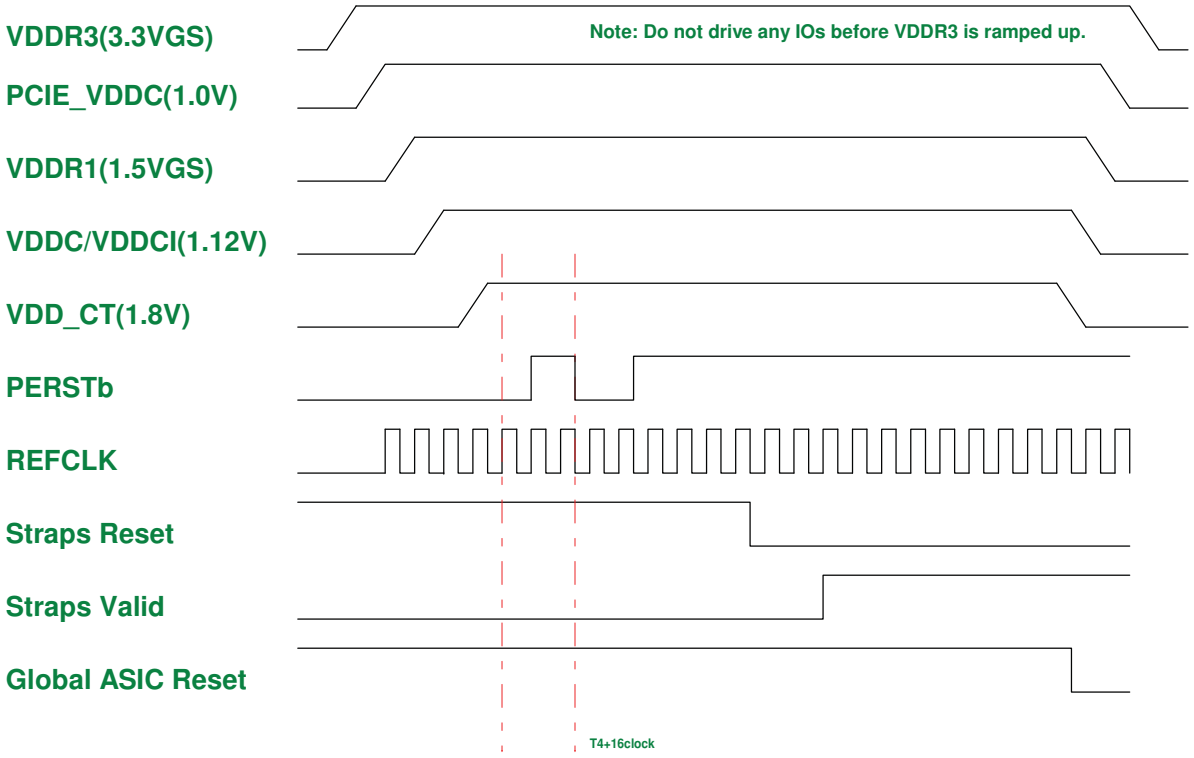
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



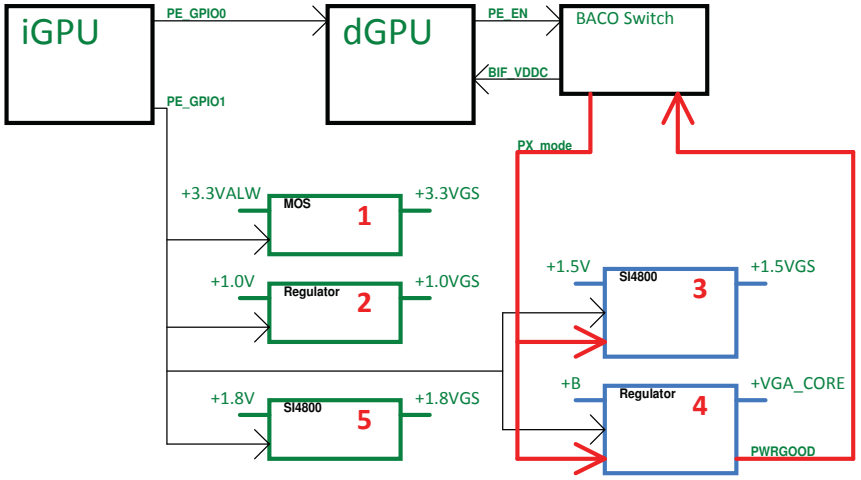
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

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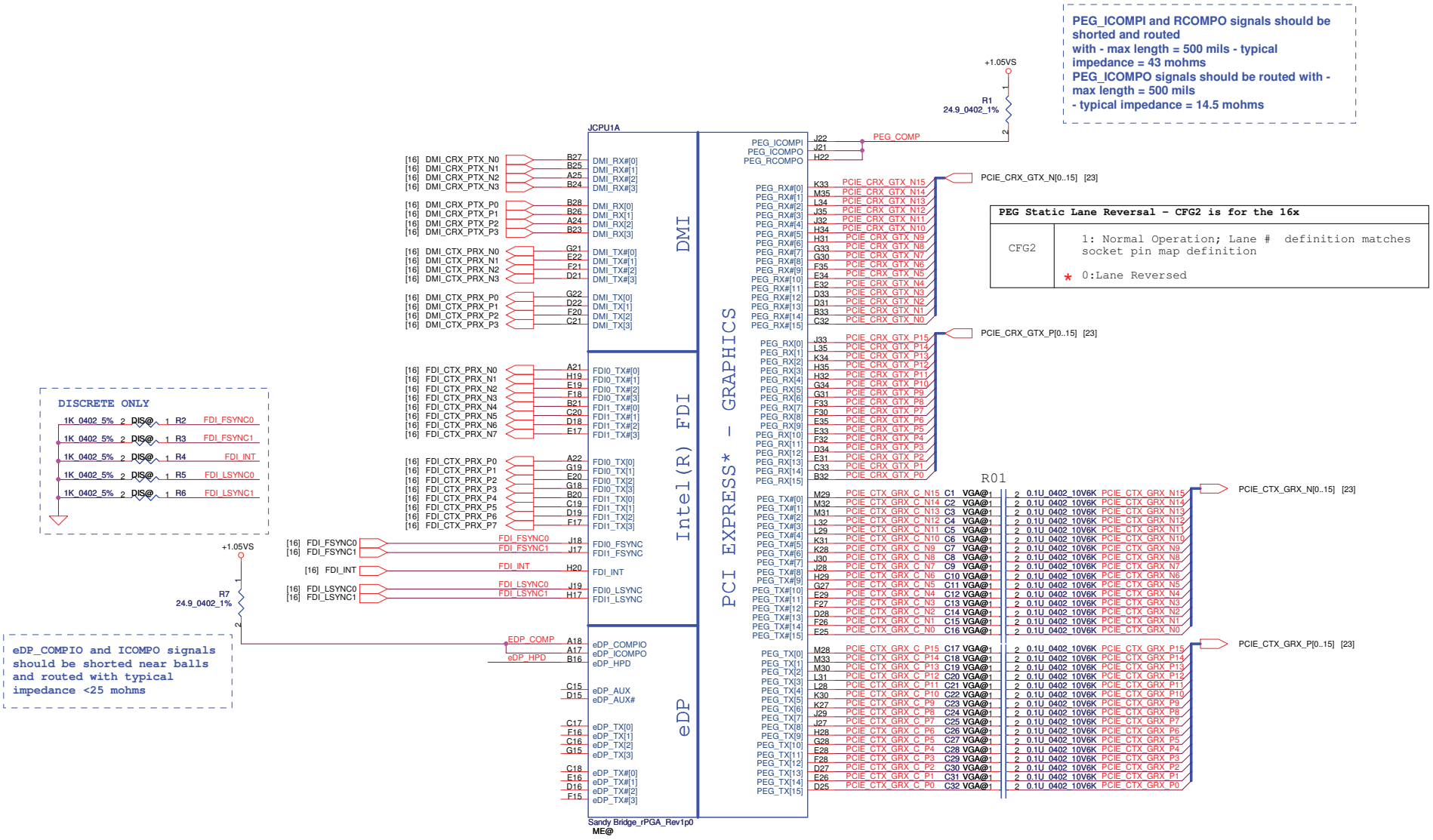

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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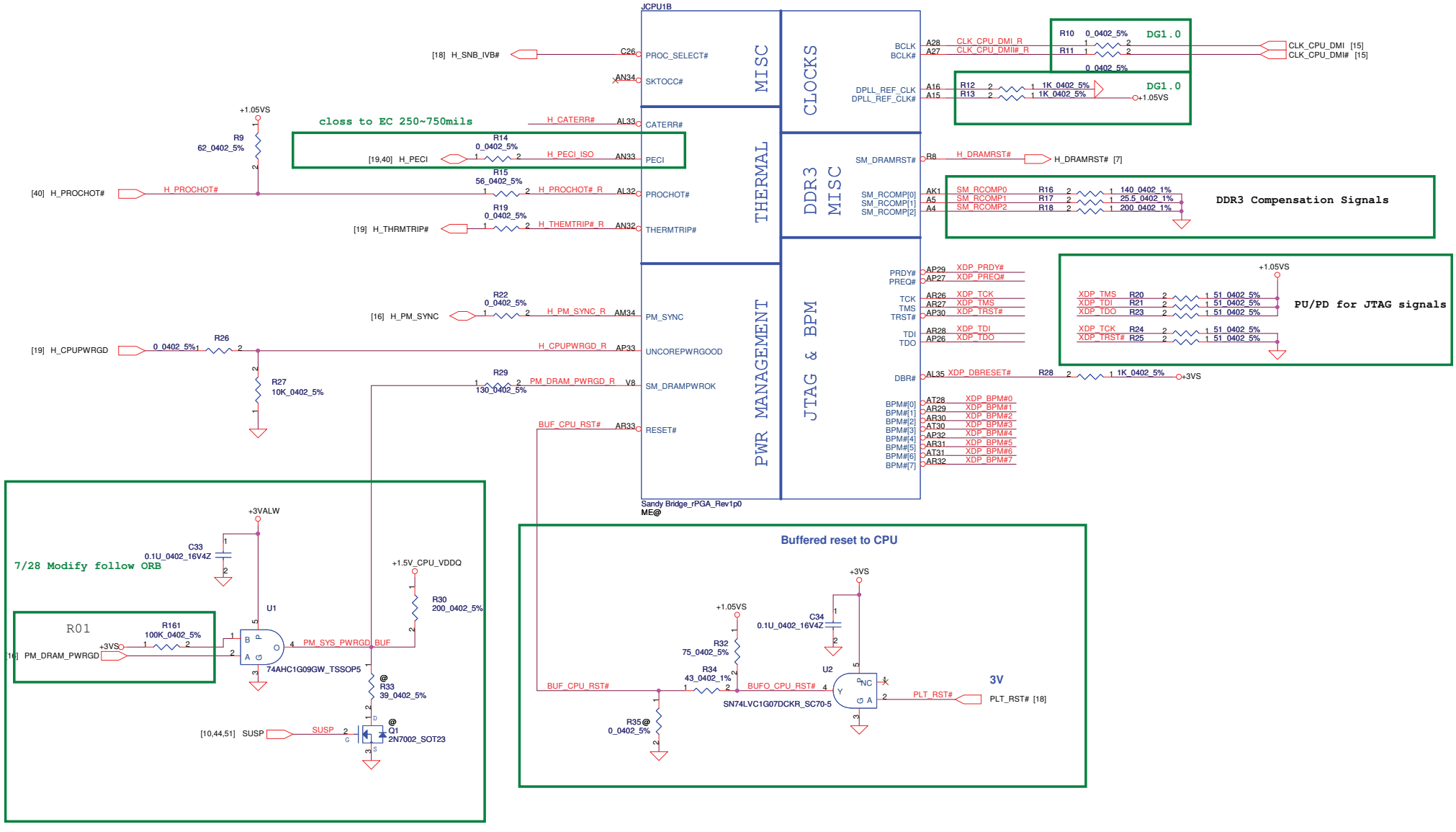

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Title: PROCESSOR(2/7) PM,XDP,CLK

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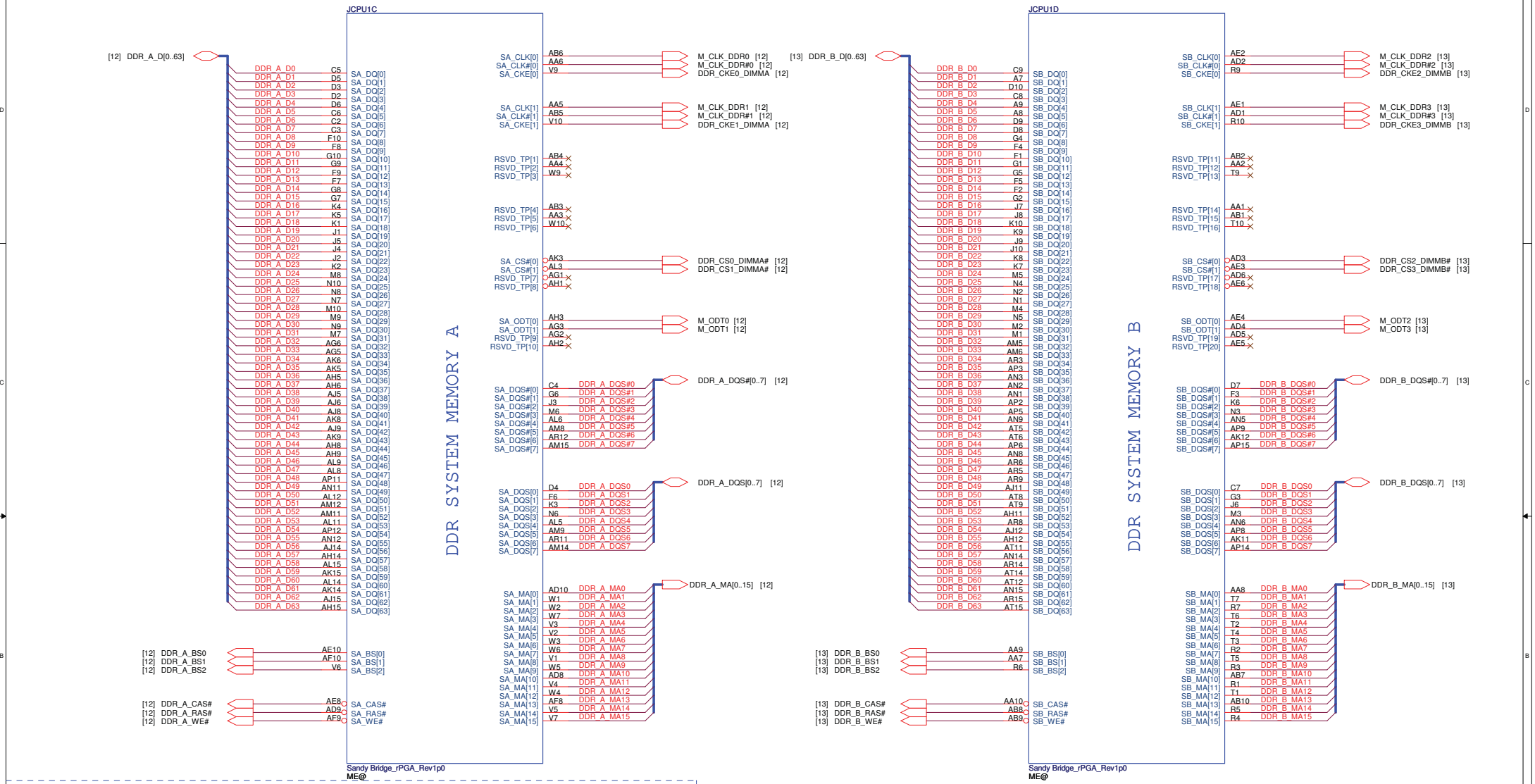

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Title: **PROCESSOR(3/7) DDRIII**

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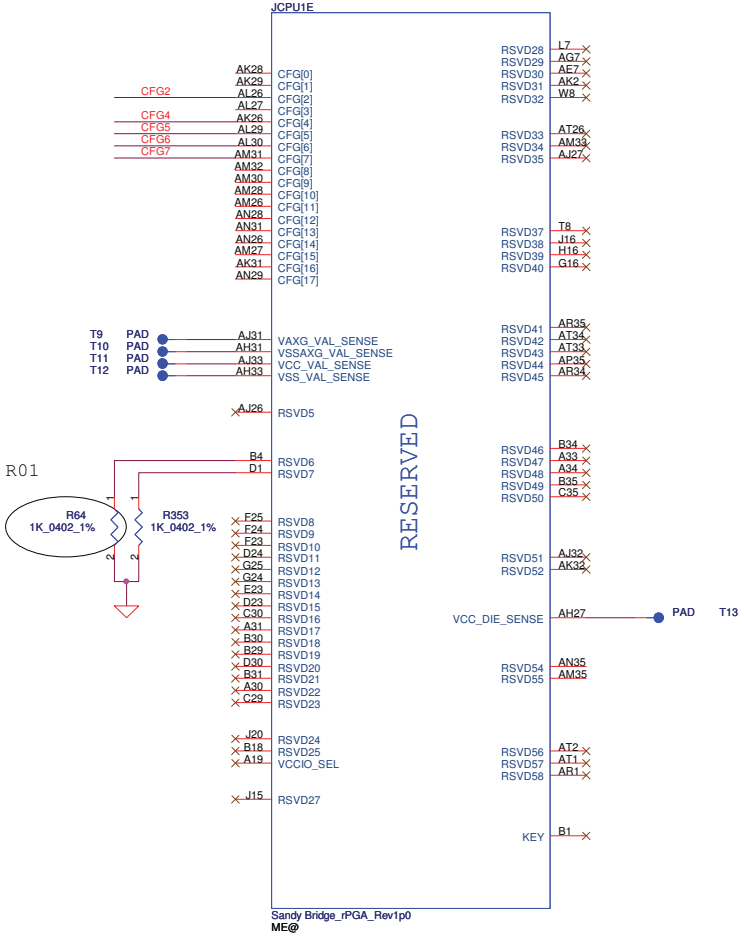
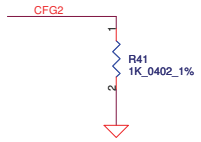
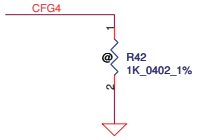
CFG Straps for Processor

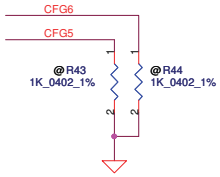




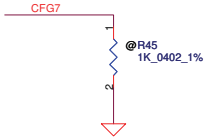
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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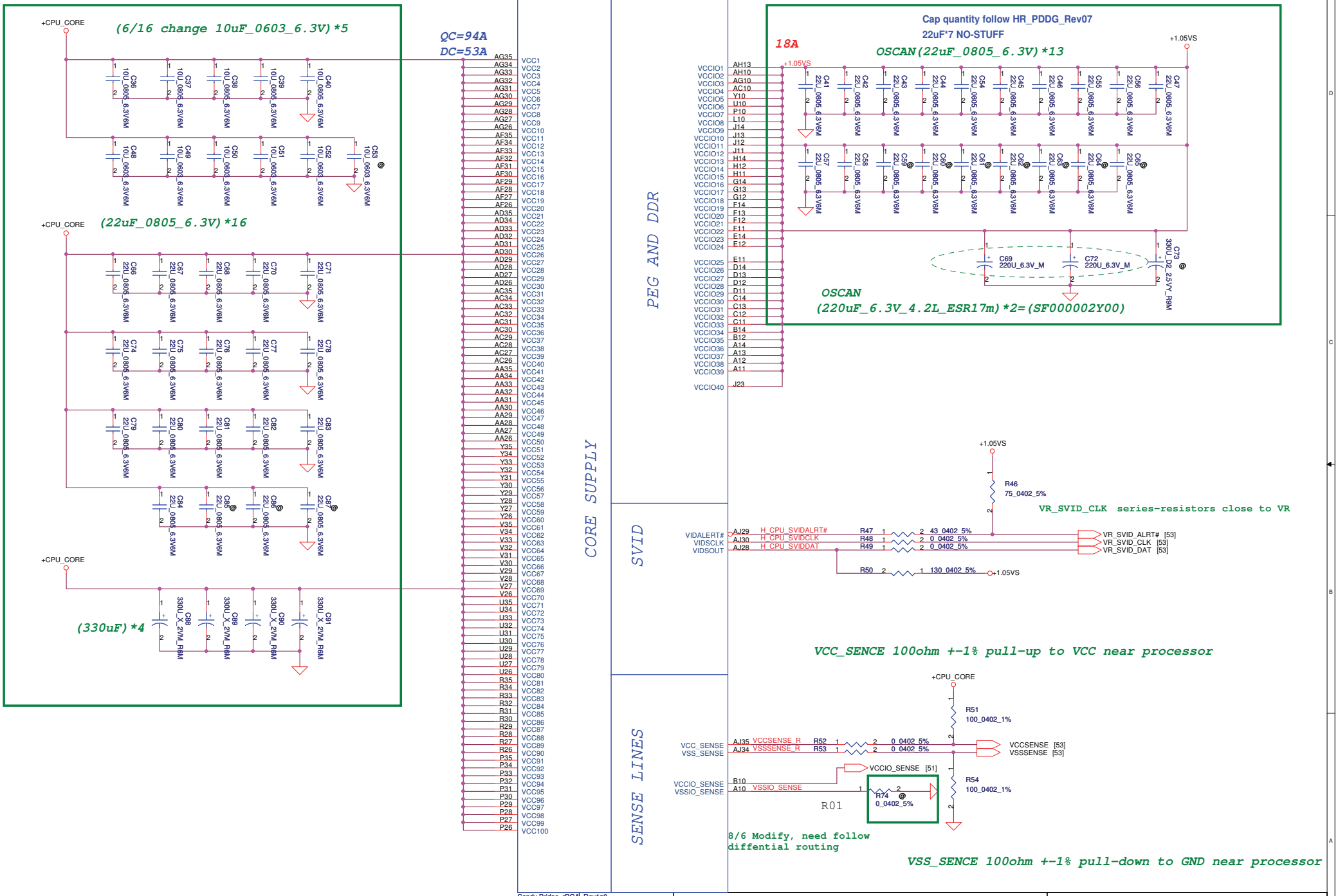
POWER



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Title: PROCESSOR(5/7) PWR,BYPASS

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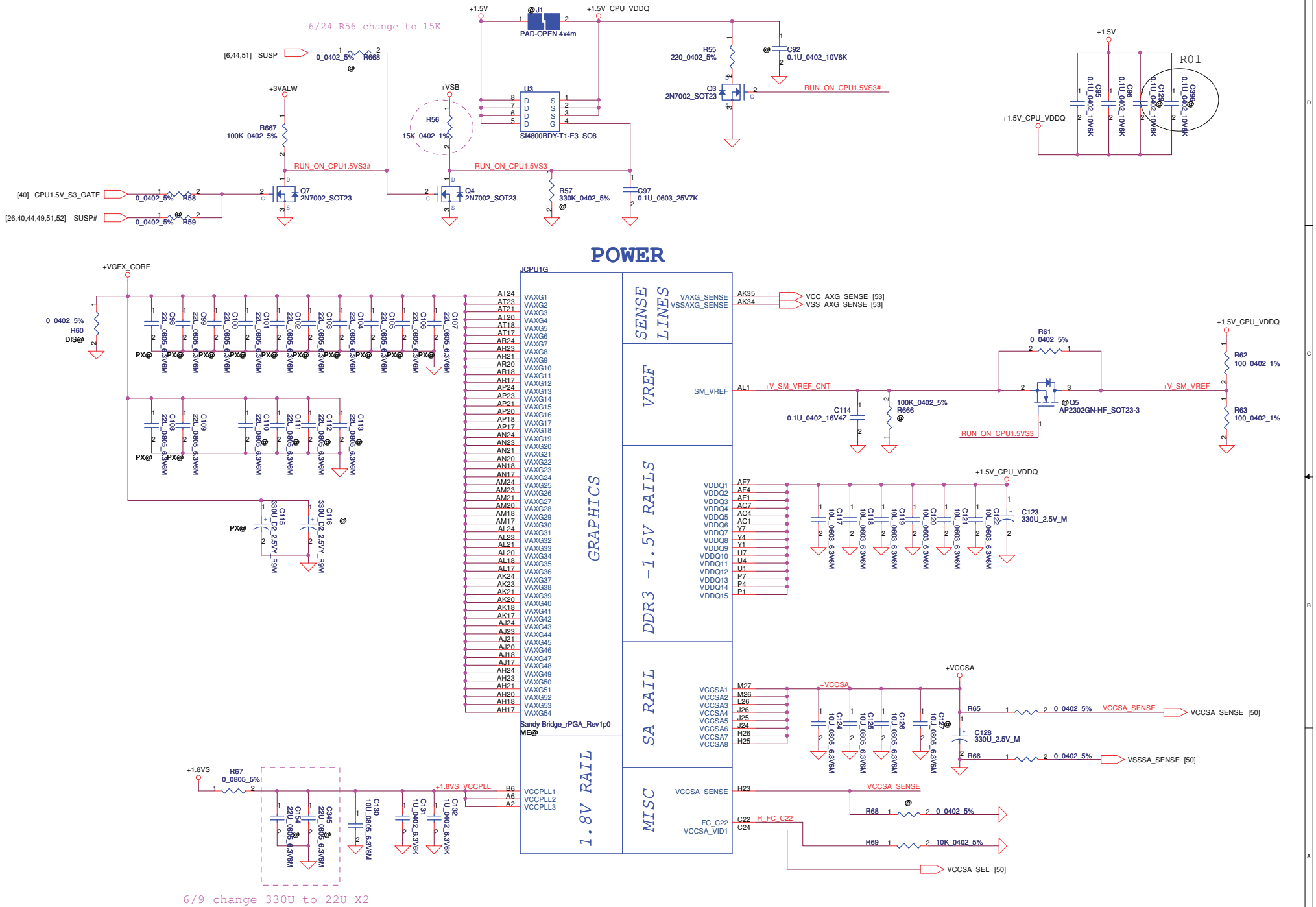

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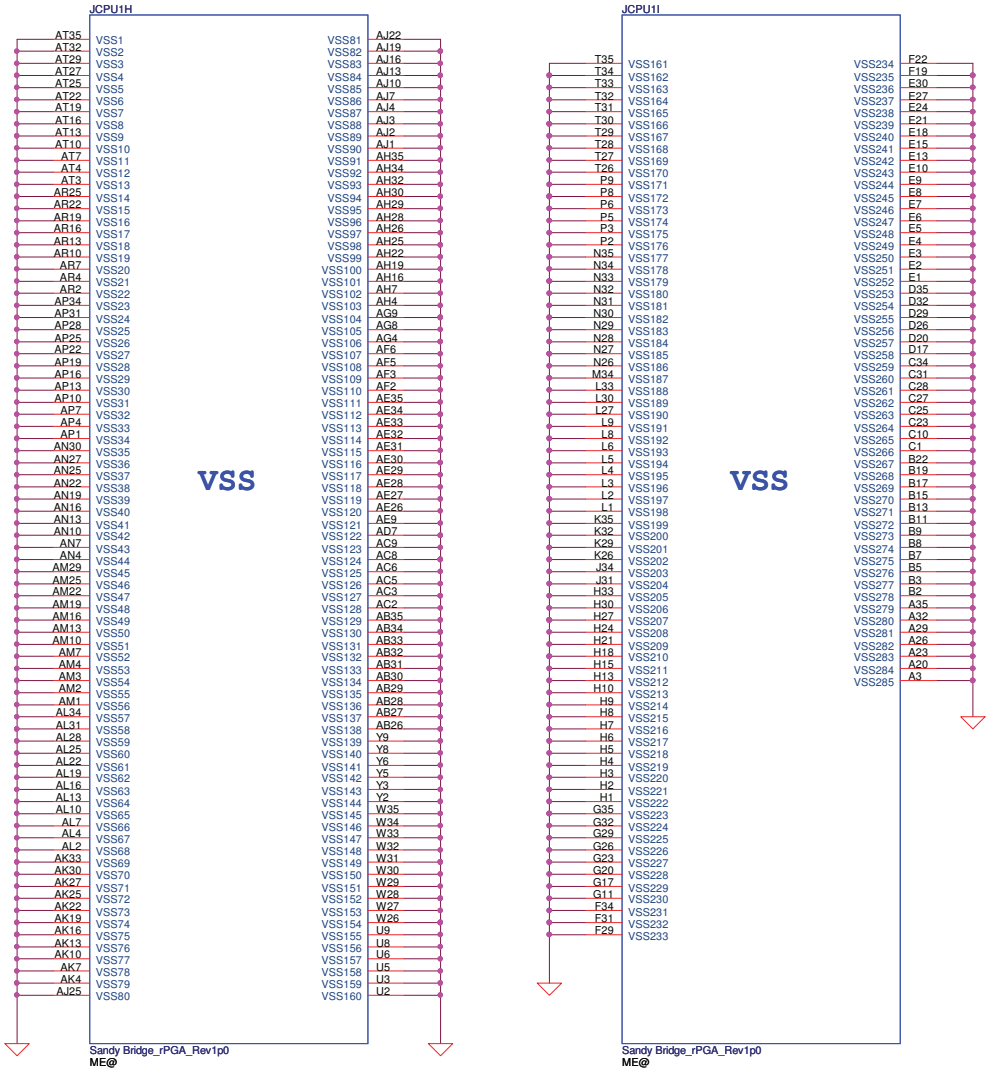

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DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@

[7] DDR_A_D[0..63]
[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_MA[0..15]

+VREF_DQ_DIMMA: R70 1K_0402_1%, R71 1K_0402_1%

DDR3_DRAMRST# [7,13]

[7] DDR_CKE0_DIMMA — DDR_CKE1_DIMMA [7]

[7] DDR_A_BS2

[7] M_CLK_DDR0, [7] M_CLK_DDR#0 — M_CLK_DDR1 [7], M_CLK_DDR#1 [7]

[7] DDR_A_BS0 — DDR_A_BS1 [7], DDR_A_RAS# [7]

[7] DDR_A_WE#, [7] DDR_A_CAS# — DDR_CS0_DIMMA# [7], M_ODT0 [7]

[7] DDR_CS1_DIMMA# — M_ODT1 [7]

+VREF_CA: R72 1K_0402_1%, R73 1K_0402_1%

SMB_DATA_S3 [13,15,34], SMB_CLK_S3 [13,15,34]

+3VS: R81 10K_0402_5%, R83 10K_0402_5%

+0.75VS

0.65A@0.75V

Layout Note: Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

Layout Note: Place near DIMM

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

7/28 Update connect GND directly

Layout Note: Place near DIMM

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Title: DDRIII-SODIMM SLOT1

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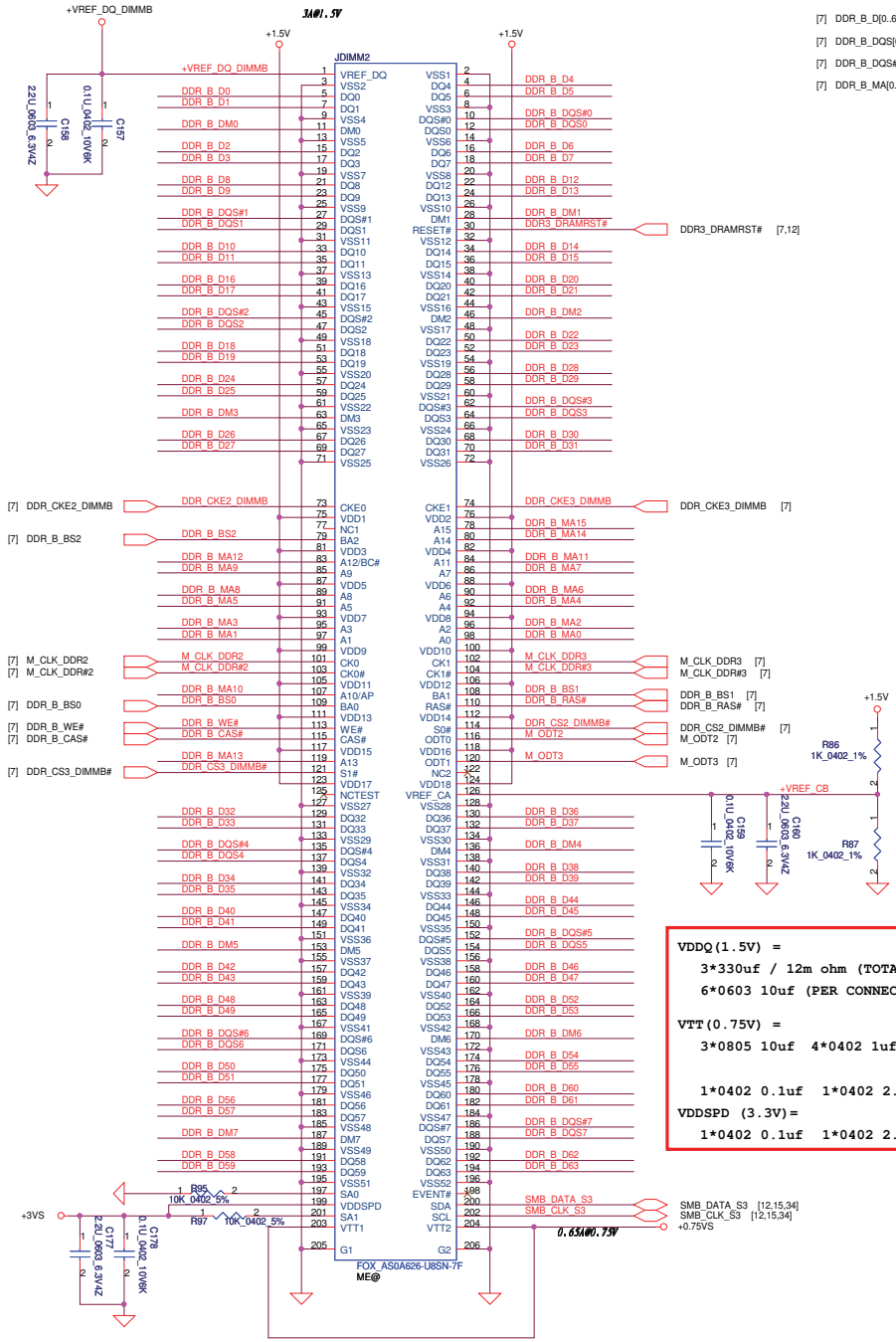
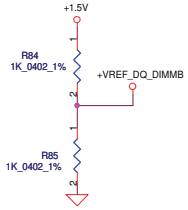




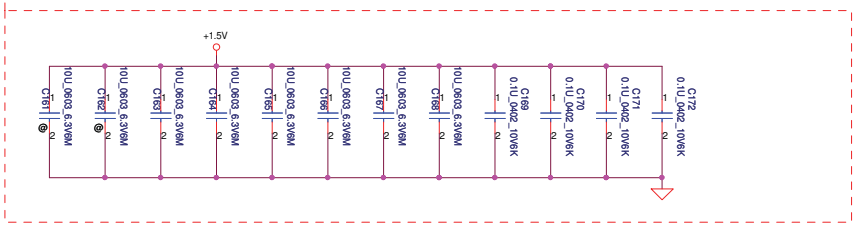
For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note: Place near DIMM

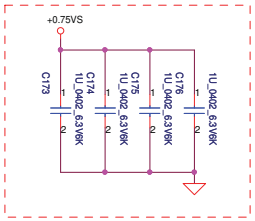
(10uF_0603_6.3V)*8

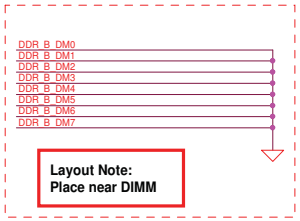
(0.1uF_402_10V)*4



Layout Note: Place near DIMM

7/28 Update connect GND directly





Layout Note: Place near DIMM

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 13 of 57

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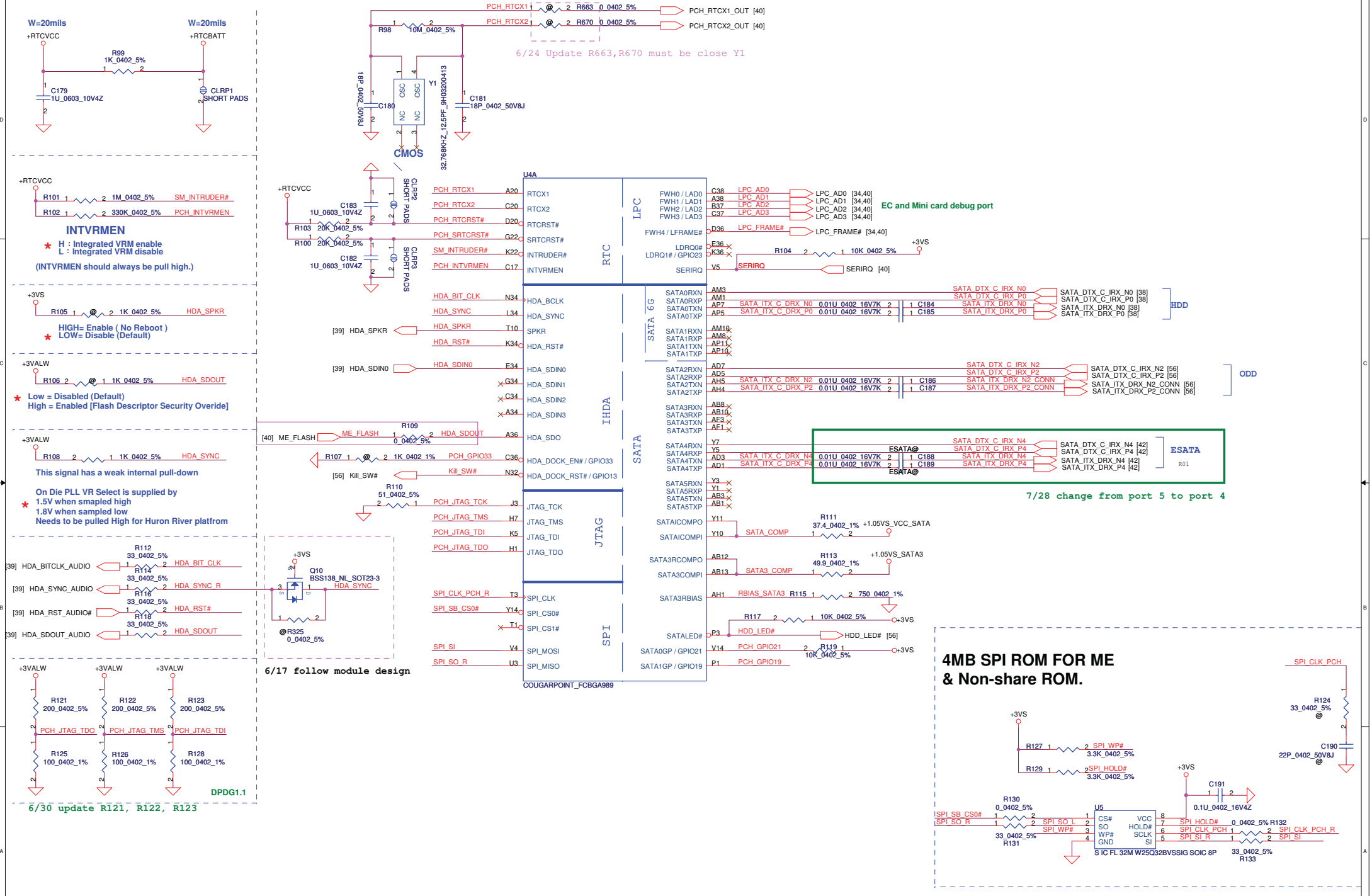

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Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 14 of 57

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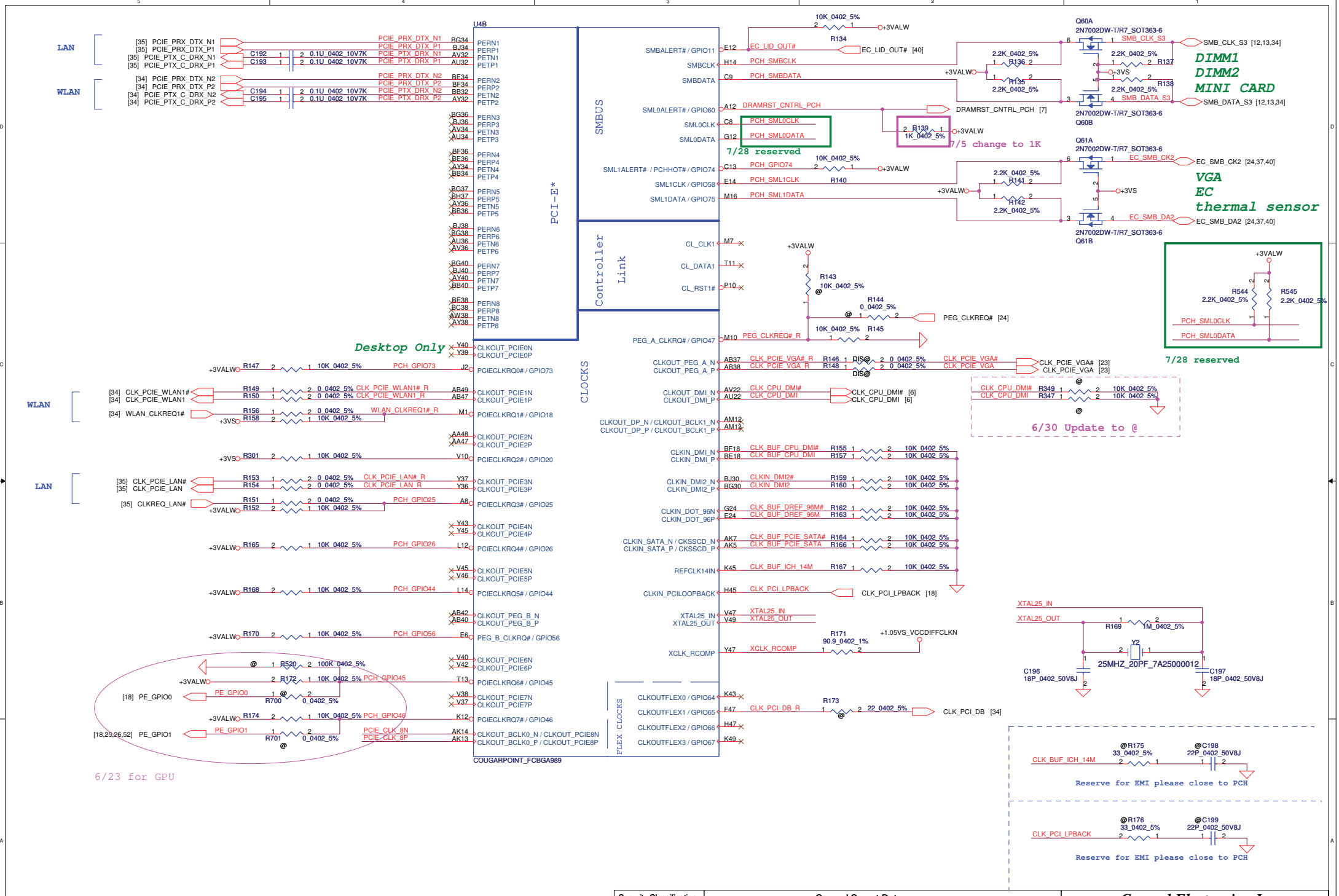

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Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 15 of 57

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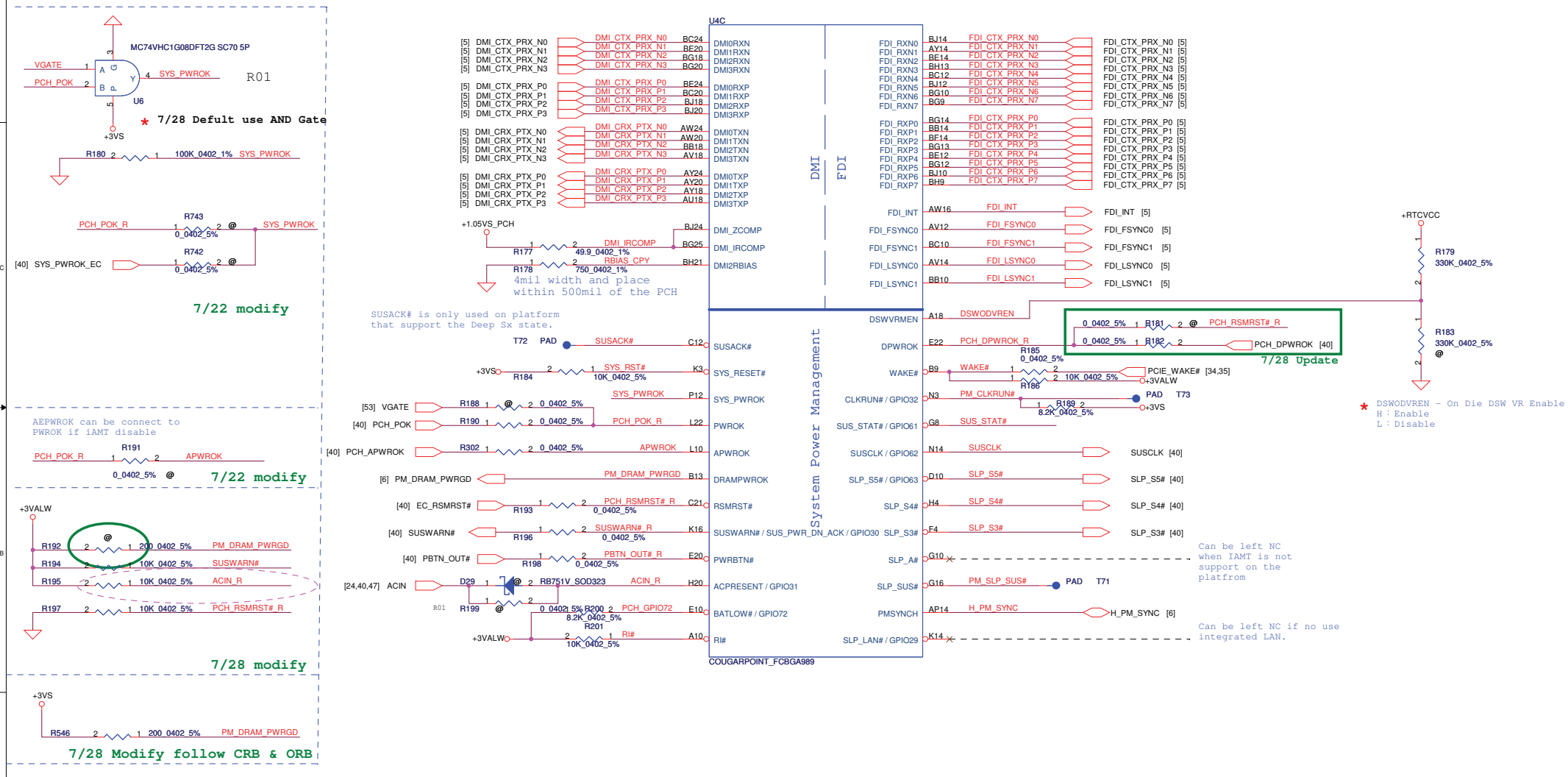

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,**

Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 16 of 57

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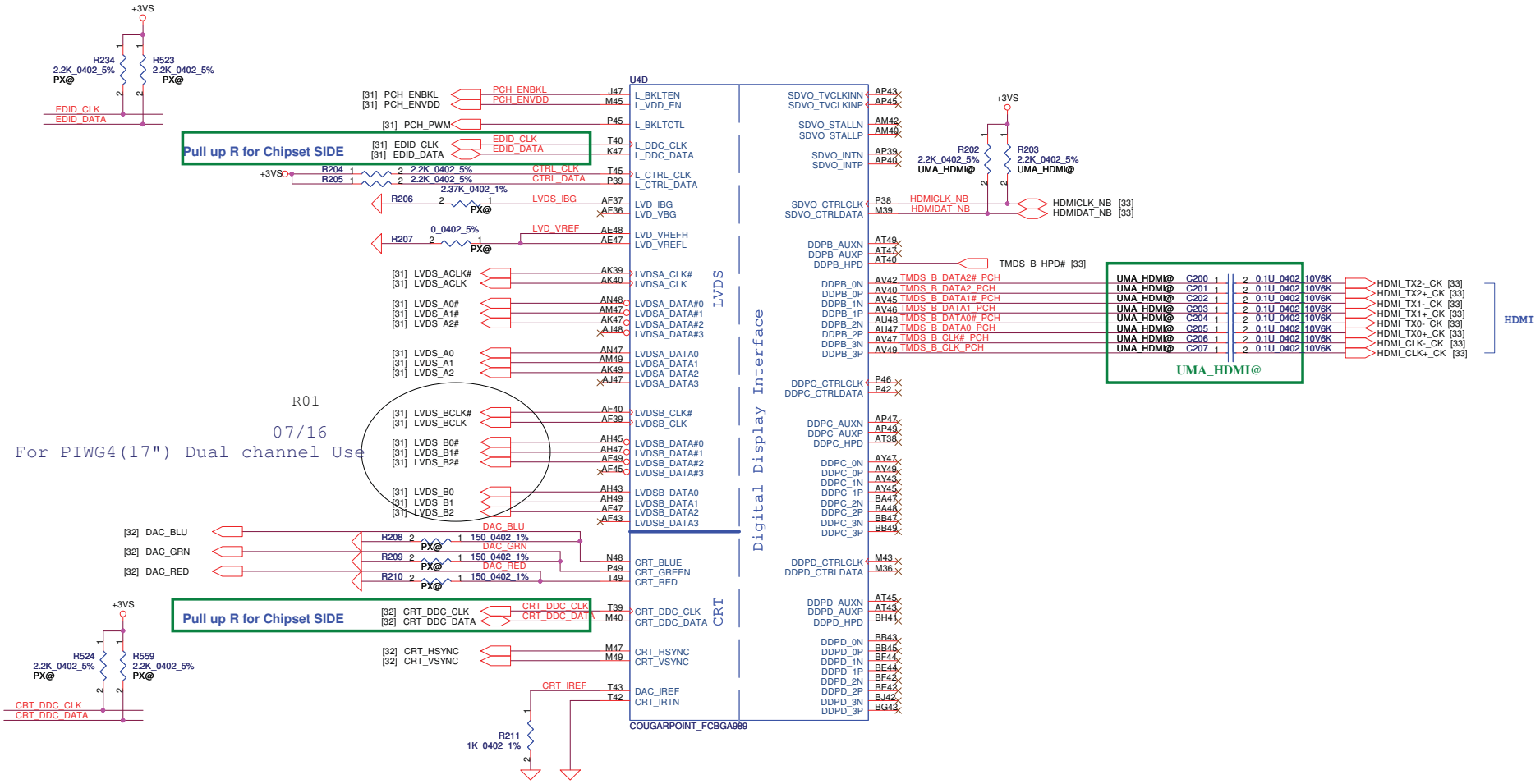

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Compal Electronics, Inc.

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 17 of 57

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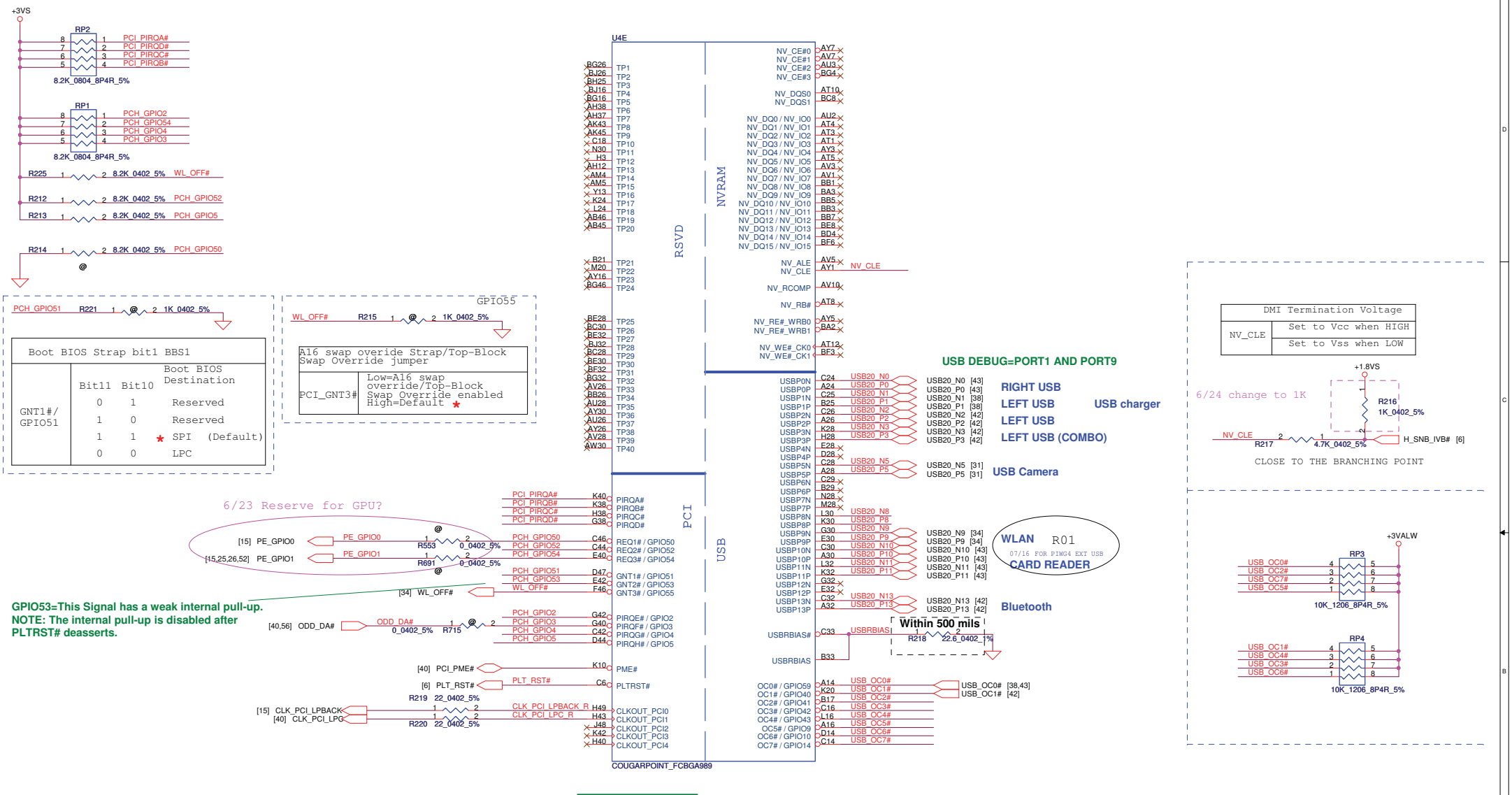

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: LA-6758P | Rev: 0.1

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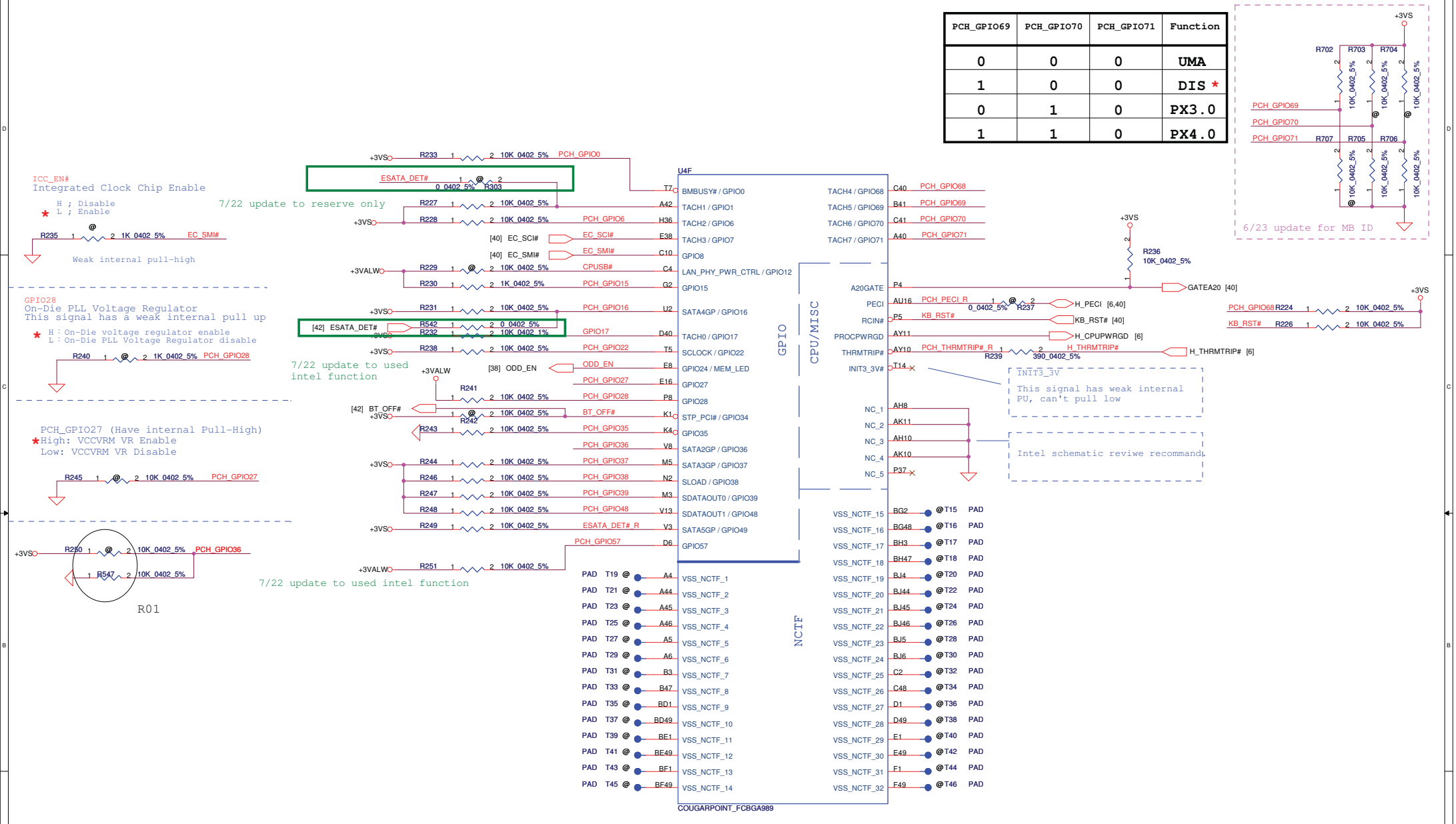
PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	0	0	DIS *
0	1	0	PX3.0
1	1	0	PX4.0



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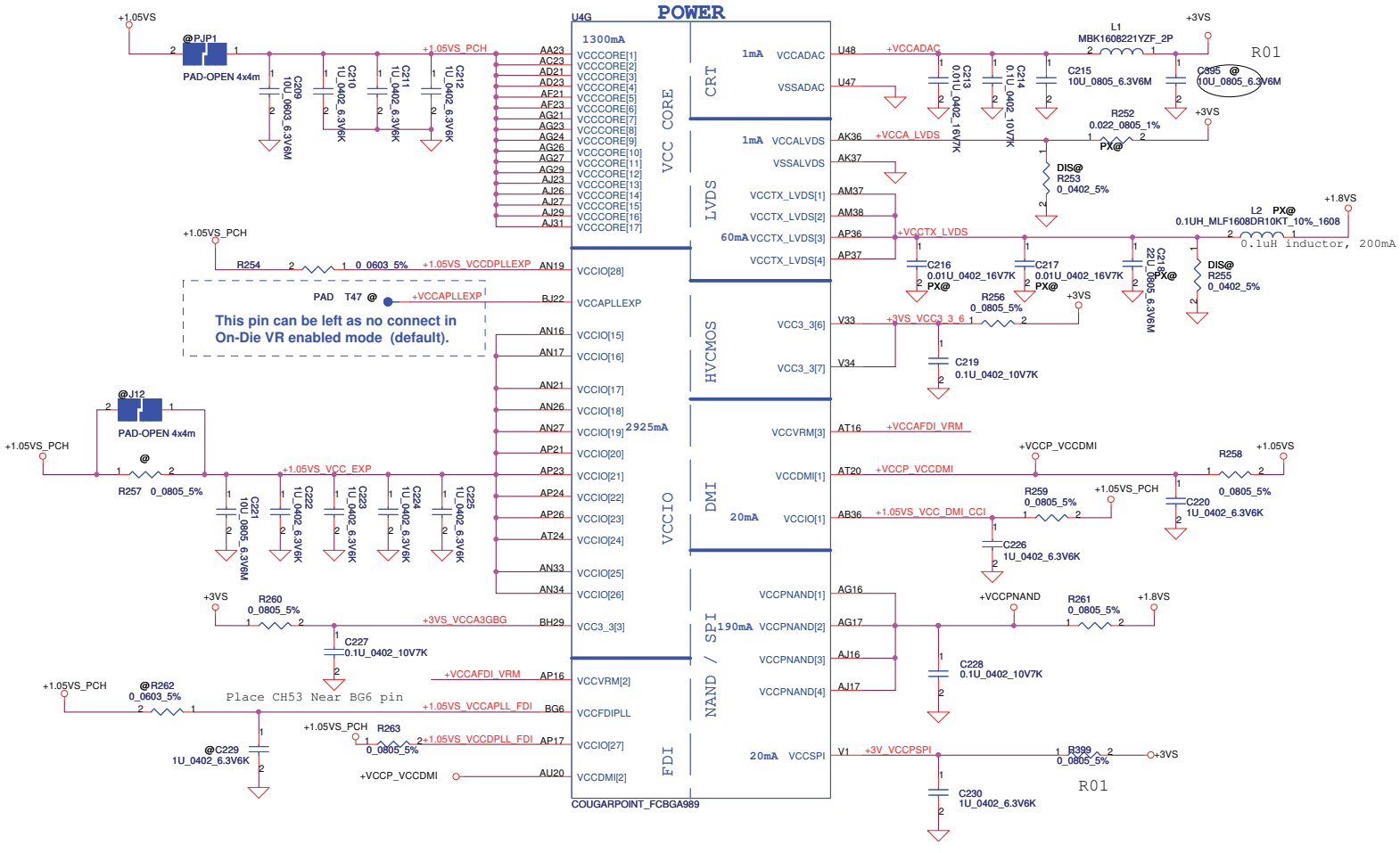
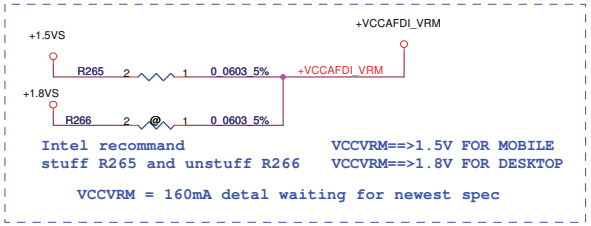
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 19 of 57





PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-6758P | Rev: 0.1

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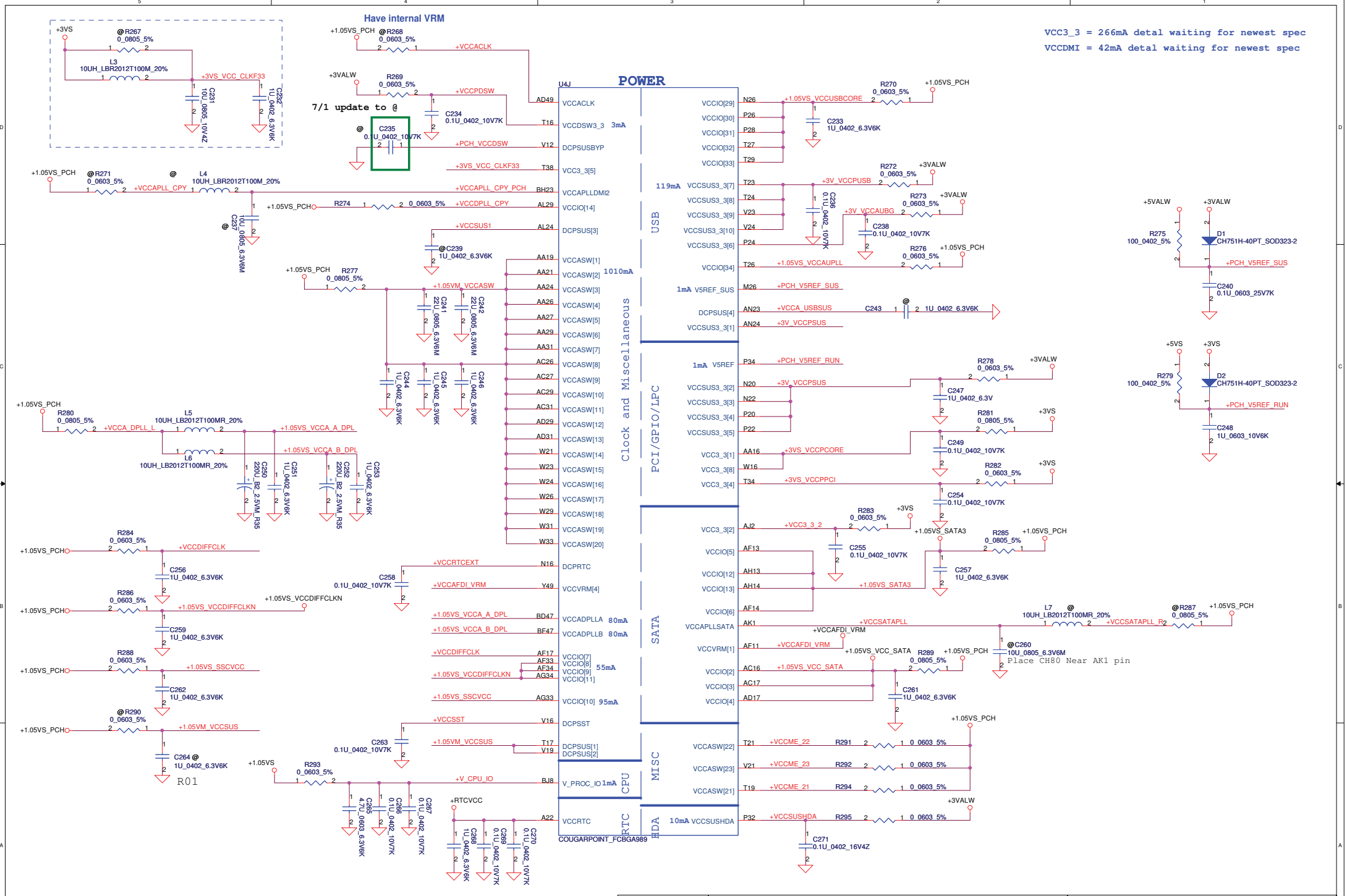

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Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 21 of 57

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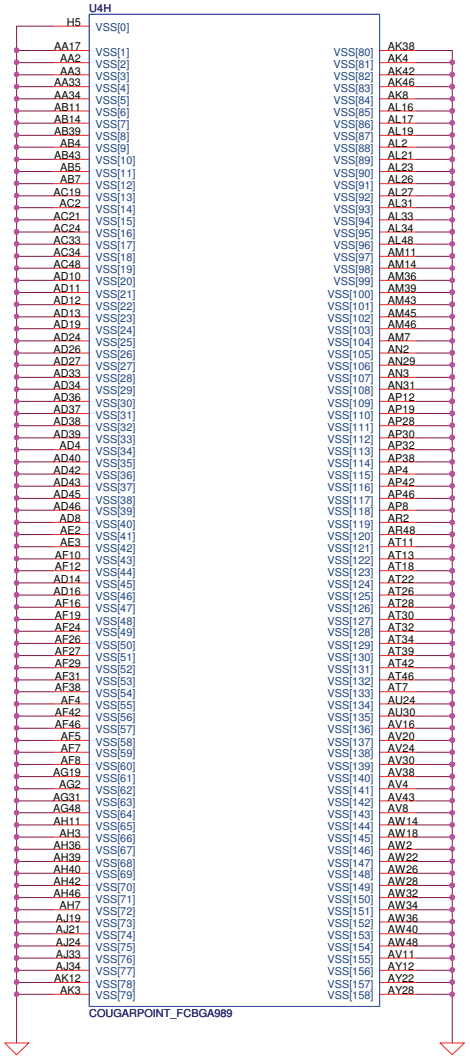

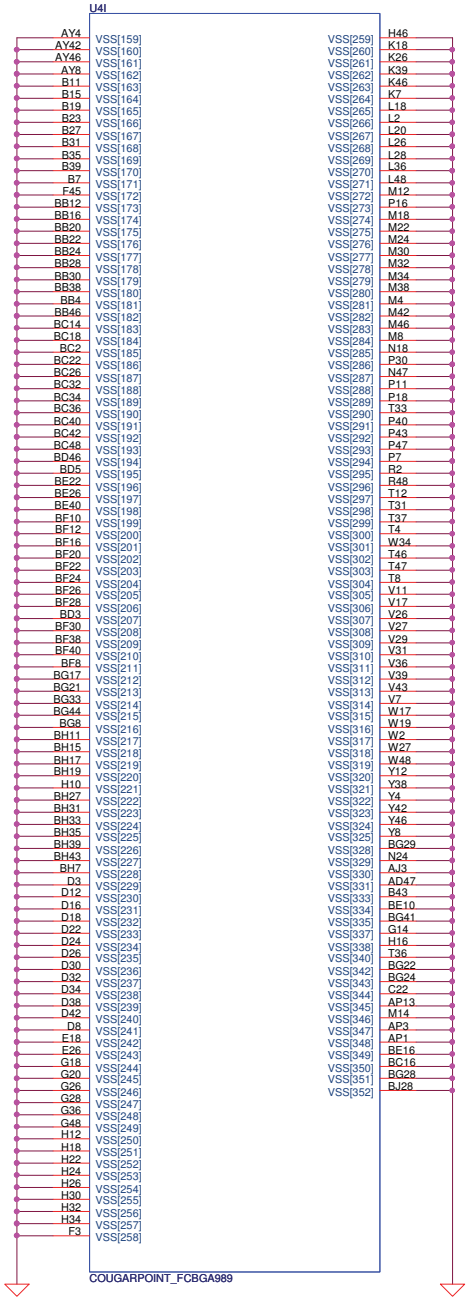

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Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

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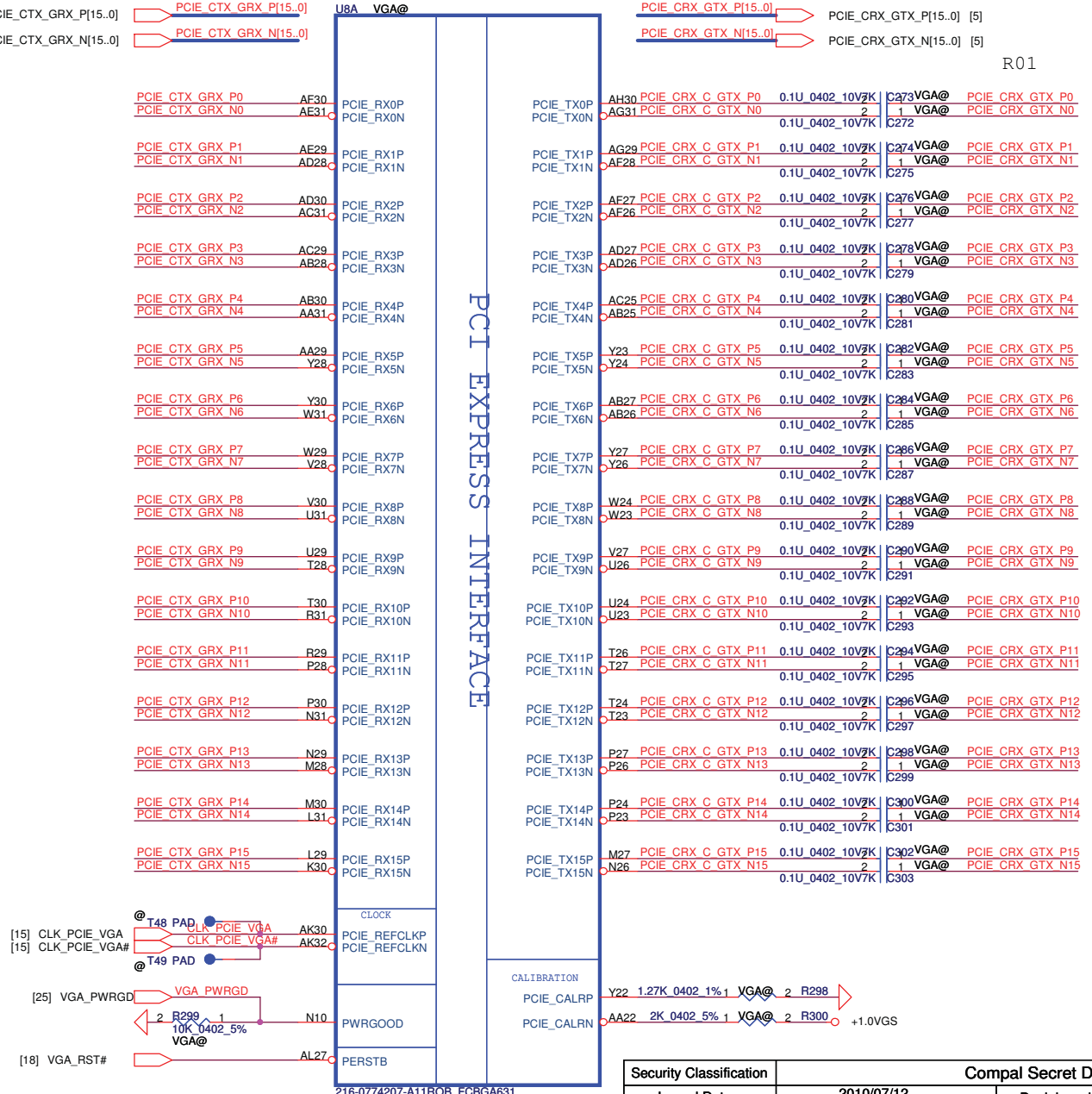
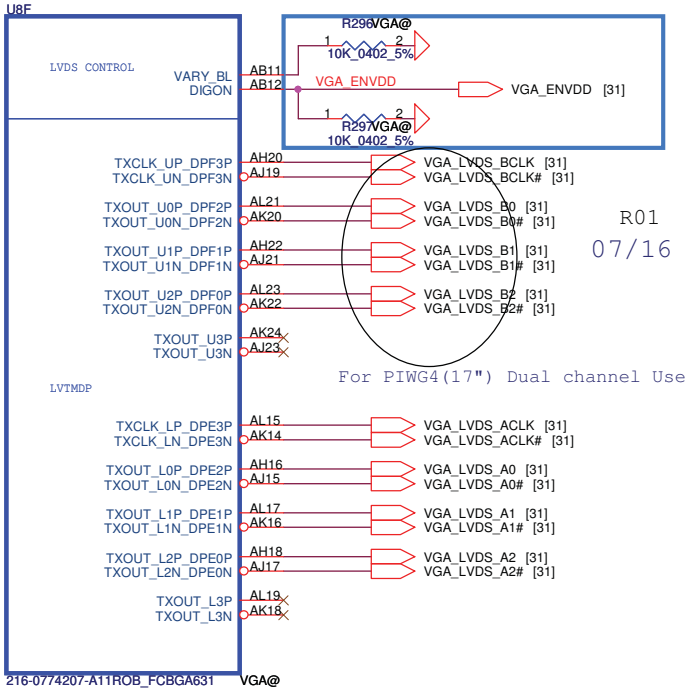


PCIE LANE



LVDS

VGA 0609

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: RobsonXT-S3 PCIE/LVDS
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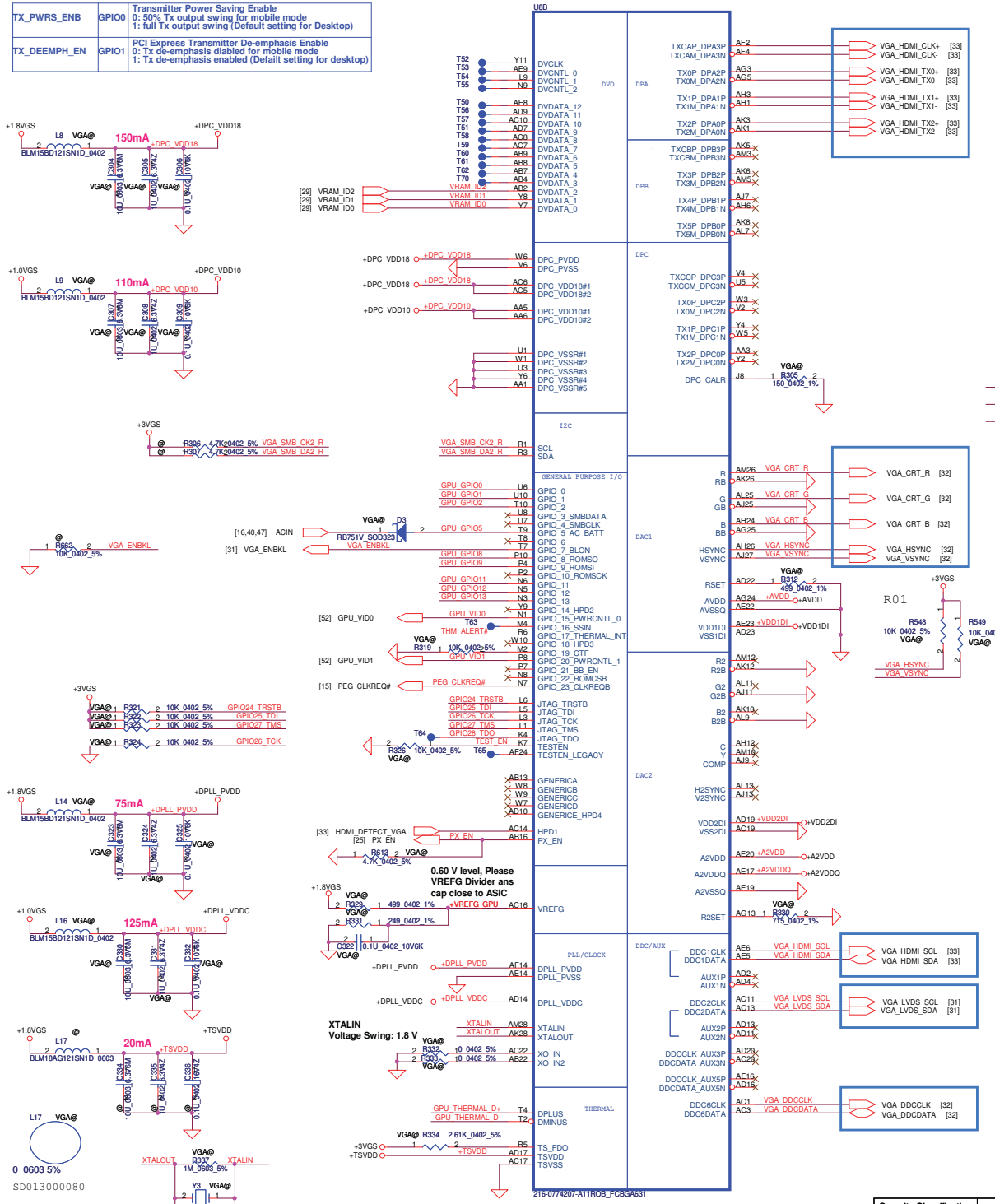
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

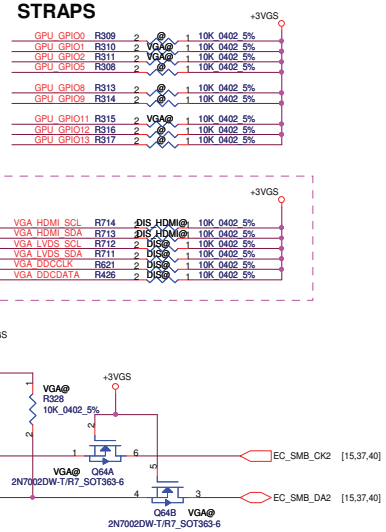
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

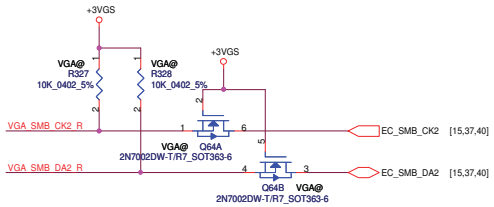
AMD RESERVED CONFIGURATION STRAPS

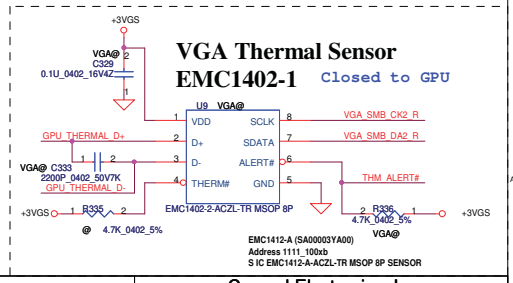
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

STRAPS







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Compal Electronics, Inc.

Title: RobsonXT-S3 Main Generic/MSIC

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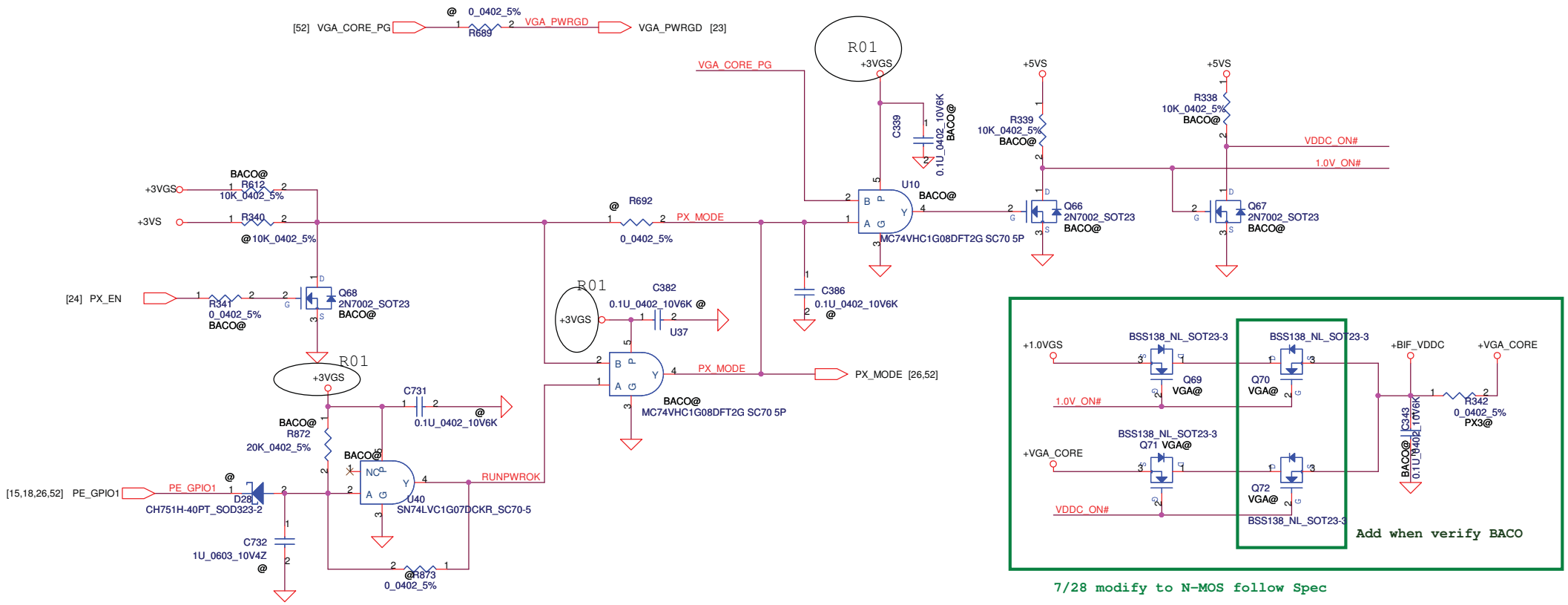

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Compal Electronics, Inc.

Title: PARK-S3 Main Generic/MSIC

Size: B | Document Number: LA-6758P | Rev: 0.1

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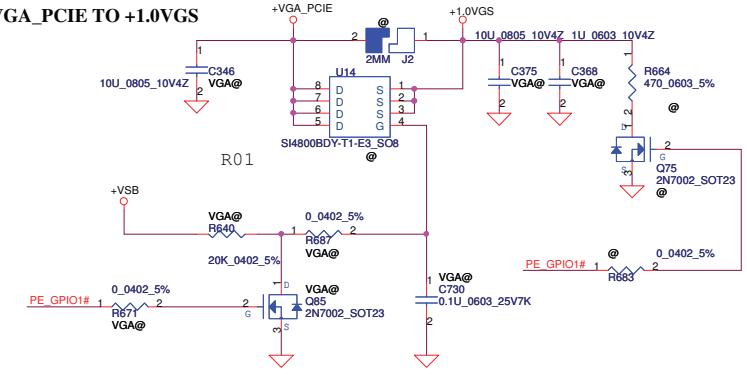
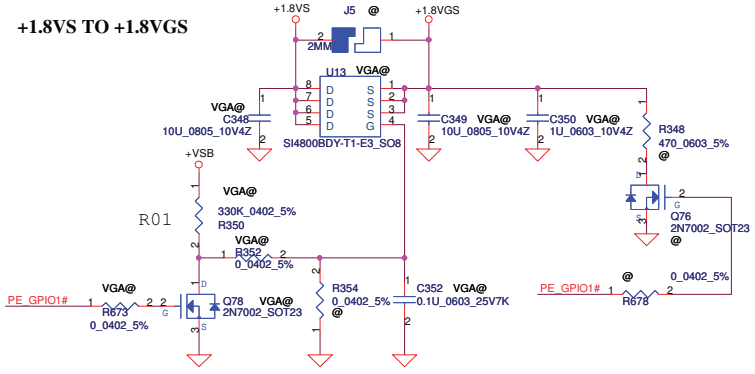
EVT Short J2 for DIS only

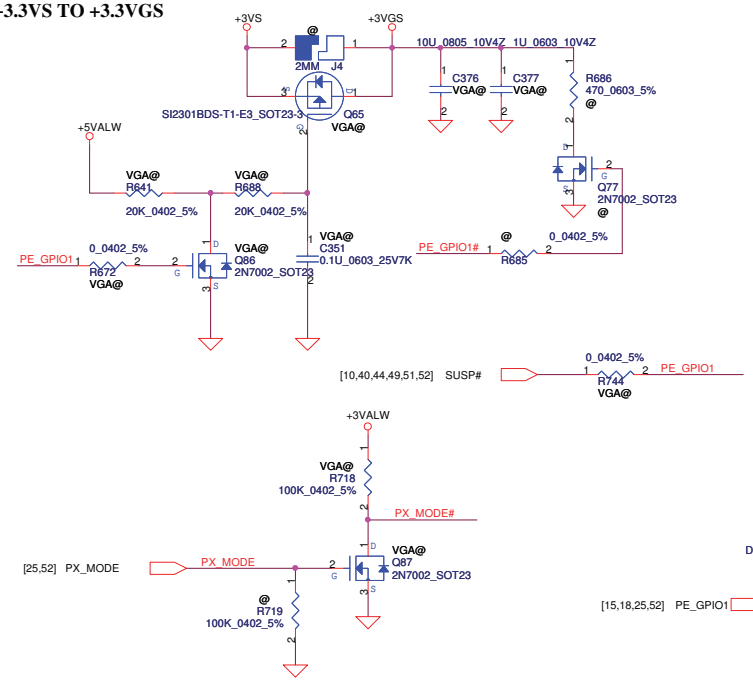
+VGA_PCIE TO +1.0VGS



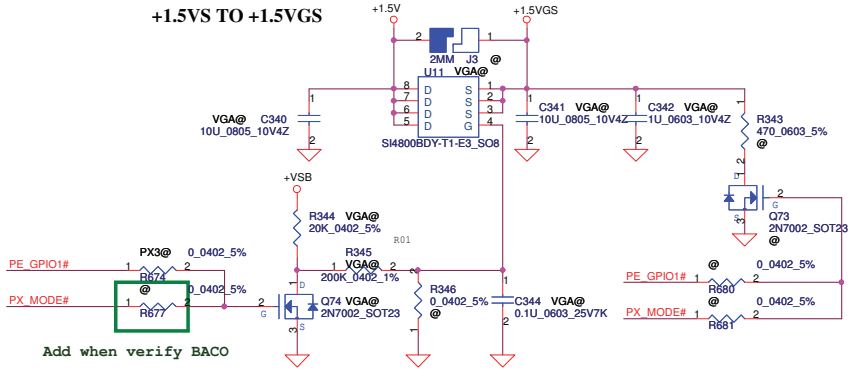
+1.8VS TO +1.8VGS



+3.3VS TO +3.3VGS



+1.5VS TO +1.5VGS



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Issued Date	2010/07/12	Deciphered Date 2012/07/11	Title PARK-S3 Main Generic/MSIC

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Custom	LA-6758P	0.1

Date: Tuesday, August 17, 2010 Sheet 26 of 57

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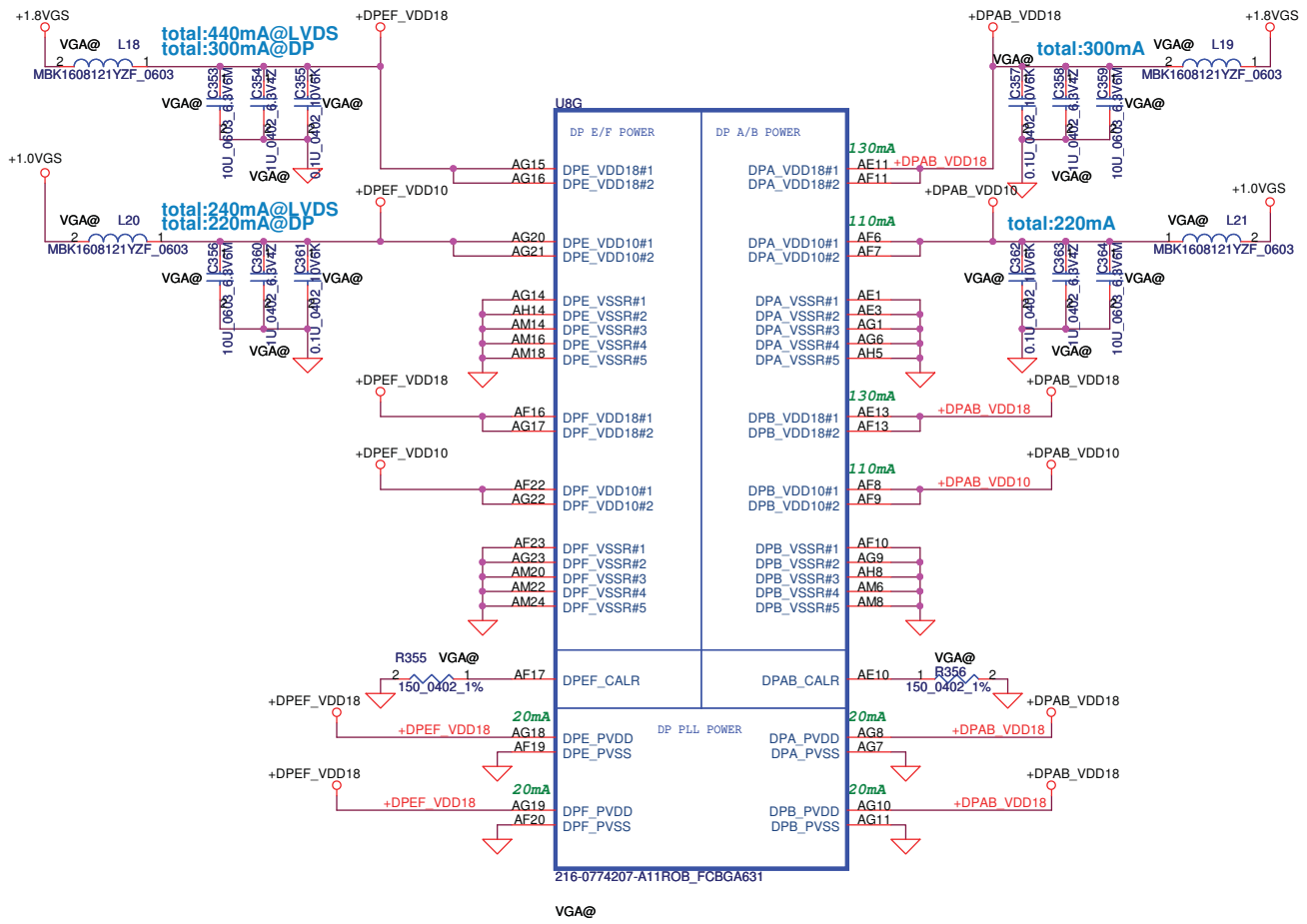

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: RobsonXT-S3 DP PWR

Size: B | Document Number | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 27 of 57

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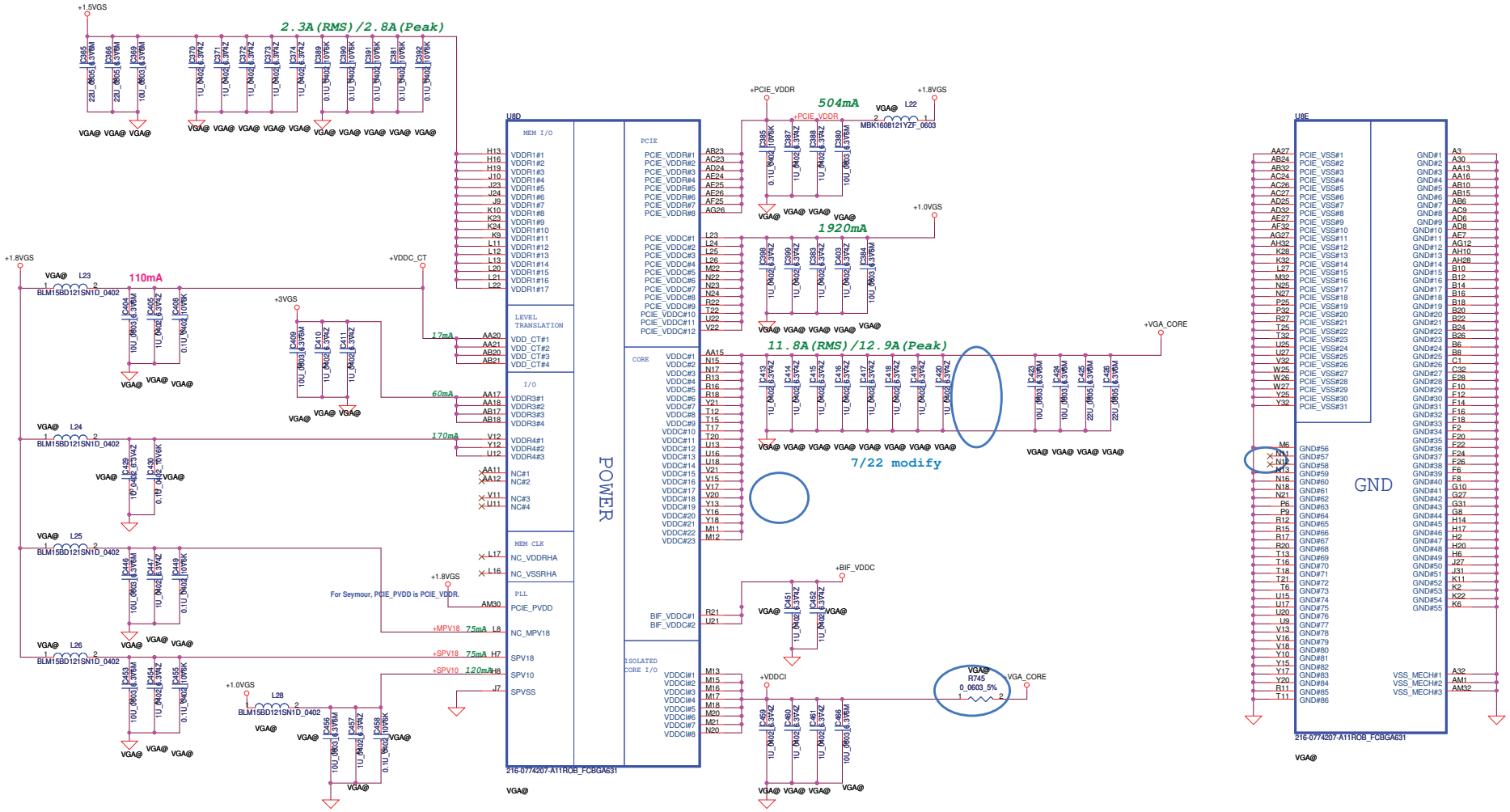

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: RobsonXT-S3 PWR/GND

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Size	Document Number	Rev
C		0.1

Date: Tuesday, August 17, 2010 Sheet 28 of 57

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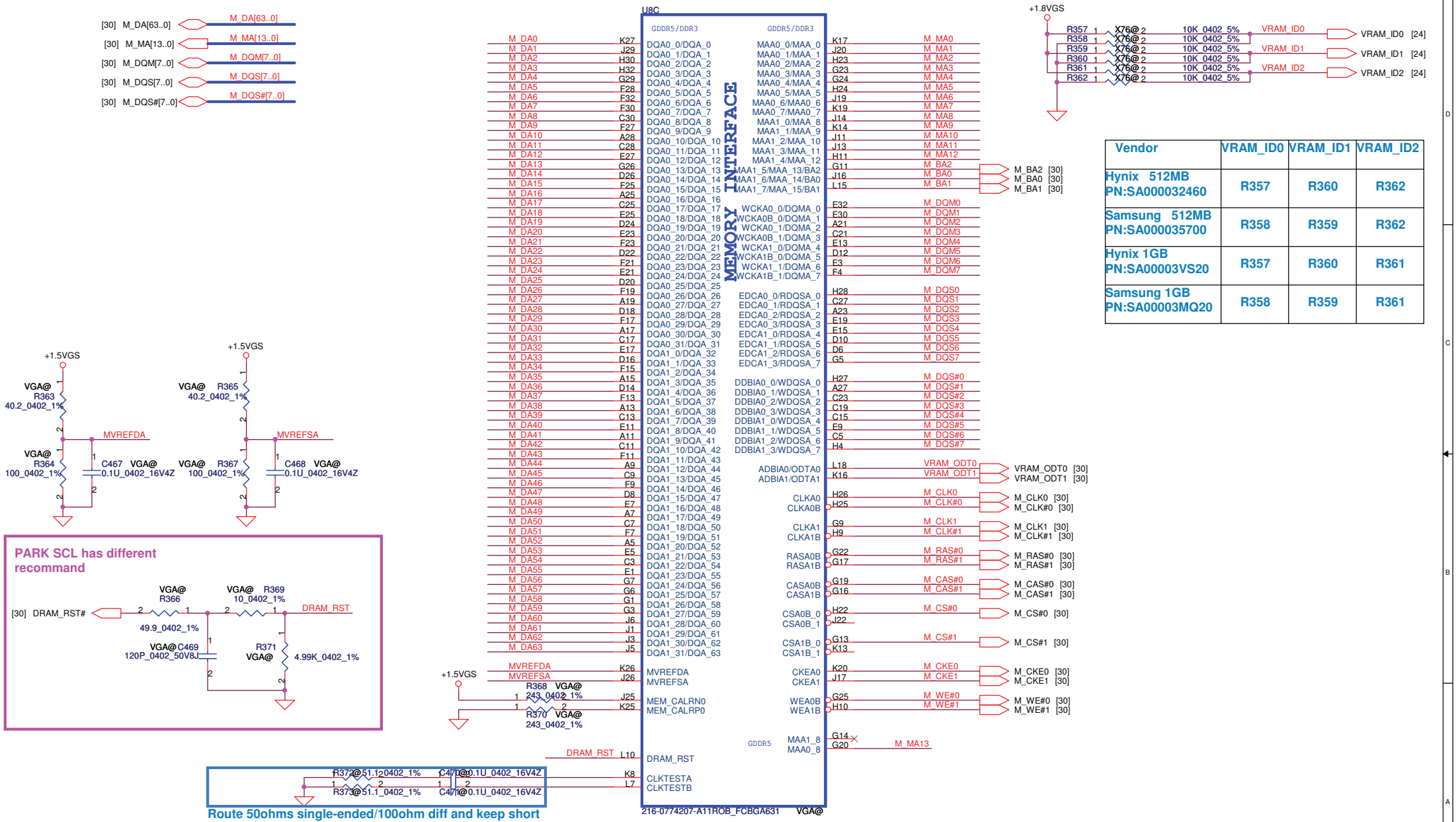

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 512MB PN:SA000032460	R357	R360	R362
Samsung 512MB PN:SA000035700	R358	R359	R362
Hynix 1GB PN:SA00003VS20	R357	R360	R361
Samsung 1GB PN:SA00003MQ20	R358	R359	R361

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: RobsonXT-S3 MEM Interface

Size: B | Document Number | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 29 of 57

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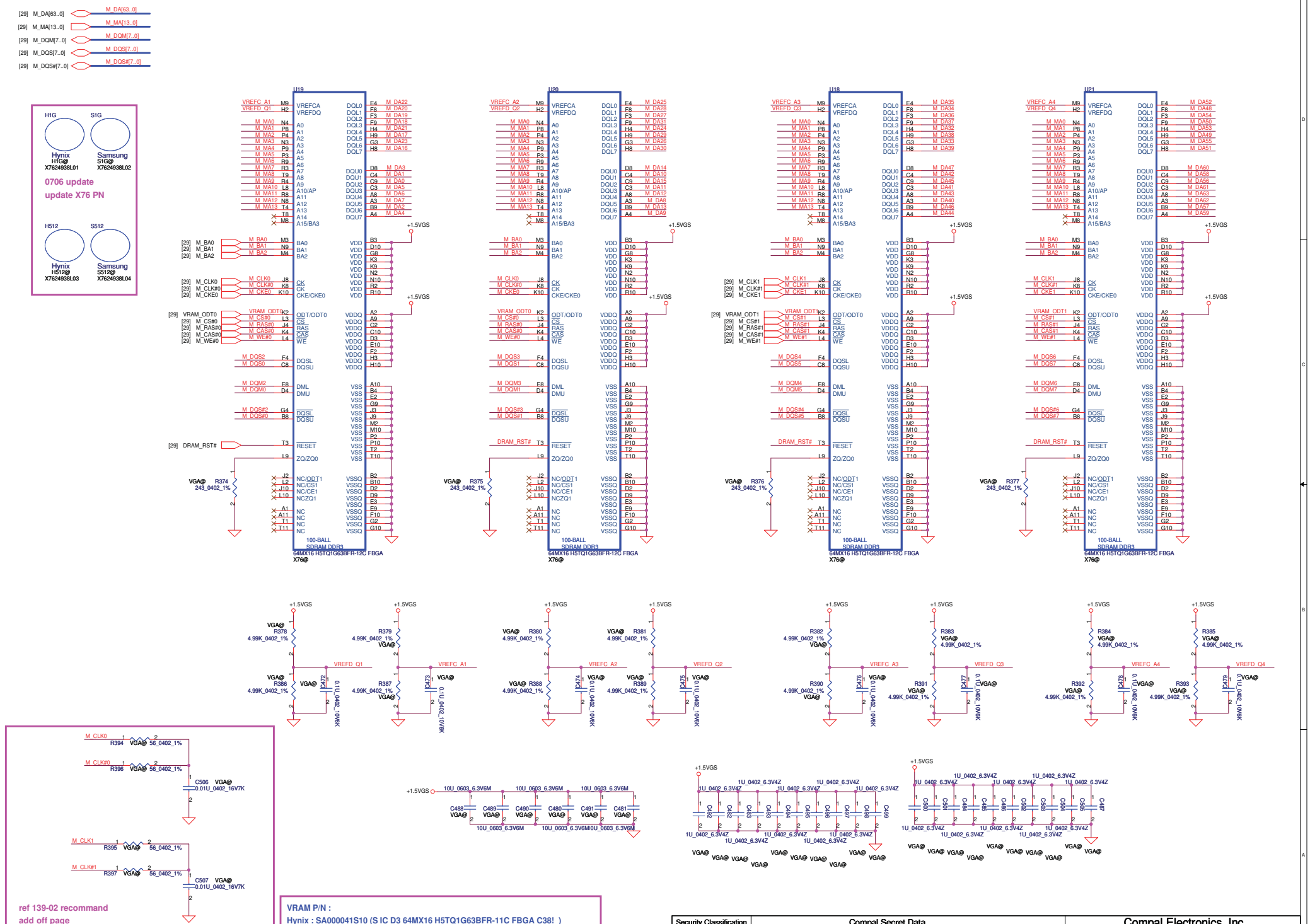

ref 139-02 recommand
add off page
Park SCL recommand pu 60.4 ohm to 1.5VGS
0619 update

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VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: RobsonXT-S3 VRAM

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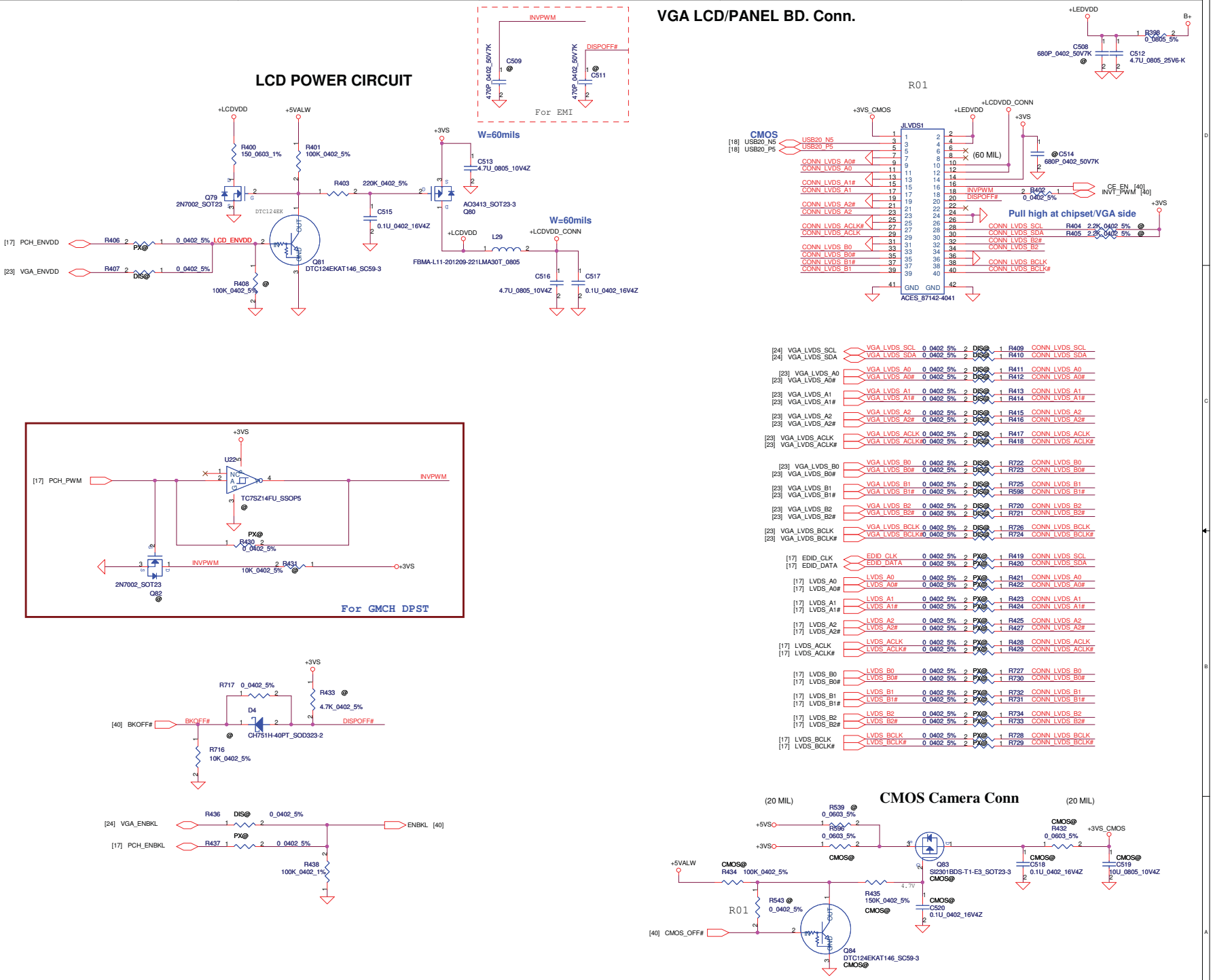
VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: LVDS/CAMERA

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 31 of 57

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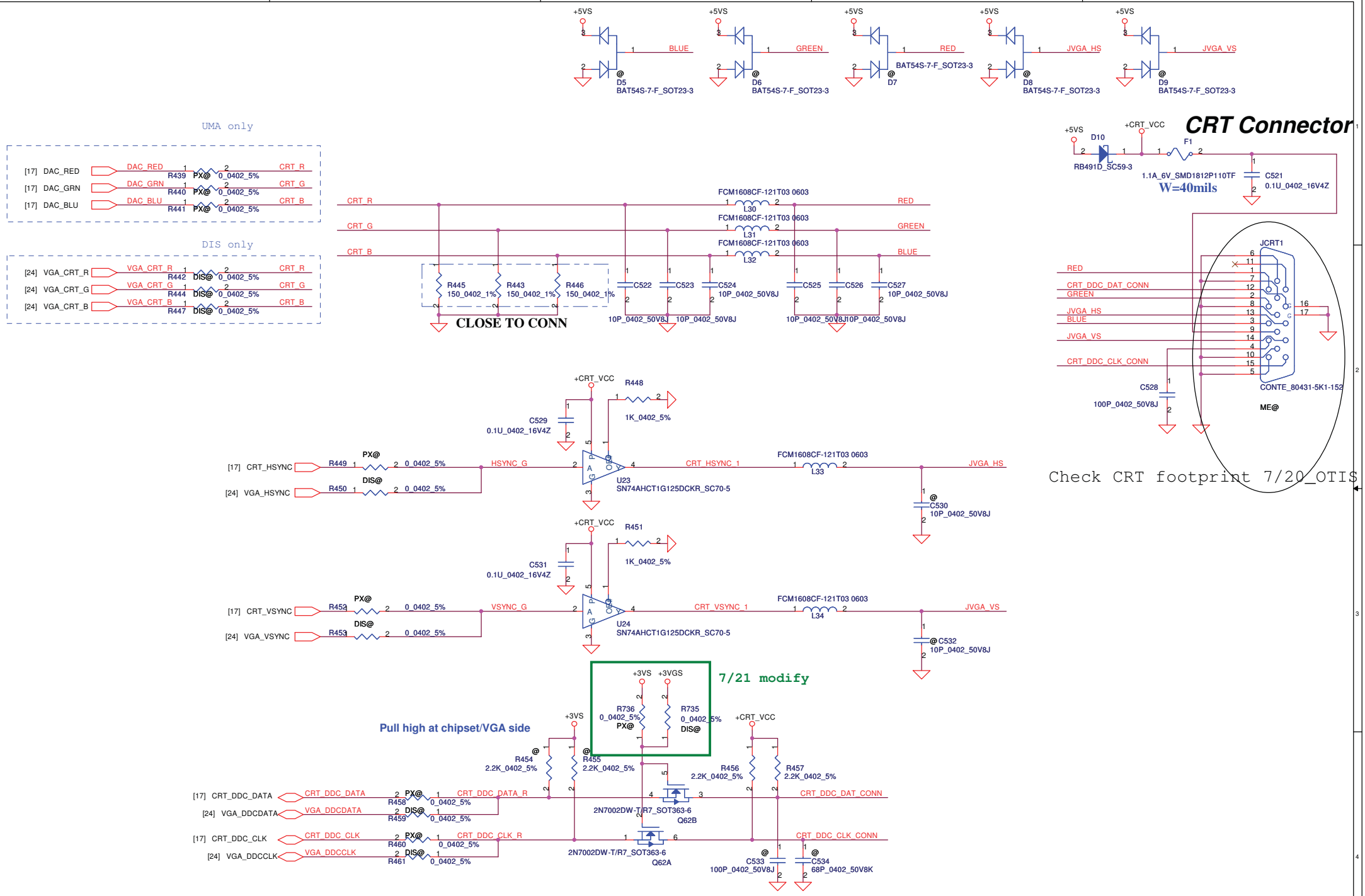

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 32 of 57

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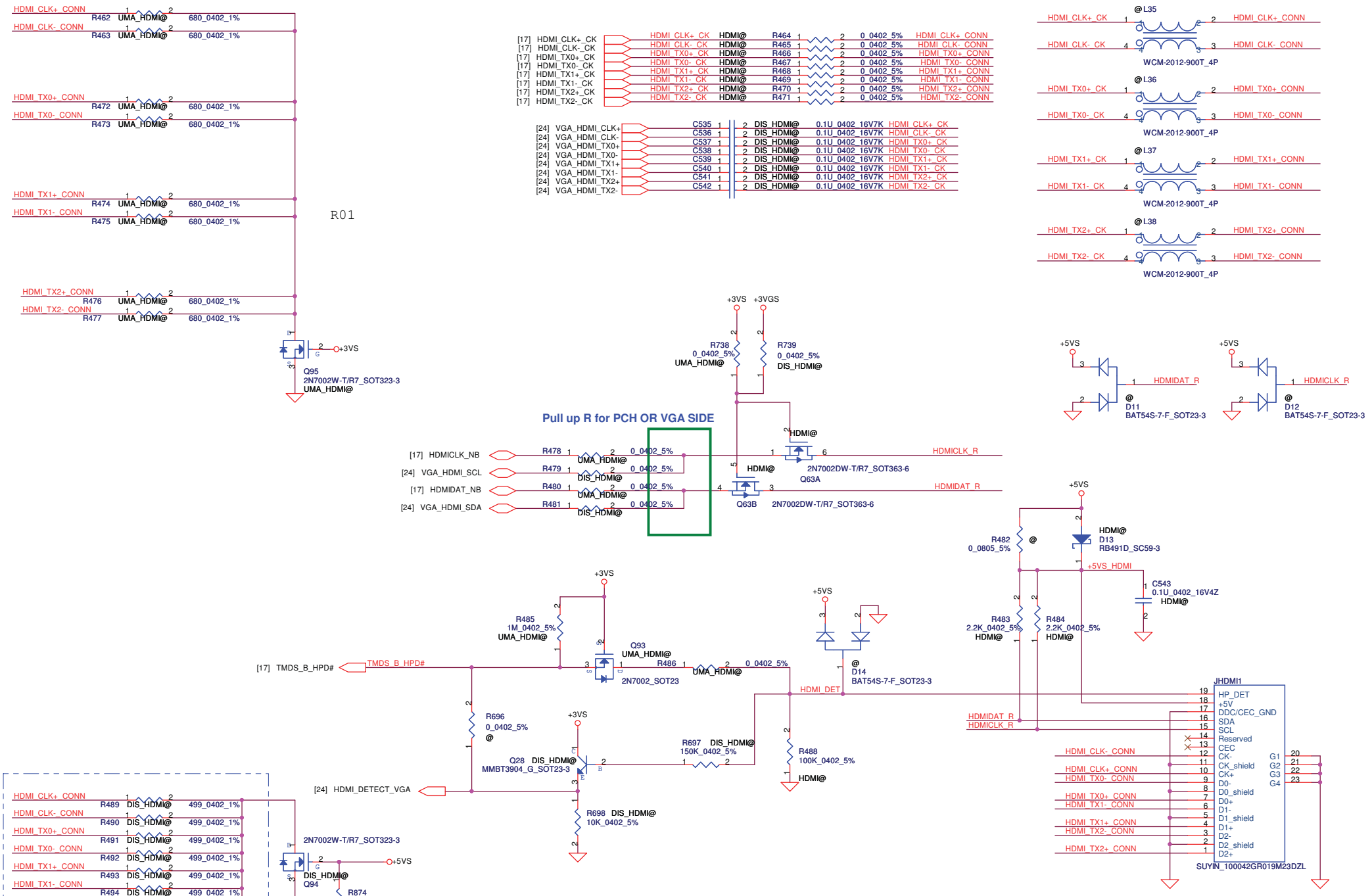

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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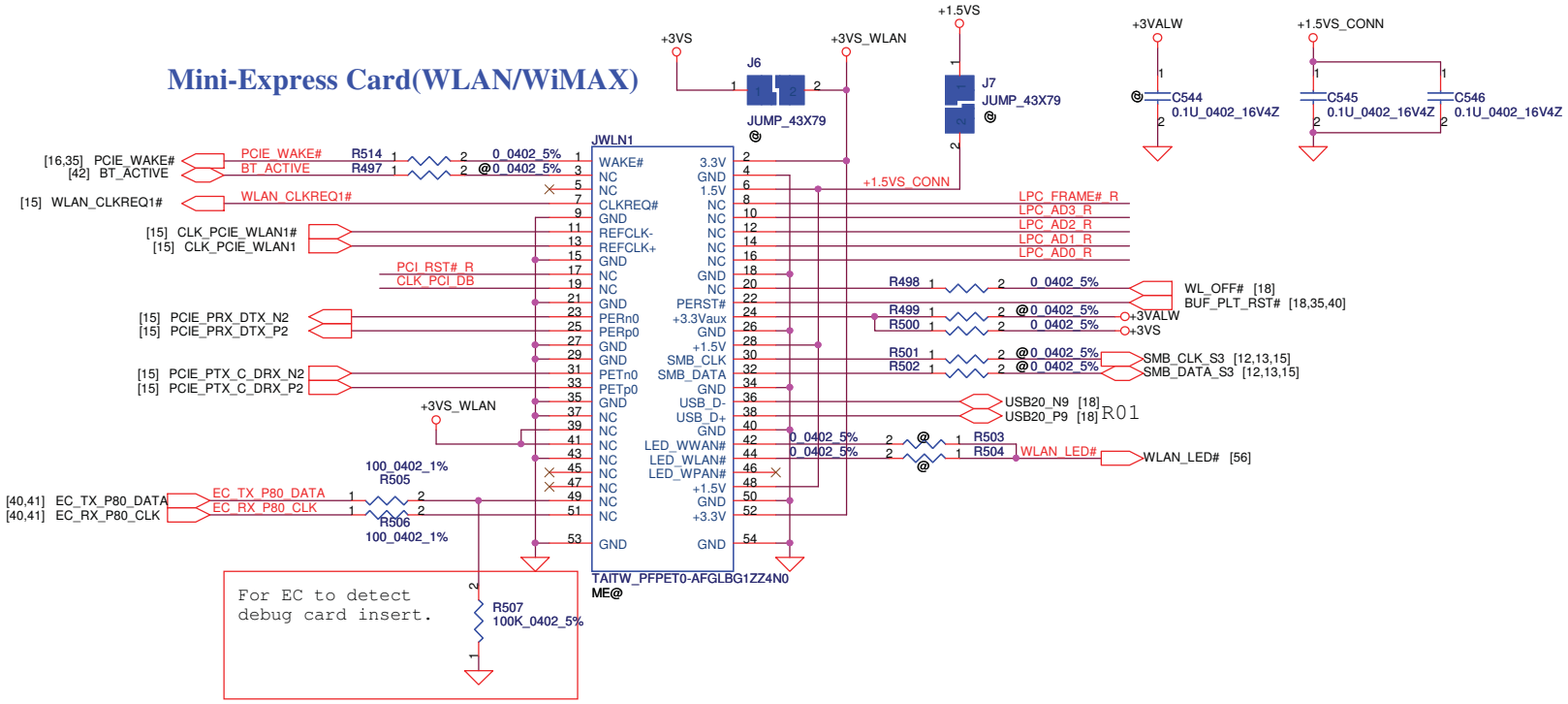
Compal Electronics,Ltd.

Title: **HDMI CONN**

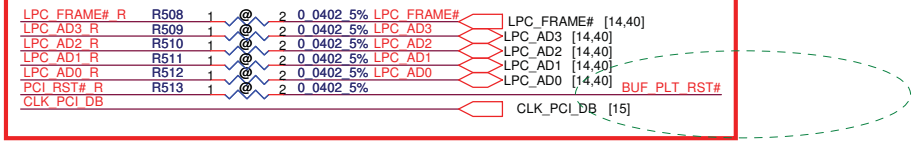
Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 33 of 57

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



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Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

Size | Document Number: **LA-6758P** | Rev 0.1

Date: Tuesday, August 17, 2010 | Sheet 34 of 57

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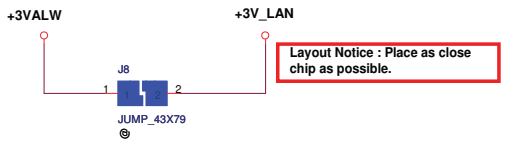
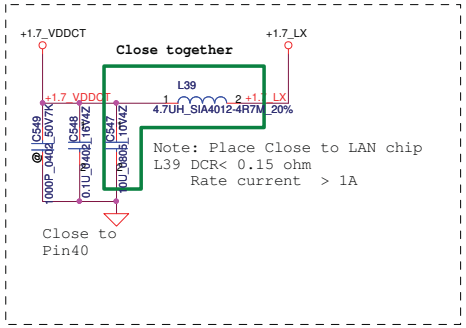
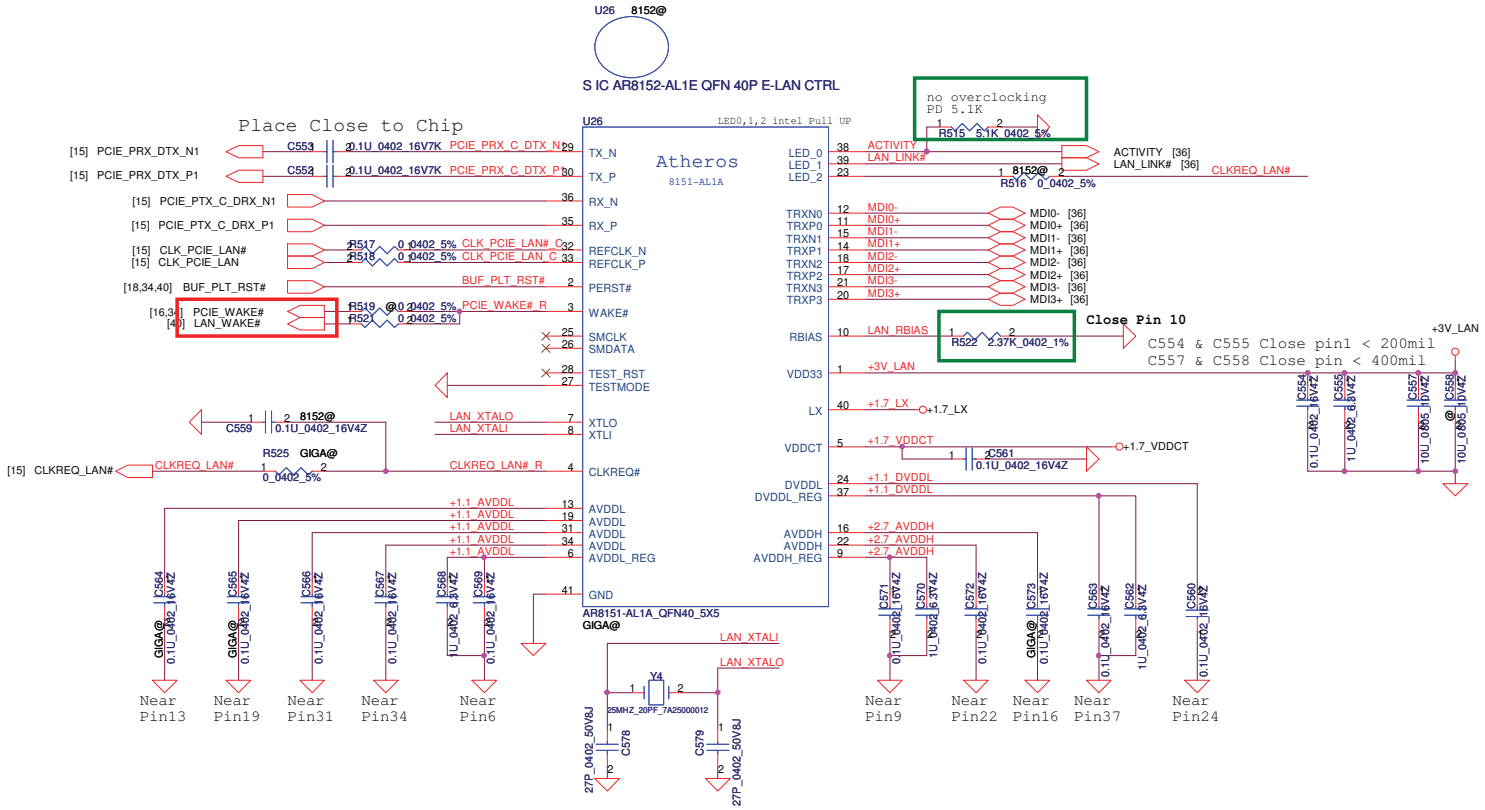


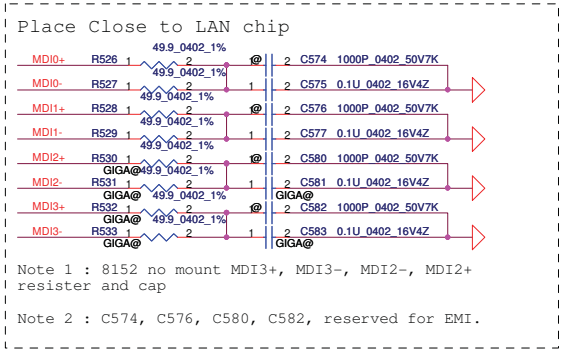
Atheros request can't disable LAN power



Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--





	Pin4	Configure R525	Configure C559		Pin23	Configure R516
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

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Compal Electronics, Inc.

Title: LAN-AR8151/8152

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 35 of 57

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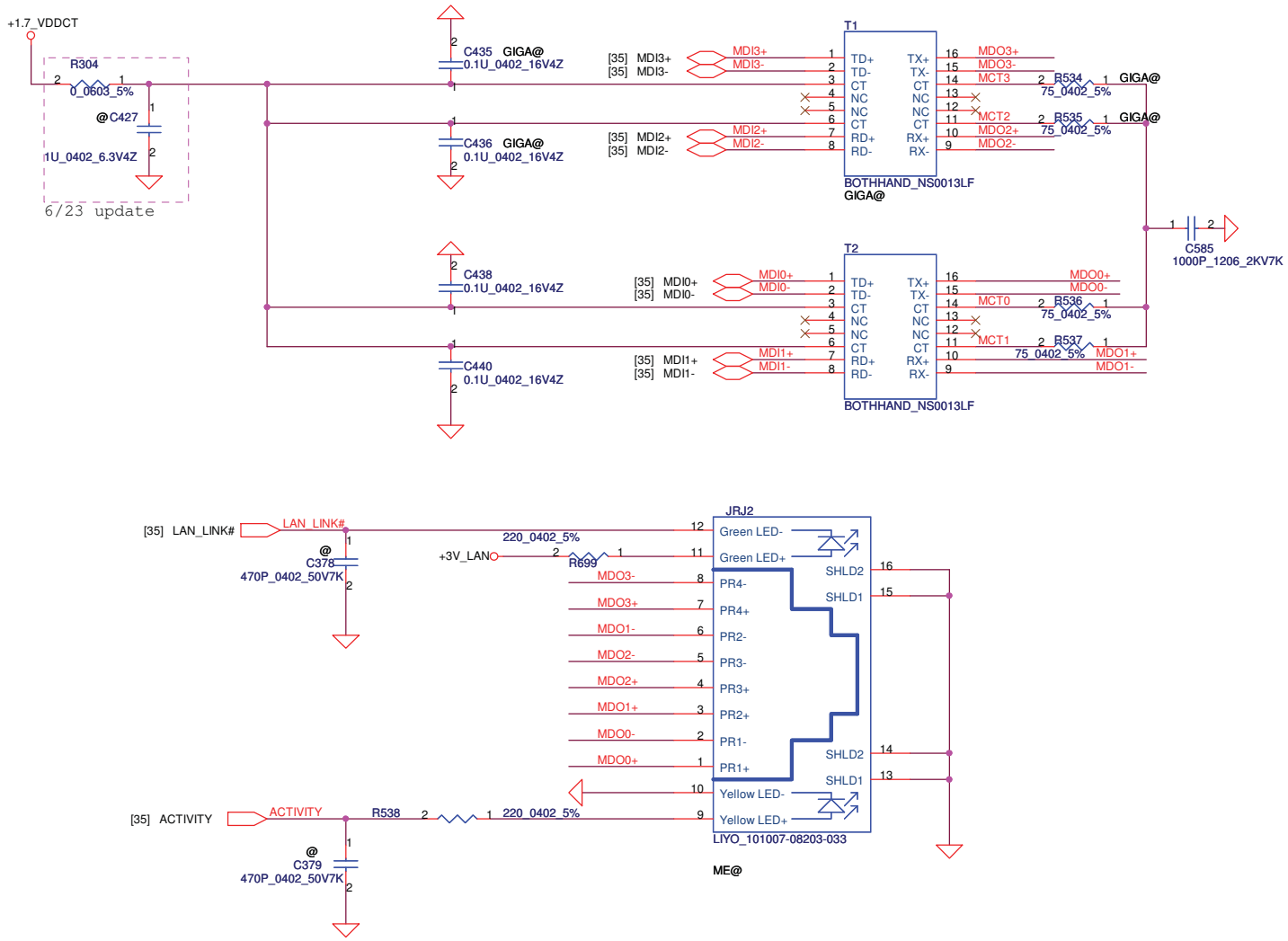

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Compal Electronics, Inc.

Title: **LAN_Transformer**

Size: B | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 36 of 57

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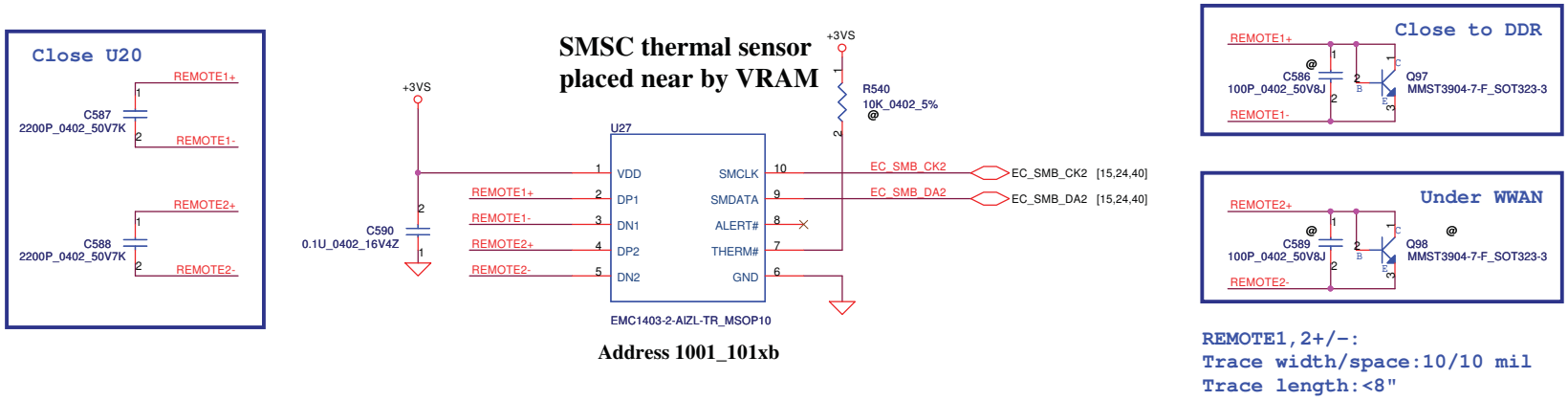
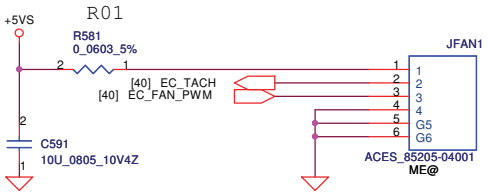


Address 1001_101xb

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



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Compal Electronics,Ltd.

Title: EMC1403_Thermal sensor/FAN

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 37 of 57

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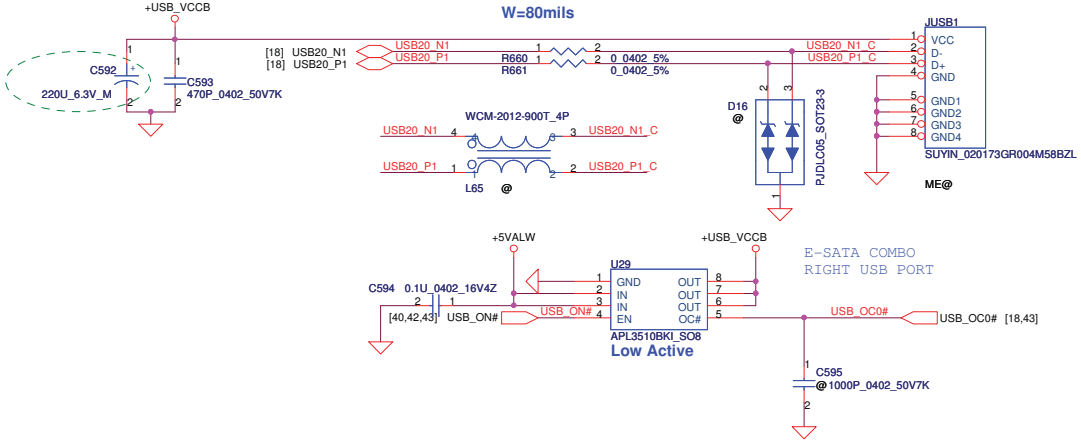
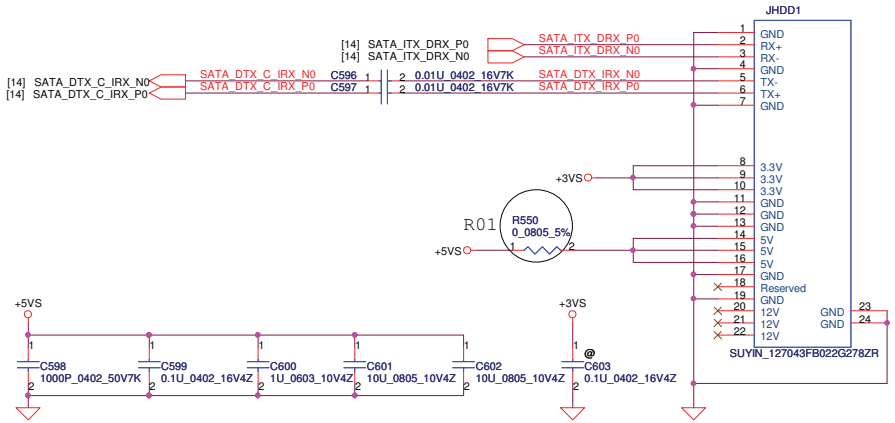
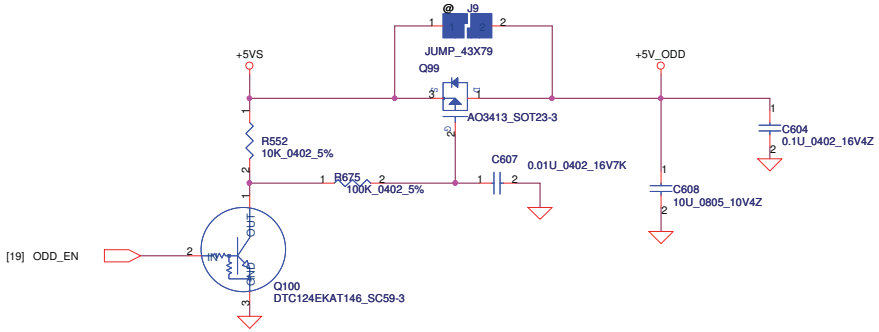
Left USB Conn.



SATA HDD Conn.



ODD Power Control



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Compal Electronics, Inc.

Title: **HDD/ODD Connector**

Size: B | Document Number: **LA-6758P** | Rev: 0.1

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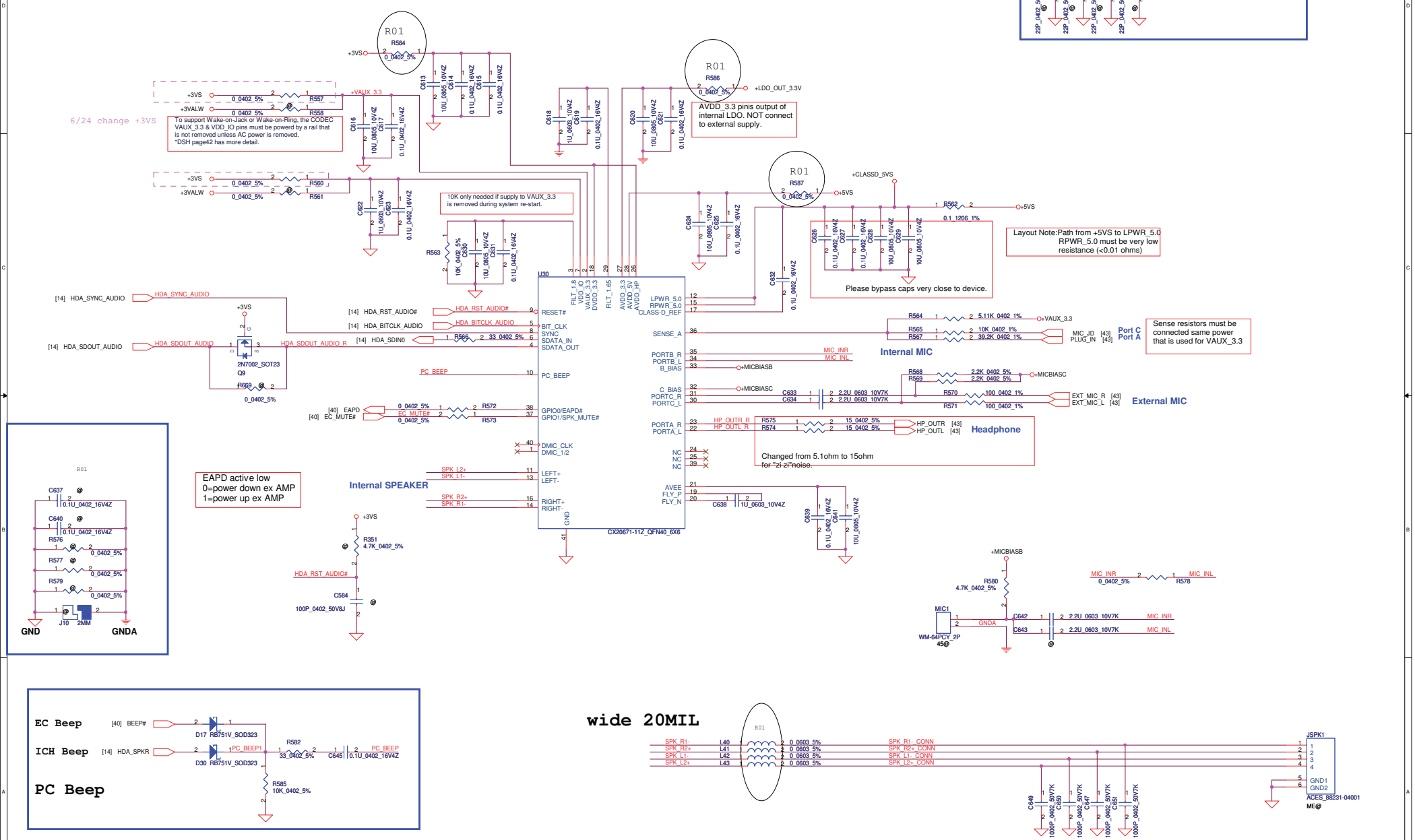
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data			Compal Electronics,Ltd.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: CX20671 Codec
				Size: C; Document Number: LA-6758P; Rev: 0.1
				Date: Tuesday, August 17, 2010; Sheet 39 of 57

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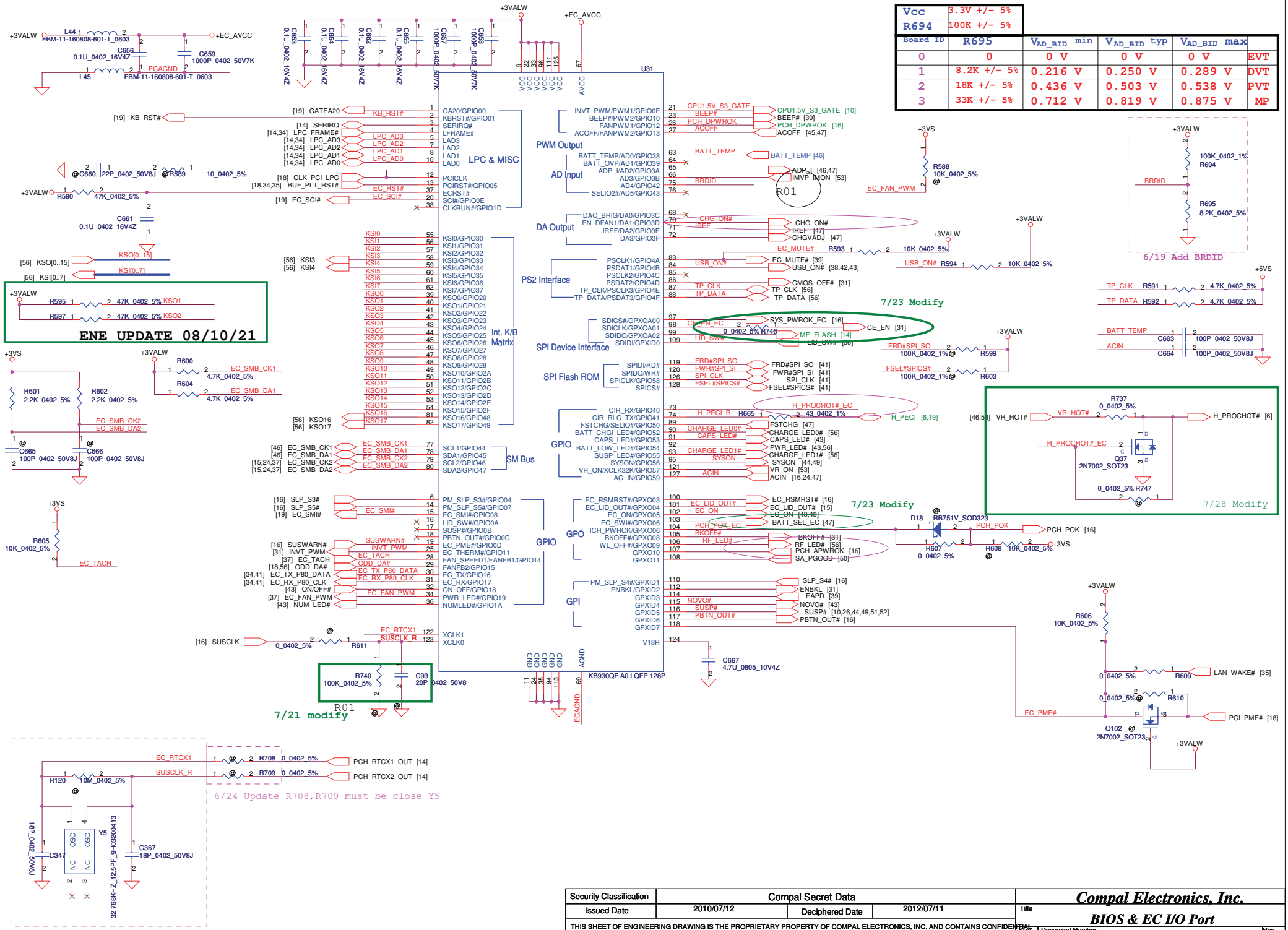
Vcc	3.3V +/- 5%
R694	100K +/- 5%

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP



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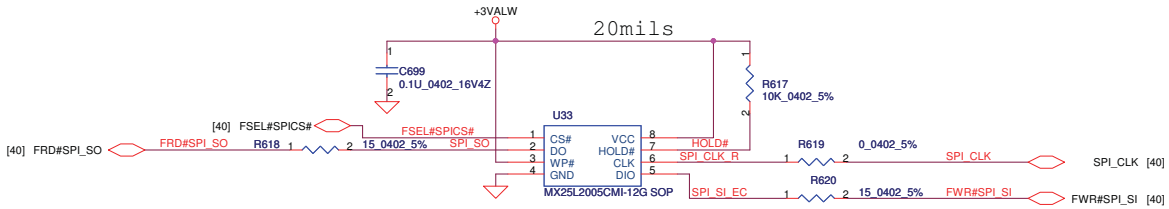
Compal Electronics, Inc.

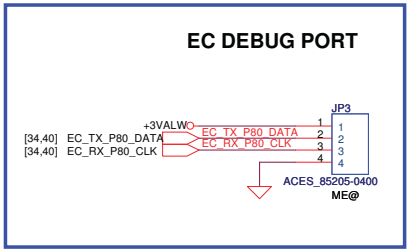
Title: **BIOS & EC I/O Port**

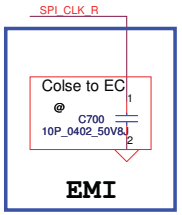
Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

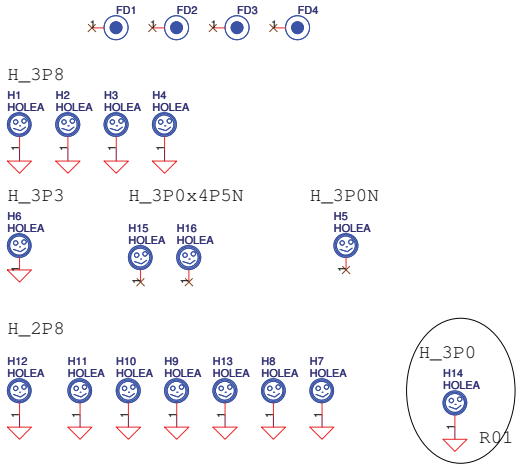
Date: Tuesday, August 17, 2010 | Sheet 40 of 57

FOR EC 256KB SPI ROM
(150mil PACKAGE)









Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: LED/EC SPI ROM
				Size: B; Document Number: LA-6758P; Rev: 0.1
				Date: Tuesday, August 17, 2010; Sheet 41 of 57

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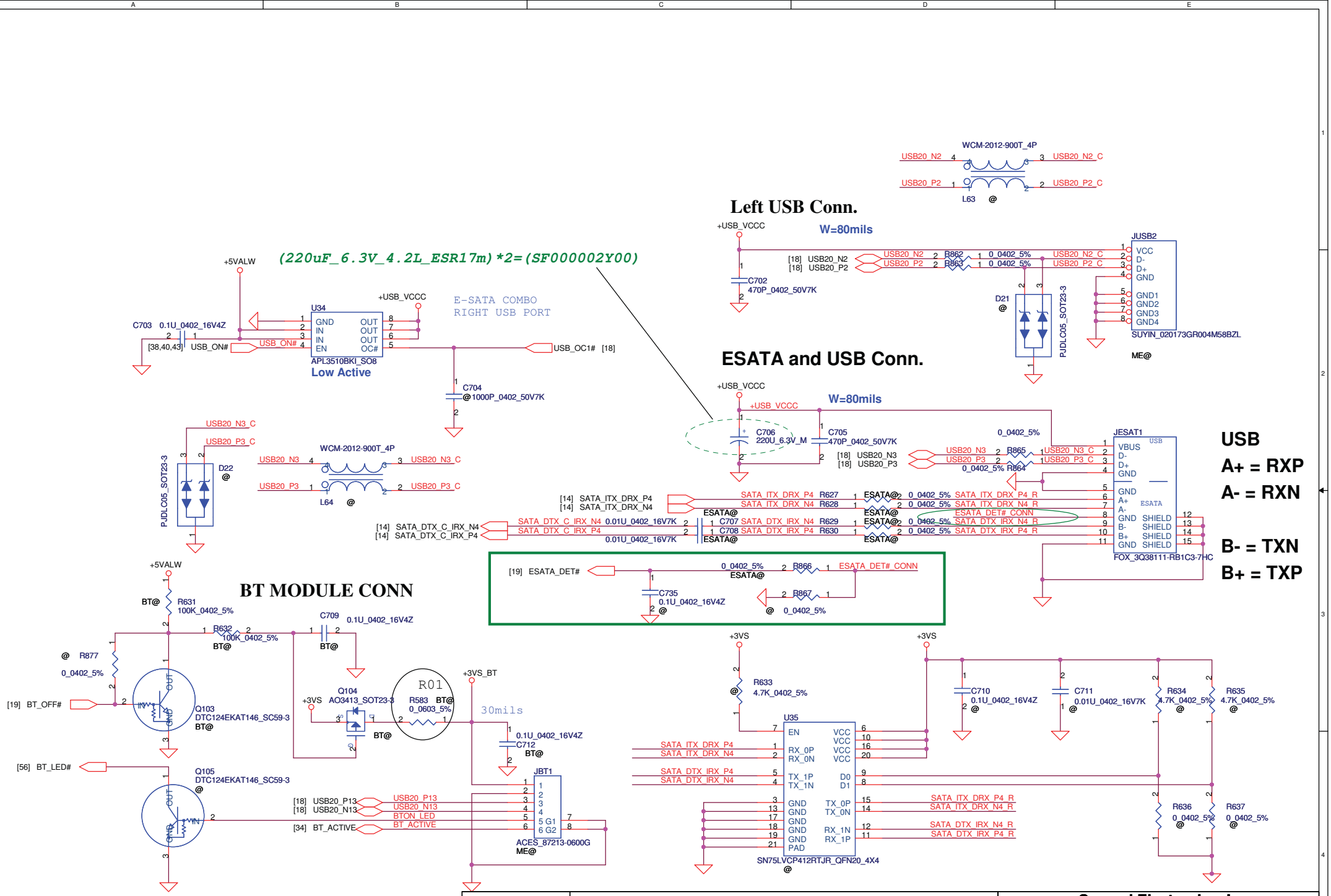

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 42 of 57

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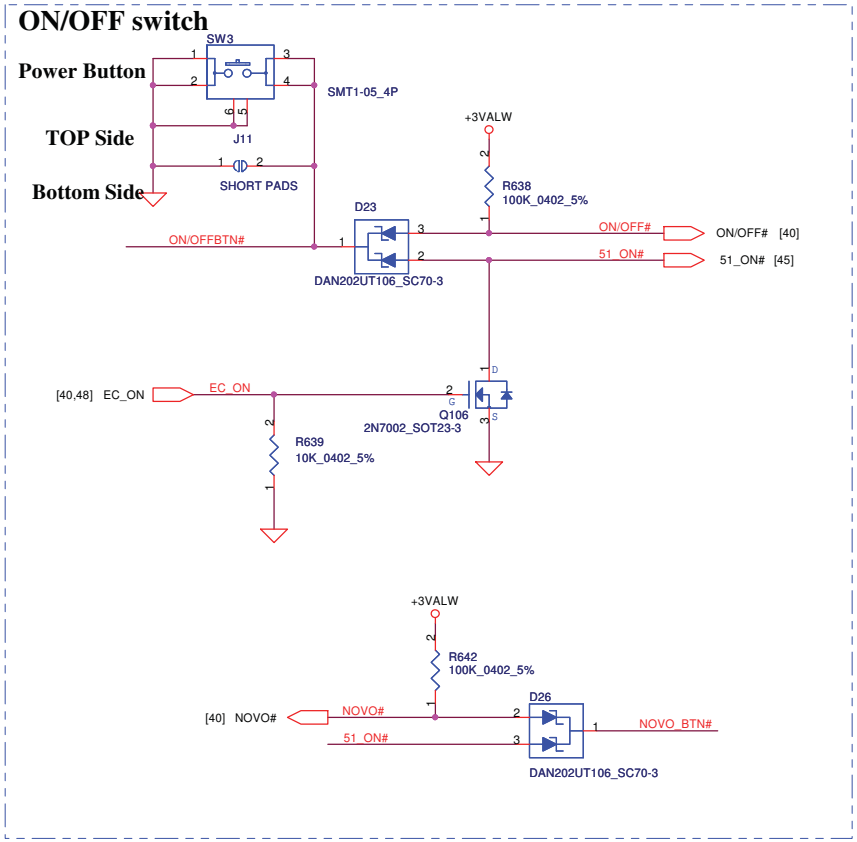
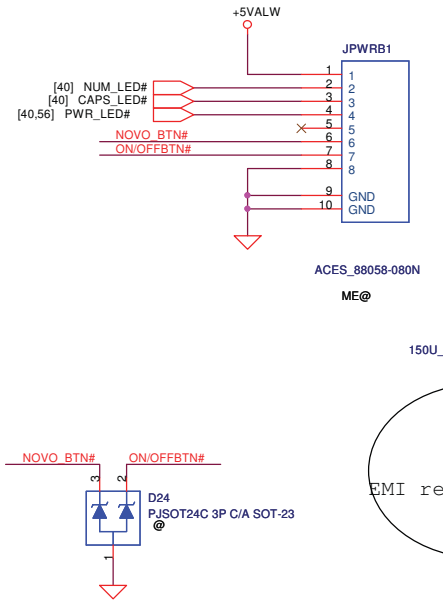
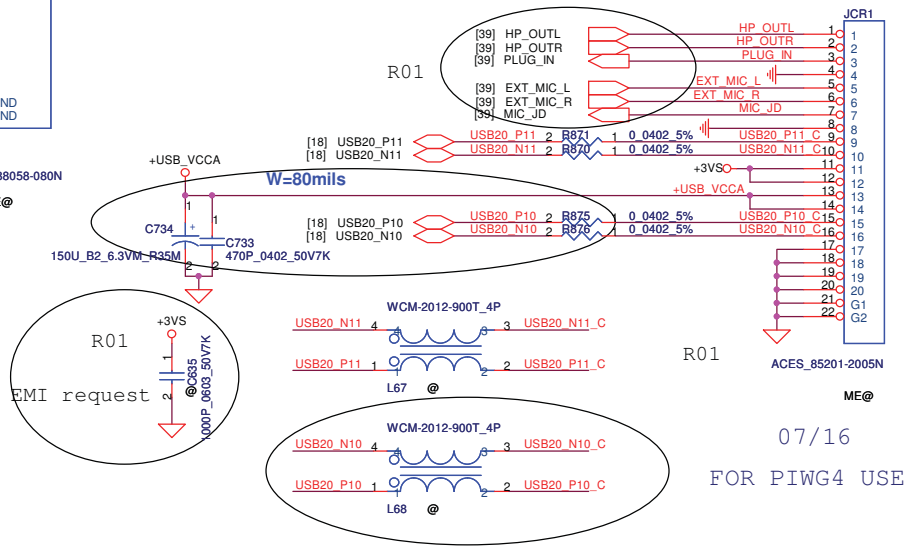
ON/OFF switch



Power Bottom Board Conn. 8pin



Card Reader/Audio Jack SB CONN

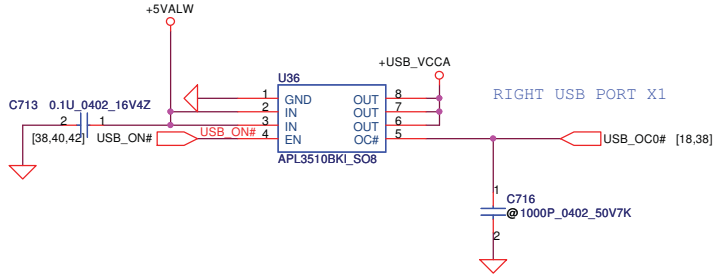


07/16

FOR PIWG4 USE

EMI REQUEST 1ST = SCA00000E00

2ST = SCA00000R00

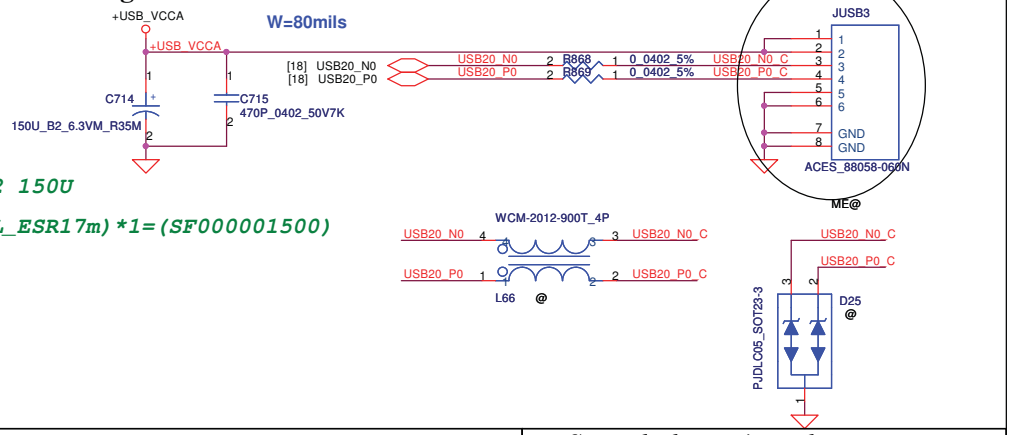


07/16

FOR PIWG4 USE

R01

Right USB Conn.



6/9 change to B2 150U

*(220uF_6.3V_5.8L_ESR17m)*1=(SF000001500)*

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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Compal Electronics,Ltd.

Title: **other IO connector**

Size: Custom | Document Number: **LA-6758P** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 43 of 57

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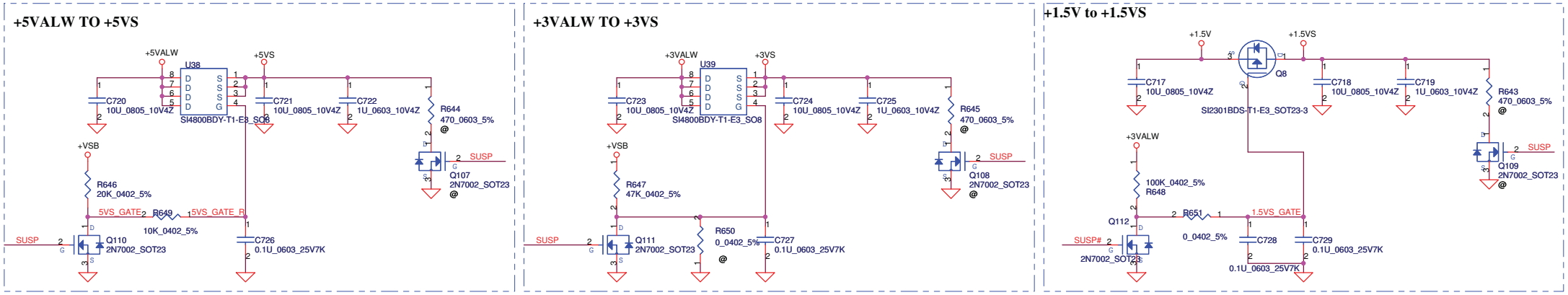
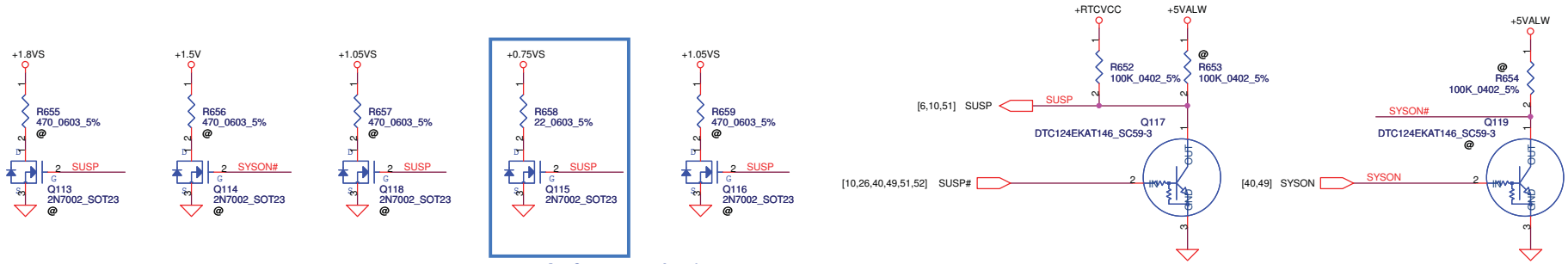


6/13 change SI4800 to SI2301



For Intel S3 Power Reduction.

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-6758P | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 44 of 57

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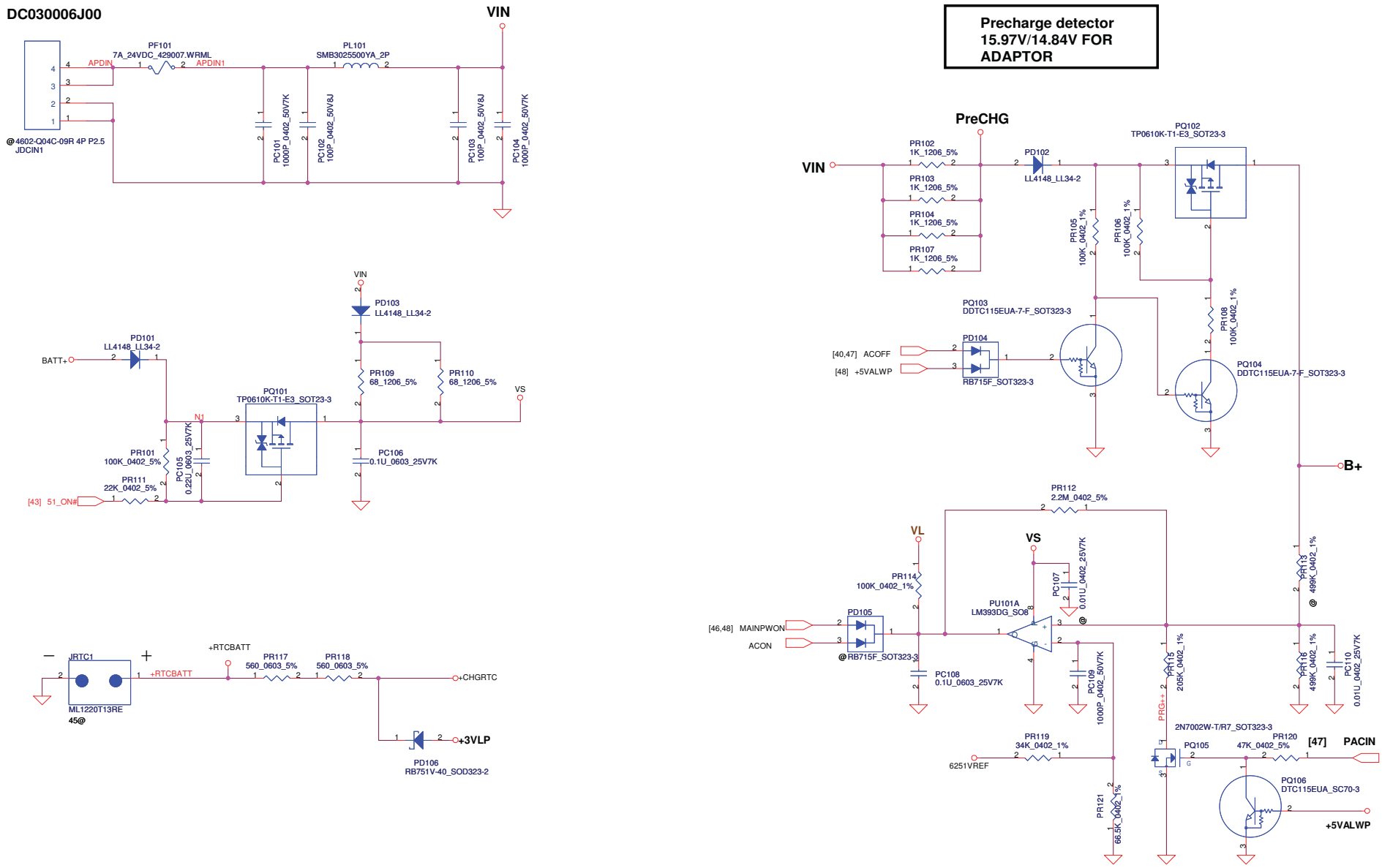

ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 45 of 57

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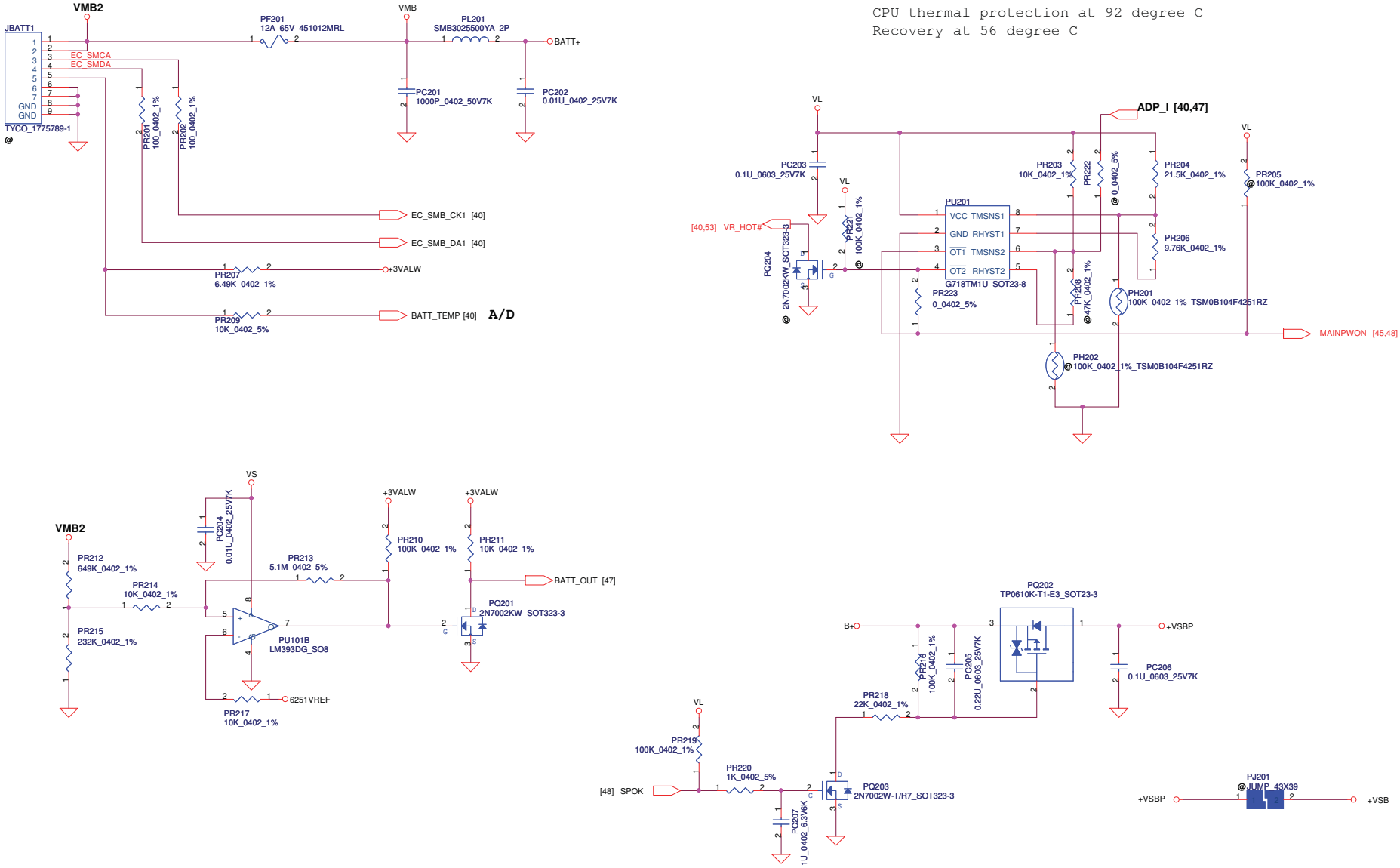
PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size: Custom | Document Number: **PIWG4** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 46 of 57

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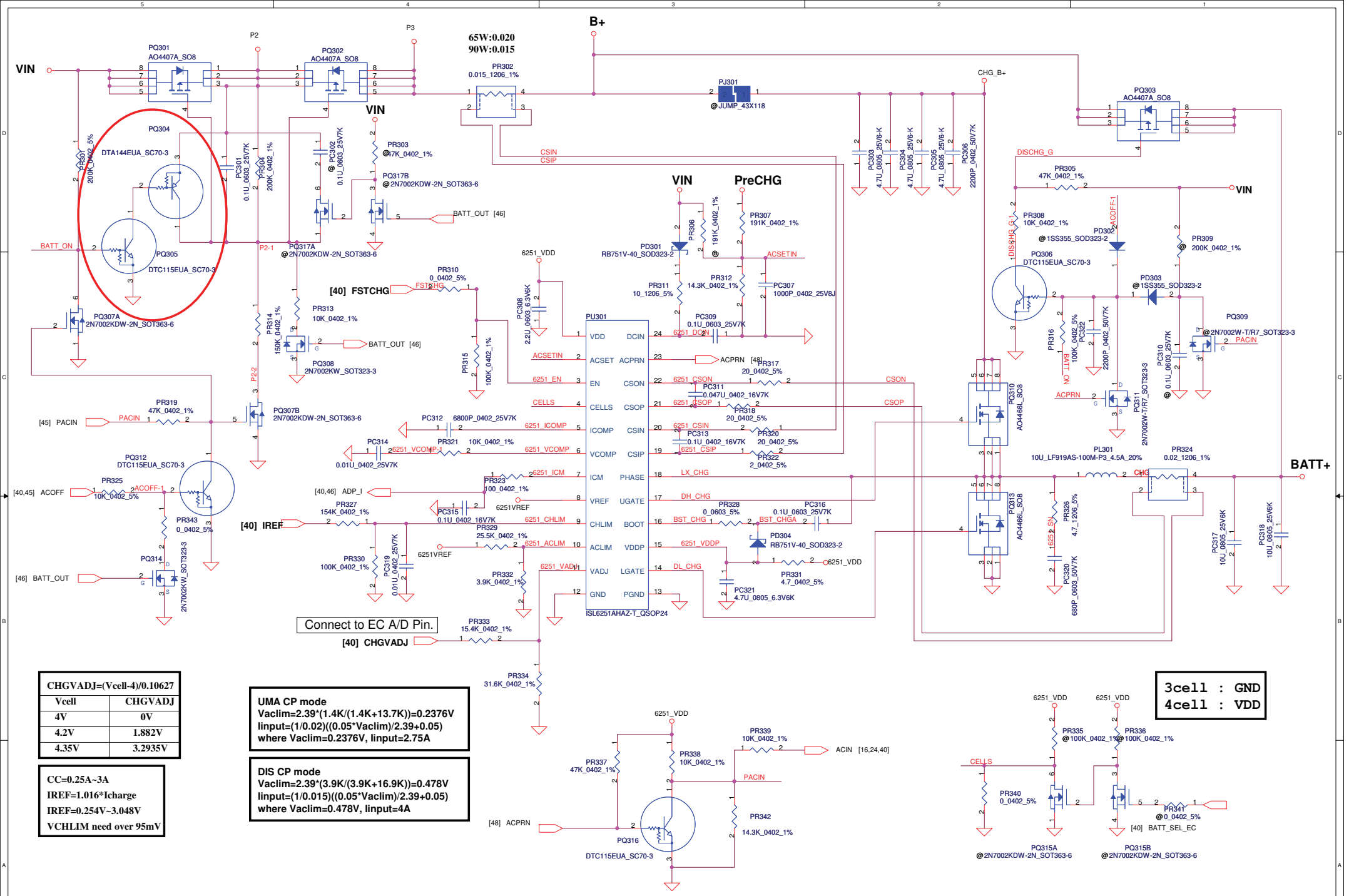

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

UMA CP mode
Vaclim=2.39*(1.4K/(1.4K+13.7K))=0.2376V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2376V, Iinput=2.75A

DIS CP mode
Vaclim=2.39*(3.9K/(3.9K+16.9K))=0.478V
Iinput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.478V, Iinput=4A

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

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Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: PIWG4 | Rev: 0.1

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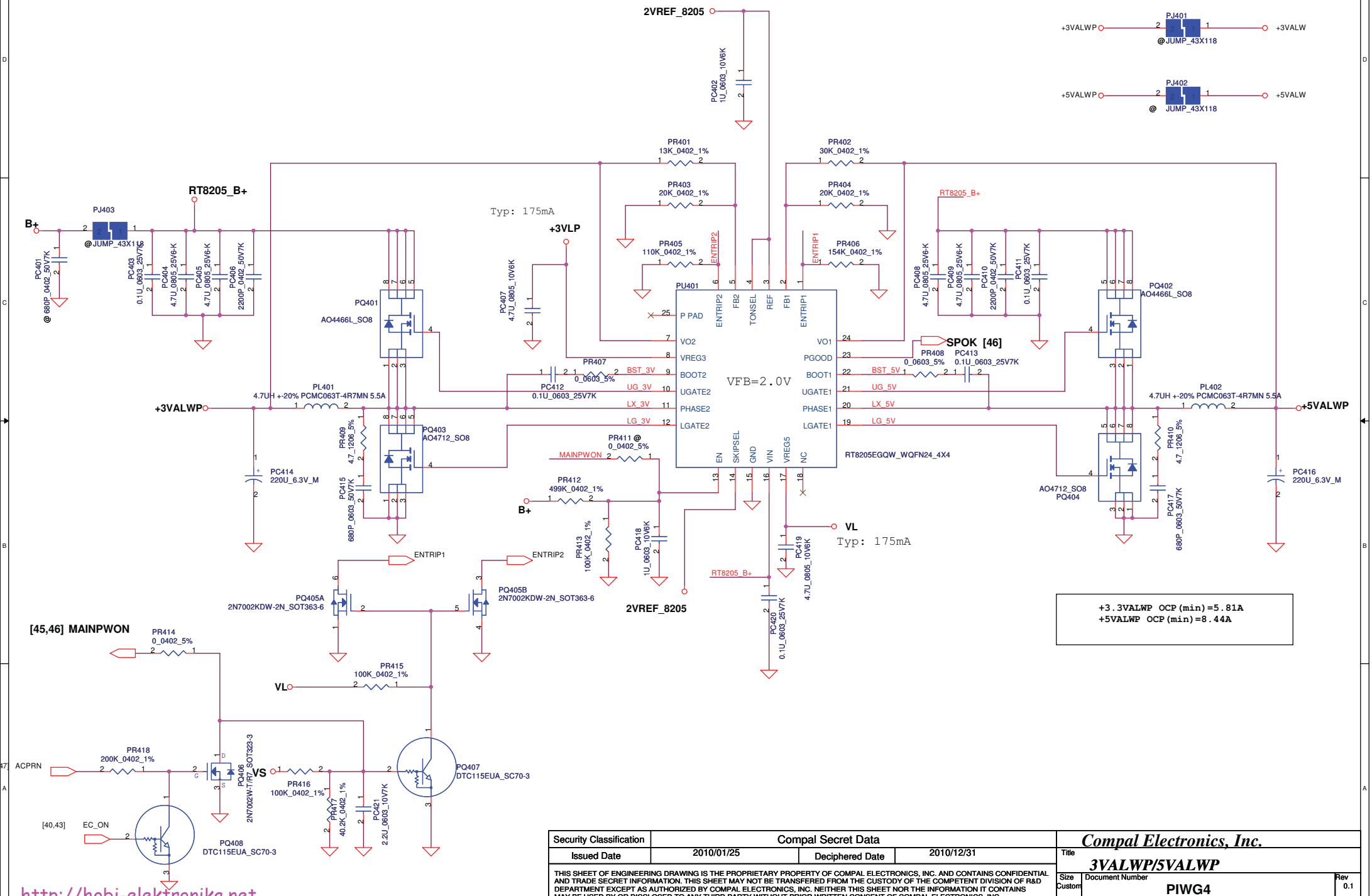
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 48 of 57

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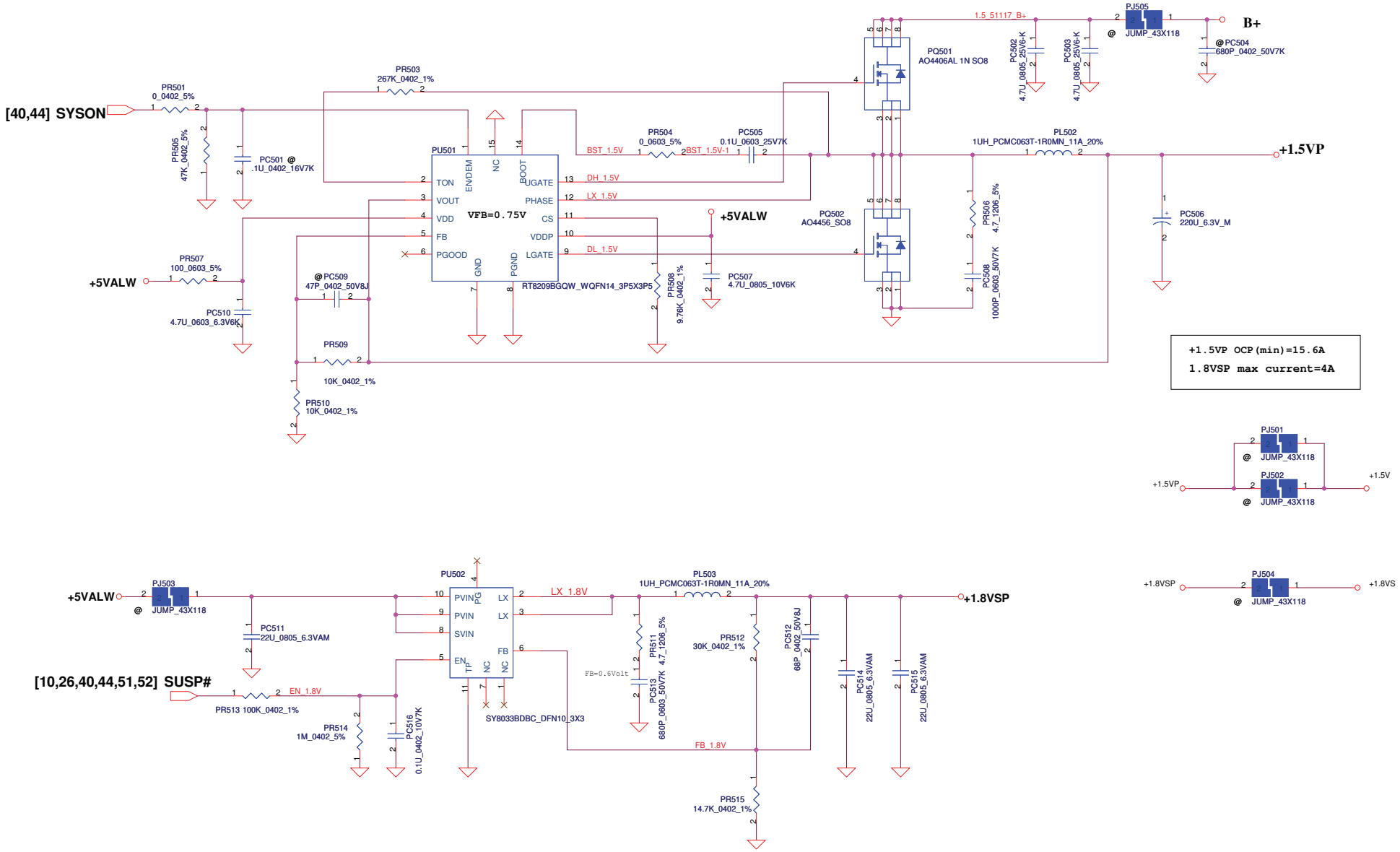

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

Size: Custom | Document Number: **PIWG4** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 49 of 57

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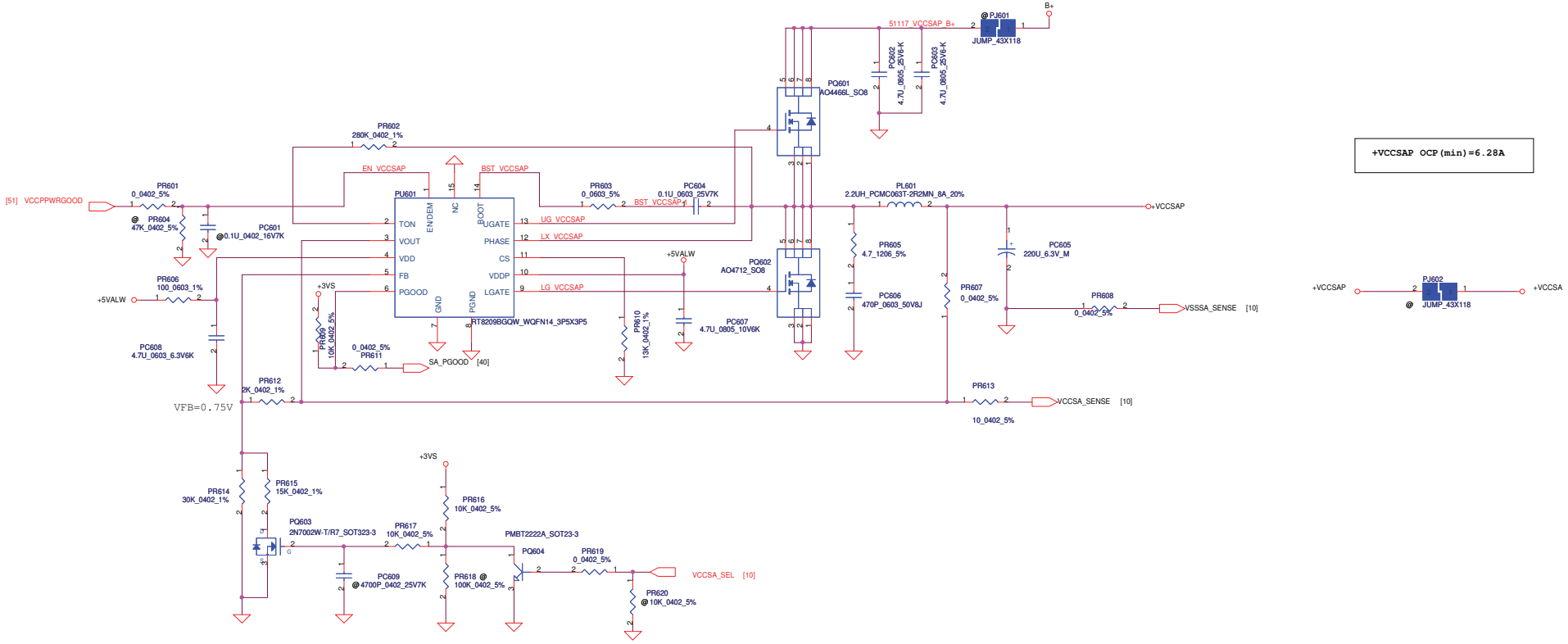

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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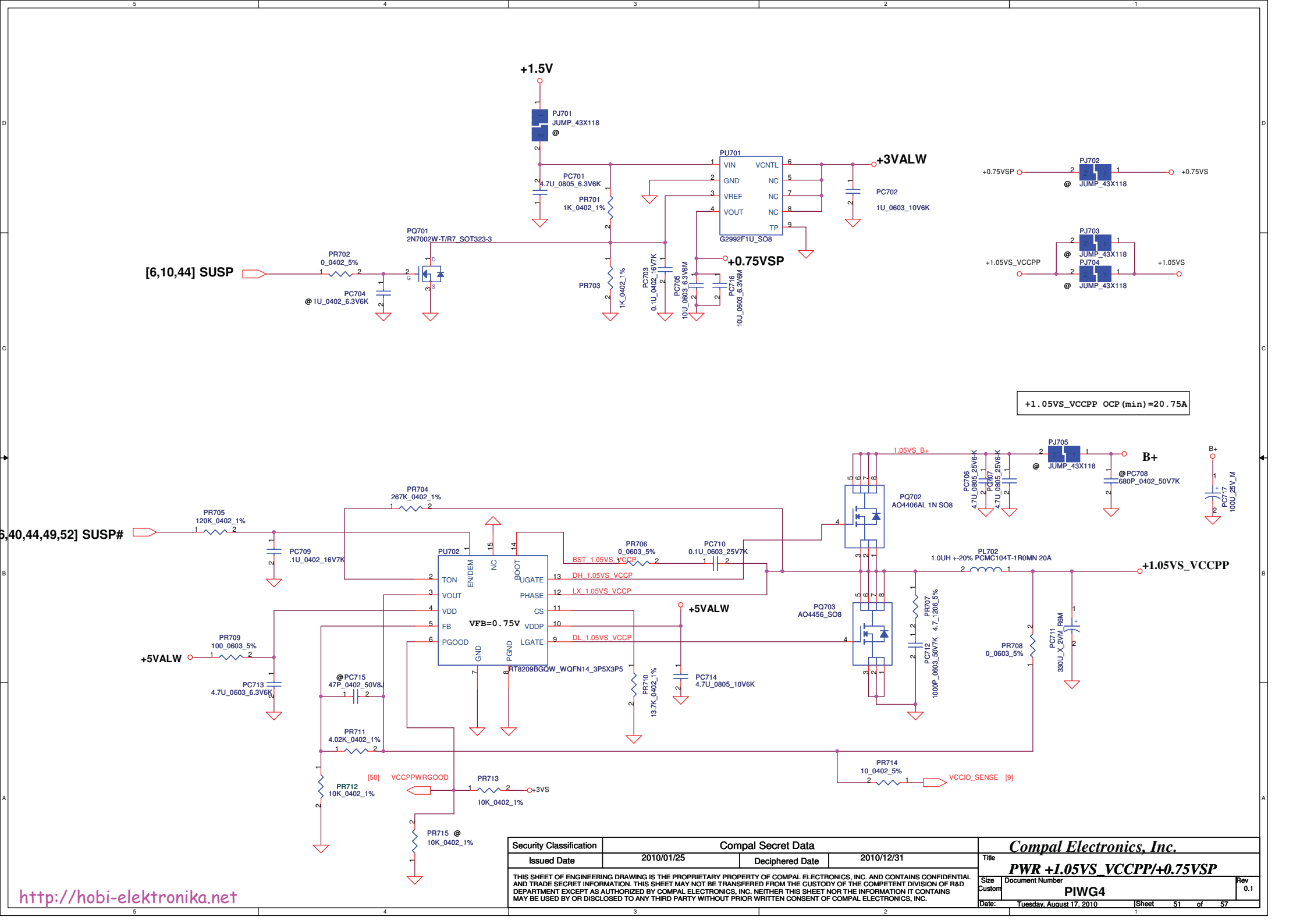
Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 50 of 57



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Compal Electronics, Inc.

Title: **PWR +1.05VS_VCCPP/+0.75VSP**

Size: Custom | Document Number: **PIWG4** | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 51 of 57

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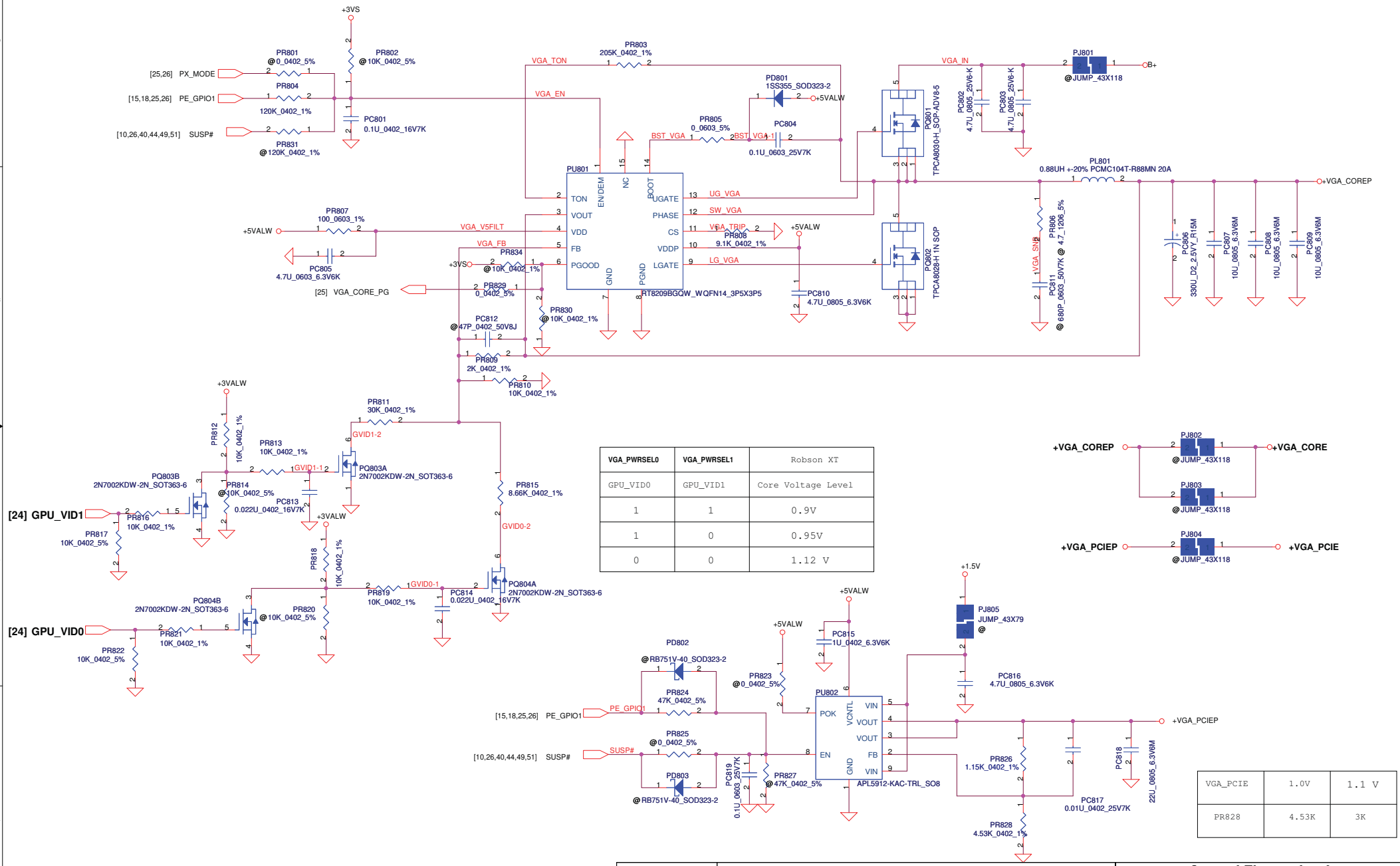

VGA_PWRSEL0	VGA_PWRSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V

VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: VGA_CORE/PCIE

Size | Document Number: PIWG4 | Rev: 0.1

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Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

```
+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V      *10
(2)22U_0805_6.3V   *15
(3)470U_D2_2V       *4(ESR=4.5m ohm)

*OCP setting value=71A
```

```
+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V   *12
(2)470U_D2_2V       *2(ESR=4.5m ohm)

*OCP setting value=37A
```

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Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: PIWG4 | Rev: 0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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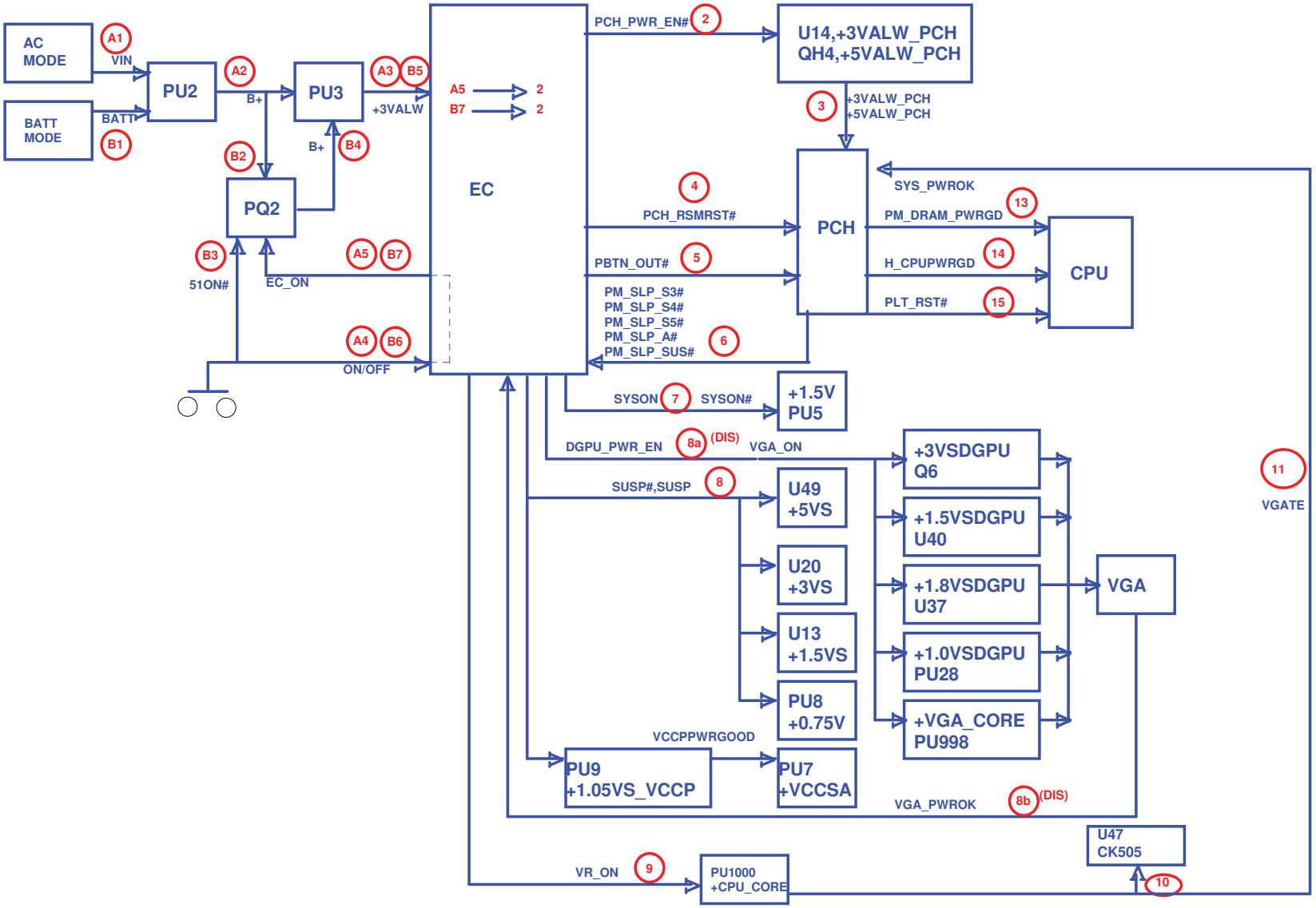
Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PIWG4 | Rev: 0.1

Date: Tuesday, August 17, 2010 | Sheet 54 of 57



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				Date: Tuesday, August 17, 2010 / Sheet 55 of 57

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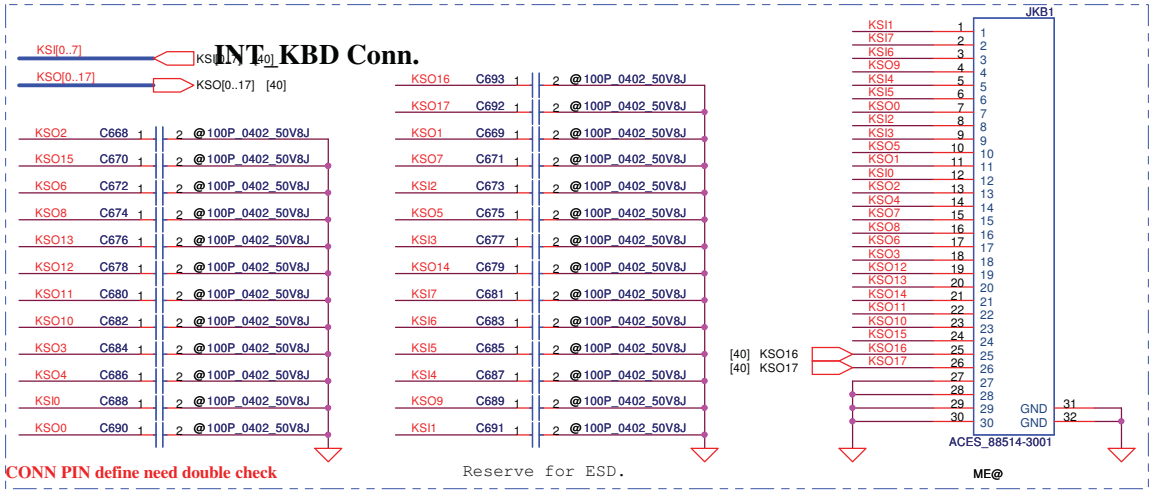
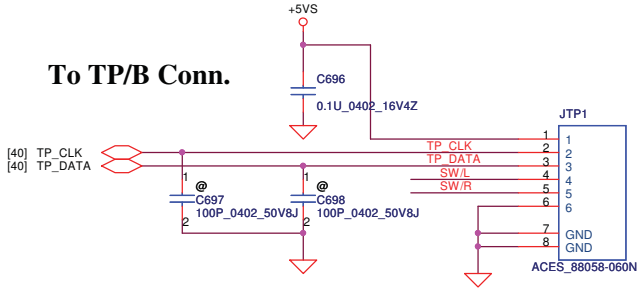
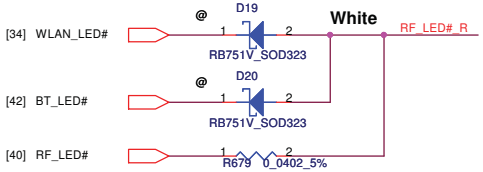
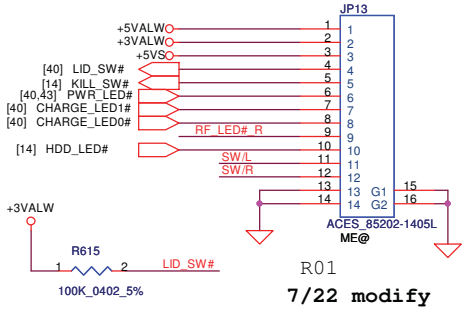
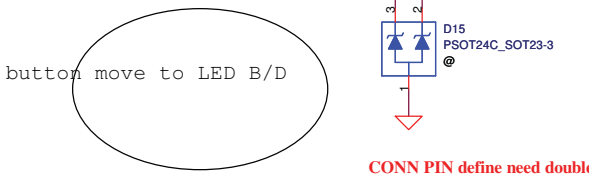
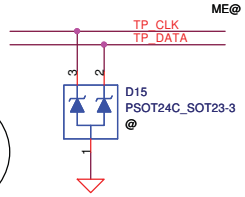






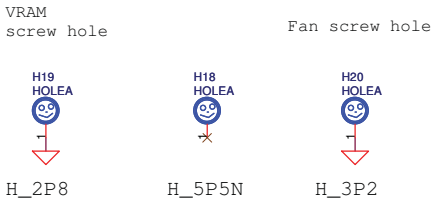


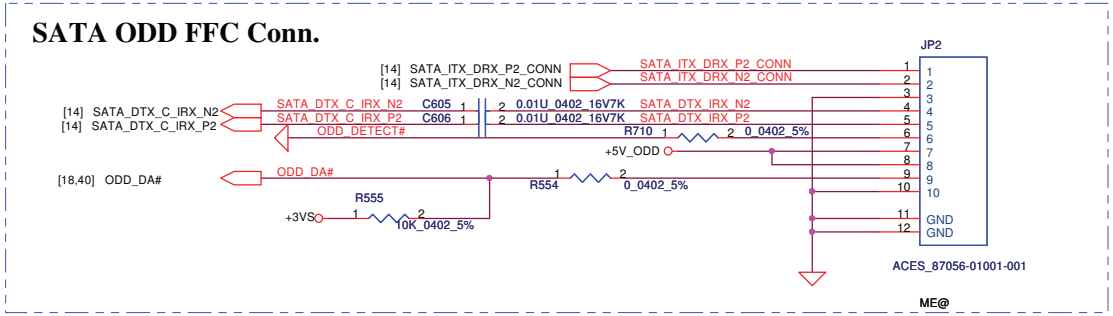




CONN PIN define need double check

For 17" M/B to LED/B





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PHASE	PAGE	Modification list	PURPOSE
0.2	P31	Change CRT Symbol	For CRT footprint issue
0.2	P31	Del C510	For Non-used part
0.2	P39	change C610 pin 1 net name	change C610 pin 1 net name to correct
0.2	P35	U25 change to U26	For co-lay 10/100 and GIGA
0.2	P32	Add R735,R736	For DIS only SMBus pull high
0.2	P33	Add R738,R739	For DIS only SMBus pull high
0.2	P33	Change Q63 BOM structure to HDMI@	For DIS HDMI function
0.2	P40	Add R740, C93	For EC request
0.2	P18	Change R215 pin1 net name	Change R215 pin1 net name to correct
0.2	P18	Add R741	Add R741 for Reserved PE_GPIO0
0.2	P16	Add R742, R743	For PCH power sequence
0.2	P38	Del U28, R542~R551 , J12	Del USB charger circuit
0.2	P40	Add EC pin 97,98,103	Add EC pin 97 for SYS_PWROK_EC , pin 98 for CE_EN , pin 103 for BATT_SEL_EC
0.2	P24	Change R662 pin 2 net name	Change R662 pin 2 net name to correct
0.2	P28	Del C421,C422,C431,C432,C433, L27, Add R745, U8 pin N11,N12 change to NC	For AMD new document suggestion
0.2	P26	Add R744	Add R744 for control PE_GPIO1 from SUSP#
0.2	P39	Change J10 footprint and Add J13	Change J10 footprint by DFx request and Add J13 by vendor suggestion
0.2	P39	Change PC_Beep circuit	Change PC_Beep circuit
0.2	P6	Add R161, R182, R192 BOM structure hange to @	Follow ORB circuit
0.2	P58/59	Add R615 in 15" and 17" page	Pull high LID_SW# at M/B side
0.2	P31	Add Q83 pin 1 power net name +CMOS_PW	For power trace net
0.2	P56/57/58	Change JP21 to JKB1	Change connector to standard name
0.2	P56/57/58	Change JP4 to JTP1	Change connector to standard name
0.2	P43/60	Change JP6 to JPWRB1	Change connector to standard name
0.2	P34	Change JP1 to JWLN1	Change connector to standard name
0.2	P42	Change JP5 to JBT1	Change connector to standard name
0.2	P43/60	Change JP7 to JCR1	Change connector to standard name
0.2	P19	Add R542	For ESATA detect function
0.2	P42	Add R886, R887 , C735	For ESATA detect function
0.2	P31	Add R543	For reserve EC control directly
0.2	P39	Change J10 footprint, Del C635, C636	Change J10 for DFx and Del component for layout
0.2	P42	Add R877	For reserve EC control directly
0.2	P42	SW3 BOM structure change to @	For ME ASSY concern
0.2	P24	R324 BOM structure change, del @	For AMD update
0.2	P25	Change Q69,Q70,Q71,Q72 to BSS138, change Q66,Q67 pin 1 net name, D28 change to @	For Change BACO part follow AMD reference DATA ,D28 change to @ for leakage
0.2	P42	Change ESATA from port 5 to port 4	For intel risk
0.2	P15	Add R544,R545	For Pull high SMBus
0.2	P12/13	Del R74~R80,R82 R88~R94,R96	For DDR3 DM Bus to GND
0.2	P16	Add R182,R546	Add 186 for reserve sequence, Add R546 for follow CRB & ORB
0.2	P20	Del Add J12, R257 change to @	For voltage drop

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