

Compal Confidential

KALH0 /KAL90+ /KALG0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-3-4

REV:1.0

<http://shop36609371.taobao.com/>
QQ:52643956

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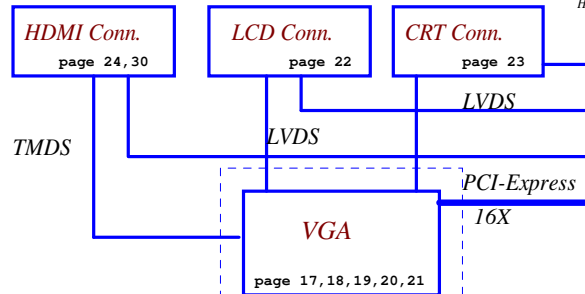
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Thermal Sensor
EMC 1402
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Clock Generator
ICS9LPRS387
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FSB
667/800/1066MHz
H_A#(3..35) H_D#(0..63)



Intel Cantiga
uFCBGA-1329
page 7, 8, 9, 10, 11, 12, 13

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 800/1066
204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3 page 13, 14

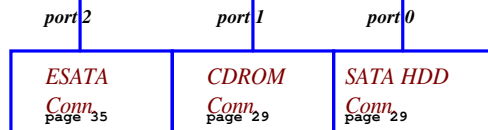
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JMB385
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LAN(GbE)
ATHEROS AR8121
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MINI Card x2
WLAN, Robson2
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New Card
Socket
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RJ45
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BGA-676
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USB conn x3
USB port 0, 2, 5
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Bluetooth
Conn
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CMOS
Camera
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LS-4494P
Finger Print
AES1610

3.3V 48MHz USB
3.3V 24.576MHz/48Mhz HD Audio

GMCH HDA
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MDC 1.5
Conn
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HDA Codec
ALC888S-VC
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VGA HDA
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Audio AMP
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Phone Jack x3
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LPC BUS

ENE KB926
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Touch Pad
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Int.KBD
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EC I/O Buffer
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BIOS
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CIR
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KALG0

LS-4495P
USB/B Conn.
USB port 1
LS-4921P
FUN Conn.
LS-4494P
FINGERPRINT/Comm

KALH0

KAL90+
LS-4493P
Media/B Conn.
LS-4498P
FUN Conn.
LS-4492P
E_KEY/B Conn.
LS-4495P
USB/B Conn.
USB port 1

LS-4495P
USB/B Conn.
USB port 1
LS-5042P
LED/B Conn.
LS-5041P
Media/B Conn.

RTC CKT.
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Power On/Off CKT.
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DC/DC Interface CKT.
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Power Circuit DC/DC
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POWER SW
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA/DDR3	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V GM LVDS MODULE	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG6SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX: KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX: KAL90@/PM@/888VC@/8121@
KALH0-GM45	XXXXXXXXXX: KALH0@/GM@/888VC@/8121@/GM45@
KALH0-GL40	XXXXXXXXXX: KALH0@/GM@/888VC@/8121@/GL40@
KALH0-PM45	XXXXXXXXXX: KALH0@/PM@/888VC@/8121@
KAL90+ -UMA	GM@/888VC@/8121@/GM45@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@
KAL90+ -Dis	PM@/888VC@/8121@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@/PM45@
KALG0 -UMA (GL40)	KALG0@/GM@/888VC@/8121@/GL40@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -Dis	KALG0@/PM@/888VC@/8121@/PM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -UMA (GM45)	KALG0@/GM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -DIS (GM45)	KALG0@/PM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@

KALG0 LAN to AR-8131----- 8121@ Change to 8131@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

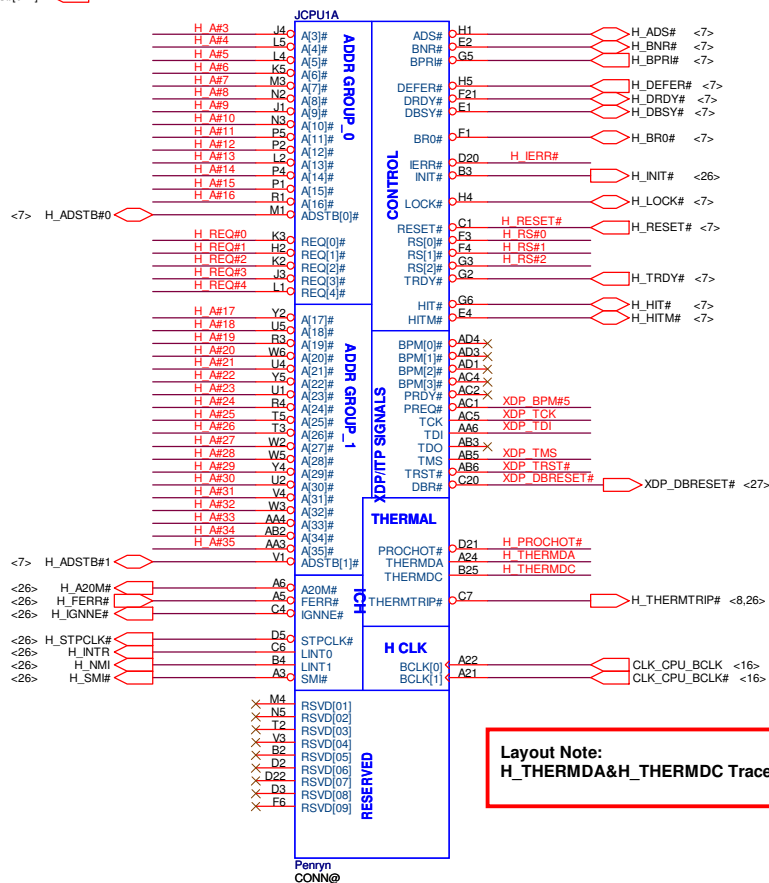
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
KAL90	KAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@
KAL90-G0	KAL90_G0@
KAL90-H0	KAL90_H0@
KALG0	KALG0@
KALH0	KALH0@
ALC268	268@
	KAL90_90+@
	KAL90_H0_G0@
	KAL90+_G0
	KALH0_G0
	KAL90_G0_90+@
	KAL90_H0_90+@
	KAL90+_PCB@
	KALG0_PCB@

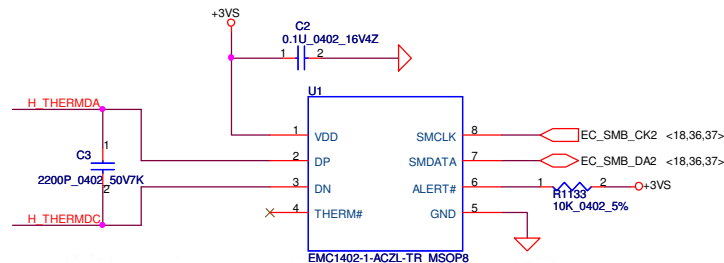
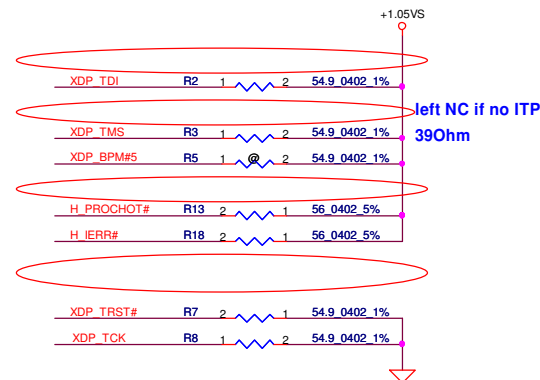
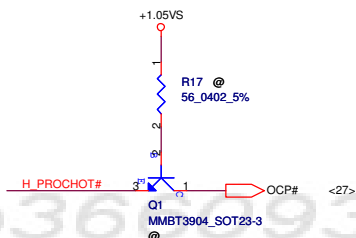
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<7> H_A#(3..35)  H_A#(3..35)
 <7> H_REQ#(0..4)  H_REQ#(0..4)
 <7> H_RS#(0..2)  H_RS#(0..2)

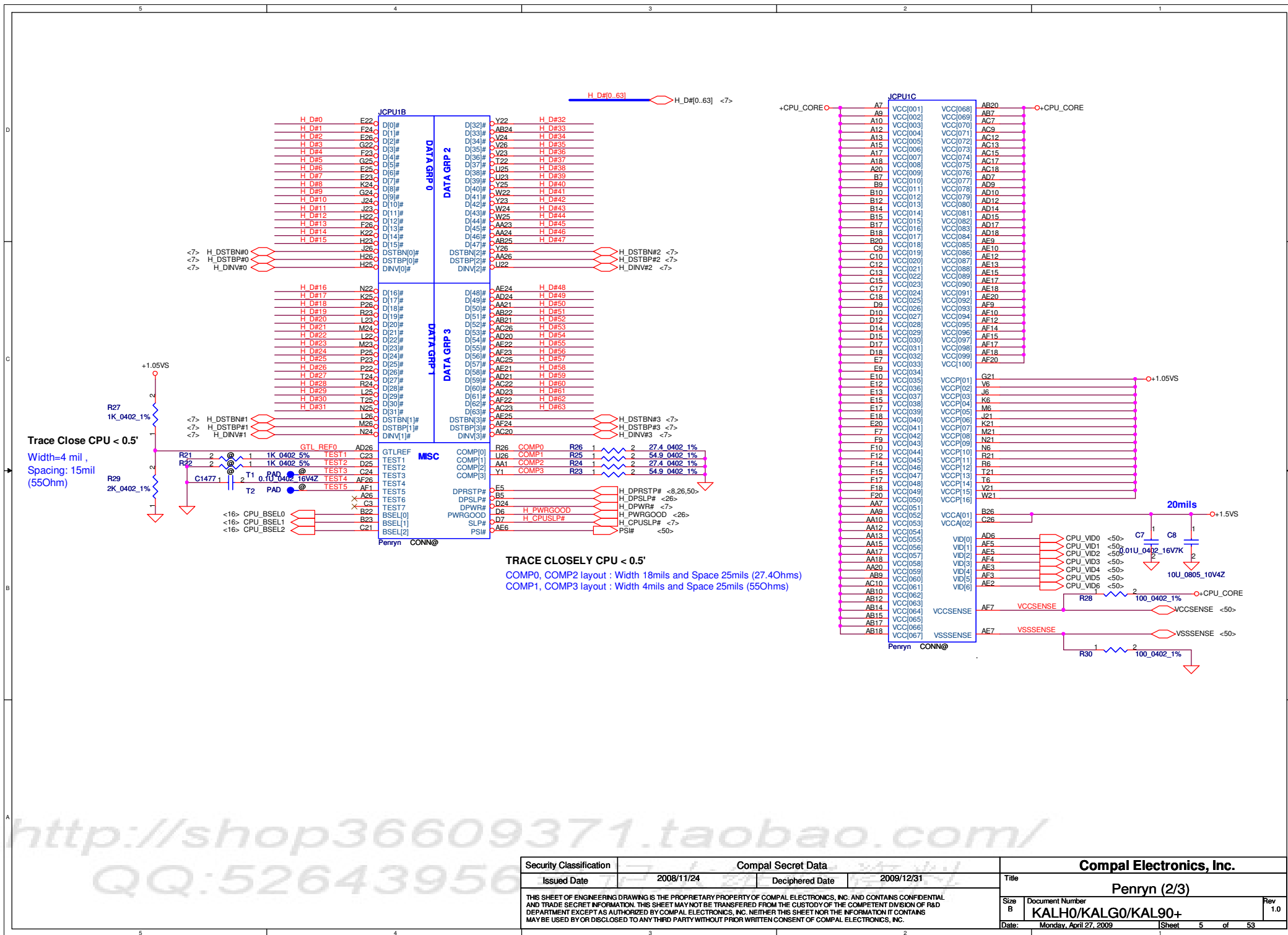


Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

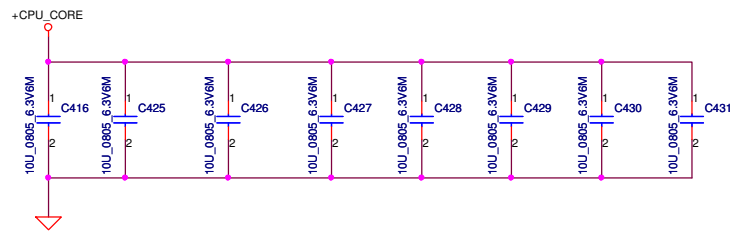
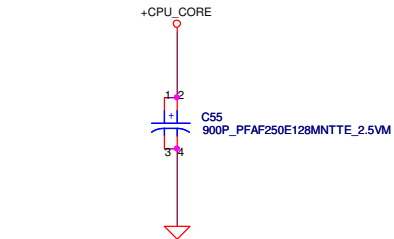
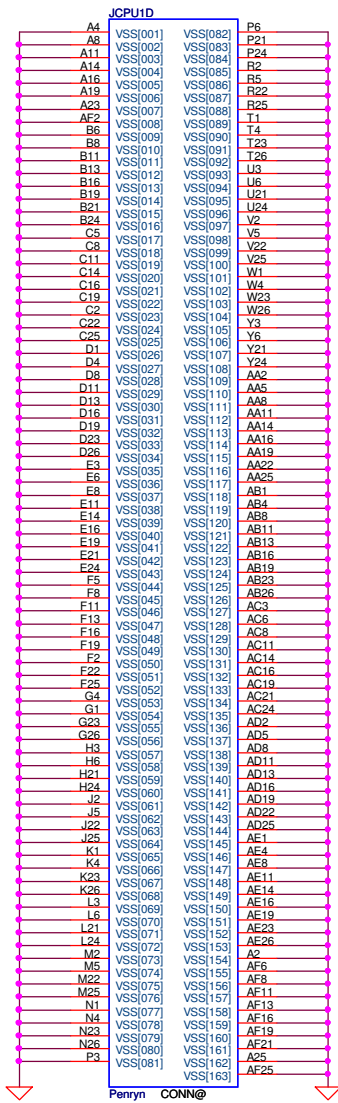


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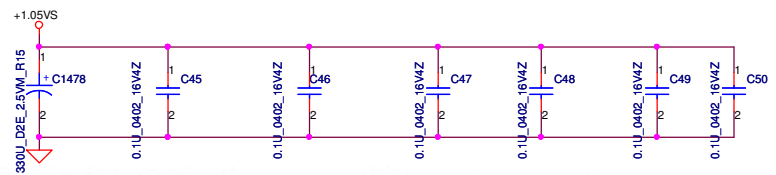


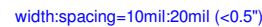
TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

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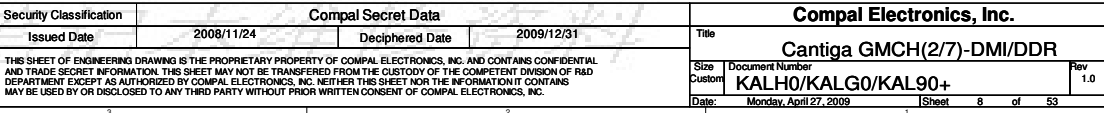


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



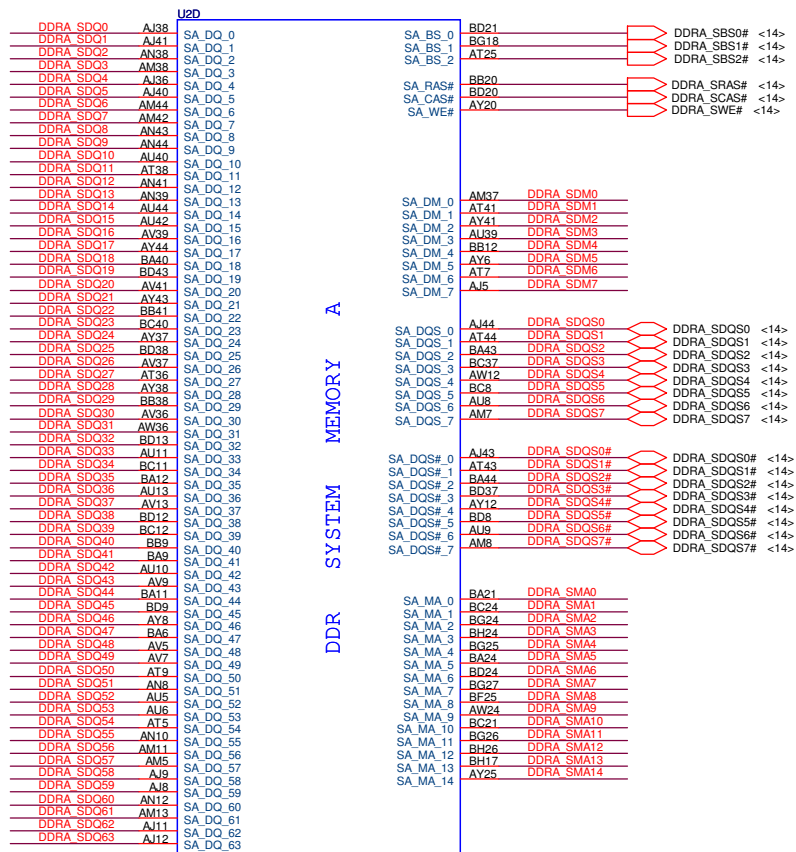


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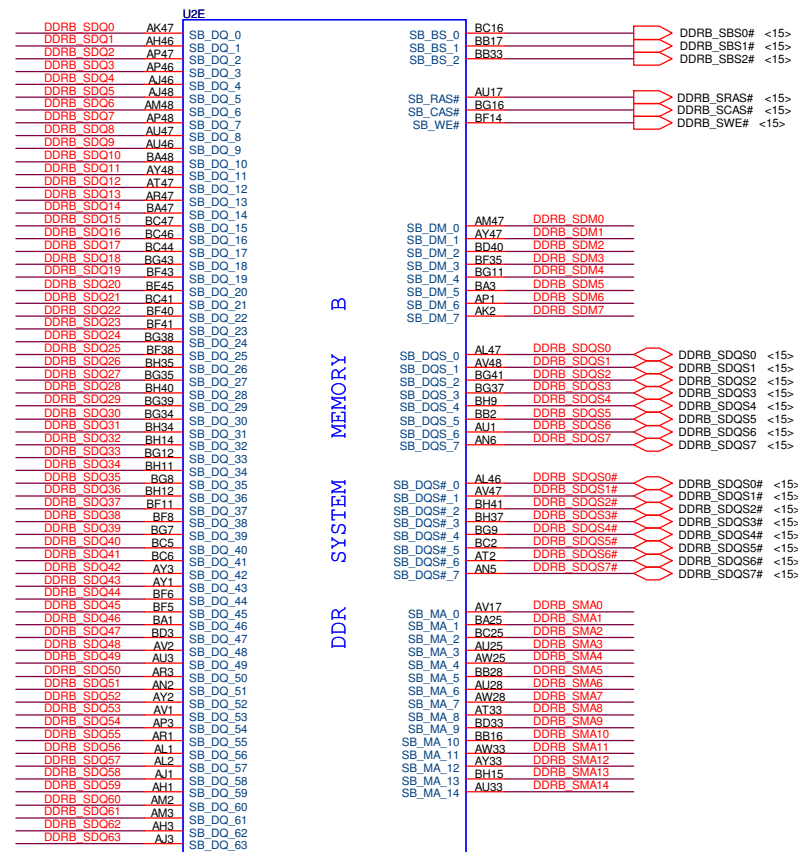


<14> DDRA_SDQ[0..63] DDRA_SDQ[0..63]
<14> DDRA_SDM[0..7] DDRA_SDM[0..7]
<14> DDRA_SMA[0..14] DDRA_SMA[0..14]

<15> DDRB_SDQ[0..63] DDRB_SDQ[0..63]
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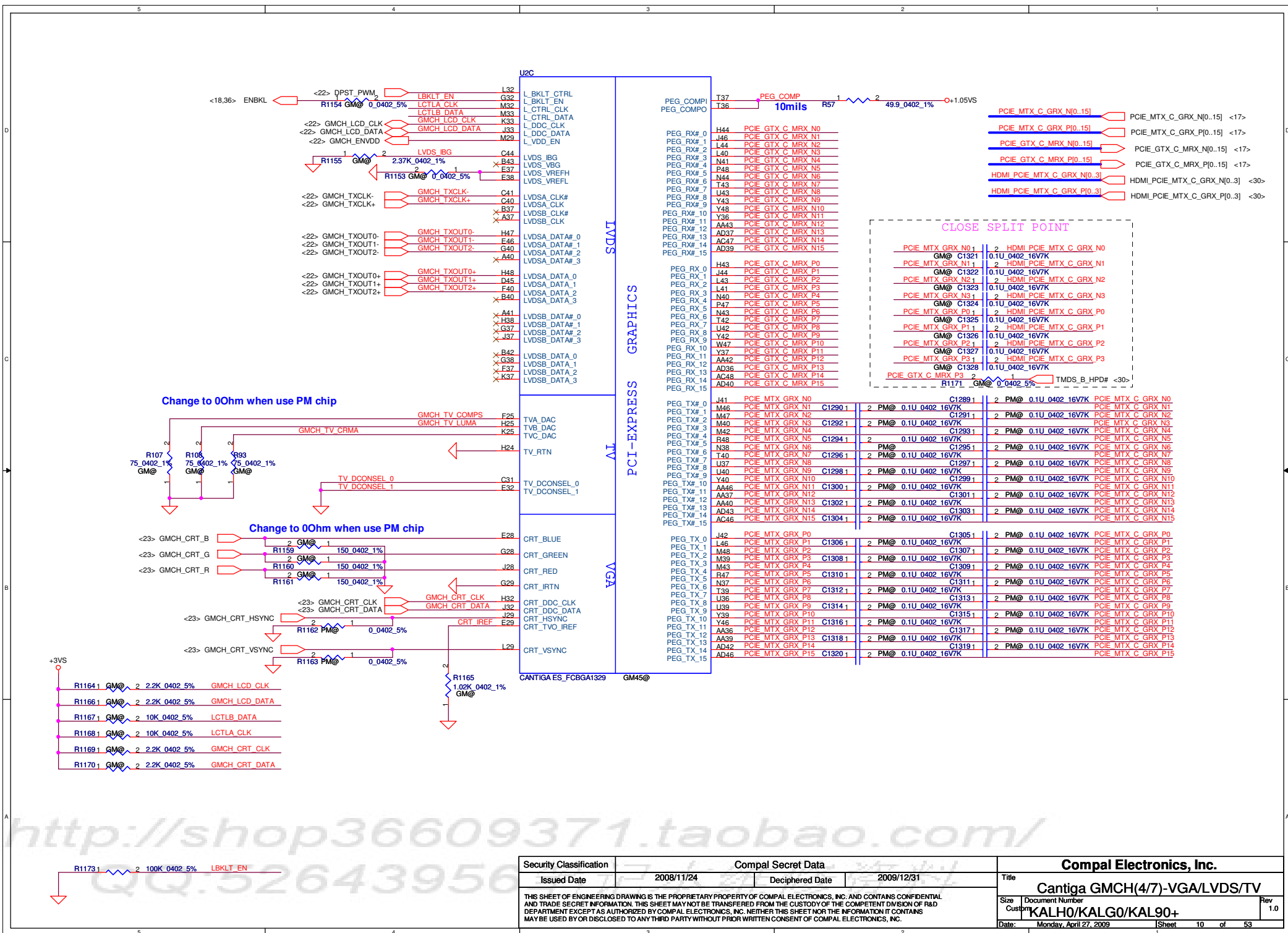


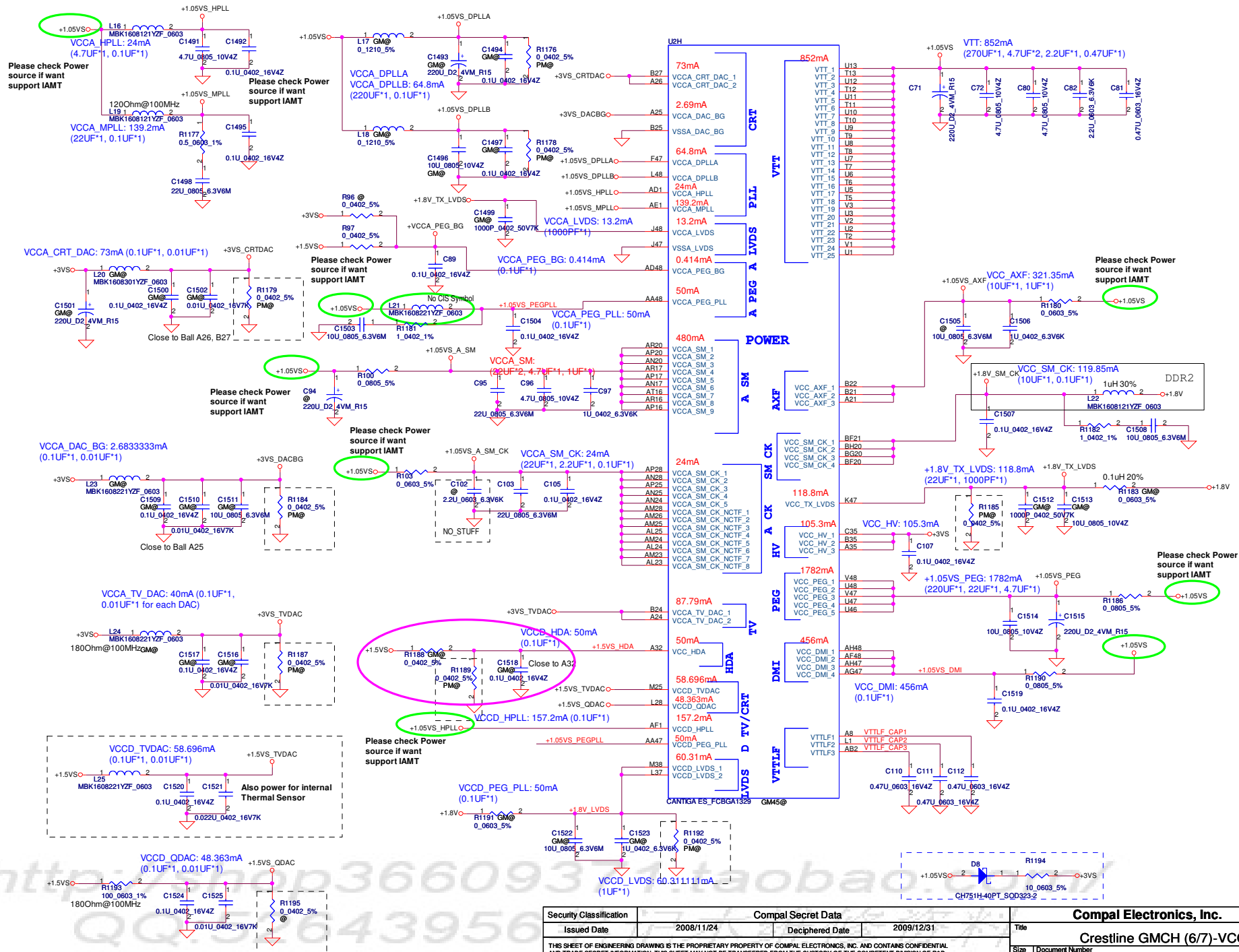
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GM45@

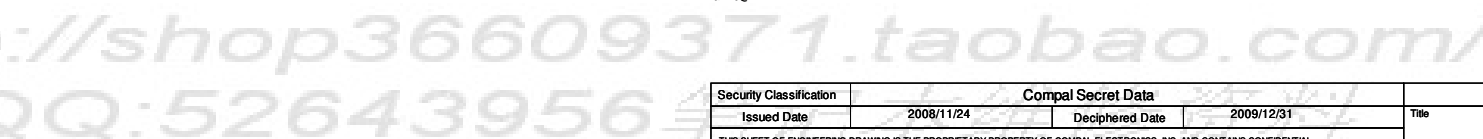


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GM45@

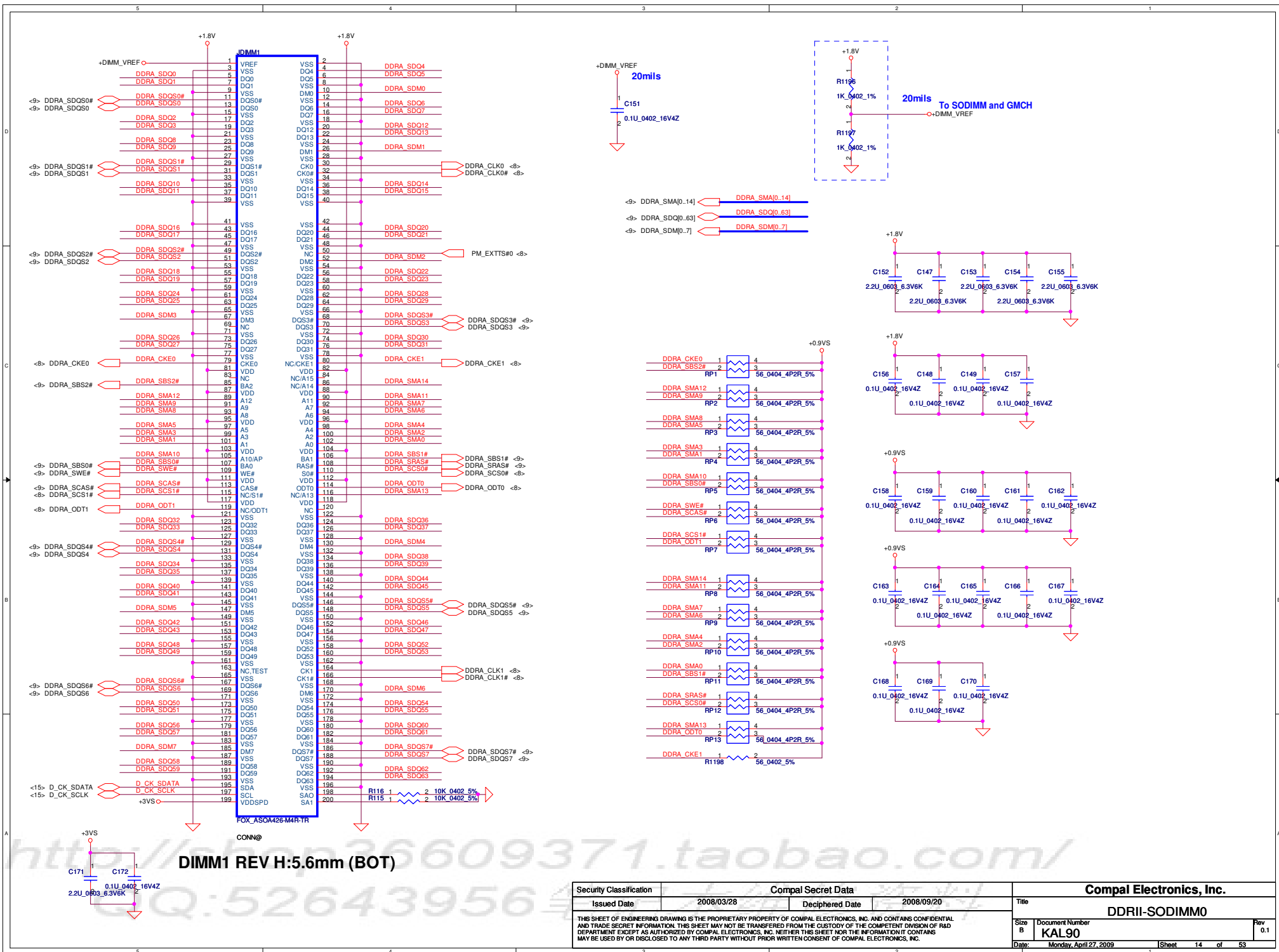
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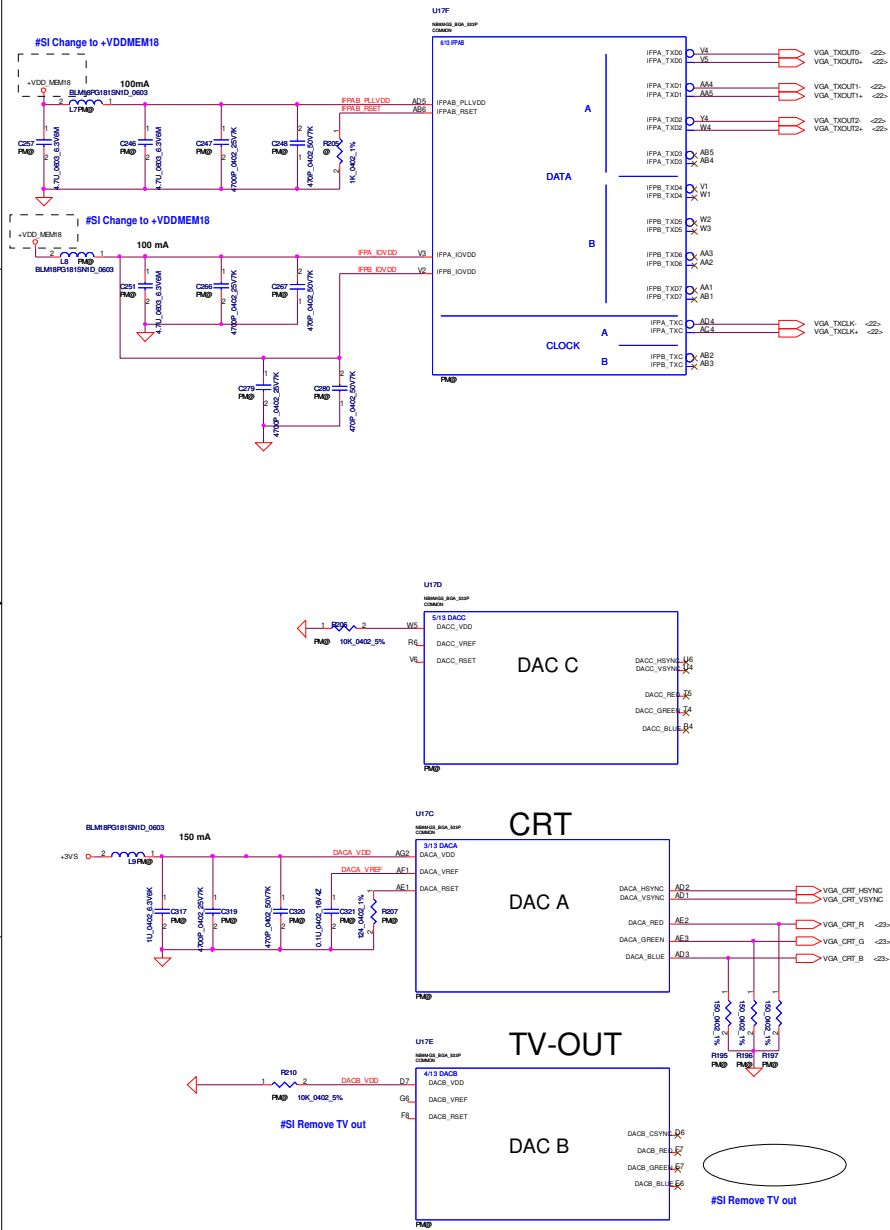




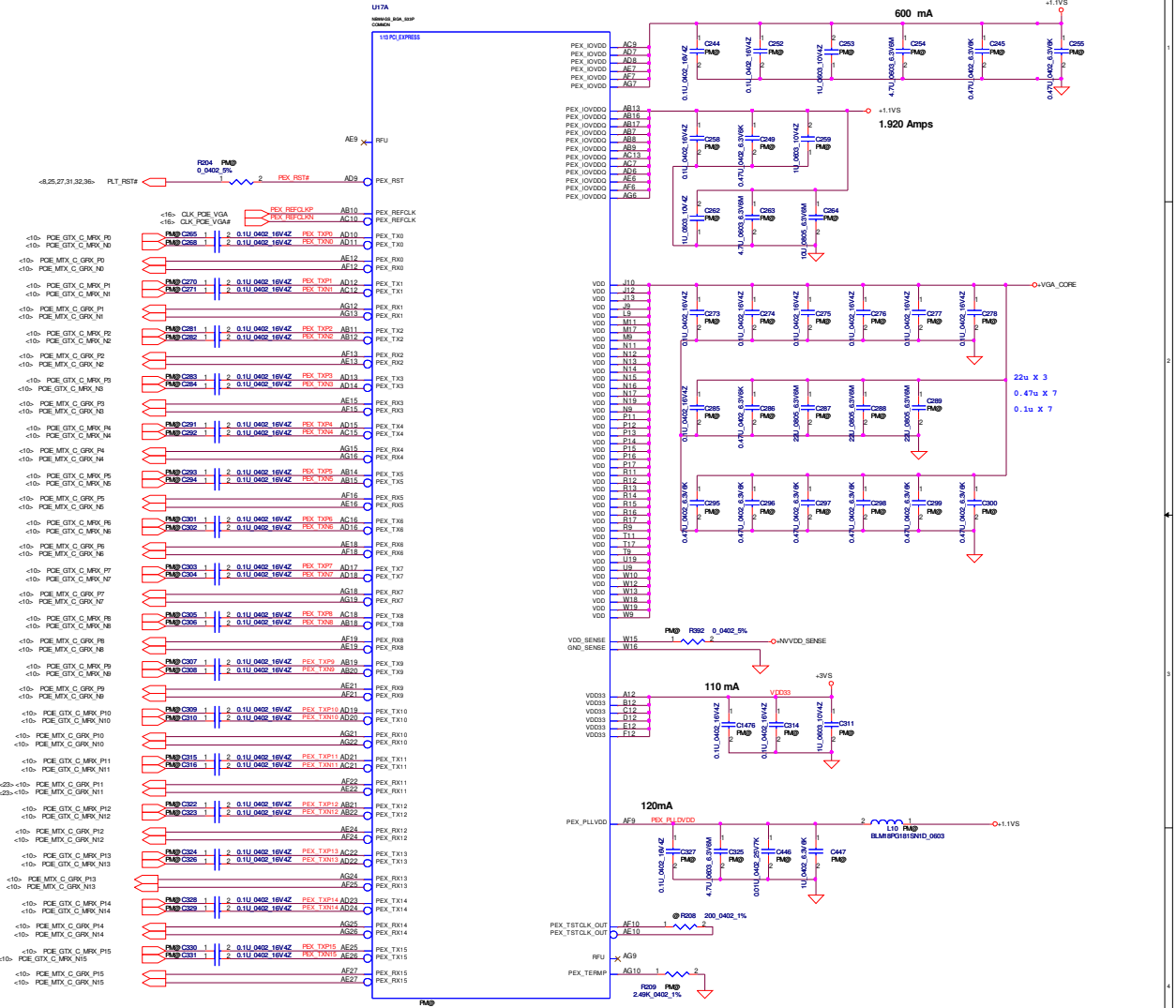
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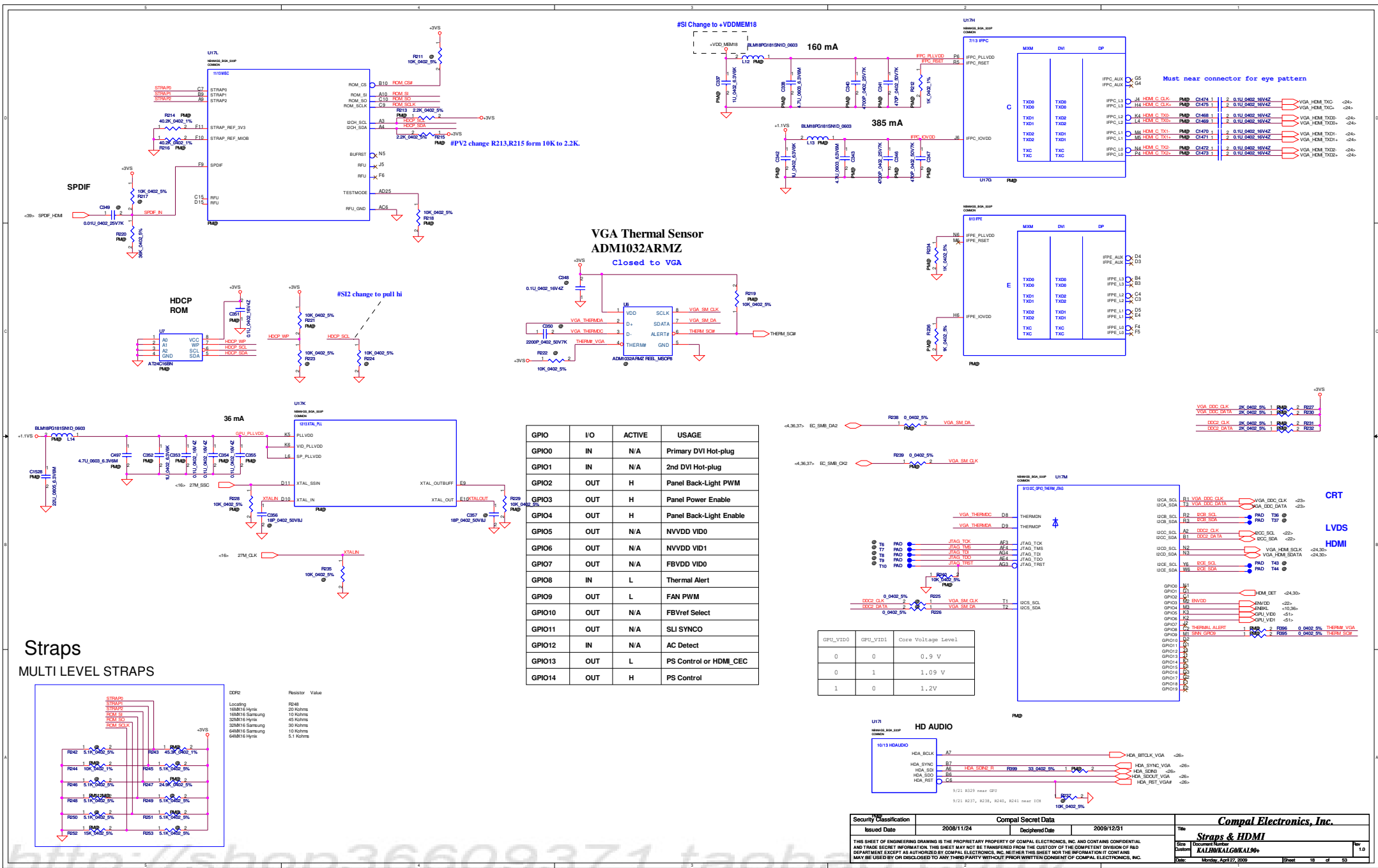
LVDS & DAC Interface



PEG Interface



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GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VIDO
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VIDO
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	SLI SYNC0
GPIO11	IN	N/A	AC Detect
GPIO12	IN	N/A	PS Control or HDMI_CEC
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control

GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.09 V
1	0	1.2V

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Straps & HDMI		KALINKALGKAL90	
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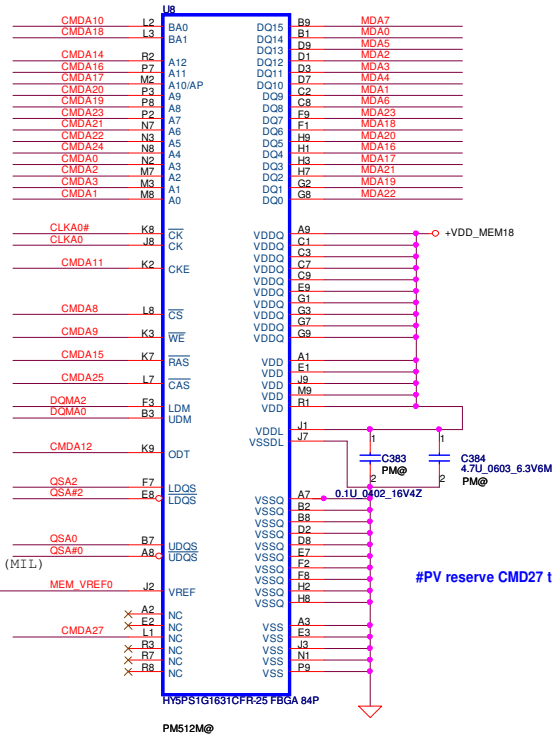
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Date	Docuement Number	Rev		
Monday, April 27, 2009	KALHWGKALG0490	1.0		
	Sheet	19	of	53

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

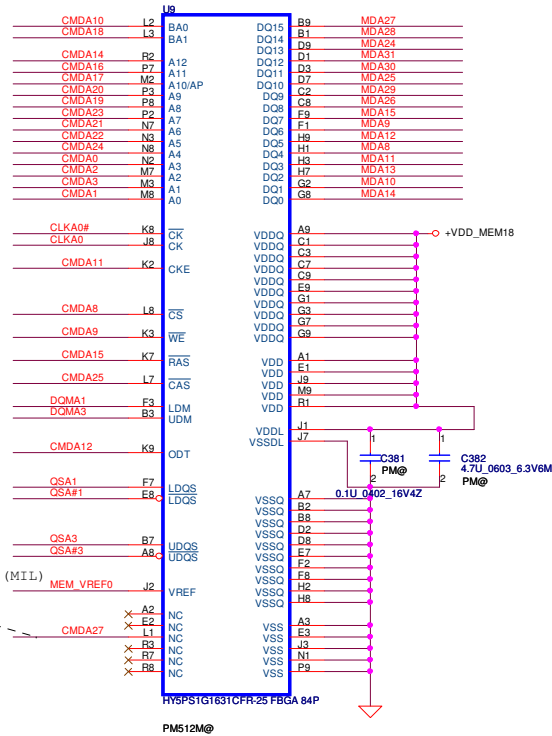
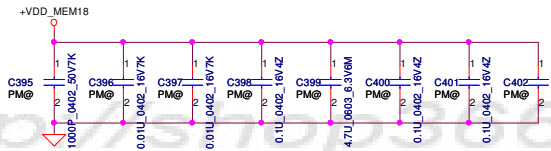
64Mx16 DDR2 400MHz*4==>512MB

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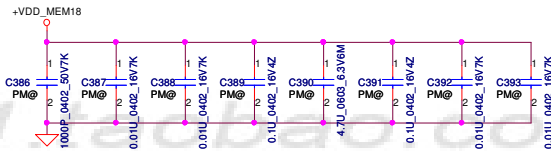


#PV reserve CMD27 to suport 64M x 16

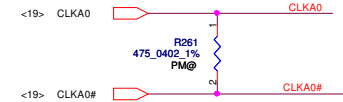
DDR2 BGA MEMORY



DDR BGA MEMORY



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

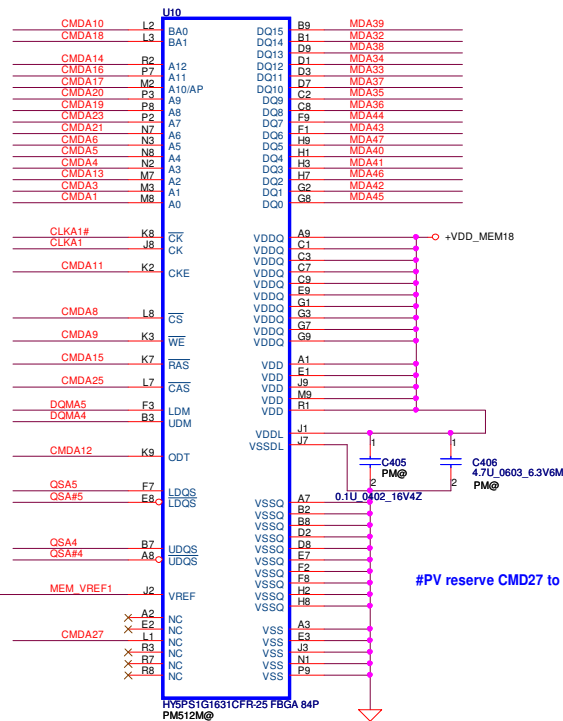
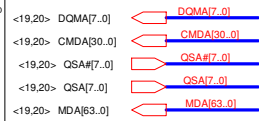


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					KAL90
				Date:	Monday, April 27, 2009
				Sheet	7 of 16

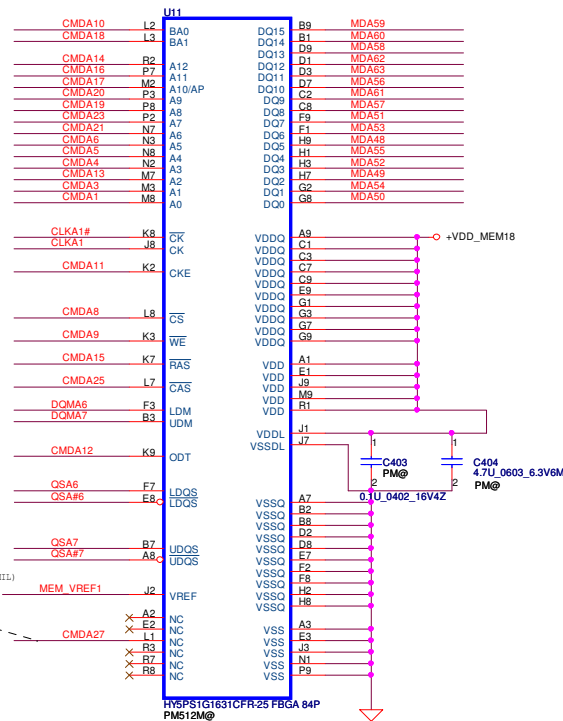
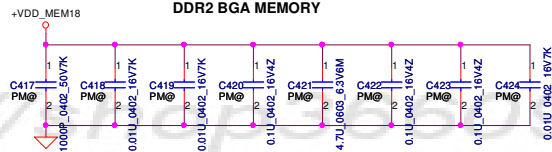
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

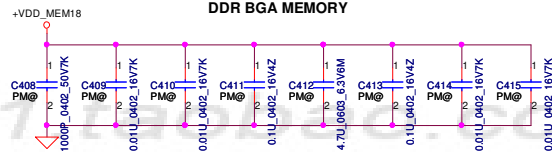
64Mx16 DDR2 400MHz*4==>512MB



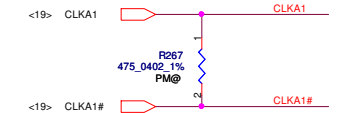
DDR2 BGA MEMORY



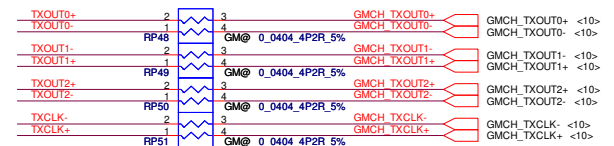
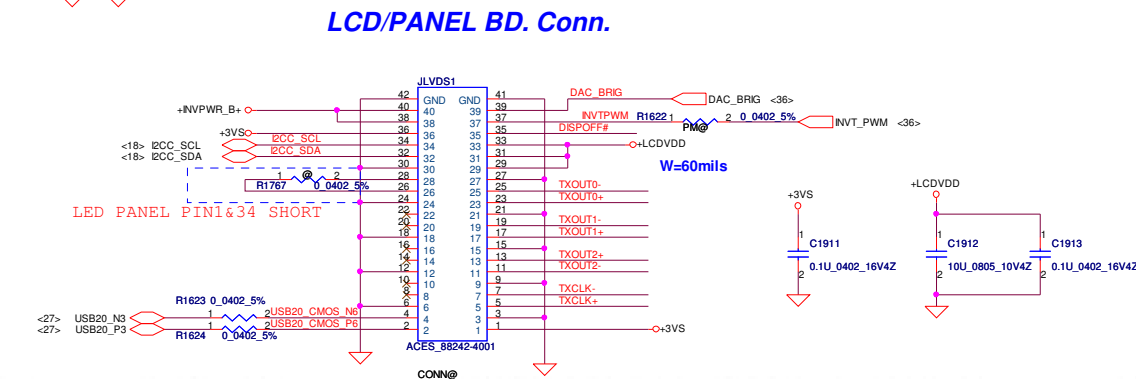
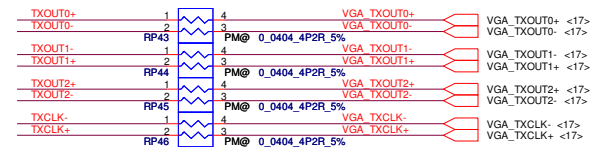
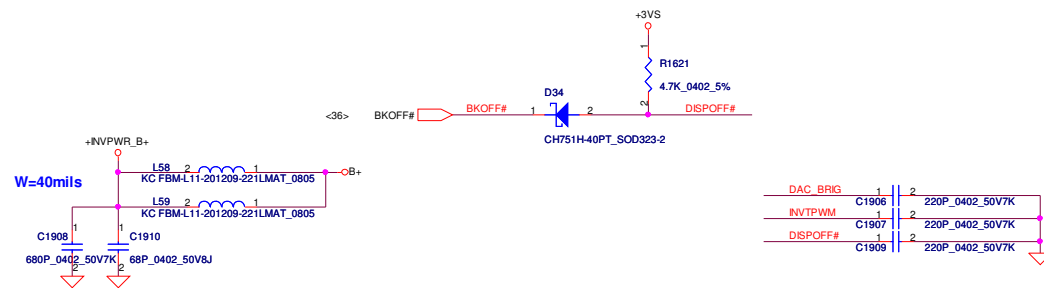
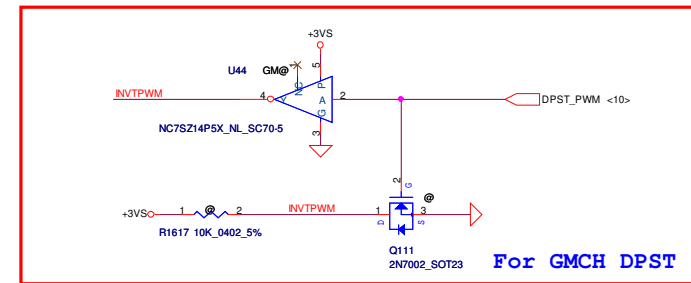
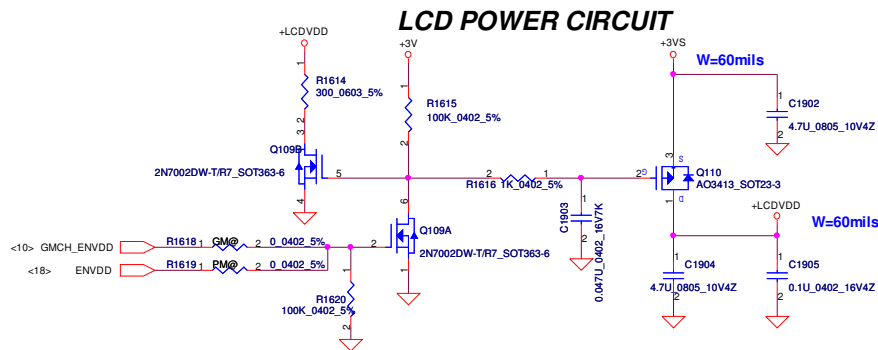
DDR BGA MEMORY



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

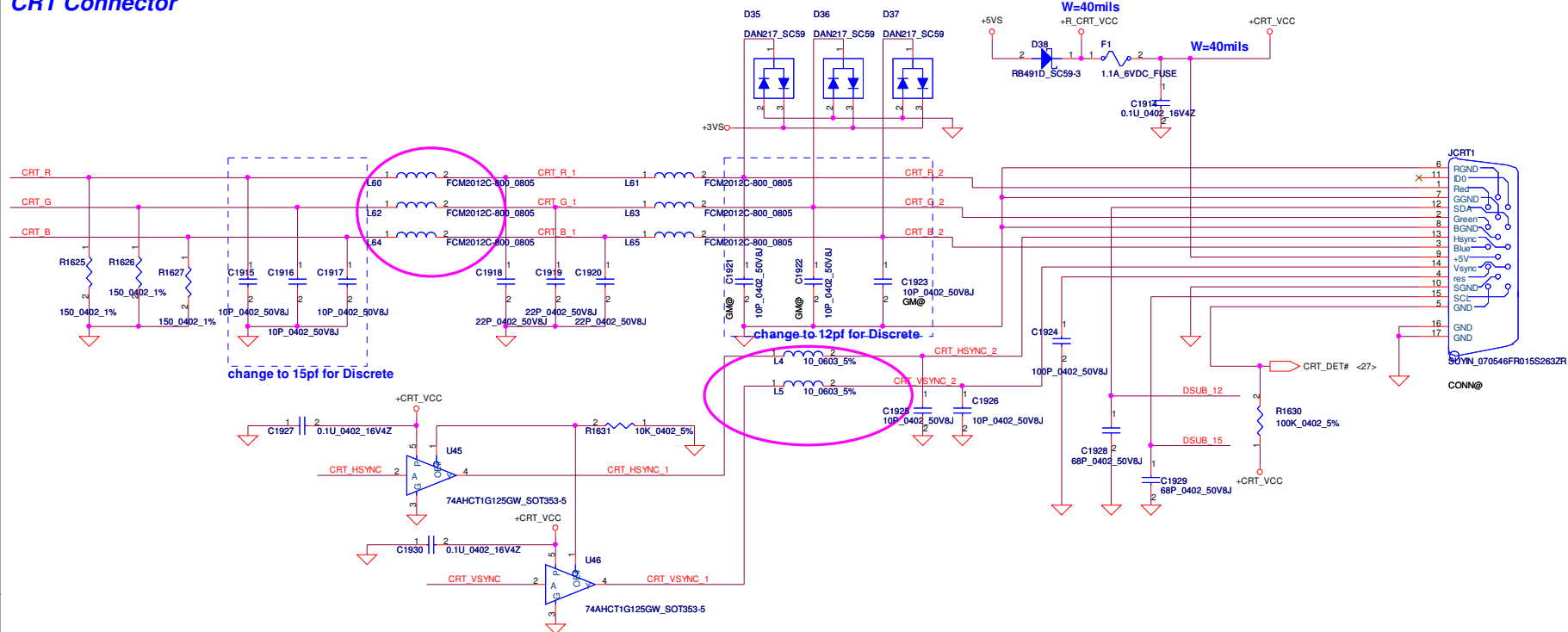


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Date: Monday, April 27, 2009				Sheet	8 of 16

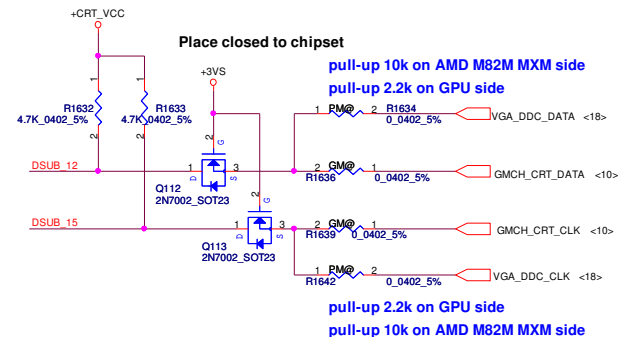


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Size	Document Number	Customer	KALH0/KALG0/KAL90+	Rev	1.0
Date	Monday, April 27, 2009	Sheet	22	of	53

CRT Connector

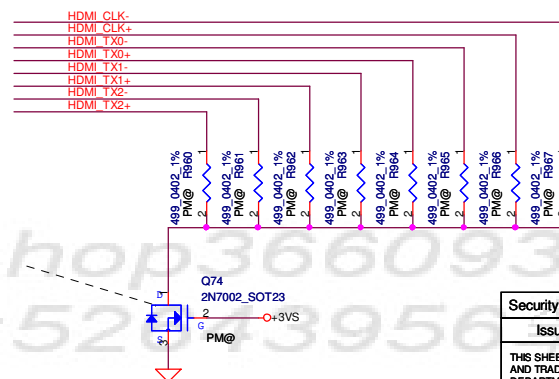
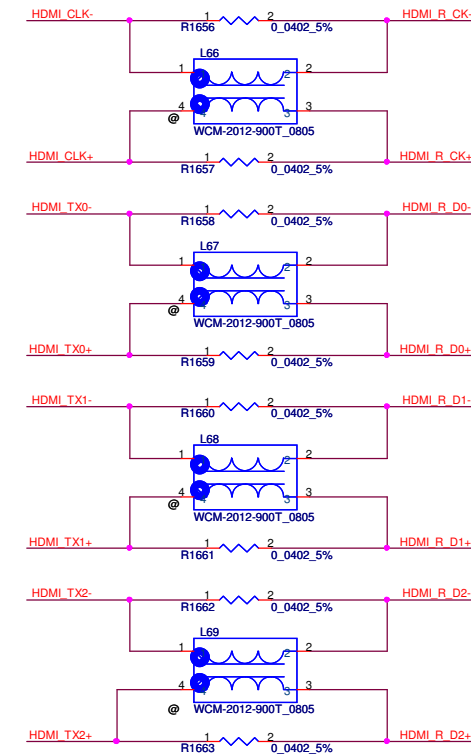
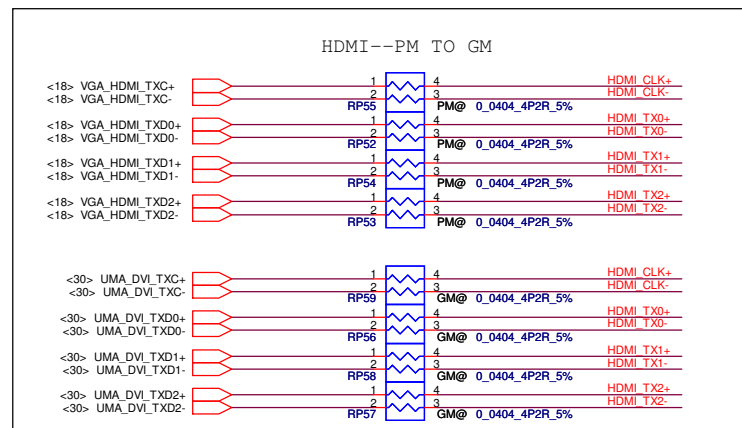
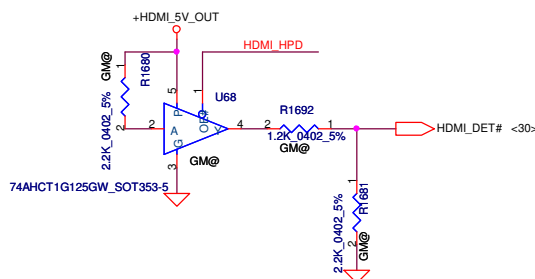
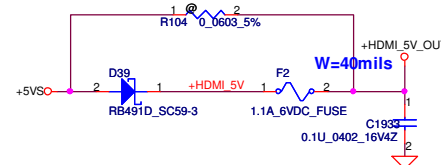
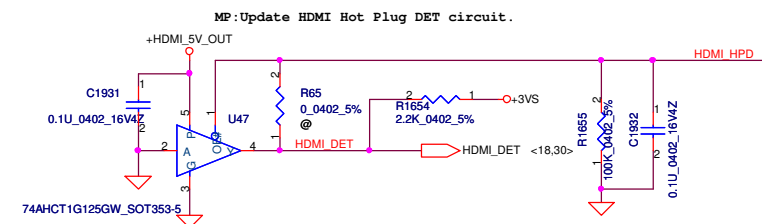
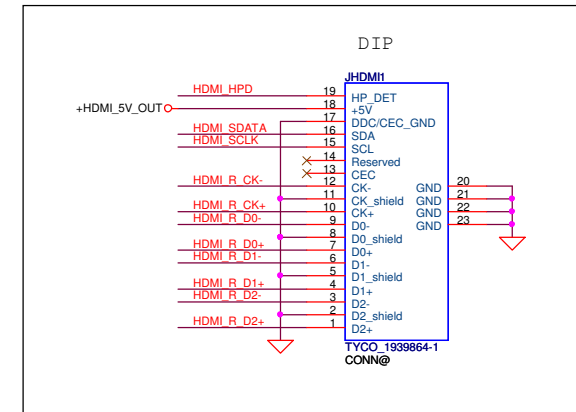
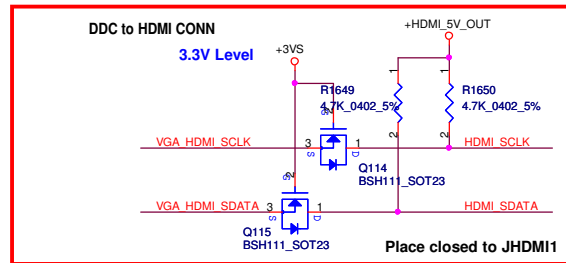
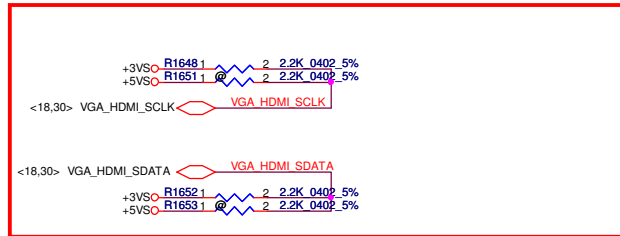


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<10> GMCH_CRT_B	R1638	1	GM@	2	0_0402_5%	CRT_B
<10> GMCH_CRT_G	R1640	1	GM@	2	0_0402_5%	CRT_G
<10> GMCH_CRT_R	R1641	1	GM@	2	0_0402_5%	CRT_R
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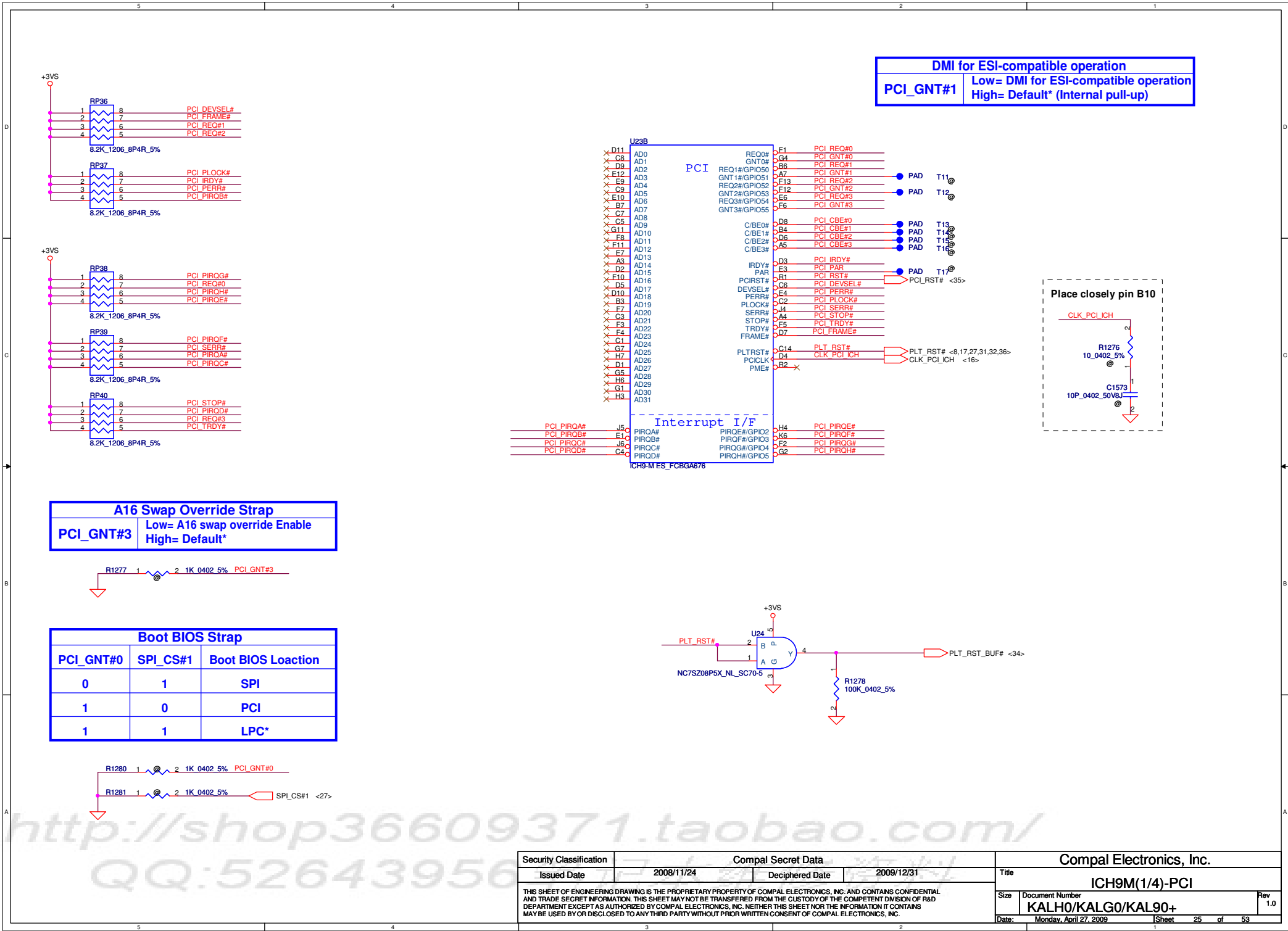


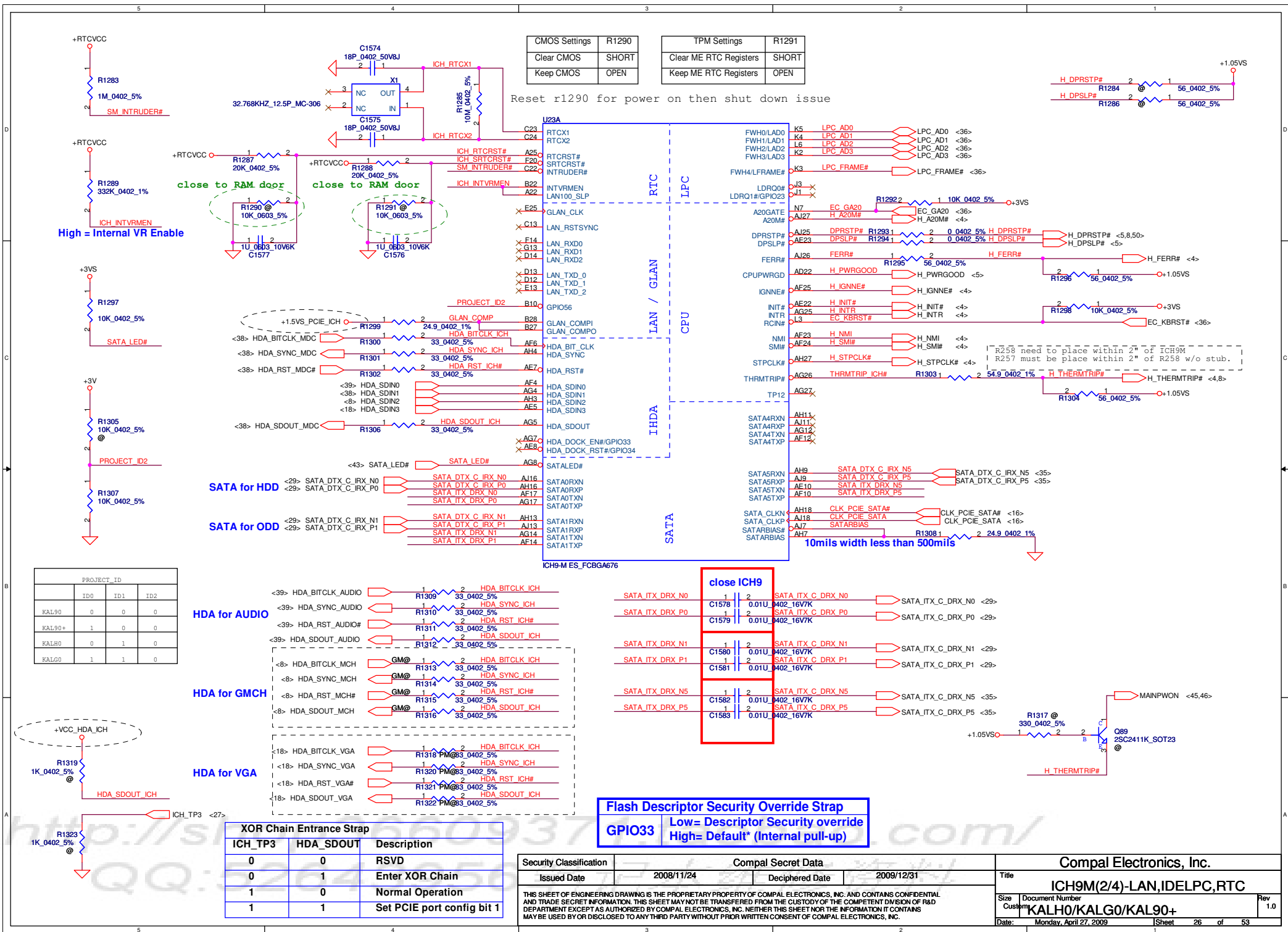
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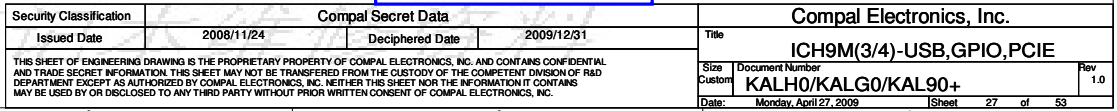
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	CRT Connector	
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				Date	Monday, April 27, 2009
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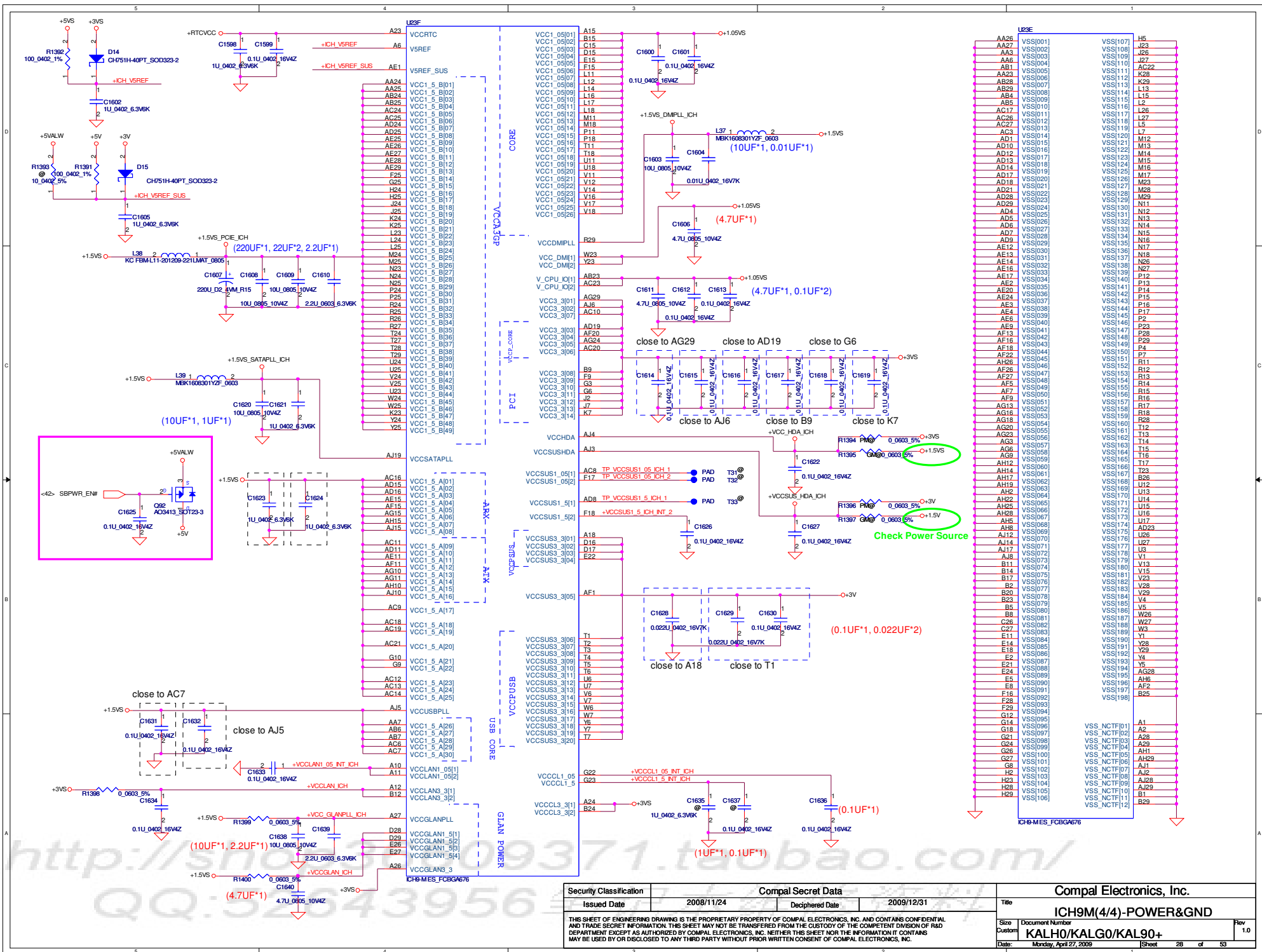


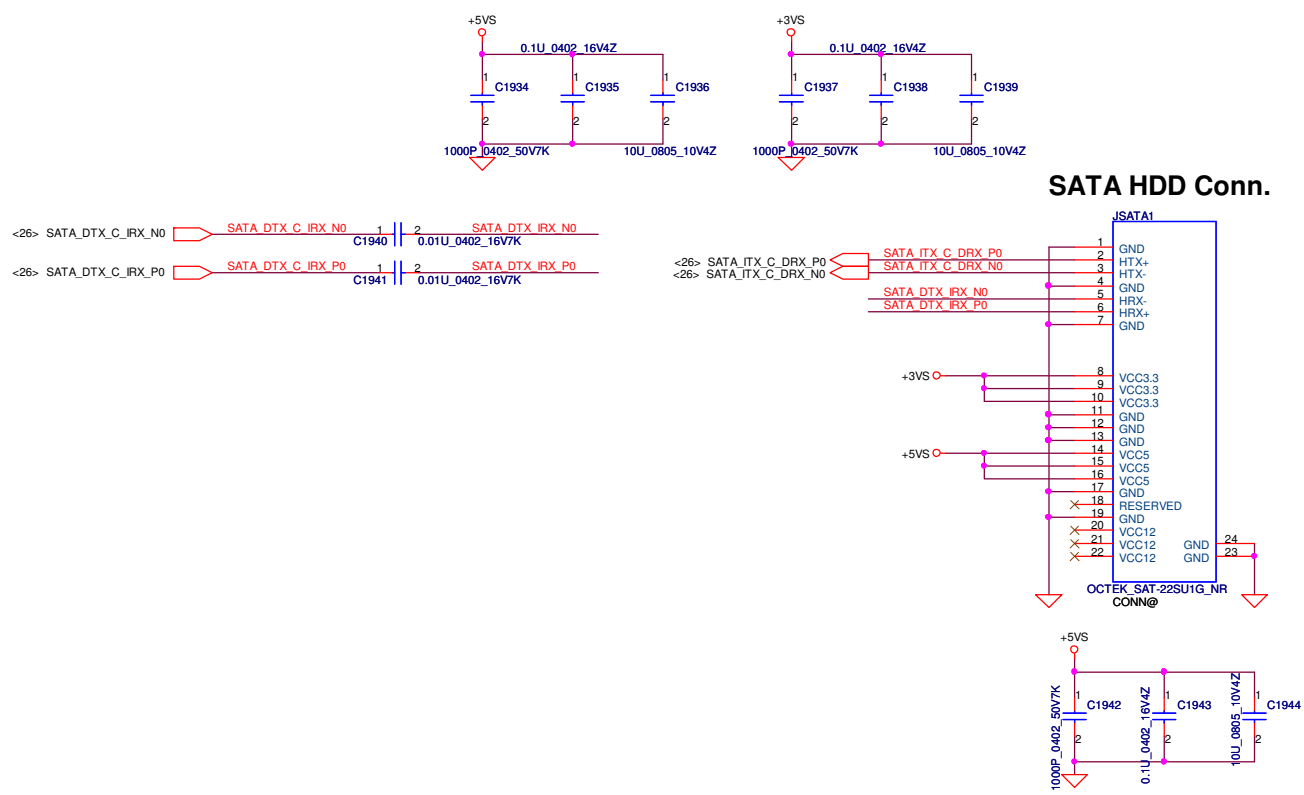
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				Date	Monday, April 27, 2009
				Sheet	24 of 53











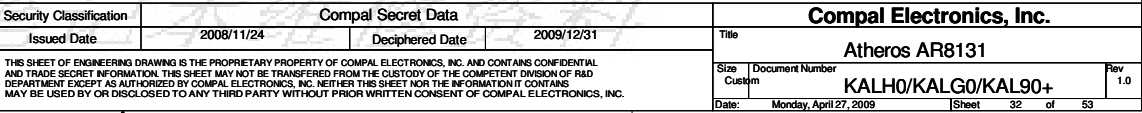
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				Rev	1.0





LAN AR8121/8112

The diagram illustrates the PCB layout for a LAN interface. It features a central LAN AR8121/8112 chip connected to an RJ45 connector (RJ45 GND) and a microcontroller (350uH_GSL5009-1 LF). The layout includes power planes, decoupling capacitors, and signal traces. A green box highlights EMI mitigation components for LAN_ACTIVITY# and LAN_LINK# signals.

Key Components and Connections:

- LAN AR8121/8112:** The main LAN chip, connected to the RJ45 connector and the microcontroller.
- RJ45 GND:** Ground connection for the RJ45 connector.
- 350uH_GSL5009-1 LF:** A microcontroller or logic device connected to the LAN chip.
- Decoupling Capacitors:** Various capacitors (C2003, C2004, C2005, C2006, C2007, C2008, C2009, C2010, C2011, C2012) are used for power plane decoupling and signal conditioning.
- Signal Traces:** Traces for LAN_ACTIVITY#, LAN_LINK#, and LAN_GND are shown, with a green box highlighting EMI mitigation components for LAN_ACTIVITY# and LAN_LINK#.

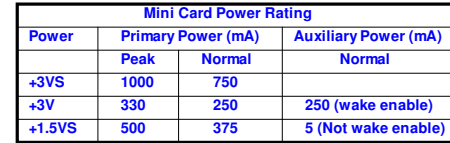
Legend:

- LAN_ACTIVITY#:** Signal trace with EMI mitigation components (C2011, C2012).
- LAN_LINK#:** Signal trace with EMI mitigation components (C2011, C2012).

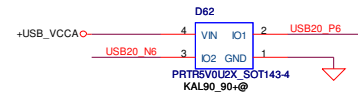
For EMI

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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	LAN Magnetic & RJ45	
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				KALH0/KALG0/KAL90+		
Date: Monday, April 27, 2009		Sheet 33 of 53				

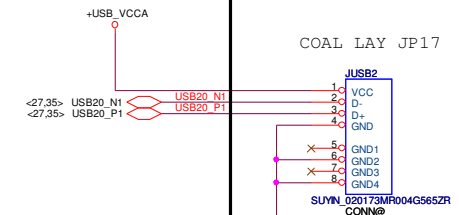
For Robson2



USB CONN.



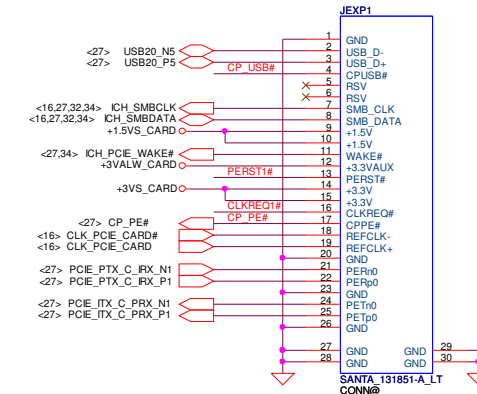
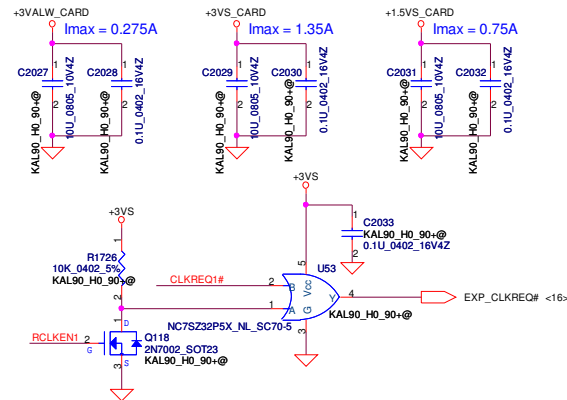
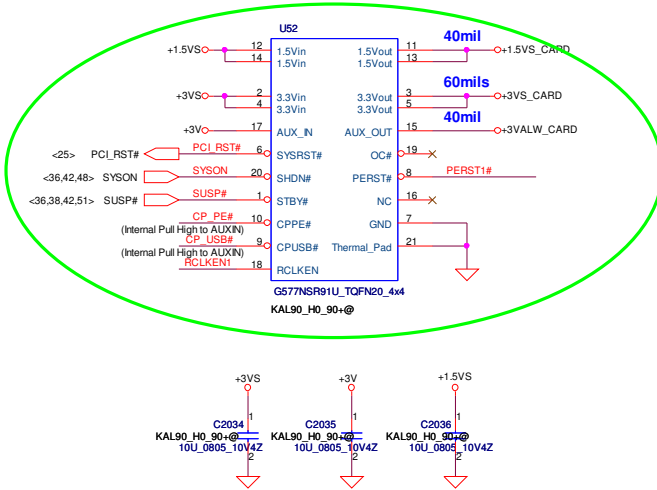
For Wireless LAN



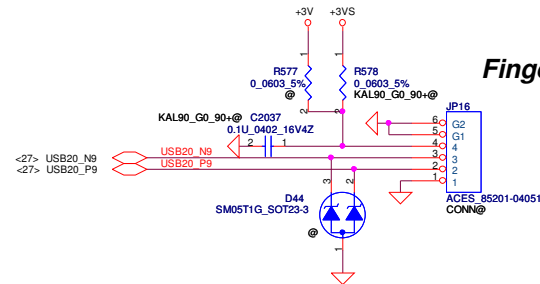
To USB/B Connector



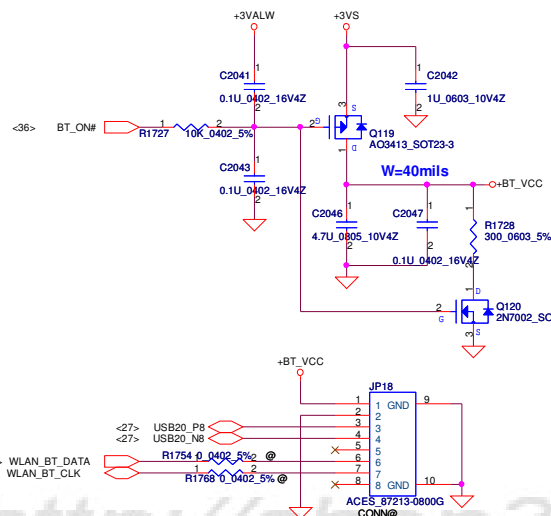
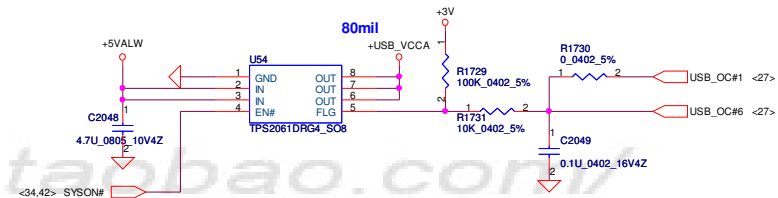
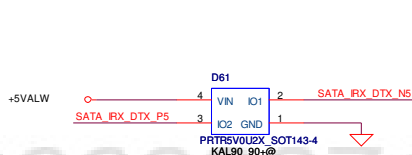
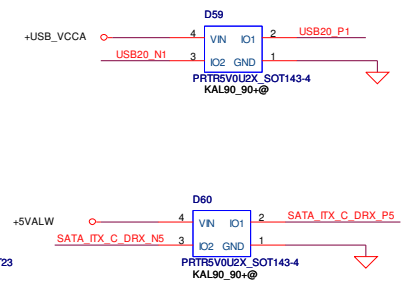
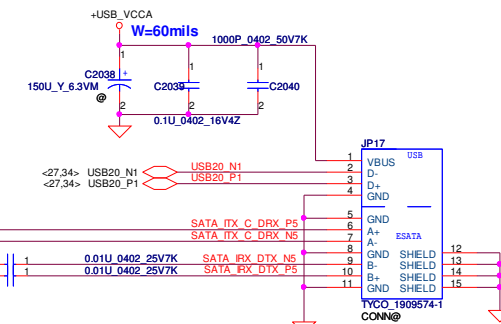
New Card Power Switch



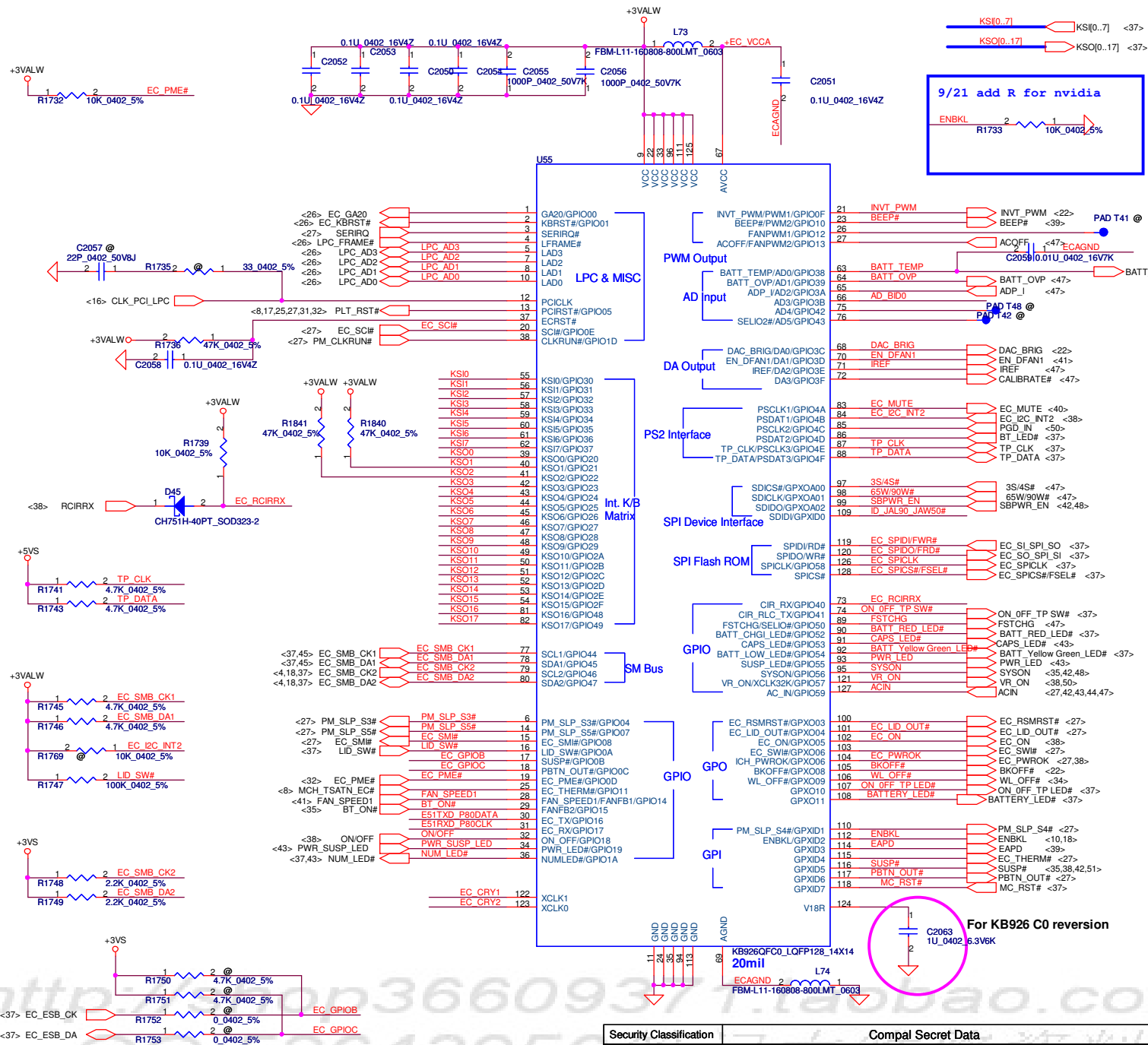
Finger Print Conn.



Bluetooth Conn.

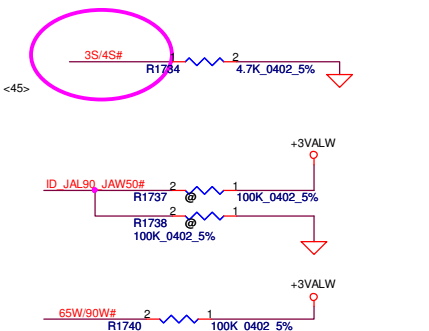
**ESATA CONN**

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				KALH0/KALG0/KAL90+	
Date: Monday, April 27, 2009				Sheet 35	of 53

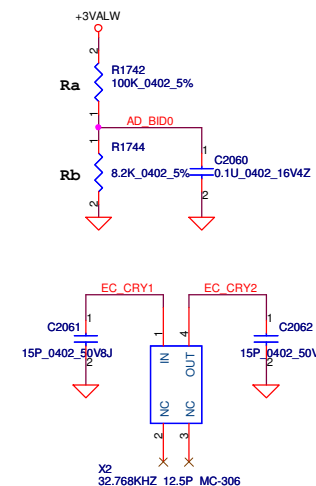


For EC Tools

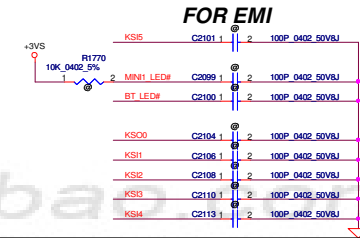
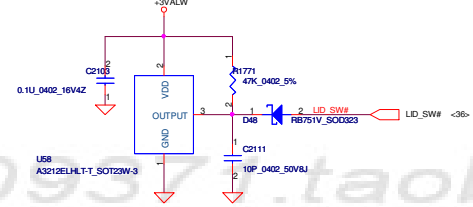
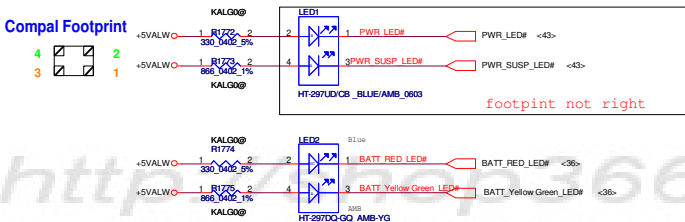
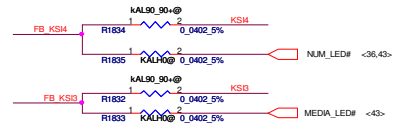
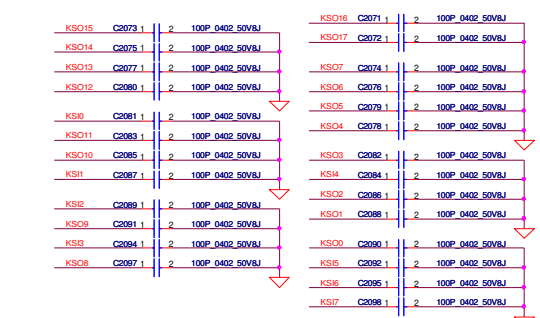
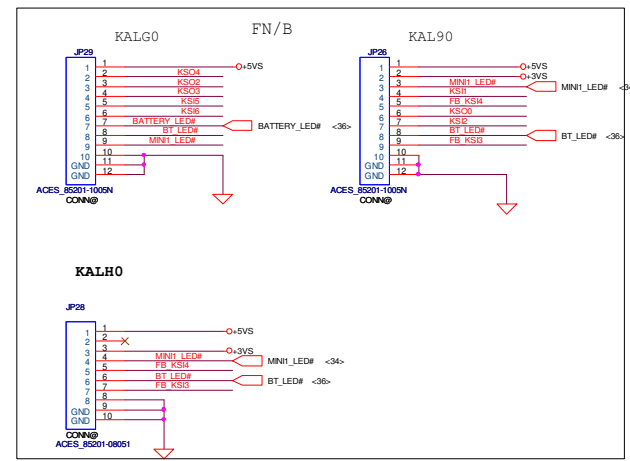
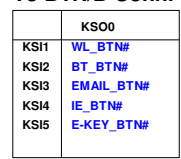
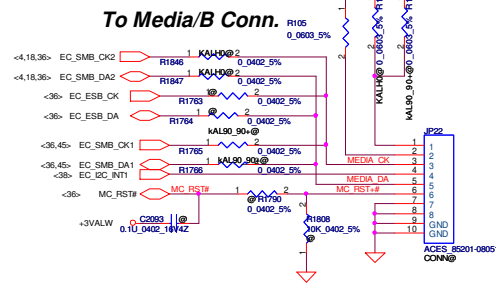
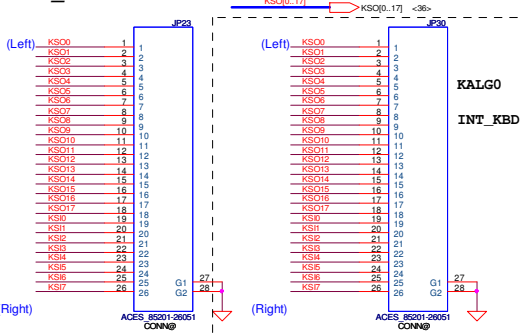
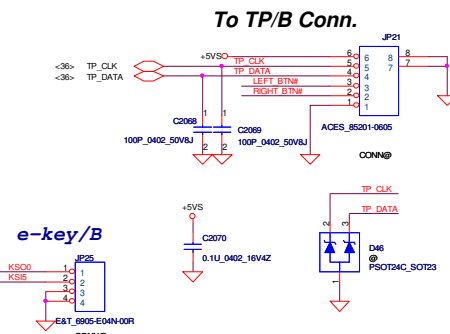
Place on RAM door



Analog Board ID definition,
Please see page 3.



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Issued Date	2008/11/24	Deciphered Date	2009/12/31	EC ENE KB926	
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Date: Monday, April 27, 2009				Sheet 36	of 53

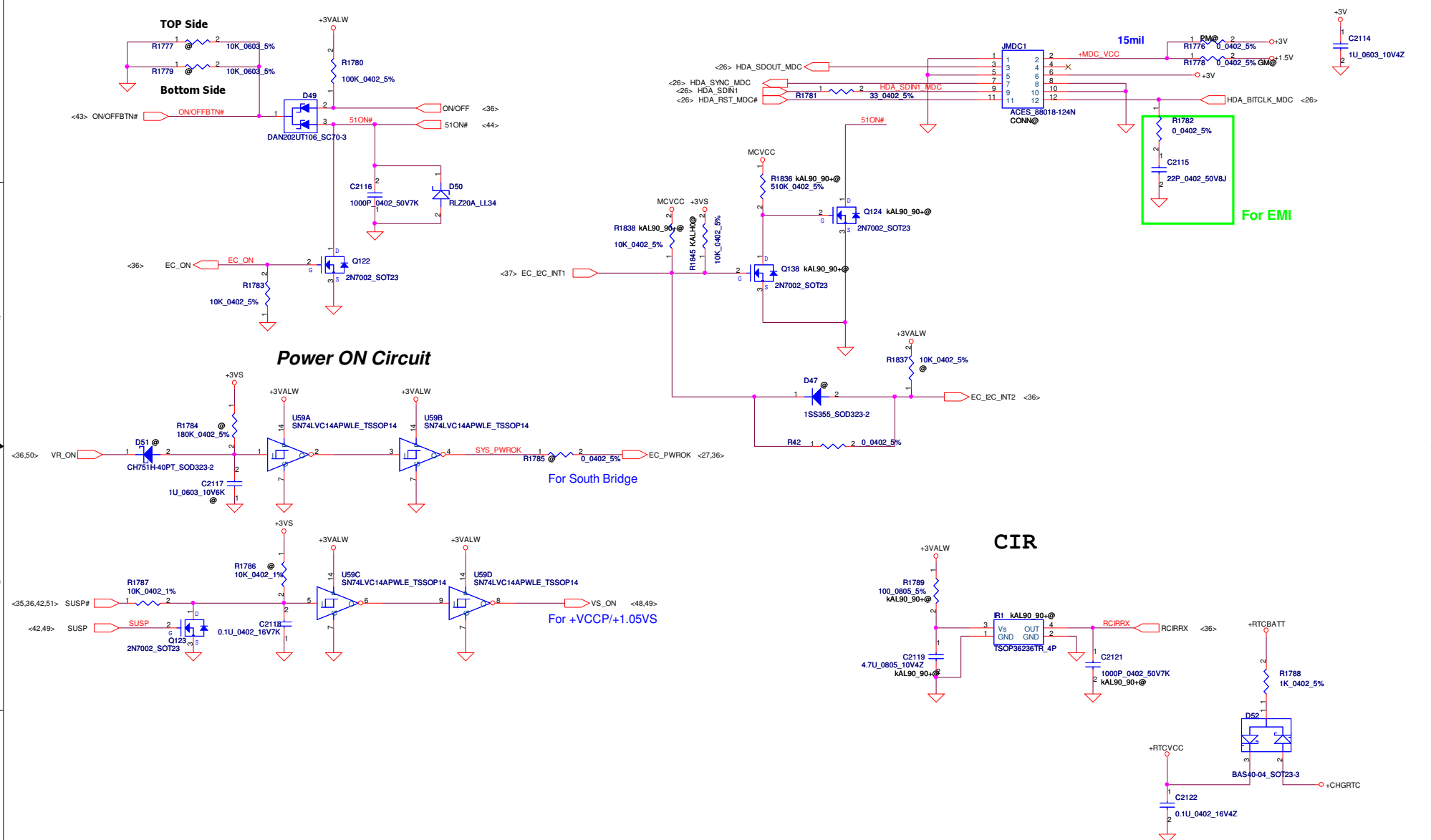


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	BIOS, I/O Port & K/B Connector
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Date	Monday, April 22, 2009	Sheet	37	of	53

ON/OFF switch

Power Button

HDA MDC Conn.

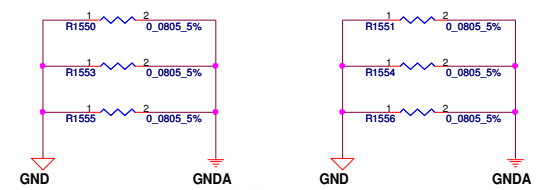
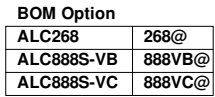


Power ON Circuit

CIR

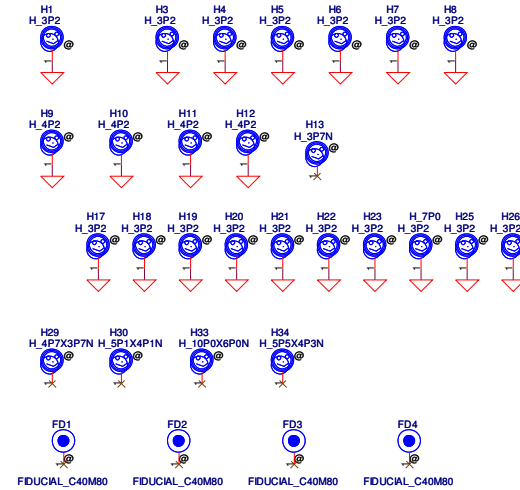
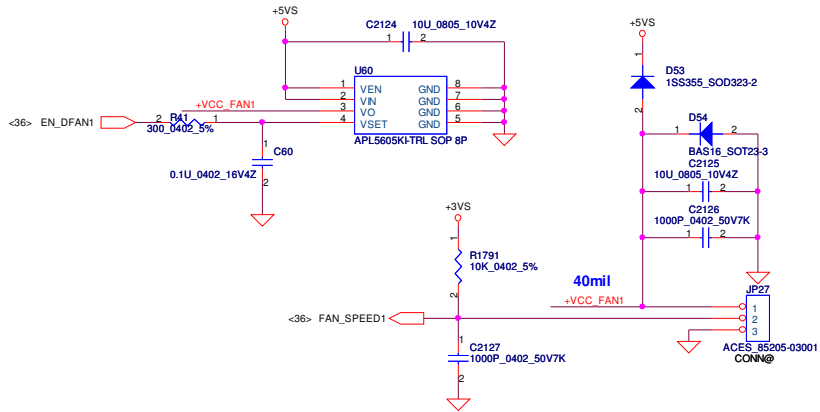
<http://shop36609371.taobao.com/>
QQ:52643956

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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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Size	B	Document Number	KALH0/KALG0/KAL90+		Rev
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	HD Audio Codec ALC888S-VC
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				Rev	1.0

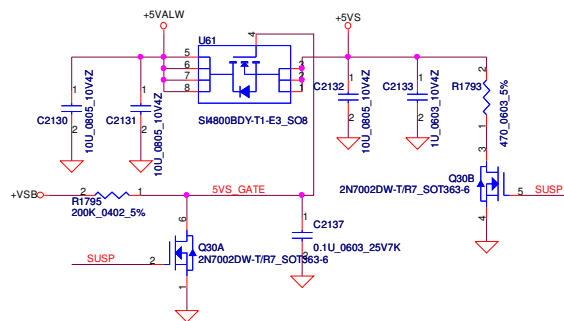
FAN1 Conn



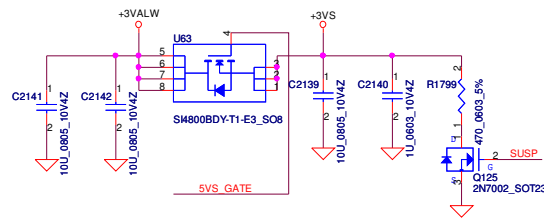
<http://shop36609371.taobao.com/>
 QQ:52643956

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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title		
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Size	B	Document Number	KALH0/KALG0/KAL90+	Rev	1.0	
Date:	Monday, April 27, 2009			Sheet	41	of 53

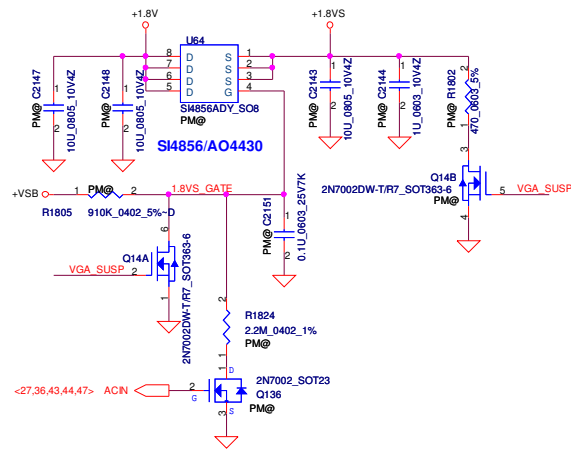
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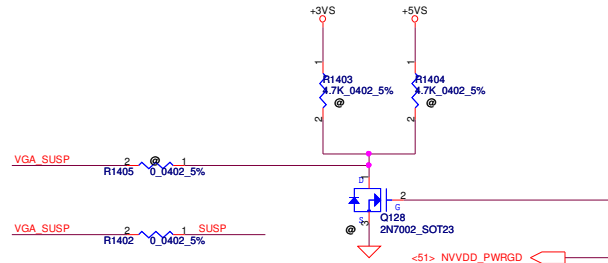
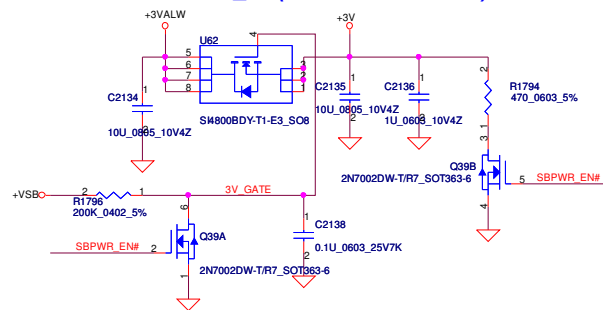
+3VALW TO +3VS



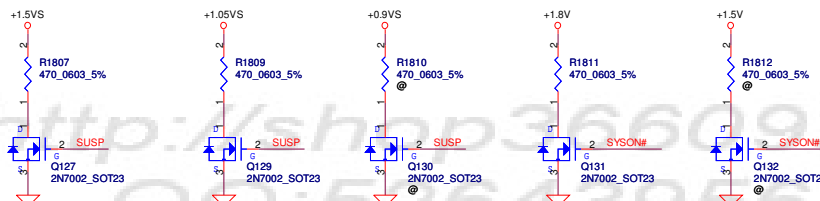
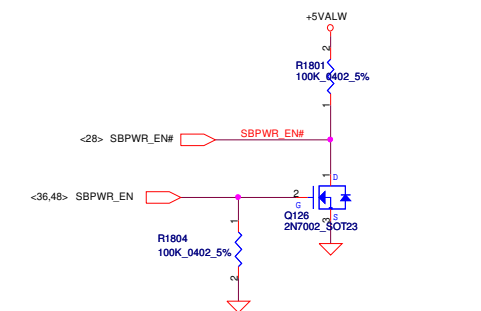
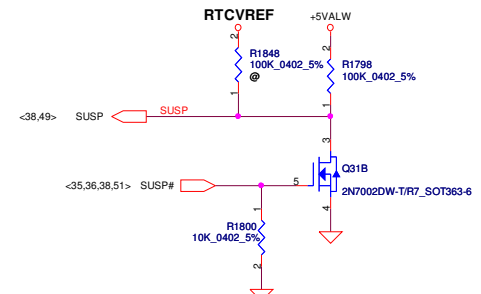
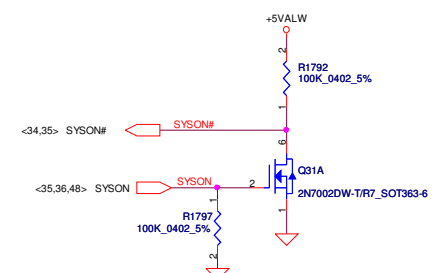
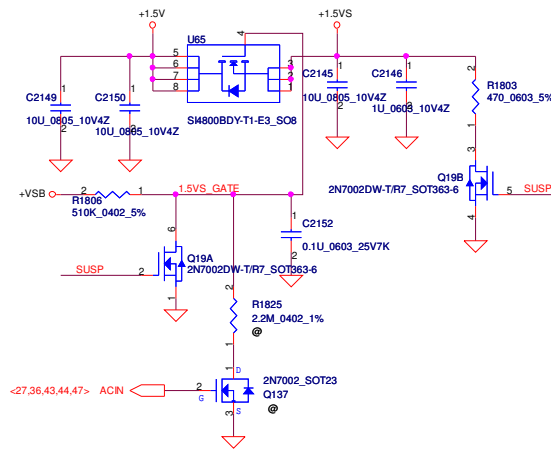
+1.8V to +1.8VS



+3VALW TO +3V_SB(ICH8M AUX Power)

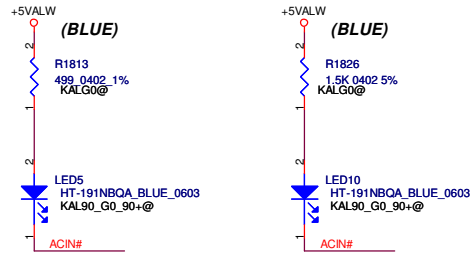


+1.5V to +1.5VS

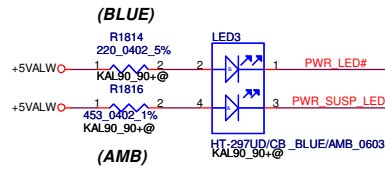


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Size	B	Document Number	KALH0/KALG0/KAL90+		Rev
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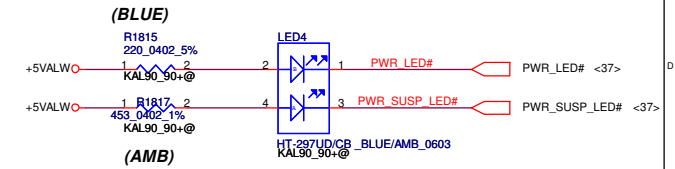
Enlightener LED



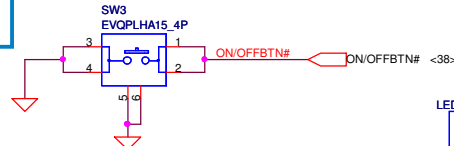
ON/OFF LED LEFT



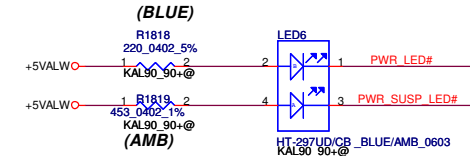
ON/OFF LED RIGHT



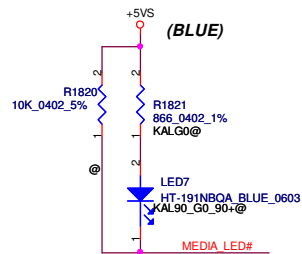
ON/OFF Button



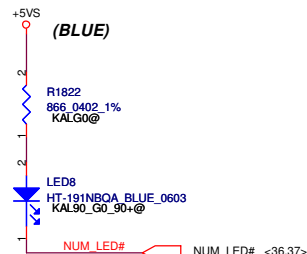
ON/OFF LED DOWN



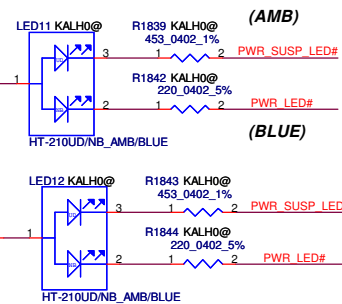
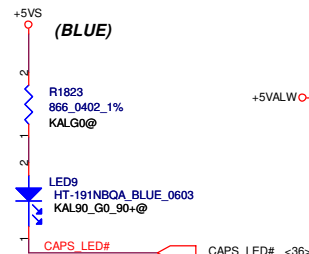
MEDIA_LED



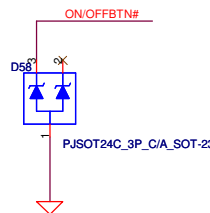
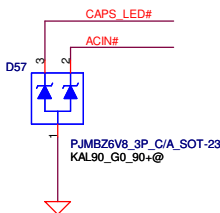
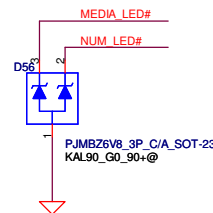
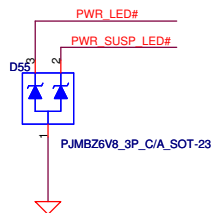
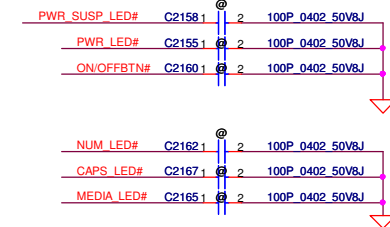
NUM_LED



CAPS_LED

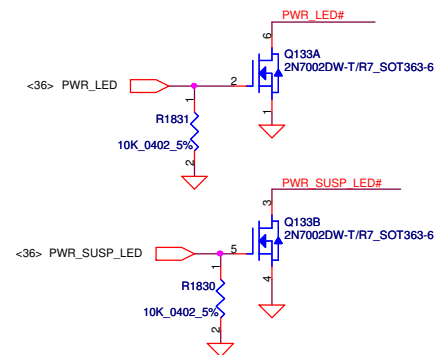
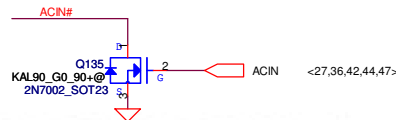
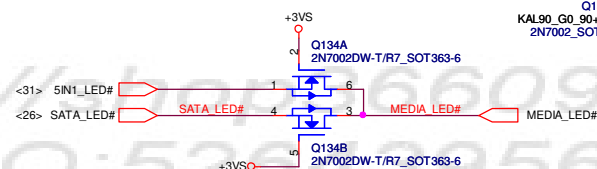


FOR EMI

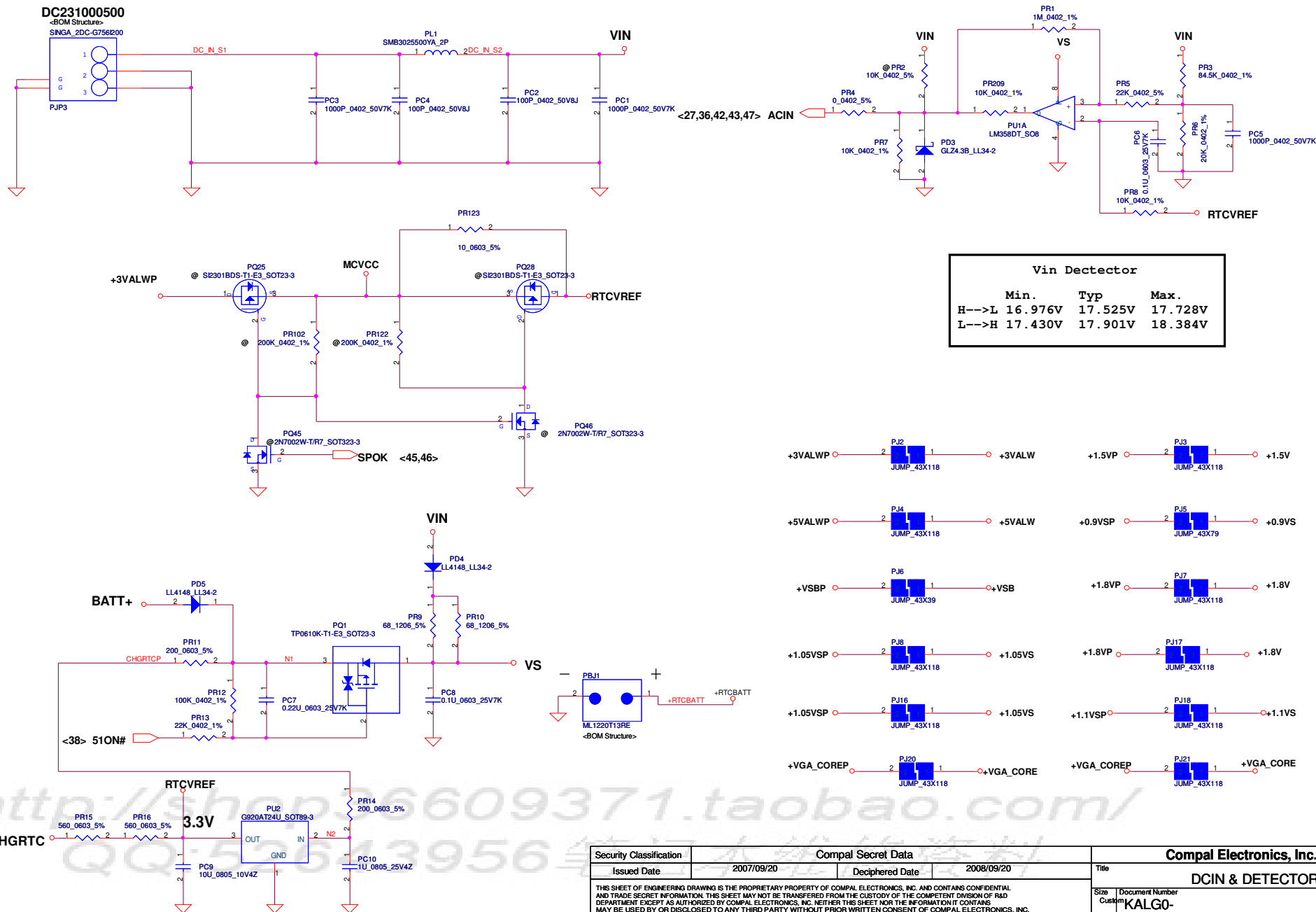


D1 D2 D3 USE PANJIT PJMBZ6V8
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6.8V

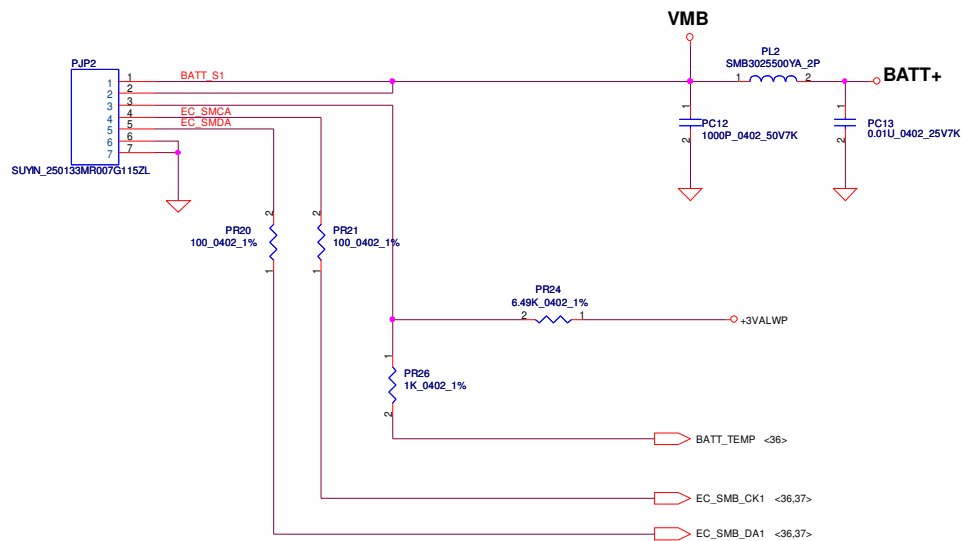
D4 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



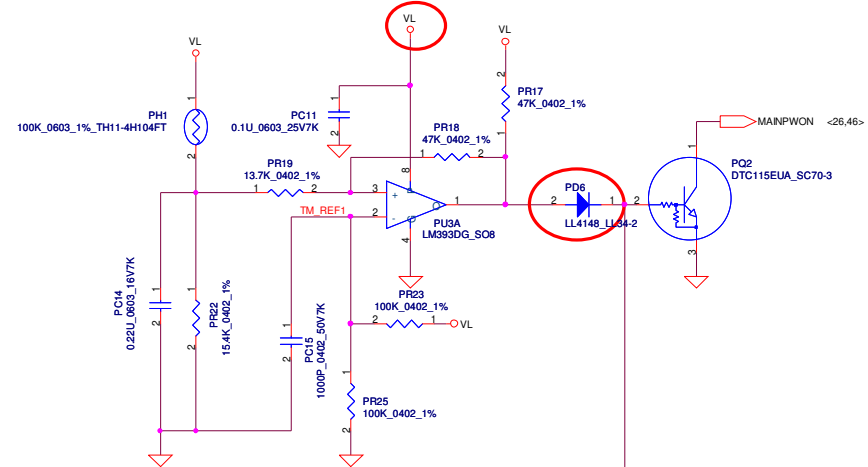
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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Size	Custom	Document Number	KALH0/KALG0/KAL90+	Rev	
Date	Monday, April 27, 2009	Sheet	43	of 53	



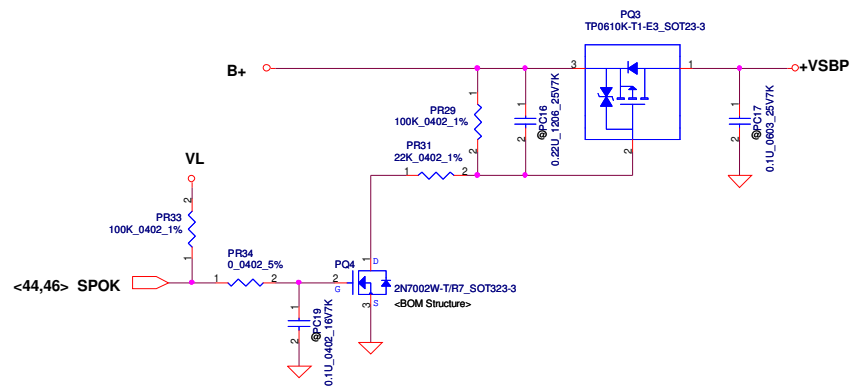
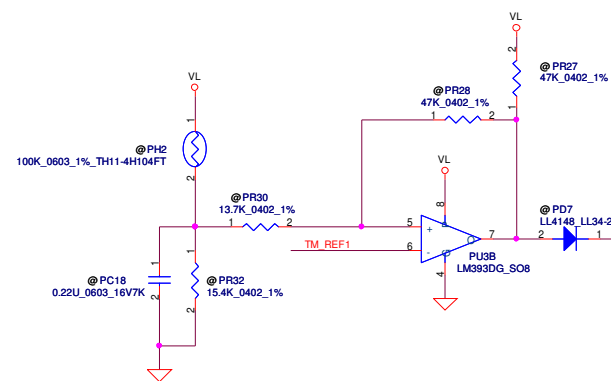
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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Size	Document Number	Rev		0.1	
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PH1 under CPU bottom side :
CPU thermal protection at 96 degree C
Recovery at 60 degree C

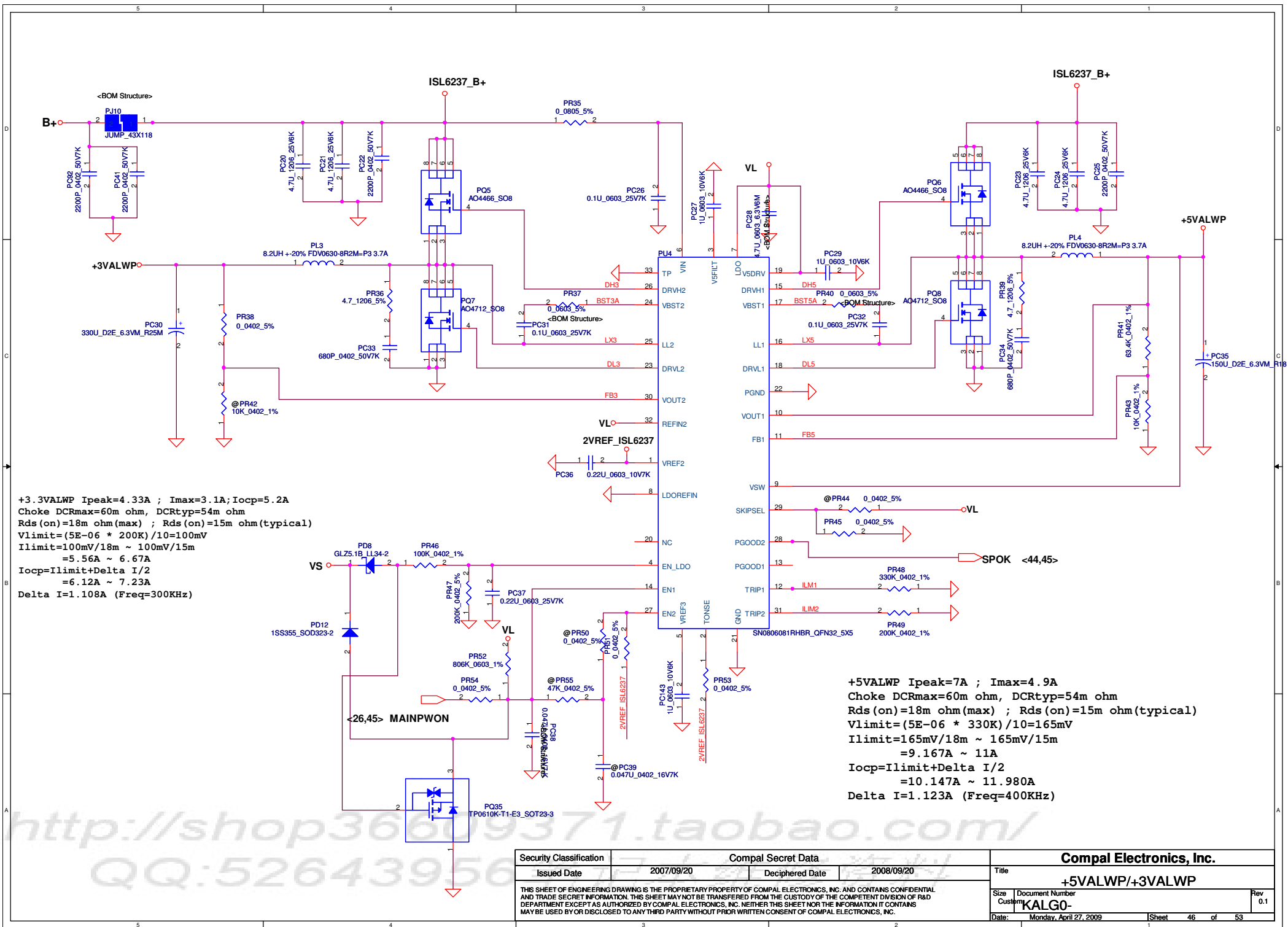


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



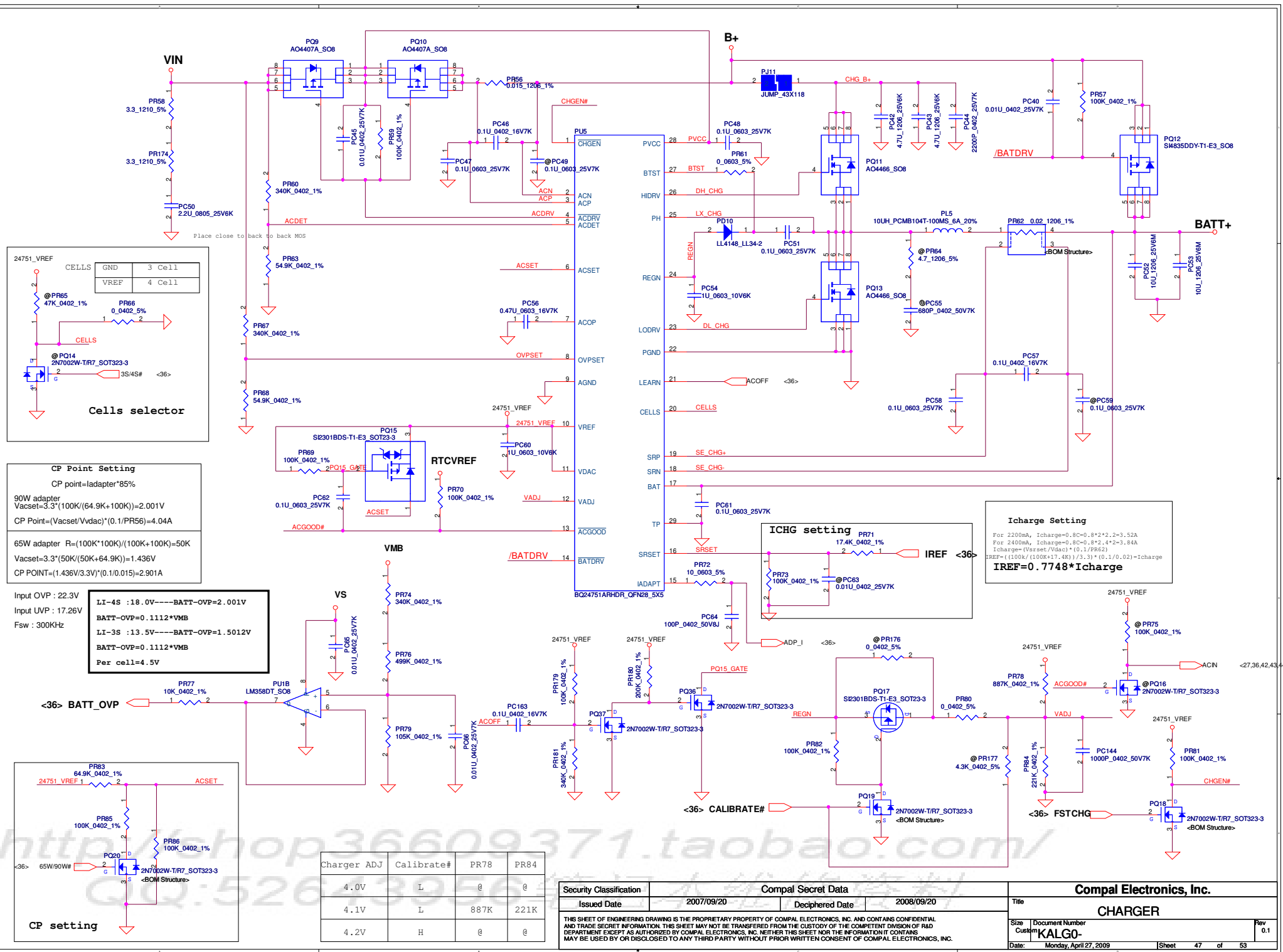
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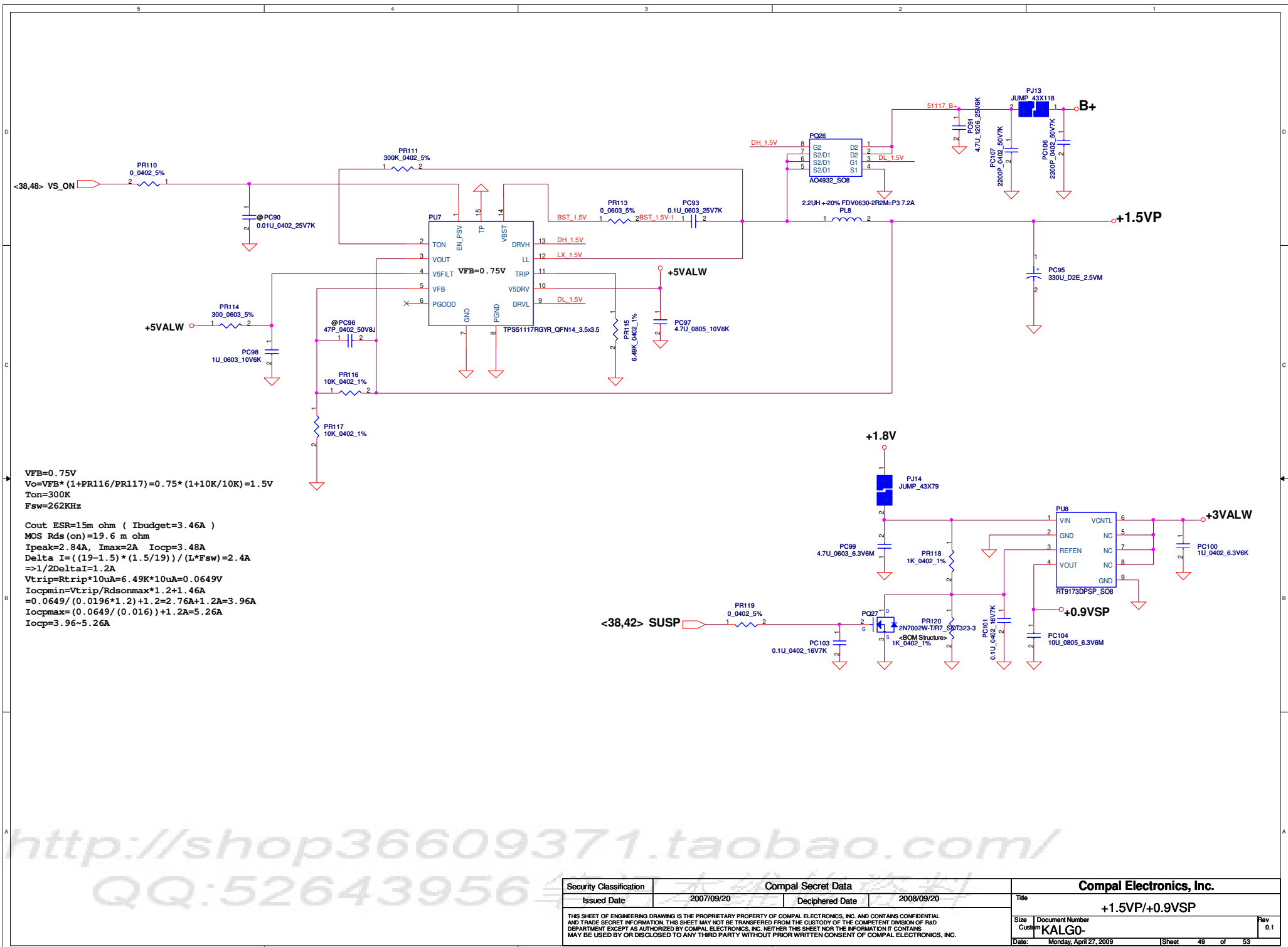
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title
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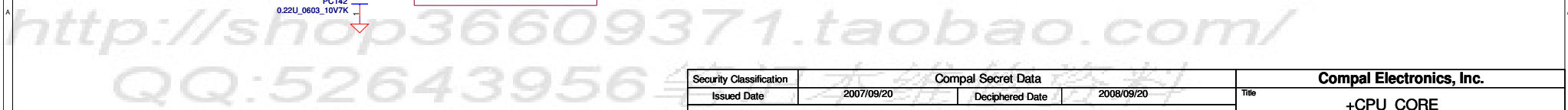


+3.3VALWP Ipeak=4.33A ; Imax=3.1A;Iocp=5.2A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/18m ~ 100mV/15m
=5.56A ~ 6.67A
Iocp=Ilimit+Delta I/2
=6.12A ~ 7.23A
Delta I=1.108A (Freq=300KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.123A (Freq=400KHz)



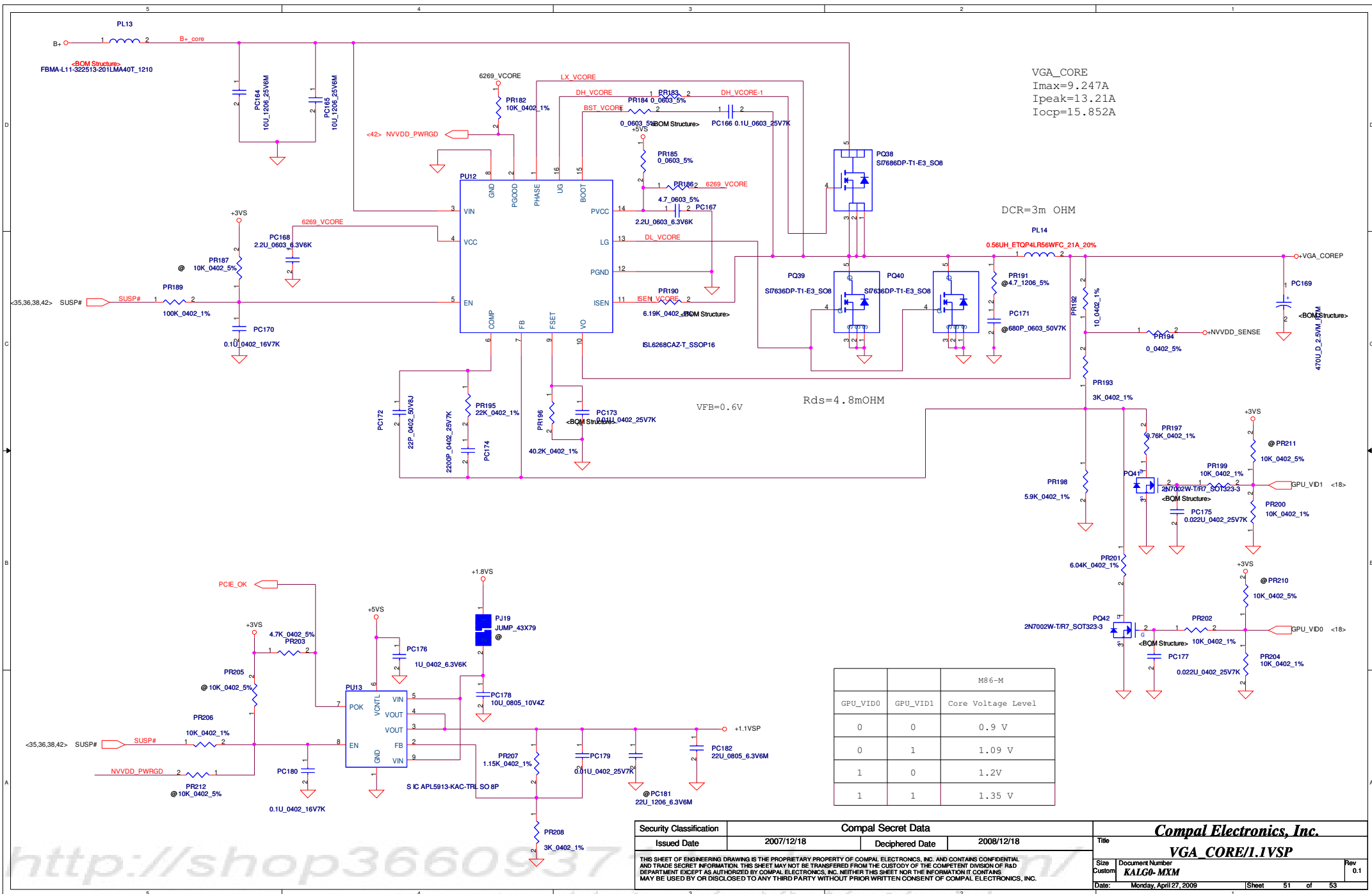




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 Custom: KALGO-

Date: Monday, April 27, 2009 Sheet: 50 of 53



Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR196 value	VGA OCP	0.3	50	change the resistance value of pr196 from 57.6K to 40.2K	2009/02/06	PVT
2	Change PL14 value	prevent OVP occur	0.3	50	change the inductance value of pl14 from 1uH to 0.56 uH	2009/02/06	PVT
3	Change PU4 IC part number	vender suggestion	0.3	45	change part number to SA00002V400	2009/02/06	PVT
4							
5							
6							

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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
				PIR (PWR)	
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B --> C Change List

0220-----
Page 6, Change C98 BOM structure to @

0218-----
Page 20, Add R569 with BOM structure @
Page 23, R34, R38, R40, R53, R54, R55 change BOM structure to @
Page 31, Change R215 to 18K
Update Power Schematics

0213-----
Page 11, Delete R113
Add J1 JUMP_43X79 with BOM structure @
Page 31, R558, R559 0 ohm with BOM structure @
R560, R561 4.7K with BOM structure @
Page 32, R562, R563 0 ohm with BOM Structure @
R564, R565 0 ohm
Page 38, Delete C619
Add R566, R567, R568 0_0603 with BOM Structure JAL90@

0204-----
Page 12, Change L31 to MBK1608301YZF_0603 with BOM structure GM@
Change R163 to 0_0805_5%
Page 23, Change BOM Structure of U5 to @
Page 27, Change BOM Structure of R555 and R550 to @
Page 33, Change R217 to 31.6K_0402_1%
Change C313 to 1U_0603_10V6K
Page 34, Change R503 to FBMA-L10-160808-301LMT_0603

01/31-----
Page 23, Delete U10

01/29-----
Page 23, Change R152 BOM Structure to @

01/24-----
Page 4, Change U8 to SA00001Z700 (EMC1402)
Page 33, Change C338 to SE076104K80
Page 35, Mount C584

01/23-----
Page 38 Delete F3, R558~560, C609~614

01/22-----
Page 11, Delete R79
Change J1 Symbol to JUMP_43X79
Page 33, Add R557 10K (Check)
Change R245 BOM Structure with @
Page 38, Add C609~614, R558~560 (Check)
C607,608, 615~619 (Check)

01/17-----
Page 11, Add R79 0_0805
Update Power Schematics

01/16-----
Page 11, Delete R79 0_0805
Add J1 JUMP_43X79
Page 16, Change C296, R301 to 27P_0402
Page 19, Change L17, L19, L21 BOM structure to GM@
Page 23, Mount U29, R339
Add U10 with BOM structure @ (Co-lay with U5)
Change R340 Bom structure to @
Change U5 to MX25L4005AMC-12G_SO8 (SA00002A900)

Page 27, Change U26, C420 BOM structure to @
Change R550 to 0_0402
Add R555 0_0402
Page 32, Change R269 to 240_0402_5%, R267 to 453_0402_1%
Change R268 pin1 connect to +5VALW
Page 33, Change R217 to 18K_0402_1% with BOM structure PM@
Page 35, Add R551,R552, R553, R554 75_0603_1% with BOM structure JAL90@
Add D32 PJDLC05_SOT23-3

Page 38, Add F3 3A_15VDC_SMD2920P300TF/15
Page 49, Add R551,R552, R553, R554 1K_0603_1% with BOM structure 268@
Add L17, L19, L21 0_0805 with BOM structure PM@
Update U38 (ALC268-VB1-GR) PN:SA00001GD10 for JAW50

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