

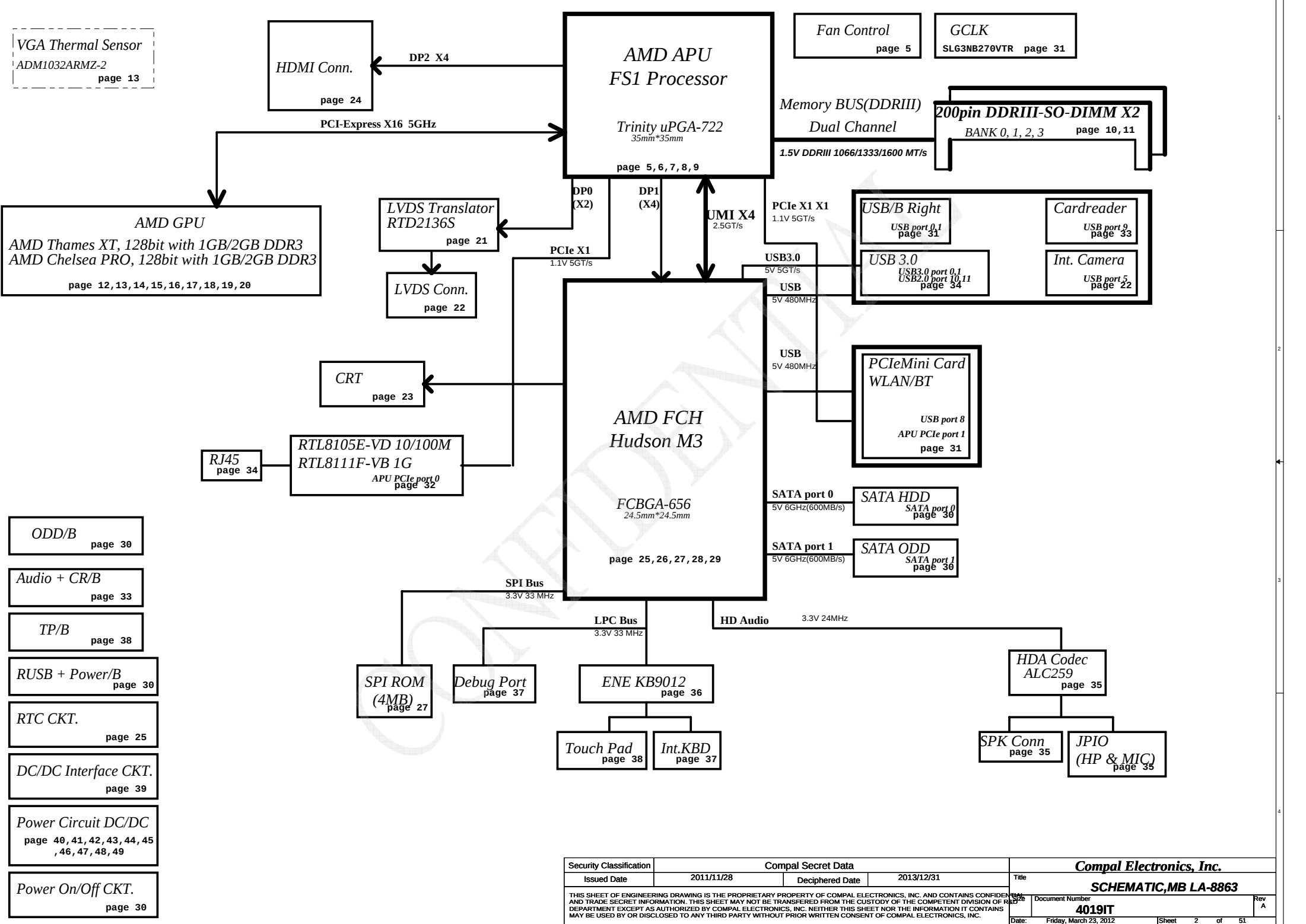
QMLE4/5

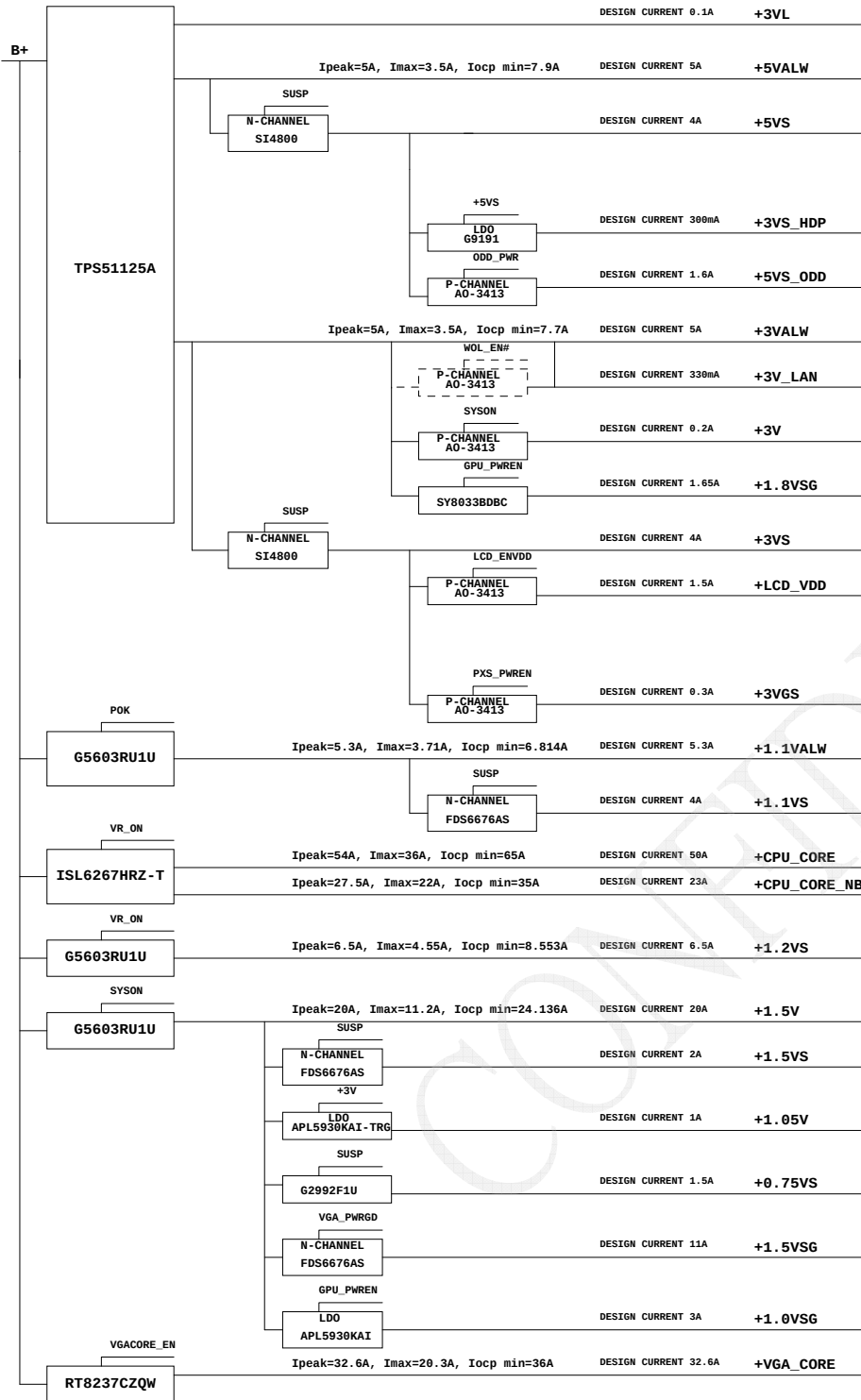
Eureka Discrete

LA-8863P REV 0.3 Schematic

**AMD Trinity APU / Hudson M3 FCH
Thames XT & Chelsea PRO
2012-03-13 Rev 0.3**

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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VGS +1.8VSG +1.5VSG +1.0VSG
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress		COMMON		UMA	PowerXpress	Discrete
BTO	IHDMI@		HDMI@		UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function	MINI PCI-E SLOT	LAN				
description		LAN				
explain		10/100M		GIGA		
BTO		8105ELD0@	8105ESWR@	8111E@		

Function		Cam & Mic	Panel			
description		Cam & Mic	Panel (DIS@)			
explain		Cam & Mic				
BTO		CAM@				

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		FCH			
description	PowerXpress		FCH			
explain	BACO mode	Non-BACO	Hudson-M2	Hudson-M3		
BTO	BACO@	NOBACO@	M2@	M3@		

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	90 H	1001 000xb
+3VS	DDR SO-DIMM 1	92 H	1001 001xb
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011x b
+3VL	Charger IC	12 H	0001 001x b
EC SM Bus3 Address			
+3VS	LVDS EEPROM	A8 H	1010 1000 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	APU Thermal Sensor	98 H	1001 100x b
+3VS	GPU Internal Thermal	82 H	1000 001x b
+3VS	GPU External Thermal	9A H	1001 101x b
+3VS	GPU External Thermal	9A H	1001 101x b

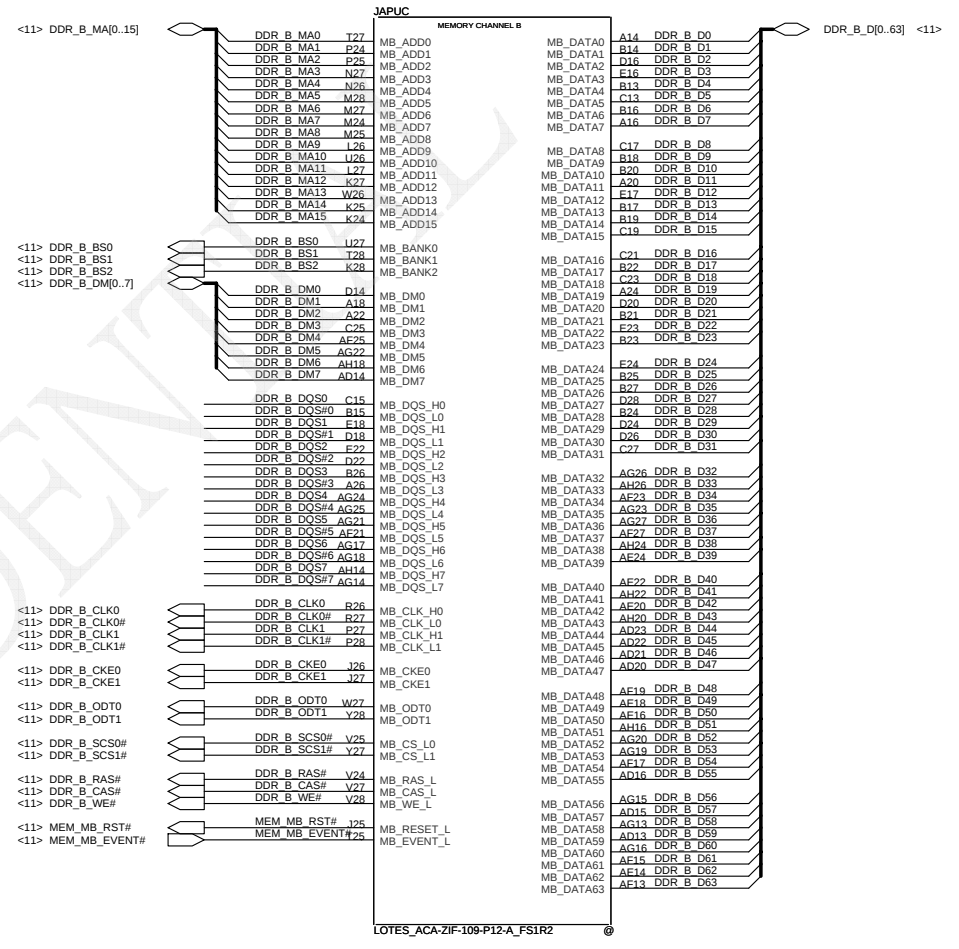
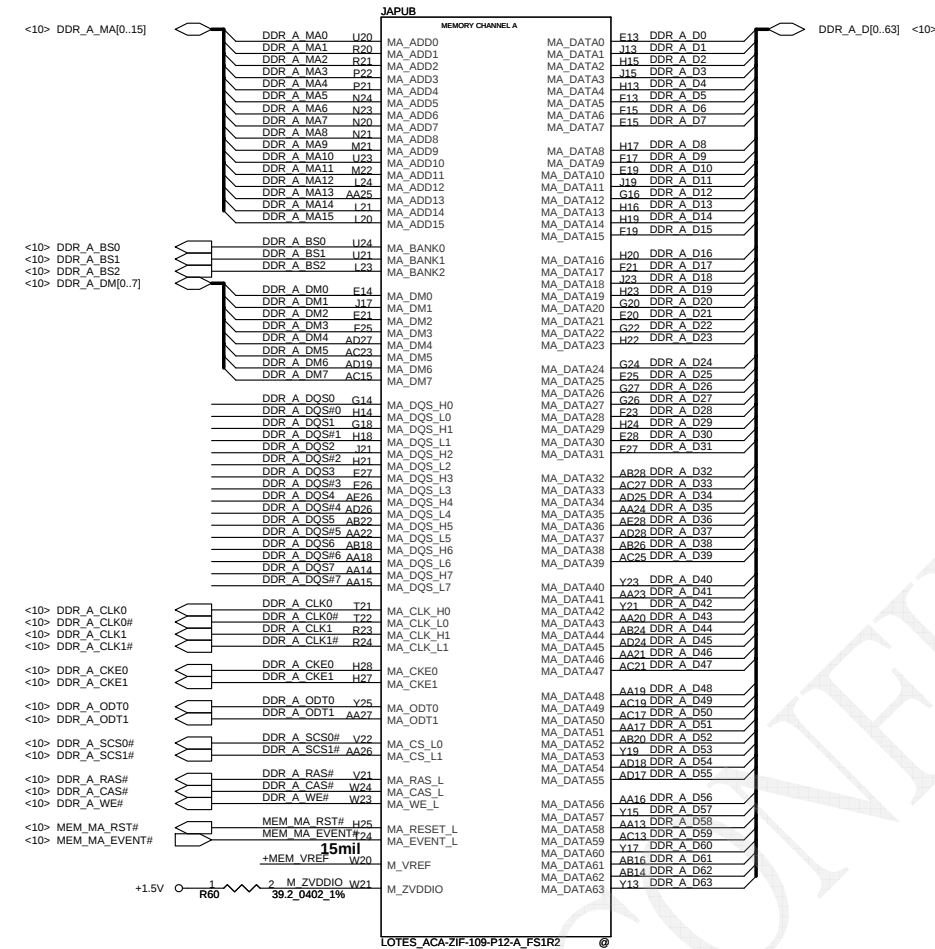
STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

<10> DDR_A_DQS[0..7]

<10> DDR_A_DQS# [0..7]

<11> DDR_B_DQS[0..7]

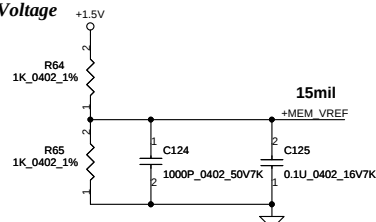
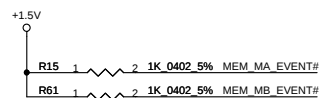
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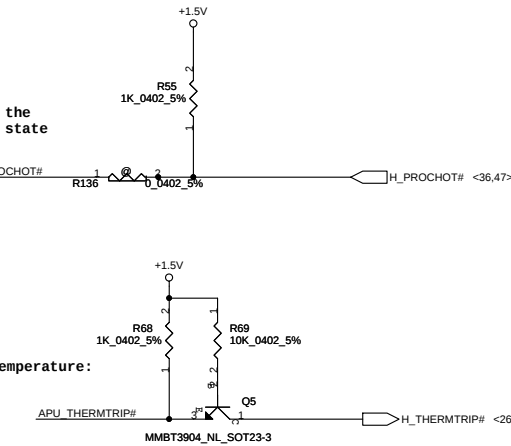
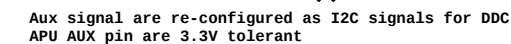
LOTES_ACA-ZIF-109-P12-A_FS1R2

EVENT# pull high

0.75V Reference Voltage

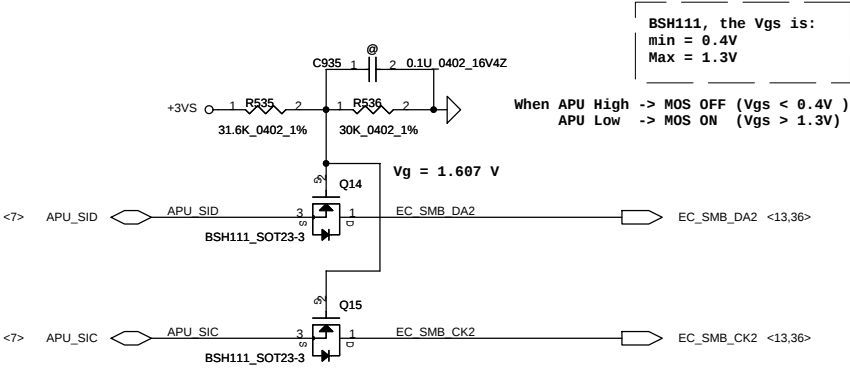


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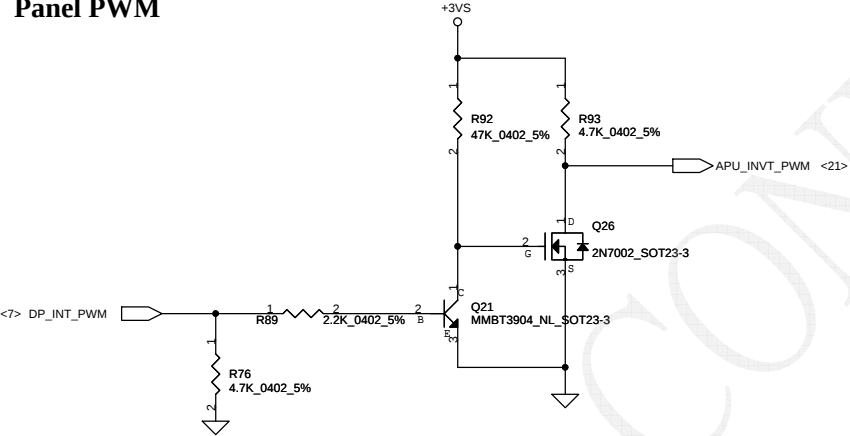


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CPU TSI interface level shift

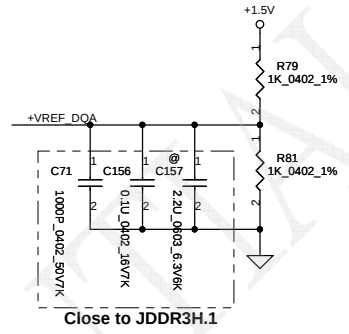
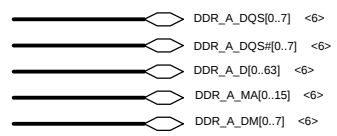
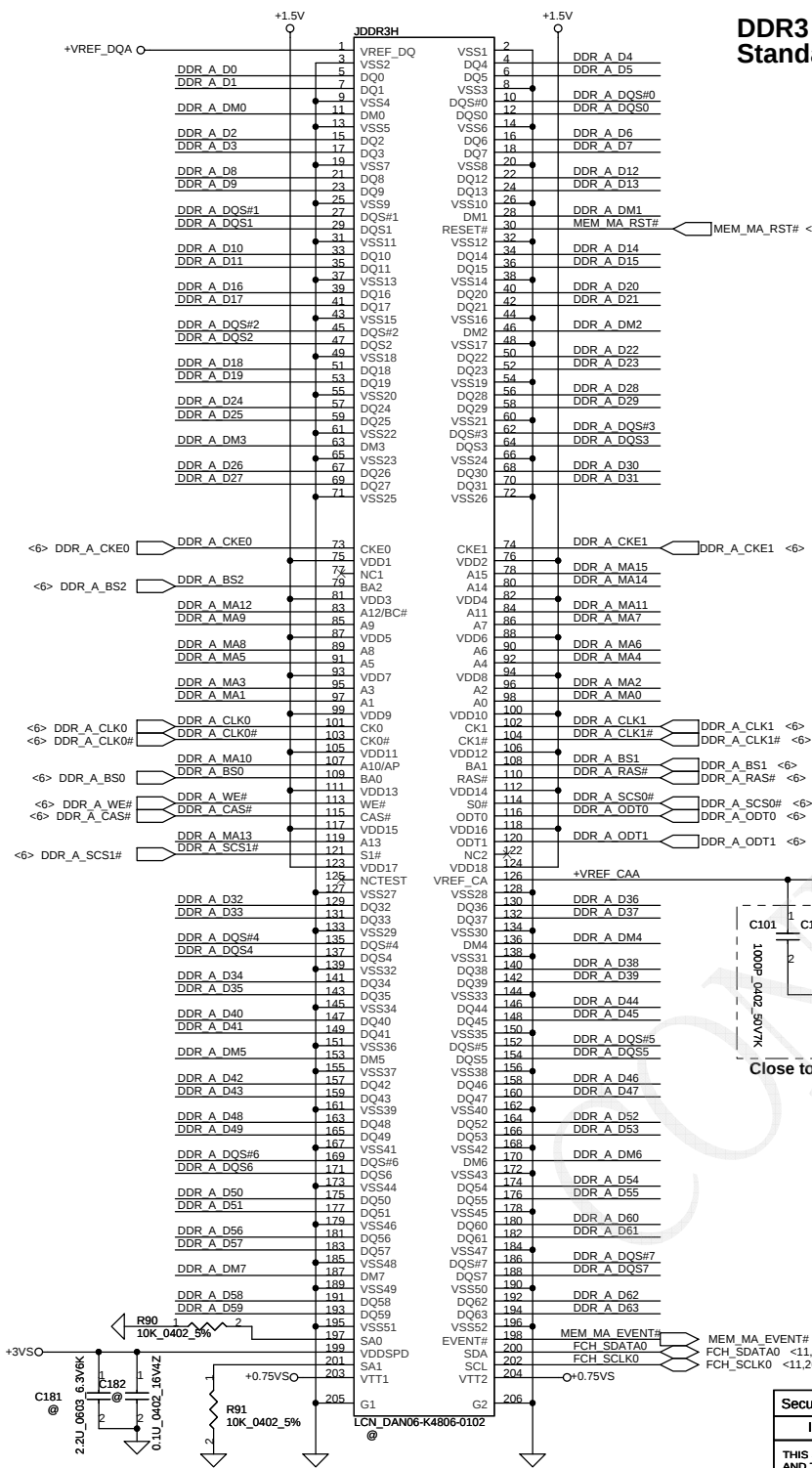


Panel PWM

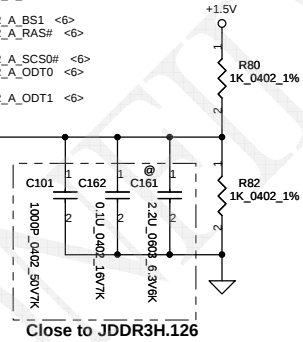
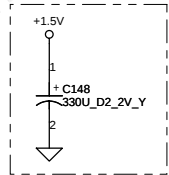


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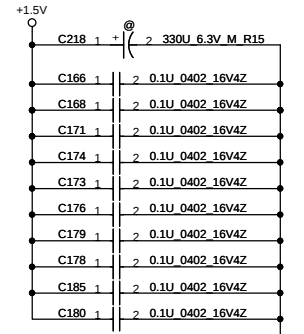
DDR3 SO-DIMM A Standard Type



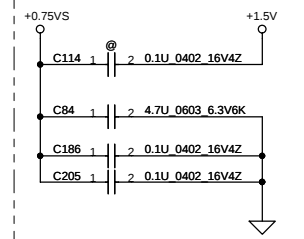
Co-layout with C218 on PVT



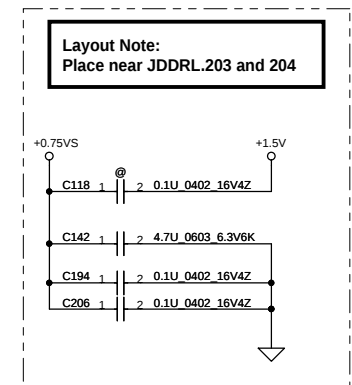
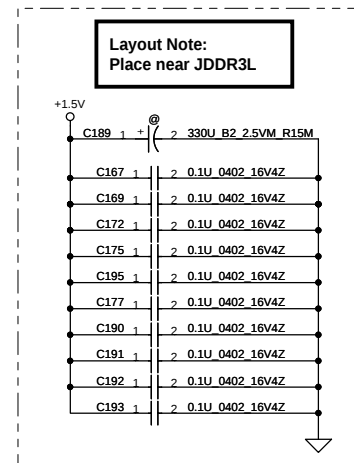
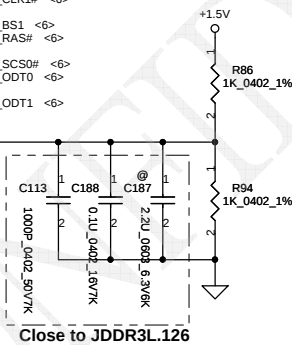
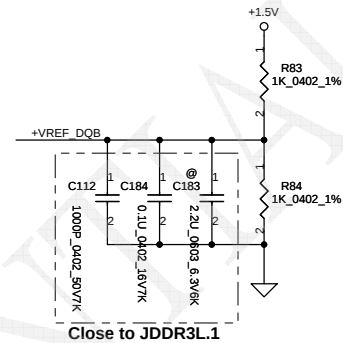
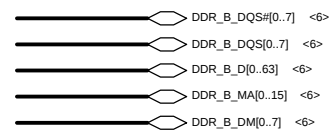
Layout Note:
Place near JDDR3H



Layout Note:
Place near JDDR3H.203 and 204



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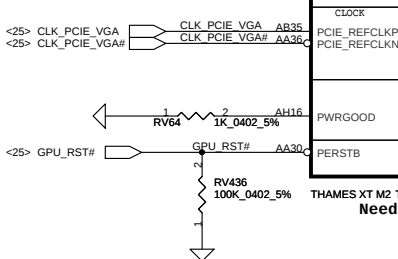
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PCIE GTX C CRX P[0..15] PCIE GTX_C_CRX_P[0..15] <5>
PCIE GTX C CRX N[0..15] PCIE GTX_C_CRX_N[0..15] <5>

Close to UV1

PCIE_CTX_C_GRX_P0 AA38	PCIE_CTX_C_GRX_N0 Y37	PCIE_TX0P	Y33 PCIE GTX CRX P0 0.1U 0402 16V7K 2 1 CV73	PCIE GTX C CRX P0
PCIE_CTX_C_GRX_P1 Y35	PCIE_CTX_C_GRX_N1 W36	PCIE_TX0N	Y32 PCIE GTX CRX N0 0.1U 0402 16V7K 2 1 CV74	PCIE GTX C CRX N0
PCIE_CTX_C_GRX_P2 W38	PCIE_CTX_C_GRX_N2 V37	PCIE_TX1P	W33 PCIE GTX CRX P1 0.1U 0402 16V7K 2 1 CV71	PCIE GTX C CRX P1
PCIE_CTX_C_GRX_P3 V35	PCIE_CTX_C_GRX_N3 U36	PCIE_TX1N	W32 PCIE GTX CRX N1 0.1U 0402 16V7K 2 1 CV72	PCIE GTX C CRX N1
PCIE_CTX_C_GRX_P4 U38	PCIE_CTX_C_GRX_N4 T37	PCIE_TX2P	U33 PCIE GTX CRX P2 0.1U 0402 16V7K 2 1 CV69	PCIE GTX C CRX P2
PCIE_CTX_C_GRX_P5 T35	PCIE_CTX_C_GRX_N5 R36	PCIE_TX2N	U32 PCIE GTX CRX N2 0.1U 0402 16V7K 2 1 CV70	PCIE GTX C CRX N2
PCIE_CTX_C_GRX_P6 R38	PCIE_CTX_C_GRX_N6 P37	PCIE_TX3P	U30 PCIE GTX CRX P3 0.1U 0402 16V7K 2 1 CV67	PCIE GTX C CRX P3
PCIE_CTX_C_GRX_P7 P35	PCIE_CTX_C_GRX_N7 N36	PCIE_TX3N	U29 PCIE GTX CRX N3 0.1U 0402 16V7K 2 1 CV68	PCIE GTX C CRX N3
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PCIE_CTX_C_GRX_P9 M35	PCIE_CTX_C_GRX_N9 L36	PCIE_TX4N	T32 PCIE GTX CRX N4 0.1U 0402 16V7K 2 1 CV66	PCIE GTX C CRX N4
PCIE_CTX_C_GRX_P10 L38	PCIE_CTX_C_GRX_N10 K37	PCIE_TX5P	T30 PCIE GTX CRX P5 0.1U 0402 16V7K 2 1 CV63	PCIE GTX C CRX P5
PCIE_CTX_C_GRX_P11 K35	PCIE_CTX_C_GRX_N11 J36	PCIE_TX5N	T29 PCIE GTX CRX N5 0.1U 0402 16V7K 2 1 CV64	PCIE GTX C CRX N5
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		PCIE_TX8P	N33 PCIE GTX CRX P8 0.1U 0402 16V7K 2 1 CV57	PCIE GTX C CRX P8
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		PCIE_TX9P	N30 PCIE GTX CRX P9 0.1U 0402 16V7K 2 1 CV55	PCIE GTX C CRX P9
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		PCIE_TX11P	L30 PCIE GTX CRX P11 0.1U 0402 16V7K 2 1 CV51	PCIE GTX C CRX P11
		PCIE_TX11N	L29 PCIE GTX CRX N11 0.1U 0402 16V7K 2 1 CV52	PCIE GTX C CRX N11
		PCIE_TX12P	K33 PCIE GTX CRX P12 0.1U 0402 16V7K 2 1 CV49	PCIE GTX C CRX P12
		PCIE_TX12N	K32 PCIE GTX CRX N12 0.1U 0402 16V7K 2 1 CV50	PCIE GTX C CRX N12
		PCIE_TX13P	J33 PCIE GTX CRX P13 0.1U 0402 16V7K 2 1 CV47	PCIE GTX C CRX P13
		PCIE_TX13N	J32 PCIE GTX CRX N13 0.1U 0402 16V7K 2 1 CV48	PCIE GTX C CRX N13
		PCIE_TX14P	K30 PCIE GTX CRX P14 0.1U 0402 16V7K 2 1 CV45	PCIE GTX C CRX P14
		PCIE_TX14N	K29 PCIE GTX CRX N14 0.1U 0402 16V7K 2 1 CV46	PCIE GTX C CRX N14
		PCIE_TX15P	H33 PCIE GTX CRX P15 0.1U 0402 16V7K 2 1 CV43	PCIE GTX C CRX P15
		PCIE_TX15N	H32 PCIE GTX CRX N15 0.1U 0402 16V7K 2 1 CV44	PCIE GTX C CRX N15

PCI EXPRESS INTERFACE



Chelsea Only

RV198 1.69K 0402 1% CH@

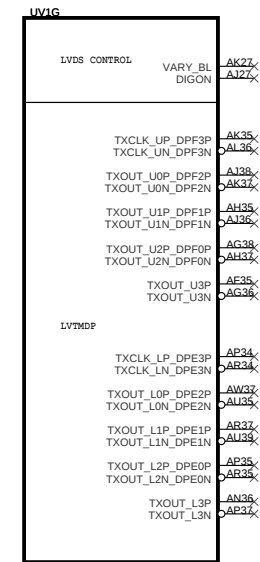
Thames Only

RV63 1.27K 0402 1% TH@

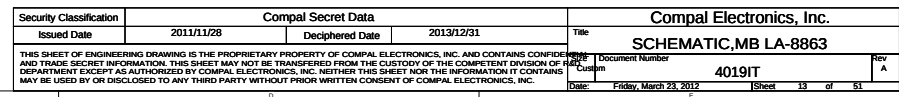
RV65 2K 0402 1% TH@

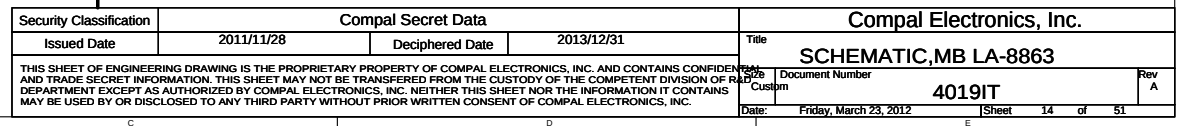
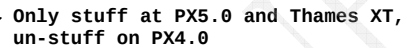
Install 2K for Thames/Seymour

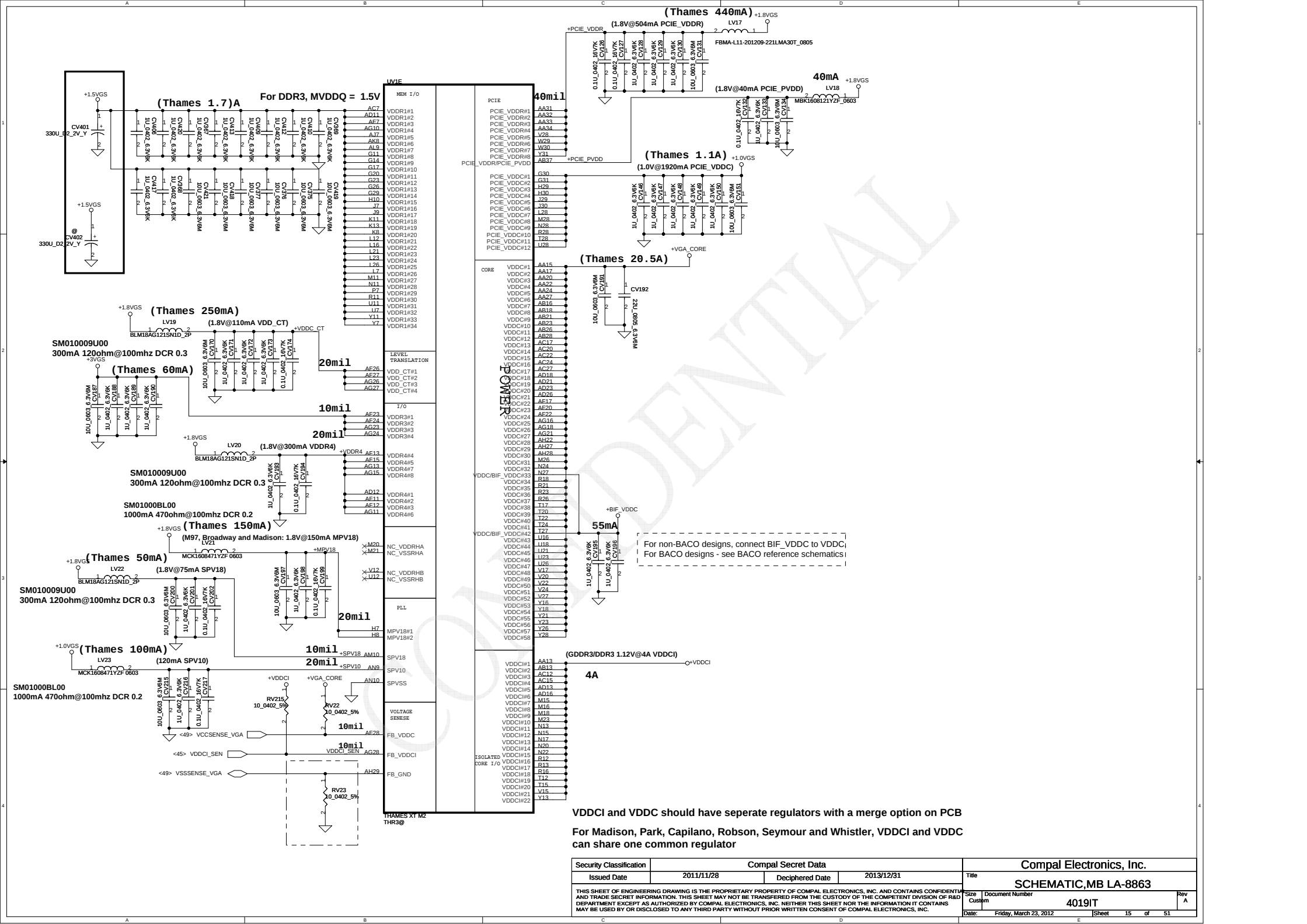
LVDS Interface

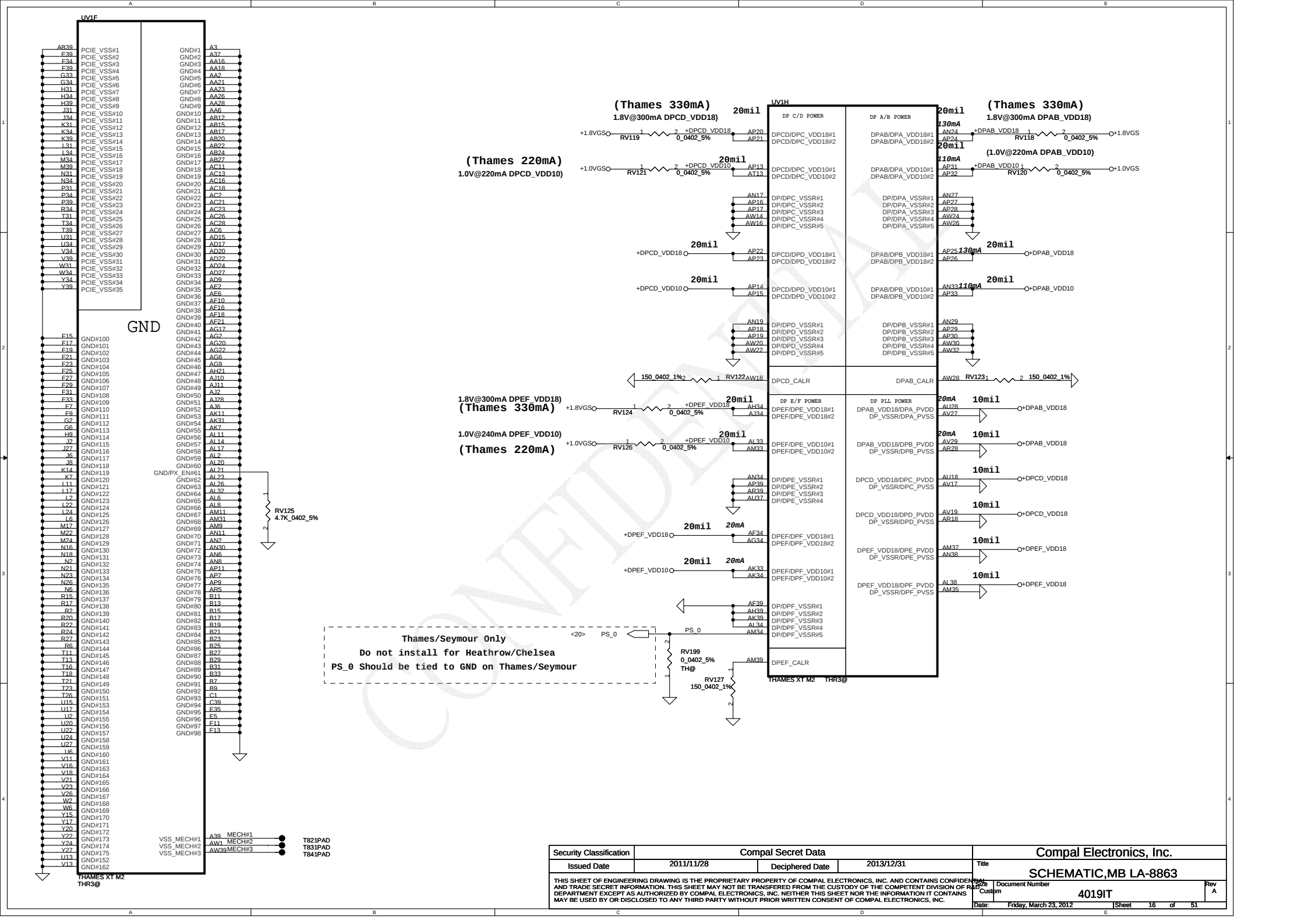


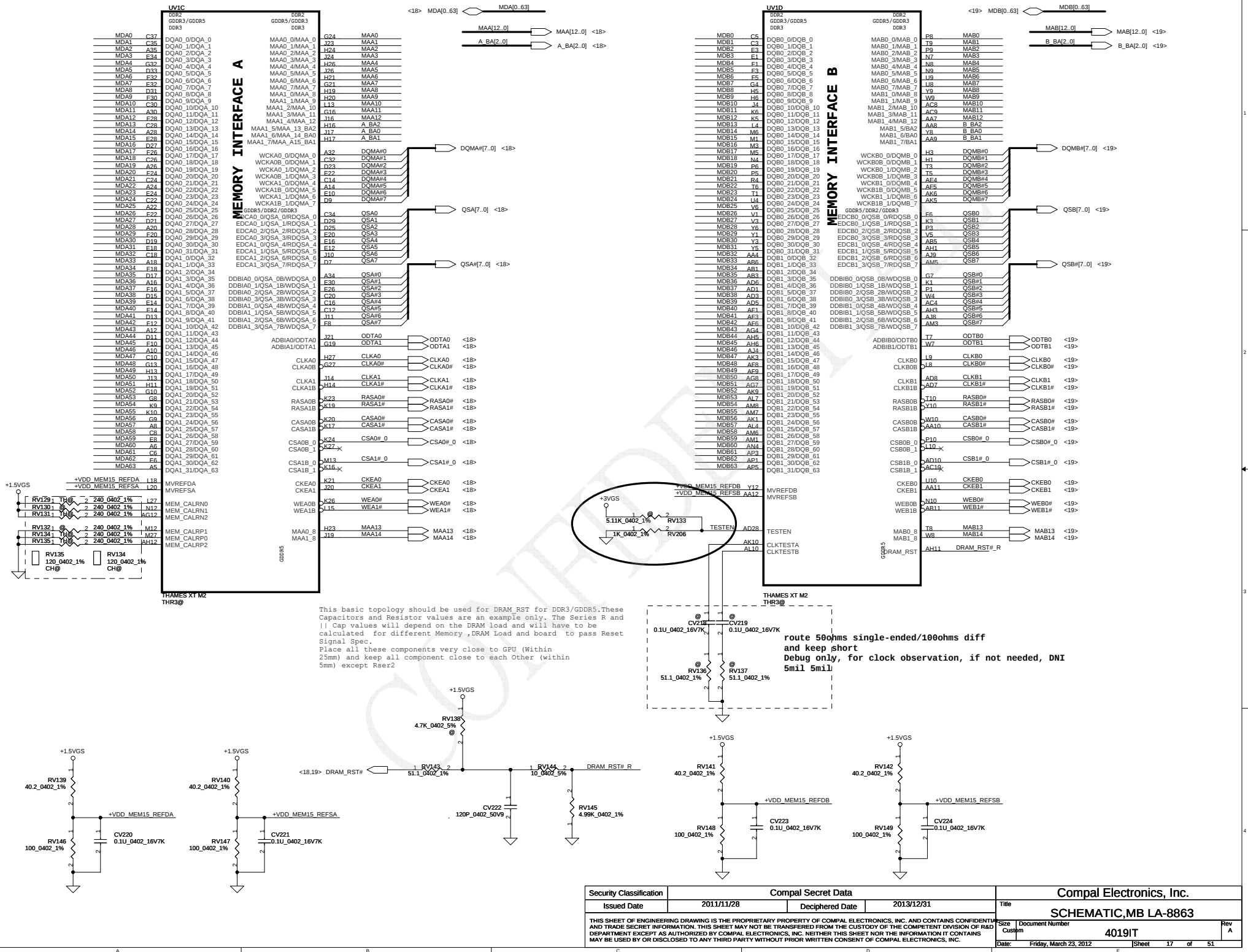
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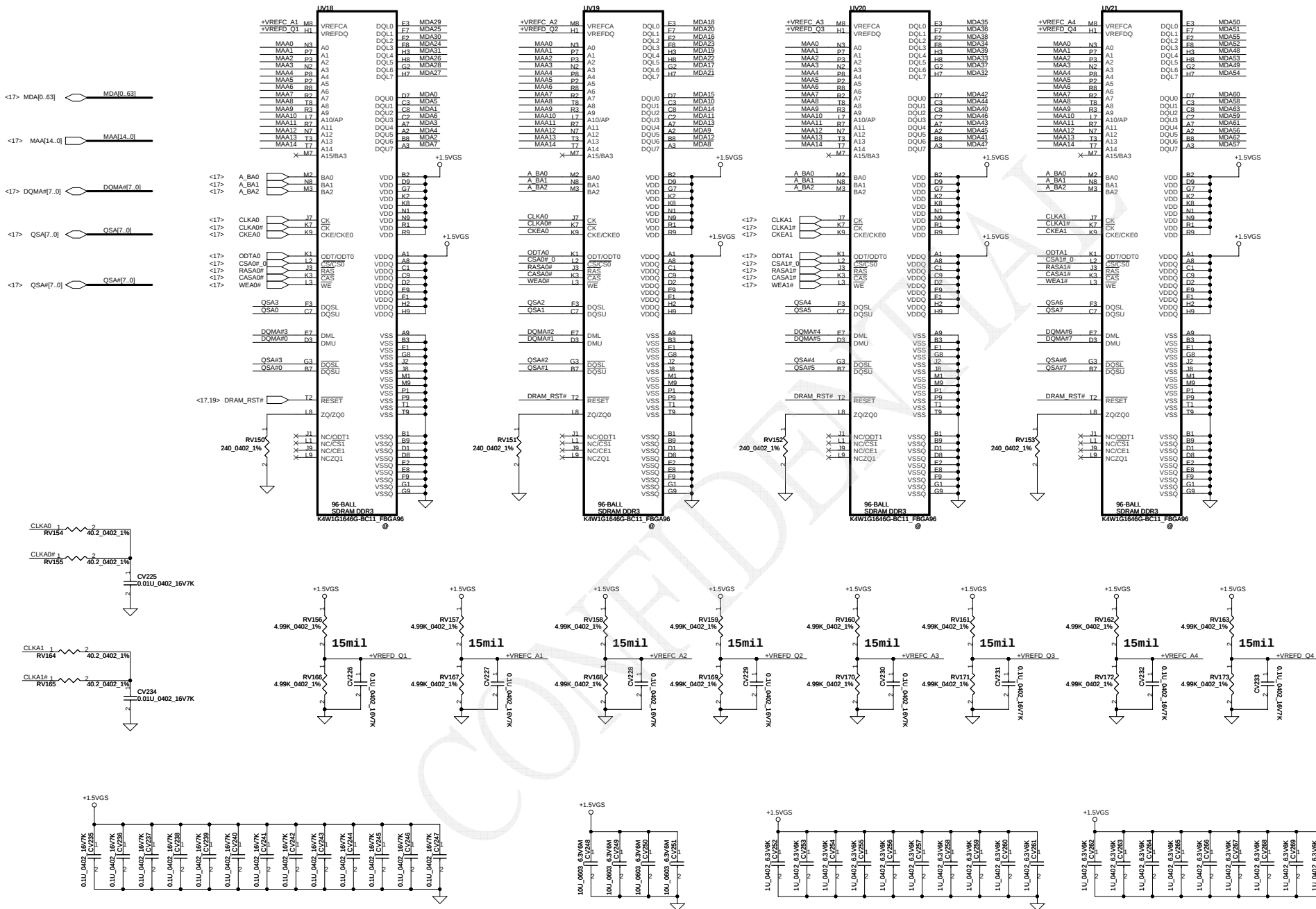






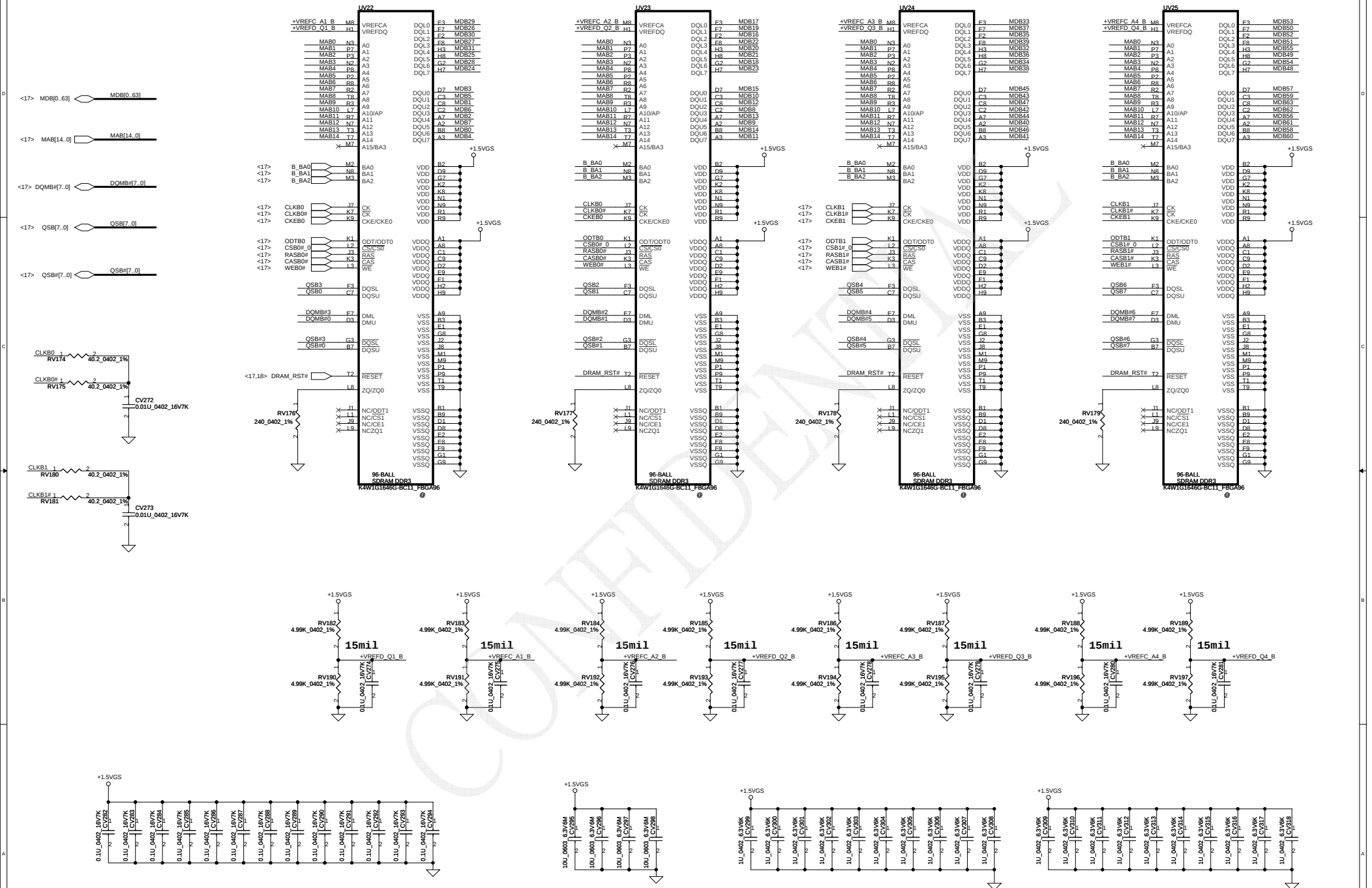


CHANNEL A: 512MB/1024MB DDR3



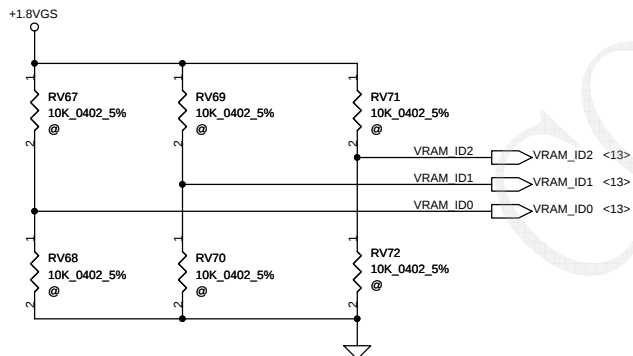
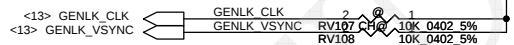
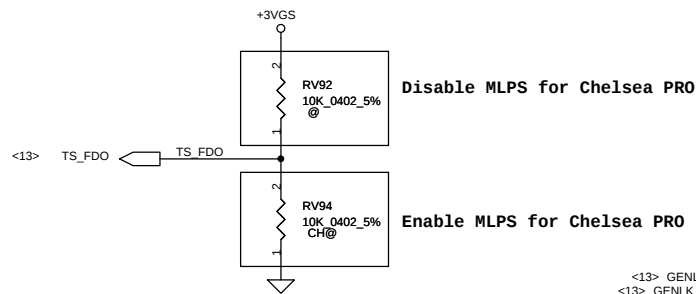
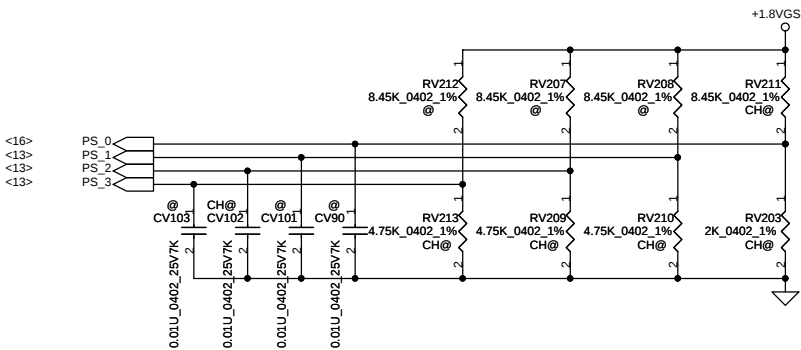
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CHANNEL B: 512MB/1024MB DDR3



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				Size C Document Number Rev A	
				4019TT	
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	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0	1 1	0 0 1	NC	8.45k	2k
PS_1	1 1	0 0 0	NC	NC	4.75k
PS_2	0 0	0 0 0	680 nF	NC	4.75k
PS_3	1 1	0 0 0	NC	NC	4.75k



VRAM Straps

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (1G)	H5TQ1G63DFR-11C Hynix 1GB SA000041S20	RV68 0	RV70 0	RV72 0
*64MX16 (1G)	R4W1G1646G-BC11 Samsung 1GB SA00004GS00	RV67 1	RV70 0	RV72 0
128M16 (2G)	H5TQ2G63BFR-11C Hynix 2GB SA00003YO00	RV68 0	RV69 1	RV72 0
*128M16 (2G)	R4W2G1646C-BC11 Samsung 2GB SA000047Q00	RV67 1	RV69 1	RV72 0

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

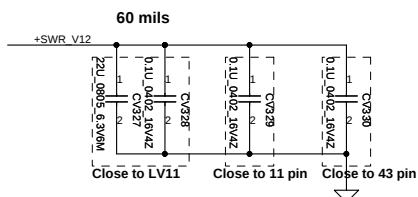
MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select 256MB: 0 0 1	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsea PRO)	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO2	PCIe Gen3 capability 0: 2.5GT/s 1: 5GT/s	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO8	PCIe clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsea PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIe full TX output swing 0: Half swing 1: Full swing	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enable 0: Disable 1: Enable	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM 0: Disable 1: Enable	0
PS_2[4]	VGA_DIS	GPIO9	VGA disable 0: Enable 1: Disable	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]			
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]			
AUD[1] AUD[0]	HSYNC VSYNC			
			AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0

AMD RESERVED CONFIGURATION STRAPS

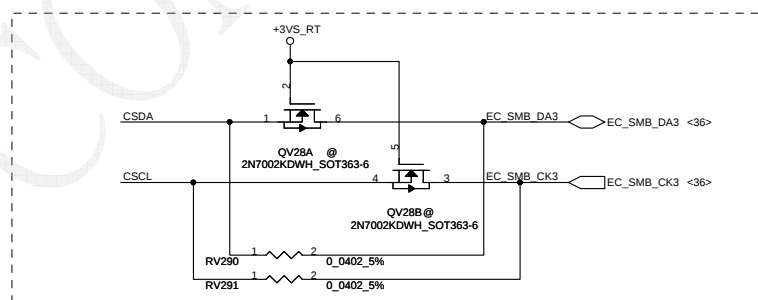
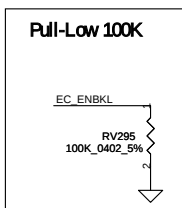
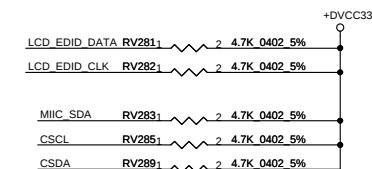
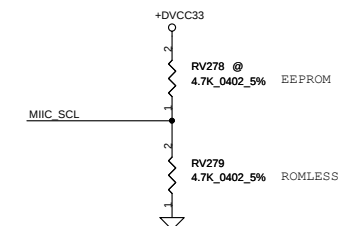
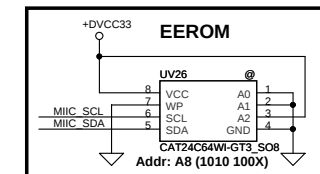
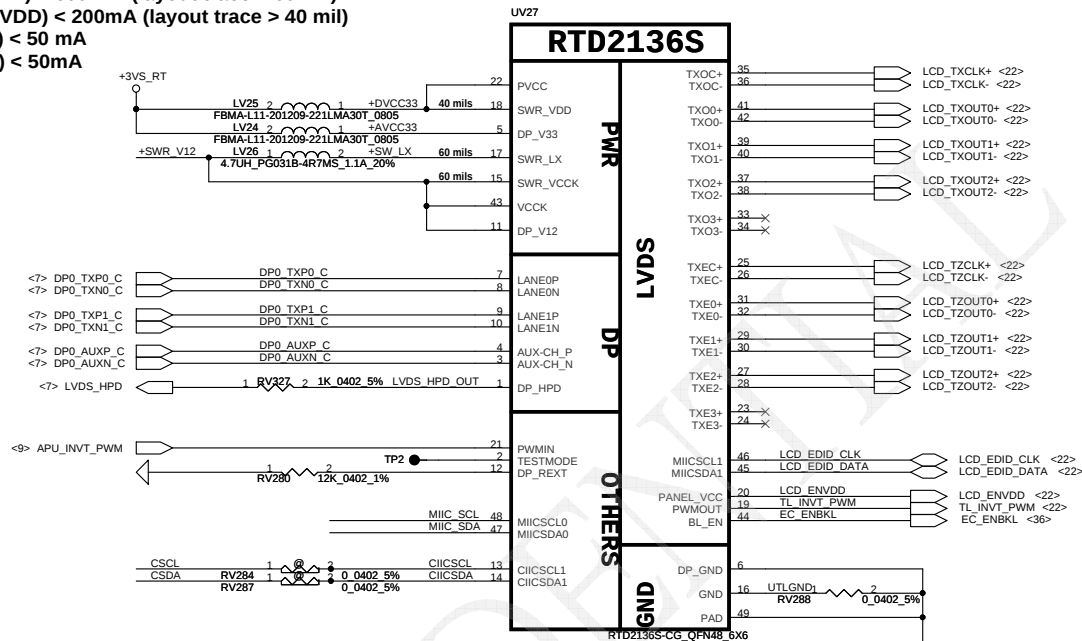
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

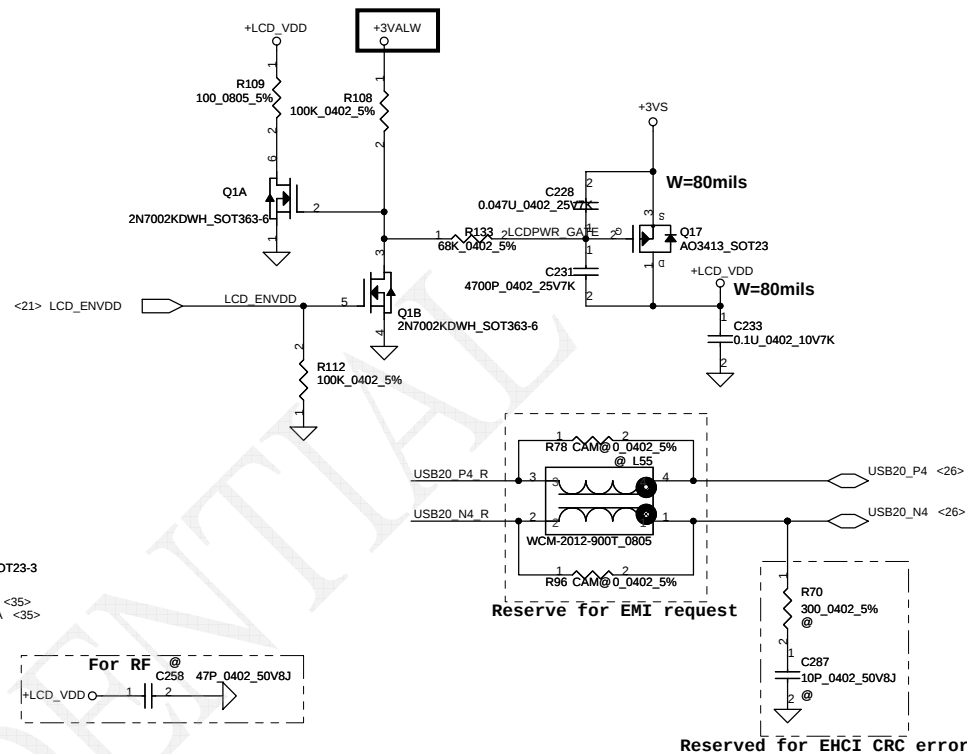
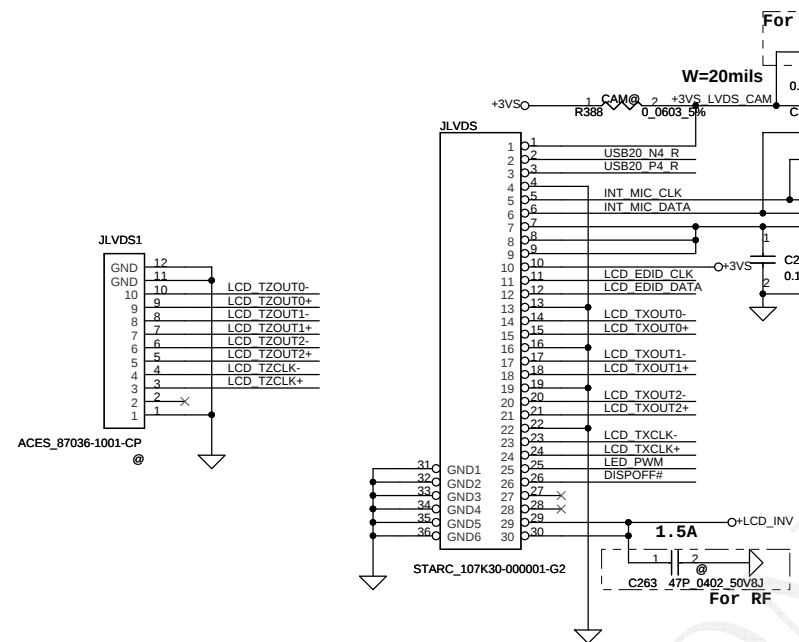
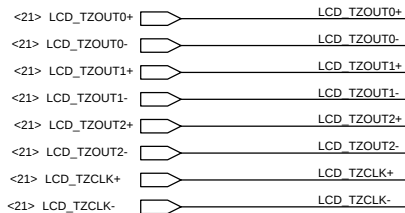
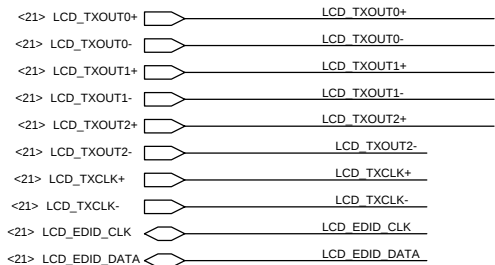
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- Pin5 (DPV33) < 20mA
- Pin 11 (DPV12) < 100mA
- Pin 15 (SWR_VCCX) < 100mA (layout trace > 60 mil)
- Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
- Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
- Pin 22 (PVCC) < 50 mA
- Pin 43 (VCCK) < 50mA

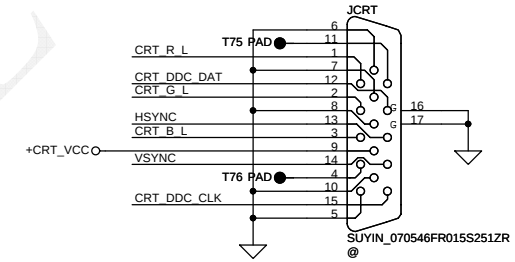
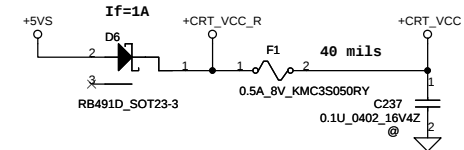


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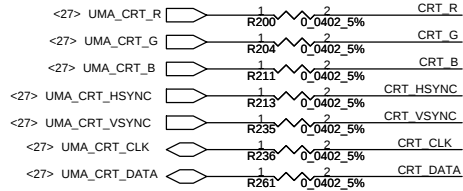


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CRT CONNECTOR

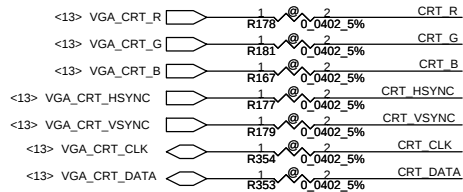


For PowerXpress

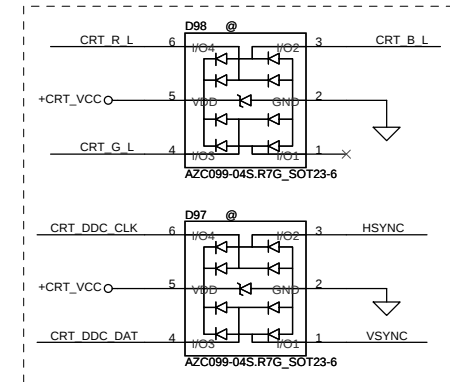
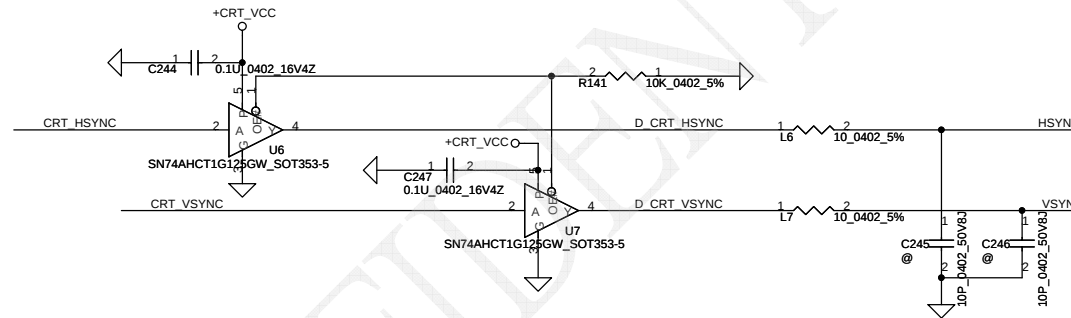
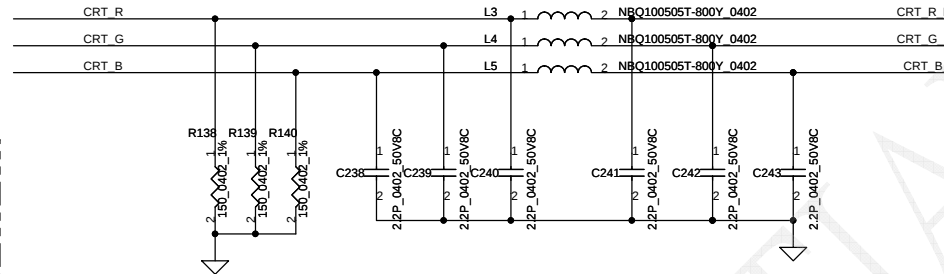


Close to CRT Connector

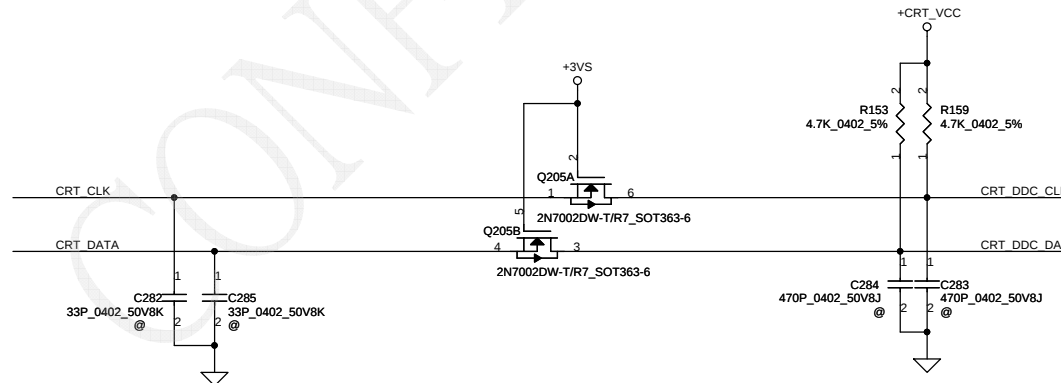
For Debug



Close to CRT Connector



2/9: Add for ESD request

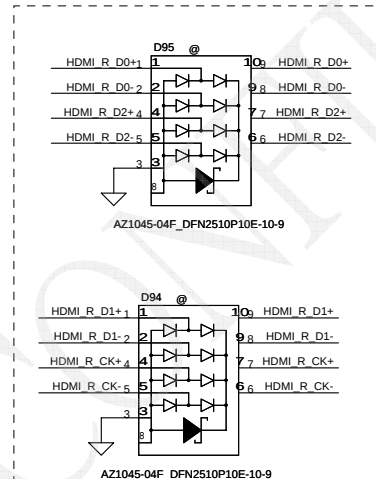
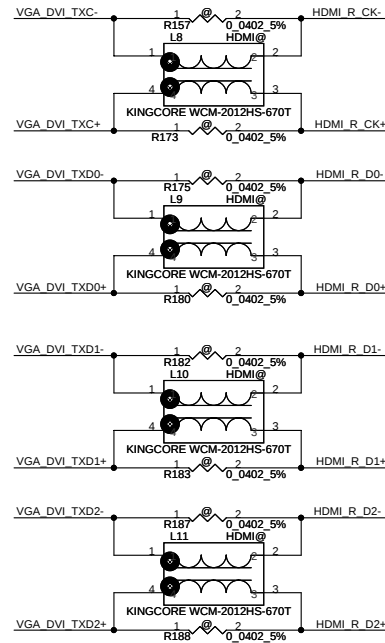
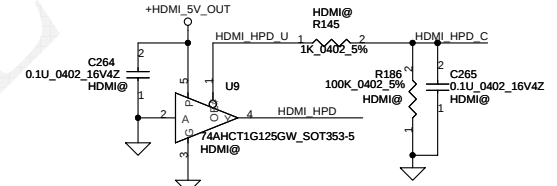
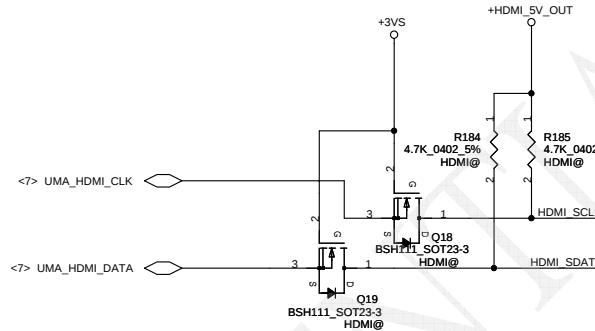


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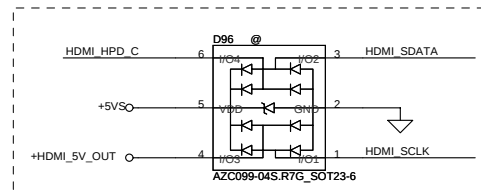
OE#	A	Y
L	L	L
L	H	H
H	X	Z

Change R184 and R185 from 2K to 4.7K
for HDMI detect issue on preMP

<7> UMA_HDMI_TXC+	C310	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXC+
<7> UMA_HDMI_TXC-	C321	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXC-
<7> UMA_HDMI_TX0+	C326	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD0+
<7> UMA_HDMI_TX0-	C313	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD0-
<7> UMA_HDMI_TX1+	C309	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD1+
<7> UMA_HDMI_TX1-	C314	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD1-
<7> UMA_HDMI_TX2+	C318	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD2+
<7> UMA_HDMI_TX2-	C322	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD2-

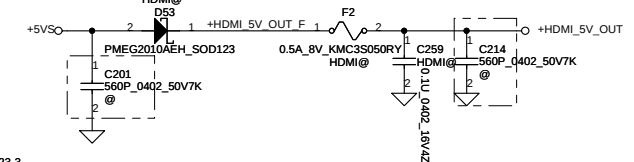


2/9: Add for ESD request

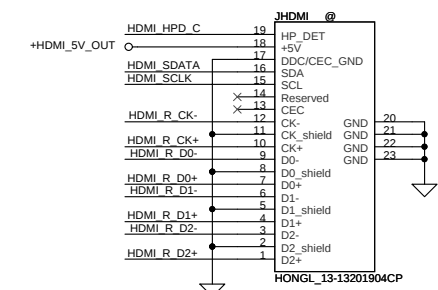


2/9: Add for ESD request

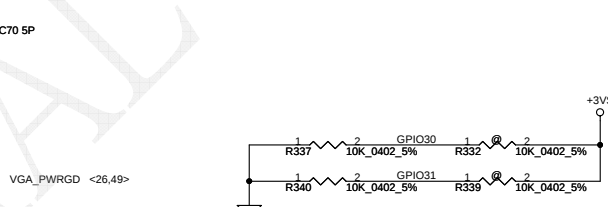
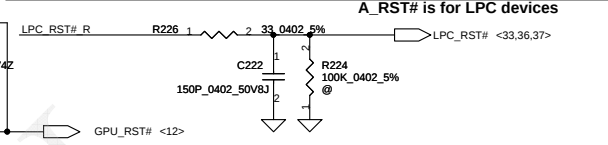
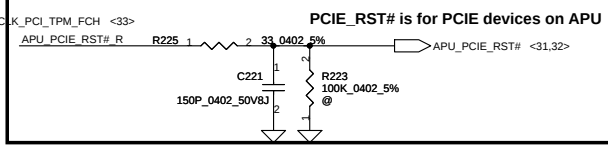
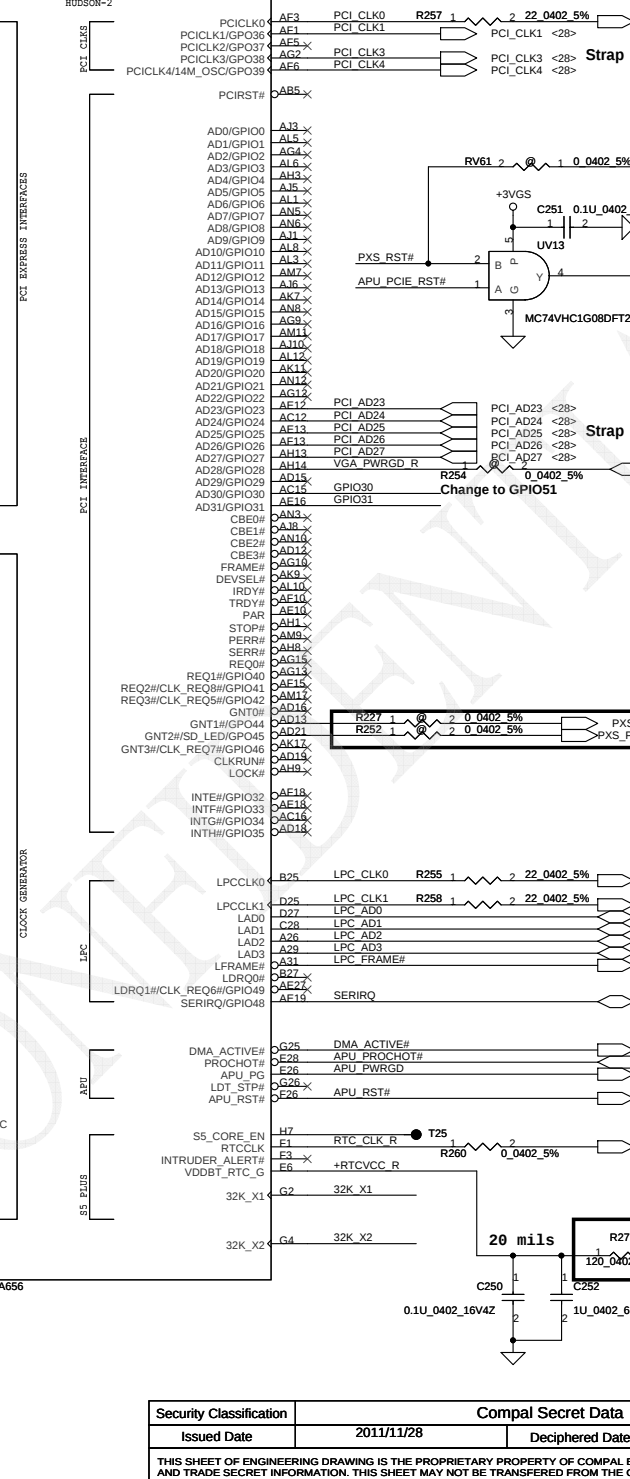
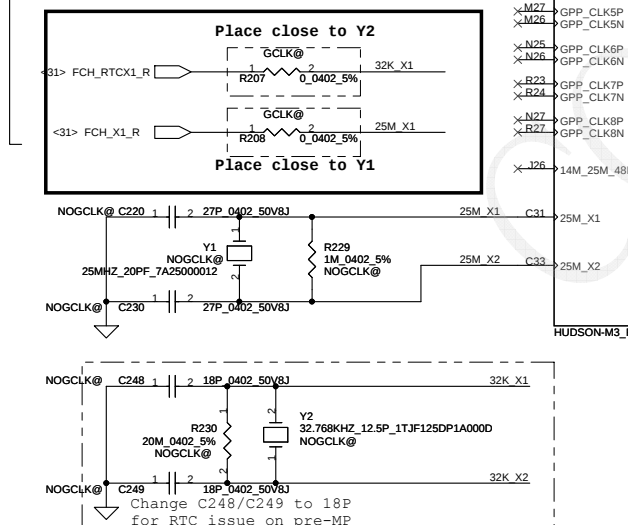
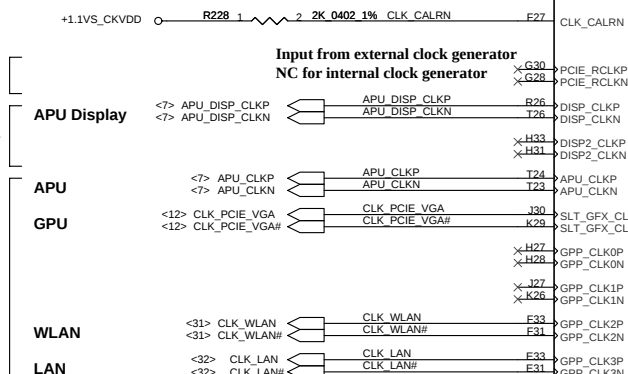
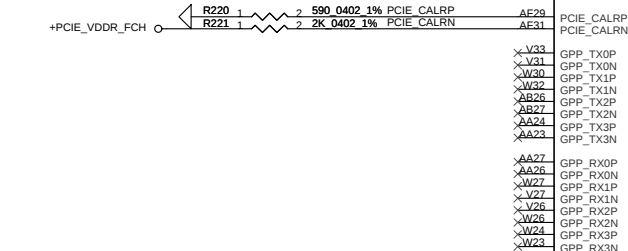
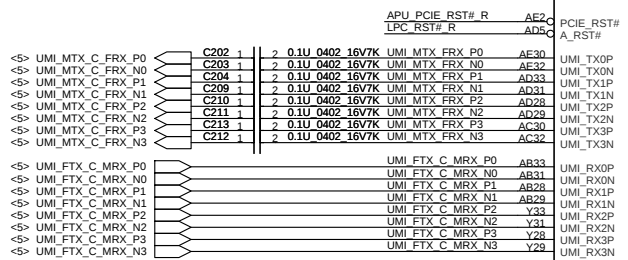
Add C201 and C214 for EMI request on PVT



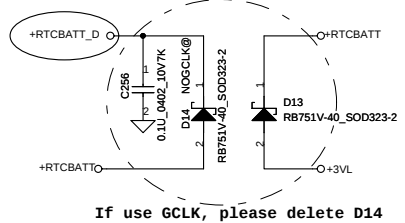
HDMI Connector



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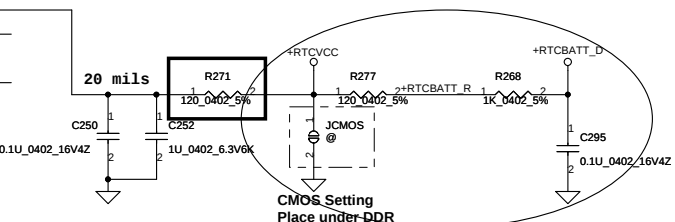


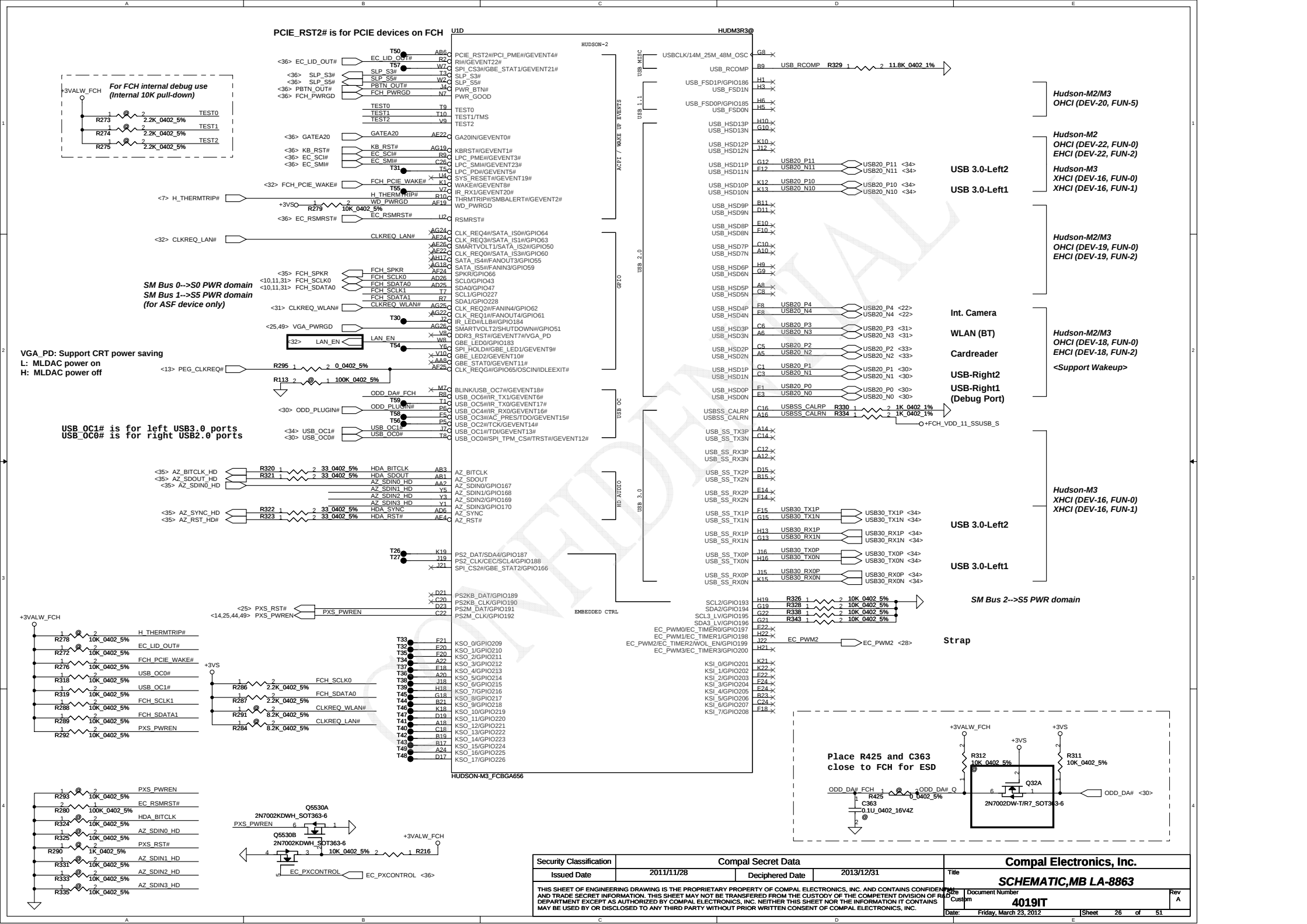
Function	GPI030	GPI031
PowerXpress	0	0
Reserved	0	1
Discrete	1	0
UMA	1	1



DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

S5_CORE_EN is for S5+ mode used to turn off +1.1VALW and +3VALW of FCH on S5+ mode

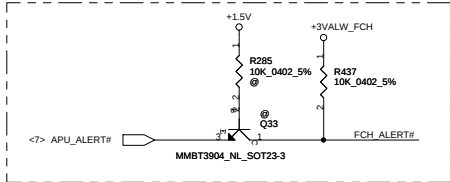




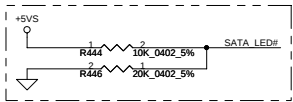
HDD

14" ODD

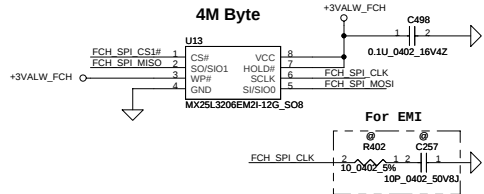
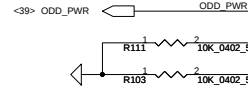
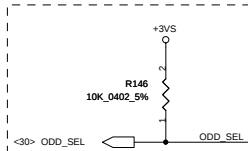
15"/17" ODD



To avoid LED flashing



ODD_SEL	SATA port	SKU
High	Port 1	14"
Low	Port 2	15"/17"



UIB

HUDSON-2

ED_C3D0

GBE_L3N1

GBE_L3N2

GBE_L3N3

GBE_L3N4

GBE_L3N5

GBE_L3N6

GBE_L3N7

GBE_L3N8

GBE_L3N9

GBE_L3N10

GBE_L3N11

GBE_L3N12

GBE_L3N13

GBE_L3N14

GBE_L3N15

GBE_L3N16

GBE_L3N17

GBE_L3N18

GBE_L3N19

GBE_L3N20

GBE_L3N21

GBE_L3N22

GBE_L3N23

GBE_L3N24

GBE_L3N25

GBE_L3N26

GBE_L3N27

GBE_L3N28

GBE_L3N29

GBE_L3N30

GBE_L3N31

GBE_L3N32

GBE_L3N33

GBE_L3N34

GBE_L3N35

GBE_L3N36

GBE_L3N37

GBE_L3N38

GBE_L3N39

GBE_L3N40

GBE_L3N41

GBE_L3N42

GBE_L3N43

GBE_L3N44

GBE_L3N45

GBE_L3N46

GBE_L3N47

HUDM3R3@

SD_CLK/CLK_2/GPIO73

SD_CMD/LOAD_2/GPIO74

SD_CMD/LOAD_2/GPIO75

SD_WP/GPIO76

SD_DATA0/SDAT1_2/GPIO77

SD_DATA1/SDAT0_2/GPIO78

SD_DATA2/GPIO79

SD_DATA3/GPIO80

GBE_COL

GBE_CRS

GBE_MDCK

GBE_MDIO

GBE_RXCLK

GBE_RXD3

GBE_RXD2

GBE_RXD1

GBE_RXD0

GBE_TXCLK

GBE_TXD3

GBE_TXD2

GBE_TXD1

GBE_TXD0

GBE_PHY_PD

GBE_PHY_RST#

GBE_PHY_INTR

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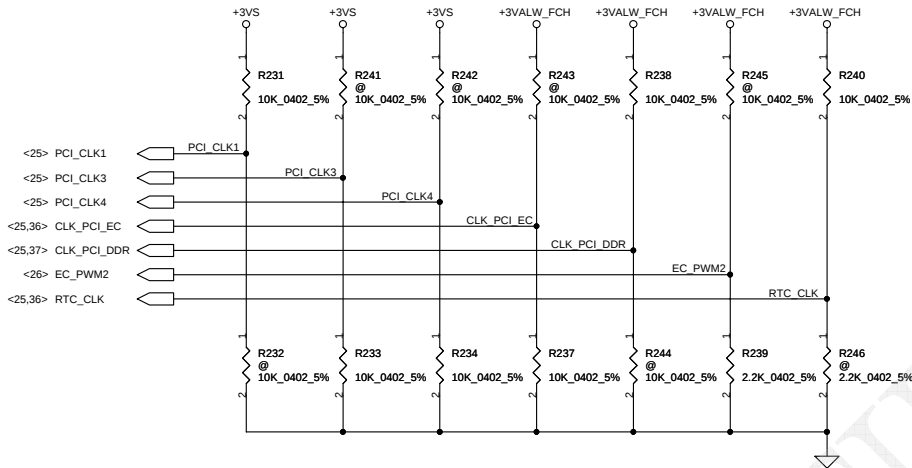
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AG1

STRAP PINS

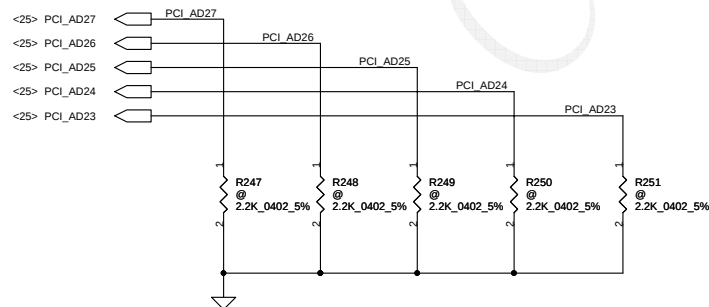
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



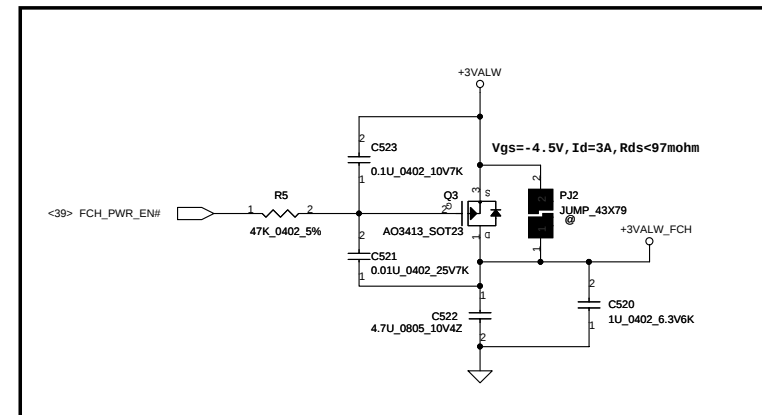
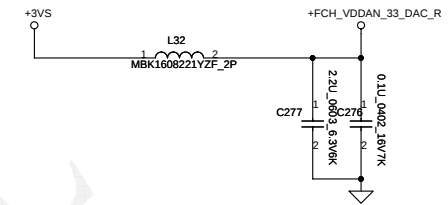
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

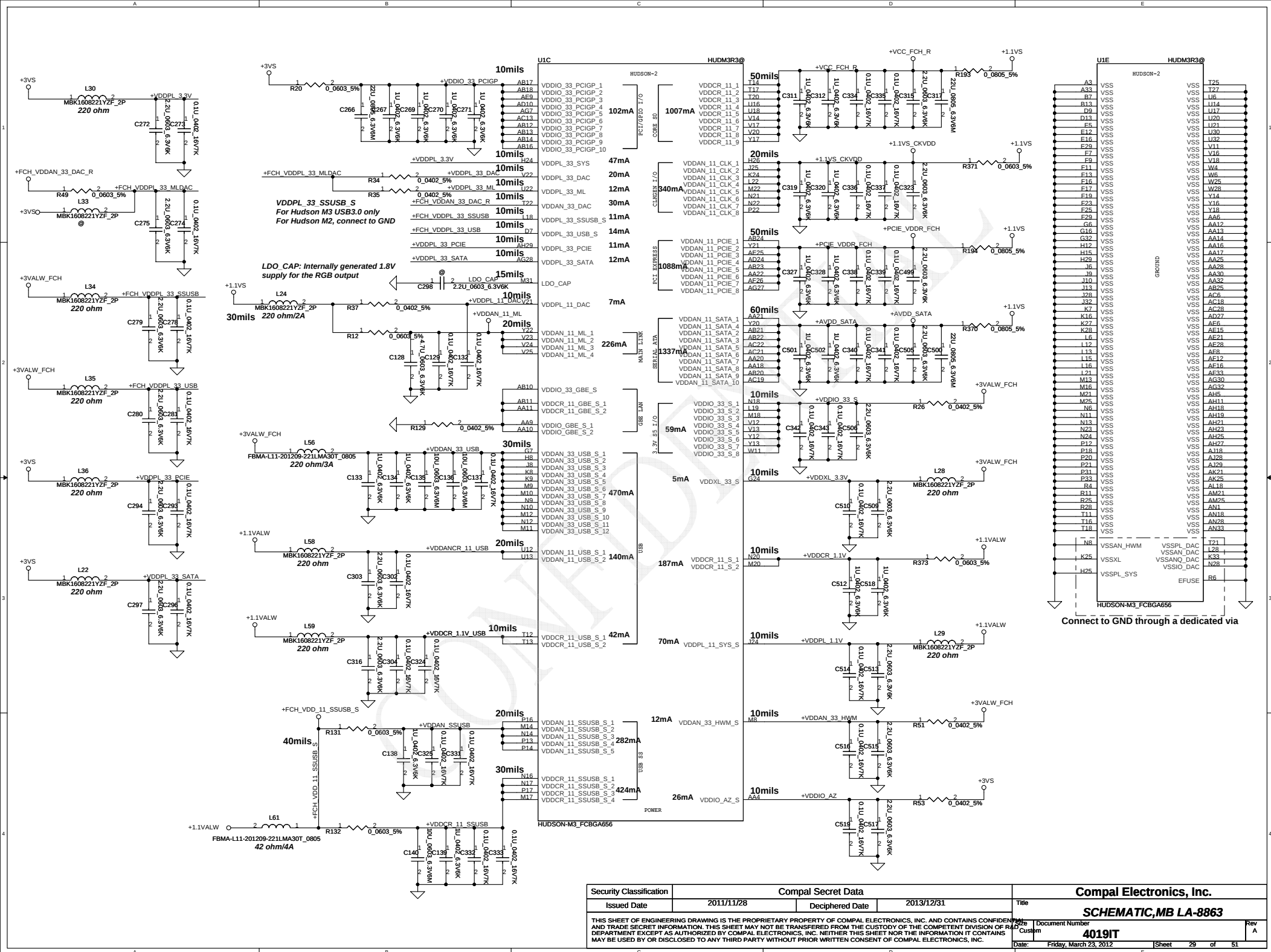
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



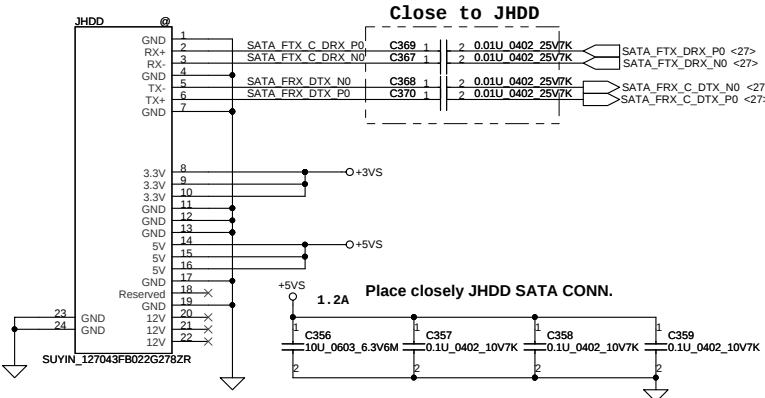
CRT Power Down Circuit



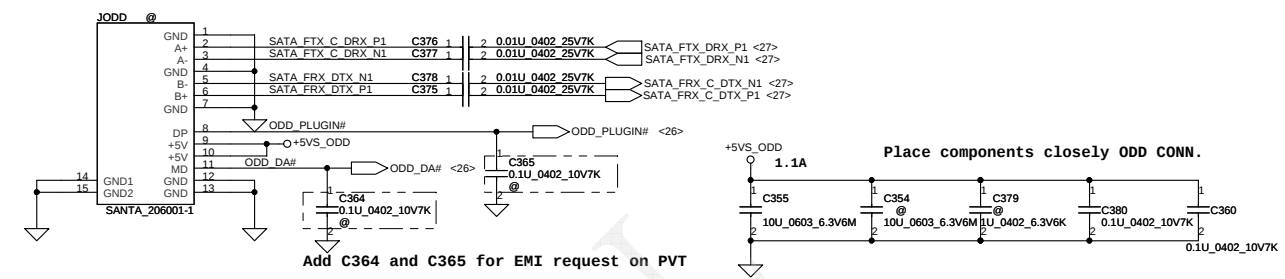
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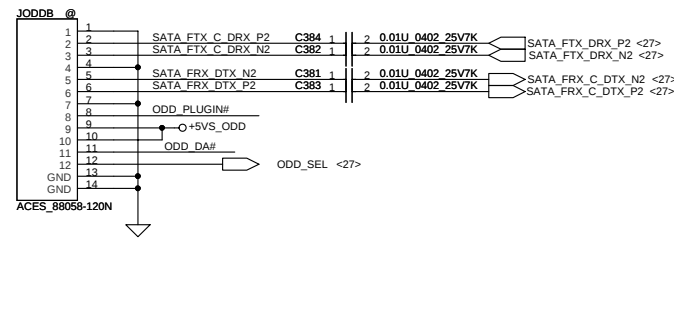
SATA HDD Conn.



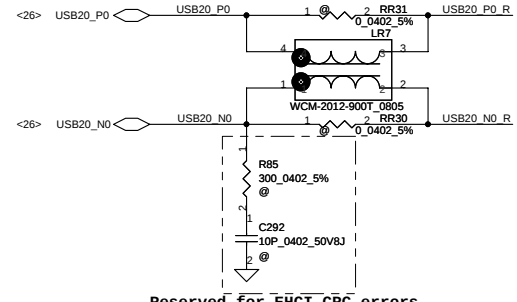
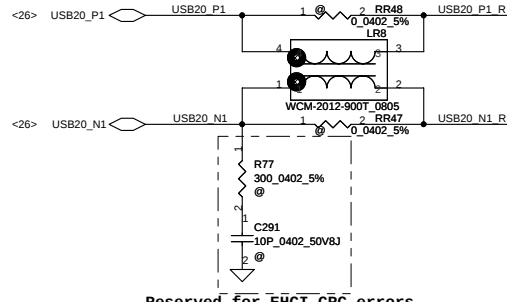
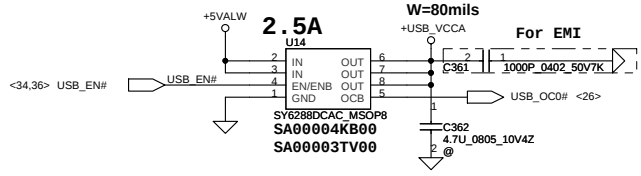
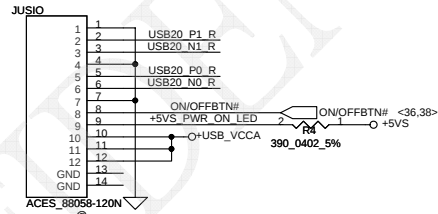
SATA ODD Conn



SATA ODD Conn (for 15"/17")



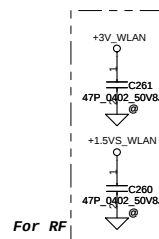
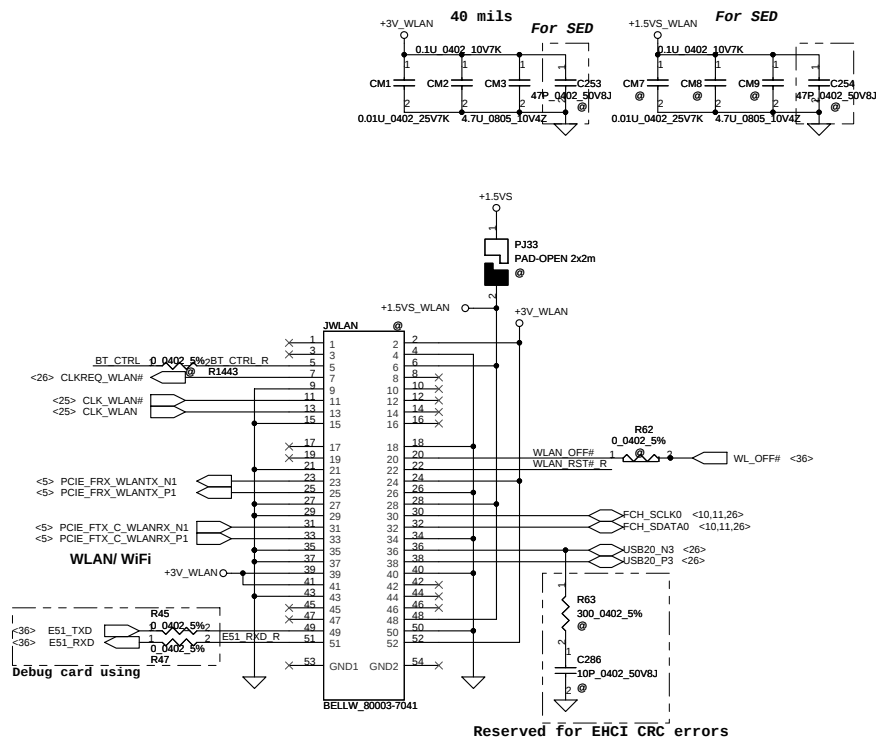
Power Button & RUSB connector



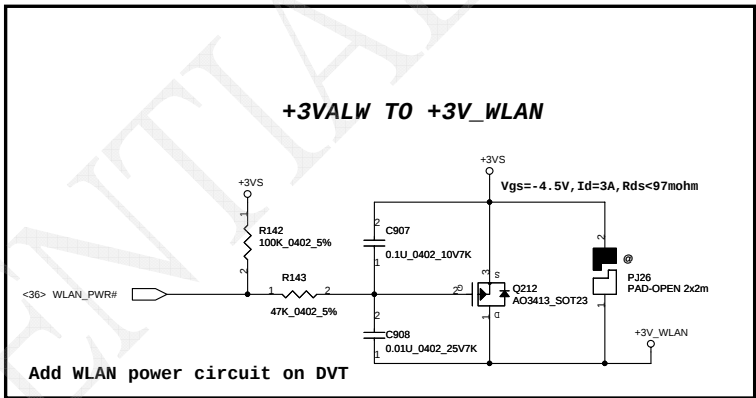
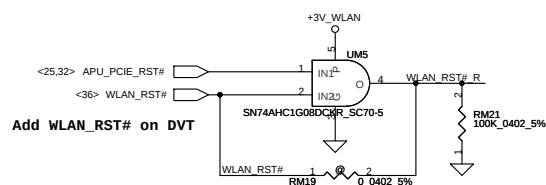
Reserved for EHCI CRC errors

Reserved for EHCI CRC errors

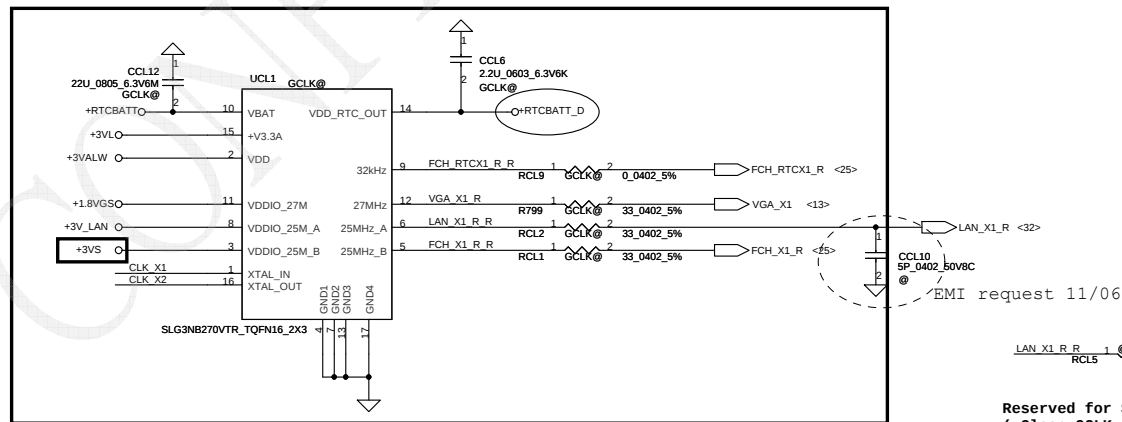
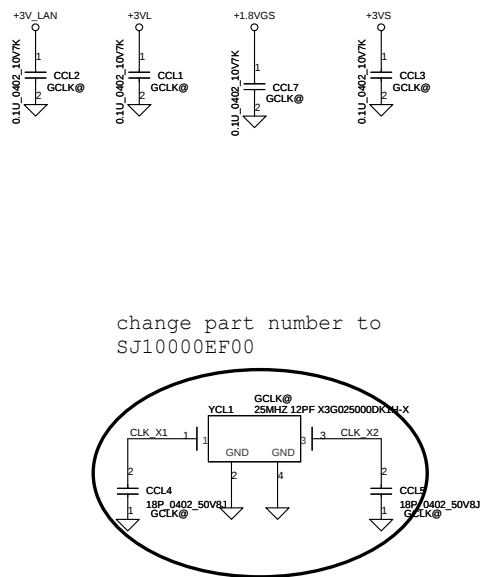
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Issued Date	2011/11/28	Deciphered Date	2013/12/31	Compal Electronics, Inc.	
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Slot 1 Half PCIe Mini Card-WLAN

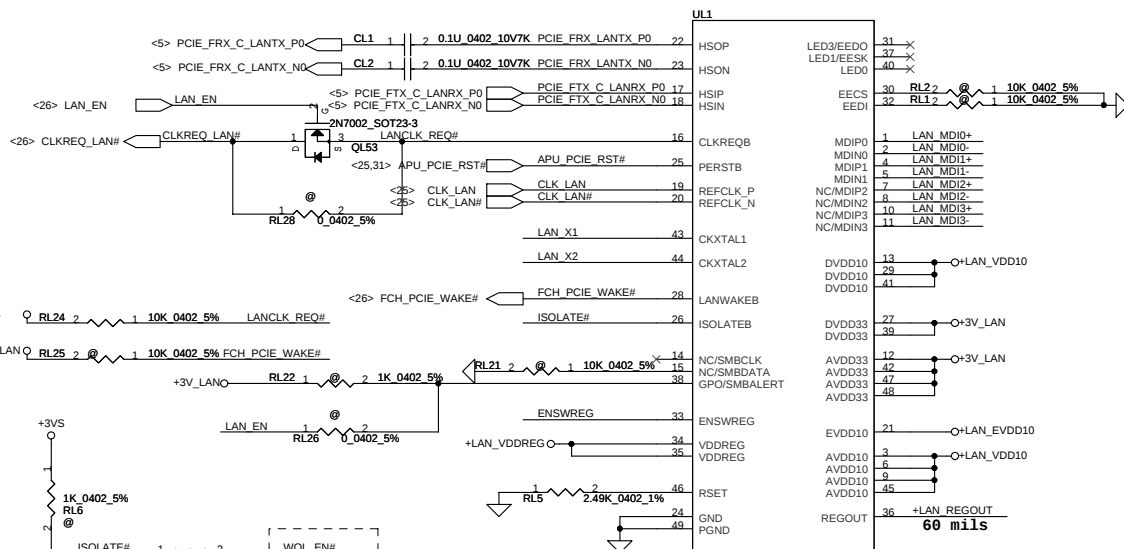
WLAN&BT Combo module circuits		
	BT on module Enable	BT on module Disable
BT_CTRL	H	L



Change to GCLK to SLG3NB270V
SA00005DP00 for 27MHz
for VGA



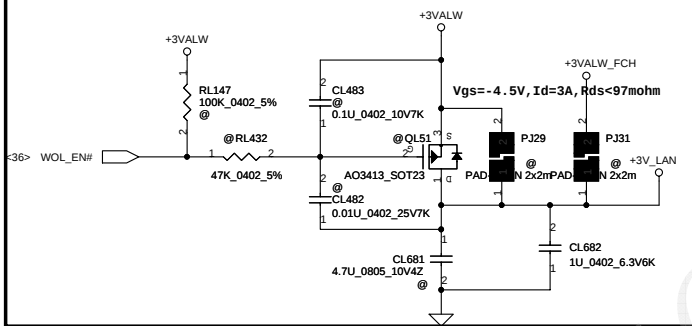
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	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

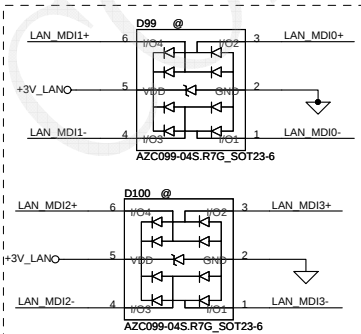
+3VALW TO +3V_LAN



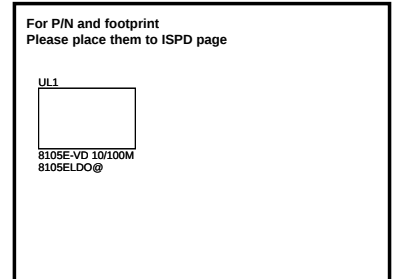
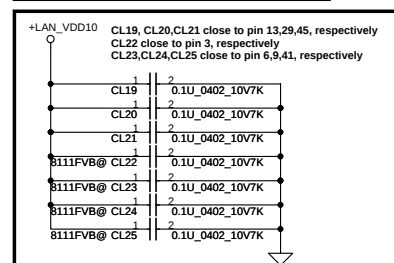
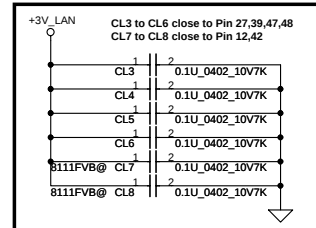
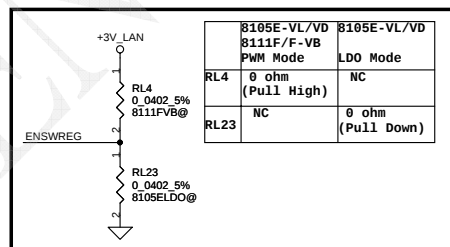
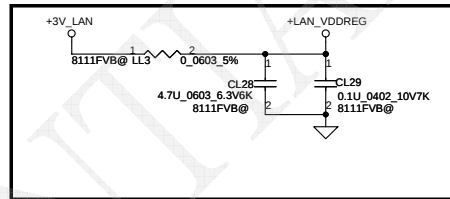
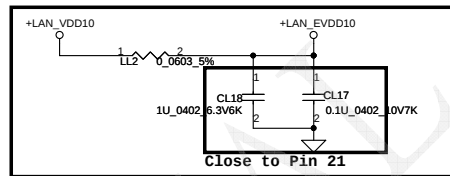
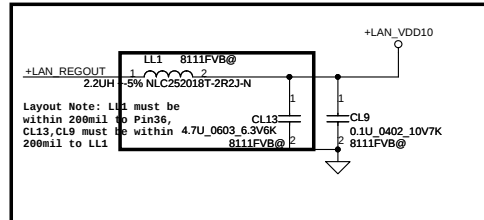
+3V_LAN rising time (10%-90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN S0	Sx	ISOLATEB S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

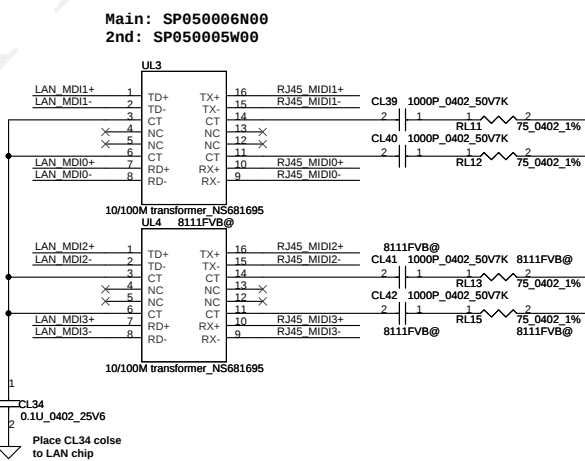
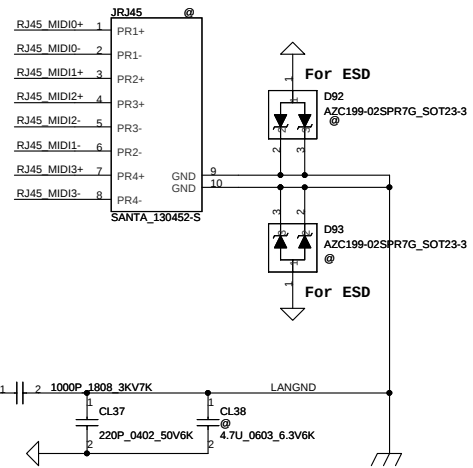
* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



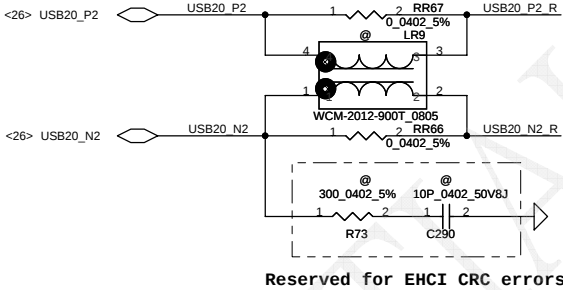
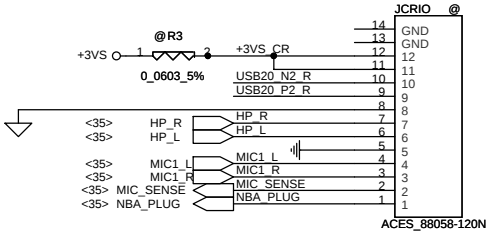
2/9: Add for ESD request



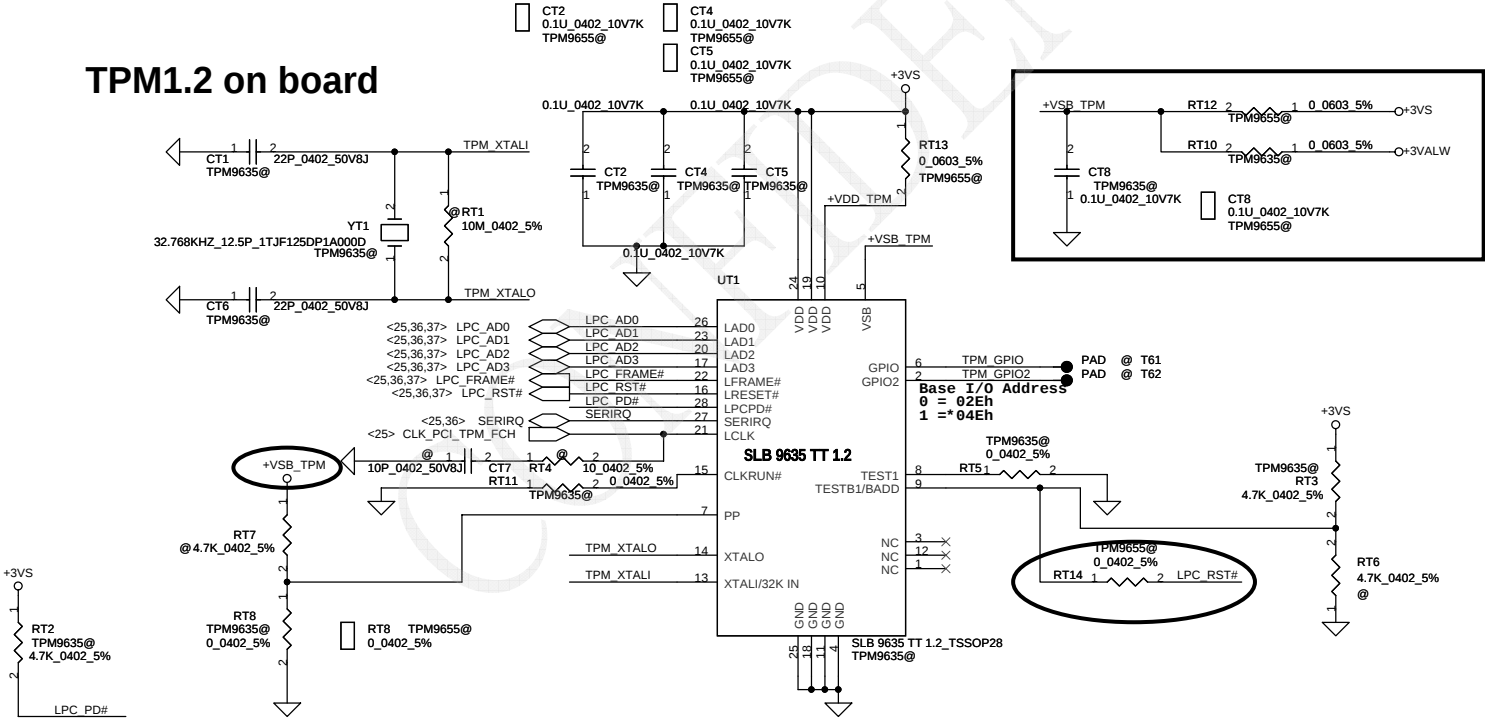
LAN Conn.



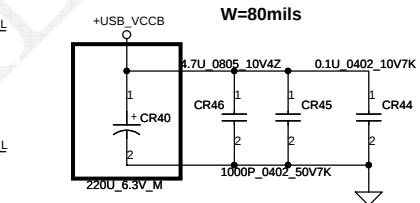
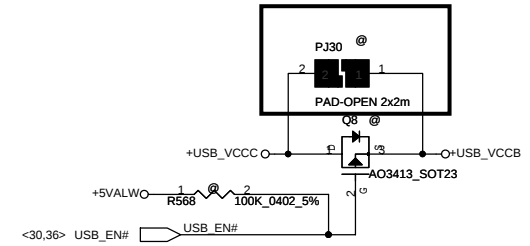
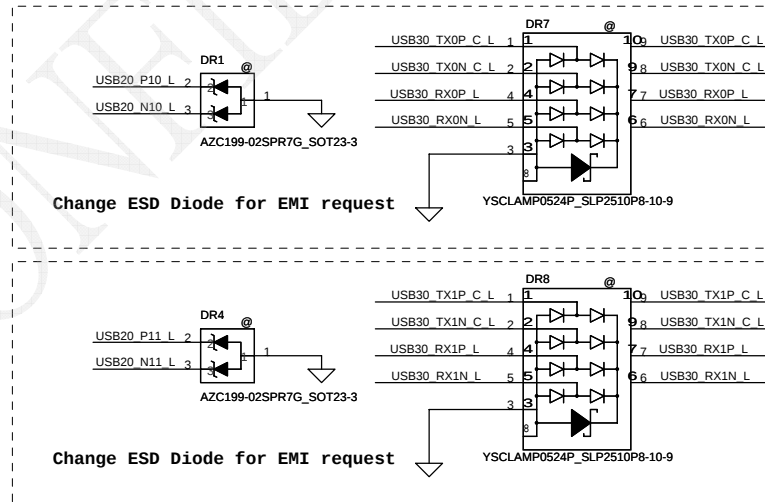
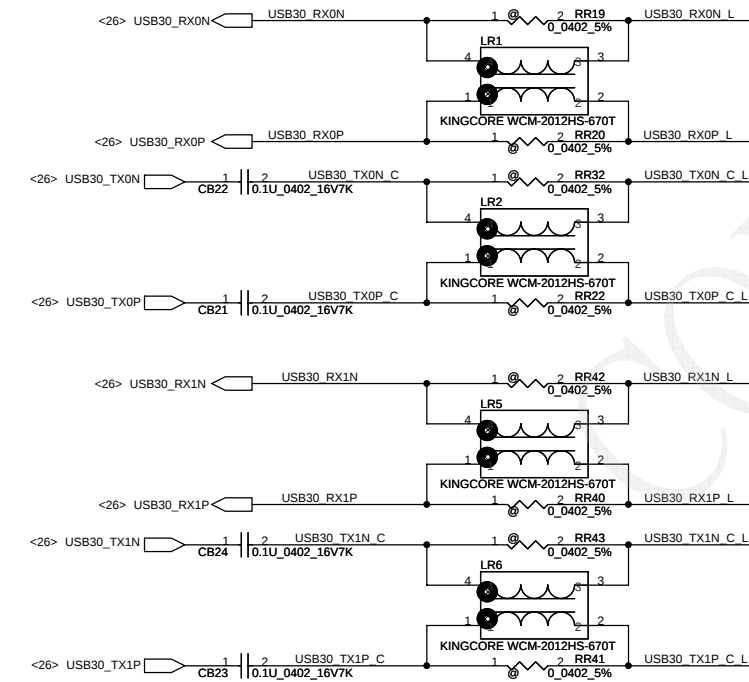
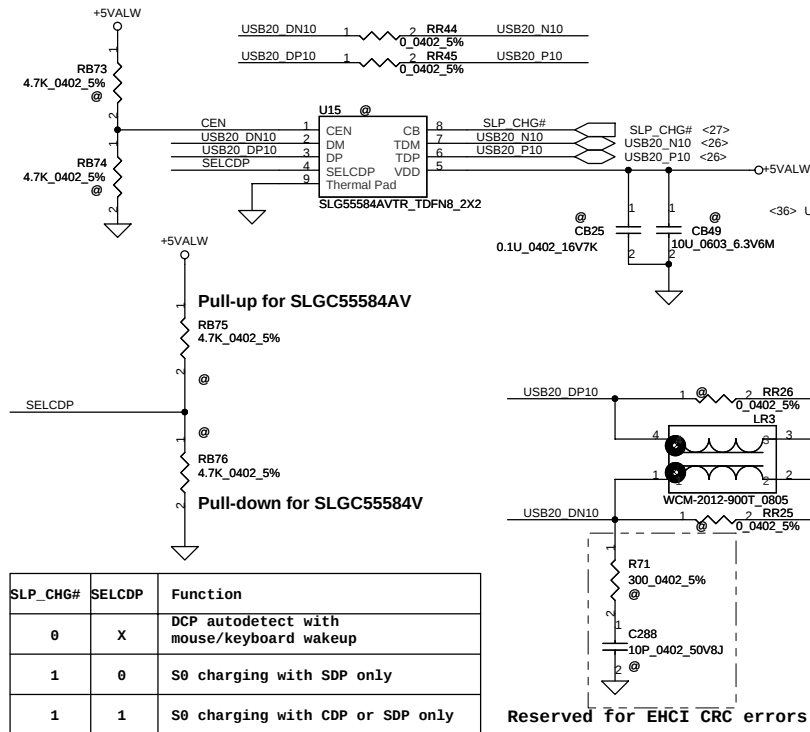
CardReader Conn.



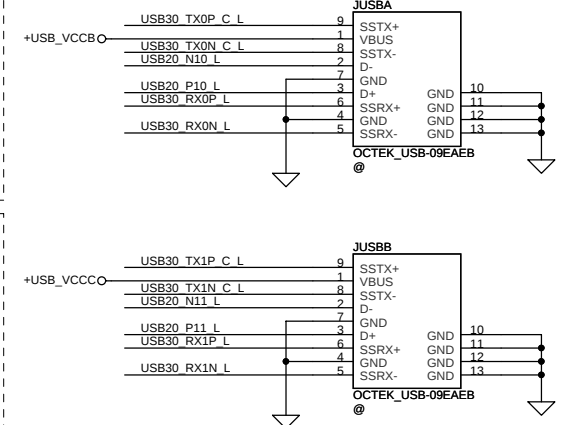
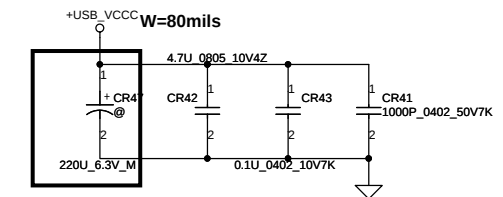
TPM1.2 on board



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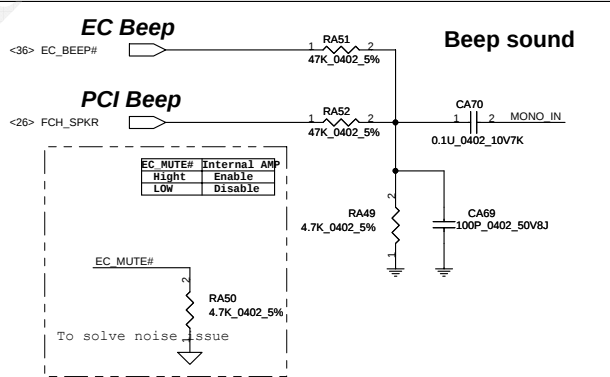
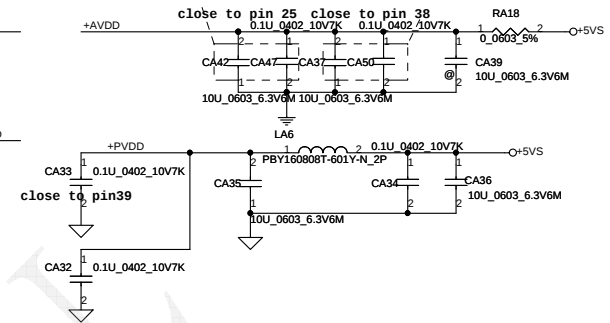
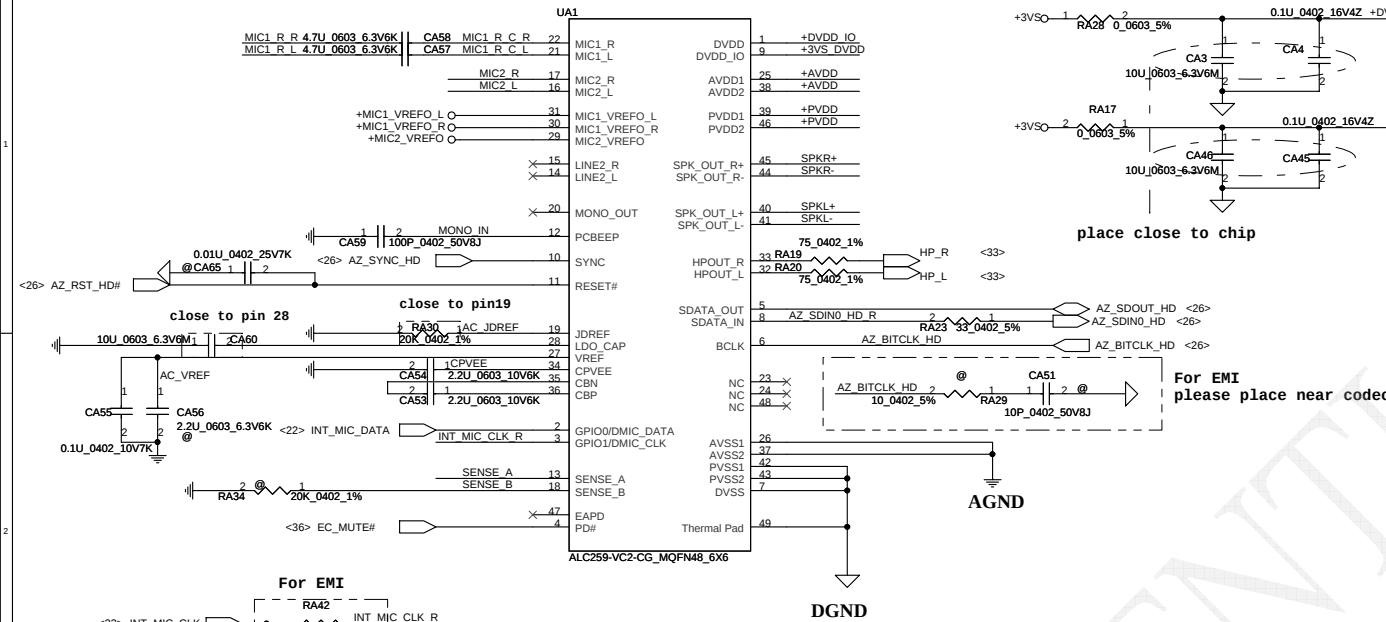


150uFx2 or 220uFx1

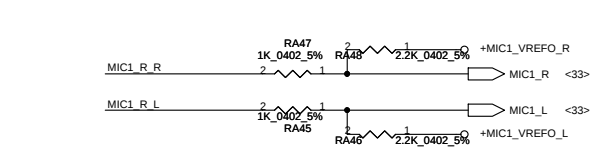


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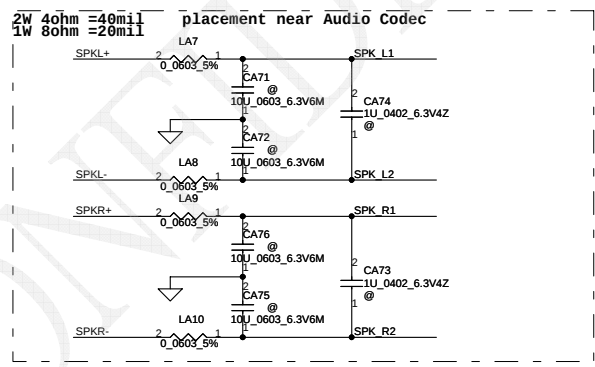
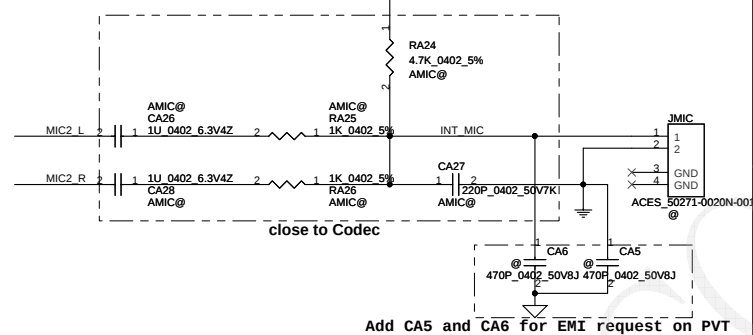
35mA for 3.3V level



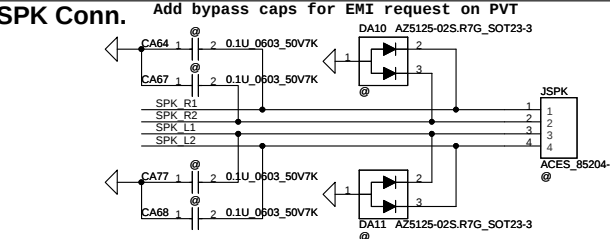
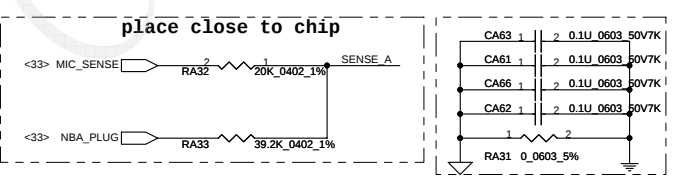
Ext.MIC/LINE IN JACK

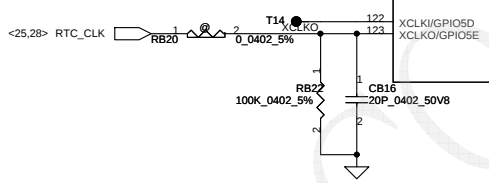
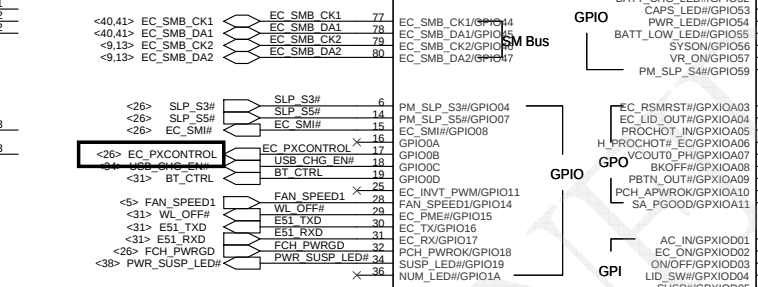
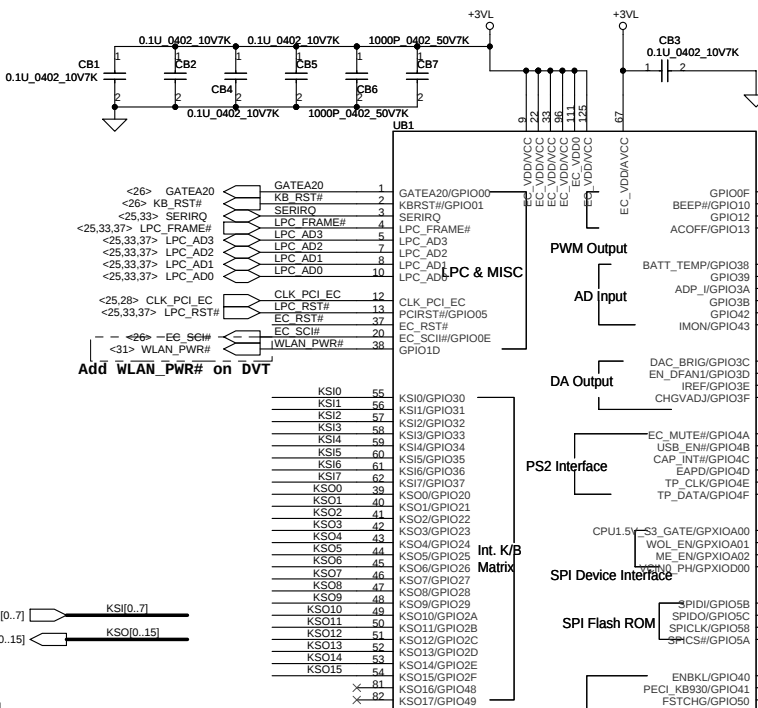
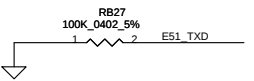
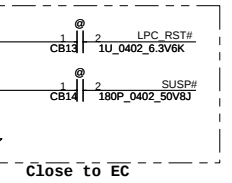
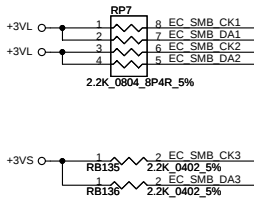
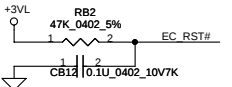
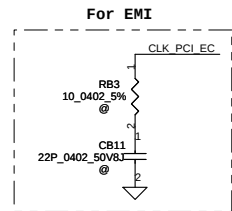


Analog MIC



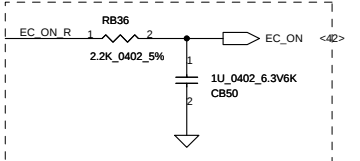
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	



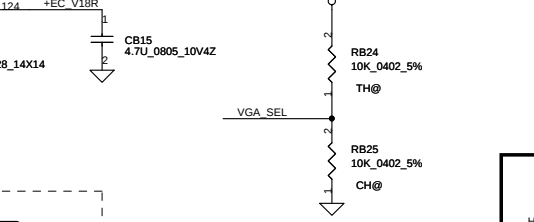
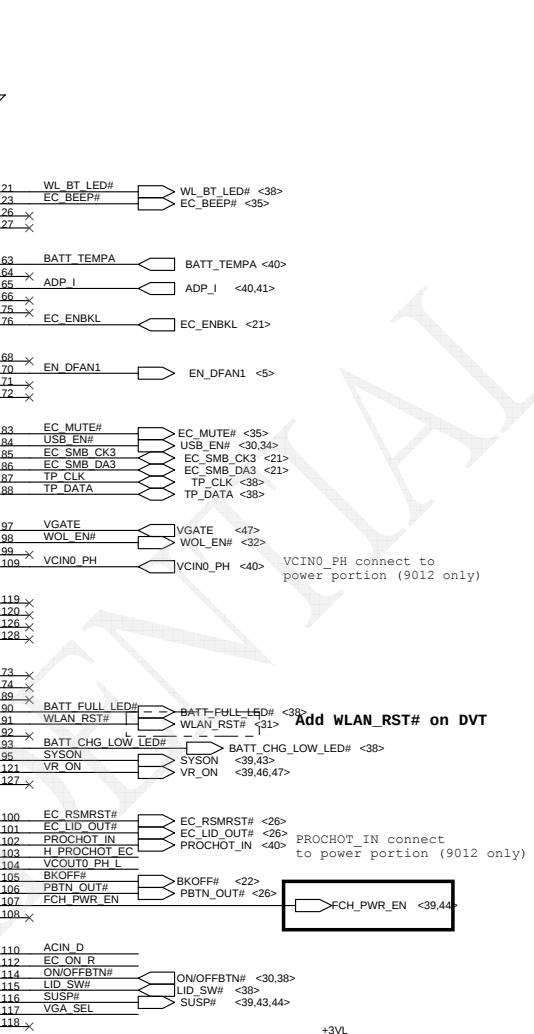


Voltage Comparator Pins FOR 9012 A3

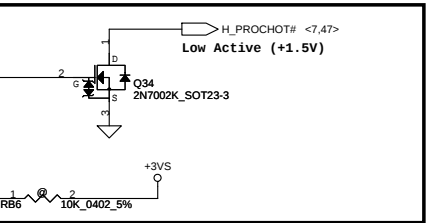
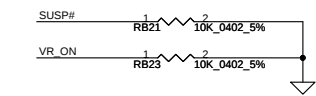
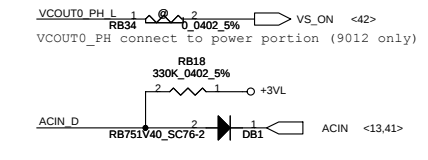
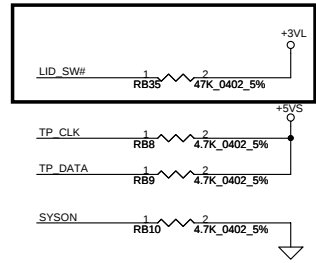
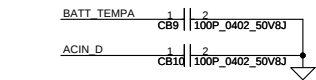
VCIN0 pin109	>1.2V	<1.2V
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



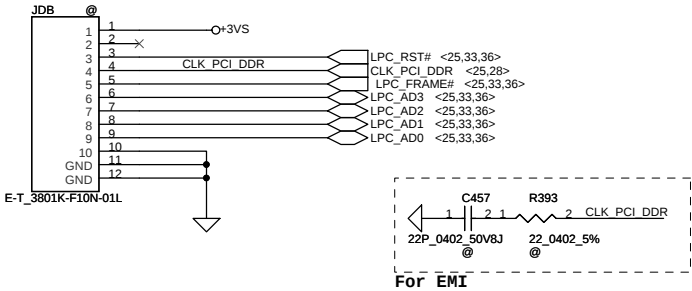
For KB9012 EC_ON low pulse work around



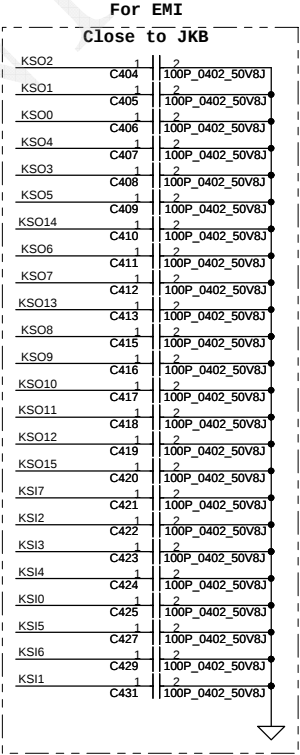
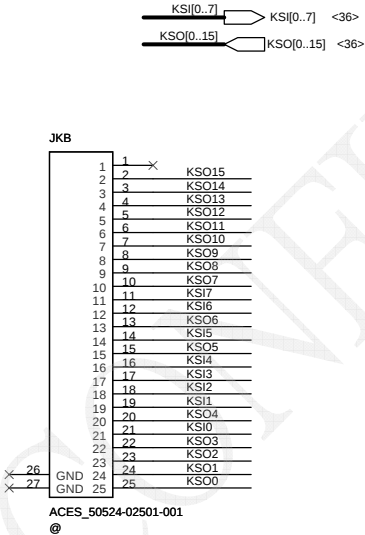
VGA_SEL	High	Low
Pin117	HIGH	LOW
Address	82h	9Ah



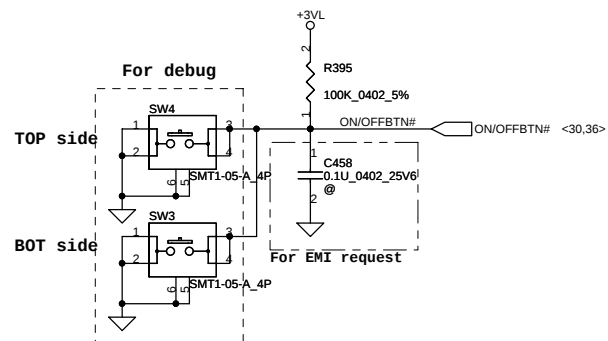
LPC Debug Port



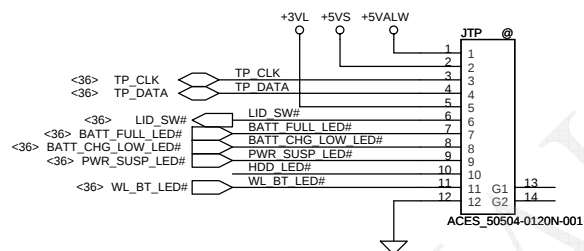
KEYBOARD CONN.



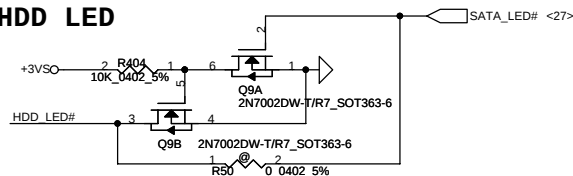
Power Button



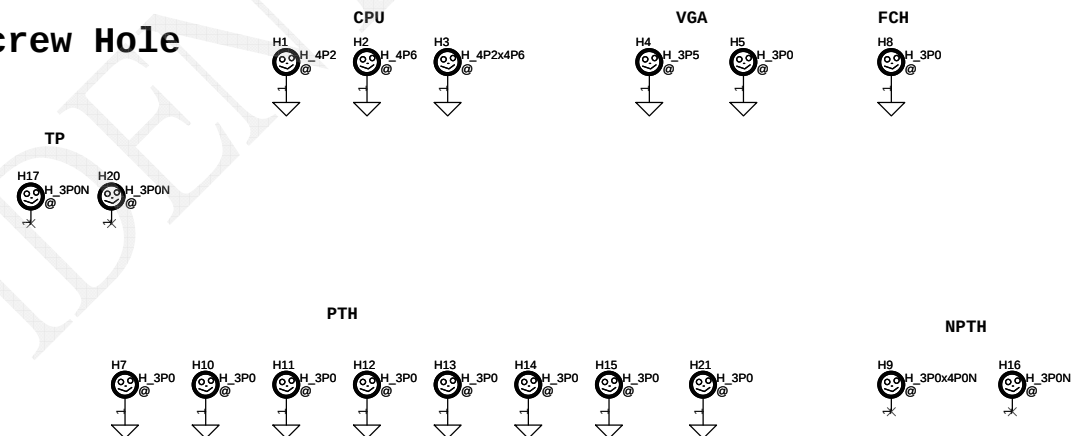
Touchpad Connector



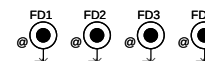
HDD LED



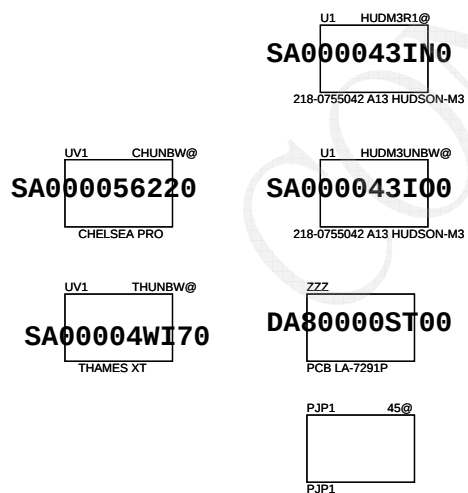
Screw Hole



PCB Fedical Mark PAD

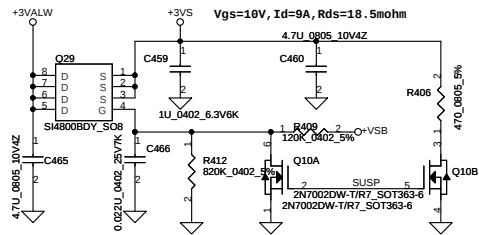


ISPD

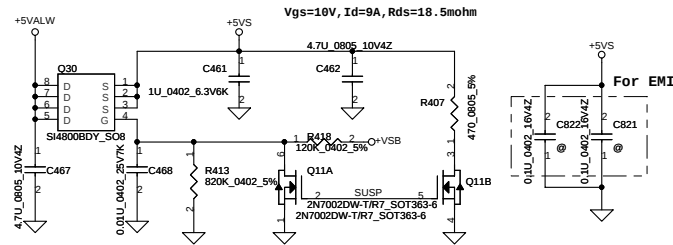


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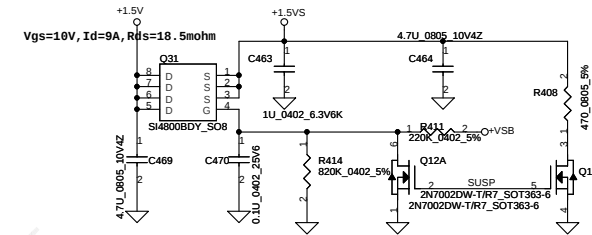
+3VALW TO +3VS



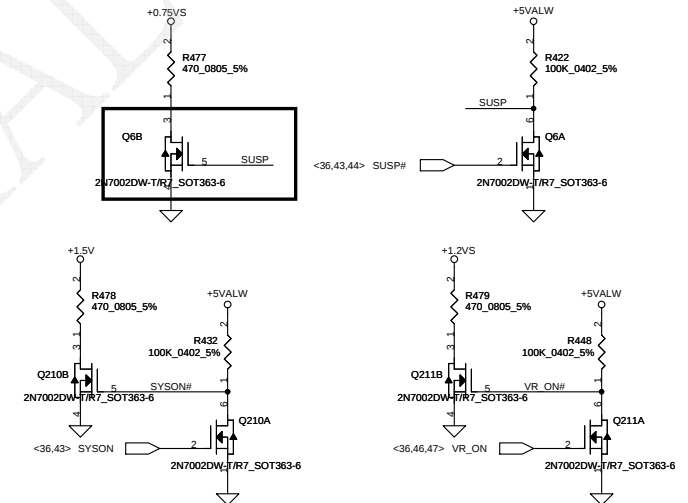
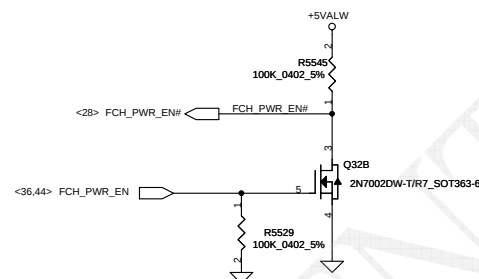
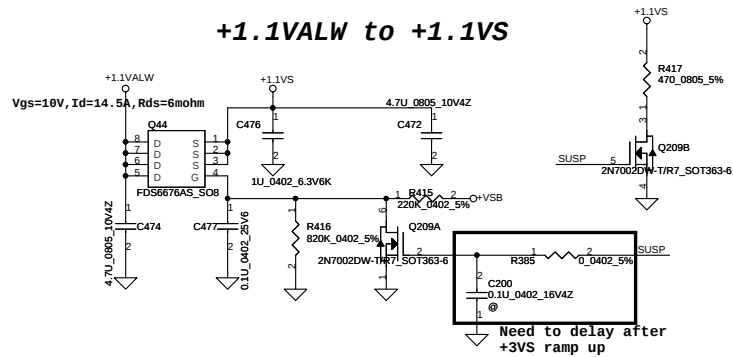
+5VALW TO +5VS



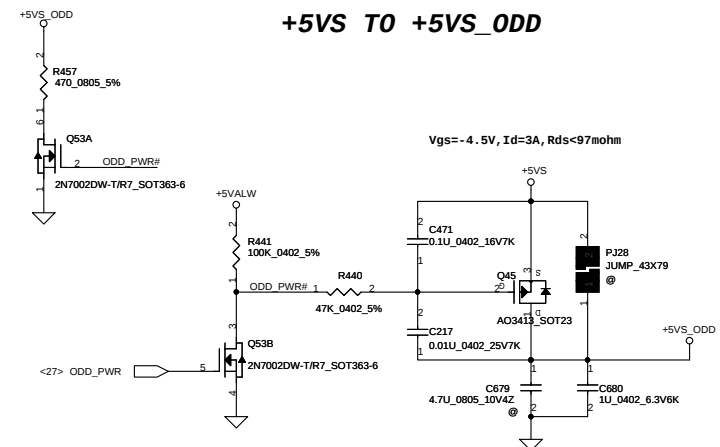
+1.5V to +1.5VS



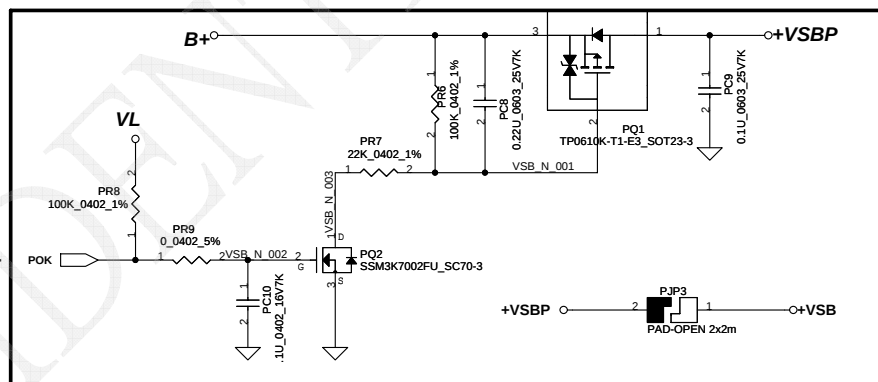
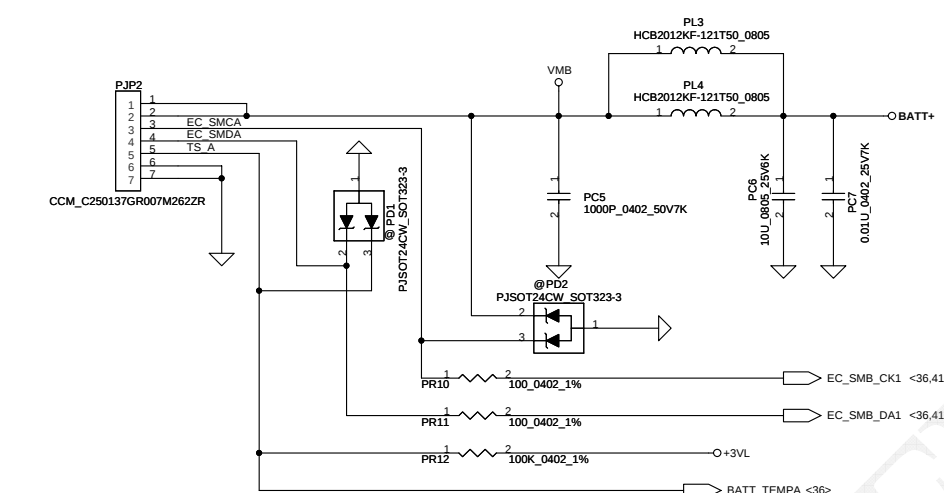
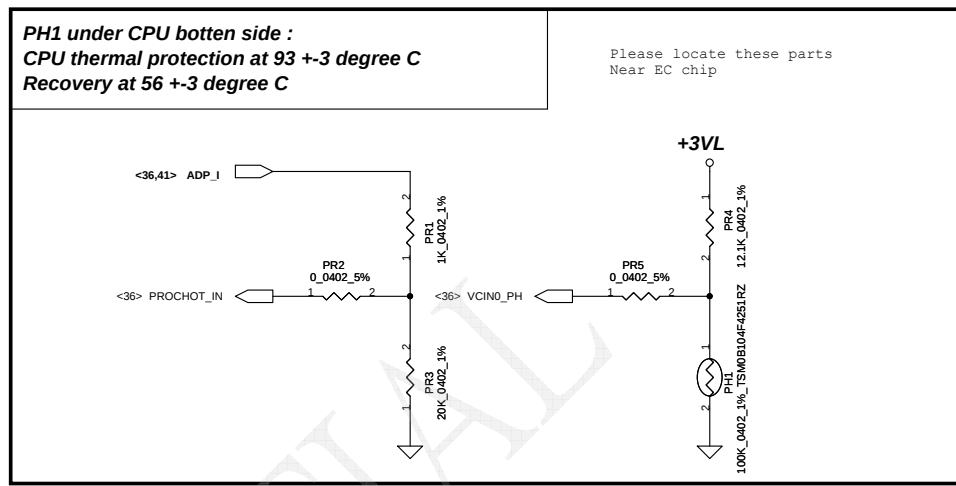
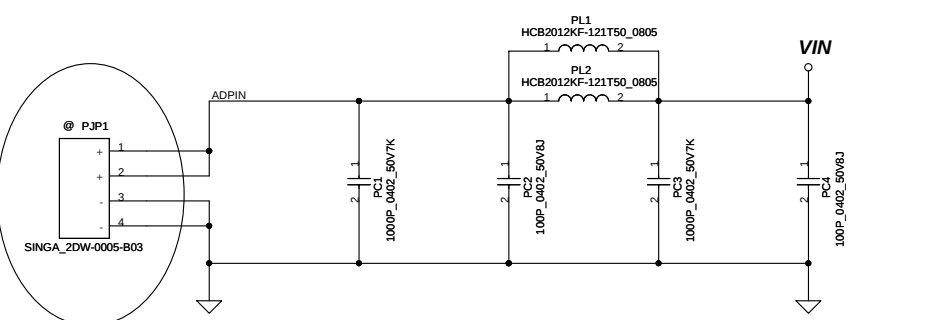
+1.1VALW to +1.1VS



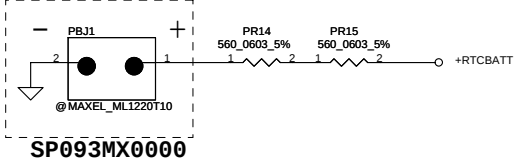
+5VS TO +5VS_ODD



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RTC Battery

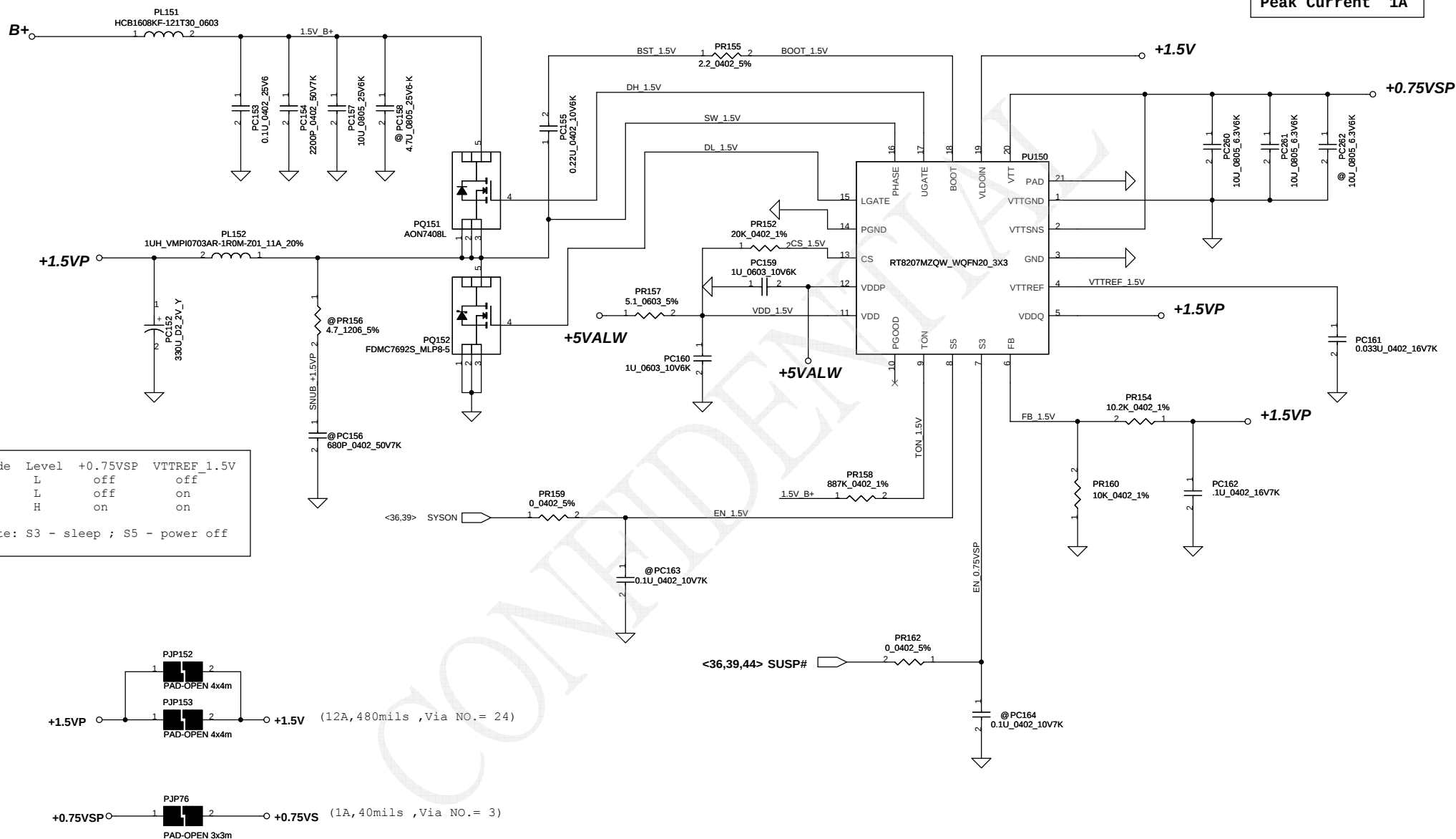


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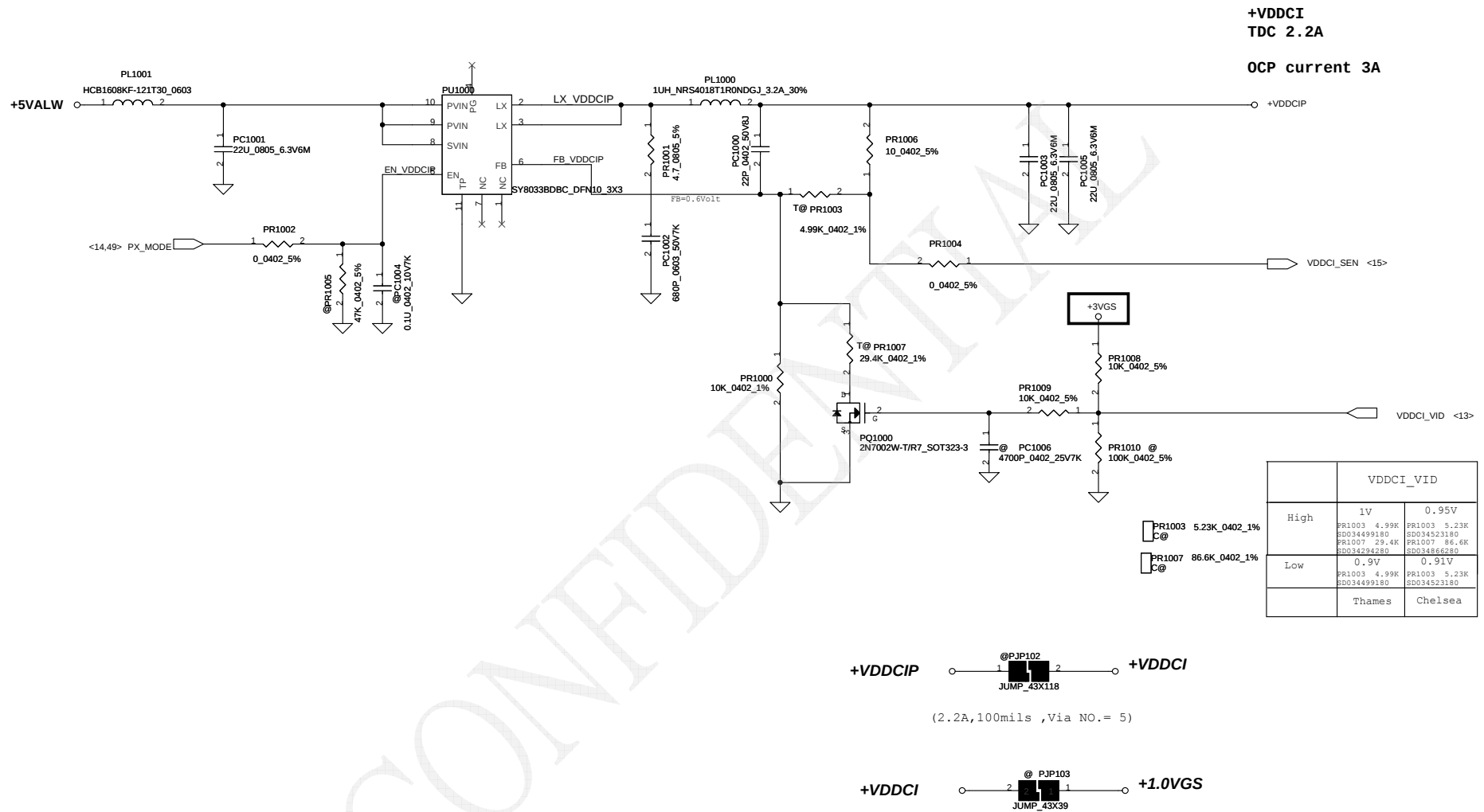
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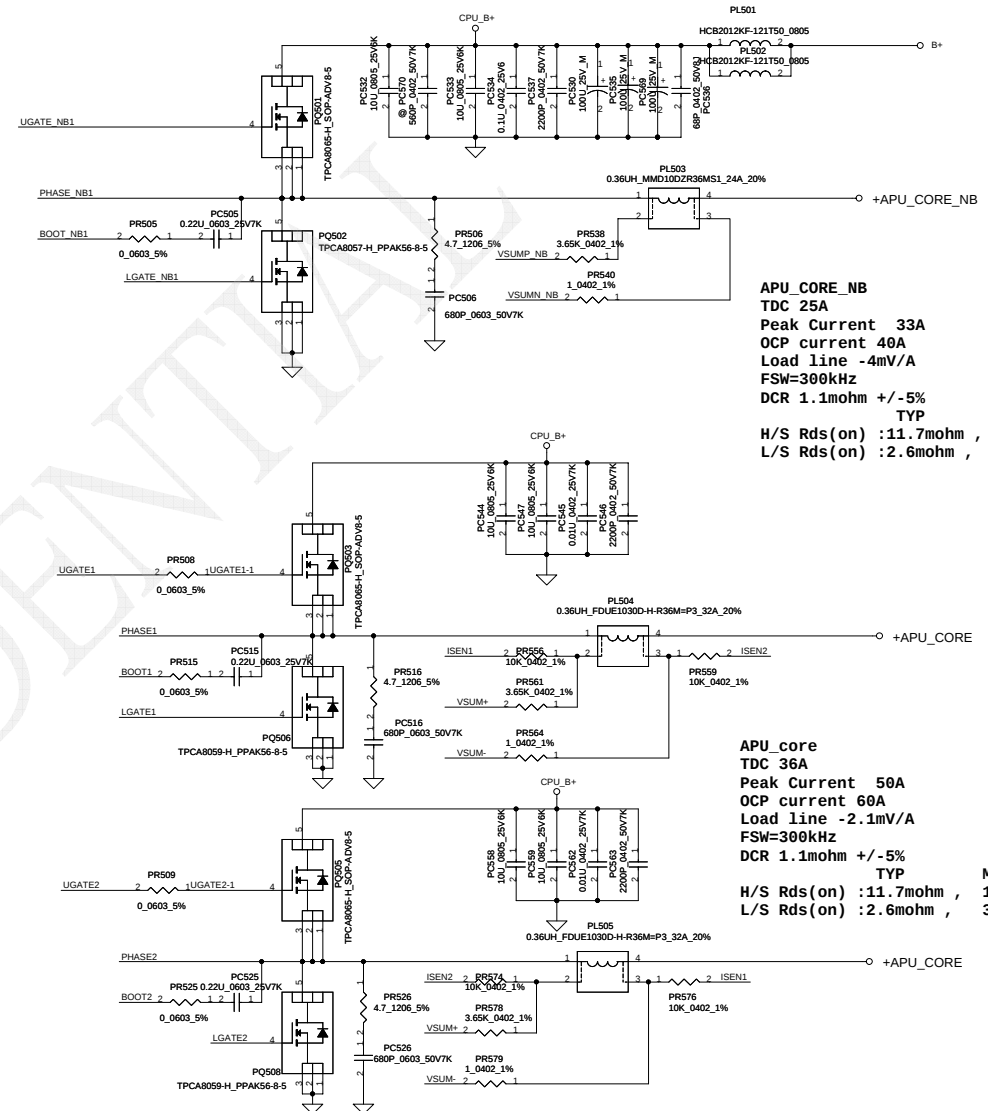
Mode	Level	+0.75VSP	VTTREF 1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



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APU_core
TDC 36A
Peak Current 50A
OCP current 60A
Load line -2.1mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
H/S Rds(on) :11.7mohm ,
L/S Rds(on) :2.6mohm ,

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The diagram shows a transformer with a primary winding connected to a 330V D2 2V_Y source. The secondary side consists of four identical windings, each labeled PC621, PC622, PC623, and PC624, all connected to a 330V D2 2V_Y source. The windings are connected in parallel to a common output line, which is then connected to a ground symbol.

capacitors under processor on bottom side of board

The schematic diagram illustrates the power supply section of the PCB. It features a +5VDC1 input connected to a series of capacitors (PC934, PC939, PC935, PC954, PC969, PC956, PC936, PC967, PC972, PC973) and a network of capacitors (PC921, PC922, PC930) connected to ground. The capacitors are labeled with their values: 1uF 0402 6.3V6K for the main line and 10uF 0603 6.3V6M for the ground network.

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HW PIR (Product Improve Record)

QMLE4 LA-8863P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/02/10

Item	Date	Page	Solution	Request
1.	1/10	P32	Add PJ31	For saving power consumption
2.	1/12	P38	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P35	Add internal MIC to MB	For customer request
4.	2/2	P14	Remove PX4.0 circuit	Support PX5.0
5.	2/2	P31	Add PJ26,PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P33	Update JCRI0 pin definition	Change int. MIC to MB
7.	2/2	P35	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P31	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P31	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/7	P32	Change UL3 and UL4 PN to SP050005V00	For shortage

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	Request
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121~R124,R118,R119	For debug use
5.	3/7	P27	Update U13 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20,RB34,R3,RV102,R425,R136,R31,R32,R33,RV284,RV287 R62,RV277 to short pad	
8.	3/12	P24	Add C201 and C214	For EMI request
9.	3/12	P30	Add C364 and C365	For EMI request
10.	3/12	P35	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/02/14	P40-PWR-DCIN/BATT CONN/OTP	Delete PR12,PR13	Circuit modify
2.	2012/02/14	P41-PWR-CHARGER	Change PR211 to 0.01_1206_1%,PL201 to1UH 4*4*2 Add PC207,PC208,PC217,PC2I8,Delete PC232,PC233	Circuit modify
3.	2012/02/14	P43-PWR-1.5VP/+0.75VSP	Change PL152 to SH00000KS00	Circuit modify
4.	2012/02/14	P44-PWR-+1.1VALWP/+1.8VSP	Change PR718 to 47K,add PC187	HW request
5.	2012/02/14	P46-+1.2VSP/+2.5VSP PR127 to SD034105380	Change PL122 to 2.2uH(SH000000MR00),	Circuit modify
6.	2012/02/14	P37-PWR +CPU CORE	Change PQ502 to TPCA8057	Circuit modify
7.	2012/03/06	P40-PWR-DCIN/BATT CONN/OTP	Add PR12(100KQ)	Circuit modify

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