

COMPAL CONFIDENTIAL

MODEL NAME : **PAL70**

PCB NO : **LA-6611P (DAA00001W10)**

BOM P/N : **43XXXXXXLXX**

GPIO MAP Version 1010

E3 MACALLAN 13" UMA BGA Sandy Bridge + FCBGA PCH Cougar Point-M 2010-01-21 REV : 1.0(A00)

Items	R1 P/N	R3 P/N
CPU 2.5G	SA00004EL2L	SA00004EL3L
CPU 2.6G	SA00004EM2L	SA00004EM3L
CPU 2.7G	SA00004F02L	SA00004F03L
CPU 2.1G	SA00004KP1L	SA00004KP2L
PCH	SA00004IW2L	SA00004IW3L
LAN	SA00003SI4L	SA00003SI5L
USH	SA00003AO1L	SA00003AO2L

@ : Nopop Component

MB Type	BOM P/N	TPM		TCM		With SPI	With TAA
		1@	3@	2@	4@	5@	6@
2.5G CPU TPM EN/ TCM DIS/W TAA	43193431L06	*	*				*
2.5G CPU TPM EN/ TCM DIS/W/SPI	43193431L03	*	*			*	
2.5G CPU TPM DIS/ TCM EN				*	*		*
2.5G CPU TPM DIS/ TCM EN/W/SPI				*	*	*	
2.5G CPU TPM DIS/ TCM DIS			*	*			*
2.5G CPU TPM DIS/ TCM DSI /W/ SPI	43193431L15		*	*		*	
2.6G CPU TPM EN/ TCM DIS/W TAA	43193431L07	*	*				*
2.6G CPU TPM EN/ TCM DIS/W/SPI	43193431L04	*	*			*	
2.6G CPU TPM DIS/ TCM EN				*	*		*
2.6G CPU TPM DIS/ TCM EN/W/SPI				*	*	*	
2.6G CPU TPM DIS/ TCM DIS			*	*			*
2.6G CPU TPM DIS/ TCM DSI /W/ SPI	43193431L16		*	*		*	
2.7G CPU TPM EN/ TCM DIS/W TAA	43193431L08	*	*				*
2.7G CPU TPM EN/ TCM DIS/W/SPI	43193431L05	*	*			*	
2.7G CPU TPM DIS/ TCM EN				*	*		*
2.7G CPU TPM DIS/ TCM EN/W/SPI				*	*	*	
2.7G CPU TPM DIS/ TCM DIS			*	*			*
2.7G CPU TPM DIS/ TCM DSI /W/ SPI	43193431L17		*	*		*	

MB PCB	
Part Number	Description
DAA00001W00	PCB PAL70 LA6611

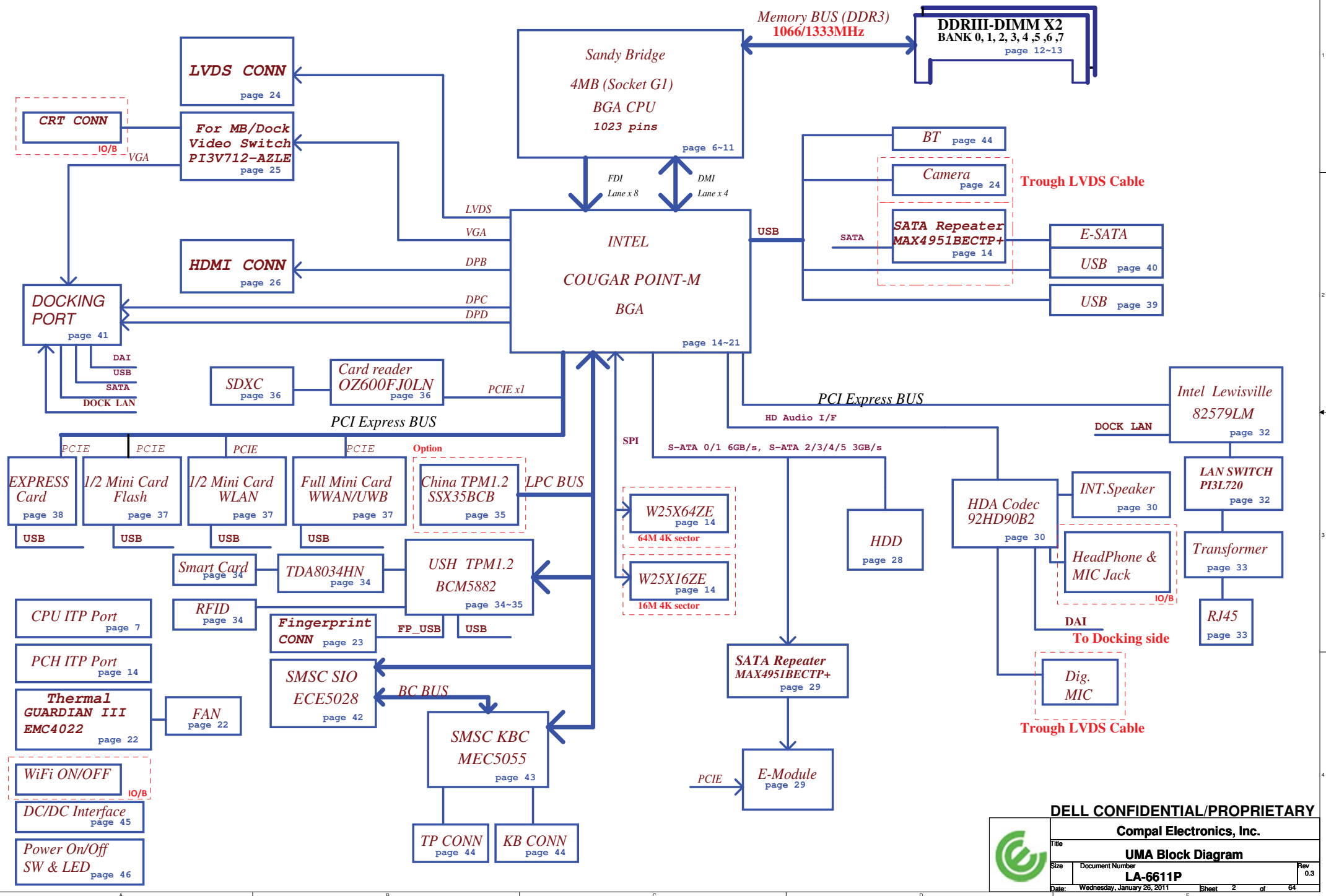
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

Stack up

Layer	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
SolderMask	min 0.4	0.50
Add Plating	1.30	1.05
Top/L1(signal)	0.5oz(0.68)	0.65
Prepreg	1080LRC	2.65
	0.5oz	0.65
Core	3mil	3.09
L3(IN1)	0.5oz	0.65
Prepreg	1080LRC+1080	5.1
L4(IN2)	1oz	1.35
Core	3mil	3.09
L5(GND2)	1oz	1.35
Prepreg	1080HRC	2.90
L6(IN3)	0.5oz	0.65
Core	6mil	6
L7(IN4)	0.5oz	0.65
Prepreg	1080HRC	2.90
L8(VCC)	1oz	1.35
Core	3mil	3.09
L9(IN5)	1oz	1.35
Prepreg	1080LRC+1080	5.1
L10(IN6)	0.5oz	0.65
Core	3mil	3.09
L11(GND3)	0.5oz	0.65
Prepreg	1080LRC	2.65
Bottom/L12(signal)	0.5oz(0.68)	0.65
Add Plating	1.30	1.05
SolderMask	min 0.4	0.50
Overall Thickness	1.36mm+/-10%	53.36

PCH

USB PORT#	DESTINATION
0	JUSB1 (Ext Right Side)
1	none
2	Right Side (ESATA)
3	none
4	WLAN/WIMAX
5	WWAN/UWB
6	Flash
7	USH->BIO
8	DOCKING
9	DOCKING
10	Express card
11	Bluetooth
12	Camera
13	none

USH

0	BIO
1	NA

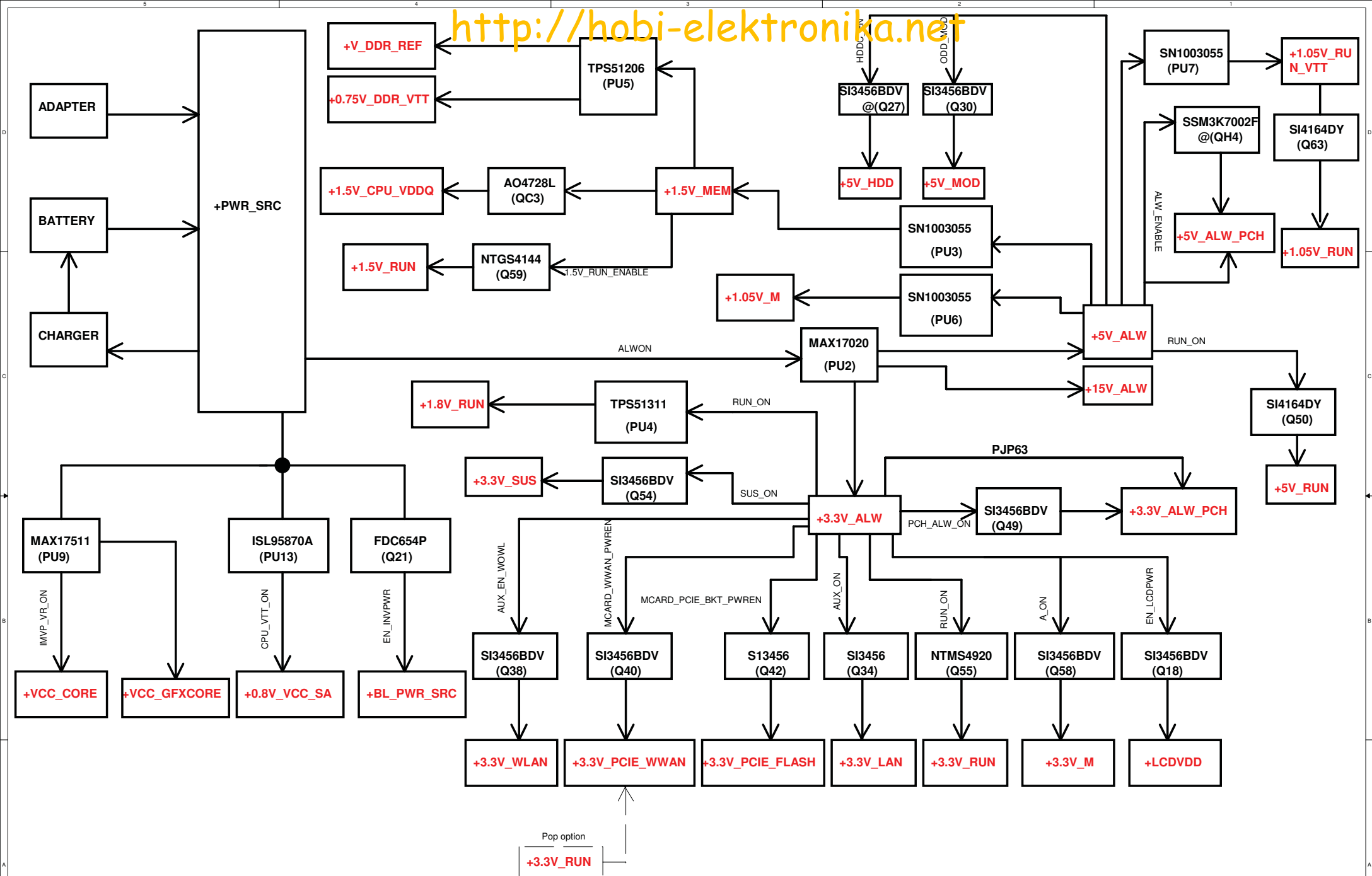
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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Index and Config.		
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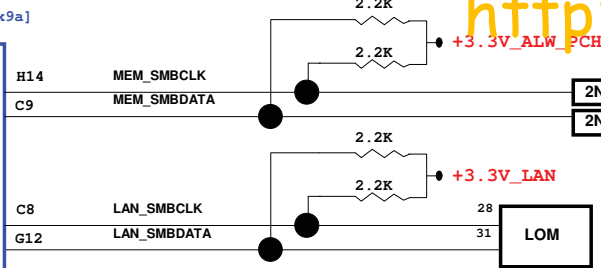
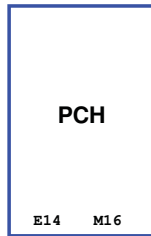


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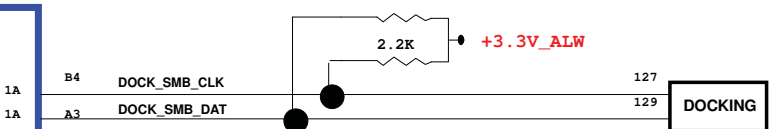
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Power Rail				
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SMBUS Address [0x9a]

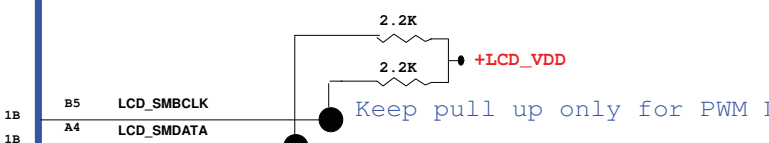


SMBUS Address [C8]

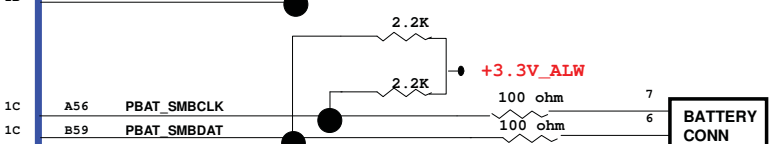


SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

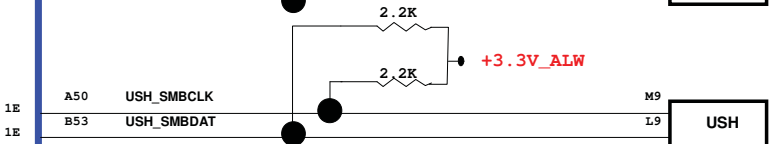
KBC



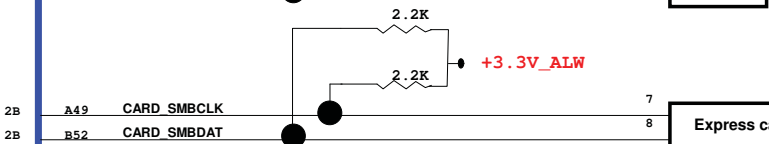
Keep pull up only for PWM LCD



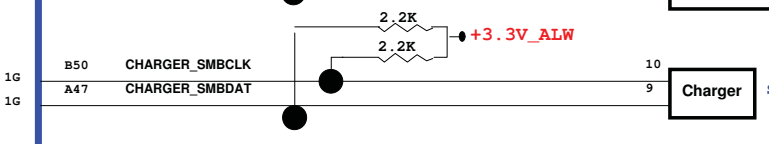
SMBUS Address [0x16]



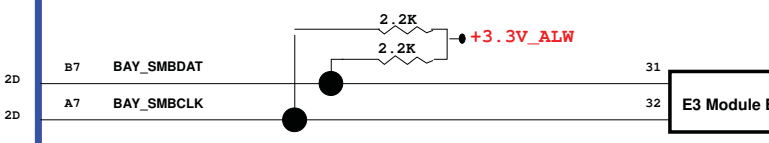
SMBUS Address [0xa4]



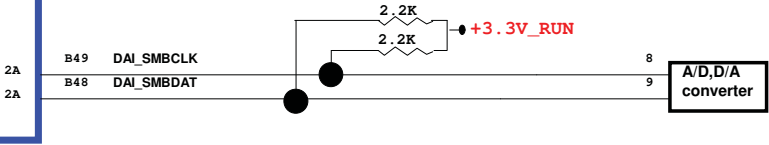
SMBUS Address [TBD]



SMBUS Address [0x12]



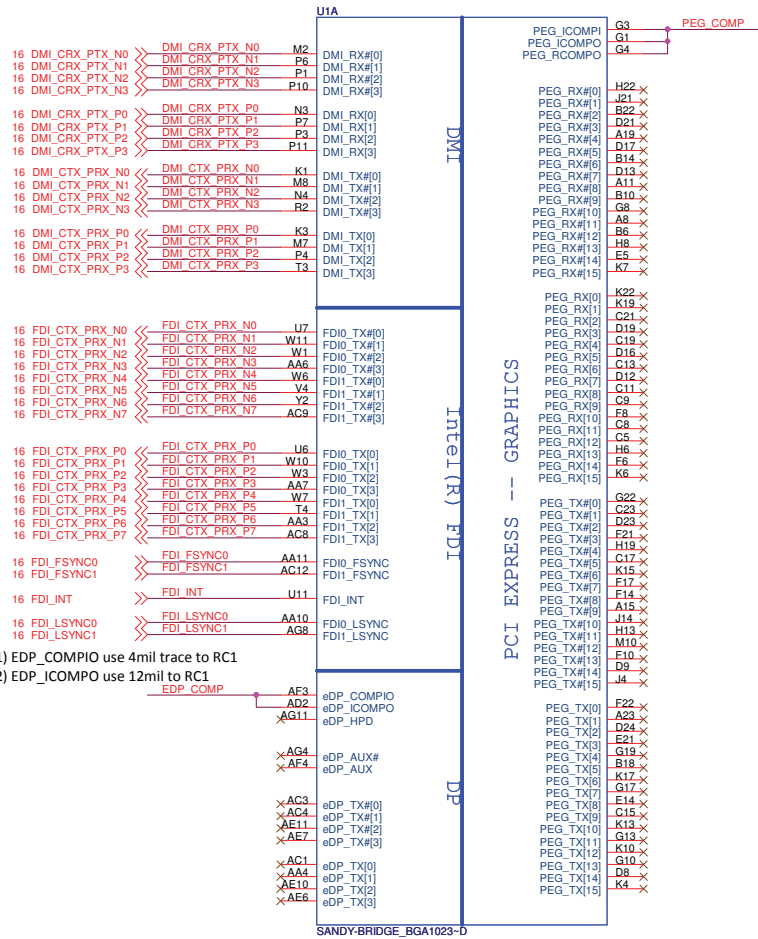
SMBUS Address [0xd2]



SMBUS Address [0x30]

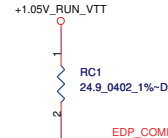
MEC 5055

- (1) PEG_RCOMP (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2
(2) PEG_ICOMPO use 12mil connect to RC2



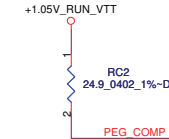
- (1) EDP_COMPIO use 4mil trace to RC1
(2) EDP_ICOMPO use 12mil to RC1

DP Compensation

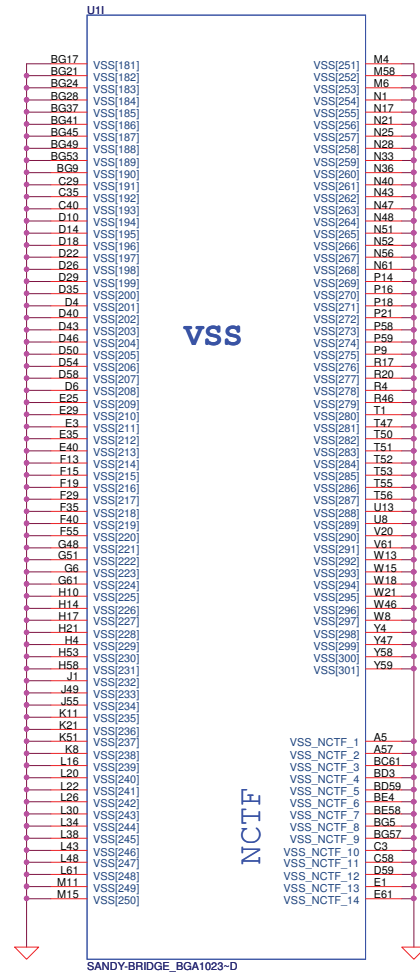


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG Compensation



PEG_ICOMPI and RCOMP signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



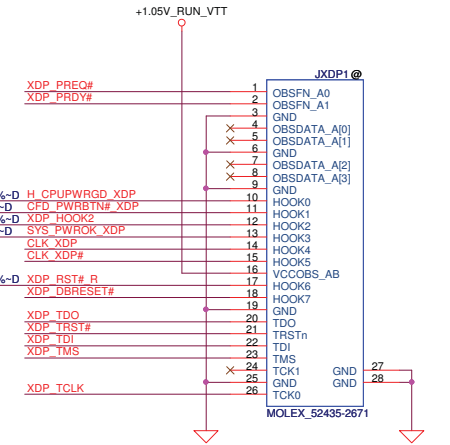
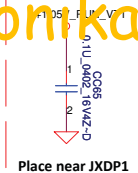
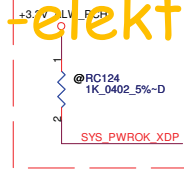
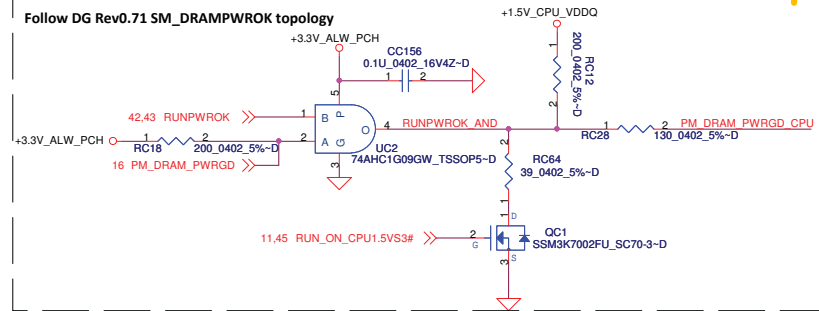
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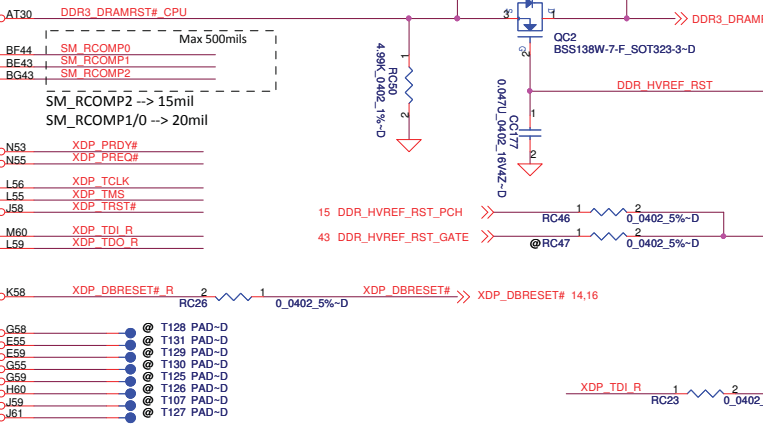
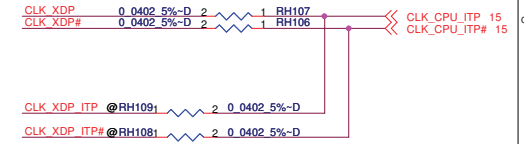
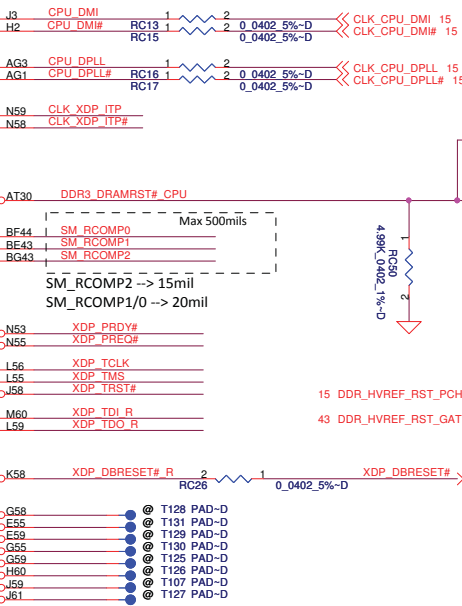
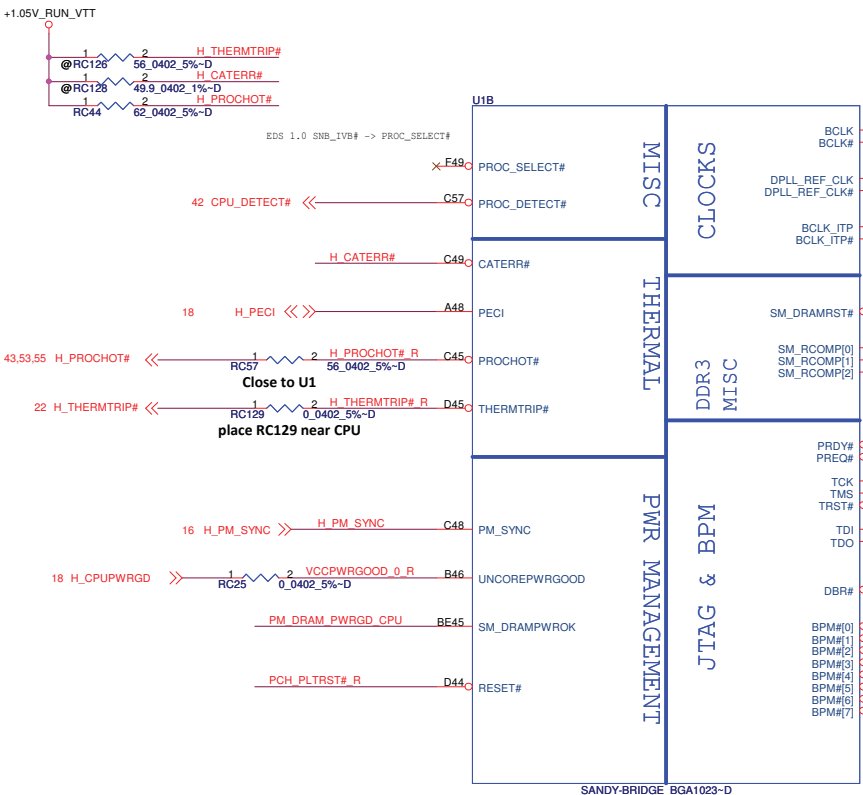
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Sandy Bridge (1/6)			
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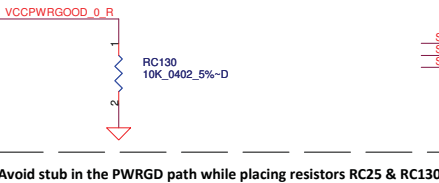
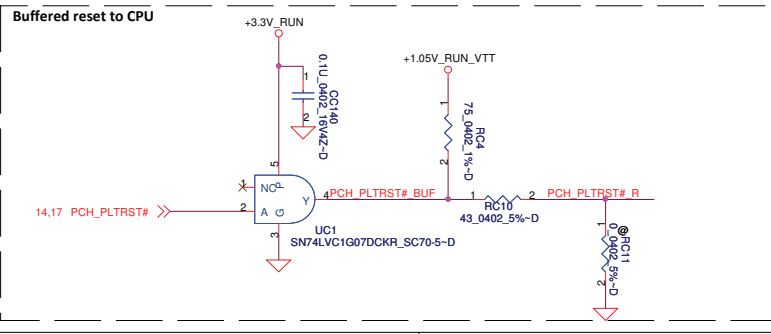
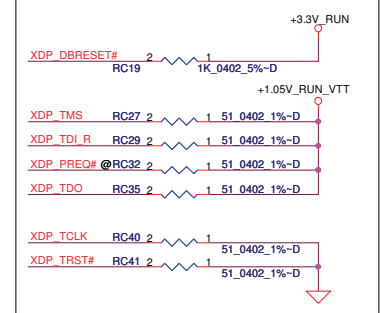
Follow DG Rev0.71 SM_DRAMPWROK topology



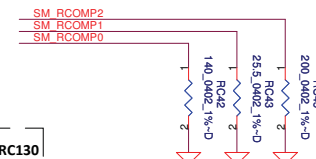
The resistor for HOOK2 should be replaced such that the stub is very small on CFG0 net



PU/PD for JTAG signals



Avoid stub in the PWRGD path while placing resistors RC25 & RC130



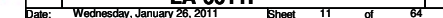
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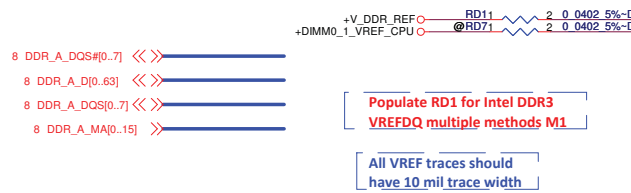
		Compal Electronics, Inc.	
Sandy Bridge (2/6)		LA-6611P	
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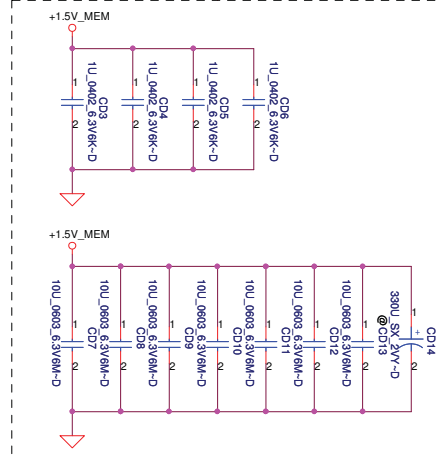


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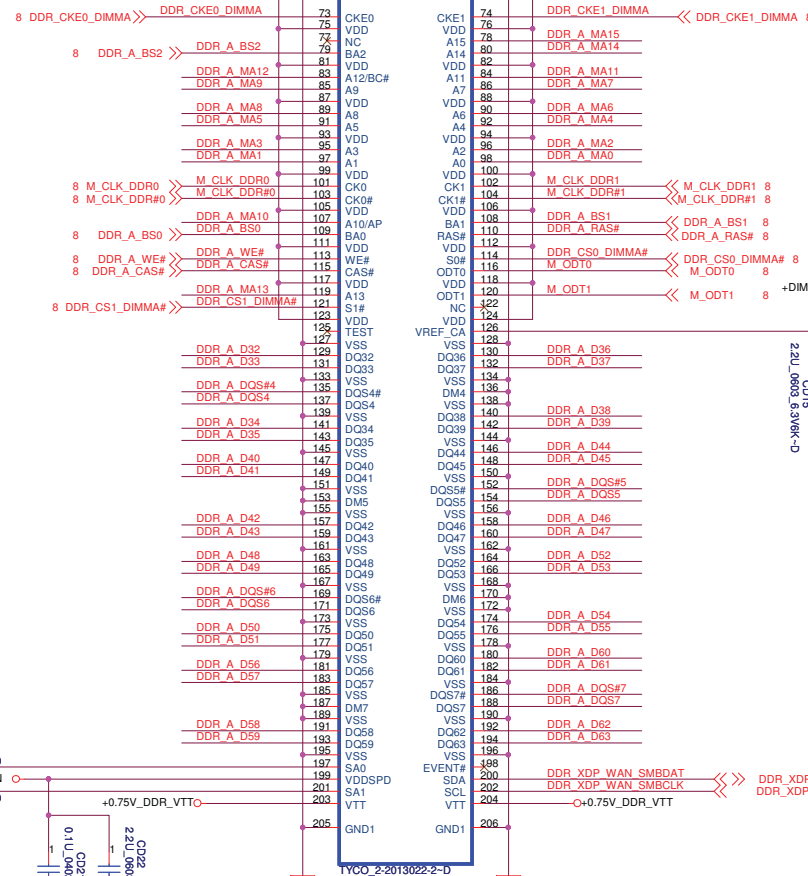
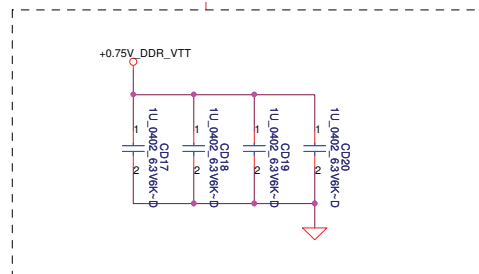




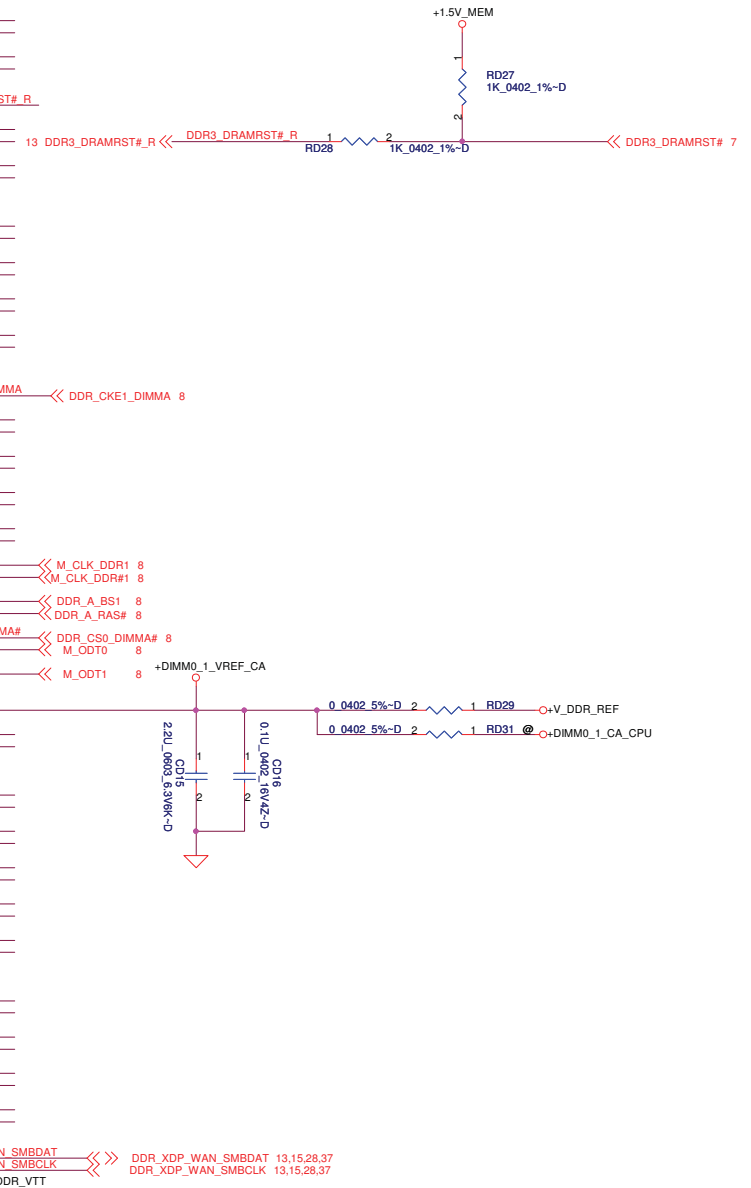
Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA.203,204



DIMMA H=4.0mm
Link Done



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DDRIII-SODIMM SLOT1

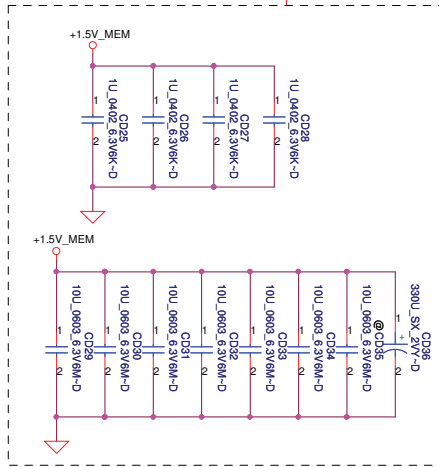
LA-6611P

0.3

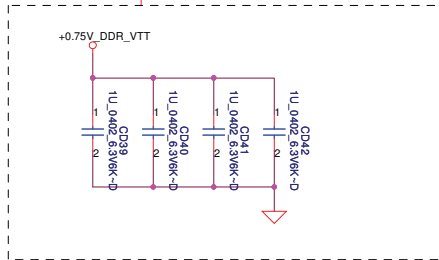
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8 DDR_B_DQS#[0..7] <<>>
8 DDR_B_D[0..63] <<>>
8 DDR_B_DQS[0..7] <<>>
8 DDR_B_MA[0..15] <<>>

Layout Note:
Place near JDIMMB



Layout Note:
Place near JDIMMB.203,204



Populate RD1 for intel DDR3
VREFDQ multiple methods M1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

+3.3V_RUN

+3.3V_RUN

+0.75V_DDR_VTT

+0.75V_DDR_VTT

+0.75V_DDR_VTT

+0.75V_DDR_VTT

+0.75V_DDR_VTT

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+0.75V_DDR_VTT

+0.75V_DDR_VTT

8 DDR_CKE2_DIMMB <<>>

8 DDR_BS2 <<>>

8 M_CLK_DDR2 <<>>

8 M_CLK_DDR2 <<>>

8 DDR_BS0 <<>>

8 DDR_WE# <<>>

8 DDR_CAS# <<>>

8 DDR_CS3_DIMMB# <<>>

8 DDR_CKE3_DIMMB <<>>

8 DDR_BS1 <<>>

8 M_CLK_DDR3 <<>>

8 M_CLK_DDR3 <<>>

8 DDR_BS1 <<>>

8 M_ODT2 <<>>

8 M_ODT2 <<>>

8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 DDR_CS3_DIMMB# <<>>

8 DDR_BS1 <<>>

8 M_CLK_DDR3 <<>>

8 M_CLK_DDR3 <<>>

8 DDR_BS1 <<>>

8 M_ODT2 <<>>

8 M_ODT2 <<>>

8 M_ODT3 <<>>

8 M_ODT3 <<>>

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8 M_ODT3 <<>>

8 DDR_BS1 <<>>

8 M_CLK_DDR3 <<>>

8 M_CLK_DDR3 <<>>

8 DDR_BS1 <<>>

8 M_ODT2 <<>>

8 M_ODT2 <<>>

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8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 DDR_BS1 <<>>

8 M_CLK_DDR3 <<>>

8 M_CLK_DDR3 <<>>

8 DDR_BS1 <<>>

8 M_ODT2 <<>>

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8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 DDR_BS1 <<>>

8 M_CLK_DDR3 <<>>

8 M_CLK_DDR3 <<>>

8 DDR_BS1 <<>>

8 M_ODT2 <<>>

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8 M_ODT3 <<>>

8 M_ODT3 <<>>

8 DDR_BS1 <<>>

8 M_CLK_DDR3 <<>>

8 M_CLK_DDR3 <<>>

8 DDR_BS1 <<>>

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8 M_ODT3 <<>>

DIMMB H=8mm Link Done

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DDRIII-SODIMM SLOT2

LA-6611P

Rev 0.3

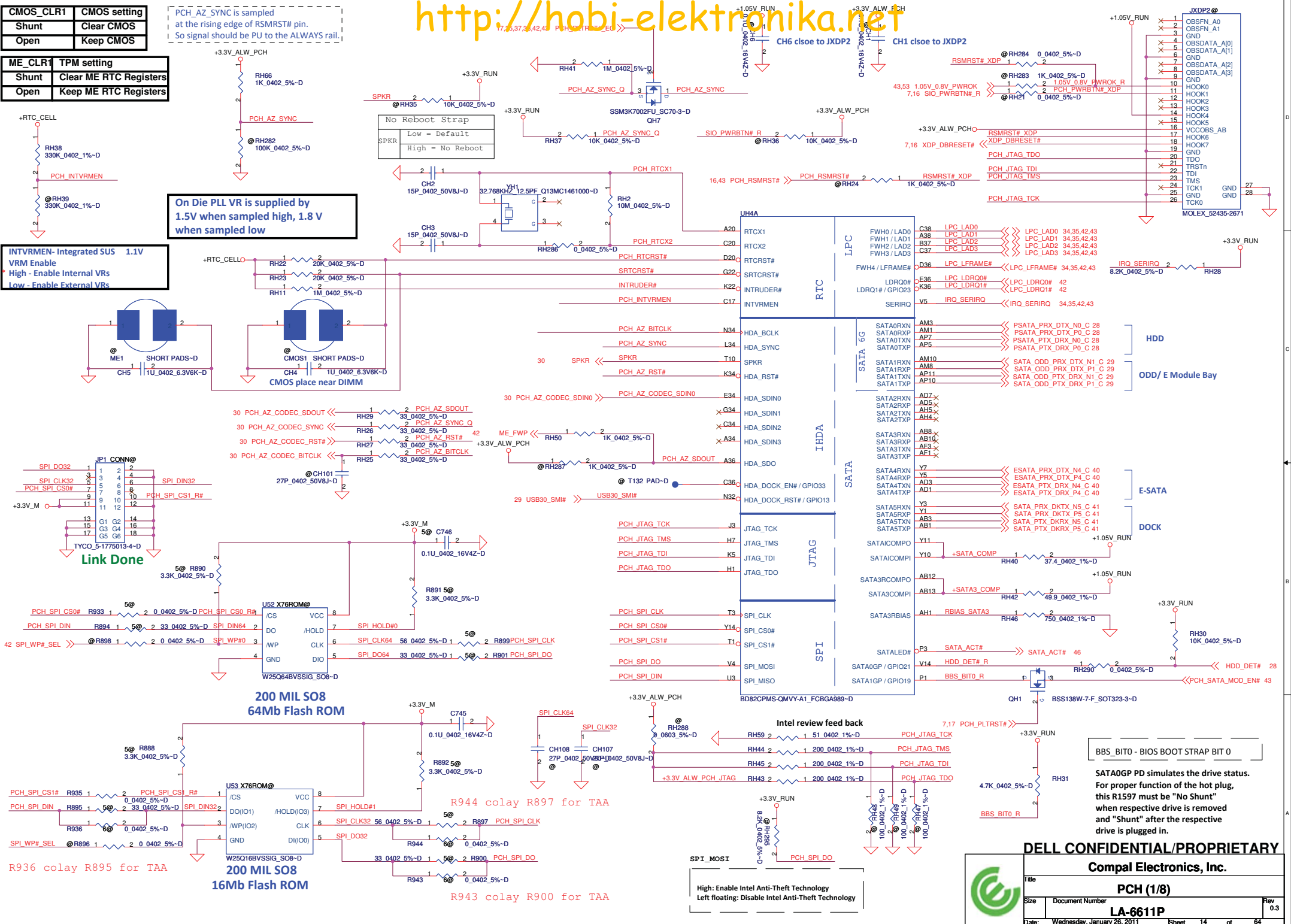
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ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS 1.1V
VRM Enable
• High - Enable Internal VRs
Low - Enable External VRs



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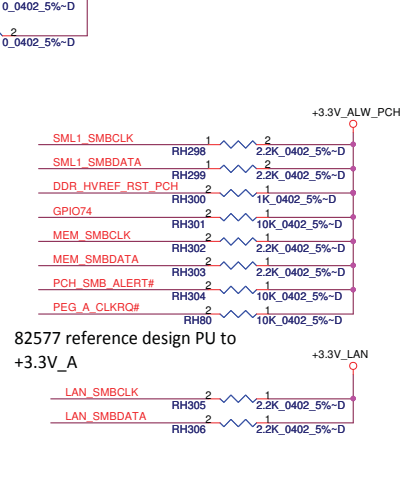
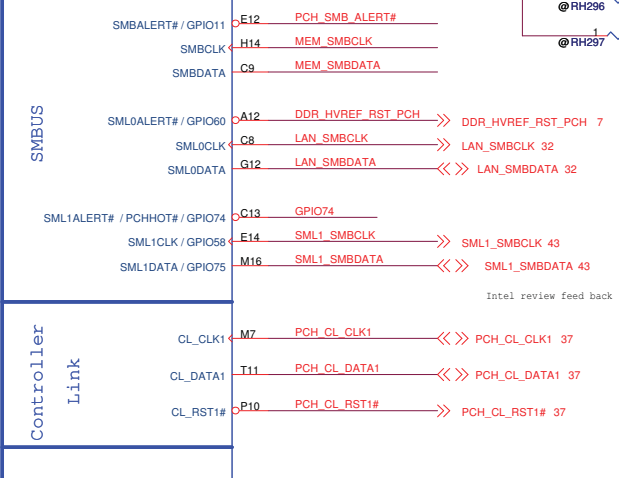
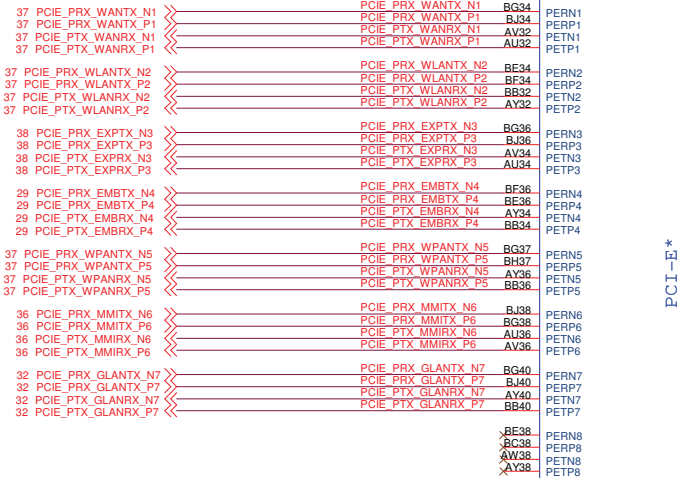
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PCH (1/8)

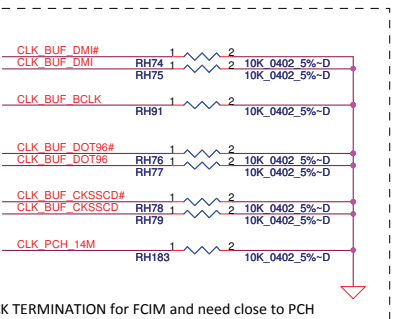
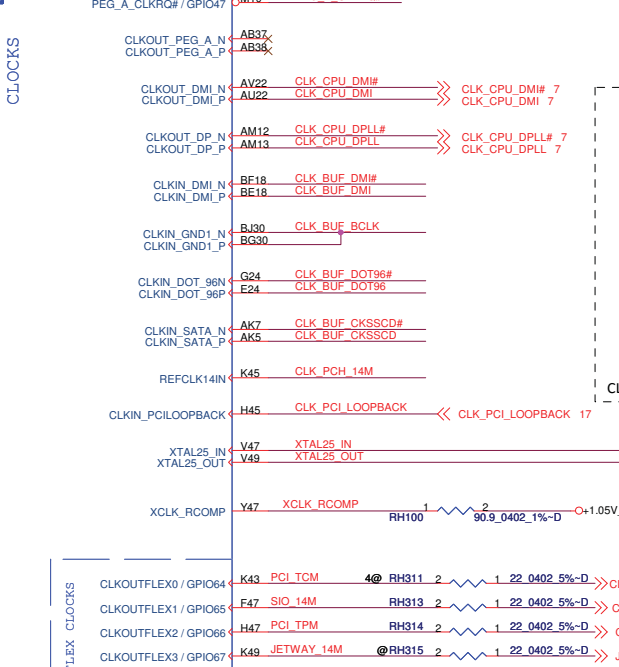
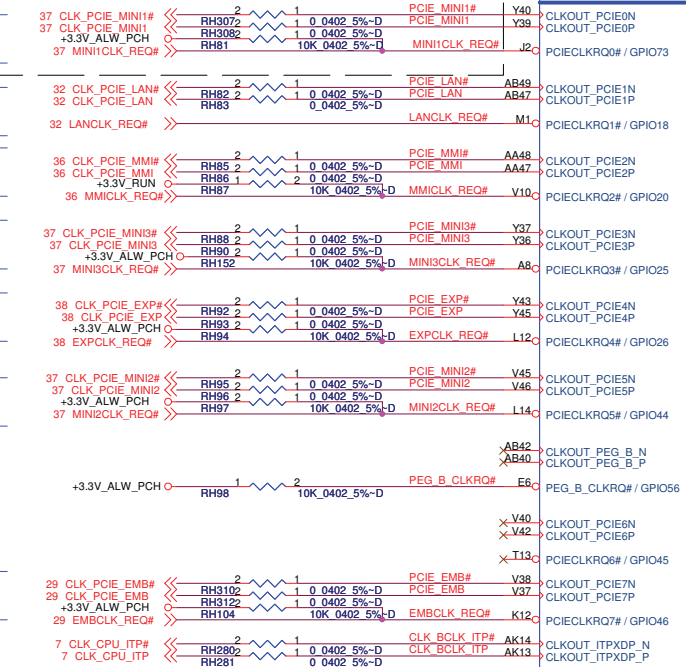
LA-6611P

Rev
0.3

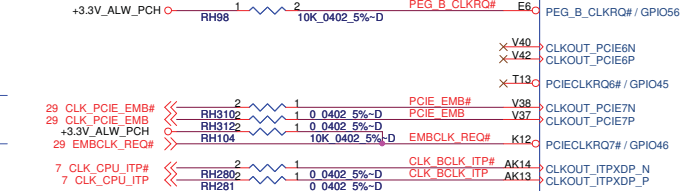
10/100/1G LAN --->



82577 reference design PU to
+3.3V_A



CLOCK TERMINATION for FCIM and need close to PCH



```
PCIE REQ power rail
suspend: 0 3 4 5 6 7
core: 1 2
```

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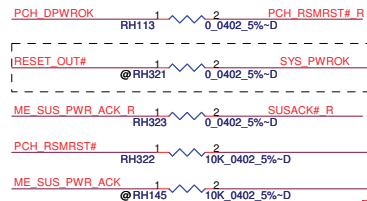
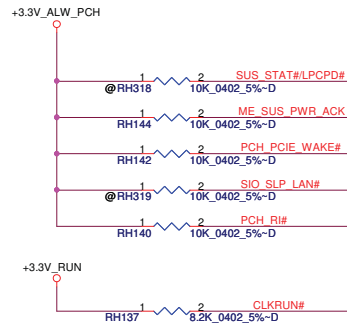
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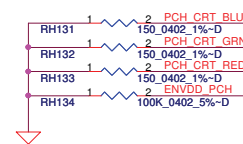
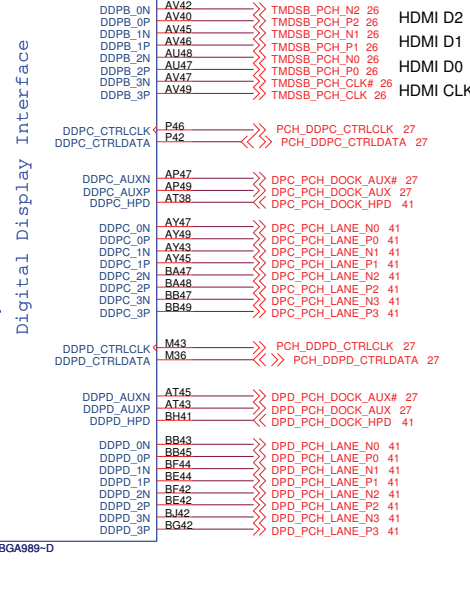
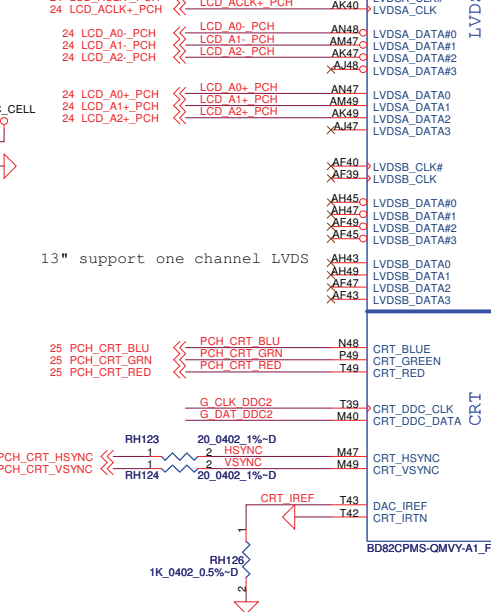
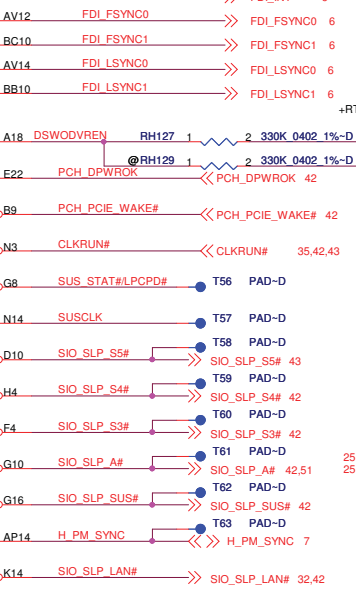
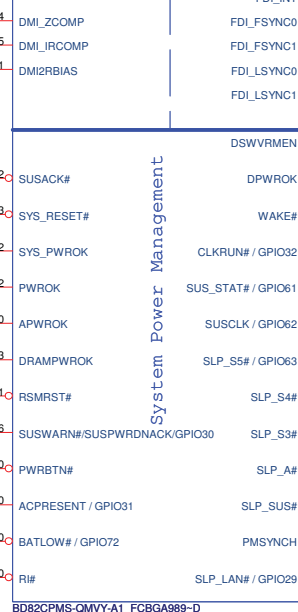
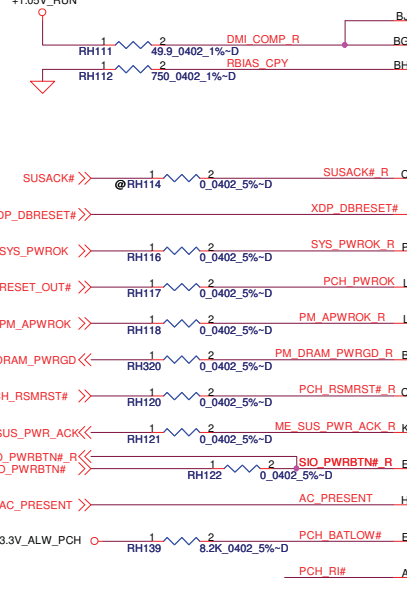
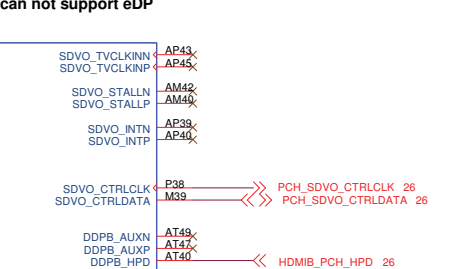
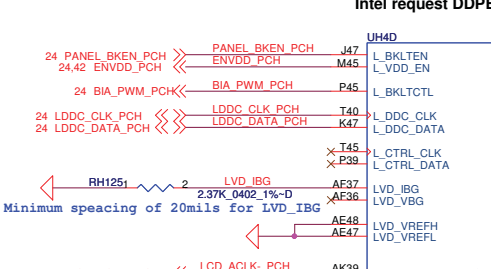
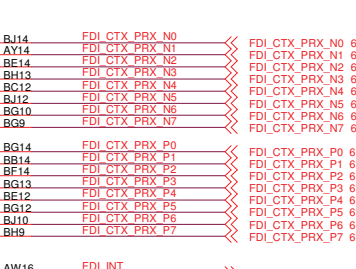
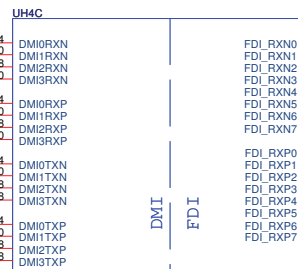
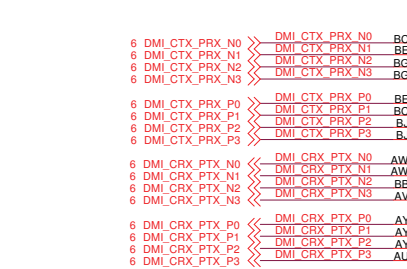
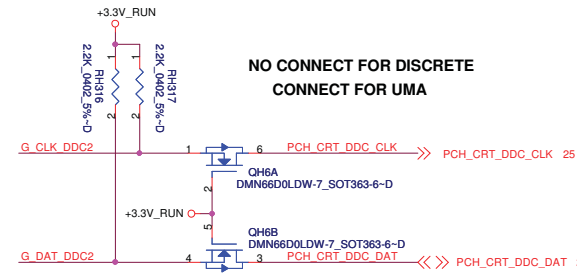
PCH (2/8)

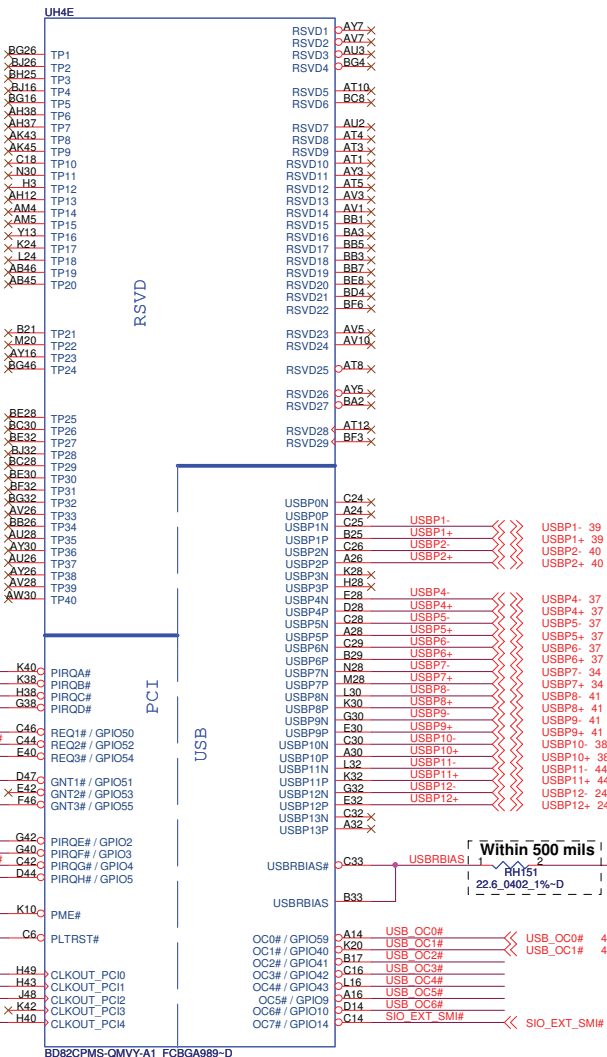
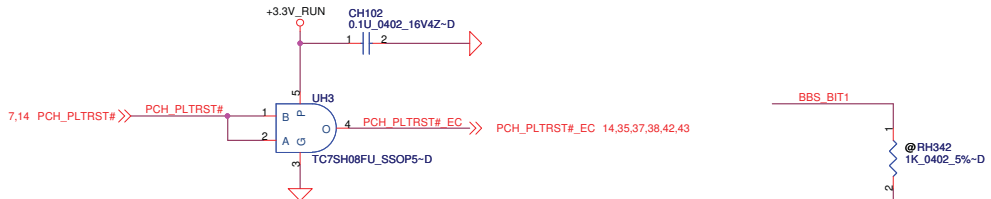
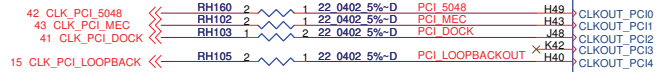
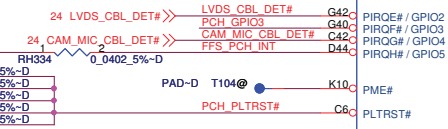
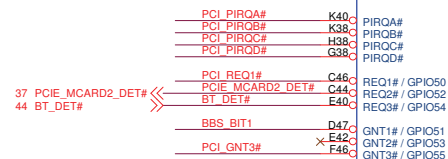
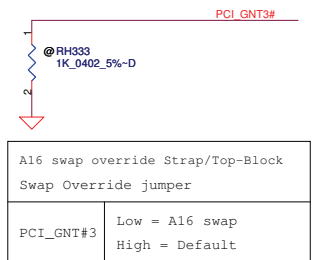
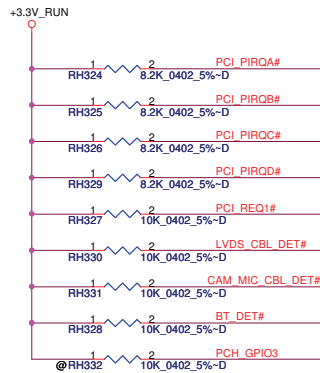
LA-6611P

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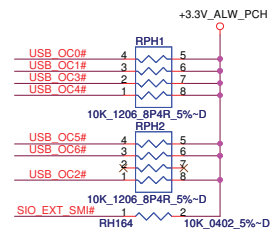


DSWODVREN - On Die DSW VR Enable	
Enabled (DEFAULT)	
HIGH: RH127 STUFFED, RH129 UNSTUFFED	
Disabled	
LOW: RH129 STUFFED, RH127 UNSTUFFED	





- >Right Side
- >Right Side (ESATA)
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >DOCK
- >Express Card
- >Blue Tooth
- >Camera



Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

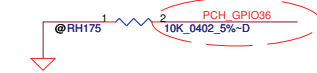
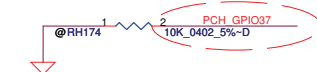
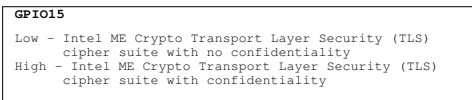
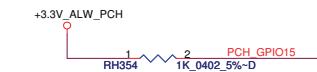
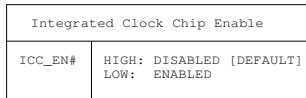
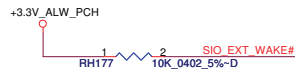
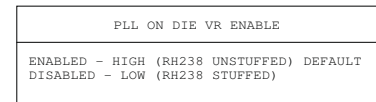
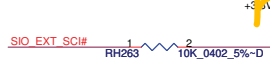
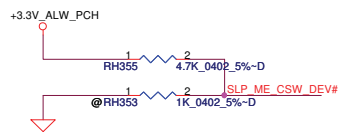
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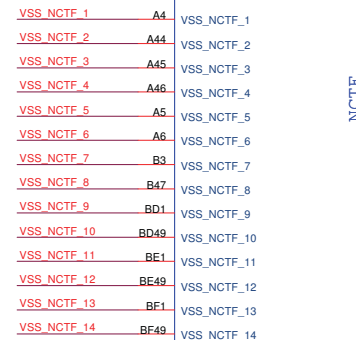
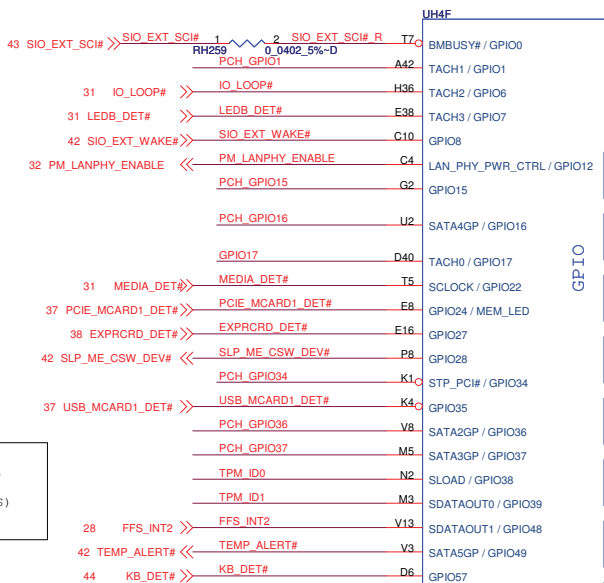
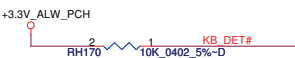
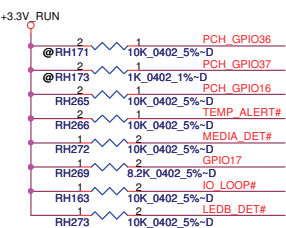
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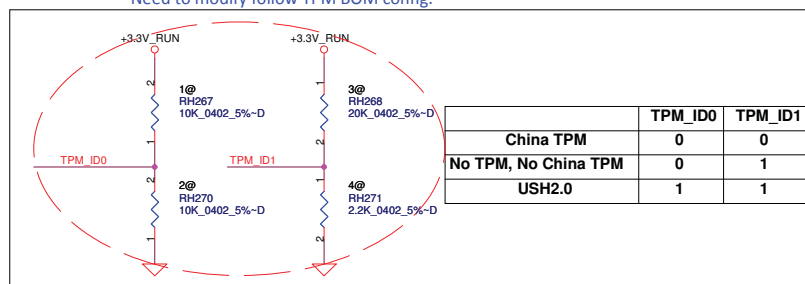


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

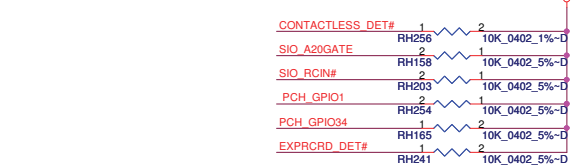
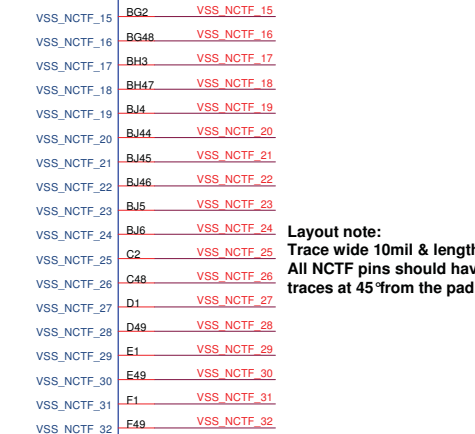
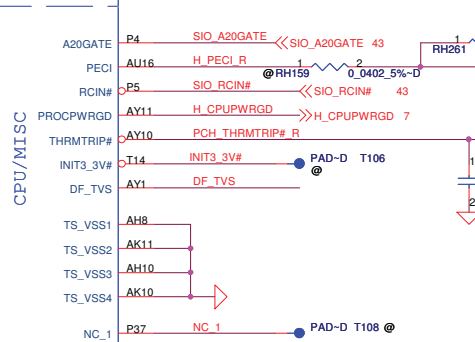
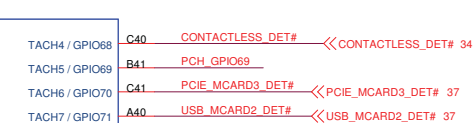


BD82CPMS-QM VY-A1_FCBGA989-D

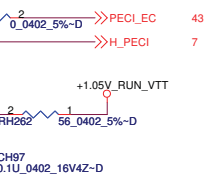
Need to modify follow TPM BOM config.



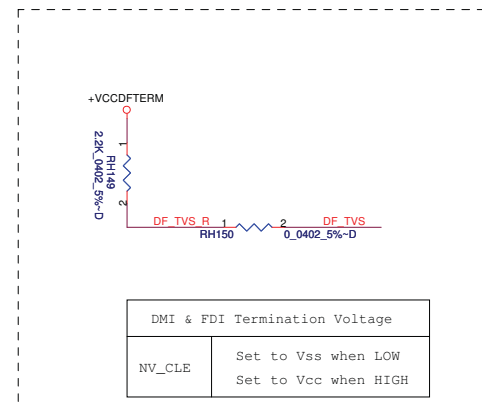
	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH2.0	1	1



GPIO27 (EXPRCRD_DET#)
Default = Do not connect (floating)
High (1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

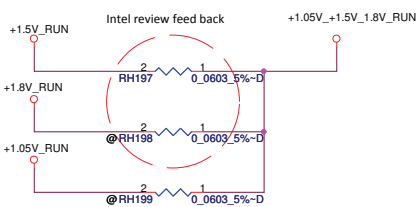
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PCH (5/8)

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UH4H		
H5	VSS[0]	
AA1.7	VSS[1]	AK38
AA2	VSS[2]	VSS[80]
AA3	VSS[3]	VSS[81]
AA3.3	VSS[4]	VSS[82]
AA3.4	VSS[5]	VSS[83]
AB1.1	VSS[6]	VSS[84]
AB1.4	VSS[7]	VSS[85]
AB3.9	VSS[8]	VSS[86]
AB4	VSS[9]	VSS[87]
AB4.3	VSS[10]	VSS[88]
AB5	VSS[11]	VSS[89]
AB7	VSS[12]	VSS[90]
AC1.9	VSS[13]	VSS[91]
AC2	VSS[14]	VSS[92]
AC2.1	VSS[15]	VSS[93]
AC2.4	VSS[16]	VSS[94]
AC3.3	VSS[17]	VSS[95]
AC3.4	VSS[18]	VSS[96]
AC4.8	VSS[19]	VSS[97]
AD1.0	VSS[20]	VSS[98]
AD1.1	VSS[21]	VSS[99]
AD1.2	VSS[22]	VSS[100]
AD1.3	VSS[23]	VSS[101]
AD1.9	VSS[24]	VSS[102]
AD2.4	VSS[25]	VSS[103]
AD2.6	VSS[26]	VSS[104]
AD2.7	VSS[27]	VSS[105]
AD3.3	VSS[28]	VSS[106]
AD3.4	VSS[29]	VSS[107]
AD3.6	VSS[30]	VSS[108]
AD3.7	VSS[31]	VSS[109]
AD3.8	VSS[32]	VSS[110]
AD3.9	VSS[33]	VSS[111]
AD4	VSS[34]	VSS[112]
AD4.0	VSS[35]	VSS[113]
AD4.2	VSS[36]	VSS[114]
AD4.3	VSS[37]	VSS[115]
AD4.5	VSS[38]	VSS[116]
AD4.6	VSS[39]	VSS[117]
AD8	VSS[40]	VSS[118]
AE2	VSS[41]	VSS[119]
AE3	VSS[42]	VSS[120]
AF1.0	VSS[43]	VSS[121]
AF1.2	VSS[44]	VSS[122]
AD1.4	VSS[45]	VSS[123]
AD1.6	VSS[46]	VSS[124]
AF1.6	VSS[47]	VSS[125]
AF1.9	VSS[48]	VSS[126]
AF2.4	VSS[49]	VSS[127]
AF2.6	VSS[50]	VSS[128]
AF2.7	VSS[51]	VSS[129]
AF2.9	VSS[52]	VSS[130]
AF3.1	VSS[53]	VSS[131]
AF3.8	VSS[54]	VSS[132]
AF4	VSS[55]	VSS[133]
AF4.2	VSS[56]	VSS[134]
AF4.6	VSS[57]	VSS[135]
AF5	VSS[58]	VSS[136]
AF7	VSS[59]	VSS[137]
AF8	VSS[60]	VSS[138]
AG1.9	VSS[61]	VSS[139]
AG2	VSS[62]	VSS[140]
AG3.1	VSS[63]	VSS[141]
AG4.8	VSS[64]	VSS[142]
AH1.1	VSS[65]	VSS[143]
AH3	VSS[66]	VSS[144]
AH3.6	VSS[67]	VSS[145]
AH3.9	VSS[68]	VSS[146]
AH4.0	VSS[69]	VSS[147]
AH4.2	VSS[70]	VSS[148]
AH4.6	VSS[71]	VSS[149]
AH7	VSS[72]	VSS[150]
AJ1.9	VSS[73]	VSS[151]
AJ2.1	VSS[74]	VSS[152]
AJ2.4	VSS[75]	VSS[153]
AJ3.3	VSS[76]	VSS[154]
AJ3.4	VSS[77]	VSS[155]
AK1.2	VSS[78]	VSS[156]
AK3	VSS[79]	VSS[157]
		VSS[158]

BD82CPMS-QMVFY-A1_FCBGA989-D

UH4H		
AY4	VSS[159]	H46
AY4.2	VSS[160]	VSS[259]
AY4.6	VSS[161]	VSS[260]
AY8	VSS[162]	VSS[261]
B1.1	VSS[163]	VSS[262]
B1.5	VSS[164]	VSS[263]
B1.9	VSS[165]	VSS[264]
B2.3	VSS[166]	VSS[265]
B2.7	VSS[167]	VSS[266]
B3.1	VSS[168]	VSS[267]
B3.5	VSS[169]	VSS[268]
B3.9	VSS[170]	VSS[269]
B7	VSS[171]	VSS[270]
F4.5	VSS[172]	VSS[271]
BB1.2	VSS[173]	VSS[272]
BB1.6	VSS[174]	VSS[273]
BB2.0	VSS[175]	VSS[274]
BB2.2	VSS[176]	VSS[275]
BB2.4	VSS[177]	VSS[276]
BB2.8	VSS[178]	VSS[277]
BB3.0	VSS[179]	VSS[278]
BB3.8	VSS[180]	VSS[279]
BB4	VSS[181]	VSS[280]
BB4.6	VSS[182]	VSS[281]
BC1.4	VSS[183]	VSS[282]
BC1.8	VSS[184]	VSS[283]
BC2	VSS[185]	VSS[284]
BC2.2	VSS[186]	VSS[285]
BC2.6	VSS[187]	VSS[286]
BC3.2	VSS[188]	VSS[287]
BC3.4	VSS[189]	VSS[288]
BC3.6	VSS[190]	VSS[289]
BC4.0	VSS[191]	VSS[290]
BC4.2	VSS[192]	VSS[291]
BC4.8	VSS[193]	VSS[292]
BD.22	VSS[194]	VSS[293]
BD5	VSS[195]	VSS[294]
AP1.2	VSS[196]	VSS[295]
BE2.6	VSS[197]	VSS[296]
BE4.0	VSS[198]	VSS[297]
BF1.0	VSS[199]	VSS[298]
BF1.2	VSS[200]	VSS[299]
BF1.6	VSS[201]	VSS[300]
BF2.0	VSS[202]	VSS[301]
BF2.2	VSS[203]	VSS[302]
BF2.4	VSS[204]	VSS[303]
BF2.6	VSS[205]	VSS[304]
BF2.8	VSS[206]	VSS[305]
BD3	VSS[207]	VSS[306]
BF3.0	VSS[208]	VSS[307]
AT1.3.8	VSS[209]	VSS[308]
BF4.0	VSS[210]	VSS[309]
BF8	VSS[211]	VSS[310]
BG1.7	VSS[212]	VSS[311]
BG2.1	VSS[213]	VSS[312]
BG3.3	VSS[214]	VSS[313]
BG4.4	VSS[215]	VSS[314]
BG8	VSS[216]	VSS[315]
BH1.1	VSS[217]	VSS[316]
BH1.5	VSS[218]	VSS[317]
BH1.7	VSS[219]	VSS[318]
BH1.9	VSS[220]	VSS[319]
H1.0	VSS[221]	VSS[320]
BH2.7	VSS[222]	VSS[321]
BH3.1	VSS[223]	VSS[322]
BH3.3	VSS[224]	VSS[323]
BH3.5	VSS[225]	VSS[324]
BH3.9	VSS[226]	VSS[325]
BH4.3	VSS[227]	VSS[326]
BH7	VSS[228]	VSS[327]
D3	VSS[229]	VSS[328]
D12	VSS[230]	VSS[329]
D16	VSS[231]	VSS[330]
D18	VSS[232]	VSS[331]
D22	VSS[233]	VSS[332]
D24	VSS[234]	VSS[333]
D26	VSS[235]	VSS[334]
D30	VSS[236]	VSS[335]
D32	VSS[237]	VSS[336]
D34	VSS[238]	VSS[337]
D38	VSS[239]	VSS[338]
D42	VSS[240]	VSS[339]
D8	VSS[241]	VSS[340]
E1.8	VSS[242]	VSS[341]
E28	VSS[243]	VSS[342]
G1.8	VSS[244]	VSS[343]
G20	VSS[245]	VSS[344]
G26	VSS[246]	VSS[345]
G28	VSS[247]	VSS[346]
G36	VSS[248]	VSS[347]
G48	VSS[249]	VSS[348]
H12	VSS[250]	VSS[349]
H22	VSS[251]	VSS[350]
H24	VSS[252]	VSS[351]
H26	VSS[253]	VSS[352]
H30	VSS[254]	
H32	VSS[255]	
H34	VSS[256]	
F3	VSS[257]	
	VSS[258]	

BD82CPMS-QMVFY-A1_FCBGA989-D

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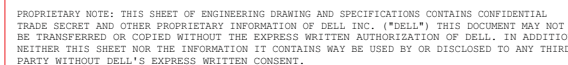


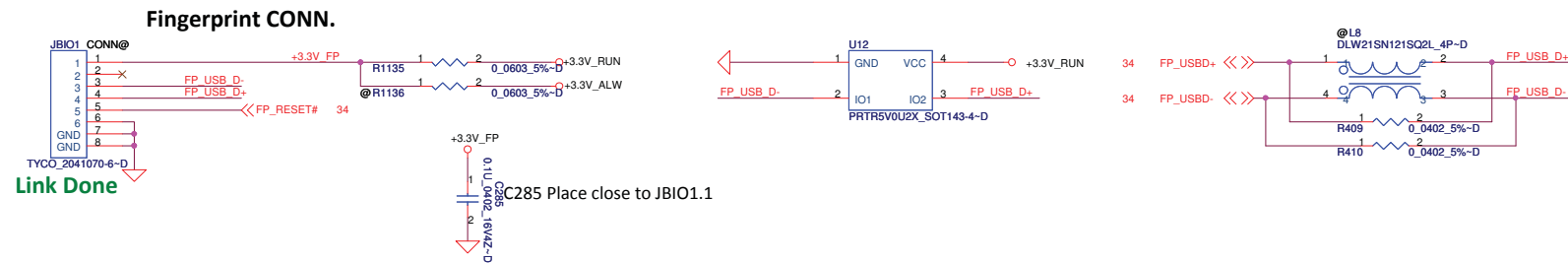
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Size	Document Number	Rev
	LA-6611P	0.3
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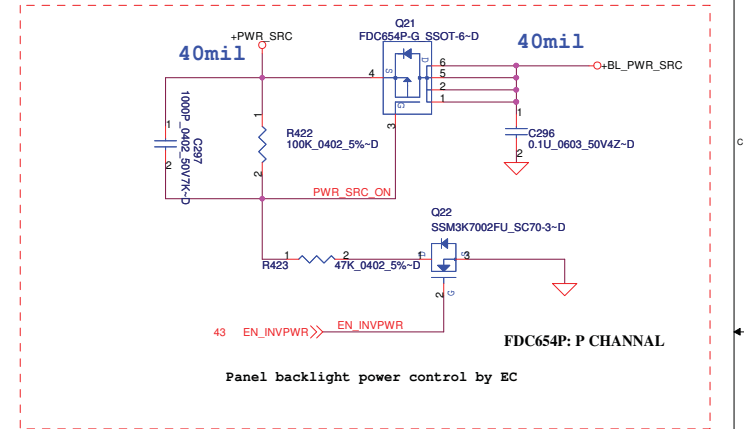
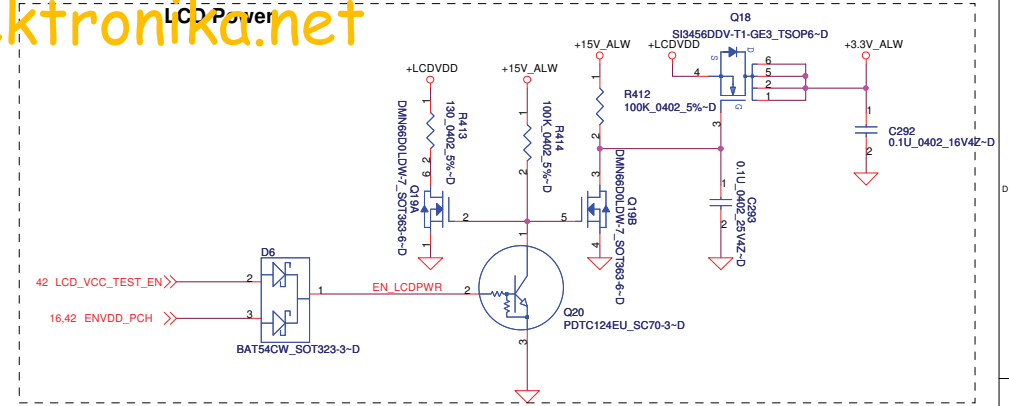
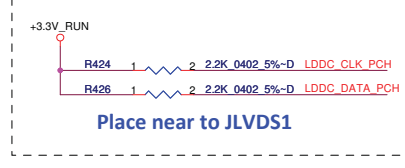
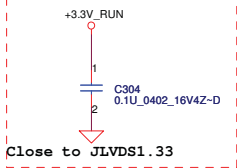
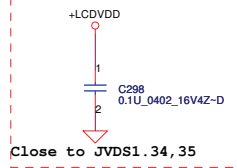
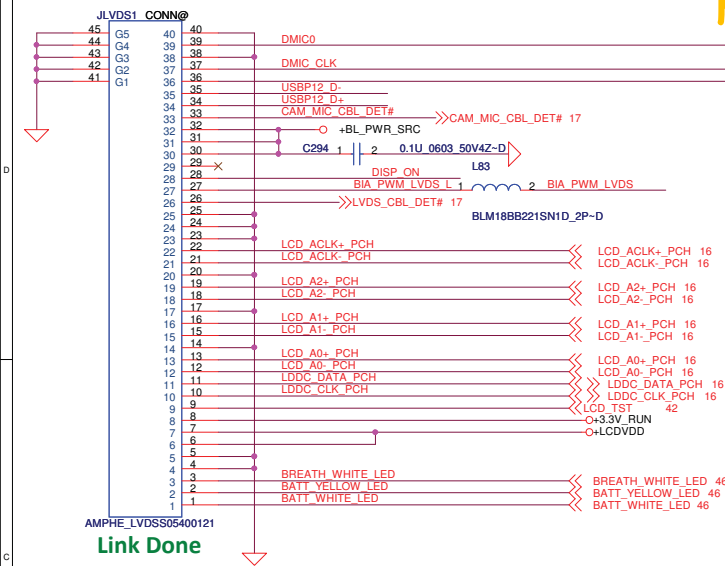
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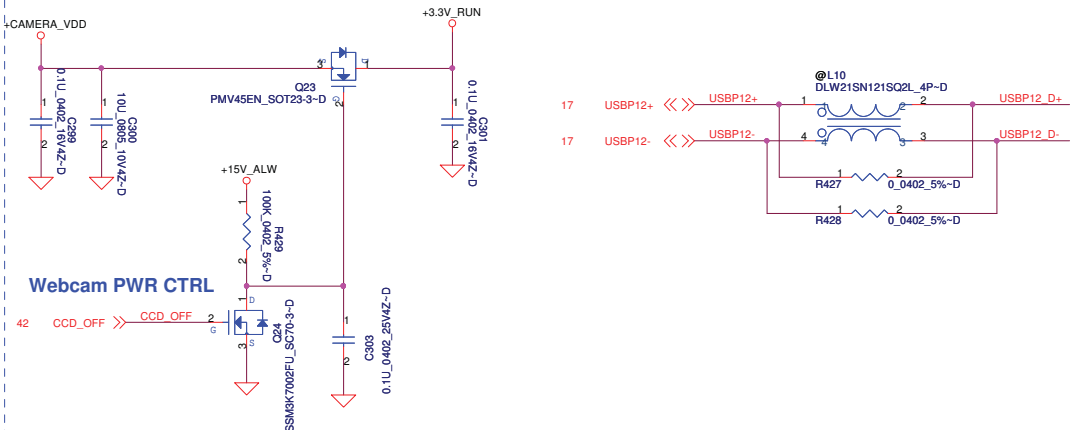
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For Webcam

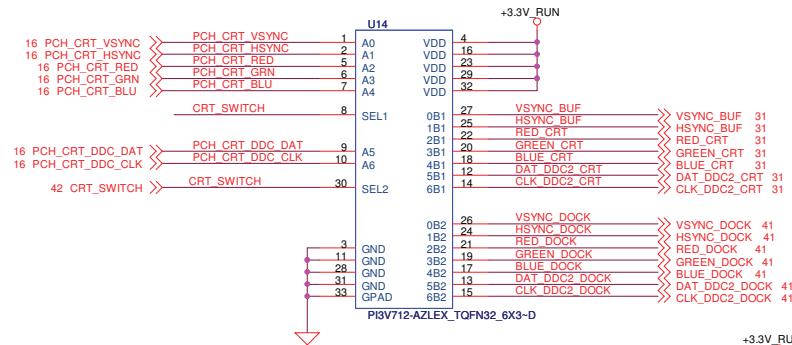


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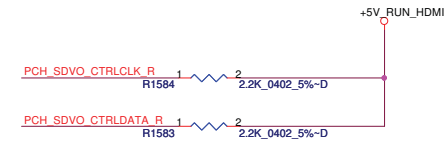
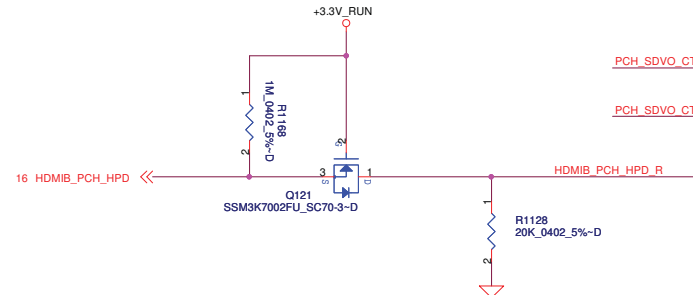
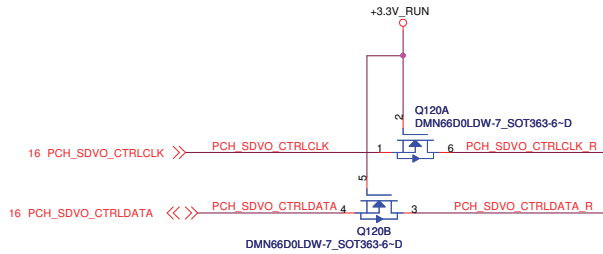
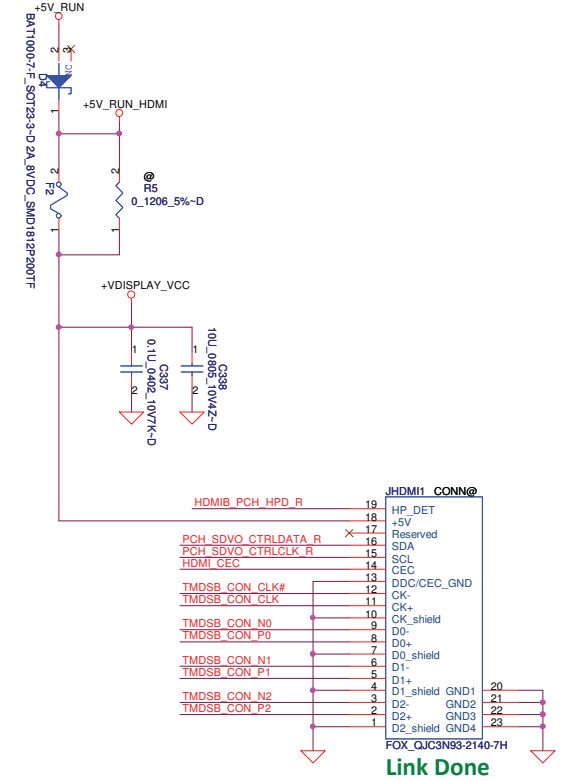
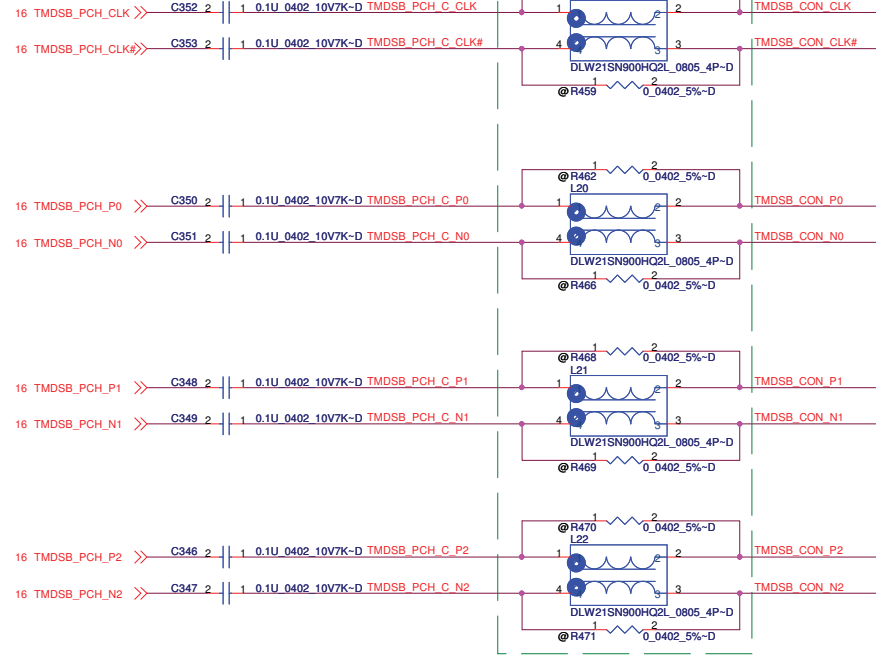
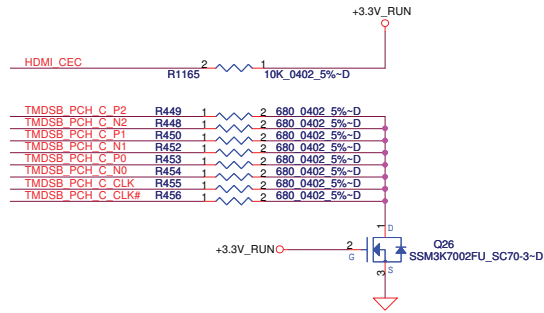
VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

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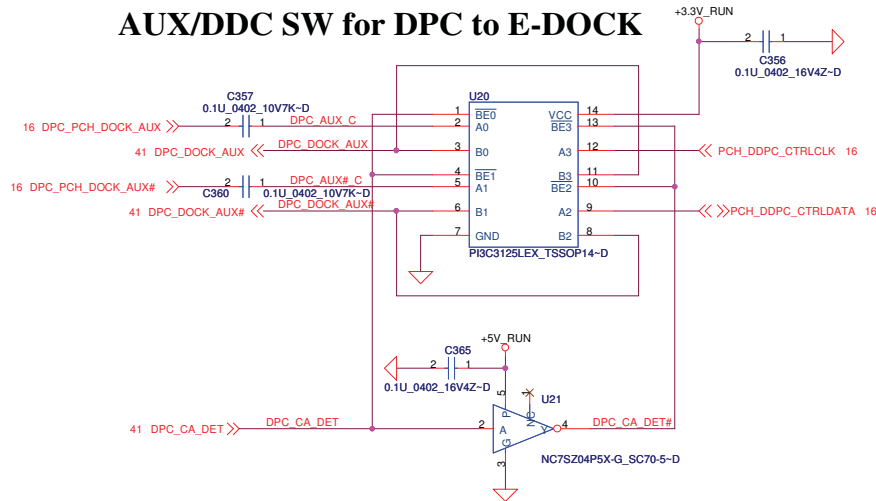
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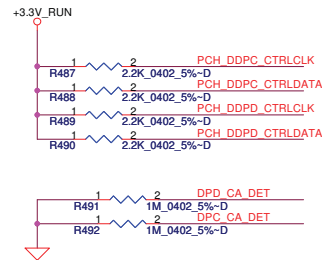
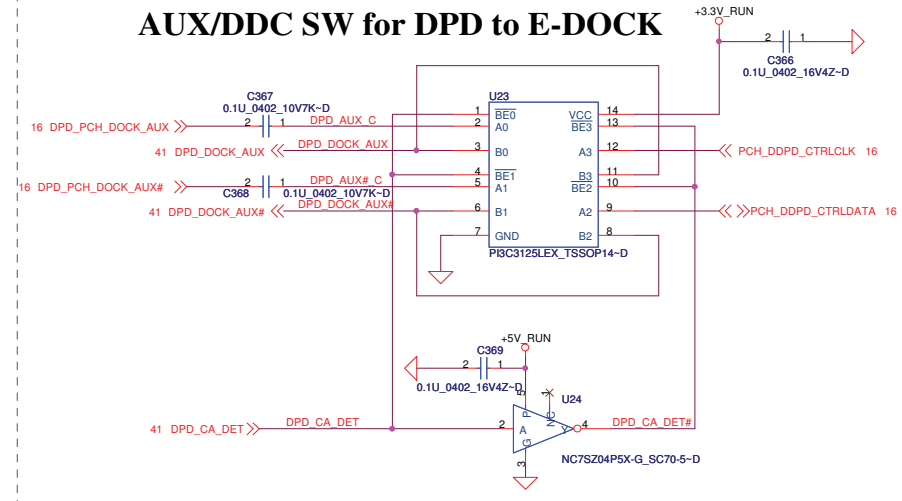


HDMI port			Rev
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AUX/DDC SW for DPC to E-DOCK



AUX/DDC SW for DPD to E-DOCK



Intel WW18 Strapping option

Intel WW18 Strapping option

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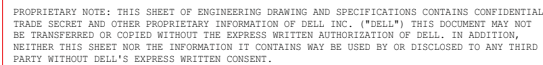
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	DP SW		
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22



SA00003LH1L SA00003ZX0L

MAXIM	TI
pop	depop
depop	pop

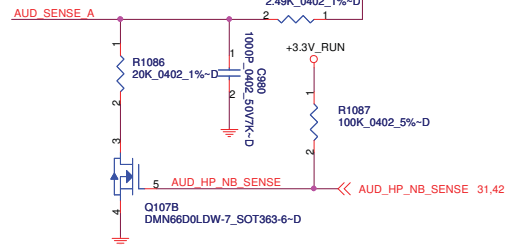
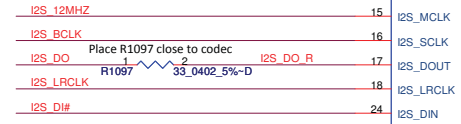
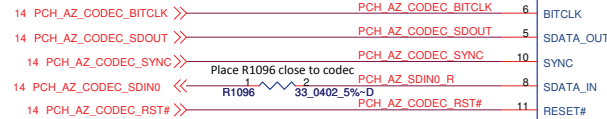
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Size	Document Number	Rev
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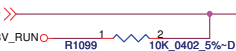
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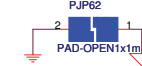
Link Done
Speaker Connector



Place closely to Pin 14

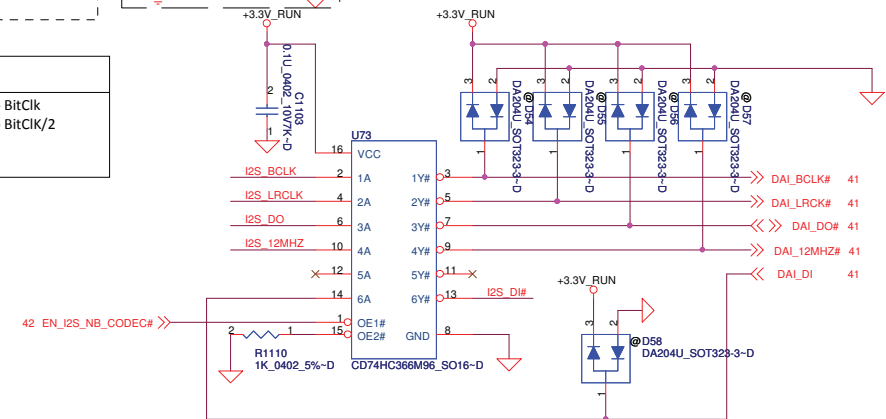
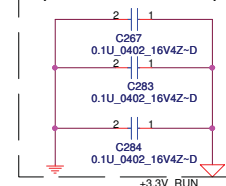


Tie Analog Ground to Digital ground under codec by a single point



Resistor	SENSE_A	SENSE_B
39.2K	PORT A (HP0)	PORT E
20K	PORT B (HP1)	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

place at GNDA and DGND plane

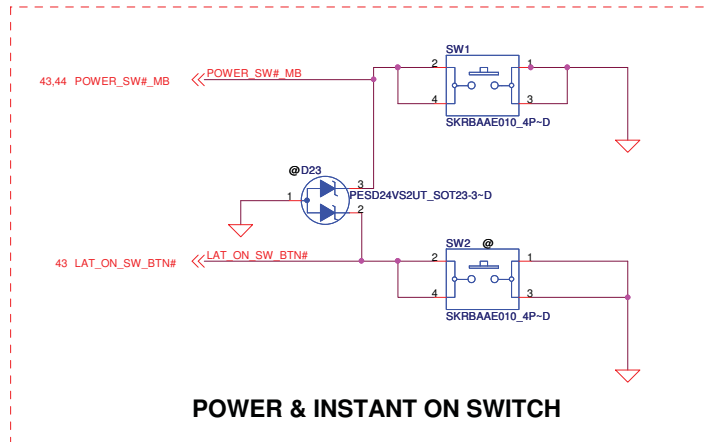


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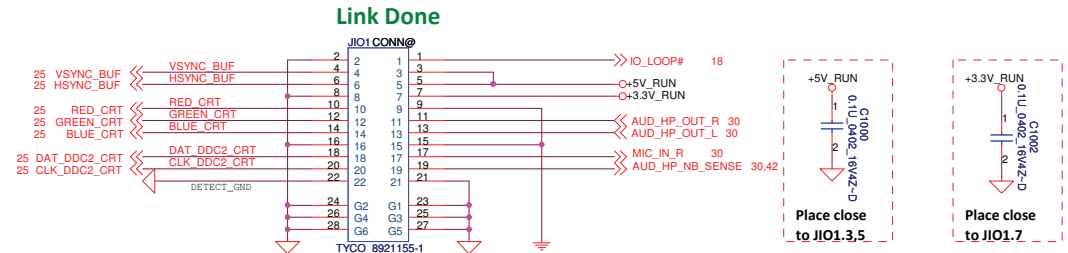
Azalia (HD) Codec

LA-6611P

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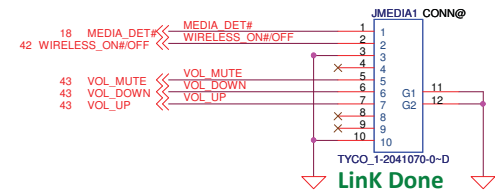


I/O board CONN. LS-6611P

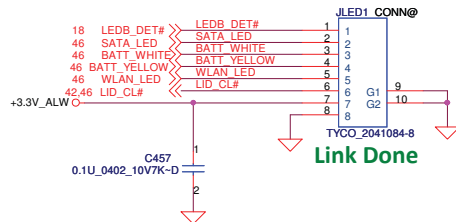


Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

Media Board LS-6613P



LED Board with Lid LS-6612P

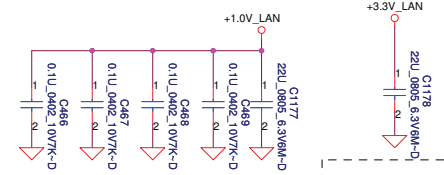


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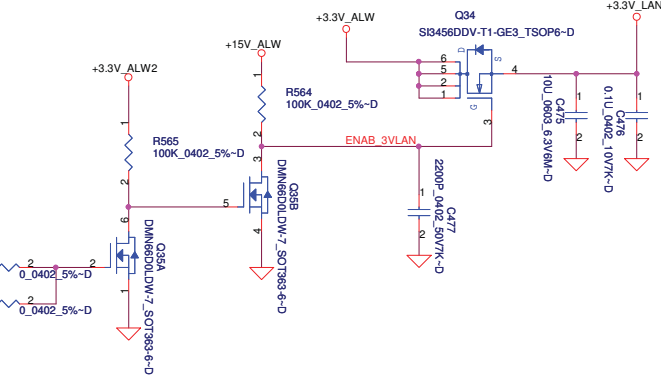
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Size	Document Number	Rev	
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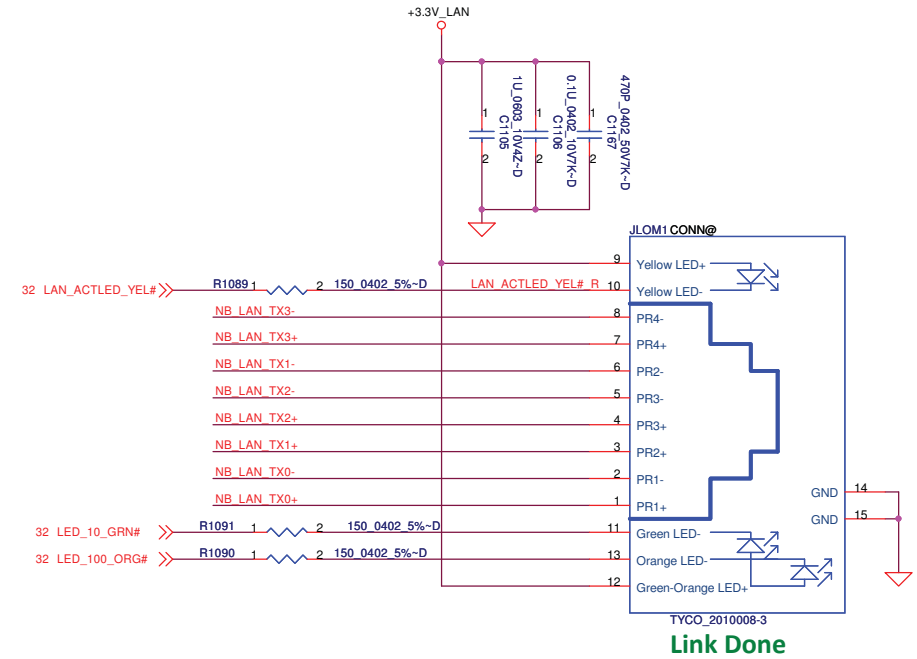
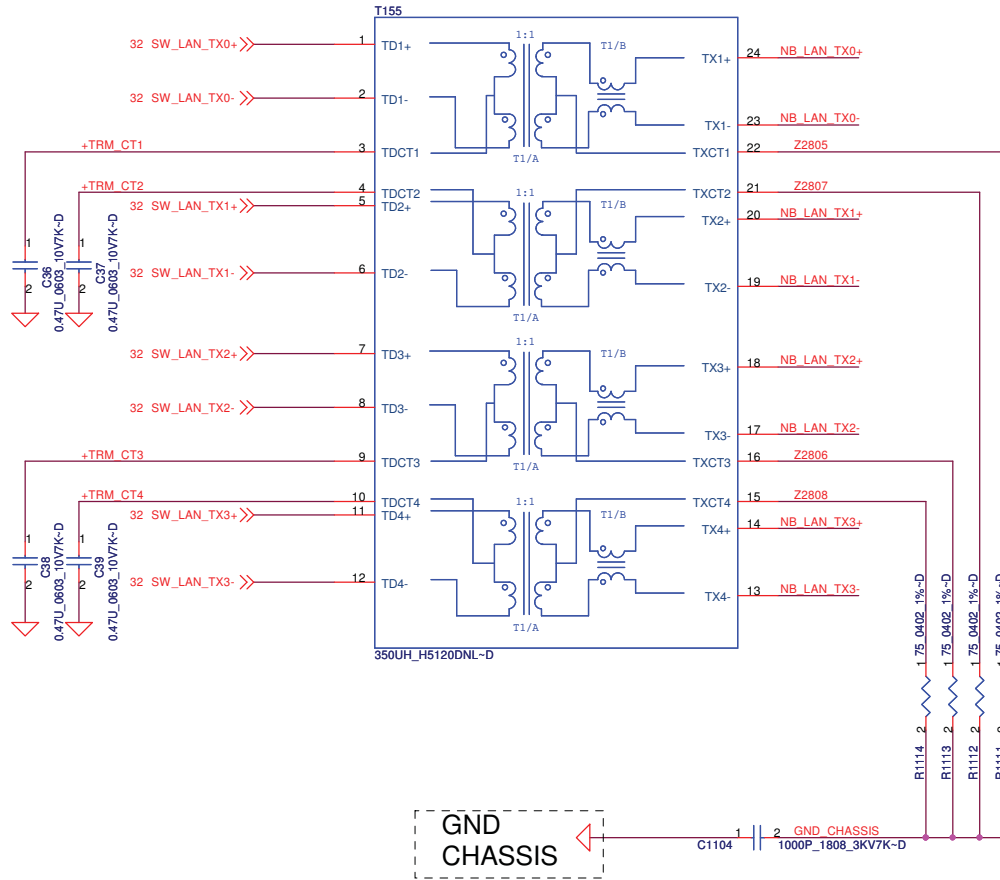


+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548

[illegible]

DOCKED 1: TO DOCK
0: TO RJ45

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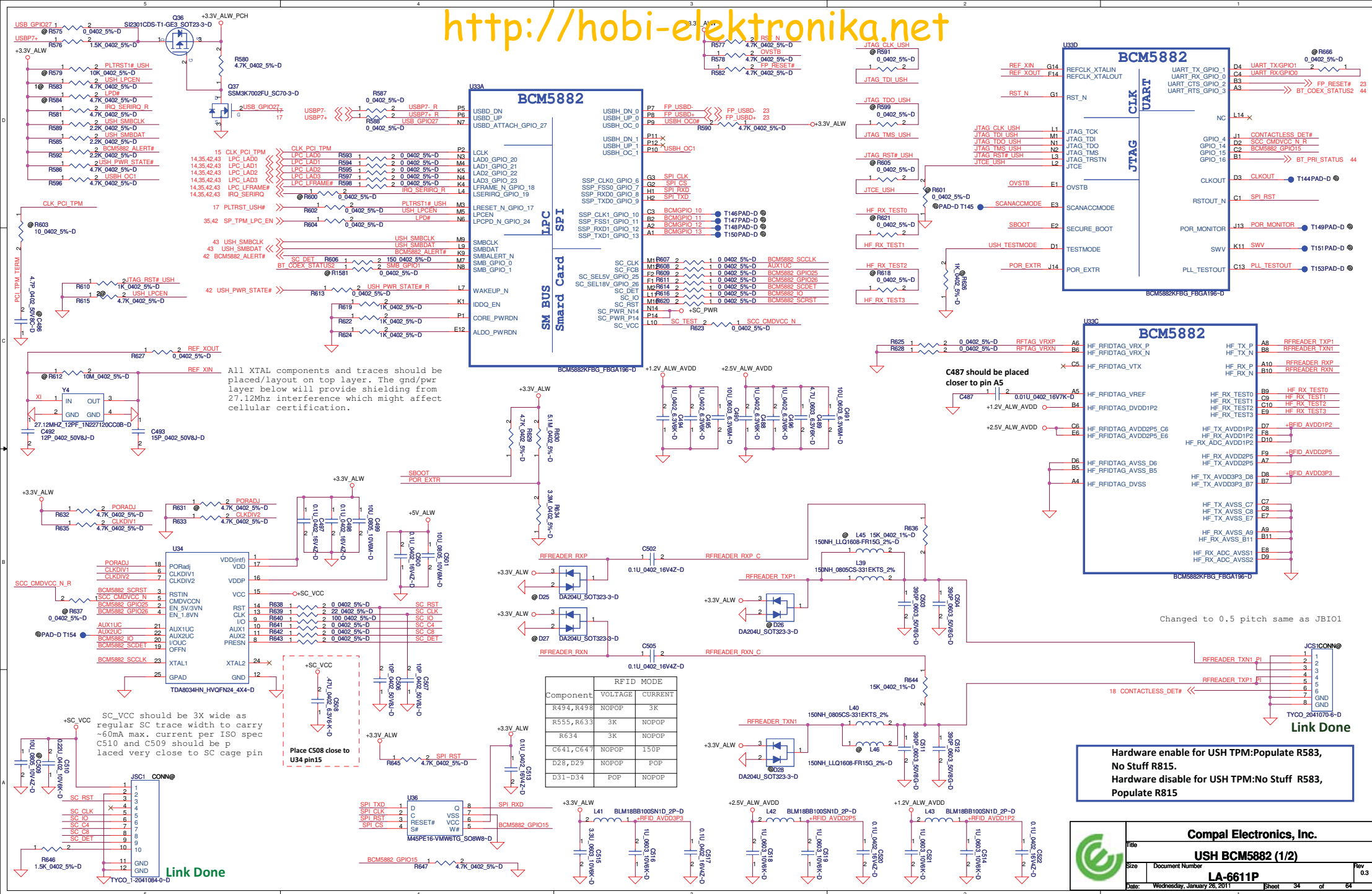
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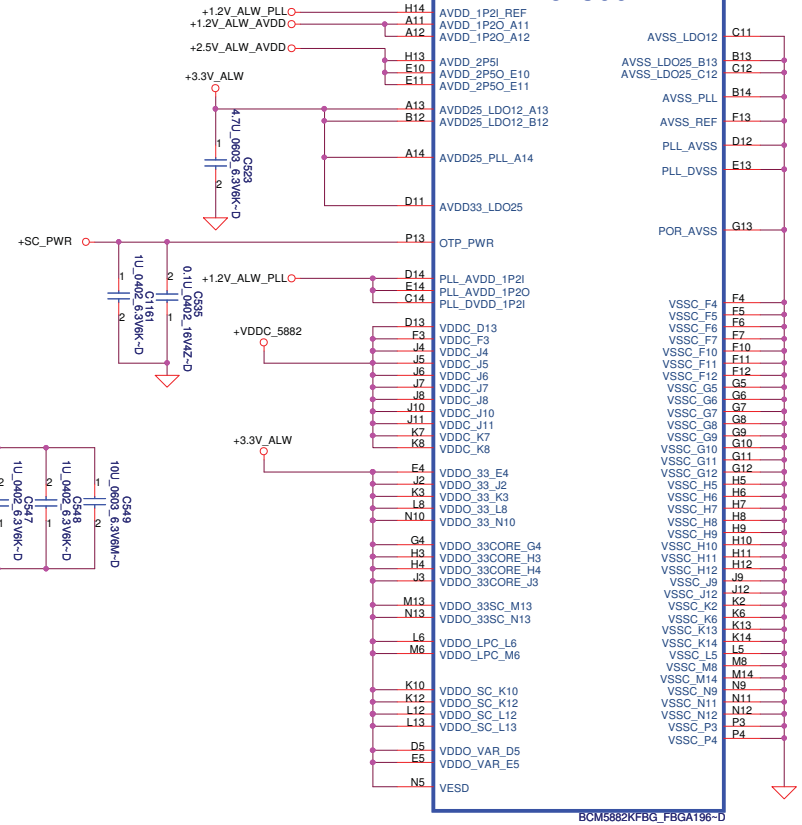
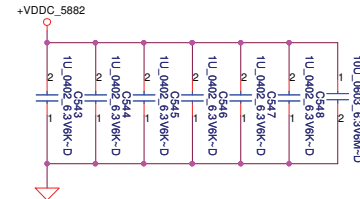
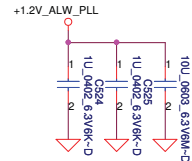
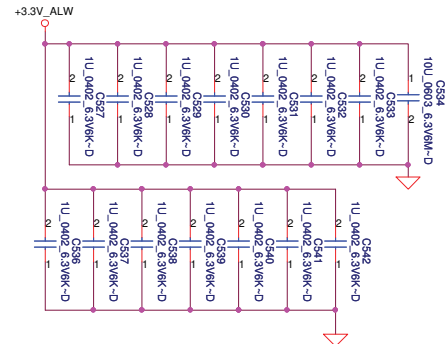
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Size	Document Number	LA-6611P	
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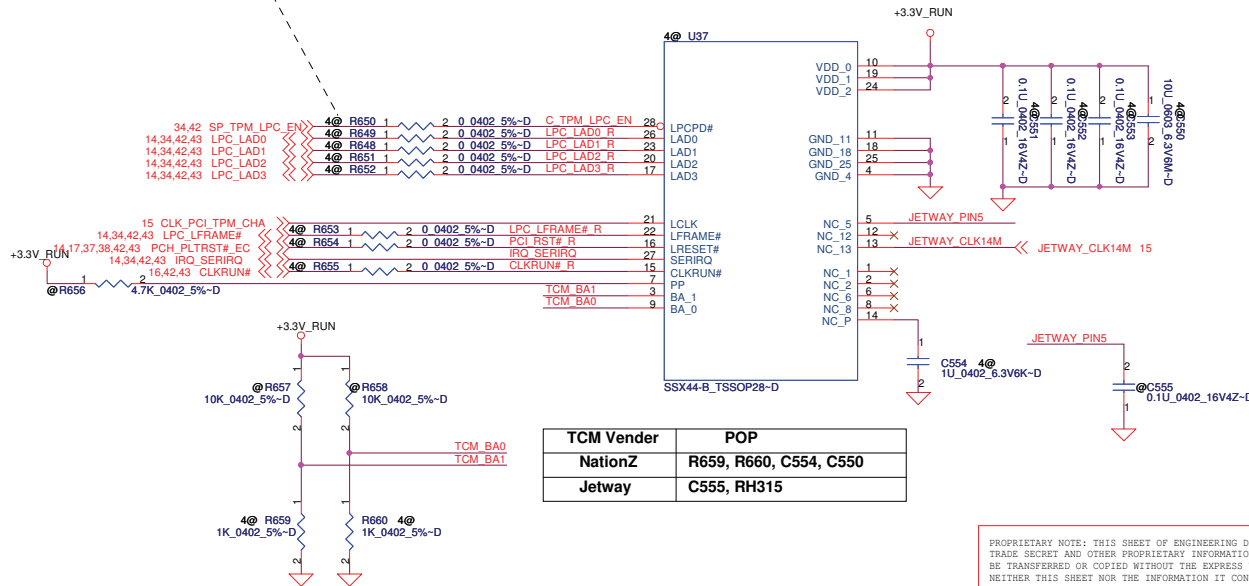
Rev 0.3





LOW:Power Down Mode
High:Working Mode

China TCM: NationZ & Jetway co-lay



USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
USH_LPCEN	PU R583	@	POP	@
	PD R615	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R772	@	@	@
PCH GPIO39 ->TPM_ID1	PU RH268	@	@	POP
	PD RH271	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU RH267	POP	POP	@
	PD RH270	@	@	POP

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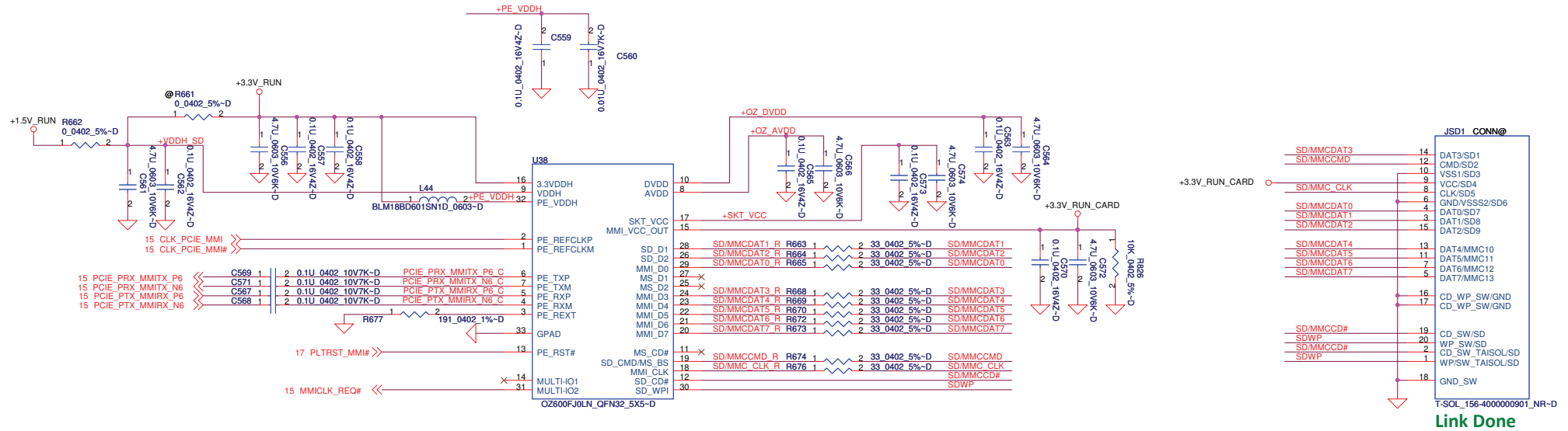
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USH BCM5882 (2/2)

LA-6611P

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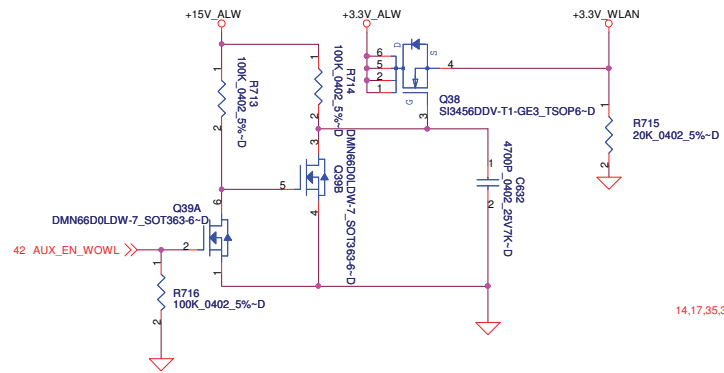
LA-6591P

Rev 0.3

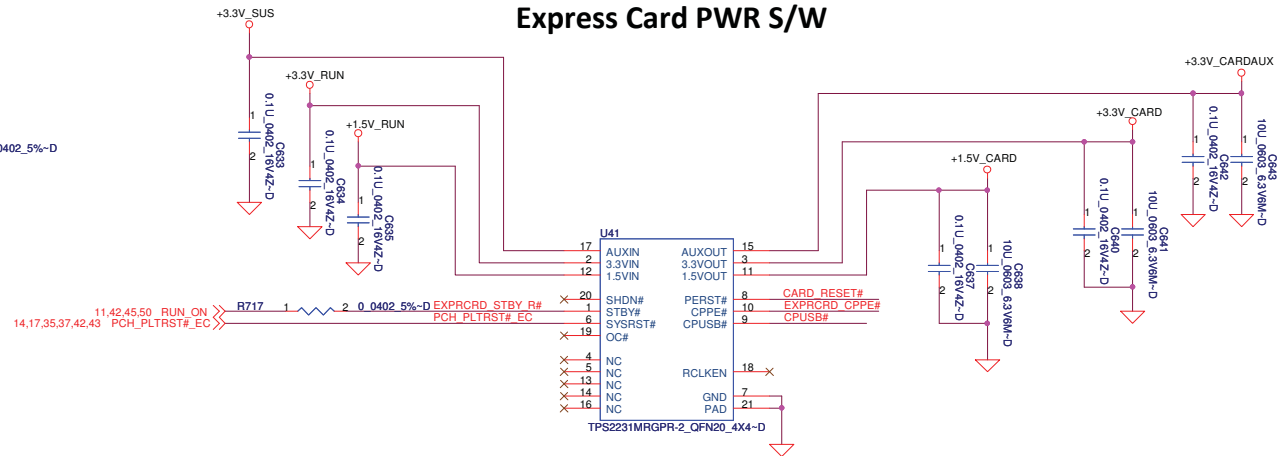
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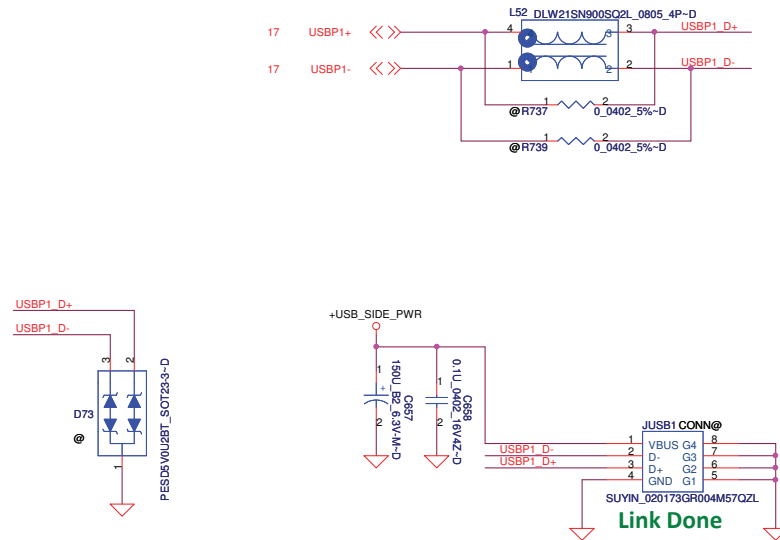
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Power Control for Mini card2



Express Card PWR S/W





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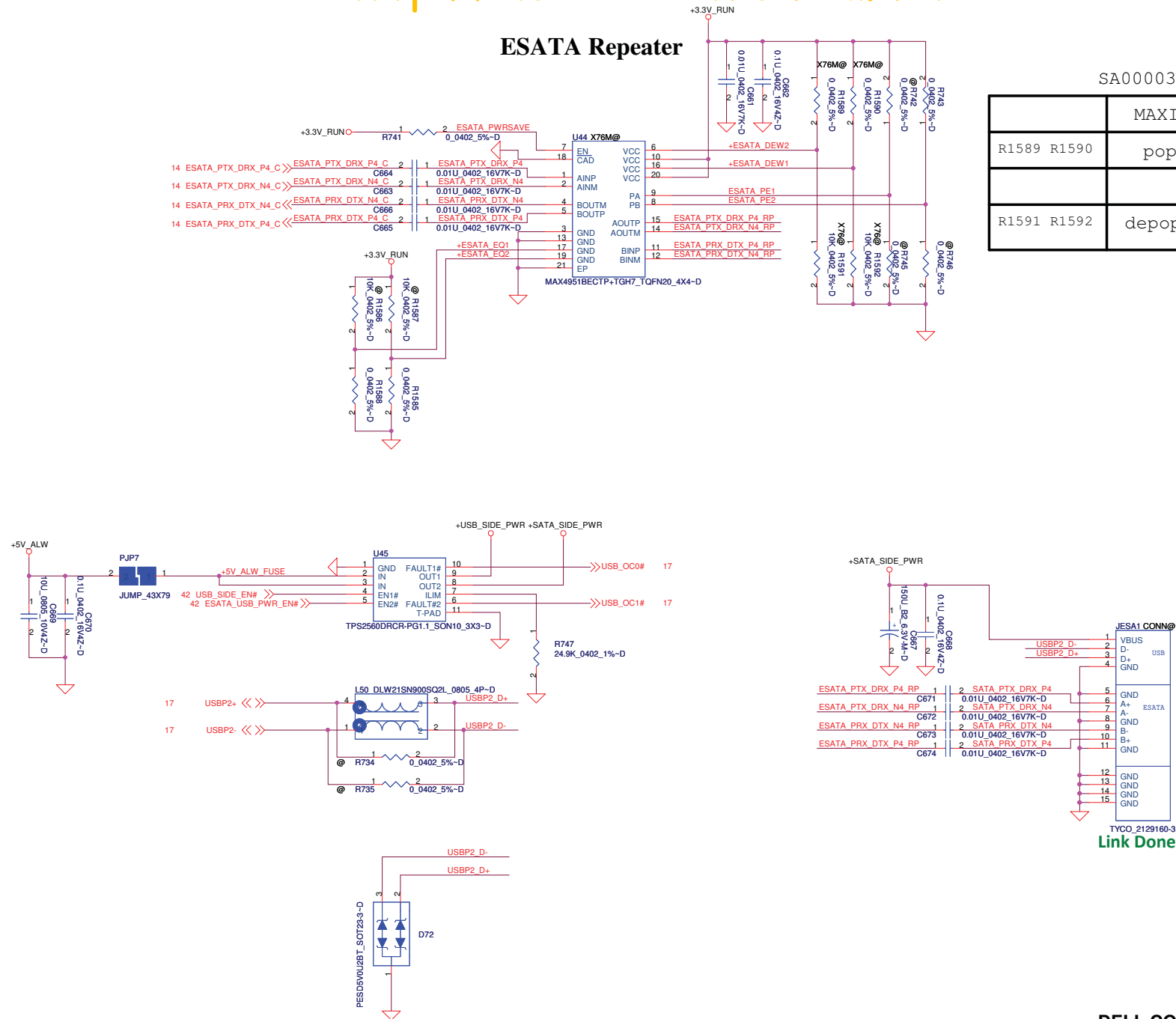


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ESATA Repeater



SA00003LH1L SA00003ZX0L

	MAXIM	TI
R1589 R1590	pop	depop
R1591 R1592	depop	pop

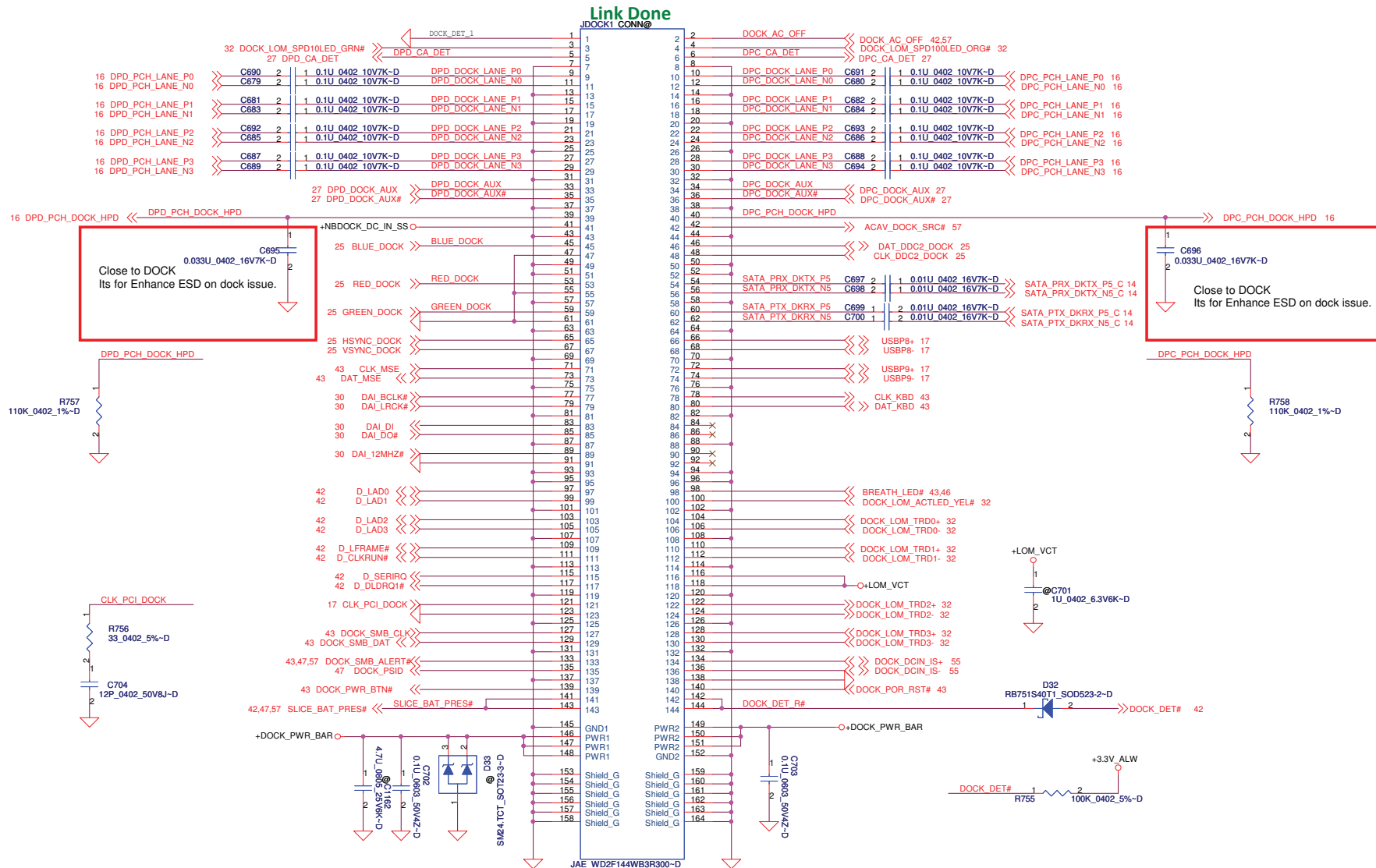
TYCQ_2129160-3
Link Done

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Title	USB/ESATA/IO		
Size	Document Number	Rev	0.3
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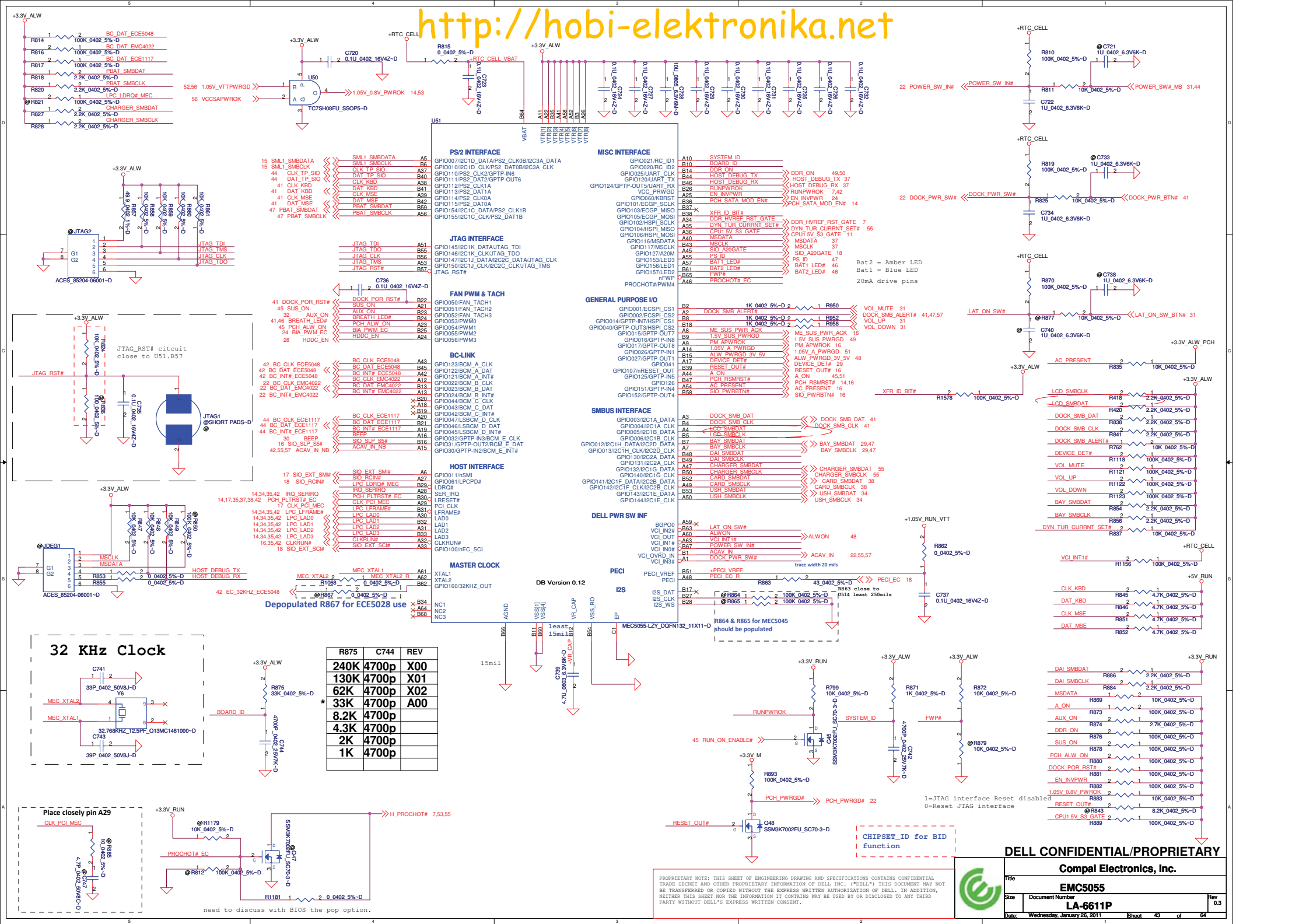
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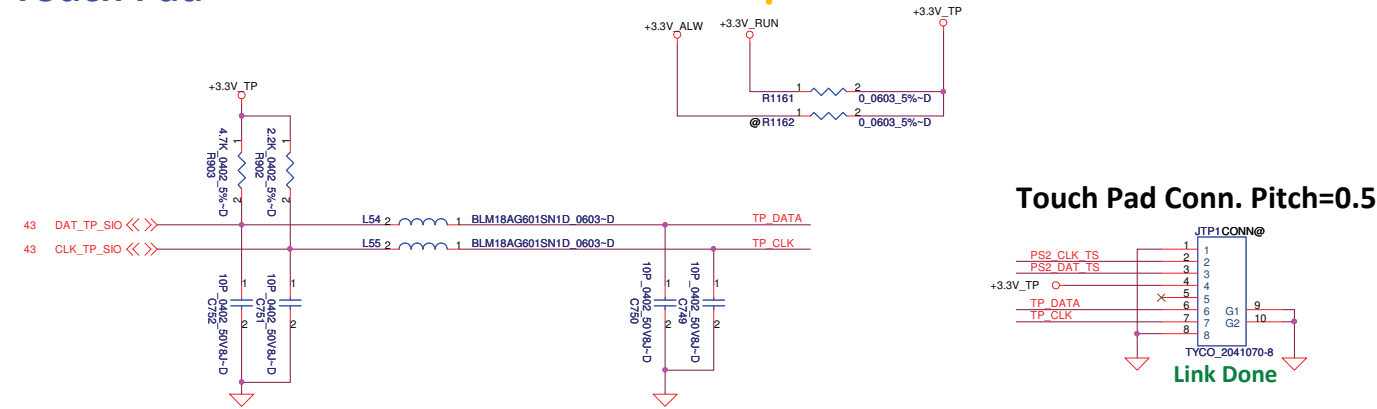
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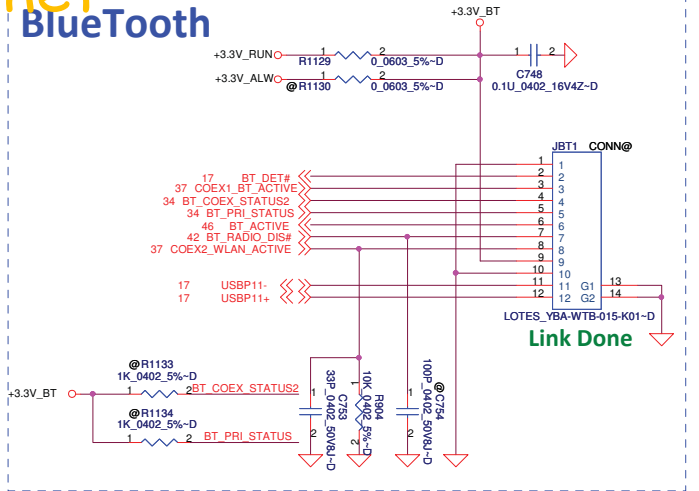
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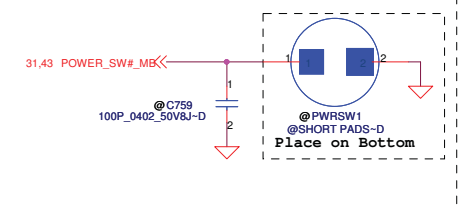
Touch Pad



BlueTooth

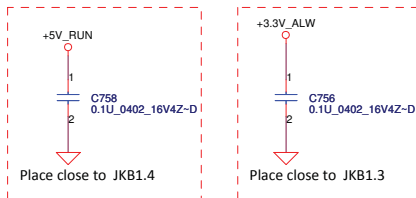
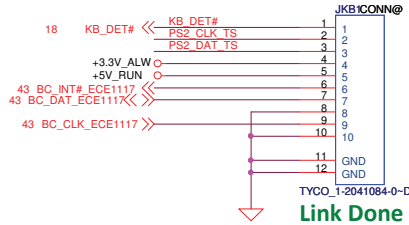


Power Switch for debug



Keyboard

KB Conn. Pitch=1.0mm



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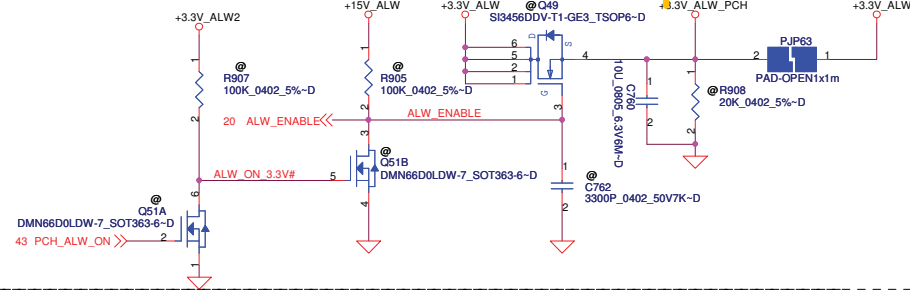


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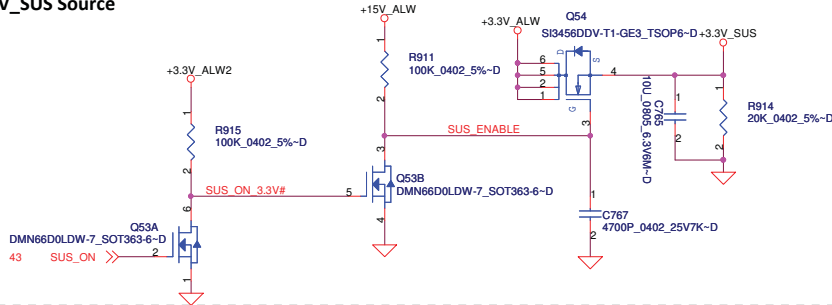
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Title			
Int KB/Touch PAD/BT			
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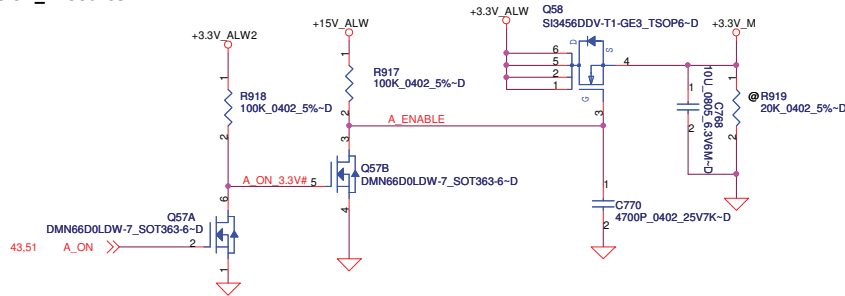
+3.3V_ALW_PCH Source



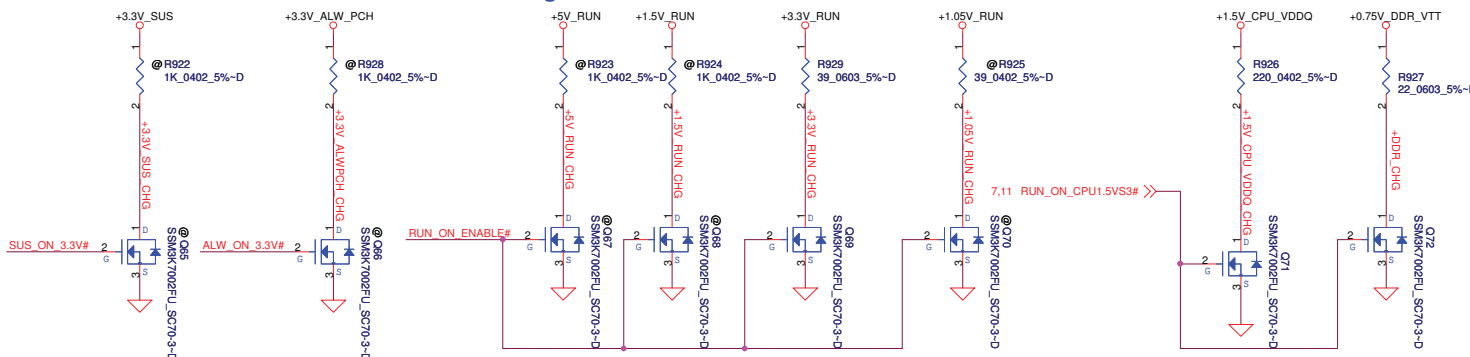
+3.3V_SUS Source



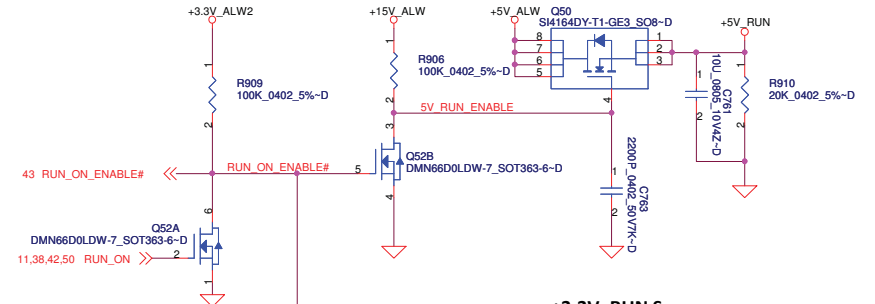
+3.3V_M Source



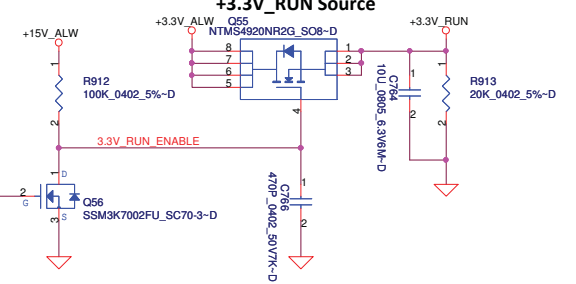
Discharge Circuit



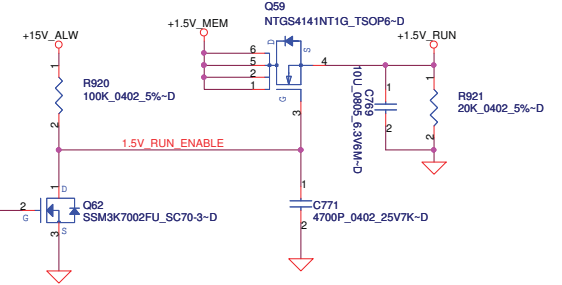
DC/DC Interface



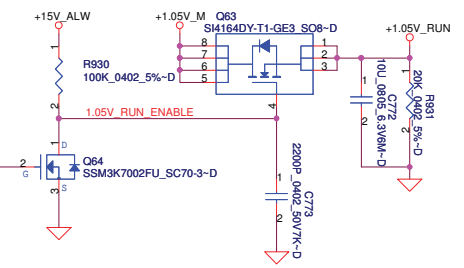
+3.3V_RUN Source



+1.5V_RUN Source



+1.05V_RUN Source



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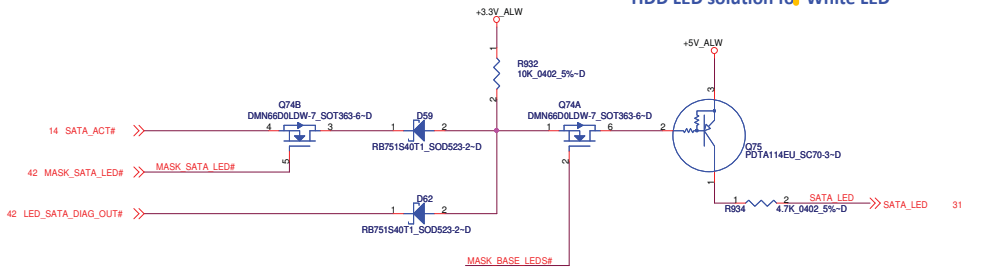
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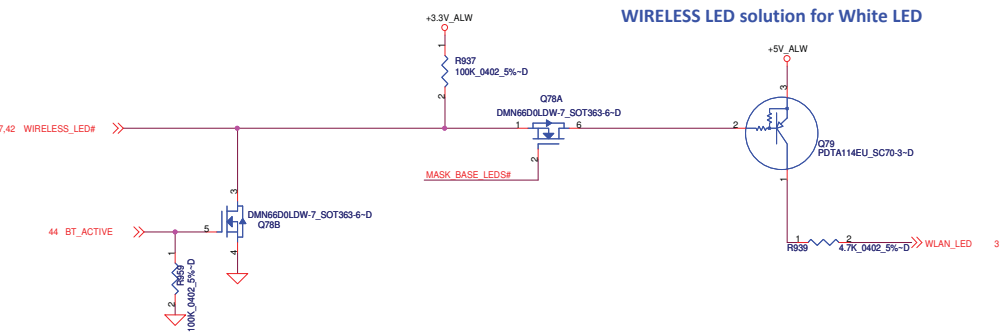
POWER CONTROL			
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HDD LED solution for White LED

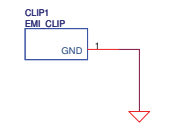


WIRELESS LED solution for White LED

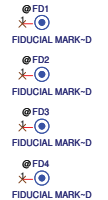


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

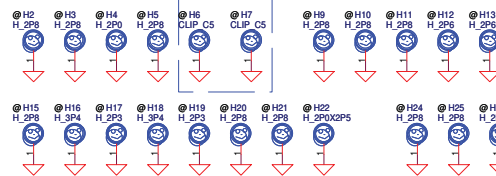
EMI CLIP



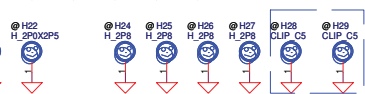
Fiducial Mark



LVDS standoff



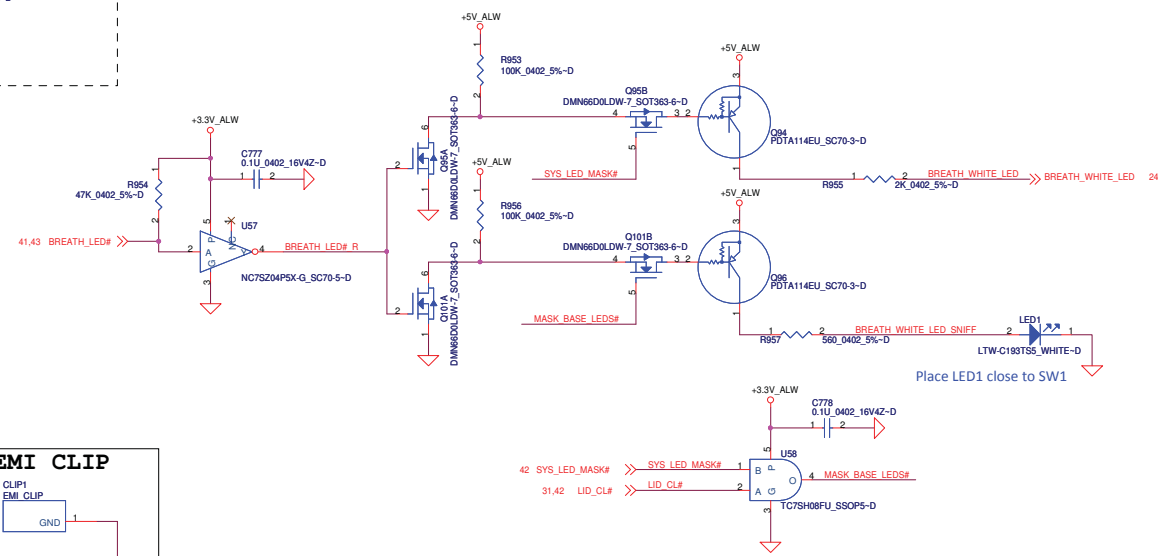
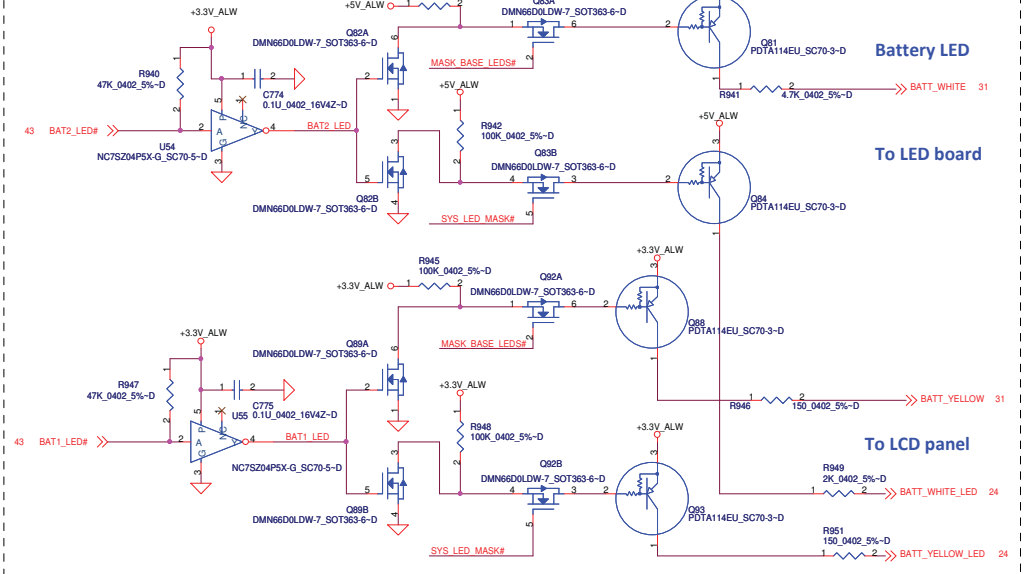
PCH standoff



Battery LED

To LED board

To LCD panel



Place LED1 close to SW1

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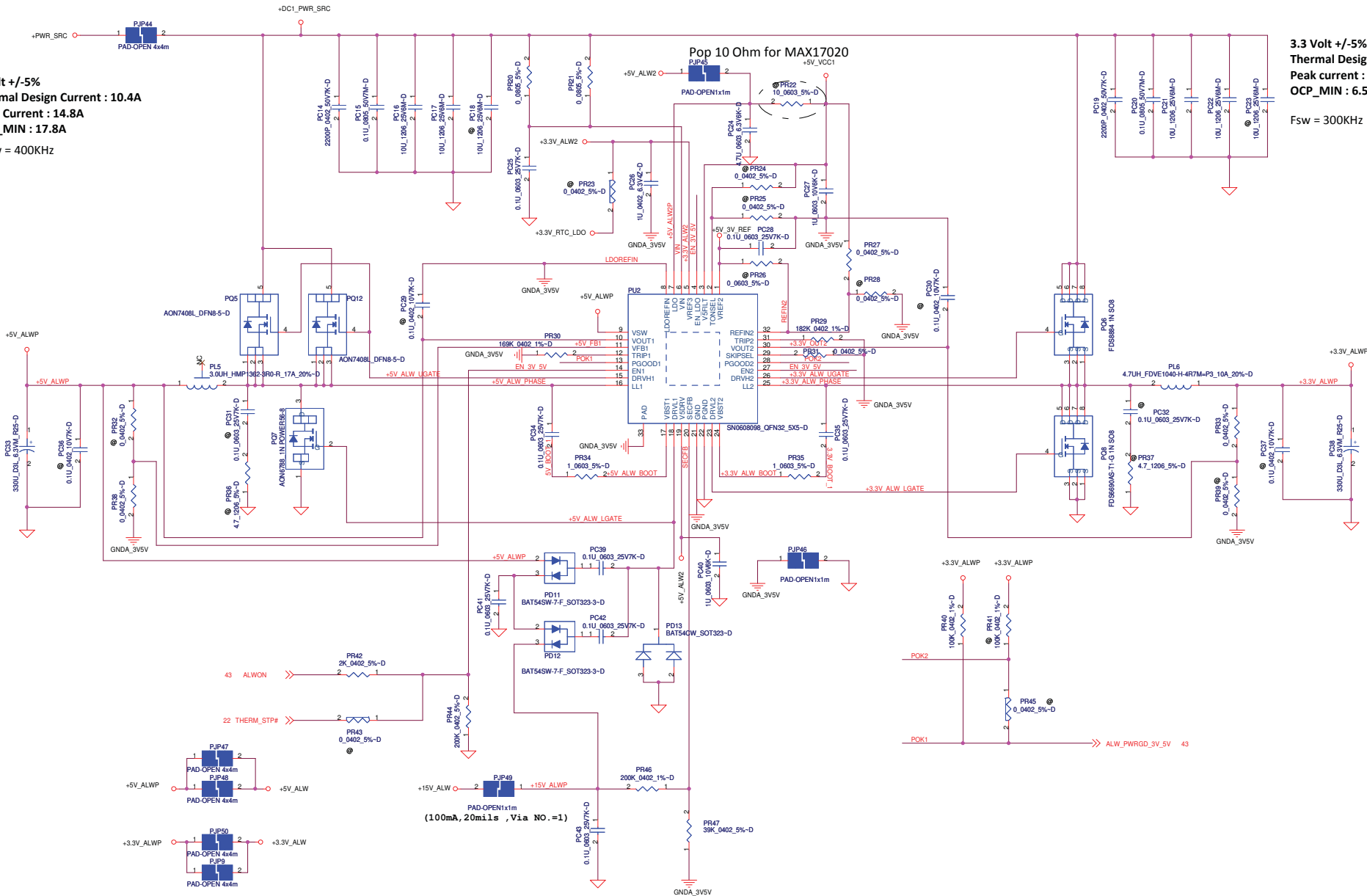
PAD & ME & LED

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5 Volt +/-5%
Thermal Design Current : 10.4A
Peak Current : 14.8A
OCP_MIN : 17.8A
Fsw = 400KHz

3.3 Volt +/-5%
Thermal Design Current : 3.8A
Peak current : 5.4A
OCP_MIN : 6.5A
Fsw = 300KHz



		PU2	PR22
Main	X7629631L90	SN0608098	un-pop
2nd	X7629631L91	MAX8878	10_ohm

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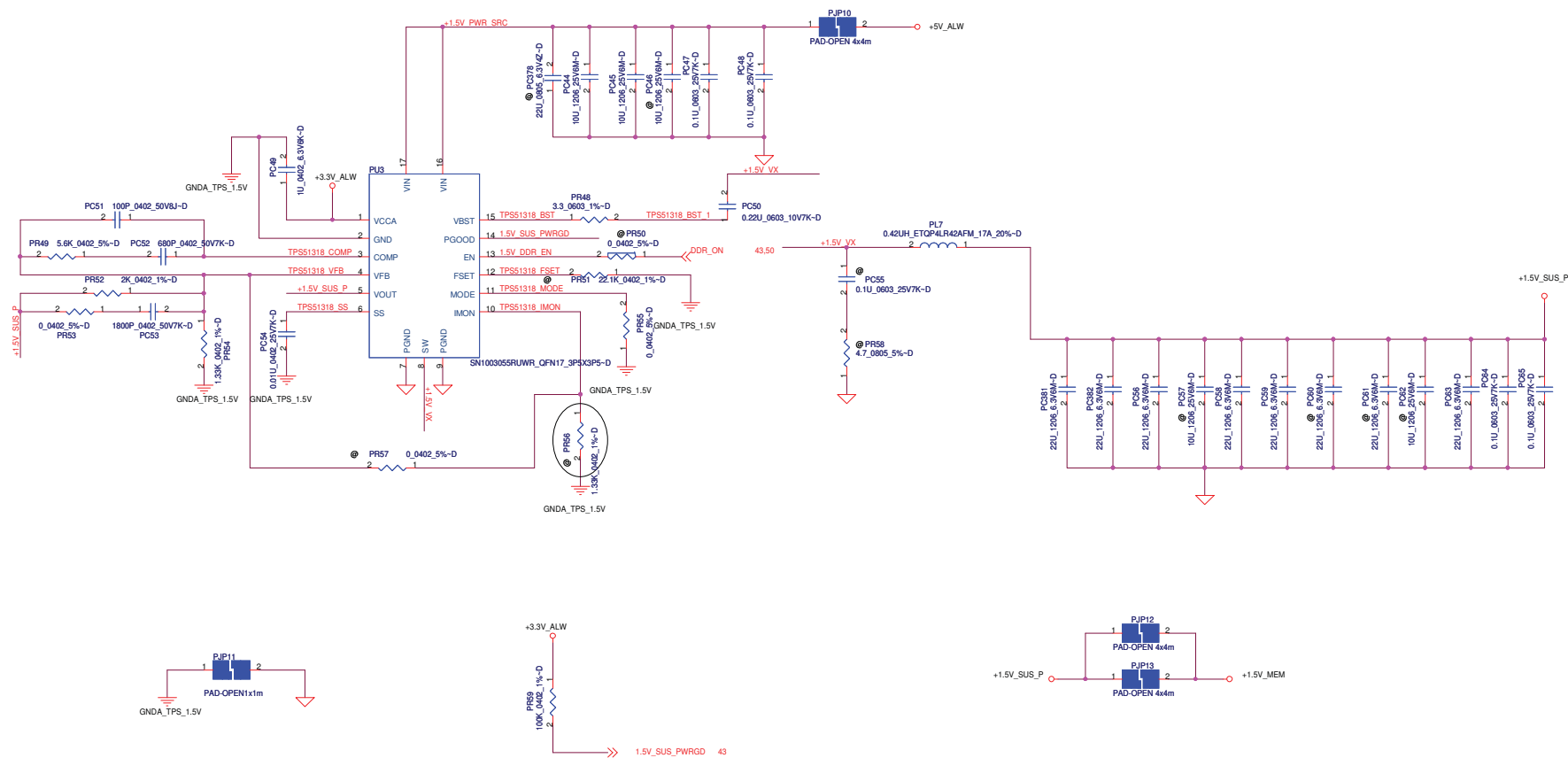
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DC/DC +3V/ +5V

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1.5 Volt $\pm 5\%$
Thermal Design Current: 9.8A
Peak current: 13.9
OCP_MIN:16.7A



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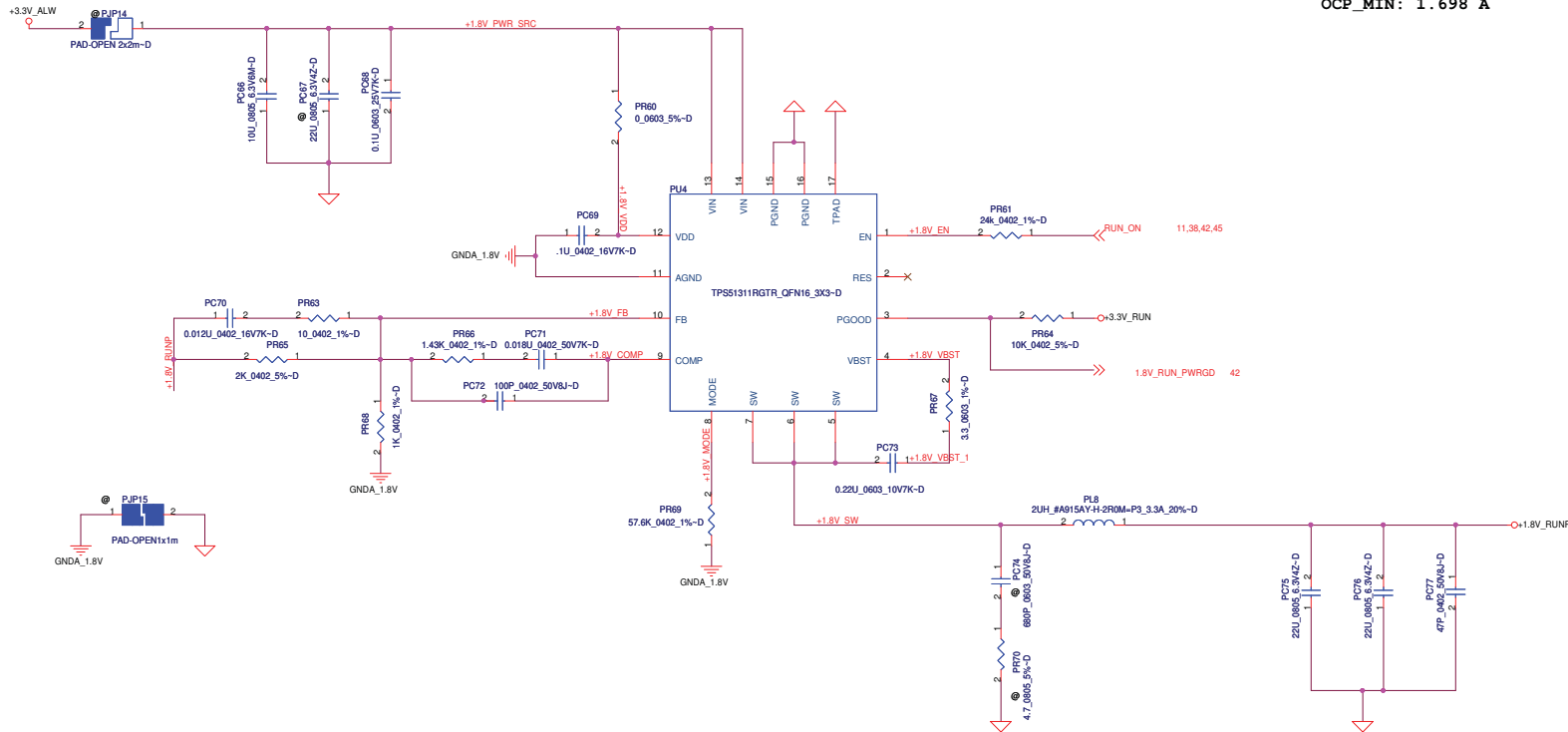
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+1.5V MEM

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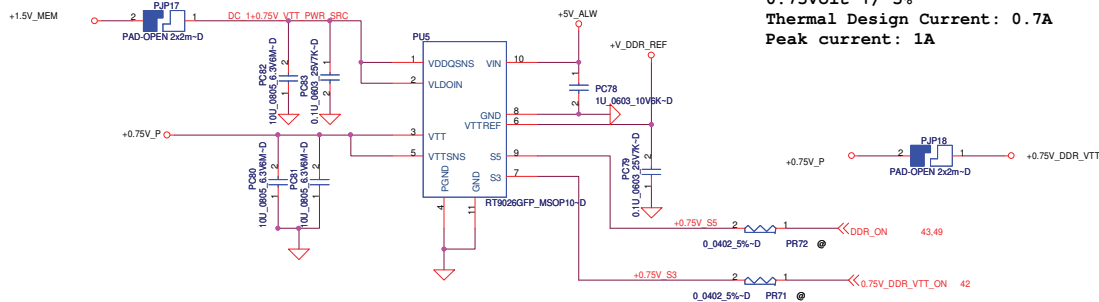
1.8 Volt +/-5%
Thermal Design Current: 0.99 A
Peak current: 1.415 A
OCP_MIN: 1.698 A



+0.75V_DDR_VTT

DDR3 Termination

0.75Volt +/-5%
Thermal Design Current: 0.7A
Peak current: 1A



VOUT=1.8V
L=3.3uF
Fsw=290KHz
D=0.092
Input Ripple Current=TDC*(D*(1-D))^0.5=0.884A
Output Ripple Current=1.707A
Output Ripple Voltage=1.707*15m=20.5mV

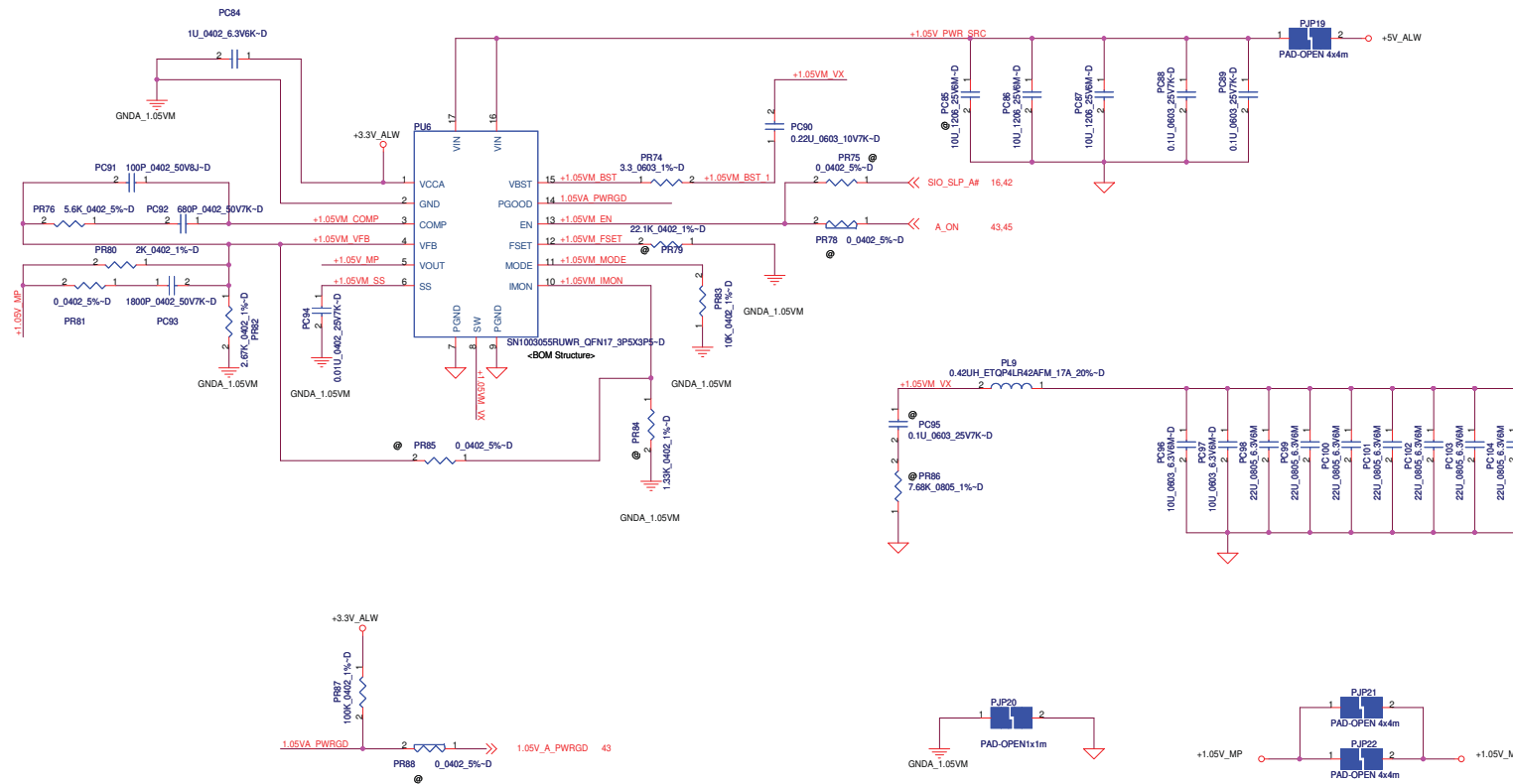
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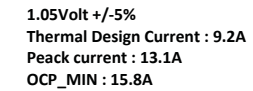
+0.75V_DDR VT/+1.8V_RUN

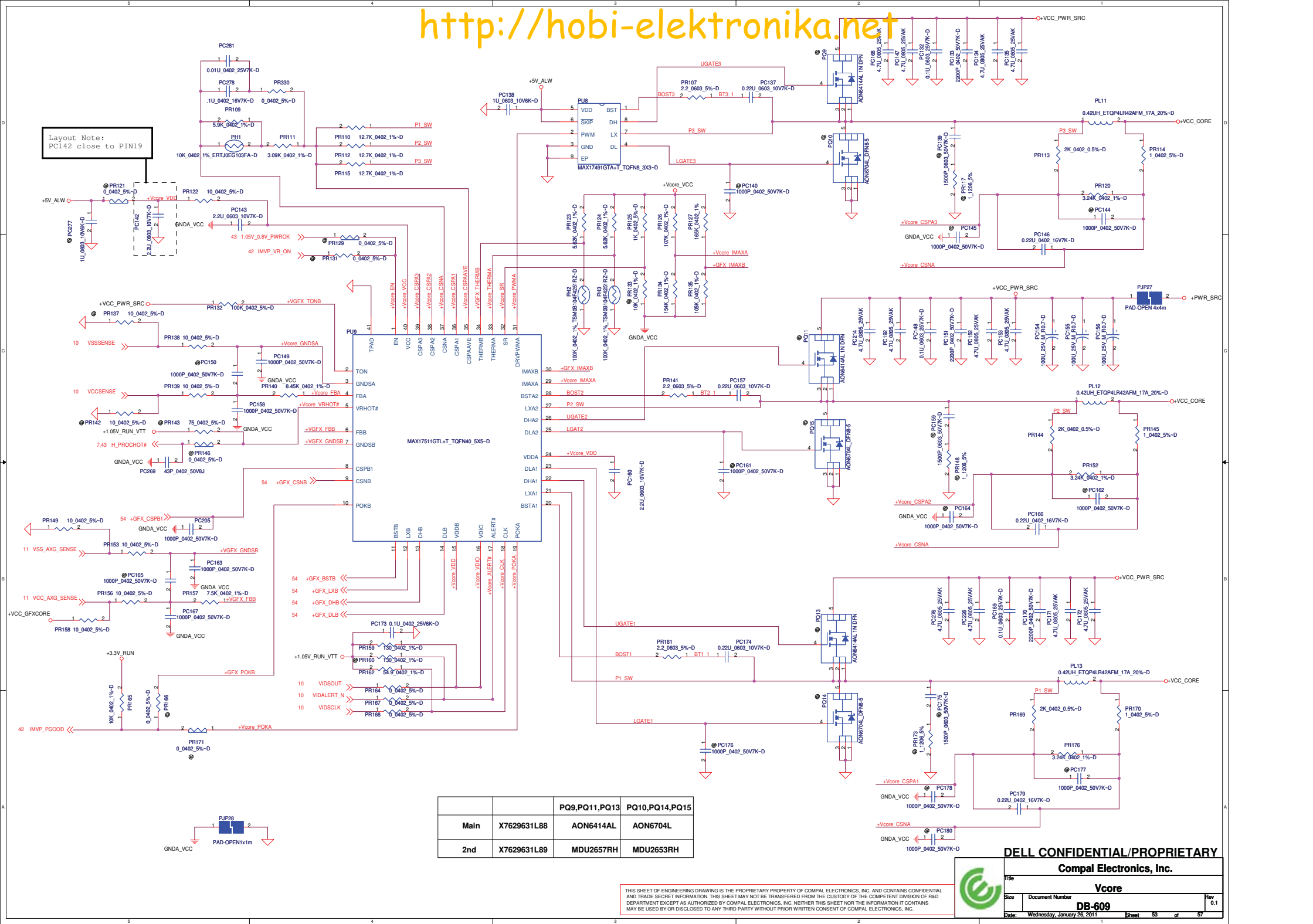
Size Document Number LA-6611P Rev 0.1
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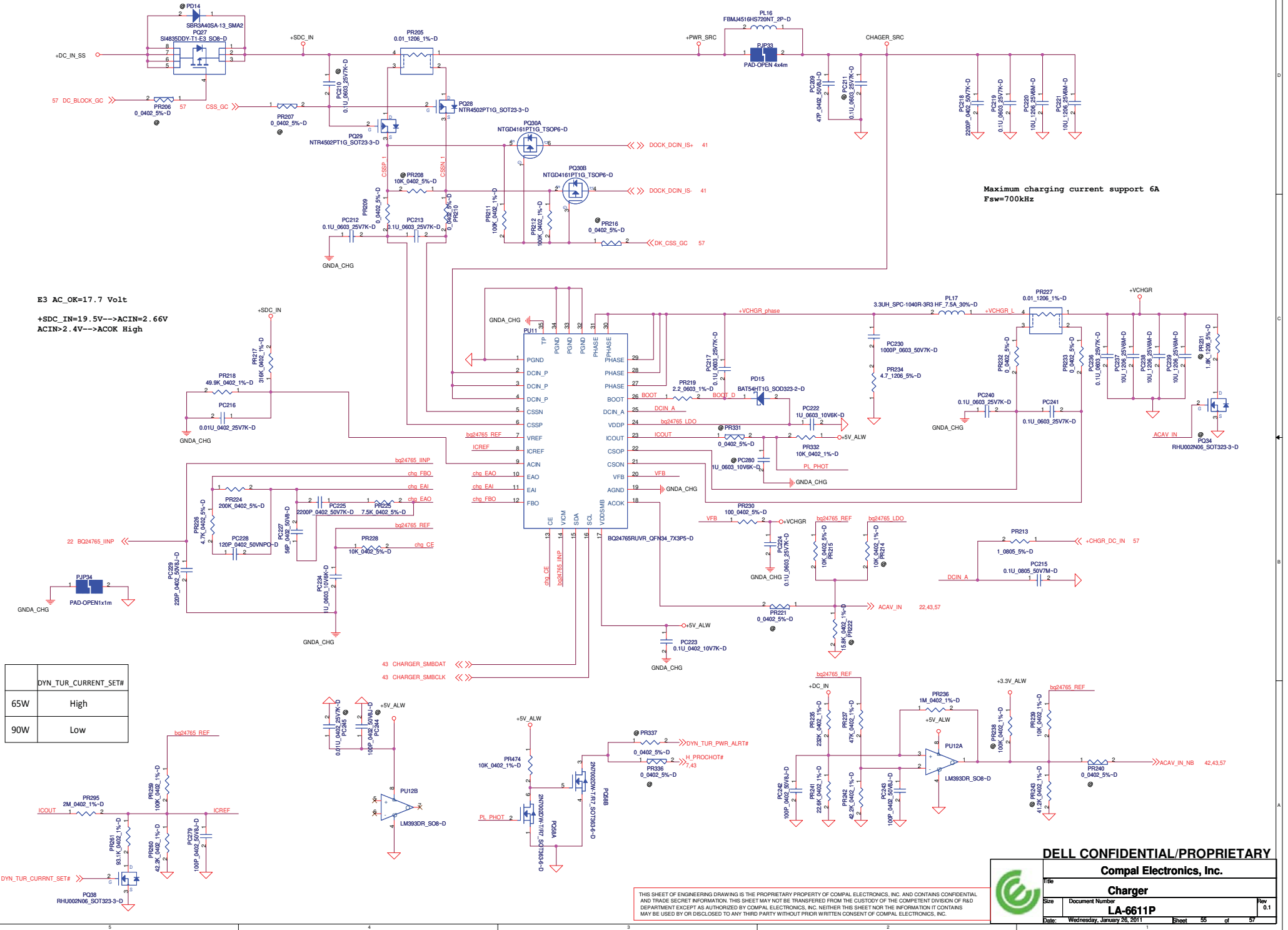
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1.05 Volt +/-5%
Thermal Design Current : 2.7A
Peak current : 3.9A
OCP_MIN :4.7A



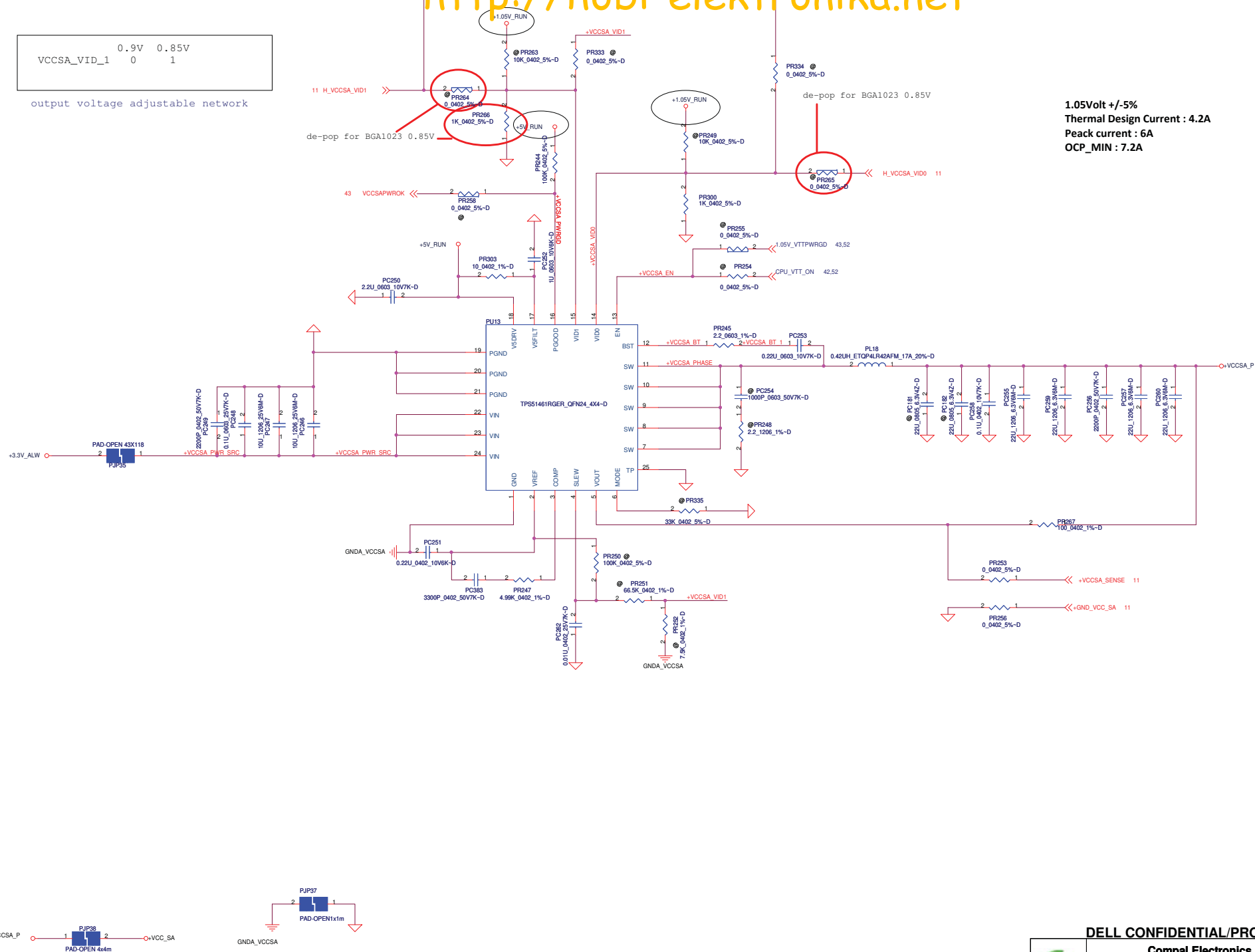




	0.9V	0.85V
VCCSA_VID_1	0	1

output voltage adjustable network

1.05Volt +/-5%
Thermal Design Current : 4.2A
Peak current : 6A
OCP_MIN : 7.2A





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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	14	HW	7/13/2010	COMPAL	Modify TAA SPI ROM topology	Add R933 0-ohm & Remove SPI_HOLD#0 and SPI_WP#0 connect to JP1	X01
2	11, 56	HW	7/22/2010	COMPAL	Modify net name	Change +0.8V_VCC_SA to +VCC_SA	X01
3	22, 25, 28 32, 42, 43 45, 11, 20 37, 11,	HW	7/22/2010	COMPAL	Follow PPM recommendation to change material	Change capacitors from 10uF_0805_10V_Y5V to 10uF_0805_6.3V_X5R: C305, C316, C387, C1181, C705, C728, C760, C764, C765, C768, C769, C772, CC135, CH58, CH73, CH80 Change capacitors from 10uF_0805_6.3V to 10uF_0603_6.3V: C475, C638, C641, C643 Change resistors to 0402 size: RC134, RH201, RH253, RH208, RH213 Delete RH192 and add PJP52	X01
4	14	HW	7/22/2010	COMPAL	De-pop PCH XDP	De-pop RH36, RH283, RH21, RH24, CH1, CH6	X01
5	14, 29, 43	HW	7/22/2010	COMPAL	Modify Module Bay circuit	Change net name ODD_DET# to PCH_SATA_MOD_EN#, r and USB_MCARD3_DET# to remove R1069, R1182, R1188, R425, Add R513, Q76, Q123B, change BAY SM bus PU rail to +3.3V_ALW	X01
6	18	HW	7/22/2010	COMPAL	Follow Intel Design Guide Rev1.0	Change RH149 to 1k and RH150 to 4.7k	X01
7	22	HW	7/22/2010	COMPAL	Change MAX8731_IINP connection	Change to VCP	X01
8	22	HW	7/22/2010	SMSC	Per SMSC request	Add R404 10K pull down of TEST1 pin	X01
9	26	HW	7/22/2010	COMPAL	For Safety request	Add D4 and R5 co-lay with F2,	X01
10	40	HW	7/22/2010	COMPAL	Change ESATA repeater	Add R1585~R1588, and change U44 to MAX4951BECTP	X01
11	30	HW	7/22/2010	COMPAL	Change codec to ZB version	Change Codec part number to SA00003ZZ1L and stuff C962	X01
12	34	HW	7/22/2010	COMPAL	Change RFID capacitors for more popular	Change C502, C505 from 1uF to 0.1uF	X01
13	24, 46	HW	7/22/2010	COMPAL	Correct net name for LED signal	Modify signal name BREATH_BLUE_LED to BREATH_WHITE_LED and BREATH_BLUE_LED_SNIFF to BREATH_WHITE_LED_SNIFF	X01
14	42	HW	7/22/2010	COMPAL	Add 0 ohm resistor for SUSACK#	Add R1132 and add net name SUSACK#_EC	X01
15	32	HW	7/22/2010	INTEL	Remove useless resistors	Remove R556, R558, R559, R560 and short it.	X01
16	32, 28, 29 38, 45	HW	7/22/2010	COMPAL	Change part for Halogen free	Change Q18, Q27, Q30, Q34, Q38, Q40, Q42, Q49, Q54, Q58 to HF part	X01
17	10	HW	7/22/2010	COMPAL	CC129~CC134 D2T LESR5M EOL	Change CC129~CC134 to SGA00004X0L	X01
18	37	HW	7/22/2010	COMPAL	Modify Module Bay circuit	De-pop C627, R712	X01
19	7	HW	7/22/2010	COMPAL	For support XDP device	De-pop RC9	X01
20	42	HW	7/22/2010	COMPAL	Base on GPIO map to modify	Change SLICE_BAT_PRES# pull up power rail from +3.3V_ALW2 to +3.3V_ALW	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	43	HW	7/22/2010	COMPAL	Base on GPIO map to modify	Add R889 for CPU1.5V_S3_GATE pull down	X01
22	15,18	HW	7/22/2010	COMPAL	Base on GPIO map to modify	Remove RH238,RH172 and change connection form SLP_ME_CSW_DEV# from GPIO45 to GPIO28	X01
23	24	HW	7/22/2010	COMPAL	PWM function	Remove R1139,R1140 and add D68,D69, pop R1137	X01
24	37,46	HW	7/22/2010	COMPAL	Modify LED circuit	Remove R1578,R1579,R1580,D42,D60,D61, add Q77,Q124,R705,R718,R719	X01
25	15,32	HW	7/22/2010	COMPAL	EOL concern	Change Y3 and YH2 from 1Y725000CE1A to 7A25000110	X01
26	24,27,46	HW	7/22/2010	COMPAL	Change part for Halogen free part	Change QC5 to NTR4501NT1G, U21,U24,U54,U55,U57 change to NC7SZ04P5X-G, Q21 change to FDC654P-G	X01
27	36	HW	7/22/2010	O2-Mirco	Add discharge circuit for +3.3V_RUN_CARD	Add R826 on +3.3V_RUN_CARD	X01
28	31,42,46	HW	7/22/2010	COMPAL	Remove mute function and LED	Remove R1109,Q119,Q105,Q102,R1059,R1061	X01
29	17,18,43	HW	7/22/2010	COMPAL	To solve back drive issue	Remove USB_OC7# signal and RH254, change connection from PCH GPIO1 to GPIO14,and change RH164 pull up power rail from +3.3V_RUN to +3.3V_ALW_PCH	X01
		HW	7/22/2010	COMPAL			
30	18	HW	7/22/2010	COMPAL	Add pull up for PCH GPIO1	Change RH254 to 10K and pull high to +3.3V_RUN	X01
31	29,45	HW	7/22/2010	COMPAL	For cost saving	Add PJP63,RH202, no stuff QH4,Q49,RH278,R908	X01
32	42	HW	7/22/2010	COMPAL	Follow GPIO 0720	Add DYN_TUR_PWR_ALRT# up power rail and change R796 pull from +3.3V_RUN to +3.3V_ALW	X01
33	43	HW	7/22/2010	COMPAL	Follow GPIO 0720	Add DYN_TUR_CURRNT_SET# up power rail and change R837 pull from +3.3V_RUN to +3.3V_ALW	X01
34	28,46	HW	7/22/2010	COMPAL	Part leverage select	Change D16,D59,D62 to SC100000S0L	X01
35	14	HW	7/22/2010	COMPAL	Follow Intel XDP design guide	Change RH43,RH44,RH45 to 200 ohm	X01
36	24,40	HW	7/22/2010	INTEL	Change material for small size	Change C300,C669 from 1206 16V to 0805 10V	X01
37	39,40	HW	7/22/2010	COMPAL	Remove useless capacitors	Remove C1151~C1154	X01
38	37	HW	7/22/2010	COMPAL	Add 0 ohm R on PCIE_MCARD2_DET#	Add R725	X01
39	43	HW	7/22/2010	COMPAL	Follow GPIO MAP 0720	Add R1578 for XFR.	X01
40	42	HW	7/22/2010	COMPAL	Add 0 ohm for TEMP_ALERT#	Add R773	X01
41	44	HW	7/22/2010	COMPAL	Solution +1.5V_RUN voltage drop issue	Change Q59 from SI3456BDV to NTGS4141NT1G	X01
42	46	HW	7/27/2010	COMPAL	Add pull down 100k on BT_ACTIVE	Add R959	

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44	40	HW	7/27/2010	COMPAL	Follow Vender request.	R1589~R1592	X01
45	43	HW	7/27/2010	COMPAL	BID change	Change R875 to 130K	X01
45	22	HW	7/27/2010	COMPAL	Chnage thermal diode connection	Remove C268	X01
46	18, 30	HW	7/28/2010	COMPAL	Remove SPEAKER_DET# PAID.	Chnage SPEAKER_DET# to GPIO17, and change speaker connector to SP02000H900	X01
47	14, 47	HW	7/28/2010	COMPAL	Remove RTC_DET# PAID.	Remove RH31, add T132	X01
48	22	HW	7/28/2010	COMPAL	Follow connector list	change FAN connector to SP02000TI00	X01
49	33	HW	7/28/2010	COMPAL	Follow connector list	Re-link RJ45 symbol	X01
50	44	HW	7/28/2010	COMPAL	Follow connector list	Chnage keyboard connector to pitch 1	X01
51	34	HW	7/28/2010	COMPAL	Remove Broadcom debug connector	Remove JBRCM1 and add R666 no stuff	X01
52	47	HW	7/28/2010	COMPAL	Change RTC connector	Change to TYCO_2-1775293-2	X01
53	43	HW	08/05/2010	COMPAL	Change signal net name	Change 0.8V_VCCPWROK net name to VCCSAPWROK	X01
54	30	HW	08/13/2010	COMPAL	Fix Speaker EMI issue	Change R1183~R1186 to L78~L81 pop C973~C976, C267, C283 and C284	X01
55	39, 40	HW	08/13/2010	COMPAL	Fix USB EMI issue	pop L50, L52, depop R737, R739, R734, R735	X01
56	29	HW	08/13/2010	COMPAL	Change ODD repeater	Chnage ODD repesater to MAX4951B and R1174, R1176, R1169, R1171 to 0 ohm	X01
57	43	HW	08/13/2010	COMPAL	EOL concern	Change Y6 to SJ132P7KW1L same as YH1	X01
58	22	HW	08/13/2010	COMPAL	Change FAN conn type for ME request	change FAN connector to SP02000CB0L	X01
59	14	HW	08/13/2010	COMPAL	Change TAA topology	redefine JP1 TAA pin define	X01
60	10	HW	08/16/2010	COMPAL	Follow PPDG1.2 Vcore 2.2uf 0402 QTY from 55 to 35 pcs	remove CC199, CC103, CC120, CC142, CC141, CC171, CC139, CC134, CC133, CC200 CC101, CC128, CC153, CC102, CC126, CC105 16pcs depop 4 pcs CC152, CC121, CC127 and CC160	X01
61	18	HW	08/16/2010	COMPAL	Follow INTEL DG DF_TV5 pull high value	Change RH150 to 0 ohm RH149 to 2.2K ohm	X01
62	14 15 43	HW	08/16/2010	COMPAL	Crystal EA	Change C743=39pF CH2, CH3=15pF CH18, CH19=10pF and YH2 to SJ100008E0L	X01
63	22	HW	08/17/2010	COMPAL	reserve cap for CPU remote diode	Add C286	X01
64	14	HW	08/17/2010	COMPAL	reserve Resistance and Cap for SPI EA	Add CH107, CH108, R935	X01

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65	34	HW	8/20/2010	COMPAL	BRCM request RFID filter need have 400mA max	Change L39 and L40 to SHI0000CH0L.Reserve L45,L46 colay	X01
66	14	HW	8/23/2010	COMPAL	Improve SPI EA for SPI_CLK	Change R899 and R897 to 56 ohm	X01
67	30	HW	8/23/2010	COMPAL	Follow connector list	Change Speaker CONN to SP021007221	X01
68	42	HW	8/24/2010	COMPAL	RF noise	pop R794 R795 to 10 ohm,C712 C713 to 10p	X01
69	14	HW	8/25/2010	COMPAL	Improve SPI power path	Always pop C745	X01
70	36	HW	8/25/2010	COMPAL	O2 recommend add cap for +PE_VDDH	add C559 0.1uF C560 0.01uF	X01
71	14 18	HW	8/26/2010	COMPAL	Follow INTEL DPDG	reserve RH31,RH355 for GPIO19/GPIO28	X01
72	14	HW	8/27/2010	COMPAL	remove double reserve cap for BIT_CLK	remove CH100	X01
73	16	HW	8/27/2010	COMPAL	reserve ME_SUS_PWR_ACK pull down	reserve RH145	X01
74	26	HW	8/27/2010	COMPAL	Follow INTEL HDMI DG	remove R1164,R458,R1128--->20K add R1593 depop D65	X01
75	11	HW	8/30/2010	COMPAL	Change QC5 VGS to 20V part	Change QC5 to SB00000HK0L	X01
76	37	HW	9/1/2010	COMPAL	Depop SIM card ESD diode	Depop U40	X01
77	24	HW	10/6/2010	COMPAL	Change RB751V to HF part	Change D63,D64,D68,D69 to SCS00004L0L	X02
78	24	HW	10/6/2010	COMPAL	AUO panel can't adjust brightness	Change R1137 from 100k to 10k	X02
79	14,18	HW	10/6/2010	Intel	Follow DG1.5 and schematic check list rev1	Add RH41,depop RC96 and RC97,change RH177 to 10K	X02
80	30,31	HW	10/6/2010	IDT	To solve pop noise and detect issue	Add U6,Q33,Q46,D70,D71,R425,R33,R38,R430,R352,R1088,C967,C307,C308,R161	X02
81	32,42	HW	10/11/2010	COMPAL	LOM Cable Detect function	add U15, C478 change TP_DET# netname to WLAN_LAN_DISB# JTP1 pin1 change to GND	X02
82	42	HW	10/11/2010	COMPAL	Change Board ID to X02	Change R875 to 62K	X02
83	17	HW	10/11/2010	Intel	Follow Intel check list rev1.2	Add @RH332	X02
84	46	HW	10/11/2010	COMPAL	LED brightness test result	Change R957 to 560,R941,R939,R934 to 4.7k,R955,R949 to 2K	X02
85	24, 30	HW	10/19/2010	EMI	EMI issue for PWM and DMIC_CLK	Add L83,change R1582 to L82	X02
86	30	HW	10/19/2010	COMPAL	Change Codec rev to YA	Change U72 to SA00003ZZ2L	X02
87	32	HW	10/19/2010	COMPAL	Change LAN stepping to C0	Change U31 to SA00003SI2L	X02
88	39,40	HW	10/19/2010	ESD	PT ESD test result	Change U91,U92 to D72,D73. Pop D73	X02
89	24	HW	10/19/2010	Compal	PT ESD test result	remove D7,D8,DE1~DE4	X02

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90	32	HW	10/19/2010	COMPAL	IEEE test result	Change L30~L37 to 12nH	X02
91	28	HW	10/19/2010	COMPAL	Support SSD hard drive	Add PJP64,C399,C402	X02
92	31,43	HW	10/19/2010	COMPAL	Non-support Latitude on	depop SW2,C740,R877	X02
93	22	HW	10/19/2010	COMPAL	Change OTP set to 91 degree	Change R406 to 1.15k	X02
94	26	HW	10/20/2010	COMPAL	HDMI SDVO CTRL PU same as 14"	del D65,R1593	X02
95	30,42	HW	10/20/2010	COMPAL	GPIO map change AUD_NB_MUTE to AUD_NB_MUTE#	change AUD_NB_MUTE to AUD_NB_MUTE#	X02
96	14	HW	10/26/2010	COMPAL	Follow Intel CRB FAB2 PCH XDP schematic	Add @RH284	X02
97	41	HW	11/1/2010	COMPAL	EMI dock clk issue	pop R756=33ohm C704=12pf	X02
98	18	HW	11/1/2010	COMPAL	Follow schmaitc check list	depop RH174 RH175	X02
99	14	HW	11/8/2010	COMPAL	For easy control TAA/nonTAA BOM	Add R936 colay R895,R944 colay R897,R943 colay R900	X02
100	15	HW	11/8/2010	COMPAL	DF416400 AMT_Run MEflow Stress test fai	depop RH296 RH297,pop QH5 RH302,RH303	X02
101	25	HW	11/10/2010	COMPAL	Pericom VGA SW high EOS failure rate	Change C321,C318 from 0.1uF to 0.01uF(pin4,pin23)	X02
102	6-11,14-21	HW	11/10/2010	COMPAL	Change CPU PCH PN to QS sample	Change UH4 PN to SA00004IW1L ,U1 PN to SA00004EL1L	X02
103	46	HW	11/10/2010	ME	Change KB screw hole	Change H12 H13 from 2.3 to 2.6	X02
104	22	HW	11/10/2010	COMPAL	Thermal request change OTP set to 94 degree	Change R406 to 1.4k	X02
105	28	HW	11/18/2010	COMPAL	Follow Intel CRB SMBUS PU value	Change R501 R502 from 2.2k to 10k	X02
106	28,45	HW	11/19/2010	COMPAL	For cost saving(+5V_HDD / +3.3V_ALW_PCH)	De-pop R499,R500,C393,Q28,R905,R907,C762,Q51	X02
107	17,39	HW	12/23/2010	COMPAL	SW WHQL request USB debug need USB port1	Change USB port0 to port1	A00
108	43	HW	12/27/2010	COMPAL	Change Board ID to A00	Change R875 to 33k	A00
109	43	HW	12/27/2010	COMPAL	To solve backdrive issue	Pop Q45	A00
200	34-35	HW	12/27/2010	COMPAL	Change USH chip to CID7	Change U33 to SA00003AO2L	A00
201	30-31	HW	1/3/2011	COMPAL	remove MIC external detect	del U6,Q33,Q46,D70,D71,R425,R33,R38,R430,R352,R1088,C967,C307,C308,R161	A00
202	14	HW	1/5/2011	COMPAL	For cost saving	De-pop RH47,RH48,RH49,RH288	A00
203	22	HW	1/18/2011	COMPAL	Same as 14	Change R385 to 10K	A00
204	44	HW	1/21/2011	COMPAL	DF445509:TP will malfunction intermittently.	Change R902 to 2.2K	A00
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1	47	+DCIN	7/15	Compal	System can't recognize battery issue	Change PBATT2 Pin2 connection from Z4304 to Z5304 Change PBATT2 Pin2 connection from Z4305 to Z5305 Change PBATT2 Pin2 connection from Z4306 to Z5306	
2	47	+DCIN	7/15	Compal	System can't recognize battery issue	Change PR77 pin2 connection from BAY_SMBCLK to BAY_SMBDAT	
3	55	Charger	7/15	Compal	System can't recognize battery issue	Change PU11 pin 15 connection from CHARGER_SMBCLK to CHARGER_SMBDAT Change PU11 pin 16 connection from CHARGER_SMBDAT to CHARGER_SMBCLK	
4	47	+DCIN	8/4	Compal	Follow Macallan 14 for new battery cell	Change PL1 from SM01002078L to SM010009C8L and add PL20 Change PL19 from SM01002078L to SM010009C8L	
5	48	3/5V	8/4	Compal	Follow Macallan 14	Change PC24 from 4.7u/6.3V/0805 (SE093475K8L) to 4.7u/6.3V/0603 (SE107475K8L)	
6	47	+DCIN	8/4	Compal	RTC remove detect function (7/29 EE mail)	Delete JRTC1 pin2 RTC_DET# connection	
7	56	+VCC_SA	8/4	Compal	Follow Macallan 14 VCCSA not fix at 0.8V. change net name from +0.8V_VCC_SA to +VCC_SA	Change +0.8V_VCC net name to +VCCSA_P Change 0.8V_VCCPWROK net name to VCCSAPWROK	
8	55	Charger	8/4	Compal	Follow Macallan 14	Depop PD14 SBR3A40SA (SC100003J00)	
9	57	Selector	8/4	Compal	Follow Macallan 14 Leakage issue on PD16	Change PD16 from SBR3A40SA (SC100003J00) to ES2AA (SC100005A0L)	
10	55	Charger	8/4	Compal	Follow Macallan 14 Add adapter protection circuit for turbo mode	Add PU11 pin8 connection ICREF Add PU11 pin23 connection ICOUT Add PR259,PR260,PR261,PR295, PR331,PR332 Add PC279,PC280 Add PQ38	
11	56	VCCSA	8/18	Intel	Intel change BGA1023 VID table VID0 0 VID1 1 voltage from 0.8V to 0.85V	Change VID setting	
12	53,54	Vcore, VGFX	8/18	Maxim	Reserve 0402 cap pad for transient fine tune	Add PC281 and PC282 0402 cap location	
13	53,54	Vcore, VGFX	8/18	Maxim	change setting for Pass2 sample	Change PR330 from 2_ohm to 0_ohm Change PR127 from 150K_ohm to 165K_ohm Change PR135 from 100K_ohm to 105K_ohm Change PR157 from 8.66K_ohm to 10.2K_ohm Change PR190 from 1.43K_ohm to 1.37K_ohm Change PR192 from 2_ohm to 0_ohm de-pop PR201 Change PR110 PR112 PR115 from 12.7K_ohm to 13.3K_ohm	
14	53,54	Vcore, VGFX	8/18	Compal	Change PQ9 PQ10 PQ11 to prevent COS issue	Change PQ9 form CSD86350Q5D to PQ9 AON6414AL + PQ10 AON6704L Change PQ10 form CSD86350Q5D to PQ11 AON6414AL + PQ15 AON6704L Change PQ11 form CSD86350Q5D to PQ3 AON6414AL + PQ14 AON6704L	
15	56	VCCSA	8/23	TI	Change Thermal pad to PGND	Change PU13 pin 25 from GNDA_VCCSA to PGND	
16	56	VCCSA	8/23	TI	For batter output voltage accuracy	Add PC383 from PR247 pin2 to PU13 pin2	
17	55	Charger	8/24	Dell	Add turbo mode adapter protection by H_PROCHOT#	Add PR336 PR337 for pop option to select H_PROCHOT# or DYN_TUR_PWR_ALRT#	

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