Mosaic Schematics Document

uFCBGA/uFCPGA Northwood

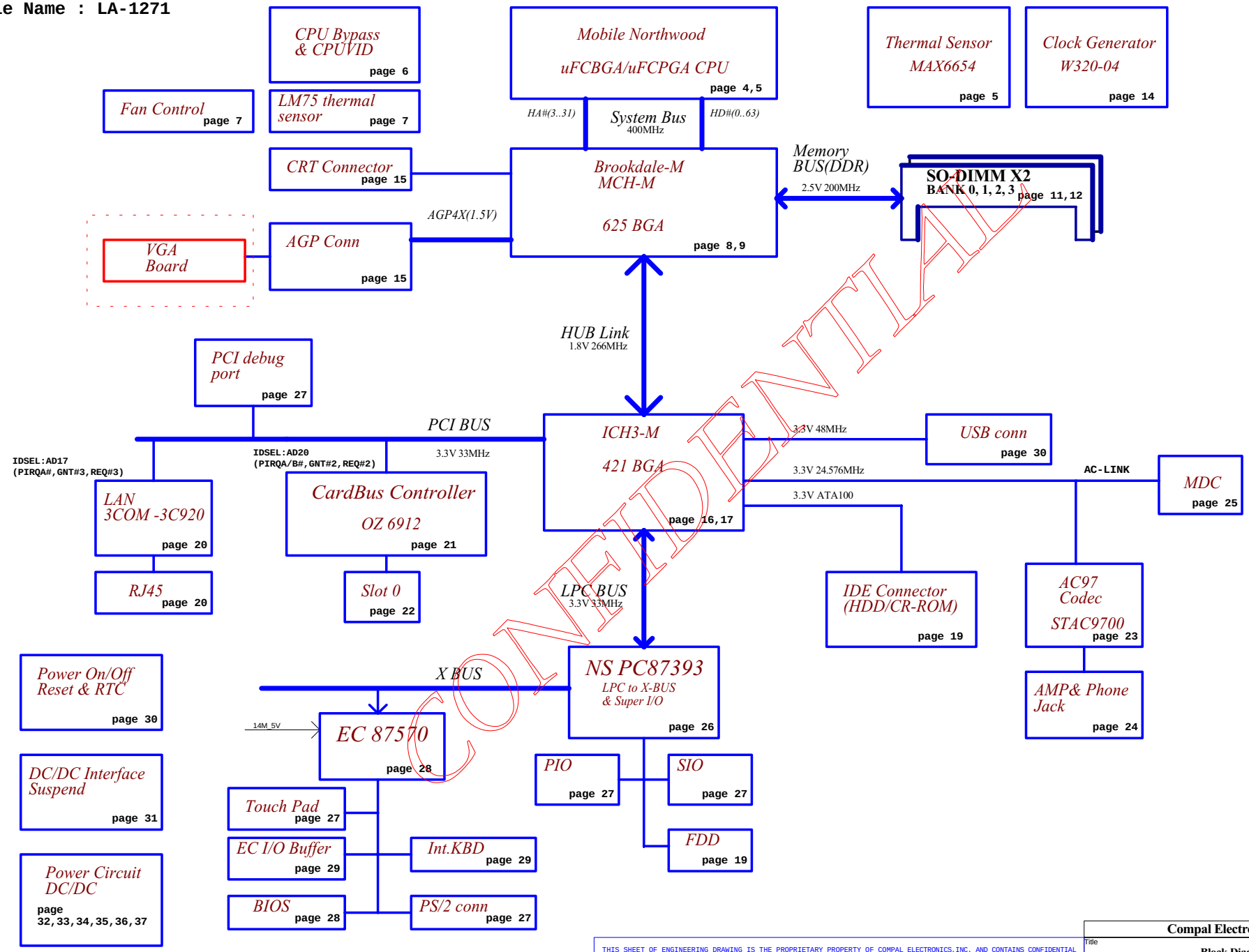
2001-09-19

REV: 0.1

Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: ADY13 LA-1271	Rev: 0.1
Date: Wednesday, September 19, 2001	Sheet 1 of 37	

Model Name :ADY13(Mosaic)

File Name : LA-1271



Compal Electronics, Inc.		
Title: Block Diagram		
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Function \ Model	Mosaic	Midas
FDD	YES	YES
PS/2	YES	YES
Serial port	NO	NO
Parallel port	YES	YES
RJ45	YES	YES
OZ6912/TPS2211	YES	YES
3Com Lan chipset(3C920)	YES S/W disable	YES

Note1:
"@" means all model depop

Note2:
Removed serial port,because add 2nd Fan

Power Managment table

State \ Signal	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	CHIPS Rev	CHIPS Rev
SST-Build	RG82845 A3(QC45)	FW82801CAM B1(QC42)

Compal Electronics, Inc.

Title: Note & Revision

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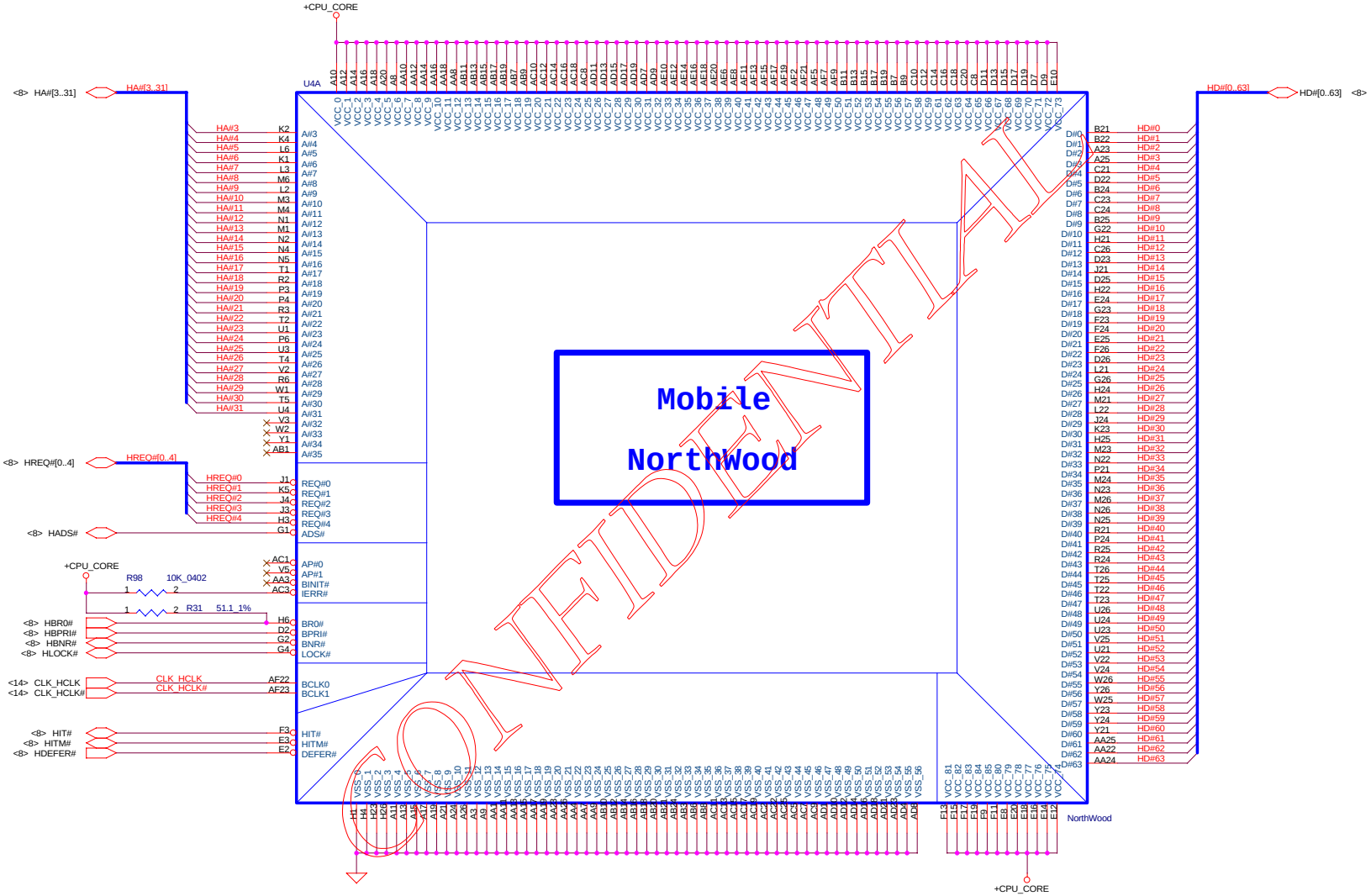

Compal Electronics, Inc.

Title: **Mobile Northwood uFCPGA**

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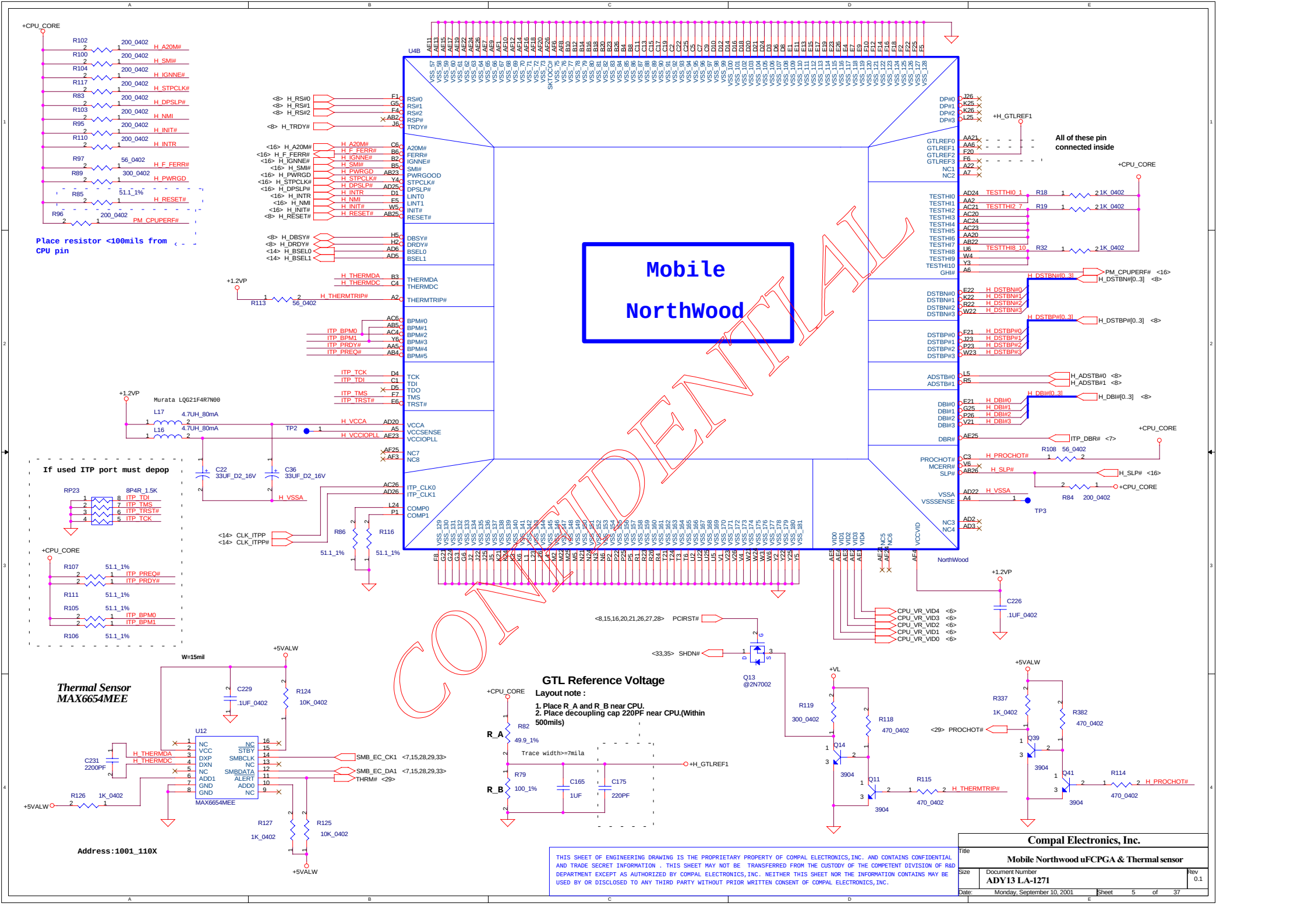

Compal Electronics, Inc.		
Title: Mobile Northwood uFCPGA & Thermal sensor		
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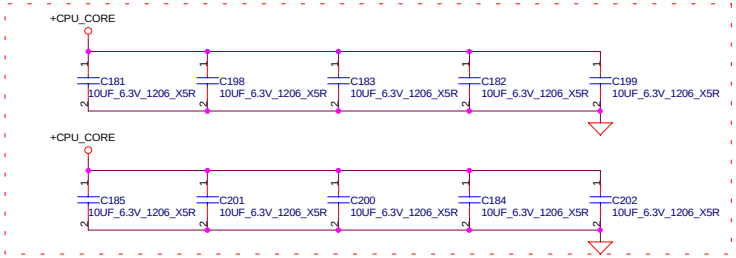
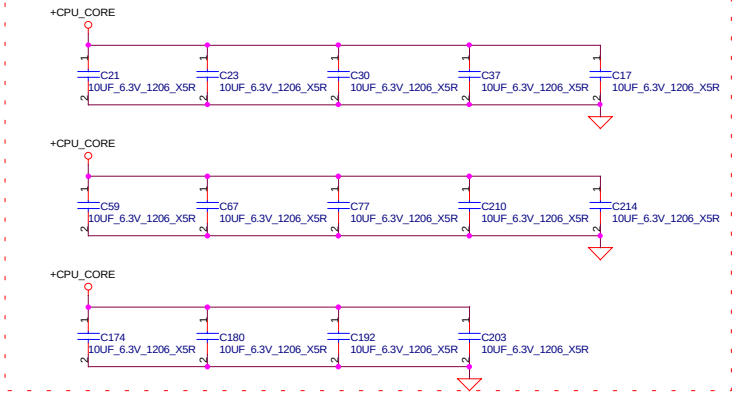
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

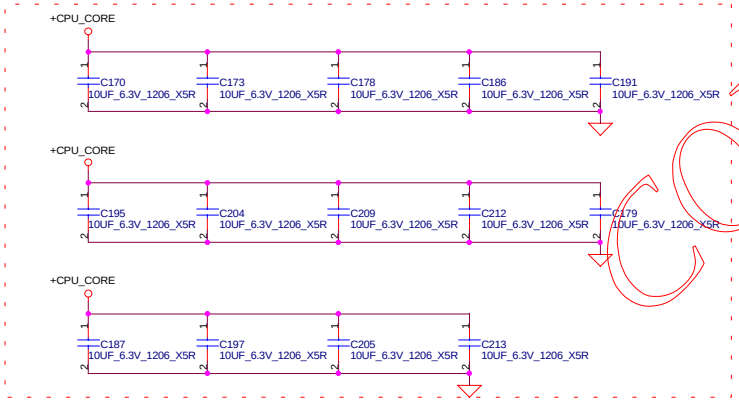
Please place these cap in the socket cavity area



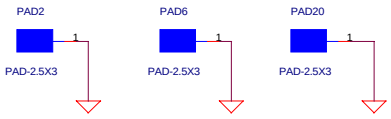
Please place these cap on the socket north side



Please place these cap on the socket south side



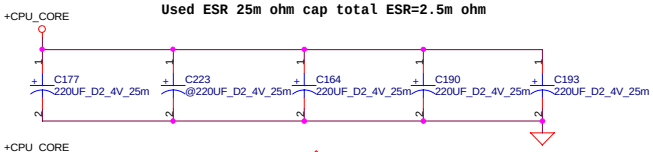
EMI Clip PAD for CPU

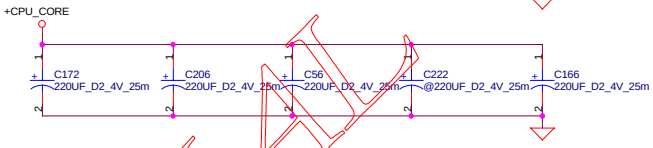


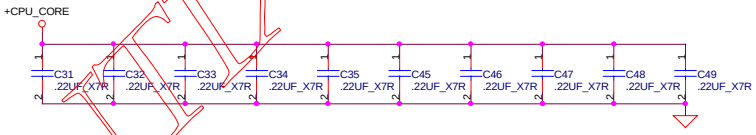
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

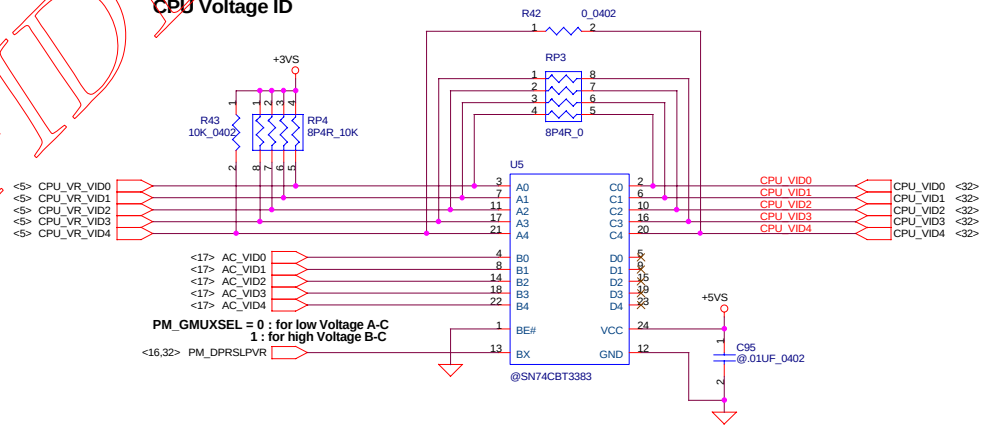
Used ESR 25m ohm cap total ESR=2.5m ohm







CPU Voltage ID



Compal Electronics, Inc.

Title: **CPU Bypass & CPU VID**

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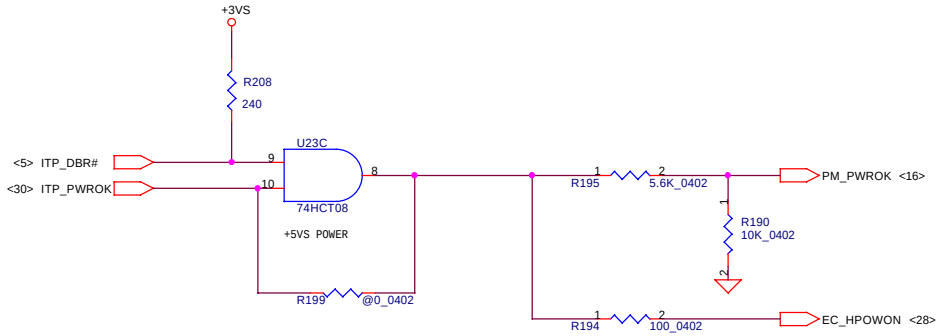
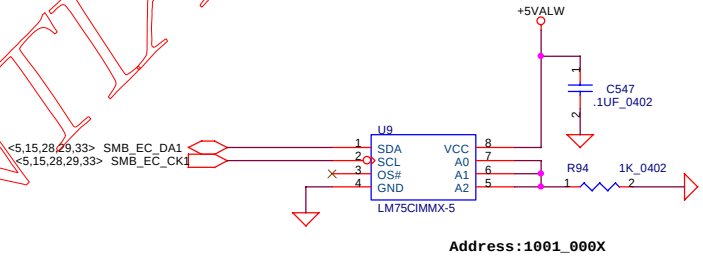
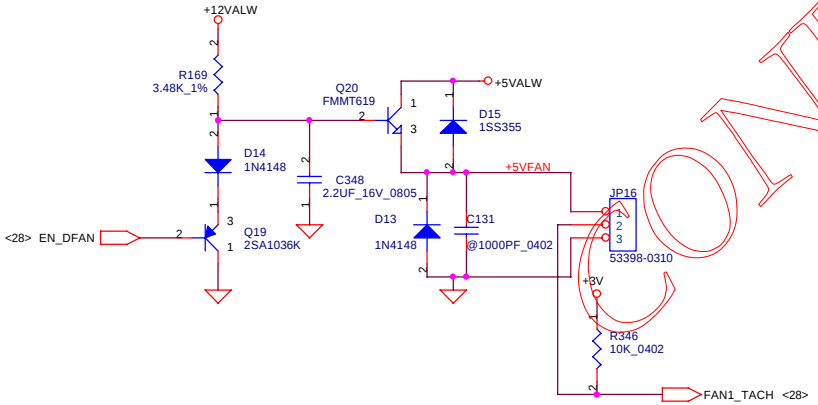
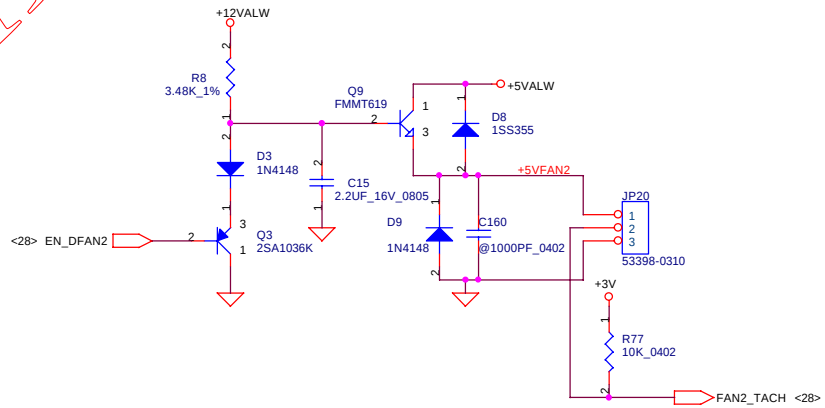




Fan1 Control circuit



Fan2 Control circuit



COMPAL Electronics,Inc	
Title	LM75 Thermal sensor & Fan control
Size	Document Number: ADY13 LA-1271 — Rev: 0.1
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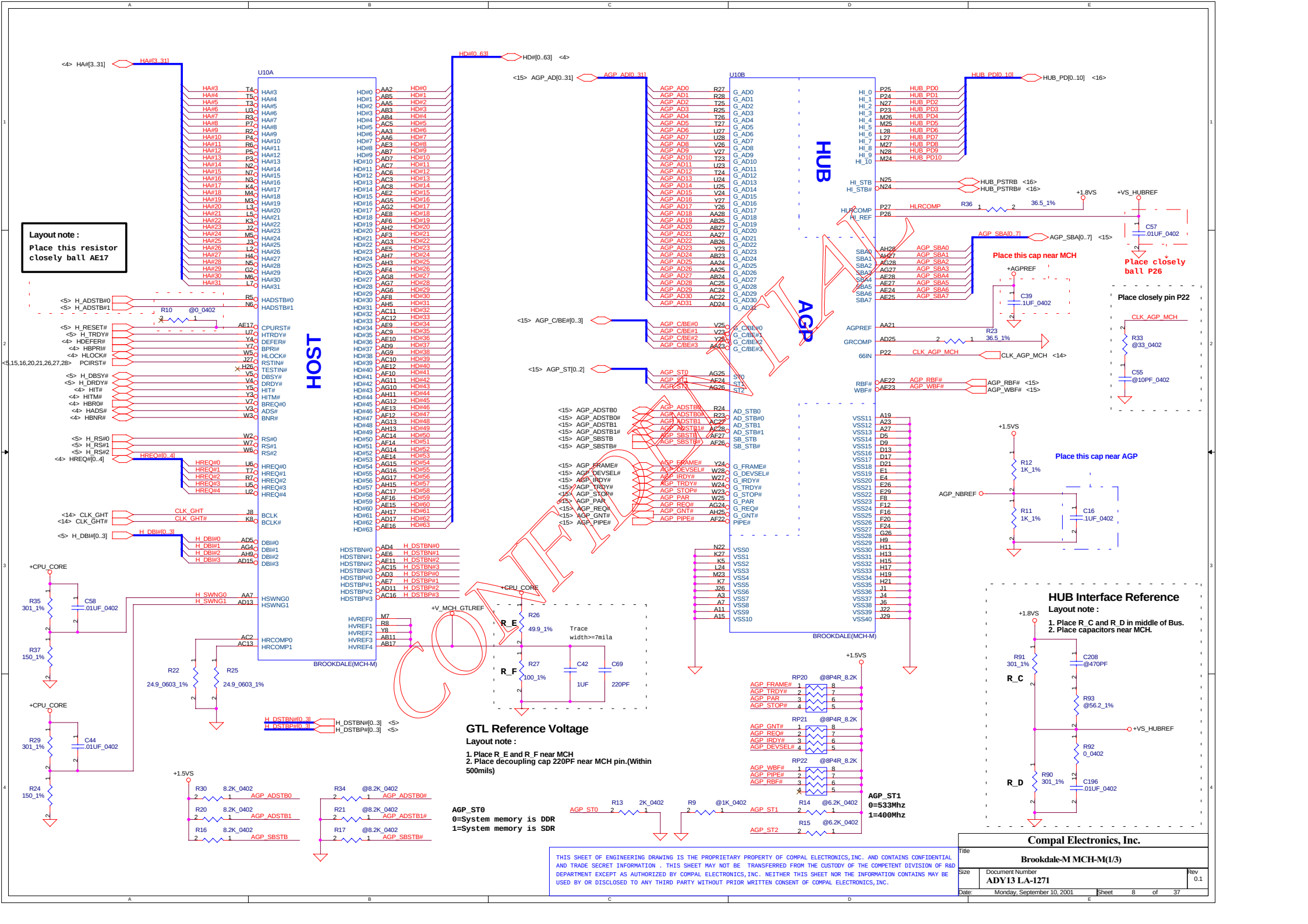
Layout note :
Place this resistor closely ball AE17
HOST
BROOKDALE(MCH-M)
HUB
AGP
BROOKDALE(MCH-M)
Place this cap near MCH
Place closely ball P26
Place closely pin P22
Place this cap near AGP
GTL Reference Voltage
Layout note :
1. Place R_E and R_F near MCH
2. Place decoupling cap 220PF near MCH pin.(Within 500mils)
AGP_ST0
0=System memory is DDR
1=System memory is SDR
AGP_ST1
0=533Mhz
1=400Mhz
HUB Interface Reference
Layout note :
1. Place R_C and R_D in middle of Bus.
2. Place capacitors near MCH.
Compal Electronics, Inc.
Brookdale-M MCH-M(1/3)
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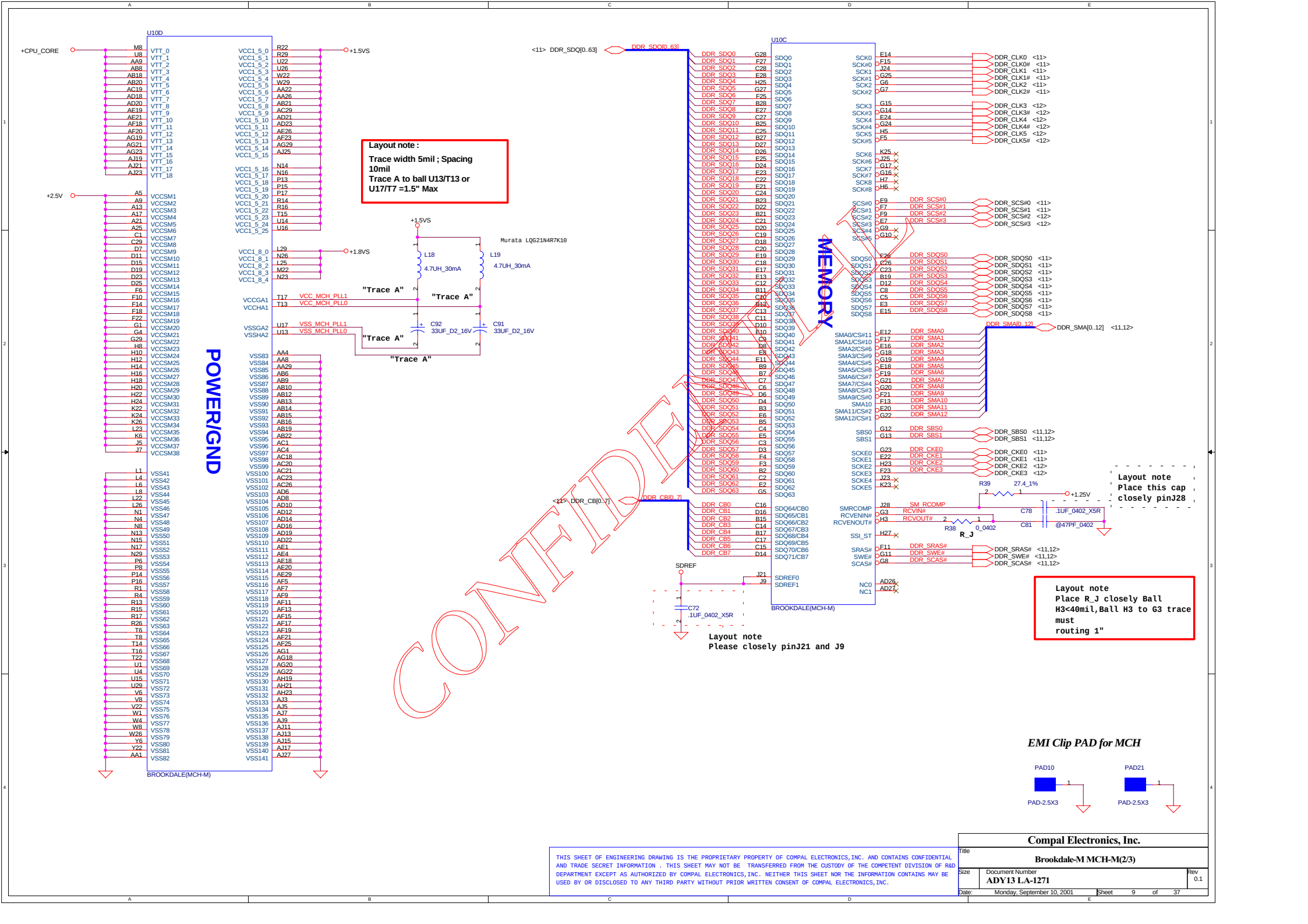

Compal Electronics, Inc.	
Title	Brookdale-M MCH-M(2/3)
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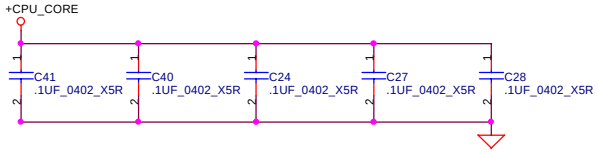
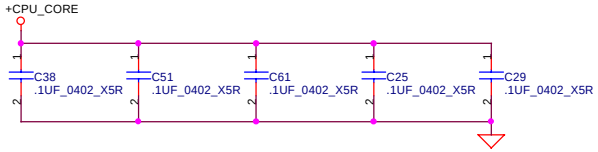
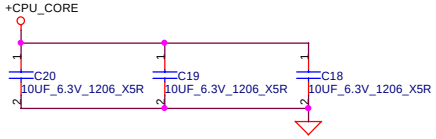
Layout note : Processor system bus

Distribute as close as possible to MCH Processor Quadrant.(between VTTFSB and VSS pin)

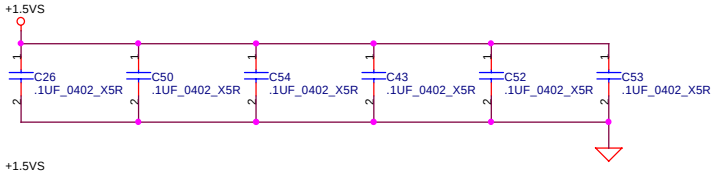


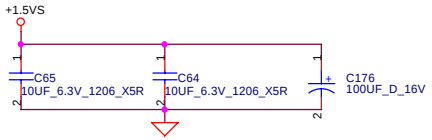




Layout note : AGP/CORE

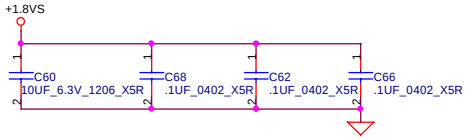
Distribute as close as possible to MCH Processor Quadrant.(between VCCAGP/VCCCORE and VSS pin)





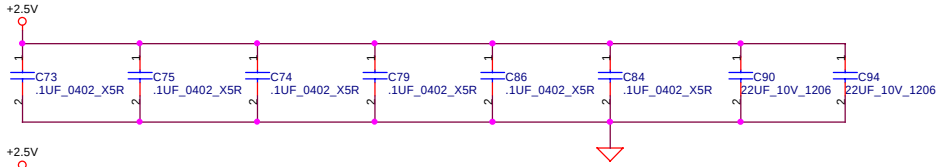
Layout note : Hub-Link

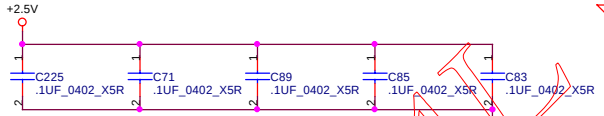
Distribute as close as possible to MCH Processor Quadrant.(between VCCHL and VSS pin)

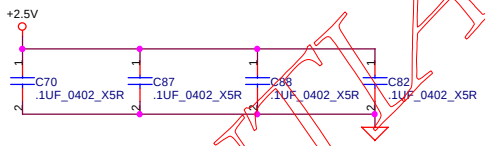


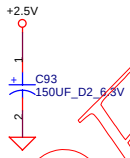
Layout note : DDR Memory interface

Distribute as close as possible to MCH Processor Quadrant.(between VCCSM and VSS pin)









Compal Electronics, Inc.		
Title: MCH-M Decoupling		
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Layout note

Place these resistor closely DIMM0, all trace length<750mil

RP48 4P2R_22: DDR_SDQ0 / DDR_SDQ4 — DDR_DQ0 / DDR_DQ4
RP24 4P2R_22: DDR_SDQ1 / DDR_SDQ5 — DDR_DQ1 / DDR_DQ5
RP49 4P2R_22: DDR_SDQ6 / DDR_SDQS0 — DDR_DQ6 / DDR_DQS0
RP25 4P2R_22: DDR_SDQ2 / DDR_SDQ3 — DDR_DQ2 / DDR_DQ3
RP50 4P2R_22: DDR_SDQ8 / DDR_SDQ7 — DDR_DQ8 / DDR_DQ7
RP26 4P2R_22: DDR_SDQ9 / DDR_SDQ12 — DDR_DQ9 / DDR_DQ12
RP51 4P2R_22: DDR_SDQS1 / DDR_SDQ13 — DDR_DQS1 / DDR_DQ13
RP27 4P2R_22: DDR_SDQ10 / DDR_SDQ14 — DDR_DQ10 / DDR_DQ14
RP52 4P2R_22: DDR_SDQ15 / DDR_SDQ11 — DDR_DQ15 / DDR_DQ11
RP29 4P2R_22: DDR_SDQ16 / DDR_SDQ20 — DDR_DQ16 / DDR_DQ20
RP53 4P2R_22: DDR_SDQ21 / DDR_SDQ17 — DDR_DQ21 / DDR_DQ17
RP30 4P2R_22: DDR_SDQ18 / DDR_SDQS2 — DDR_DQ18 / DDR_DQS2
RP54 4P2R_22: DDR_SDQ19 / DDR_SDQ22 — DDR_DQ19 / DDR_DQ22
RP31 4P2R_22: DDR_SDQ24 / DDR_SDQ23 — DDR_DQ24 / DDR_DQ23
RP55 4P2R_22: DDR_SDQ25 / DDR_SDQ28 — DDR_DQ25 / DDR_DQ28
RP32 4P2R_22: DDR_SDQS3 / DDR_SDQ29 — DDR_DQS3 / DDR_DQ29

RP56 4P2R_22: DDR_SDQ30 / DDR_SDQ26 — DDR_DQ30 / DDR_DQ26
RP33 4P2R_22: DDR_SDQ31 / DDR_SDQ27 — DDR_DQ31 / DDR_DQ27
RP57 4P2R_22: DDR_CB5 / DDR_CB4 — DDR_F_CB5 / DDR_F_CB4
RP34 4P2R_22: DDR_CB1 / DDR_CB0 — DDR_F_CB1 / DDR_F_CB0
RP58 4P2R_22: DDR_CB2 / DDR_SDQS8 — DDR_F_CB2 / DDR_DQS8
RP28 4P2R_22: DDR_CB3 / DDR_CB6 — DDR_F_CB3 / DDR_F_CB6
RP68 4P2R_22: DDR_CB7 — DDR_F_CB7
RP59 4P2R_22: DDR_SDQ36 / DDR_SDQ32 — DDR_DQ36 / DDR_DQ32
RP39 4P2R_22: DDR_SDQ33 / DDR_SDQ37 — DDR_DQ33 / DDR_DQ37
RP40 4P2R_22: DDR_SDQ38 / DDR_SDQS4 — DDR_DQ38 / DDR_DQS4
RP60 4P2R_22: DDR_SDQ39 / DDR_SDQ34 — DDR_DQ39 / DDR_DQ34
RP41 4P2R_22: DDR_SDQ44 / DDR_SDQ35 — DDR_DQ44 / DDR_DQ35
RP61 4P2R_22: DDR_SDQ45 / DDR_SDQ40 — DDR_DQ45 / DDR_DQ40
RP42 4P2R_22: DDR_SDQS5 / DDR_SDQ41 — DDR_DQS5 / DDR_DQ41
RP62 4P2R_22: DDR_SDQ43 / DDR_SDQ42 — DDR_DQ43 / DDR_DQ42
RP43 4P2R_22: DDR_SDQ47 / DDR_SDQ46 — DDR_DQ47 / DDR_DQ46

<9> DDR_SDQ[0..63]
<9> DDR_CB[0..7]
<9> DDR_SDQS[0..8]
DDR_SDQ[0..63]
DDR_CB[0..7]
DDR_SDQS[0..8]

RP63 4P2R_22: DDR_SDQ49 / DDR_SDQ48 — DDR_DQ49 / DDR_DQ48
RP44 4P2R_22: DDR_SDQ53 / DDR_SDQ52 — DDR_DQ53 / DDR_DQ52
RP64 4P2R_22: DDR_SDQ54 / DDR_SDQS6 — DDR_DQ54 / DDR_DQS6
RP45 4P2R_22: DDR_SDQ55 / DDR_SDQ50 — DDR_DQ55 / DDR_DQ50

RP65 4P2R_22: DDR_SDQ56 / DDR_SDQ51 — DDR_DQ56 / DDR_DQ51
RP46 4P2R_22: DDR_SDQ60 / DDR_SDQ57 — DDR_DQ60 / DDR_DQ57
RP66 4P2R_22: DDR_SDQS7 / DDR_SDQ61 — DDR_DQS7 / DDR_DQ61
RP47 4P2R_22: DDR_SDQ62 / DDR_SDQ58 — DDR_DQ62 / DDR_DQ58
RP67 4P2R_22: DDR_SDQ63 / DDR_SDQ59 — DDR_DQ63 / DDR_DQ59

+2.5V
+2.5V
SDREF
C260 .1UF_0402

JP22 (DDR-SODIMM_200_Normal)

	VREF	VREF	
	VSS	VSS	
DDR_DQ4	DQ0	DQ4	DDR_DQ0
DDR_DQ5	DQ1	DQ5	DDR_DQ1
	VDD	VDD	
DDR_DQS0	DQS0	DM0	
DDR_DQ3	DQ2	DQ6	DDR_DQ6
	VSS	VSS	
DDR_DQ7	DQ3	DQ7	DDR_DQ2
DDR_DQ12	DQ8	DQ12	DDR_DQ8
	VDD	VDD	
DDR_DQ13	DQ9	DQ13	DDR_DQ9
DDR_DQS1	DQS1	DM1	
	VSS	VSS	
DDR_DQ14	DQ10	DQ14	DDR_DQ10
DDR_DQ11	DQ11	DQ15	DDR_DQ15
	VDD	VDD	
<9> DDR_CLK1	CK0	VDD	
<9> DDR_CLK1#	CK0#	VSS	
	VSS	VSS	
DDR_DQ20	DQ16	DQ20	DDR_DQ16
DDR_DQ17	DQ17	DQ21	DDR_DQ21
	VDD	VDD	
DDR_DQS2	DQS2	DM2	
DDR_DQ22	DQ18	DQ22	DDR_DQ18
	VSS	VSS	
DDR_DQ23	DQ19	DQ23	DDR_DQ19
DDR_DQ28	DQ24	DQ28	DDR_DQ24
	VDD	VDD	
DDR_DQ29	DQ25	DQ29	DDR_DQ25
DDR_DQS3	DQS3	DM3	
	VSS	VSS	
DDR_DQ26	DQ26	DQ30	DDR_DQ30
DDR_DQ27	DQ27	DQ31	DDR_DQ31
	VDD	VDD	
DDR_F_CB4	CB0	CB4	DDR_F_CB5
DDR_F_CB0	CB1	CB5	DDR_F_CB1
	VSS	VSS	
DDR_DQS8	DQS8	DM8	
DDR_F_CB6	CB2	CB6	
	VDD	VDD	DDR_F_CB2
DDR_F_CB7	CB3	CB7	DDR_F_CB3
	DU	DU/RESET#	
	VSS	VSS	
<9> DDR_CLK0	CK2	VSS	
<9> DDR_CLK0#	CK2#	VDD	
	VDD	VDD	
<9> DDR_CKE1	CKE1	CKE0	DDR_CKE0
DDR_SMA12	DU/A13	DU/BA2	
DDR_SMA9	A12	A11	DDR_SMA11
	A9	A8	DDR_SMA8
	VSS	VSS	
DDR_SMA7	A7	A6	DDR_SMA6
DDR_SMA5	A5	A4	DDR_SMA4
DDR_SMA3	A3	A2	DDR_SMA2
DDR_SMA1	A1	A0	DDR_SMA0
	VDD	VDD	
DDR_SMA10	A10/AP	BA1	DDR_SBS1
DDR_SBS0	BA0	RAS#	DDR_SRAS#
DDR_SWE#	WE#	CAS#	DDR_SCAS#
DDR_SCS#0	S0#	S1#	DDR_SCS#1
	DU	DU	
	VSS	VSS	
DDR_DQ36	DQ32	DQ36	DDR_DQ32
DDR_DQ33	DQ33	DQ37	DDR_DQ37
	VDD	VDD	
DDR_DQS4	DQS4	DM4	
DDR_DQ38	DQ34	DQ38	DDR_DQ34
	VSS	VSS	
DDR_DQ39	DQ35	DQ39	DDR_DQ35
DDR_DQ44	DQ40	DQ44	DDR_DQ40
	VDD	VDD	
DDR_DQ45	DQ41	DQ45	DDR_DQ41
DDR_DQS5	DQS5	DM5	
	VSS	VSS	
DDR_DQ43	DQ42	DQ46	DDR_DQ42
DDR_DQ47	DQ43	DQ47	DDR_DQ46
	VDD	VDD	
	VDD	CK1#	DDR_CLK2#
	VSS	CK1	DDR_CLK2
	VSS	VSS	
DDR_DQ49	DQ48	DQ52	DDR_DQ48
DDR_DQ53	DQ49	DQ53	DDR_DQ52
	VDD	VDD	
DDR_DQS6	DQS6	DM6	
DDR_DQ54	DQ50	DQ54	DDR_DQ50
	VSS	VSS	
DDR_DQ55	DQ51	DQ55	DDR_DQ51
DDR_DQ56	DQ56	DQ57	DDR_DQ57
	VDD	VDD	
DDR_DQ60	DQ57	DQ61	DDR_DQ61
DDR_DQS7	DQS7	DM7	
	VSS	VSS	
DDR_DQ62	DQ58	DQ62	DDR_DQ58
DDR_DQ63	DQ59	DQ63	DDR_DQ59
	VDD	VDD	
	SDA	SA0	
	SCL	SA1	
	VDD_SPD	SA2	
	VDD_ID	DU	

<12,14> DIMM_SMDATA
<12,14> DIMM_SMCLK
+3VS

DDR_DQ[0..63] — DDR_DQ[0..63] <12>
DDR_F_CB[0..7] — DDR_F_CB[0..7] <12>
DDR_DQS[0..8] — DDR_DQS[0..8] <12>

DDR_SMA[0..12] <9,12>

RP8 4P2R_10: DDR_SMA12 / DDR_SMA9 — DDR_F_SMA12 / DDR_F_SMA9
RP35 4P2R_10: DDR_SMA8 / DDR_SMA11 — DDR_F_SMA8 / DDR_F_SMA11
RP7 4P2R_10: DDR_SMA7 / DDR_SMA5 — DDR_F_SMA7 / DDR_F_SMA5
RP36 4P2R_10: DDR_SMA4 / DDR_SMA6 — DDR_F_SMA4 / DDR_F_SMA6
RP6 4P2R_10: DDR_SMA3 / DDR_SMA1 — DDR_F_SMA3 / DDR_F_SMA1
RP37 4P2R_10: DDR_SMA0 / DDR_SMA2 — DDR_F_SMA0 / DDR_F_SMA2
R44 10_0402: DDR_SMA10 — DDR_F_SMA10

<12> DDR_F_SMA[0..12]

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

Layout note

Place these resistor closely DIMM0, all trace length Max=1.3"

+1.25V
RP89 4P2R_56: DDR_CKE1 / DDR_CKE0
RP94 4P2R_56: DDR_SCS#0 / DDR_SCS#1

Layout note

Place these resistor closely DIMM0, all trace length<=750mil

<9,12> DDR_SBS0 / DDR_SWE# — RP5 4P2R_10 — DDR_F_SBS0 / DDR_F_SWE# <12>
<9,12> DDR_SCAS# / DDR_SRAS# — RP38 4P2R_10 — DDR_F_SCAS# / DDR_F_SRAS# <12>
<9,12> DDR_SBS1 — R137 10_0402 — DDR_F_SBS1 <12>

DIMM0

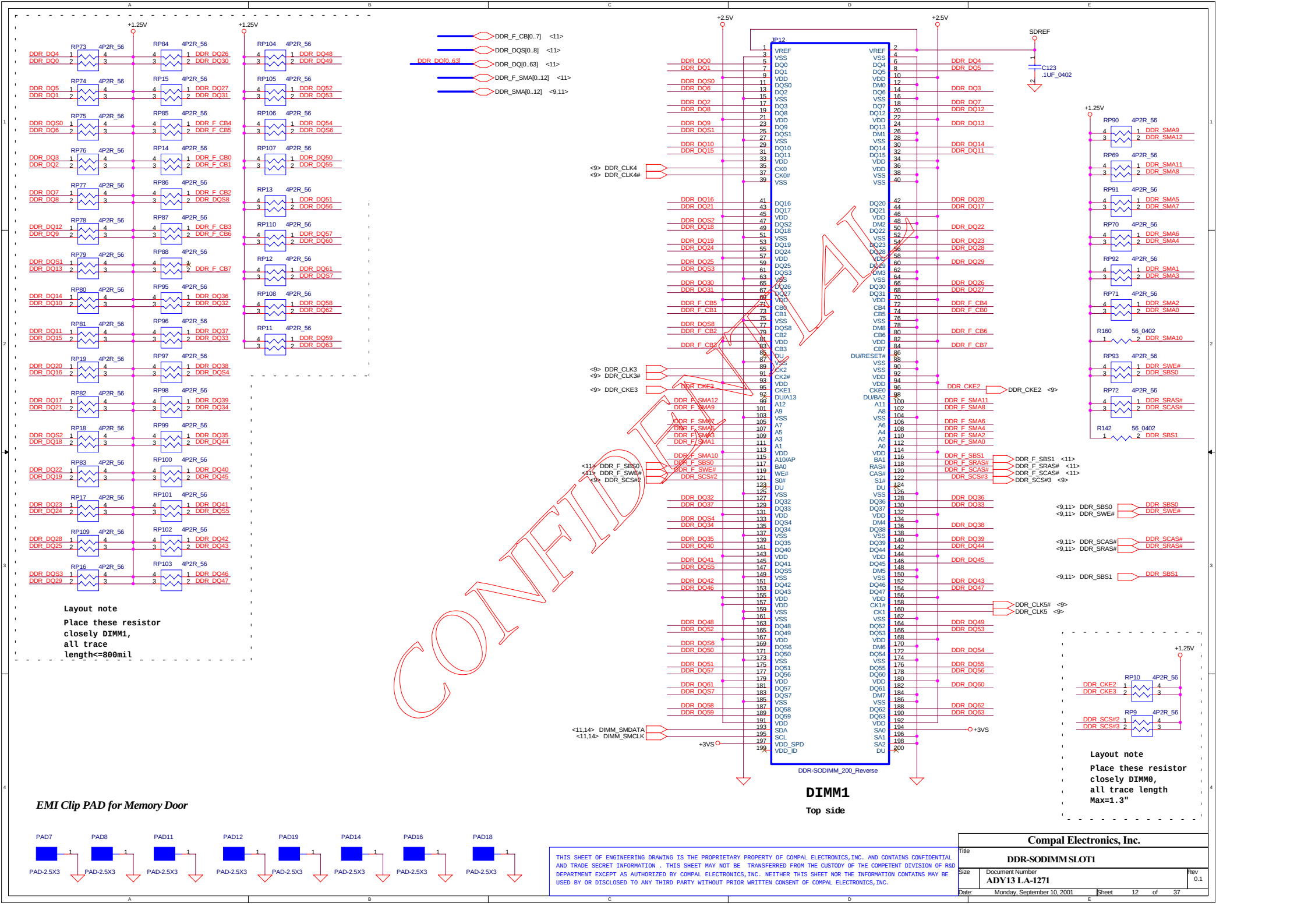
Bottom side

Compal Electronics, Inc.

Title: **DDR-SODIMM SLOT1**

Size | Document Number: **ADY13 LA-1271** | Rev: 0.1

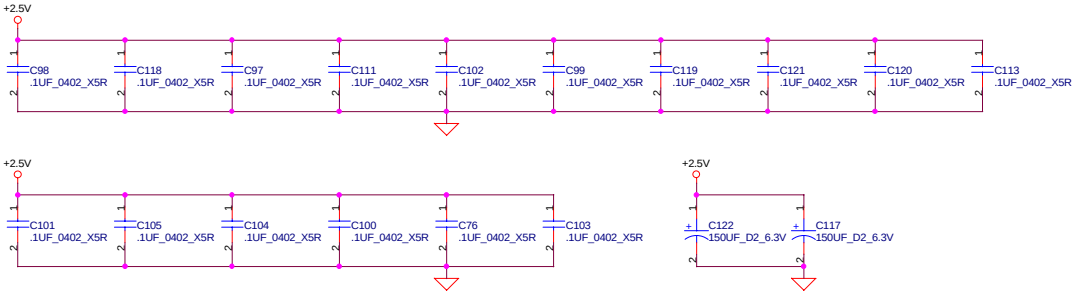
Date: Monday, September 10, 2001 | Sheet 11 of 37



Compal Electronics, Inc.		
Title: DDR-SODIMM SLOT1		
Size	Document Number: ADY13 LA-1271	Rev: 0.1
Date: Monday, September 10, 2001	Sheet 12 of 37	

Layout note :

Distribute as close as possible to DDR-SODIMM.

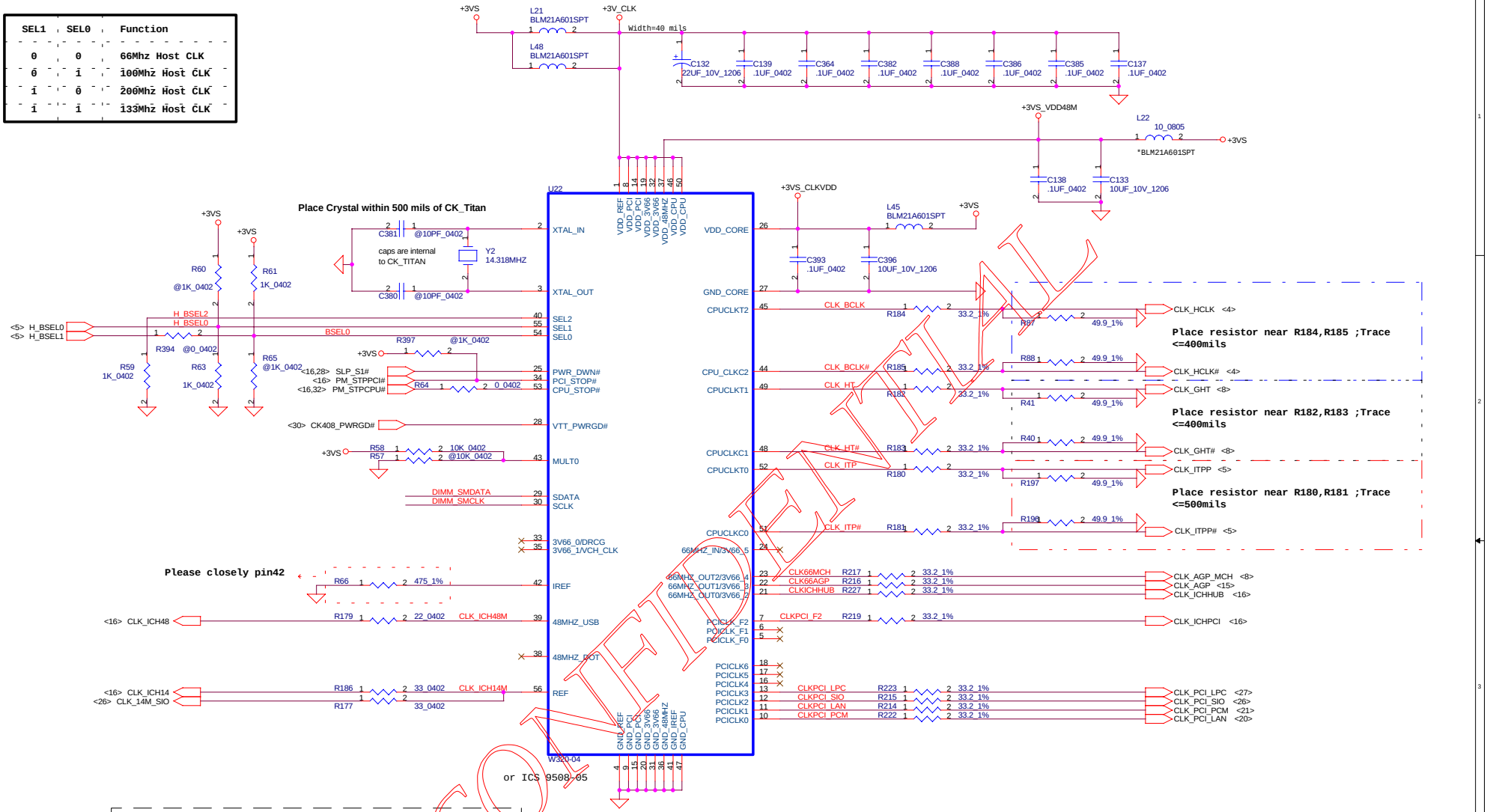


Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V

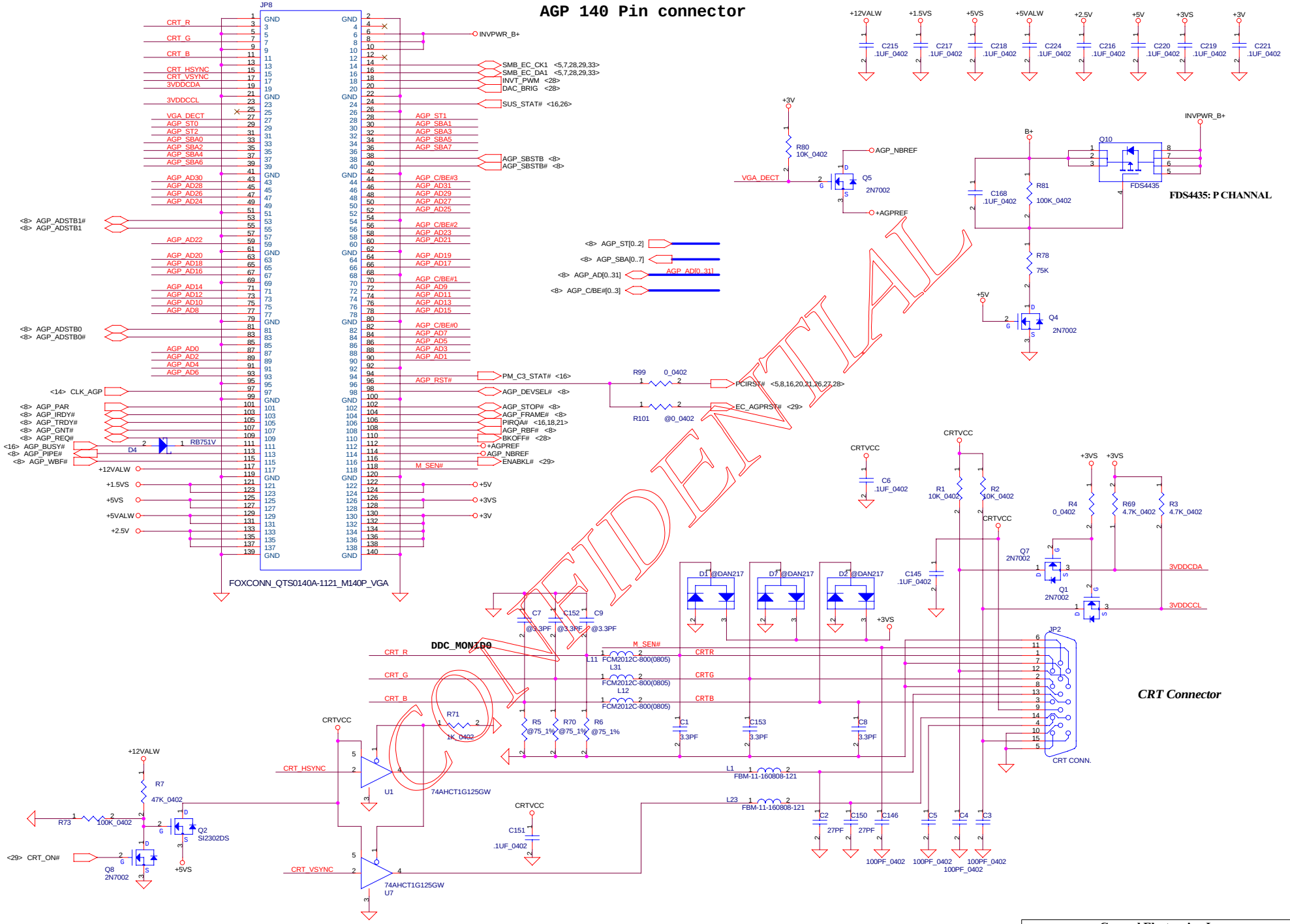
Compal Electronics, Inc.	
Title	DDR SODIMM Decoupling
Size	Document Number: ADY13 LA-1271 — Rev: 0.1
Date: Wednesday, September 19, 2001	Sheet 13 of 37

SEL1	SEL0	Function
0	0	66Mhz Host CLK
0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK



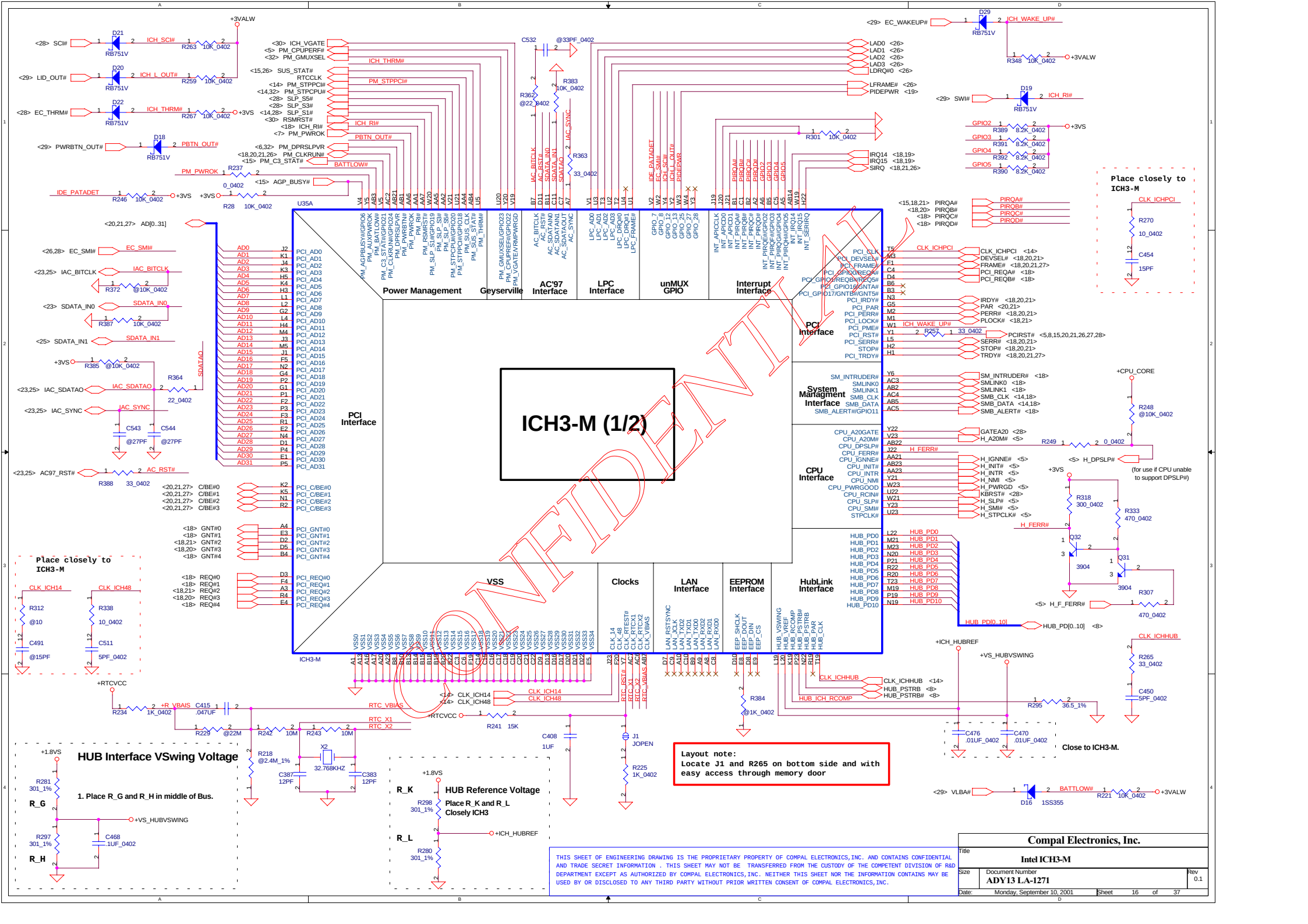
Compal Electronics, Inc.	
Title	Clock Generator
Size	Document Number: ADY13 LA-1271
Rev	0.1
Date:	Monday, September 10, 2001
Sheet	14 of 37

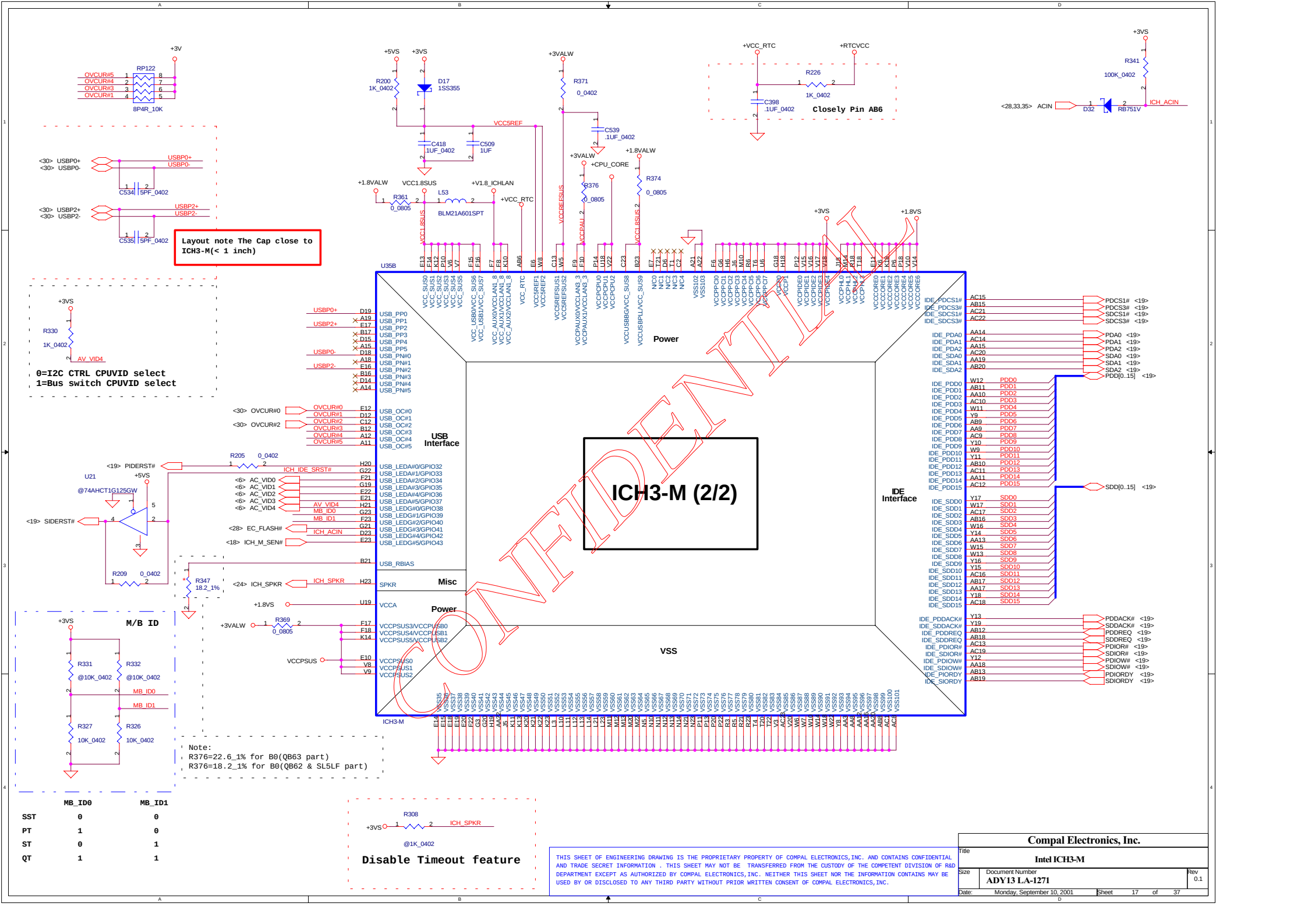
AGP 140 Pin connector



Compal Electronics, Inc.	
Title	AGPConn. & CRT
Size	Document Number ADY13 LA-1271
Rev	0.1
Date: Monday, September 10, 2001	Sheet 15 of 37

ICH3-M (1/2)




ICH3-M (2/2)
U35B
ICH3-M
Power
USB Interface
Misc
Power
VSS
IDE Interface
RP122
8P4R_10K
OVCUR#5
OVCUR#4
OVCUR#3
OVCUR#1
USBP0+
USBP0-
USBP2+
USBP2-
C534 5PF_0402
C535 5PF_0402
Layout note The Cap close to ICH3-M(< 1 inch)
R200 1K_0402
D17 1SS355
C418 1UF_0402
C509 1UF
VCC5REF
R371 0_0402
C539 .1UF_0402
+3VALW
+1.8VALW
+CPU_CORE
R376 0_0805
R374 0_0805
R361 0_0805
L53 BLM21A601SPT
+V1.8_ICHLAN
+VCC_RTC
VCC1.8SUS
+VCC_RTC
+RTCVCC
R226 1K_0402
C398 .1UF_0402
Closely Pin AB6
R341 100K_0402
ACIN
D32 RB751V
ICH_ACIN
R330 1K_0402
AV_VID4
0=I2C CTRL CPUVID select
1=Bus switch CPUVID select
R205 0_0402
PIDERST#
ICH_IDE_SRST#
U21
@74AHCT1G125GW
SIDERST#
R209 0_0402
R347 18.2_1%
AC_VID0
AC_VID1
AC_VID2
AC_VID3
AC_VID4
MB_ID0
MB_ID1
EC_FLASH#
ICH_ACIN
ICH_M_SEN#
ICH_SPKR
R369 0_0805
M/B ID
R331 @10K_0402
R332 @10K_0402
R327 10K_0402
R326 10K_0402
Note:
R376=22.6_1% for B0(QB63 part)
R376=18.2_1% for B0(QB62 & SL5LF part)
MB_ID0 MB_ID1
SST 0 0
PT 1 0
ST 0 1
QT 1 1
R308 @1K_0402
ICH_SPKR
Disable Timeout feature
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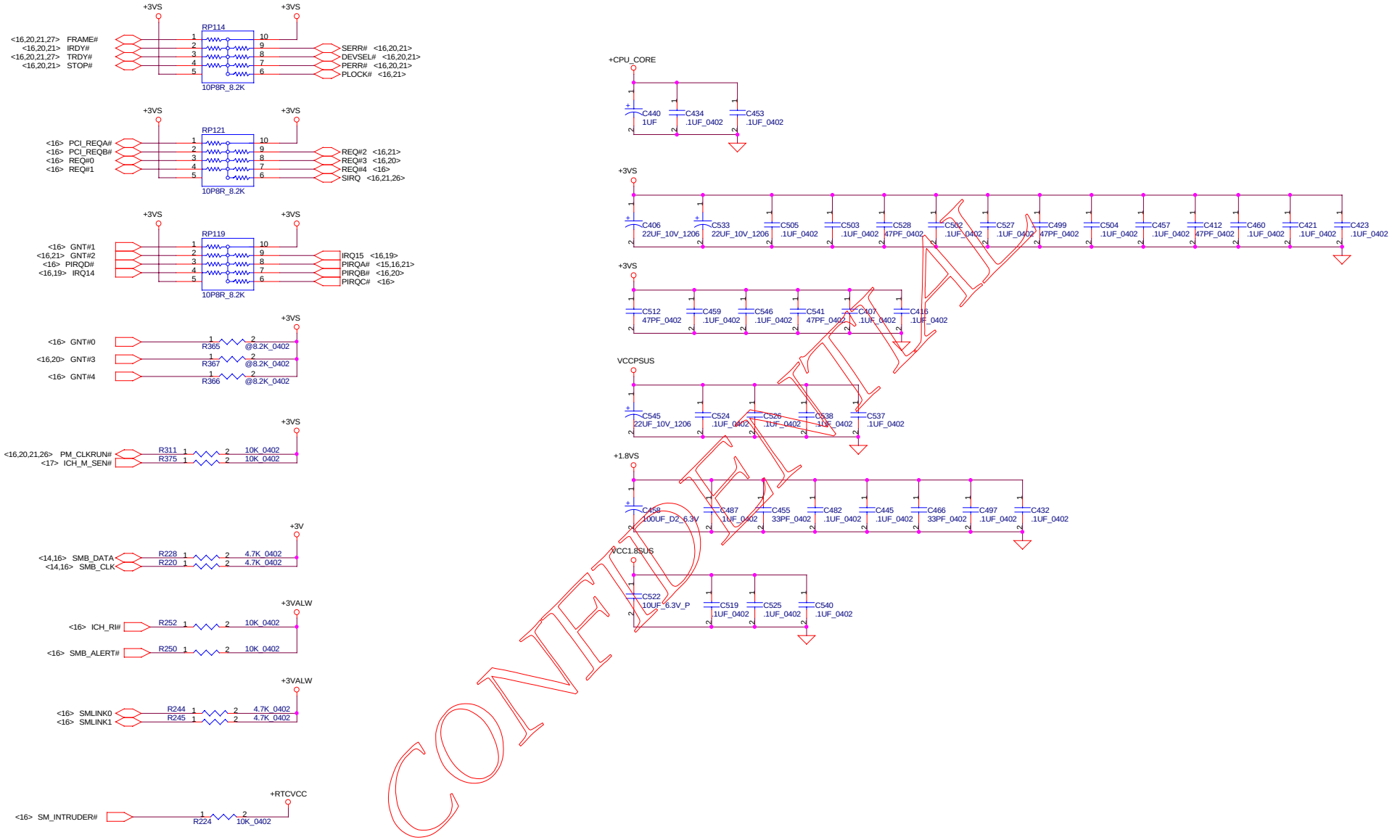
Compal Electronics, Inc.
Intel ICH3-M
Size
Document Number
ADY13 LA-1271
Rev 0.1
Date: Monday, September 10, 2001
Sheet 17 of 37



Compal Electronics, Inc.	
Title	ICH3-M Decoupling & Pull-Up
Size	Document Number: ADY13 LA-1271
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Date:	Monday, September 10, 2001
Sheet	18 of 37

HDD Connector

<17> PDD[0..15] — PDD[0..15]

Correct HDD pin define ,pls update layout

JP18

<17> PIDERST# — PDD7 PDD6 PDD5 PDD4 PDD3 PDD2 PDD1 PDD0 — PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15

R198 @10K_0402

<17> PDDREQ — PDDREQ

<17> PDIOW# — PDIOW#

<17> PDIOR# — PDIOR#

<17> PDIORDY — PDIORDY

RPDDACK# — RIRQ14

PCSEL — R188 470_0402

<17> PDA1 — PDA2 <17>

<17> PDA0 — PDCS3# <17>

<17> PDCS1# — PHDD_LED#

+5VSHDD — +5VSHDD

HH99221-S6-HDDCON

Placea caps. near HDD CONN.

+5VSHDD

C369 1000PF_0402 — C367 10UF_16V_1206 — C366 10UF_16V_1206 — C134 1UF_25V_0805 — C136 .1UF_0402

Layout Note: +5VSHDD trace width 60 mil

+3VS — R193 4.7K_0402 — PDIORDY

<17> PDDACK# — R192 22_0402 — RPDDACK#

<16,18> IRQ14 — R191 22_0402 — RIRQ14

PDDREQ — R189 @5.6K_0402 — C365 33PF_0402

CD-ROM Connector

<17> SDD[0..15] — SDD[0..15]

C280 47PF_0402

C333 47PF_0402 — CD_AGND <23>

<23> INT_CD_L — INT_CD_R <23> — C337 47PF_0402

<17> SIDERST# — SIDERST#

JP15

SDD7 SDD6 SDD5 SDD4 SDD3 SDD2 SDD1 SDD0 — SDD8 SDD9 SDD10 SDD11 SDD12 SDD13 SDD14 SDD15

R51 @10K_0402

SDDREQ <17> — SDDREQ

<17> SDIOW# — SDIOW# — SDIOR# <17>

<17> SDIORDY — SDIORDY

RSDDACK# — RSDDACK#

RIRQ15 — RIRQ15

<17> SDA1 — PDIAG# — R148 100K_0402 — +5VS

<17> SDA0 — SDA2 <17>

<17> SDCS1# — SDCS3# <17>

SHDD_LED# — W=80mils

+5VS — +5VS

C271 .1UF_0402

SEC_CSEL

R139 470_0402

CD-ROM CONN.

+3VS — R151 4.7K_0402 — SDIORDY

<17> SDDACK# — R152 22_0402 — RSDDACK#

<16,18> IRQ15 — R149 22_0402 — RIRQ15

SDDREQ — R155 @5.6K_0402 — C277 33PF_0402

Placea caps. near CDROM CONN.

+5VS

C258 1000PF_0402 — C257 .1UF_0402 — C110 1UF_25V_0805 — C96 10UF_16V_1206

+5VS

C262 1000PF_0402 — C263 .1UF_0402 — C112 1UF_25V_0805 — C116 10UF_16V_1206

+12VALW — R176 100K_0402 — +5VS — Q23 SI2301DS — +5VSHDD

<16> PIDEPWR — Q22 2N7002 — R178 150K — C359 .01UF_0402

SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

S 3 2 G

D 1

FDD Connector

+5VS

JP24

<26> INDEX# — INDEX# — +5V INDEX +5V DRIVE SELECT +5V DISK CHANGE NC READY DENSITY OUT MOTOR ON NC DIRECTION DENSITY 2 STEP GND / NC WRITE DATA GND WRITE GATE GND TRACK 00 NC / GND WRITE PROTECT GND READ DATA GND SIDE 1 SELECT

<26> DRV0# — DRV0#

<26> DISKCHG# — DISKCHG#

<26> MTR0# — MTR0#

3MODE# 11

<26> FDDIR# — FDDIR#

3MODE# 13

<26> STEP# — STEP#

<26> WDATA# — WDATA#

<26> WGATE# — WGATE#

<26> TRK0# — TRK0#

<26> WRPRT# — WRPRT#

<26> RDATA# — RDATA#

<29> FDD_PRES# — FDD_PRES#

<26> HDSEL# — HDSEL#

ACES 85201-2605-FDDCON

Placec caps. near FDD CONN.

+5VS

C536 .1UF_0402 — C529 10UF_16V_1206 — C523 1UF_25V_0805 — C520 .1UF_0402

<26> 3MODE# — 3MODE# — R336 @0_0402 — 3MODE# 11 — R335 0_0402 — 3MODE# 13

DISKCHG# INDEX# WRPRT# TRK0# — RP120 8P4R_1K — +5VS

WDATA# WGATE# HDSEL# FDDIR# — RP115 10P8R_1K — STEP# MTR0# RDATA# DRV0# — +5VS

+5VS — R62 100K_0402 — R187 100K_0402

PHDD_LED# — U23D 74HCT08

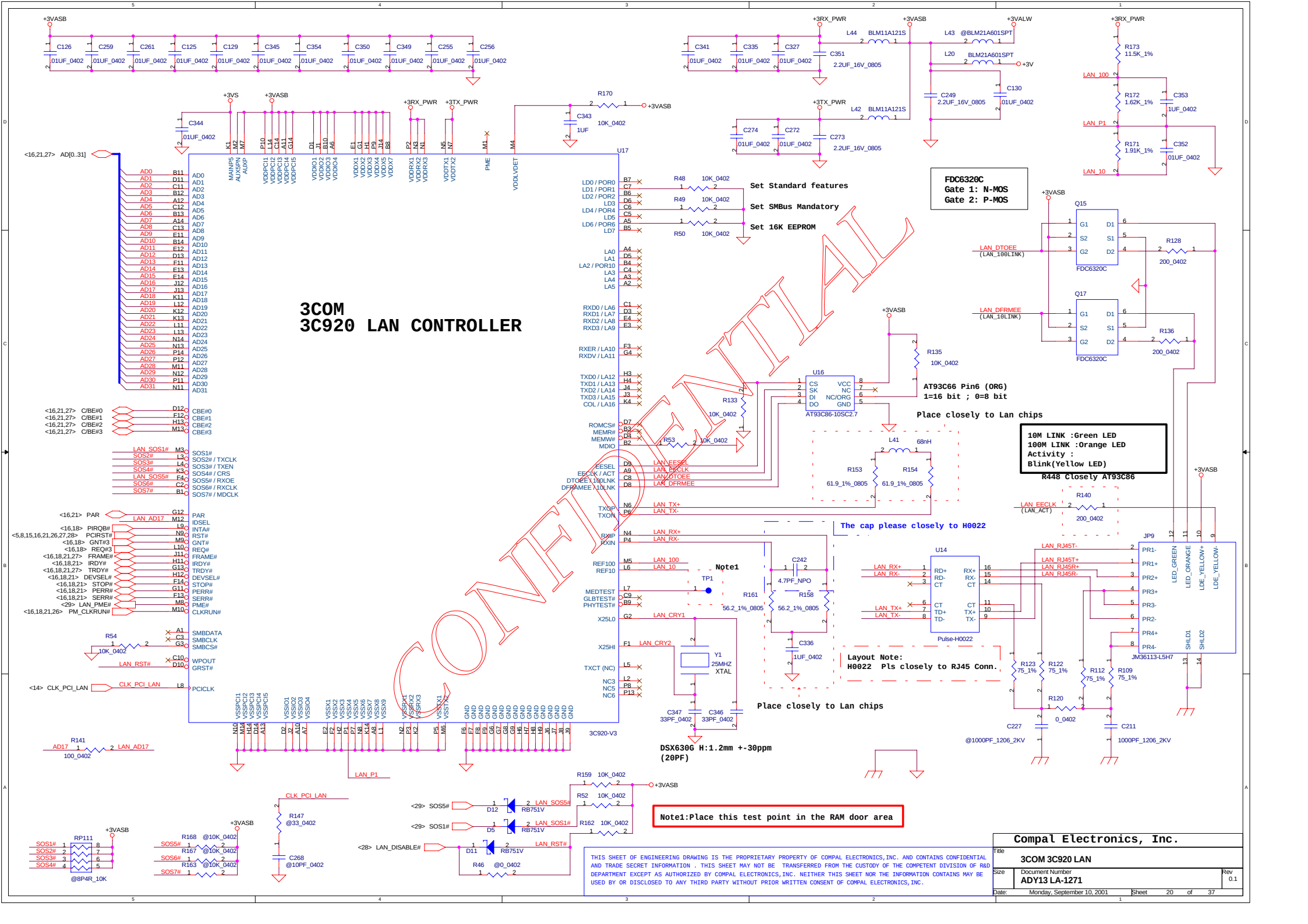
SHDD_LED#

DRV0#

+5VS — C135 .1UF_0402 — U23A 74HCT08 — ACT_LED# — ACT_LED# <27>

Compal Electronics, Inc.		
Title: IDE/FDD/CD-ROM Module		
Size	Document Number: ADY13 LA-1271	Rev: 0.1
Date: Monday, September 10, 2001	Sheet 19 of 37	

3COM
3C920 LAN CONTROLLER

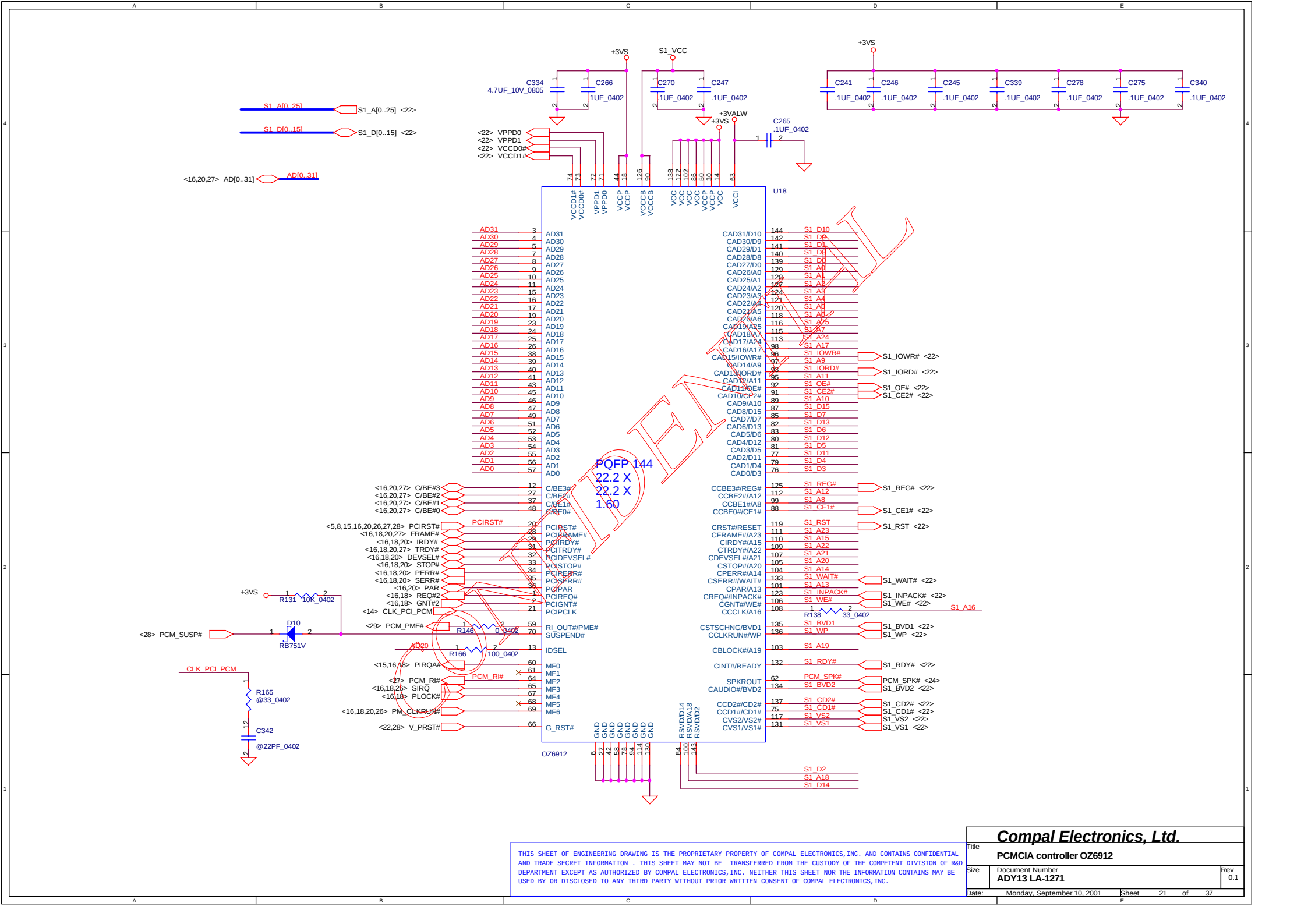


Compal Electronics, Inc.

Title: 3COM 3C920 LAN

Size: | Document Number: ADY13 LA-1271 | Rev: 0.1

Date: Monday, September 10, 2001 | Sheet 20 of 37


+3VS
S1_VCC
+3VALW
C334
4.7UF_10V_0805
C266
.1UF_0402
C270
.1UF_0402
C247
.1UF_0402
C241
C246
C245
C339
C278
C275
C340
C265
.1UF_0402
S1_A[0..25]
S1_A[0..25] <22>
S1_D[0..15]
S1_D[0..15] <22>
<22> VPPD0
<22> VPPD1
<22> VCCD0#
<22> VCCD1#
<16,20,27> AD[0..31]
AD[0..31]
U18
PQFP 144
22.2 X
22.2 X
1.60
OZ6912
R131 10K_0402
R146 0_0402
R166 100_0402
R165 @33_0402
C342 @22PF_0402
R138 33_0402
D10
RB751V
<28> PCM_SUSP#
<29> PCM_PME#
CLK_PCI_PCM
PCM_RI#
AD20
S1_IOWR# <22>
S1_IORD# <22>
S1_OE# <22>
S1_CE2# <22>
S1_REG# <22>
S1_CE1# <22>
S1_RST <22>
S1_WAIT# <22>
S1_INPACK# <22>
S1_WE# <22>
S1_BVD1 <22>
S1_WP <22>
S1_RDY# <22>
PCM_SPK# <24>
S1_BVD2 <22>
S1_CD2# <22>
S1_CD1# <22>
S1_VS2 <22>
S1_VS1 <22>
S1_A16
S1_D2
S1_A18
S1_D14
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Compal Electronics, Ltd.
Title
PCMCIA controller OZ6912
Size
Document Number
ADY13 LA-1271
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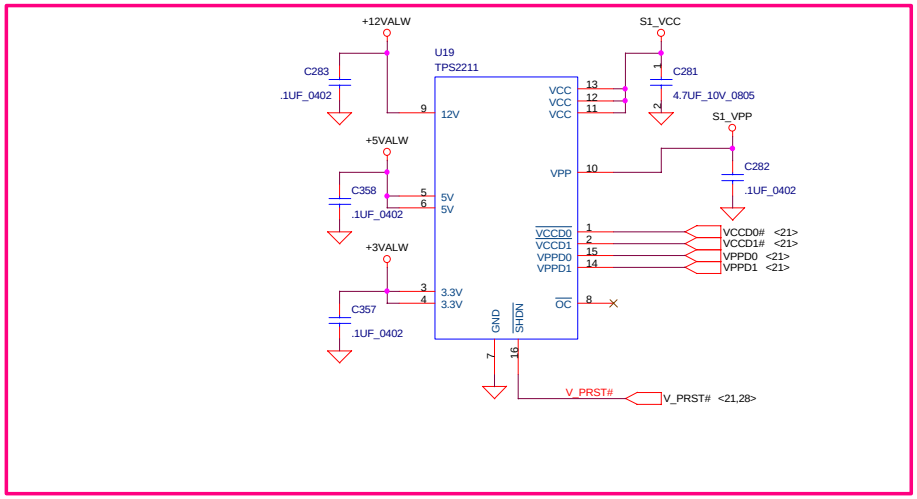
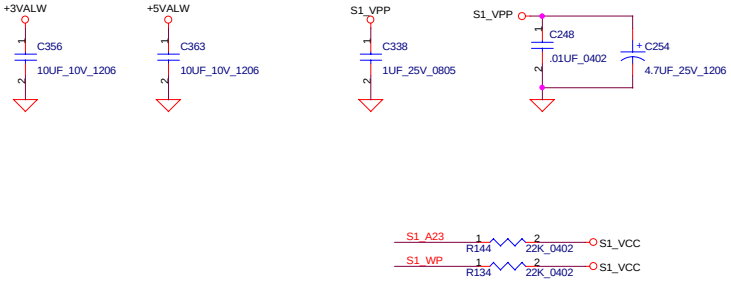
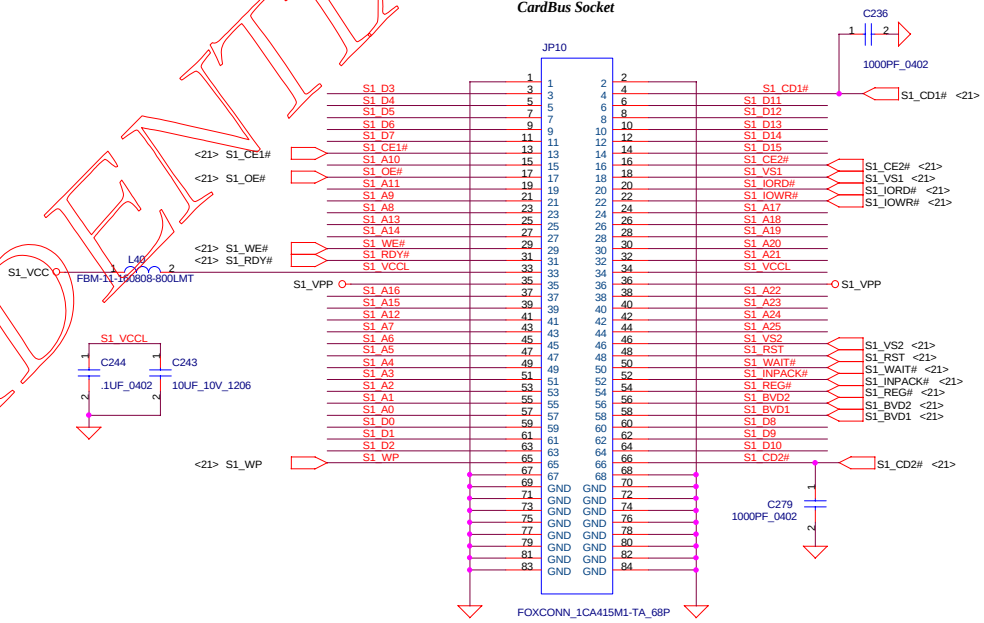
0.1
Date: Monday, September 10, 2001
Sheet 21 of 37

PCMCIA Power Controller

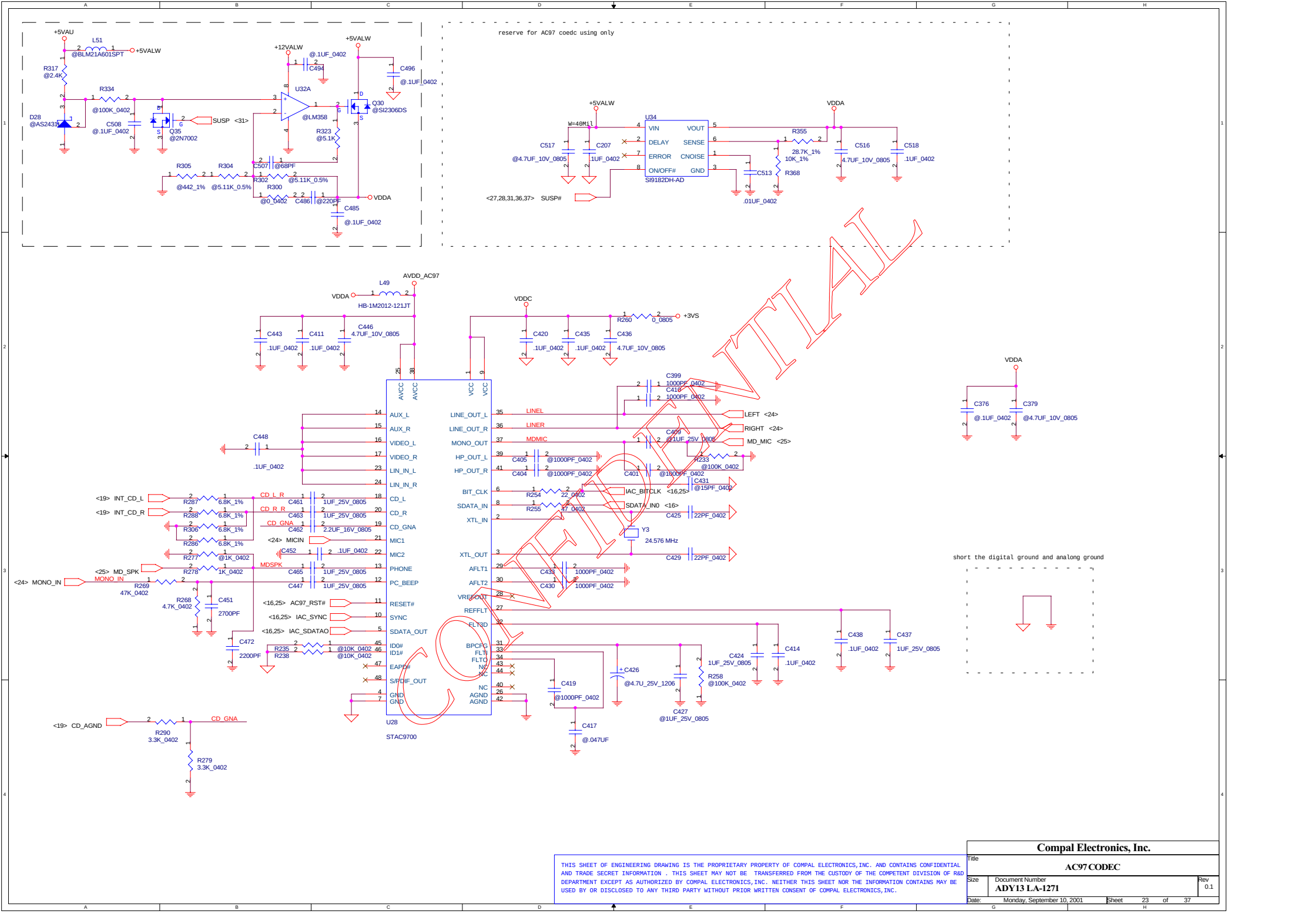




CardBus Socket

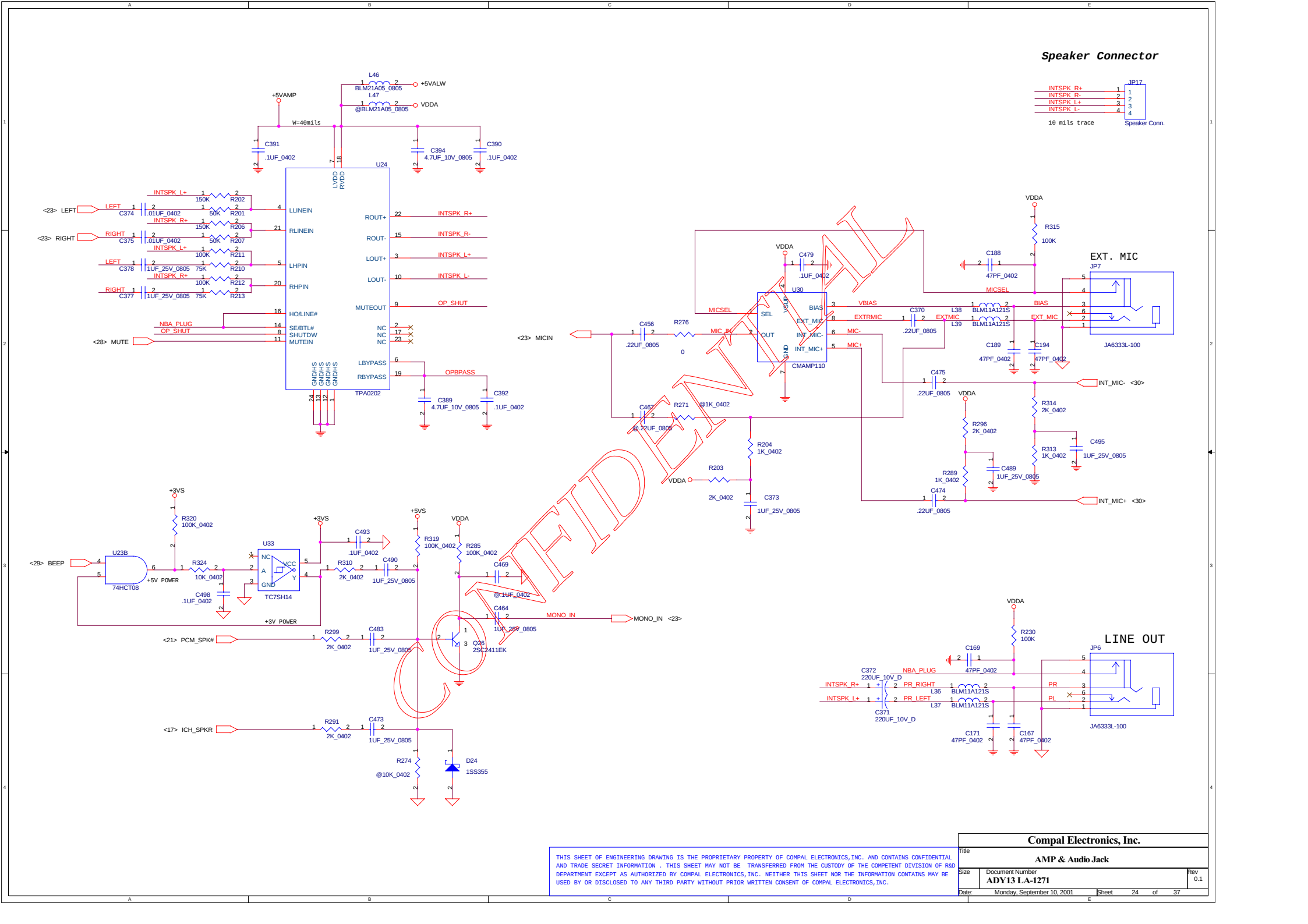


Compal Electronics, Inc.		
Title: CardBus Socket		
Size	Document Number: ADY13 LA-1271	Rev: 0.1
Date: Monday, September 10, 2001	Sheet 22 of 37	



Compal Electronics, Inc.

Title	AC97 CODEC	
Size	Document Number ADY13 LA-1271	Rev 0.1
Date: Monday, September 10, 2001	Sheet 23 of 37	

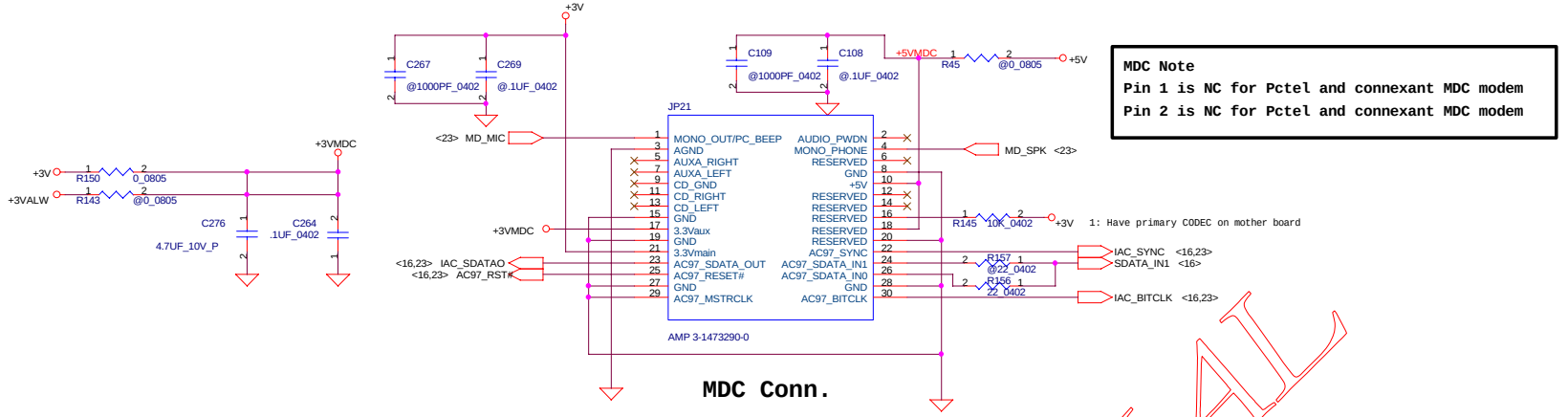


Compal Electronics, Inc.

Title: **AMP & Audio Jack**

Size	Document Number	Rev
	ADY13 LA-1271	0.1

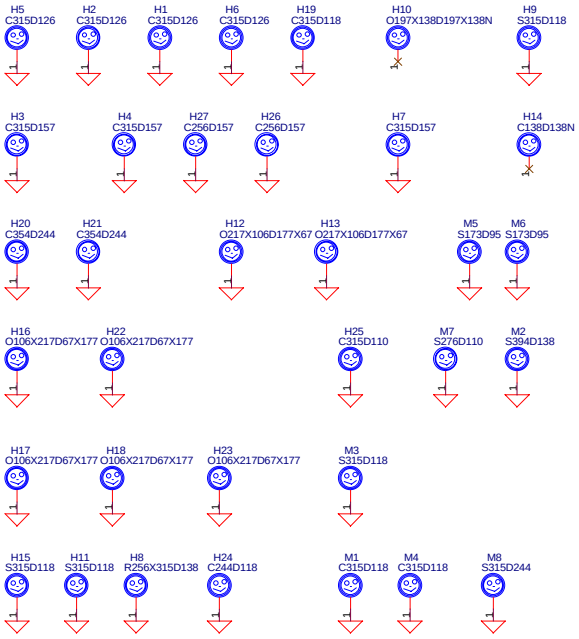
Date: Monday, September 10, 2001 Sheet 24 of 37



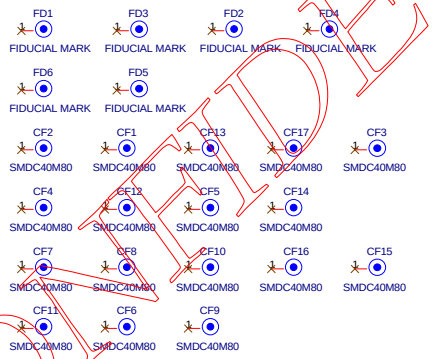
MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

MDC Conn.

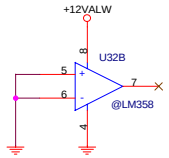
Screw Hole

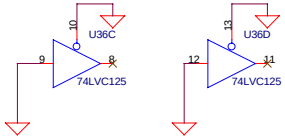


Fiduial Mark

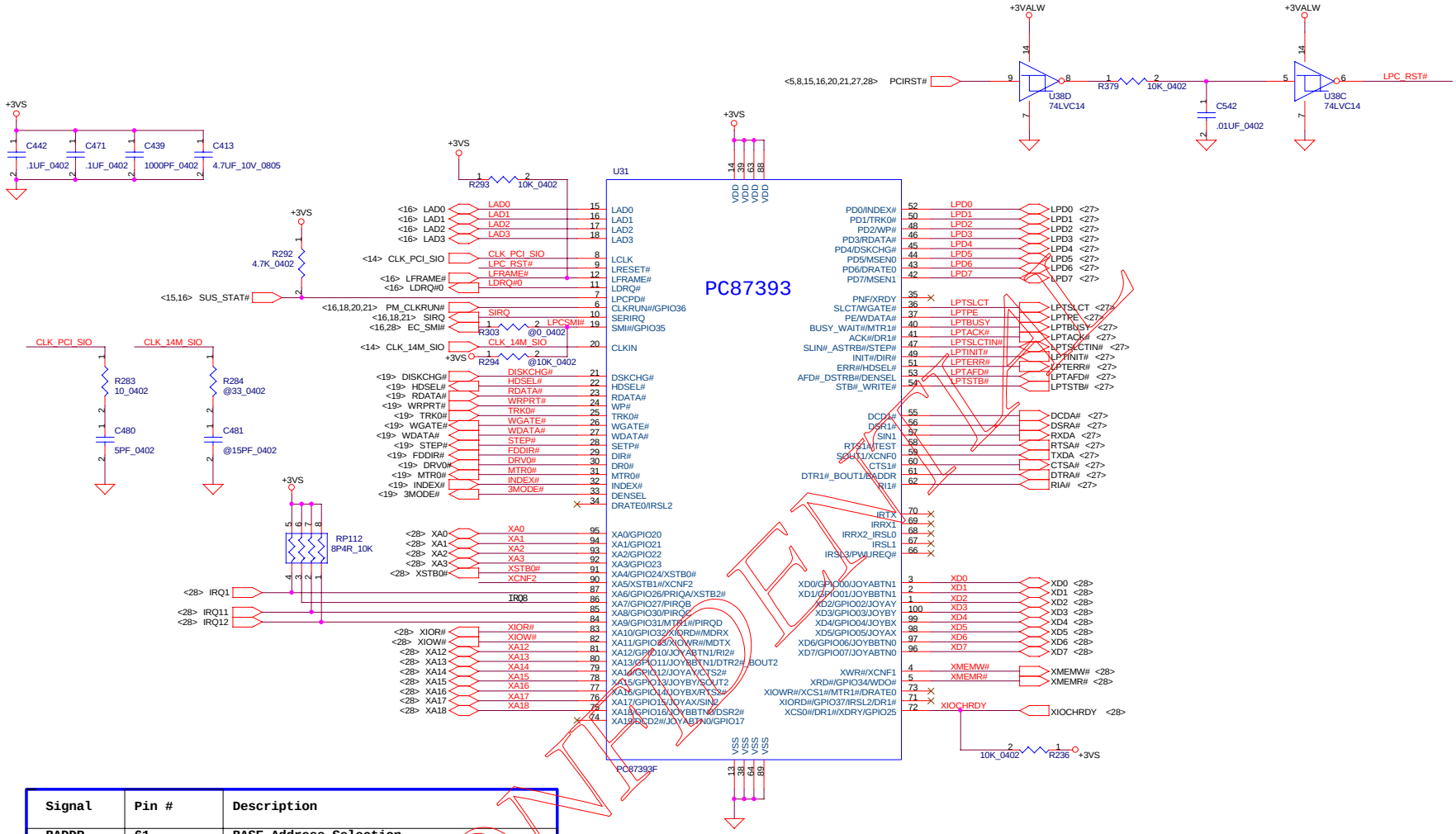


Spare Logic Gate





Compal Electronics, Inc.		
Title: MDC connector / Skew Hole		
Size	Document Number: ADY13 LA-1271	Rev: 0.1
Date: Monday, September 10, 2001	Sheet 25 of 37	



Signal	Pin #	Description
BADDR	61	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F
TEST	58	"0": Normal (Default) "1": Test Mode
XCNF[2:0]	90, 4, 59	

2	1	0	Function
x	0	0	No BIOS
x	0	1	Normal Mode. XRDY disabled
(default) 0	1	0	Latch Mode. XA12-19, XRDY enabled
1	1	0	Latch Mode. GPIO10~17,XRDY enabled
0	1	1	Latch Mode. XA12-19, XRDY disabled
1	1	1	Latch Mode. GPIO10~17,XRDY disabled

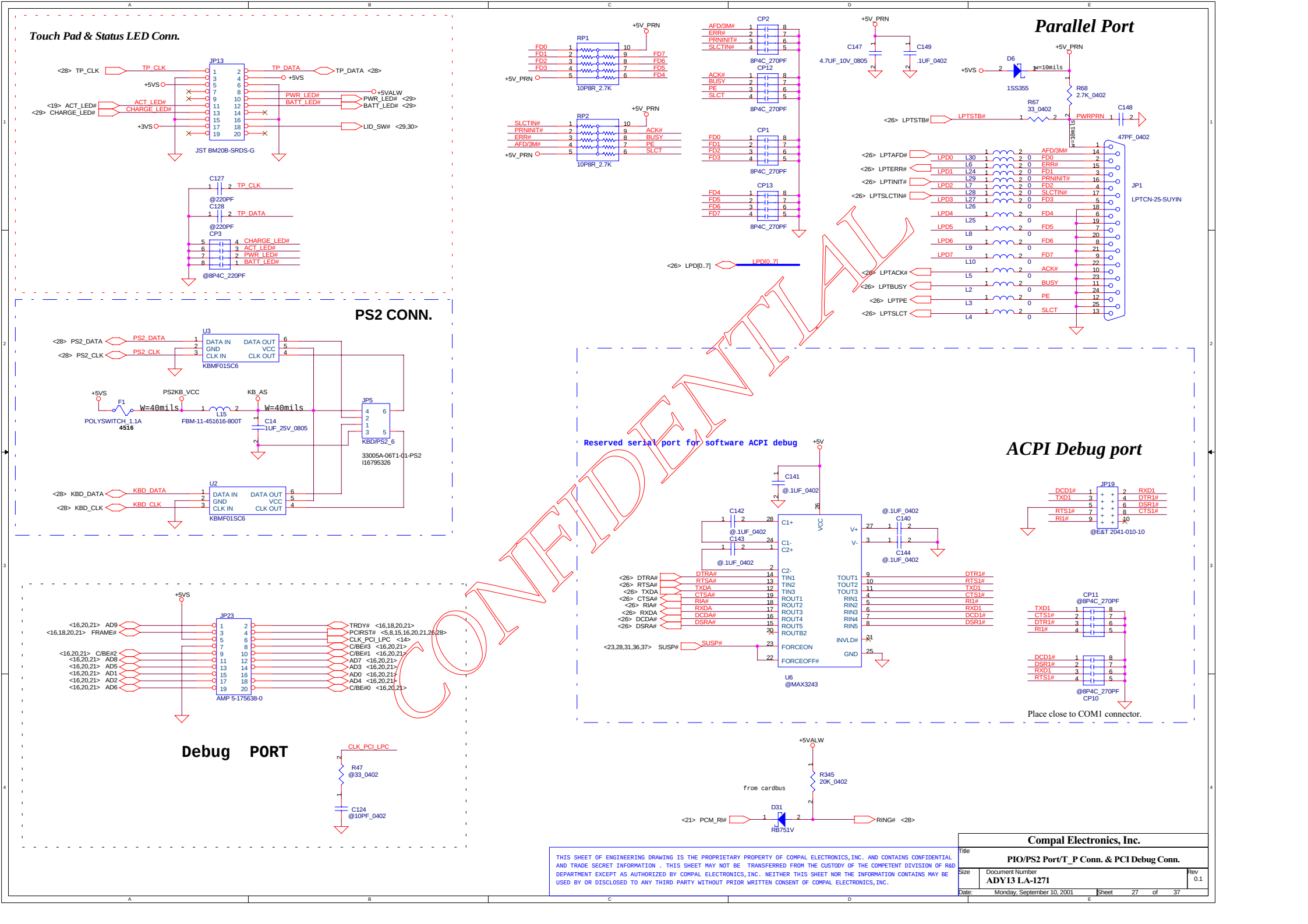
* 1 ROM SOLUTION

Compal Electronics, Inc.

Title: LPC Super I/O NS PC87393

Size: | Document Number: ADY13 LA-1271 | Rev: 0.1

Date: Monday, September 10, 2001 | Sheet 26 of 37



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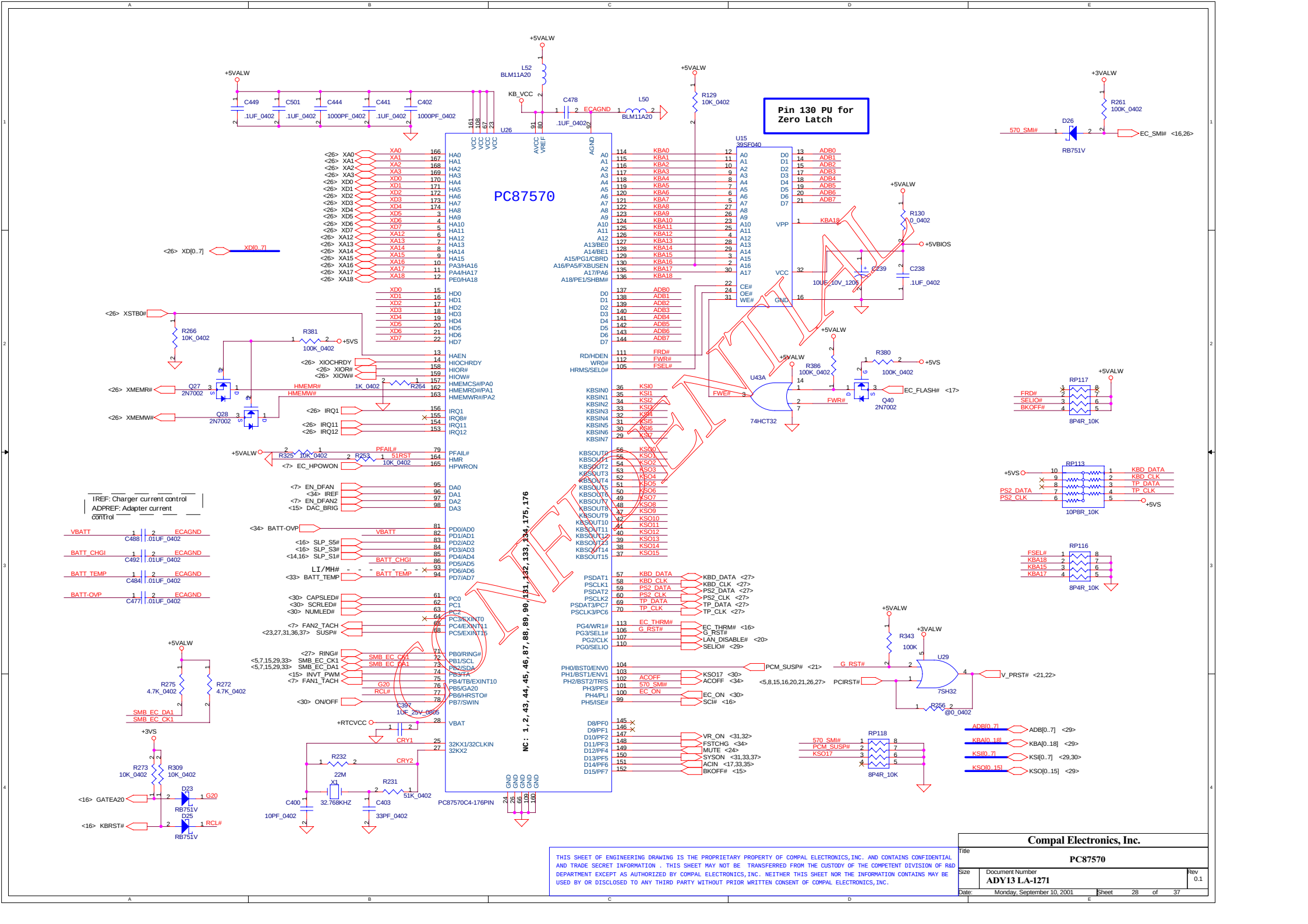
Compal Electronics, Inc.

Title	PIO/PS2 Port/T_P Conn. & PCI Debug Conn.	
Size	Document Number ADY13 LA-1271	Rev 0.1
Date: Monday, September 10, 2001	Sheet 27 of 37	



Compal Electronics, Inc.

Title	PC87570	
Size	Document Number: ADY13 LA-1271	Rev: 0.1
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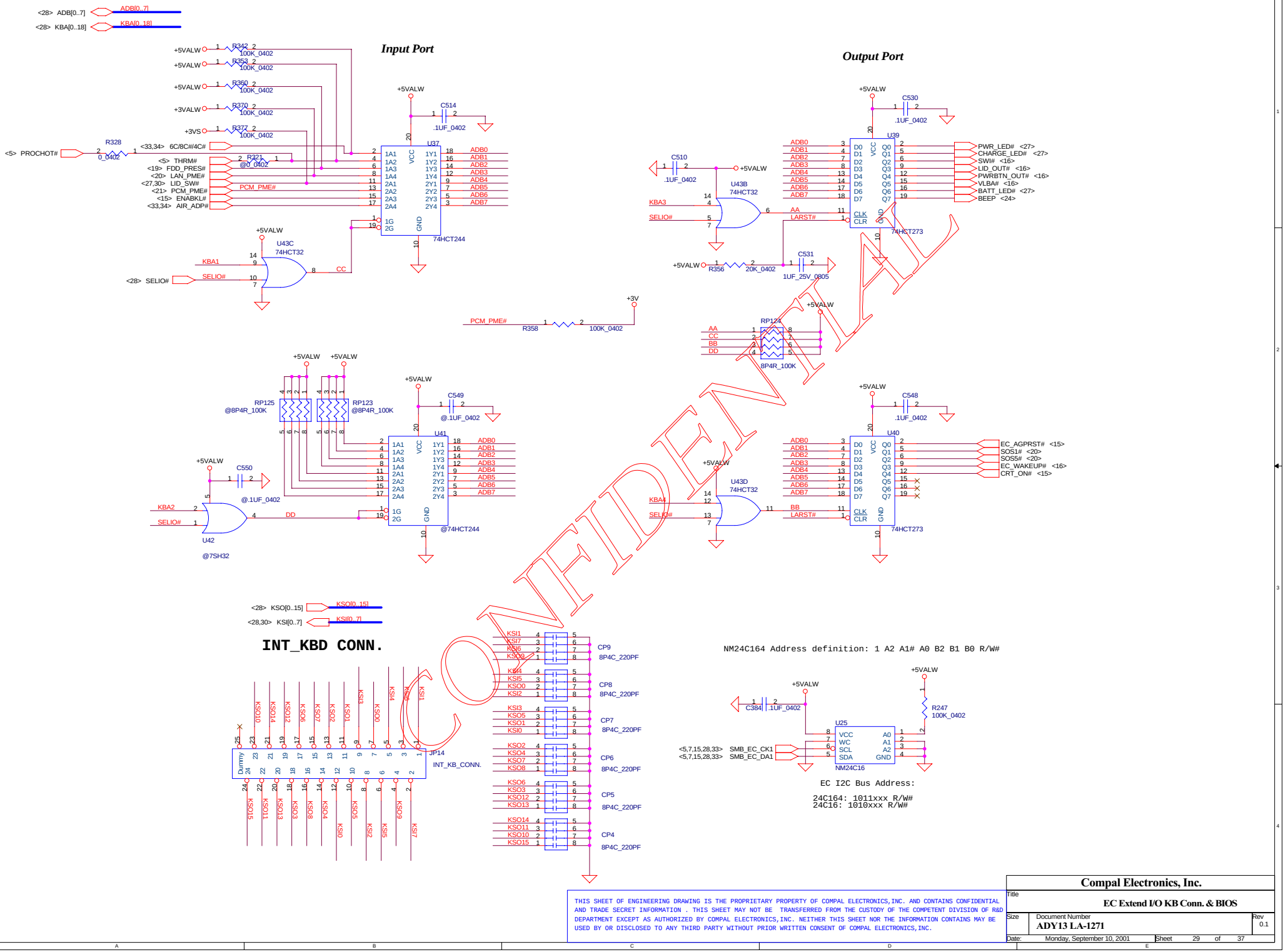

Compal Electronics, Inc.

Title	EC Extend I/O KB Conn. & BIOS	
Size	Document Number ADY13 LA-1271	Rev 0.1
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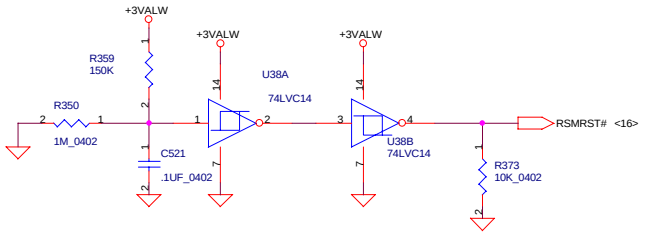
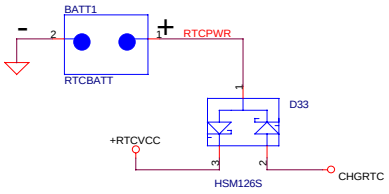
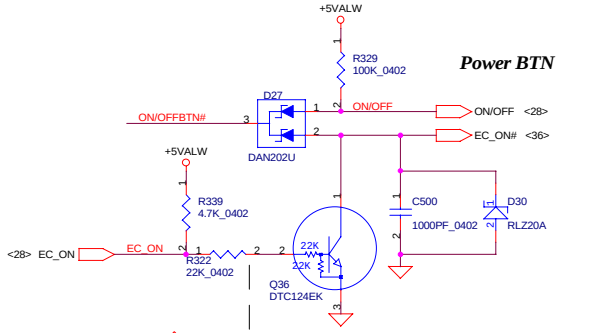
Power ON Circuit



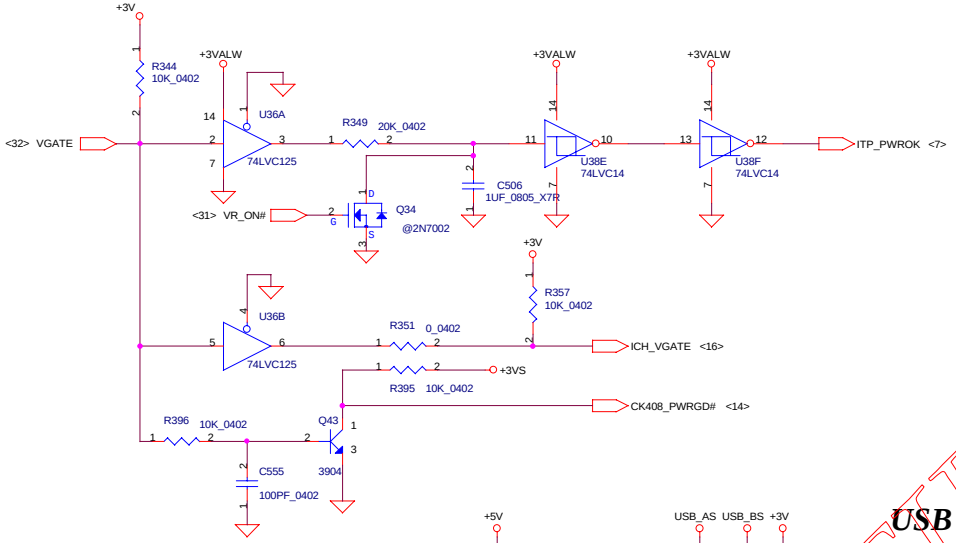
RTC Battery



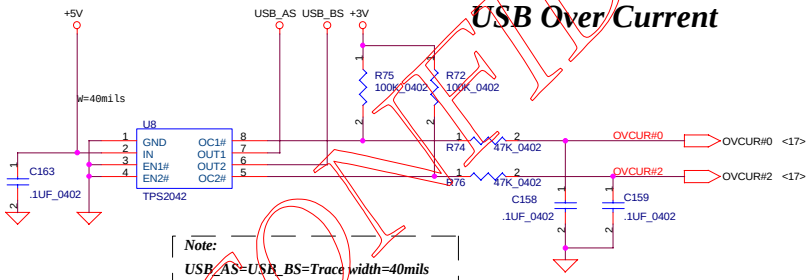
Power BTN



WHEN R=0,Vbe=1.35V
WHEN R=33K,Vbe=0.8V

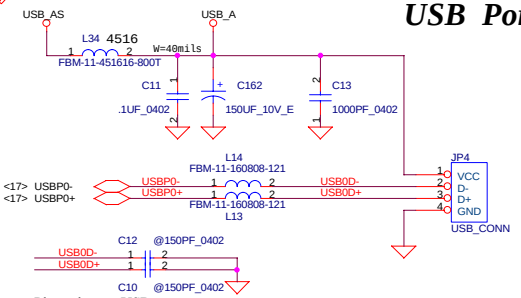


USB Over Current



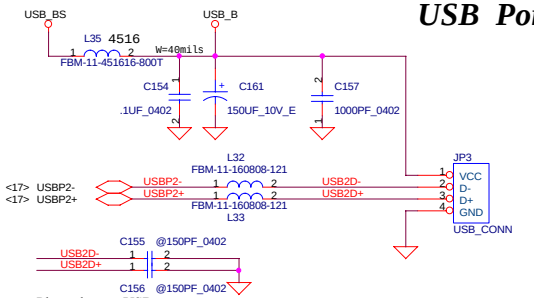
Note:
USB_AS=USB_BS=Trace width=40mils

USB Port 0



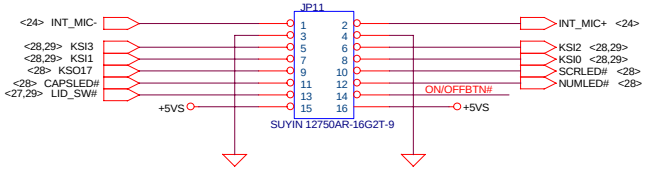
Place close to USB connector.

USB Port 1



Place close to USB connector.

LID Switch & Function Button



Compal Electronics, Inc.	
Title	Power OK/Reset/RTC battery/USB Conn.& Lid Switch
Size	Document Number: ADY13 LA-1271 — Rev: 0.1
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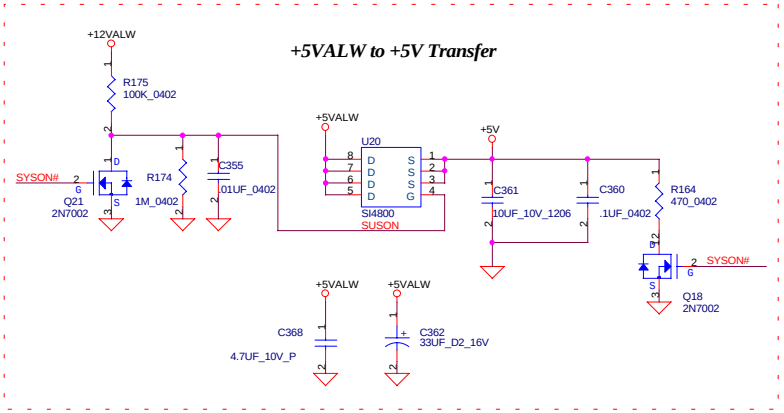
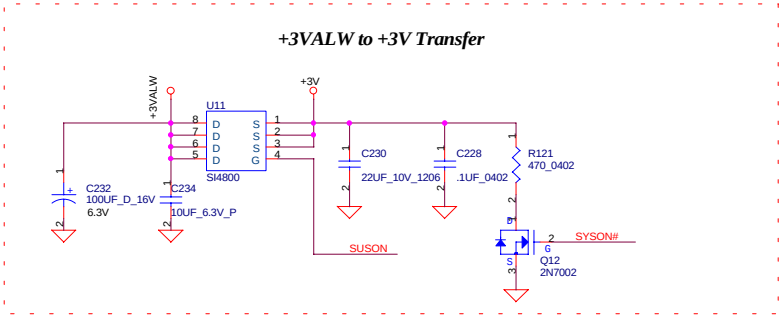
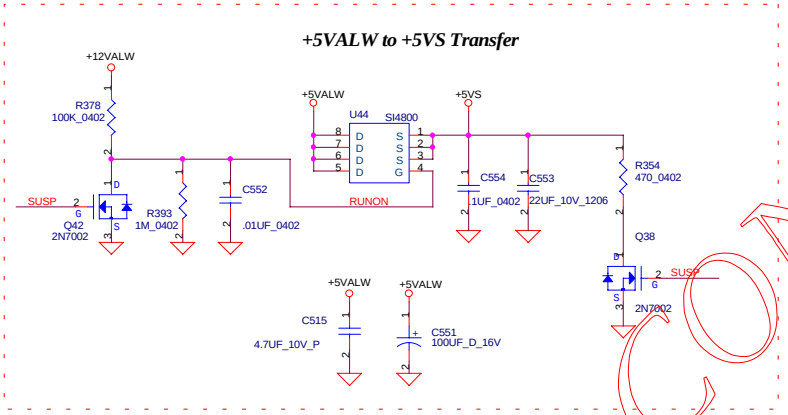
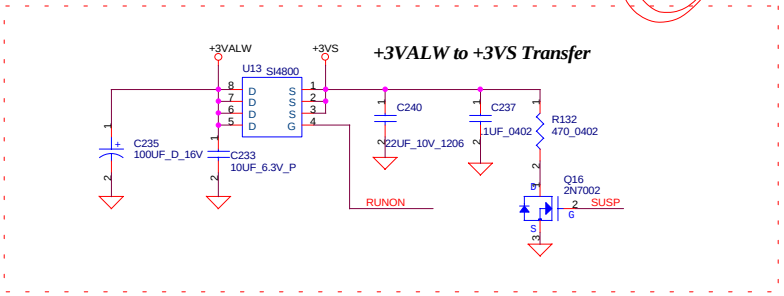
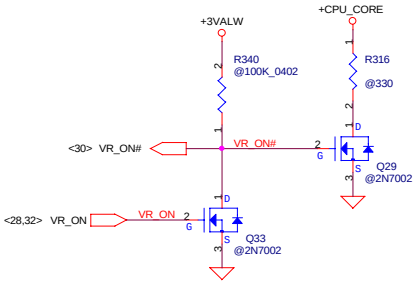


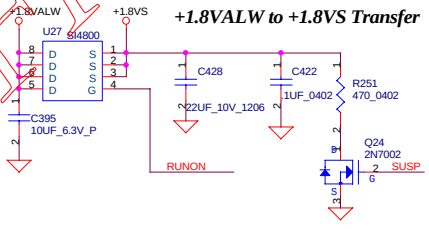


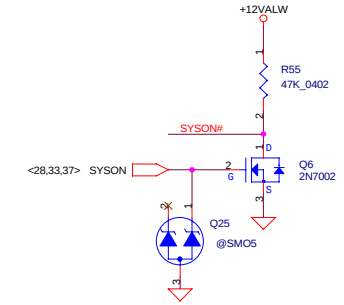


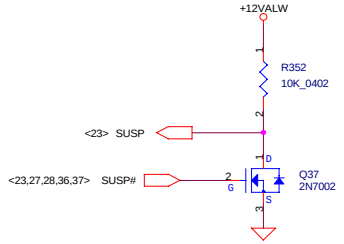




1.8VALW/+1.5VS Power direct provide







Compal Electronics, Inc.		
Title: DC/DC Circuit		
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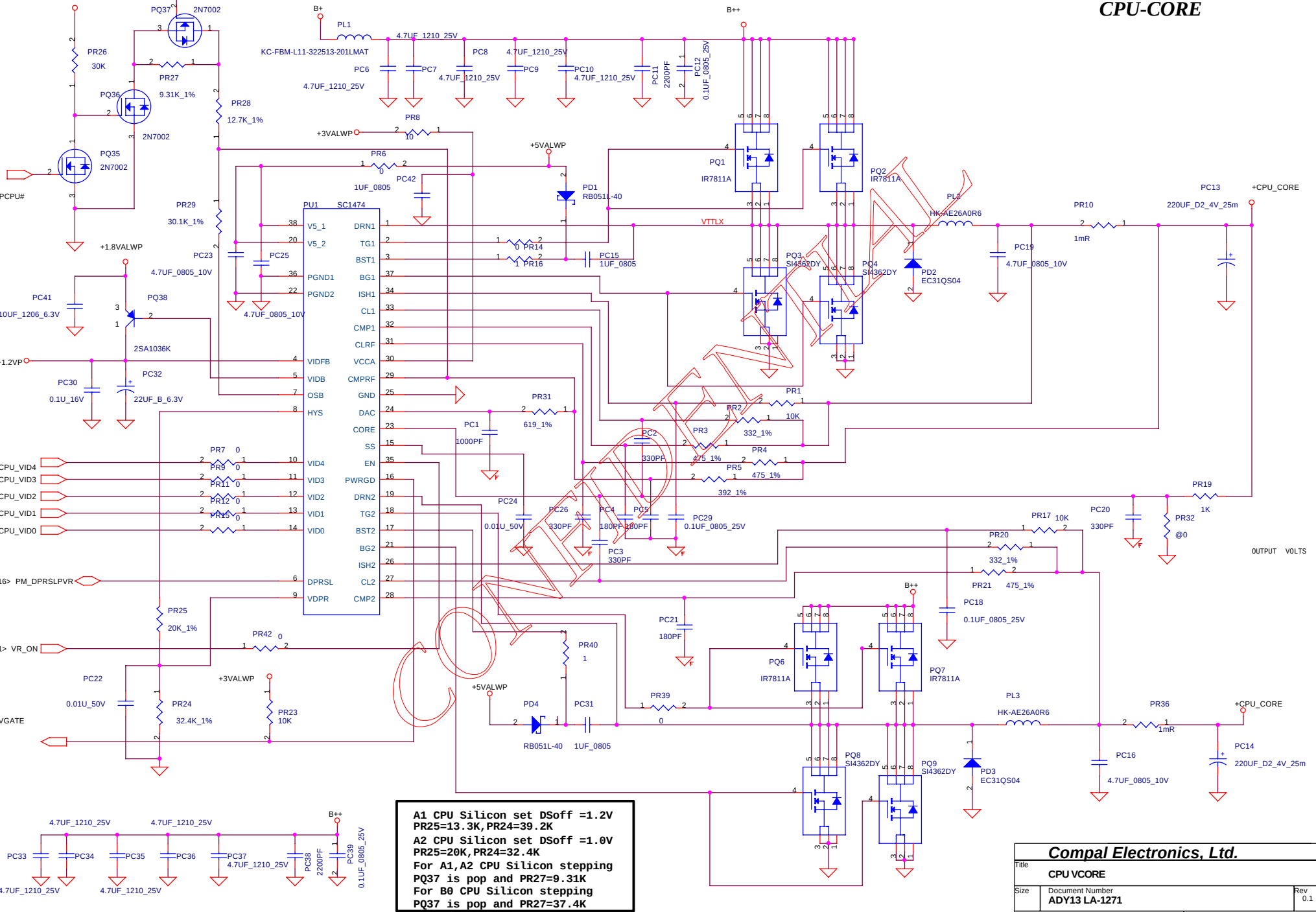
CPU-CORE



Compal Electronics, Ltd.		
Title: CPU VCORE		
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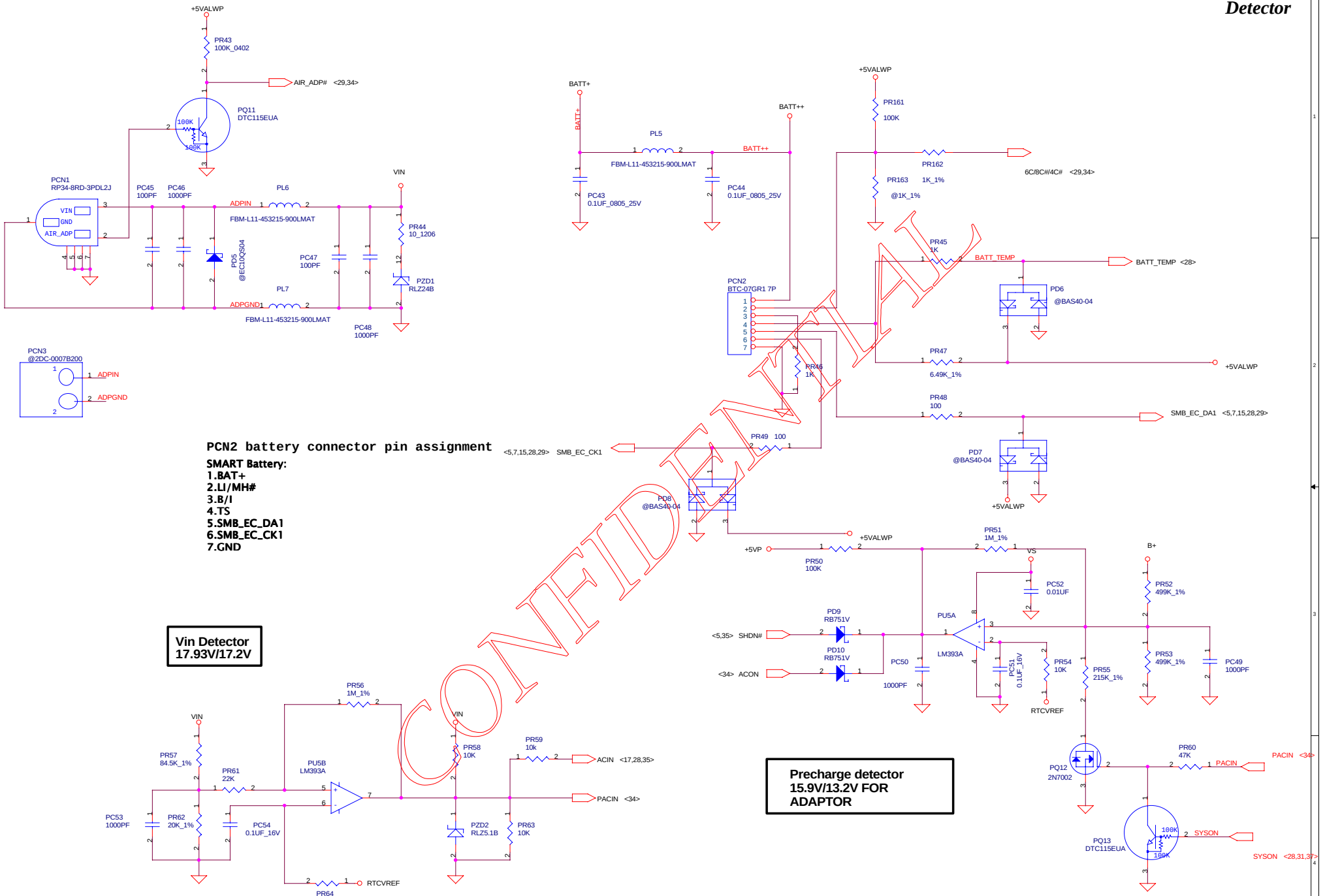
Detector



PCN2 battery connector pin assignment

SMART Battery:
1.BAT+
2.LI/MH#
3.B/I
4.TS
5.SMB_EC_DA1
6.SMB_EC_CK1
7.GND

Vin Detector 17.93V/17.2V

Precharge detector 15.9V/13.2V FOR ADAPTOR

Compal Electronics, Inc.		
Title: Detector		
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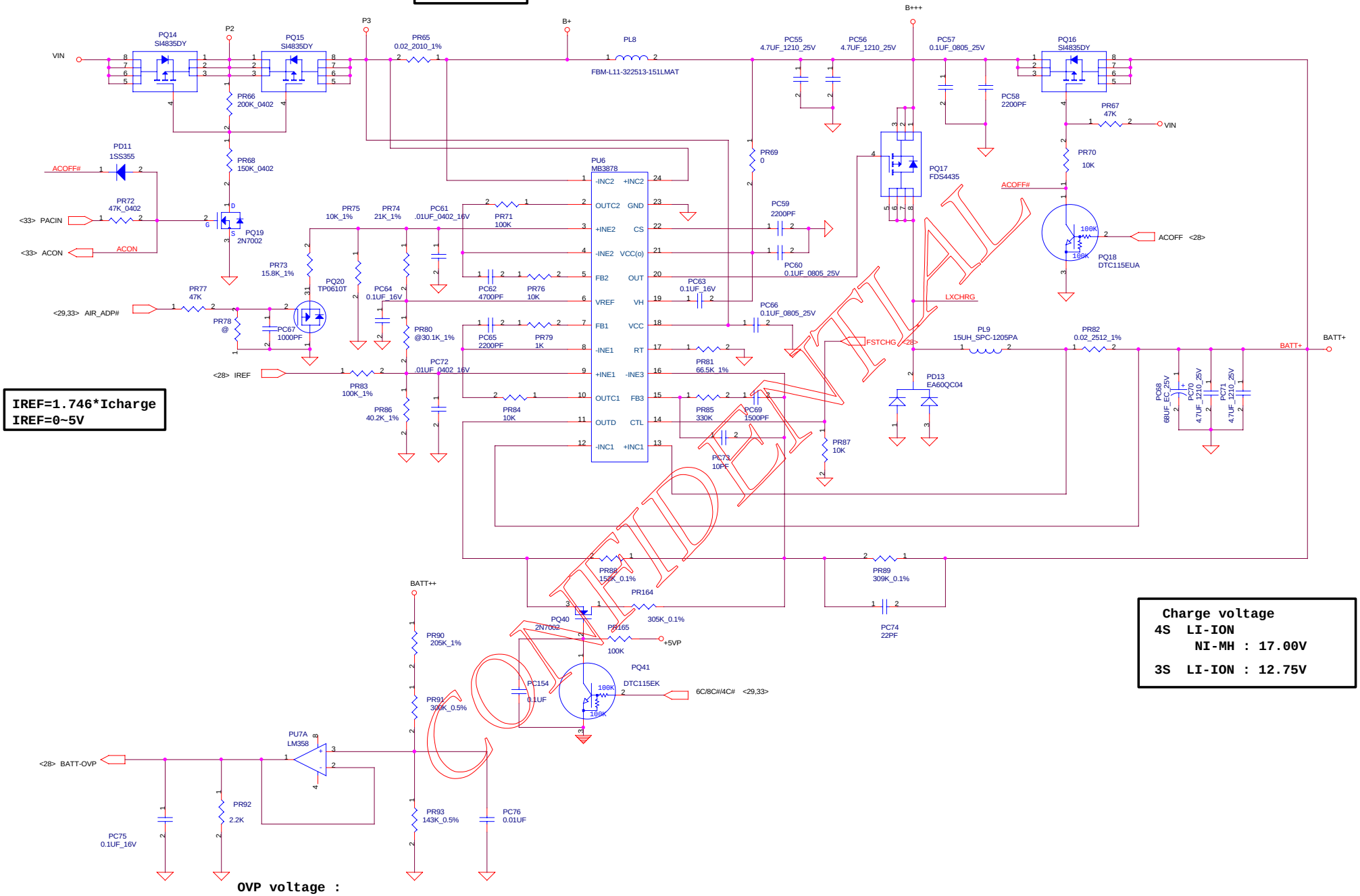
Charger

Iadp=0~3.22A
Iair=0~2.26A <-----Actually about 3A



IREF=1.746*Icharge
IREF=0~5V

Charge voltage
4S LI-ION
NI-MH : 17.00V
3S LI-ION : 12.75V

OVP voltage :
LI-4S :18.3V----BATT-OVP=4.04V
LI-3S :13.5V----BATT-OVP=3.82V
BATT-OVP=0.2206*BATT++

Compal Electronics, Inc.		
Title: Charger		
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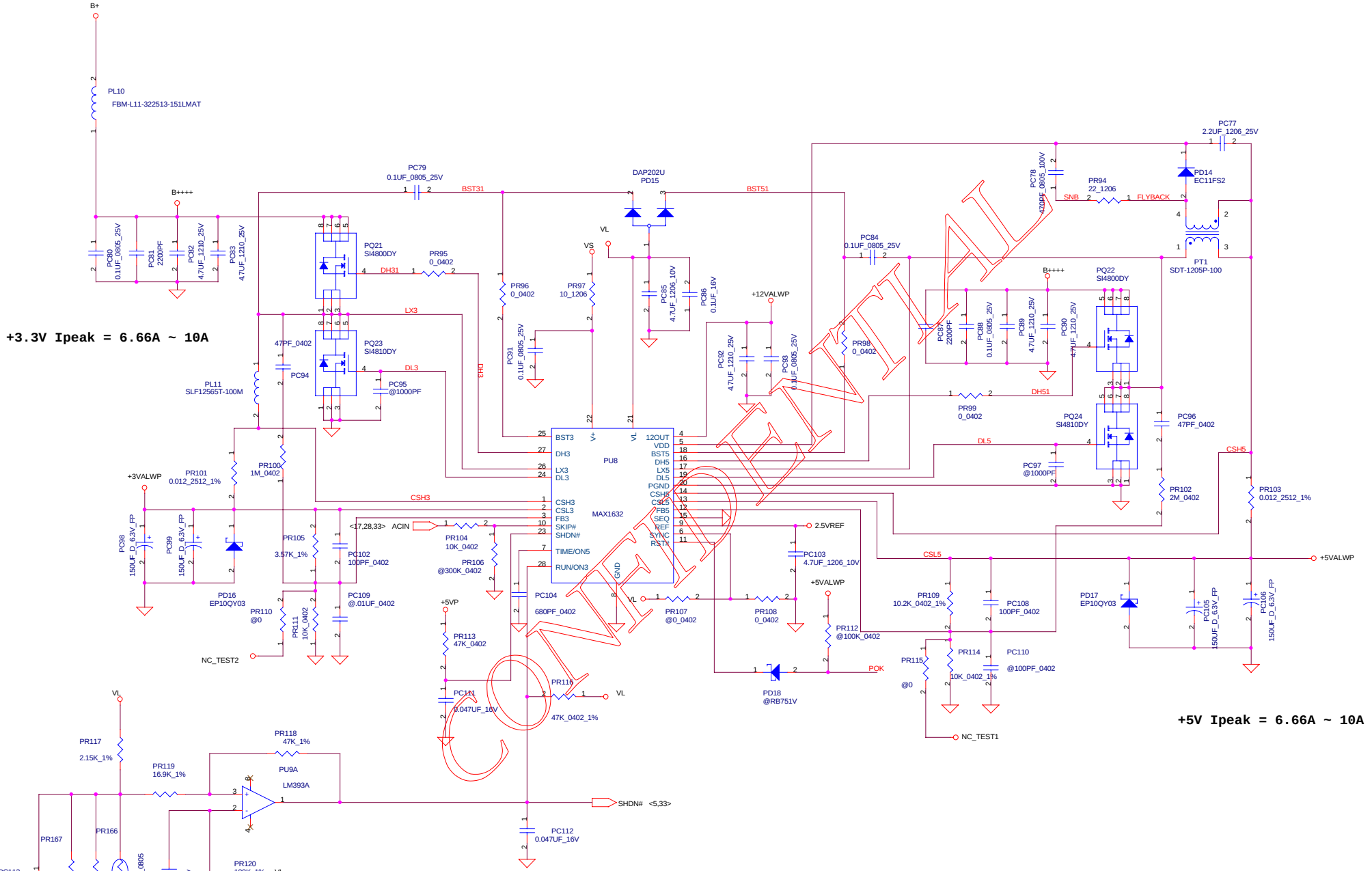
+3.3V/+5V/+12V



Compal Electronics, Inc.	
Title	+3.3V/+5V/+12V
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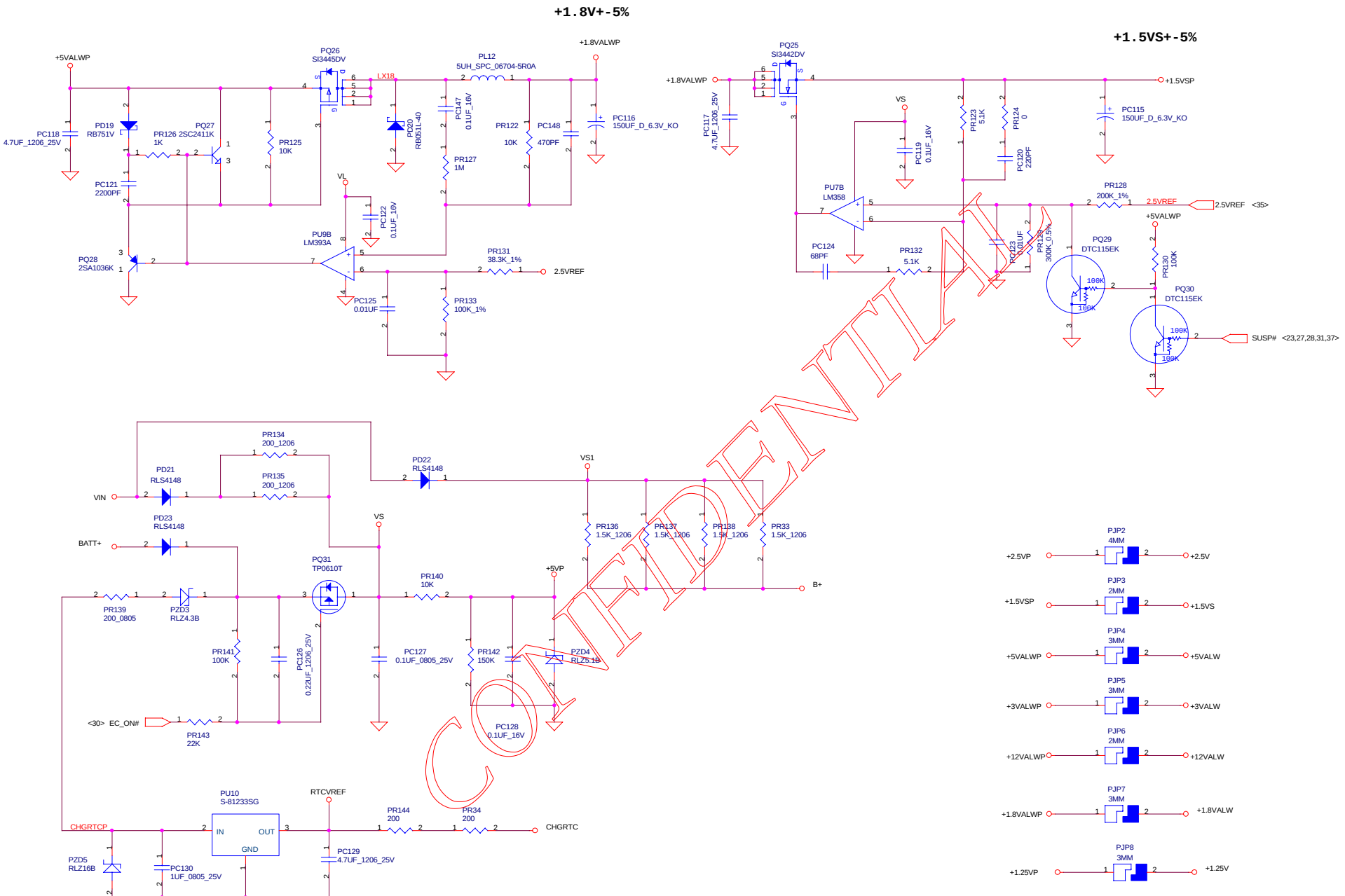
+1.8VALW/+1.5VS



Compal Electronics, Inc.		
Title: +1.8VALW		
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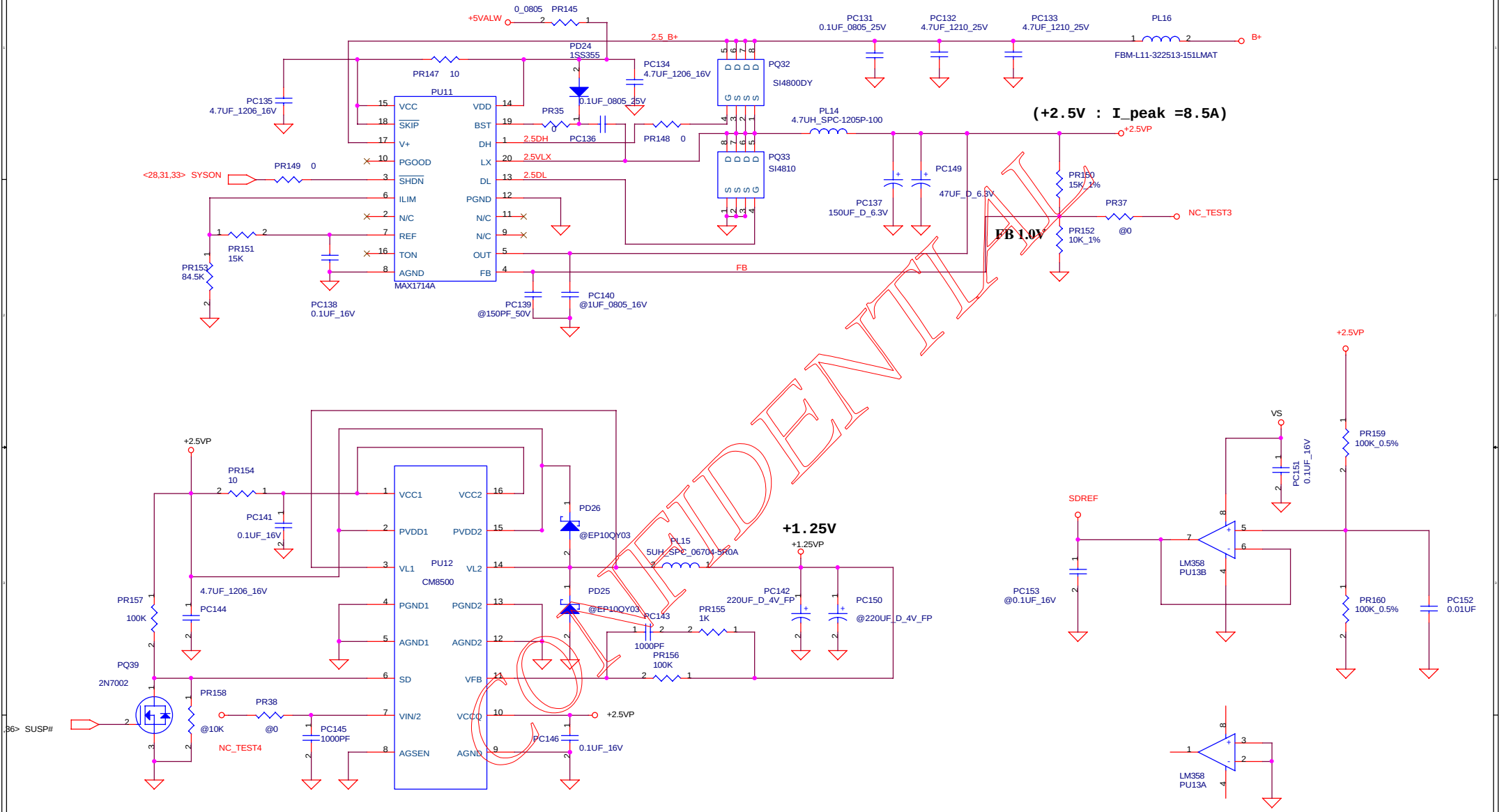

COMPAL ELECTRONICS, INC	
Title	DDR POWER 2.5V & 1.25V
Size: B	Document Number: ADY13 LA-1271
Rev: 0.1	
Date: Monday, September 10, 2001	Sheet 37 of 37