COMPAL CONFIDENTIAL

MODEL NAME : ***TOBAGO***

COMPAL P/N : ***45128331001/45128331002***

PCB NO : ***LA2151***

Revision : ***1.0 (DELL: A00)***

TOBAGO Schematics Document

uFCBGA/uFCPGA Mobile Dothan
Intel Alviso + ICH6M

2004-11-03

REV : 1.0 (DELL: A00)

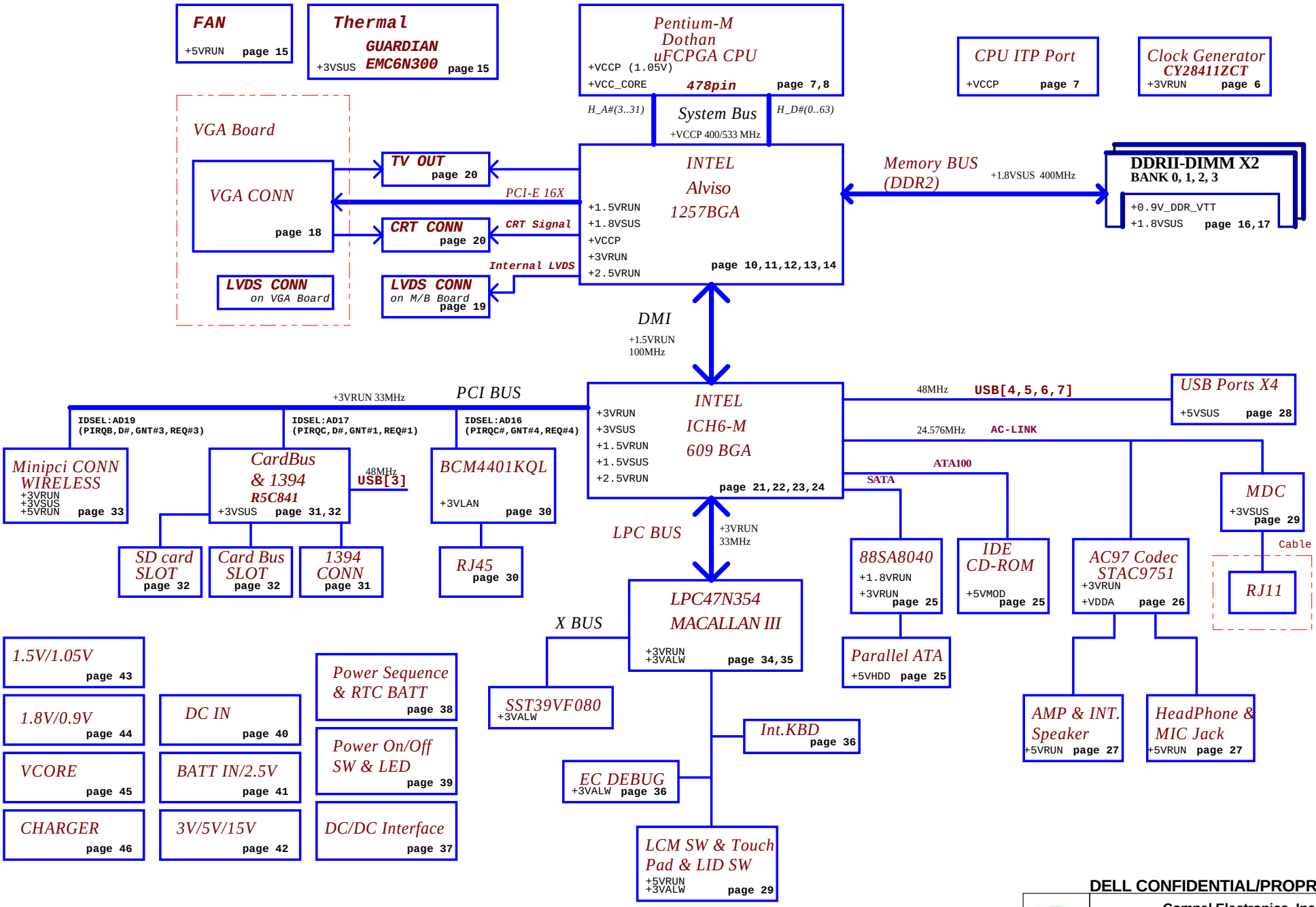
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: TOBAGO-LA2151 | Rev: 0.6

Date: Wednesday, November 03, 2004 | Sheet 1 of 51

Model : Tobago



Compal Electronics, Inc.		
Title: Block Diagram		
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Ceramic Capacitors :

0.1U_0402_6.3VXX

- Tolerance
- Temperature Characteristics
- Rated Voltage
- Package Size
- Value

Tantalum or Polymer Capacitors :

10U_D2_10VX_R45

- Low ESR Mark : 45 m ohm
- Tolerance
- Rated Voltage
- Package Size
- Value

Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NPO	COG	X6S	BJ	CH	CJ	CK	SH	SJ

H	I	J	K
UJ	UK	SL	X5S

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+-0.05PF	+-0.1PF	+-0.25PF	+-0.5PF	+-1PF	+-2%	+-3%	+-5%

K	M	N	P	Q	V	X	Z	
+-10%	+-20%	+-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

NOTE1:

@XX : Depop component

1@XX : Pop for Integrated Graphic

2@XX : Pop for External Graphic

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
LAN	AD16	4	C
MINI PCI	AD19	3	D,B

PM TABLE

State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +3VRUN +1.8VRUN +0.9V_DDR_VTT +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB TABLE

USB PORT#	DESTINATION
0	NC
1	NC
2	Blue tooth
3	PCMCIA
4,5	REAR
6,7	SIDE

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Title: Index and Config.

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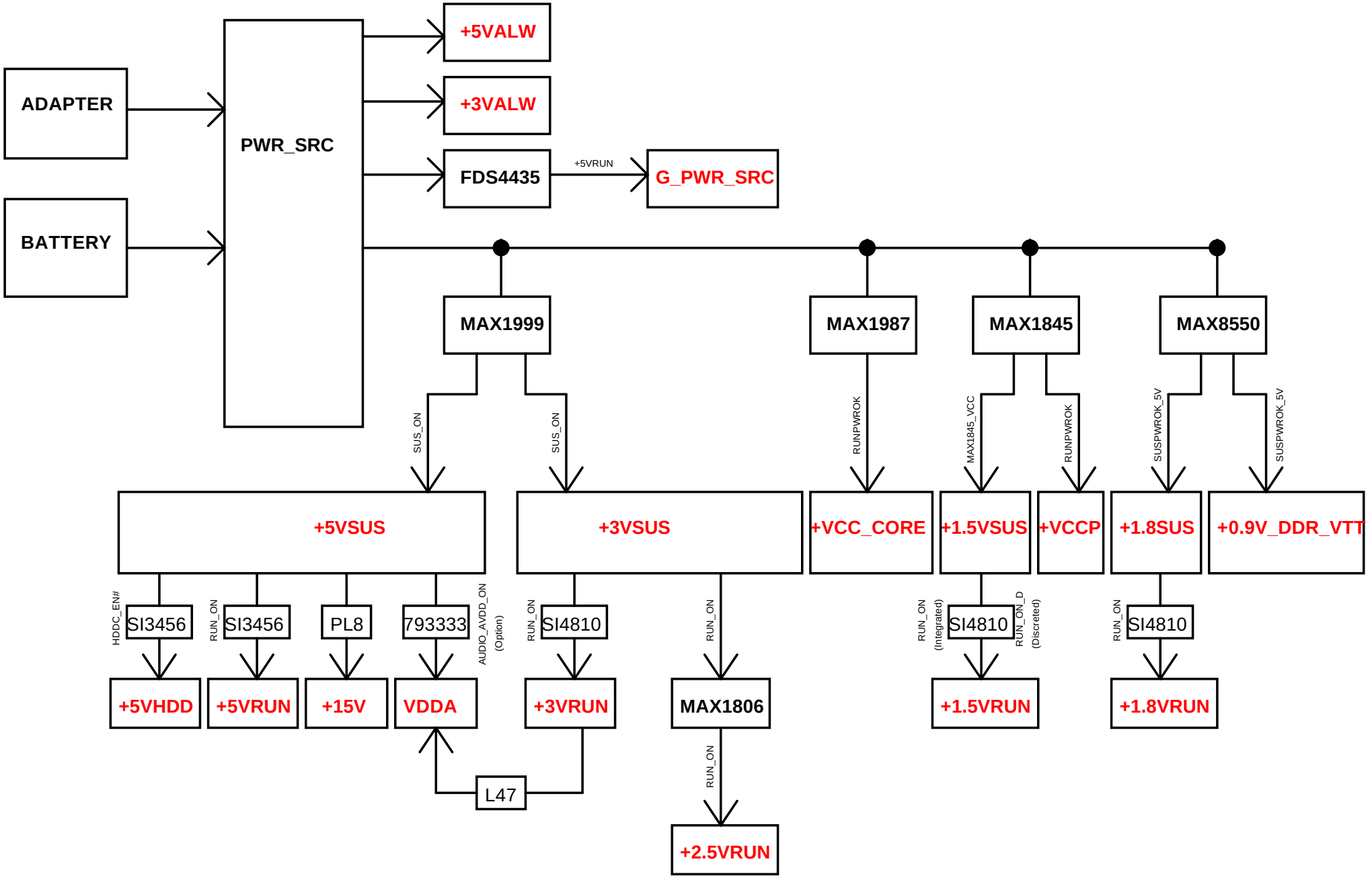

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Title: Power Rail

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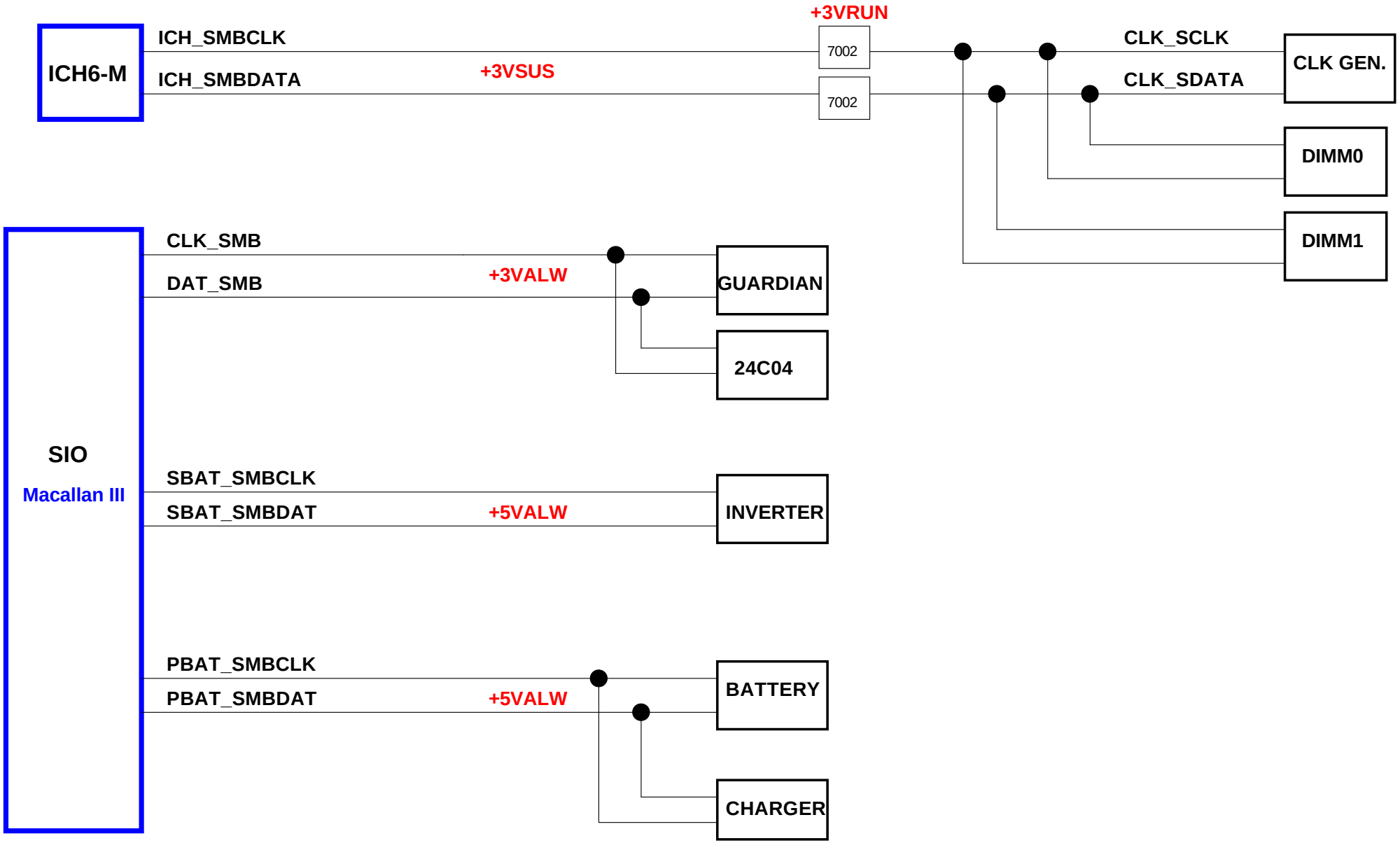

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Title: SMBUS TOPOLOGY

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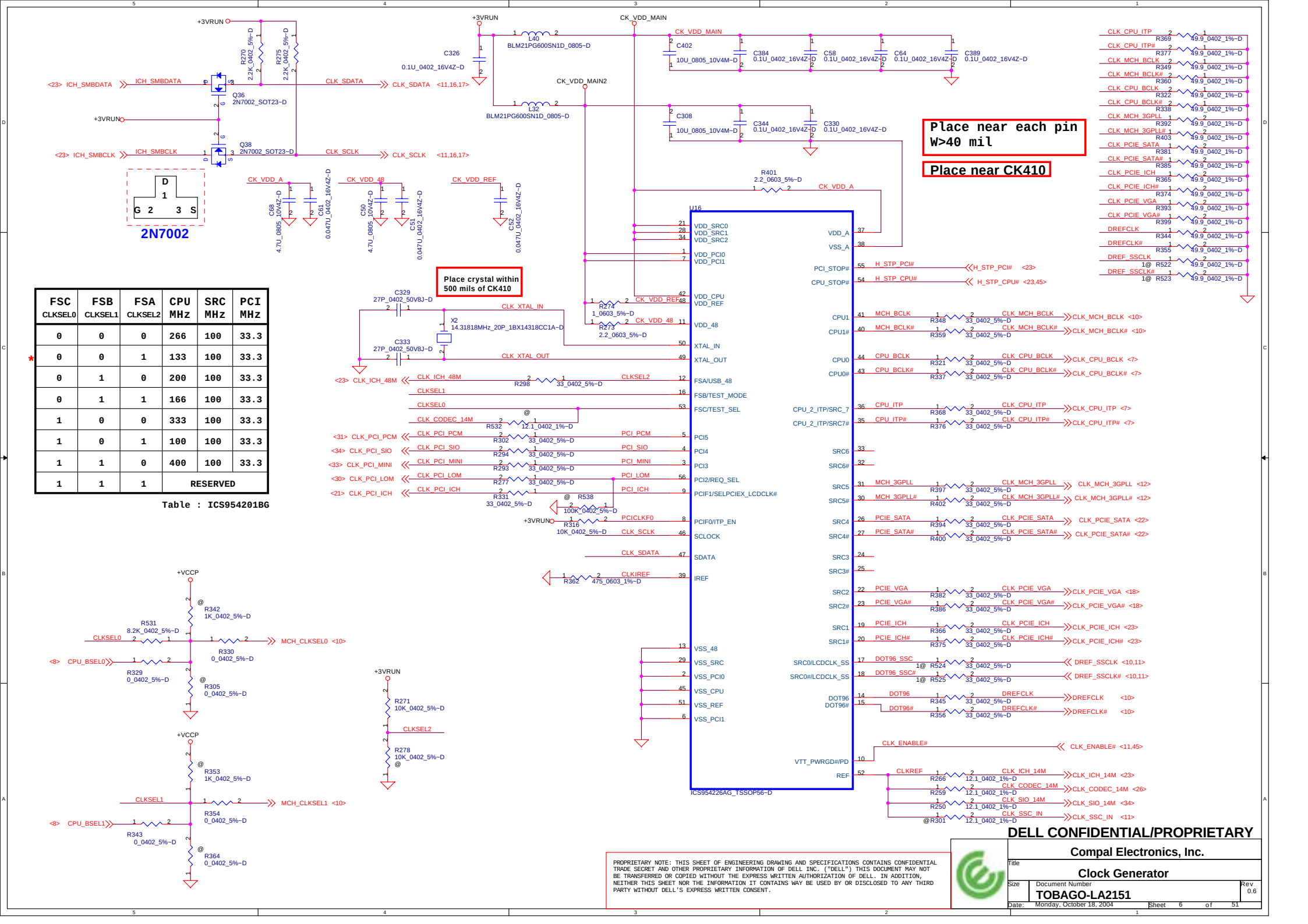

FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
* 0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	RESERVED		

Table : ICS954201BG

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Title: Clock Generator

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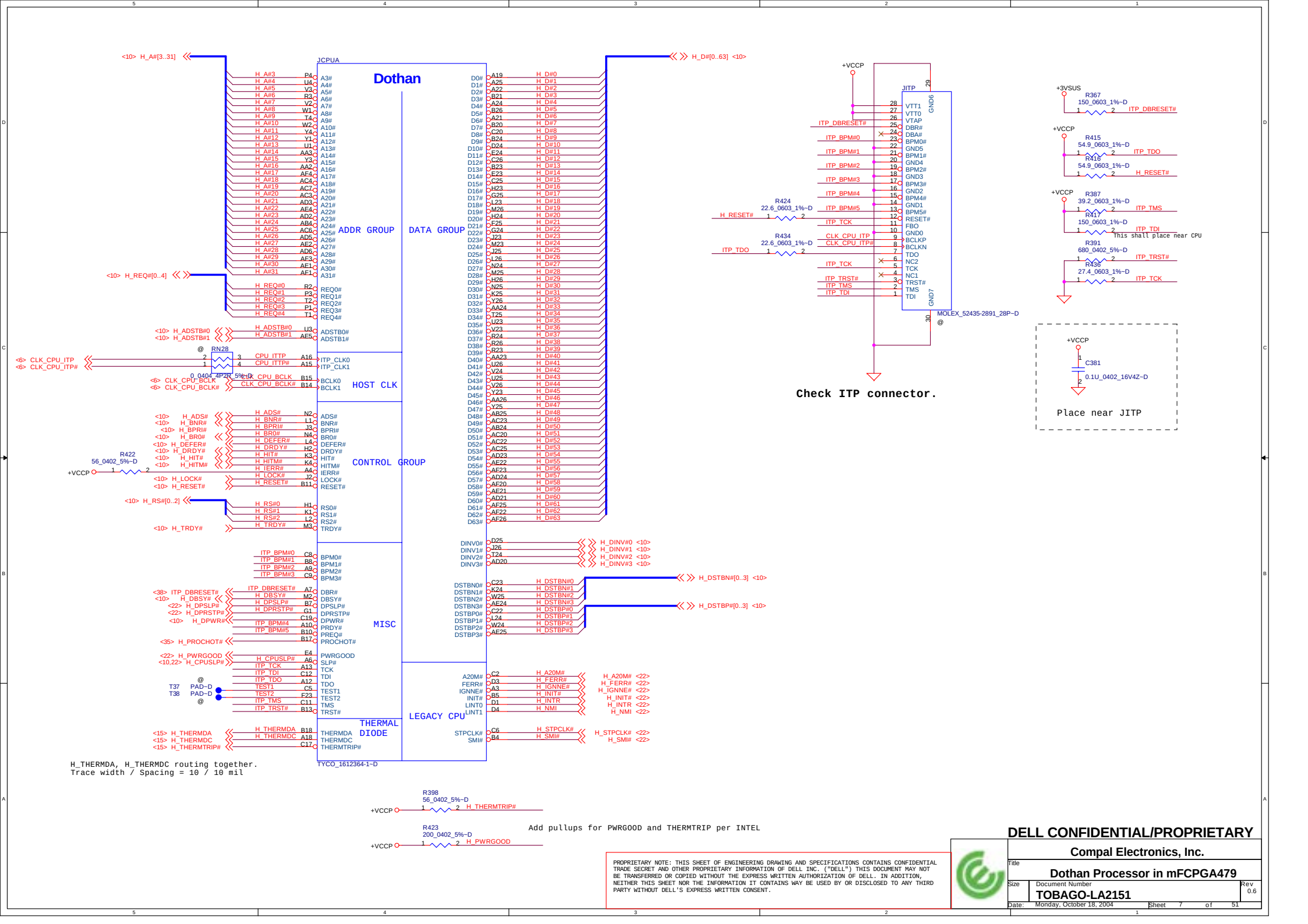

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Title: Dothan Processor in mFCPGA479

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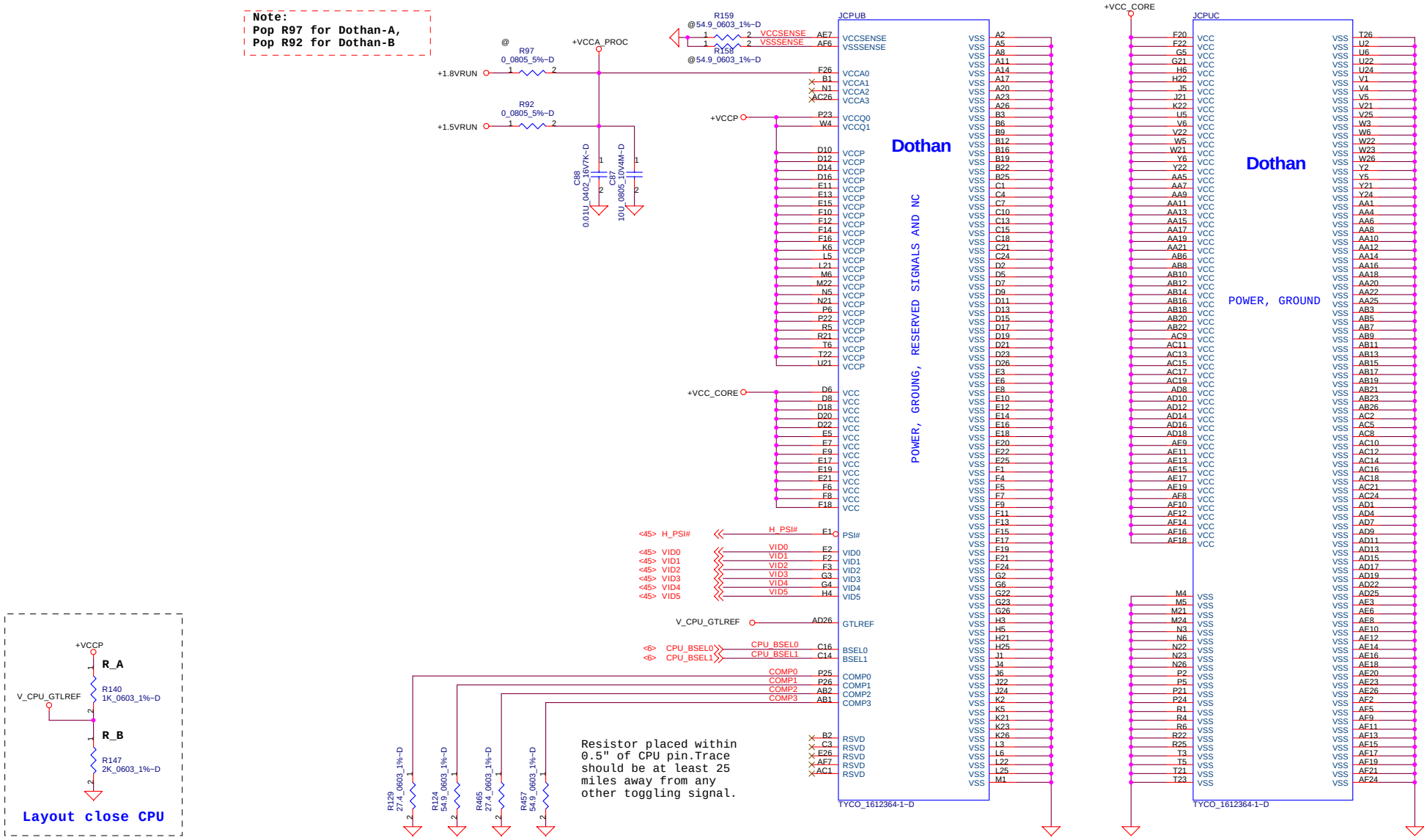

Compal Electronics, Inc.

Title: Dothan Processor in mFCPGA479

Size: | Document Number: TOBAGO-LA2151 | Rev: 0.6

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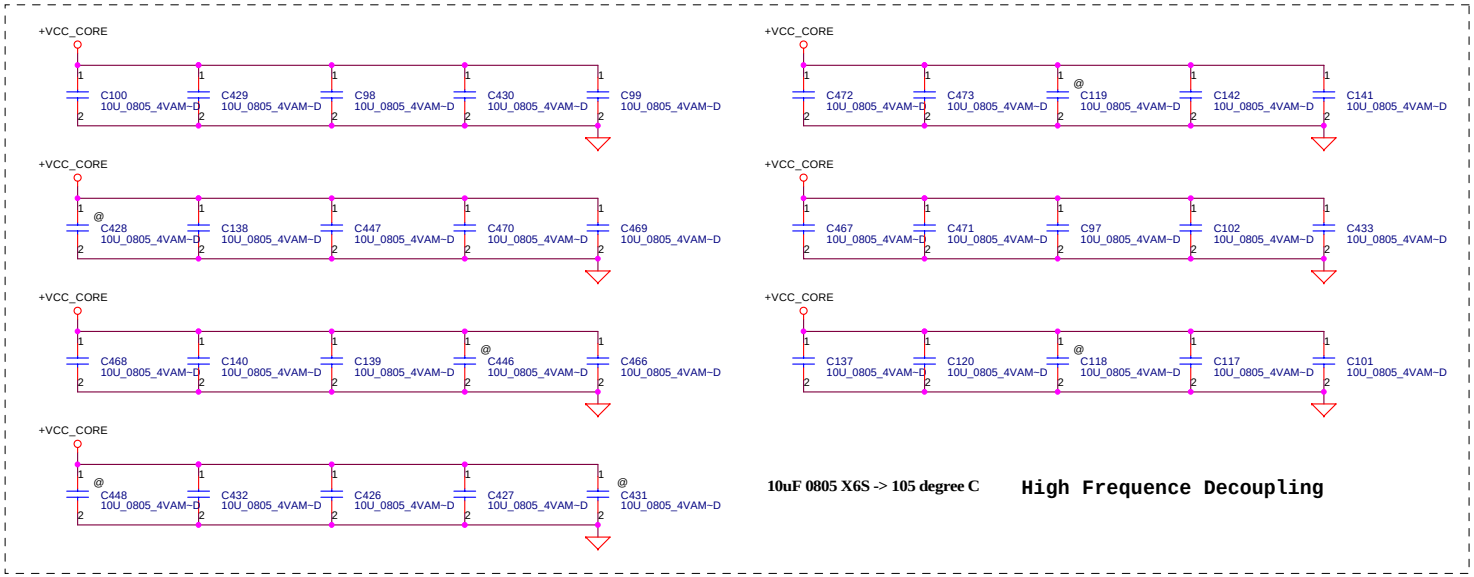
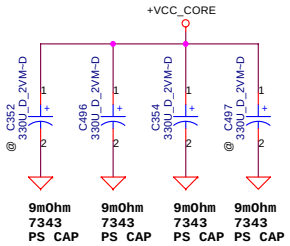
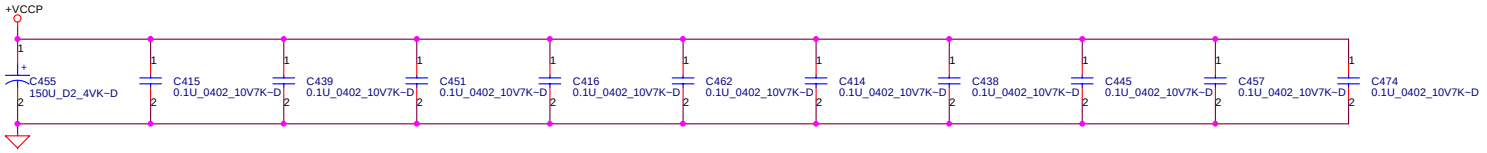


Near VCORE regulator.



ESR <= 3m ohm
Capacitor > 880uF



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Title: CPU Bypass

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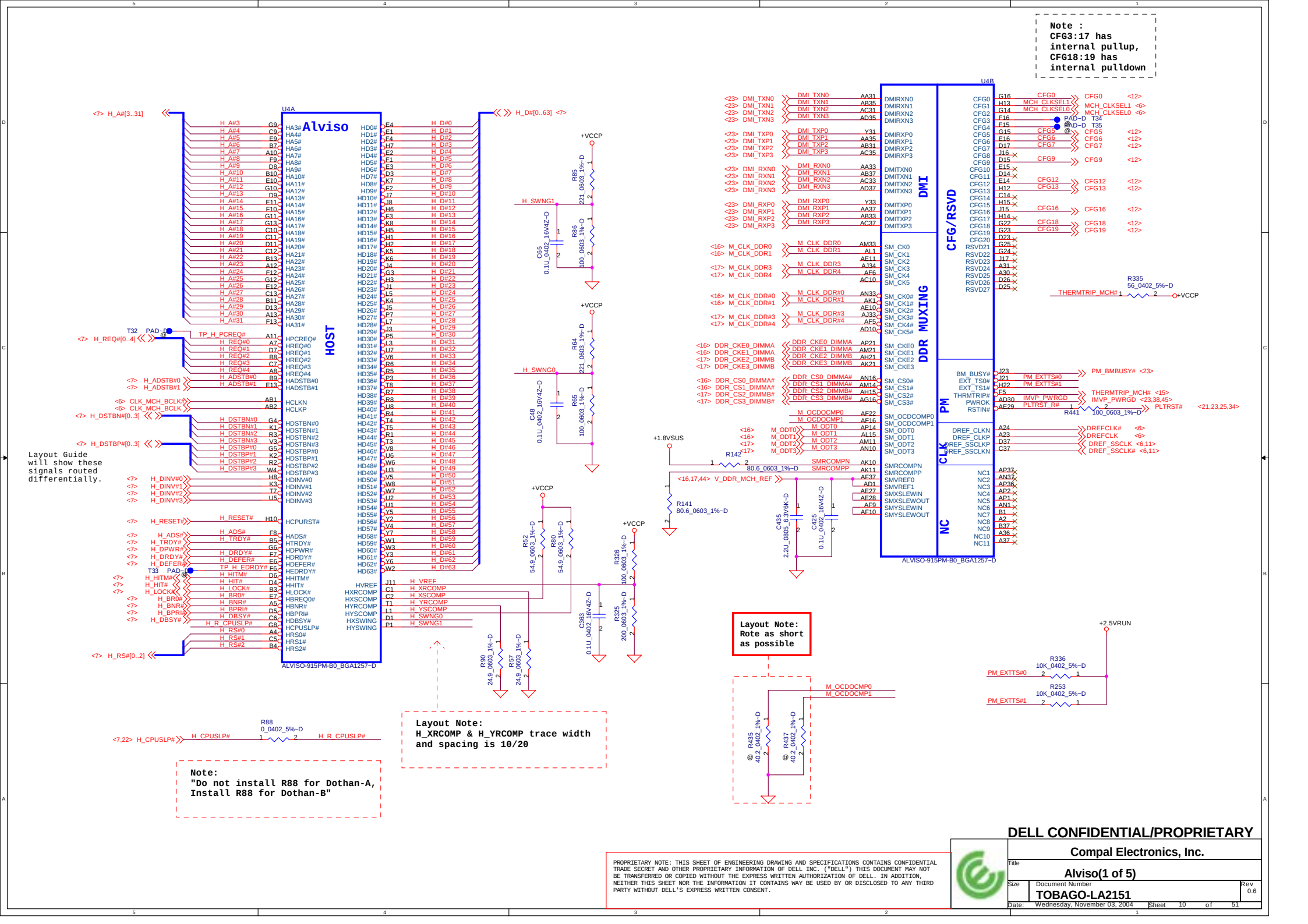
Note :
CFG3:17 has internal pullup, CFG18:19 has internal pulldown
U4A
Alviso
HOST
ALVISO-915PM-B0_BGA1257~D
U4B
DMI
DDR MUXING
CFG/RSVD
PM
CLK
NC
ALVISO-915PM-B0_BGA1257~D
Layout Guide will show these signals routed differentially.
Layout Note: H_XRCOMP & H_YRCOMP trace width and spacing is 10/20
Layout Note: Rote as short as possible
Note: "Do not install R88 for Dothan-A, Install R88 for Dothan-B"
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Title
Alviso(1 of 5)
Size
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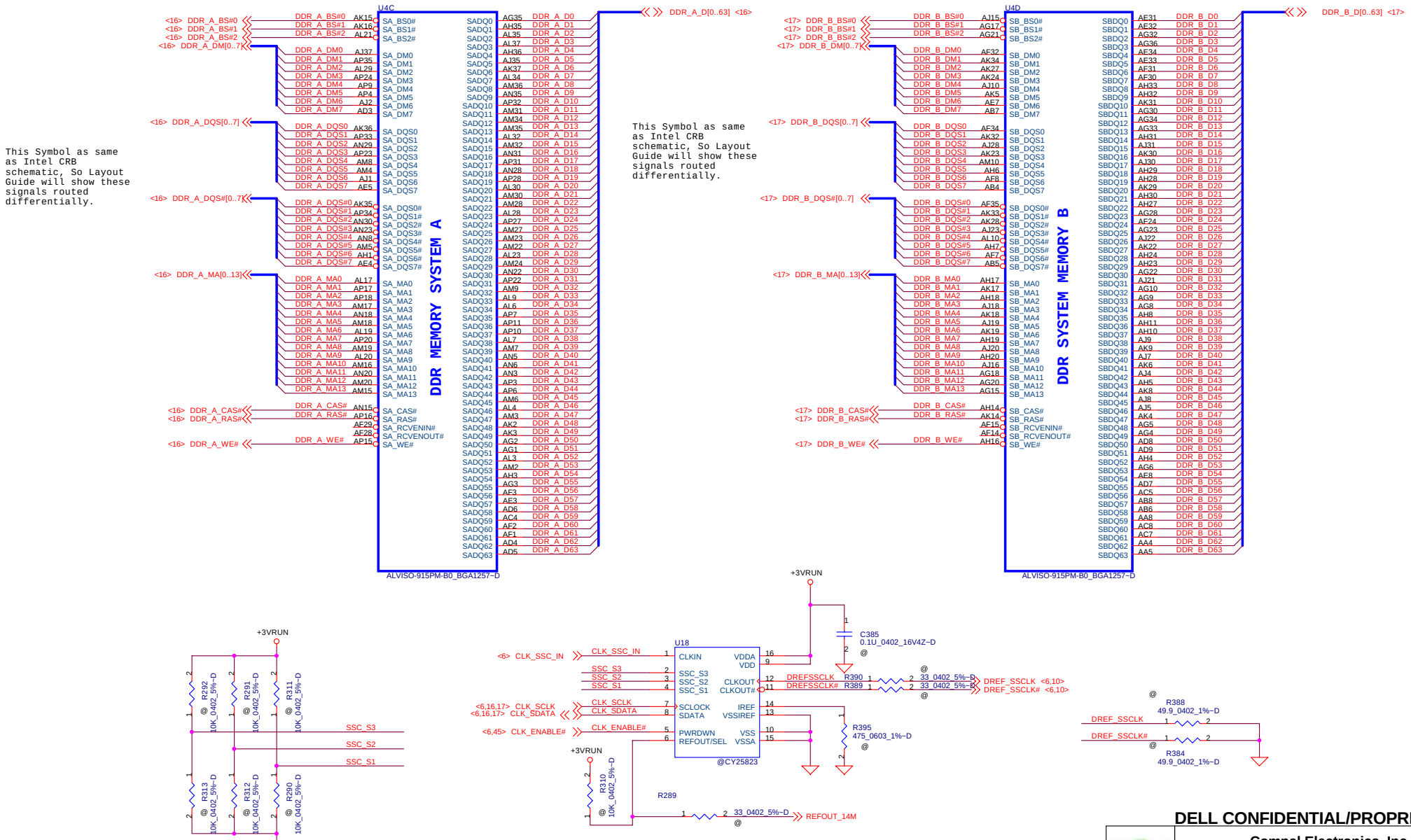

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Title: Alviso(2 of 5)

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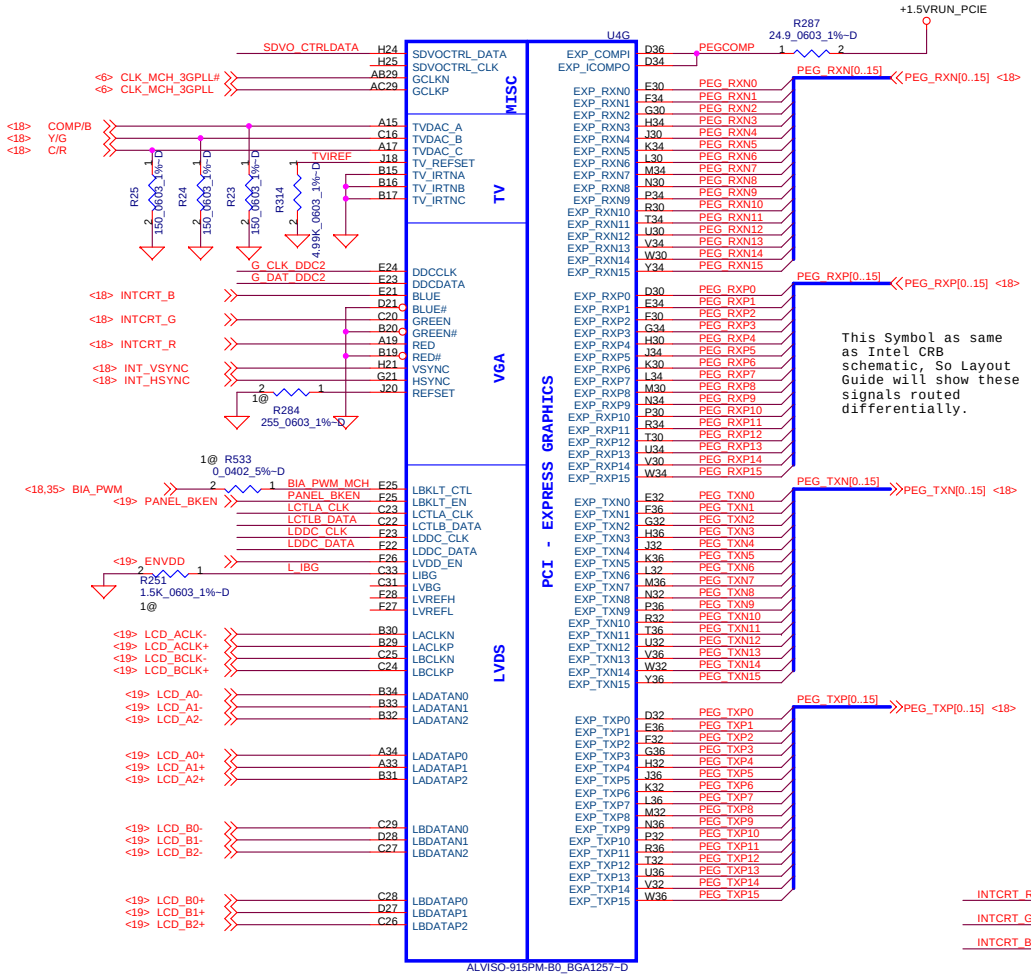
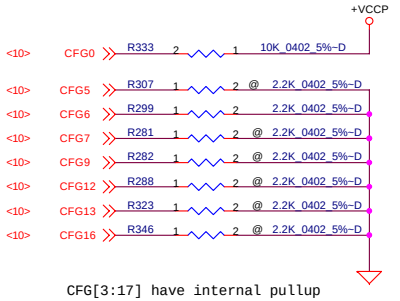


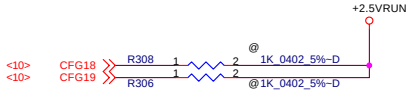
This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.

Strap Table

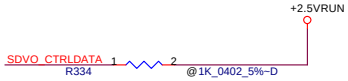
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V
SDVO_CTRLDATA	Low = No SDVO Device Present (Default) * High = SDVO Device Present



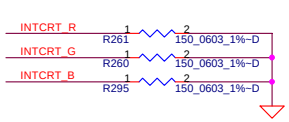
CFG[3:17] have internal pullup

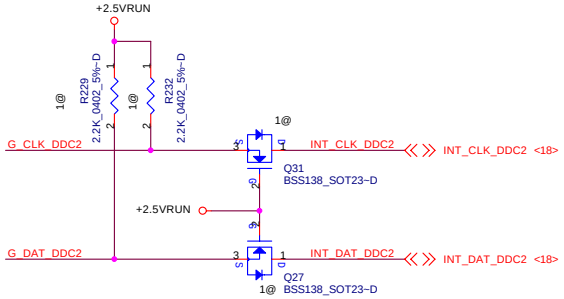


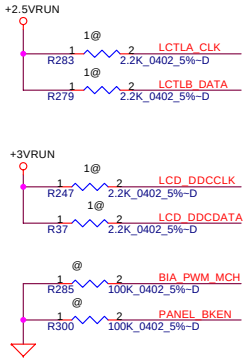
CFG[18:19] have internal pulldown

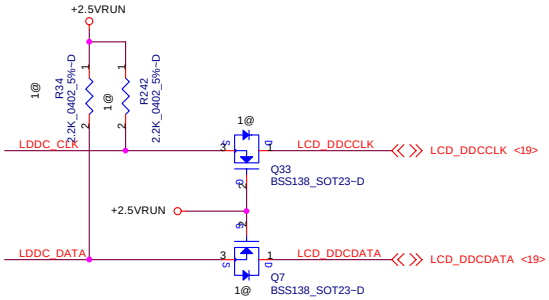


Have internal pulldown









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Title: Alviso(3 of 5)

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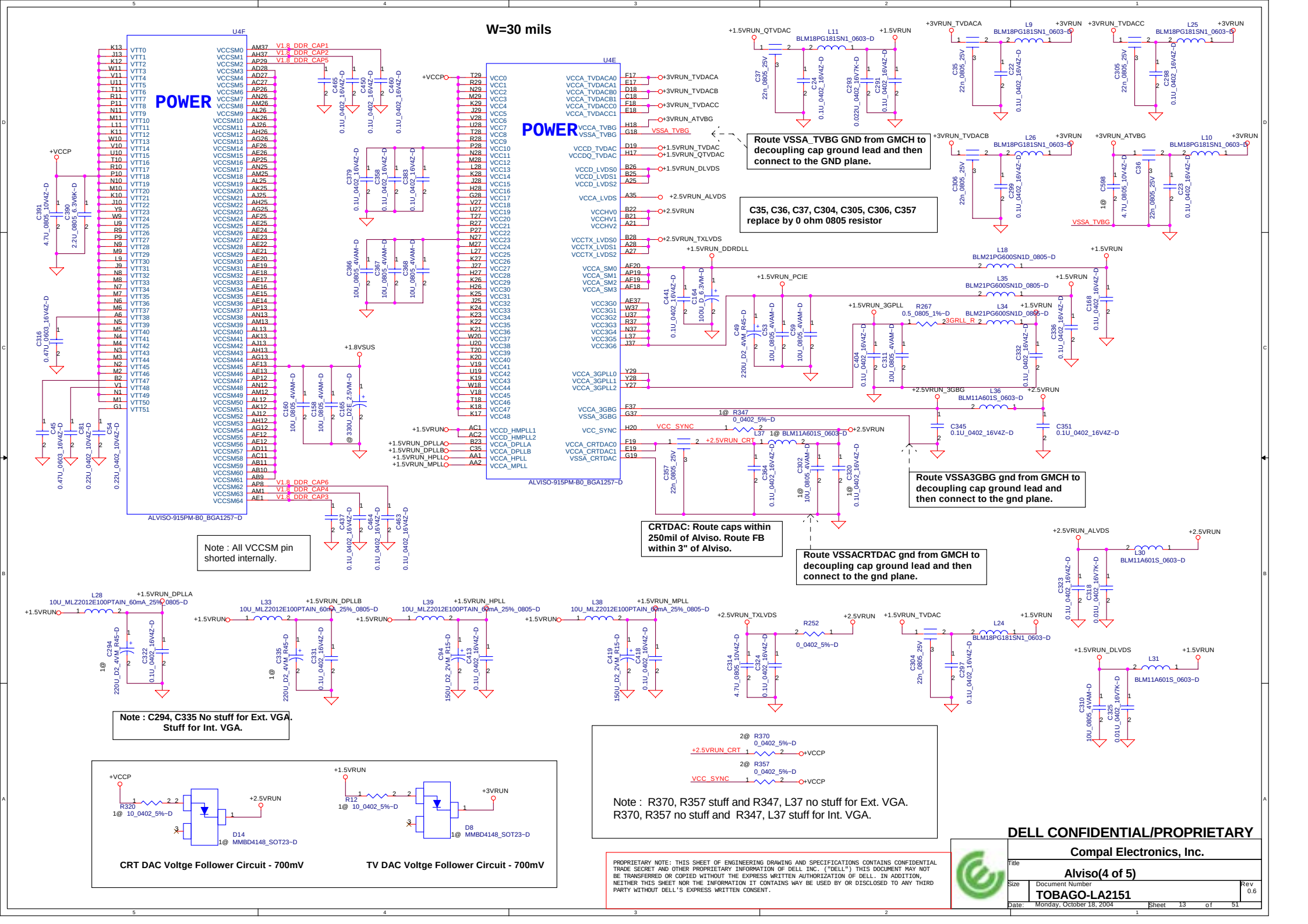

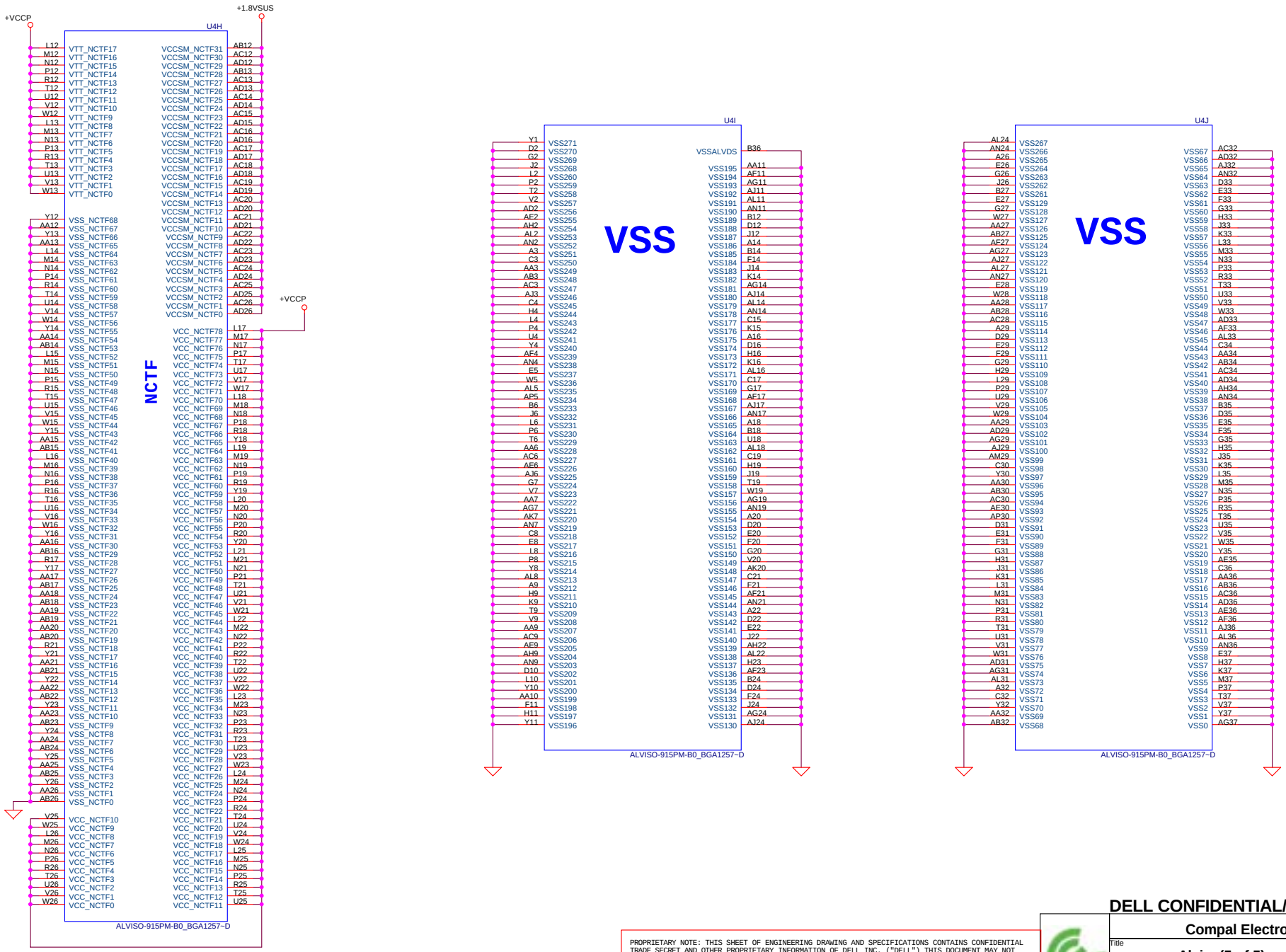

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Title: Alviso(5 of 5)

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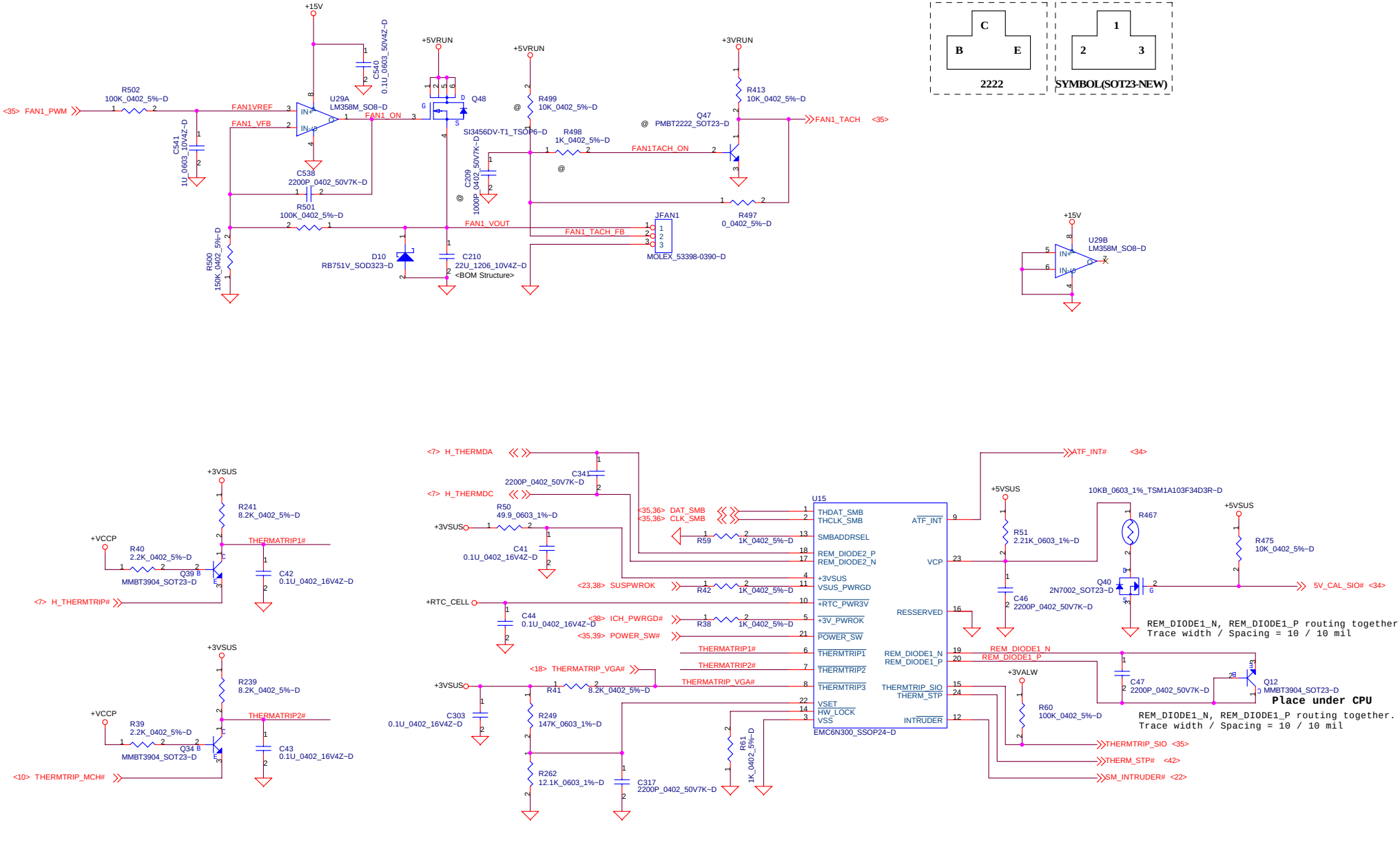
FAN1 Control and Tachometer



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Title: FAN & Thermal Sensor

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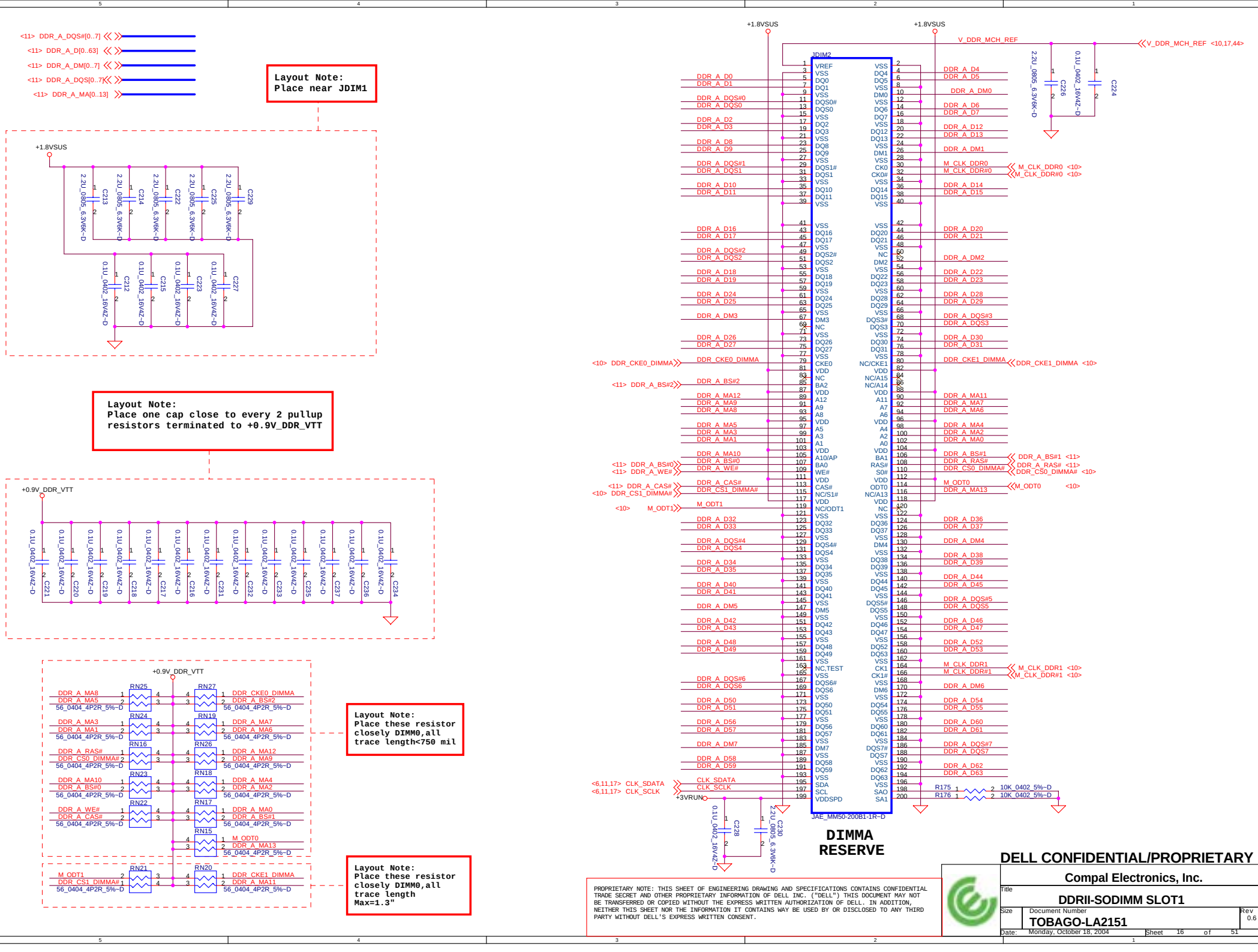
Layout Note:
Place near JDIM1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil
Layout Note:
Place these resistor
closely DIMM0,all
trace length
Max=1.3"
JDIM2
JAE_MM50-200B1-1R-D
DIMMA
RESERVE
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Title
DDRII-SODIMM SLOT1
Size
Document Number
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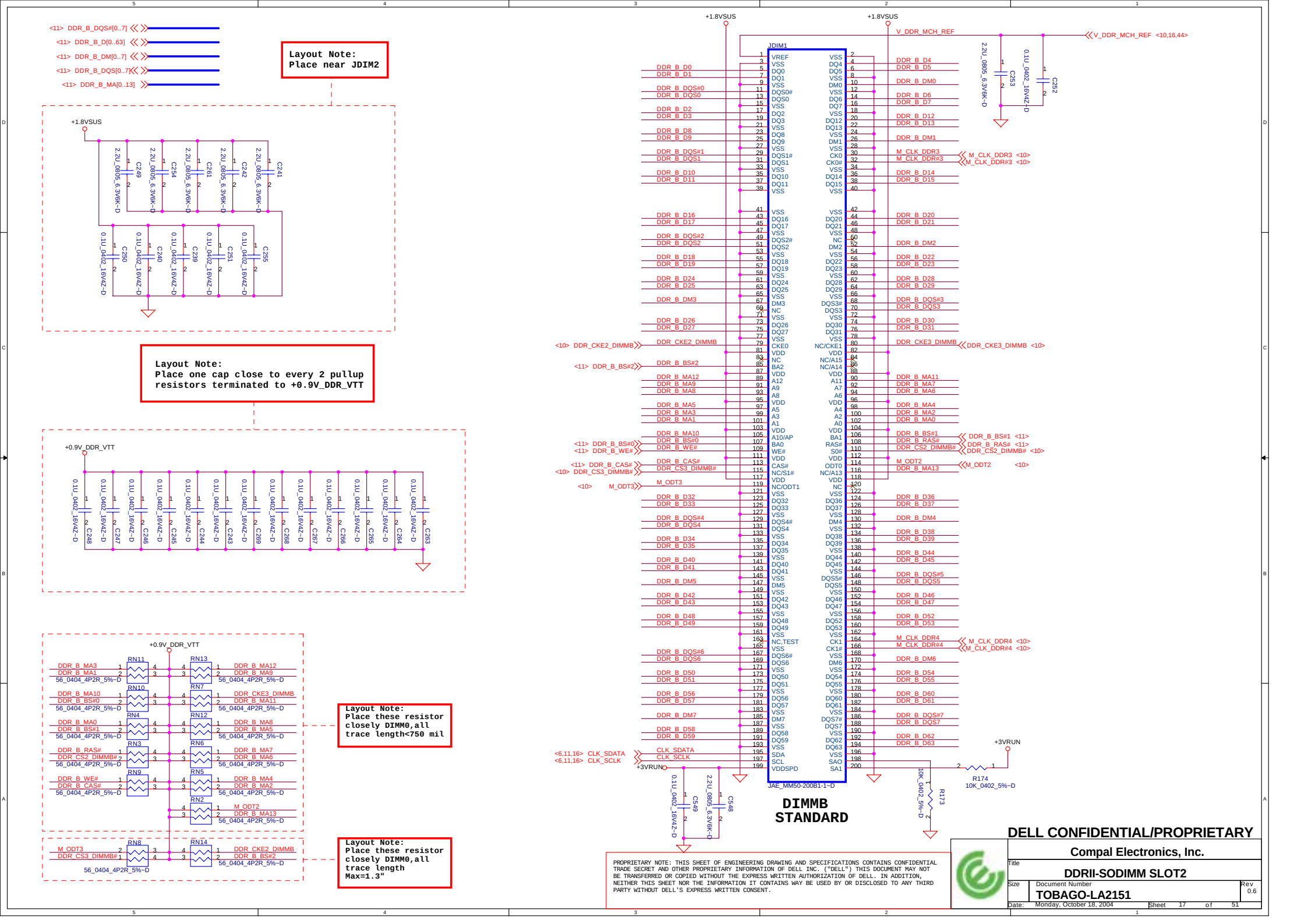
Layout Note:
Place near JDIM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil
Layout Note:
Place these resistor
closely DIMM0,all
trace length
Max=1.3"
JDIM1
JAE_MM50-200B1-1~D
DIMMB
STANDARD
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DDRII-SODIMM SLOT2
TOBAGO-LA2151
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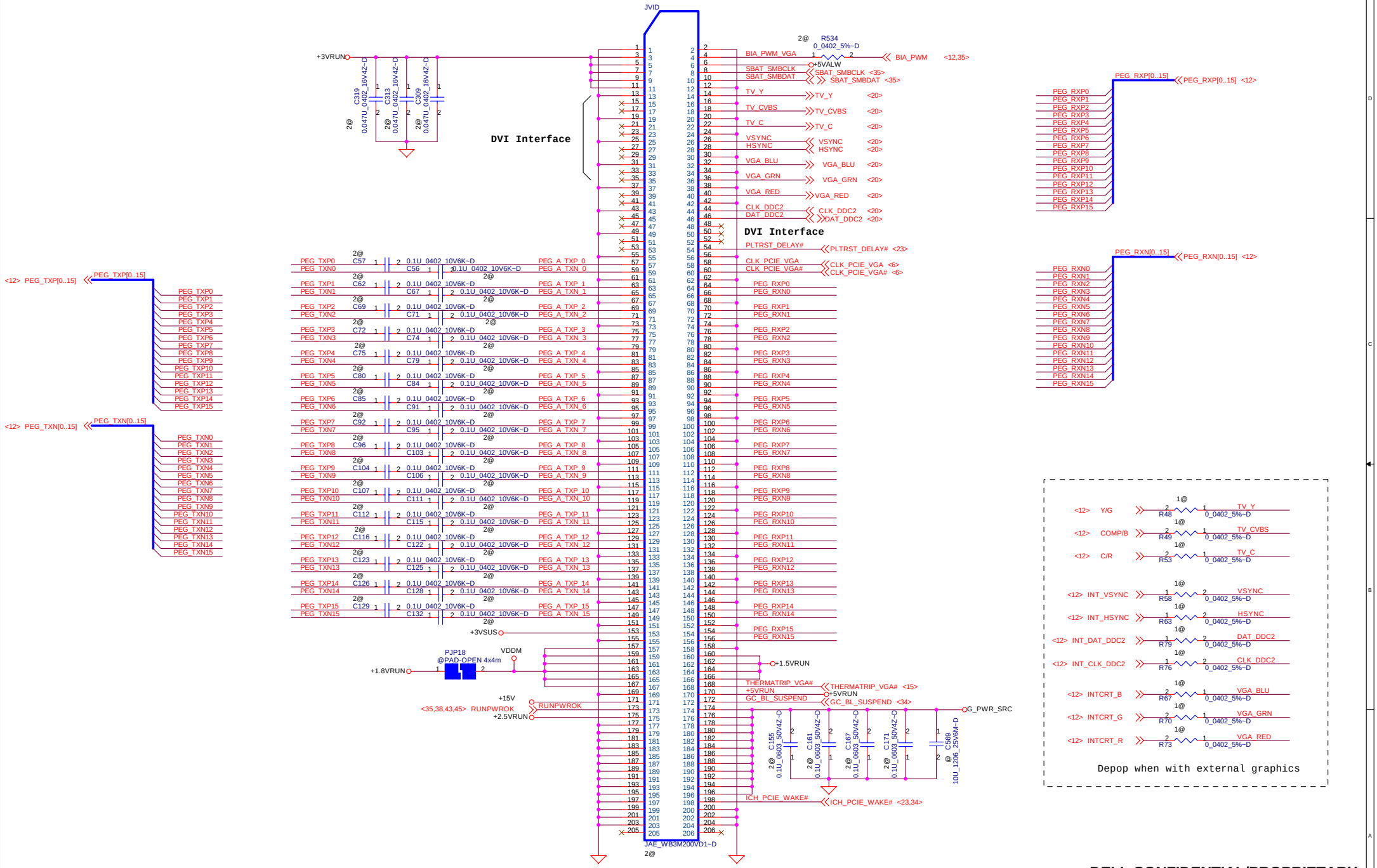

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Title: VGA connector

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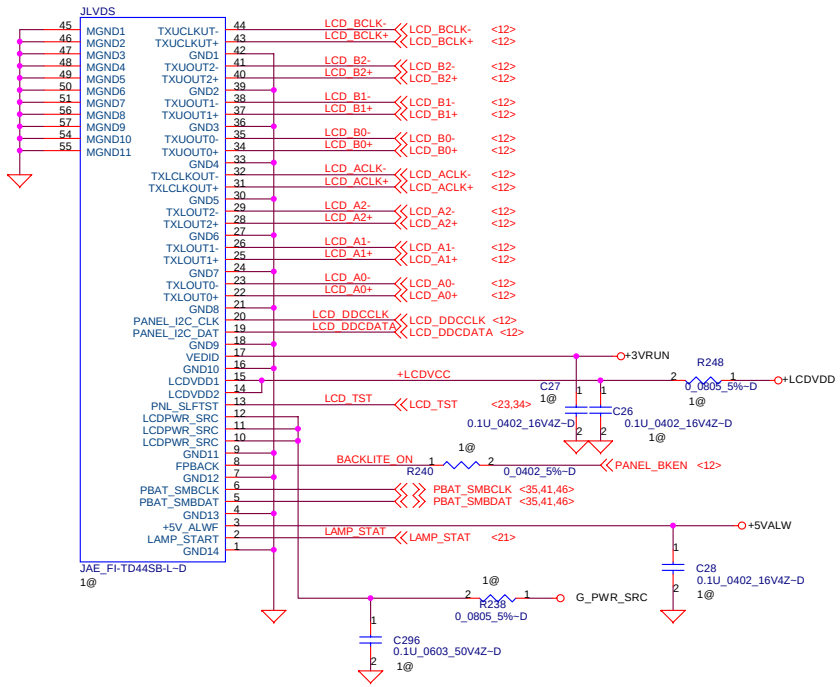

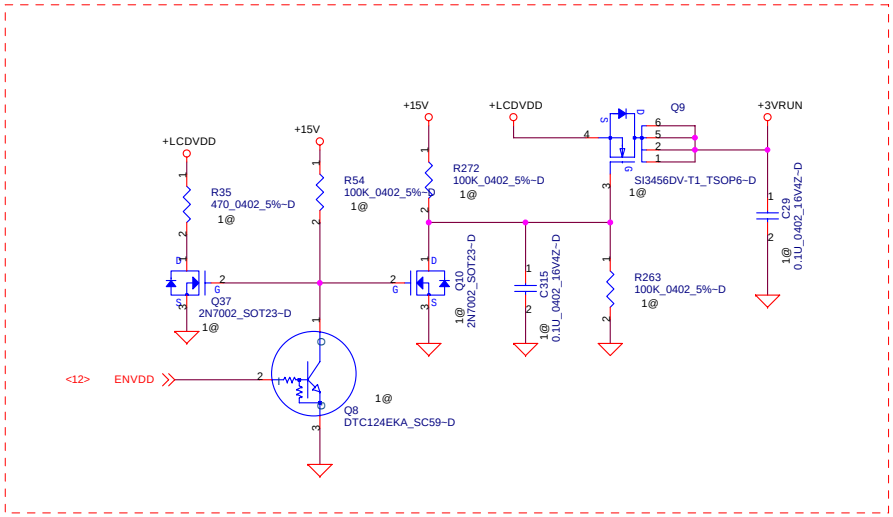

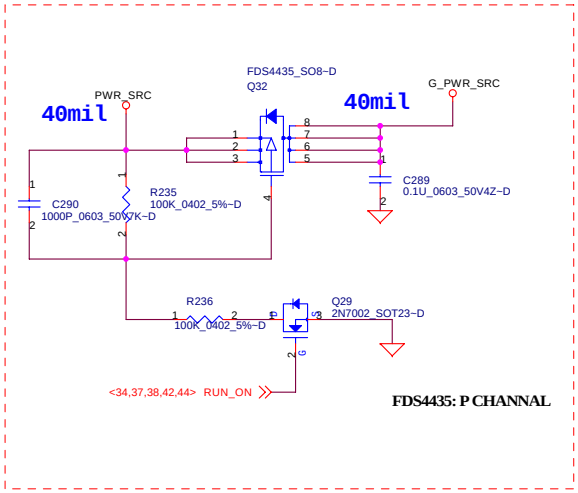

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Title: Internal LVDS

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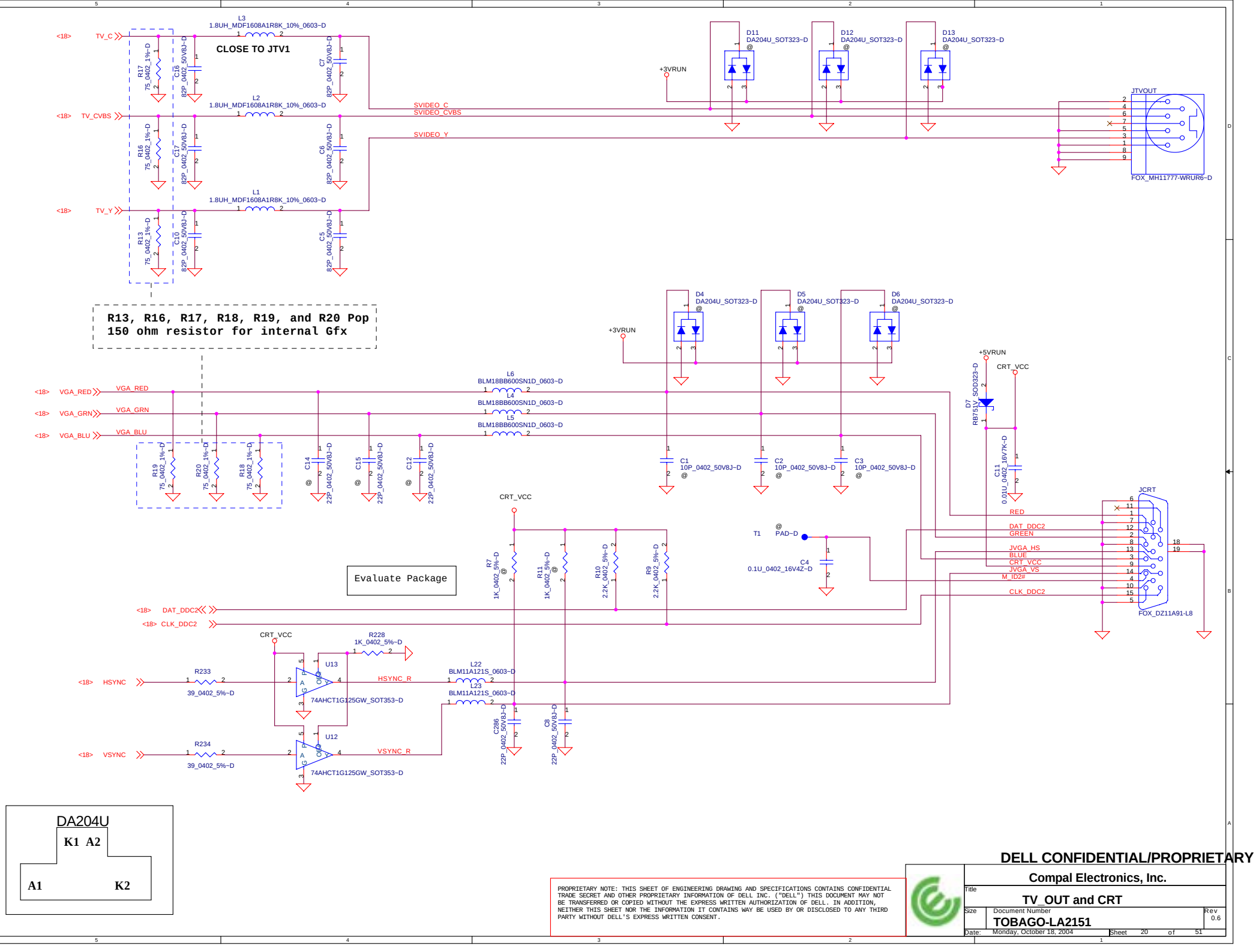
CLOSE TO JTV1
R13, R16, R17, R18, R19, and R20 Pop
150 ohm resistor for internal Gfx
Evaluate Package
DA204U
K1 A2
A1 K2
JTVOUT
FOX_MH11777-WRUR6-D
JCRT
FOX_DZ11A91-L8
74AHCT1G125GW_SOT353-D
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Compal Electronics, Inc.
TV_OUT and CRT
TOBAGO-LA2151
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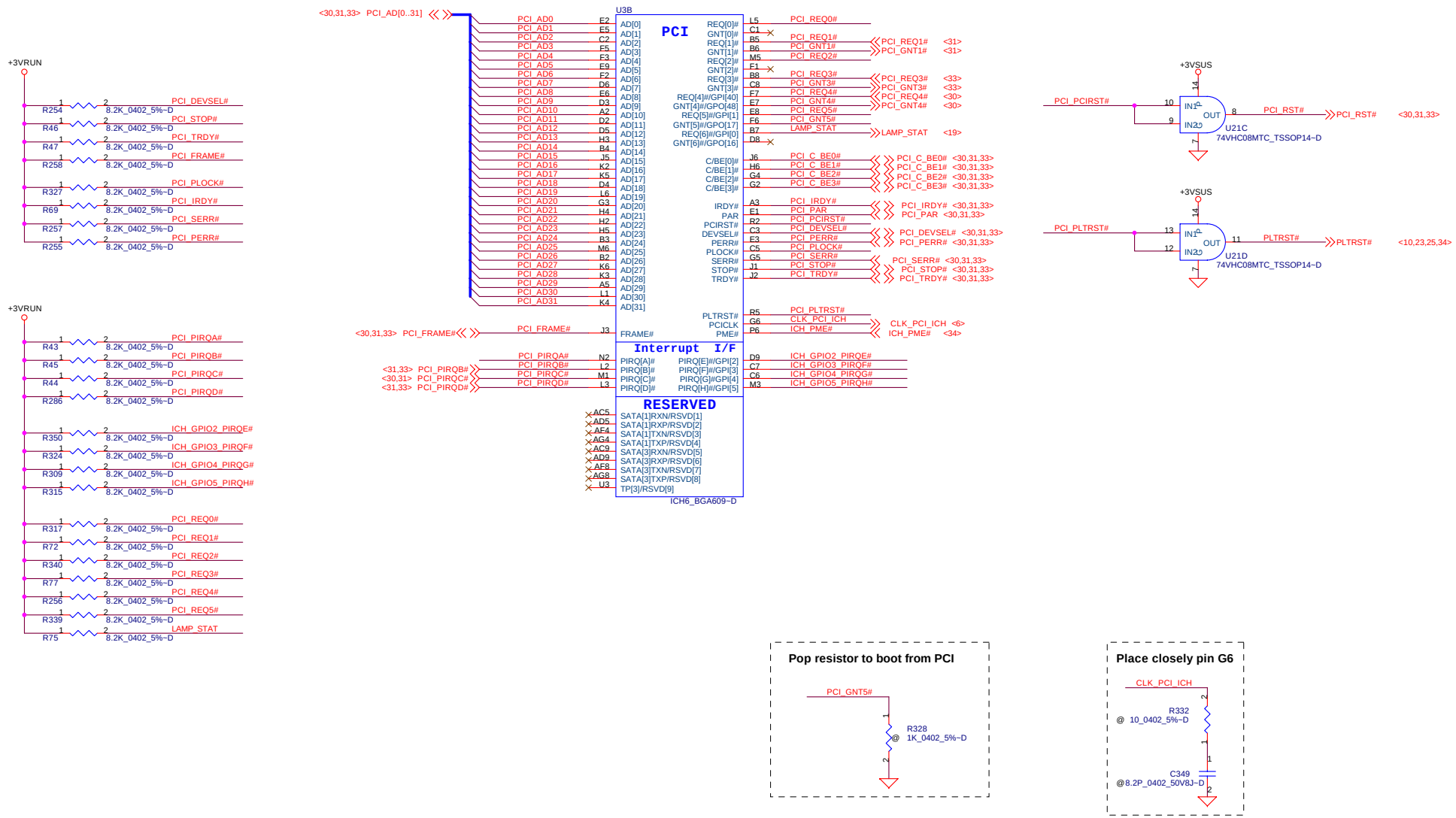

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Title: ICH6(1/4)

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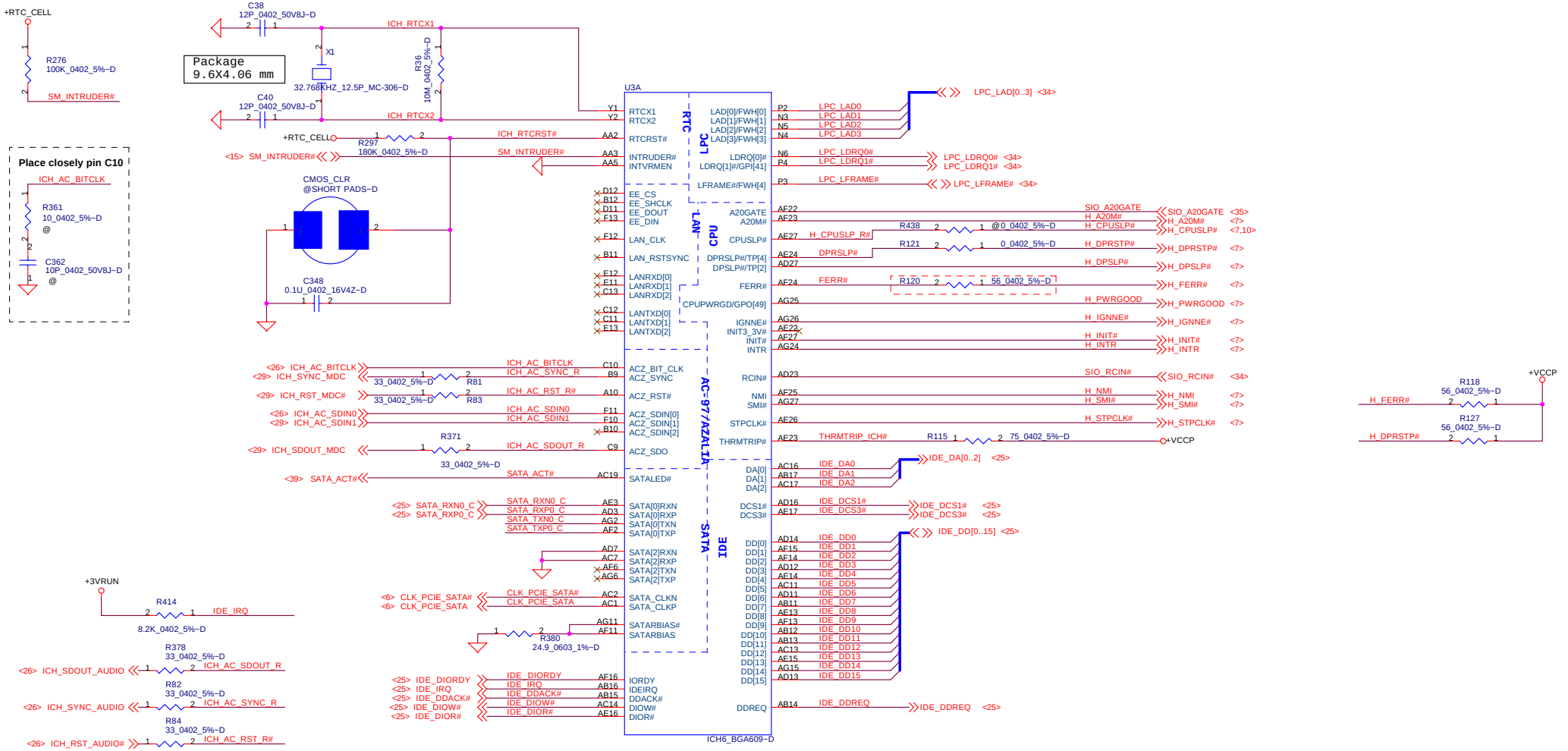

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Title: ICH6(2/4)

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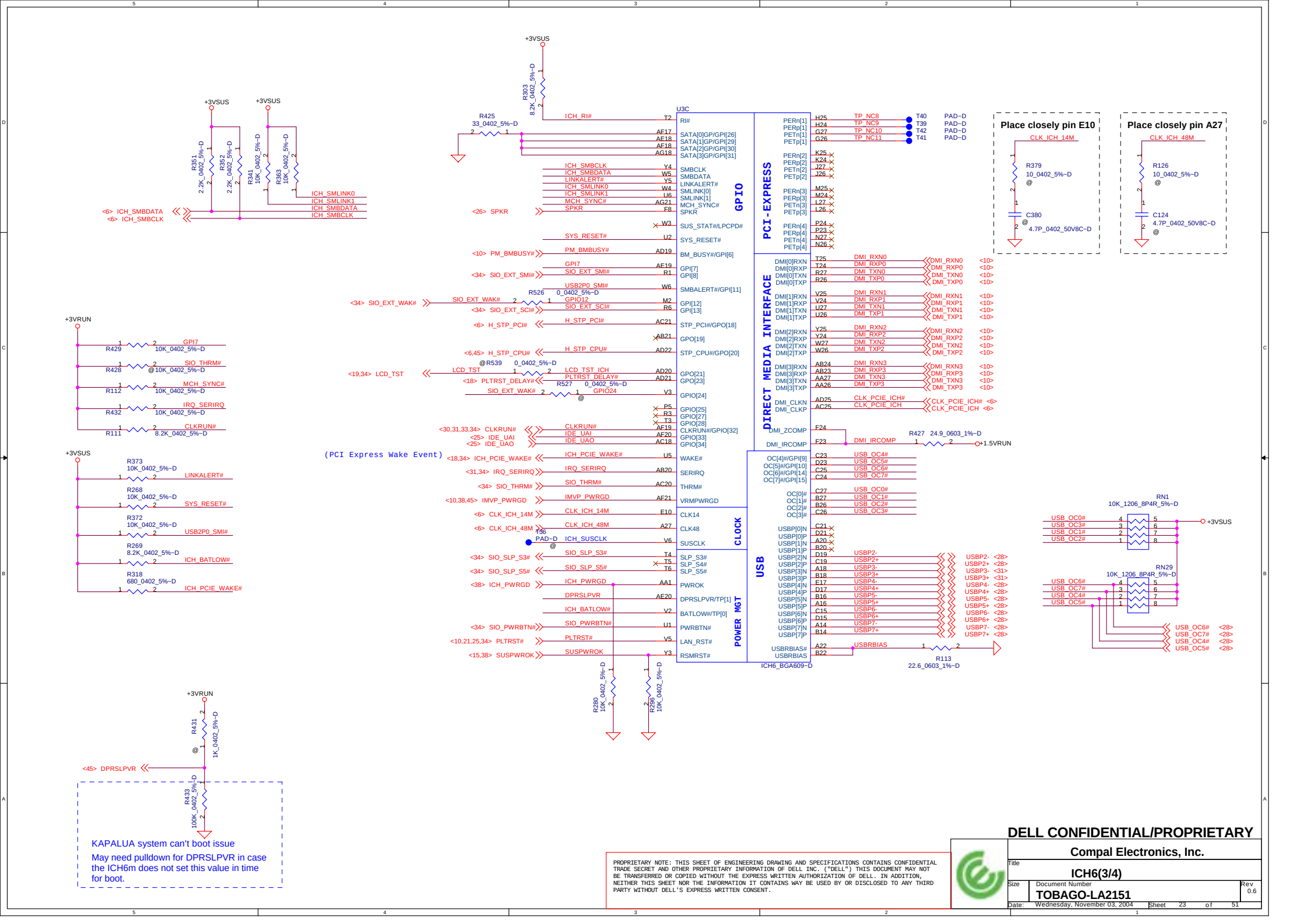
+3VSUS
R303 8.2K_0402_5%~D
U3C
R425 33_0402_5%~D
ICH_RI#
RI#
SATA[0]GP/GPI[26]
SATA[1]GP/GPI[29]
SATA[2]GP/GPI[30]
SATA[3]GP/GPI[31]
GPIO
SMBCLK
SMBDATA
LINKALERT#
SMLINK[0]
SMLINK[1]
MCH_SYNC#
SPKR
SUS_STAT#/LPCPD#
SYS_RESET#
BM_BUSY#/GPI[6]
GPI[7]
GPI[8]
SMBALERT#/GPI[11]
GPI[12]
GPI[13]
STP_PCI#/GPO[18]
GPO[19]
STP_CPU#/GPO[20]
GPO[21]
GPO[23]
GPIO[24]
GPIO[25]
GPIO[27]
GPIO[28]
CLKRUN#/GPIO[32]
GPIO[33]
GPIO[34]
WAKE#
SERIRQ
THRM#
VRMPWRGD
CLOCK
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
DPRSLPVR/TP[1]
BATLOW#/TP[0]
PWRBTN#
LAN_RST#
RSMRST#
POWER MGT
PCI-EXPRESS
PERn[1]
PERp[1]
PETn[1]
PETp[1]
PERn[2]
PERp[2]
PETn[2]
PETp[2]
PERn[3]
PERp[3]
PETn[3]
PETp[3]
PERn[4]
PERp[4]
PETn[4]
PETp[4]
TP_NC8
TP_NC9
TP_NC10
TP_NC11
PAD~D
DIRECT MEDIA INTERFACE
DMI[0]RXN
DMI[0]RXP
DMI[0]TXN
DMI[0]TXP
DMI[1]RXN
DMI[1]RXP
DMI[1]TXN
DMI[1]TXP
DMI[2]RXN
DMI[2]RXP
DMI[2]TXN
DMI[2]TXP
DMI[3]RXN
DMI[3]RXP
DMI[3]TXN
DMI[3]TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
R427 24.9_0603_1%~D
+1.5VRUN
USB
OC[4]#/GPI[9]
OC[5]#/GPI[10]
OC[6]#/GPI[14]
OC[7]#/GPI[15]
OC[0]#
OC[1]#
OC[2]#
OC[3]#
USBP[0]N
USBP[0]P
USBP[1]N
USBP[1]P
USBP[2]N
USBP[2]P
USBP[3]N
USBP[3]P
USBP[4]N
USBP[4]P
USBP[5]N
USBP[5]P
USBP[6]N
USBP[6]P
USBP[7]N
USBP[7]P
USBRBIAS#
USBRBIAS
R113 22.6_0603_1%~D
ICH6_BGA609~D
Place closely pin E10
CLK_ICH_14M
R379 10_0402_5%~D
C380 4.7P_0402_50V8C~D
Place closely pin A27
CLK_ICH_48M
R126 10_0402_5%~D
C124 4.7P_0402_50V8C~D
RN1 10K_1206_8P4R_5%~D
RN29 10K_1206_8P4R_5%~D
+3VRUN
GPI7 10K_0402_5%~D
SIO_THRM# 10K_0402_5%~D
MCH_SYNC# 10K_0402_5%~D
IRQ_SERIRQ 10K_0402_5%~D
CLKRUN# 8.2K_0402_5%~D
LINKALERT# 10K_0402_5%~D
SYS_RESET# 10K_0402_5%~D
USB2P0_SMI# 10K_0402_5%~D
ICH_BATLOW# 8.2K_0402_5%~D
ICH_PCIE_WAKE# 680_0402_5%~D
(PCI Express Wake Event)
R351 2.2K_0402_5%~D
R352 2.2K_0402_5%~D
R341 10K_0402_5%~D
R363 10K_0402_5%~D
ICH_SMLINK0
ICH_SMLINK1
ICH_SMBDATA
ICH_SMBCLK
R280 10K_0402_5%~D
R286 10K_0402_5%~D
R431 1K_0402_5%~D
R433 100K_0402_5%~D
DPRSLPVR
KAPALUA system can't boot issue
May need pulldown for DPRSLPVR in case the ICH6m does not set this value in time for boot.
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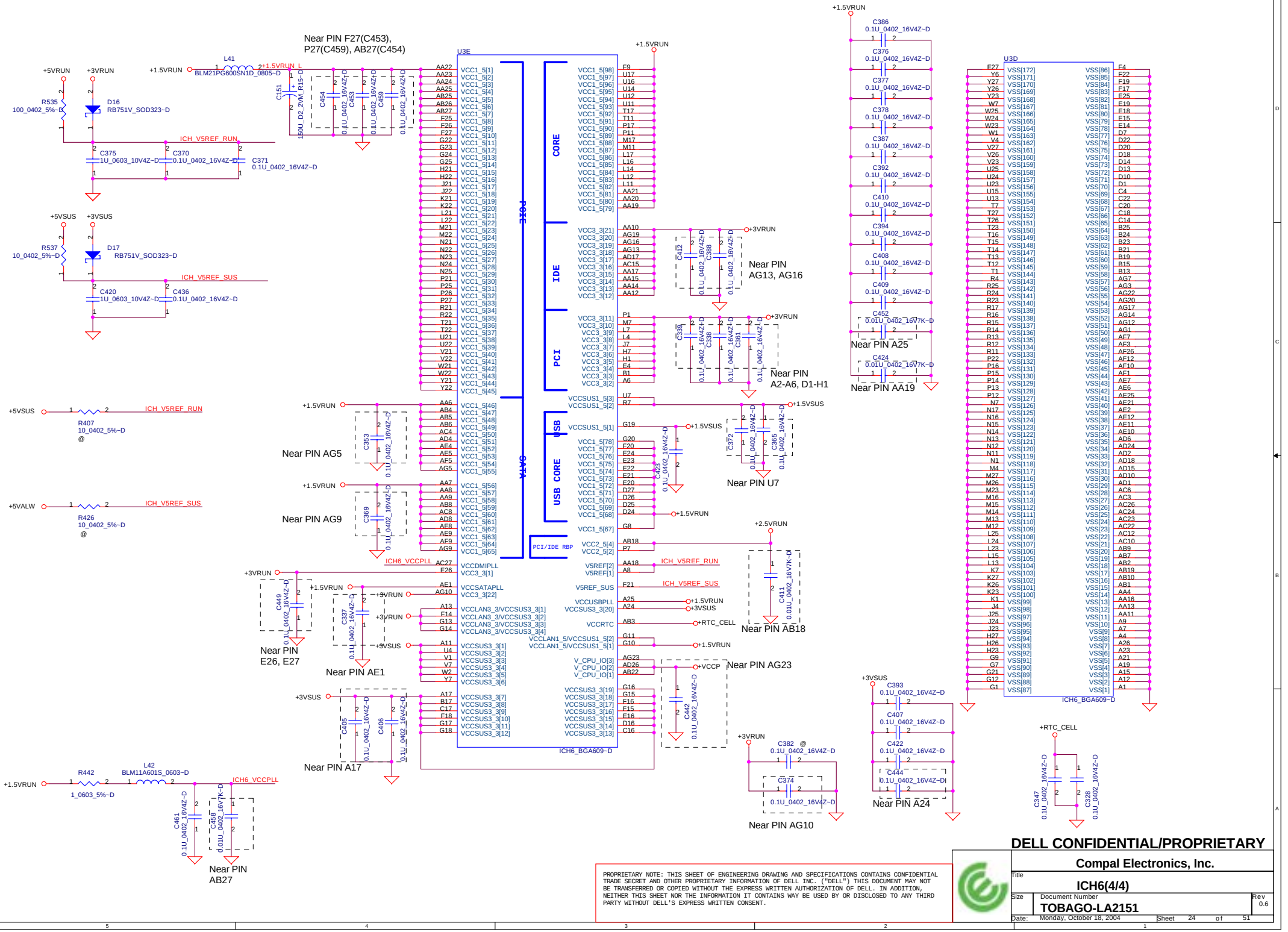
Compal Electronics, Inc.
Title
ICH6(3/4)
Size
Document Number
TOBAGO-LA2151
Rev 0.6
Date: Wednesday, November 03, 2004
Sheet 23 of 51


Near PIN F27(C453), P27(C459), AB27(C454)
U3E
CORE
FSBE
IDE
PCI
USB
USB CORE
SATA
PCI/IDE RBP
ICH6_BGA609~D
Near PIN AG13, AG16
Near PIN A2-A6, D1-H1
Near PIN AA19
Near PIN A25
Near PIN U7
Near PIN AB18
Near PIN AG23
Near PIN AG10
Near PIN A24
Near PIN AG5
Near PIN AG9
Near PIN E26, E27
Near PIN AE1
Near PIN A17
Near PIN AB27
U3D
ICH6_BGA609~D
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Compal Electronics, Inc.
ICH6(4/4)
TOBAGO-LA2151
Monday, October 18, 2004
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Sets maximum transfer rate and UDMA mode

CNFG2 INT PD	CNFG1	CNFG0 INT PD	NOTE
0	0	0	Device Mode 100MB/s
0	0	1	Device Mode 133MB/s
0	1	0	Device Mode 150MB/s
1	0	0	Host Mode 100MB/s
1	0	1	Host Mode 133MB/s
1	1	0	Host Mode 150MB/s
0	1	1	Reserved
1	1	1	Reserved

Pleace near HD CONN

Pleace near U178

HDD Connector

CD-ROM Connector

25MHz reference clock T[4:3] = 01

Place near connector side.

Compal Electronics, Inc.

Title: SATA Bridge

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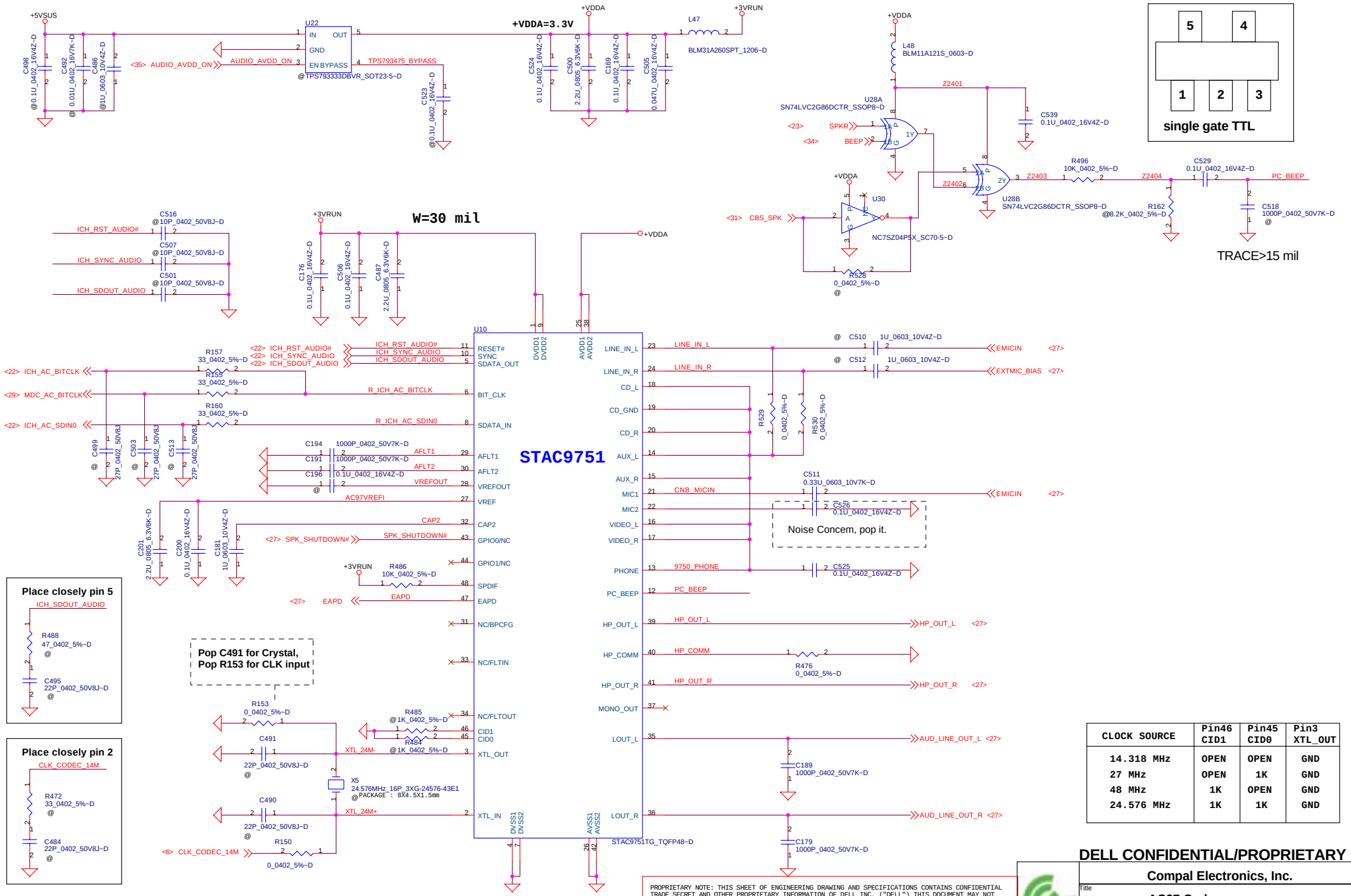
Date: Monday, October 18, 2004 | Sheet 25 of 51



CLOCK SOURCE	Pin46 CID1	Pin45 CID0	Pin3 XTL_OUT
14.318 MHz	OPEN	OPEN	GND
27 MHz	OPEN	1K	GND
48 MHz	1K	OPEN	GND
24.576 MHz	1K	1K	GND

Compal Electronics, Inc.

Title: AC97 Codec

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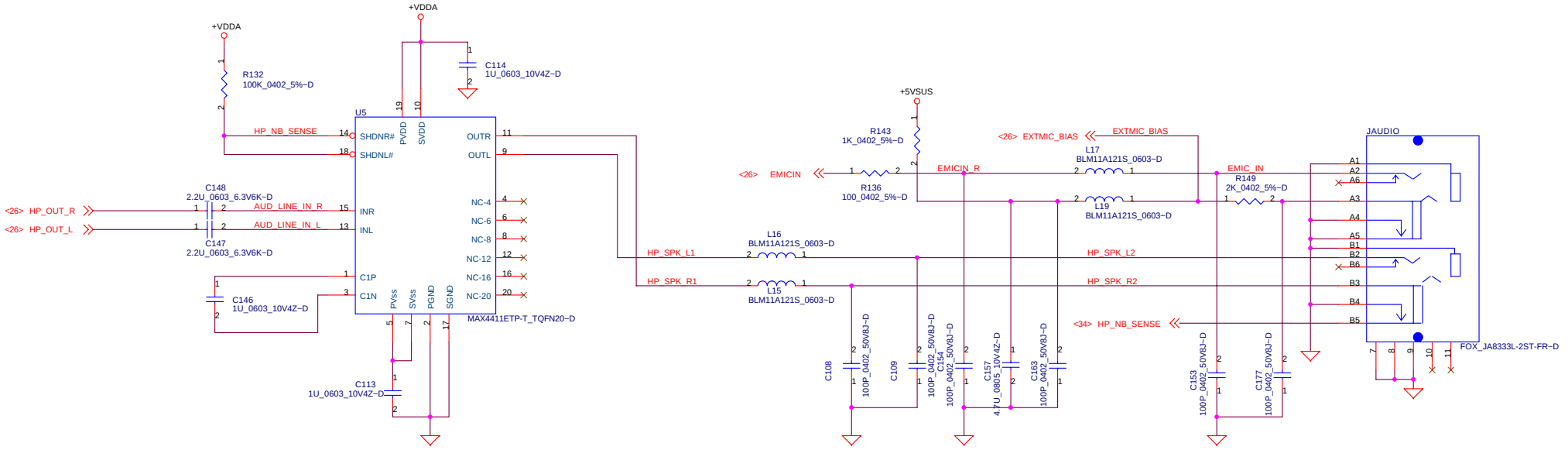
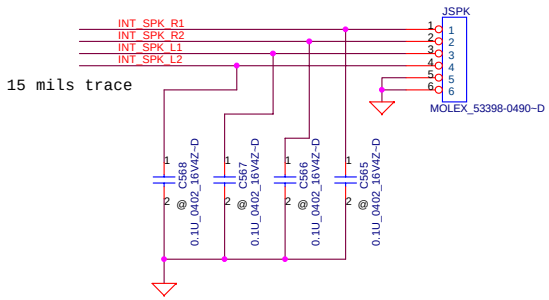
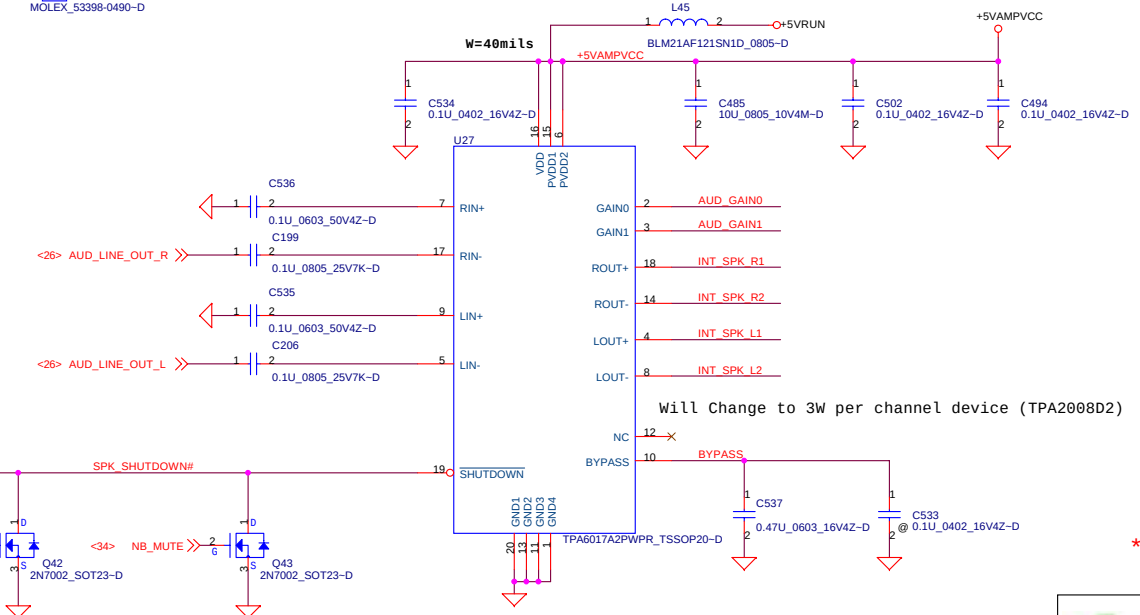
Date: Monday, October 18, 2004 | Sheet 26 of 51

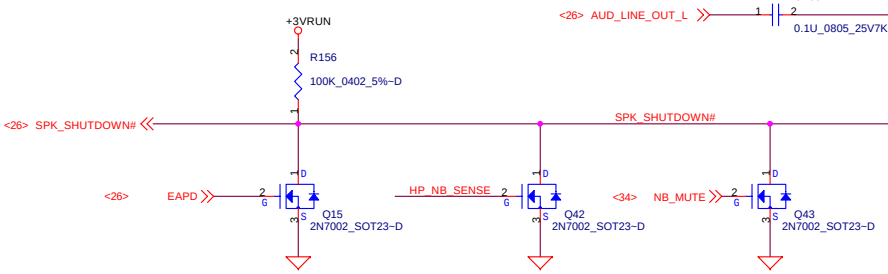


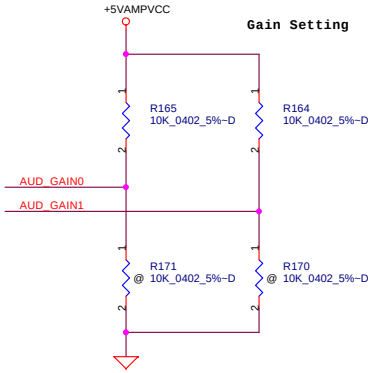
Speaker Connector



LINE OUT







GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

*

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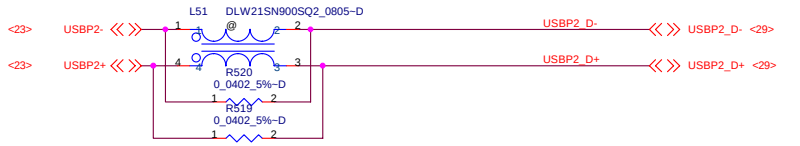
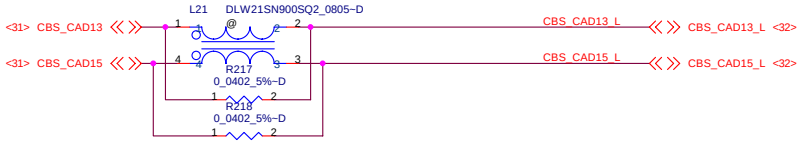
Compal Electronics, Inc.

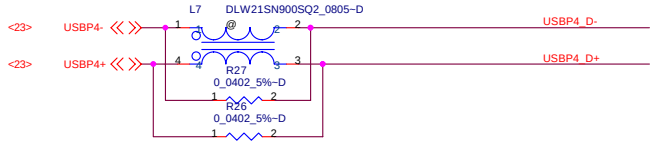
Title: AMP and PHONE JACK

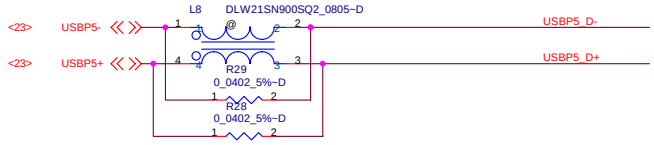
Size: | Document Number: TOBAGO-LA2151 | Rev: 0.6

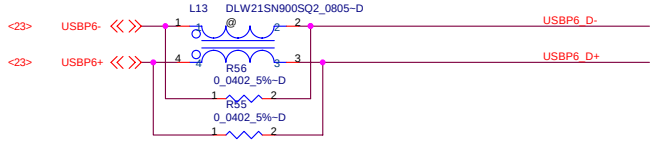
Date: Monday, October 18, 2004 | Sheet 27 of 51

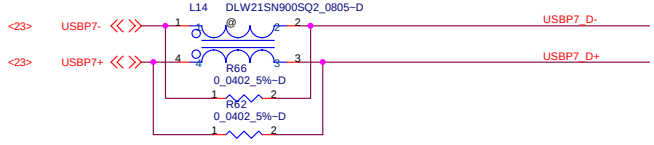


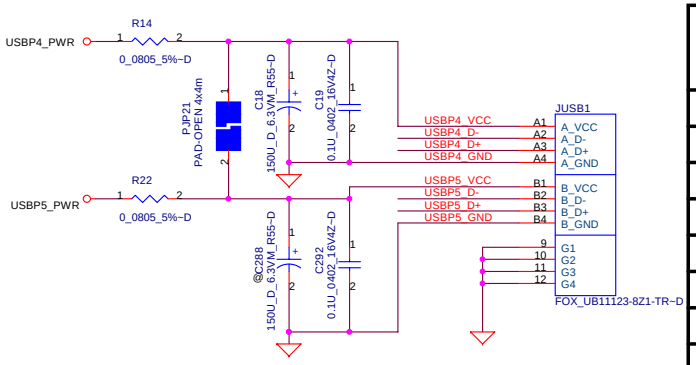




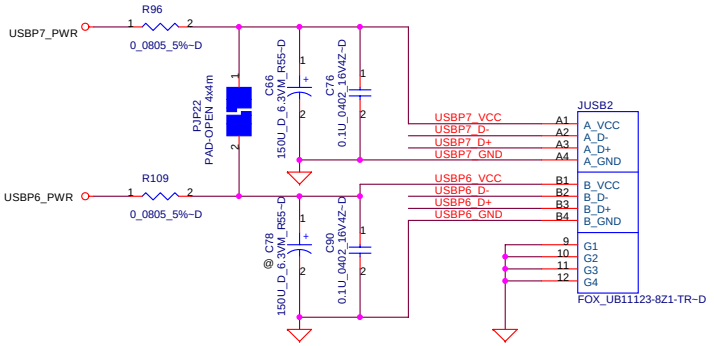


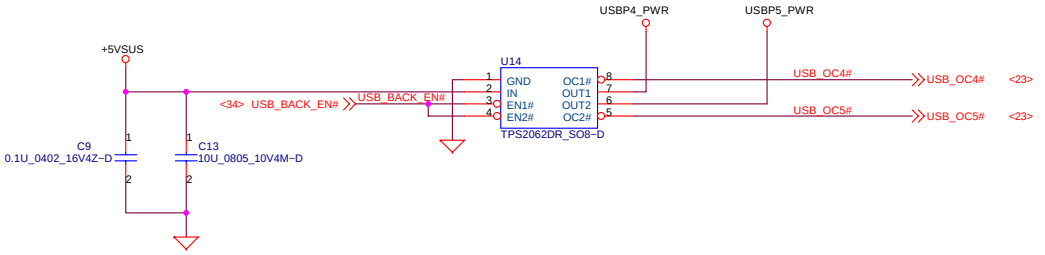


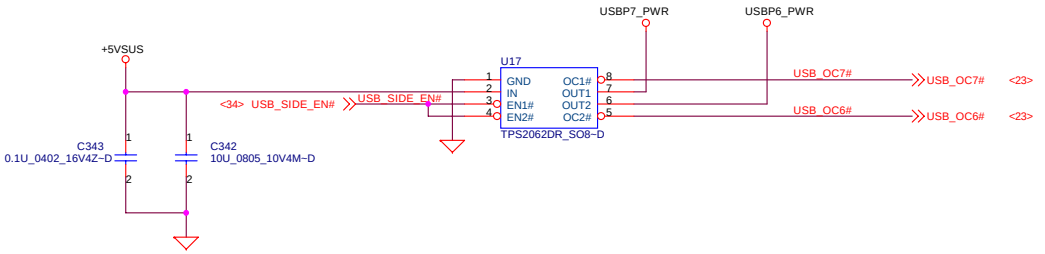




USB PORT#	DESTINATION
0	Reserve
1	Reserve
2	BlueTooth
3	NEW Connector
4	JUSB1(UP)
5	JUSB1(LOW)
6	JUSB2(LOW)
7	JUSB2(UP)







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Compal Electronics, Inc.

Title: USB 2.0 Port

Size: | Document Number: TOBAGO-LA2151 | Rev: 0.6

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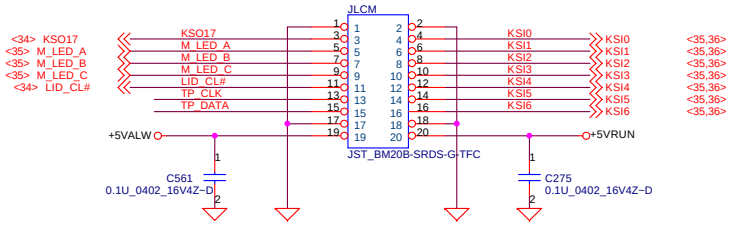
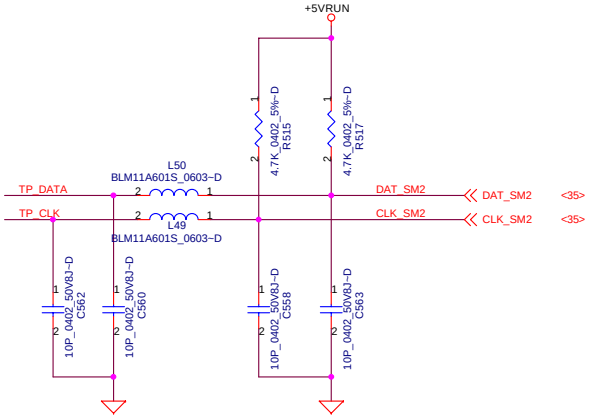
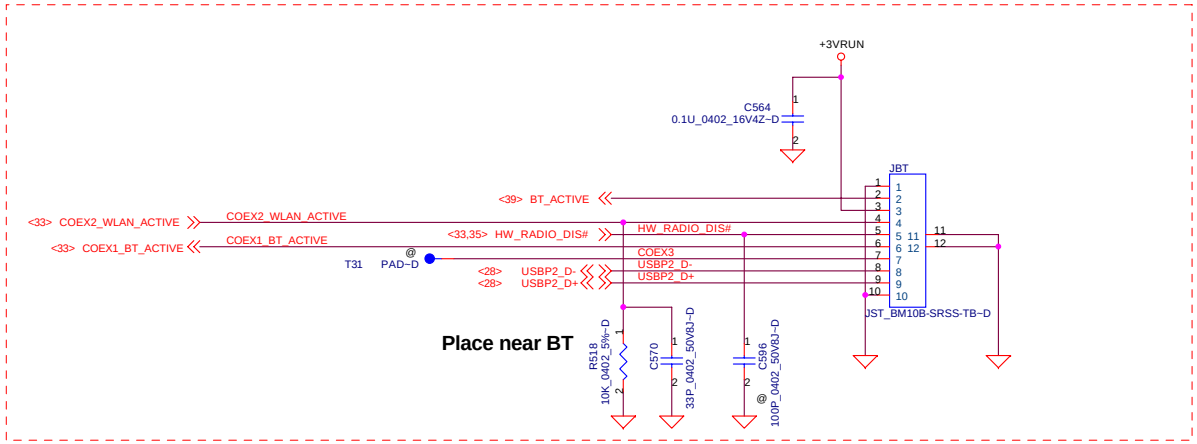
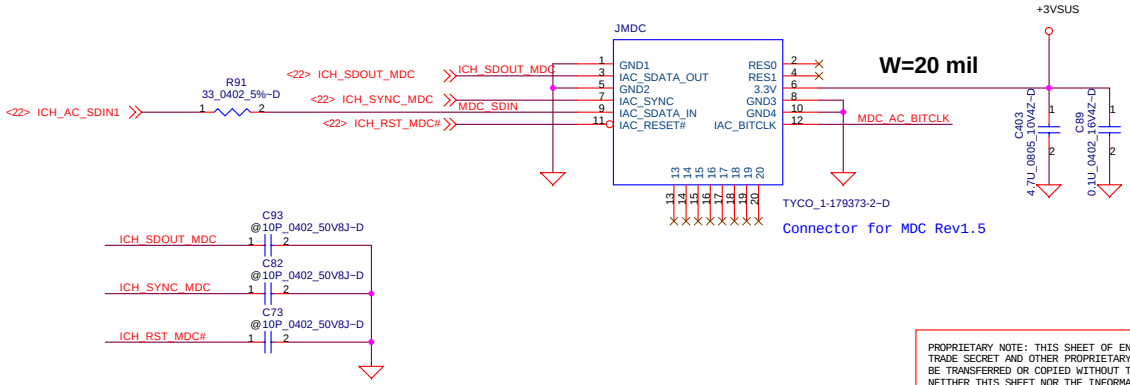
LCM & Direct play SW & T PAD

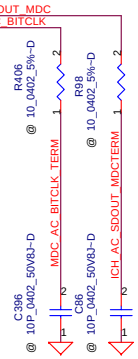




0402 Resistor reserve for ESD







New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12

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Compal Electronics, Inc.

Title: BT PORT and MDC

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WLAN	LOM	LED (JP28)
WLAN_LINK_80211A	LINK_LED100#	ORANGE (100M)
WLAN_LINK_10_LDE	LINK_LED10#	GREEN (10M)
WLAN_ACT_LED	ACTLED#	YELLOW
WLAN_LINK_80211A WLAN_LINK_10_LDE	NC	ORANGE/GREEN

	SPROM_DOUT	SPROM_CLK
1Kb	None	None
4Kb	10K Pullup	None
16Kb	None	10K Pullup

Broadcom
BCM 4401L

BCM4401_LQFP128

Place close to pin 57

Place close to pin 69

Place closely pin 118

Place close to LAN chip

AT93C46-10SI-2.7_SO8-D

TYCO_1368398-1-D

4 X 75 OHMS

25MHZ_20PF_1BG250000CK1A-D

BLM11A121S_0603-D

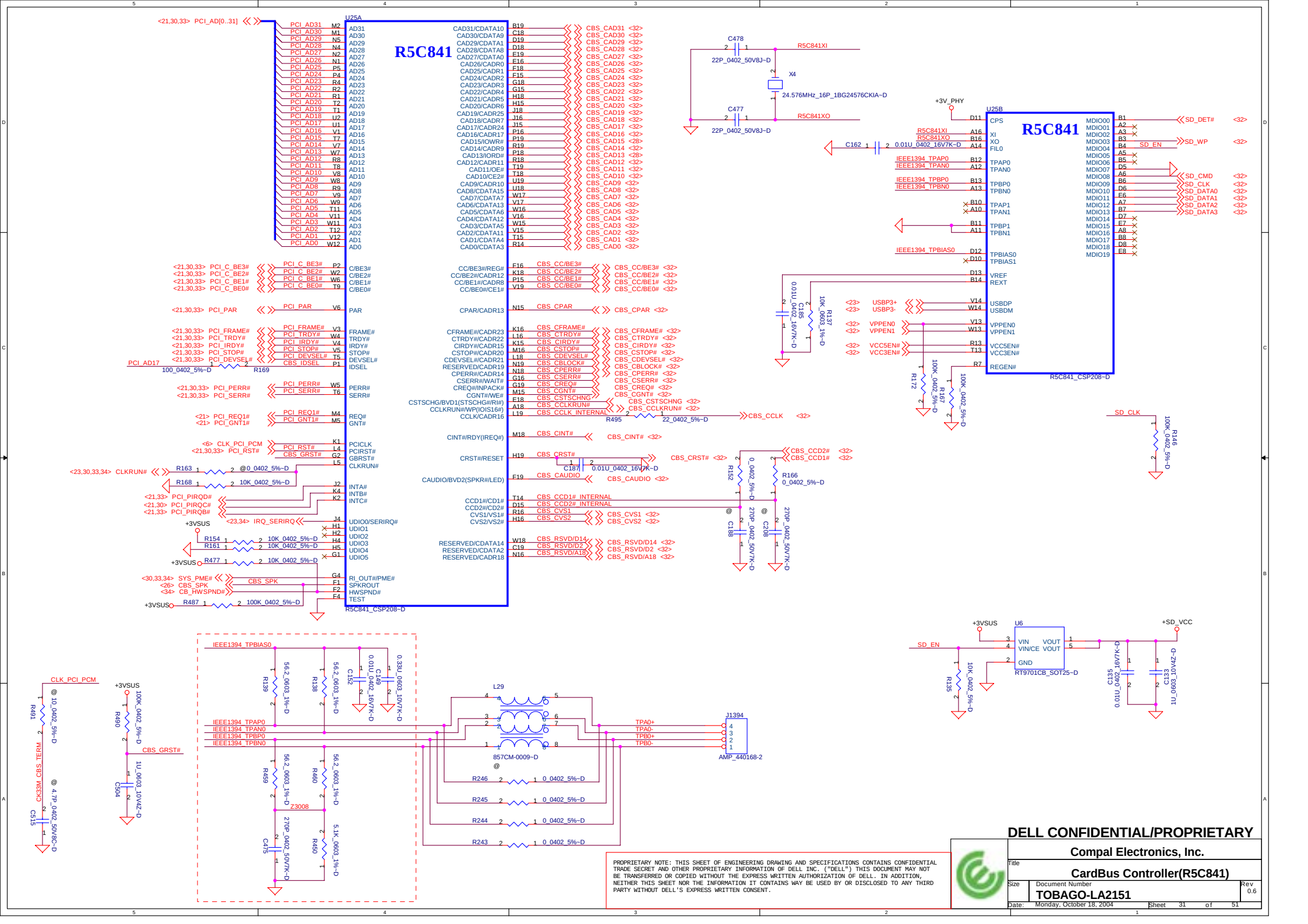
220n_LCN0603T-R22J-S_5%_0603-D

Compal Electronics, Inc.

Title: BROADCOM 4401L LAN

Size: | Document Number: TOBAGO-LA2151 | Rev: 0.6

Date: Monday, October 18, 2004 | Sheet 30 of 51



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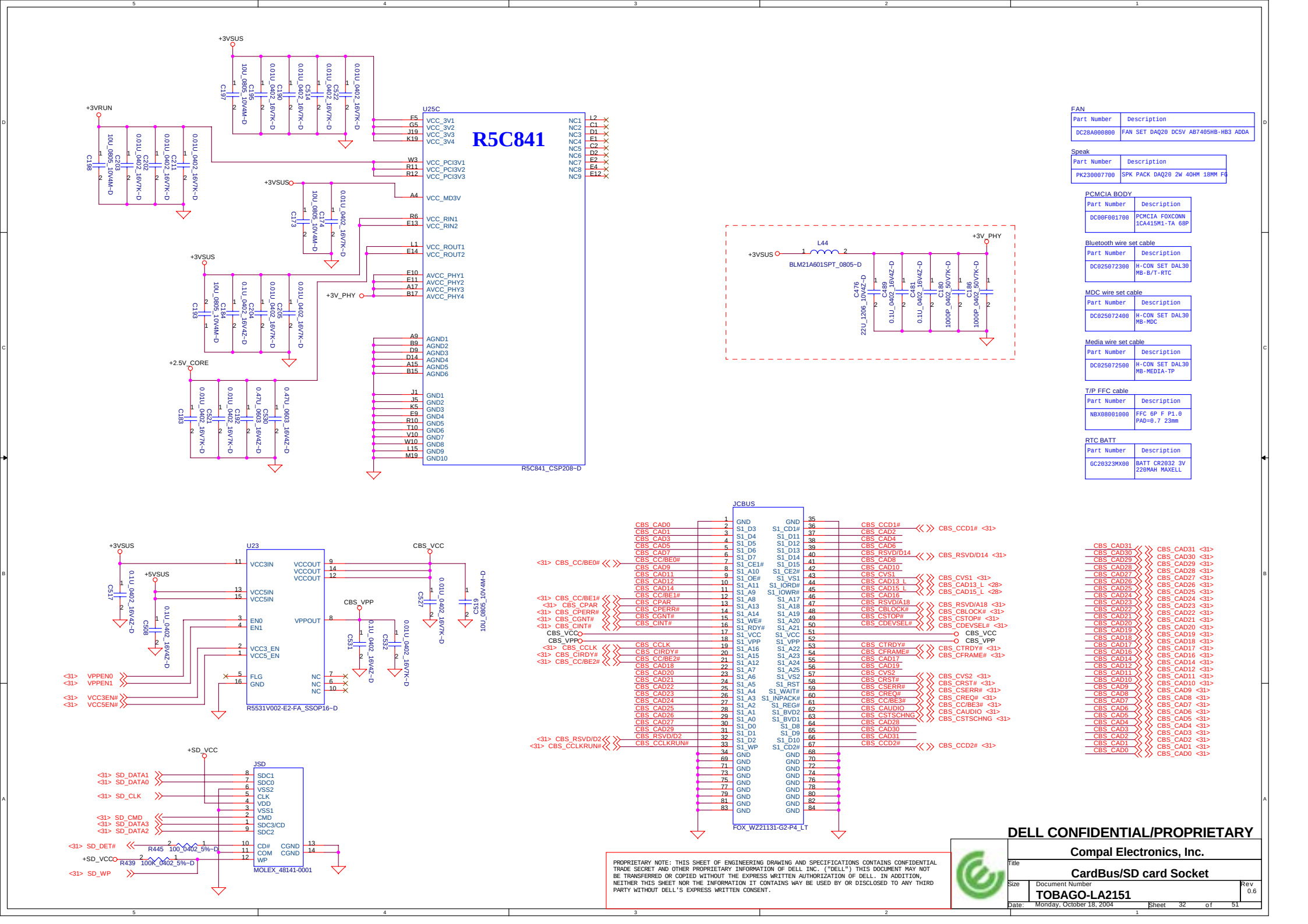

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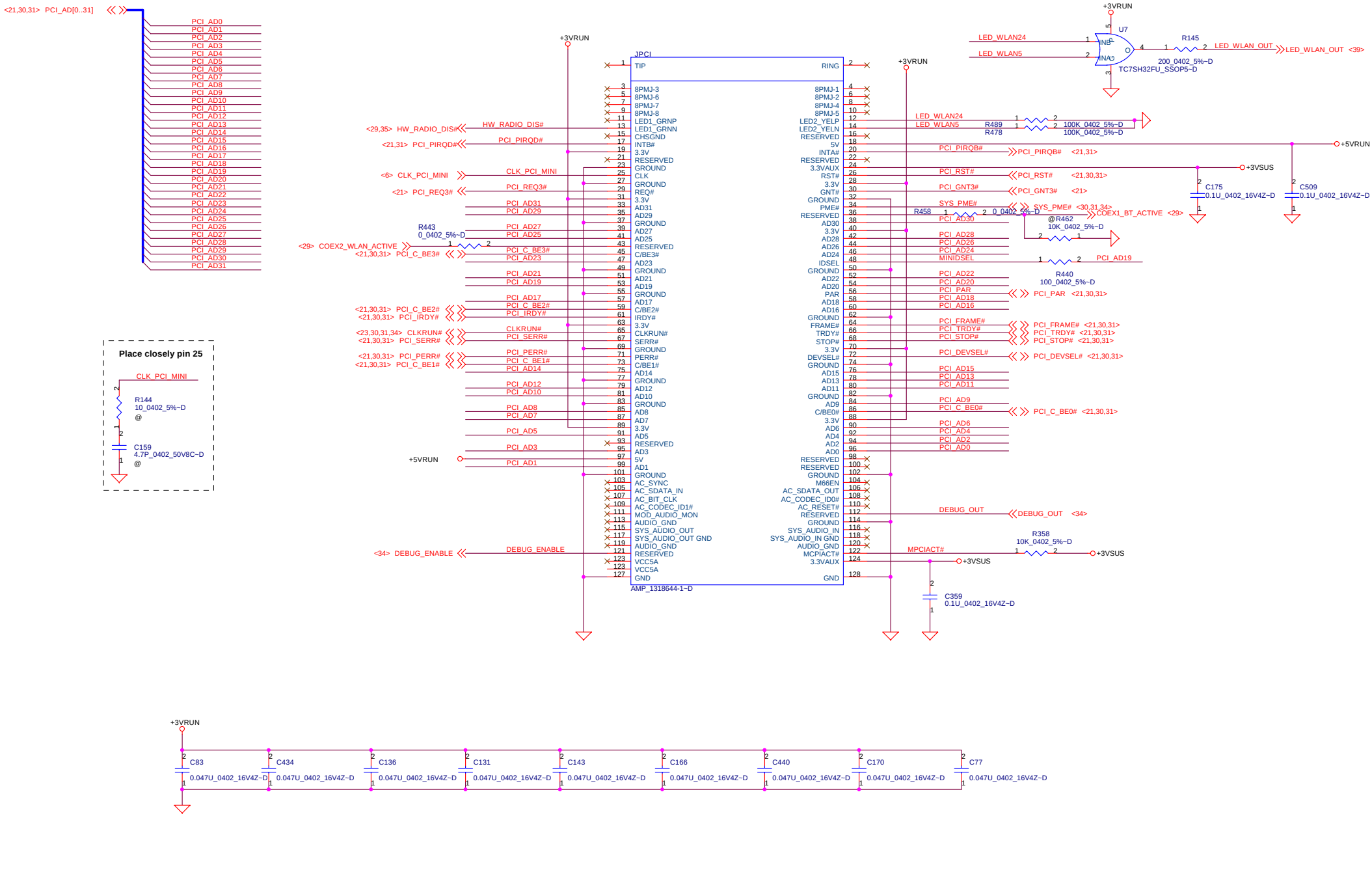

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Compal Electronics, Inc.	
Title	MINIPCI
Size	Document Number: TOBAGO-LA2151
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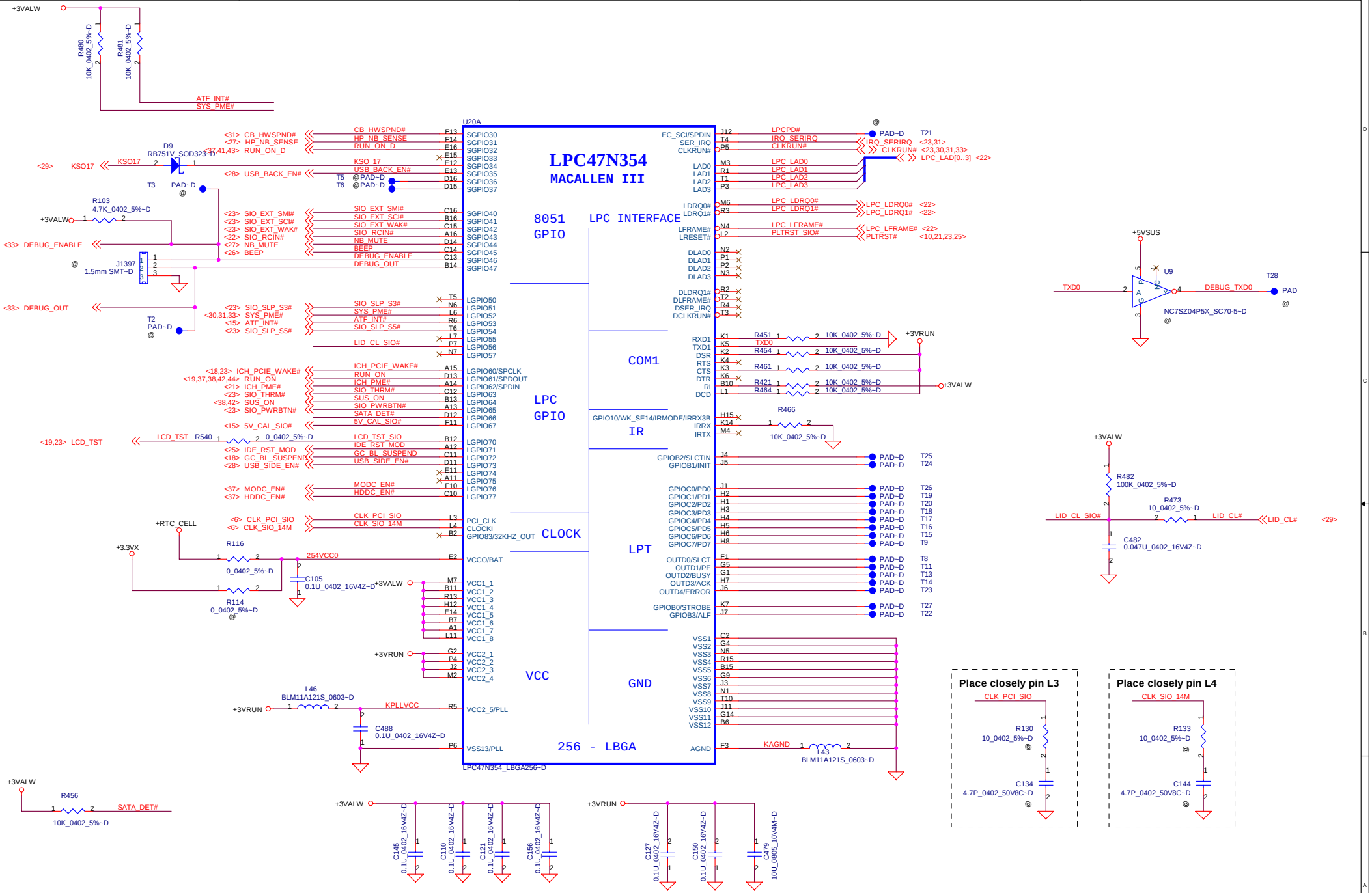
Date: Monday, October 18, 2004	Sheet 33 of 51


U20A
LPC47N354
MACALLEN III
8051 GPIO
LPC INTERFACE
LPC GPIO
COM1
IR
CLOCK
LPT
VCC
GND
256 - LBGA
LPC47N354_LBGA256-D
SGPIO30
SGPIO31
SGPIO32
SGPIO33
SGPIO34
SGPIO35
SGPIO36
SGPIO37
SGPIO40
SGPIO41
SGPIO42
SGPIO43
SGPIO44
SGPIO45
SGPIO46
SGPIO47
LGPIO50
LGPIO51
LGPIO52
LGPIO53
LGPIO54
LGPIO55
LGPIO56
LGPIO57
LGPIO60/SPCLK
LGPIO61/SPDOUT
LGPIO62/SPDIN
LGPIO63
LGPIO64
LGPIO65
LGPIO66
LGPIO67
LGPIO70
LGPIO71
LGPIO72
LGPIO73
LGPIO74
LGPIO75
LGPIO76
LGPIO77
PCI_CLK
CLOCKI
GPIO83/32KHZ_OUT
VCCO/BAT
VCC1_1
VCC1_2
VCC1_3
VCC1_4
VCC1_5
VCC1_6
VCC1_7
VCC1_8
VCC2_1
VCC2_2
VCC2_3
VCC2_4
VCC2_5/PLL
VSS13/PLL
EC_SCI/SPDIN
SER_IRQ
CLKRUN#
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#
LFRAME#
LRESET#
DLAD0
DLAD1
DLAD2
DLAD3
DLDRQ1#
DLFRAME#
DSER_IRQ
DCLKRUN#
RXD1
TXD1
DSR
RTS
CTS
DTR
RI
DCD
GPIOB2/SLCTIN
GPIOB1/INIT
GPIOC0/PD0
GPIOC1/PD1
GPIOC2/PD2
GPIOC3/PD3
GPIOC4/PD4
GPIOC5/PD5
GPIOC6/PD6
GPIOC7/PD7
OUTD0/SLCT
OUTD1/PE
OUTD2/BUSY
OUTD3/ACK
OUTD4/ERROR
GPIOB0/STROBE
GPIOB3/ALF
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
AGND
GPIO10/WK_SE14/IRMODE/IRRX3B
IRRX
IRTX
+3VALW
+3VRUN
+3.3VX
+RTC_CELL
+5VSUS
Place closely pin L3
Place closely pin L4
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Compal Electronics, Inc.
Title
SIO (1/2)
Size
Document Number
TOBAGO-LA2151
Rev
0.6
Date: Monday, October 18, 2004
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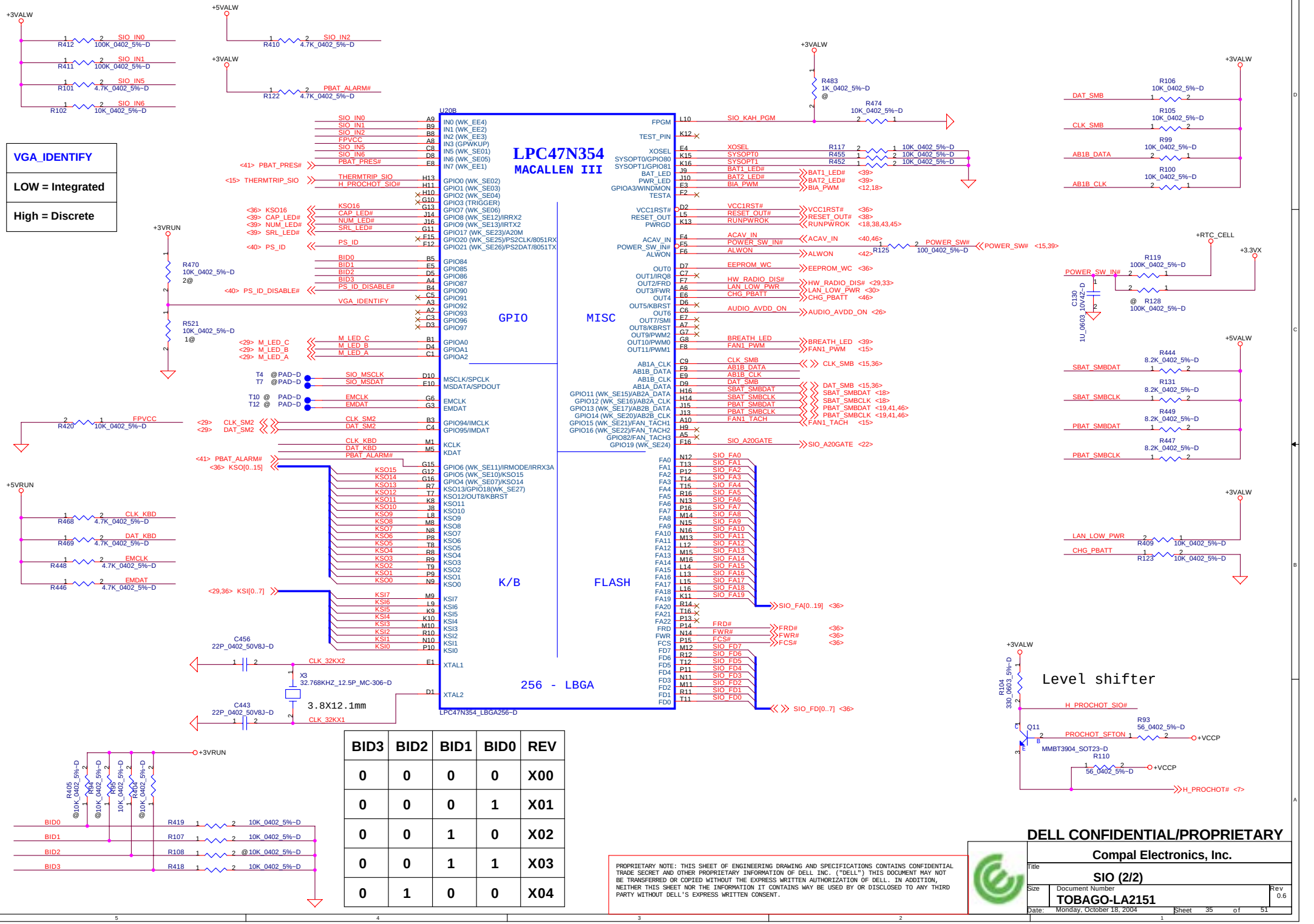
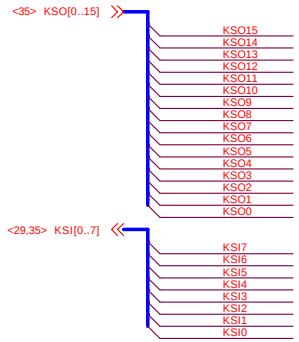
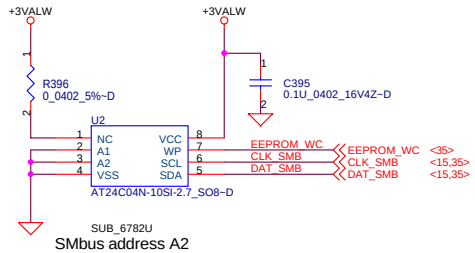
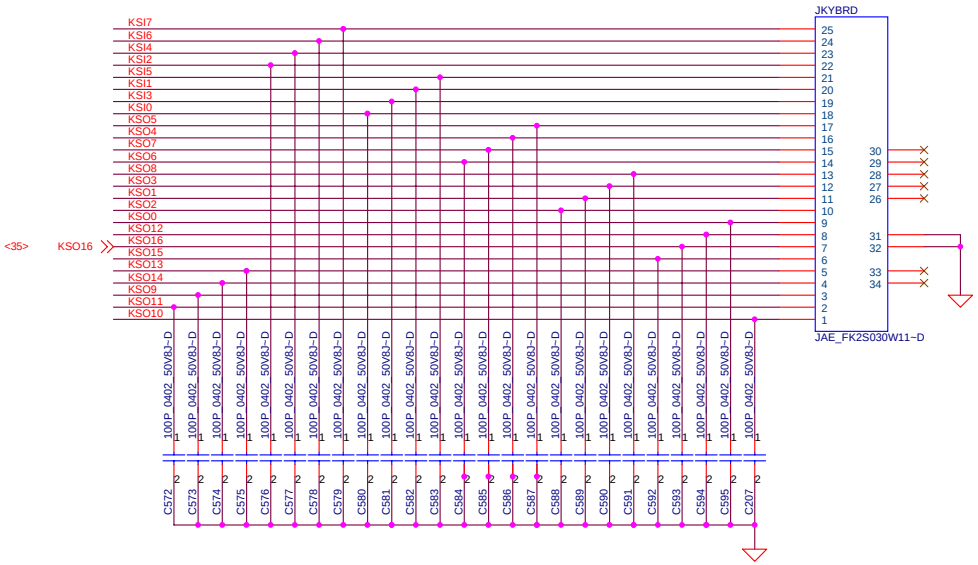
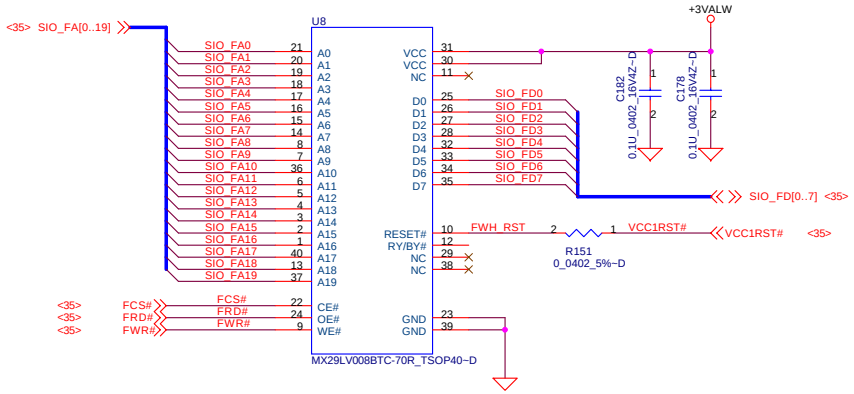


BID3	BID2	BID1	BID0	REV
0	0	0	0	X00
0	0	0	1	X01
0	0	1	0	X02
0	0	1	1	X03
0	1	0	0	X04









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Compal Electronics, Inc.

Title: INT KB

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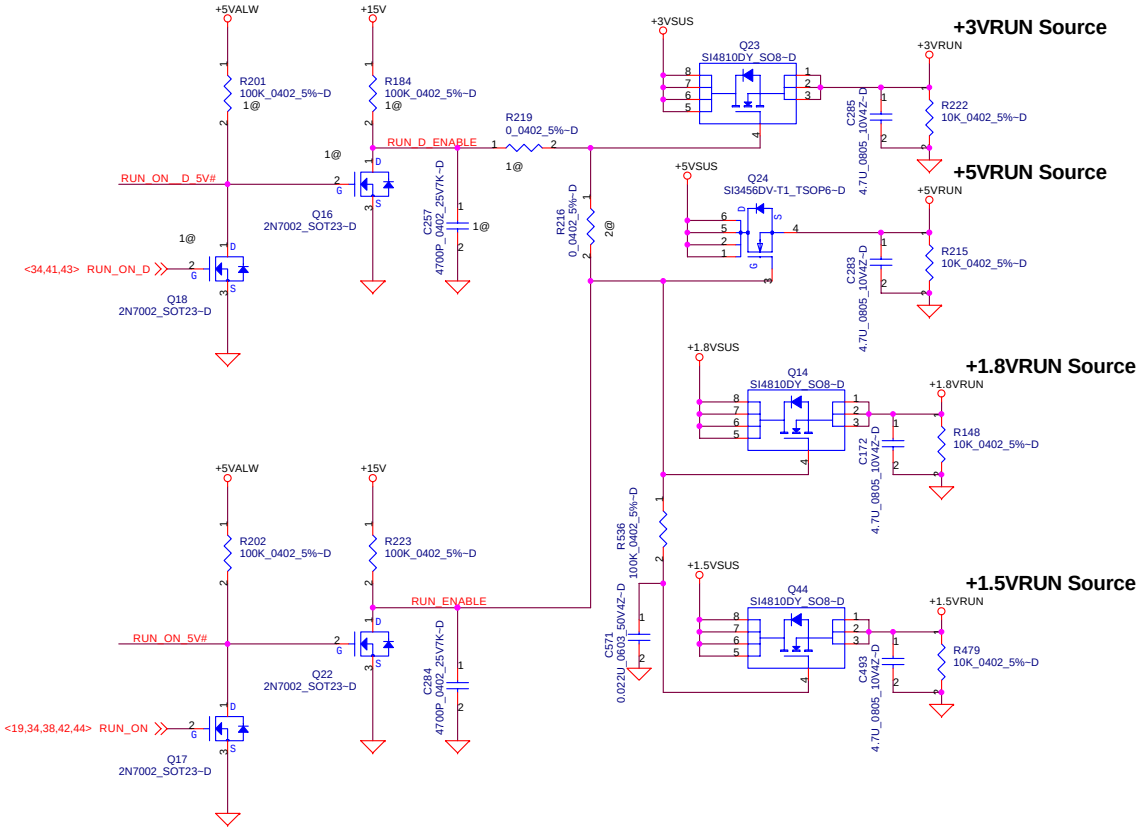
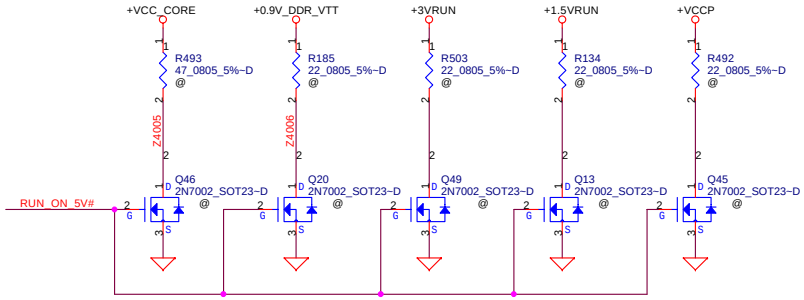
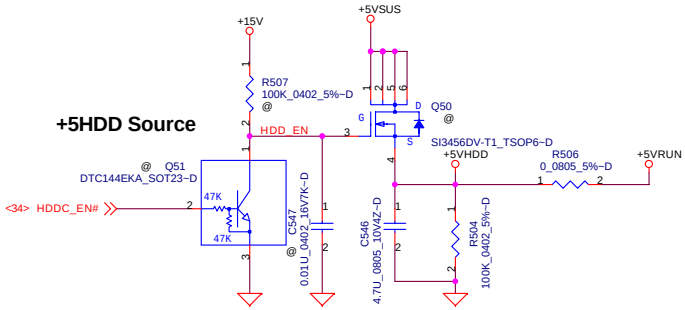
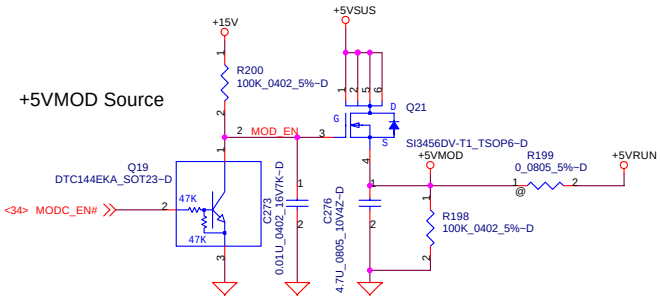
Run Planes Enable









Compal Electronics, Inc.	
Title	POWER CONTROL
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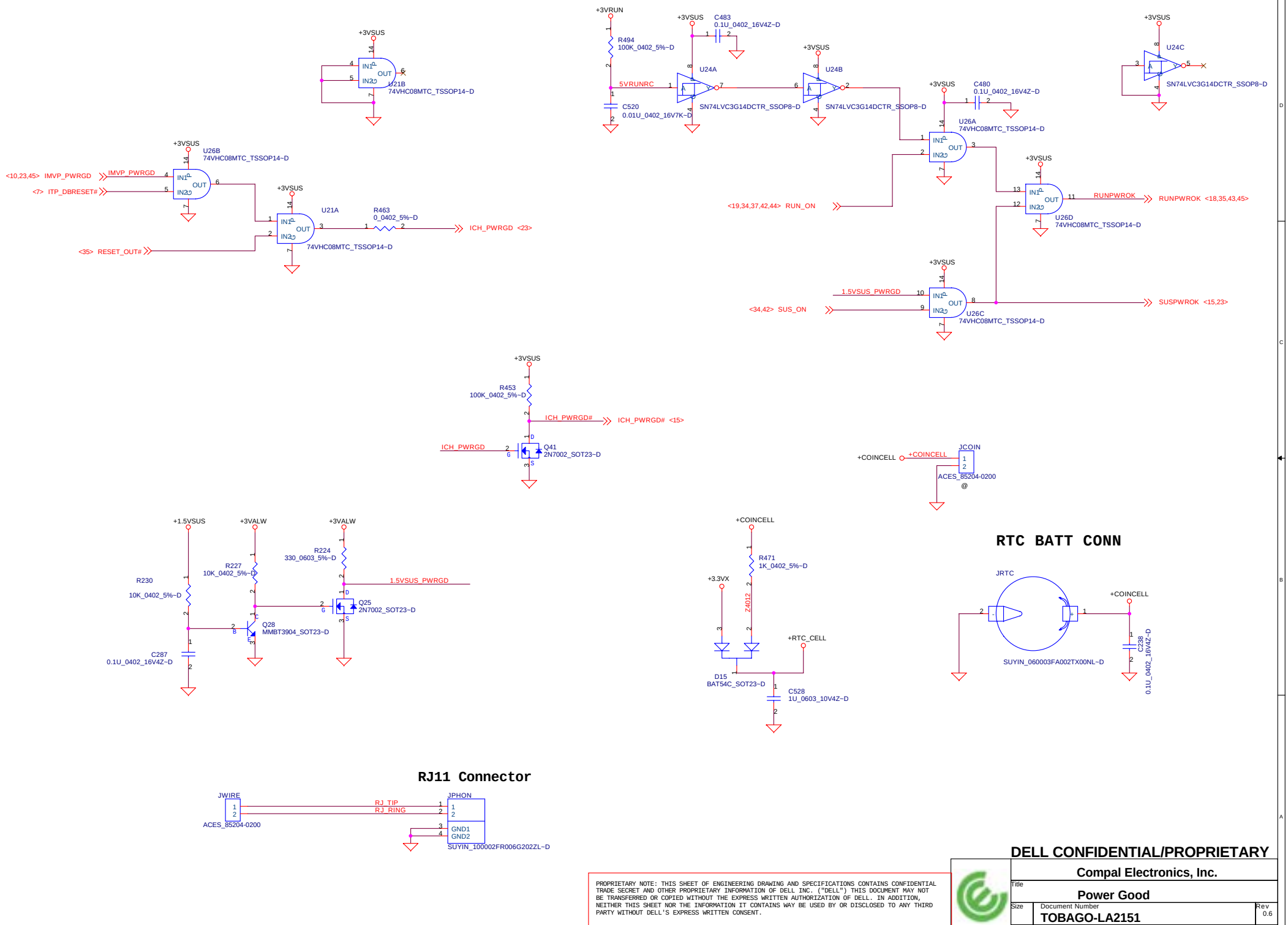

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Compal Electronics, Inc.

Title: Power Good

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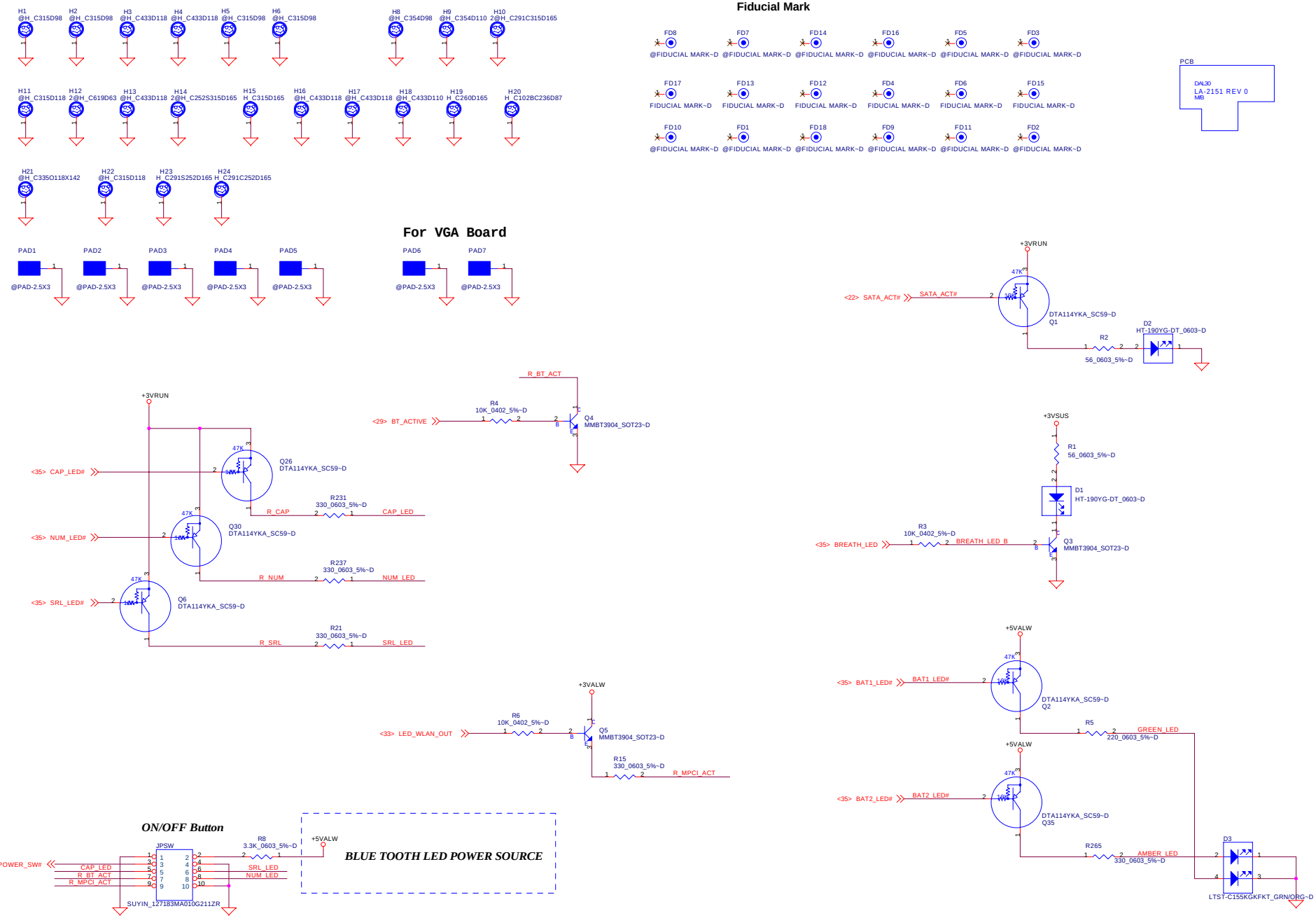

Compal Electronics, Inc.

Title: PAD and Standoff

Size | Document Number: TOBAGO-LA2151 | Rev: 0.6

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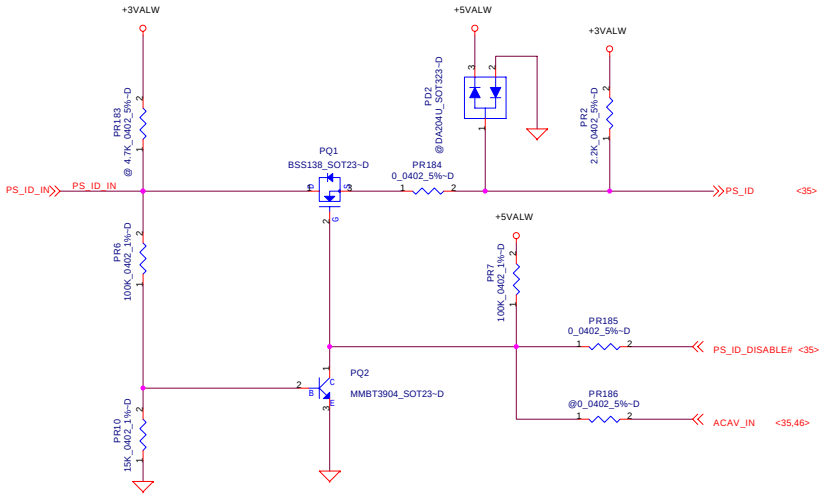

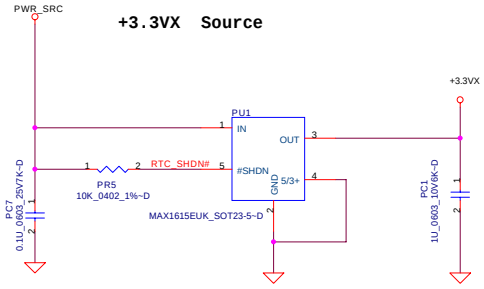

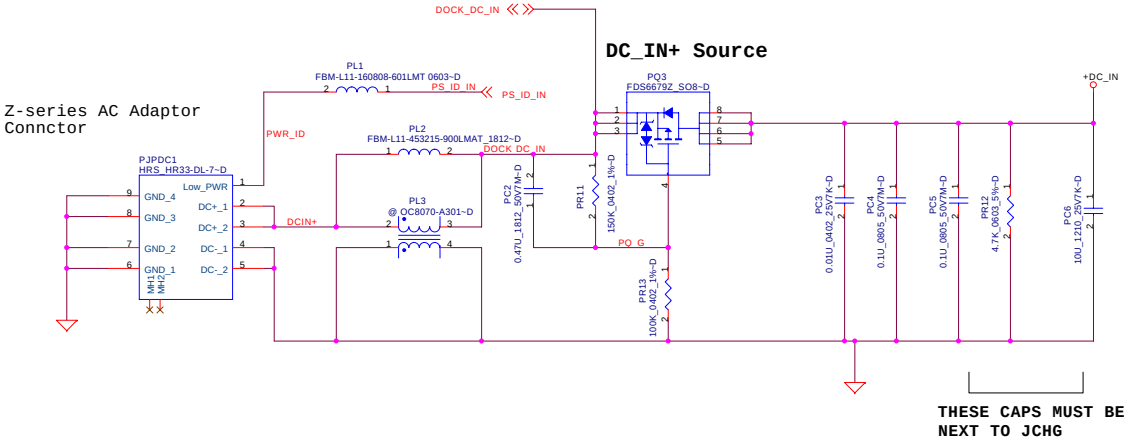

Compal Electronics, Inc.

Title: +DCIN

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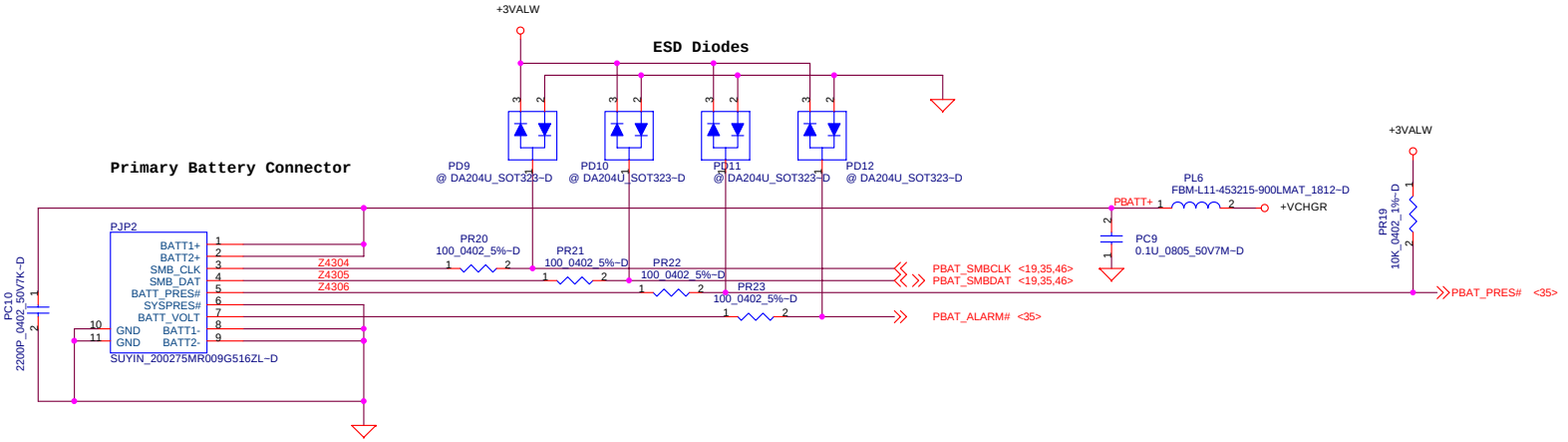
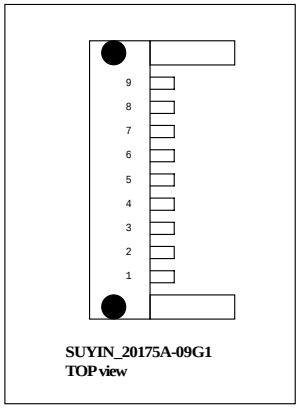
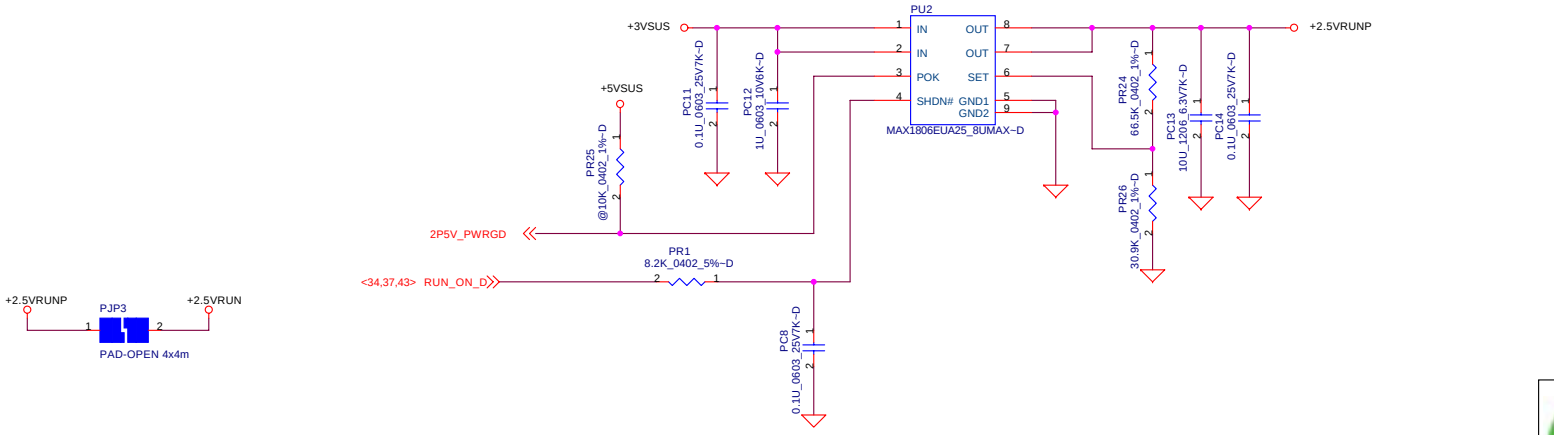




+2.5VRUN

R1=R2* (Vo/ 0.8 -1), R2:25K~100K.



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Compal Electronics, Inc.

Title: Battery Conn./+2.5V

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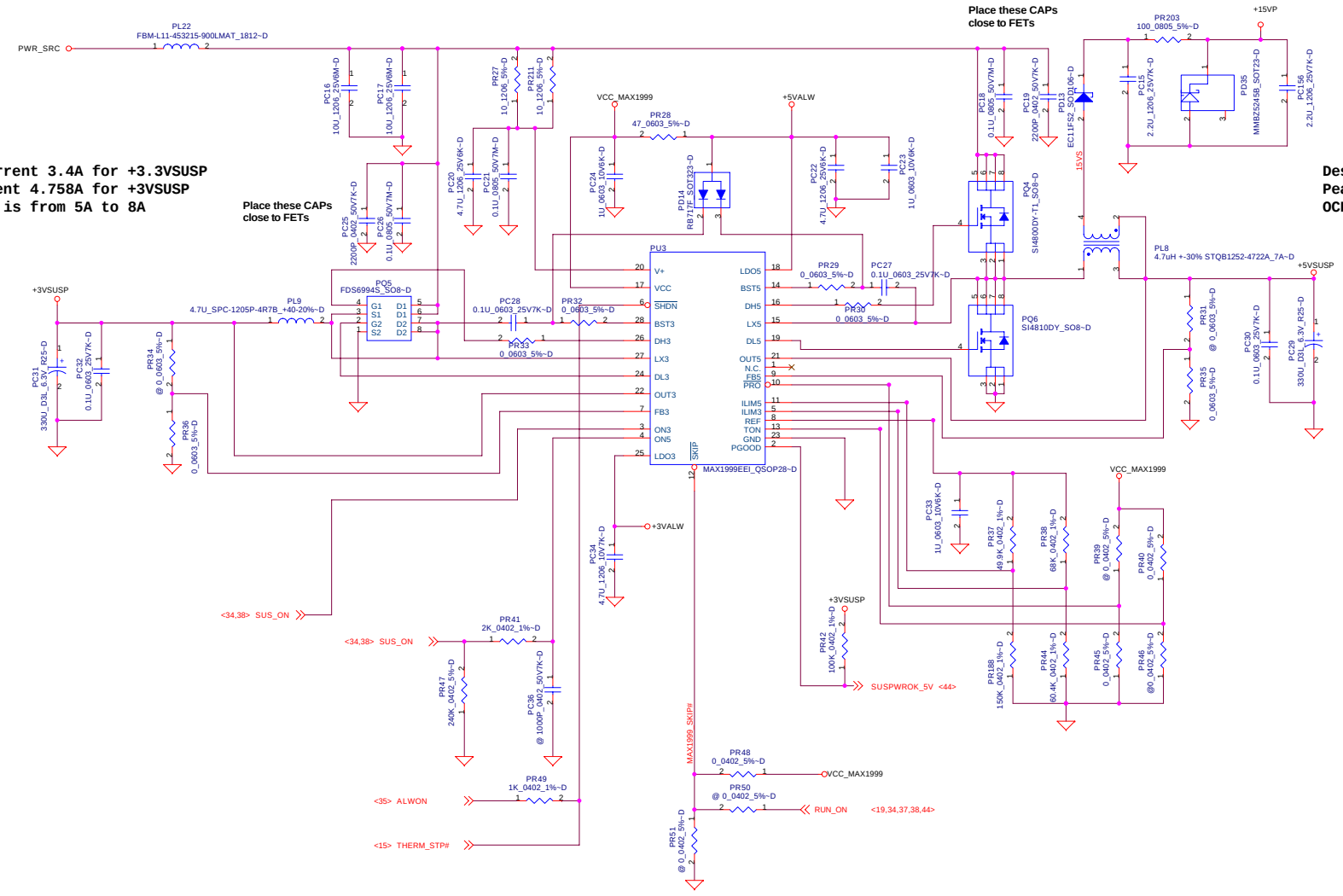
DC/DC +3V/ +5V/ +15V



Design current 3.4A for +3.3VSUSP
Peak current 4.758A for +3VSUSP
OCP point is from 5A to 8A

Design current 4A for +5VSUS
Peak current 5.7A for +5VSUSP
OCP point is from 6A to 9A

Compal Electronics, Inc.

Title: +3.3V/+5V/+15V

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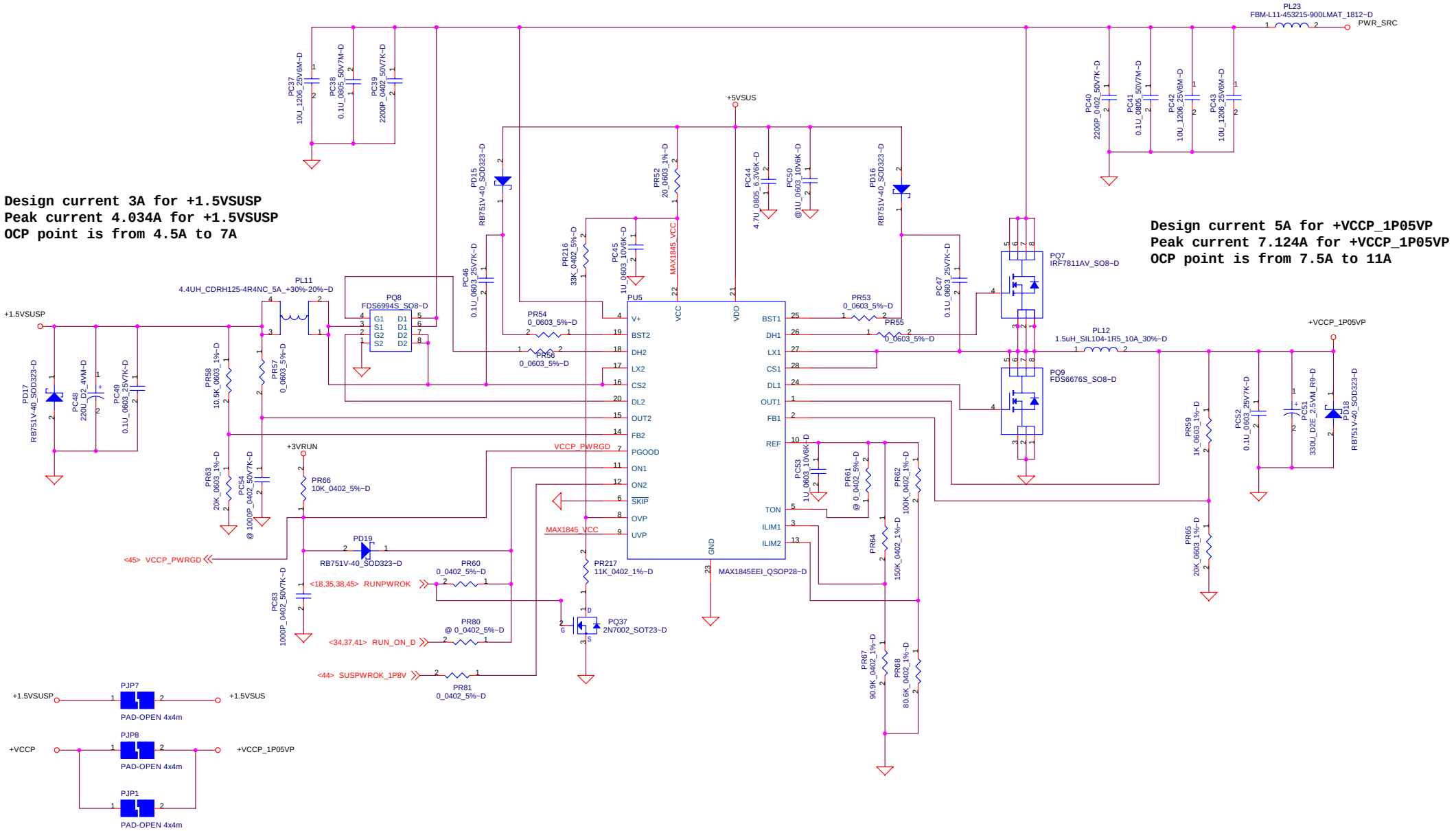
+1.5VSUSP / +VCCP_1P05VP



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Compal Electronics, Inc.

Title: +1.5VSUSP /+VCCP_1P05VP

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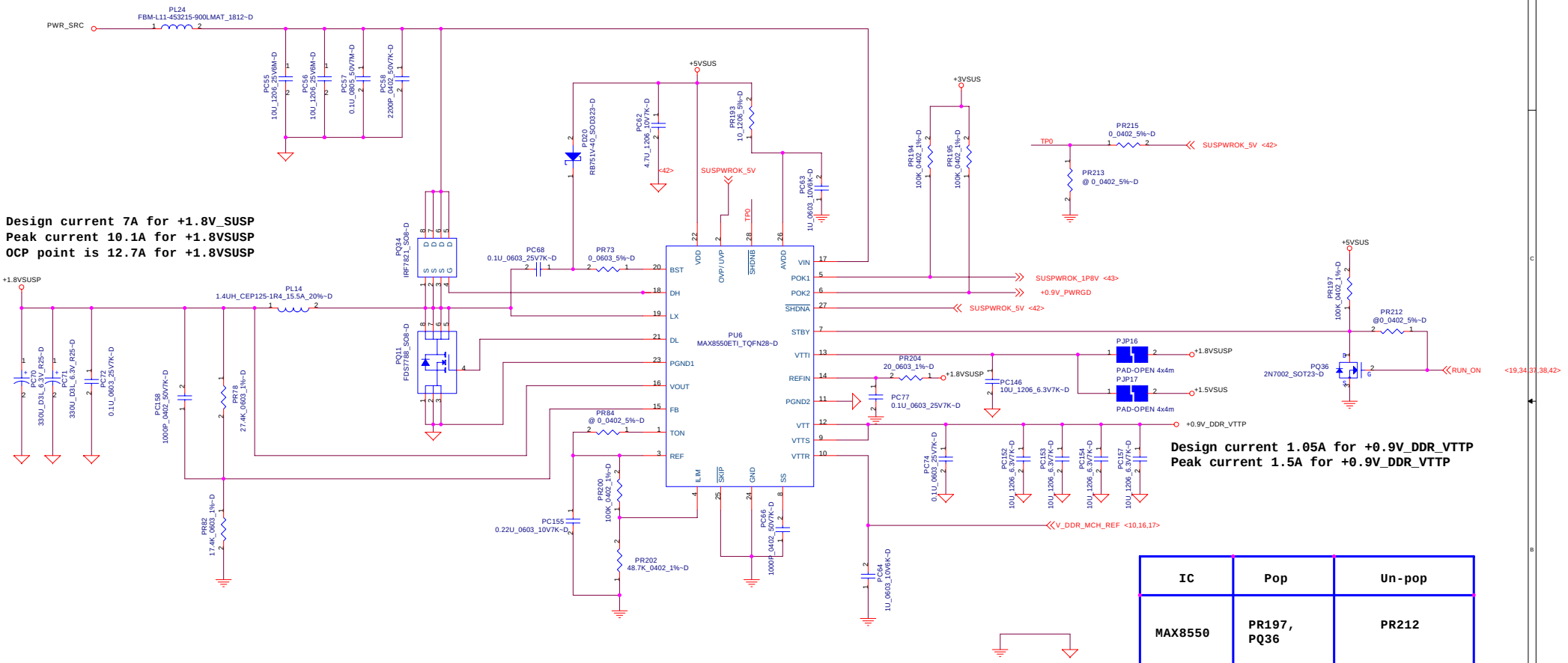
+1.8VSUSP/ +0.9V_DDR_VTT

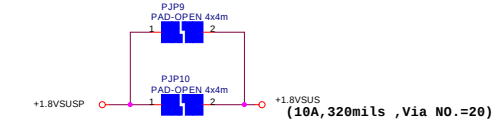
DDR2 Termination

Design current 7A for +1.8V_SUSP
Peak current 10.1A for +1.8VSUSP
OCP point is 12.7A for +1.8VSUSP



Design current 1.05A for +0.9V_DDR_VTTP
Peak current 1.5A for +0.9V_DDR_VTTP

IC	Pop	Un-pop
MAX8550	PR197, PQ36	PR212
MAX8550A	PR212	PR197, PQ36



(10A,320mils ,Via NO.=20)

(3A,200mils ,Via NO.=6)

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Compal Electronics, Inc.
Title: +1.8VSUSP/ +0.9V_DDR_VT
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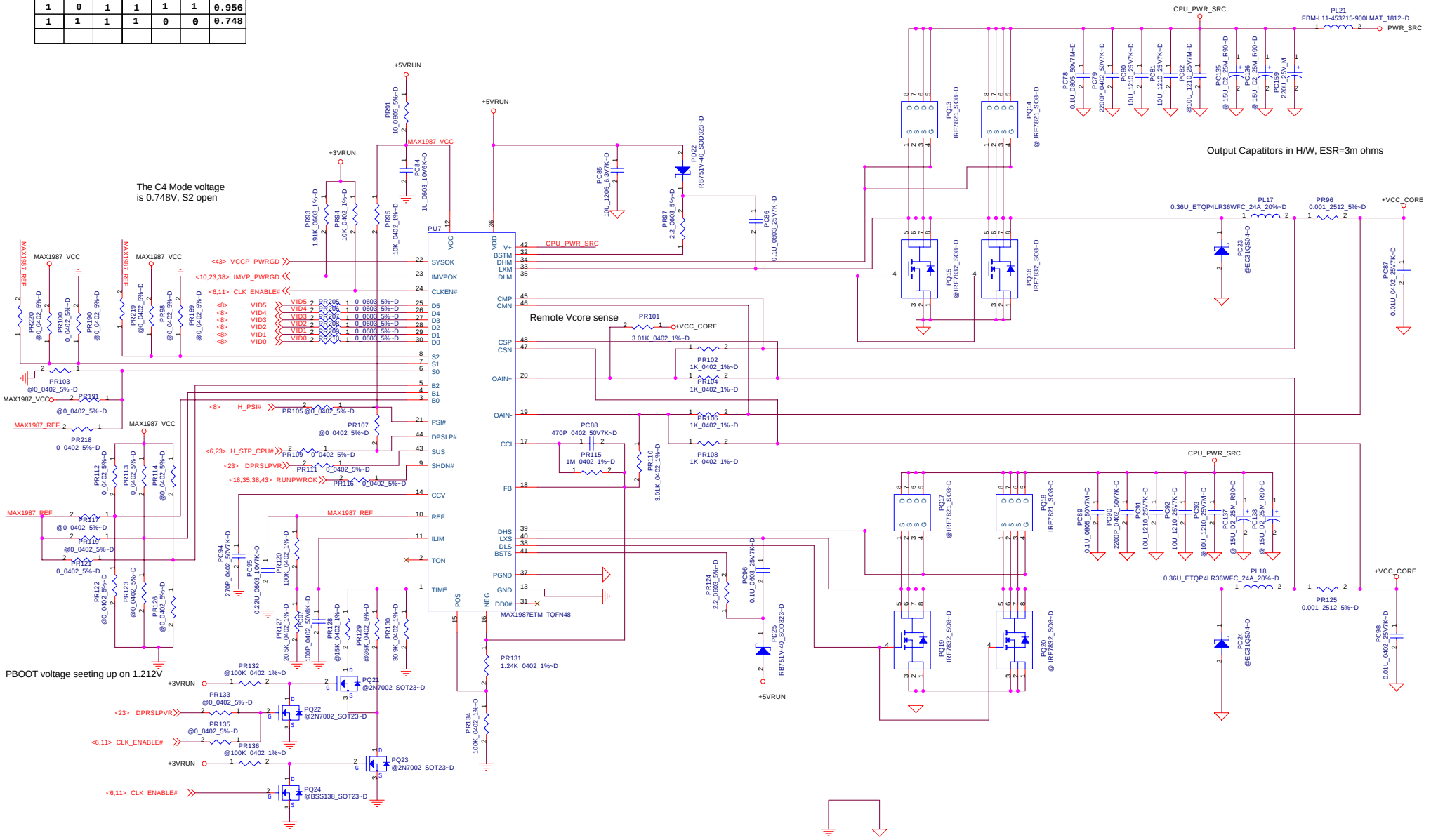
V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	1	1	1	0	1.484
0	1	1	0	0	1	1.308
1	0	1	1	1	1	0.956
1	1	1	1	0	0	0.748



Change PR130:30.9k. Delete PR128/PR129/PR132/PR133/PR136/PQ21/PQ22/PQ23/PQ24 for BANIAS and DOTHAN
PR128/PR129/PR132/PR133/PR136/PQ21/PQ22/PQ23/PQ24 are only for YONAH CPU.
TRANSITION TIMING:
(a): START-UP and SHUTDOWN(SUS=LOW,RUNPWROK=LOW):2mV/us
(b): ENTER SUSPEND (SUS=HIGH,RUNPWROK=HIGH): 8.6mV/us
(c): EXIT SUSPEND (SUS=LOW, RUNPWROK=HIGH): 24.7mV/us

Compal Electronics, Inc.

Title: +VCORE

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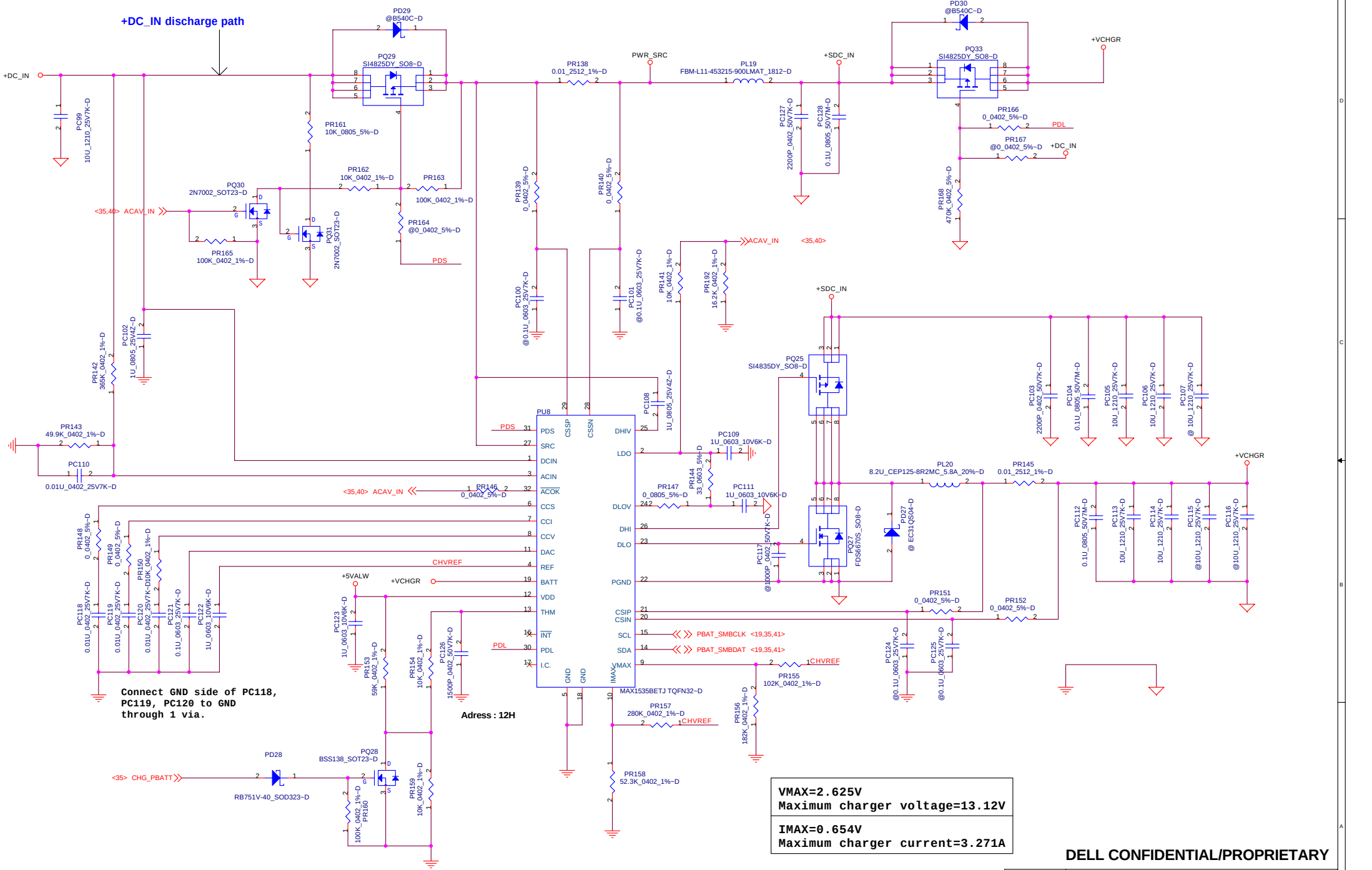

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Compal Electronics, Inc.	
Title	Charger
Size	Document Number: TOBAGO-LA2151
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	ALL	H/W	01/19	Roger	Rename component location for manufacture	Update schematic and board file component reference	0.1
2	30	H/W	01/19	Roger	R2151 tie +3VLAN to GND via LAN transformer	Change R1251 (0_0402_5%~D) to C34(1000P_0402_50V7K~D)	0.1
3	39	H/W	01/19	Roger	The light of WLAN and Blue tooth LED too dim	Change R8, R15 from 330 ohm to 56 ohm	0.1
4	34	H/W	01/19	Roger	Add the COM port debug circuit	Add U184 for COM port debug	0.1
5	36	H/W	01/28	Roger	Rotate the Keyboard connector 180 degree	Reconnect keyboard signals to CN1,CN2,CN3,CN4,CN5,C207 for layout smoothly	0.1
6	36	H/W	01/30	Roger	Keep more spacing for VGA thermal solution	Delete JP3 debug port to save spacing for ROM part placement	0.1
7	12	H/W	02/03	Roger	+2.5VRUN is margin for 2N7002	Change Q7,Q27,Q31,Q33 gate voltage from +2.5VRUN to +3VRUN	0.1
8	06	H/W	02/04	Roger	Change R330 and R354 to 0 ohms per Intel review.	Change R330 and R354 from 1K to 0 ohms	0.1
9	38	H/W	02/04	Roger	Resolves the issue where 1.5VSUS_PWRGD goes high before +1.5VSUS	Change R230 from 330 to 10K ohm and R227 from 1K to 10K ohms	0.1
10	37	H/W	02/09	Roger	Resolves the issue where +1.5VRUN drop 100 mV from +1.5VSUS to +1.5VRUN.	Change Q44 from SI3456 to SI4810 that have lower Rds on.	0.1
11	18	H/W	02/09	Roger	Add a bulk cap for G_PWR_SRC	Add C569 for G_PWR_SRC placement near JVID	0.1
12	39	H/W	02/09	Roger	BAT1_LED# should drive the GREEN LED, BAT2_LED# should drive the ORANGE LED	Change R5 pin 2 connect to D3 pin4, R265 pin2 connect to D3 pin2	0.1
13	21	H/W	02/09	Roger	Follow X01 Gerber Gate Checklist item 11	Change R328 from 0 ohm to 1K ohm and add note "Pop resistor to boot from PCI".	0.1
14	38	H/W	02/09	Roger	Follow X01 Gerber Gate Checklist item 12, ICH_PWRGD circuit match Laguna	Remove R470 and no connect U21B, RESET_OUT# connector to U21A pin 2.	0.1
15	35	H/W	02/09	Roger	Change Board ID to X01	Depop R419 and populate R405	0.1
16	35	H/W	02/09	Roger	System will auto power on when AC plug in if RTC coin battery not implement	Change C130 from 1U to 100P to reduce POWER_SW_IN# rising time.	0.1
17	06	H/W	02/10	Roger	Reserve SSC clock for internal graphic for clock generator ICS954206	96MHz SSC clock connect to U16 pin 17,18. Add the serie damping R524, R525, pull down resistor R522, R523.	0.1
18	ALL	H/W	02/11	Roger	Change connector name to match the naming rule	Change JP5 to JMOD, JP6 to JWIRE, JP2 to JPSW, JP1 to JLVDS, JP4 to JCRT	0.1
19	23	H/W	02/16	Roger	+1.5VRUN leakage issue at system into S3 status	ICH6M GPIO24 connect to SIO_EXT_WAK# for option the GPIO power plane	0.1
20	39	ME	02/17	Roger	Change screw hole size for system assembly	H15 change diameter form 3 mm to 4.2 mm, H18 change diameter from 3 mm to 2.8 mm	0.1
21	34	H/W	02/22	Roger	Change the power source from +RTC_CELL to +3.3VX	Depop R116 and pop R114, Depop R119 and pop R128	0.1
22	35	H/W	02/22	Roger	Auto power on when AC plug in issue will be using the BIOS fix	C130 change from 100P 0603 to 1U 0603	0.1
23	39	H/W	03/12	Roger	LED_WLAN_OUT should drive green LED	Change R15 from 56 ohms to 330 ohms	0.1
24	29,39	H/W	03/12	Roger	Blue tooth and meida blue LED trun on voltage Vf is 2.7 to 3.9V. +3.3V have risk don't trun on LED.	Change Q4 pin 1 and JLCM pin19 power source from +3VALW to +5VALW	0.1

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	35	H/W	03/17	Roger	SIO SM Bus EA measure issue for rising and falling time	R131, R444, R447, R449 change from 22K ohms to 8.2K ohms	0.3
26	6	H/W	03/17	Roger	ICH SM Bus EA measure issue for rising and falling time	R270, R275 change from 100K ohms to 2.2K ohms	0.3
27	19	H/W	03/17	Roger	LCDVDD component unnecessary for external board	Depop Q8, Q9,Q10, Q37, R35, R54, R263, R272, C29, C315 on external board and pop on internal board	0.3
28	13	H/W	03/18	Roger	Remove CRT, LVDS, TV DAC power beads and caps	Depop L9, L10, L11, L25, L26, L24, C24, C291, C293, C22, C298, C299, C23, C323, C310, C297, C314, C331, C322, C37, C35, C305, C306, C36, C304 on external board and pop on internal board	0.3
29	31	H/W	03/19	Roger	Card bus EA measure CBS_CCLK rising and falling failure issue	R495 change from 47 ohms to 22 ohms	0.3
30	27	H/W	03/23	Roger	ME change audio jacks to combined jack	Change JAUDIO symbol to combined two jacks, delete JHP	0.3
31	15	H/W	03/25	Roger	PT layout issue list item 6, consistent with other platforms	Change U15 pin 10 power source from +3.3VX to +RTC_CELL	0.3
32	26	H/W	03/25	Roger	Layout issue list item 16, pop issue and the static noise during post and idle in Windows	Add a non-popped inverter U30 add a 0 ohm R528 around the inverter	0.3
33	25	H/W	03/25	Roger	Issue list item 8, connect UART interface to ICH GPIO for debug	Connect U11 pin 45 (UAO) to ICH6 pin AC18 (GPIO34). Connect U11 pin 43 (UAI) to ICH6 pin AF20 (GPIO33)	0.3
34	26	H/W	03/25	Roger	Issue list item 11, allow the capability to disable the line in option	Connect a no popped 0 ohm R529 from LINE_IN_L to 9750_PHONE. Connect a no popped 0 ohm R530 from LINE_IN_R to 9750_PHONE	0.3
35	39	H/W	03/25	Roger	Issue list item 12, blue LED to dim	LED & R58 move to collection side of BJT. Q4 pin 3 connect to GND, JPSW pin 2 change to connect +5VALW.	0.3
36	18	H/W	03/25	Roger	Issue list item 9, C569 not require fo now	Add non-popped symbol for C569	0.3
37	29	H/W	03/26	Roger	EMI request add a cap place near R518 for blue tooth	Add C570 (33P_0402_50V8J~D)	0.3
38	34	H/W	03/28	Roger	Issue list item 7, swap SIO_PWRBTN# and ICH_PCIE_WAKE# to fix WOL issue on Laguna	Swap SIO_PWRBTN# (U20 pin A15) and ICH_PCIE_WAKE# (U20 pin A13)	0.3
39	35	H/W	03/28	Roger	Change board ID to (0010) for X02 board	Pop R94, R419 and non-popped R107, R405	0.3
40	6	H/W	03/28	Roger	Reserved clock gernerator pin53 for 14.318 MHz for ICS 954206	Add a 12.1 ohms series resistor R531 to U16 pin 53 and connect to CLK_CODEC_14M. Isolation resistor R531 connect to CLKSEL0	0.3
41	6	H/W	04/01	Roger	TV out B/W issue on UMA configuration	Pop C329 and C333 with 27P to fine tune the crystal frequency and clock sequence	0.3
42	15	H/W	04/02	Roger	FAN RPM detect issue	Change C209 to 1000P and de-popped	0.3
43	26	H/W	04/04	Roger	Solve the pop issue and the static noise during post and idle in Windows	Pop U30 inverter and depop R528 (0_0402_5%)	0.3
44	27	H/W	04/04	Roger	Tune audio amplifier gain to 21.6dB	Pop R164 (10K_0402_5%) and depop R107 (10K_0402_5%)	0.3
45	37	H/W	04/04	Roger	For the +5VHDD power source, use +5VRUN	Depop Q51, Q50, R507, C547 and pop R506 (0_0805_5%)	0.3
46	27	H/W	04/04	Roger	Dell Audio team request	C535, C536 change from 0.47UF to 0.1UF and C199, C206 change from 2.2UF to 0.1F	0.3
47	38	H/W	04/07	Roger	PCI clocks to ICH_PWRGD timing too late issue. SPEC is at least 99 ms	Change C520 form 0.1UF to 0.01UF	0.3
48	13	H/W	04/07	Roger	Intel Design Guide recommend populate TV DAC & CRT DAC power inputs filtering	Change back population L9, L10, L11, L25, L26, L24, C24, C291, C293, C22, C298, C299, C23, C323, C310, C297, C314, C331, C322, C37, C35, C305, C306, C36, C304 on external board	0.3

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
49	6,10,22	H/W	04/28	Roger	Modify pop option for B1 stepping Dothan CPU for ST build	Depop R305, R364, R438. Pop R329, R343, R88 for both UMA and discrete mother board	0.4
50	18,35	H/W	05/06	Roger	Add smart dimmer function for VGA board	U20 pin E3 (BIA_PWM) connect to JVID pin4 isolate by R534 and U4 pin E25 isolate by R533	0.4
51	24	H/W	05/06	Roger	ICH_V5REF_RUN leakage issue	Reserve R535 for +5VRUN power source	0.4
52	6	H/W	05/17	Roger	R274 burn out issue	Change R274 (1 ohm) from 0402 to 0603 size, R273,R401(2.2 ohms) from 0402 to 0603 size.	0.4
53	39	H/W	05/19	Roger	Increase breath and HDD active LED light	Breath LED circuit change to like the bluetooth LED circuit, R1 & R2 change from 330 ohms to 56 ohms	0.4
54	25	H/W	05/19	Roger	X03 issue list item7, modify the SATA crystal circuit	Connect R190 pin1 to U11 pin23, connect pin2 to Y1 pin 2	0.4
55	25	H/W	05/19	Roger	X03 issue list item8,reserve oscillator for istead of crystal for marvell 8040	Add a non-pop oscillator Y3 (25MHz) connect to U11 pin22, Pin23	0.4
55	24	H/W	05/19	Roger	X03 issue list item8, ICH leakage issue	Reserve R537 connect +5VSUS for ICH_5VREF_SUS power source	0.4
56	15	H/W	06/01	Roger	OTP shutdown temperature varies. Offset 6 degree C to 79 degree C	Change R249 from 13.1K ohms to 147K ohms to set VSET to 0.25V	0.4
57	27	H/W	06/01	Roger	When audio recorded, CPU fan noise will be covered from +5VRUN	R143 change from +5VRUN to +5VSUS	0.4
58	25	H/W	06/07	Roger	HDD can't detect issue	C279, C280 change to 12 PF, Add a 25M oscillator reserve for Marvel 8040	0.4
59	36	H/W	06/07	Roger	EMC request pop keyboard matrix signal bypass caps.	Change CN1~CN6 to single 100pF cap for cost saving	0.4
60	35	H/W	06/07	Roger	Change board ID for X03 (R04)	Pop R405 and de-pop R419 (BID : 0011)	0.4
61	6	H/W	06/07	Roger	X03 issue list item 19, add pull down resistor for SRC/CLKREQ select	Add R538 (0 ohm) for pull down U16 pin 56	0.4
62	39	H/W	06/07	Roger	X03 issue list item 20, Bluetooth LED is too bright	Change R8 from 56 ohms to 1K ohms	0.4
63	27	H/W	06/08	Roger	Audio codec and U5 (MAX4411) were unified into the same power	U5 pin10, 19 and R132 pin1 change connect from +3VRUN to +VDDA	0.4
64	27	H/W	06/08	Roger	Audio amplifier power and gain setting pull up power were unified into the same power	R164 pin1 and R165 change connect from +5VRUN to +5VAMPVCC	0.4
65	13	H/W	06/09	Roger	UMA platform TV out water wave issue	Add C598 (4.7U_0805_10V4Z) for +3VRUN_ATVBG bulk	0.4
66	29	H/W	06/09	Roger	Media board signal EMI resistors no necessary now	Remove R188,R189,R193,R194,R195,R196,R197,R208,R209,R220,R221	0.4
67	25	H/W	06/11	Roger	X03 issue list item 28	Connect R204 pin1 to U11 (Marvel 8040) pin22	0.4
68	28	H/W	06/11	Roger	X03 issue list item 29,30	Add PJP21 between USBP4_PWR and USBP5_PWR, PJP22 between USBP7_PWR and USBP8_PWR	0.4
69	34,35	H/W	06/11	Roger	X03 issue list item 31,32	Pop R116 and no-pop R114, pop R119 and no-pop R128 to change power source from +3.3VX to +RTC_CELL	0.4
70	37	H/W	06/11	Roger	Supply +1.8VRUN for Graphic board from Mother board	Change Q14 from SI2456 to SI4810 for larger power margin.	0.4
71	38	H/W	06/11	Roger	Reserved option to use the Sullivan/Laguna rbatt	Add JCOIN connect to +COINCELL	0.4
72	30	H/W	06/11	Roger	According to the cystal vendor measure report	Change R264 from 200 to 820 ohms to reduce the drive level	0.4

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
73	37	H/W	06/11	Roger	+5VRUN glitch when HDD shut down	Populate Q50, Q51,R507,C547 and de-pop R506	0.4
74	26	H/W	06/14	Roger	Disable the Line In MIC function for	No Pop C510 and C512 & Pop R529 and R530	0.4
75	27	H/W	06/14	Roger	X03 issue list item 21	Change C147 and C148 from 1uF (0603) to 3.3uF (0603)	0.4
76	12	H/W	06/15	Roger	X03 issue list item 41	Change Q33, Q7, Q31, and Q27 to BSS138 and use +2.5VRUN for gate voltage	0.4
77	24	H/W	06/15	Roger	X03 issue list item 40	Change R535 to 100 ohm per Intel spec	0.4
78	22	H/W	06/17	Roger	Pop resistor for support deeper sleep	Pop R121 (0_0402_5%) and R127 (56_0402_5%)	0.4
79	25	H/W	06/17	Roger	Implement oscillator for Marvel 8040	De-pop Y1, R204, R190, C279, C280	0.4
80	28	H/W	07/21	Roger	Move USB power jump to close bulk cap	PJP21 connect R14 pin2 and R22 pin2. PJP22 connect R96 pin2 and R109 pin2	0.6
81	35	H/W	07/21	Roger	Change board ID for V0.6	Depop R94, R405, R108 and pop R107, R419, R95	0.6
82	23,34	H/W	07/27	Roger	LCD_TST for panel control by ICH6-M and SIO	LCD_TST connect to ICH6-M pin AD20(GPO21) and Macallan pin B12 (LGPIO70) isolate by R539,R540	0.6
83	9	H/W	08/01	Roger	Reduce CUP core caps for cost saving	Depop C428, C446, CC448, C431, C119, C118	0.6
84	13	H/W	08/29	Roger	Change +1.5VRUN_DPLLA, +1.5VRUN_DPLLB, +1.5VRUN_HPLL, +1.5VRUN_MPLL inductance	Change L28, L33, L38, L39 to TDK 10U_MLZ2012E100PTAIN 10 UH inductance	0.6
85	39	H/W	08/11	Roger	Balance LED brightness	Change R5 value from 330 ohms to 220 ohms	0.6
86	6	H/W	09/03	Roger	Dell other project have issue at CLKSEL0 signal	Depop R532 and pop R259	0.6
87	36	H/W	09/23	Roger	SST flash ROM part have crash issue, need to further clarify	Change SST 39VF080 to MXIC MX29LV008BTC-70R	0.6
88	39	H/W	09/23	Roger	Change the LED from non clear lens to clear lens	Change D1, D2, D3 from HARVATEK to Lite-on	0.6
89	15	H/W	11/03	Roger	Forcecon CPU fan acoustic issue	Pop C538 (2200P_0402_25V7K)	1.0
90	23	H/W	11/03	Roger	Intel sighting report #67725 workround	Pop R433 (100K_0402)	1.0
91	10	H/W	11/03	Roger	Intel sighting report #68363 workround	De-pop R435, R437	1.0
92	39	H/W	11/03	Roger	Blue tooth LED is too bright	Change R8 from (1K_0603) to (3.3K_0603)	1.0
92	19	H/W	11/03	Roger	fine tune G_PWR_SRC lag +3VRUN sequence issue	Change C290 form 0.1UF to 1000PF	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	POWER	01/30	Demon	Change charger current	Change PR158 from 90.9K to 52.3K	0.1
2	44	POWER	01/30	Demon	Change DDR2 solution	Change PU6 from SC1486 to MAX8550 and other component at P44	0.1
3	42	POWER	01/30	Demon	Dell request to add components	Change PC15 from 4.7u to 2.2u, add PR203(100 ohm) and PC156(2.2u)	0.1
4	40	POWER	02/06	Demon	Dell request to change component	Change PR2 from 1.5k to 2.2k	0.1
5	43	POWER	02/13	Demon	Dell request to change component	Change PC51 from 330U 25m ohm to 330U 9m ohm	0.1
6	40	POWER	03/17	Demon	EMI request	Delete PL3 and pop PL2, add PL21 FBM-L11-453215-900LMAT_1812~D	0.2
7	45	POWER	03/17	Demon	EMI request	Change PR97,PR124 from 0 ohm to 2.2 ohm	0.2
8	44	POWER	03/17	Demon	Double Plus at high side gate	Add PC158 1000P	0.2
9	42	POWER	03/25	Demon	EMI request	Add PL22 FBM-L11-453215-900LMAT_1812~D	0.2
10	43	POWER	03/25	Demon	EMI request	Add PL23 FBM-L11-453215-900LMAT_1812~D	0.2
11	44	POWER	03/25	Demon	EMI request	Add PL24 FBM-L11-453215-900LMAT_1812~D	0.2
12	43	POWER	03/29	Demon	Increase 1.5VSUS voltage spec of power source for GMCH 1.5V Vcc power on Tobago	Change PR58 from 10K to 11K	0.2
13	40	POWER	04/05	Demon	DELL EE request	Change PQ1 from 2N7002 to BSS138	0.2
14	42	POWER	05/10	Demon	DELL power team request	Change PR27 from 4.7ohm to 10ohm, and add PR211 10ohm	0.3
15	46	POWER	05/10	Demon	DELL request	Change PU8 from MAX1535AETJ to MAX1535BETJ	0.3
16	44	POWER	05/14	Demon	For vender new version MAX8550A	Add PR212,PR215 0 ohm , and un-pop PQ36, PR197,PR213,PR214, and change PU6 from MAX8550 to MAX8550A	0.3
17	45	POWER	05/19	Demon	DELL request	Change PQ13,PQ17 from IRF7811AV to IRF7821 and PQ15,PQ19 from SI4362 to IRF7832 and un-pop PQ16,PQ20	0.3
18	44	POWER	05/31	Demon	DELL request	Change PC152, PC153, PC154,PC157 from 22uF to 10uF	0.3
19	48	POWER	05/31	Demon	Modify layout	Un-pop PQ15 and PQ17, pop PQ16 and PQ18	0.3
20	44	POWER	05/31	Demon	Modify schematic the same with Laguna and change switching frequencies from 450kHz to 300kHz	Un-pop PR84	0.3
21	43	POWER	06/07	Demon	DELL request, for MAX1845 negative voltage issue.	Add PQ37 2N7002 and PR216 33k ohm.	0.3
22	41	POWER	06/07	Demon	Modify 2.5V power sequence	Change PR1 from 0 ohm to 8.2k ohm and add PC8 0.1u.	0.3
23	43	POWER	06/10	Demon	Change 1.55V to 1.525V	Change PR58 from 11K to 10.5K.	0.3
24	44	POWER	06/10	Demon	For MAX8550	Add PQ36 and PR197 100k ohm, and delete PR212 0 ohm.	0.3
25	43	POWER	06/15	Demon	For power sequence	Pop PR60 and un-pop PR80 at External and Internal M/B.	0.3
26	43	POWER	07/08	Demon	For MAX1845 OVP issue	Add PR217 11k ohm.	0.4
27	45	POWER	07/08	Demon	For MAX1987 C4 Voltage	Add PR218 0 ohm and delete PR103 0 ohm and un-popPR219,PR220	0.4
28	45	POWER	07/21	Demon	For noise issue	Add a un-pop component PC159	0.4