

COMPAL CONFIDENTIAL

MODEL NAME : HAU30

PCB NO : LA-3071P

COMPAL P/N : DA800004H1L

Crockett Schematics Document

uFCBGA Mobile Yonah-ULV
Intel Calistoga-GMS + ICH7M

2006 - 5 - 12

REV : 1.0 (DELL: A00)

MB PCB

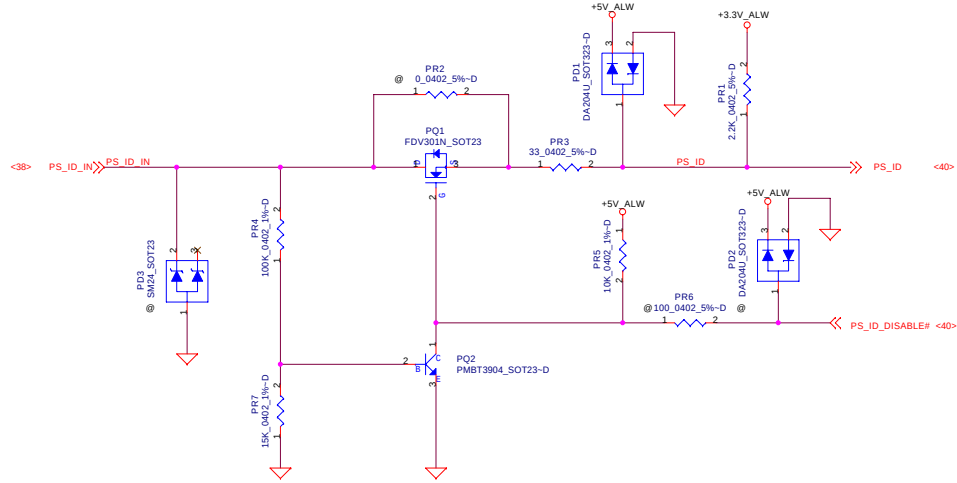
Part Number	Description
DA800004H1L	PCB 00B LA-3071P REV1 M/B

BOM NO. 43140131L01
PCB P/N: DA800004H1L

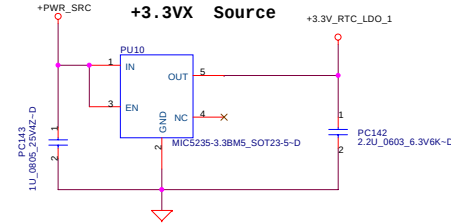
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Title			
Cover Sheet			
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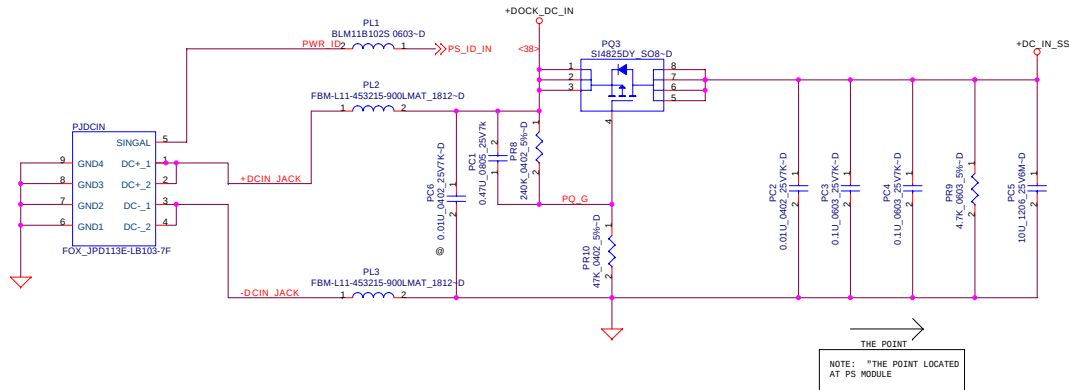
PS_ID Detector



+3.3VX Source



+DC_IN Source



THE POINT
NOTE: "THE POINT LOCATED
AT PS MODULE

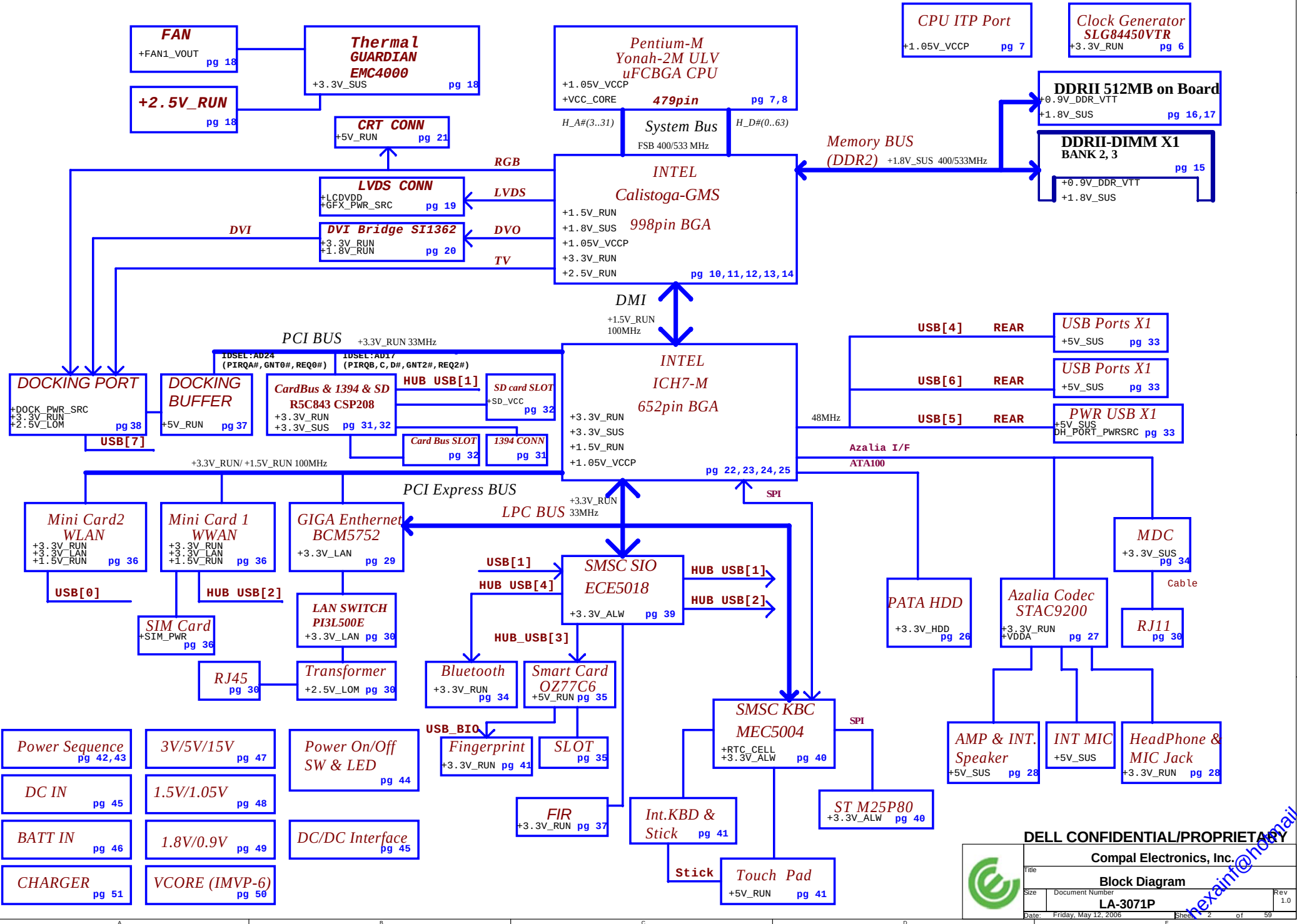
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+DCIN

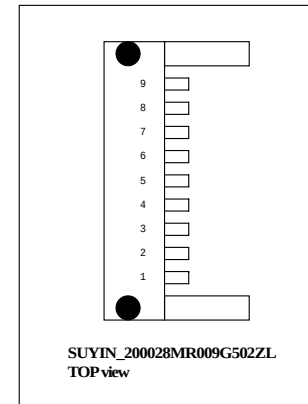
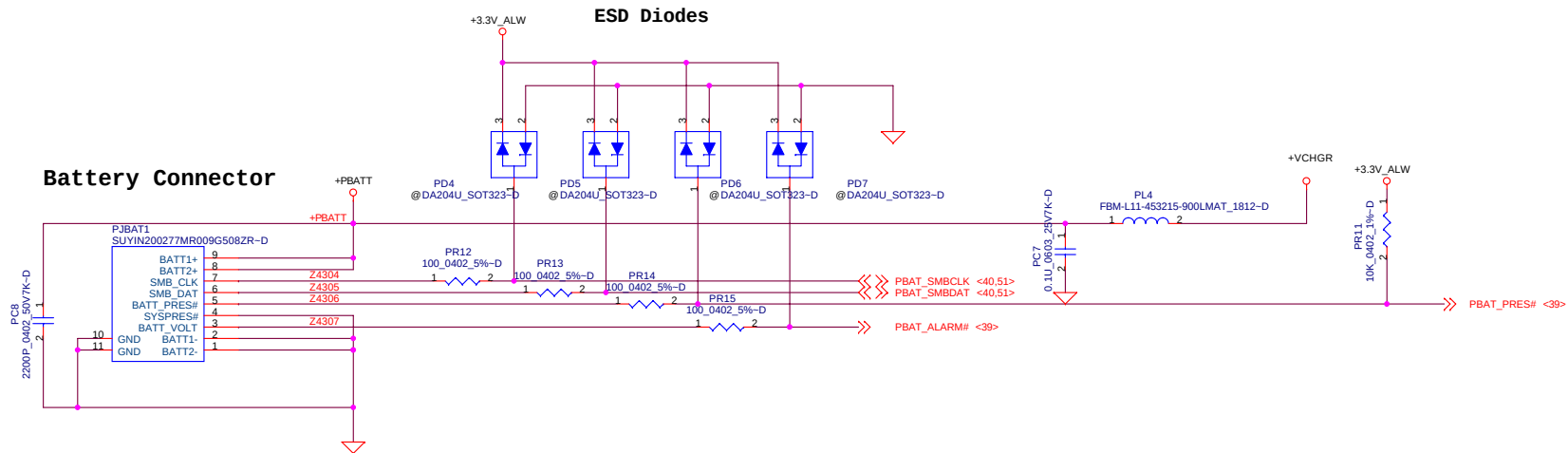
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Block Diagram			
LA-3071P			
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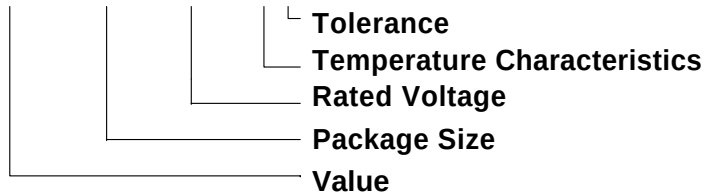


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Battery Conn			
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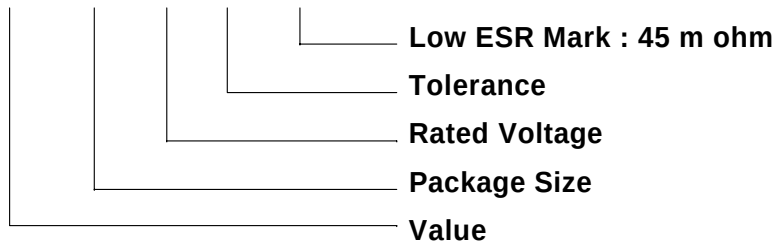
Ceramic Capacitors :

0.1U_0402_6.3VXX



Tantalum or Polymer Capacitors :

10U_D2_10VX_R45



Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NPO	C0G	X6S	BJ	CH	CJ	CK	SH	SJ

H	I	J	K
UJ	UK	SL	X5S

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1PF	+2%	+3%	+5%

K	M	N	P	Q	V	X	Z	
+10%	+20%	+30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

NOTE1:

@XX : Depop component

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	2	B, C, D
DOCKING	AD24	0	A

PM TABLE

State \ power plane	+3.3V_ALW +5V_ALW	+3.3V_SRC +3.3V_SUS +5V_SUS +1.8V_SUS +15V_SUS	+5V_RUN +3.3V_RUN +1.8V_RUN +0.9V_DDR_VTT +1.5V_RUN +VCC_CORE +1.05V_VCCP +2.5V_RUN
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB TABLE

USB PORT#	DESTINATION	USB HUB	DESTINATION
0	Mini 2(WLAN)	1	PC Card Bay
1	USB Hub (5018)	2	Mini 1(WWAN)
2	N/A	3	SMART CARD
3	N/A	4	Blue tooth
4,6	REAR		
5	PWR USB	USB HUB on OZ77C6LN	DESTINATION
7	Docking	DP_HUB	Fingerprint

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DC/DC +3V/ +5V/ +15V

3.3 Volt +/- 5%
Design Current: 6.5 A
Maximum current: 9.1A
OCp: 10.95A

15-Volt
Maximum Current: 10mA

5 Volt +/- 5%
Design Current:3.63A
Maximum current: 5.191 A
OCp: 6.35A

5V OCP
 $F_{sw}=290 \text{ KHZ}$
 $R_{ds_on_MAX}=20m$; $I_{trip_MIN}=8.5uA$; $L=4.7uH$
 $\Delta I_{out}=V_{out}/L * 1/F_{sw} * (1-V_{out}/V_{in})$
 $=5/4.7u * 1/290K * (1-5/19)=2.7A$
 $I_{valley_MIN}=I_{trip}*R_{trip}/R_{ds_on}=8.5u*10K/20m=4.25A$
 $I_{ocp_MIN}=4.25+2.7/2=5.6A$
 $I_{ocp}=5+2.7/2=6.35A$

3.3V OCP
 $F_{sw}=440 \text{ KHZ}$
 $R_{ds_on_MAX}=15m$; $I_{trip_MIN}=8.5uA$; $L=2.7uH$
 $\Delta I_{out}=V_{out}/L * 1/F_{sw} * (1-V_{out}/V_{in})$
 $=3.3/2.7u * 1/440K * (1-3.3/19)=2.3A$
 $I_{valley_MIN}=I_{trip}*R_{trip}/R_{ds_on}=8.5u*14.7K/15m=8.33A$
 $I_{valley}=I_{trip}*R_{trip}/R_{ds_on}=10u*14.7K/15m=9.8A$
 $I_{ocp_MIN}=8.33+2.3/2=9.48A$
 $I_{ocp}=9.8+2.3/2=10.95A$

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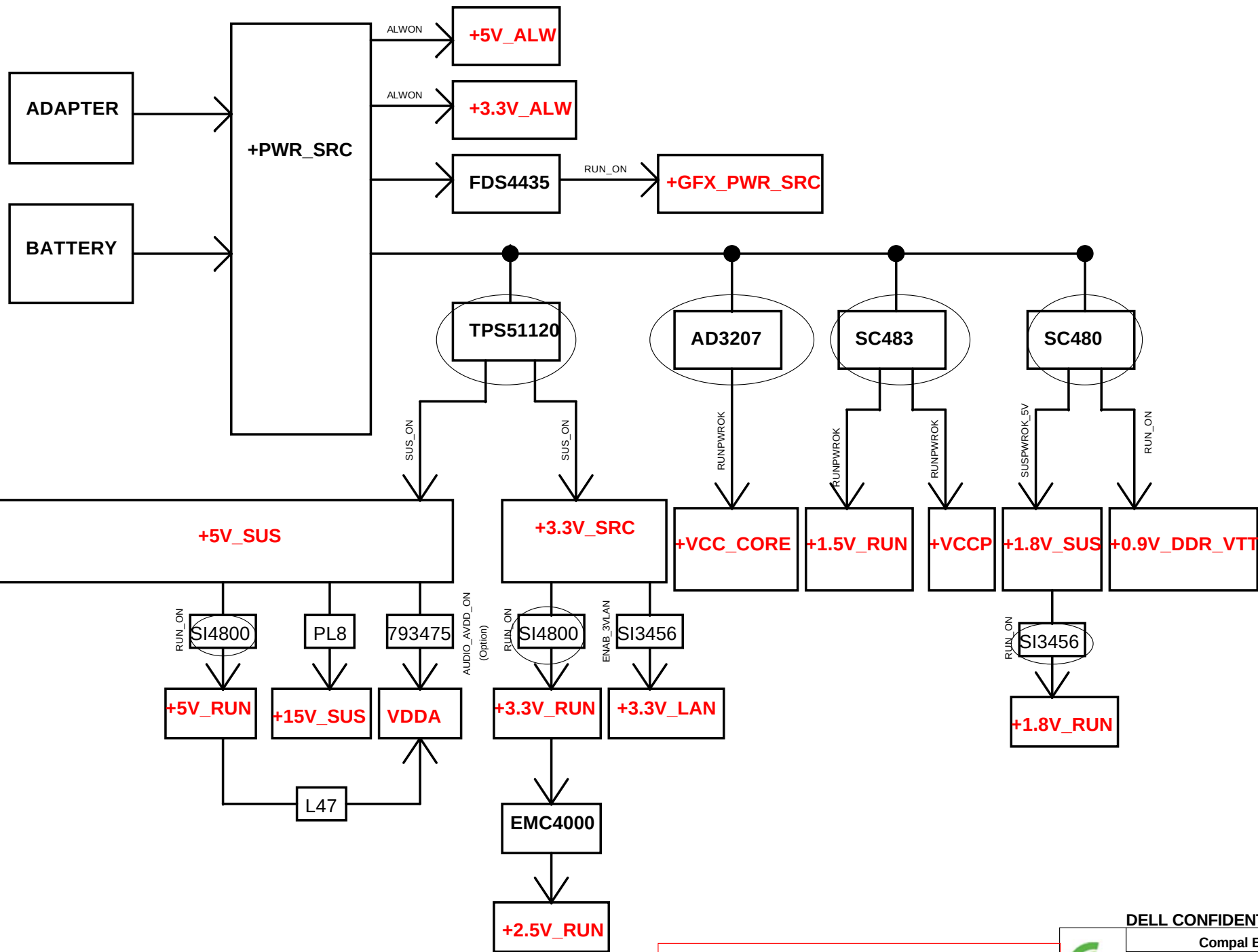
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+3.3V/+5V/+15V

LA-3071P

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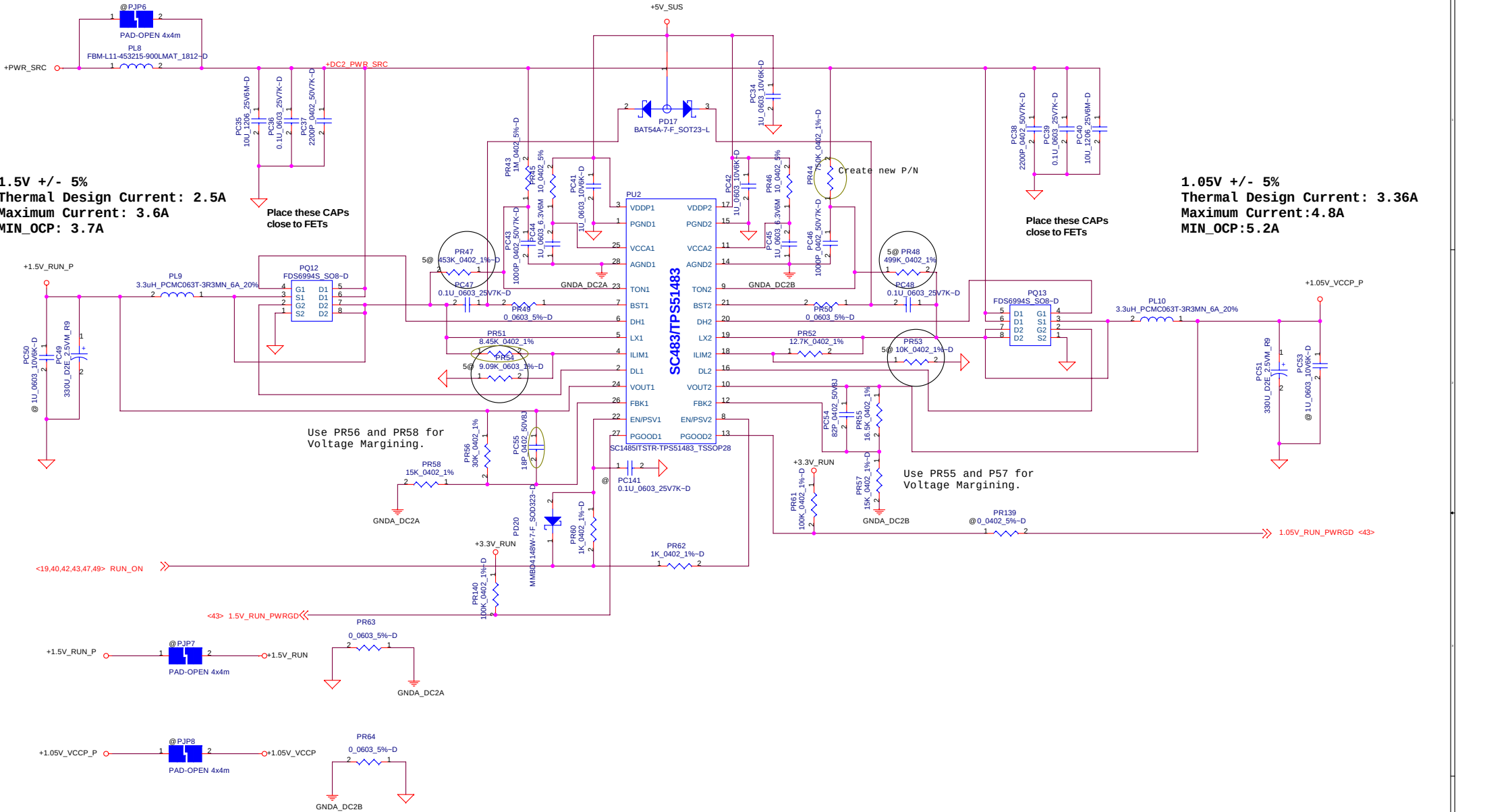
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Power Rail

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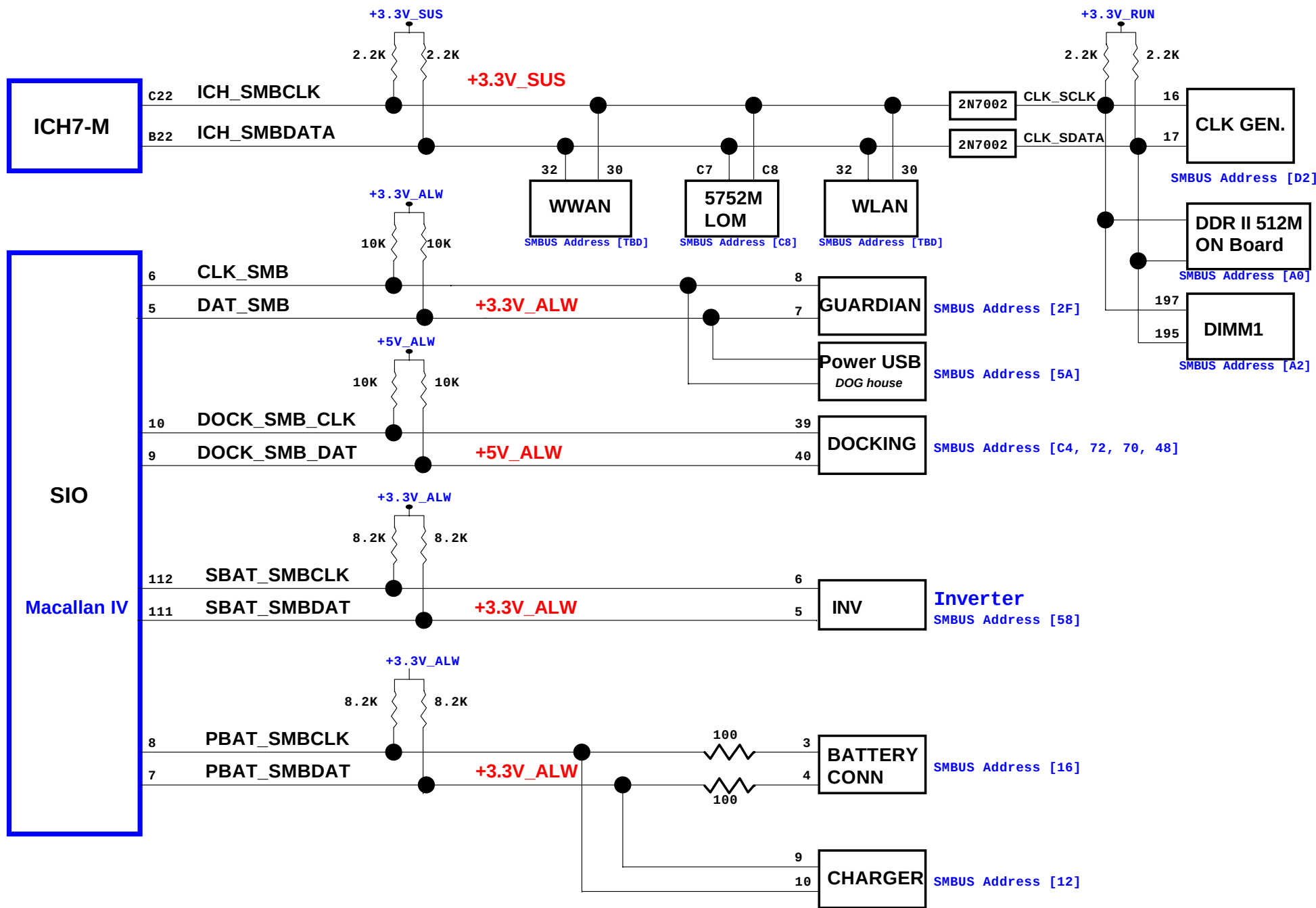
BOM Structure	Description
@	Do Not Populate
4@	Populate for Semtech - SC483 Only
5@	Populate for Ti - TPS51483 Only

Ref Des	SC483	TPS52483
PR56	30.0K	15.0K
PR58	15.0K	15.0K
PR55	16.5K	11.8K
PR57	15.0K	29.4K

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+1.5VRUNP /+VCCP_1P05VP			
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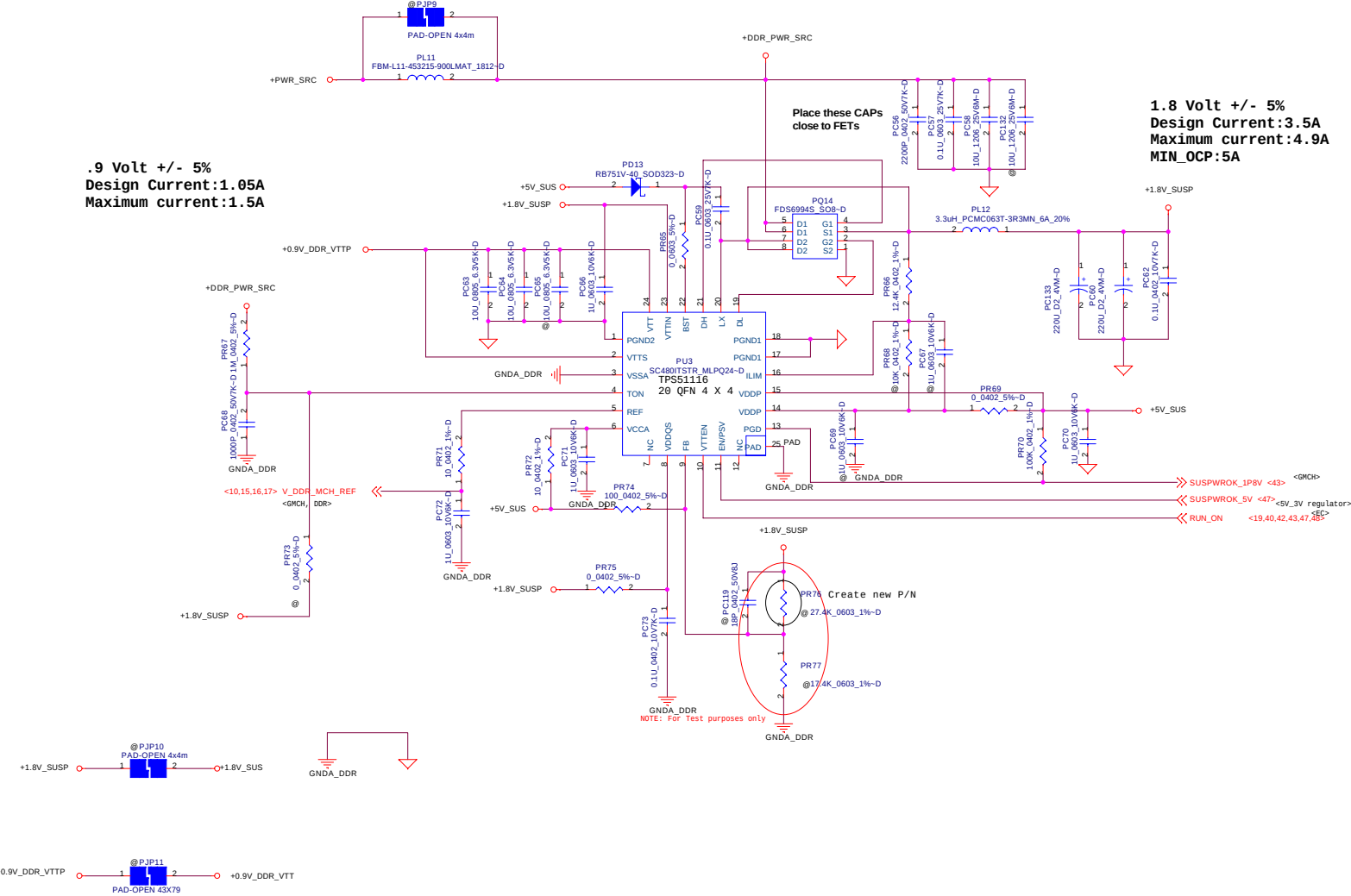
nexus@compal.com

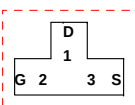
NOTE: Component Values Shown for SEMTECH SC480 ONLY.
For Texas Instruments TPS51116, Please USE Reference BOM.

.9 Volt +/- 5%
Design Current:1.05A
Maximum current:1.5A

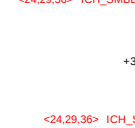
1.8 Volt +/- 5%
Design Current:3.5A
Maximum current:4.9A
MIN_OCP:5A

Place these CAPS
close to FETs



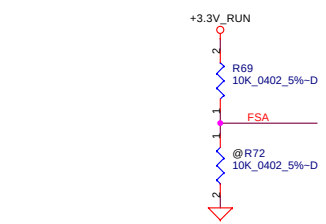


2N7002

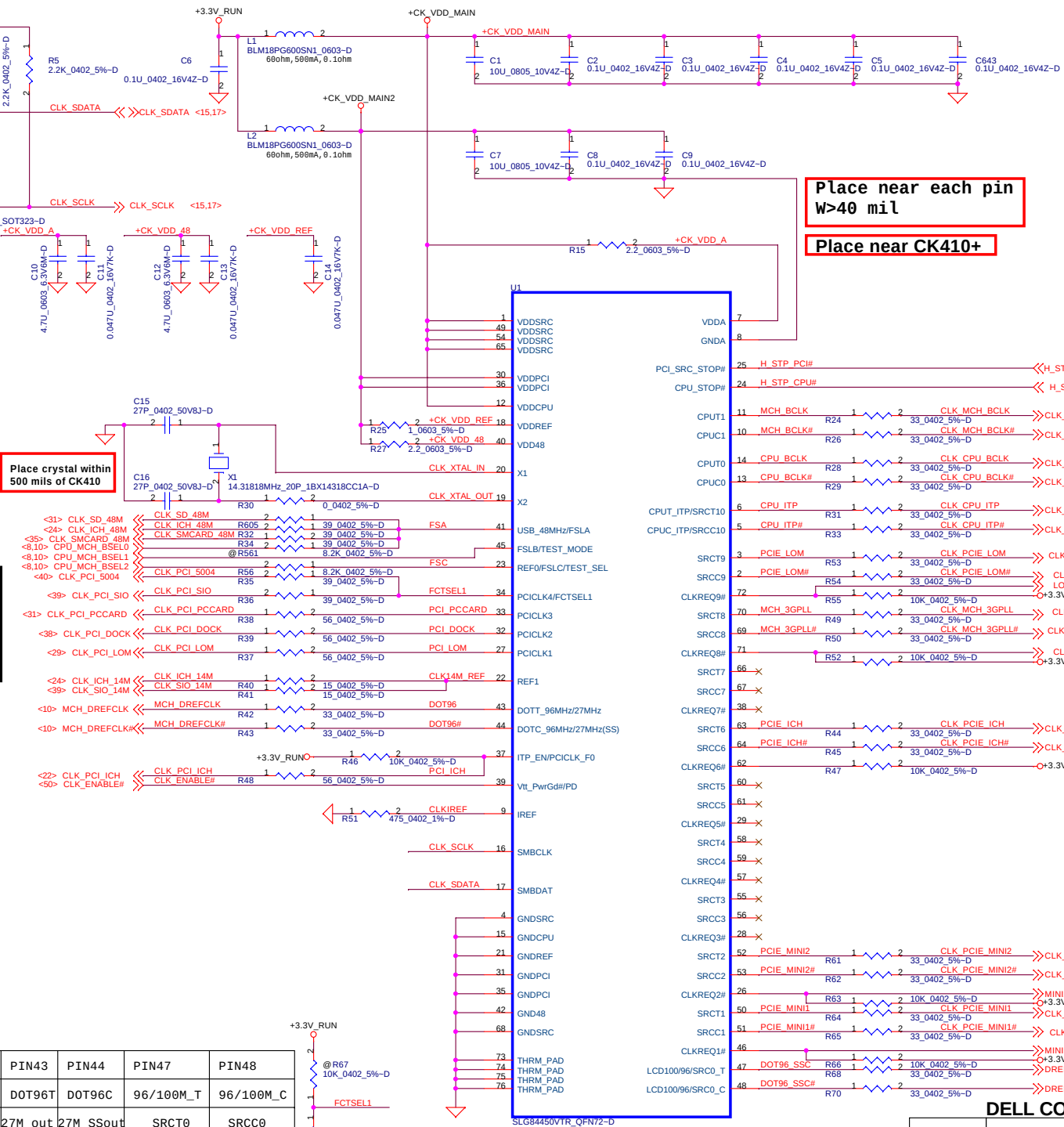


FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	Reserve		

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

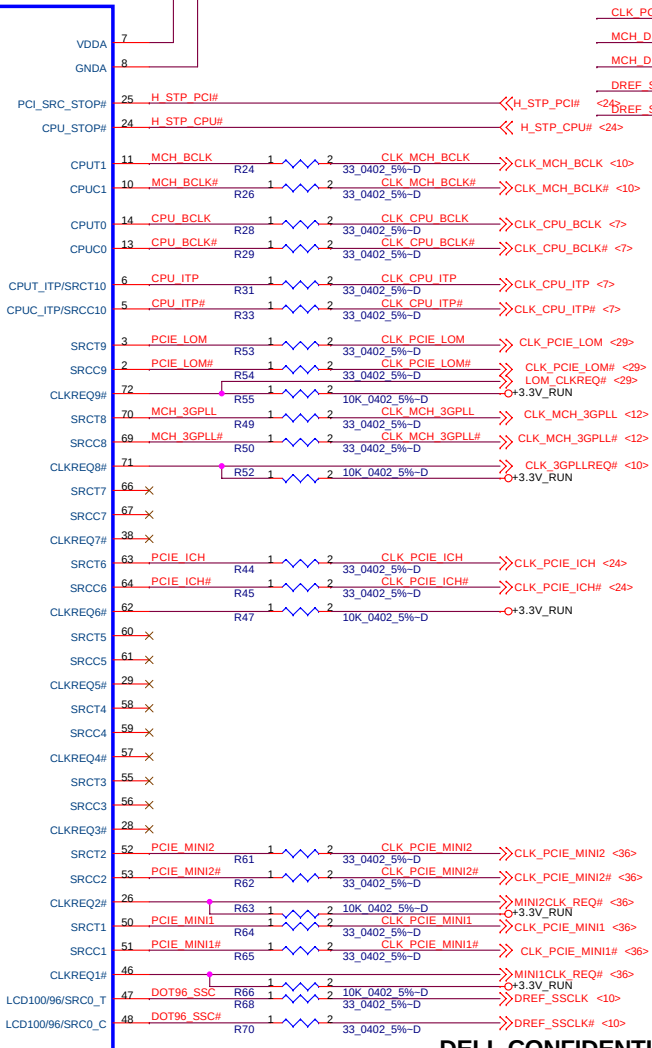
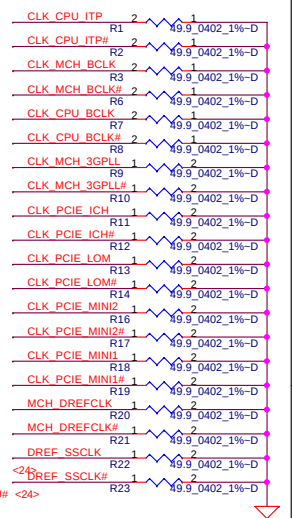


FCTSEL1	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27M_out	27M SSout	SRCT0	SRCC0



Place near each pin
w>40 mil

Place near CK410+



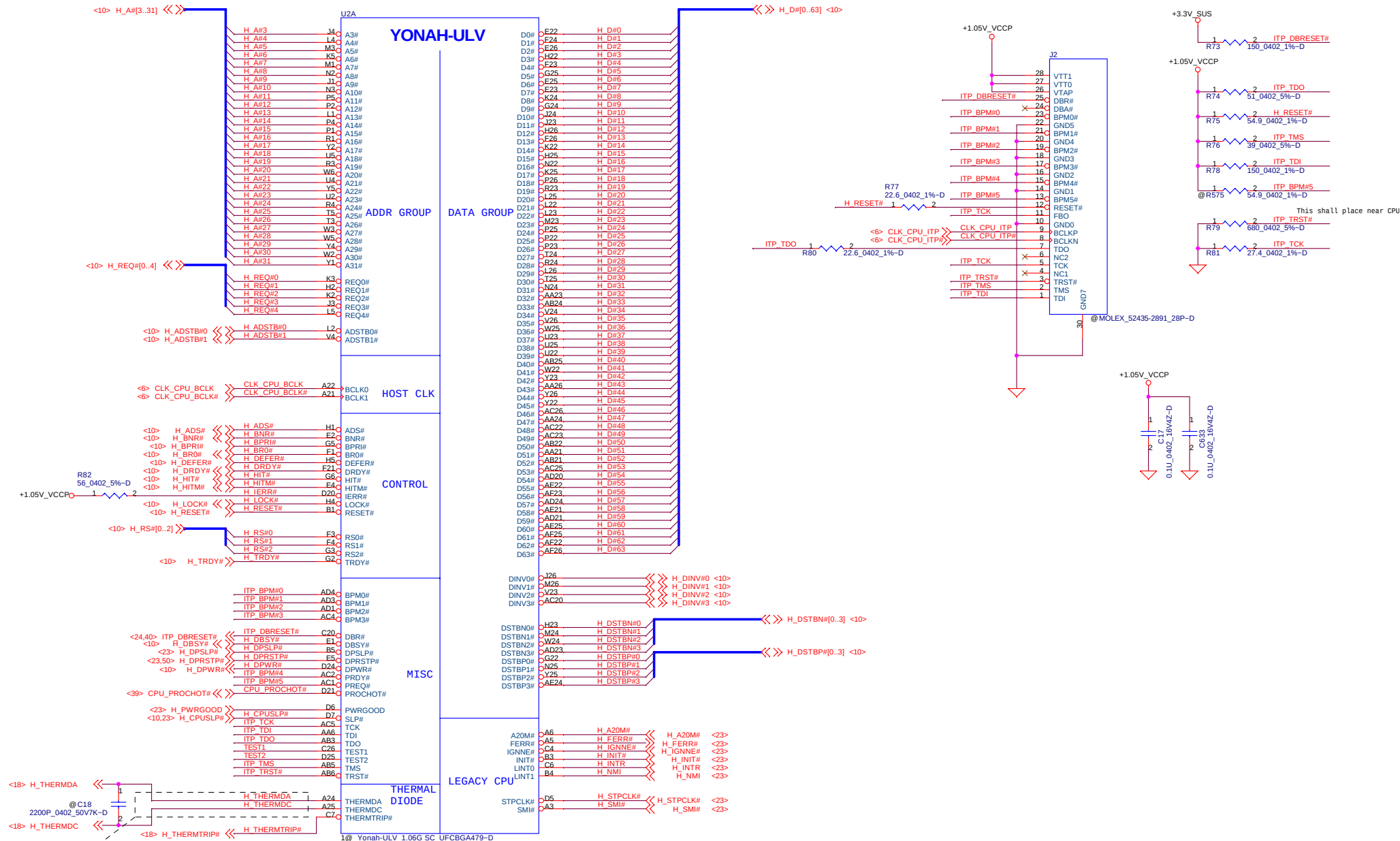
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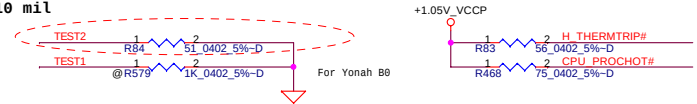
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Clock Generator			
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H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



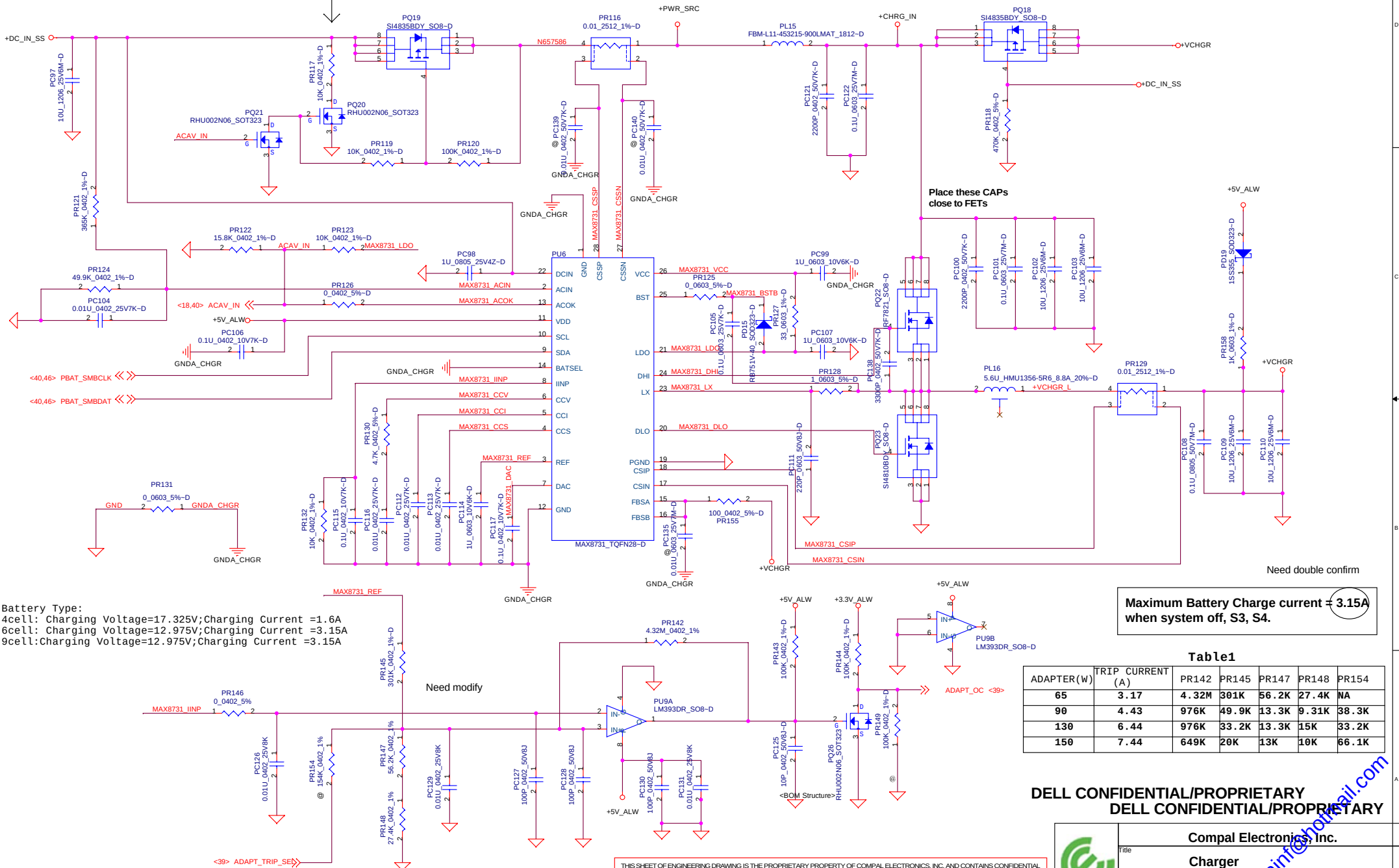
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Yonah-ULV in mFCPGA479				
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Smart Charger

+DC_IN discharge path

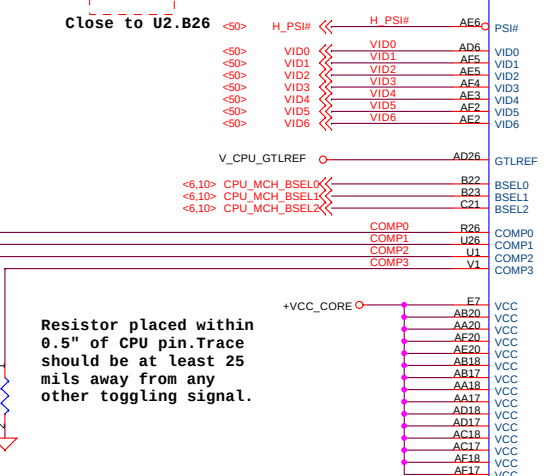
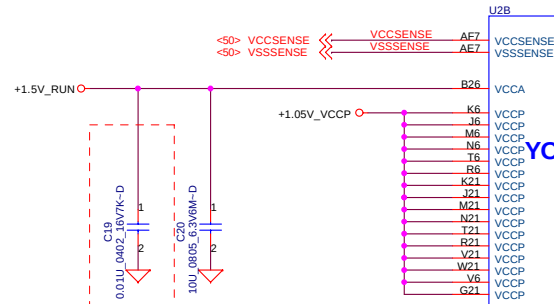
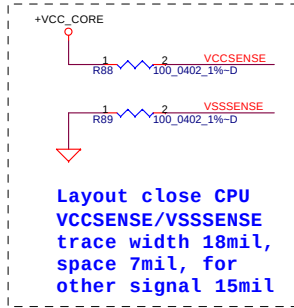
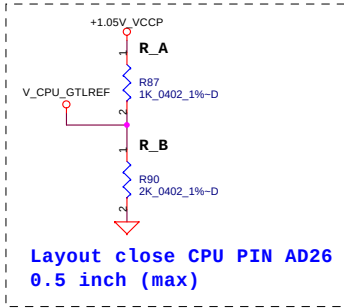


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		Charger	
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Length match within 25 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

YONAH-ULV

POWER, GROUND, RESERVED SIGNALS AND NC

YONAH-ULV

POWER, GROUND

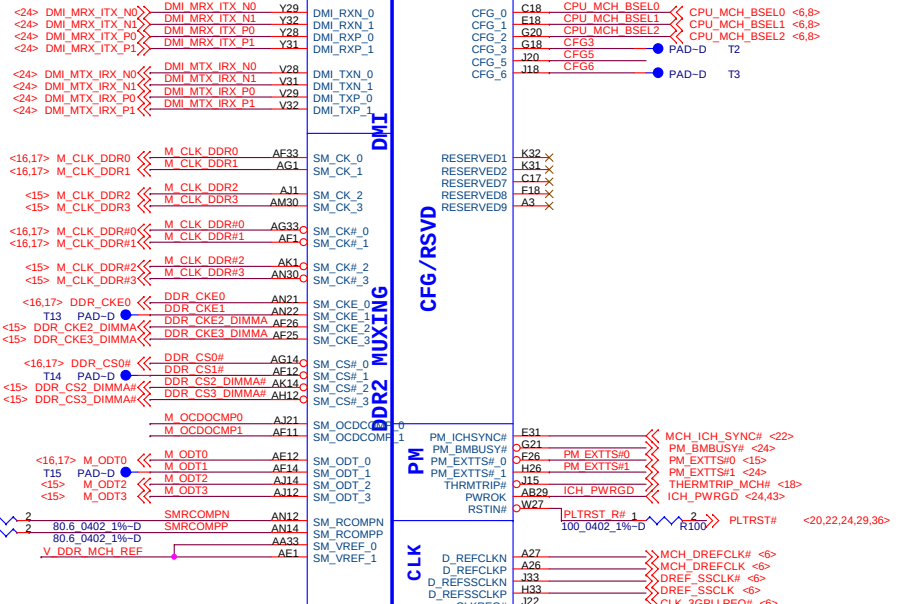
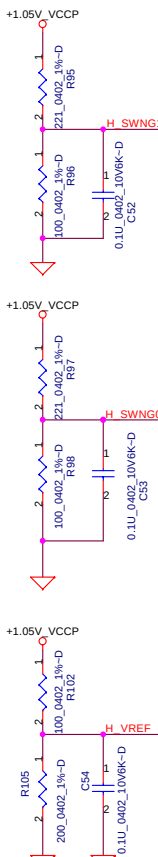
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Yonah-ULV in mFCBGA479

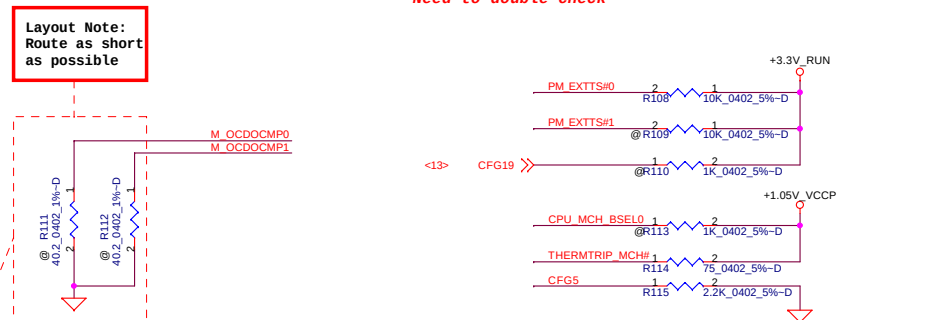
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Strap Pin Table	
CFG5	Low = DMI x 2 * High = DMI x 4
CFG19 (DMI Lane Reversal)	Low = Normal Operation (Default): Lane number in Order High = Reverse Lane

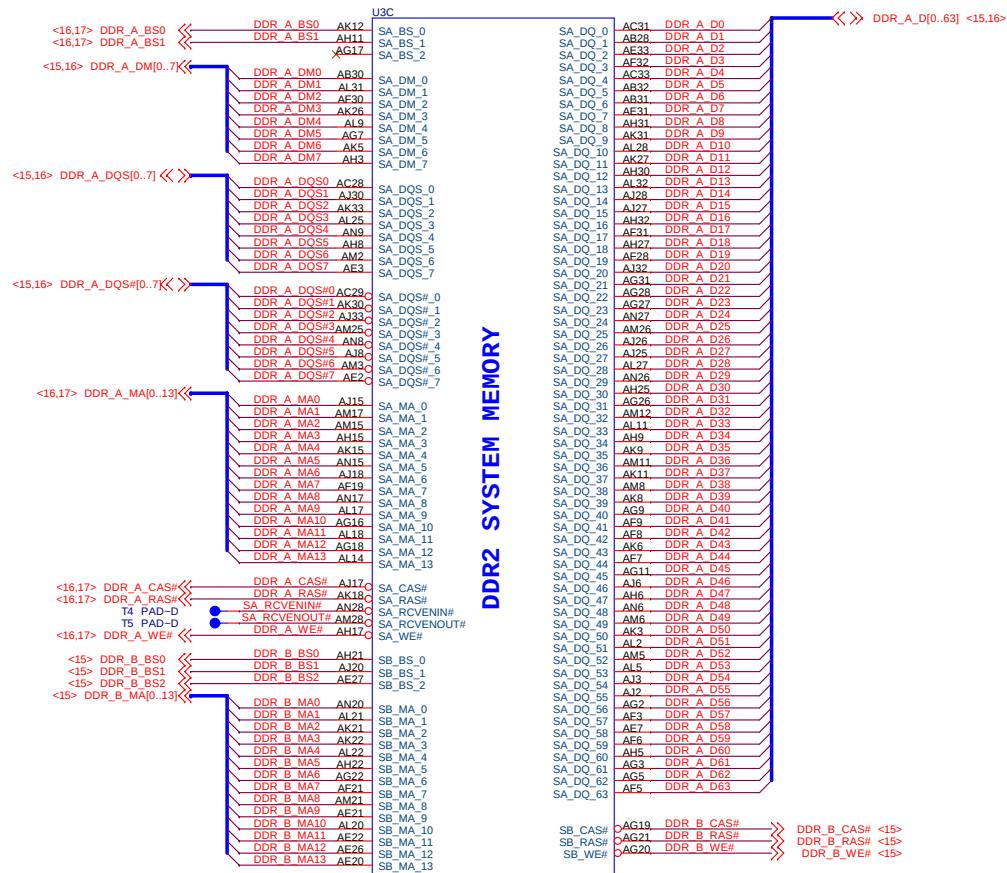
Calistoga-GMS not have CFG4,CFG[7..18],CFG[20]
Need to double check



Layout Note:
Route as short
as possible

Stuff R111 & R112 for A1 Calistoga

Layout Note:
H_XRCOMP & H_YRCOMP trace width
and spacing is 10/20



Calistoga-GMS_FCBGA998-0

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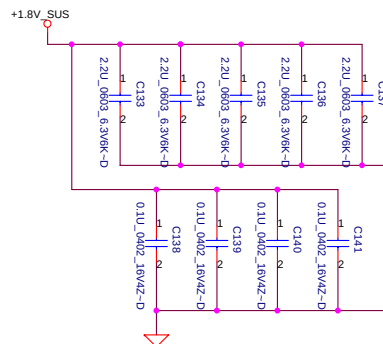
Calistoga(2 of 5)

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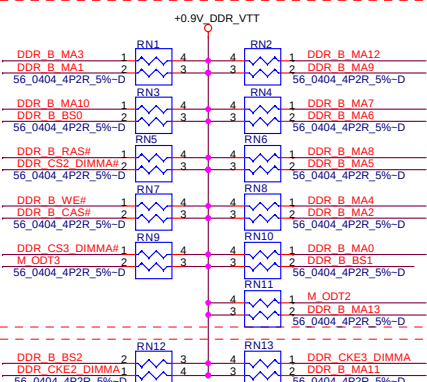
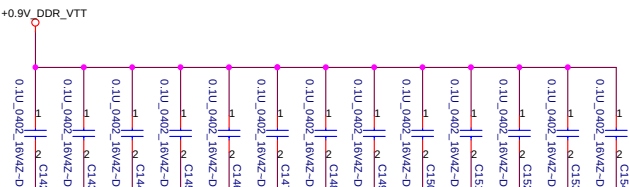
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<11.16> DDR_A_DQS#[0..7] <<>>
 <11.16> DDR_A_D[0..63] <<>>
 <11.16> DDR_A_DM[0..7] <<>>
 <11.16> DDR_A_DQS[0..7K] <<>>
 <11> DDR_B_MA[0..13] <<>>

Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor closely DIMM0, all trace length<750 mil

Layout Note:
Place these resistor closely DIMM0, all trace length Max=1.3"

ON Bottom SIDE



DIMMA STANDARD

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DDRRII-SODIMM SCOT1

LA-3071P

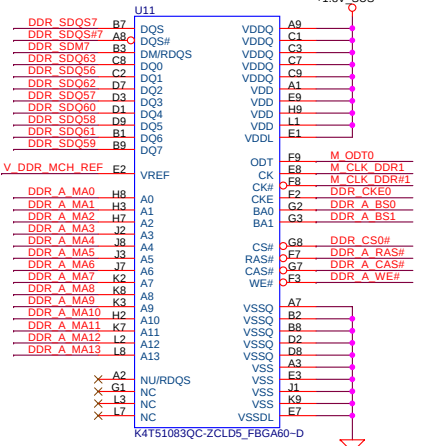
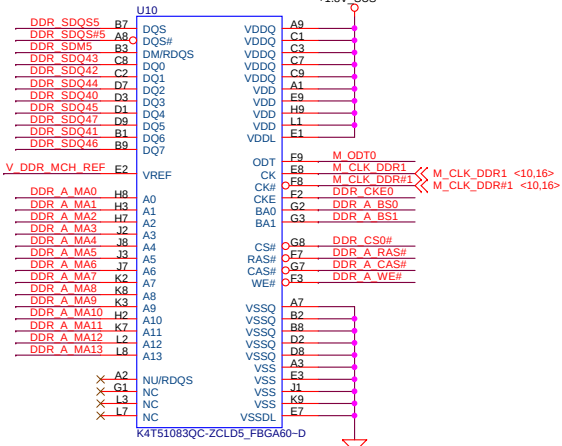
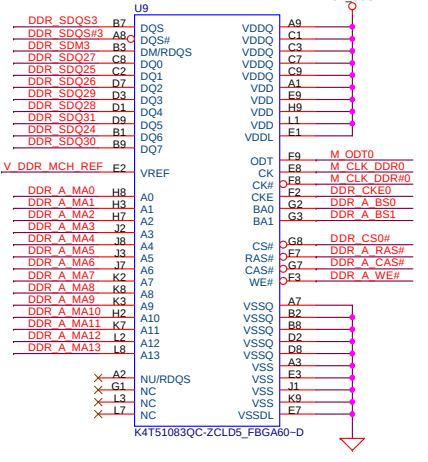
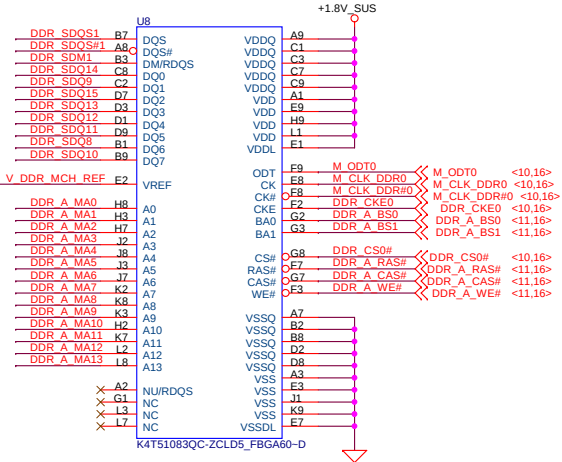
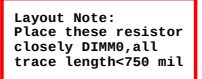
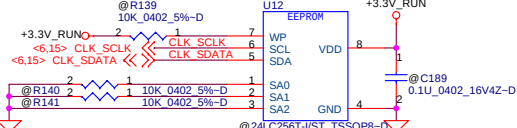
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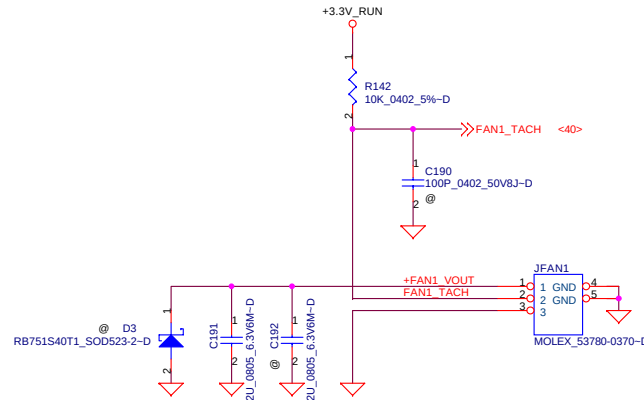


next@compal.com

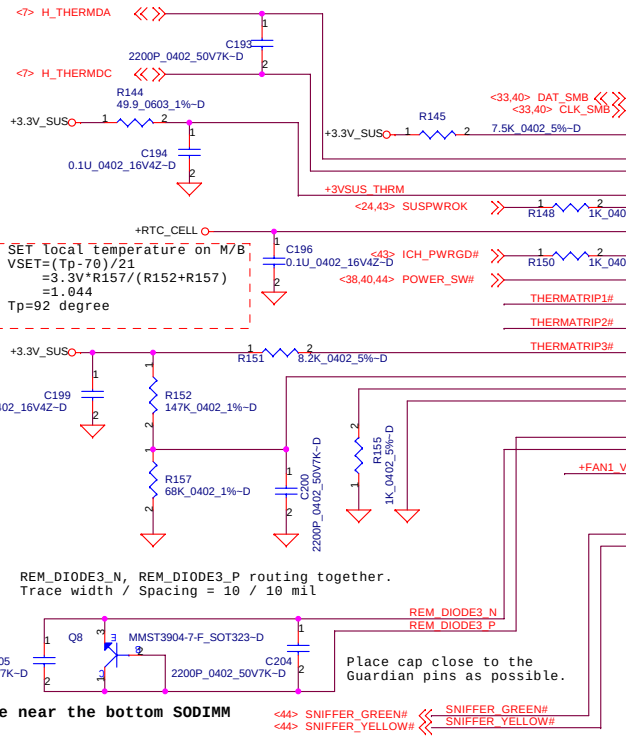
The schematic diagram illustrates the power supply section of the 68000 microprocessor. It features a three-stage voltage divider network. The first stage takes a +1.8V input and divides it by 2 (C165, R165) to produce 0.9V (C164, R164). The second stage divides 0.9V by 2 (C163, R163) to produce 0.45V (C162, R162). The third stage divides 0.45V by 2 (C161, R161) to produce 0.225V (C160, R160). The output is connected to the VDD pin of the 68000. The diagram also shows the connection of the 68000's VDD, VDDQ, and VDDP pins to the power supply network.



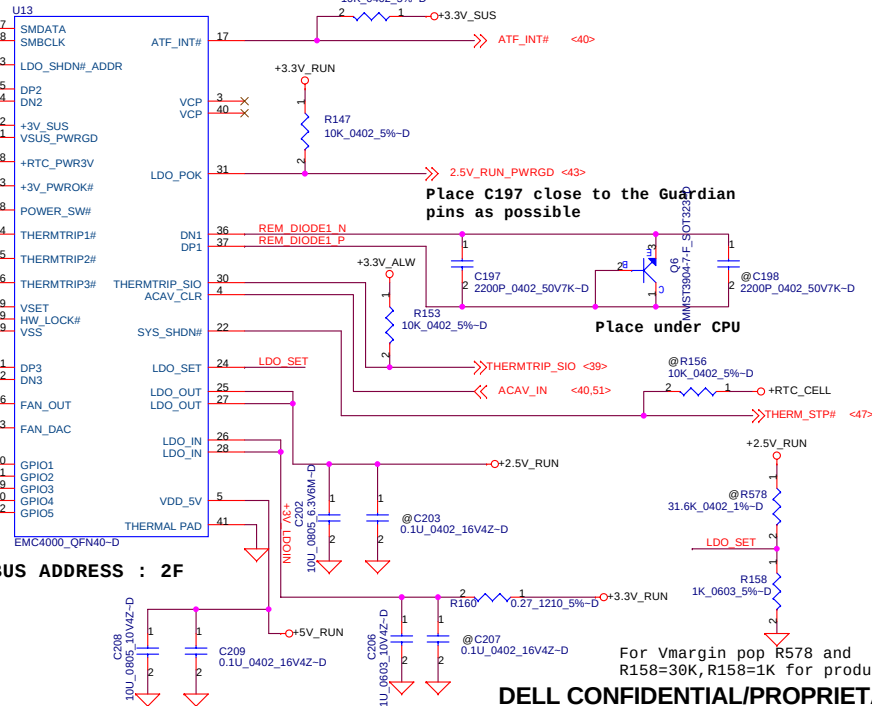
FAN1 Control and Tachometer



Place C341 close to the Guardian pins as possible



Use Rev:C
Need create P/N



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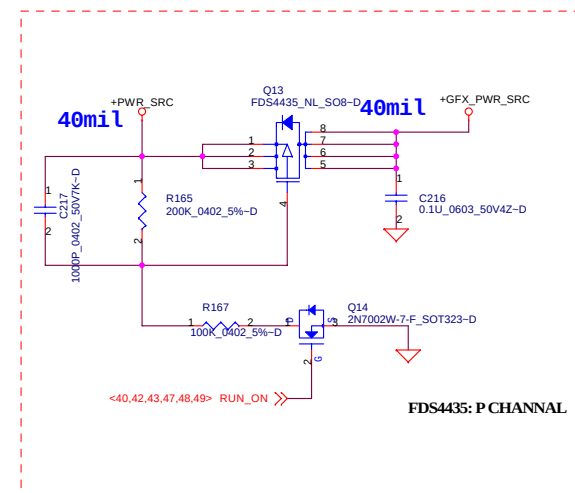
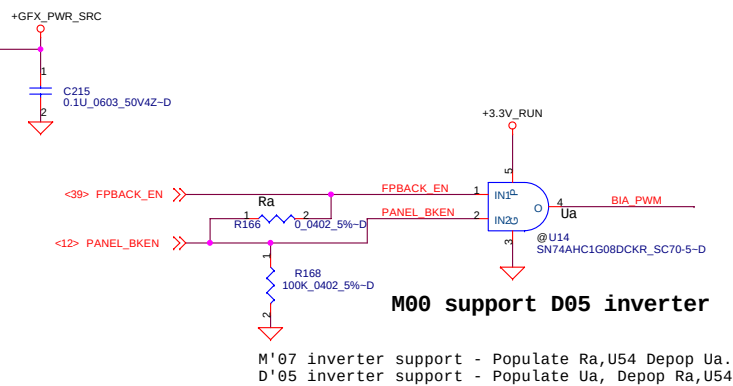
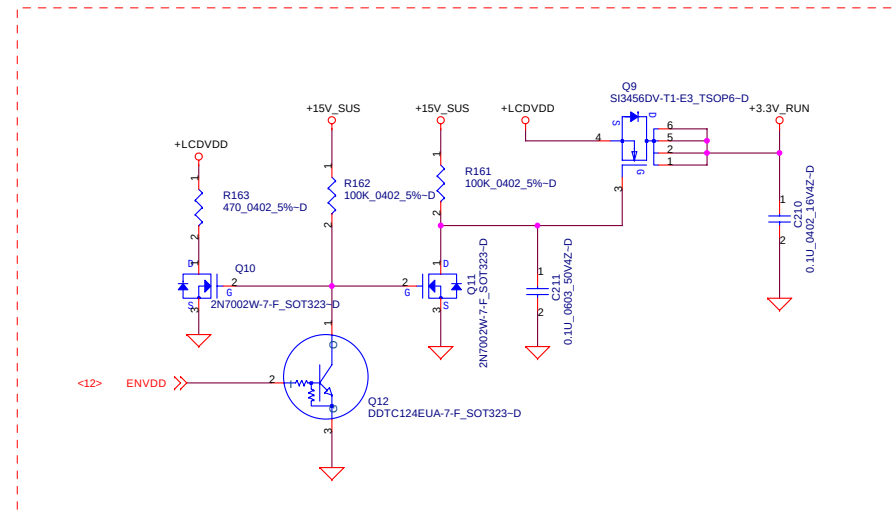
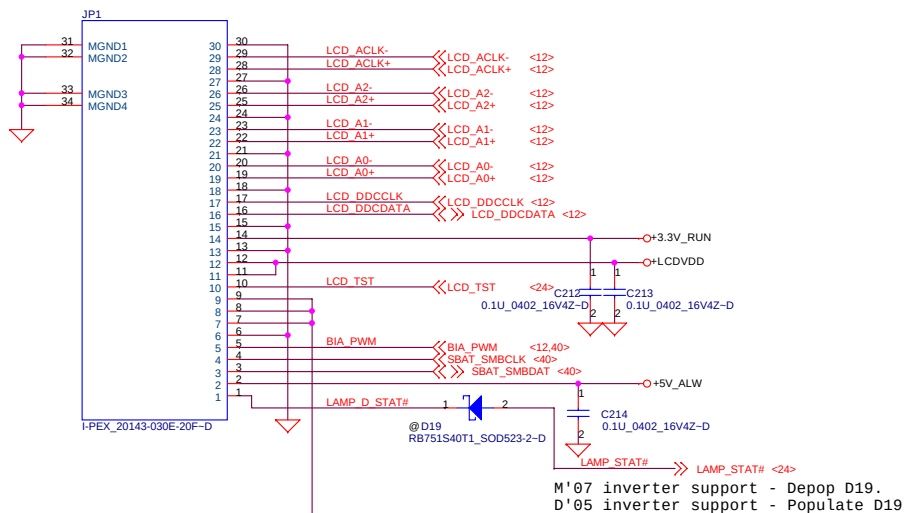
FAN & Thermal Sensor

LA-3071P

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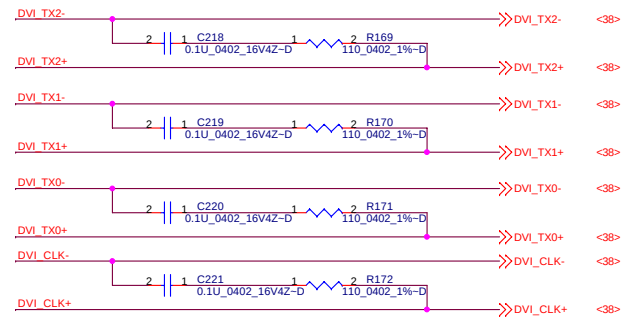
Compal Electronics, Inc.

Internal LVDS

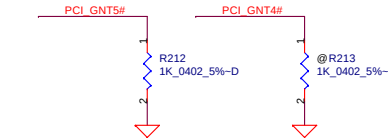
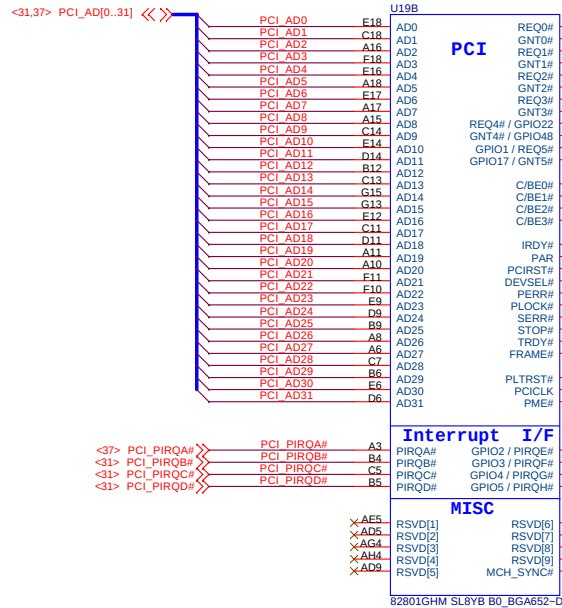
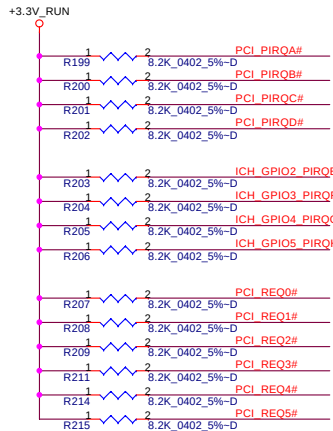
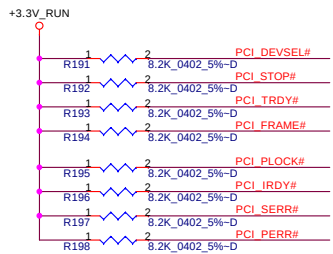
LA-3071P

Rev 1.0

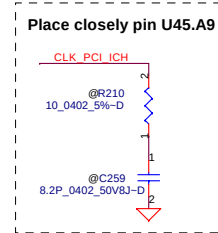
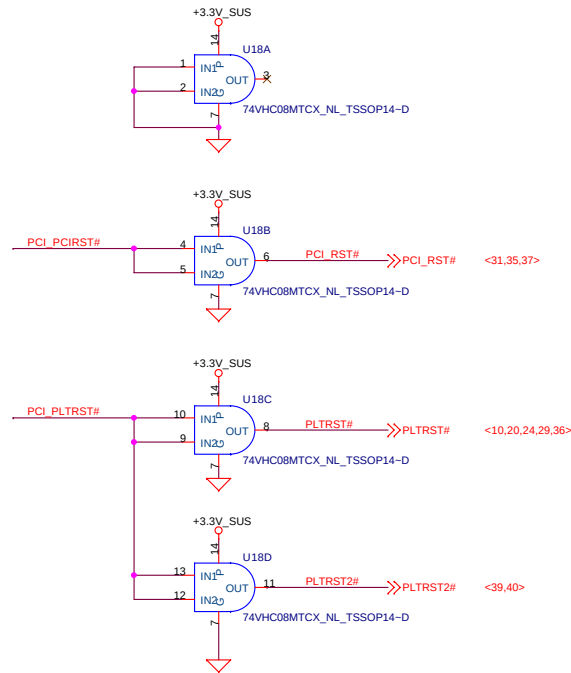
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	GNT5# R214	GNT4# R213
LPC (11)	unstuff	unstuff
PCI (10)	unstuff	stuff
SPI (01)	stuff	unstuff



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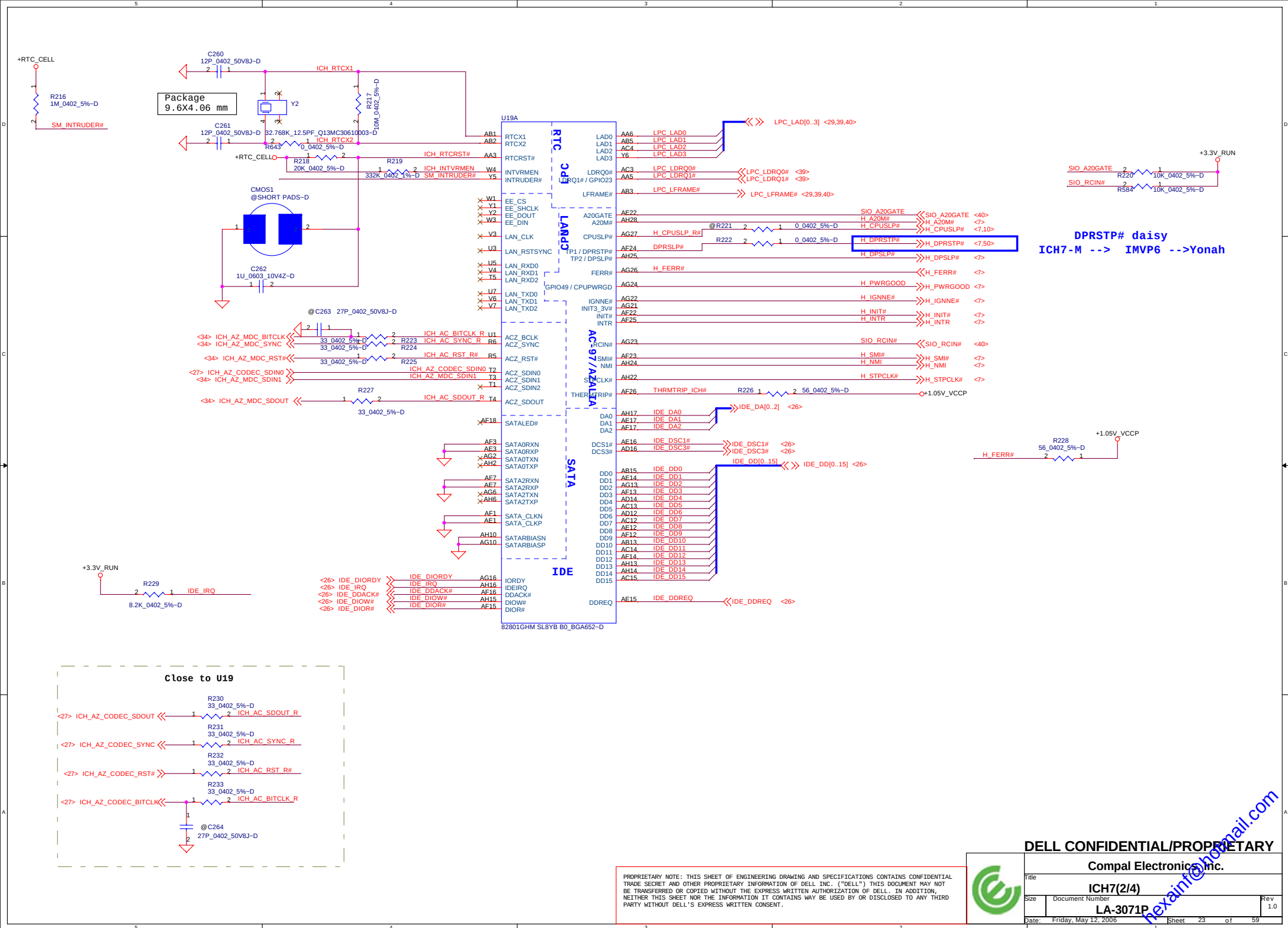
Compal Electronics, Inc.

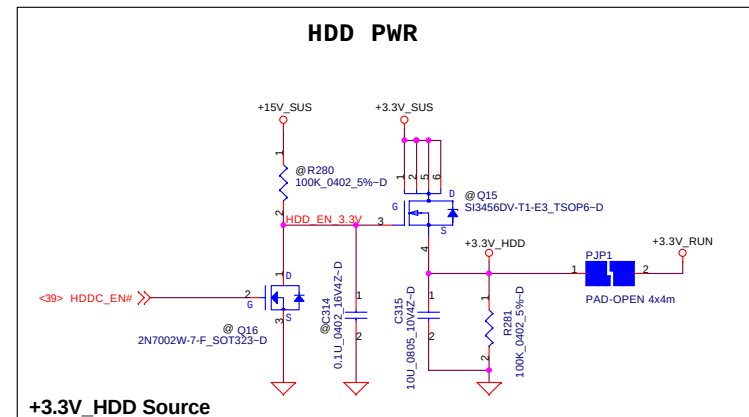
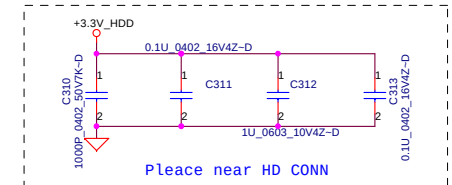
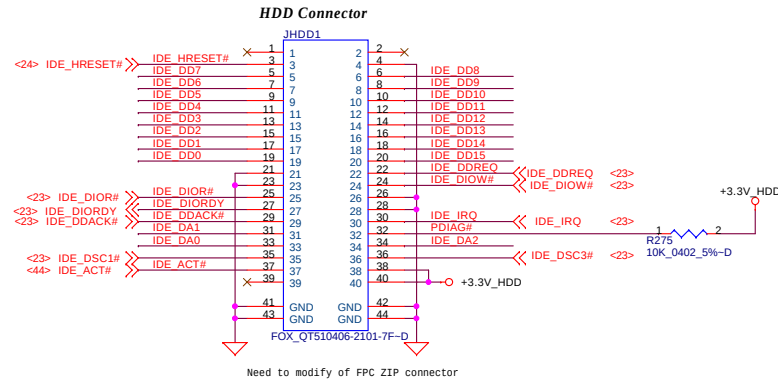
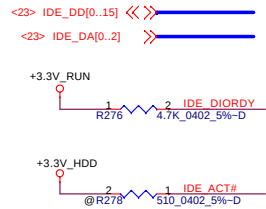
ICH7(1/4)

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Date: Friday, May 12, 2006 Sheet 22 of 59

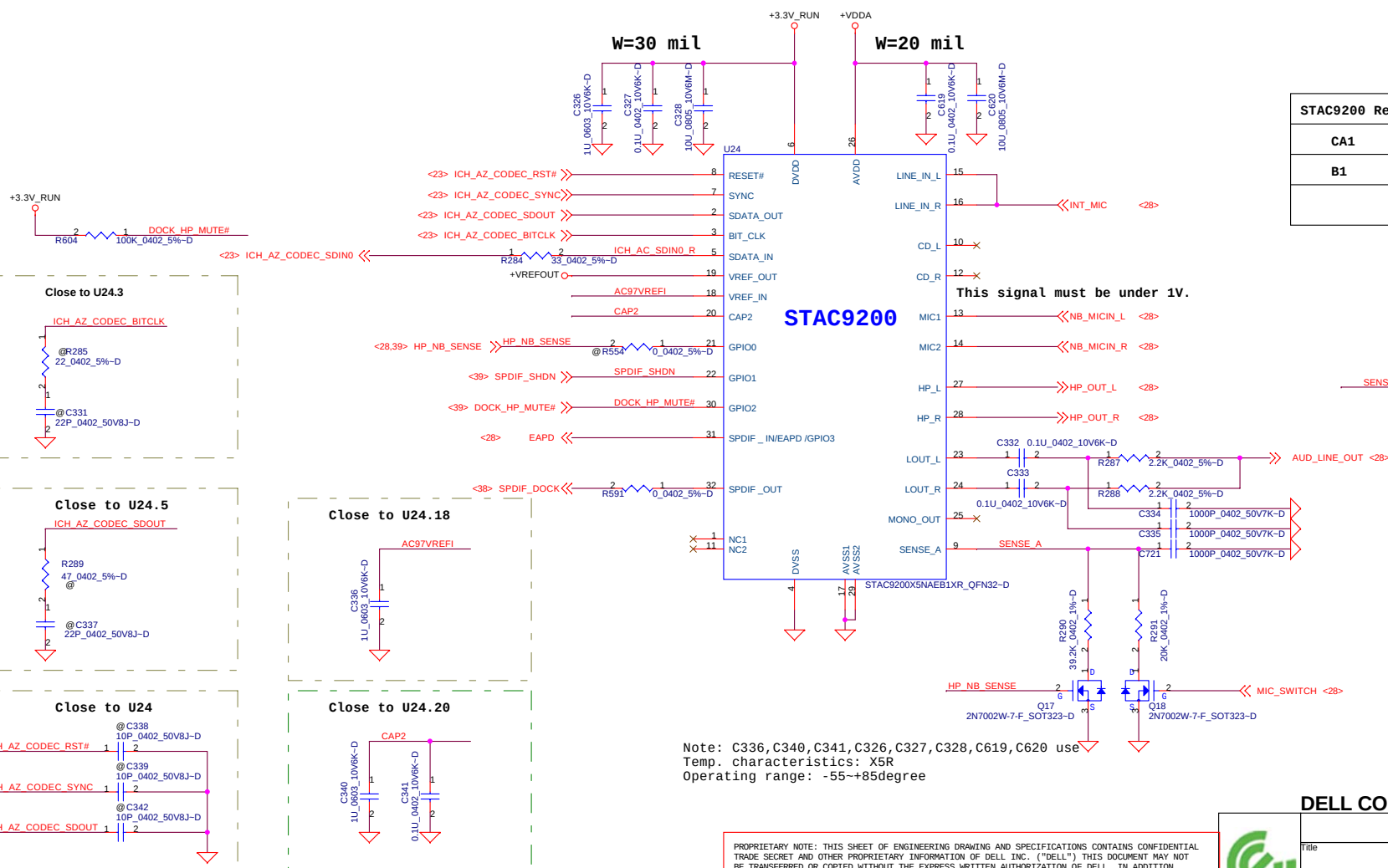
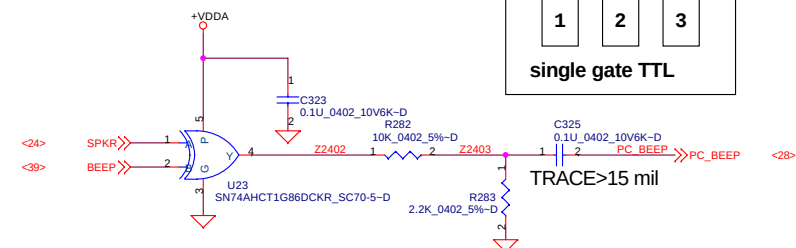
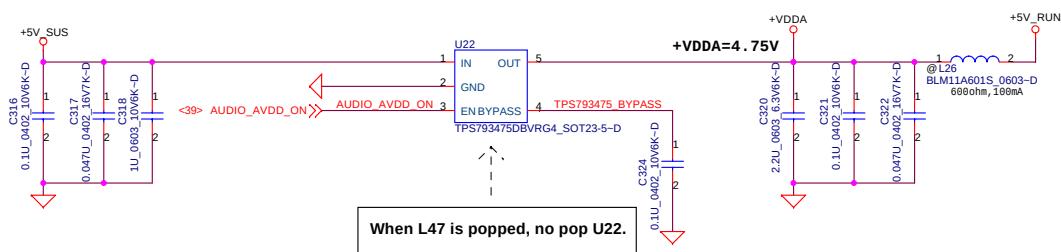
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Title IDE HDD Connector			
Size	Document Number		Rev
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STAC9200 Rev.	R22	R109
CA1	5.11K	10K
B1	39.2K	20K

Note: C336, C340, C341, C326, C327, C328, C619, C620 use
Temp. characteristics: X5R
Operating range: -55~+85degree

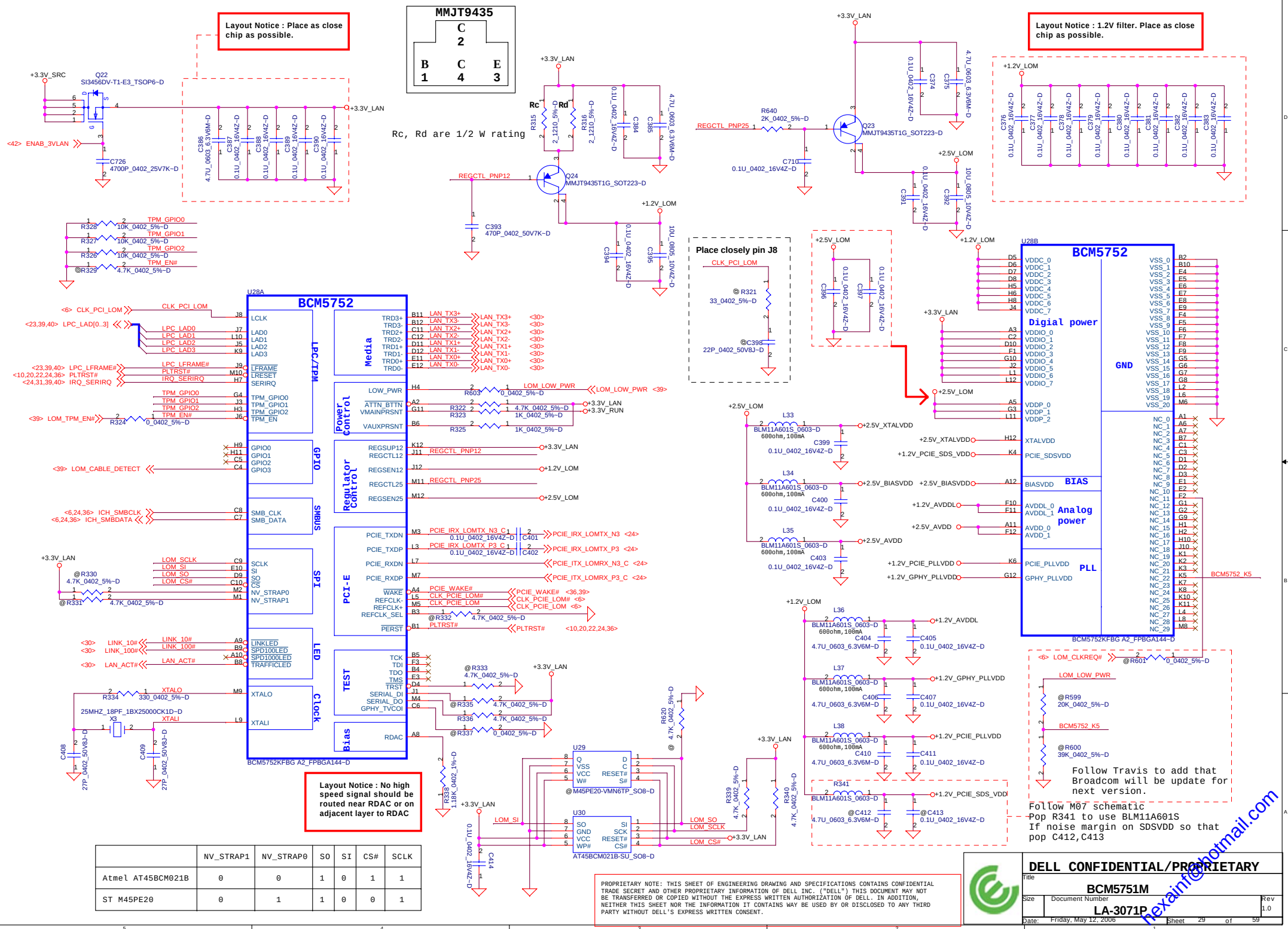
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Azalia (HD) Codec

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	NV_STRAP1	NV_STRAP0	S0	SI	CS#	SCLK
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

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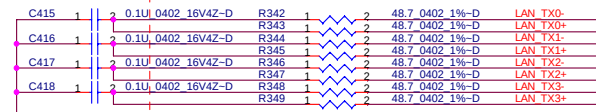


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BCM5751M

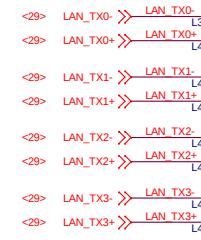
	LA-3071P	1.0
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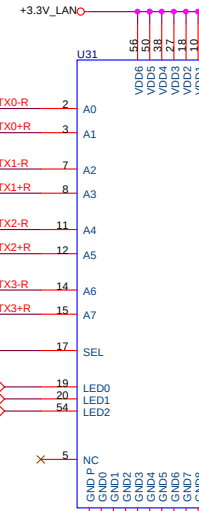


Layout Notice : Place termination as close as ASIC as possible

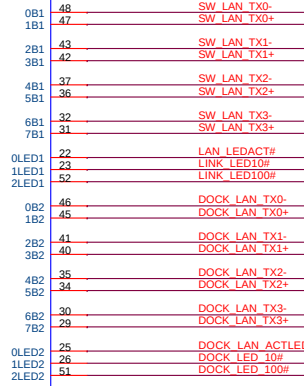
The resistors need at least 1/16W



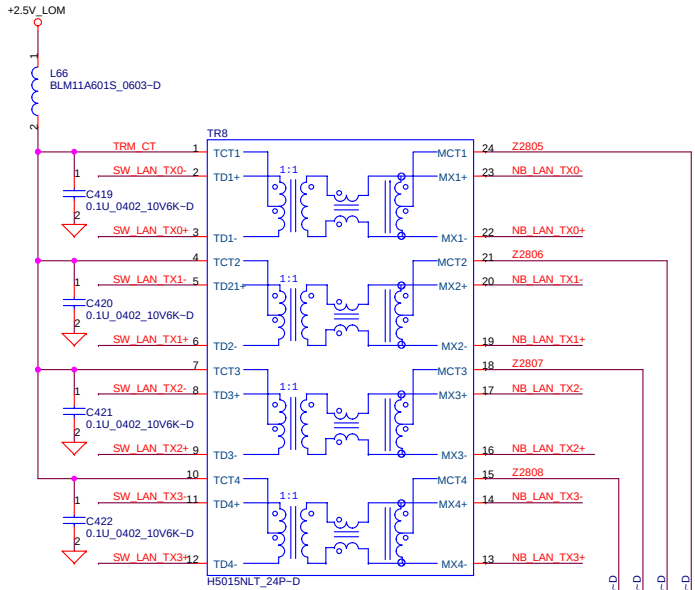
Layout Notice : Place bead as close PI3L500 as possible



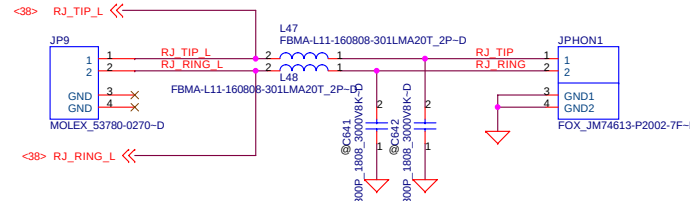
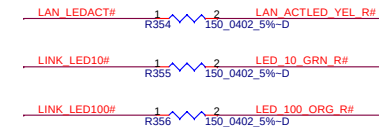
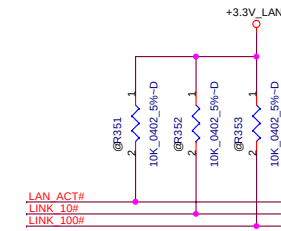
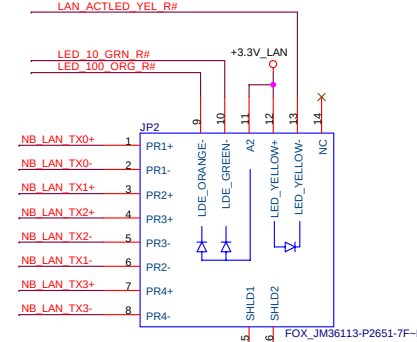
LAN ANALOG SWITCH



TO DOCK



GND CHASIS



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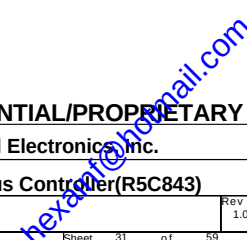


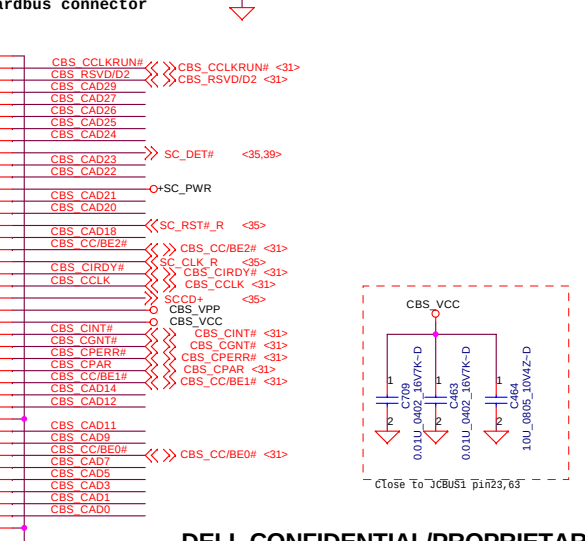
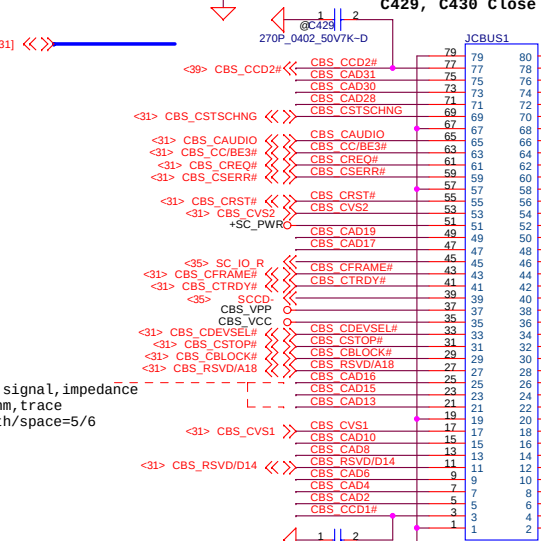
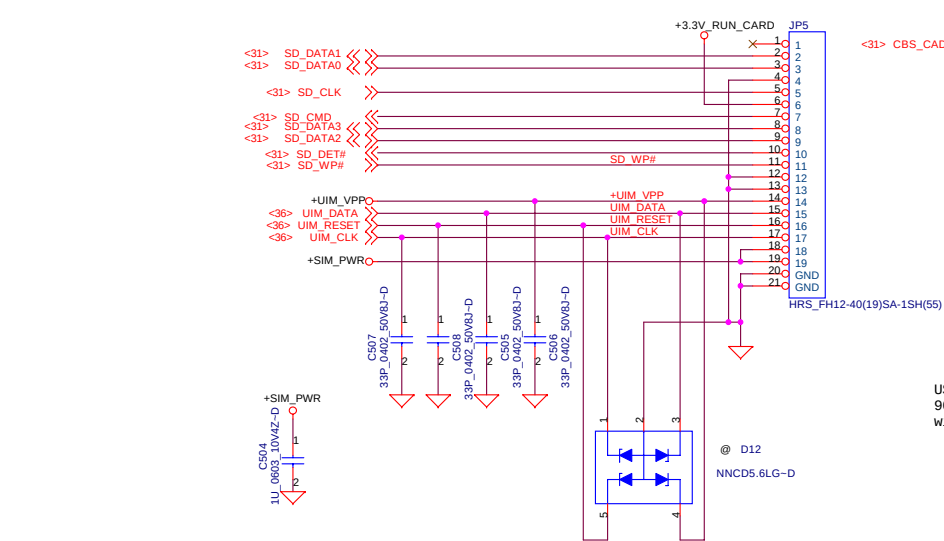
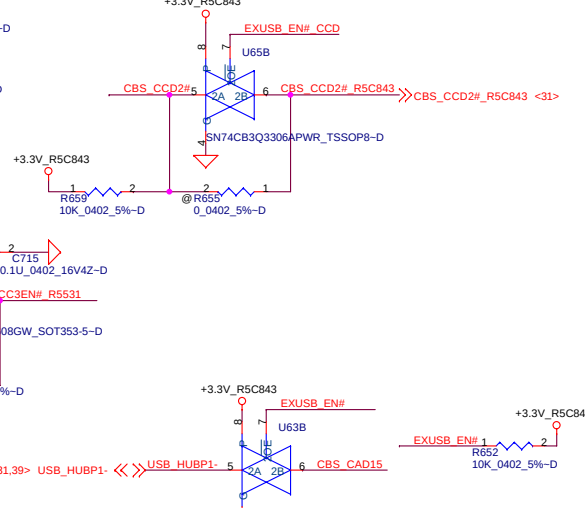
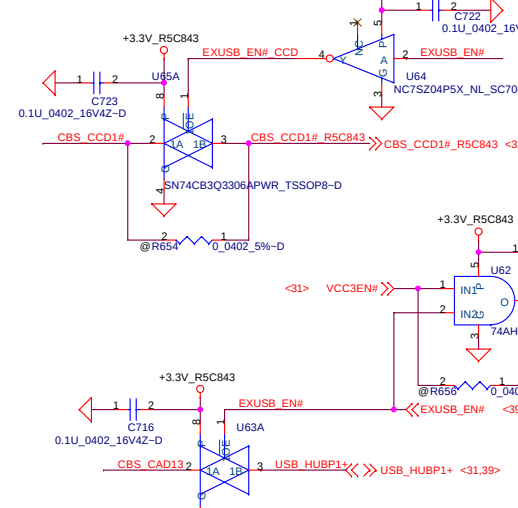
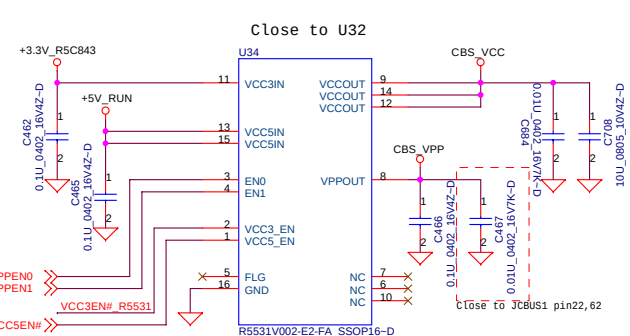
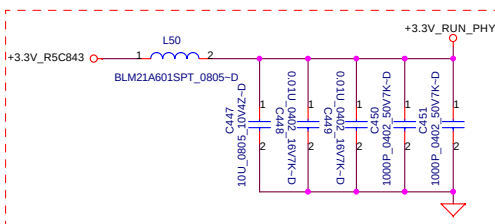
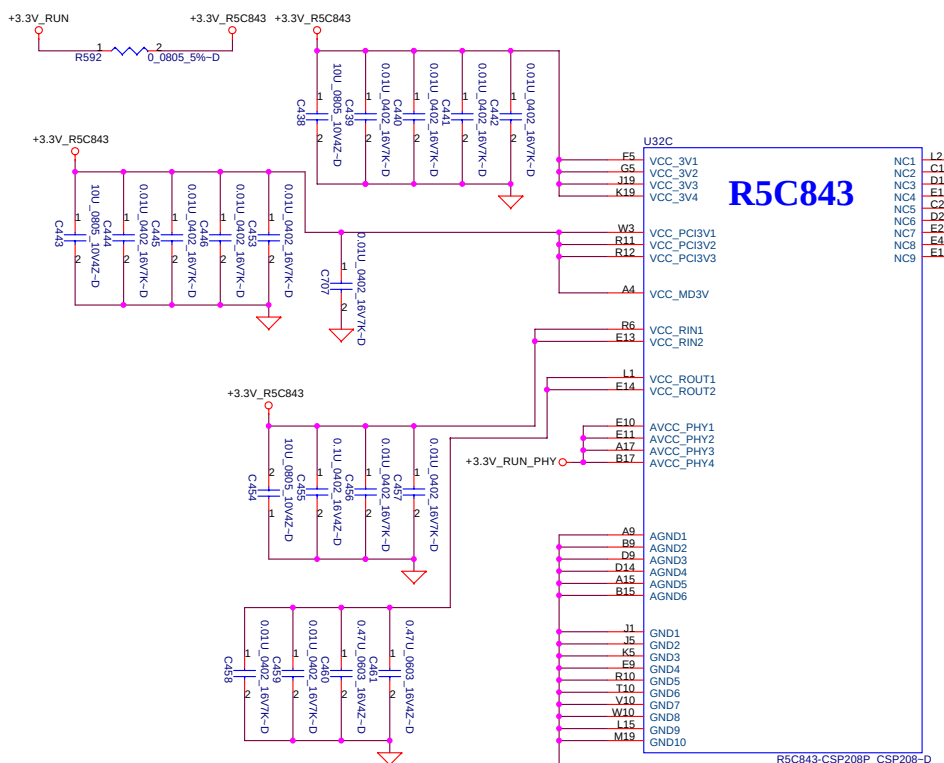
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LAN TRANSFORMER

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SIM & SD CARD will combine together, the connector will update to 18pin

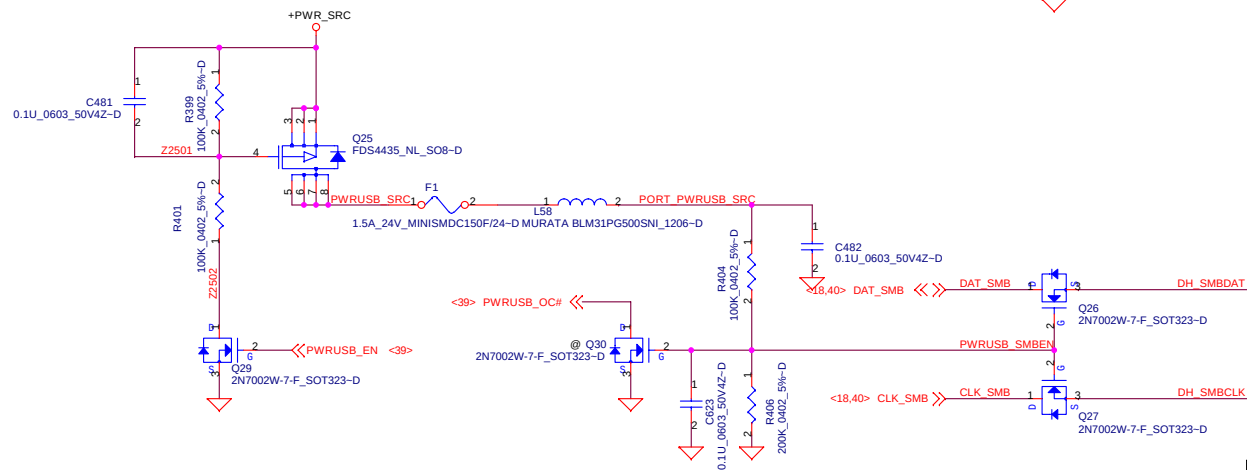
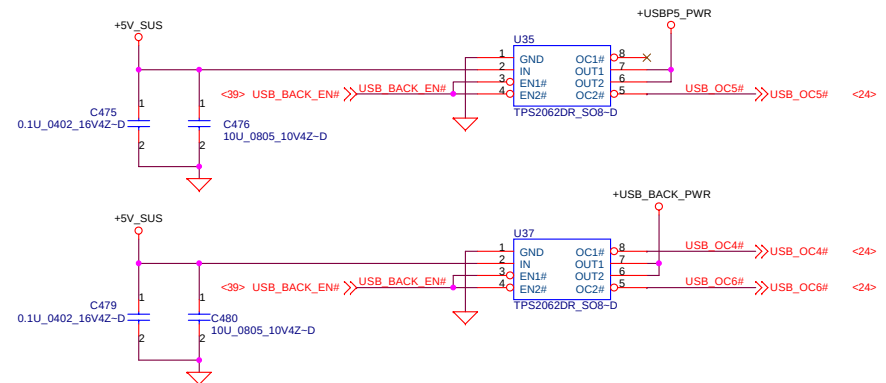
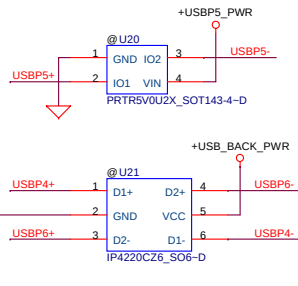
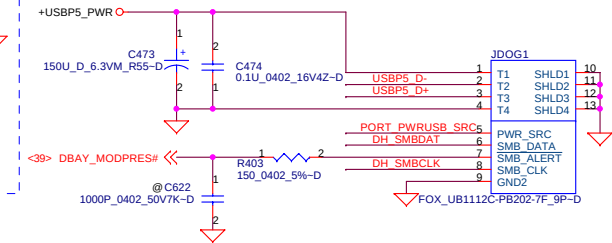
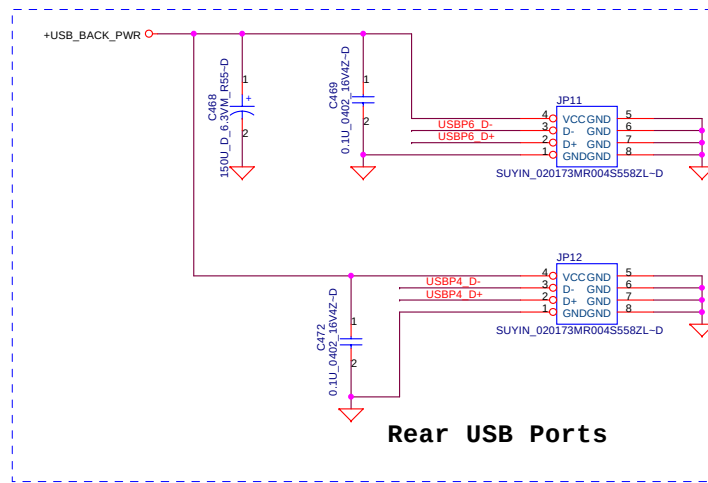
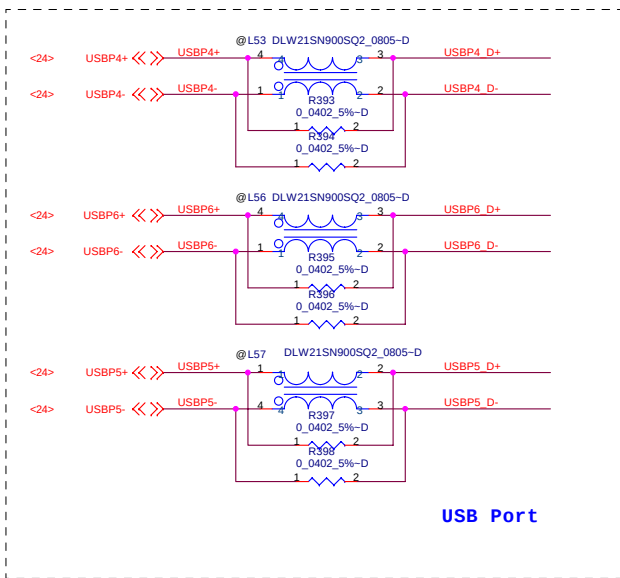
USB signal, impedance 90ohm, trace width/space=5/6

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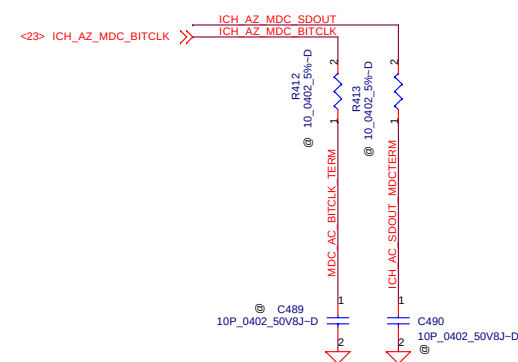
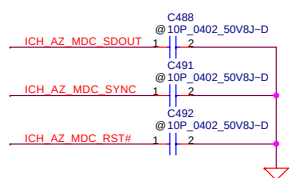
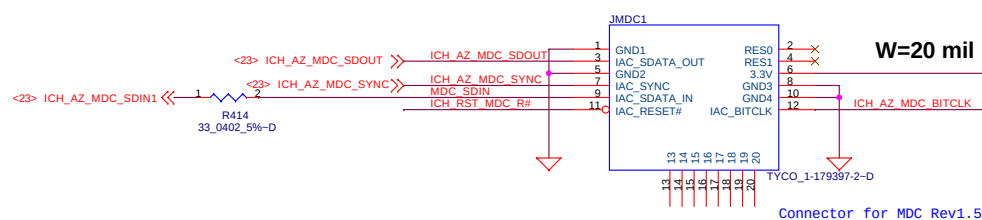
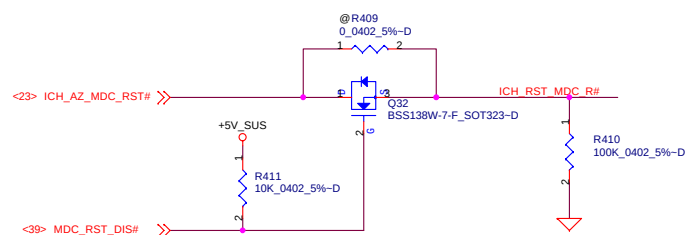
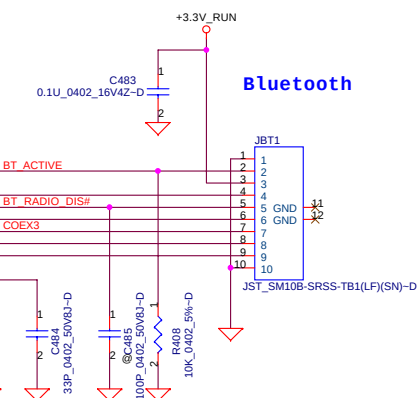


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CardBus/SD card Socket		
File	Document Number	Rev
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Compal Electronics Inc.			
USB 2.0 Port			
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New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12

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Compal Electronics, Inc.

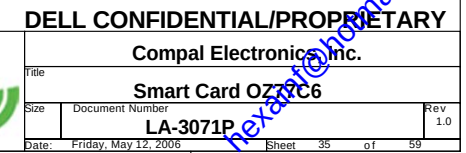
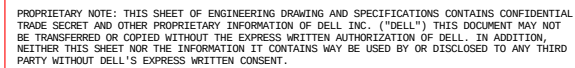
BT PORT & MDC

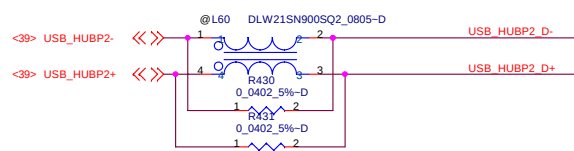
LA-3071P

Rev	1.0
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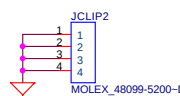
Date: Friday, May 12, 2006

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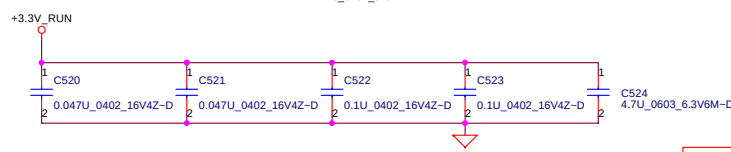
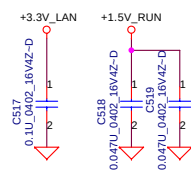
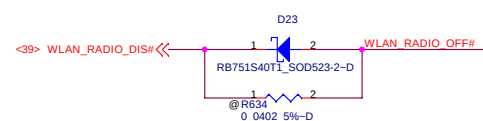
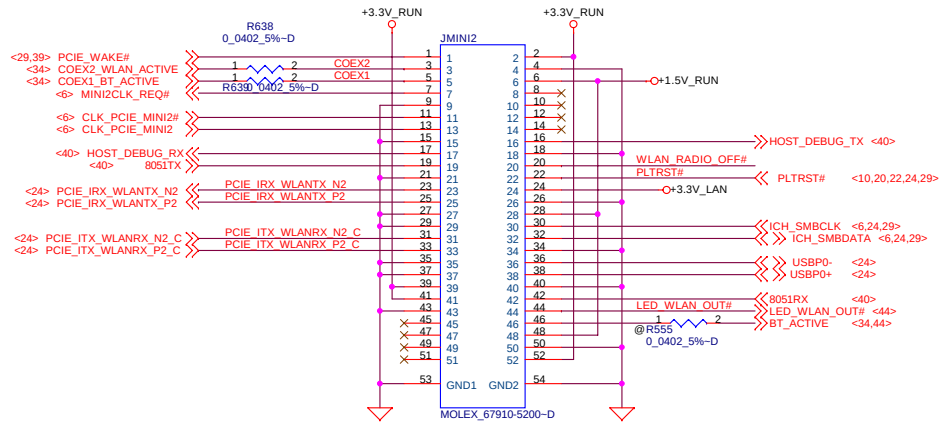
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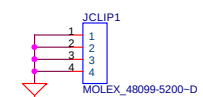
Mini Card Wire less LAN



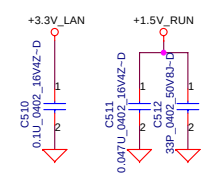
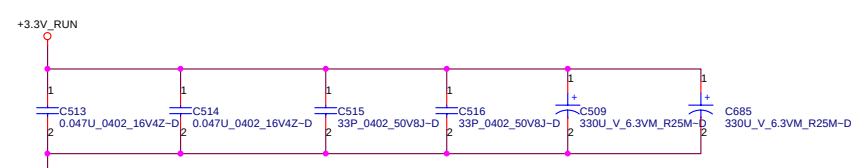
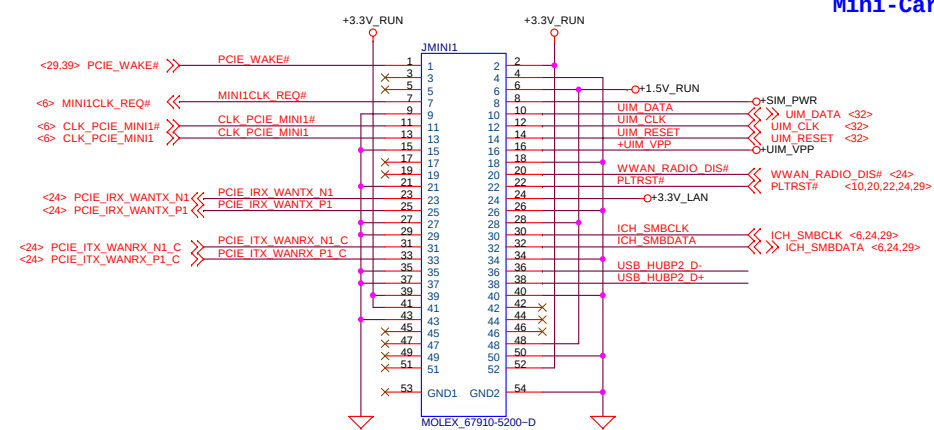
Mini-Card Latch



Mini Card Wire less WAN



Mini-Card Latch



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA

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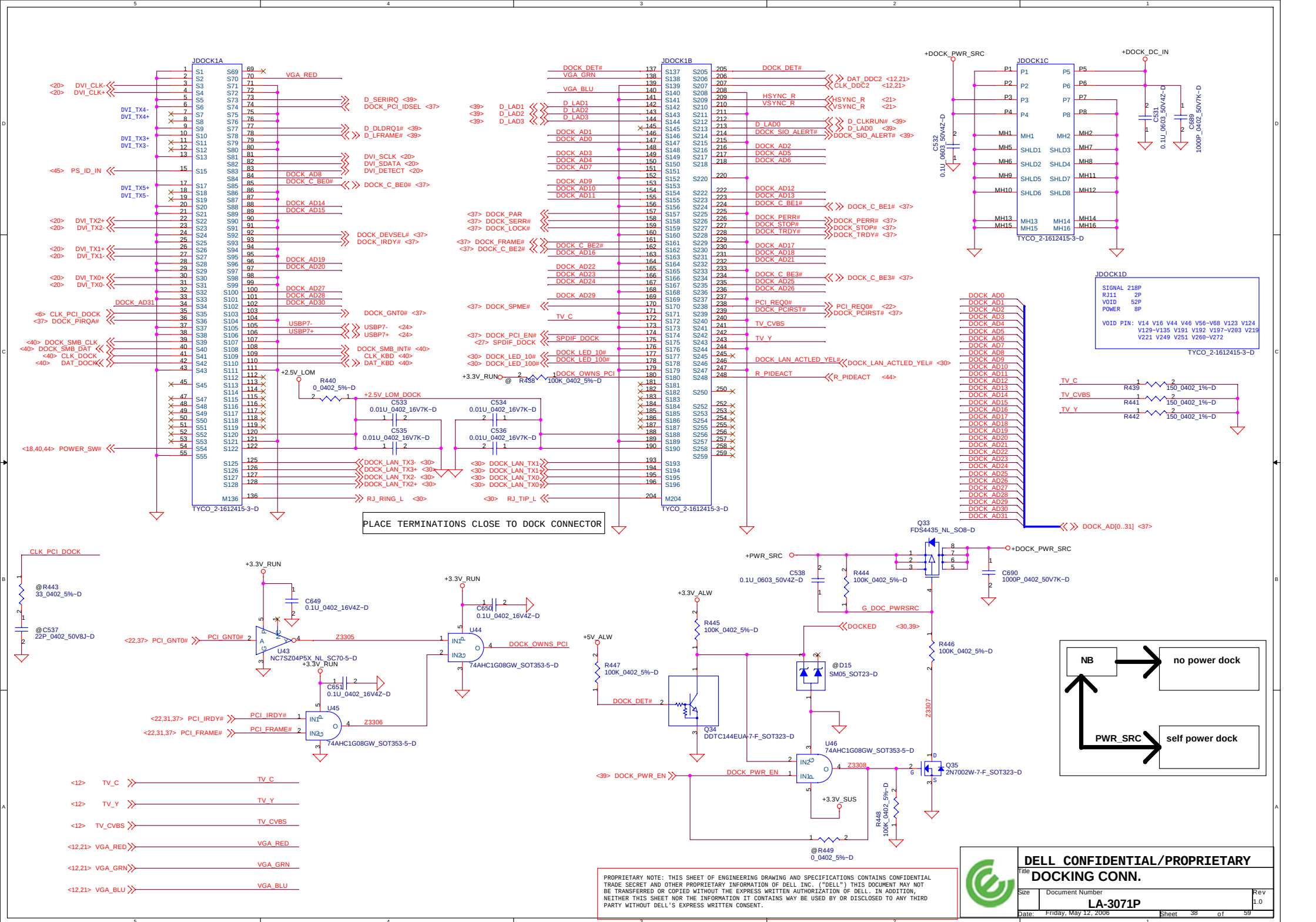
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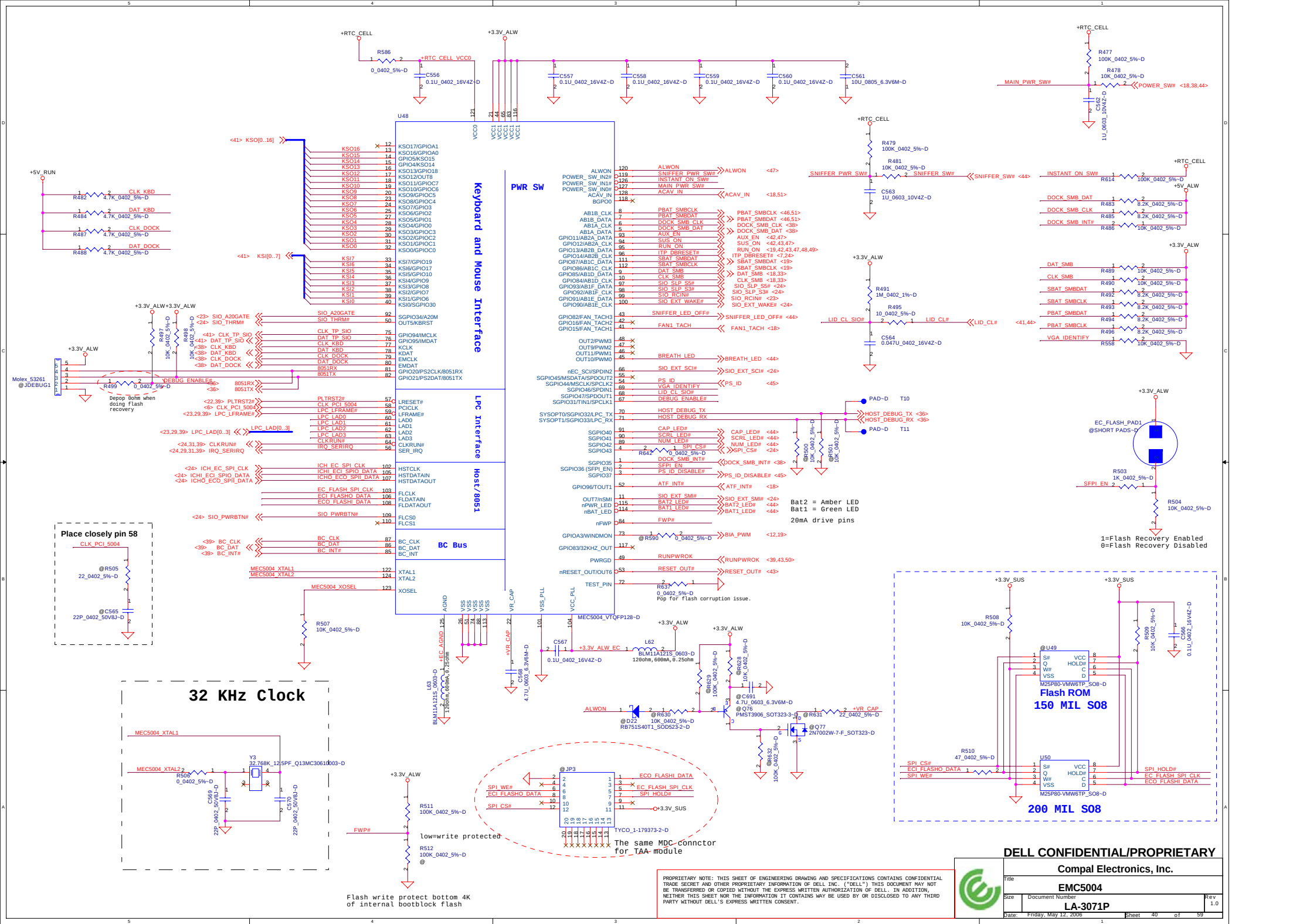
Compal Electronics, Inc.

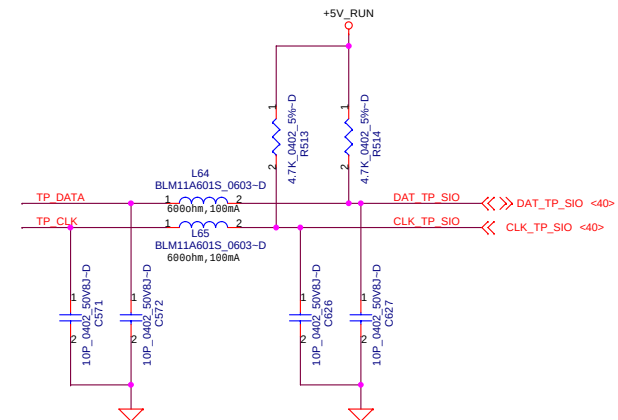
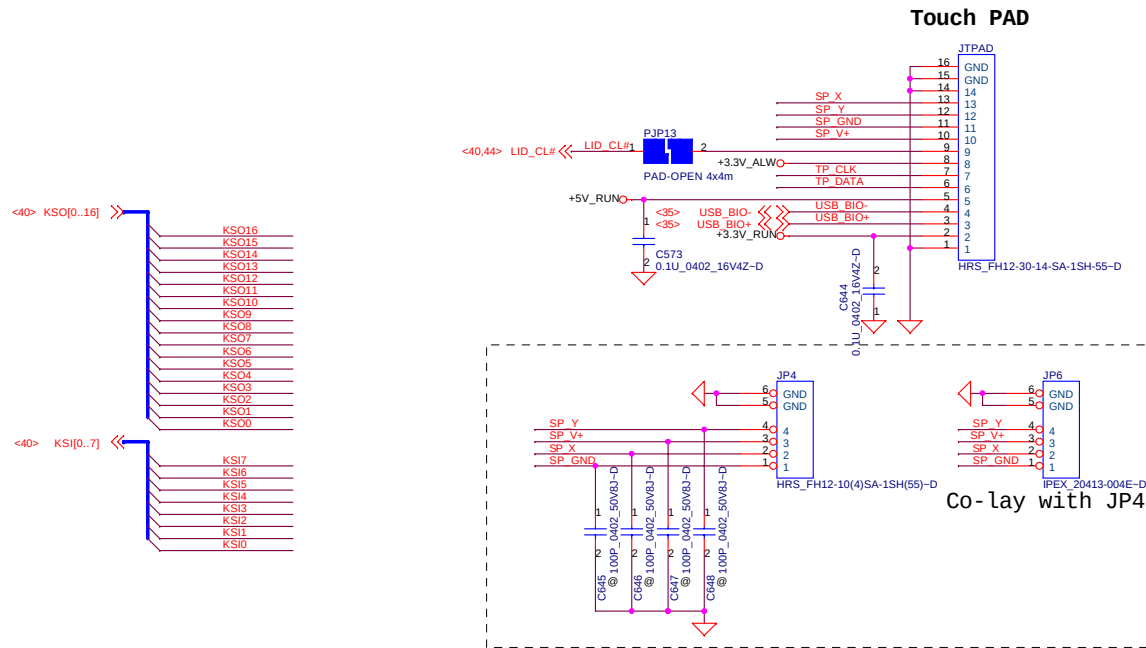
Mini Card

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Part Number	Description
PK230005C8L	SPK PACK 00B 1W 80HM

Part Number	Description
DC000002T0L	PCMCIA FOXCONN ICA80501-CR-4F

Part Number	Description
DC02000900L	H-CONN SET 00B M/B-B/T

Part Number	Description
DC02000900L	H-CONN SET 00B M/B-MDC

Part Number	Description
DA30000101L	FPC 00B LF-3072P REV1 1/P FPC WITH 810

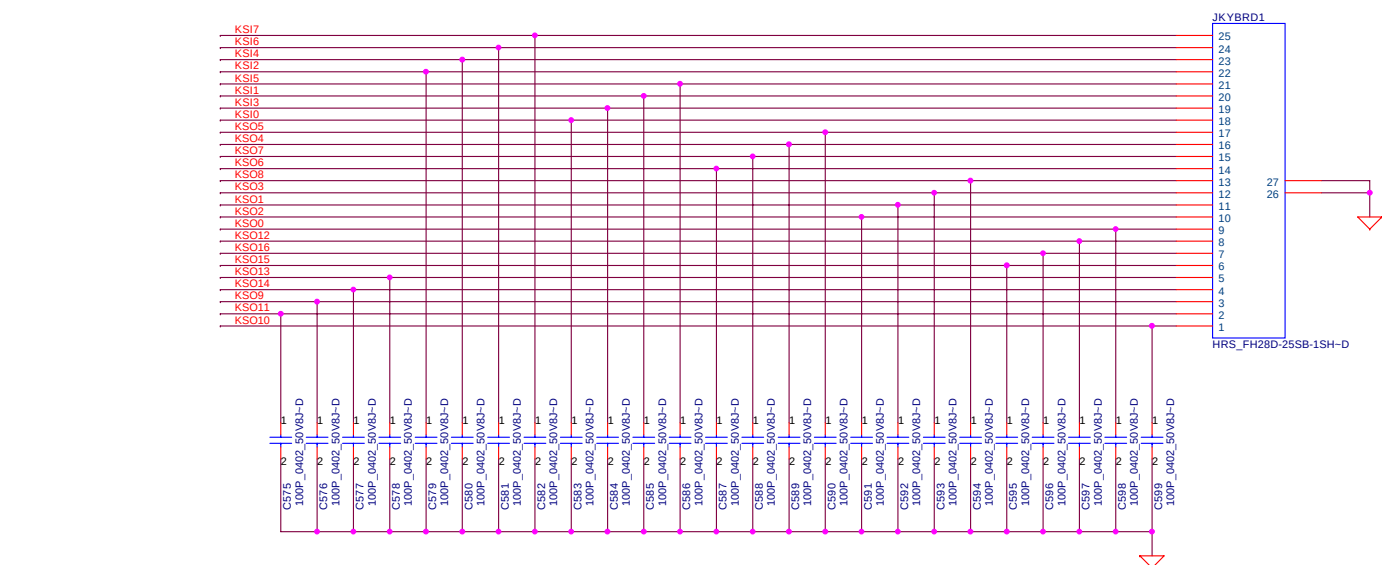
Part Number	Description
DC02000900L	H-CONN SET 00B MB-LCD 12 WXGA

Part Number	Description
DA300001N1L	FPC 00B LF-3071P REV1 HITACHI

Part Number	Description
GC020008000	BATT CR2025 W/CABLE 170MAH MB 00B 0FD

Part Number	Description
PK000003M0L	TRACK PAD ALPS KEDDEN10A BIOSENSOR

Part Number	Description
DA300001S1L	FPC 00B LF-3073P REV1 LED FPC



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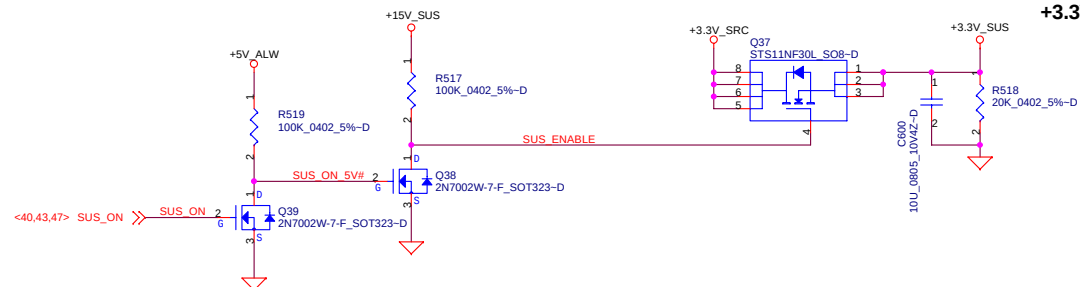
INT KB & FT & LID & TOUCH PAD

LA-3071P

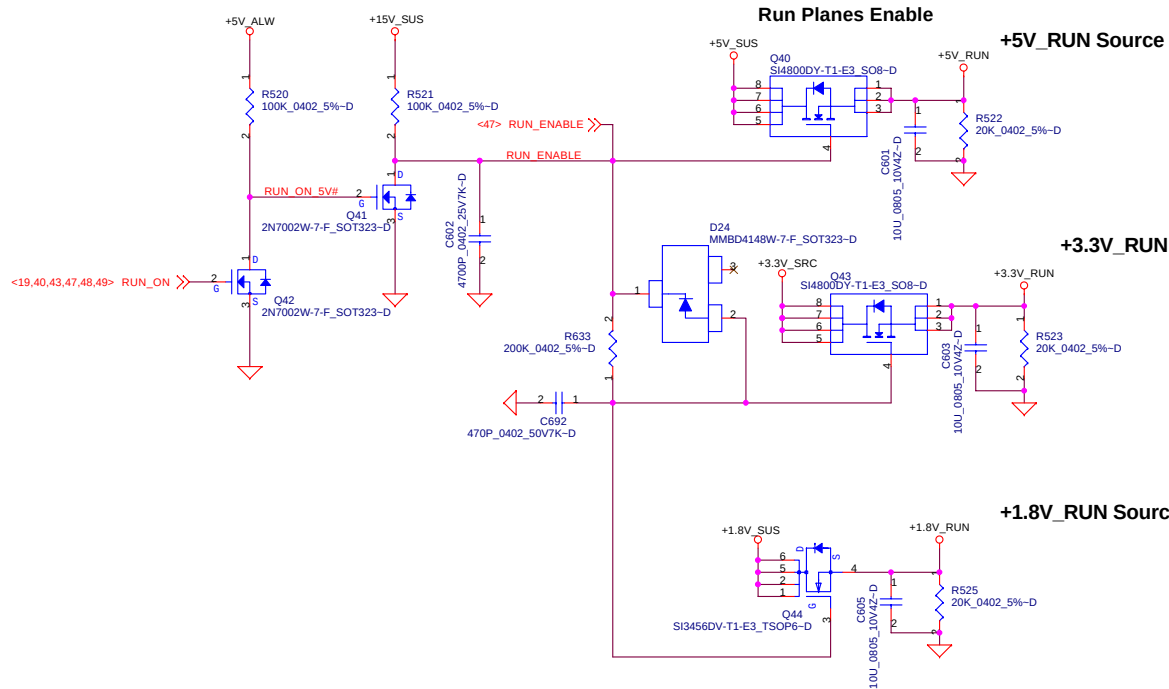
Rev 1.0

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DC/DC Interface

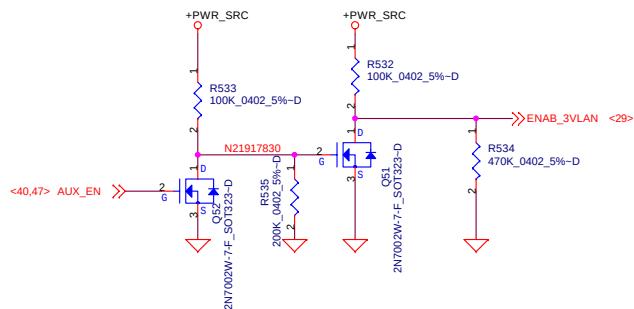
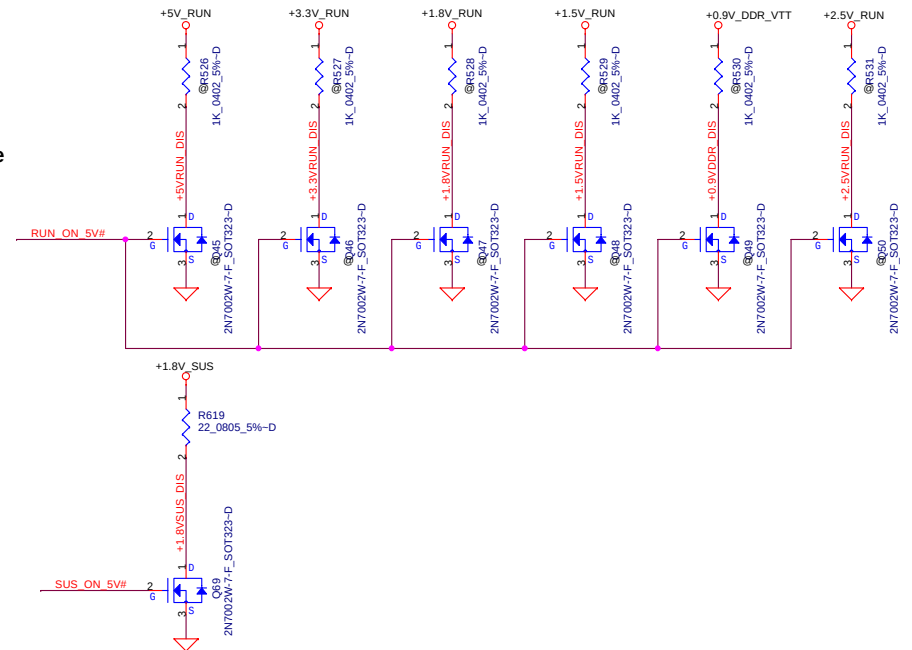


+3.3V_SUS Source



+1.8V_RUN Source

Discharge Circuit



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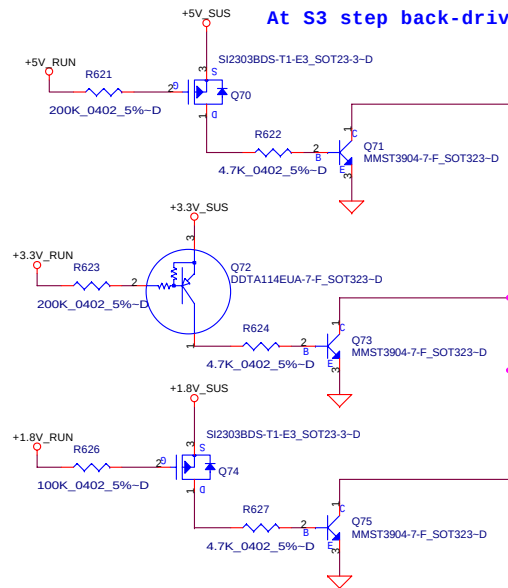
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POWER CONTROL

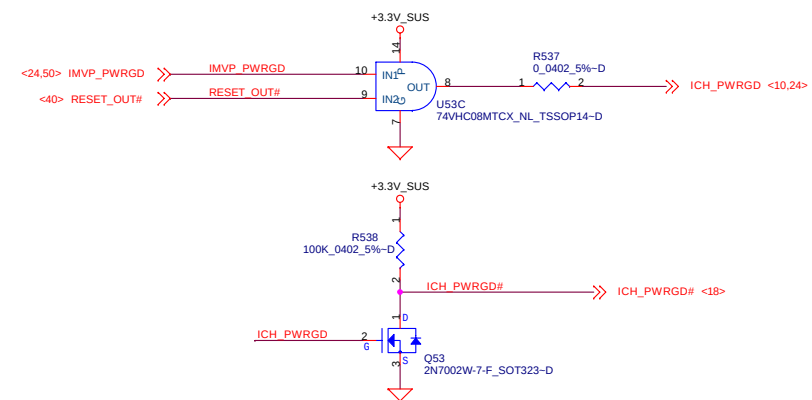
LA-3071P

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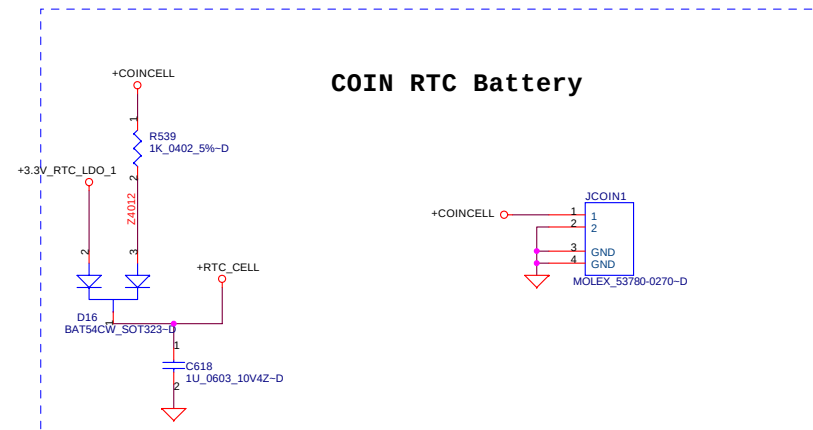
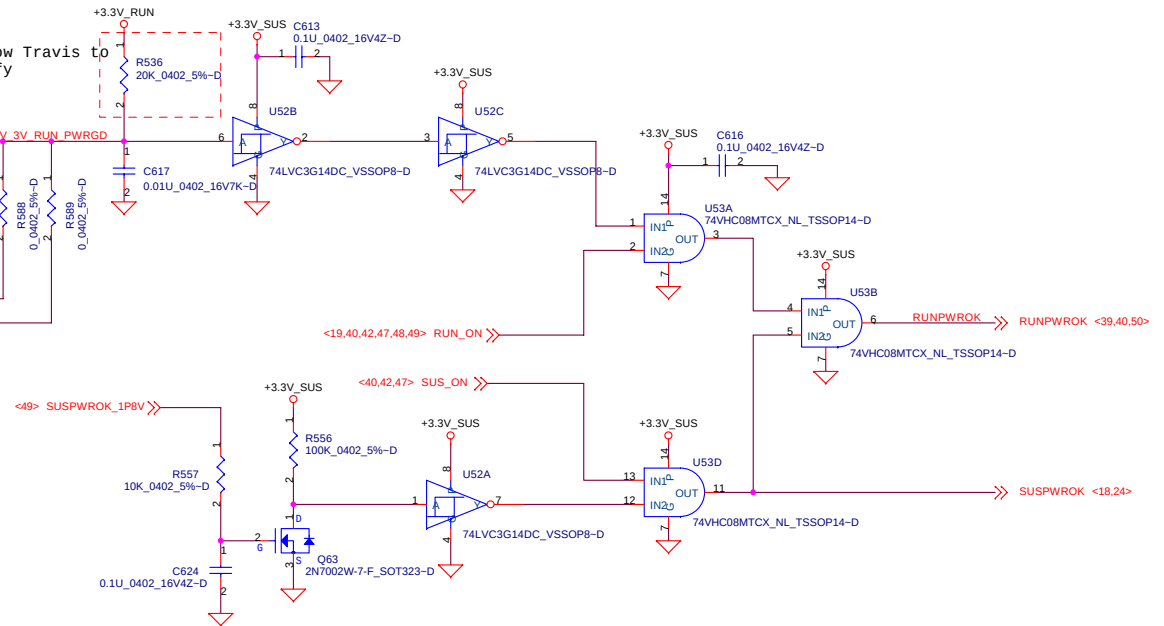
At S3 step back-drive: 78mV, change to SI2303



At S3 step back-drive:198mV, change to SI2303



Follow Travis to
modify

**COIN RTC Battery**

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Power Good

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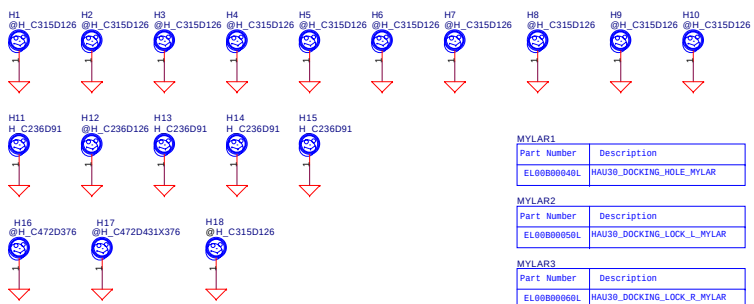
INITIAL/PROPRIETARY

Electronics, Inc.

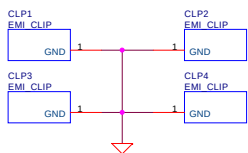
Good

1P

Rev 1.0



MDC Cable latch



Part Number	Description
EL00800040L	HAU30_DOCKING_HOLE_MYLAR

Part Number	Description
EL00800056L	HAU30_DOCKING_LOCK_L_MYLAR

Part Number	Description
EL00800066L	HAU30_DOCKING_LOCK_R_MYLAR

Part Number	Description
EL00800070L	HAU30_MYLAR_DOR2

Part Number	Description
EL008000800	HAU30_MYLAR_WLAN_MAA

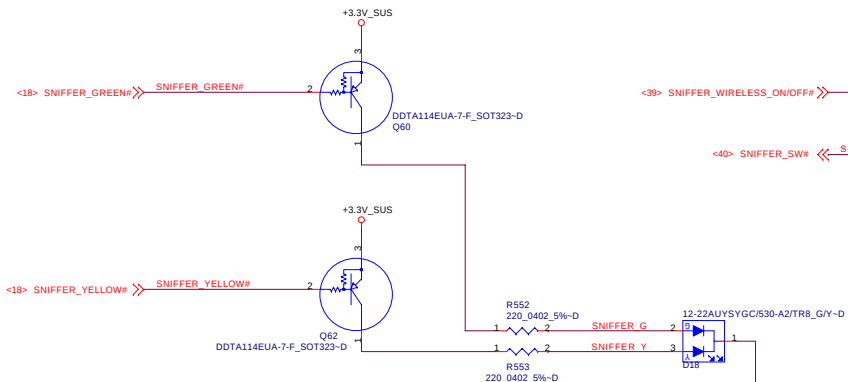
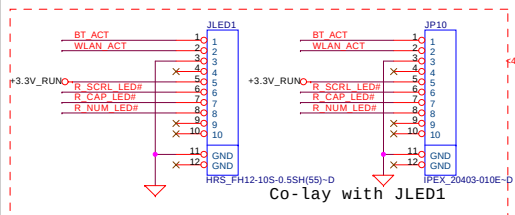
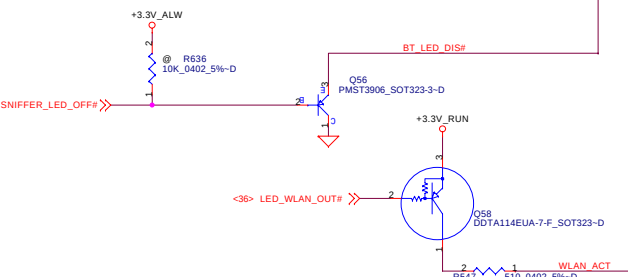
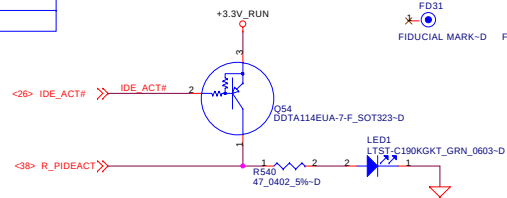
Part Number	Description
EL008000X00	HAU30_MYLAR_HDD

Part Number	Description
EL008000A0L	HAU30_MYLAR_FAN

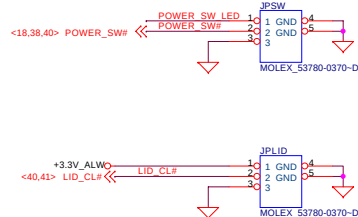
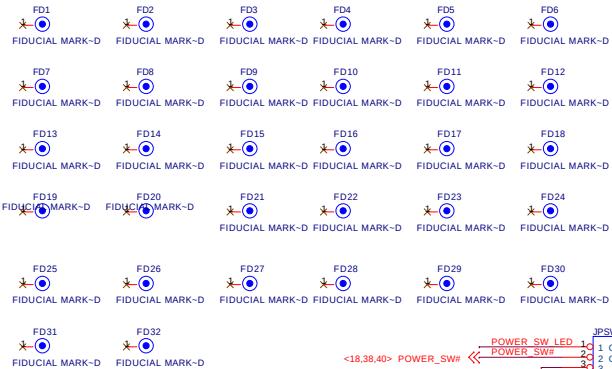
Part Number	Description
FH00800066L	HAU30_MTC_RUBBER

Part Number	Description
EL008000000	HAU30_RUBBER_MDC

Part Number	Description
MAA00015360	SCREW M M 2.00 3.0L K 4.60 2K NL + CR3+



Fiducial Mark



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PAD and Standoff

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IMVP-6 solution for Yonah ULV: 1-phase/9A

PL13
FBMA-L11-321611-800LMA40T

Thermistor PH1 should be placed close to the hot spot of the VR

NOTE: (Connection VCore output Cap GND)
De-populate PR113 and PR115 when CPU is present

NOTE

Single Core (YONAH ULV)	- Choke: PL14 is 0.88u H - MOS: PQ27 - PR104 is 309K.(OCP:14A) - PR114 is 2.37K.(Load Line: -5.1m) - PR101 is 10K. - PR88 is 820P ; 8. STUFF PC80 - PR90 is 390P.
Dual Core (YONAH ULV)	- Choke: PL14 is 0.45u H - MOS: PQ27. - PR104 is 215K.(OCP:20A) - PR114 is 5.76K.(Load Line: -2.1m) - PR101 is 20K. - PR88 is 470P ; 8. NO-STUFF PC80 - PR90 is 470P.
Dual Core (MEROM ULV)	- Choke: PL14 is 0.45u H - MOS: PQ16 and PQ27 - PR104 is 215K.(OCP:20A) - PR114 is 5.76K.(Load Line: -2.1m) - PR101 is 20K. ; 8. NO-STUFF PC80 - PR88 is 470P - PR90 is 470P.

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+VCORE

LA-3071P

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7	H/W	10/14	INTEL	H_DPRSTP# & H_DPSLP# not need pull down resistor for Intel request	Remove R85,R86	0.2
2	15	H/W	10/14	Steve	S0-DIMMA SM Bus address define need change from A4 to A2 for 945GMS DDR support one channel issue.	Change R135 from pull down to pull up +3.3V_RUN Change R136 from pull up to pull down and change from 100K to 10K	0.2
3	41	H/W	10/14	Steve	Touch PAD module issue	Change JTPAD1.14 from +3.3V_RUN to GND	0.2
4	42	H/W	10/14	Steve	Power sequence issue that +1.8V_RUN too late on +VCC_CORE	Remove R524,C604	0.2
5	43	H/W	10/14	Steve	Add +5V,+3V,+1.8V_RUN power sequence schematic to control sequence	Add R621,R622,R623,R624,R626,R627,Q70,Q71,Q72,Q73,Q74,Q75	0.2
6	17	H/W	10/15	Steve	945GMS support CKE0,CS0#,ODT0 to control on board RAM,so remove CKE1,CS1#,ODT1	Remove RN76,RN80 and add R625,previously T13,T14,T15 for DDR_CKE1,DDR_CS1#,M_ODT1	0.2
7	39	H/W	10/15	Steve	Change BID from X00 to X01	Un-pop R473,pop R469	0.2
8	44	H/W	10/15	Steve	Remove CAP,NUM,SCRL,BT,WLAN LED from M/B to FFC and CAP,NUM,SCRL direct driving LED from MEC5004.	Remove LED6,LED7,LED8,LED9,LED10,Q64,Q65,Q66,add JLED1	0.2
9	19	H/W	10/17	Steve	945GMS control panel backlite (BIA_PWM), the voltage level is 3.3V, so don't need add component for voltage level shift.	Remove U54	0.2
10	40	H/W	10/17	Steve	Resolve EC code damage issue	Reserved R628,R629,R630,R631,R632,C691,Q76,Q77,D22(depopped)	0.2
11	31	H/W	10/27	Steve	Follow M07_R5C843 refer schematic to modify.	Change C424,C425 from 22P to 12P	0.2
12	42	H/W	10/27	Steve	Resolve IMVP_PWRGD glitch during power on/S3 resume	Add R633,C692	0.2
13	9	H/W	10/27	Steve	For Dual Core CPU action	Reserved C693,C694,C695,C696,C697,C698,C699,C700,C701,C702,C703,C704,C705,C706(depopped)	0.2
14	36	H/W	10/27	Steve	Support WoW function for prevent backdrive.	Add D23,no pop R634	0.2
15	34	H/W	10/27	Steve	Keep the BT LED off when the SNIFFER is turned on.	Add R635,R636,Q78	0.2
16	40	H/W	10/31	Steve	Resolve EC flash corruption issue.	Add R637 to pull down.	0.2
17	9	H/W	11/1	Steve	Support one core CPU that follow Intel request just pop 8pcs of 22uF MLCC Cap.	Pop C21,C23,C26,C28,C29,C31,C34,C36	0.2
18	42	H/W	11/3	Dell	Correct C692 value	Change to 470PF	0.2
19	34	H/W	11/3	Dell	SNIFFER_LED_OFF# should be pull up to +3.3V_SUS	Change to pull up power source from +5V_SUS to +3.3V_SUS	0.2
20	36	H/W	11/7	CoE	Nimi-Card Reset change to PLTRST#	Follow CoE M07-Nimicard-a07	0.2
21	36	H/W	11/7	CoE	Nimi-Card WLAN COEX2_WLAN_ACTIVE AND COEX1_BT_ACTIVE ADD 0 ohms: R638 and R639	Follow CoE M07-Nimicard-a07	0.2

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Title Changed-List History 1			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	36	H/W	11/7	CoE	C685 STUFFED	Follow CoE M07-Nimicard-a07	0.2
23	32	H/W	11/7	CoE	SIM Module C505, C506, C507, C508 Change to 33P_0402, and C508 stuffed	Follow CoE M07-Nimicard-a07	0.2
24	44	H/W	11/7	Steve	Sniffer LED Indicator Error	Swap D18 pin2,3 of LED	0.2
25	24	H/W	11/8	CoE	R370 Move to ICH7 side	Follow CoE M07-ICH a07	0.2
26	31	H/W	11/8	CoE	C428, C429, C430 add the note to close connector	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
27	31	H/W	11/8	CoE	C424, C425 add a note to change the value after measure the starting value	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
28	31	H/W	11/8	CoE	C431 change from 0.01u to 0.1u	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
29	31	H/W	11/8	CoE	+SD_VCC change to +3.3V_RUN_CARD	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
30	32	H/W	11/8	CoE	VCC_PCI/ VCC_MD3V add C707_0.01u	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
31	32	H/W	11/8	CoE	R389_100 remove	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
32	32	H/W	11/8	CoE	C448/ C449 /C684 change to 0.01u_0402	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
33	32	H/W	11/8	CoE	VCC_CBS add C708_10u and C709_0.01u	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
34	32	H/W	11/8	CoE	+VCC_CBS rename to VCC_CBS, +CBS_VPP rename to CBS_VPP	FollowM07_R5C843_REF_SCHEMATICS_A00	0.2
35	44	H/W	11/8	CoE	Bluetooth LED disable function when Sniffer Active update, follow travis: R636 pull-up to +3.3_ALW, Q56 --> 3906, R635 --> remove. But depop R636	Follow Travis	0.2
36	29	H/W	11/9	Brocadcom	Change RDAC for Broadcom request.	Change R338 from 1.15K to 1.18K.	0.2
37	34	H/W	12/8	Steve_Wang	Resolve Bluetooth LED always light	Pop R408	0.3
38	9	H/W	12/8	Steve_Wang	Separate BOM type for different CPU.	Pop 10 for Signal core 1.06G Pop 20 for Singal core 1.2G Pop 30 for Dual core 1.06G	0.3
39	29	H/W	12/13	Steve_Wang	Prevent Q23 damage issue for transfor +3.3V_LAN to +2.5V_L0M	Add R640,C710	0.3
40	20	H/W	12/13	Steve_Wang	Resolve DVI test fail issue	1. Change C245,C236 from 0.1U to 10U 2. Change R169,R170,R171,R172 from 300ohm to 110ohm 3. Change R175 from 300ohm to 220ohm 4. Pop C238,C247	0.3
41	26	H/W	12/13	Steve_Wang	Resolve-HDD_EN# have spike when power on	Change R279 from 100K to 4.7K	0.3
42	39	H/W	12/13	Steve_Wang	Change BID from X01 to X02	Unpop R469,R474; pop R470,R473	0.3

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Title Changed-List History			
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43	39	H/W	12/14	CoE	C638 STUFFED	Follow CoE M07_EC_Latitude_A07	0.3
44	26	H/W	12/14	CoE	Change HDD_EN# signal from ICH to SIO	1.Change HDD_EN# from ICH to ECE5018 pin106. 2.Add R644 to pull-up +3.3V_ALW 3.Delete R279 to pull-down 4.Rename signal at ICH to RSVD_HDDC_EN# and add Test Point	0.3
45	24,40	H/W	12/16	CoE	SPI_CS# have spike over 4.5V when power on	Add R641,R642 damping to prevent.	0.3
46	31	H/W	12/19	MikeCC_Huang	Measure SD EA find Data overshoot,undershot over 3.3V	Add R645,R646,R647,R648 damping to meliorate.	0.3
47	21	H/W	12/20	DELL	+CRT_VCC current limit issue	Add 1206 Res of R649.	0.3
48	28	H/W	12/21	DELL	Fine tuning AUD_LINE_OUT signal	Change C368 from 0.0047u(X5R) to 4700P(X7R)	0.3
49	24	H/W	12/21	DELL	Follow DELL request	Change R265 contact from R641 pin1 to pin2	0.3
50	27,28	H/W	12/21	DELL	Follow DELL request	Change Audio by-pass cap to X5R	0.3
51	18	H/W	12/21	DELL	Follow DELL request	Add VSET,LD0_SET note	0.3
52	21	H/W	12/21	COE	Follow COE M07_CRT_LVDS_DVI rev A07schematic	Add R650,R651	0.3
53	42	H/W	12/21	COE	Follow COE M07_System power sequence_A07 schematic	Add D24 for fast turn Off FET	0.3
54	43	H/W	12/21	COE	Follow COE M07_System power sequence_A07 schematic	Change Q63 from MMBT3904 to 2N7002 that it has good margin to turn	0.3
55	28	H/W	12/22	COE	Follow COE M07_AUDIO_A05 schematic	Add EAPD signal & Q79 for power saving control	0.3
56	29	H/W	12/23	Crystal EA	Follow vendor suggest to modify resistor to match crystal negative resistor EA	Change R334 from 200 to 330ohm	0.3
57	31	H/W	12/23	Crystal EA	Follow vendor suggest to modify cap to match crystal EA	Change C424,C425 from 12P to 18P.	0.3
58	21	H/W	12/23	RGA EA	For 1pix 1600x1200 rising/falling time over spec issue	Change L18,L19,L20 from 60ohm to 22ohm	0.3
59	39	H/W	12/23	Crystal EA	Follow vendor suggest to modify crystal	Change Y1 from 24MHz_20pF to 24MHz_12pF	0.3
60	30	H/W	12/26	DELL	Follow DELL resolution of test Media Slice,APR,DAPR return loss issue	1.Change R342,R343,R344,R345,R346,R347,R348,R349 from 49.9 to 48.7ohm 2.Change L39,L40,L41,L42,L43,L44,L45,L46 from 24NH to 39NH	0.3
61	30	H/W	2/18	EMI	EMI test ISN of LAN on 10/100 item fail.The solution are pop C421,C422 and change C419~C422 character from Y5Vto X5R	1.Pop C421,C422 2.Change C419~C422 character from Y5V to X5R	0.4
62	31	H/W	2/18	STEVE_WANG	System can't boot issue.	Unpop R609	0.4
63	28	H/W	2/27	DELL	Follow DELL request to modify amplifier gain from 10db to 15.6db for fix small sound on speaker issue	Unpop R311,R312; pop R310,R313	0.4
64	28	H/W	2/27	DELL	Follow DELL request to modify cap value from 0.047u to 4700p for best pop and click performance	Change C367,C369,C371 from 0.047U to 4700P	0.4
65	9	H/W	3/2	DELL	Follow Intel document to modify 330u 7mohm to 6mohm	Change C41,C42,C43,C44,C705,C706 from 330U 7mohm to 6mohm	0.4
66	12	H/W	3/2	DELL	Follow DELL request to add shunt caps between LVDS signal.	Add 10P_0402 of C711,C712,C713,C714	0.4
67	32	H/W	3/6	DELL	DELL support Express USB Card can't work on R5C843 issue.	Add schematic of U62,U63,U64,U65,C715,C716,C722,C723,R652,R654,R655	0.4

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68	39	H/W	3/7	DELL	DELL support Express USB Card can't work on R5C843 issue.	Reserve 0ohm of R653 for control Express card detect.	0.4
69	18	H/W	3/9	Thermal	Modify OTP thermal shut down to 91 degree.	Change R157 from 41.2K to 68K	0.4
70	31	H/W	3/10	Mikecc_Huang	SD bus signal overshoot/undershoot over spec.	Add C717,C718,C719C720	0.4
71	27	H/W	3/10	SIGMATEL	Follow sigmatel request to add cap for SENSE_A signal	Add 1000P cap	0.4
72	28	H/W	3/10	SIGMATEL	Follow sigmatel request to add NB_MUTE signal for control MAX4411 shutdown.	Add Q80 of NB_SENSE signal to control MAX4411 shutdown	0.4
73	28	H/W	3/10	SIGMATEL	Follow sigmatel request to add ESD diode for avoid High pol	Reserve D25	0.4
74	28	H/W	3/10	SIGMATEL	Follow sigmatel request for MIC BIAS.	Unpop R299,R300	0.4
75	35	H/W	3/10	DELL	Modiy USB_BIO-/USB_BIO+ ESD IC to choke	Add R657,R658; reserve L67,C724,C725; delete U55	0.4
76	35	H/W	3/10	Mikecc_Huang	Advoid LID_CL# have some error on ALPS touchpad module.	Add PJP13	0.4
77	32	H/W	4/10	Mikecc_Huang	Result remove PCMCIA Card can't reduce default issue	Add R659	1.0
78	41	H/W	4/10	DELL	Improve LVDS for 3 dB (CDMA, GSM) at 1900 band	Pop C575~C599 Change C712,C713,C714 from 10P to 3.3P.	1.0
79	39	H/W	4/10	Steve_Wang	Change Board ID from X02 to A00	Pop R473,R474,R471;unpop R469,R470,R475	1.0
80	6	H/W	4/17	Steve_Wang	Result WWAN noise issue	Change R35,R36,R32,R34,R605 from 15ohm to 39ohm Change R37,R38,R39,R48 from 33ohm to 56ohm	1.0
81	29	H/W	4/21	DELL	Add cap for damp power-up surge current	Add C726 of 4700P Cap.	1.0
82	6	H/W	4/28	DELL	Result WWAN noise issue	Unpop R561	1.0
83	6	ME	4/28	CT_Huang	Avoid FPC easy to remove from connector	Add JP6,JP10 that co-lay with JP4,JLED1	1.0
84	9	Power	4/28	Kenneth_Chang	Result DC CPU noise	Remove C24,C32,C695,C696,C701,C702	1.0
85	44	H/W	5/9	Steve_Wang	Result HDD,Power,Battery Charger,Bluetooth,WLAN LED lightness irregularity issue	Change R615,R543 to 51ohm,R540 to 47ohm;R542,R547 to 330ohm,R551 to 56ohm	1.0
86	44	H/W	5/12	Steve_Wang	Result NUM,CAP,SCRL,Bluetooth,WLAN LED brightness irregularity issue	Change R545,R546,R547,R548 to 510ohm,R542 to 1Kohm	1.0

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1	51	PWR	10/14	Kenny	For support Adapter 45W	Add PR154 154K_0402_1% (SD03415438L) connect net (ADAPT_TRIP_SEL) to PU9_2 Add net name "ADAPT_TRIP_SEL"	0.2
2	51	PWR	10/14	Kenny	FBSA of the MAX8731 for dV/dt filtering per DELL's recommendation	Add PC135 0.01U_0603_25V (SD03415438L) connect FBSA to GND	0.2
3	51	PWR	10/27	Kenny	Moved battery voltage feedback to charge states	Connected pins 15 and 16 together changed connection to +VCHGR. Add PR155	0.2
4	51	PWR	10/27	Kenny	Added layout notes for PC135 and PC136		0.2
5	51	PWR	10/27	Kenny	Adjusted the current setting of the "UL" circuit and added hysteresis	change value of the PR142 from 499K to 4.32M, change value of the PR148 from 33.2K to 27.4K	0.2
6	50	PWR	10/27	Kenny	Adjusted the Load line setting	change value of the PR108 from 249K to 12K, change value of the PR114 from 48.7K to 2.37K Remove PC93	0.2
7	50	PWR	10/27	Kenny	Adjusted the transient setting	Change value of the PR106 from 511K to 392K, Change value of the PR114 from 82.5K to 160K Add PC94 as originally 1000pF	0.2
8	47	PWR	10/31	Kenny	When AC souce plug in, the suson turn on about 120ms immediately.	Change value of the PR27 from 10K to 0, Change value of the PR30 from 10K to 0. Add PR156 and PR157	0.2
9	47	PWR	11/02	Kenny	Remove PR156 and change PR157 location from PR30_1 to PR30_2.		0.2
10	51	PWR	11/02	Kenny	Vcore noise issue and ME's high limit	Remove PC74 and add PC Change value of the PC79 from 1210 type to 1206, Change value of the PC80 from 1210 type to 1206	0.2
11	51	PWR	11/07	Kenny	Follow MAX8731 reference schematic of A07 version	Add Table1 for ADP_OCP circuit. Modify value of PR147 from 59K to 56.2K	0.2
12	47	PWR	11/07	Kenny	Follow TPS51120 reference schematic of A06 version	Change value of the PR27 from 0 to 10K, Change value of the PR30 from 0 to 10K.	0.2
13	51	PWR	11/29	Kenny	Follow COE reference schematic of A09 version. PC135 may not be needed	Change PC135 to "NO STUFF"	0.3
14	51	PWR	11/29	Kenny	Follow COE reference schematic of A09 version. PC138 may be needed	Add PC138	0.3
15	51	PWR	12/12	Kenny	Deeply discharged battery problem	Add PR158 and PD19	0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	50	PWR	12/15	Kenny	Resolve a Choke for Dual Core CPU	Add PL17 and POP 4@ for Dual core	0.3
2	46	PWR	12/15	Kenny	Modify battery connector the same pine length for P+ and GND	Change P/N form DC040001R0L to DC04000380L	0.3
3	51	PWR	12/20	Kenny	Solve Inaccuracte CP point for 65W adapter-in current	Add PC139 and PC140 for "NO STUFF"	0.3
4	47	PWR	12/20	Kenny	TDC requirement	Add PR159	0.3
5	50	PWR	12/20	Kenny	We plan to add MOSFET for dual core CPU and have layout space limitation. So change PL13 size from 1810 to 1206.	Change PL13 size from 1810 to 1206.	0.3
6	48	PWR	12/21	Kenny	Delay the 1.5VRUN to meet Intel spec for the 3VRUN vs 1.5VRUN specification.	Add PD20 and PC141	0.3
7	47	PWR	12/21	Kenny	GG Issue item 19	Change to 0 ohms for PR159	0.3
8	50	PWR	12/21	Kenny	EMI test is ok, and have layout limitation issue for Dual core after adding low side MOS	Del PR151 and PC83	0.3
9	49	PWR	12/21	Kenny	Follow M07_DDRII_SC480_TPS51116_A04 circuit	Change PR78 to 27.4K, PR77 to 17.4K.	0.3
10	47	PWR	12/22	Kenny	TDC requirement	Change to 470K ohms for PR159	0.3
11	48	PWR	12/22	Kenny	Follow M07_1_05V1_5V_SC483_TPS51483_A07 circuit	"NO STUFF" for PC141	0.3
12	49	PWR	12/22	Kenny	Modify single and dual core note		0.3
13	50	PWR	12/23	Kenny	TDC requirement	Change PC90 from 680p to 390pF	0.3
14	50	PWR	12/26	Kenny	Modify the Footprint for PQ16		0.3
15	47	PWR	12/27	Kenny	Kemet CAP quantity issue	Change from SGA00000N8L to SGA00001A8L for 2 pcs. (PC25) Change from SGA00000N8L to SGA1933131L for 2 pcs. (PC23)	0.3

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1	48	PWR	2/11	Kenny	Footprint error for PD20	Modify footprint from S0D323 to S0T323	0.4
2	51	PWR	2/11	Kenny	Location error for MOSFET	STUFF for PQ27, NO-STUFF for PQ16	0.4
3	50	PWR	2/20	Kenny	The OCP setting is 20 A for Dual Core CPU	Adding NO-stuff for 215K on PR104	0.4
4	50	PWR	2/21	Kenny	The load line is "-2.1m" for Dual Core CPU.	Adding NO-stuff for 5.76K on PR114	0.4
5	48	PWR	2/22	Kenny	CYNTEC is not on DELL's AVL	Change the vender from DELTA to CYNTEC on PL9 and PL10	0.4
6	49	PWR	2/22	Kenny	CYNTEC is not on DELL's AVL	Change the vender from DELTA to CYNTEC on PL12	0.4
7	47	PWR	2/22	Kenny	Follow COE schetmatic for A06 version	Modify net name from +3.3V_ALW to +3.3V_RTC_LDO for PU7_PIN5	0.4
8	51	PWR	2/23	Kenny	Follow COE schetmatic for A11 version	Modify PQ18 and PQ19 from SI4825 to SI4835	0.4
9	47	PWR	2/24	Kenny	No 2nd source for PC25	Change from SGA00001A8L to SGA1933131L for 2 pcs. (PC25)	0.4
10	47	PWR	3/6	Kenny	+3.3V_RTC_LDO voltage drop issue	Add PU10, PC143, PC142, PR160, PR162 and PR161	0.4
11	45	PWR	3/8	Kenny	+3.3V_RTC_LDO voltage drop issue	Move PU10, PC143 and PC142 from page47 to page45	0.4
12	50	PWR	3/17	Mike	Error description for Dual Core load line	Dual Core Load Line change to 2.1mohm	0.4
13	47	PWR	4/25	Kenny	+3.3V_RTC_LDO voltage drop issue	change PR40 from 470K to 4.7K, - change PR159 from 470K to 2.2M, - change PC32 from 0.1U to 0.01uF, - add UN-STYFF Schottky diode PD21 in parallel to PR159	0.5
14	48	PWR	4/25	Kenny	Delta ckoke has dimension issue	Change the vender from CYNTEC to DELTA on PL9 and PL10	0.5
15	49	PWR	4/25	Kenny	Delta ckoke has dimension issue	Change the vender from CYNTEC to DELTA on PL9 and PL10	0.5

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1	50	PWR	4/25	Kenny	CPU noise issue	For Dual CPU: Modify PR101 from 10K to 20K PC88 from 820P to 470P PC90 from 390P to 470P	0.5
2	50	PWR	4/28	Kenny	CPU noise issue	No STUFF PC80 for DUAL CORE CPU	

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