

Compal confidential

Schematics Document

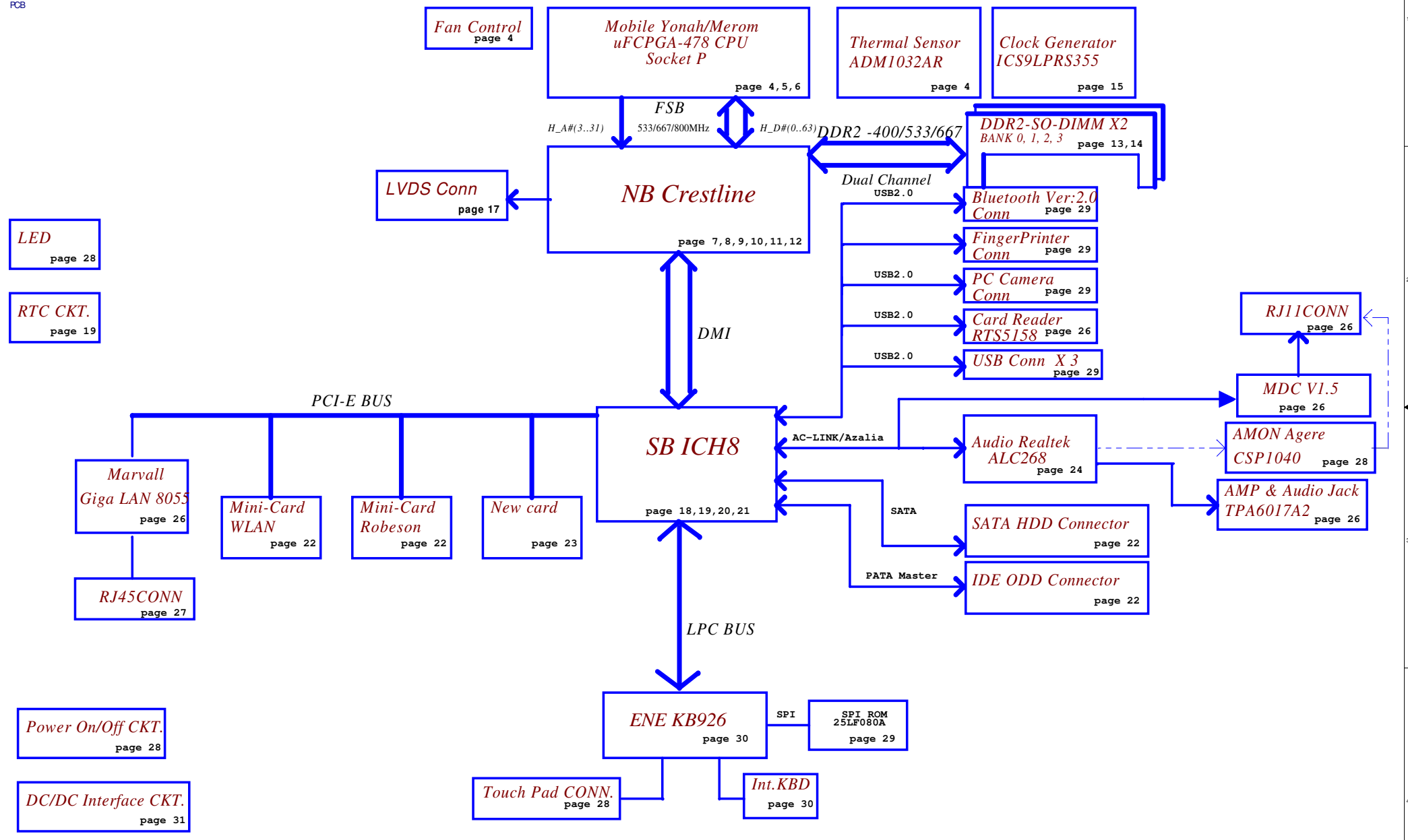
Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-24
REV: 0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/02/13	Deciphered Date	2006/07/26	Title		
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Supra 1.0 (Merom +Crestline+ICH8) 12"

ZZZ1
PCB



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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

I2C / SMBUS ADDRESSING

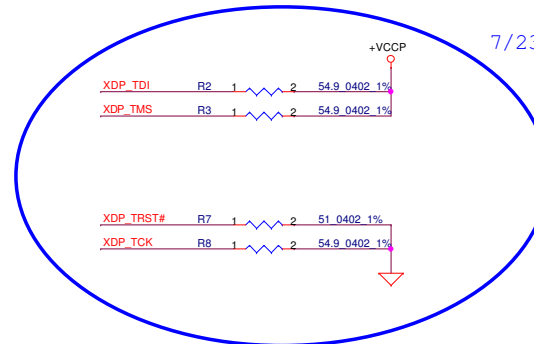
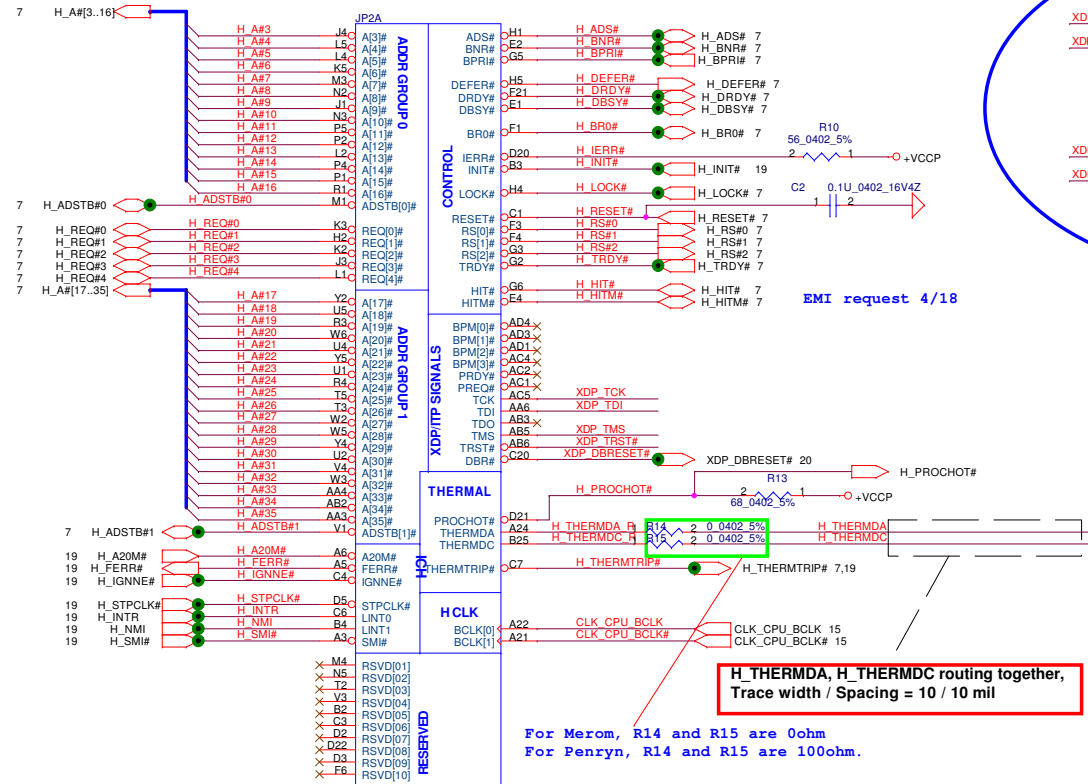
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

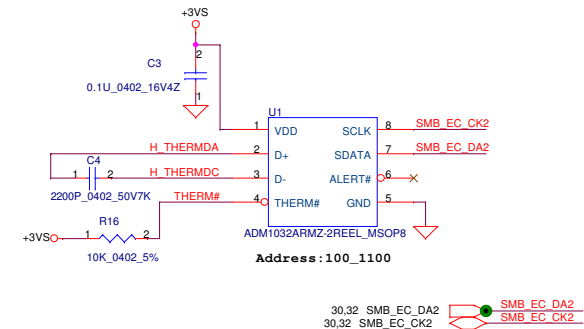
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43XXXXXX

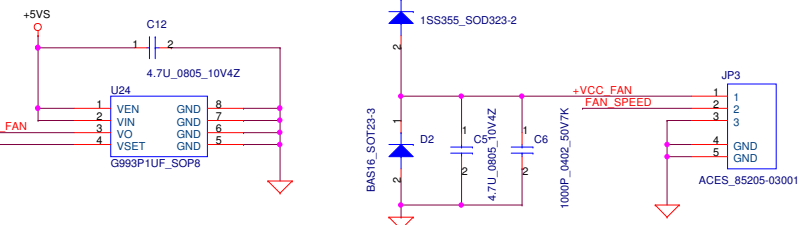
Jump-Short: PJP?



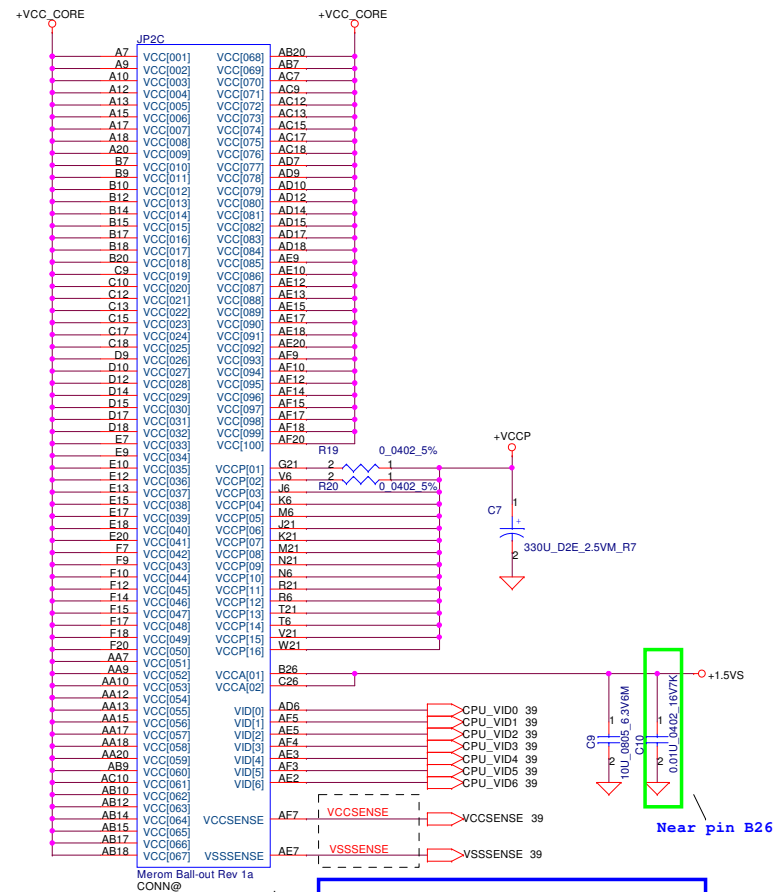
Thermal Sensor ADM1032ARMZ



Voltage Fan Control circuit



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2006/02/13				2006/03/10				Merom(1/3)-AGTL+/XDP			
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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

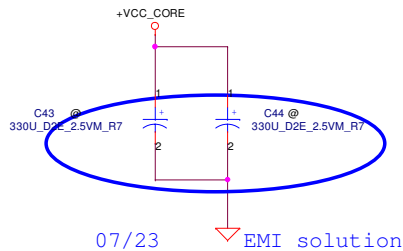
Circuit diagram showing the connection of the CPU pin AD26 to the V_CPU_GTLREF signal. The signal is connected to a resistor network consisting of R28 (1K_0402_1%) and R30 (2K_0402_1%) in series, connected to +VCCP and ground.

Length match within 25 mils.
The trace width/space/other is
20/7/25.

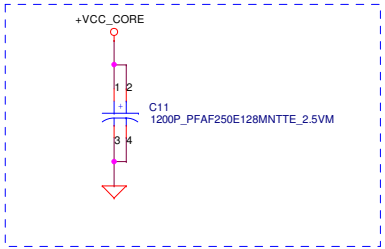
Close to CPU pin within 500mils.

A4	JP2D	P6
A8	VSS[001]	P21
A11	VSS[002]	P24
A14	VSS[003]	R2
A16	VSS[004]	R5
A19	VSS[005]	R22
A23	VSS[006]	R25
AF2	VSS[007]	T1
B6	VSS[008]	T4
B8	VSS[009]	T23
B11	VSS[010]	T26
B13	VSS[011]	U3
B16	VSS[012]	U6
B19	VSS[013]	U21
B21	VSS[014]	U24
B24	VSS[015]	V2
C5	VSS[016]	V5
C8	VSS[017]	V22
C11	VSS[018]	V25
C14	VSS[019]	W1
C16	VSS[020]	W4
C19	VSS[021]	W23
C2	VSS[022]	W26
C22	VSS[023]	Y3
C25	VSS[024]	Y6
D1	VSS[025]	Y21
D4	VSS[026]	Y24
D8	VSS[027]	AA2
D13	VSS[028]	AA5
D16	VSS[029]	AA8
D19	VSS[030]	AA11
D23	VSS[031]	AA14
D26	VSS[032]	AA16
E3	VSS[033]	AA19
E6	VSS[034]	AA22
E8	VSS[035]	AA25
E11	VSS[036]	AB1
E14	VSS[037]	AB4
E16	VSS[038]	AB8
E19	VSS[039]	AB11
F21	VSS[040]	AB13
F24	VSS[041]	AB16
F5	VSS[042]	AB19
F8	VSS[043]	AB23
F11	VSS[044]	AB26
F13	VSS[045]	AC3
F16	VSS[046]	AC6
F19	VSS[047]	AC8
F2	VSS[048]	AC11
F22	VSS[049]	AC14
F25	VSS[050]	AC16
G4	VSS[051]	AC19
G1	VSS[052]	AC21
G26	VSS[053]	AC24
H3	VSS[054]	AD2
H6	VSS[055]	AD5
H21	VSS[056]	AD8
H24	VSS[057]	AD11
J2	VSS[058]	AD13
J5	VSS[059]	AD16
J22	VSS[060]	AD19
J25	VSS[061]	AD22
K1	VSS[062]	AD25
K4	VSS[063]	AE1
K23	VSS[064]	AE4
K26	VSS[065]	AE8
L3	VSS[066]	AE11
L6	VSS[067]	AE14
L21	VSS[068]	AE16
L24	VSS[069]	AE19
M2	VSS[070]	AE23
M5	VSS[071]	AE26
M22	VSS[072]	A2
M25	VSS[073]	AF6
N1	VSS[074]	AF8
N4	VSS[075]	AF11
N23	VSS[076]	AF13
N26	VSS[077]	AF16
P3	VSS[078]	AF19
	VSS[079]	AF21
	VSS[080]	A25
	VSS[081]	AF25
	VSS[082]	

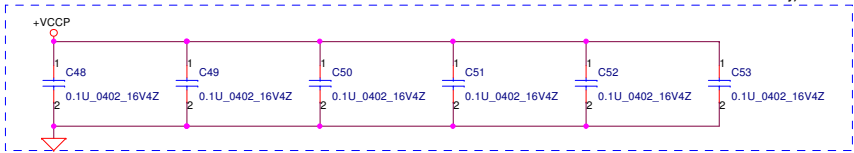
Near CPU CORE regulator



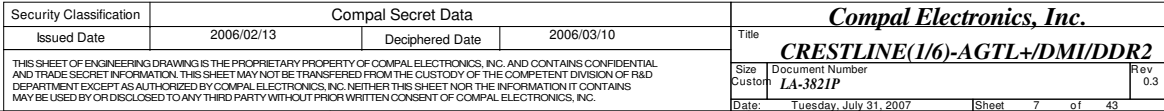
Proadlizer

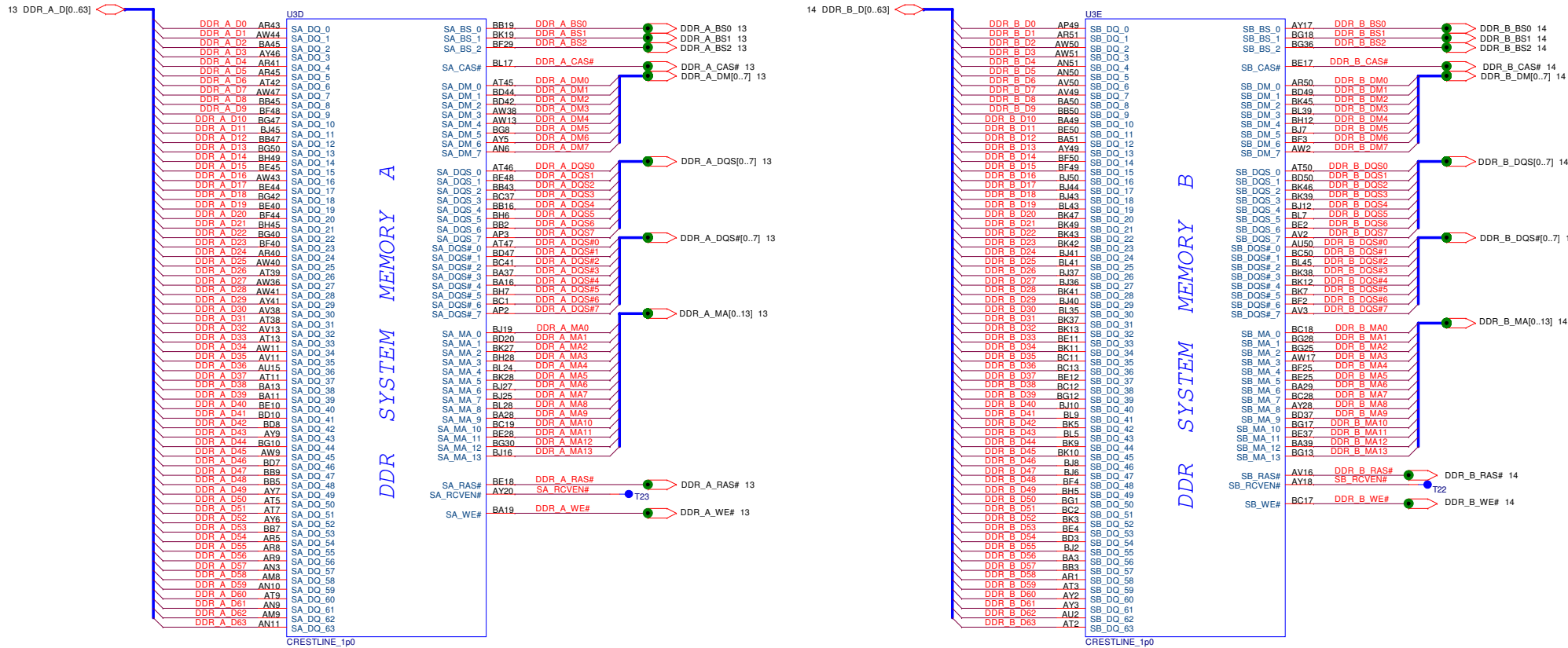


Place these inside
socket cavity on L8
(North side
Secondary)

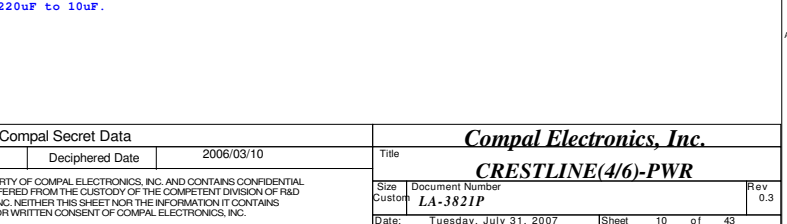
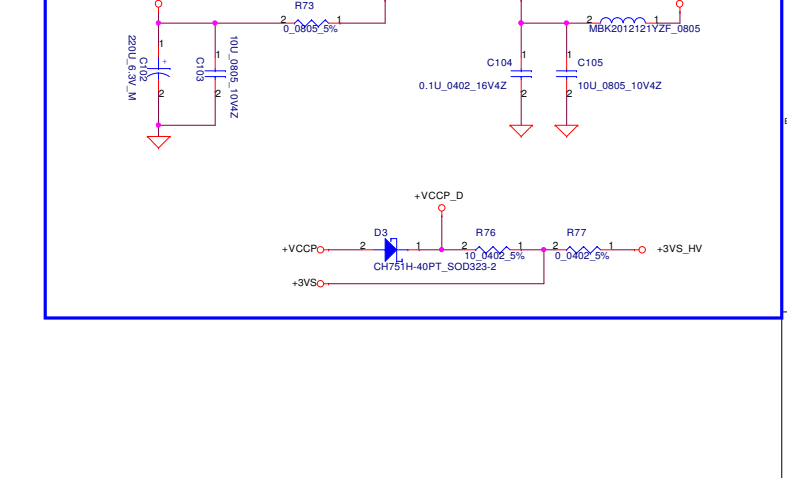
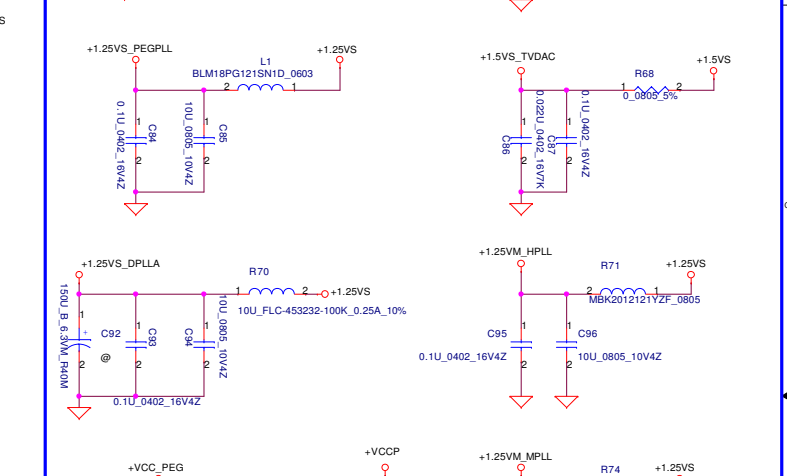
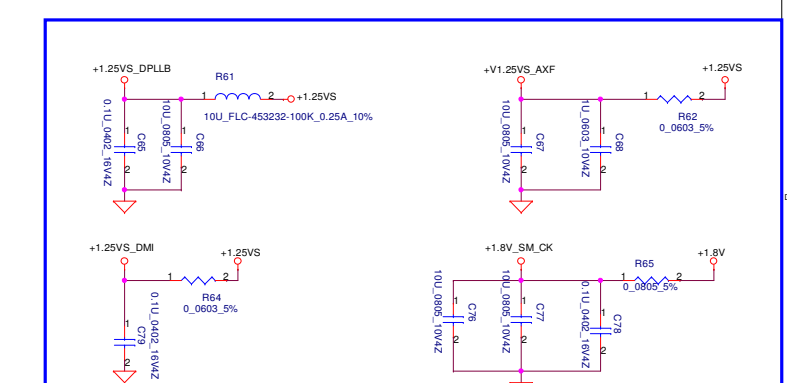
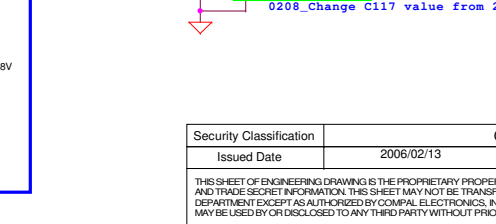
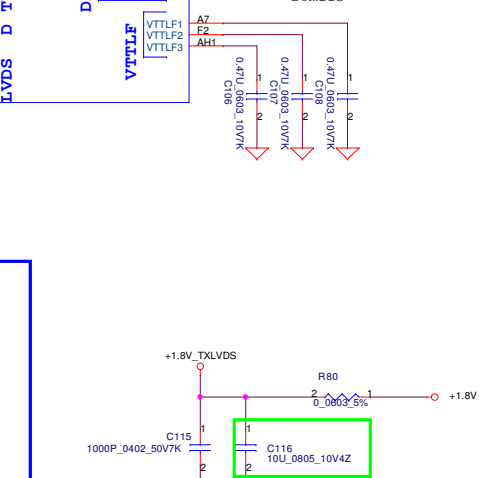
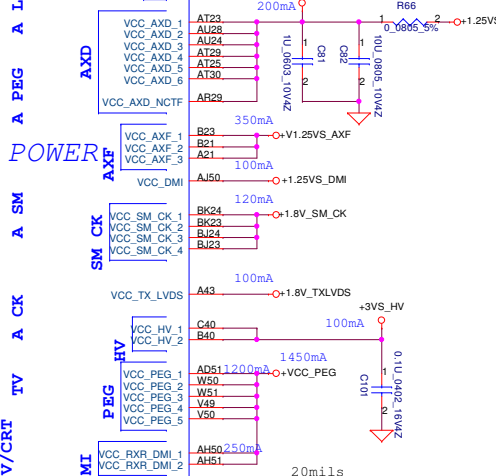
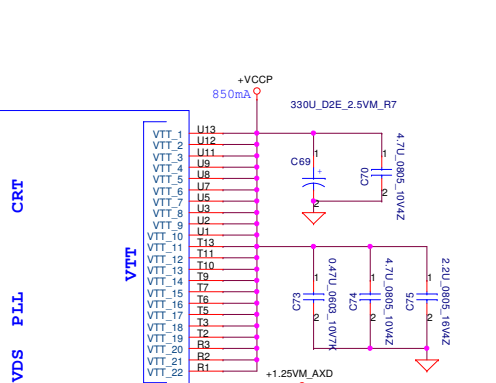
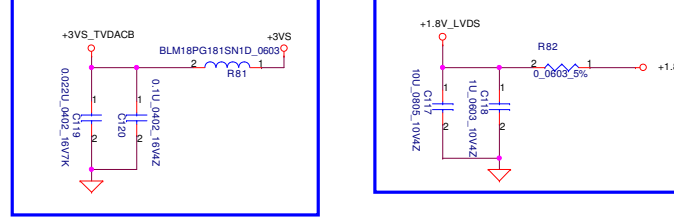
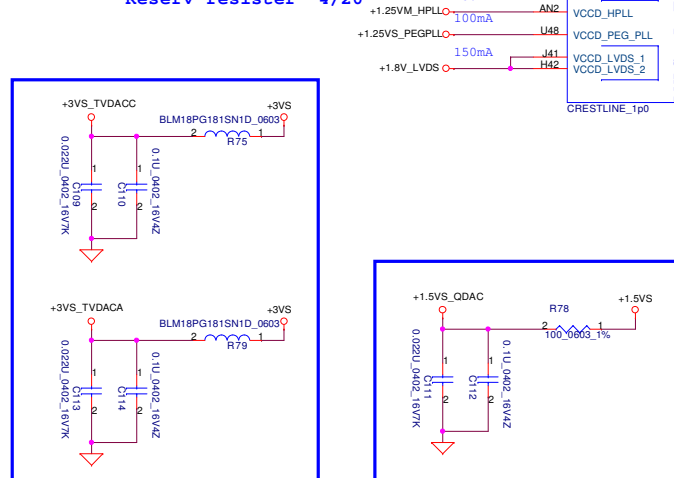
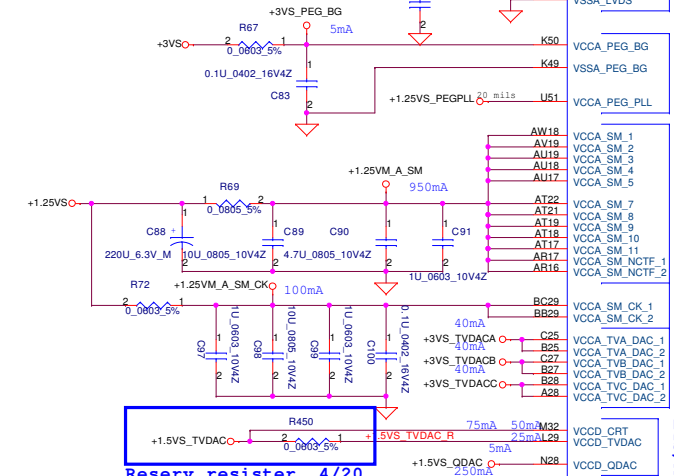
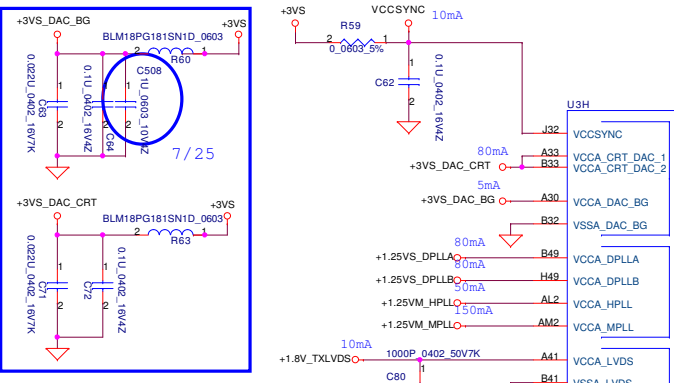


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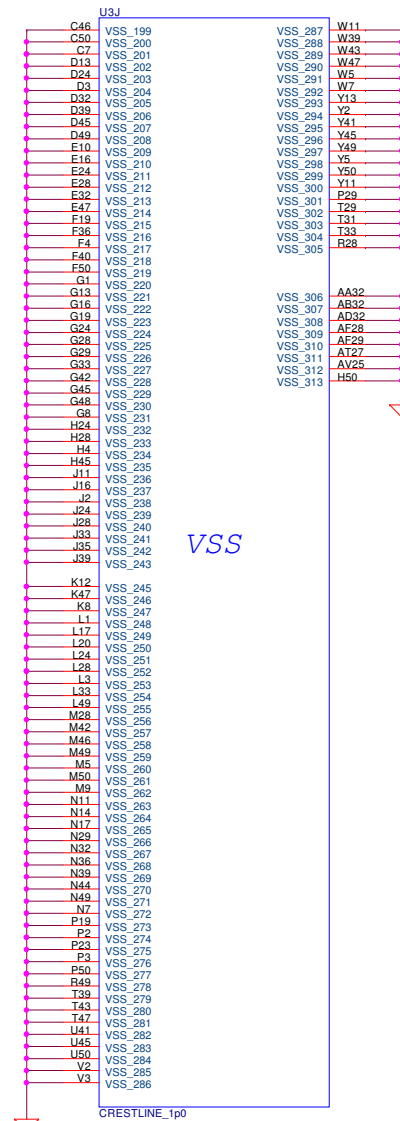
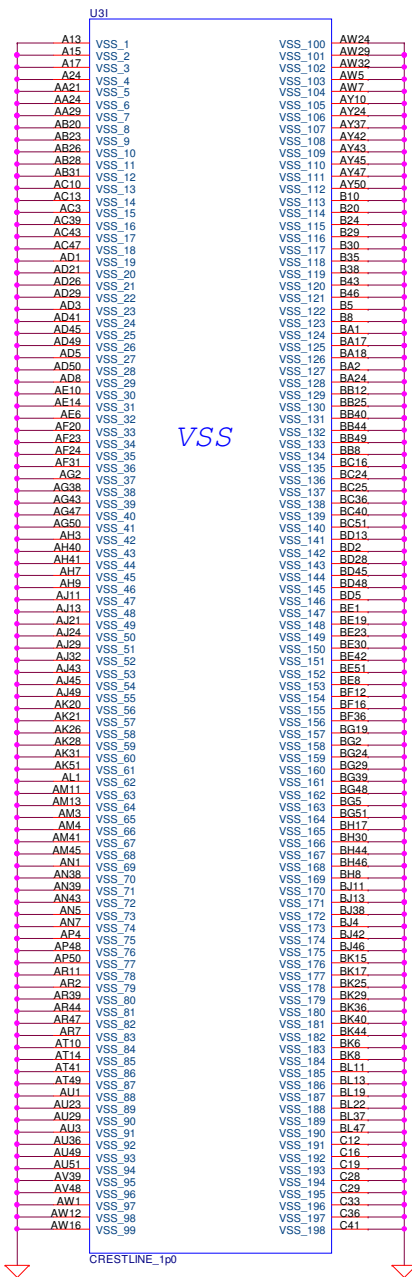




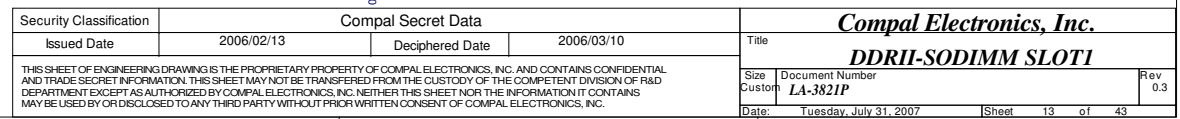
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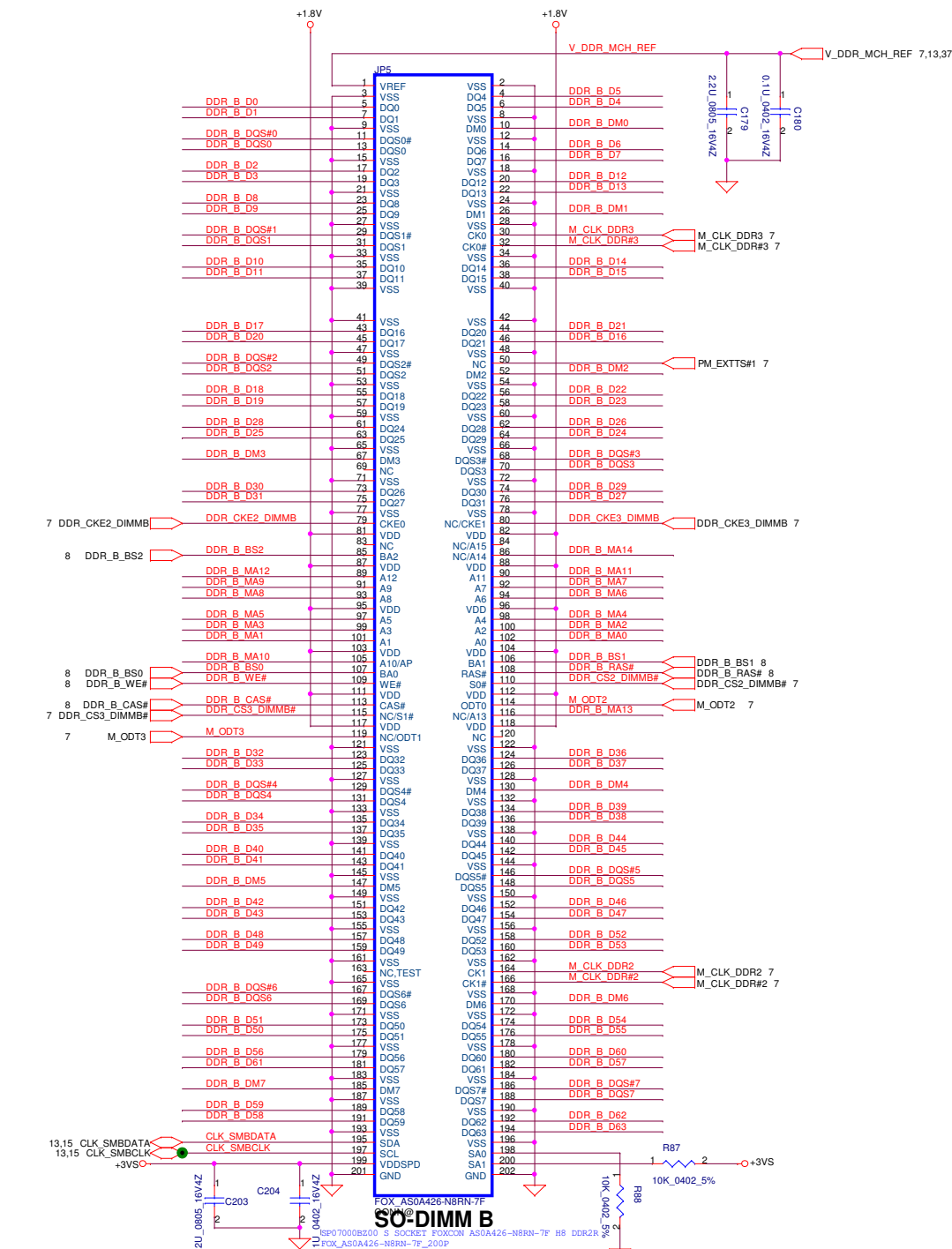
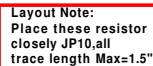
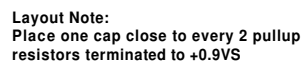
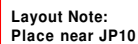


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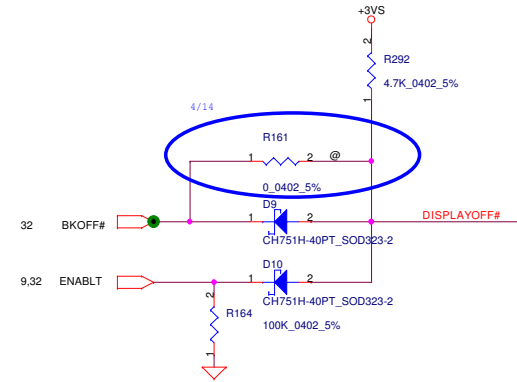
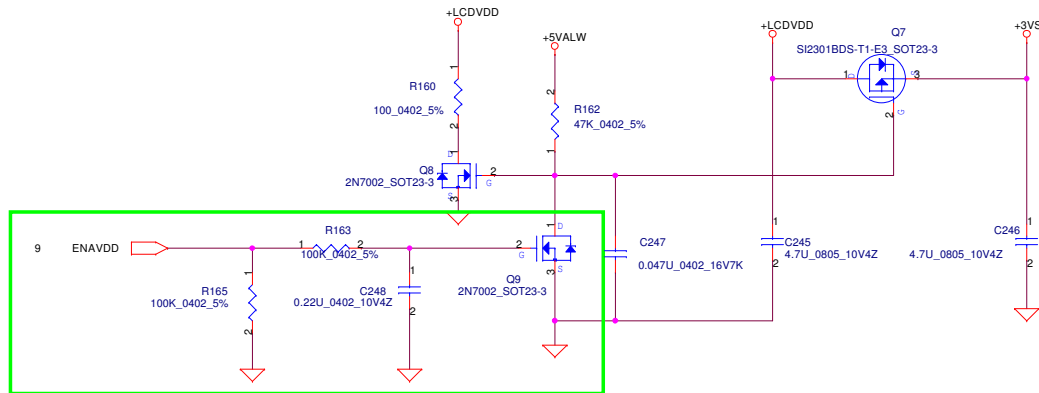
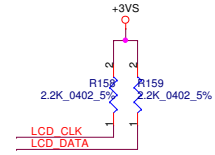
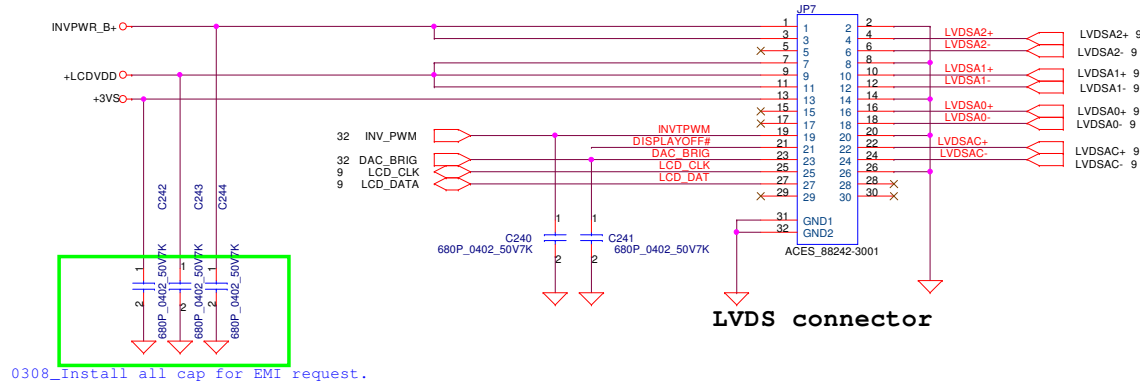
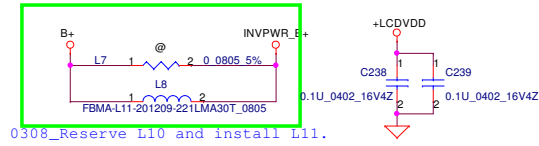
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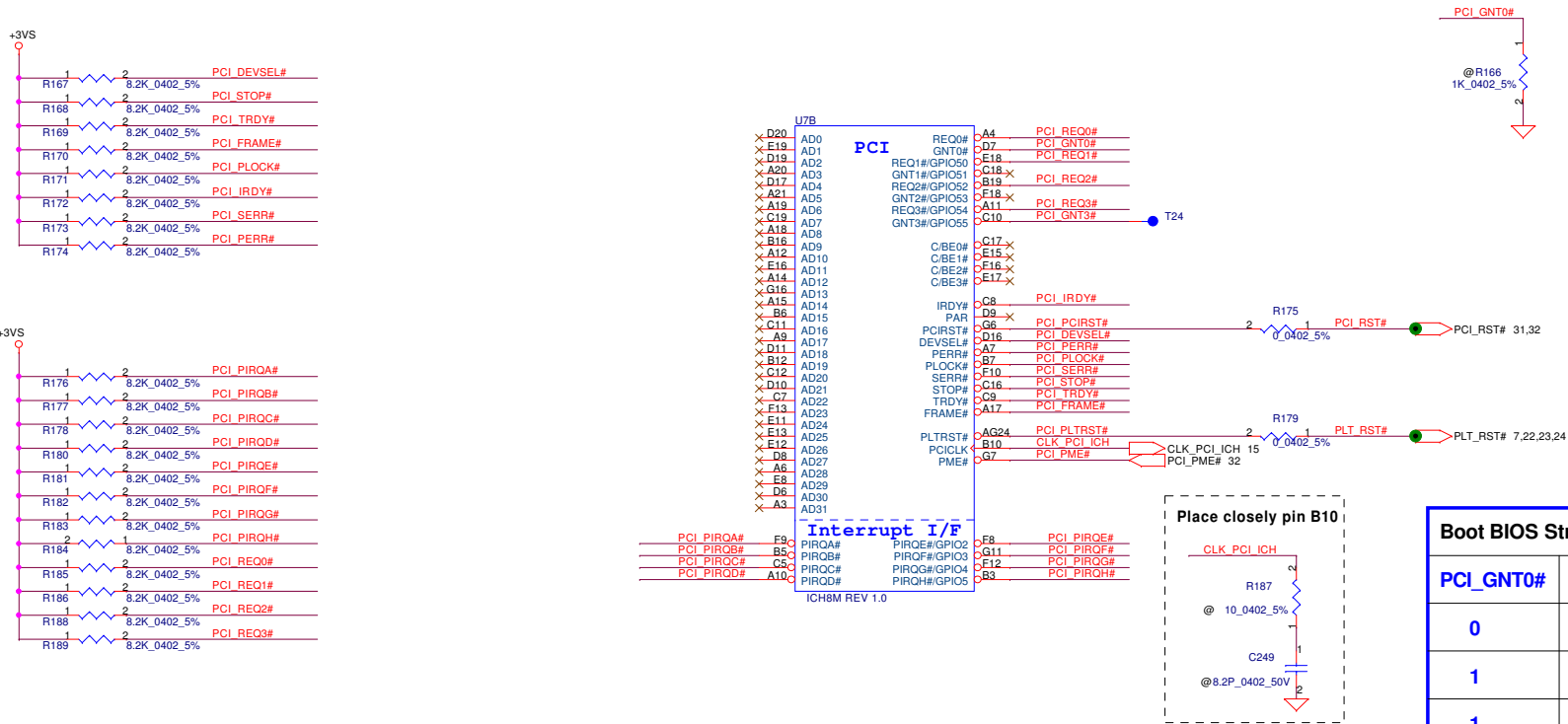


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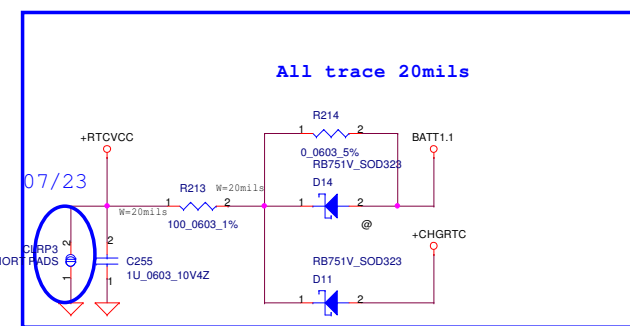
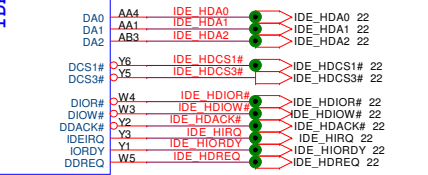
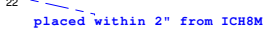
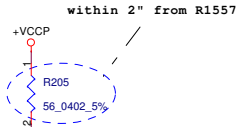
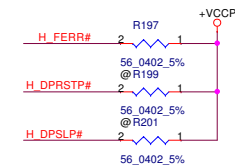
LVDS CONN



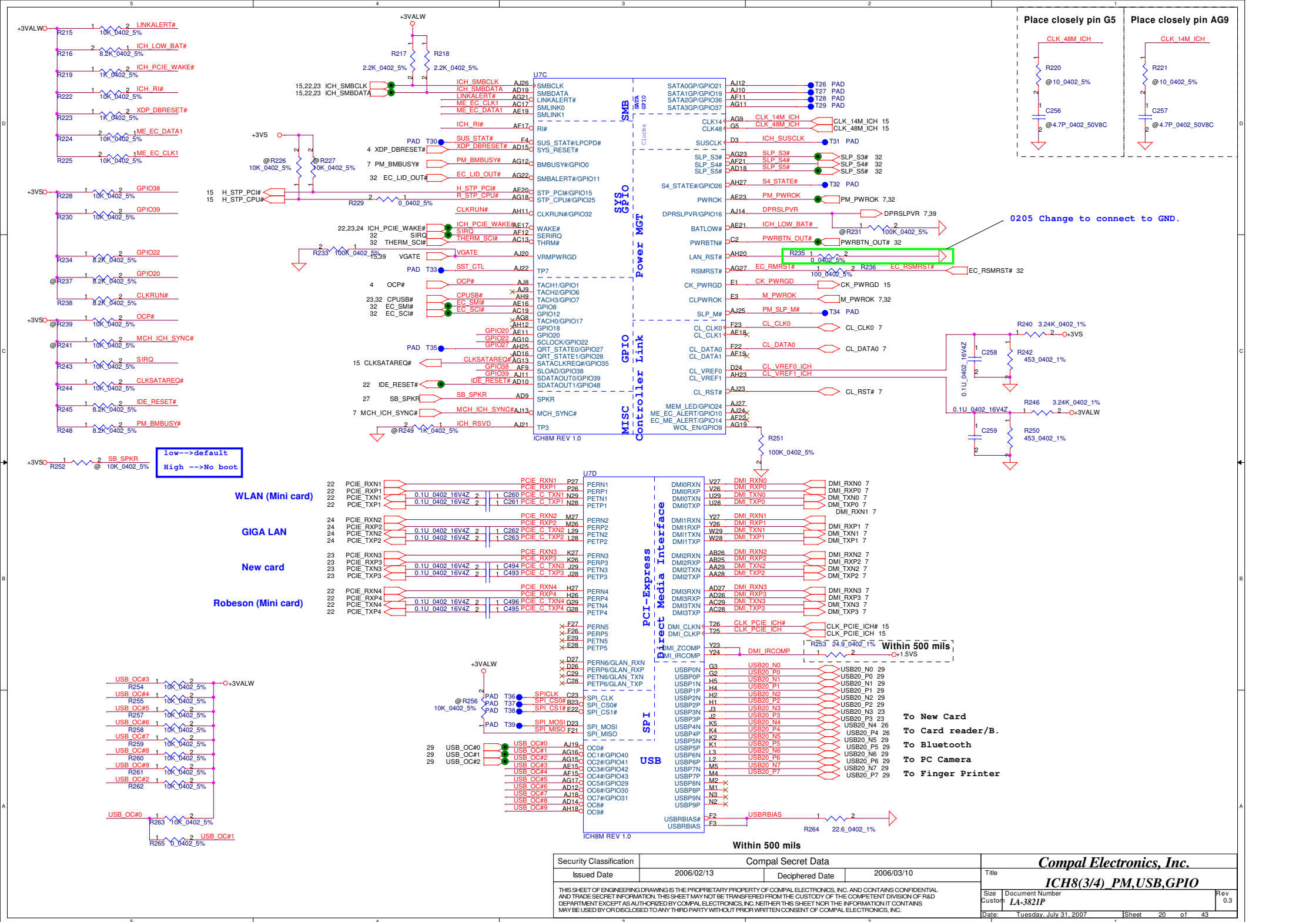
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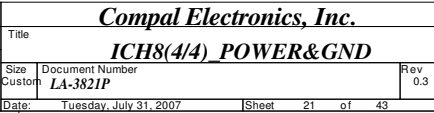


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *
A16 swap override Strap		
PCI_GNT3#	*Low= A16 swap override Enble High= Default	

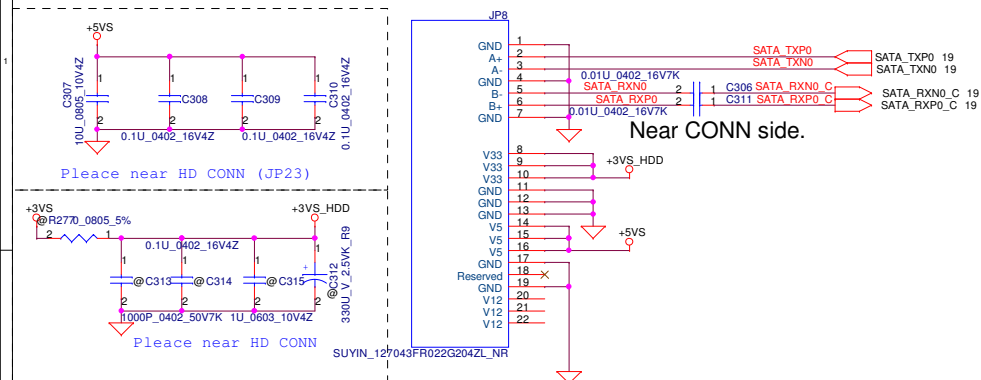


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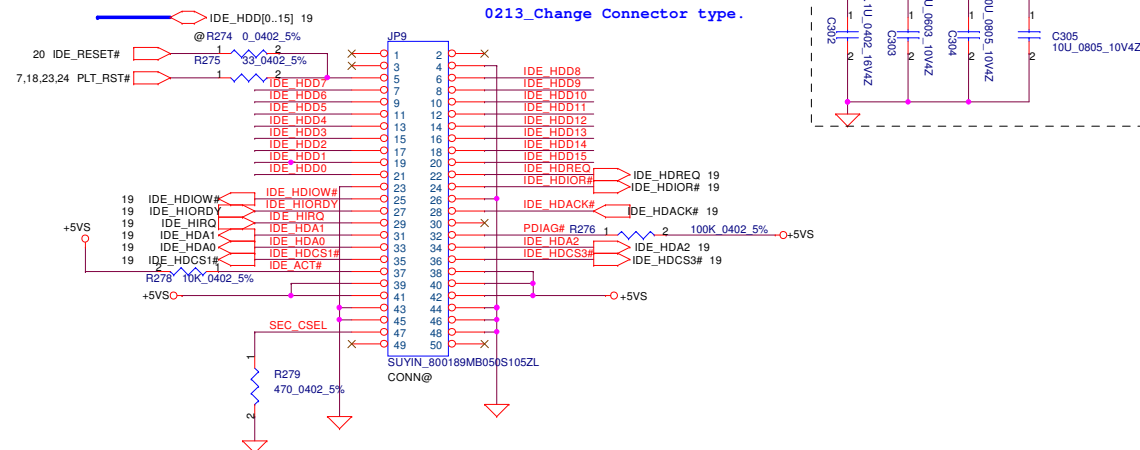




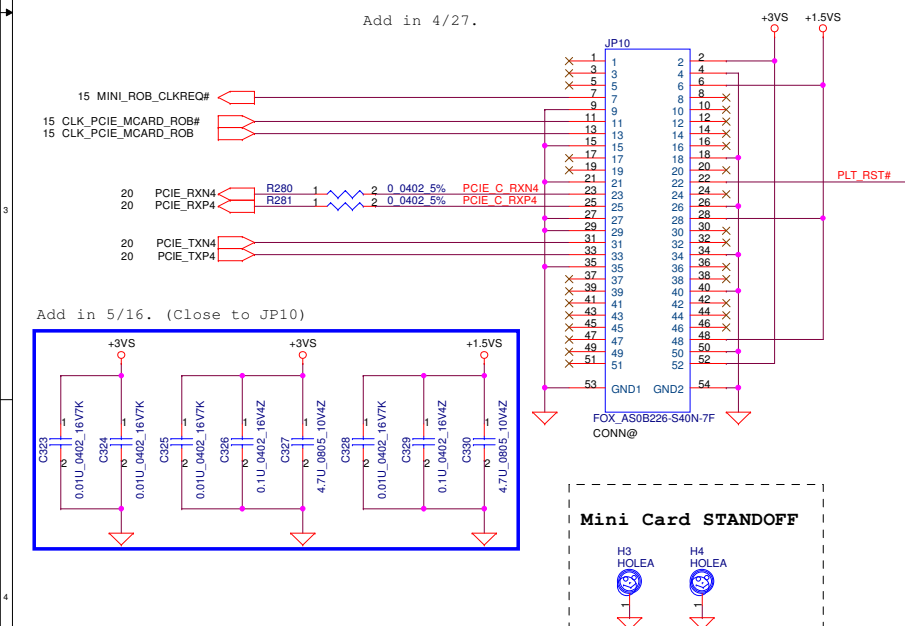
HDD Connector



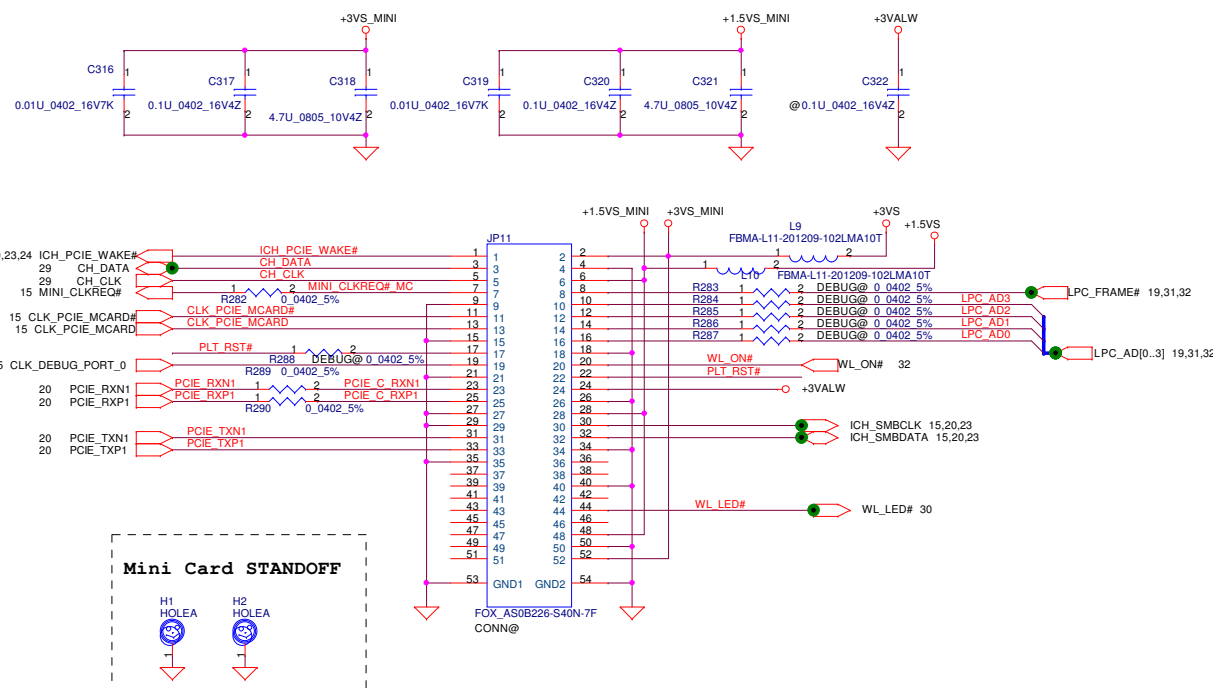
CD-ROM Connector



NAND mini Card(Robson support)

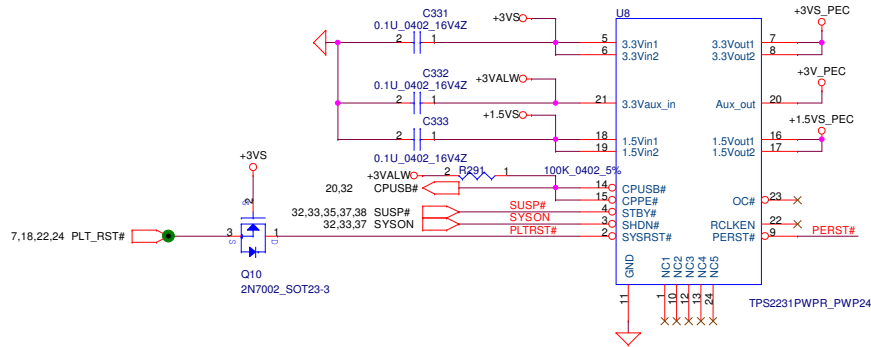


Mini-Express Card---WLAN

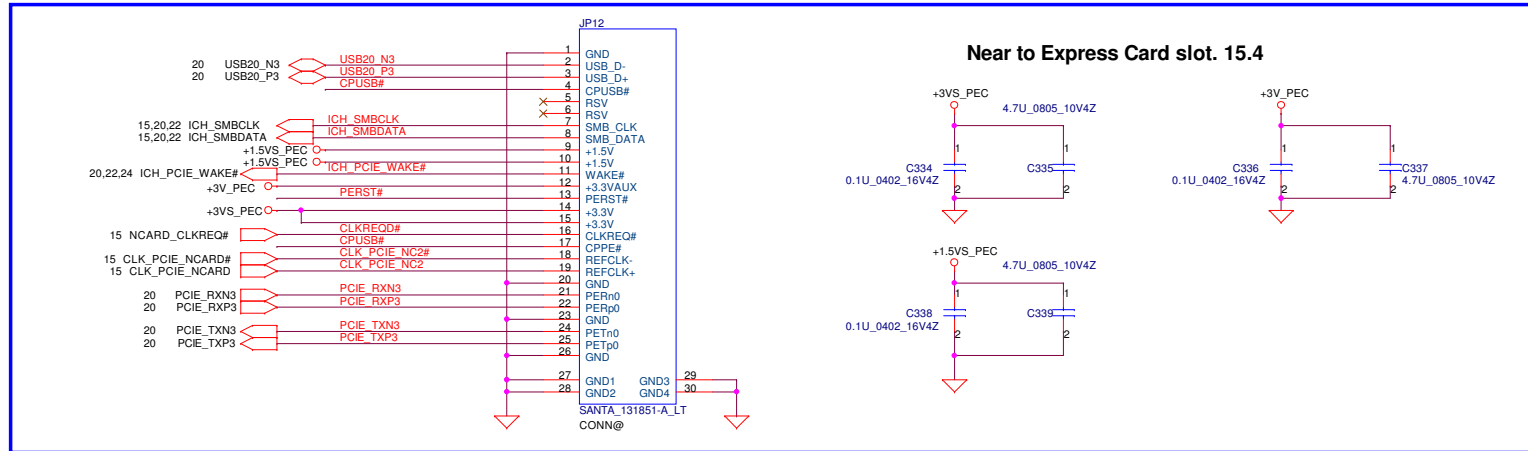


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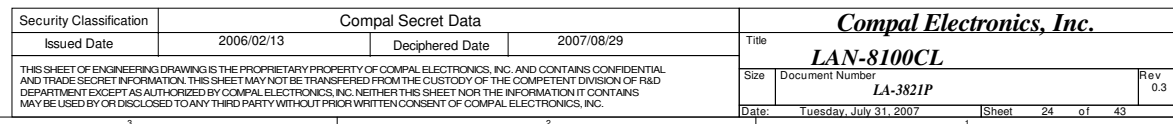
Express Card Power Switch

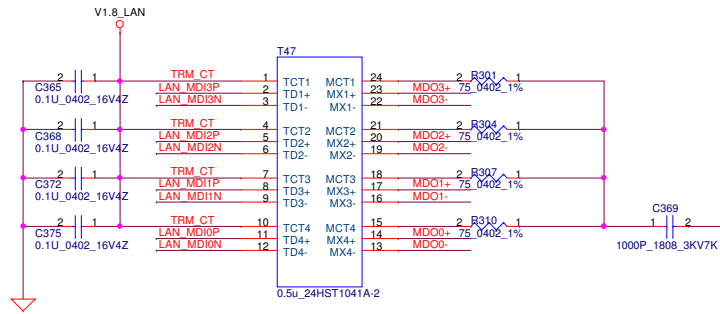
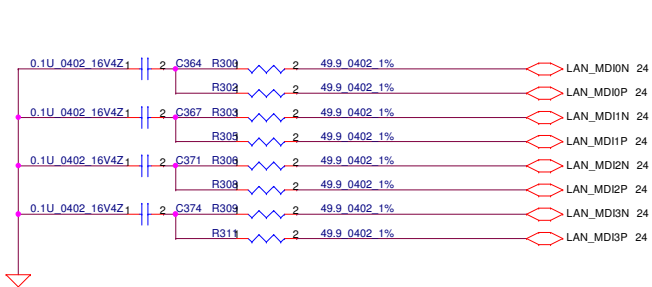


Near to Express Card slot. 15.4

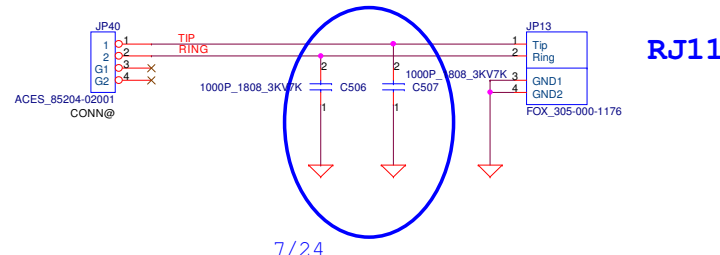
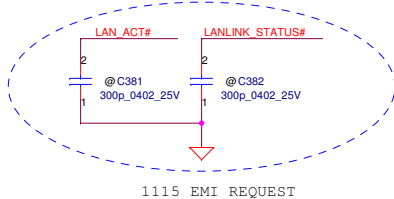
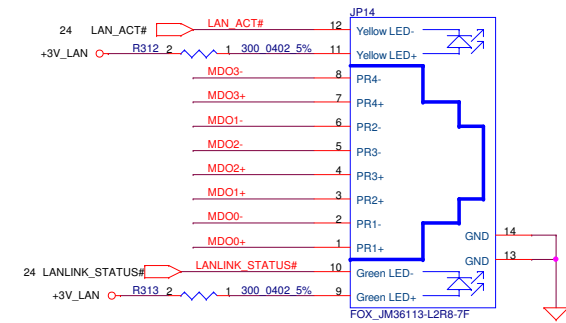


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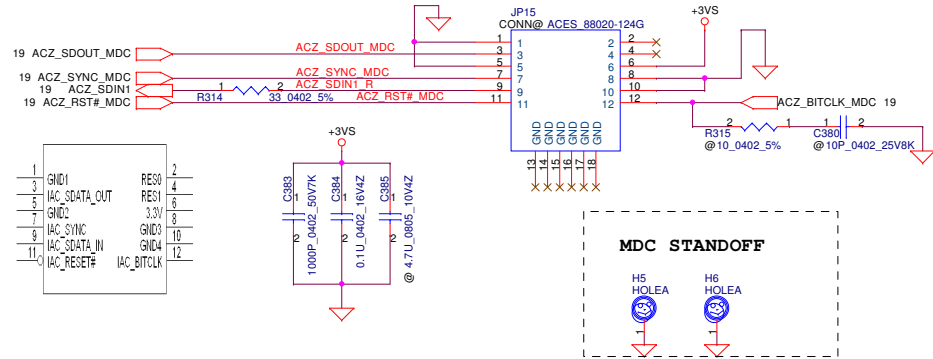


Note: MDO[3..0]+/- signals should route to JP13 first then to JP30.



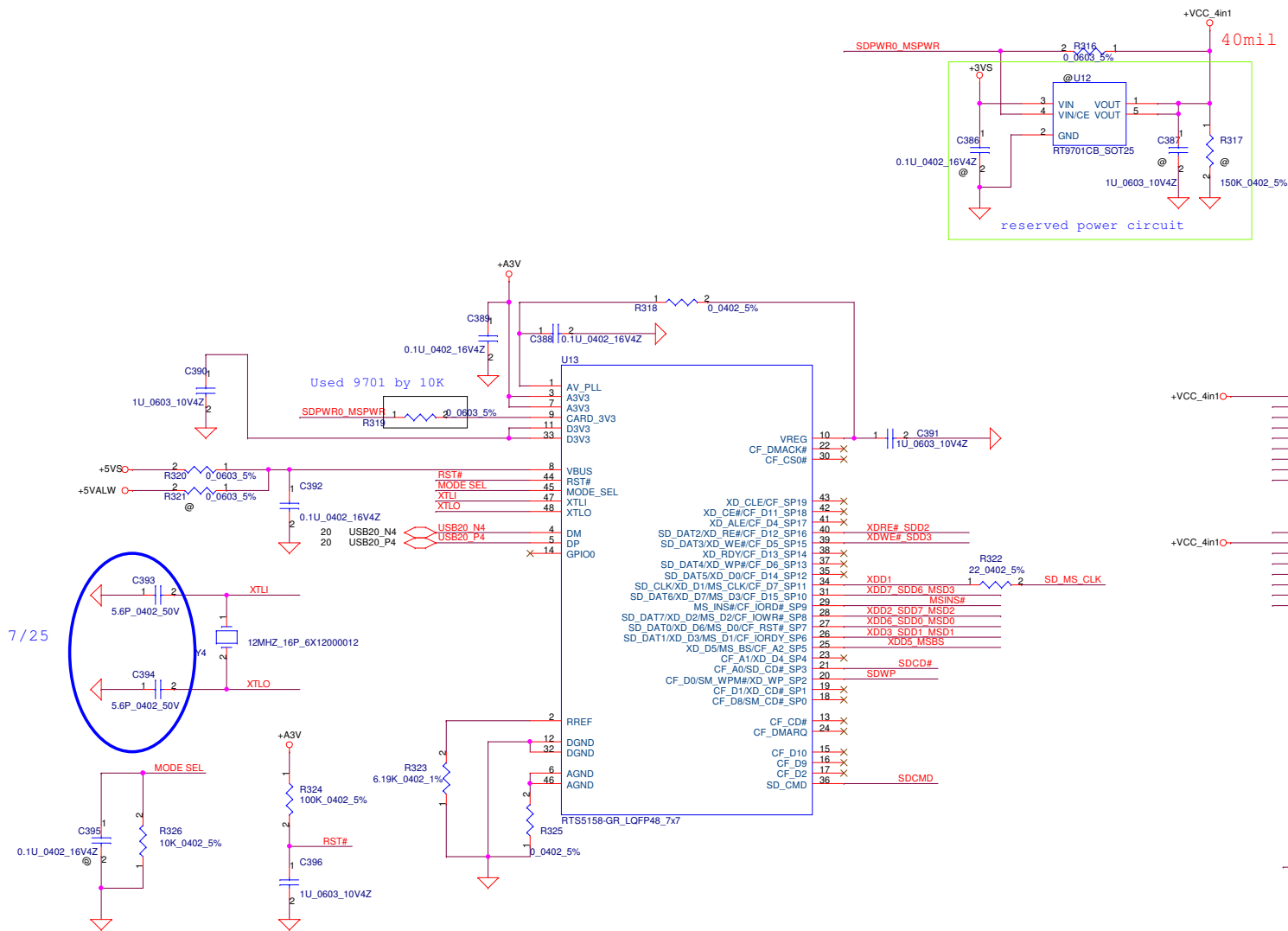
MDC 1.5 Conn.

Change type 4/25

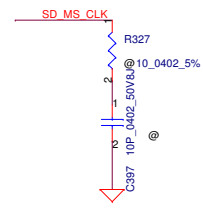
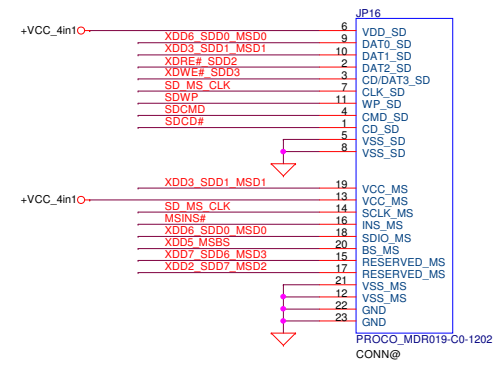


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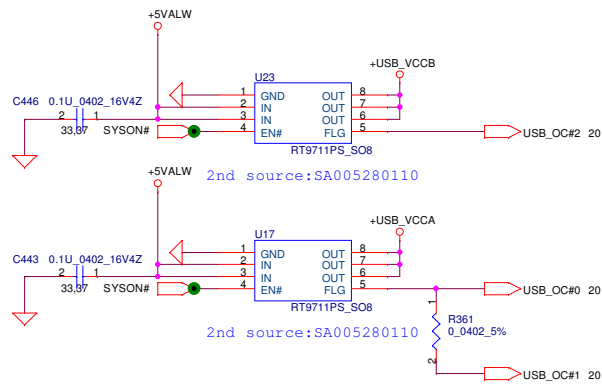


3 in 1 Card Reader

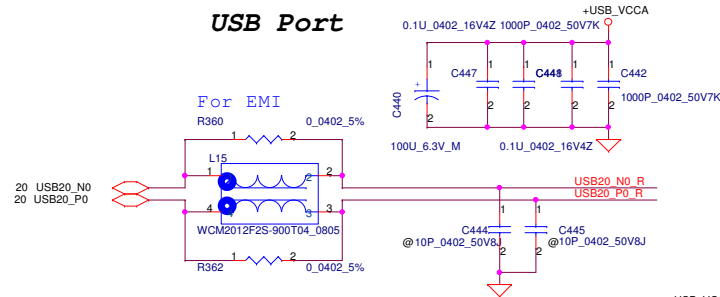


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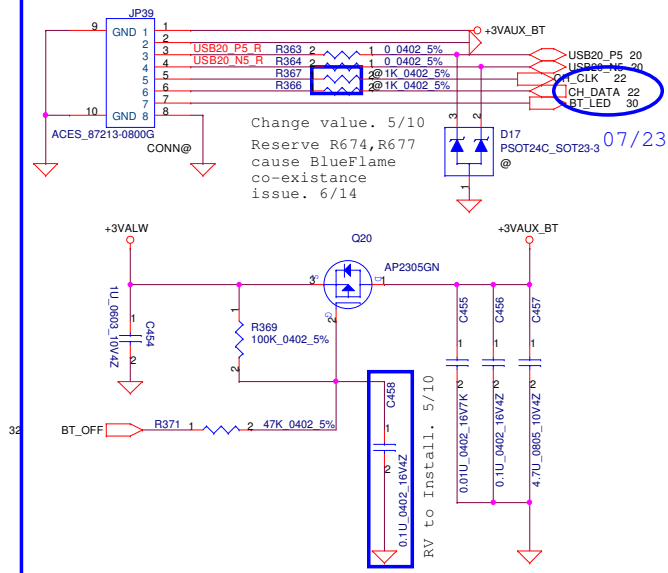
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Title			
Card reader board			
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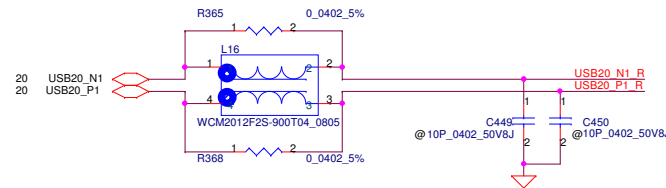
USB Port



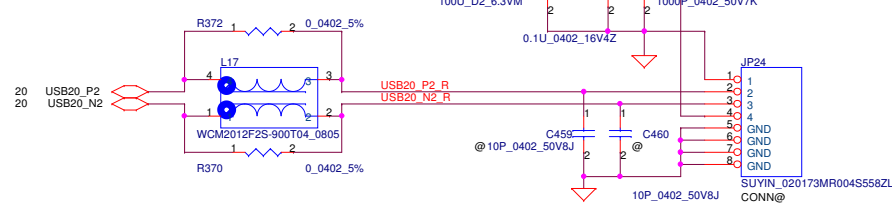
BT Connector



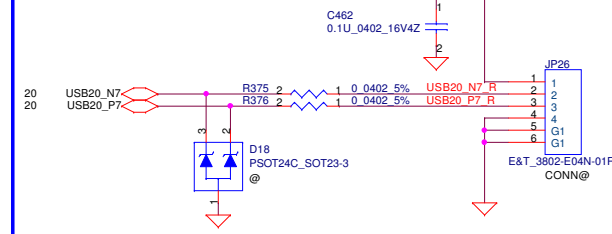
For EMI



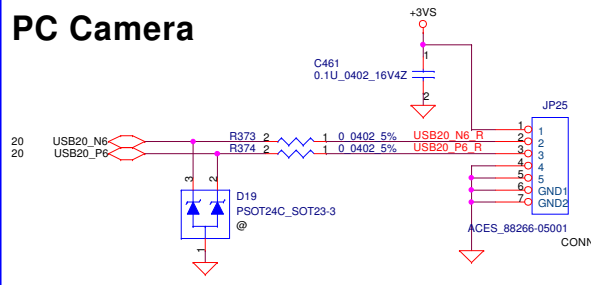
For EMI



Finger printer

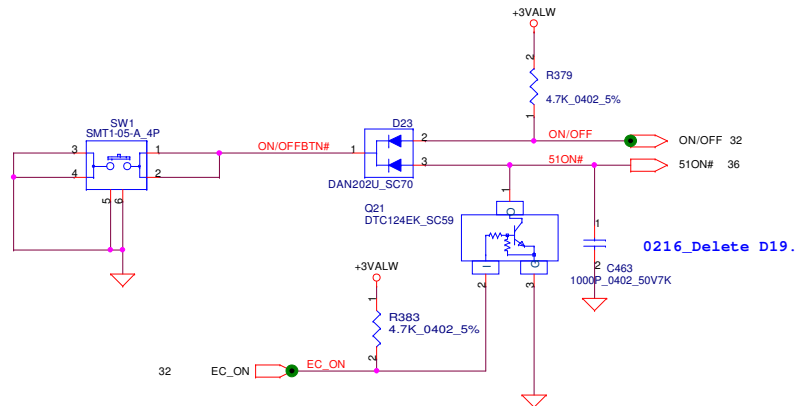


PC Camera

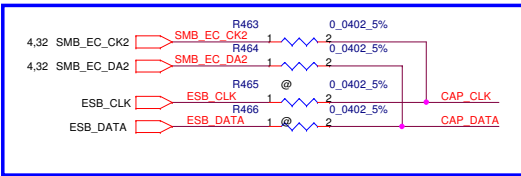


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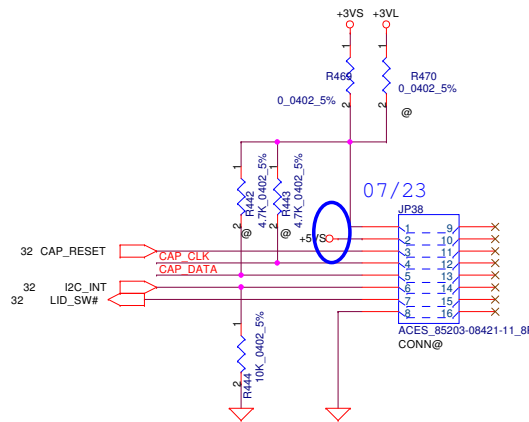
Power ON/OFF



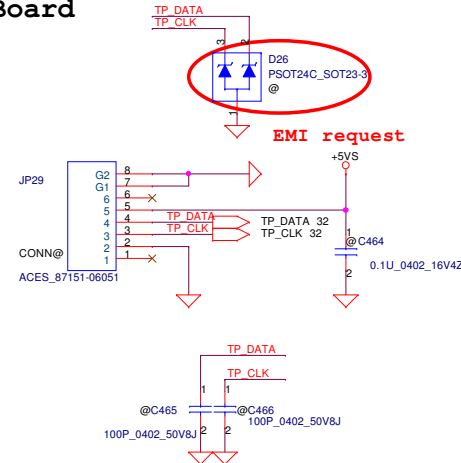
0216_Delete D19.



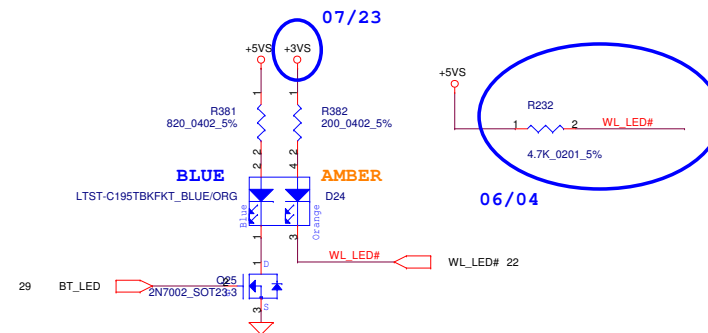
06/15 Change pin define for try ENE cap bottom



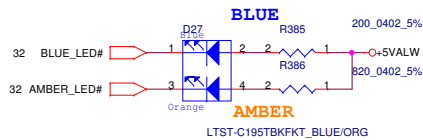
T/P Board



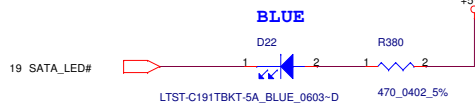
Wireless ON Amber Bluetooth ON Blue



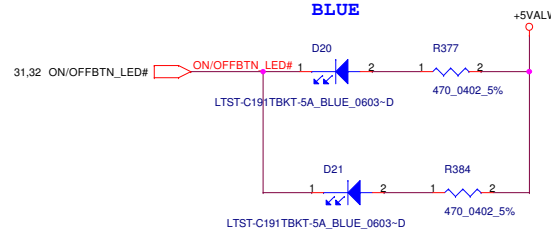
Battery Charge LED(Left 2)



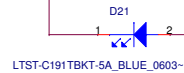
HDD LED(Left 3)



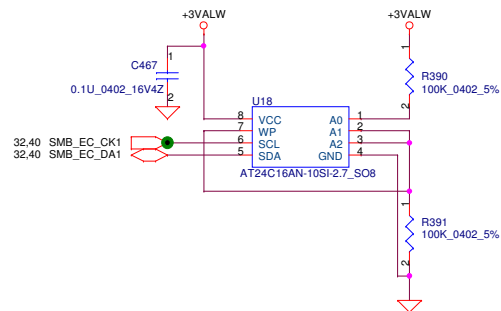
POWER LED1



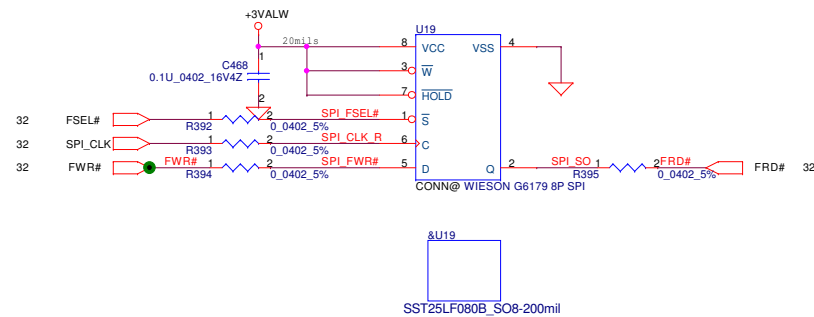
POWER LED2



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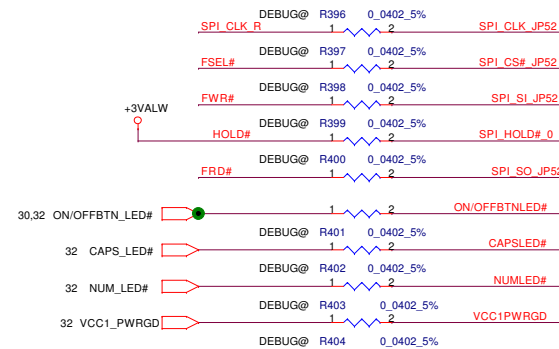
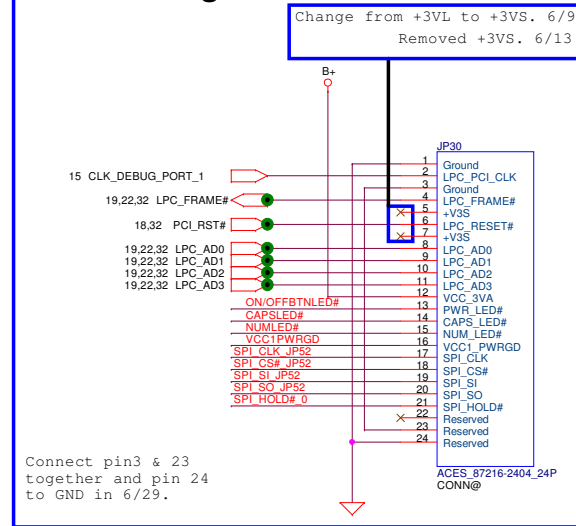


SPI ROM

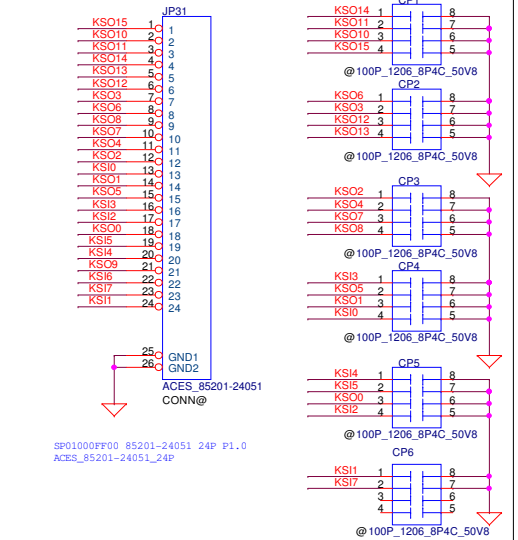
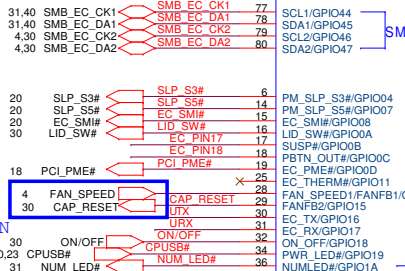
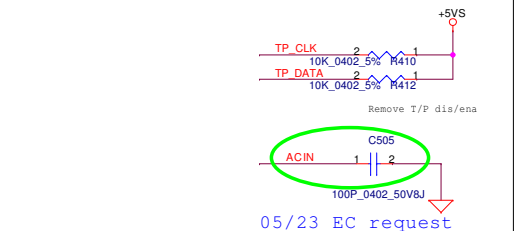
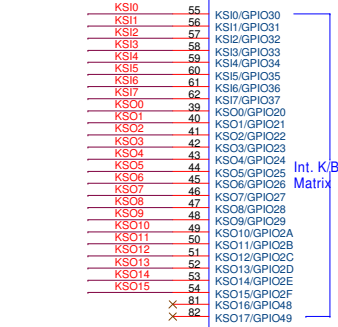
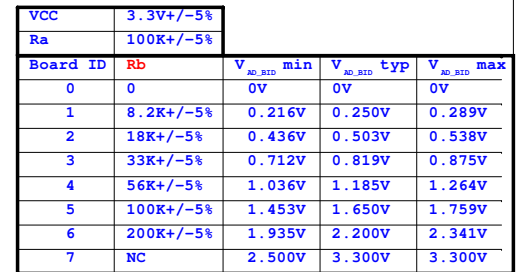
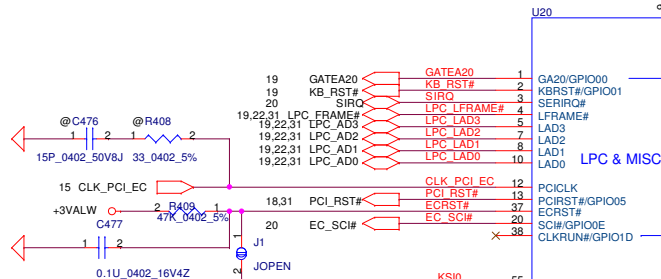
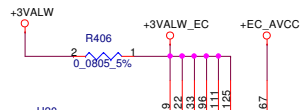


B-Test remove SPI ROM socket

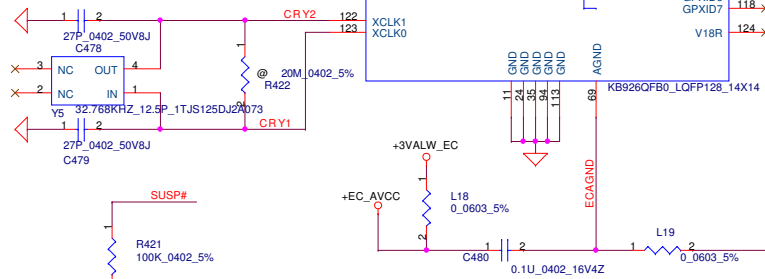
LPC Debug Port



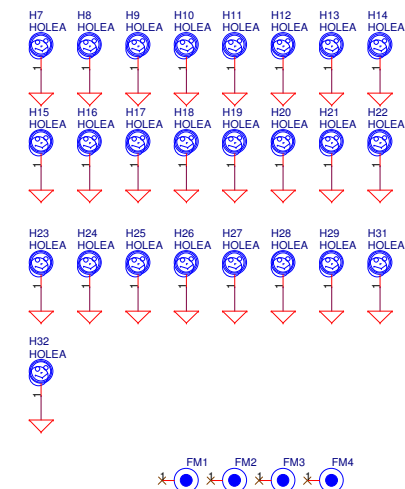
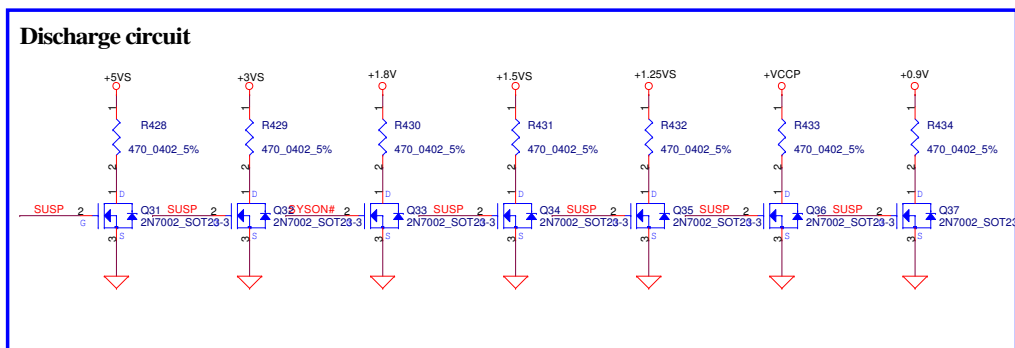
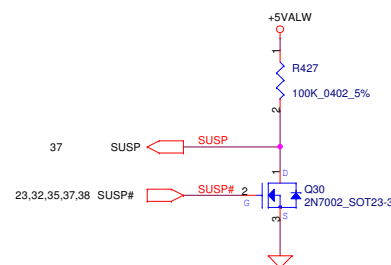
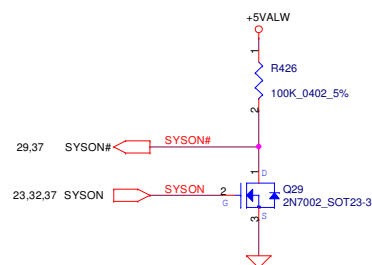
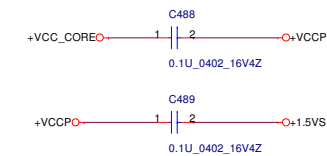
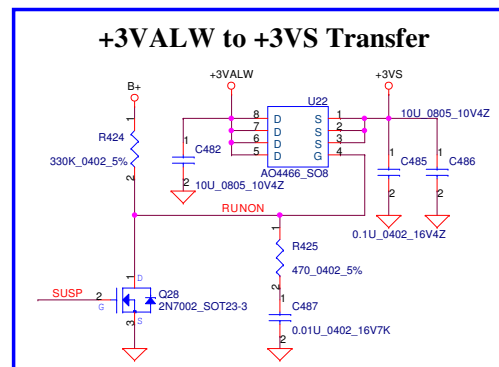
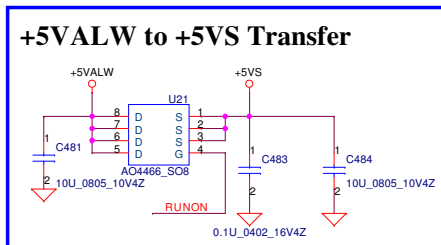
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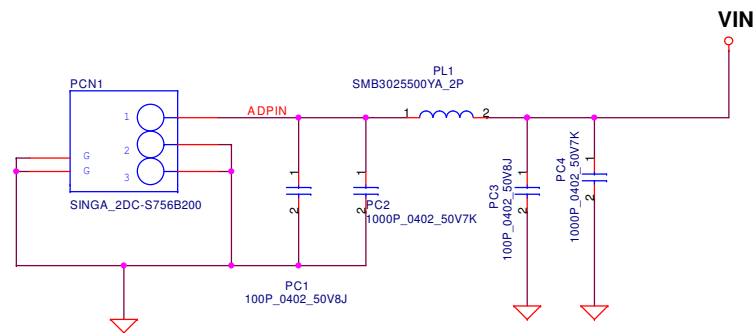
05/23 change to
voltage control FAL

[illegible]

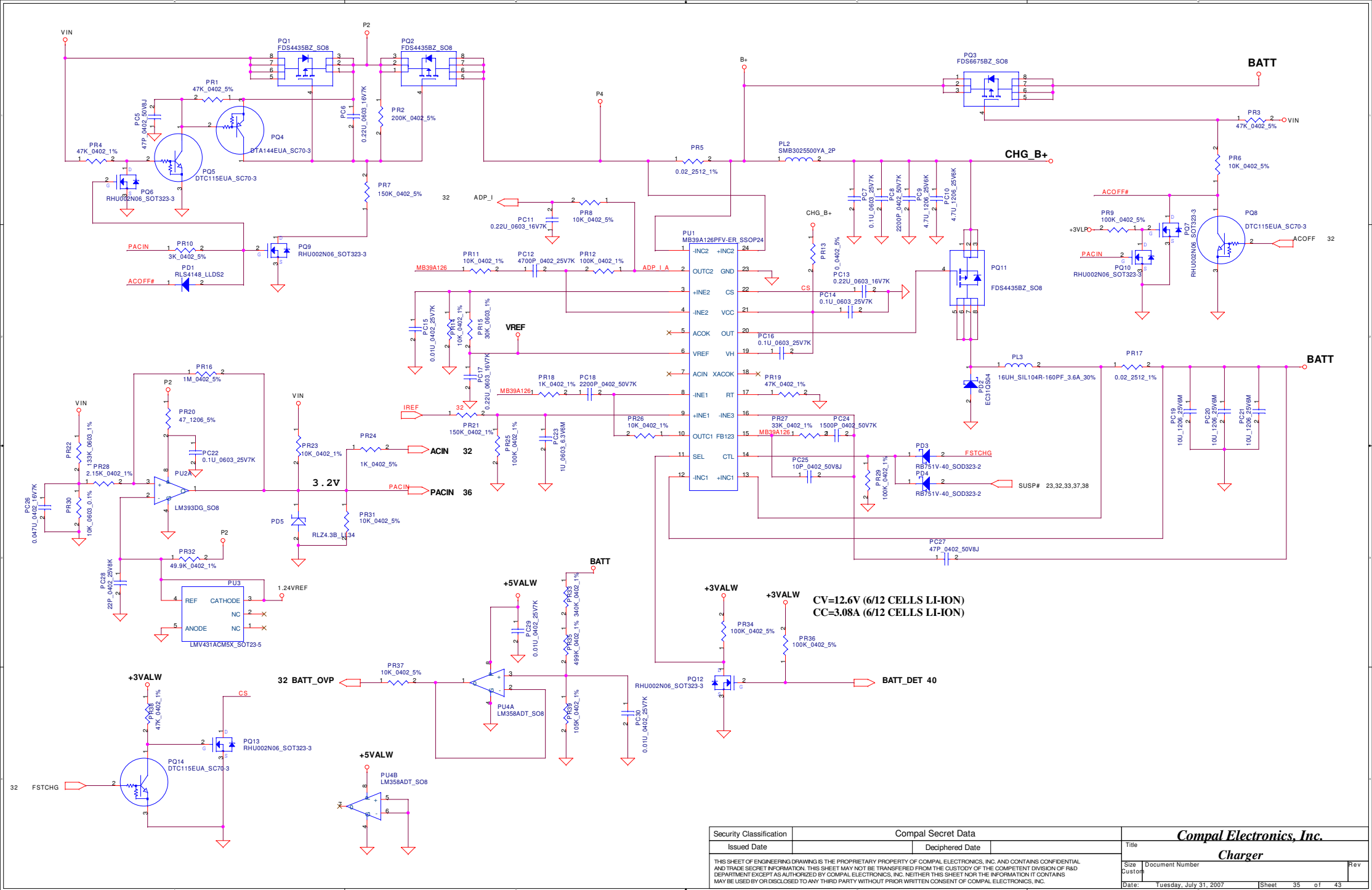
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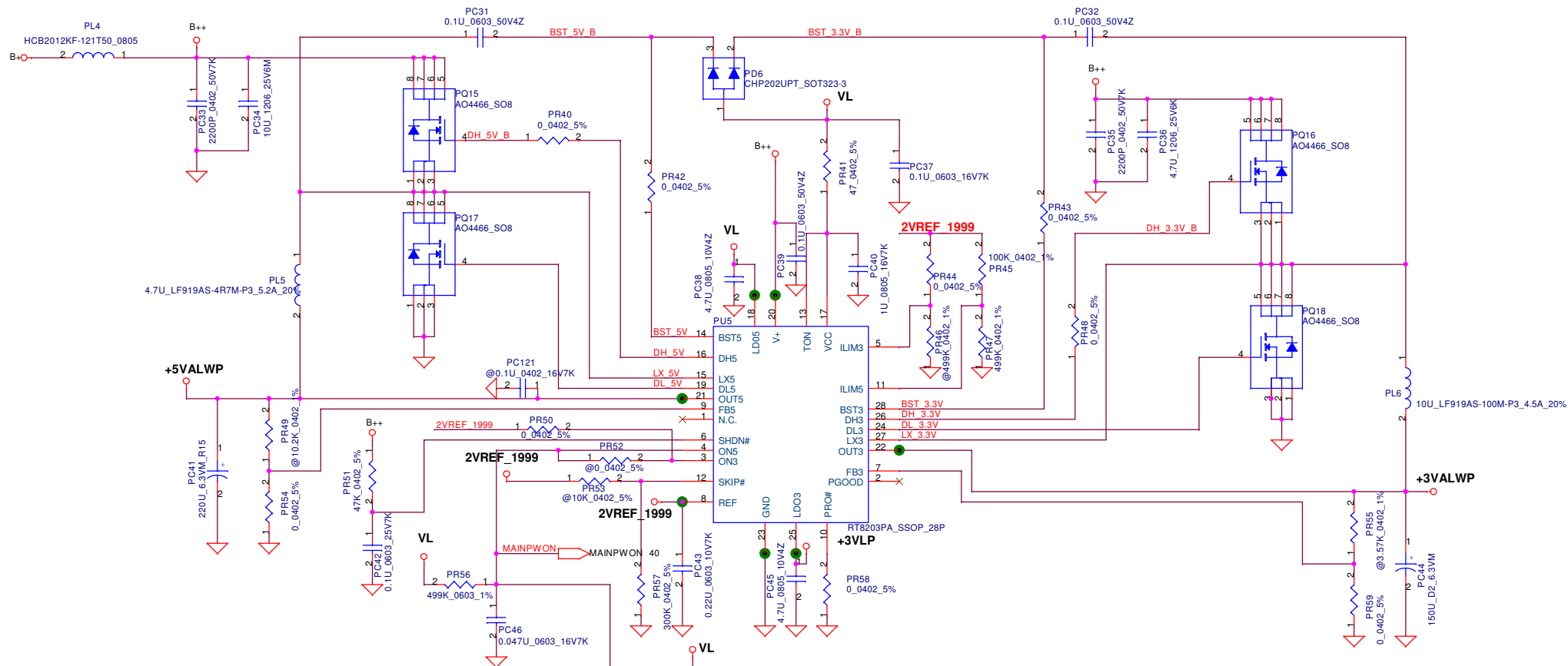


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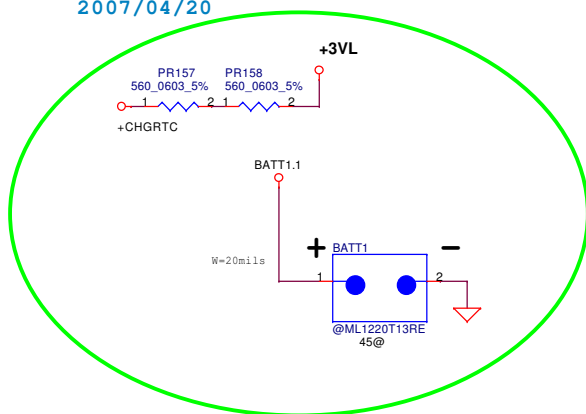


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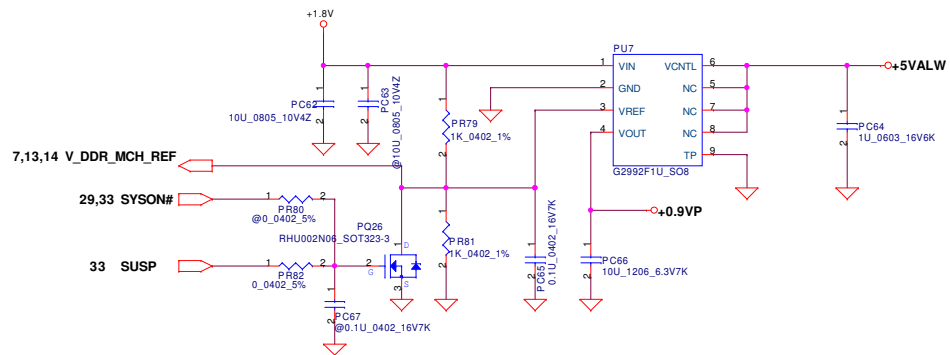
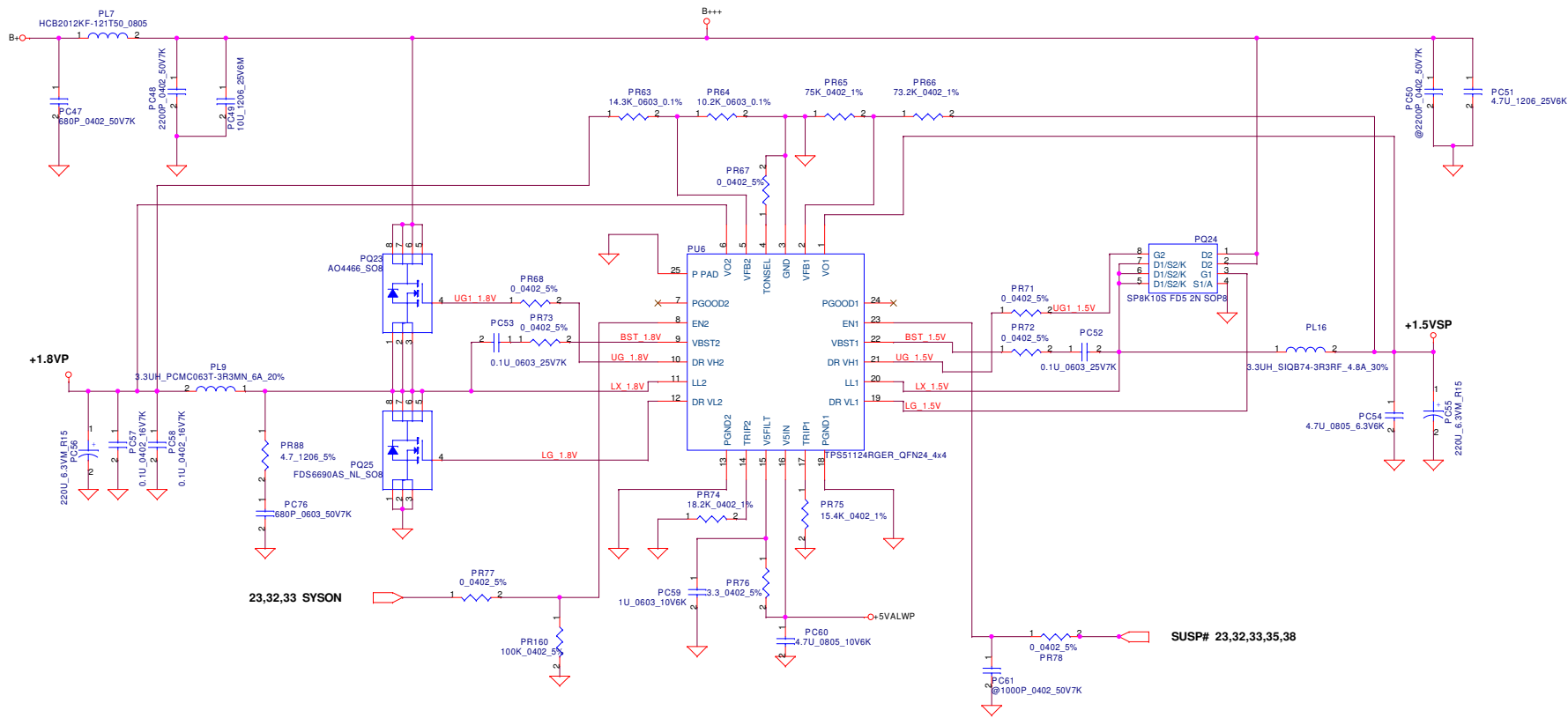




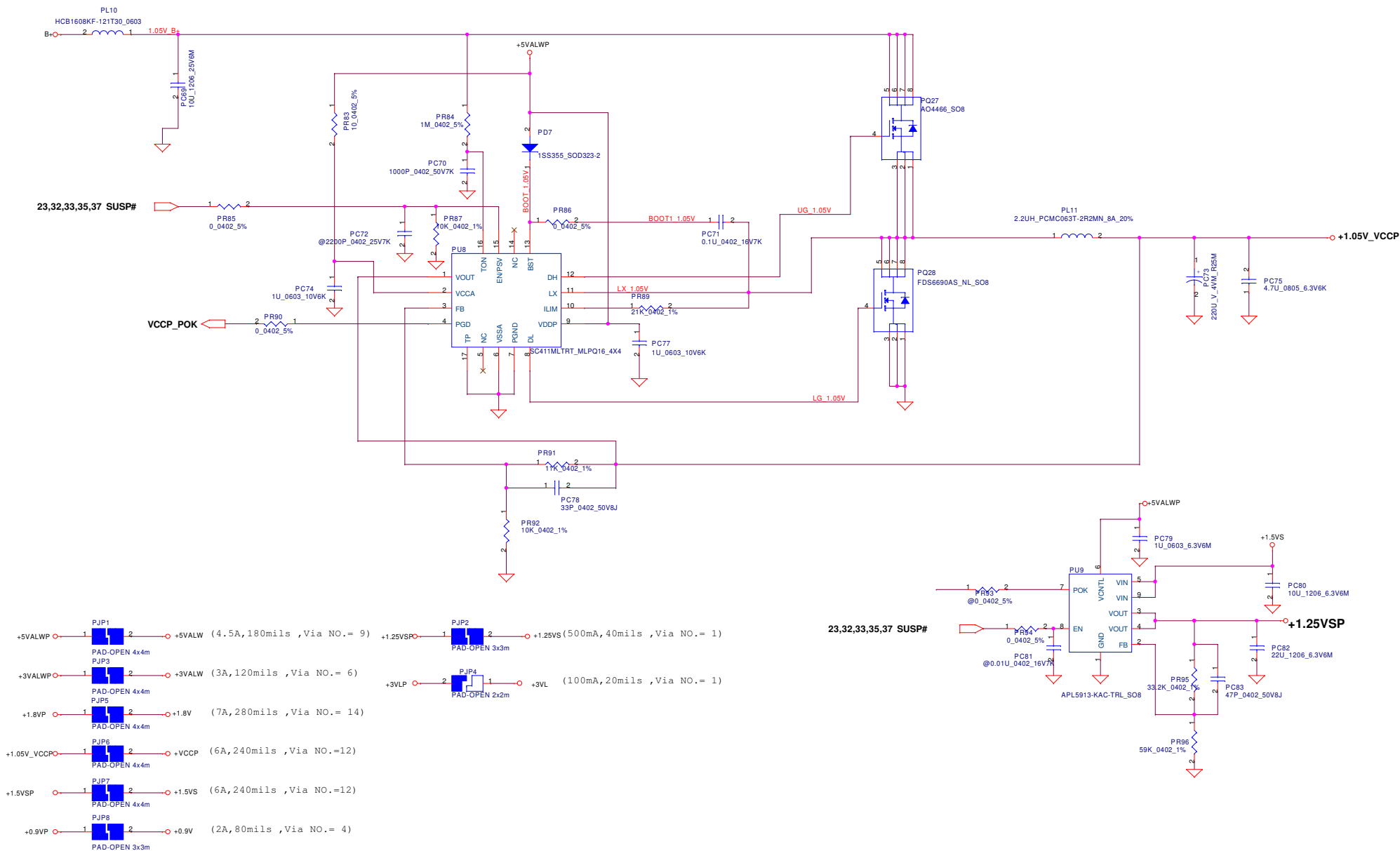
RTC Charger Circuit
2007/04/20



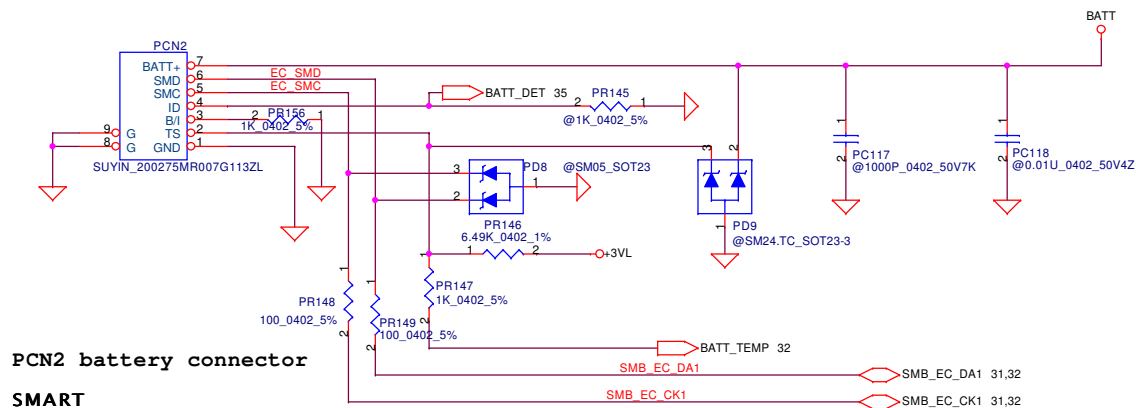
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				Size	Document Number	Rev
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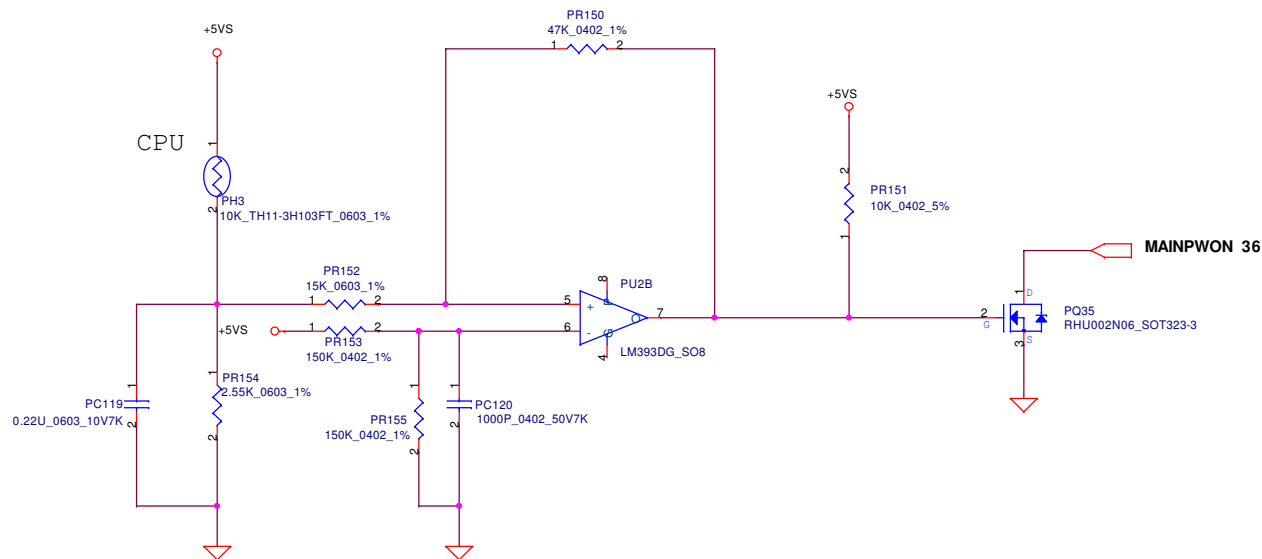


PCN2 battery connector

SMART
Battery:
7.BATT+
6.SMD
5.SMC
4.ID
3.B/I
2.TS
1.GND

PH3 under CPU bottom side :

CPU thermal protection at 90 $\pm$ 3 degree C
Recovery at 47 $\pm$ 3 degree C



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Version change list (P.I.R. List)

Power section

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Item	Reason for change	PG#	Modify List	Date	Phase
1	RT8203 crosstalk issue	37	add PC121 and 0.1uF	2007/05/24	SI
2	PU6 pin8 add a resistor to GND	38	add PR160 100K_ohm	2007/05/24	SI
3	remove PL15	36	remove PL15	2007/06/12	SI
4	EMI request	39	add PC122,PC123,PC124,PC125,PC126,PC127,PC128	2007/07/23	PV
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

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SizeCustom

Document Number

Rev0.2

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Version change list (P.I.R. List)

Power section

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Item	Reason for change	PG#	Modify List	Date	Phase
1	EC team request	32	ACIN add 100P (C505) to GND	2007/05/30	SI
2	Change Board ID	32	R407 from 0 Ohm to 8.2K,R405 install 100K	2007/05/30	SI
3	USB power switch fail	29	U23 & U17 change pin 4 from SLP_S5# to SYSON#	2007/05/30	SI
4	FAN use voltage control	4	del U2,Q1;add U24,C13 for 3 pin FAN	2007/05/30	SI
5	USB JP24 fail	29	Change pin define	2007/05/30	SI
6	Speaker output fail	28	Add R457,R458,R459 for Line_out	2007/05/30	SI
7	MS Pro fail	26	Add MS_D1,MS_D2,MS_D3 net	2007/06/06	SI
8	WLAN LED fail when disable WLAN	30	Add R232 pull high +5VS	2007/06/06	SI
9	+3VALW leakage	30	Del R387	2007/06/06	SI
10	Capacitor board fail	32	Add net CAP_RESET for Capacitor board reset	2007/06/06	SI
11	XDP fail	15	XDP clock share in robeson card	2007/06/06	SI
12	LAN power consumption is too large when S3	24	Add Q22	2007/06/14	SI
13	RJ11' cap is duplicate MDC module.	25	Delete C378,C379	2007/06/14	SI
14	Reverse some resister for tring ENE cap board	30 32	Add R460~R468,R451	2007/06/14	SI
15	+LCDVDD over current when diplay.	17	Change R163 from 47K to 100K Change C248 from 0.1U to 0.22U	2007/06/21	SI
16	LAN fail	24	Change JP14 pin define	2007/06/06	SI
17	WLAN LED (Amber led) issue	30	WLAN LED need change from +5VS to +3VS	2007/07/23	PV
18	030 project Bluetooth module issue	29	Swap pin5 & pin7	2007/07/23	PV
19	change Cap board LED supply voltage	30	from +3VS to +5VS	2007/07/23	PV
20	CMOS timing can't reset	19	SHORT PAD (CLRP3) connect between +RTCVCC and GND	2007/07/23	PV
20	EMI issue (CPU core)	5	add C43 & C44 (330U)	2007/07/23	PV
21	EMI/ESD issue (XDO connector)	4	delete XDP connector	2007/07/23	PV
22	EMI/ESD issue (RJ11 connector)	25	add 1000P at RJ11 RING & TIP	2007/07/23	PV
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