DELL Vostro 1320
COMPAL LA-4232P - KAL80

Half Penny Bridge 13.3
Compal Confidential

Schematic Document

Cantiga + ICH9

2009 / 06 / 01 Rev:1.0(A00)

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title: SCHEMATIC, M/B LA-4232P
				Size: Custom; Document Number: 401593; Rev: C
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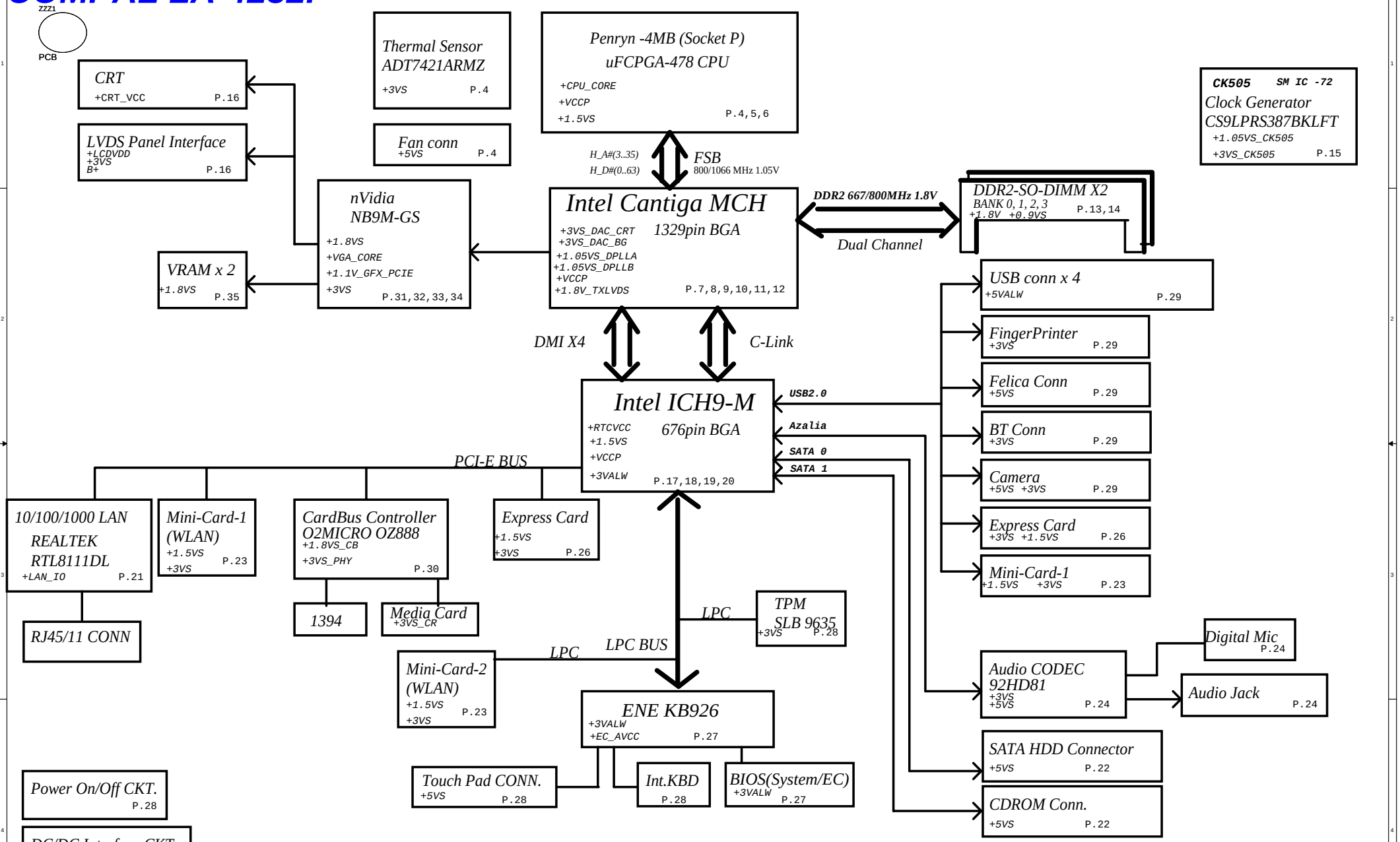
COMPAL LA-4232P

Half Penny Bridge 13.3



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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

	USB PORT#	DESTINATION
ICH9-M	0	JUSBP1
	1	CAMERA
	2	JUSBP3(SINGLE)
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3(DUEL TOP)
	9	JUSBP3(DUEL BOTTOM)
	10	NA
	11	NA

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@: connect
VGA@: discrete component
UMA@: uma component
TPM@: TPM compoent

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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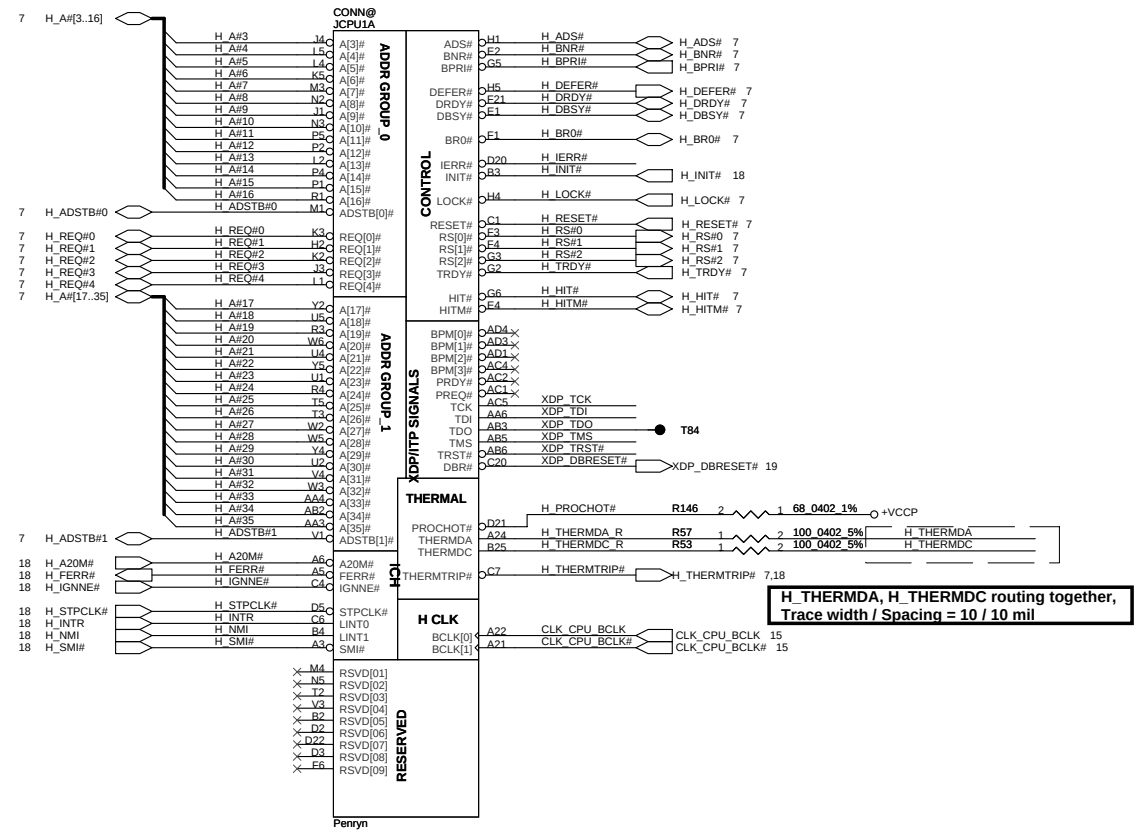
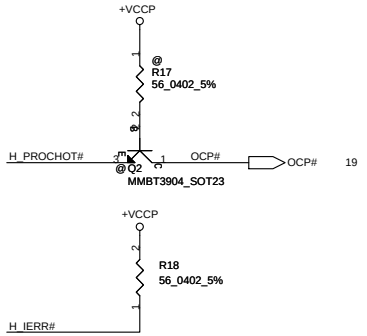
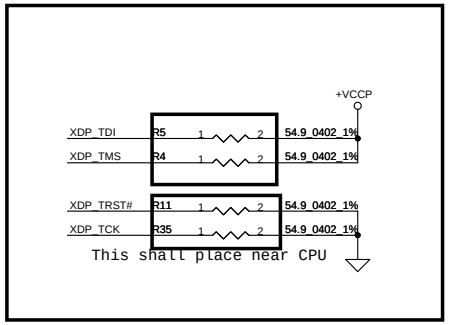
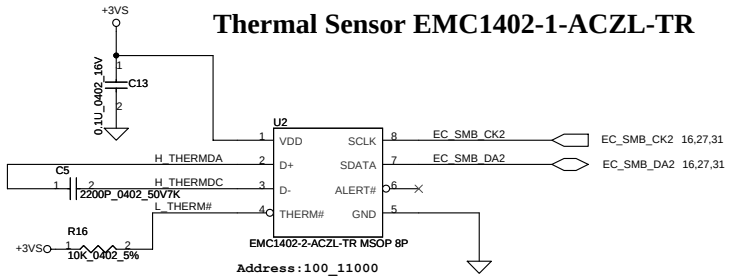


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

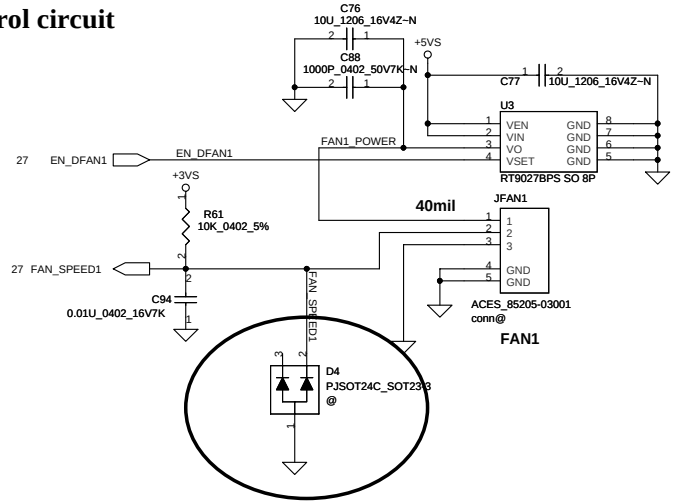




Thermal Sensor EMC1402-1-ACZL-TR



FAN Control circuit



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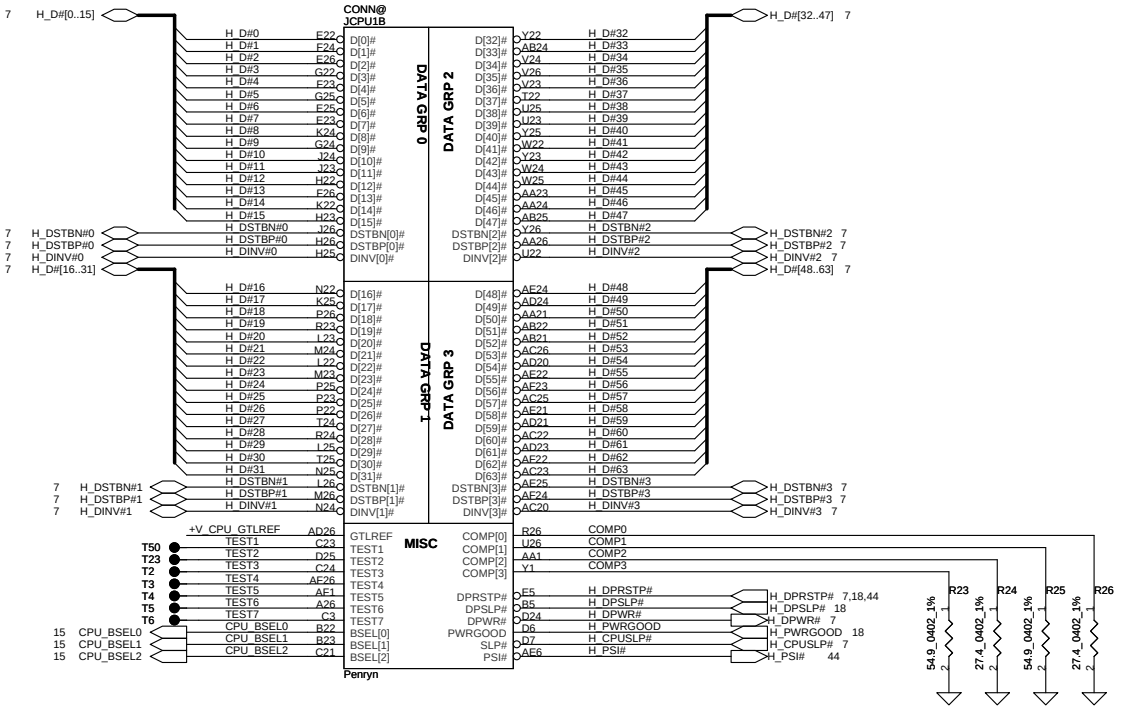
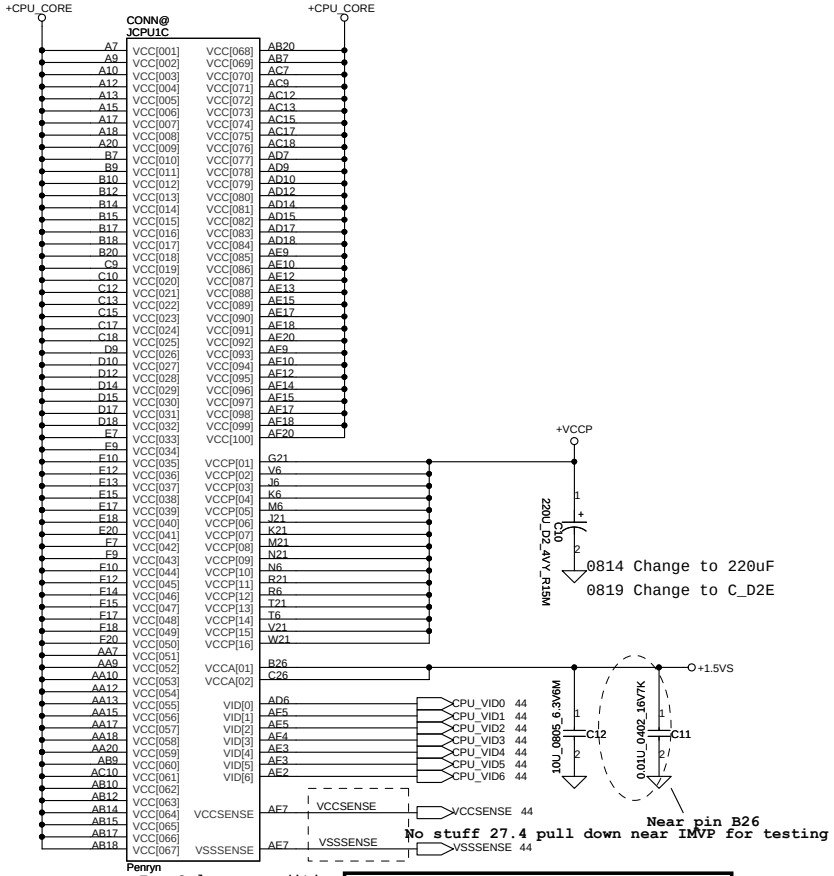




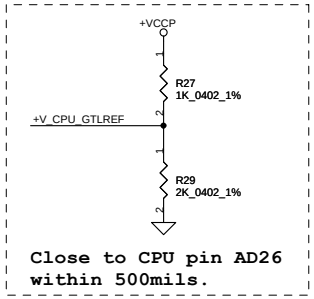
layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU

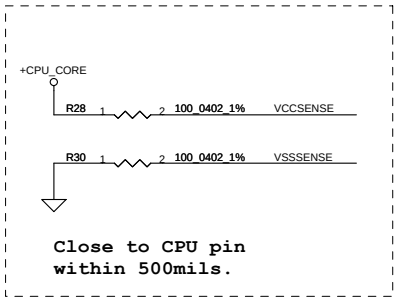
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 21 mils. COMP[1,3] trace width is 5

Length match within 25 mils. The trace width/space/other is 20/7/25.





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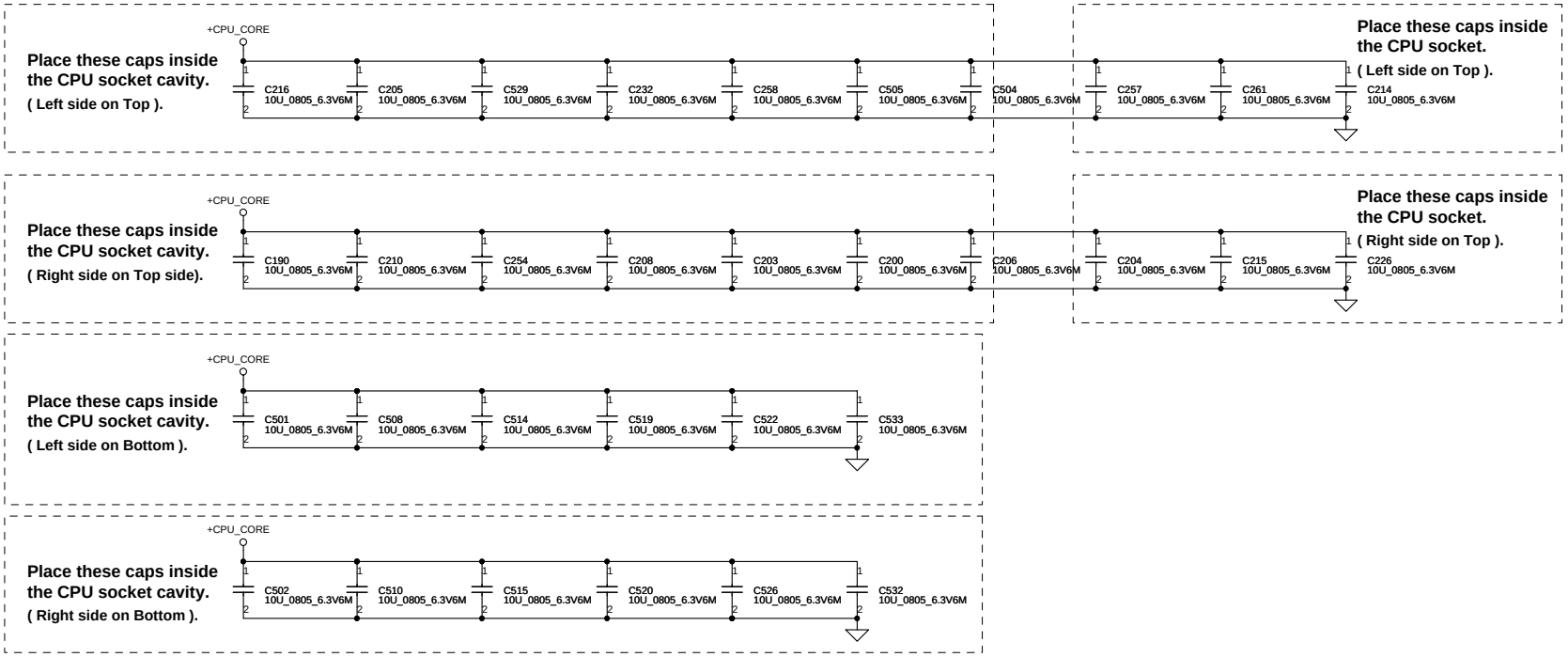
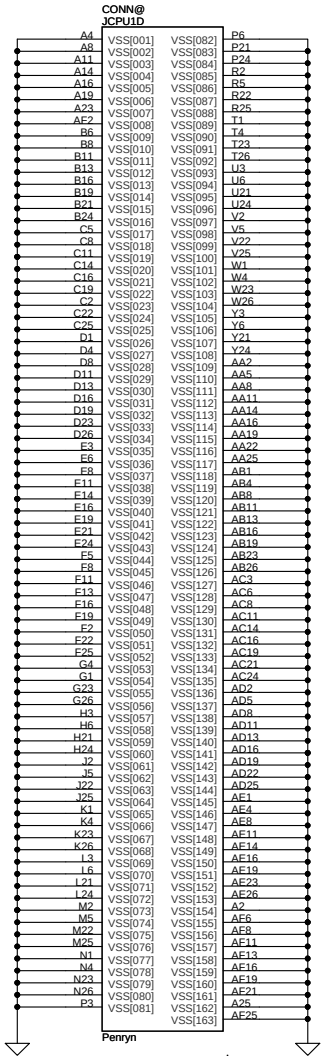
High Frequence Decoupling

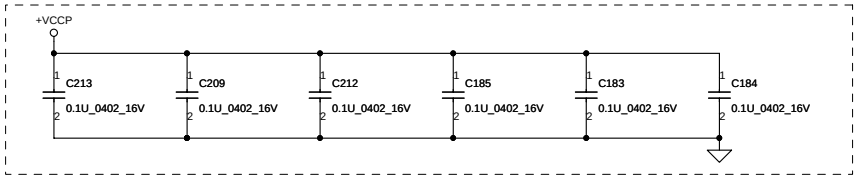
10uF 0805 X5R -> 85 degree.



ESR <= 1.5m ohm

Capacitor > 880 uF





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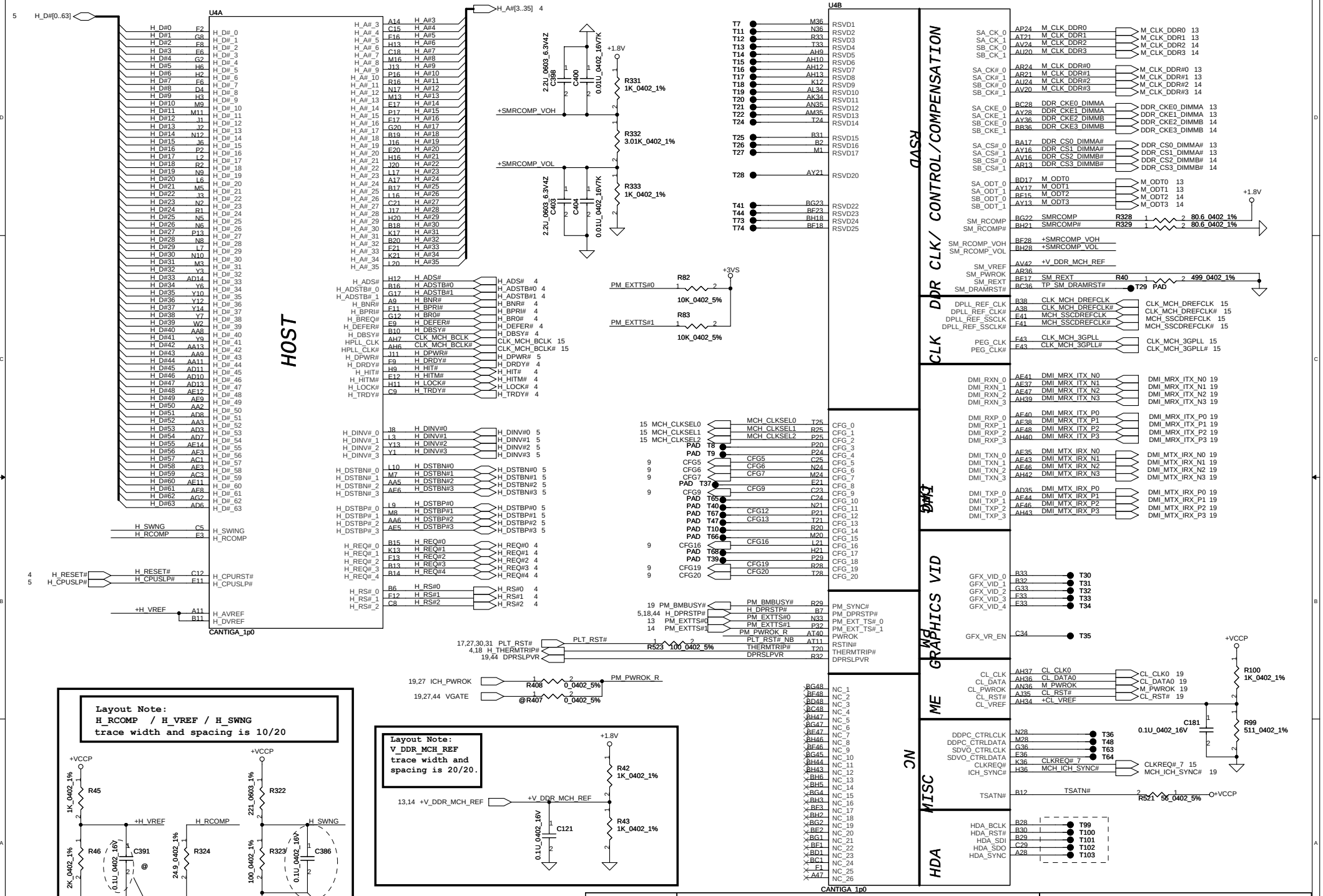
U4A
HOST
CANTIGA_1p0
U4B
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
GRAPHICS VID
ME
MISC
HDA
NC
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB
Near B3 pin
Layout Note:
V_DDR_MCH_REF
trace width and spacing is 20/20.
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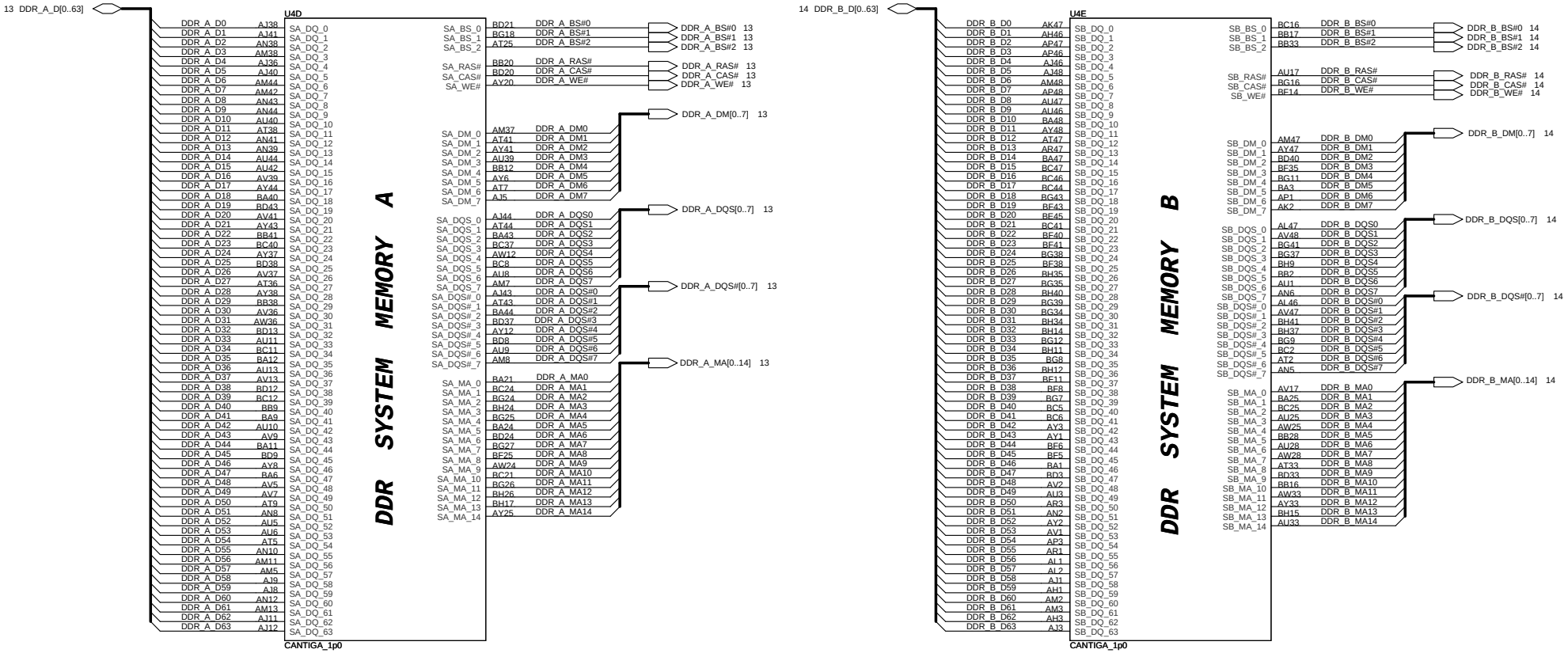

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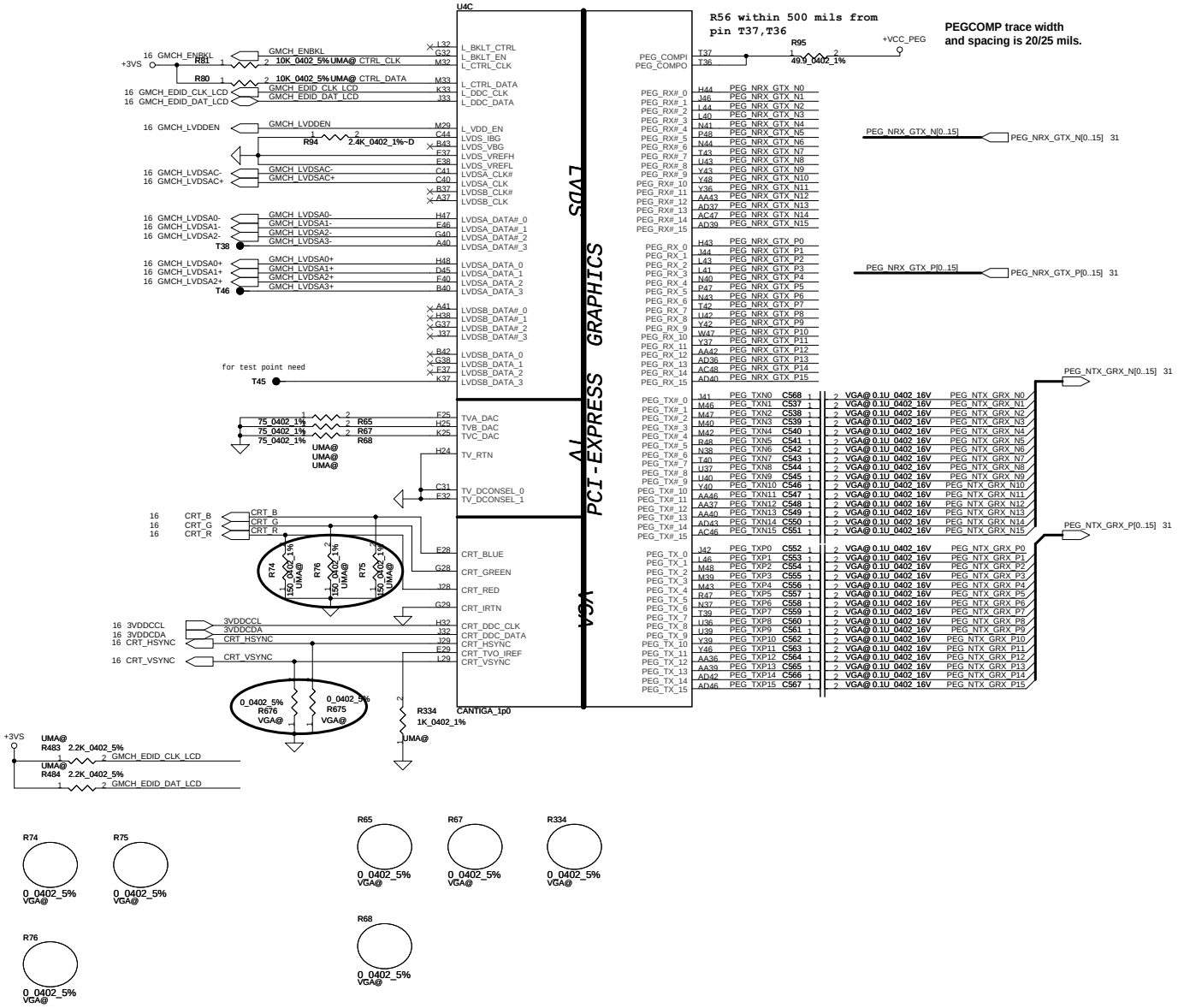
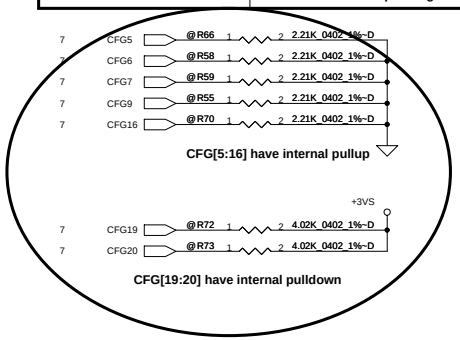


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable * 1 = The iTPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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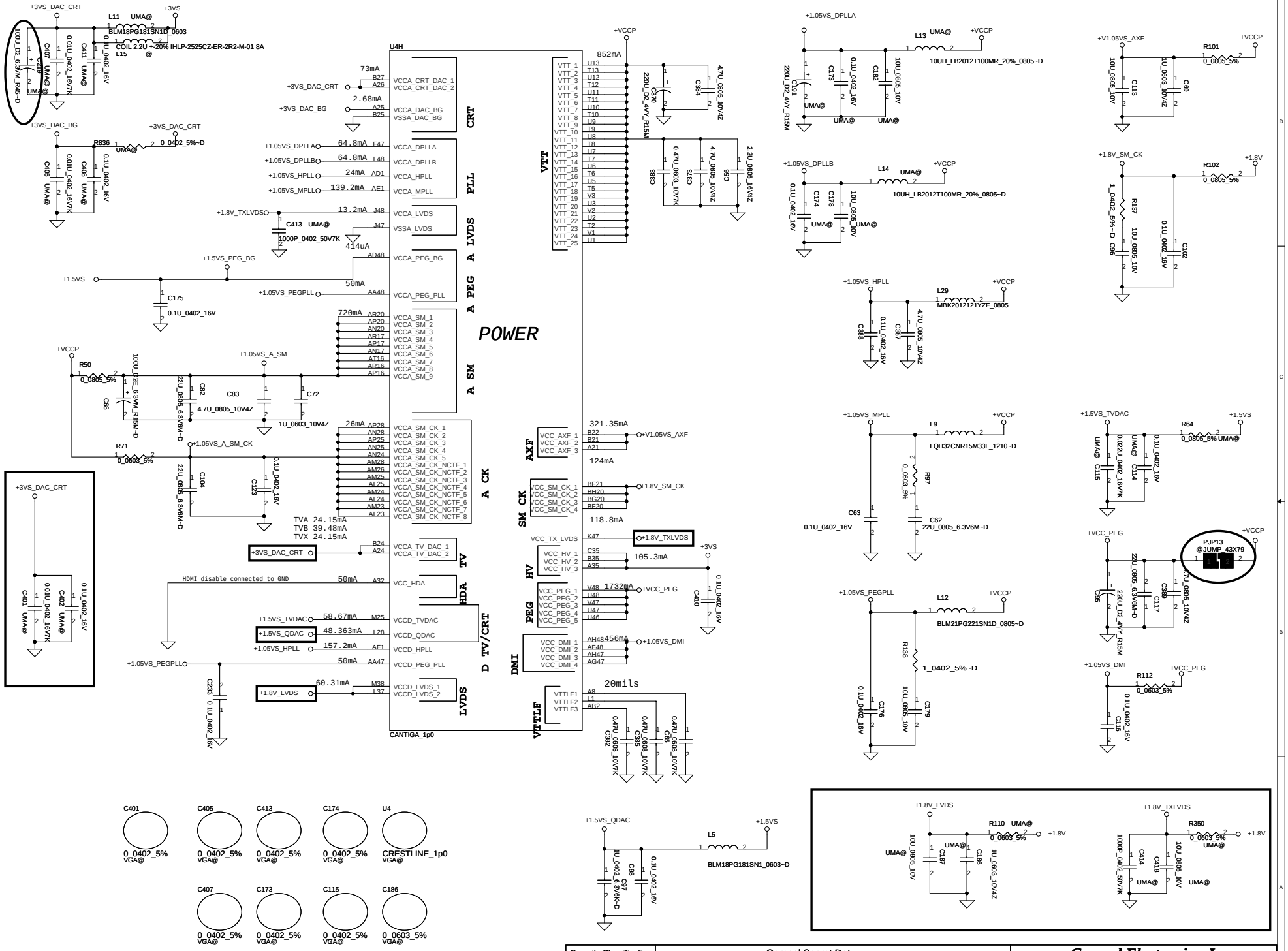

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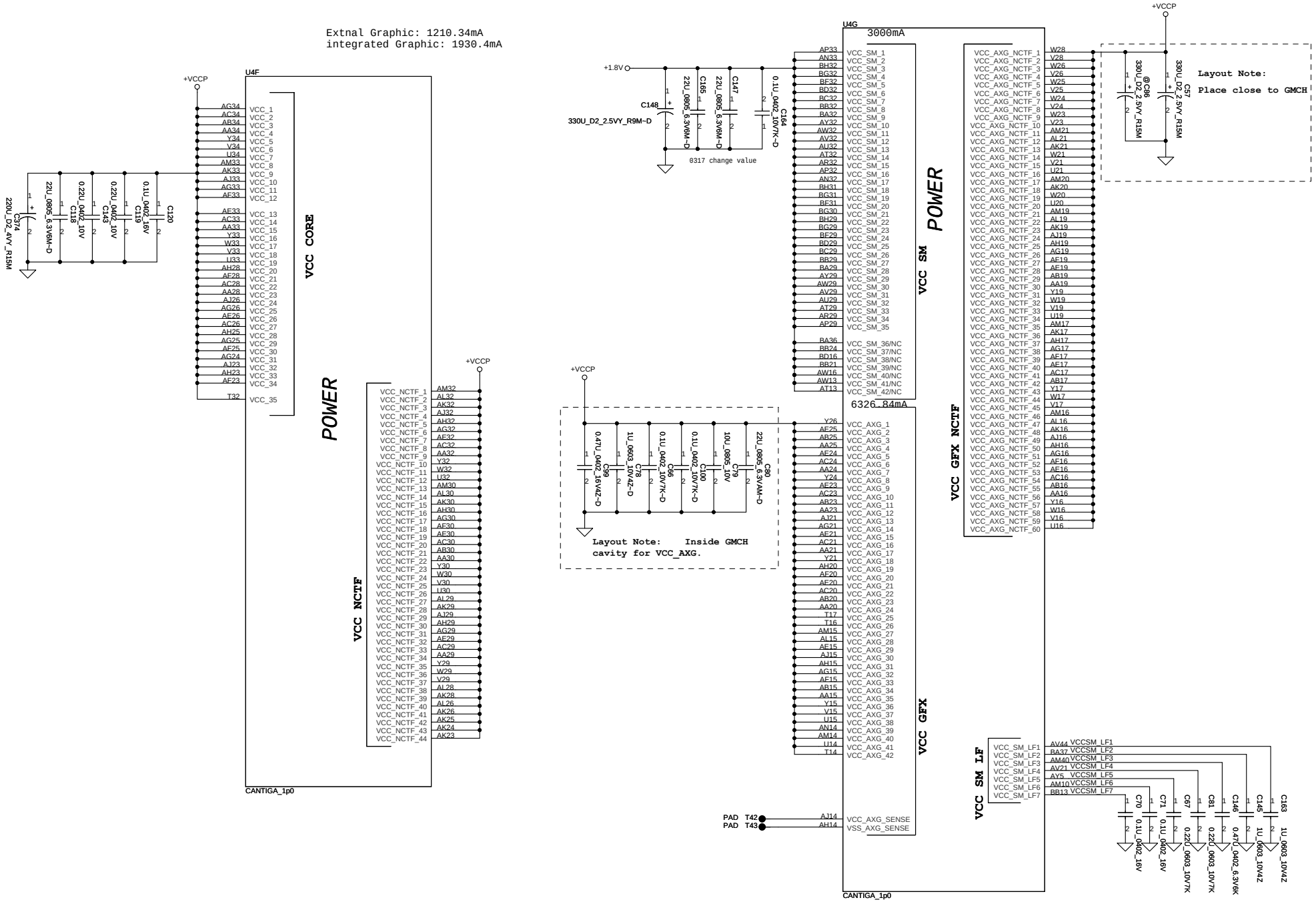

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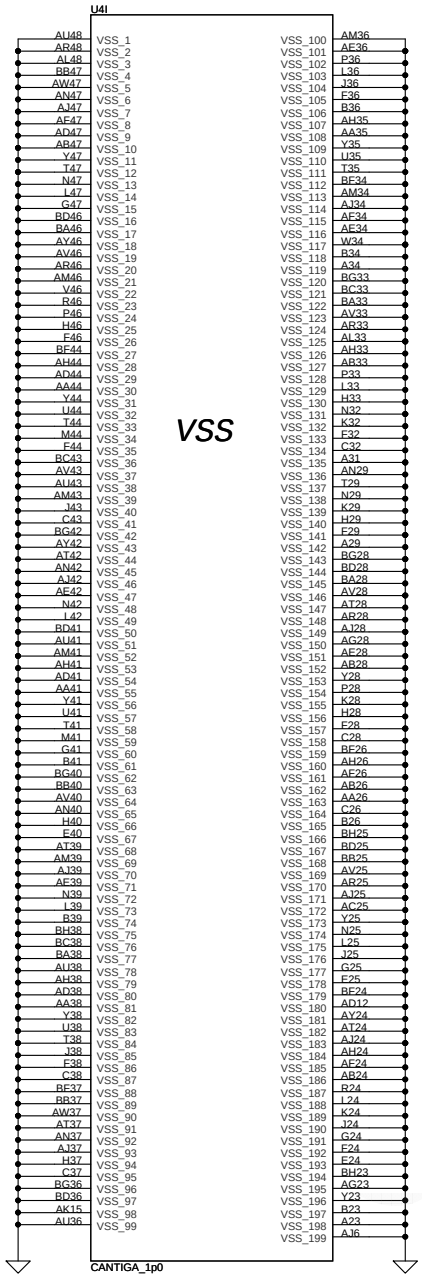

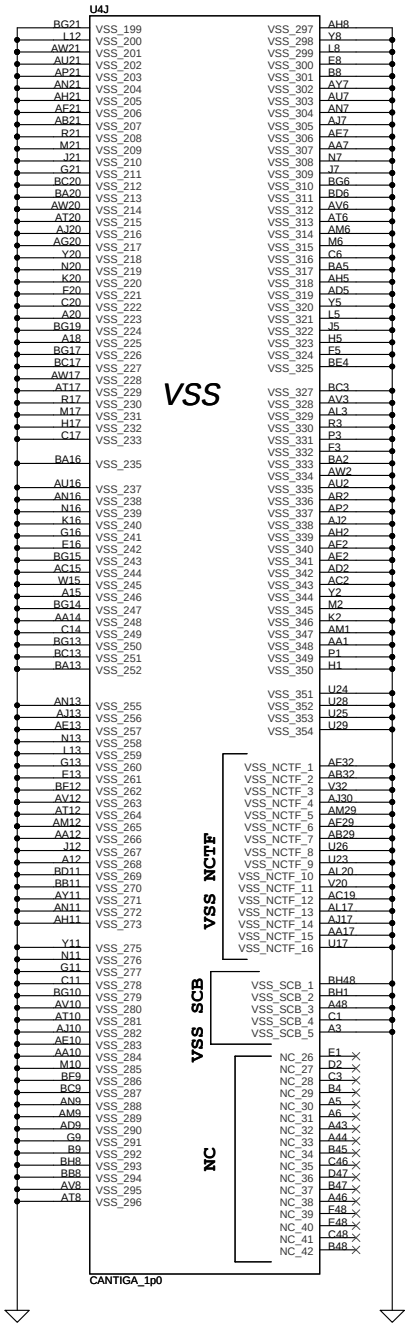

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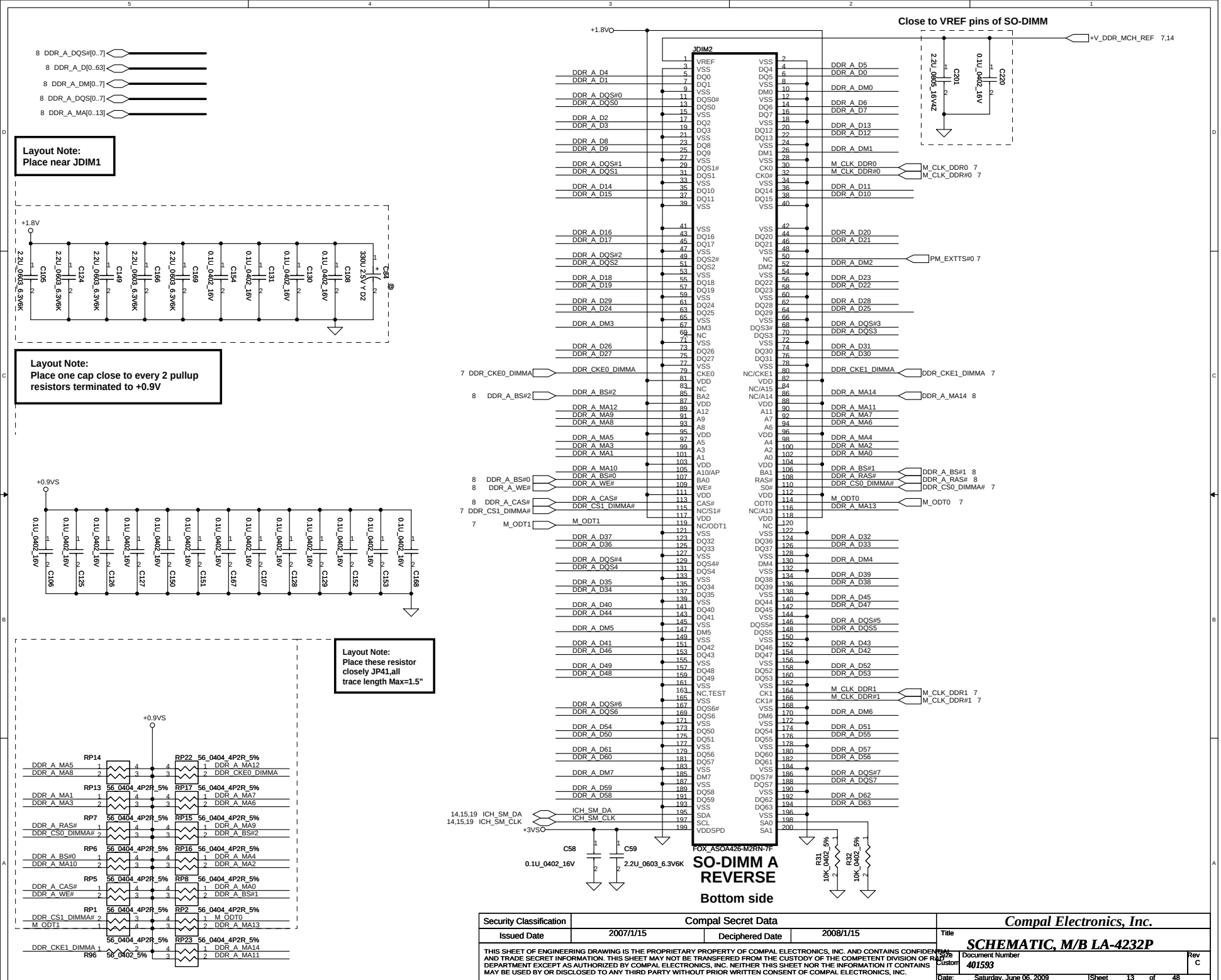

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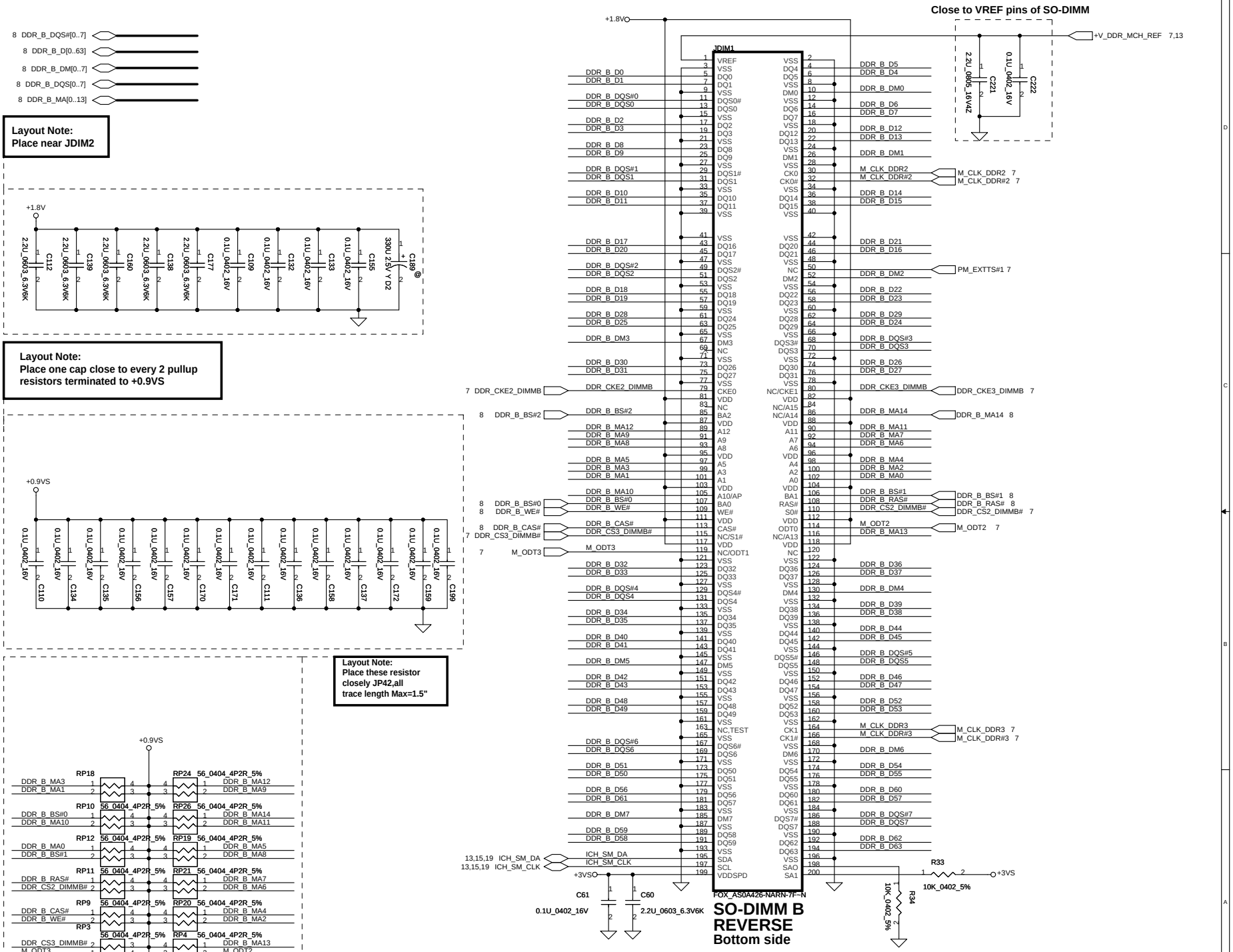

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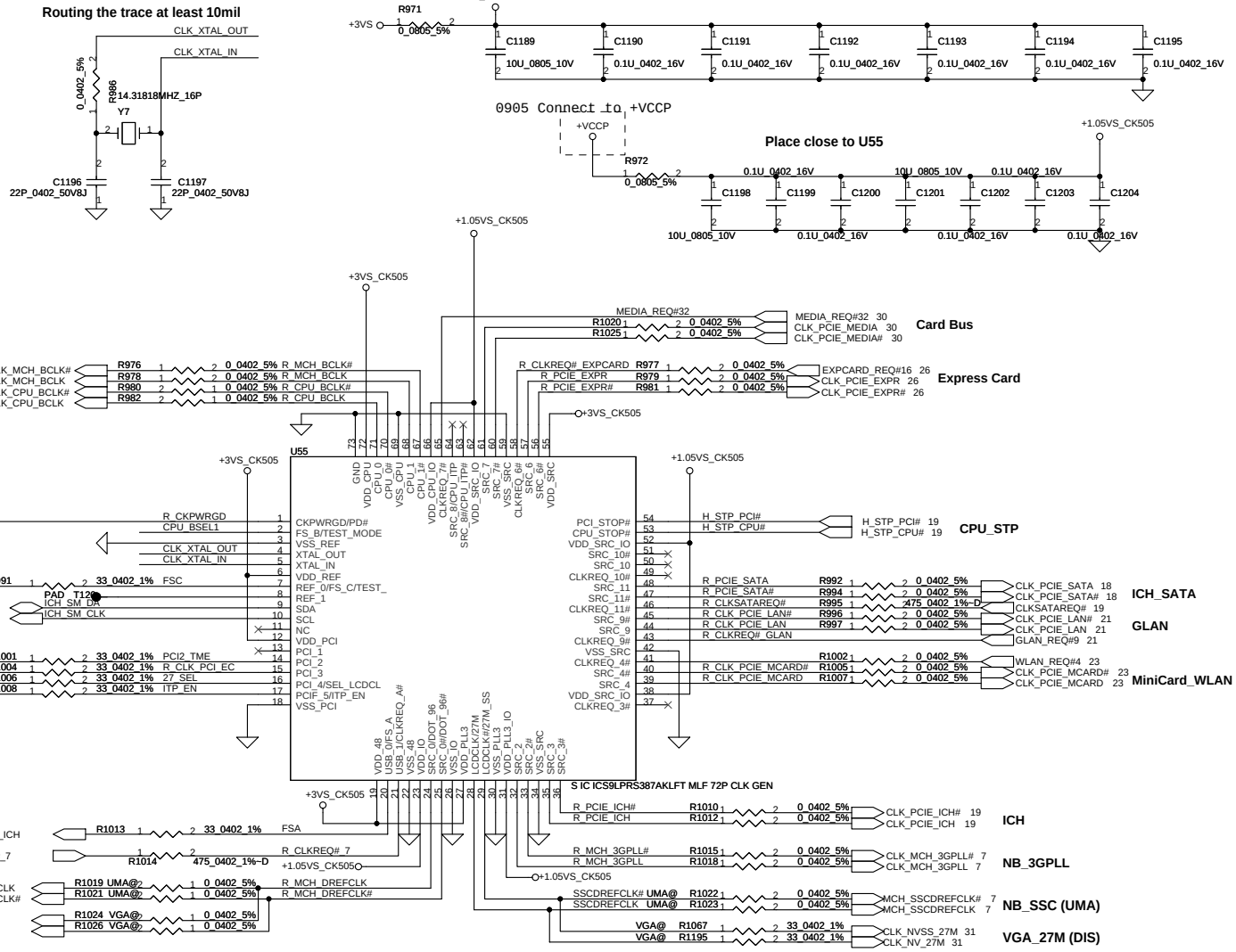
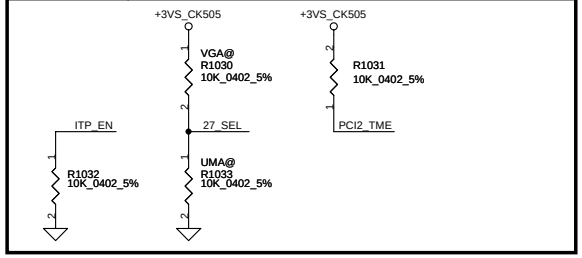
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

*



ITP_EN	* 0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed



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Issued Date	2006/02/13	Deciphered Date	2006/03/10

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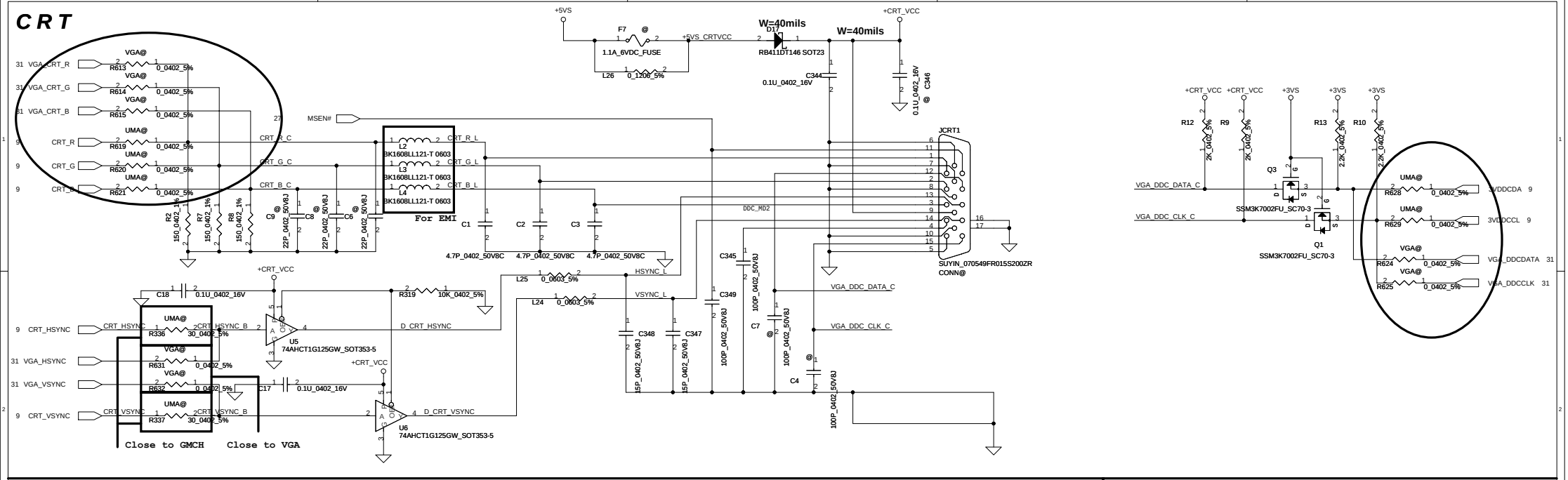
hoxain@hotmail.com

CRT



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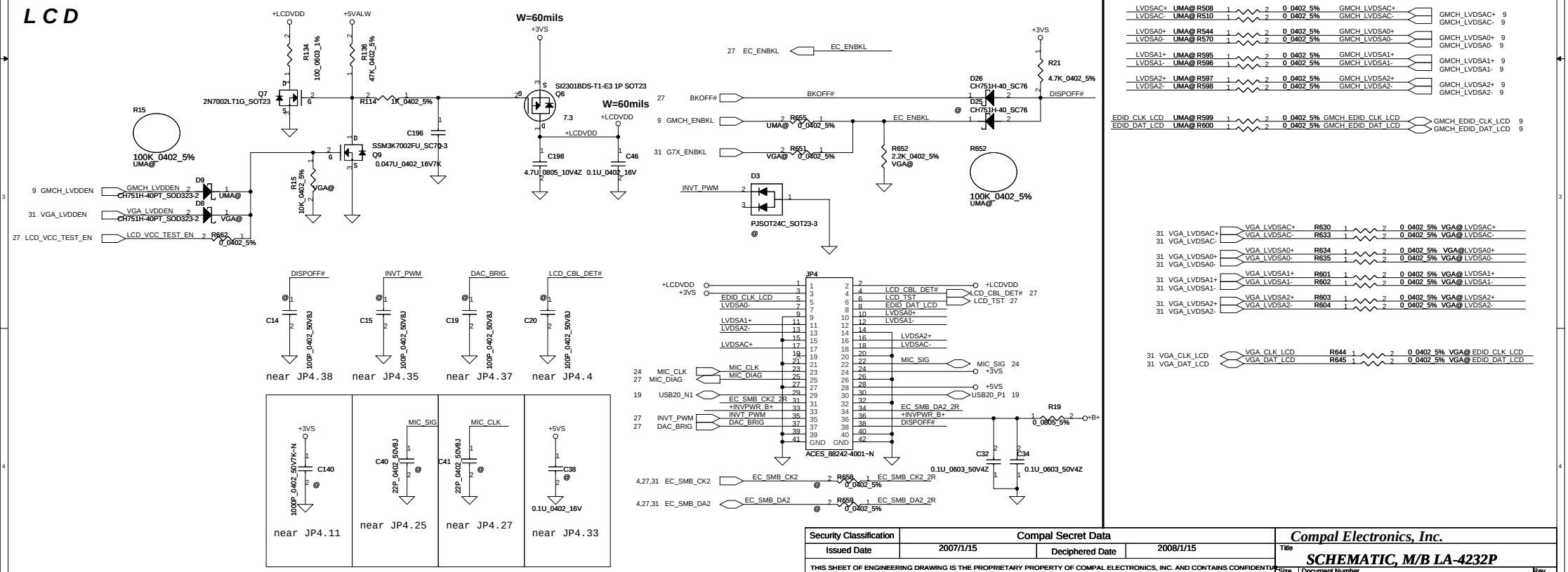

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Issued Date	2007/1/15	Deciphered Date	2008/1/15

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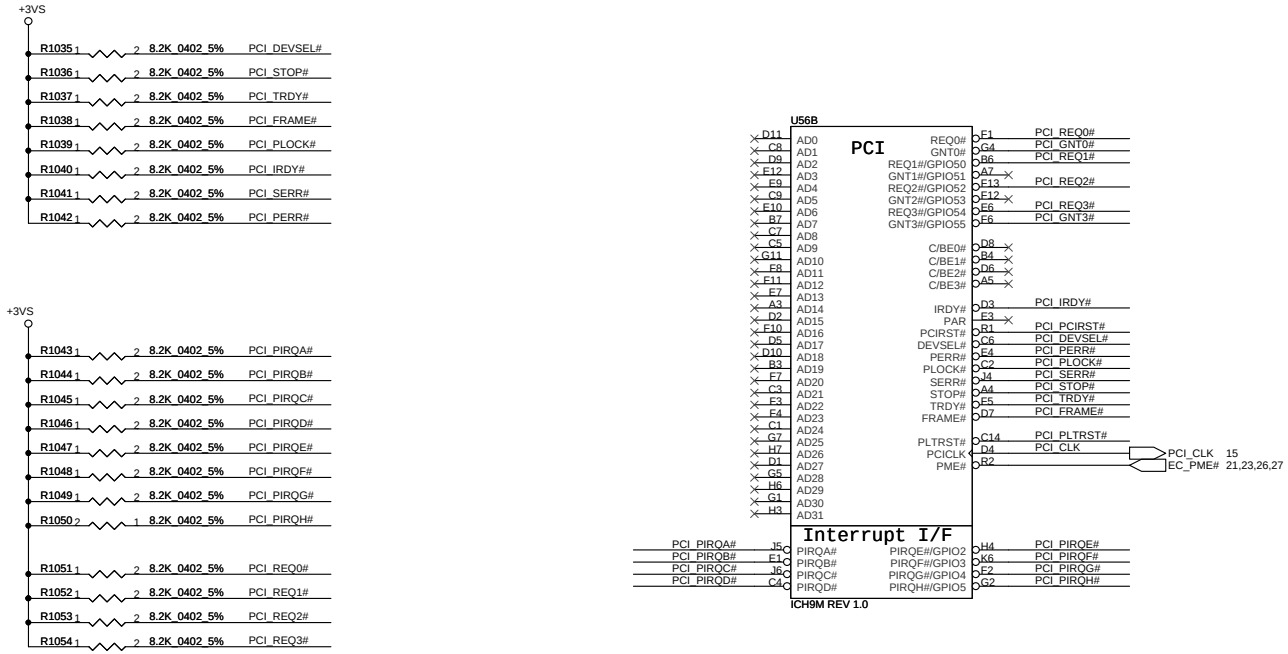
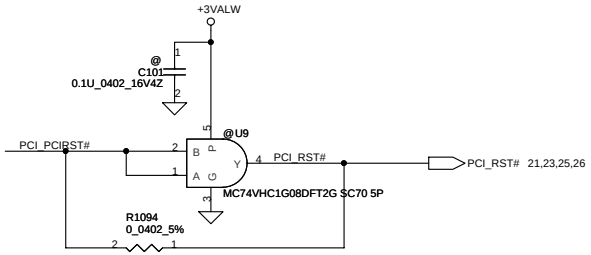
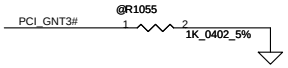
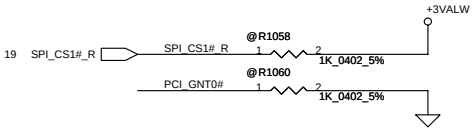


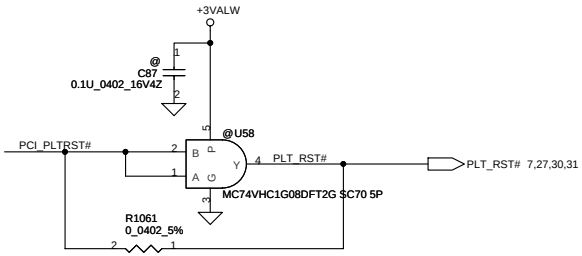


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





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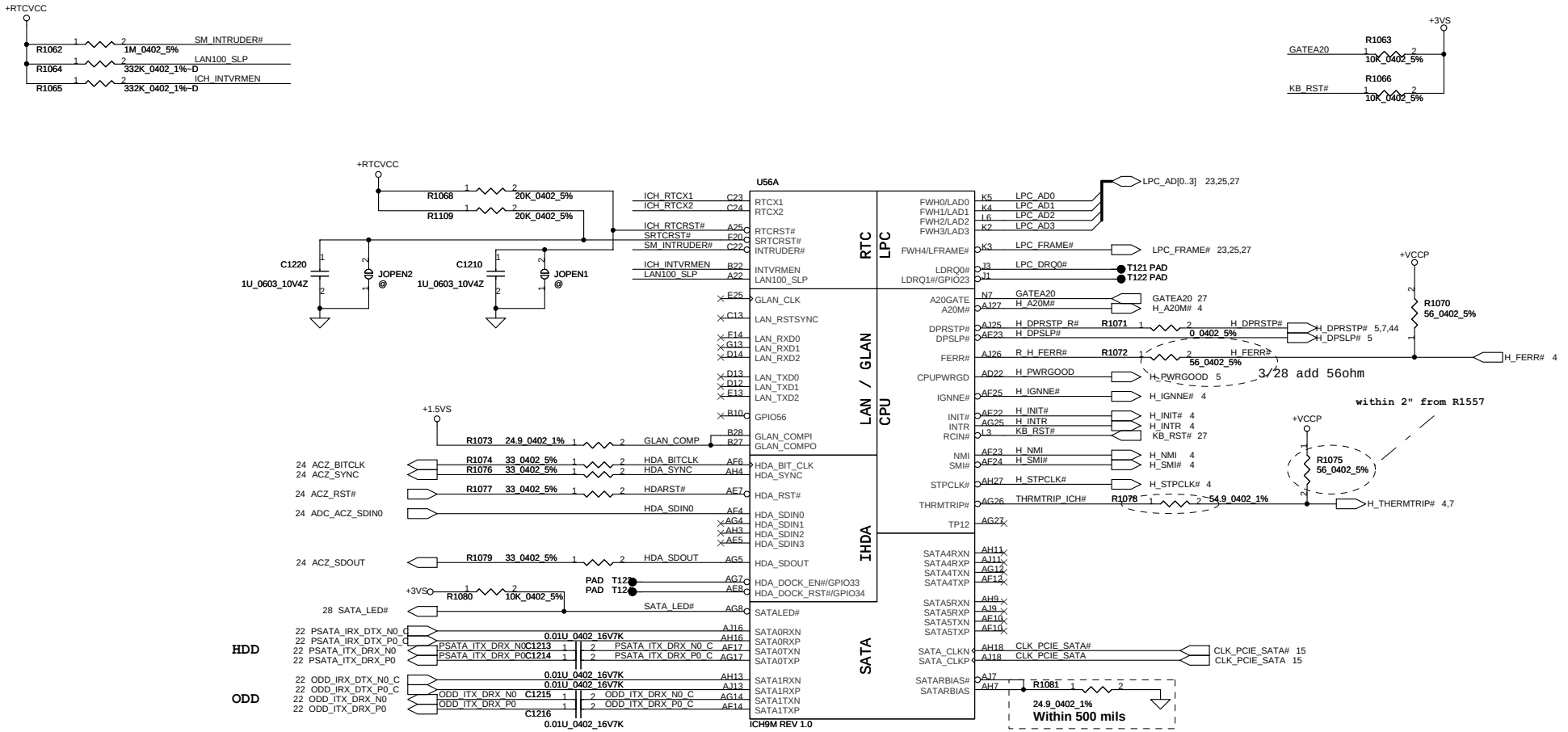

XOR CHAIN ENTRANCE STRAP:RSVD

XOR Chain Entrance Strap		
ICH_RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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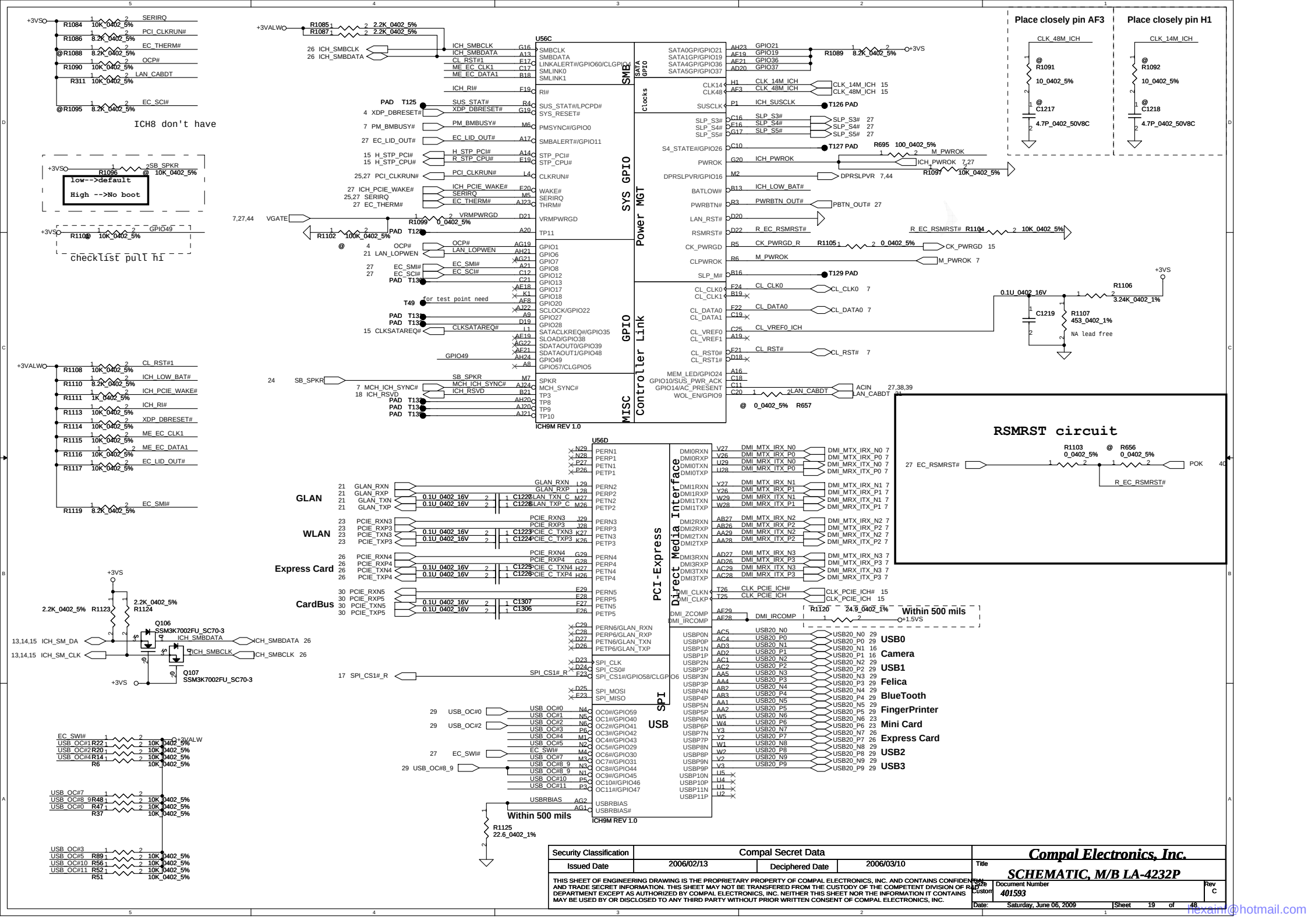
ICH8 don't have
low-->default
High -->No boot
checklist pull hi
U56C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M REV 1.0
Place closely pin AF3
Place closely pin H1
RSMRST circuit
U56D
PCI-Express
Direct Media Interface
SPI
USB
GLAN
WLAN
Express Card
CardBus
Within 500 mils
USB0
Camera
USB1
Felica
BlueTooth
FingerPrinter
Mini Card
Express Card
USB2
USB3
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Issued Date
2006/02/13
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2006/03/10
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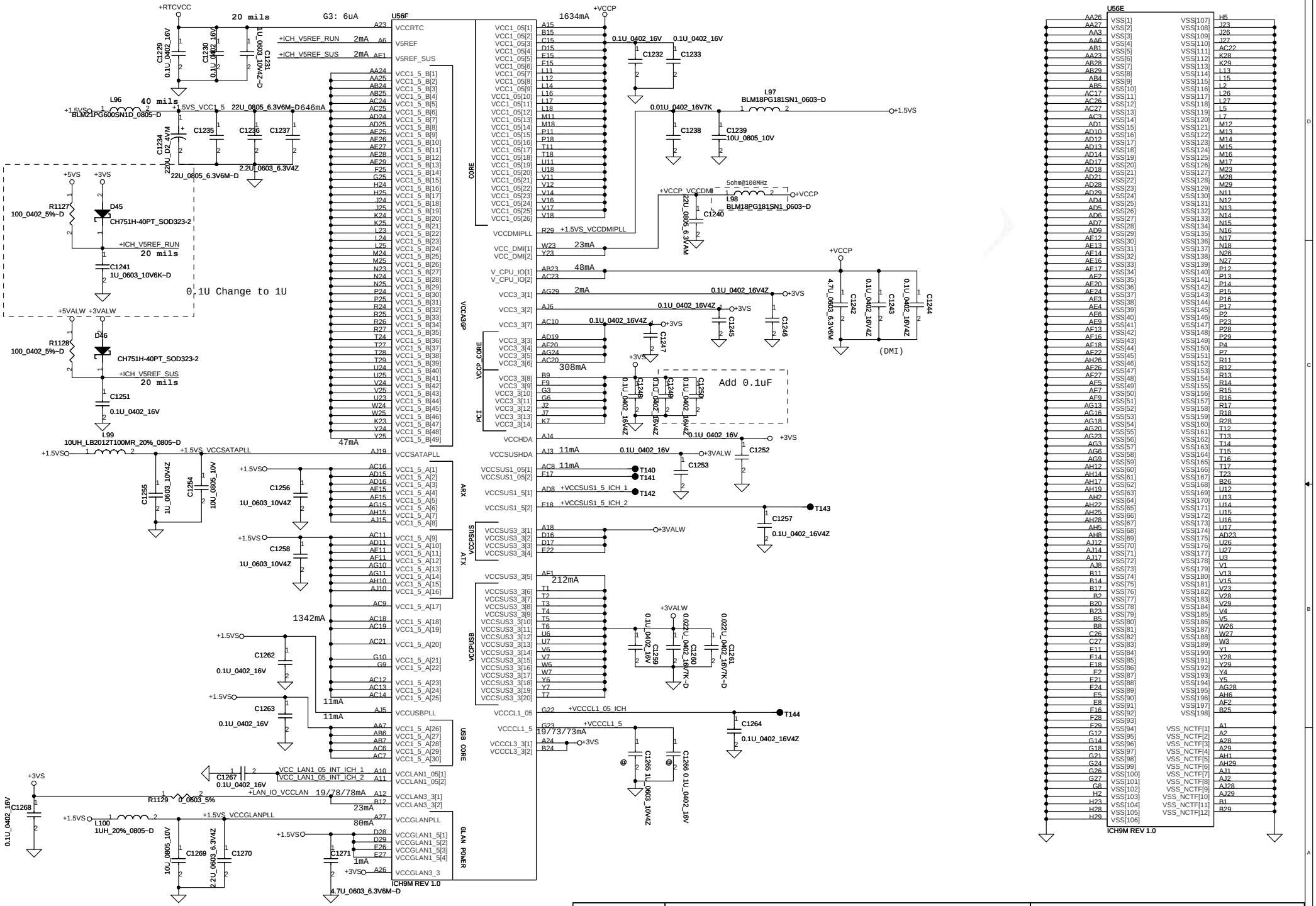

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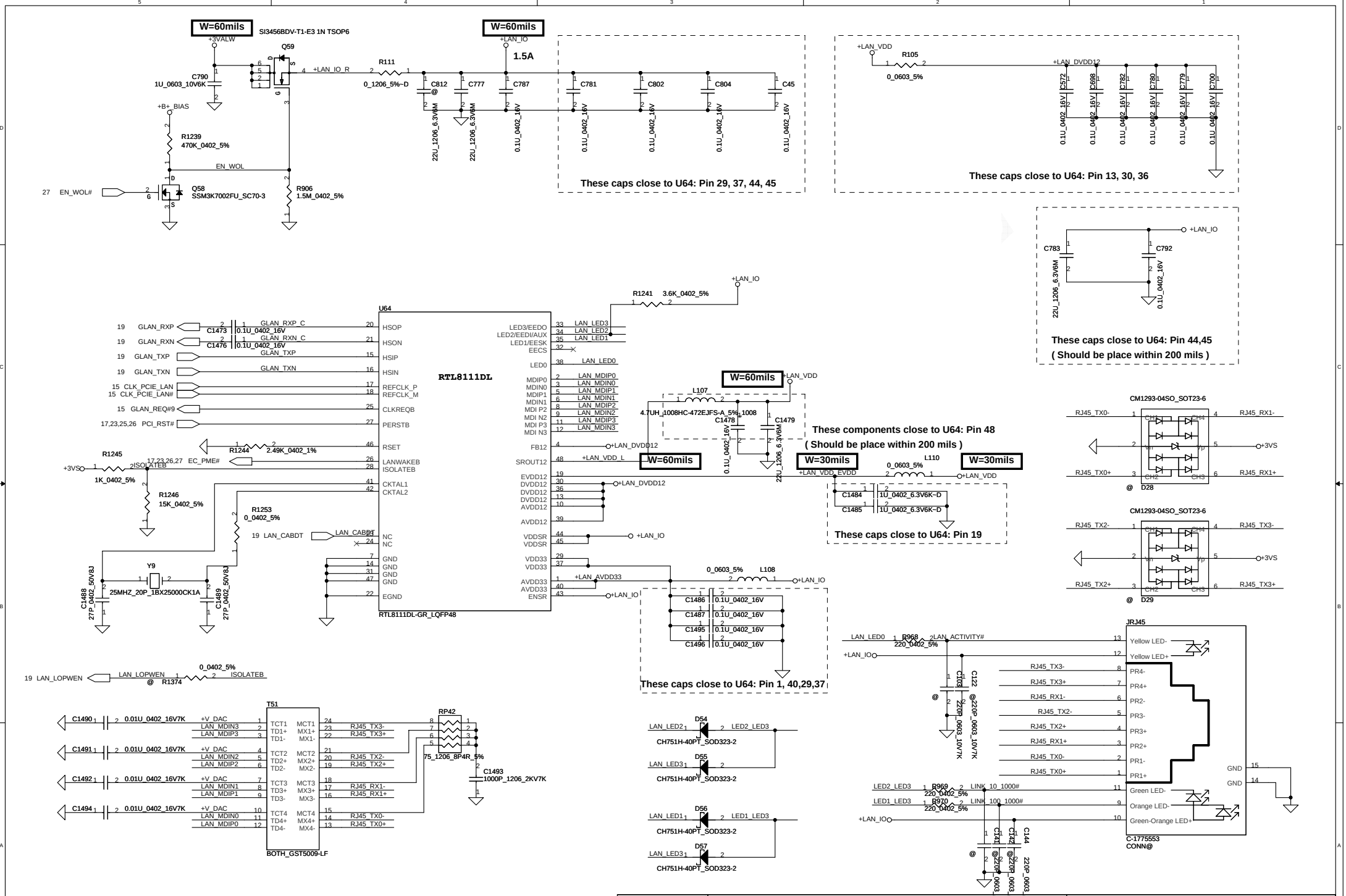

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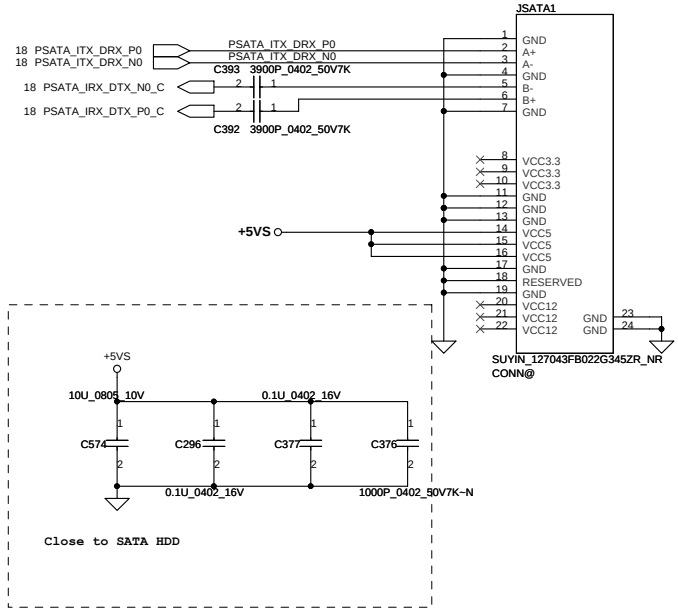

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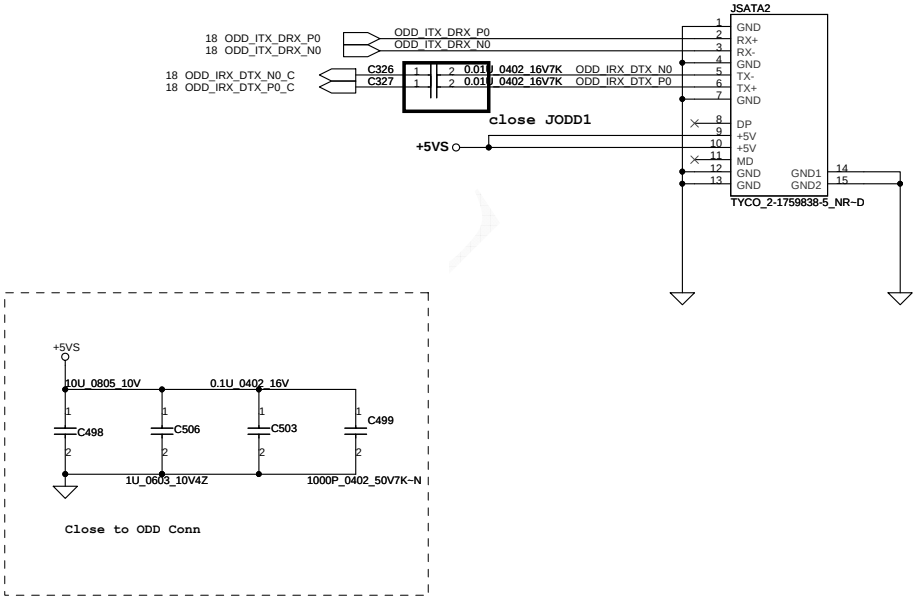

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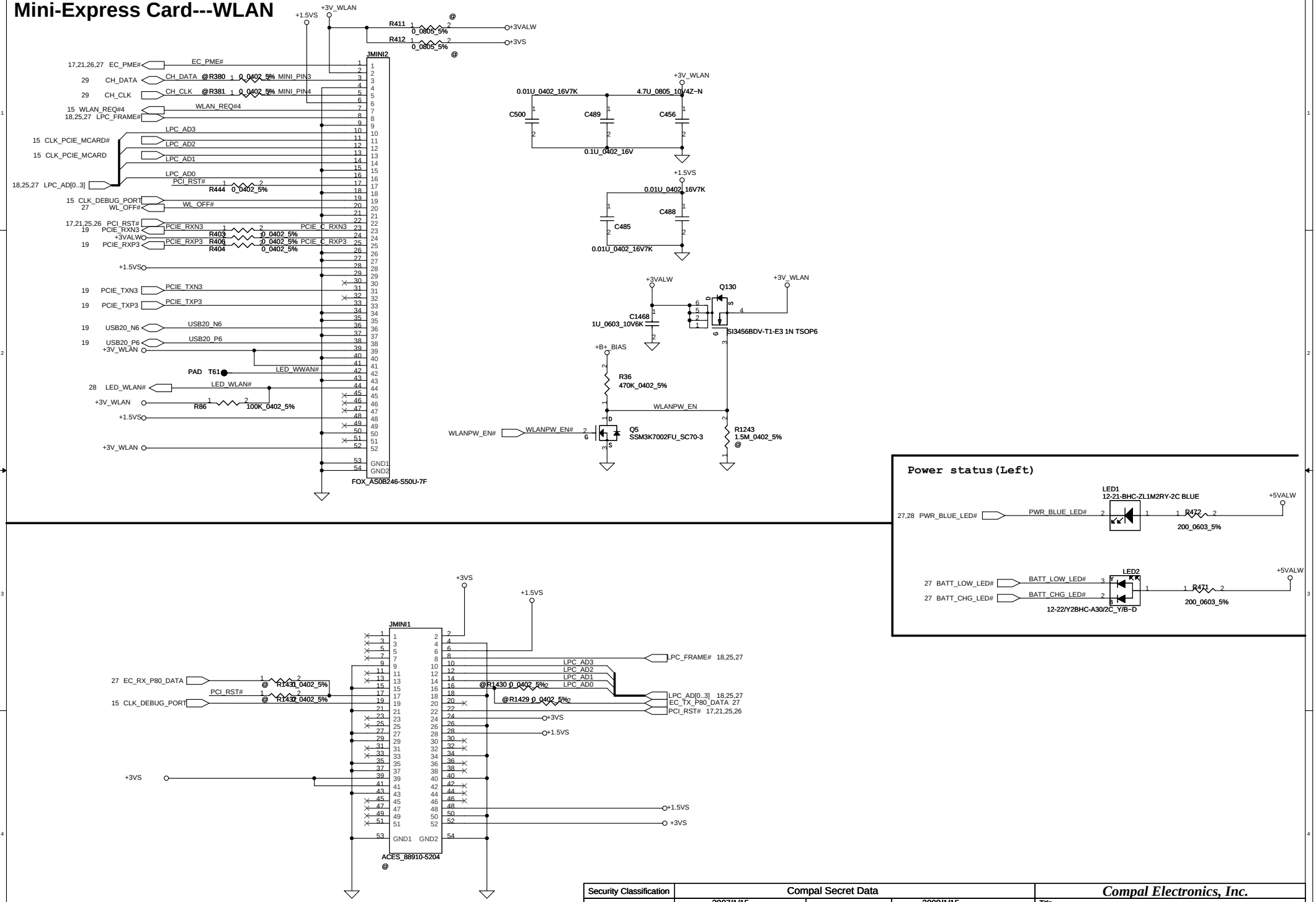
Mini-Express Card---WLAN



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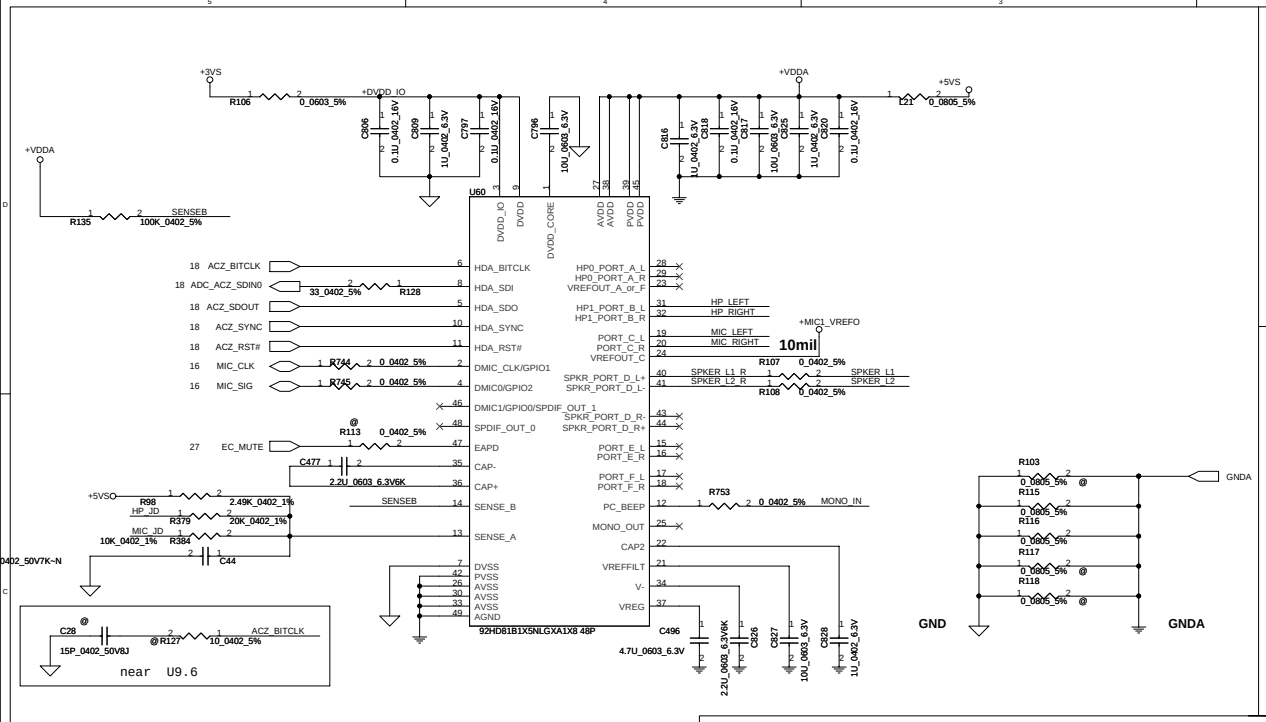

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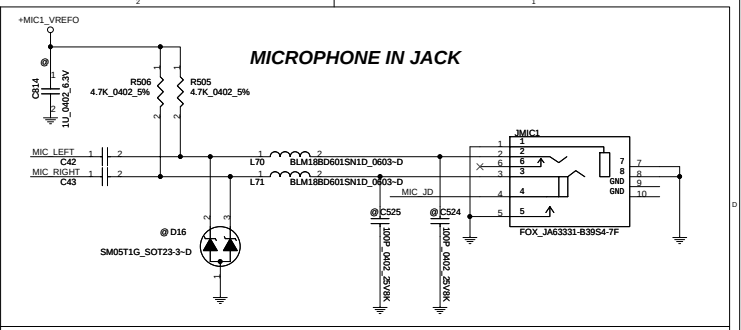

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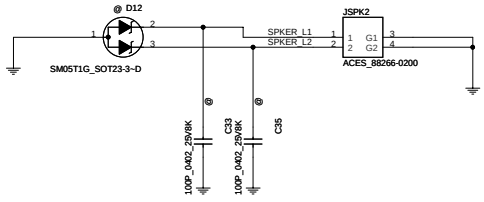

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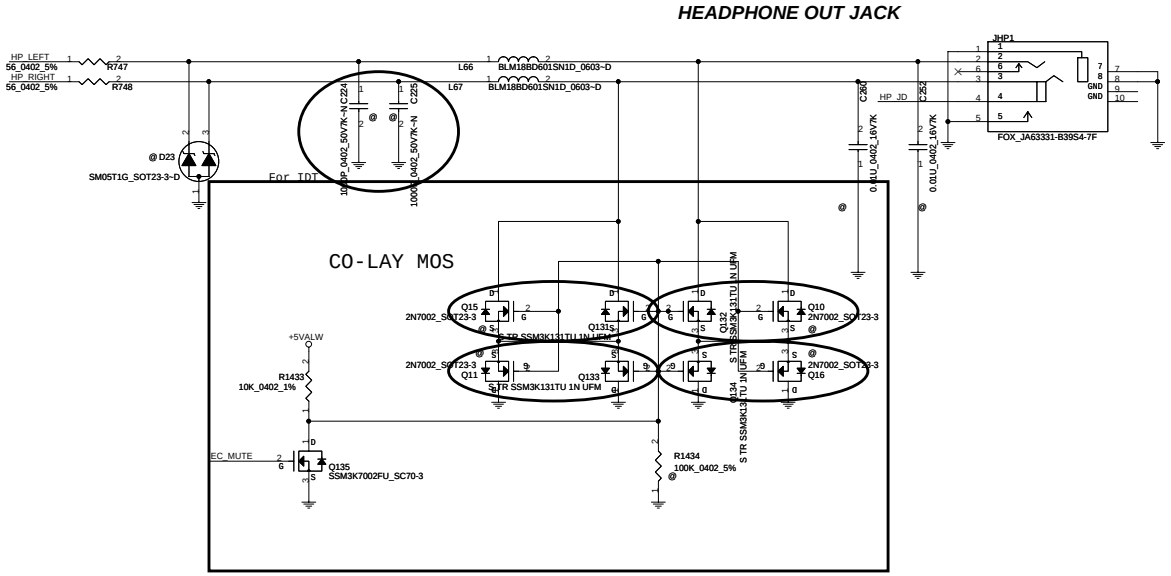

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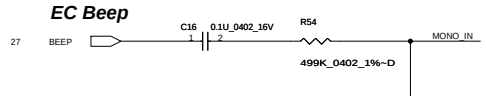

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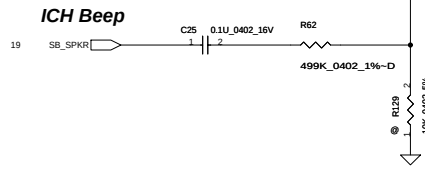

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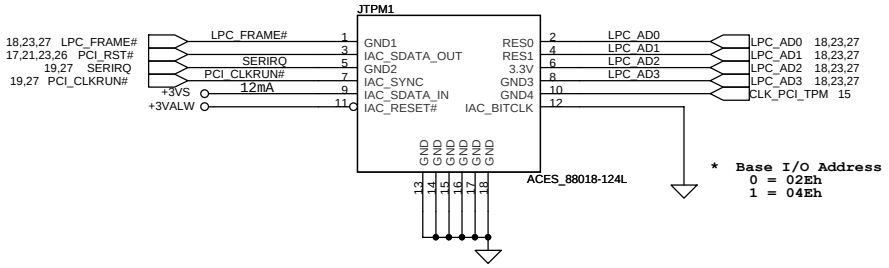
TPM 1.2

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*  Base I/O Address
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   1 = 04Eh
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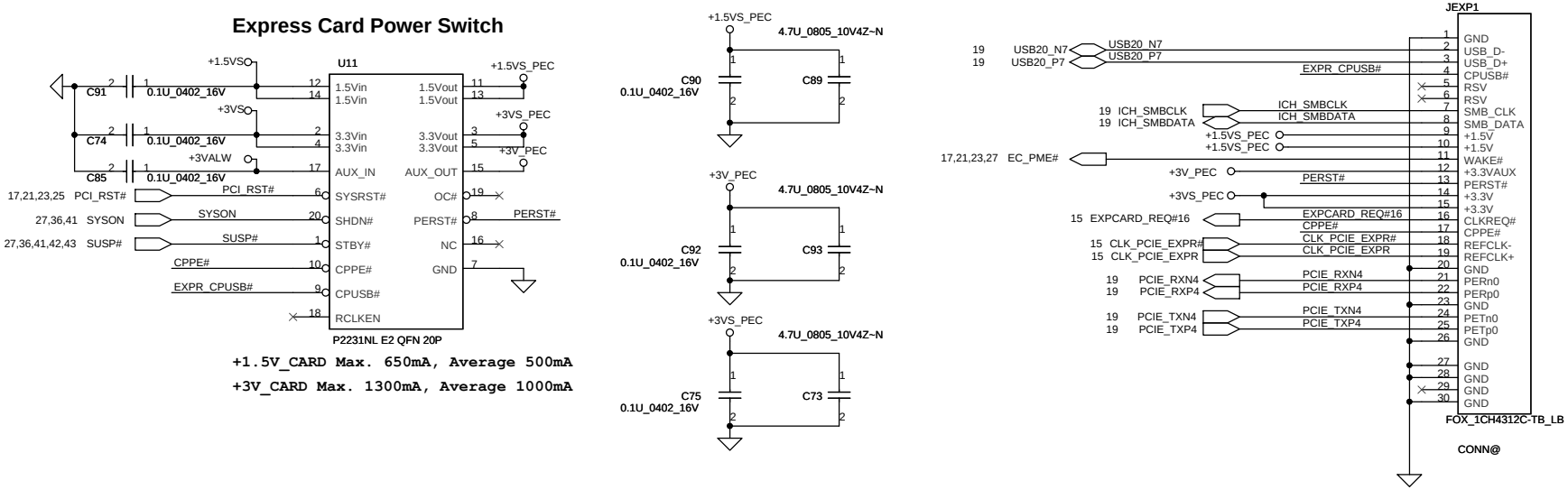
Express card



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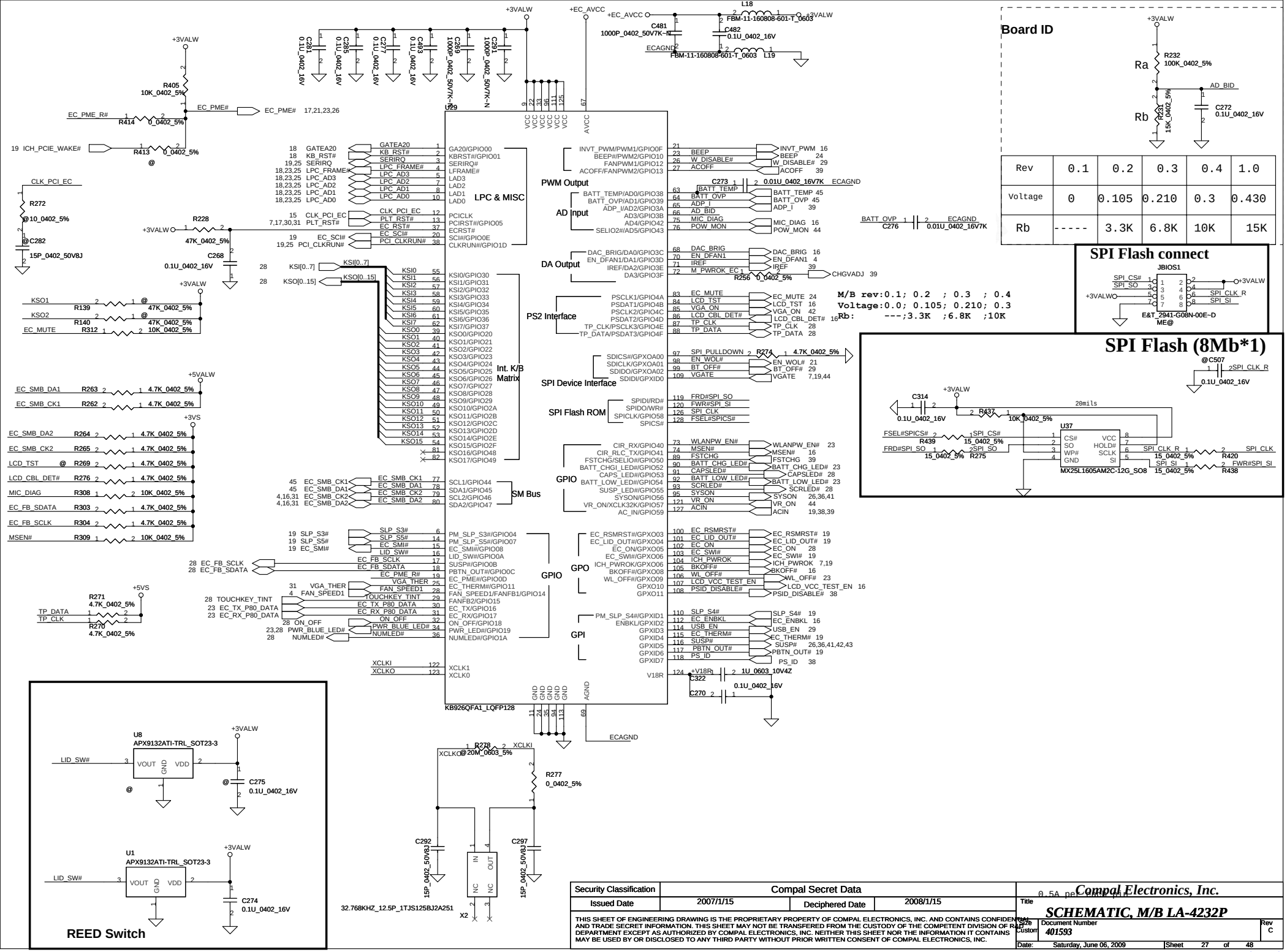

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0.5A per VRM Out

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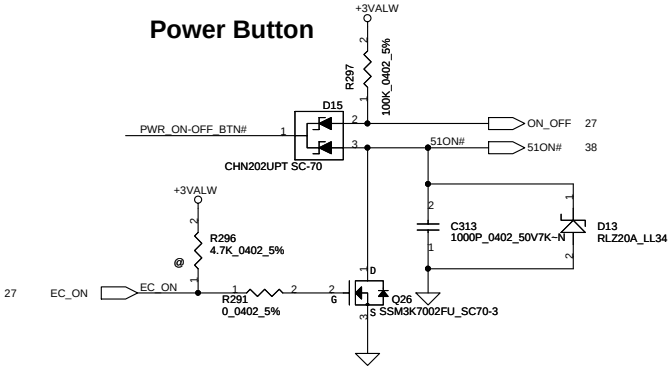
Power Button



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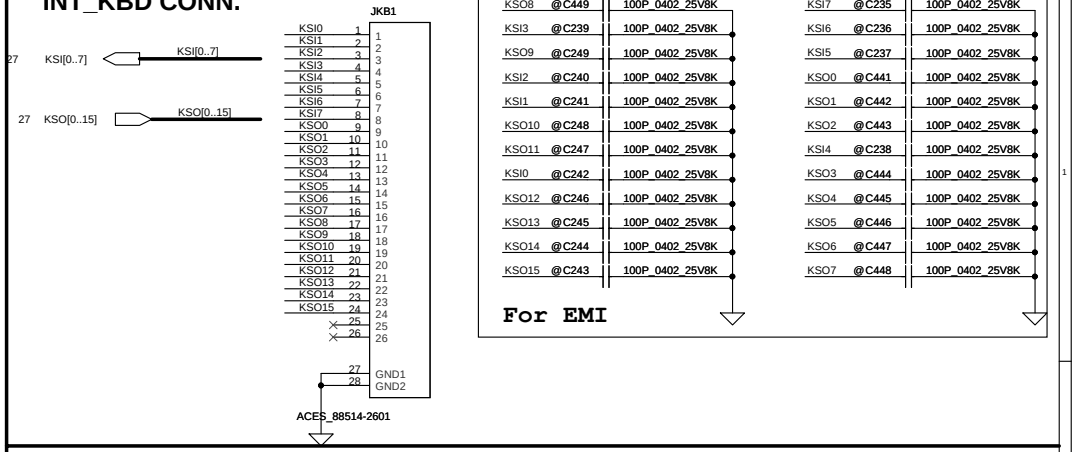

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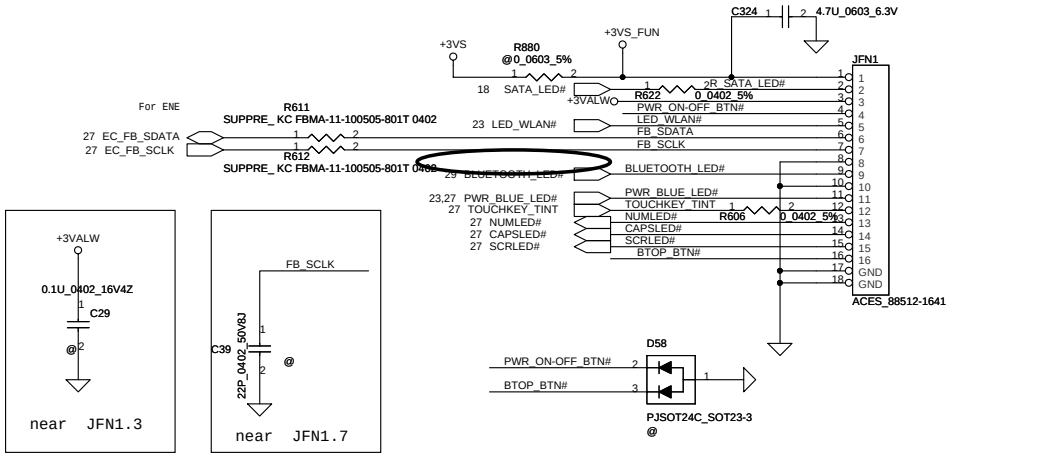

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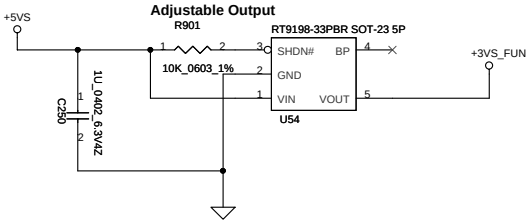

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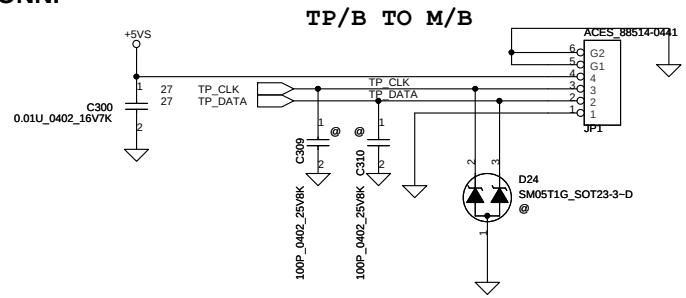

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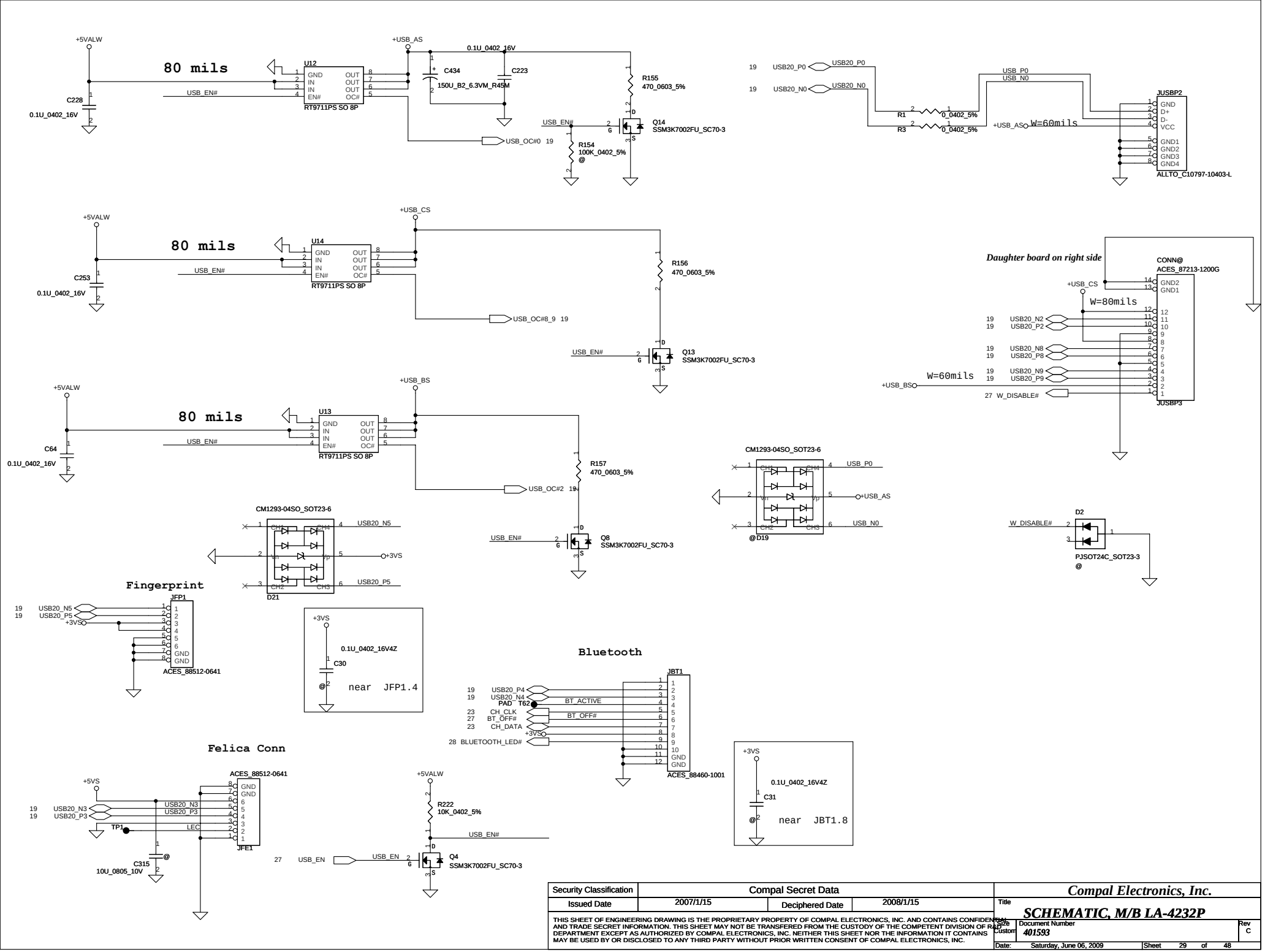

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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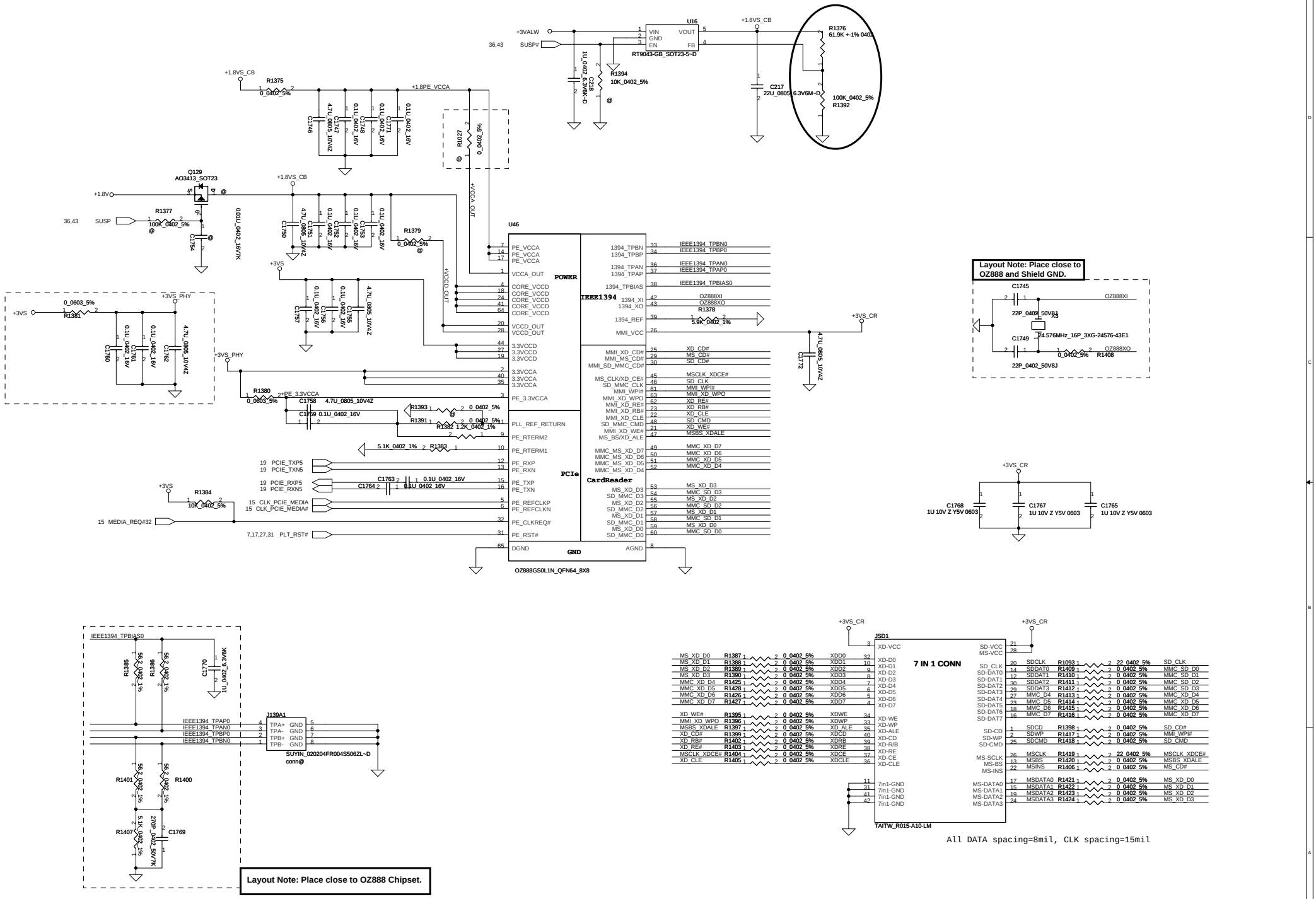

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Issued Date	2008/1/3	Deciphered Date	2009/01/3	Title: SCHEMATIC, M/B LA-4232P
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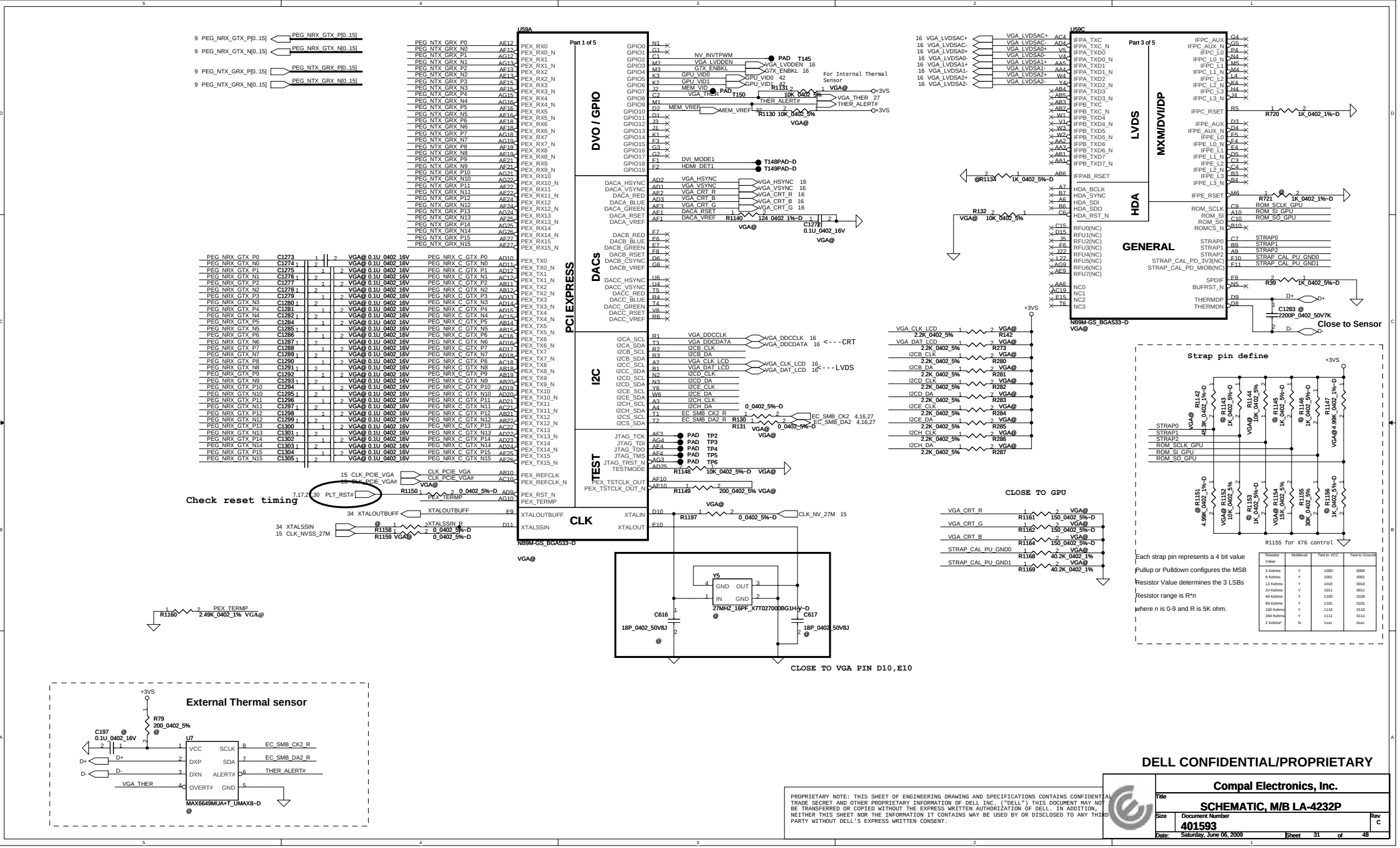

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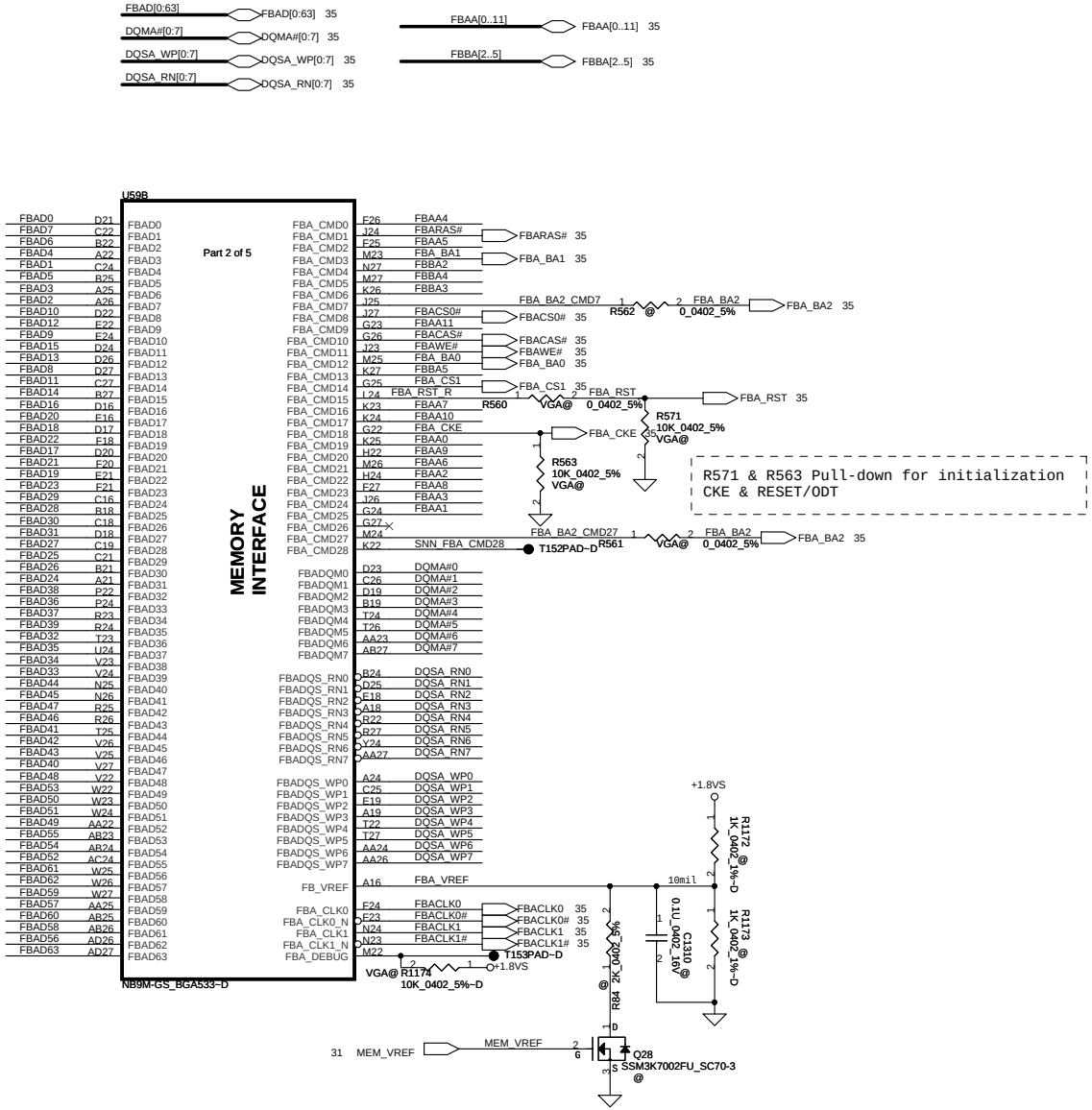

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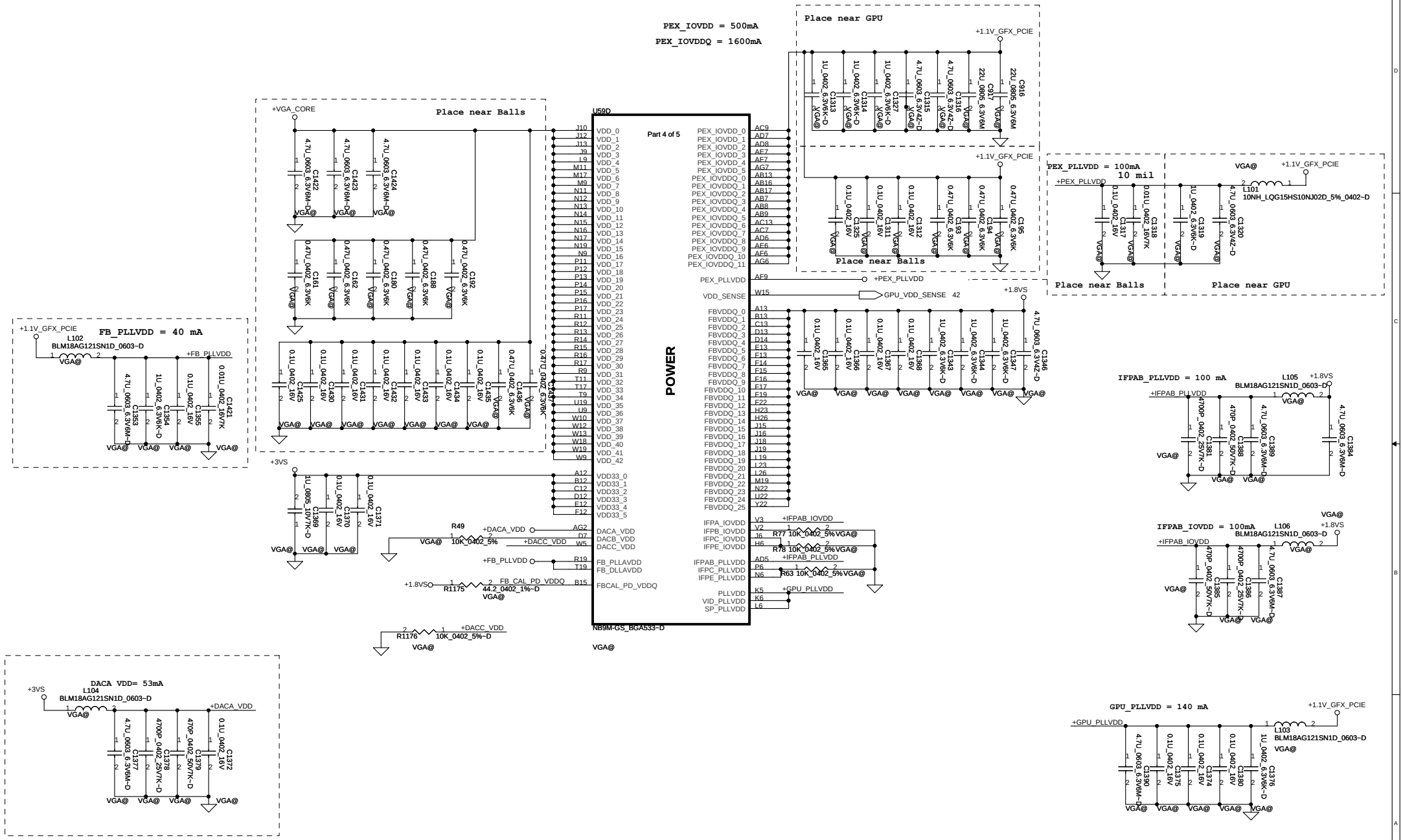

DELL CONFIDENTIAL/PROPRIETARY

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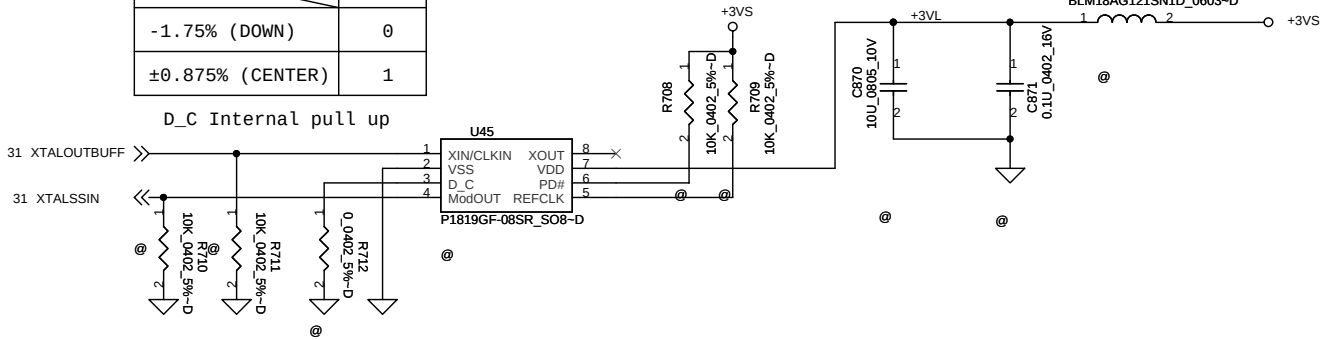
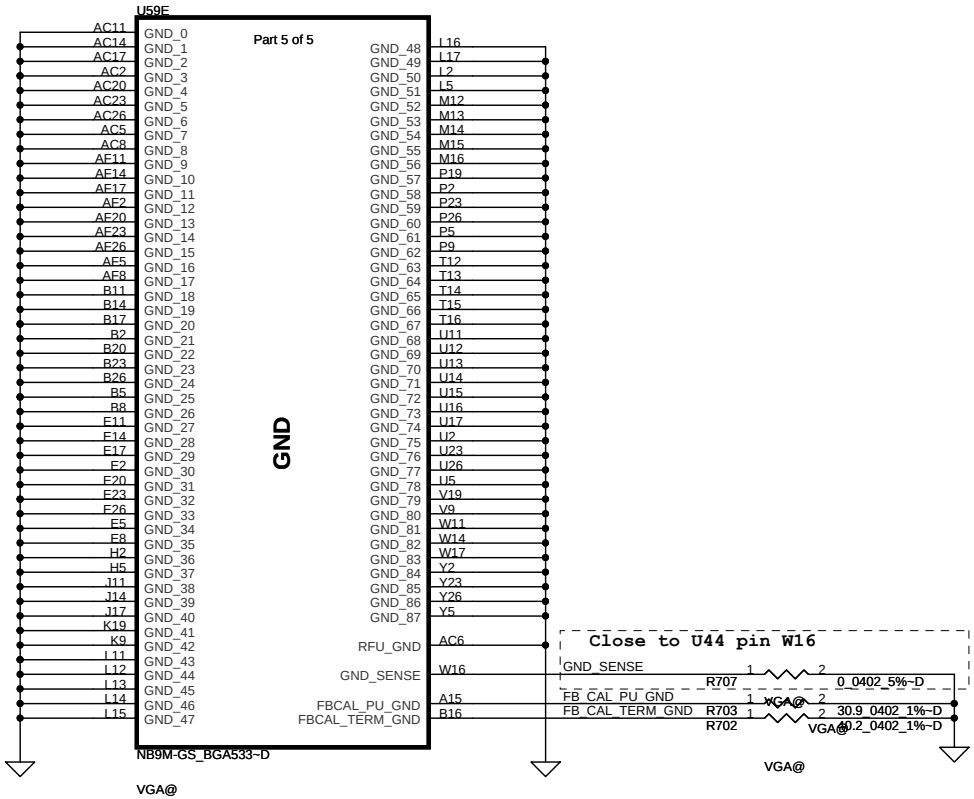
	D_C
-1.75% (DOWN)	0
±0.875% (CENTER)	1

D_C Internal pull up





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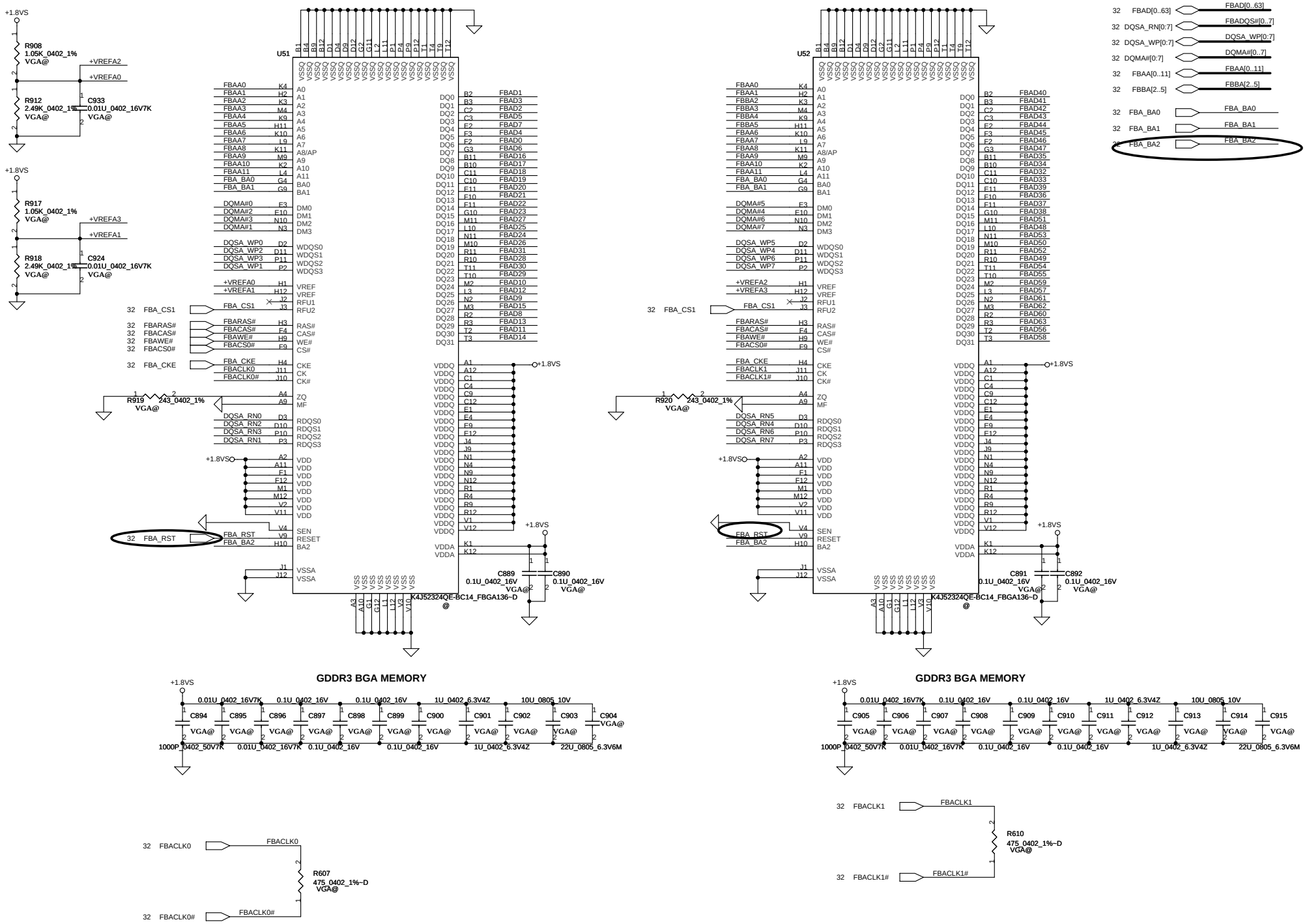

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Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-4232P

Size | Document Number: 401593 | Rev: C

Date: Saturday, June 06, 2009 | Sheet 35 of 48

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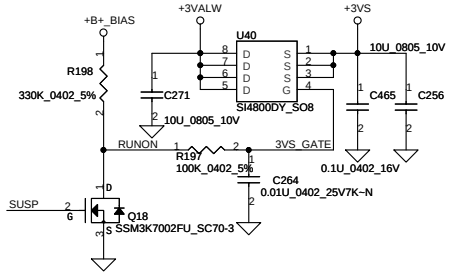
+3VALW to +3VS Transfer



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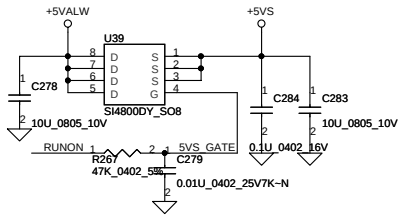

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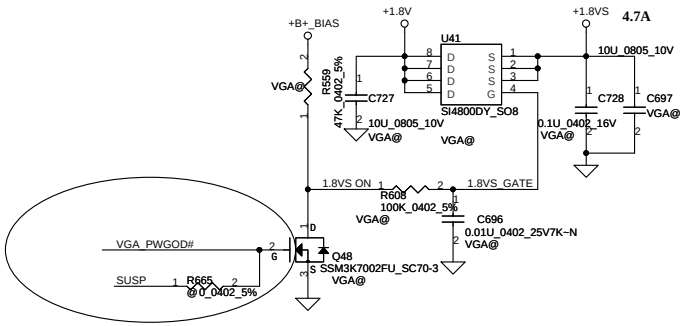
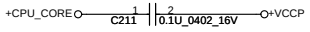
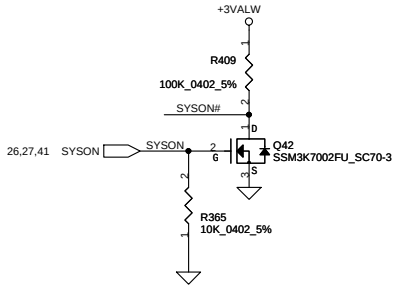
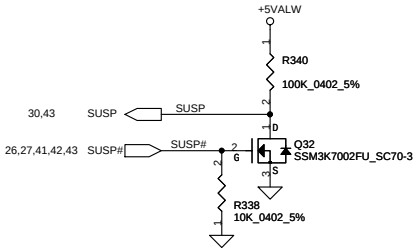
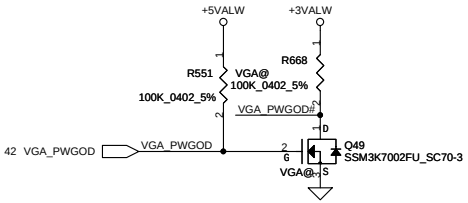




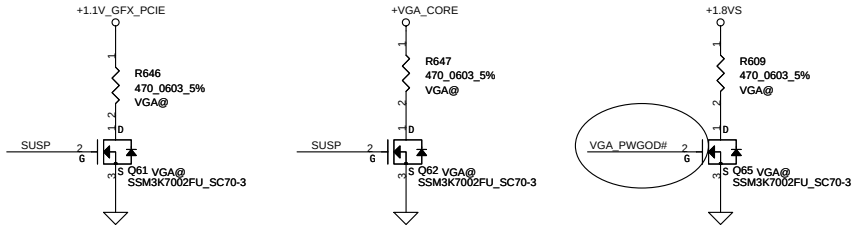




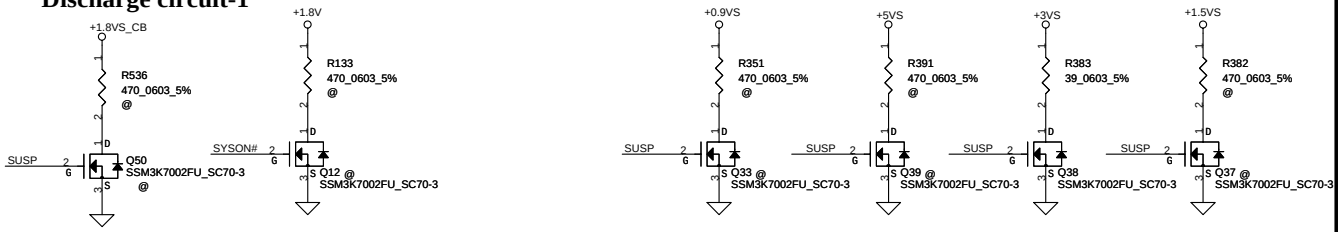


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit



Discharge circuit-1



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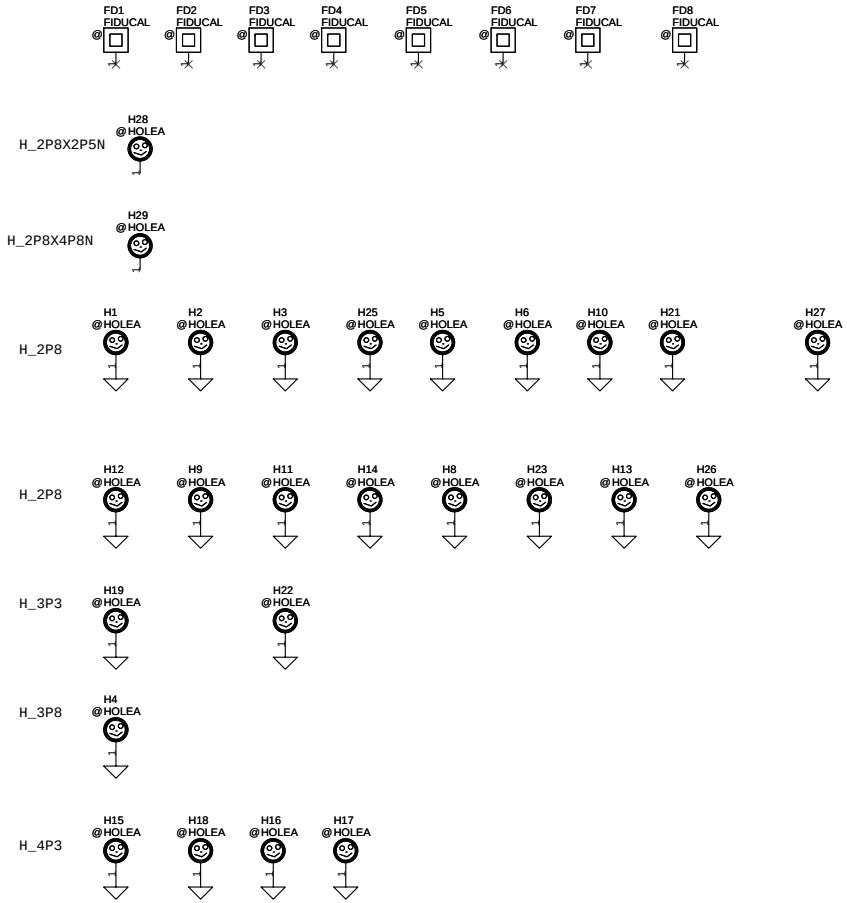

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Custom	401593	C

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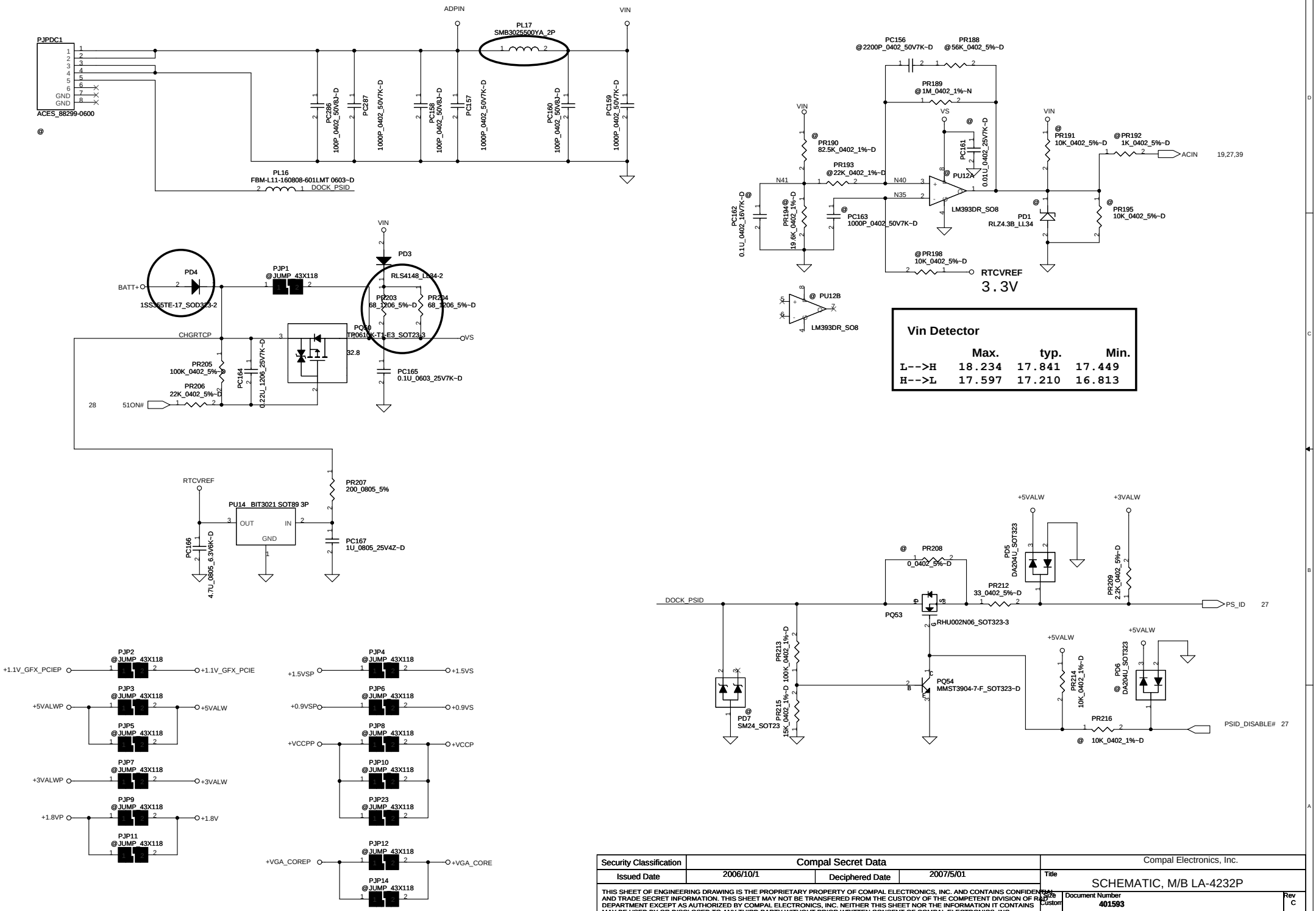

Vin Detector

	Max.	typ.	Min.
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H-->L	17.597	17.210	16.813

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Issued Date	2006/10/1	Deciphered Date	2007/5/01	Title: SCHEMATIC, M/B LA-4232P
				Size: Custom; Document Number: 401593; Rev: C
				Date: Saturday, June 06, 2009; Sheet 38 of 48

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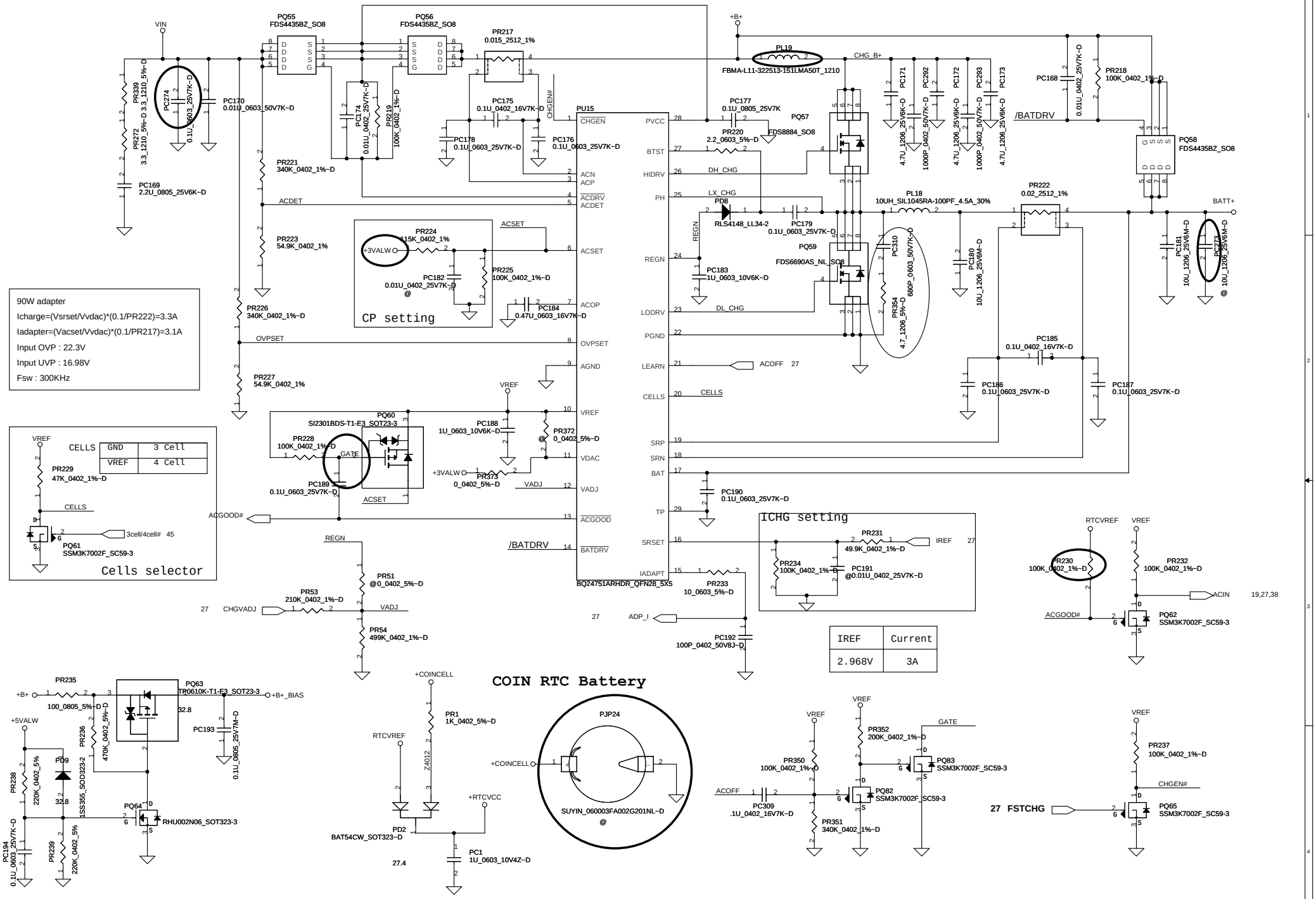

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Title: SCHEMATIC, M/B LA-4232P

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Date: Saturday, June 06, 2009 | Sheet 39 of 48

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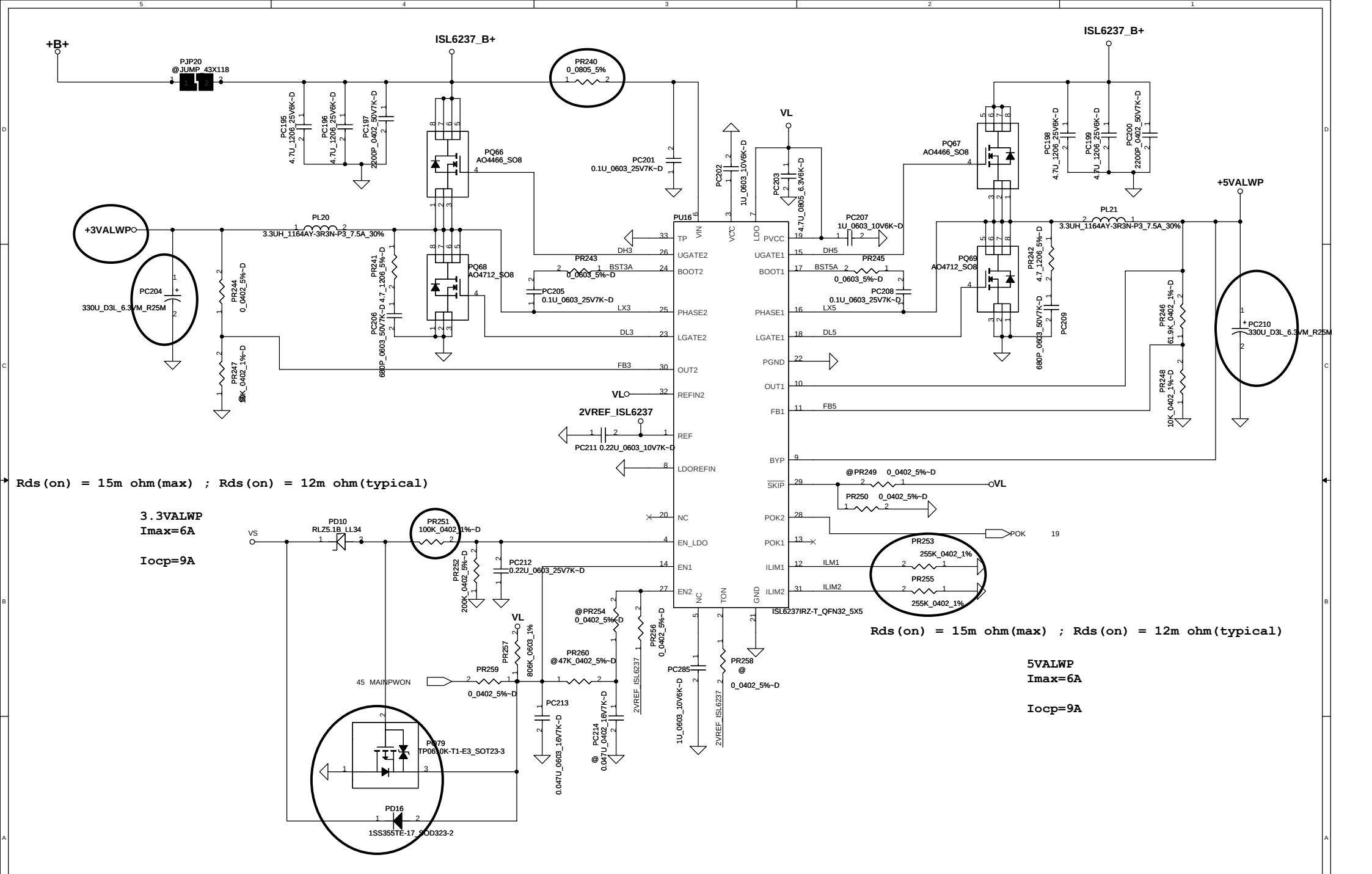

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Issued Date	2006/10/1	Deciphered Date	2007/05/30

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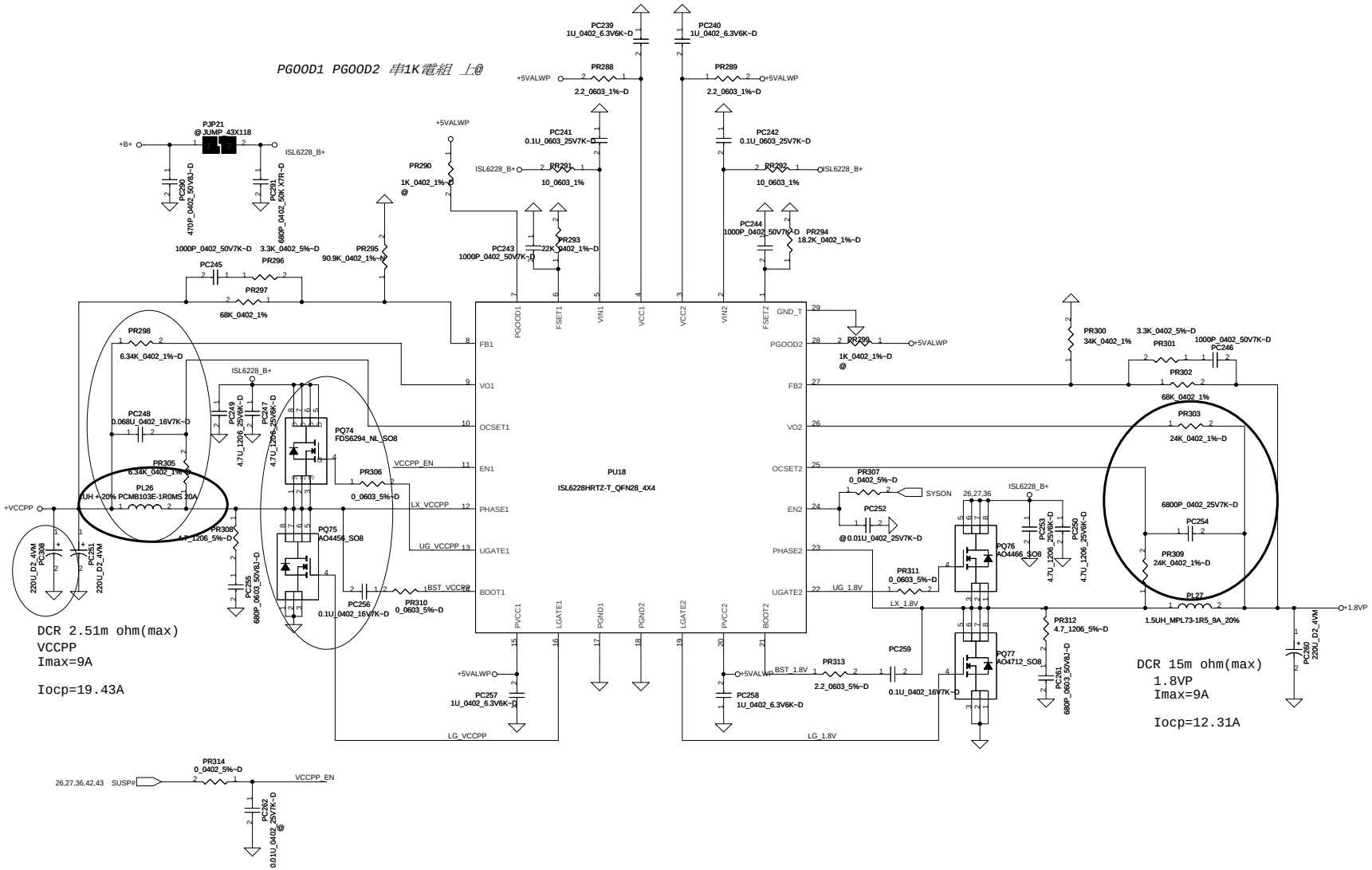

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	401593	C

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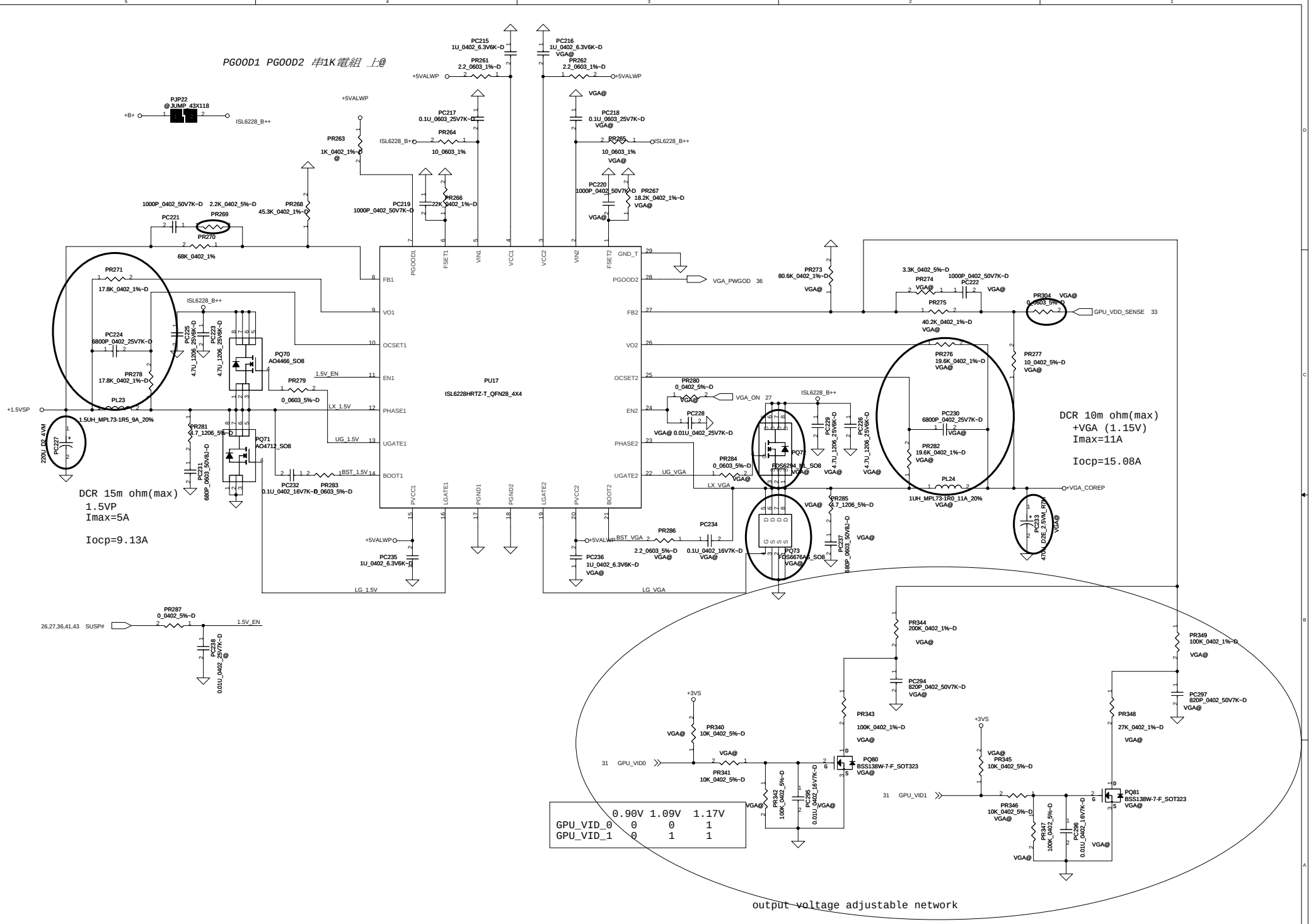

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GPU_VID_1	0	1	1

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Issued Date	2006/10/1	Deciphered Date	2007/5/01

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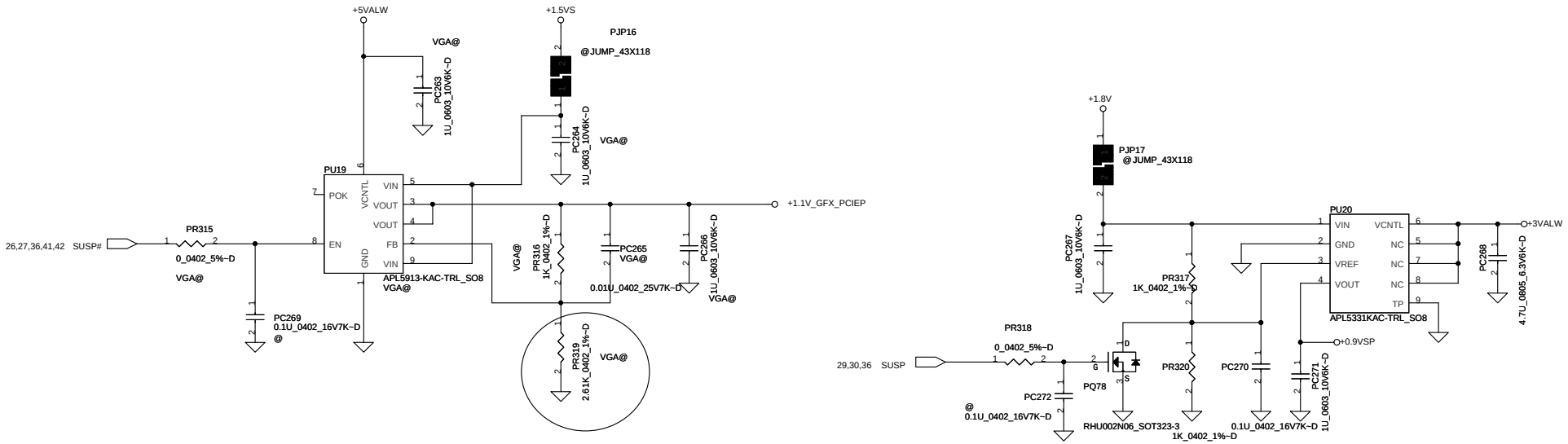

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Issued Date	2005/10/1	Deciphered Date	2007/05/30	Title: SCHEMATIC, M/B LA-4232P
				Size: Custom; Document Number: 401593; Rev: C
				Date: Saturday, June 06, 2009; Sheet 43 of 48

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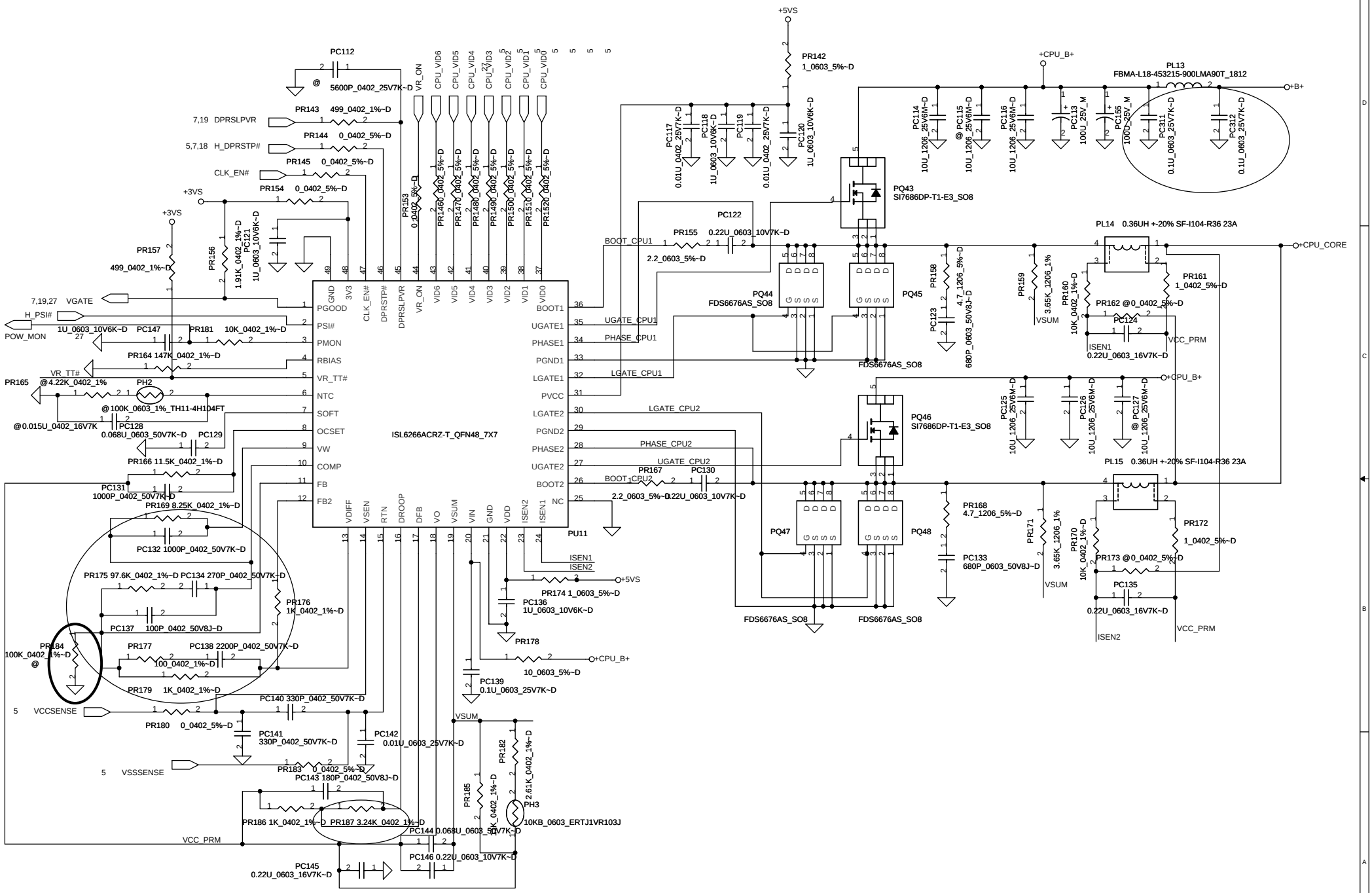

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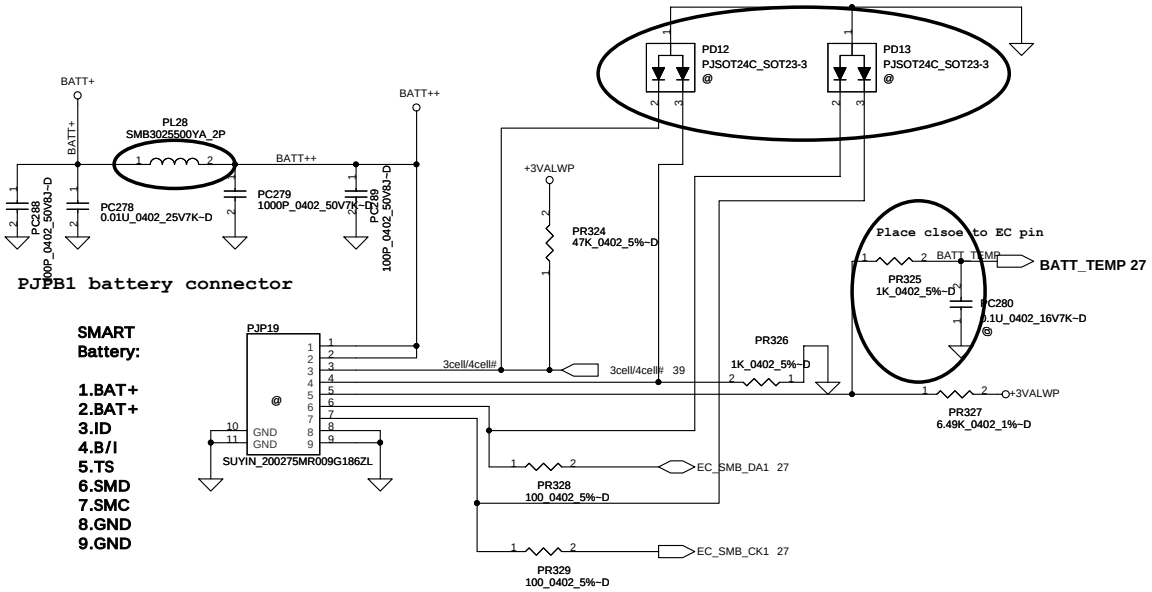
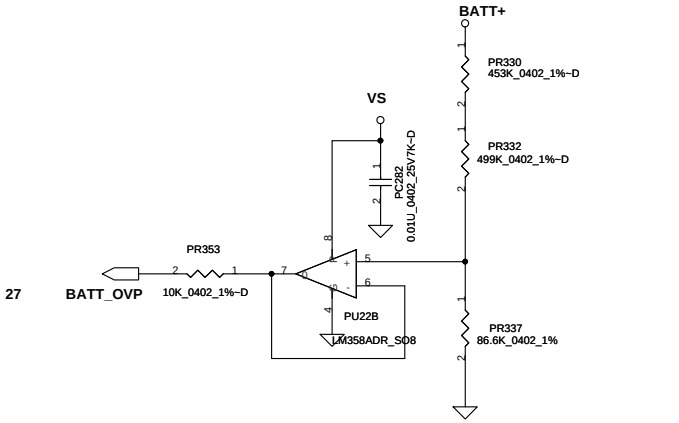
Battery Connect/OTP

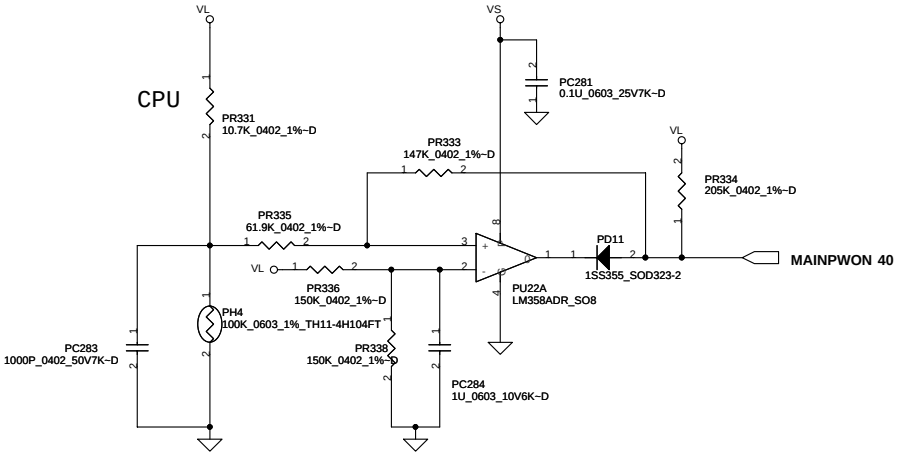


CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-OZ129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to OZ129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Frequence Decoupling Capacitance	C195 change to C1150~C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
18	20	P20-ICH9(4/4)_POWER&GND	08/04/22	compal	+5VS & +3VS have leakage	Change VCCCL3[1] [2] & VCCLAN3_3[1] [2] power source to +LAN_IO	
19	20	P09-Cantiga(3/6)-VGA/LVDS/TV	08/04/22	compal	Can't boot to OS	Add BOM Structure @	
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Version Change List (P. I. R. List) Page 1/1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	1.8VP/+VCCPP	08/10/22	COMPAL	adjust +VCCP OCP set	Change PC248 from 0.033u to 0.068u	0.2
2	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	ripple voltage fail	Change PC227 from SF22001M300 to SGA20221150	0.2
3	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	convenient test	Add PR304	0.2
4	44	CPU_CORE	08/10/22	COMPAL	load line fail	Change PR187 from 2.21K to 3.24K	0.2
5	38	DCIN / Precharge	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
6	39	Charger	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
7	40	+3VALWP/+5VALWP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
8	41	1.8VP/+VCCPP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
9	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
10	43	+0.9VSP/+1.1V_GFX_PCIEP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
11	44	CPU_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
12	45	BATTERY CONN	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
13	40	+3VALWP/+5VALWP	08/10/24	COMPAL	boost choke current rating	change PL20 PL21 from SH000006380 to SH00000AY00	0.2
14	45	BATTERY CONN	08/10/30	COMPAL	delete diode for EMD request	del PD14 PD15	0.2
15	45	BATTERY CONN	08/10/30	COMPAL	change diode for EMD request	change PD12 PD13 from SC1A204U00L to SCA00000E00	0.2
16	39	Charger	08/10/31	COMPAL	design modify	add PR372 PR373	0.2
17	41	1.8VP/+VCCPP	08/11/03	COMPAL	dynamic fail	change PC233 from SGA20221150 to SGA00001U80	0.2
18	44	CPU_CORE	08/12/08	COMPAL	cost down	change PU11 from SA00001HU80 to SA000031W00 and interrelated components	0.3
19	38	DCIN / Precharge	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
20	39	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
21	38	DCIN / Precharge	08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
22	45	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
23	39	Charger	08/12/15	COMPAL	change component for EMD request	change PJP15 to PL19 SM010016410	0.3
24	39	Charger	08/12/15	COMPAL	add capacitor for EMD request	add PC274 0.1u	0.3
25	42	1.5VSP/+VGA_CORE	09/01/19	COMPAL	adjust VGA_CORE OCP set	change PQ72 from SB00000CG00 to SB562940080	0.4
26						change PQ73 from SB00000AJ00 to SB000003W00	0.4
27						change PL24 from SH000008700 to SH000005400	0.4
28						change PR276 PR282 from 24K to 19.6K	0.4
29						change PC230 from 0.022u to 6800p	0.4
30					consumption adjust	change PR269 from 3.3K to 2.2K	0.4
31	44	CPU_CORE	09/01/19	COMPAL	vendor FAE suggest	add PC141 330p	0.4
32	45	BATTERY CONN	09/02/18	COMPAL	delete diode for ESD request	del PD12 PD13	0.4

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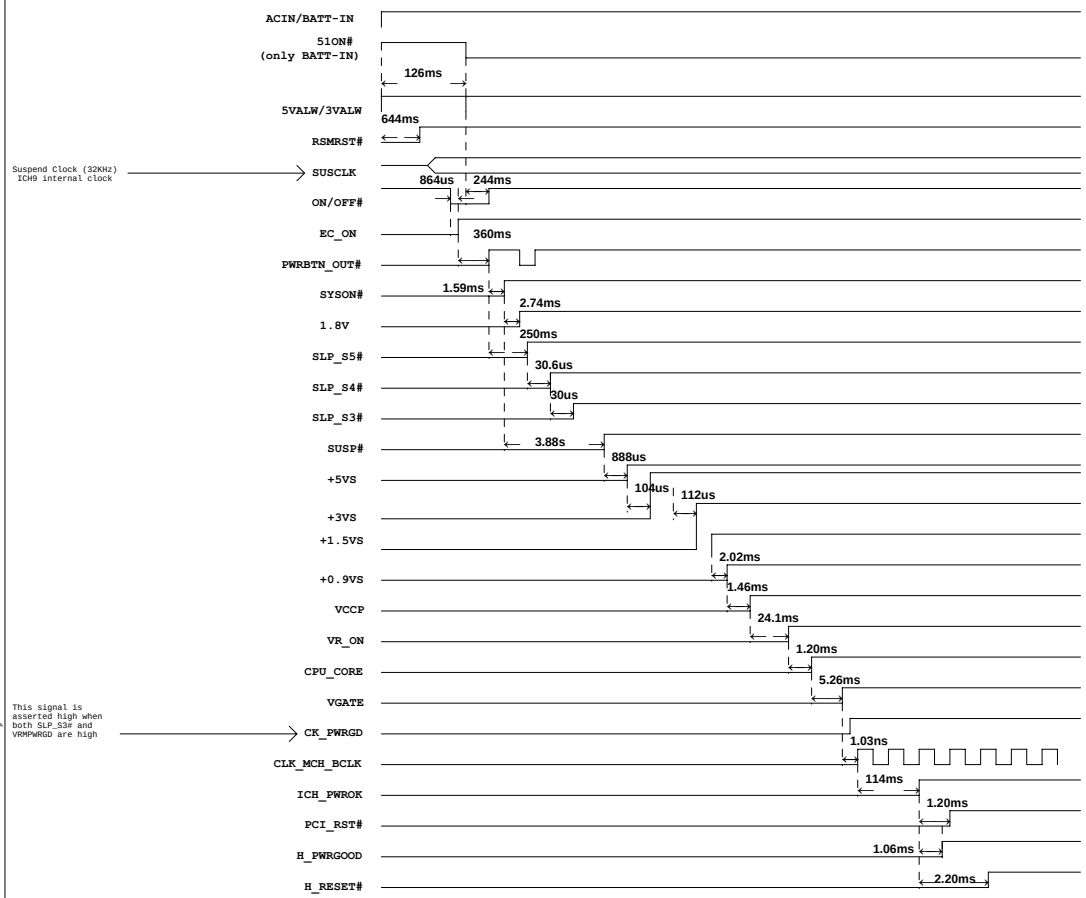
KAL80 POWER UP SEQUENCE



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