

COMPAL CONFIDENTIAL

MODEL NAME : QAL81
PCB NO : LA-7782P (DAA00002J00)
BOM P/N : TBD
GPIO MAP: E4_VC_GPIO_map_rev_0.8

Dalmore 14 DSC

Ivy Bridge + Panther POINT

2011-05-12
REV : 0.1 (X00)
@ : Nopop Component
CONN@ : Connector Component

MB Type		BOM P/N	
TPM		1@	3@
TCM		2@	4@
TPM DIS/TCM DIS		2@	3@

MB PCB	
Part Number	Description
DAA00002J00	PCB 0LE LA-7782P REV0 M/B DSC

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Title

Cover Sheet

Size

Document Number

LA-7782

Rev

0.1

Date

Tuesday, May 24, 2011

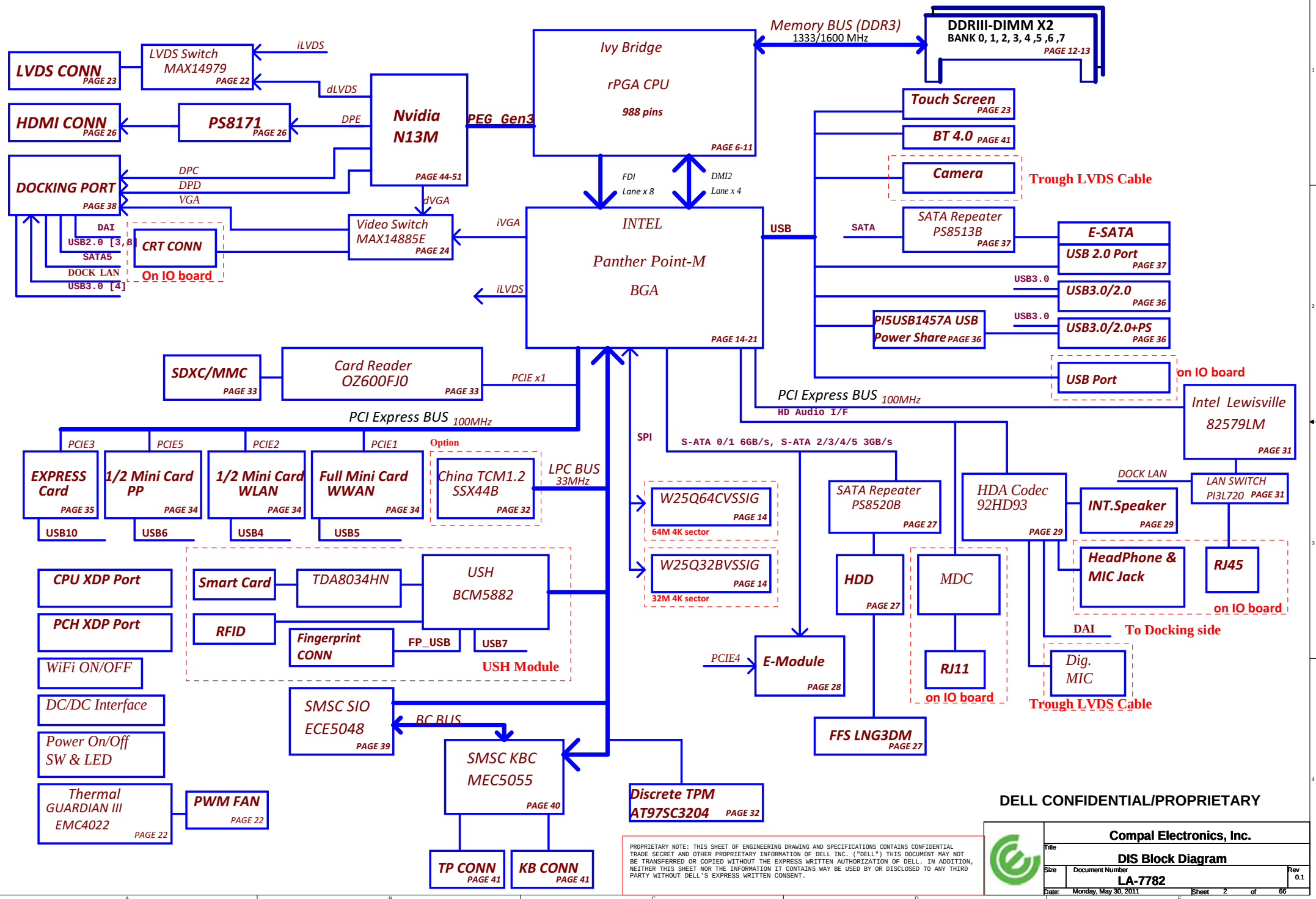
Sheet

1

of

66

Block Diagram *Compal confidential*



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

need to update Power Status and PM Table

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side Top)
	1	JUSB2 (Right side Bottom)
	2	JESA1 (Right side ESATA)
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(Flash)
	7	USH->BIO
	8	DOCKING
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

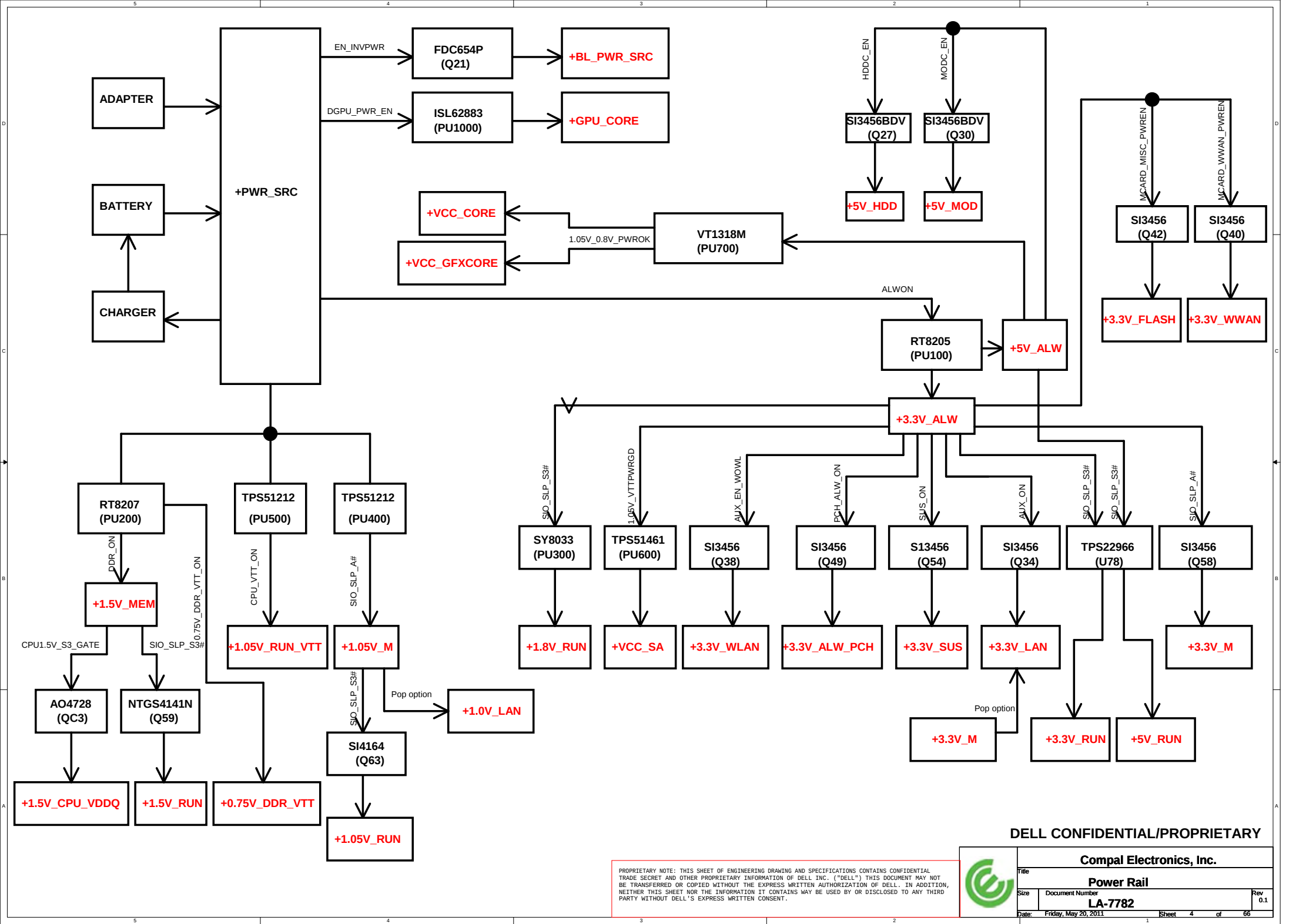
Layer No.	Name	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	min 0.4	0.50000
		Add Plating		1.45000
1	Top	Copper foil	0.5oz(0.68)	0.65000
		Prepreg	1080	2.75000
2	GND1	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
3	IN 1	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
4	GND2	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
5	IN 2	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506*2	11.50000
6	IN 3	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
7	VCC	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
8	IN 4	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
9	GND 3	Copper foil	1oz(1.35)	1.30000
		Prepreg	1080	2.75000
10	Bottom	Copper foil	0.5oz(0.68)	0.65000
		Add Plating		1.45000
		SolderMask	min 0.4	0.50000
	Overall Thickness (1.45mm ± 10%)			57.91000

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

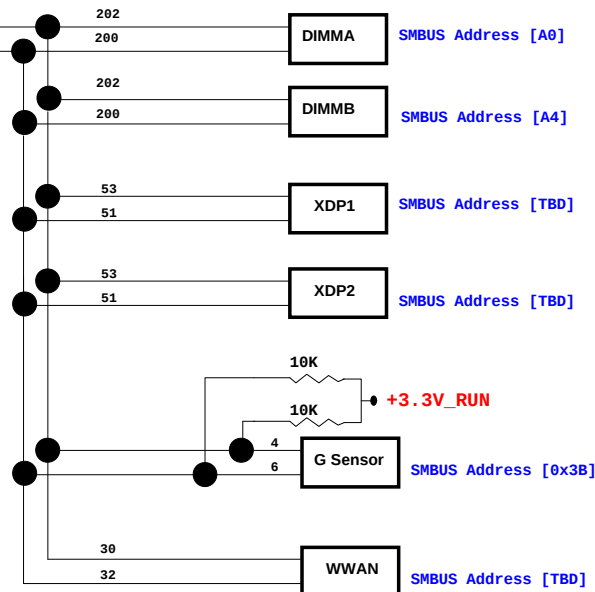
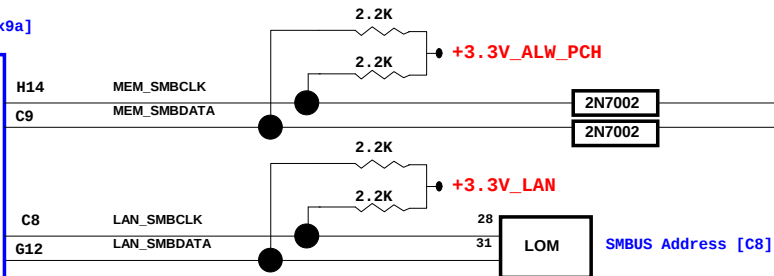
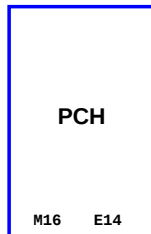
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Index and Config.			
Size	Document Number	Rev	
	LA-7782	0.1	
Date:	Friday, May 20, 2011	Sheet	3 of 66

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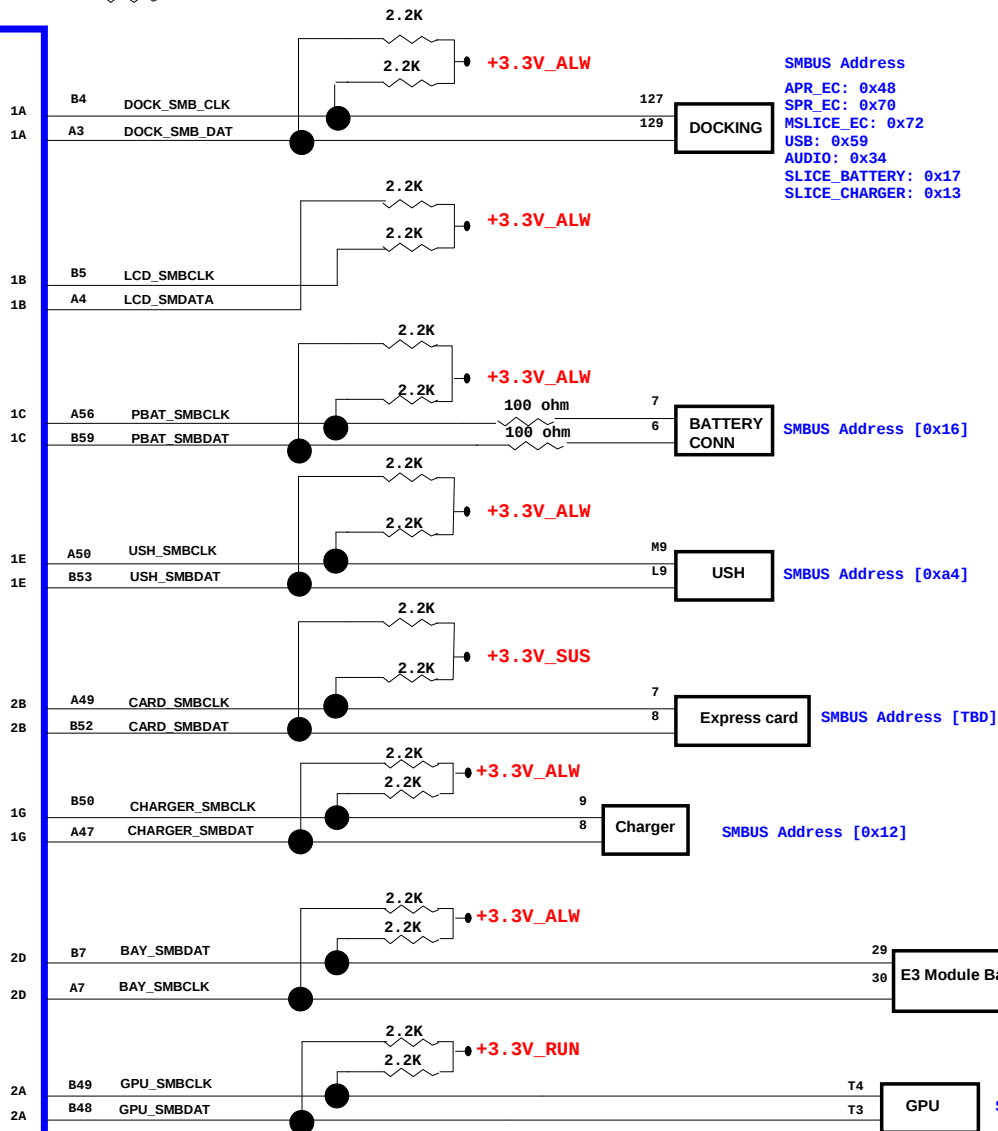


SMBUS Address [0x9a]

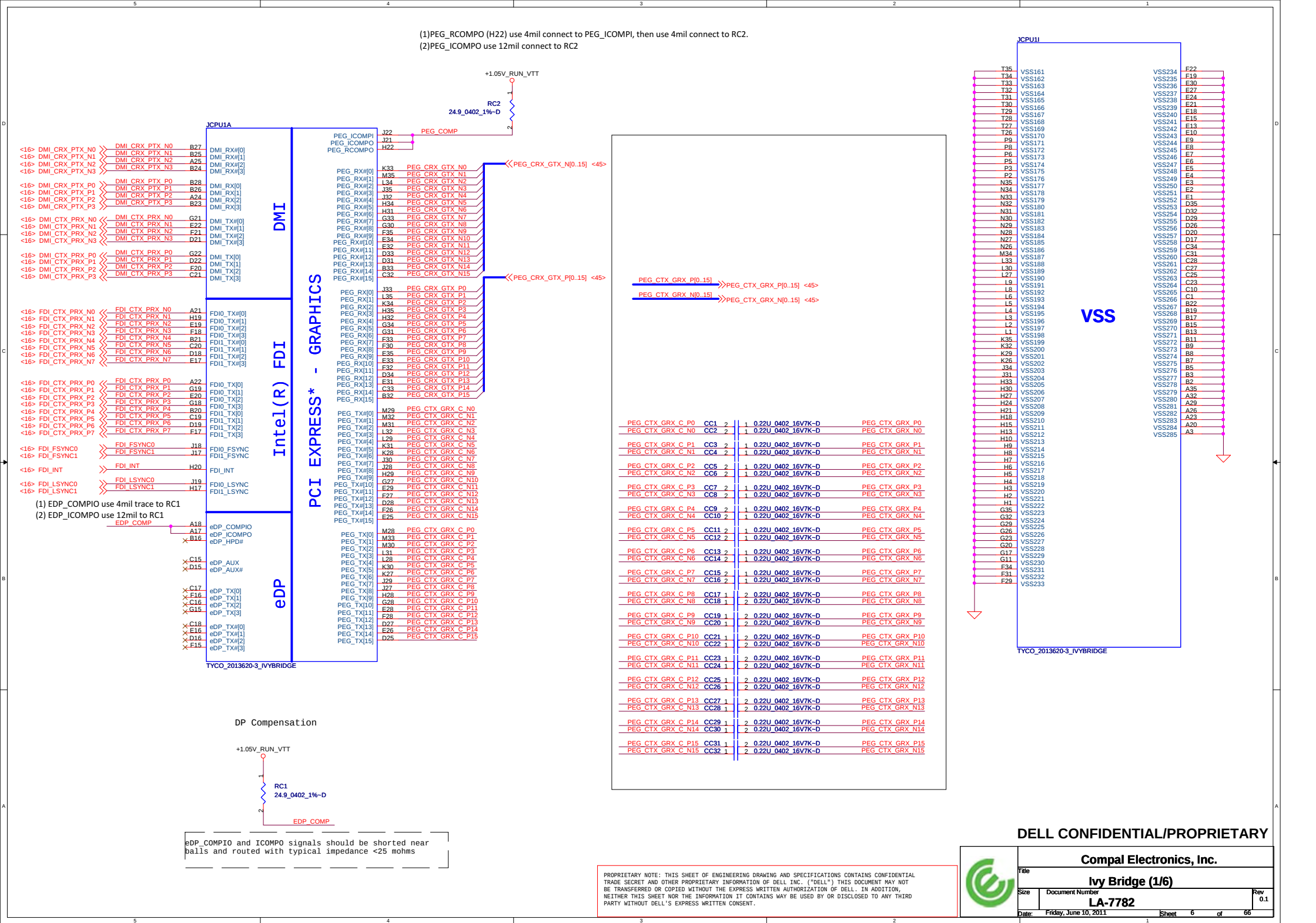


SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

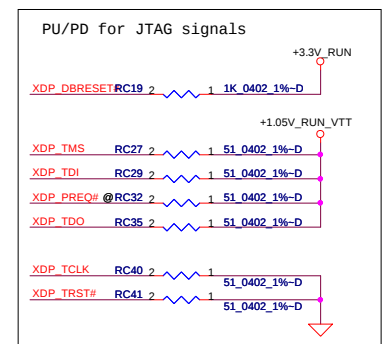
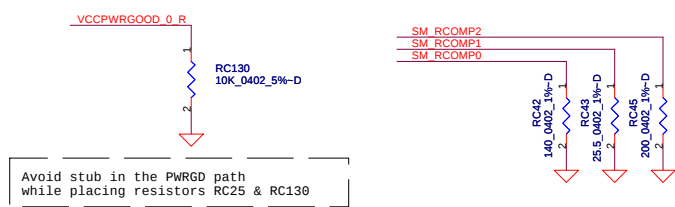
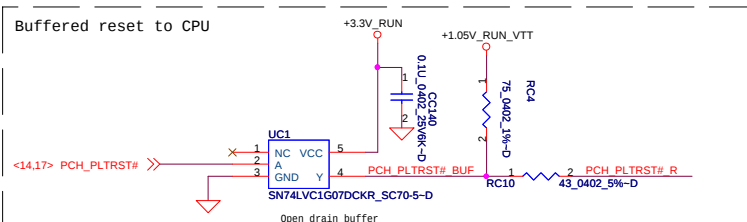
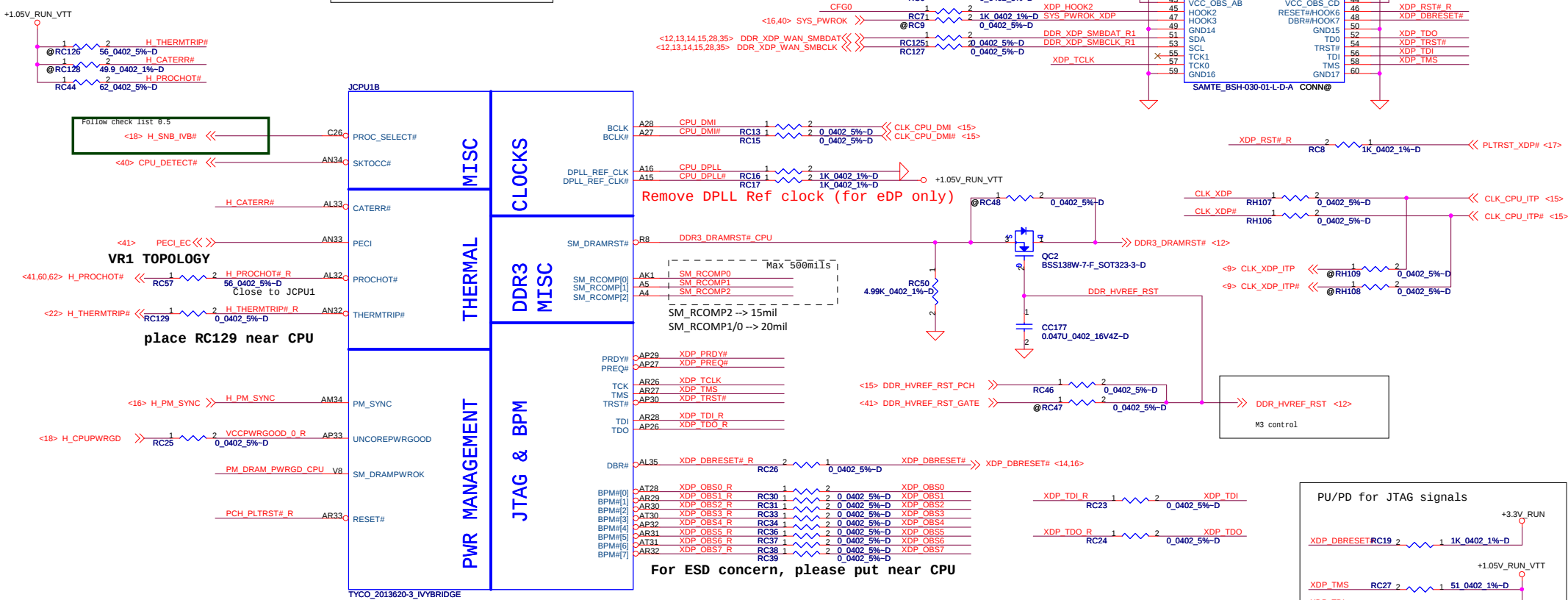
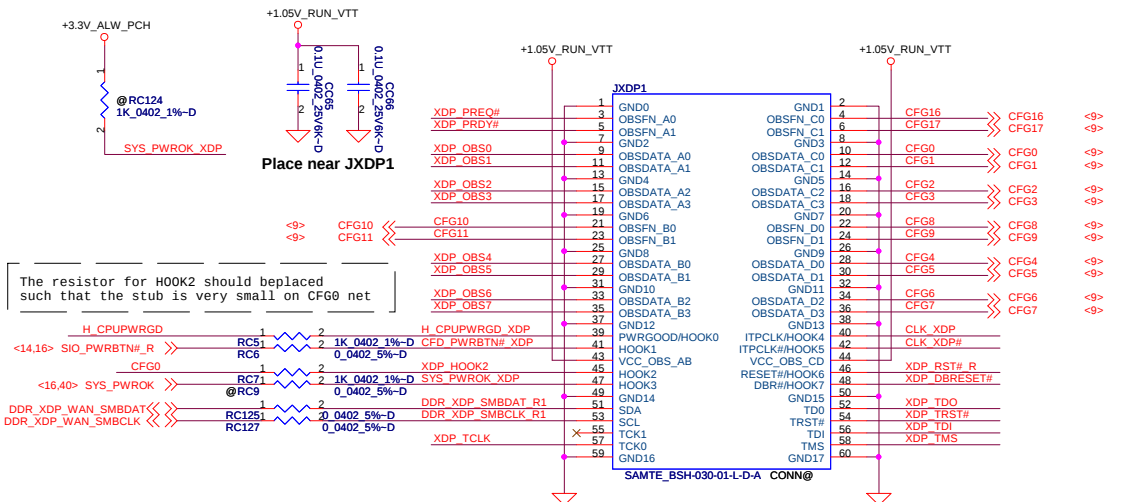
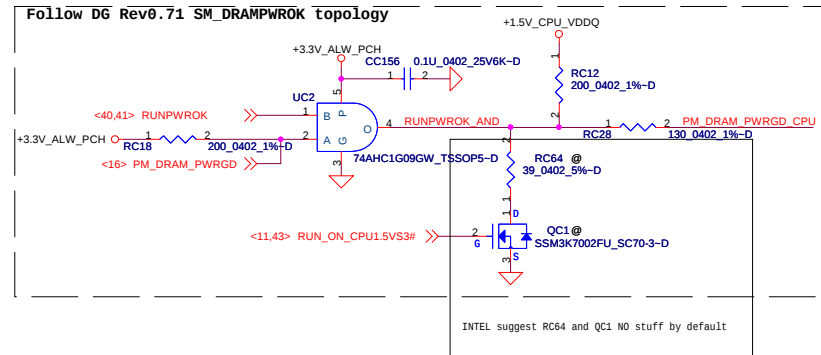
KBC



MEC 5065



Follow DG Rev0.71 SM_DRAMPWROK topology



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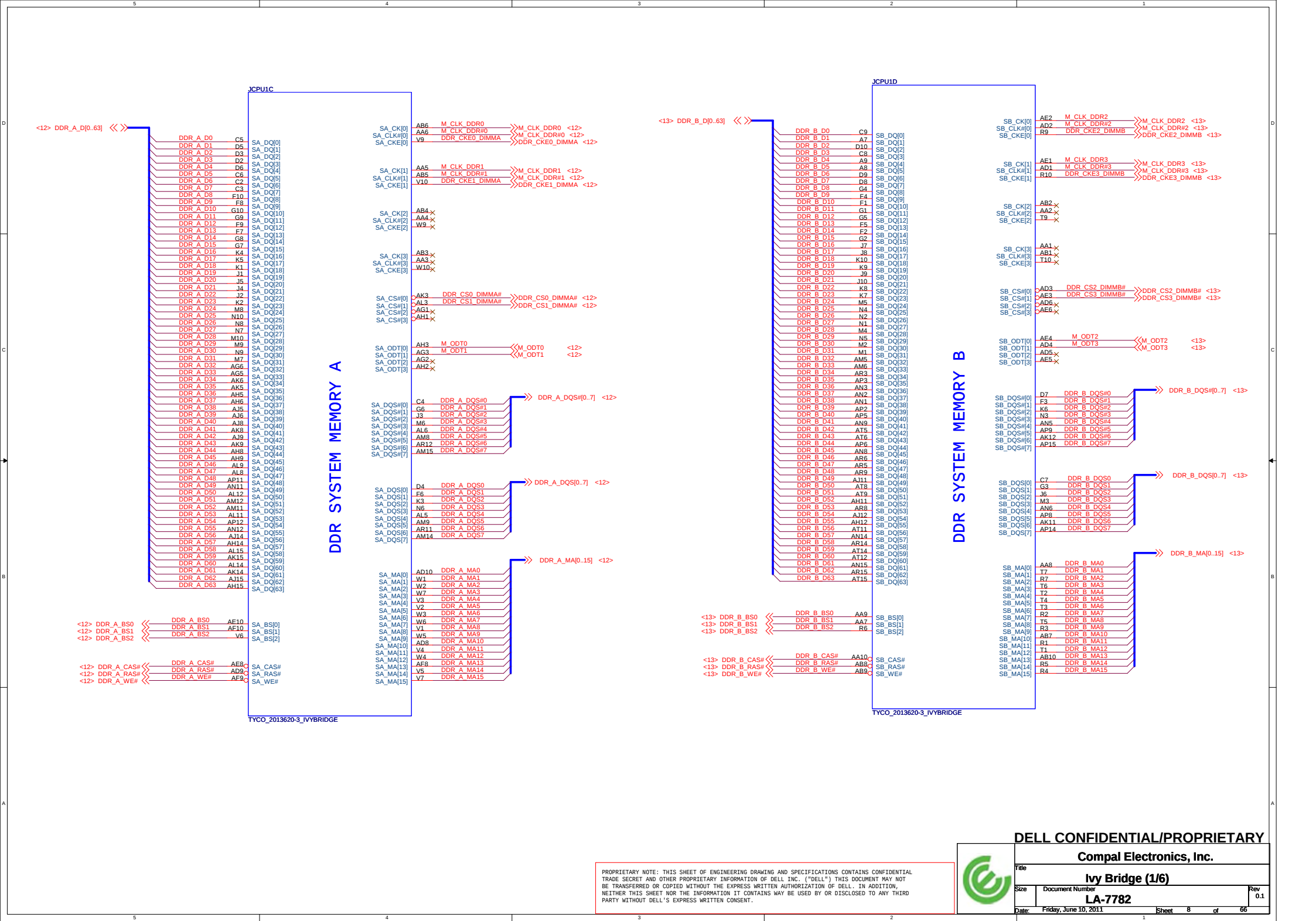
Ivy Bridge (1/6)

LA-7782

Rev

Date: Friday, June 10, 2011 Sheet 7 of 66

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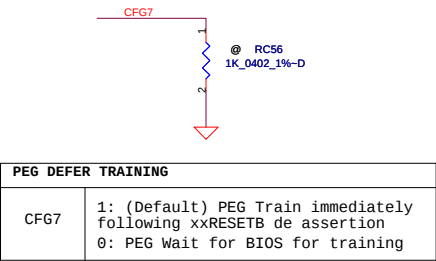
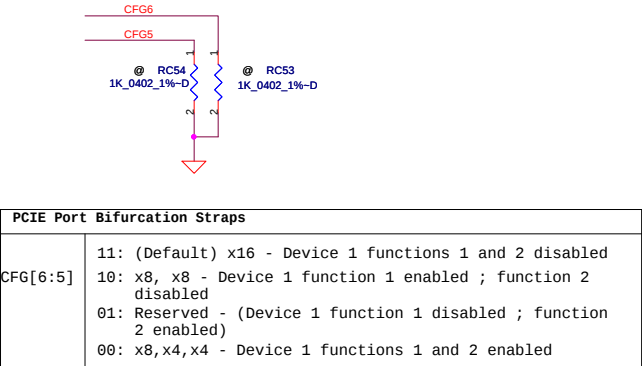
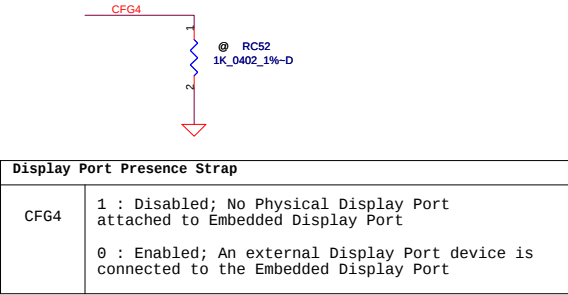
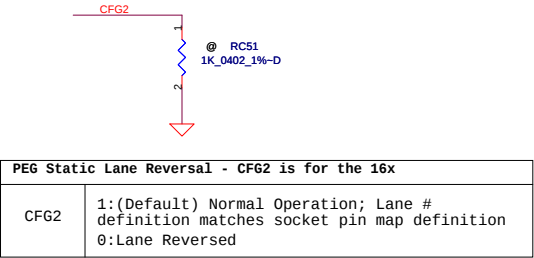
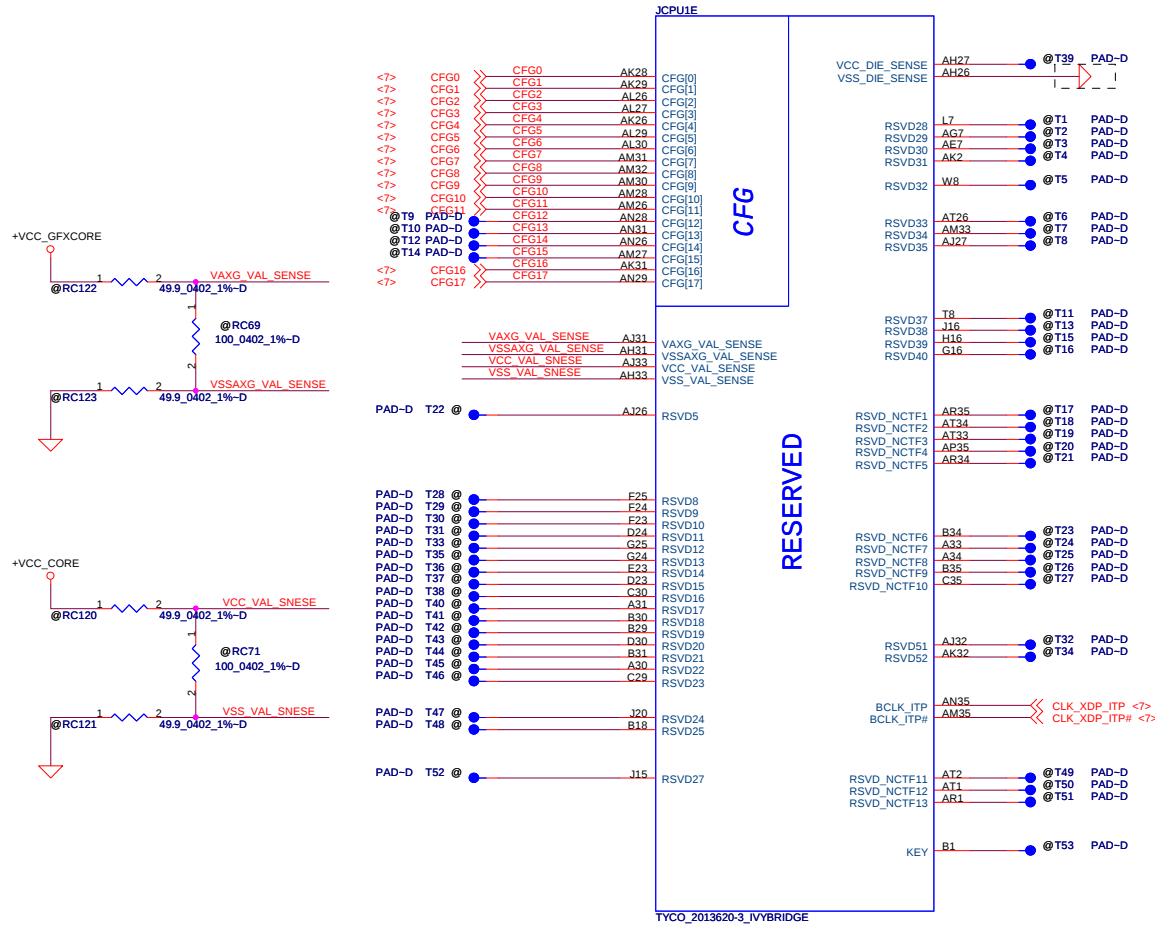


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Title			
Ivy Bridge (1/6)			
Size	Document Number	Rev	
	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	8 of 66

CFG Straps for Processor



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JCPU1F



5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_BUN & +0.75V_DDR_VTT

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JDIMM1 H=5.2

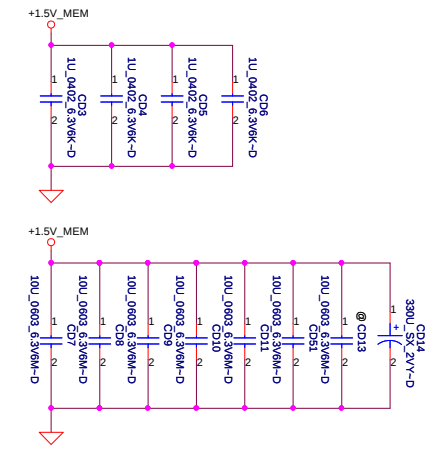
2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

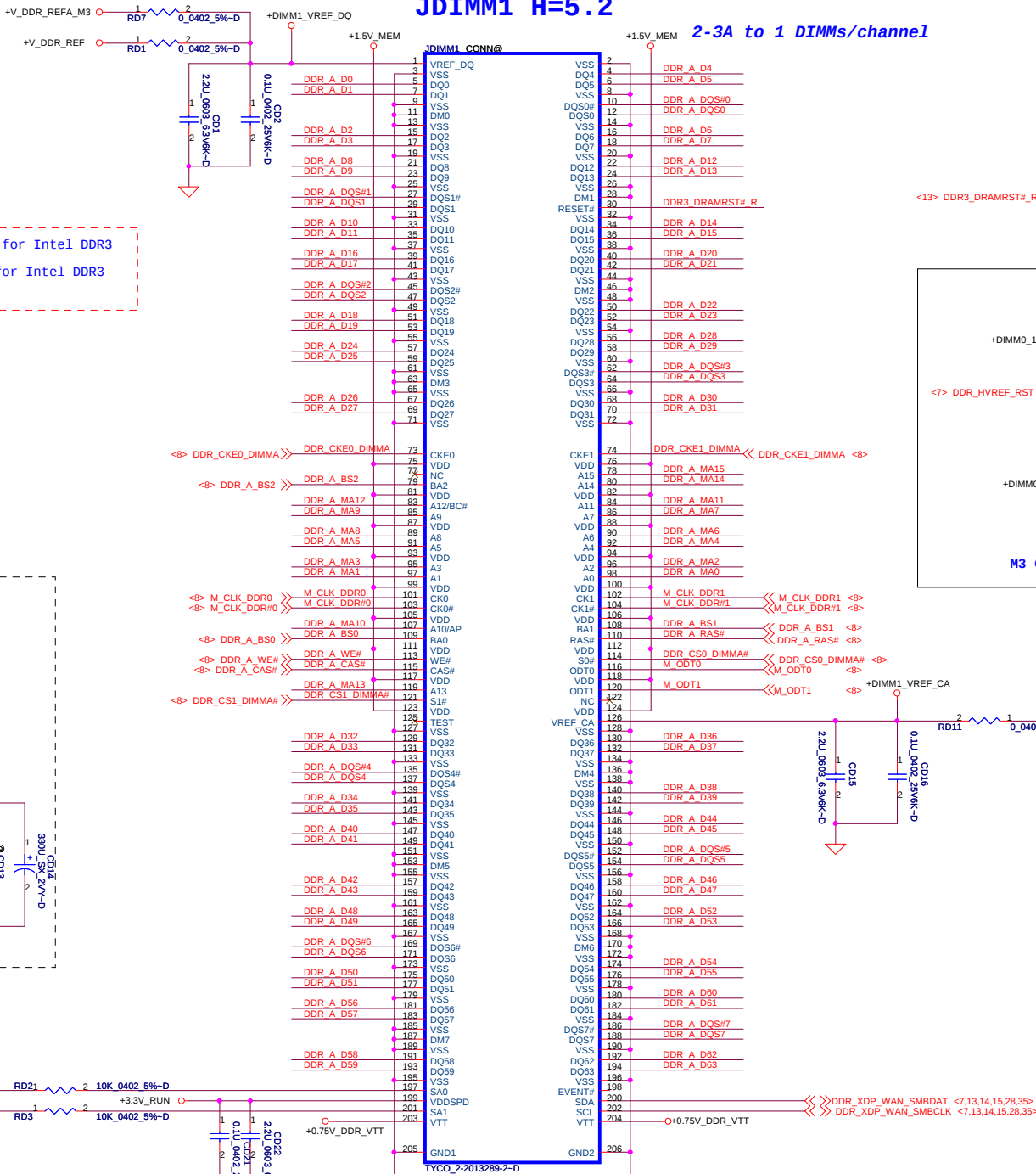
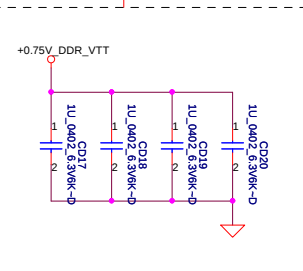
All VREF traces should have 10 mill trace width

 DDR_A_DQS#[0..7] <<>>
 DDR_A_D#[0..63] <<>>
 DDR_A_DQS#[0..7] <<>>
 DDR_A_MA#[0..15] <<>>

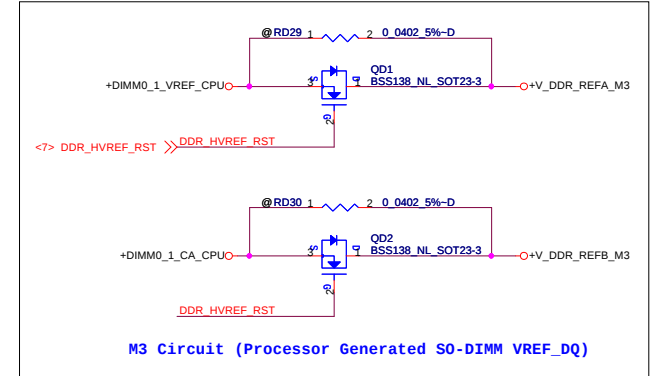
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



<13> DDR3_DRAMRST#_R <<DDR3_DRAMRST#_R 1 2 0.0402 5%-D >> DDR3_DRAMRST# <<7>



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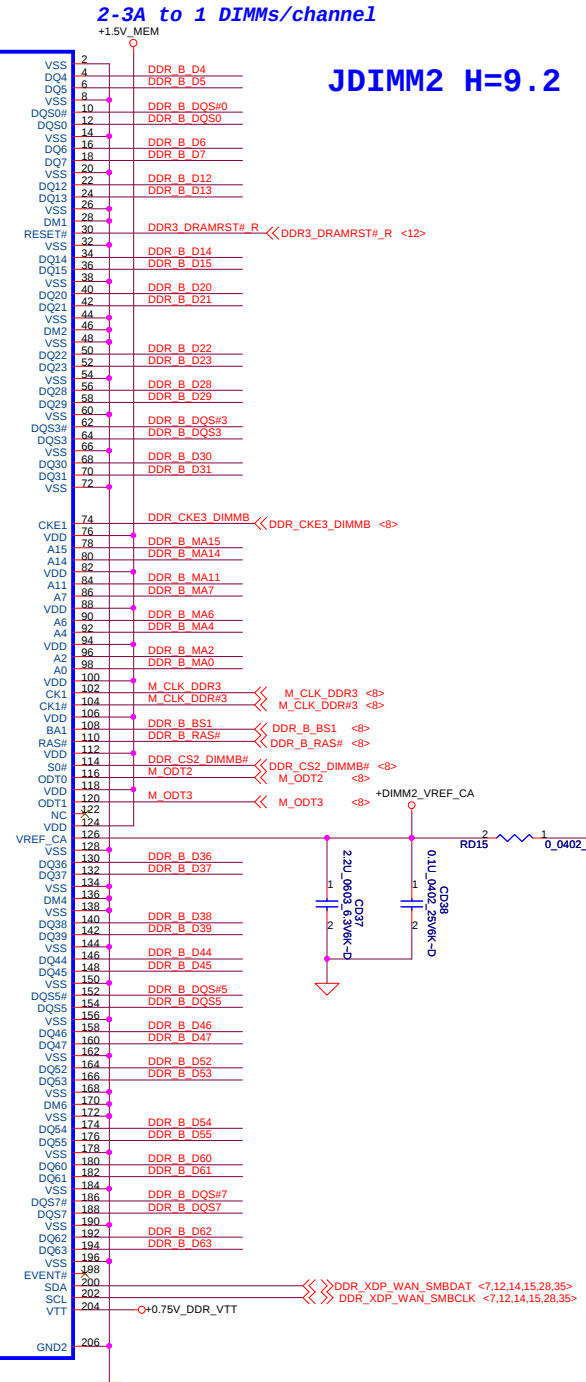
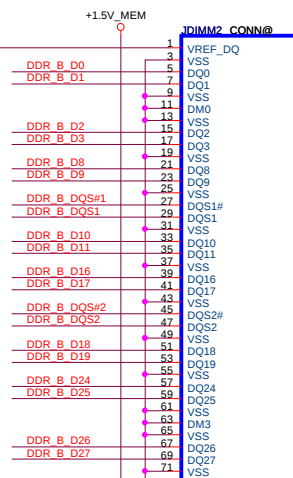
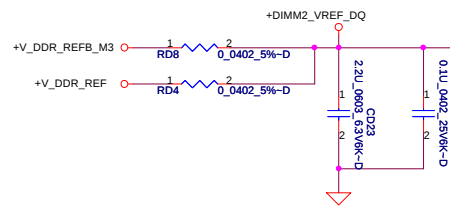
DDRIII-SODIMM SLOT1

LA-7782

Rev 0.1

Date: Friday, June 10, 2011 Sheet 12 of 66

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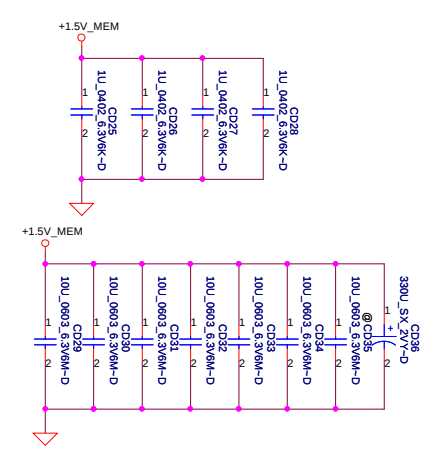
JDIMM2 H=9.2

Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

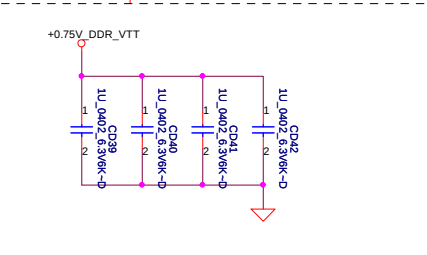
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<8> DDR_B_DQ0..63 <<>>
<8> DDR_B_DQS#0..7 <<>>
<8> DDR_B_MA[0..15] <<>>

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204

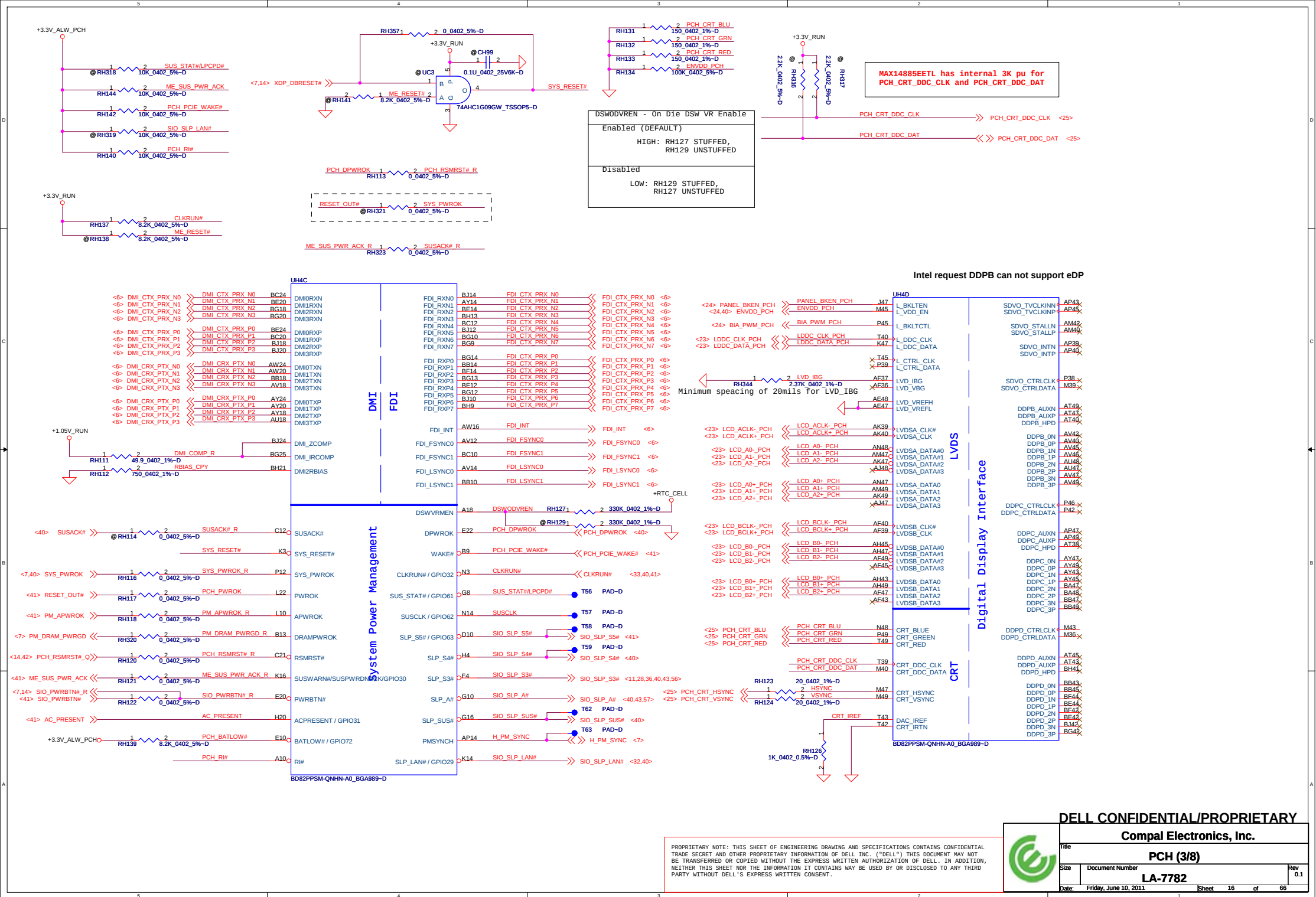


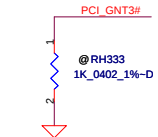
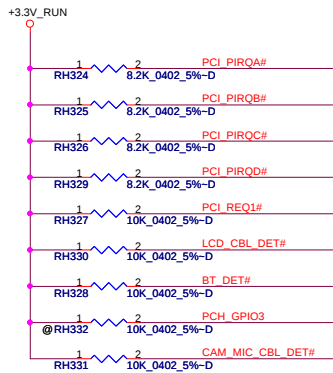
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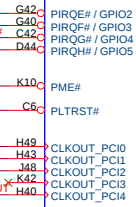
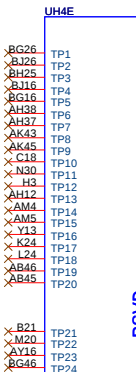
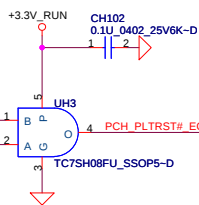
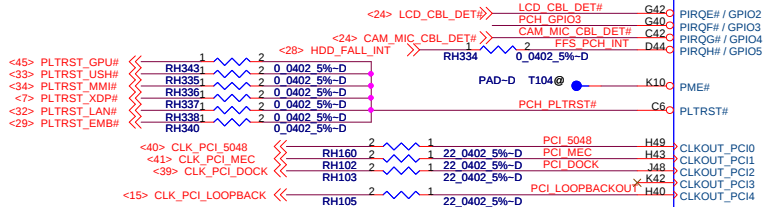


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Title			
DDRIII-SODIMM SLOT2			
LA-7782			
Size	Document Number	Rev	
LA-7782	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	13 of 66



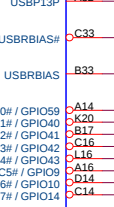
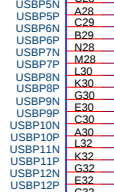
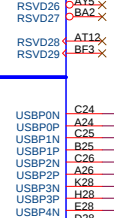
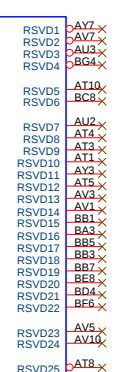


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

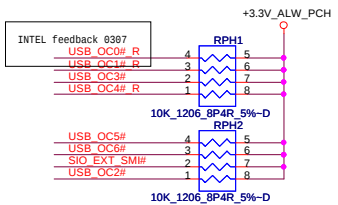
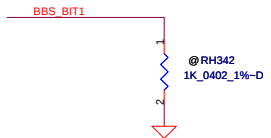
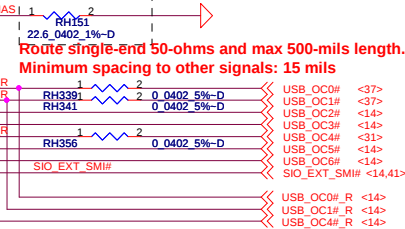


BD82PPSM-QNH-A0_BGA989-D

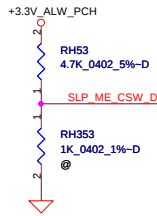
Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



- >Right Side Top
- >Right Side Bottom
- >Right side E-SATA
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >Left side
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch

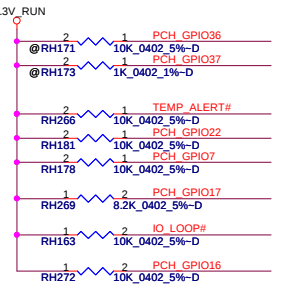
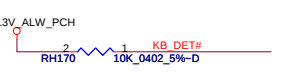
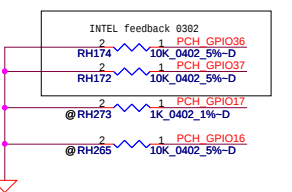
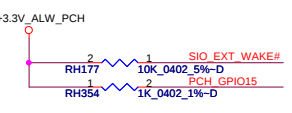


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PCH (4/8)			
LA-7782	Rev 0.1		
Date: Friday, June 10, 2011	Sheet 17 of 66		

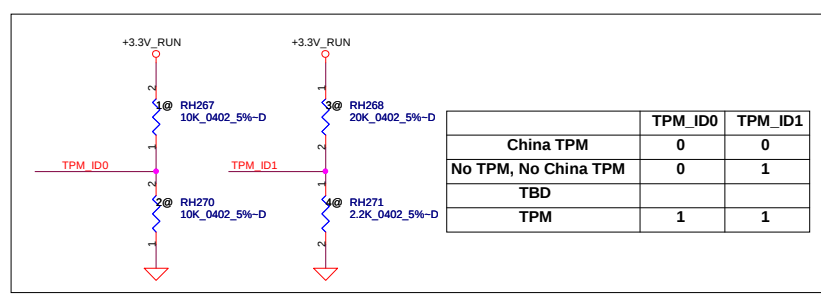


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

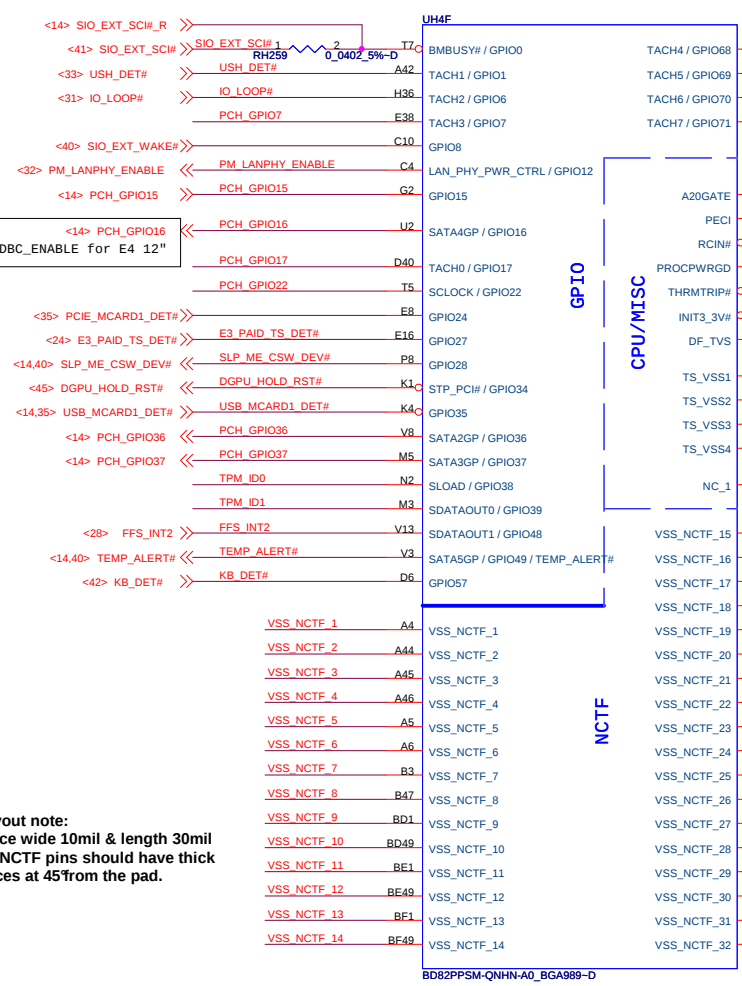
SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



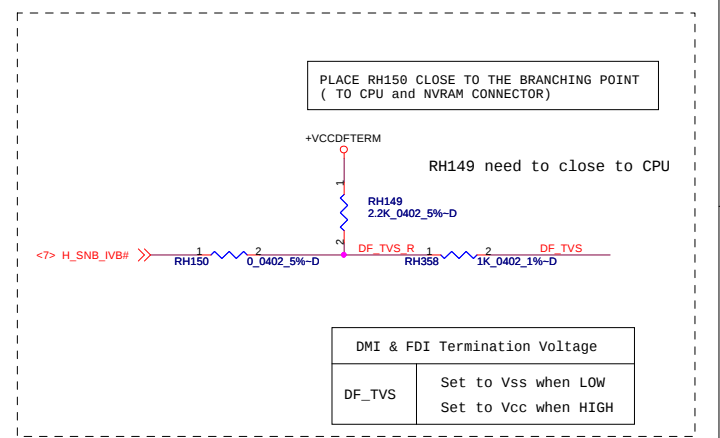
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1

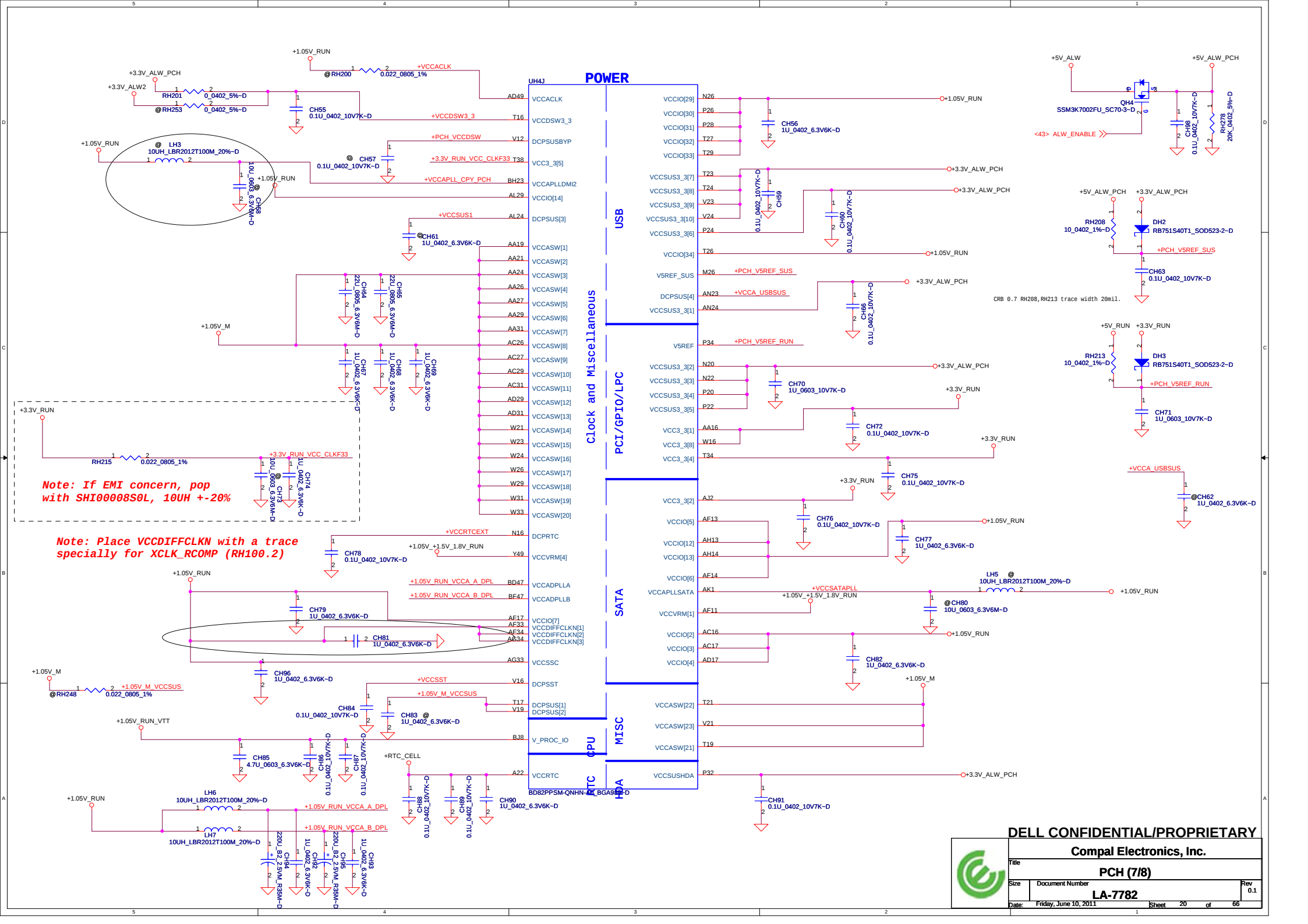


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



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Compal Electronics, Inc.			
PCH (5/8)			
LA-7782			
Rev 0.1			
Date: Friday, June 10, 2011			
Sheet 18 of 66			



DELL CONFIDENTIAL/PROPRIETARY



Compal Electronics, Inc.			
PCH (7/8)			
Size	Document Number	Rev	
	LA-7782	0.1	
Date:	Friday, June 10, 2011	Sheet	20 of 66

UH4H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK46
AA33	VSS[4]	VSS[83] AK8
AA34	VSS[5]	VSS[84] AL16
AB11	VSS[6]	VSS[85] AL17
AB14	VSS[7]	VSS[86] AL19
AB39	VSS[8]	VSS[87] AL2
AB4	VSS[9]	VSS[88] AL21
AB43	VSS[10]	VSS[89] AL23
AB5	VSS[11]	VSS[90] AL26
AB7	VSS[12]	VSS[91] AL27
AC19	VSS[13]	VSS[92] AL31
AC2	VSS[14]	VSS[93] AL33
AC21	VSS[15]	VSS[94] AL34
AC24	VSS[16]	VSS[95] AL48
AC33	VSS[17]	VSS[96] AM11
AC34	VSS[18]	VSS[97] AM14
AC48	VSS[19]	VSS[98] AM36
AD10	VSS[20]	VSS[99] AM39
AD11	VSS[21]	VSS[100] AM43
AD12	VSS[22]	VSS[101] AM45
AD13	VSS[23]	VSS[102] AM46
AD19	VSS[24]	VSS[103] AM7
AD24	VSS[25]	VSS[104] AN2
AD26	VSS[26]	VSS[105] AN29
AD27	VSS[27]	VSS[106] AN3
AD33	VSS[28]	VSS[107] AN31
AD34	VSS[29]	VSS[108] AP12
AD36	VSS[30]	VSS[109] AP19
AD37	VSS[31]	VSS[110] AP28
AD38	VSS[32]	VSS[111] AP32
AD39	VSS[33]	VSS[112] AP38
AD4	VSS[34]	VSS[113] AP4
AD40	VSS[35]	VSS[114] AP42
AD42	VSS[36]	VSS[115] AP46
AD43	VSS[37]	VSS[116] AP8
AD45	VSS[38]	VSS[117] AR2
AD46	VSS[39]	VSS[118] AR43
AD8	VSS[40]	VSS[119] AT11
AE2	VSS[41]	VSS[120] AT118
AE3	VSS[42]	VSS[121] AT122
AF10	VSS[43]	VSS[122] AT126
AF12	VSS[44]	VSS[123] AT132
AD16	VSS[45]	VSS[124] AT134
AF16	VSS[46]	VSS[125] AT139
VSS[47]	VSS[47]	VSS[126] AT142
AF19	VSS[48]	VSS[127] AT146
AF24	VSS[49]	VSS[128] AU24
AF26	VSS[50]	VSS[129] AU30
AF27	VSS[51]	VSS[130] AV16
AF29	VSS[52]	VSS[131] AV20
AF31	VSS[53]	VSS[132] AV24
AF38	VSS[54]	VSS[133] AV30
AF4	VSS[55]	VSS[134] AV38
AF42	VSS[56]	VSS[135] AV4
AF46	VSS[57]	VSS[136] AV8
AF5	VSS[58]	VSS[137] AW14
AF7	VSS[59]	VSS[138] AW18
AF8	VSS[60]	VSS[139] AW22
AG19	VSS[61]	VSS[140] AW26
AG2	VSS[62]	VSS[141] AW28
AG31	VSS[63]	VSS[142] AW32
AG48	VSS[64]	VSS[143] AW36
AH11	VSS[65]	VSS[144] AW40
AH3	VSS[66]	VSS[145] AW48
AH36	VSS[67]	VSS[146] AV11
AH39	VSS[68]	VSS[147] AY12
AH40	VSS[69]	VSS[148] AY22
AH42	VSS[70]	VSS[149] AY28
AH46	VSS[71]	VSS[150]
AH7	VSS[72]	VSS[151]
A119	VSS[73]	VSS[152]
A121	VSS[74]	VSS[153]
A124	VSS[75]	VSS[154]
A133	VSS[76]	VSS[155]
A134	VSS[77]	VSS[156]
AK12	VSS[78]	VSS[157]
AK3	VSS[79]	VSS[158]

BD82PPSM-QNHN-A0_BGA989-D

UH4I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L36
B39	VSS[170]	VSS[270] L48
B7	VSS[171]	VSS[271] M12
F45	VSS[172]	VSS[272] M18
B12	VSS[173]	VSS[273] M22
BB16	VSS[174]	VSS[274] M24
BB20	VSS[175]	VSS[275] M30
BB22	VSS[176]	VSS[276] M32
BB24	VSS[177]	VSS[277] M34
BB28	VSS[178]	VSS[278] M38
BB30	VSS[179]	VSS[279] M4
BB38	VSS[180]	VSS[280] M42
BB4	VSS[181]	VSS[281] M46
BB46	VSS[182]	VSS[282] M8
BC14	VSS[183]	VSS[283] N18
BC18	VSS[184]	VSS[284] P30
BC2	VSS[185]	VSS[285] N47
BC22	VSS[186]	VSS[286] P11
BC26	VSS[187]	VSS[287] P18
BC32	VSS[188]	VSS[288] T33
BC34	VSS[189]	VSS[289] P40
BC36	VSS[190]	VSS[290] P43
BC40	VSS[191]	VSS[291] P47
BC42	VSS[192]	VSS[292] P7
BC48	VSS[193]	VSS[293] R2
BD46	VSS[194]	VSS[294] R48
BD5	VSS[195]	VSS[295] T12
BE22	VSS[196]	VSS[296] T31
BE26	VSS[197]	VSS[297] T4
BE40	VSS[198]	VSS[298] W34
BF12	VSS[199]	VSS[299] T46
BF16	VSS[200]	VSS[300] T8
BF20	VSS[201]	VSS[301] V11
BF22	VSS[202]	VSS[302] V17
BF24	VSS[203]	VSS[303] V26
BF26	VSS[204]	VSS[304] V27
BF28	VSS[205]	VSS[305] V29
BF28	VSS[206]	VSS[306] V31
BF30	VSS[207]	VSS[307] V38
BF38	VSS[208]	VSS[308] V39
BF8	VSS[209]	VSS[309] V43
BF40	VSS[210]	VSS[310] V7
BF8	VSS[211]	VSS[311] W17
BG17	VSS[212]	VSS[312] W19
BG21	VSS[213]	VSS[313] W2
BG33	VSS[214]	VSS[314] W27
BG44	VSS[215]	VSS[315] W48
BH11	VSS[216]	VSS[316] Y12
BH15	VSS[217]	VSS[317] Y38
BH17	VSS[218]	VSS[318] Y4
BH19	VSS[219]	VSS[319] Y42
H10	VSS[220]	VSS[320] Y46
BH27	VSS[221]	VSS[321] Y8
BH31	VSS[222]	VSS[322] BG29
BH33	VSS[223]	VSS[323] N24
BH35	VSS[224]	VSS[324] A13
BH39	VSS[225]	VSS[325] AD47
BH43	VSS[226]	VSS[326] B43
BH7	VSS[227]	VSS[327] BE10
D3	VSS[228]	VSS[328] BG41
D12	VSS[229]	VSS[329] G14
D16	VSS[230]	VSS[330] H16
D18	VSS[231]	VSS[331] T36
D22	VSS[232]	VSS[332] BG22
D24	VSS[233]	VSS[333] BG24
D26	VSS[234]	VSS[334] C22
D30	VSS[235]	VSS[335] AP13
D32	VSS[236]	VSS[336] M14
D34	VSS[237]	VSS[337] AP2
D38	VSS[238]	VSS[338] AP1
D42	VSS[239]	VSS[339] BE16
D48	VSS[240]	VSS[340] BC16
E18	VSS[241]	VSS[341] BG28
E26	VSS[242]	VSS[342] B128
G18	VSS[243]	VSS[343]
G20	VSS[244]	VSS[344]
G26	VSS[245]	VSS[345]
G28	VSS[246]	VSS[346]
G36	VSS[247]	VSS[347]
G48	VSS[248]	VSS[348]
H12	VSS[249]	VSS[349]
H18	VSS[250]	VSS[350]
H22	VSS[251]	VSS[351]
H24	VSS[252]	VSS[352]
H26	VSS[253]	
H30	VSS[254]	
H32	VSS[255]	
H34	VSS[256]	
F3	VSS[257]	
	VSS[258]	

BD82PPSM-QNHN-A0_BGA989-D

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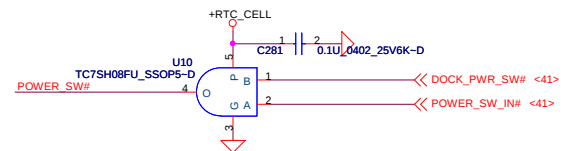
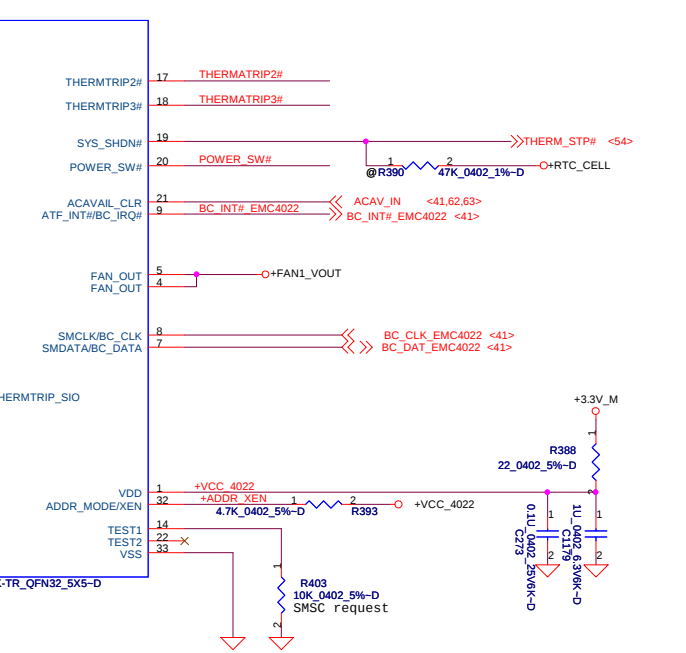
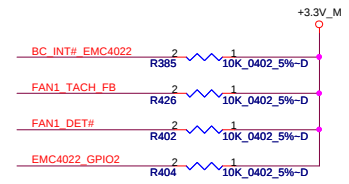
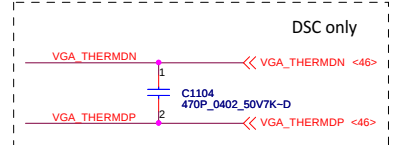
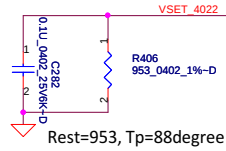
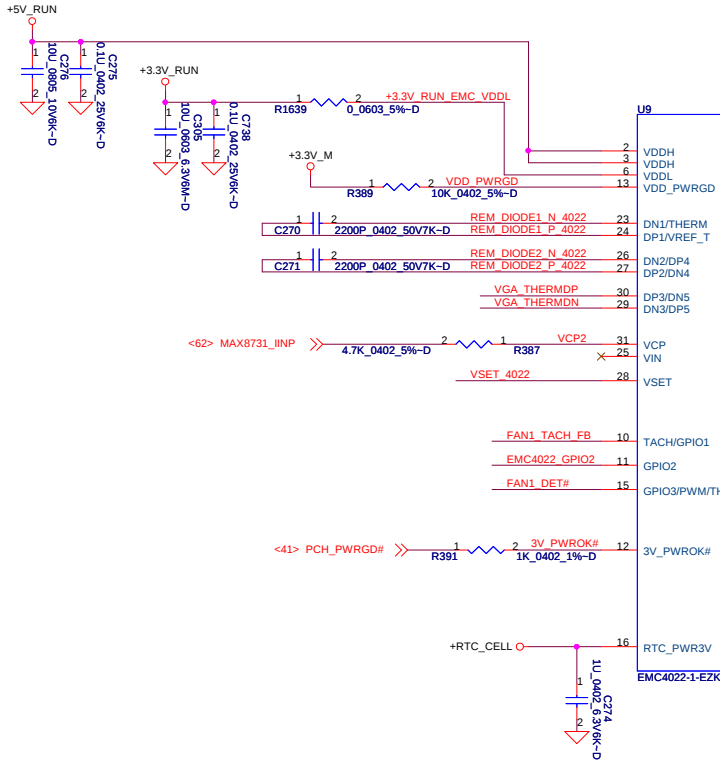
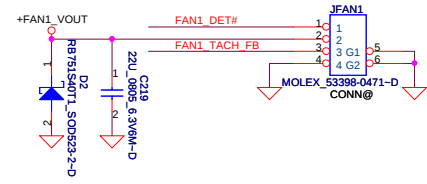
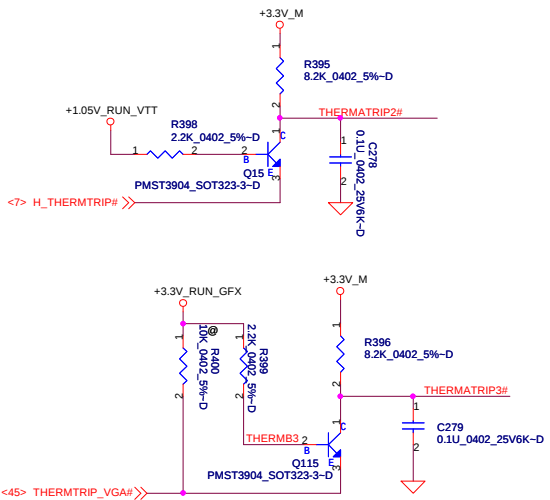
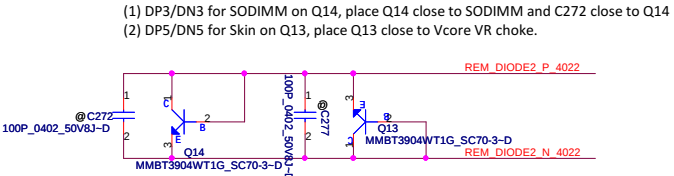
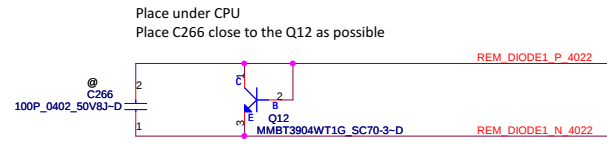
Compal Electronics, Inc.

Title PCH (8/8)

Size Document Number

LA-7782

Date Monday, May 23, 2011 Sheet 21 of 66 Rev 0.1

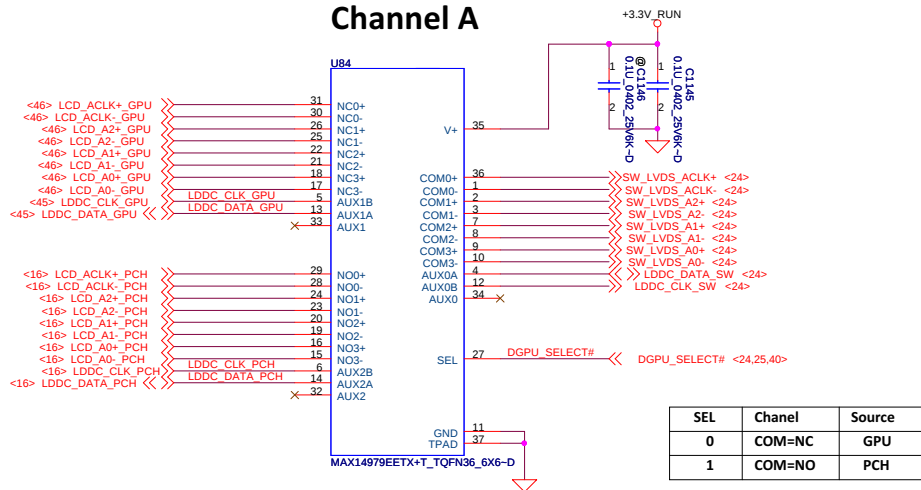


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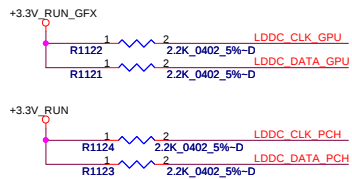
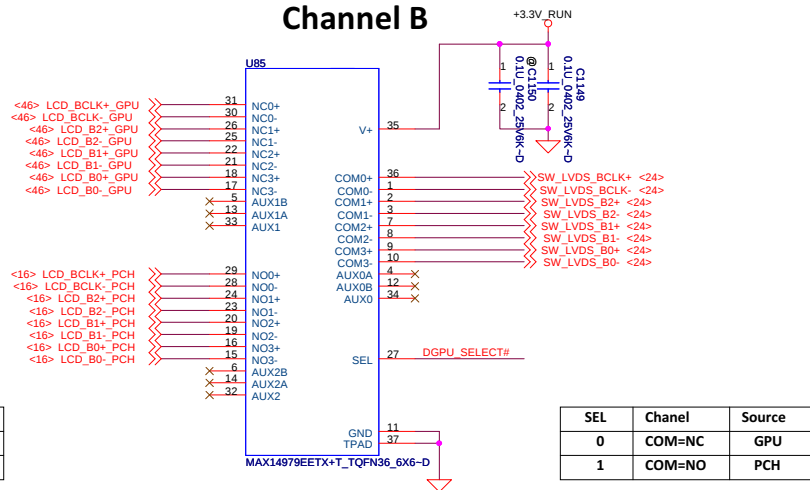
Compal Electronics, Inc.			
Title	FAN & Thermal Sensor		
Size	Document Number	Rev	
	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	22 of 66

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Channel A



Channel B



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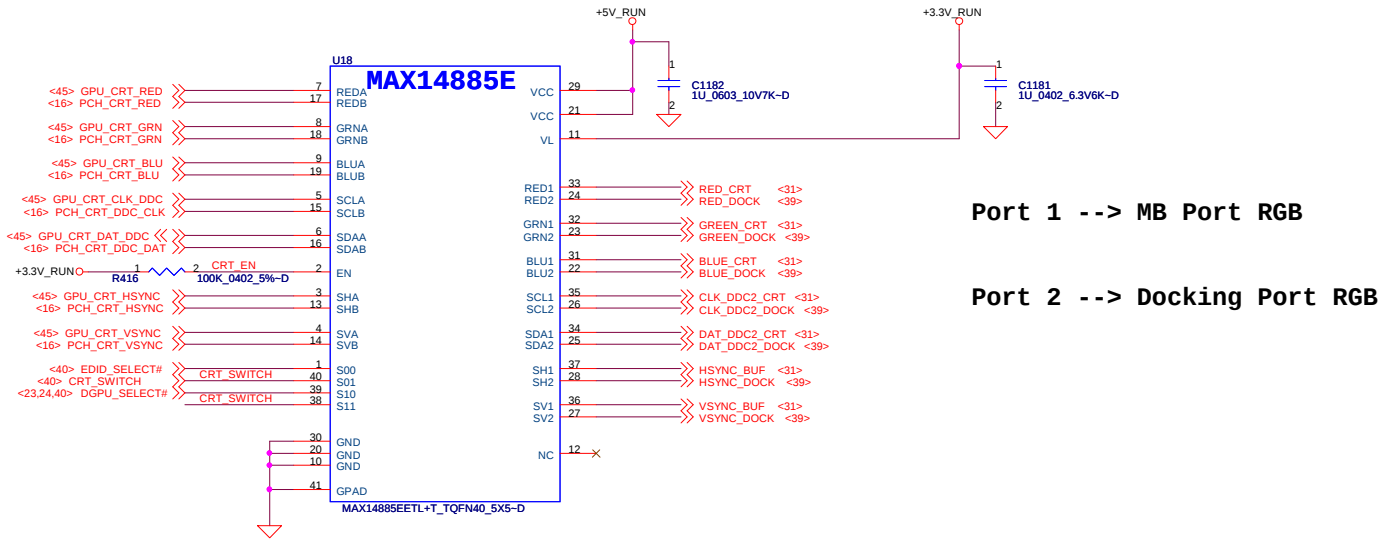
Compal Electronics, Inc.

Title			LA-7782
Size			Rev 0.1
Date			Friday, June 10, 2011
Sheet			23 of 66

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Channel A --> GPU

Channel B --> PCH

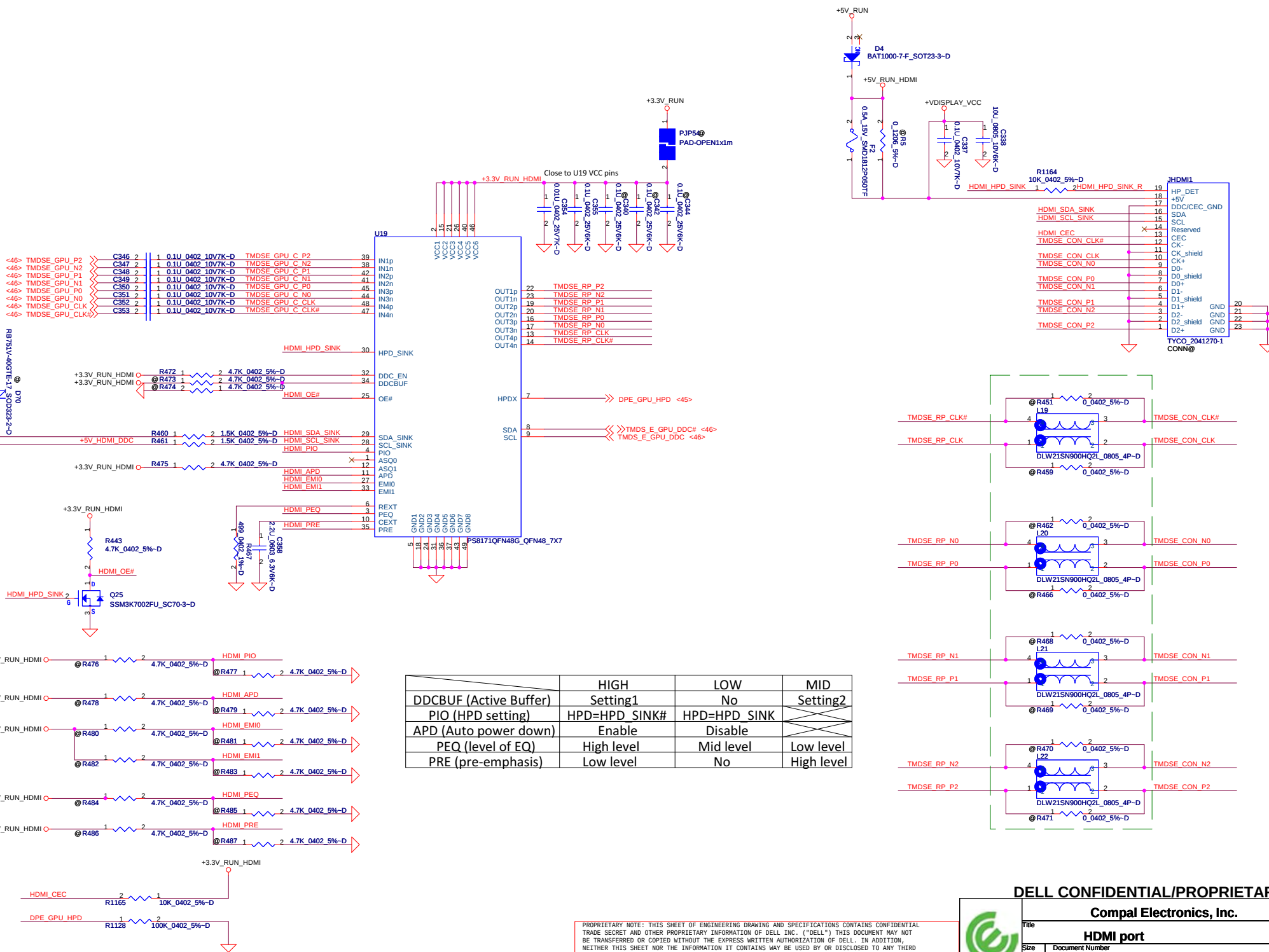


CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

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CRT/Video switch			
Size	Document Number	Rev	0.1
LA-7782			
Date:	Friday, June 10, 2011	Sheet	25 of 66

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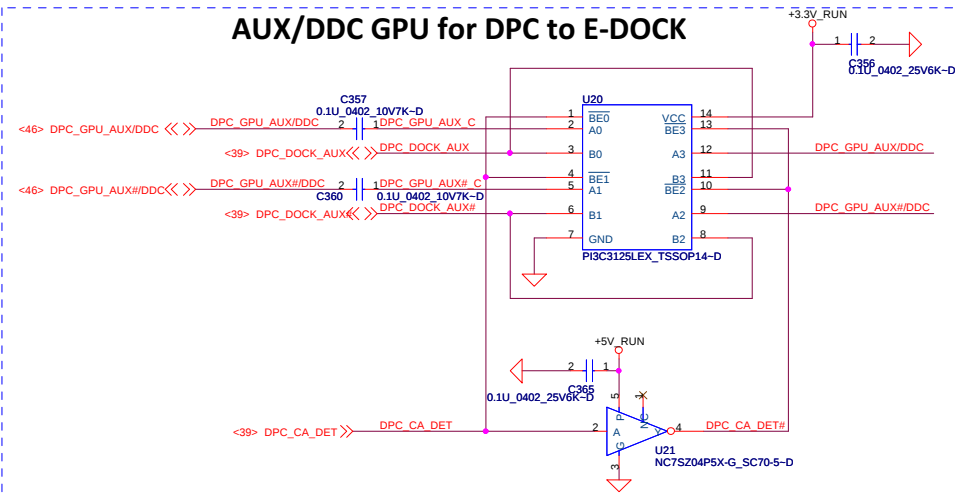
	HIGH	LOW	MID
DDCБУF (Active Buffer)	Setting1	No	Setting2
PIQ (HPD setting)	HPD=HPD_SINK#	HPD=HPD_SINK	
APD (Auto power down)	Enable	Disable	
PEQ (level of EQ)	High level	Mid level	Low level
PRE (pre-emphasis)	Low level	No	High level

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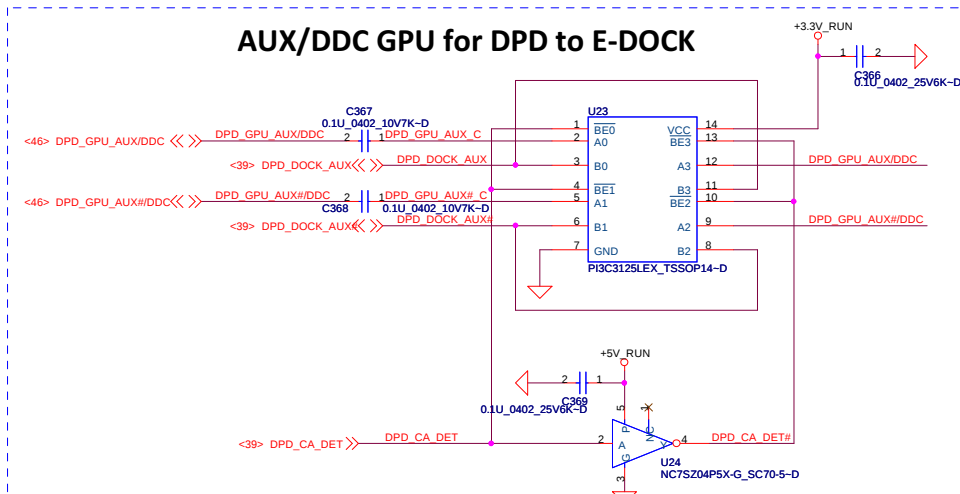
Compal Electronics, Inc.		
HDMI port		
Size	Document Number	Rev
	LA-7782	0.1
Date	Friday, June 10, 2011	Sheet 26 of 66

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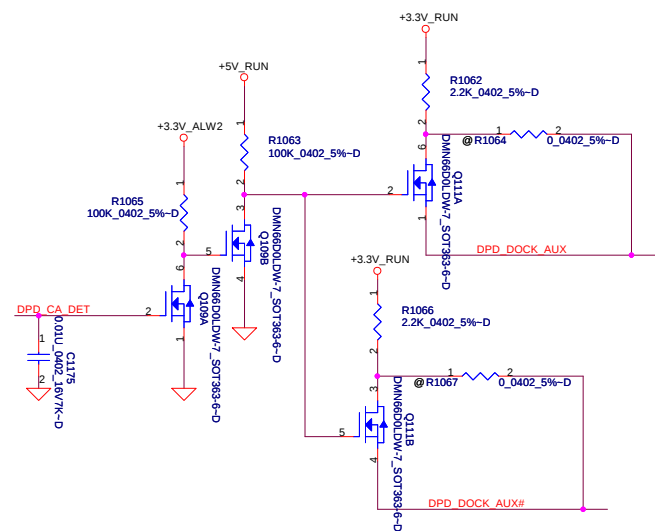
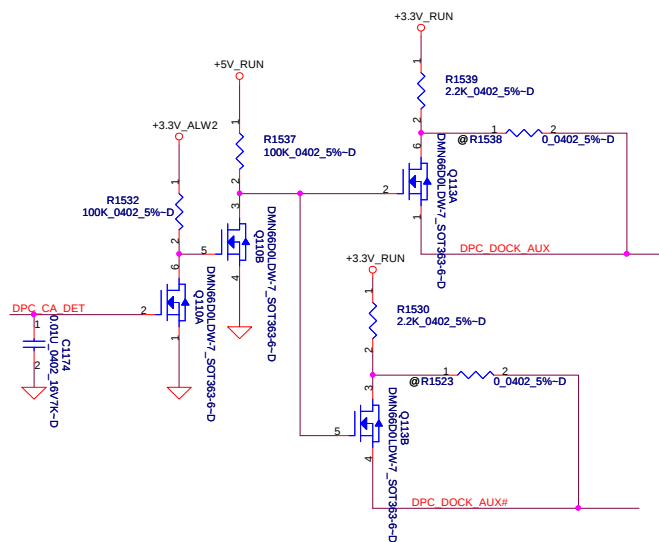
AUX/DDC GPU for DPC to E-DOCK



AUX/DDC GPU for DPD to E-DOCK



There is a new die for PI3C3125. Sample available on May.



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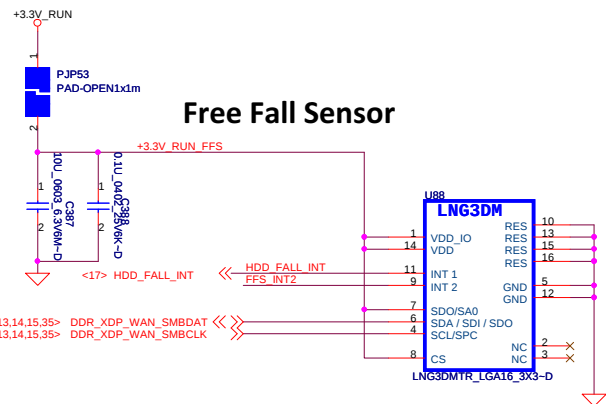


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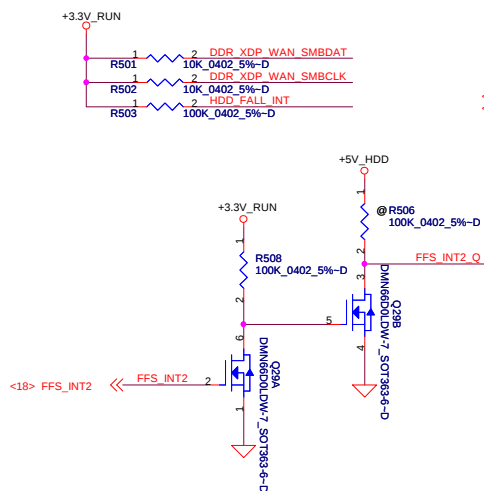
Compal Electronics, Inc.

Title **DP AUX SW**

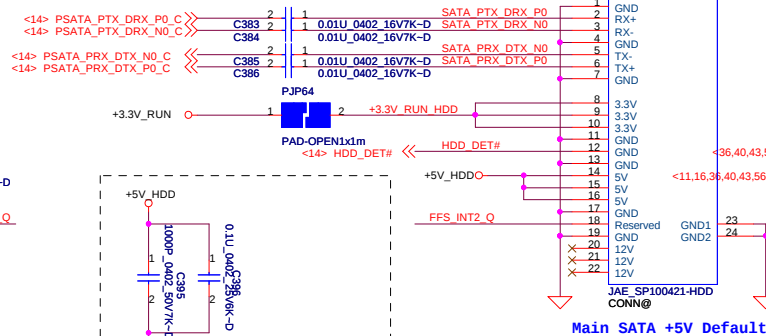
Size	Document Number	Rev
	LA-7782	0.1
Date:	Friday, June 10, 2011	Sheet 27 of 66



Free Fall Sensor

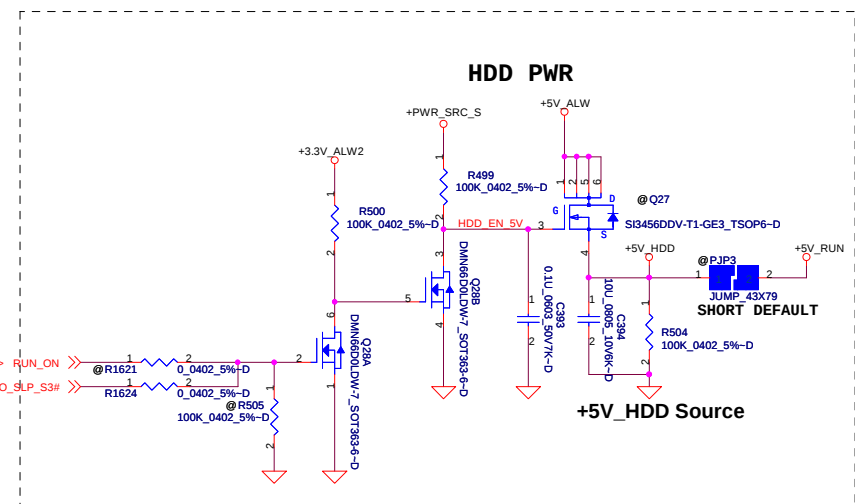


For HDD Temp.



Pleace near HDD CONN

Pleace near HDD CONN



HDD PWR

+5V_HDD Source

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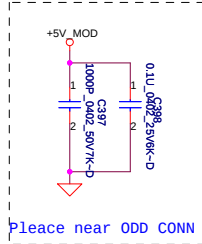
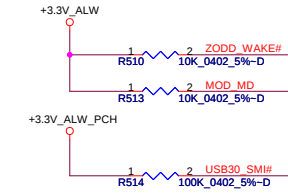
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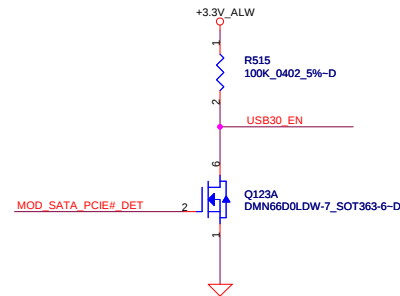
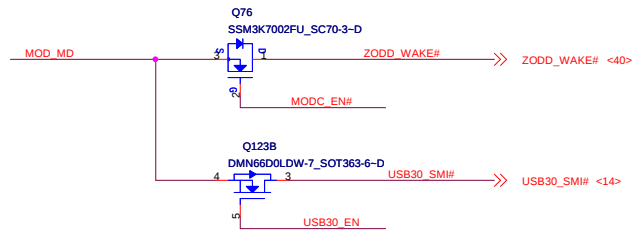
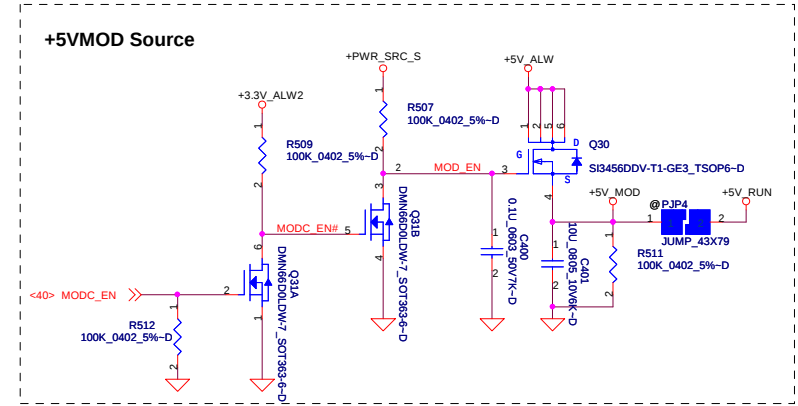
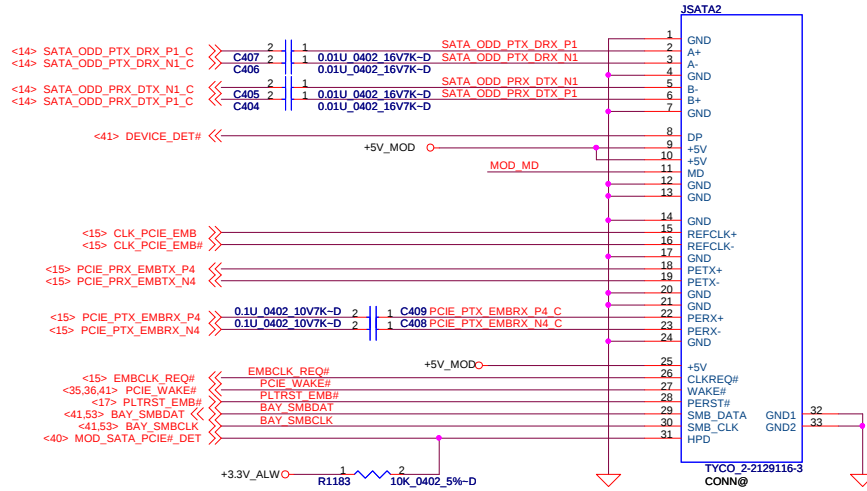
HDD CONNECTOR			
Size	Document Number	Rev	0.1
Date	Friday, June 10, 2011	Sheet	28 of 66

LA-7782

For ODD



Pleace near ODD CONN



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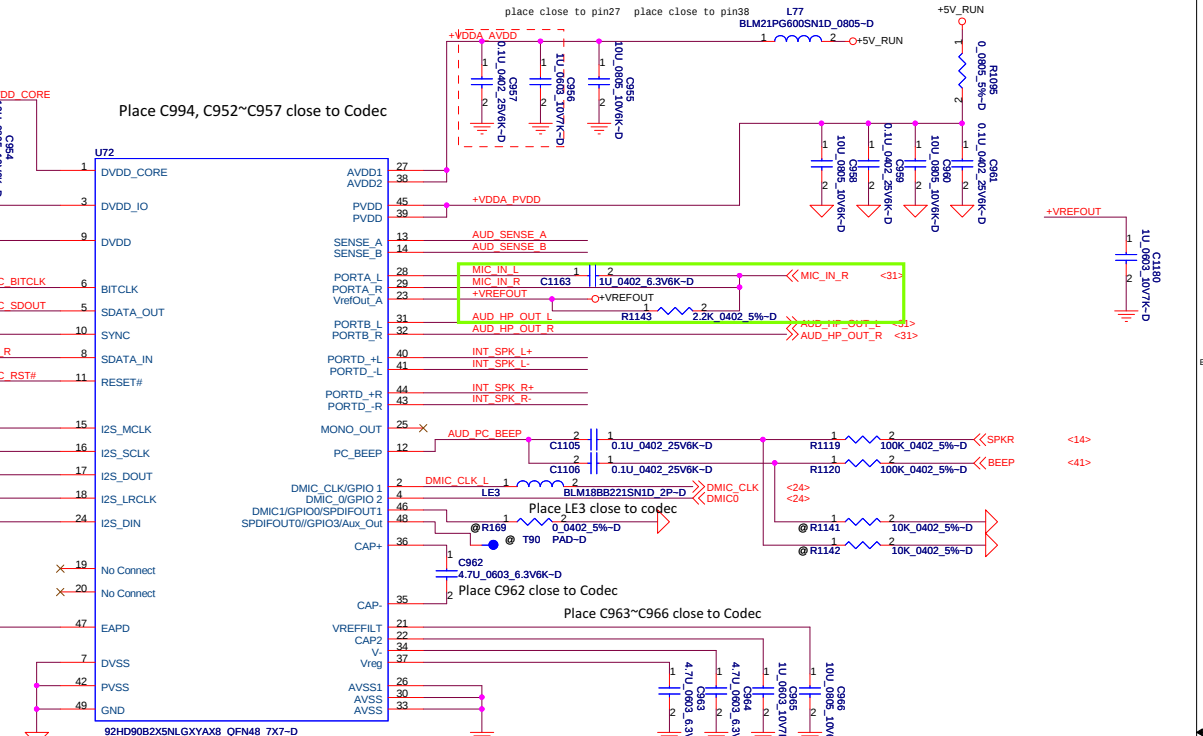
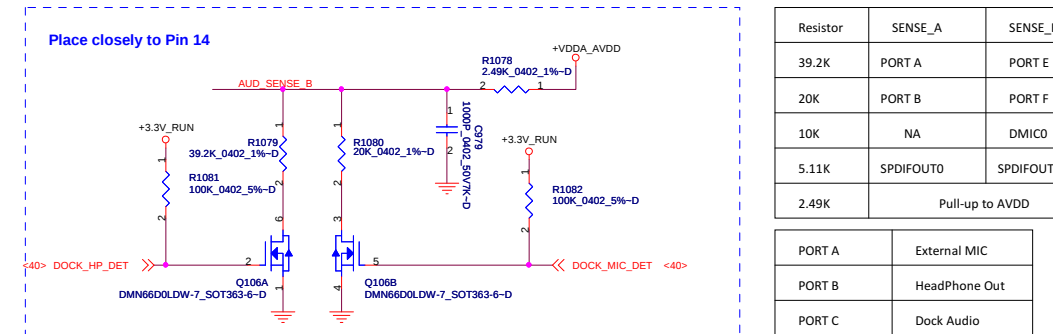
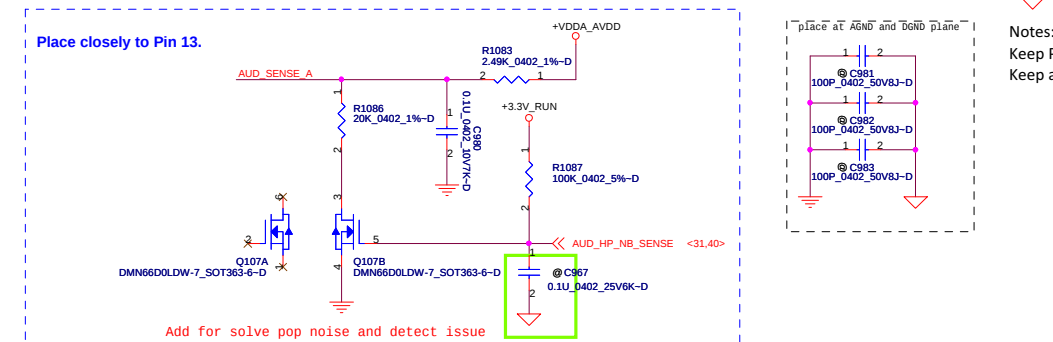
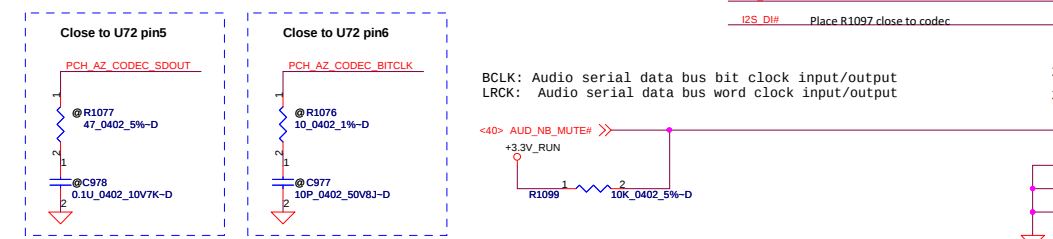
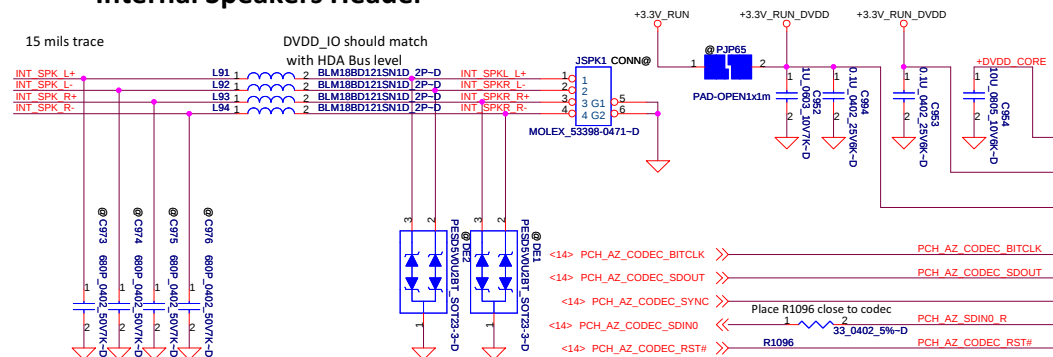
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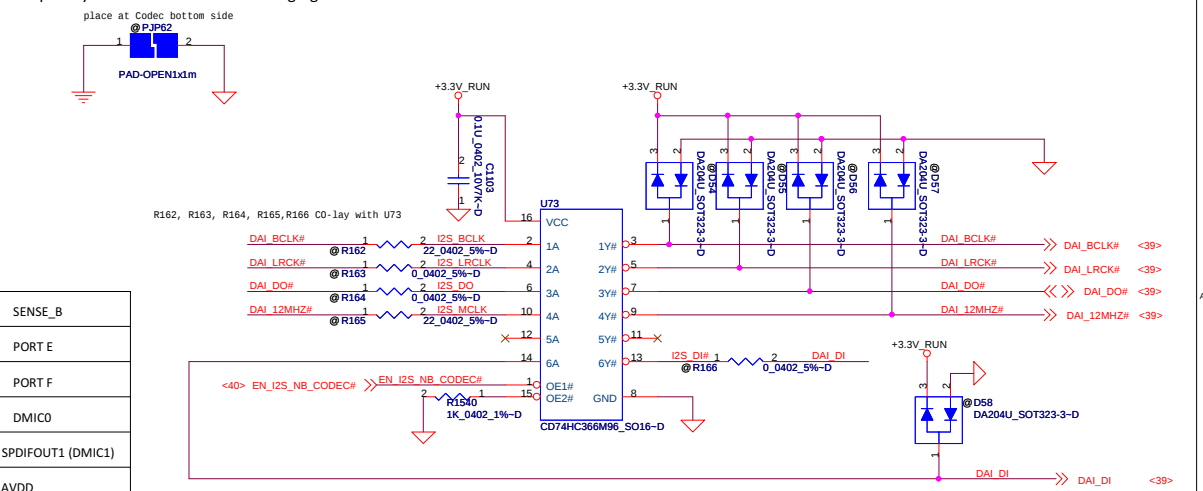


Title		
ODD CONNECTOR		
Size	Document Number	Rev
	LA-7782	0.1
Date	Friday, June 10, 2011	Sheet 29 of 66

Internal Speakers Header



Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

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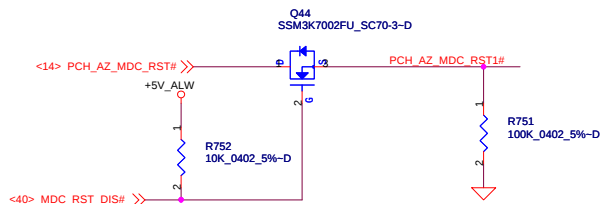
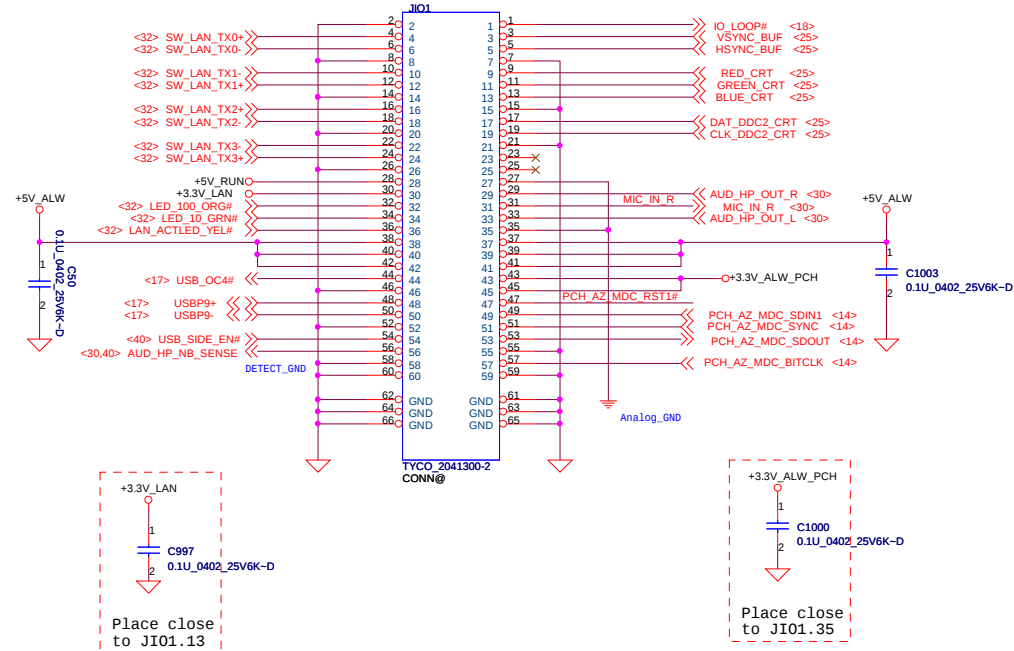
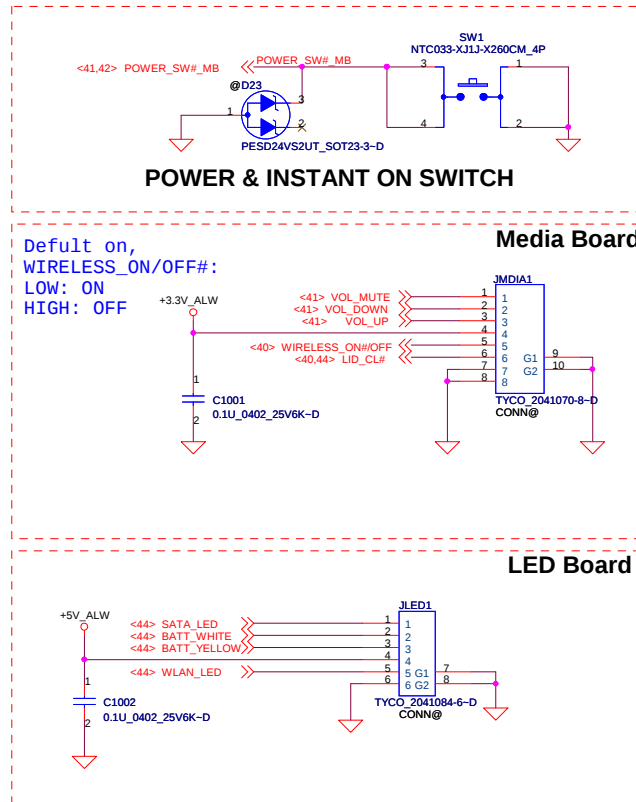
Compal Electronics, Inc.

Azalia (HD) Codec

Size	Document Number	Rev
	LA-7782	0.1
Date:	Friday, June 10, 2011	Sheet 30 of 66

I/O board CONN.

Change to TYCO_2041300-2_60P-T and Horizontal reverse to SSI

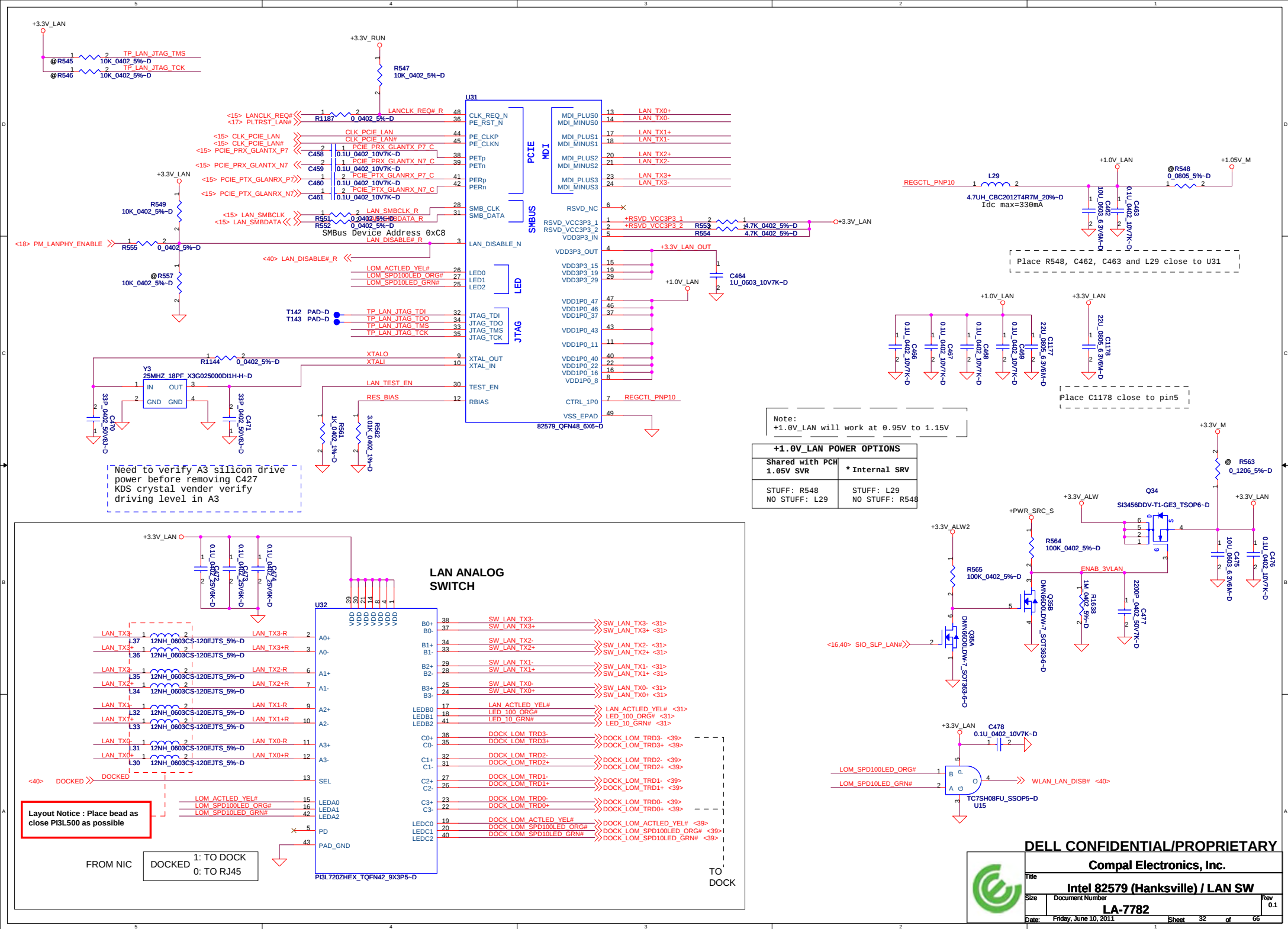


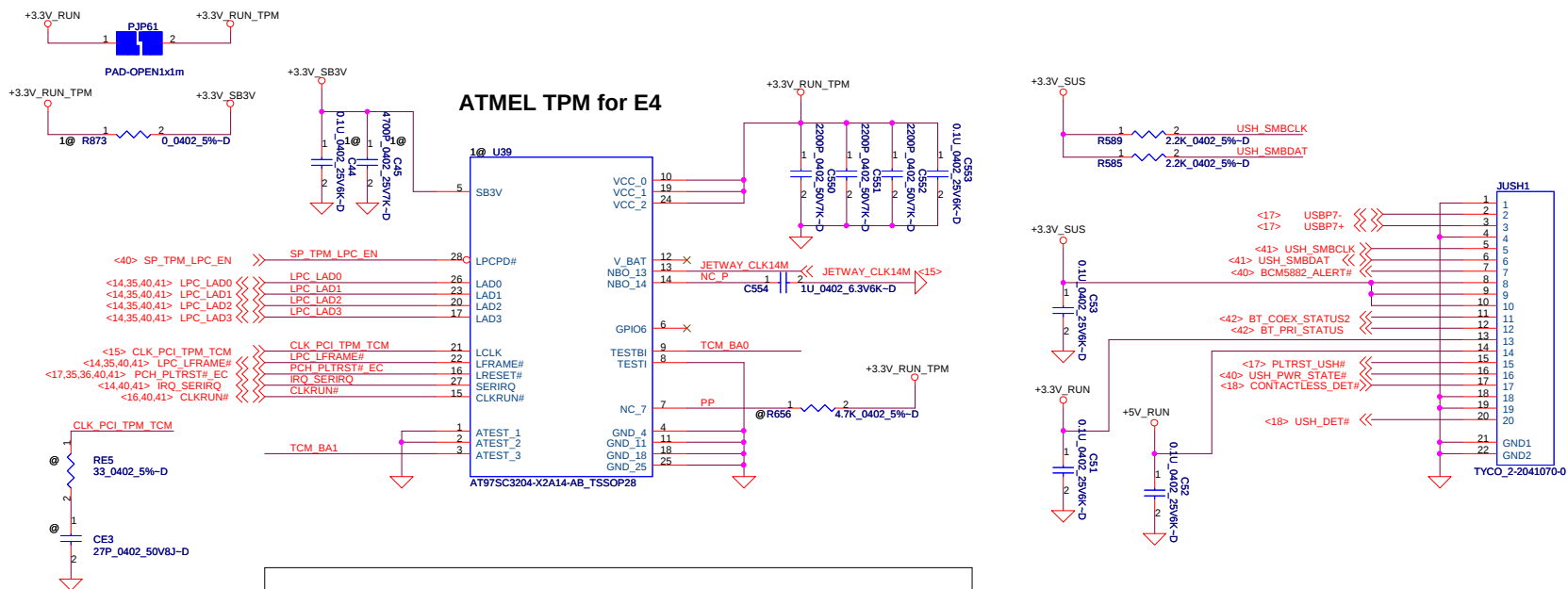
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Title	PWR SW/Sub-board Connector		
Size	Document Number	LA-7782	Rev 0.1
Date	Friday, June 10, 2011	Sheet 31	of 66



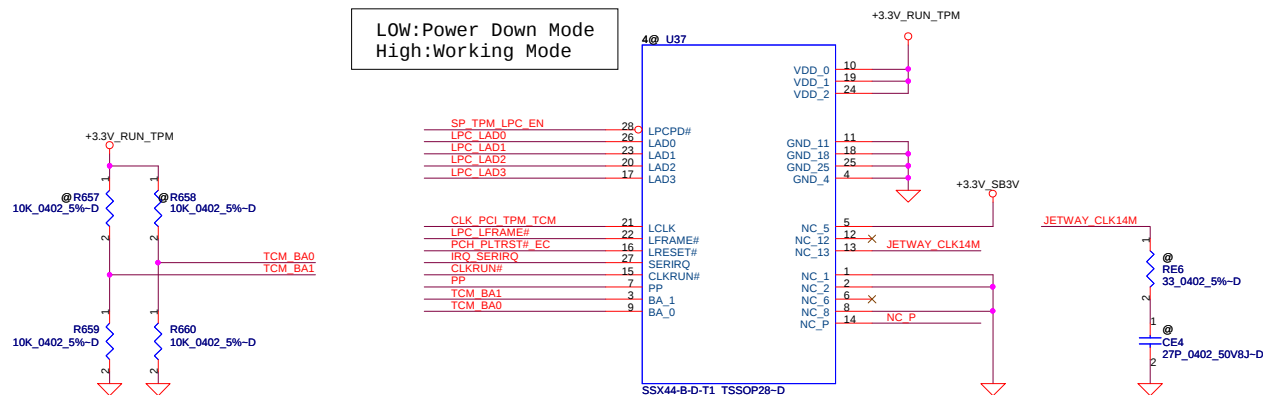


Co-lay U37 and U38

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

Low:Power Down Mode
High:Working Mode

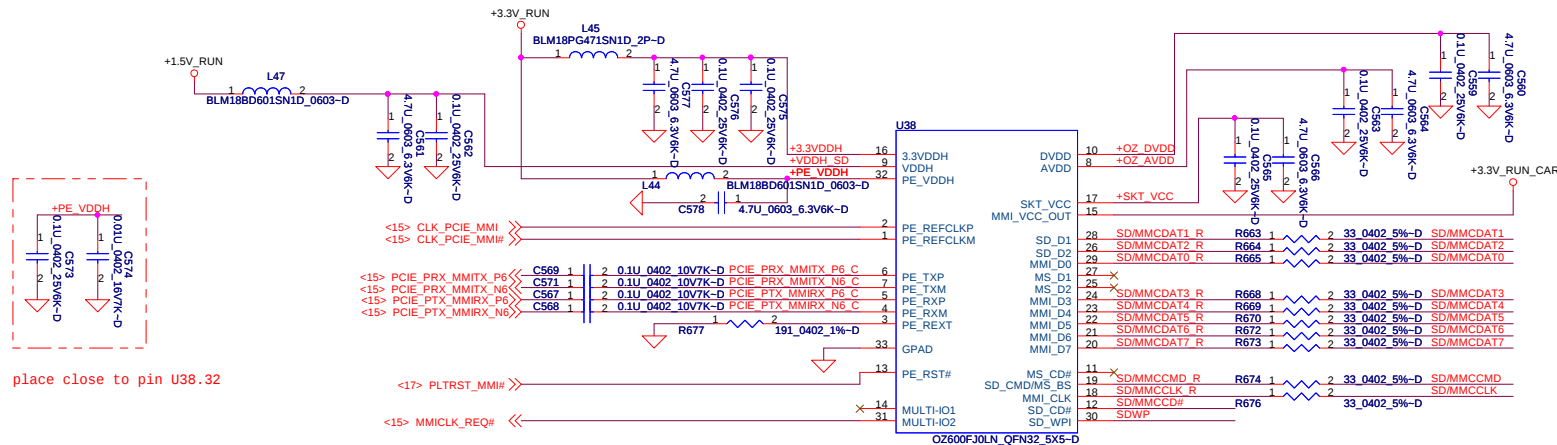


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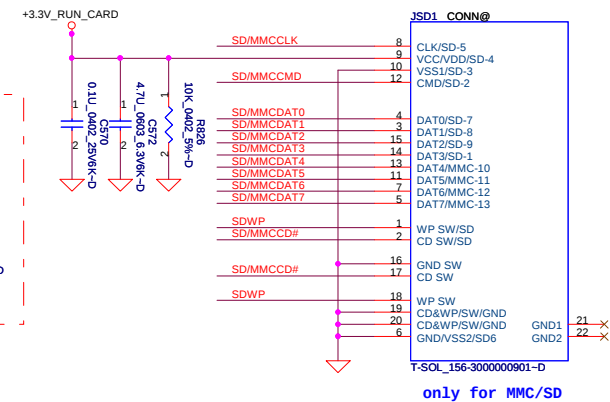
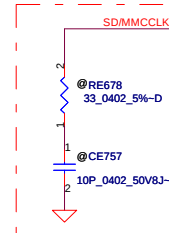
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Title			USH conn/TPM
Size	Document Number	Rev	
	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	33 of 66



Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible

EMI request



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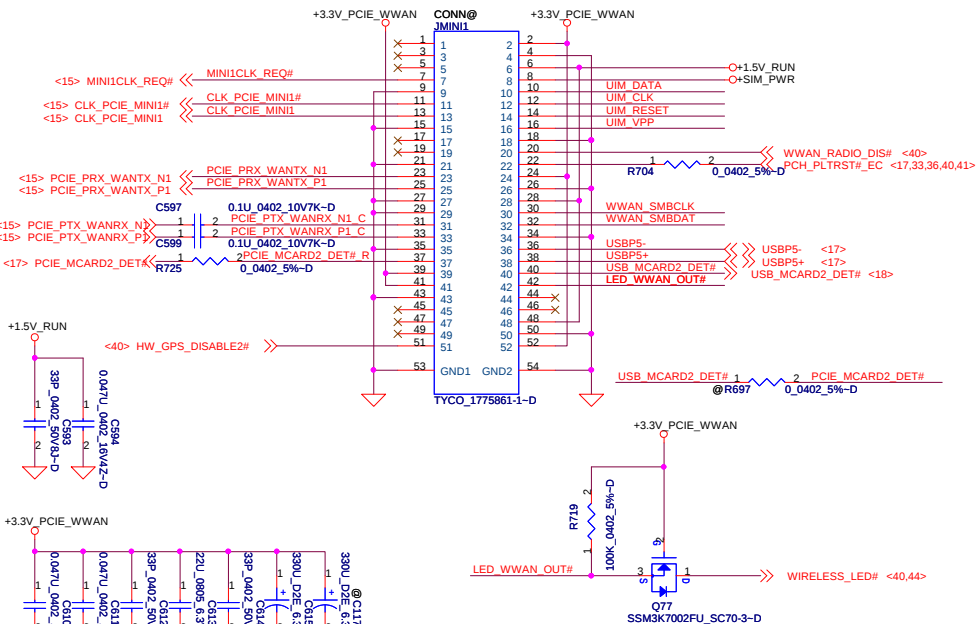


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Size	Document Number	Rev	
	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	34 of 66

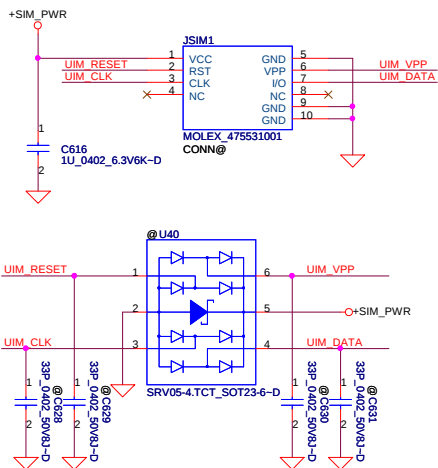
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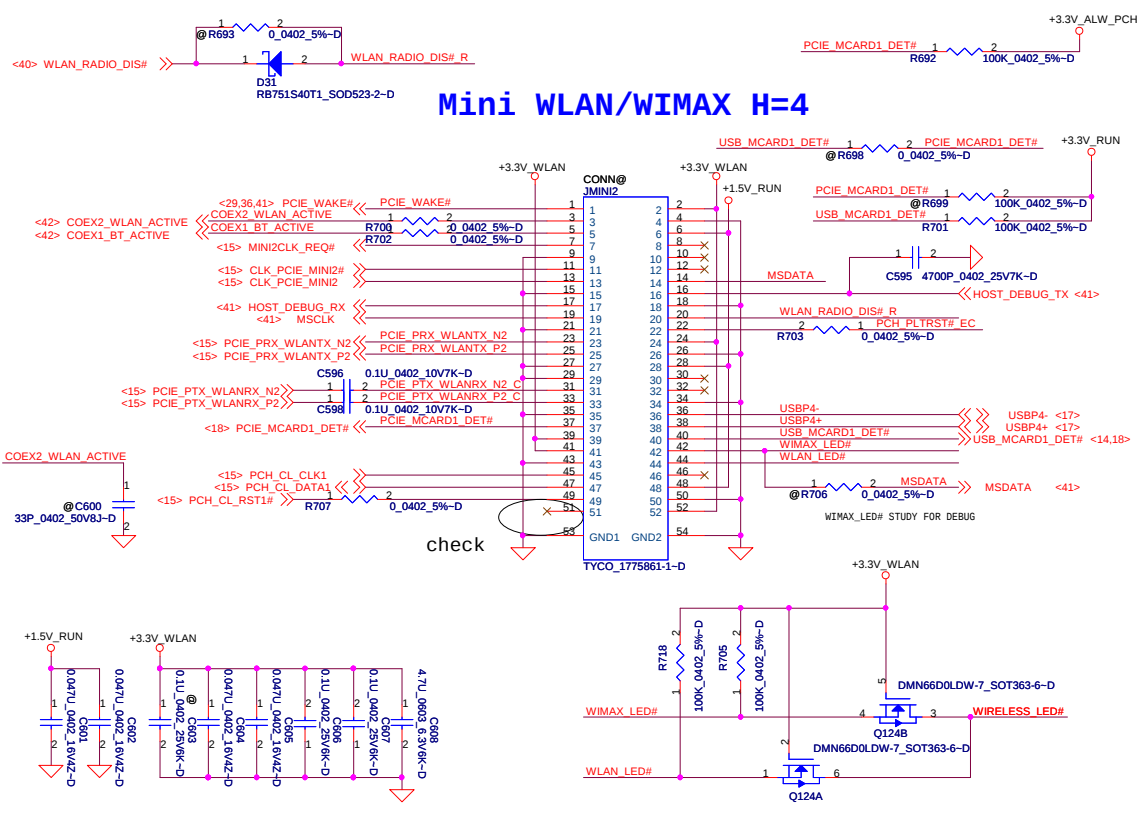
Mini WWAN/GPS/LTE H=5.2



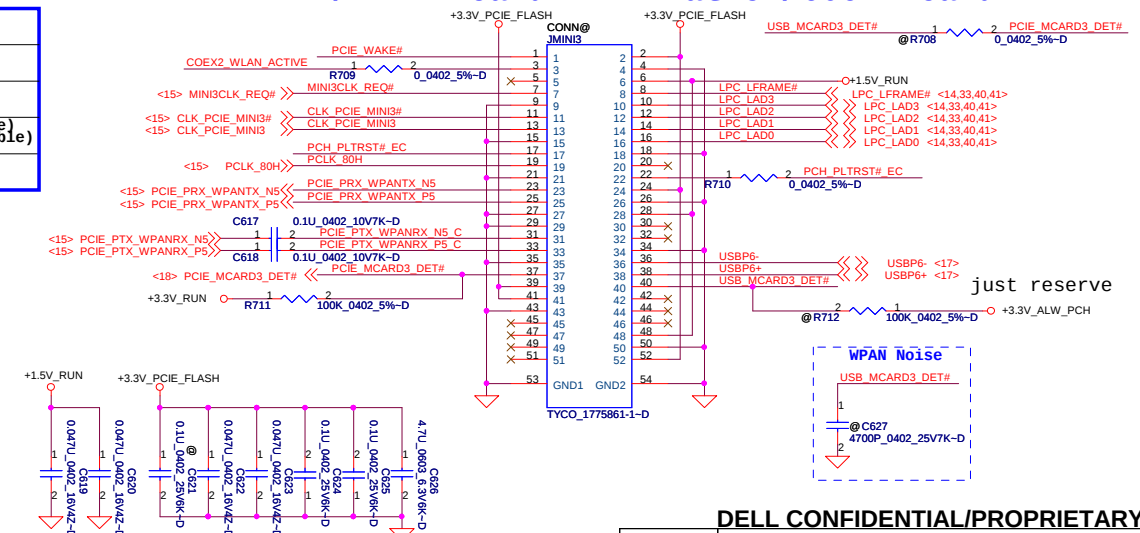
SIM Card Push-Push



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA



1/2 Minicard Pink Pather/60GHz Card H=4



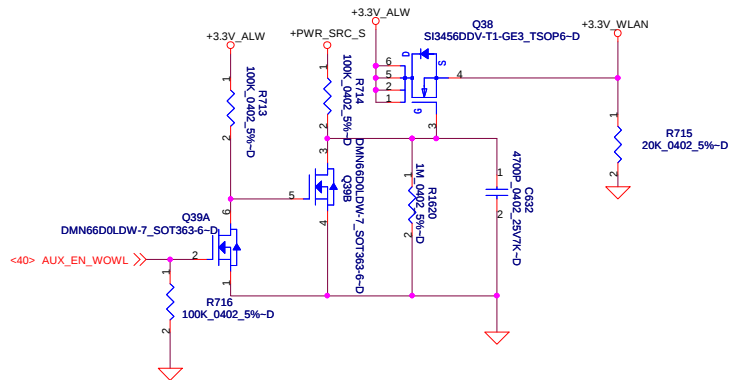
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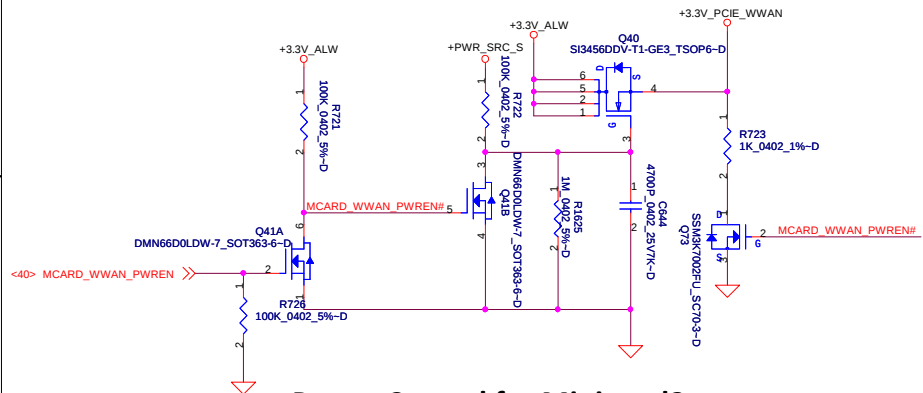
Compal Electronics, Inc.			
Mini Card			
LA-7782			
Friday, June 10, 2011	Sheet	35	of 66

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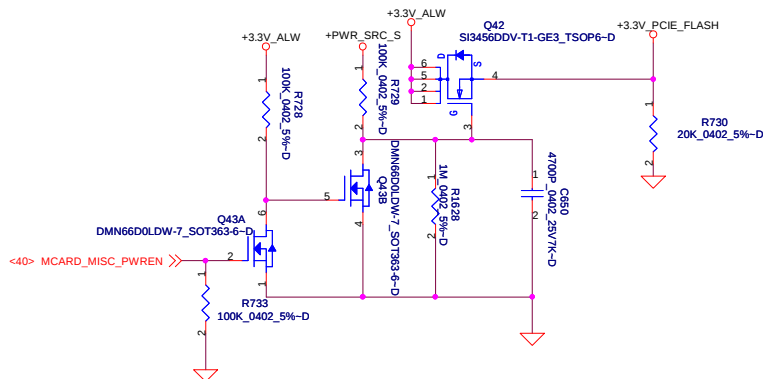
Power Control for Mini card2



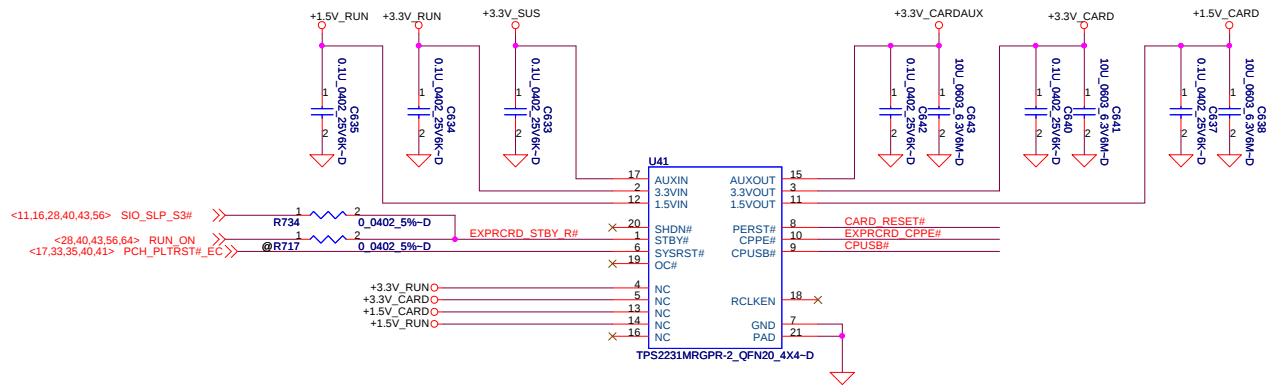
Power Control for Mini card1



Power Control for Mini card3

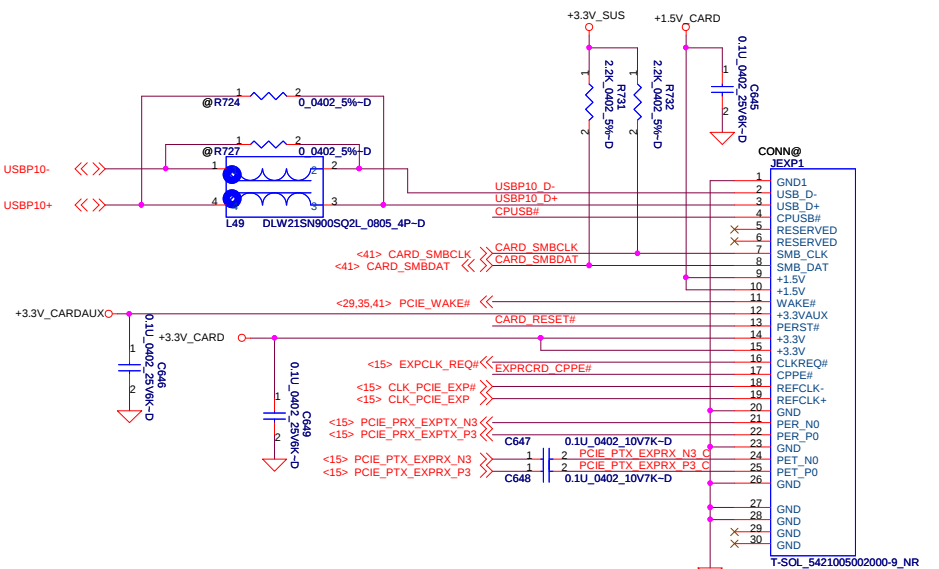


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.



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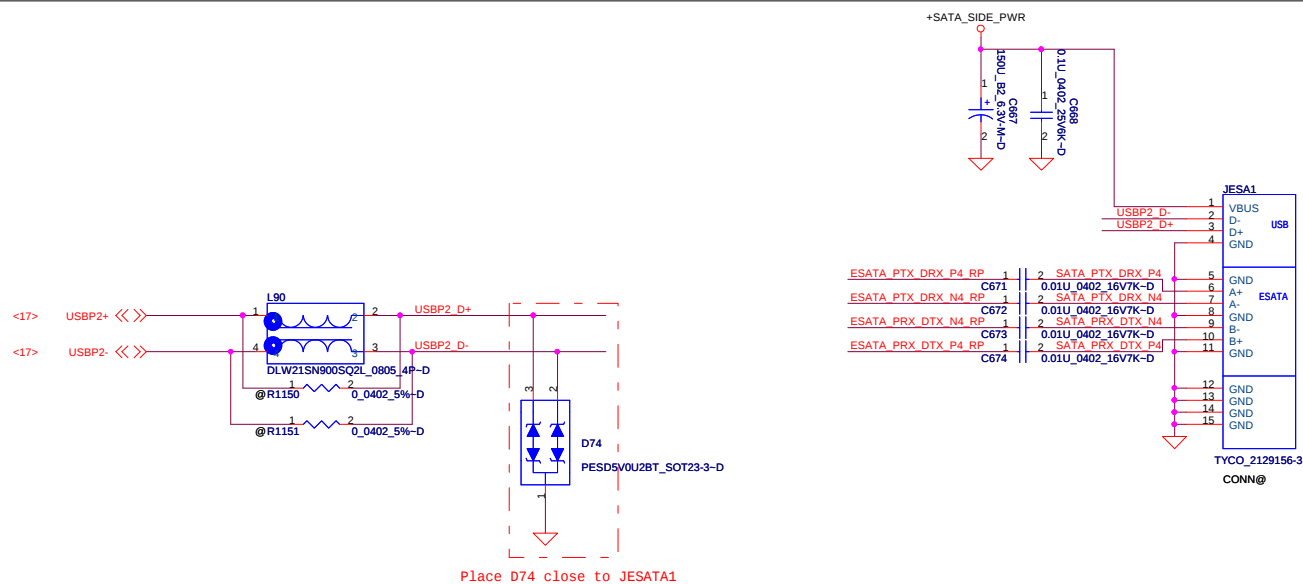
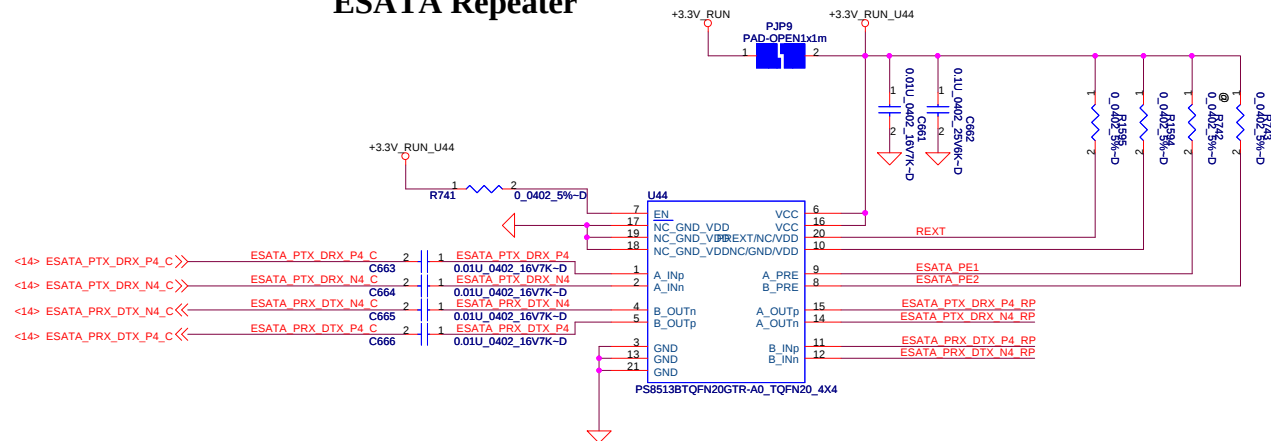
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Title	PCIE-SATA SW / PCIE PWR
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Size	Document Number	Rev
	LA 3782	0.1

LA-7782	
Date: Friday, June 10, 2011	Sheet 36 of 66

ESATA Repeater



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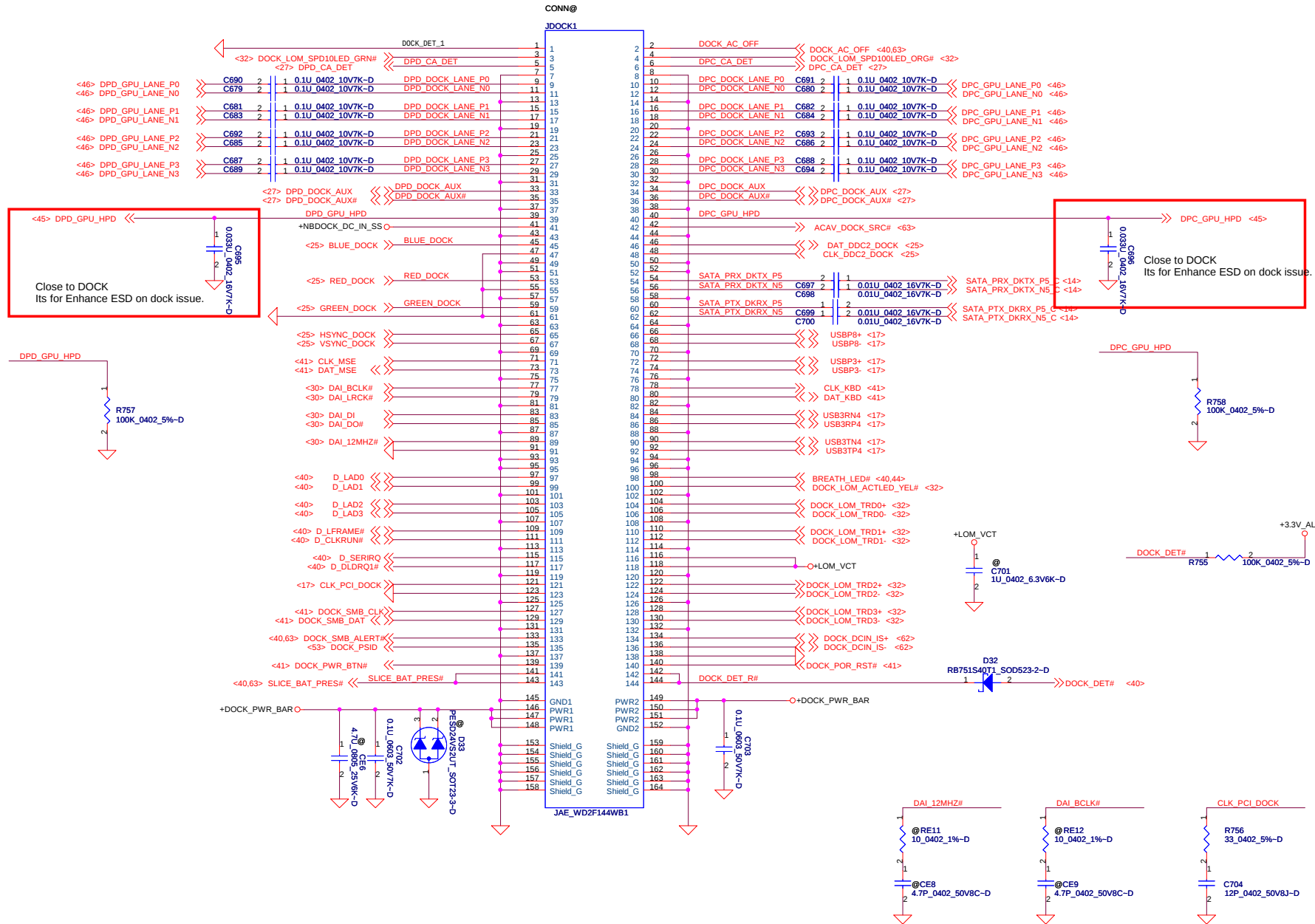
Compal Electronics, Inc.

Title	USP/ECATA/10/MDG
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USB/ESATA/IO/MDC		
Size	Document Number	Rev

Case	Document Number	Page
	LA-7782	0.1

Date:	Friday, June 10, 2011	Sheet	38	of	66
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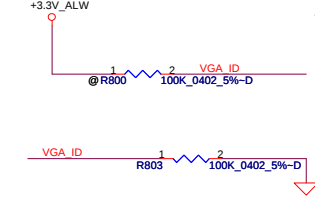
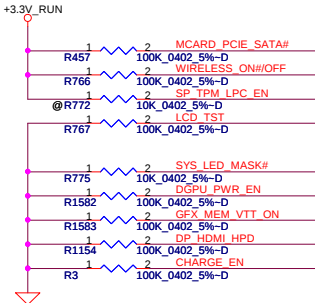
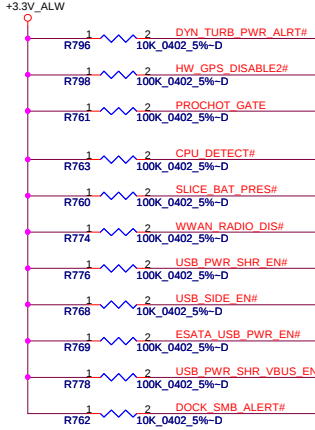
Compal Electronics, Inc.

DOCKING CONN

LA-7782

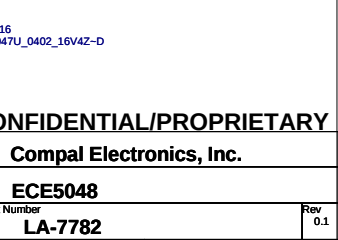
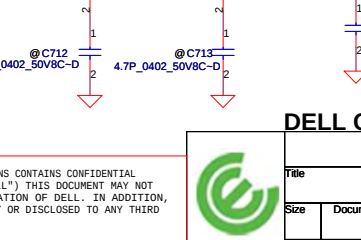
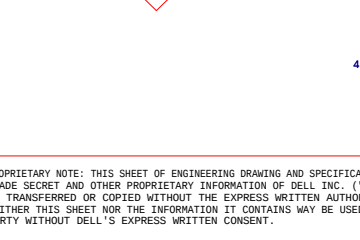
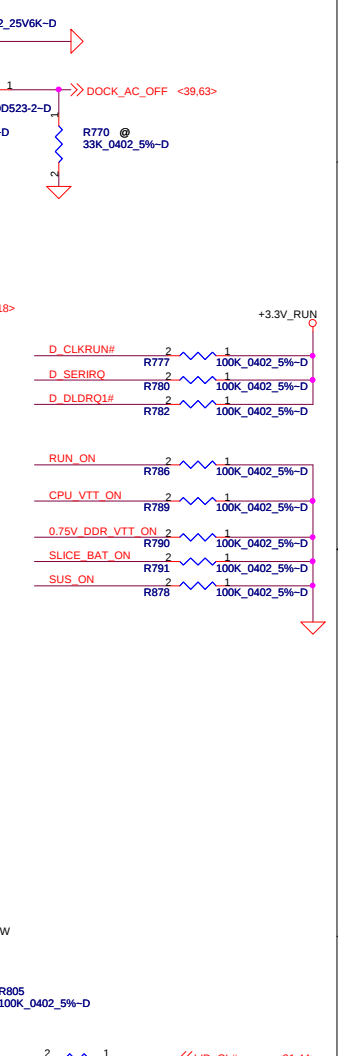
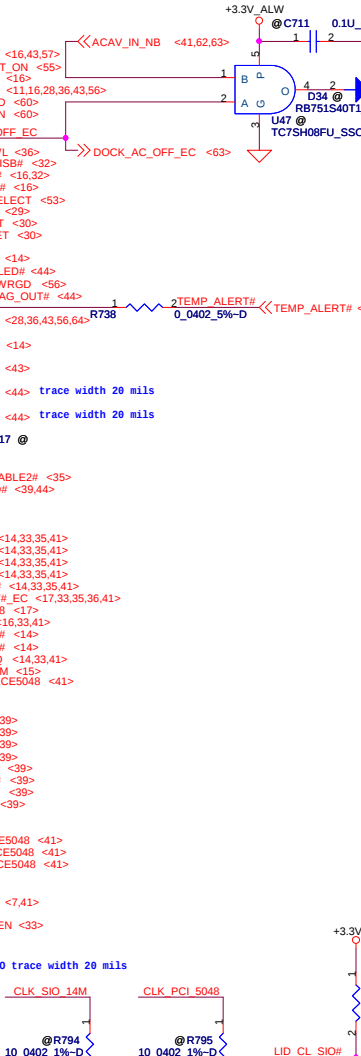
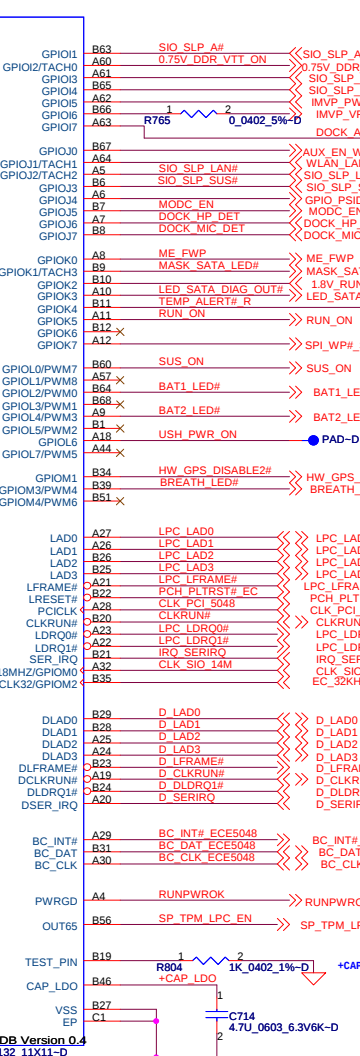
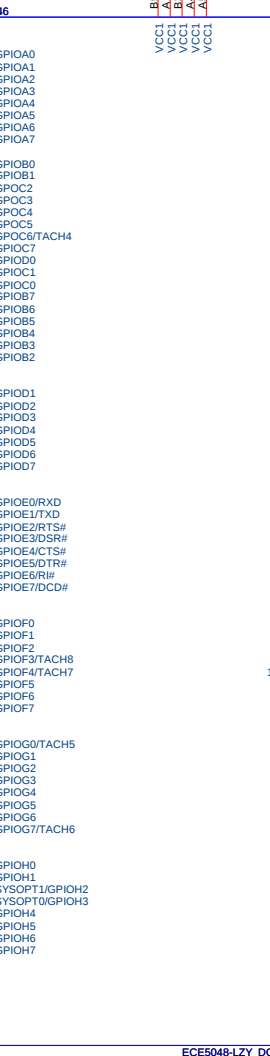
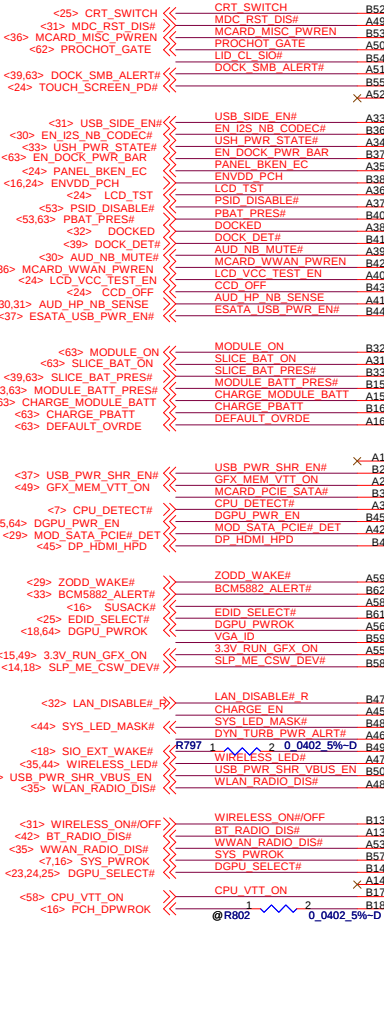
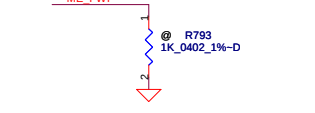
Rev 0.1

Size	Document Number	Rev
		0.1
Date	Friday, June 10, 2011	Sheet 39 of 66



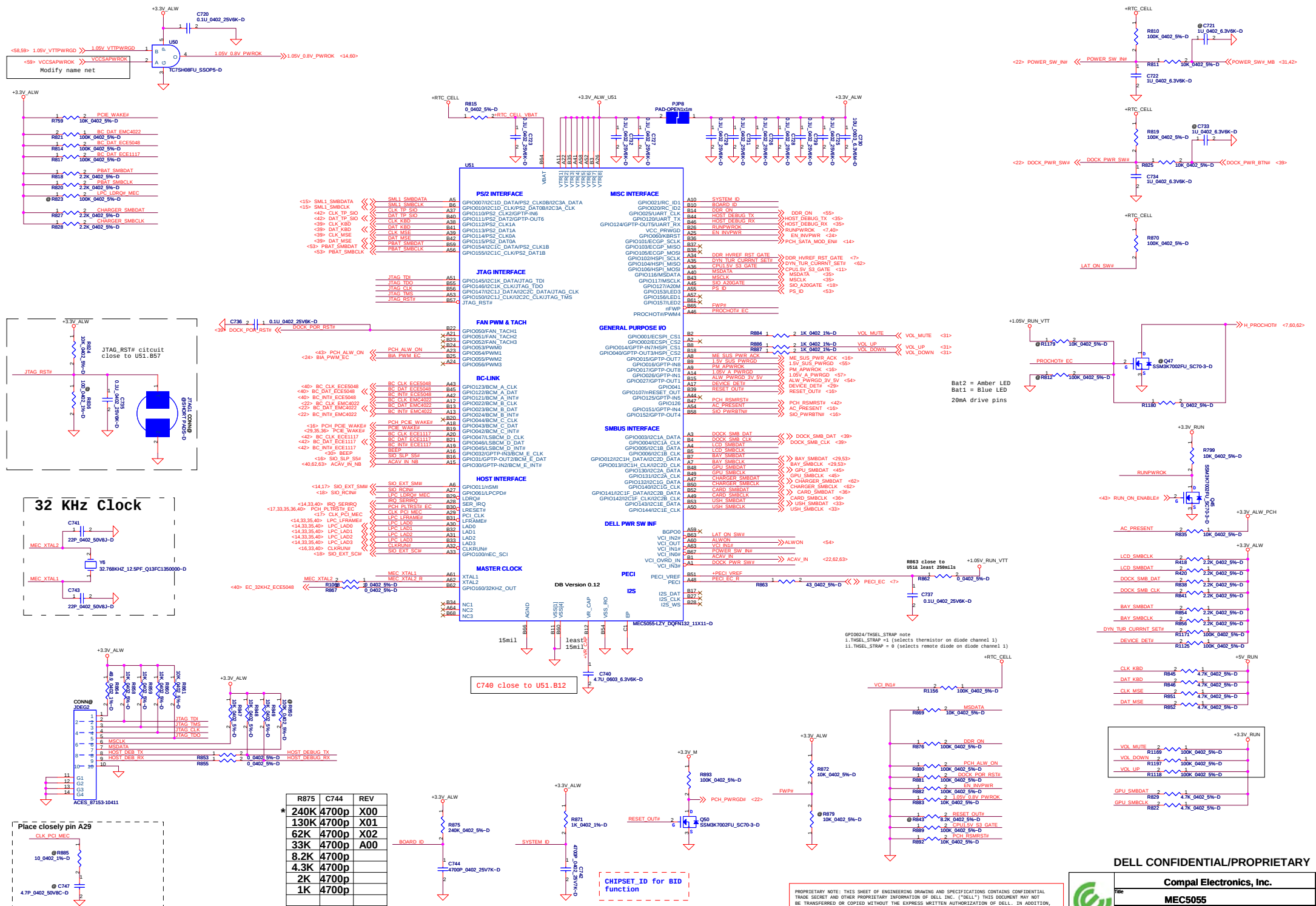
	VGA_ID0
Discrete	0
UMA	1

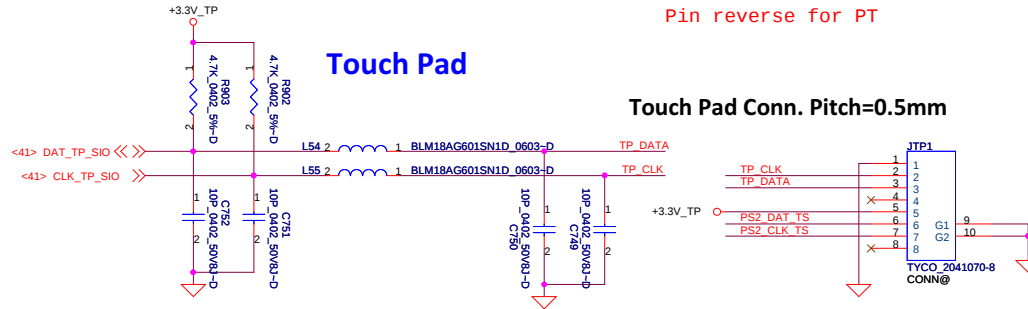
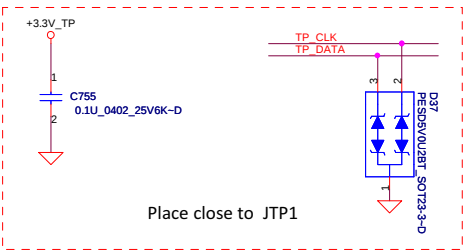
ME_FWP PCH has internal 20K PD.
(suspend power rail)



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Compel Electronics, Inc.			
Title			
ECE5048			
Size	Document Number	Rev	
	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	40 of 66

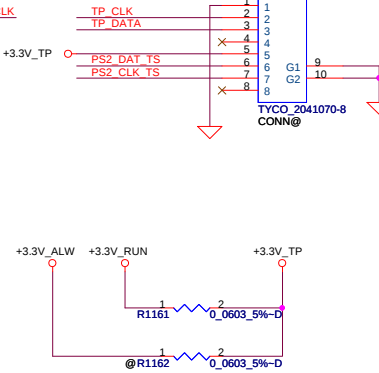
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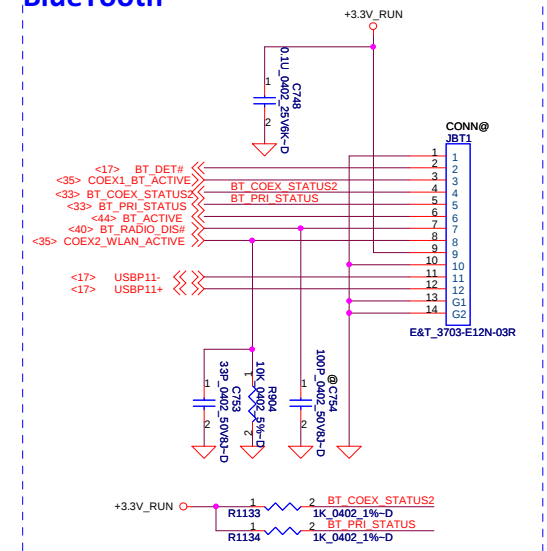


Pin reverse for PT

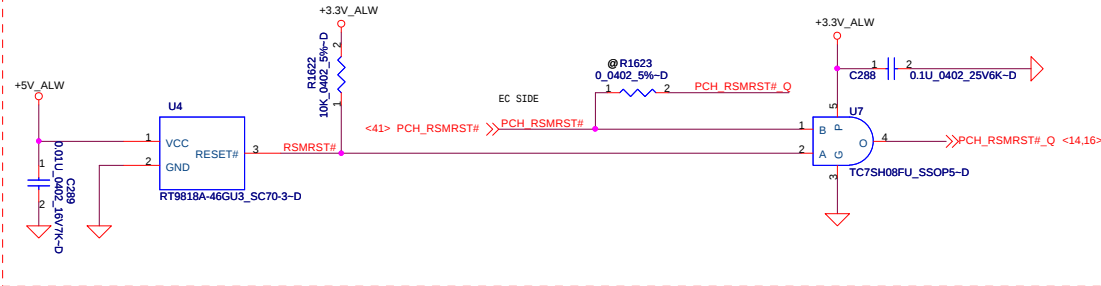
Touch Pad Conn. Pitch=0.5mm



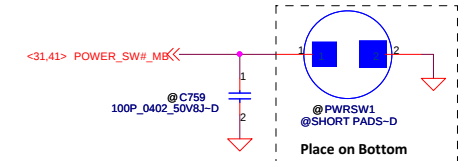
BlueTooth



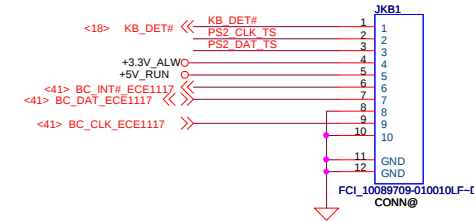
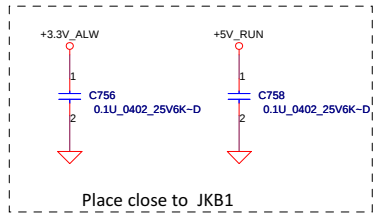
RSMRST circuit



Power Switch for debug



Change KB connector to same as JSC1
KB Conn. Pitch=1.0mm



Part Number	Description
DC280803Y8L	H-CONN SET ZJX MB-LCD 14 WGA+(-1ch)

Part Number	Description
GC28323W088	BATT C28322 2V 220MAH MAXCELL

Part Number	Description
DC28A080888	FAN SET DAQ28 DC5V AB7405HB-HB3 ADDA

Part Number	Description
PK238083Q8L	SPK PACK ZJX 2.0W 4 OHM FG

Part Number	Description
NB080808P8L	FFC 6P H P1 PAD=0.7 87.4MM MB-LED/B 0FD

Part Number	Description
NB080808S8L	FFC 12P G P.5 PAD.3 75MM MB-VOLUME/B 0FD

Part Number	Description
DC28C08188L	H-CONN SET 0FD MB-LCD CAM LED 2CHANNEL

Part Number	Description
DC381088N8	CONN SET 0FD DCJACK-MB WDMO-DC380804-0F

Part Number	Description
DC280814Z18	H-CONN SET 0FD M/B-BATTERY 9PIN

Part Number	Description
DC301088L8L	CONN SET 0FD MDC-RJ11

Part Number	Description
NB080808R8L	FFC BP F P8.5 PAD=0.3 130MM MB-TP/B 0FD

Part Number	Description
SP070807V8L	S SOCKET TYCO 1770551-1 18P H5.9 SMART

Part Number	Description
DC280814Y8L	H-CONN SET 0FD MB-BT

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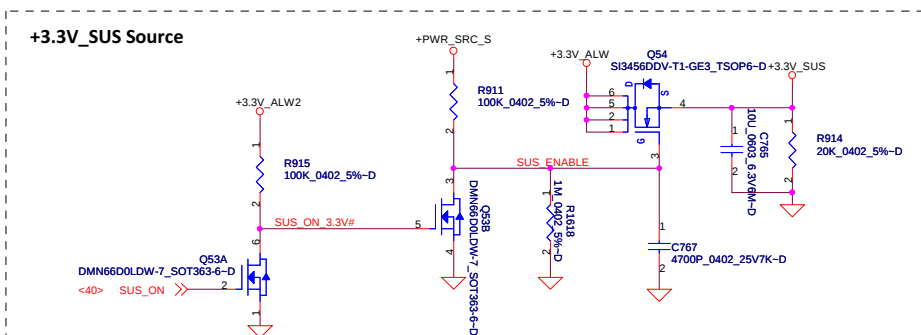
TP/KB/BT/FAN/RESET

LA-7782

Rev 0.1

Date: Friday, June 10, 2011 Sheet 42 of 66

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[illegible][illegible]

Discharge Circuit

The diagram illustrates the discharge paths for various power rails. The circuit is divided into two sections by a dashed line. The left section shows the discharge paths for +3.3V_SUS, +3.3V_ALW_PCH, +5V_RUN, +1.5V_RUN, +3.3V_RUN, +1.05V_RUN, +1.5V_CPU_VDDQ, and +0.75V_DDR_VTT. The right section shows the discharge paths for +3.3V_ALW_PCH, +5V_RUN, +1.5V_RUN, +3.3V_RUN, +1.05V_RUN, +1.5V_CPU_VDDQ, and +0.75V_DDR_VTT. The diagram is labeled 'Discharge Circuit' at the top.

The schematic diagram illustrates the power management section of the NTGS4141INT1G-TSOP6-D. It features three regulated power sources: +1.05V_RUN, +3.3V_RUN, and +5V_RUN. The +1.05V_RUN source is derived from +PWR_SRC_S through a MOSFET (Q63) and a resistor network (R930, R931). The +3.3V_RUN source is derived from +3.3V_ALW through a MOSFET (Q64) and a resistor network (R916, R913). The +5V_RUN source is derived from +5V_ALW through a MOSFET (Q52A) and a resistor network (R910, R911). The diagram also shows control signals like RUN_ON_ENABLE# and SIO_SLP_S3# and various passive components like resistors (R908, R920, R921, R930, R931, R916, R913, R910, R735, R744, R749, R747, R746) and capacitors (C771, C769, C772, C773, C1199, C1197, C1198, C764).

+1.05V_RUN Source

+3.3V_RUN Source

+5V_RUN Source

270P_0402_50V7K-D

5V

SLG59M232VTR

VIN2

VOUT2

VOUT2

GPAD

+5V_RUN

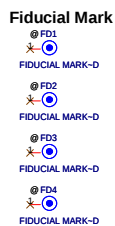
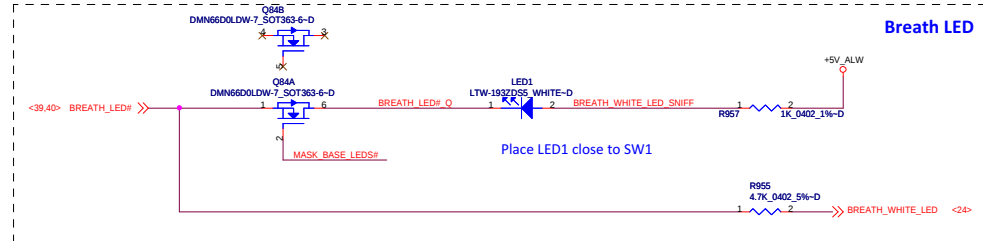
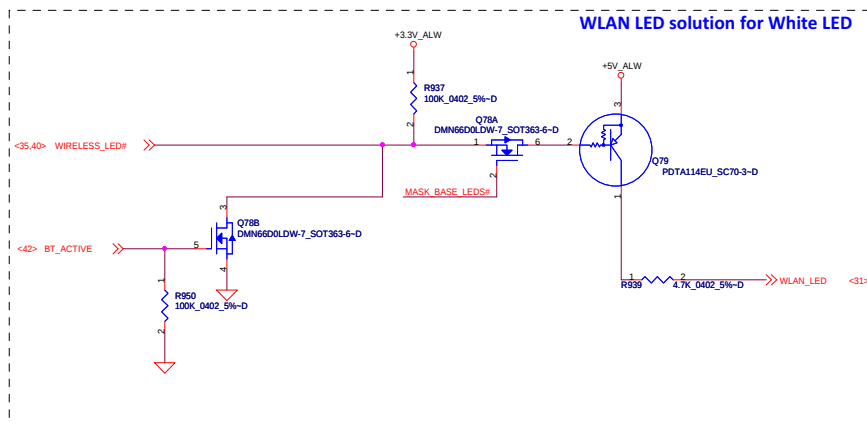
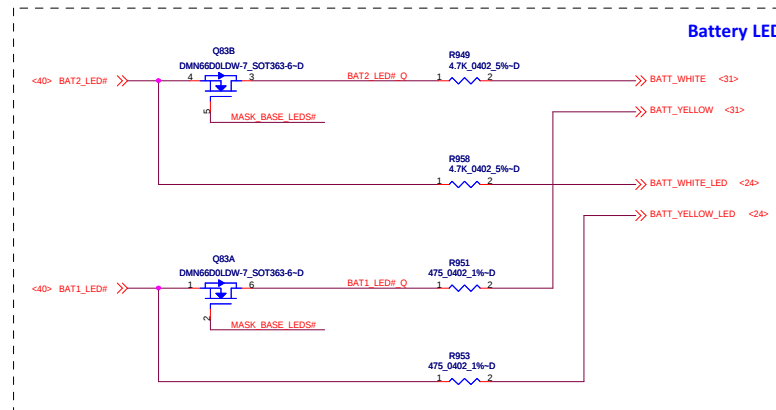
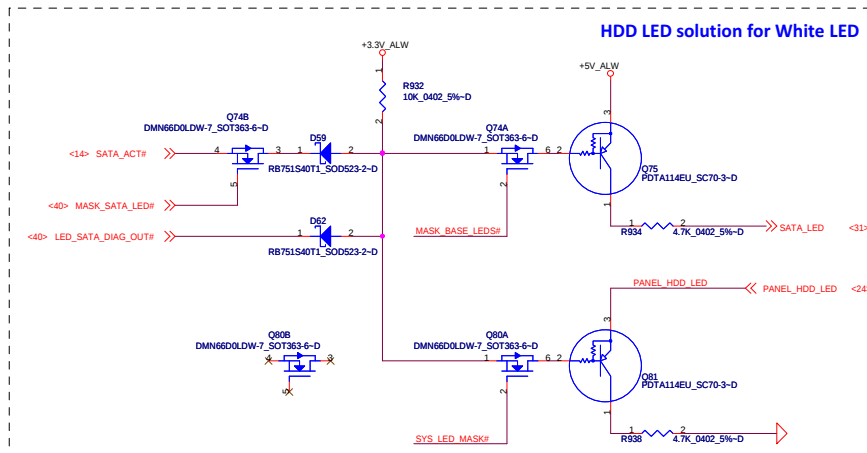
C761

0.1u 0402 25V16K-D

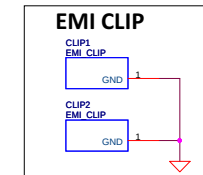
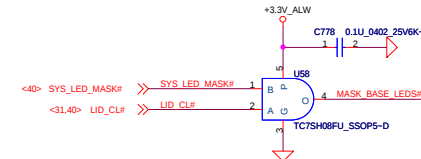
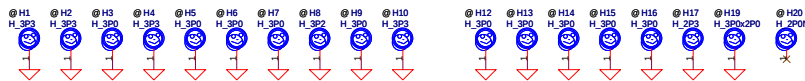
R910

20K_0402_5%-D

		DELL CONFIDENTIAL/PROPRIETARY	
		Compal Electronics, Inc.	
		POWER CONTROL	
		LA-7782	
Title		Rev 0.1	
Size		Document Number	
Date		Sheet	
Friday, June 30, 2011		43 of 66	



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



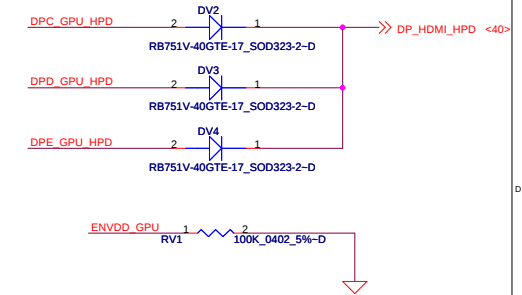
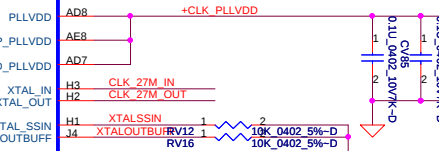
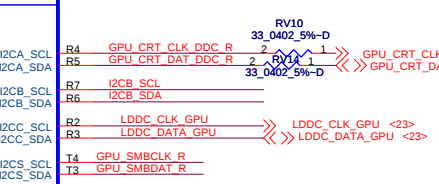
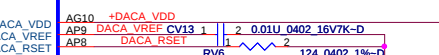
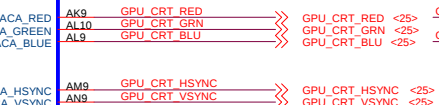
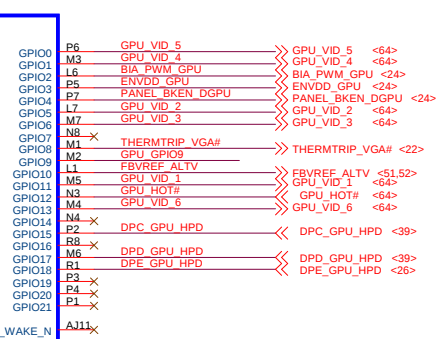
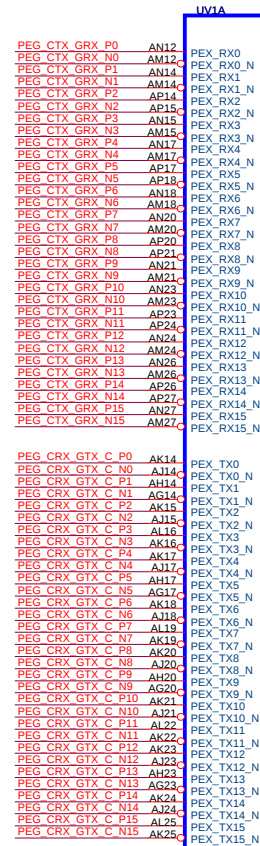
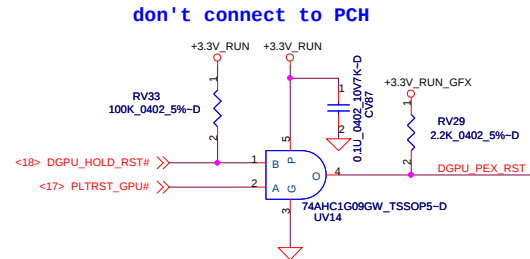
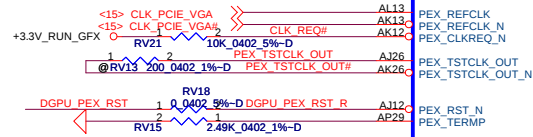
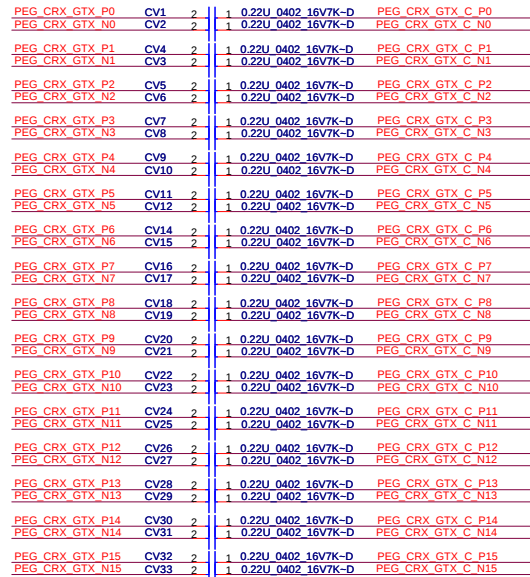
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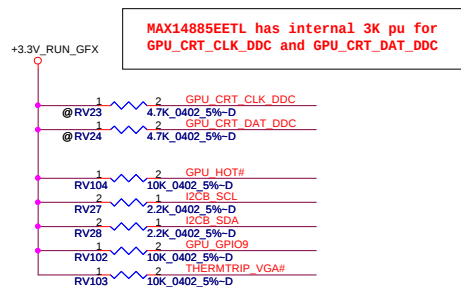
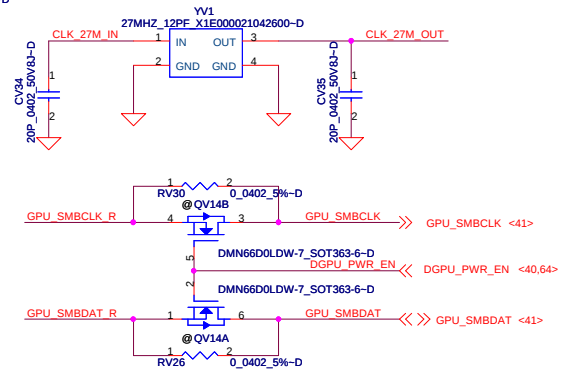
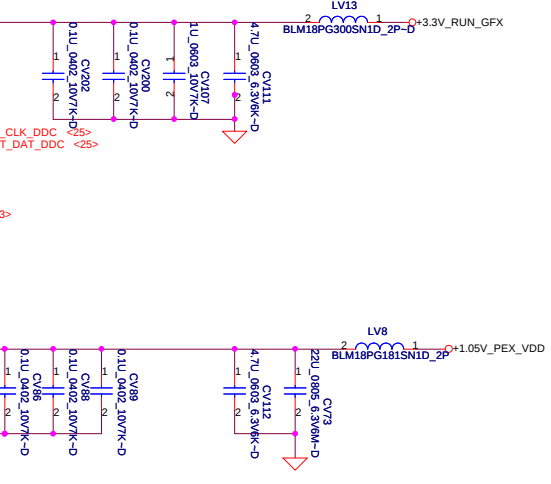
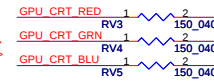
PAD and Standoff

Size: Document Number LA-7782 Rev 0.1
Date: Friday, June 10, 2011 Sheet 44 of 66

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Close to GPU



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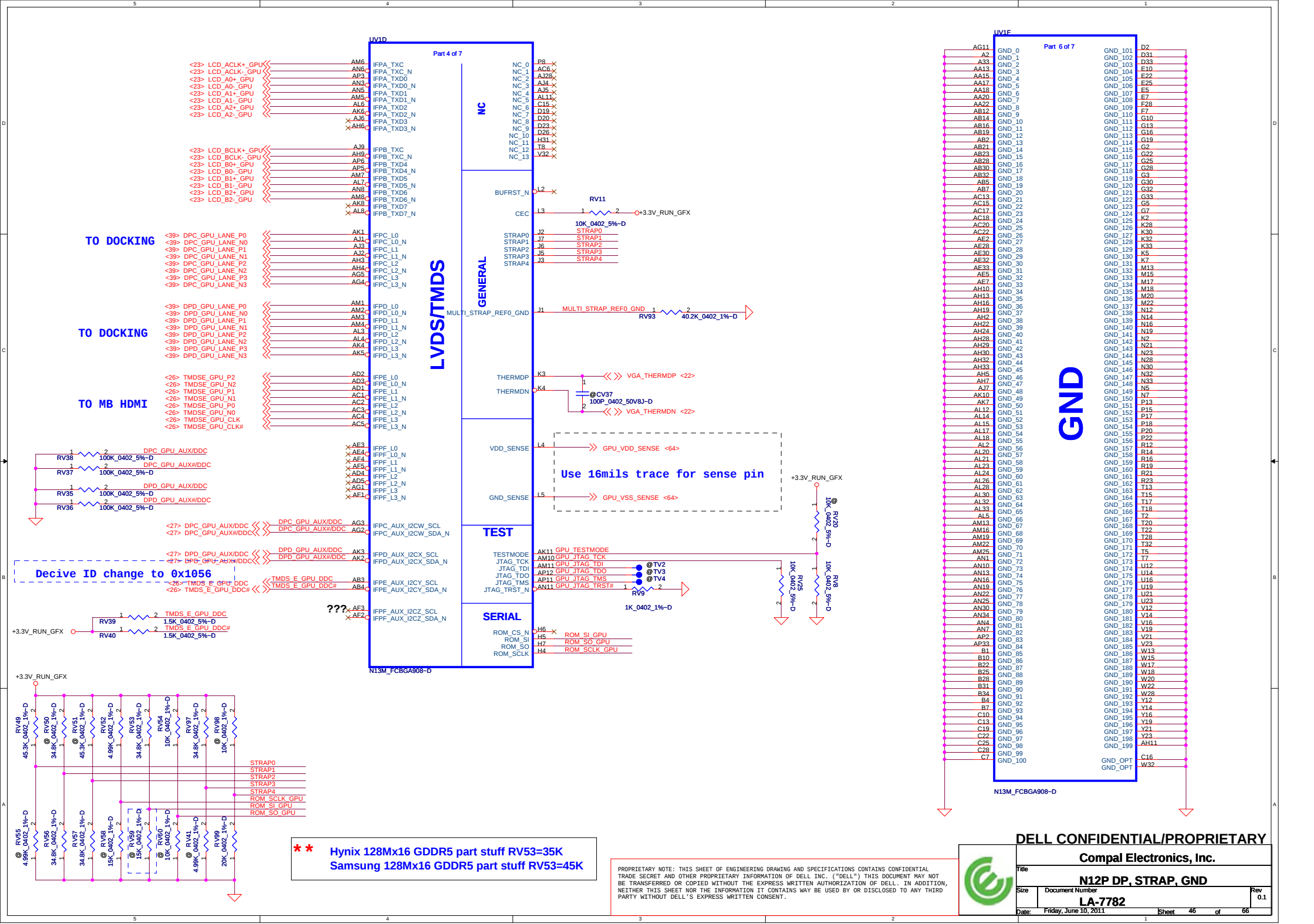
N12P PCIE,I2C,DAC,GPIO

LA-7782

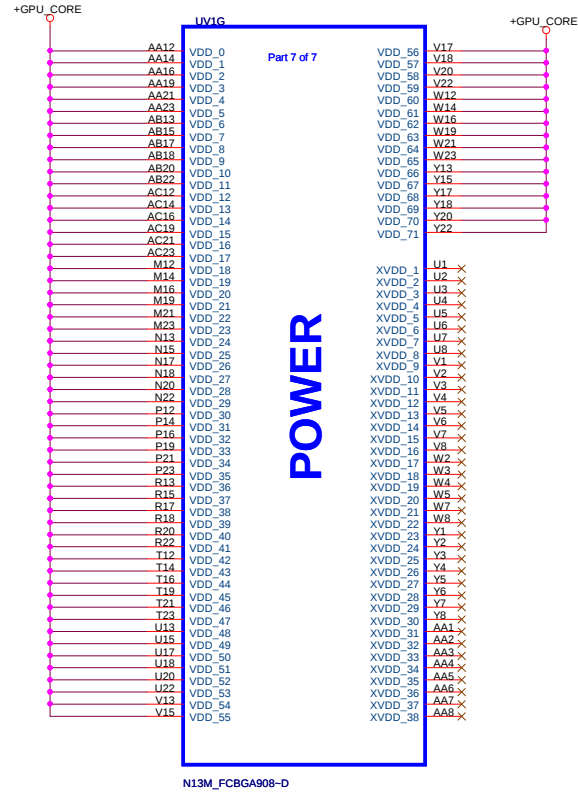
Date: Friday, June 10, 2011	Sheet 45 of 66
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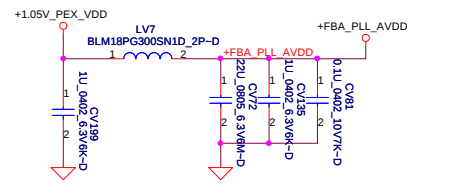
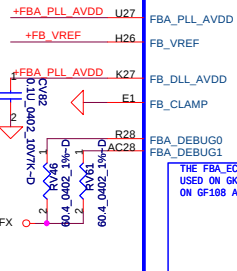
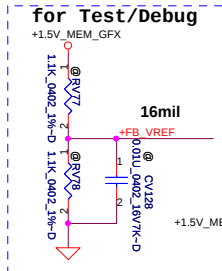
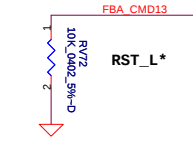
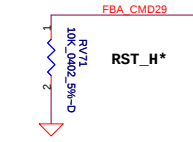
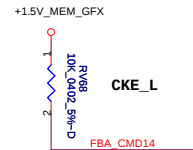
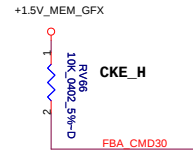
Caps on Power Side



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FBA_D[0..63] <>> FBA_D[0..63] <51,52>
FBA_CMD[0..31] <>> FBA_CMD[0..31] <51,52>
FBA_DB[0..7] <>> FBA_DB[0..7] <51,52>
FBA_EDC[0..7] <>> FBA_EDC[0..7] <51,52>



Part 2 of 7

FBA_D0	L28	FBA_D00
FBA_D1	M29	FBA_D01
FBA_D2	L29	FBA_D02
FBA_D3	M28	FBA_D03
FBA_D4	N31	FBA_D04
FBA_D5	P29	FBA_D05
FBA_D6	R29	FBA_D06
FBA_D7	P28	FBA_D07
FBA_D8	J28	FBA_D08
FBA_D9	H29	FBA_D09
FBA_D10	J29	FBA_D10
FBA_D11	H28	FBA_D11
FBA_D12	G29	FBA_D12
FBA_D13	E31	FBA_D13
FBA_D14	E32	FBA_D14
FBA_D15	F30	FBA_D15
FBA_D16	C34	FBA_D16
FBA_D17	D32	FBA_D17
FBA_D18	D32	FBA_D18
FBA_D19	C33	FBA_D19
FBA_D20	F33	FBA_D20
FBA_D21	F32	FBA_D21
FBA_D22	H33	FBA_D22
FBA_D23	H32	FBA_D23
FBA_D24	P34	FBA_D24
FBA_D25	P32	FBA_D25
FBA_D26	P31	FBA_D26
FBA_D27	P33	FBA_D27
FBA_D28	L31	FBA_D28
FBA_D29	L34	FBA_D29
FBA_D30	L32	FBA_D30
FBA_D31	L33	FBA_D31
FBA_D32	AG28	FBA_D32
FBA_D33	AF29	FBA_D33
FBA_D34	AG29	FBA_D34
FBA_D35	AF28	FBA_D35
FBA_D36	AD30	FBA_D36
FBA_D37	AD29	FBA_D37
FBA_D38	AC29	FBA_D38
FBA_D39	AD28	FBA_D39
FBA_D40	AJ29	FBA_D40
FBA_D41	AK29	FBA_D41
FBA_D42	AJ30	FBA_D42
FBA_D43	AK28	FBA_D43
FBA_D44	AM29	FBA_D44
FBA_D45	AM31	FBA_D45
FBA_D46	AN29	FBA_D46
FBA_D47	AM30	FBA_D47
FBA_D48	AN31	FBA_D48
FBA_D49	AN32	FBA_D49
FBA_D50	AP30	FBA_D50
FBA_D51	AP32	FBA_D51
FBA_D52	AM33	FBA_D52
FBA_D53	AL31	FBA_D53
FBA_D54	AK33	FBA_D54
FBA_D55	AK32	FBA_D55
FBA_D56	AD34	FBA_D56
FBA_D57	AD32	FBA_D57
FBA_D58	AC30	FBA_D58
FBA_D59	AD33	FBA_D59
FBA_D60	AF31	FBA_D60
FBA_D61	AG34	FBA_D61
FBA_D62	AG32	FBA_D62
FBA_D63	AG33	FBA_D63

MEMORY INTERFACE

FBA_CMD0	U30	FBA_CMD0
FBA_CMD1	F31	FBA_CMD1
FBA_CMD2	U29	FBA_CMD2
FBA_CMD3	R34	FBA_CMD3
FBA_CMD4	R33	FBA_CMD4
FBA_CMD5	U32	FBA_CMD5
FBA_CMD6	U33	FBA_CMD6
FBA_CMD7	U28	FBA_CMD7
FBA_CMD8	V29	FBA_CMD8
FBA_CMD9	V30	FBA_CMD9
FBA_CMD10	U34	FBA_CMD10
FBA_CMD11	U31	FBA_CMD11
FBA_CMD12	V34	FBA_CMD12
FBA_CMD13	V33	FBA_CMD13
FBA_CMD14	Y32	FBA_CMD14
FBA_CMD15	AA31	FBA_CMD15
FBA_CMD16	AA29	FBA_CMD16
FBA_CMD17	AA28	FBA_CMD17
FBA_CMD18	AC34	FBA_CMD18
FBA_CMD19	AC33	FBA_CMD19
FBA_CMD20	AA32	FBA_CMD20
FBA_CMD21	Y28	FBA_CMD21
FBA_CMD22	Y29	FBA_CMD22
FBA_CMD23	W31	FBA_CMD23
FBA_CMD24	X30	FBA_CMD24
FBA_CMD25	AA34	FBA_CMD25
FBA_CMD26	Y31	FBA_CMD26
FBA_CMD27	Y34	FBA_CMD27
FBA_CMD28	Y33	FBA_CMD28
FBA_CMD29	Y31	FBA_CMD29
FBA_CMD30	Y33	FBA_CMD30
FBA_CMD31	Y31	FBA_CMD31

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FBA_DQM1	F31	FBA_DQM1
FBA_DQM2	M32	FBA_DQM2
FBA_DQM3	AD31	FBA_DQM3
FBA_DQM4	AL29	FBA_DQM4
FBA_DQM5	AM32	FBA_DQM5
FBA_DQM6	AE34	FBA_DQM6
FBA_DQM7	AE34	FBA_DQM7

FBA_DQS_RN0	M30	FBA_DQS_RN0
FBA_DQS_RN1	E34	FBA_DQS_RN1
FBA_DQS_RN2	M34	FBA_DQS_RN2
FBA_DQS_RN3	AE30	FBA_DQS_RN3
FBA_DQS_RN4	AK31	FBA_DQS_RN4
FBA_DQS_RN5	AM34	FBA_DQS_RN5
FBA_DQS_RN6	AE34	FBA_DQS_RN6
FBA_DQS_RN7	AE34	FBA_DQS_RN7

FBA_DQS_WP0	M31	FBA_DQS_WP0
FBA_DQS_WP1	E33	FBA_DQS_WP1
FBA_DQS_WP2	M33	FBA_DQS_WP2
FBA_DQS_WP3	AE31	FBA_DQS_WP3
FBA_DQS_WP4	AK30	FBA_DQS_WP4
FBA_DQS_WP5	AN33	FBA_DQS_WP5
FBA_DQS_WP6	AE33	FBA_DQS_WP6
FBA_DQS_WP7	AE33	FBA_DQS_WP7

FBA_CMD_RFU0	R32	FBA_CMD_RFU0
FBA_CMD_RFU1	AC34	FBA_CMD_RFU1

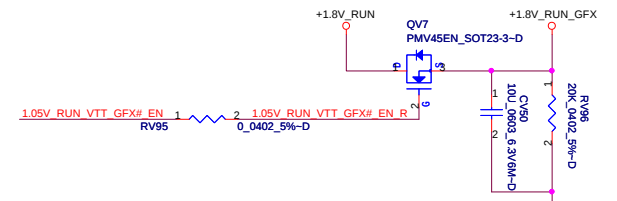
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FBA_WCK01	K31	FBA_WCK01
FBA_WCK01_N	L30	FBA_WCK01_N
FBA_WCK02	H34	FBA_WCK02
FBA_WCK02_N	J34	FBA_WCK02_N
FBA_WCK03	AG30	FBA_WCK03
FBA_WCK03_N	AG31	FBA_WCK03_N
FBA_WCK04	AJ34	FBA_WCK04
FBA_WCK04_N	AK34	FBA_WCK04_N
FBA_WCK05	F31	FBA_WCK05
FBA_WCK05_N	F32	FBA_WCK05_N
FBA_WCK06	F33	FBA_WCK06
FBA_WCK06_N	F34	FBA_WCK06_N
FBA_WCK07	F35	FBA_WCK07
FBA_WCK07_N	F36	FBA_WCK07_N

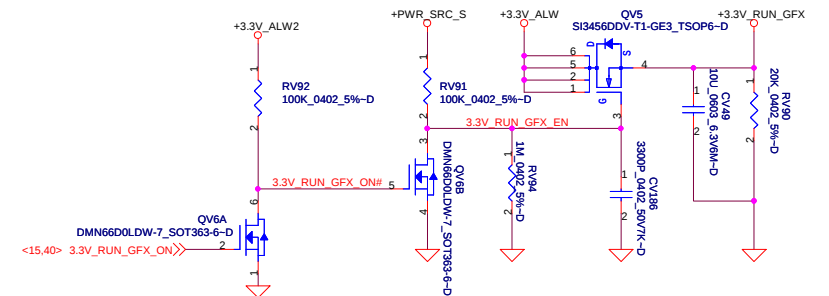
GDDR5 CMD Mapping Table

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CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD12	WE#
CMD0	CMD16	CS#
CMD8	CMD24	AB1#
CMD10	CMD26	A0 A10
CMD11	CMD27	A1 A9
CMD2	CMD18	A2 BA0
CMD1	CMD17	A3 BA3
CMD3	CMD19	A4 BA2
CMD4	CMD20	A5 BA1
CMD7	CMD23	A6 A11
CMD6	CMD22	A7 A8
CMD9	CMD25	A12 FRU
CMD14	CMD29	CKE#
CMD13	CMD29	RESET#

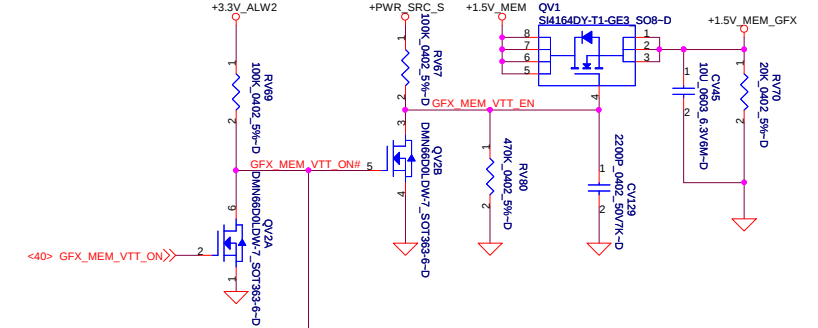
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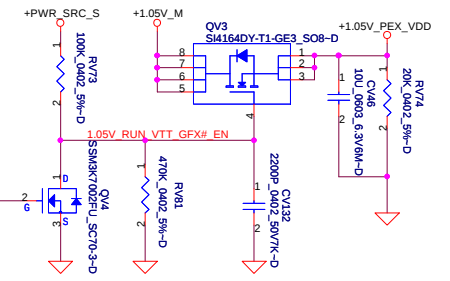
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+1.5V_MEM_GFX Source



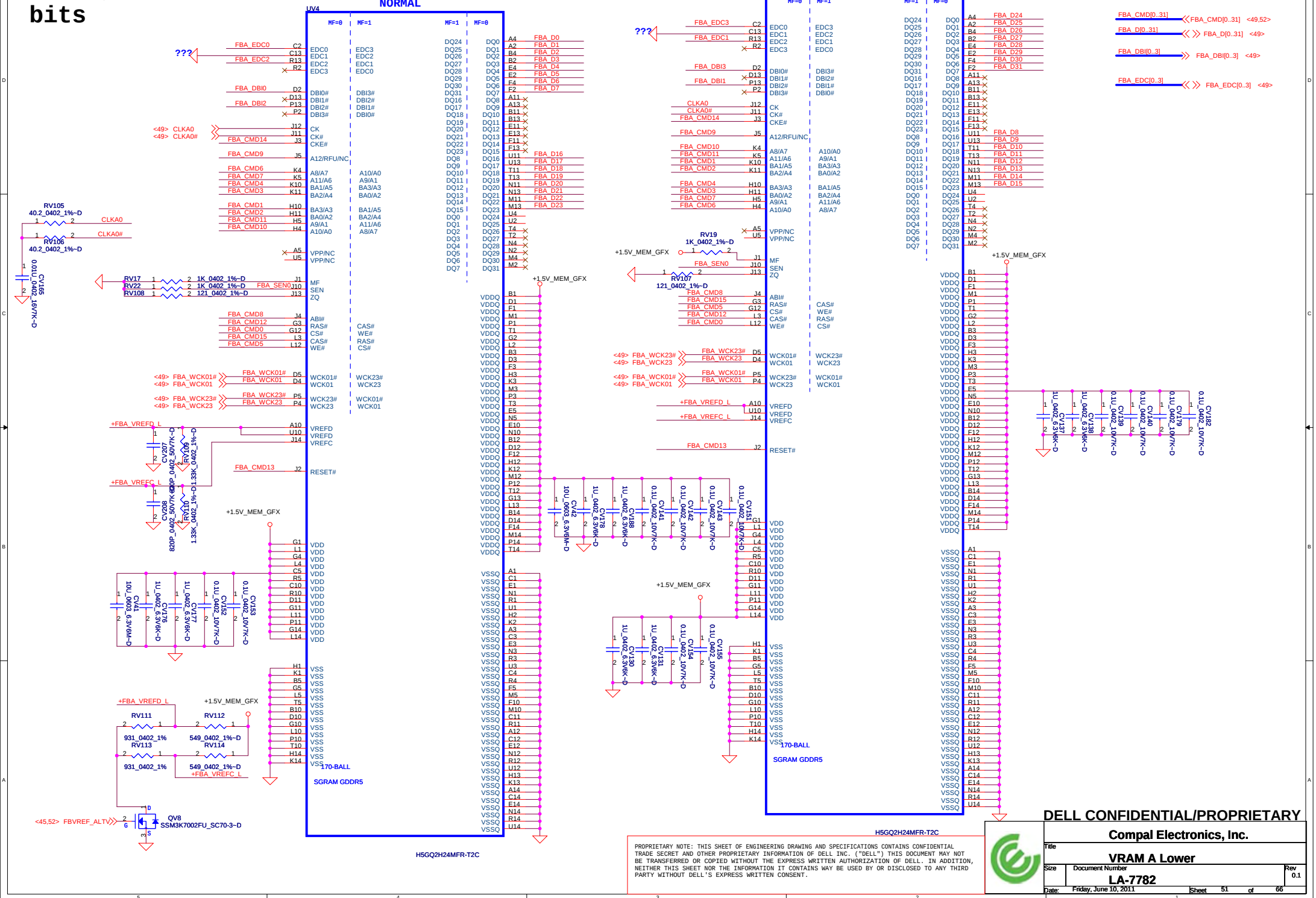
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N12P Memory			
Size	Document Number	Rev	
LA-7782		0.1	
Date	Friday, June 10, 2011	Sheet	49 of 66

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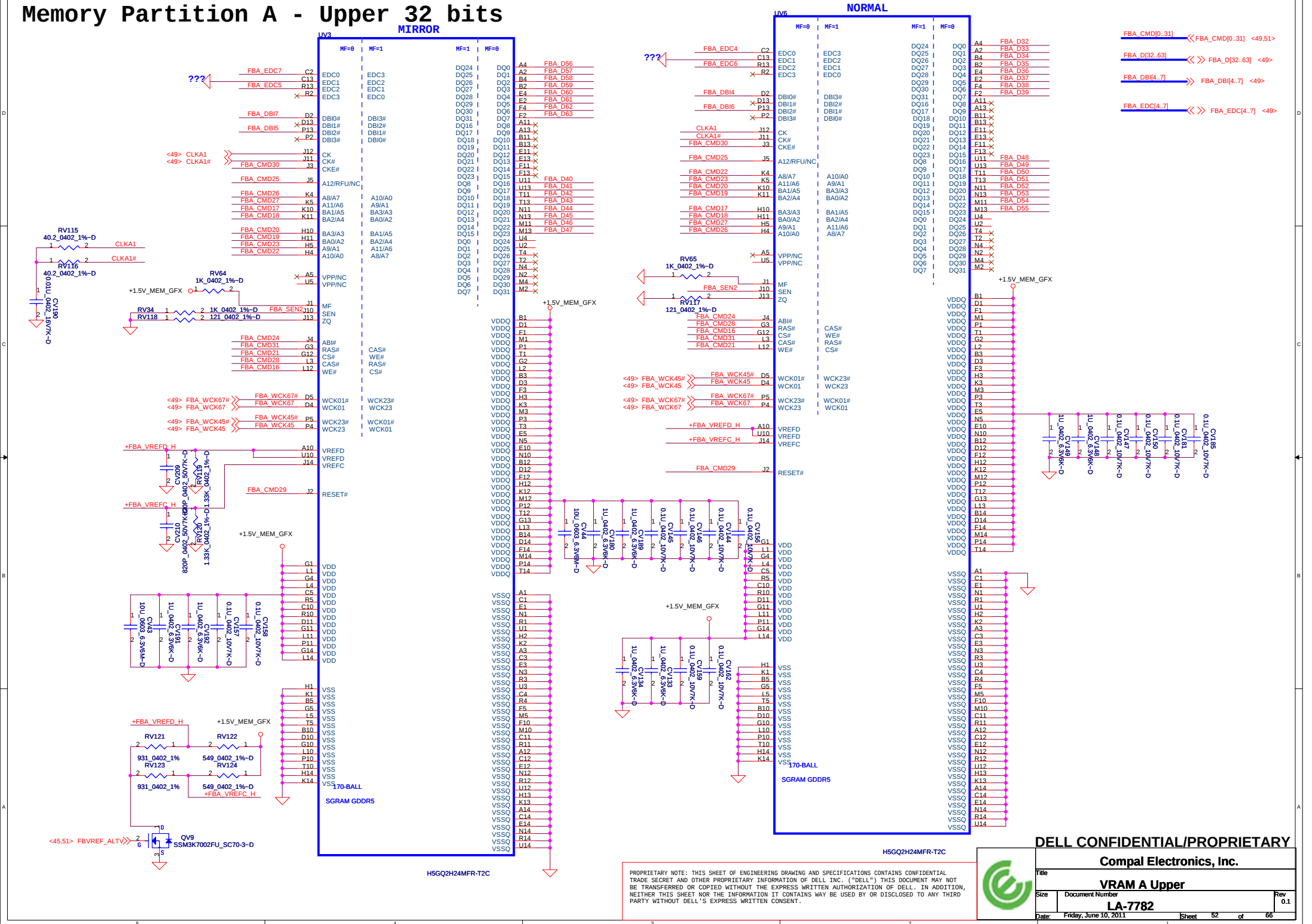
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LA-7782

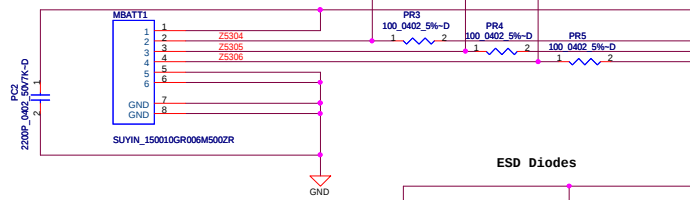
Date: Friday, June 10, 2011 Sheet 51 of 66

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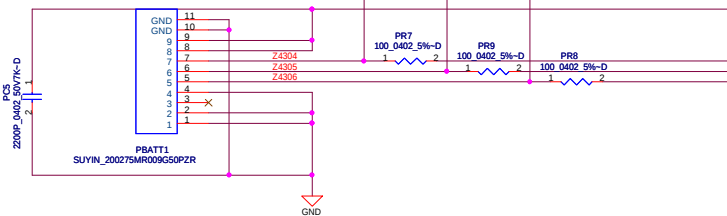
Memory Partition A - Upper 32 bits



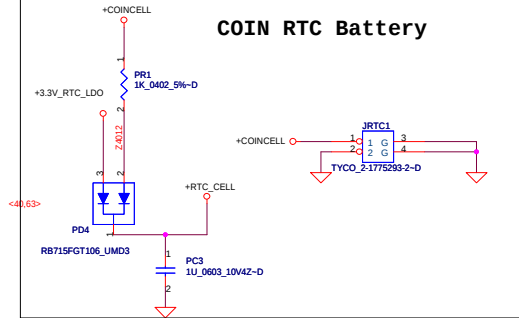
Media Bay Battery Connector



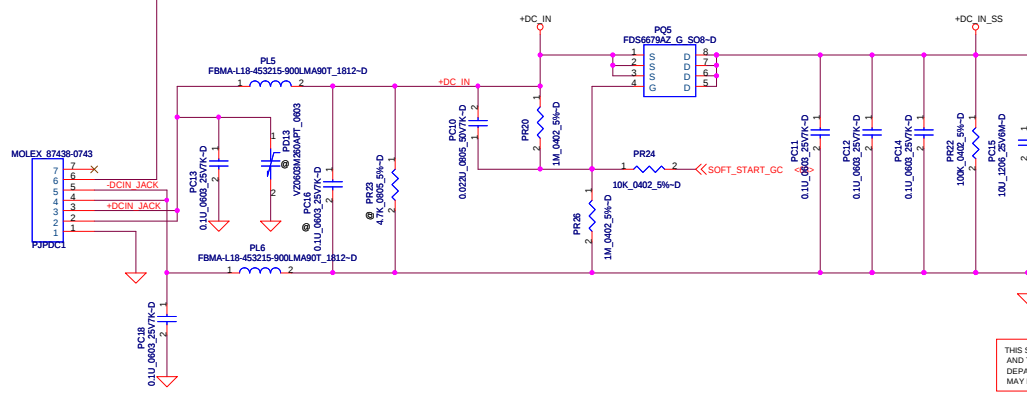
Primary Battery Connector



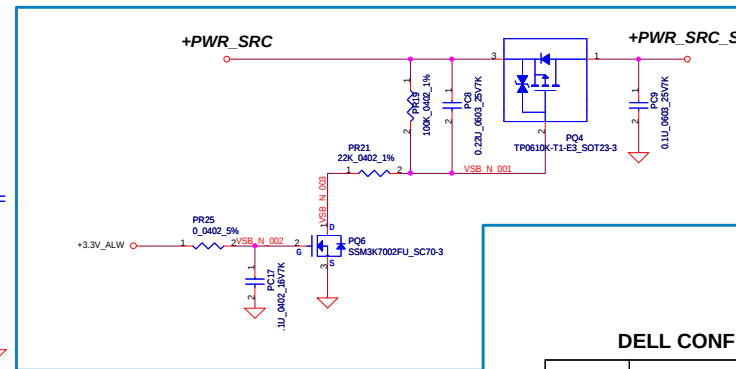
COIN RTC Battery



DC_IN+ Source



+PWR_SRC

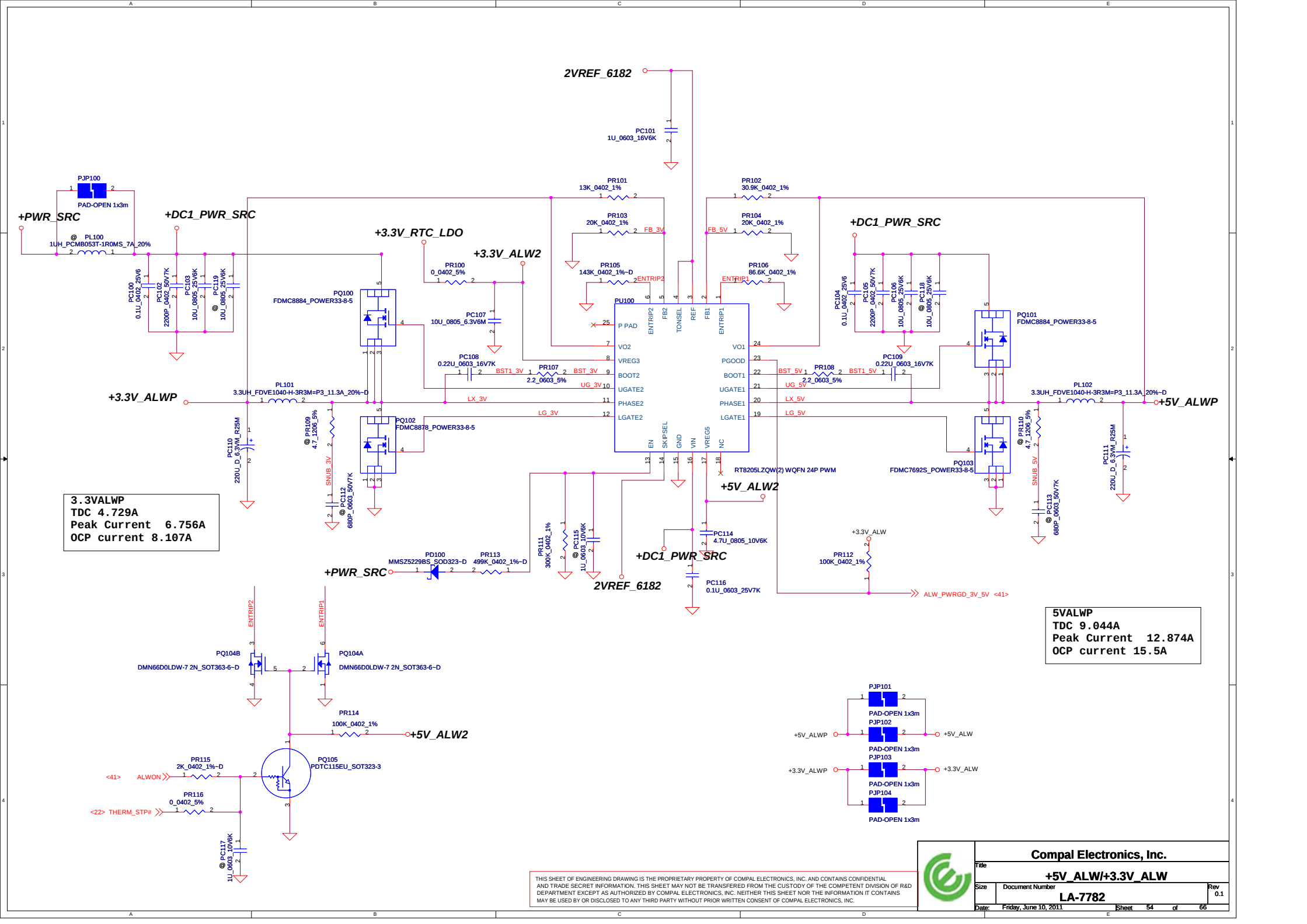


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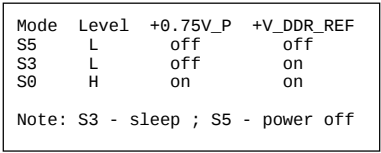


Compal Electronics, Inc.			
Title	+DCIN		
Size	Document Number	LA-7782	Rev 0.1
Date	Friday, June 10, 2011	Sheet 53	of 66

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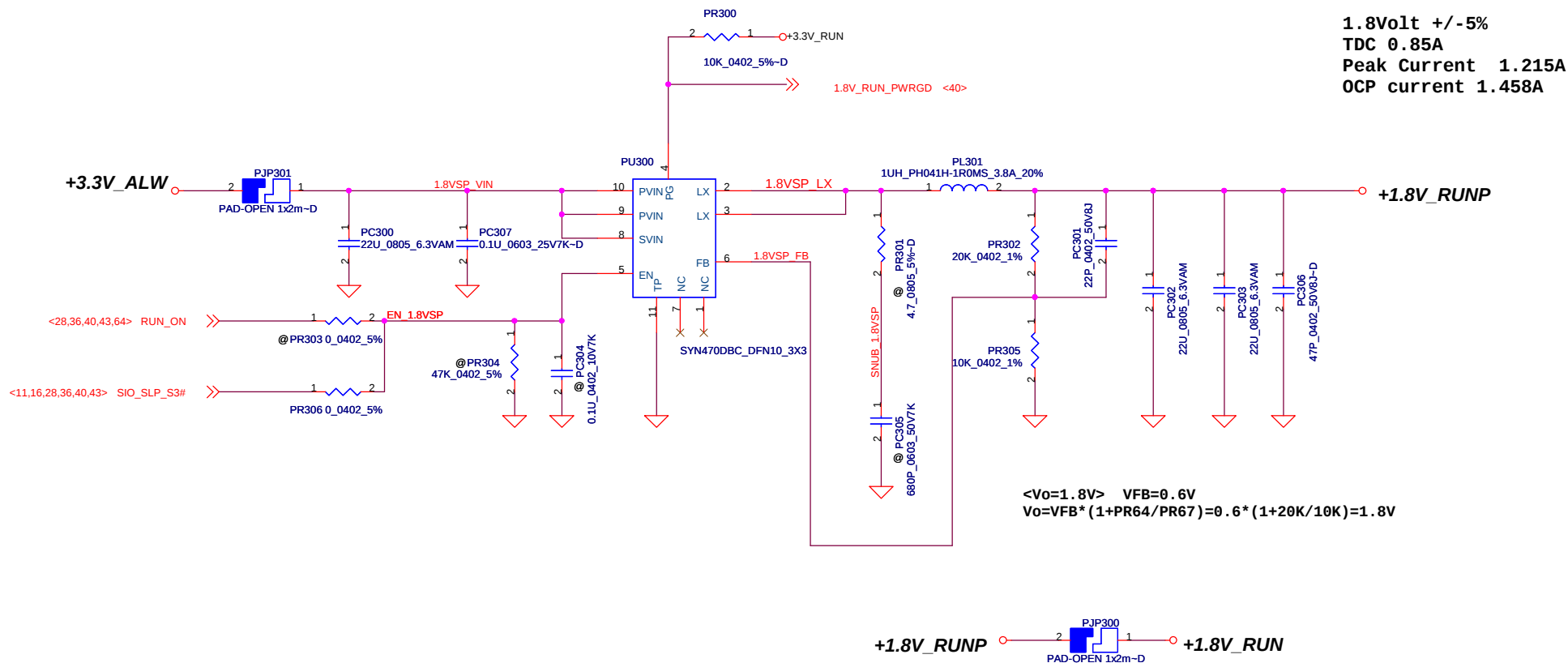


0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



Sheet 55 of 66

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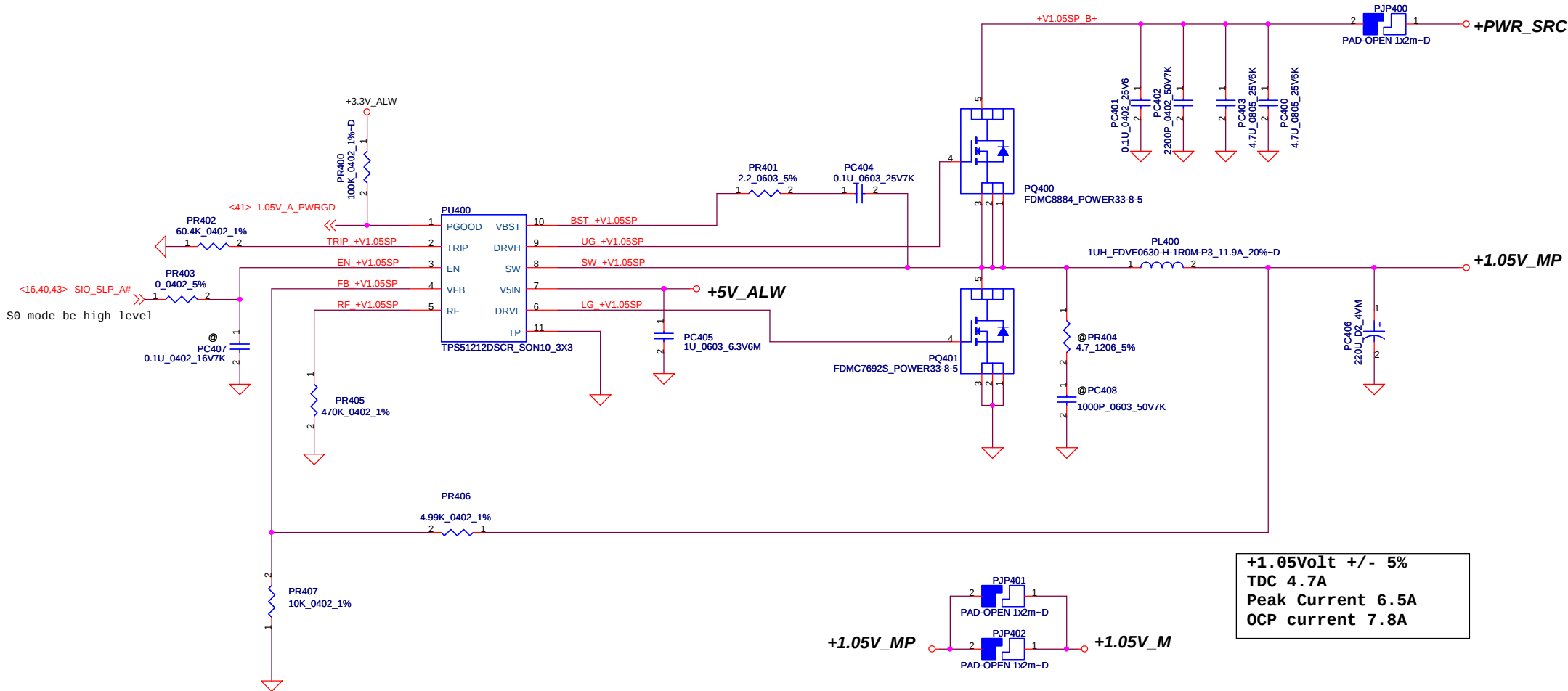


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Compal Electronics, Inc.			
Title		+1.8V_RUN	
Size	Document Number		Rev
	LA-7782		0.1
Date:	Friday, June 10, 2011		Sheet 56 of 66

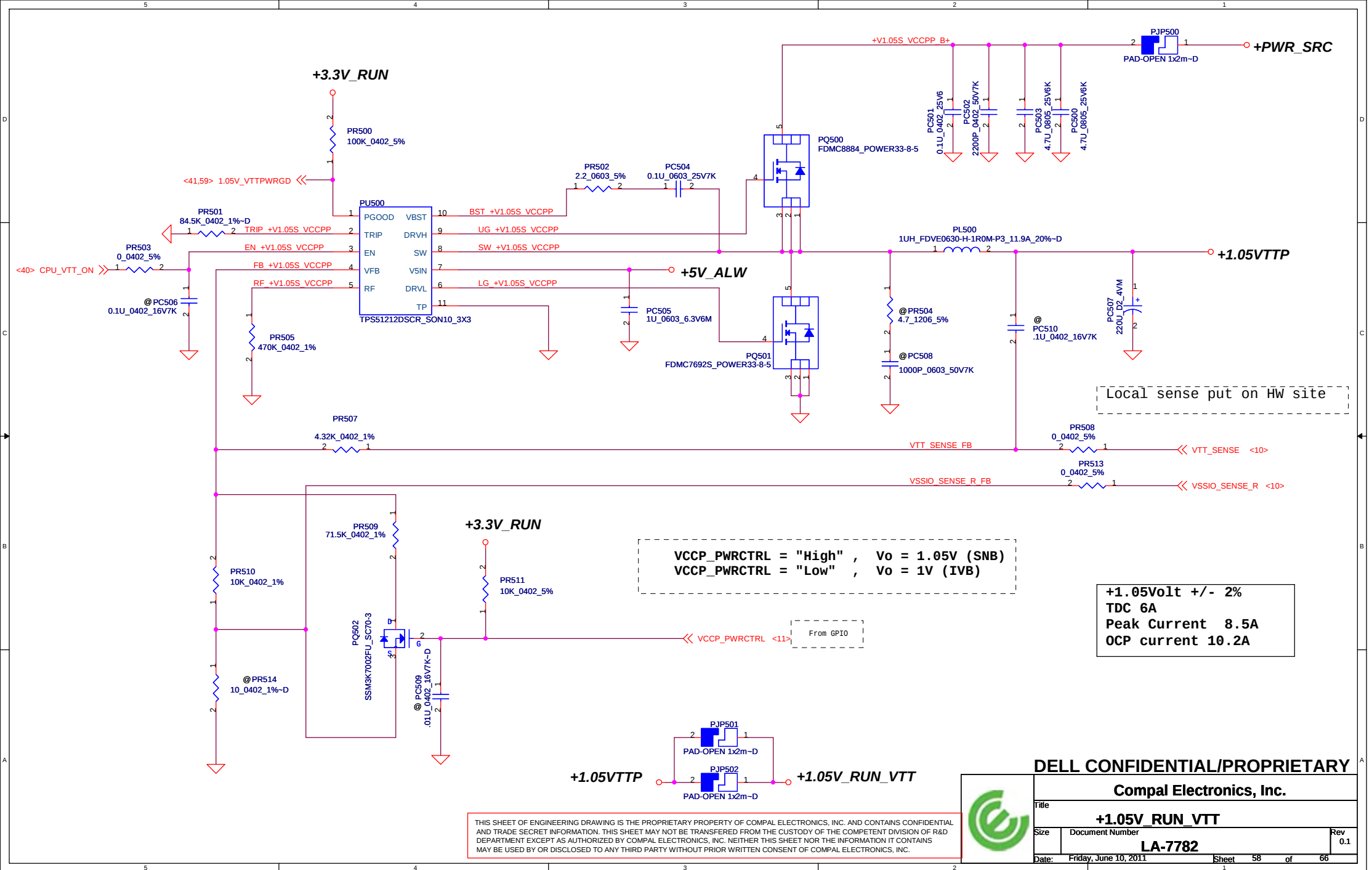


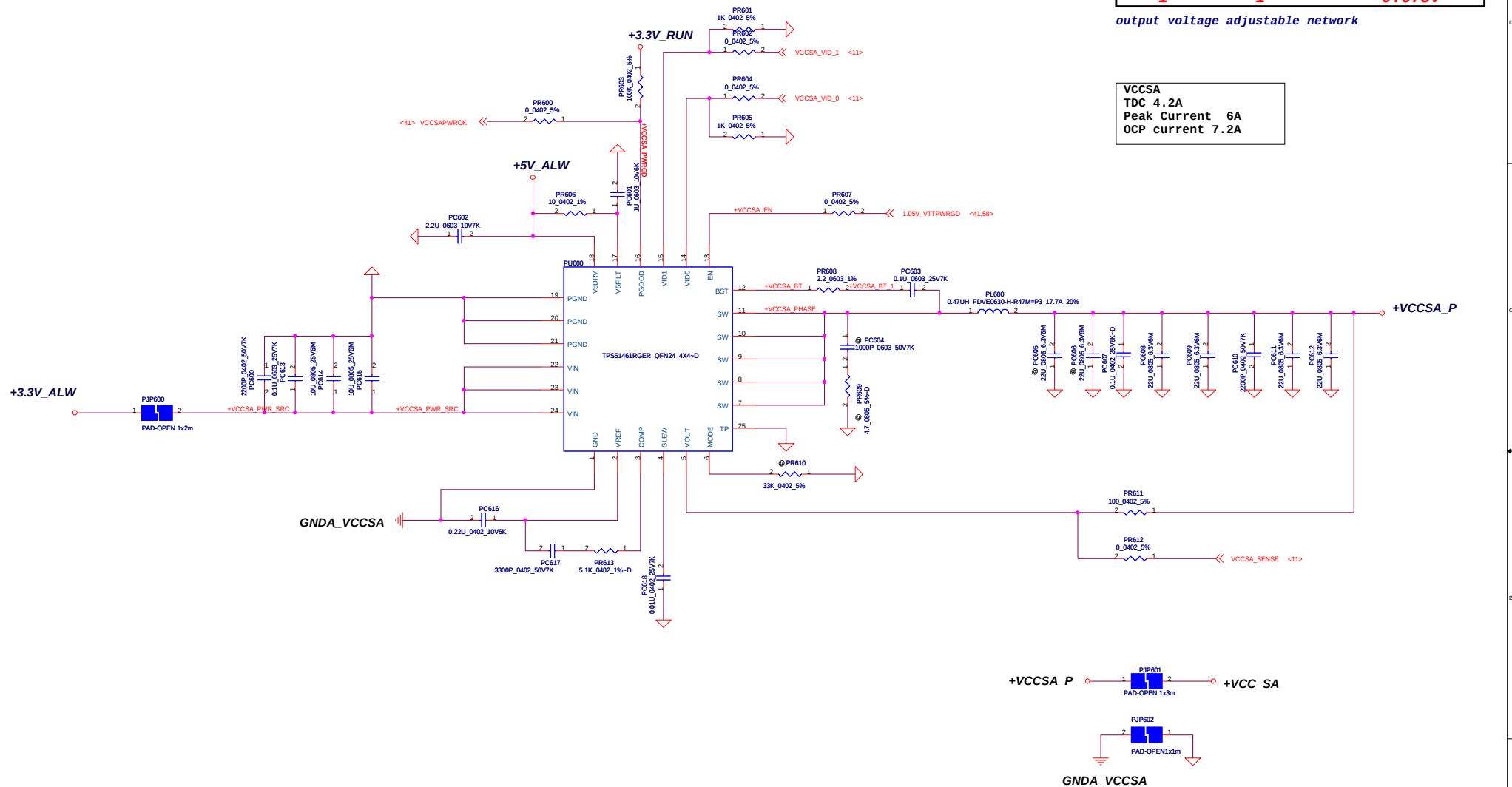
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	LA-7782		0.1
Date:	Friday, June 10, 2011	Sheet	57 of 66





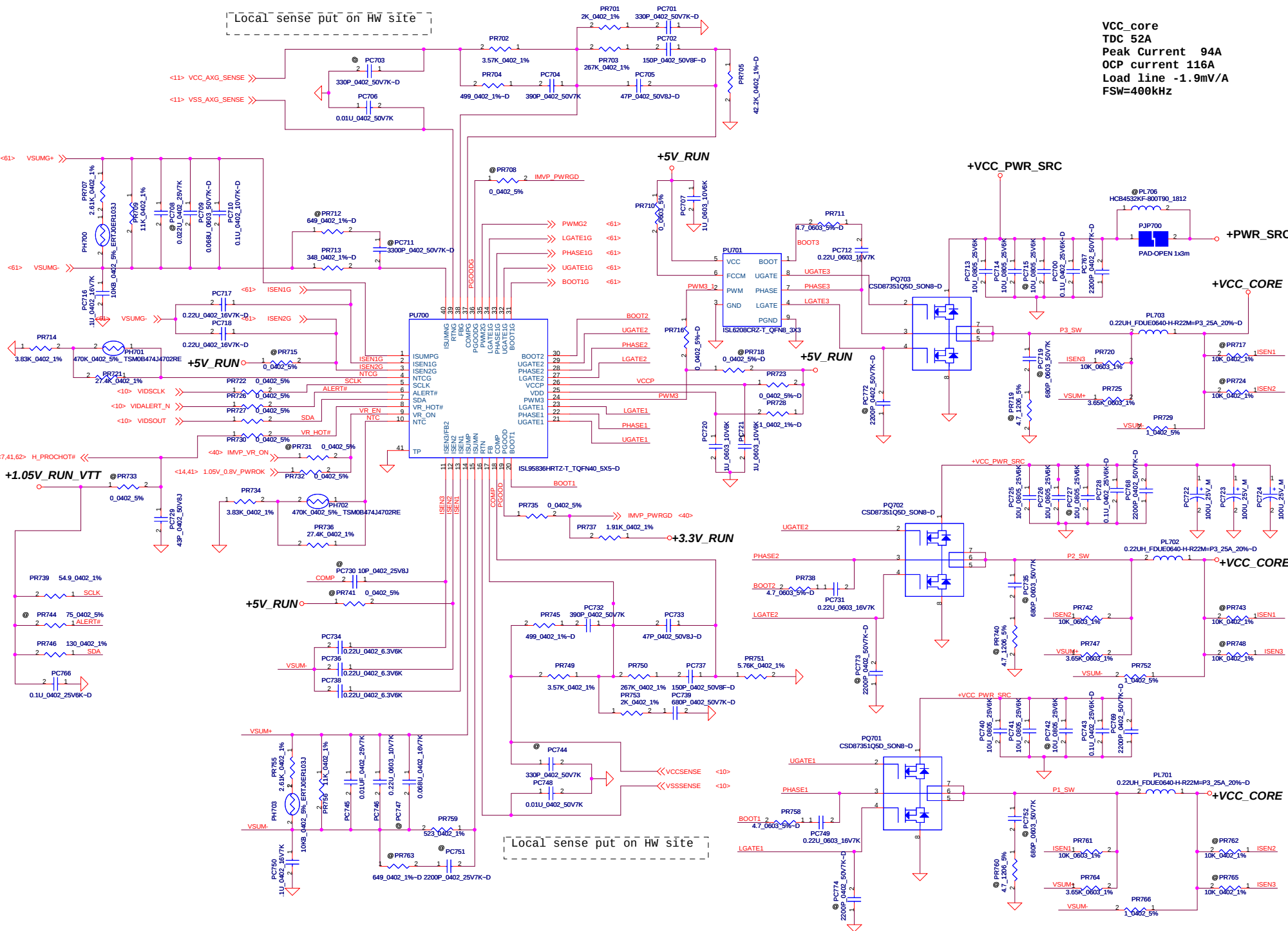
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Local sense put on HW site

VCC_core
TDC 52A
Peak Current 94A
OCP current 116A
Load line -1.9mV/A
FSW=400kHz

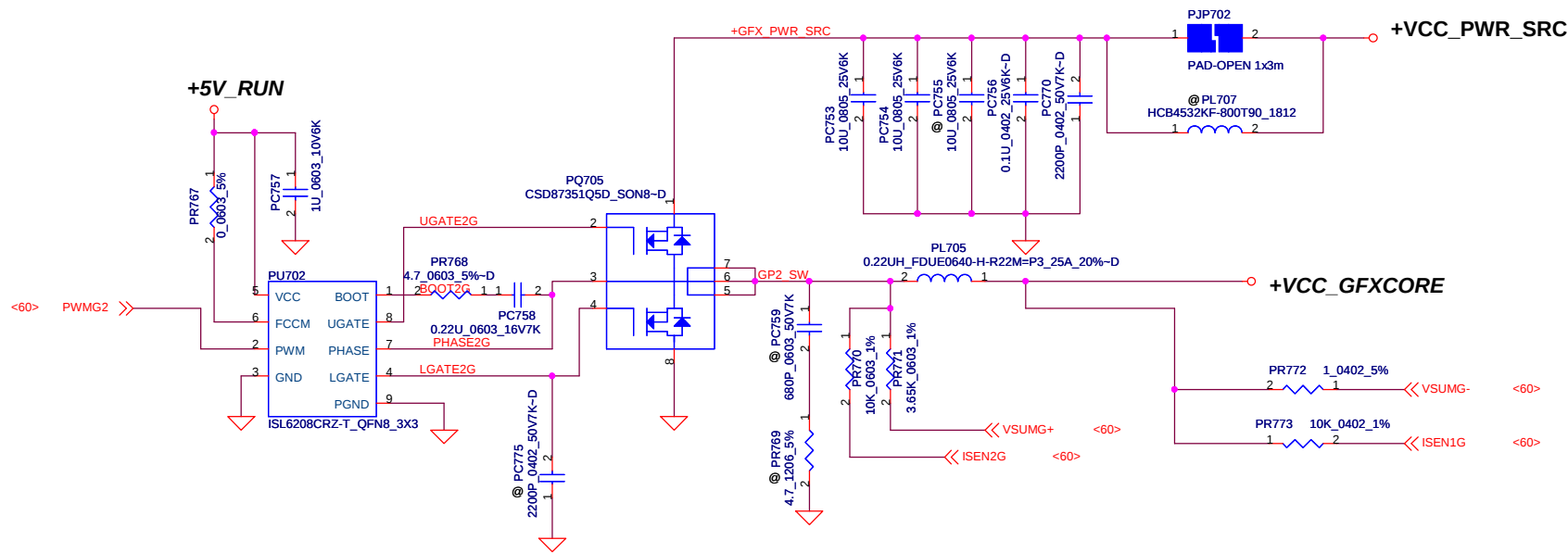


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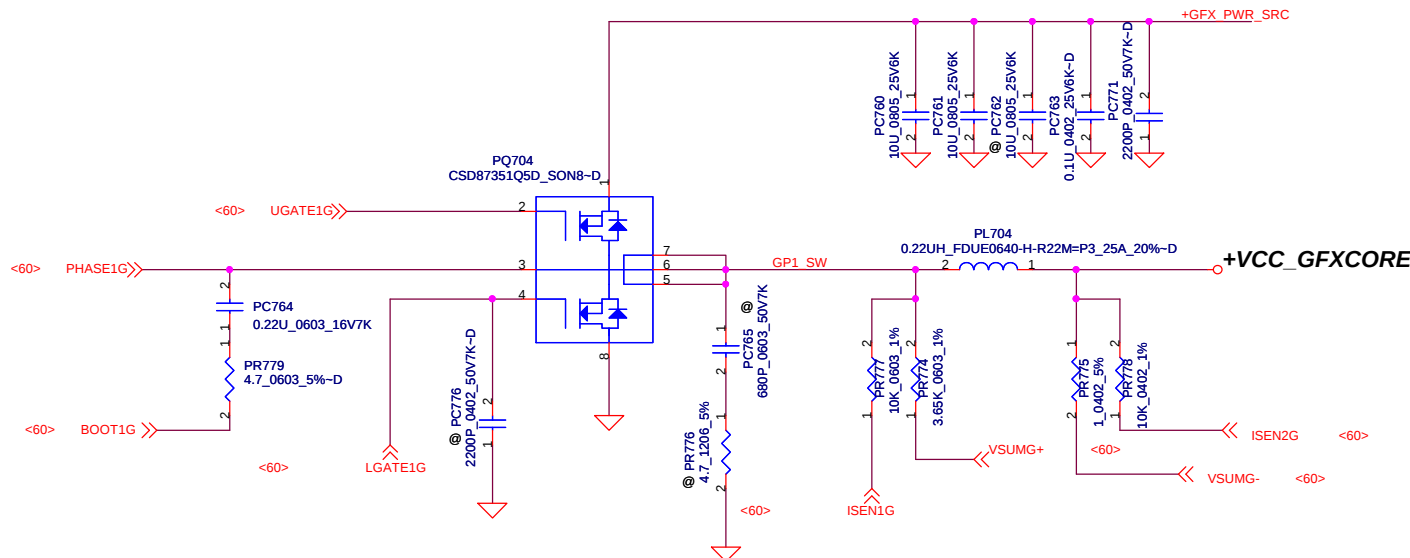


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+VCC_CORE			
File	Document Number	Rev	
	LA-7782	0.1	
Date	Friday, June 10, 2011	Sheet	80 of 86

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VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line -3.9mV/A
FSW=400kHz



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Size	Document Number	LA-7782	
Date:	Friday, June 10, 2011	Sheet	61 of 66
Rev		0.1	



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Size	Document Number LA-7782	Rev 0.1
Date: Friday, June 10, 2011 Sheet 66 of 66		