Compal confidential

Liverpool/Sunderland 10ATG

NSWAE/NTWAE LA-5331P Schematics Document

Mobile AMD S1G3/
RX881
SB710

2009-10-02 Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.		
Title	*Schematic, M/B LA-5331P*	
Size: Custom	Document Number: *401716*	Rev: C
Date: Tuesday, February 23, 2010	Sheet 1 of 54	

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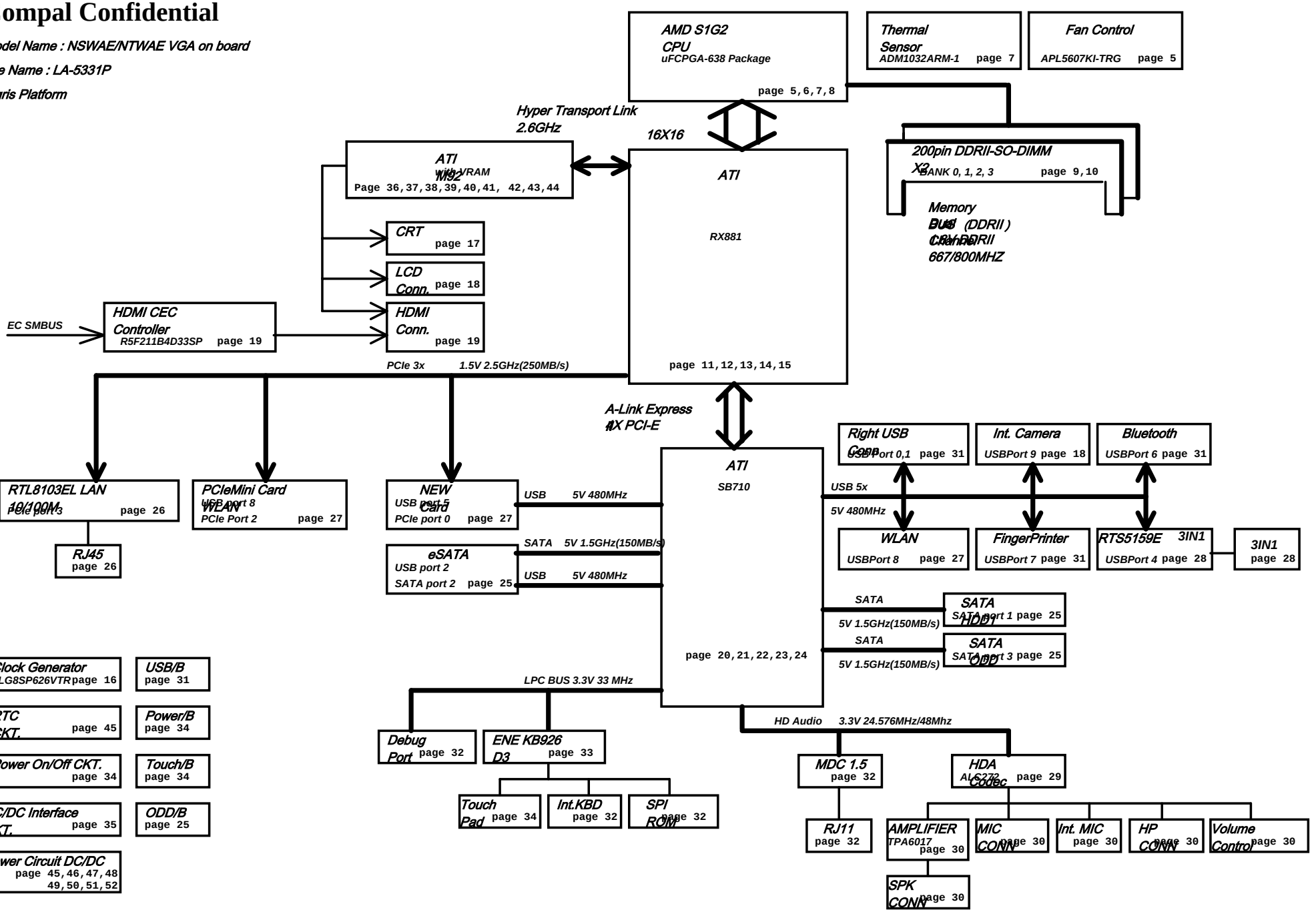
Model Name : NSWAE/NTWAE VGA on board

File Name : LA-5331P

Tigris Platform



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Title: **Schematic, M/B LA-5331P**

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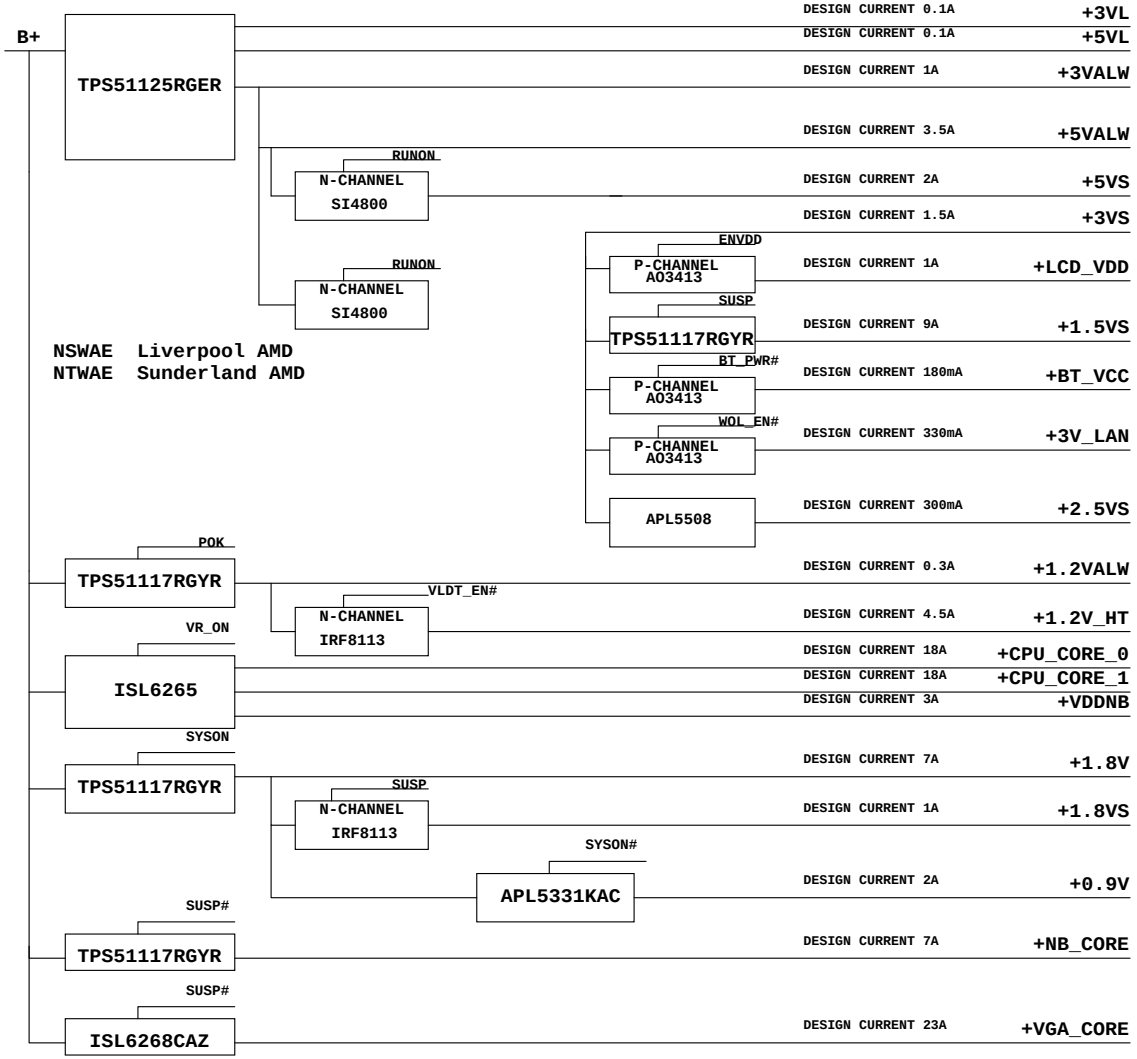

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Voltage Rails

O : ON
X : OFF

power plane / State	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D4		

EC SM Bus2 address

Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D3		

Symbol Note :

: Digital Ground

: Analog Ground

@ : just reserve , no build

DEBUG@ : reserve for debug.

Layout Notes

UMA@: means for RS780M.

BTO (Build-To-Order) Option Table

Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD		WiFi		G- sensor		3 in 1 card reader
Description	(E / A)	(B)	(R)	(S)			(H)				
Explain					16"	17"	Half - size	WIMAX	First	Second	RTS5159
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@	WIMAX@	G@ + G_1st@	G@ + G_2nd@	CARD@

Function	FingerPrinter	CAMERA & MIC		HDMI			LVDS wireset	DC-IN		CHIPSET		
Description	(F)	(X)		(Y)								
Explain		CAMERA	MIC	AMD(UMA)	ATI VGA/B	COMMON	Cost down					
BTO	FP@	CAM@	MIC@	IHDMI@	HDMI@	H@	LVDSSET@	16inch_45@	17inch_45@	PUMA@	TIGRIS@	

SMBUS Control Table

	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD	MXM Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	KB926		V	V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V							V
I2C_CLK I2C_DATA	RX881								V			
DDC_CLK0 DDC_DATA0	RX881									V		
DDC_CLK1 DDC_DATA1	RX881											
SCL0 SDA0	SB710					V	V				V	
SCL1 SDA1	SB710							V				
SCL2 SDA2	SB710											
SCL3 SDA3	SB710											

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< C1, C2 and C7 must be replaced to 10-uF for Caspian compatibility >

+1.2V_HT

VLDT CAP. Near CPU Socket

250 mil

C1 10U_0805_10V6K
C2 10U_0805_10V6K
C3 0.22U_0603_16V4Z
C4 0.22U_0603_16V4Z
C5 180P_0402_50V8J
C6 180P_0402_50V8J

11 H_CADIP[0..15] → H_CADIP[0..15]
11 H_CADIN[0..15] → H_CADIN[0..15]
H_CADOP[0..15] → H_CADOP[0..15] 11
H_CADON[0..15] → H_CADON[0..15] 11

+1.2V_HT

VLDT=500mA

JCPUA

HT LINK

D1 VLDT_A0 — VLDT_B0 AE2
D2 VLDT_A1 — VLDT_B1 AE3
D3 VLDT_A2 — VLDT_B2 AE4
D4 VLDT_A3 — VLDT_B3 AE5

+VLDT_B → C7 10U_0805_10V6K

< VLDT_A & VLDT_B : HyperTransport I/O ring power >

H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	E5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

< From NB > **< To NB >**

11 H_CLKIP0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	H_CLKOP0 11
11 H_CLKIN0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	H_CLKON0 11
11 H_CLKIP1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	H_CLKOP1 11
11 H_CLKIN1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	H_CLKON1 11
11 H_CTLIP0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	H_CTLOP0 11
11 H_CTLIN0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	H_CTLON0 11
11 H_CTLIP1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	H_CTLOP1 11
11 H_CTLIN1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	H_CTLON1 11

@ 6090022100G_B

< FAN Control Circuit : Vout = 1.6 x Vset >

+5VS

1A

+FAN1 → C192 10U_0805_10V4Z

C183 10U_0805_10V4Z

U6 APL5607KI-TRG_SO8 (EN, VIN, VOUT, VSET, GND)

@ D1 1SS355_SOD323-2

@ D2 BAS16_SOT23-3

@ C9 1000P_0402_50V7K

+FAN1 → JFAN ACES_85204-0300N (GND, GND)

+3VS → R12 10K_0402_5%

@ C8 0.01U_0402_25V7K

< From EC > 33 EN_DFAN1

FAN_SPEED1 33 **< To EC >**

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< DDR2 VREF is 0.5 ratio >

+1.8V
R1 1K_0402_1%
+MCH_REF
R2 1K_0402_1%
C12 0.1U_0402_16V7K
C13 1000P_0402_50V7K

< PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH >

DDR_A_CLK0 — C10 1.5P_0402_50V9C — DDR_A_CLK#0
DDR_B_CLK0 — C14 1.5P_0402_50V9C — DDR_B_CLK#0
DDR_A_CLK1 — C11 1.5P_0402_50V9C — DDR_A_CLK#1
DDR_B_CLK1 — C15 1.5P_0402_50V9C — DDR_B_CLK#1

Place them close to CPU within 1"

+1.8V — R4 39.2_0402_1% MEM_P — R3 39.2_0402_1% MEM_N

T2 PAD — T1 PAD — T3 PAD

+0.9V — +0.9V

< VTT regulator voltage >

JCPUB — MEM:CMD/CTRL/CLK

D10	VTT1	VTT5	W10
C10	VTT2	VTT6	AC10
B10	VTT3	VTT7	AB10
AD10	VTT4	VTT8	AA10
		VTT9	A10
AE10	MEMZP		
AE10	MEMZN	VTT_SENSE	Y10 VTT_SENSE
H16	RSVD_M1	MEMVREF	W17 +MCH_REF
		RSVD_M2	B18

< To SO_DIMMA >	10 DDR_A_ODT0	DDR_A_ODT0 T19	MA0_ODT0
	10 DDR_A_ODT1	DDR_A_ODT1 V22	MA0_ODT1
		U21	MA1_ODT0
		V19	MA1_ODT1
			MB0_ODT0 W26 DDR_B_ODT0 → DDR_B_ODT0 9
			MB0_ODT1 W23 DDR_B_ODT1 → DDR_B_ODT1 9
			MB1_ODT0 Y26
< To SO_DIMMA >	10 DDR_CS0_DIMMA#	DDR_CS0_DIMMA# T20	MA0_CS_L0
	10 DDR_CS1_DIMMA#	DDR_CS1_DIMMA# U19	MA0_CS_L1
		U20	MA1_CS_L0
		V20	MA1_CS_L1
			MB0_CS_L0 V26 DDR_CS0_DIMMB# → DDR_CS0_DIMMB# 9
			MB0_CS_L1 W25 DDR_CS1_DIMMB# → DDR_CS1_DIMMB# 9
			MB1_CS_L0 U22
< To SO_DIMMA >	10 DDR_CKE0_DIMMA	DDR_CKE0_DIMMA J22	MA_CKE0
	10 DDR_CKE1_DIMMA	DDR_CKE1_DIMMA J20	MA_CKE1
			MB_CKE0 J25 DDR_CKE0_DIMMB → DDR_CKE0_DIMMB 9
			MB_CKE1 H26 DDR_CKE1_DIMMB → DDR_CKE1_DIMMB 9
		N19	MA_CLK_H0
		N20	MA_CLK_L0
< To SO_DIMMA >	10 DDR_A_CLK0	DDR_A_CLK0 E16	MA_CLK_H1
	10 DDR_A_CLK#0	DDR_A_CLK#0 F16	MA_CLK_L1
	10 DDR_A_CLK1	DDR_A_CLK1 Y16	MA_CLK_H2
	10 DDR_A_CLK#1	DDR_A_CLK#1 AA16	MA_CLK_L2
		P19	MA_CLK_H3
		P20	MA_CLK_L3
			MB_CLK_H0 P22
			MB_CLK_L0 R22
			MB_CLK_H1 A17 DDR_B_CLK0 → DDR_B_CLK0 9
			MB_CLK_L1 A18 DDR_B_CLK#0 → DDR_B_CLK#0 9
			MB_CLK_H2 AF18 DDR_B_CLK1 → DDR_B_CLK1 9
			MB_CLK_L2 AF17 DDR_B_CLK#1 → DDR_B_CLK#1 9
			MB_CLK_H3 R26
			MB_CLK_L3 R25
< To SO_DIMMA >	10 DDR_A_MA[15..0]	DDR_A_MA0 N21	MA_ADD0
		DDR_A_MA1 M20	MA_ADD1
		DDR_A_MA2 N22	MA_ADD2
		DDR_A_MA3 M19	MA_ADD3
		DDR_A_MA4 M22	MA_ADD4
		DDR_A_MA5 L20	MA_ADD5
		DDR_A_MA6 M24	MA_ADD6
		DDR_A_MA7 L21	MA_ADD7
		DDR_A_MA8 L19	MA_ADD8
		DDR_A_MA9 K22	MA_ADD9
		DDR_A_MA10 R21	MA_ADD10
		DDR_A_MA11 L22	MA_ADD11
		DDR_A_MA12 K20	MA_ADD12
		DDR_A_MA13 V24	MA_ADD13
		DDR_A_MA14 K24	MA_ADD14
		DDR_A_MA15 K19	MA_ADD15
			MB_ADD0 P24 DDR_B_MA0 → DDR_B_MA[15..0] 9
			MB_ADD1 N24 DDR_B_MA1
			MB_ADD2 P26 DDR_B_MA2
			MB_ADD3 N23 DDR_B_MA3
			MB_ADD4 N26 DDR_B_MA4
			MB_ADD5 L23 DDR_B_MA5
			MB_ADD6 N25 DDR_B_MA6
			MB_ADD7 L24 DDR_B_MA7
			MB_ADD8 M26 DDR_B_MA8
			MB_ADD9 K26 DDR_B_MA9
			MB_ADD10 T26 DDR_B_MA10
			MB_ADD11 L26 DDR_B_MA11
			MB_ADD12 L25 DDR_B_MA12
			MB_ADD13 W24 DDR_B_MA13
			MB_ADD14 J23 DDR_B_MA14
			MB_ADD15 J24 DDR_B_MA15
< To SO_DIMMA >	10 DDR_A_BS#0	DDR_A_BS#0 R20	MA_BANK0
	10 DDR_A_BS#1	DDR_A_BS#1 R23	MA_BANK1
	10 DDR_A_BS#2	DDR_A_BS#2 J21	MA_BANK2
			MB_BANK0 R24 DDR_B_BS#0 → DDR_B_BS#0 9
			MB_BANK1 U26 DDR_B_BS#1 → DDR_B_BS#1 9
			MB_BANK2 J26 DDR_B_BS#2 → DDR_B_BS#2 9
< To SO_DIMMA >	10 DDR_A_RAS#	DDR_A_RAS# R19	MA_RAS_L
	10 DDR_A_CAS#	DDR_A_CAS# T22	MA_CAS_L
	10 DDR_A_WE#	DDR_A_WE# T24	MA_WE_L
			MB_RAS_L U25 DDR_B_RAS# → DDR_B_RAS# 9
			MB_CAS_L U24 DDR_B_CAS# → DDR_B_CAS# 9
			MB_WE_L U23 DDR_B_WE# → DDR_B_WE# 9

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< Processor DDR2 Memory Interface >

JCPUC — MEM:DATA

9 DDR_B_D[63..0] < From/To SO_DIMMB >

DDR_B_D0	C11	MB_DATA0	MA_DATA0	G12	DDR_A_D0
DDR_B_D1	A11	MB_DATA1	MA_DATA1	F12	DDR_A_D1
DDR_B_D2	A14	MB_DATA2	MA_DATA2	H14	DDR_A_D2
DDR_B_D3	B14	MB_DATA3	MA_DATA3	G14	DDR_A_D3
DDR_B_D4	G11	MB_DATA4	MA_DATA4	H11	DDR_A_D4
DDR_B_D5	F11	MB_DATA5	MA_DATA5	H12	DDR_A_D5
DDR_B_D6	D12	MB_DATA6	MA_DATA6	C13	DDR_A_D6
DDR_B_D7	A13	MB_DATA7	MA_DATA7	F13	DDR_A_D7
DDR_B_D8	A15	MB_DATA8	MA_DATA8	H15	DDR_A_D8
DDR_B_D9	A16	MB_DATA9	MA_DATA9	E15	DDR_A_D9
DDR_B_D10	A19	MB_DATA10	MA_DATA10	E17	DDR_A_D10
DDR_B_D11	A20	MB_DATA11	MA_DATA11	H17	DDR_A_D11
DDR_B_D12	C14	MB_DATA12	MA_DATA12	E14	DDR_A_D12
DDR_B_D13	D14	MB_DATA13	MA_DATA13	F14	DDR_A_D13
DDR_B_D14	C18	MB_DATA14	MA_DATA14	C17	DDR_A_D14
DDR_B_D15	D18	MB_DATA15	MA_DATA15	G17	DDR_A_D15
DDR_B_D16	D20	MB_DATA16	MA_DATA16	G18	DDR_A_D16
DDR_B_D17	A21	MB_DATA17	MA_DATA17	C19	DDR_A_D17
DDR_B_D18	D24	MB_DATA18	MA_DATA18	D22	DDR_A_D18
DDR_B_D19	C25	MB_DATA19	MA_DATA19	E20	DDR_A_D19
DDR_B_D20	B20	MB_DATA20	MA_DATA20	E18	DDR_A_D20
DDR_B_D21	C20	MB_DATA21	MA_DATA21	F18	DDR_A_D21
DDR_B_D22	B24	MB_DATA22	MA_DATA22	B22	DDR_A_D22
DDR_B_D23	C24	MB_DATA23	MA_DATA23	C23	DDR_A_D23
DDR_B_D24	E23	MB_DATA24	MA_DATA24	F20	DDR_A_D24
DDR_B_D25	E24	MB_DATA25	MA_DATA25	F22	DDR_A_D25
DDR_B_D26	G25	MB_DATA26	MA_DATA26	H24	DDR_A_D26
DDR_B_D27	G26	MB_DATA27	MA_DATA27	J19	DDR_A_D27
DDR_B_D28	C26	MB_DATA28	MA_DATA28	F21	DDR_A_D28
DDR_B_D29	D26	MB_DATA29	MA_DATA29	E22	DDR_A_D29
DDR_B_D30	G23	MB_DATA30	MA_DATA30	H20	DDR_A_D30
DDR_B_D31	G24	MB_DATA31	MA_DATA31	H22	DDR_A_D31
DDR_B_D32	AA24	MB_DATA32	MA_DATA32	Y24	DDR_A_D32
DDR_B_D33	AA23	MB_DATA33	MA_DATA33	AB24	DDR_A_D33
DDR_B_D34	AD24	MB_DATA34	MA_DATA34	AB22	DDR_A_D34
DDR_B_D35	AE24	MB_DATA35	MA_DATA35	AA21	DDR_A_D35
DDR_B_D36	AA26	MB_DATA36	MA_DATA36	W22	DDR_A_D36
DDR_B_D37	AA25	MB_DATA37	MA_DATA37	W21	DDR_A_D37
DDR_B_D38	AD26	MB_DATA38	MA_DATA38	Y22	DDR_A_D38
DDR_B_D39	AE25	MB_DATA39	MA_DATA39	AA22	DDR_A_D39
DDR_B_D40	AC22	MB_DATA40	MA_DATA40	Y20	DDR_A_D40
DDR_B_D41	AD22	MB_DATA41	MA_DATA41	AA20	DDR_A_D41
DDR_B_D42	AE20	MB_DATA42	MA_DATA42	AA18	DDR_A_D42
DDR_B_D43	AF20	MB_DATA43	MA_DATA43	AB18	DDR_A_D43
DDR_B_D44	AF24	MB_DATA44	MA_DATA44	AB21	DDR_A_D44
DDR_B_D45	AF23	MB_DATA45	MA_DATA45	AD21	DDR_A_D45
DDR_B_D46	AC20	MB_DATA46	MA_DATA46	AD19	DDR_A_D46
DDR_B_D47	AD20	MB_DATA47	MA_DATA47	Y18	DDR_A_D47
DDR_B_D48	AD18	MB_DATA48	MA_DATA48	AD17	DDR_A_D48
DDR_B_D49	AE18	MB_DATA49	MA_DATA49	W16	DDR_A_D49
DDR_B_D50	AC14	MB_DATA50	MA_DATA50	W14	DDR_A_D50
DDR_B_D51	AD14	MB_DATA51	MA_DATA51	Y14	DDR_A_D51
DDR_B_D52	AE19	MB_DATA52	MA_DATA52	Y17	DDR_A_D52
DDR_B_D53	AC18	MB_DATA53	MA_DATA53	AB17	DDR_A_D53
DDR_B_D54	AE16	MB_DATA54	MA_DATA54	AB15	DDR_A_D54
DDR_B_D55	AE15	MB_DATA55	MA_DATA55	AD15	DDR_A_D55
DDR_B_D56	AE13	MB_DATA56	MA_DATA56	AB13	DDR_A_D56
DDR_B_D57	AC12	MB_DATA57	MA_DATA57	AD13	DDR_A_D57
DDR_B_D58	AB11	MB_DATA58	MA_DATA58	Y12	DDR_A_D58
DDR_B_D59	Y11	MB_DATA59	MA_DATA59	W11	DDR_A_D59
DDR_B_D60	AE14	MB_DATA60	MA_DATA60	AB14	DDR_A_D60
DDR_B_D61	AF14	MB_DATA61	MA_DATA61	AA14	DDR_A_D61
DDR_B_D62	AF11	MB_DATA62	MA_DATA62	AB12	DDR_A_D62
DDR_B_D63	AD11	MB_DATA63	MA_DATA63	AA12	DDR_A_D63

9 DDR_B_DM[7..0] < To SO_DIMMB >

DDR_B_DM0	A12	MB_DM0	MA_DM0	F12	DDR_A_DM0
DDR_B_DM1	B16	MB_DM1	MA_DM1	C15	DDR_A_DM1
DDR_B_DM2	A22	MB_DM2	MA_DM2	E19	DDR_A_DM2
DDR_B_DM3	F25	MB_DM3	MA_DM3	F24	DDR_A_DM3
DDR_B_DM4	AB26	MB_DM4	MA_DM4	AC24	DDR_A_DM4
DDR_B_DM5	AF22	MB_DM5	MA_DM5	Y19	DDR_A_DM5
DDR_B_DM6	AC16	MB_DM6	MA_DM6	AB16	DDR_A_DM6
DDR_B_DM7	AD12	MB_DM7	MA_DM7	Y13	DDR_A_DM7

DDR_A_DM[7..0] 10 < To SO_DIMMA >

9 DDR_B_DQS[7..0] < From/To SO_DIMMB >

DDR_B_DQS0	C12	MB_DQS_H0	MA_DQS_H0	G13	DDR_A_DQS0
DDR_B_DQS#0	B12	MB_DQS_L0	MA_DQS_L0	H13	DDR_A_DQS#0
DDR_B_DQS1	D16	MB_DQS_H1	MA_DQS_H1	G16	DDR_A_DQS1
DDR_B_DQS#1	C16	MB_DQS_L1	MA_DQS_L1	G15	DDR_A_DQS#1
DDR_B_DQS2	A24	MB_DQS_H2	MA_DQS_H2	C22	DDR_A_DQS2
DDR_B_DQS#2	A23	MB_DQS_L2	MA_DQS_L2	C21	DDR_A_DQS#2
DDR_B_DQS3	F26	MB_DQS_H3	MA_DQS_H3	G22	DDR_A_DQS3
DDR_B_DQS#3	F26	MB_DQS_L3	MA_DQS_L3	G21	DDR_A_DQS#3
DDR_B_DQS4	AC25	MB_DQS_H4	MA_DQS_H4	AD23	DDR_A_DQS4
DDR_B_DQS#4	AC26	MB_DQS_L4	MA_DQS_L4	AC23	DDR_A_DQS#4
DDR_B_DQS5	AF21	MB_DQS_H5	MA_DQS_H5	AB19	DDR_A_DQS5
DDR_B_DQS#5	AF22	MB_DQS_L5	MA_DQS_L5	AB20	DDR_A_DQS#5
DDR_B_DQS6	AE16	MB_DQS_H6	MA_DQS_H6	Y15	DDR_A_DQS6
DDR_B_DQS#6	AD16	MB_DQS_L6	MA_DQS_L6	W15	DDR_A_DQS#6
DDR_B_DQS7	AE12	MB_DQS_H7	MA_DQS_H7	W12	DDR_A_DQS7
DDR_B_DQS#7	AE12	MB_DQS_L7	MA_DQS_L7	W13	DDR_A_DQS#7

< From/To SO_DIMMB >

@ 6090022100G_B

DDR_A_DQS[7..0] 10 < From/To SO_DIMMA >

Security Classification	Compal Secret Data	
Issued Date	2008-09-25	Deciphered Date 2009-09-25

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< Close to CPU >

+CPU_CORE_0

R487 10_0402_5% CPU_VDD0_RUN_FB_H

R486 10_0402_5% CPU_VDD0_RUN_FB_L

Un-Mount R489 For Caspian (Tigris)

+CPU_CORE_1

@ R489 10_0402_5% CPU_VDD1_RUN_FB_H

@ R488 10_0402_5% CPU_VDD1_RUN_FB_L

Un-Mount R488 For Caspian (Tigris)

< 200-MHz PLL Reference Clock >

16 CLK_CPU_BCLK — C20 3900P_0402_50V7K — CPU_CLKIN_SC_P

R8 169_0402_1%

16 CLK_CPU_BCLK# — C21 3900P_0402_50V7K — CPU_CLKIN_SC_N

Address:100_1100 Place close to CPU wihtin 1.5"

< Filtered PLL Supply Voltage >

+2.5VS — L1 FBM_L11_201209_300L_0805 — VDDA=300mA — +2.5VDDA

@ +C16 100U_D2_10VM

C17 4.7U_0805_10V4Z

C18 3300P_0402_50V7K

C19 0.22U_0603_16V4Z

< Serial VID Interface clock & data >

+1.8VS

R22 1K_0402_5% CPU_SVC (0718 AMD --> 1K ohm)

R23 1K_0402_5% CPU_SVD

+1.8VS

R15 300_0402_5%

20 LDT_RST# — LDT_RST#

@ C22 0.01U_0402_25V7K

+1.8VS

R21 300_0402_5%

20,51 H_PWRGD — H_PWRGD

C23 0.1U_0402_16V7K

+1.8VS

R36 300_0402_5%

12,20 LDT_STOP# — LDT_STOP#

@ C25 0.01U_0402_25V7K

+1.8VS

R30 300_0402_5%

12,20 CPU_LDT_REQ# — CPU_LDT_REQ#

@ R27 0_0402_5% CPU_LDT_REQ_R#

C24 0.01U_0402_25V7K

@ Un-Mount R27 For Caspian (Tigris)

< Differential feedback for VDDNB >

Close to CPU

+VDDNB

R484 10_0402_5% CPU_VDDNB_RUN_FB_H

R485 10_0402_5% CPU_VDDNB_RUN_FB_L

< Sideband-Temperature Sensor Interface Clock & Data>

< Sideband-Temperature Sensor Interface interrupt >

< Compensation Resistor to VSS >

< Compensation Resistor to VLDT >

+1.2V_HT — R13 44.2_0402_1% CPU_HTREF0 — R14 44.2_0402_1% CPU_HTREF1

JCPUD

+2.5VDDA — F8 VDDA1, F9 VDDA2

CPU_CLKIN_SC_P — A9 CLKIN_H

CPU_CLKIN_SC_N — A8 CLKIN_L

LDT_RST# — B7 RESET_L

H_PWRGD — A7 PWROK

LDT_STOP# — F10 LDTSTOP_L

CPU_LDT_REQ_R# — C6 LDTREQ_L

AF4 SIC, AF5 SID, AF6 ALERT_L

HT_REF0 — R6

HT_REF1 — P6

51 CPU_VDD0_RUN_FB_H — CPU_VDD0_RUN_FB_H — F6 VDD0_FB_H

51 CPU_VDD0_RUN_FB_L — CPU_VDD0_RUN_FB_L — E6 VDD0_FB_L

51 CPU_VDD1_RUN_FB_H — CPU_VDD1_RUN_FB_H — Y6 VDD1_FB_H

51 CPU_VDD1_RUN_FB_L — CPU_VDD1_RUN_FB_L — AB6 VDD1_FB_L

< Debug ready > — T9 PAD — G10 DBRDY

< JTAG debug port > — T10 PAD — AA9 TMS; T11 PAD — AC9 TCK; T12 PAD — AD9 TRST_L; T19 PAD — AE9 TDI

CPU_TEST23_TSTUPD — AD7 TEST23

H10 TEST18, G9 TEST19

CPU_TEST25_H_BYPASSCLK_H — F9 TEST25_H

CPU_TEST25_L_BYPASSCLK_L — E8 TEST25_L

CPU_TEST21_SCANEN — AB8 TEST21

CPU_TEST20_SCANCLK2 — AF7 TEST20

CPU_TEST24_SCANCLK1 — AE7 TEST24

AE8 TEST22, AC8 TEST12, AF8 TEST27

R25 0_0402_5% — C2 TEST9, AA6 TEST6

A3 RSVD1, A5 RSVD2, B3 RSVD3, B5 RSVD4, C1 RSVD5

KEY1 M11, KEY2 W18

SVC A6 CPU_SVC — CPU_SVC 51

SVD A4 CPU_SVD — CPU_SVD 51

< Serial VID Interface clock & data >

THERMTRIP_L — AF6 CPU_THERMTRIP# R

PROCHOT_L — AC7 CPU_PROCHOT# 1,8

MEMHOT_L — AA8 — R42 @300_0402_5% — +1.8V

Tigris don't need to mount it.

< Thermal Sensor Trip output >

< HTC-active state indication or command >

THERMDC — W7 THERMDC_CPU

THERMDA — W8 THERMDA_CPU

< Thermal diode cathode & anode >

+1.8V sense no support

VDDIO_FB_H — W9 — PAD T22

VDDIO_FB_L — Y9 — PAD T21

< Differential feedback for VDDIO >

< VDDIO : DDR SDRAM I/O ring power supply>

< Differential feedback for VDDNB >

< Northbridge power supply >

VDDNB_FB_H — H6 CPU_VDDNB_RUN_FB_H — CPU_VDDNB_RUN_FB_H 51

VDDNB_FB_L — G6 CPU_VDDNB_RUN_FB_L — CPU_VDDNB_RUN_FB_L 51

< Debug request >

DBREQ_L — E10 CPU_DBREQ#

TDO — AE9 — PAD T20

route as differential as short as possible testpoint under package

TEST28_H — J7 CPU_TEST28_H_PLLCHRZ_P — PAD T5

TEST28_L — H8 CPU_TEST28_L_PLLCHRZ_N — PAD T6

TEST17 — D7 CPU_TEST17_BP3 — PAD T7

TEST16 — E7 CPU_TEST16_BP2 — PAD T8

TEST15 — E7

TEST14 — C7

TEST7 — C3

TEST10 — K8 CPU_TEST10_ANALOGOUT — @R32 300_0402_5% — +1.2V_HT

TEST8 — C4

Add R32 at PVT

TEST29_H — C9 CPU_TEST29_H_FBCLKOUT_P — PAD T13

TEST29_L — C8 CPU_TEST29_L_FBCLKOUT_N — PAD T14

RSVD10 H18, RSVD9 H19, RSVD8 AA7, RSVD7 D5, RSVD6 C5

@ 6090022100G_B

Add R497 and R498 at PVT

+1.8V

R497 510_0402_5% CPU_TEST25_H_BYPASSCLK_H — @ R498 510_0402_5%

@ R499 510_0402_5% CPU_TEST25_L_BYPASSCLK_L — R500 510_0402_5%

+1.8V — R10 10K_0402_5% — @D12 CH751H-40PT_SOD323-2 — < To power circuitry> — ENTRIP2 46,48

R5 300_0402_5% — @D21 CH751H-40PT_SOD323-2 — EN0 45,48

Q3 MMBT3904_NL_SOT23-3

CPU_THERMTRIP#_R — D16 CH751H-40PT_SOD323-2 — < To SB700 ACPI block> — H_THERMTRIP# 21

+1.8V — R9 300_0402_5%

CPU_PROCHOT# 1.8 — @ R11 0_0402_5% — < To SB700 CPU block> — H_PROCHOT# 20

Add R29 and R31 at PVT

R31 300_0402_5% CPU_TEST20_SCANCLK2

R29 300_0402_5% CPU_TEST23_TSTUPD

R26 300_0402_5% CPU_TEST21_SCANEN

R28 300_0402_5% CPU_TEST24_SCANCLK1

< HDT Connector >

< R41 Close to CPU > < R494 Close to CPU >

CPU_DBREQ# — R494 0_0402_5%

+1.8V — R41 300_0402_5% — @

T23 PAD

@ R40 220_0402_5%

@ R39 220_0402_5%

@ R38 220_0402_5%

@ R37 220_0402_5%

+1.8V T24 PAD

+1.8V — LDT_RST#

JP3

@ SAMTEC_ASP-68200-07

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

< Thermal Sensor >

+3VS — C26 0.1U_0402_16V7K

U2 ADM1032ARM-1 ZREEL_MSOP8

VDD 1, D+ 2, D- 3, THERM# 4, SCLK 8, SDATA 7, ALERT# 6, GND 5

THERMDA_CPU — C27 2200P_0402_50V7K — THERMDC_CPU

< noise filter cap >

EC_SMB_CK2 — < From EC > EC_SMB_CK2 33,34,44

EC_SMB_DA2 — EC_SMB_DA2 33,34,44

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VDD decoupling : +CPU_CORE

+CPU_CORE_0
C30 330U_X_2VM_R6M
C28 330U_X_2VM_R6M
Near CPU Socket

+CPU_CORE_0
C32 22U_0805_6.3V6M
C33 22U_0805_6.3V6M
C34 22U_0805_6.3V6M
C35 22U_0805_6.3V6M
Under CPU Socket

+CPU_CORE_0
C40 0.22U_0603_16V4Z
C41 0.01U_0402_25V7K
C42 180P_0402_50V8J
Under CPU Socket

+CPU_CORE_1
C31 330U_X_2VM_R6M
C29 330U_X_2VM_R6M
Near CPU Socket

+CPU_CORE_1
C36 22U_0805_6.3V6M
C37 22U_0805_6.3V6M
C38 22U_0805_6.3V6M
C39 22U_0805_6.3V6M
Under CPU Socket

+CPU_CORE_1
C43 0.22U_0603_16V4Z
C44 0.01U_0402_25V7K
C45 180P_0402_50V8J
Under CPU Socket

VDDIO decoupling : DDR SDRAM I/O ring power

+1.8V
C46 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C48 0.22U_0603_16V4Z
C49 0.22U_0603_16V4Z
C50 180P_0402_50V8J
C51 180P_0402_50V8J
Under CPU Socket

+1.8V
C55 0.22U_0603_16V4Z
C56 0.22U_0603_16V4Z
C57 0.22U_0603_16V4Z
C58 0.22U_0603_16V4Z
Between CPU Socket and DIMM

+1.8V
C60 0.01U_0402_25V7K
C61 0.01U_0402_25V7K
Between CPU Socket and DIMM

+1.8V
180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>
C62 180P_0402_50V8J
C63 180P_0402_50V8J
C64 180P_0402_50V8J
C65 180P_0402_50V8J
Between CPU Socket and DIMM

+1.8V
C74 4.7U_0805_10V4Z
C75 4.7U_0805_10V4Z
C76 4.7U_0805_10V4Z
C77 4.7U_0805_10V4Z
Between CPU Socket and DIMM
Change to B2 size
@ C78 220U_B2_4VM_R45M

VTT decoupling.

+0.9V
C66 4.7U_0805_10V4Z
C67 4.7U_0805_10V4Z
C68 0.22U_0603_16V4Z
C69 0.22U_0603_16V4Z
C70 1000P_0402_50V7K
C71 1000P_0402_50V7K
C72 180P_0402_50V8J
C73 180P_0402_50V8J
Near CPU Socket Right side

+0.9V
C79 4.7U_0805_10V4Z
C80 4.7U_0805_10V4Z
C81 0.22U_0603_16V4Z
C82 0.22U_0603_16V4Z
C83 1000P_0402_50V7K
C84 1000P_0402_50V7K
C85 180P_0402_50V8J
C86 180P_0402_50V8J
Near CPU Socket Left side

+0.9V
C59 220U_B2_4VM_R45M
1. Near Power Supply
2. Change to B2 size

+VDDNB decoupling : Northbridge power

+VDDNB
4000mA
C52 22U_0805_6.3V6M
C53 22U_0805_6.3V6M
C54 22U_0805_6.3V6M

+CPU_CORE_0 JCPUE +CPU_CORE_1

G4	VDD0_1	VDD1_1	P8
H2	VDD0_2	VDD1_2	P10
J9	VDD0_3	VDD1_3	R4
J11	VDD0_4	VDD1_4	R7
J13	VDD0_5	VDD1_5	R9
J15	VDD0_6	VDD1_6	R11
K6	VDD0_7	VDD1_7	T2
K10	VDD0_8	VDD1_8	T6
K12	VDD0_9	VDD1_9	T8
K14	VDD0_10	VDD1_10	T10
L4	VDD0_11	VDD1_11	T12
L7	VDD0_12	VDD1_12	T14
L9	VDD0_13	VDD1_13	U7
L11	VDD0_14	VDD1_14	U9
L13	VDD0_15	VDD1_15	U11
L15	VDD0_16	VDD1_16	U13
M2	VDD0_17	VDD1_17	U15
M6	VDD0_18	VDD1_18	V6
M8	VDD0_19	VDD1_19	V8
M10	VDD0_20	VDD1_20	V10
N7	VDD0_21	VDD1_21	V12
N9	VDD0_22	VDD1_22	V14
N11	VDD0_23	VDD1_23	W4
		VDD1_24	Y2
K16	VDDNB_1	VDD1_25	AC4
M16	VDDNB_2	VDD1_26	AD2
P16	VDDNB_3		
T16	VDDNB_4	VDDIO27	Y25
V16	VDDNB_5	VDDIO26	V25
		VDDIO25	V23
H25	VDDIO1	VDDIO24	V21
J17	VDDIO2	VDDIO23	V18
K18	VDDIO3	VDDIO22	U17
K21	VDDIO4	VDDIO21	T25
K23	VDDIO5	VDDIO20	T23
K25	VDDIO6	VDDIO19	T21
L17	VDDIO7	VDDIO18	T18
M18	VDDIO8	VDDIO17	R17
M21	VDDIO9	VDDIO16	P25
M23	VDDIO10	VDDIO15	P23
M25	VDDIO11	VDDIO14	P21
N17	VDDIO12	VDDIO13	P18

+VDDNB
+1.8V
+1.8V
@ 6090022100G_B Athlon 64 S1 Processor Socket

JCPUF

AA4	VSS1	VSS66	J6
AA11	VSS2	VSS67	J8
AA13	VSS3	VSS68	J10
AA15	VSS4	VSS69	J12
AA17	VSS5	VSS70	J14
AA19	VSS6	VSS71	J16
AB2	VSS7	VSS72	J18
AB7	VSS8	VSS73	K2
AB9	VSS9	VSS74	K7
AB23	VSS10	VSS75	K9
AB25	VSS11	VSS76	K11
AC11	VSS12	VSS77	K13
AC13	VSS13	VSS78	K15
AC15	VSS14	VSS79	K17
AC17	VSS15	VSS80	L6
AC19	VSS16	VSS81	L8
AC21	VSS17	VSS82	L10
AD6	VSS18	VSS83	L12
AD8	VSS19	VSS84	L14
AD25	VSS20	VSS85	L16
AE11	VSS21	VSS86	L18
AE13	VSS22	VSS87	M7
AE15	VSS23	VSS88	M9
AE17	VSS24	VSS89	AC6
AE19	VSS25	VSS90	M17
AE21	VSS26	VSS91	N4
AE23	VSS27	VSS92	N8
B4	VSS28	VSS93	N10
B6	VSS29	VSS94	N16
B8	VSS30	VSS95	N18
B9	VSS31	VSS96	P2
B11	VSS32	VSS97	P7
B13	VSS33	VSS98	P9
B15	VSS34	VSS99	P11
B17	VSS35	VSS100	P17
B19	VSS36	VSS101	R8
B21	VSS37	VSS102	R10
B23	VSS38	VSS103	R16
B25	VSS39	VSS104	R18
D6	VSS40	VSS105	T7
D8	VSS41	VSS106	T9
D9	VSS42	VSS107	T11
D11	VSS43	VSS108	T13
D13	VSS44	VSS109	T15
D15	VSS45	VSS110	T17
D17	VSS46	VSS111	U4
D19	VSS47	VSS112	U6
D21	VSS48	VSS113	U8
D23	VSS49	VSS114	U10
D25	VSS50	VSS115	U12
E4	VSS51	VSS116	U14
F2	VSS52	VSS117	U16
F11	VSS53	VSS118	U18
F13	VSS54	VSS119	V2
F15	VSS55	VSS120	V7
F17	VSS56	VSS121	V9
F19	VSS57	VSS122	V11
F21	VSS58	VSS123	V13
F23	VSS59	VSS124	V15
F25	VSS60	VSS125	V17
H7	VSS61	VSS126	W6
H9	VSS62	VSS127	Y21
H21	VSS63	VSS128	Y23
H23	VSS64	VSS129	N6
J4	VSS65		

@ 6090022100G_B Athlon 64 S1 Processor Socket

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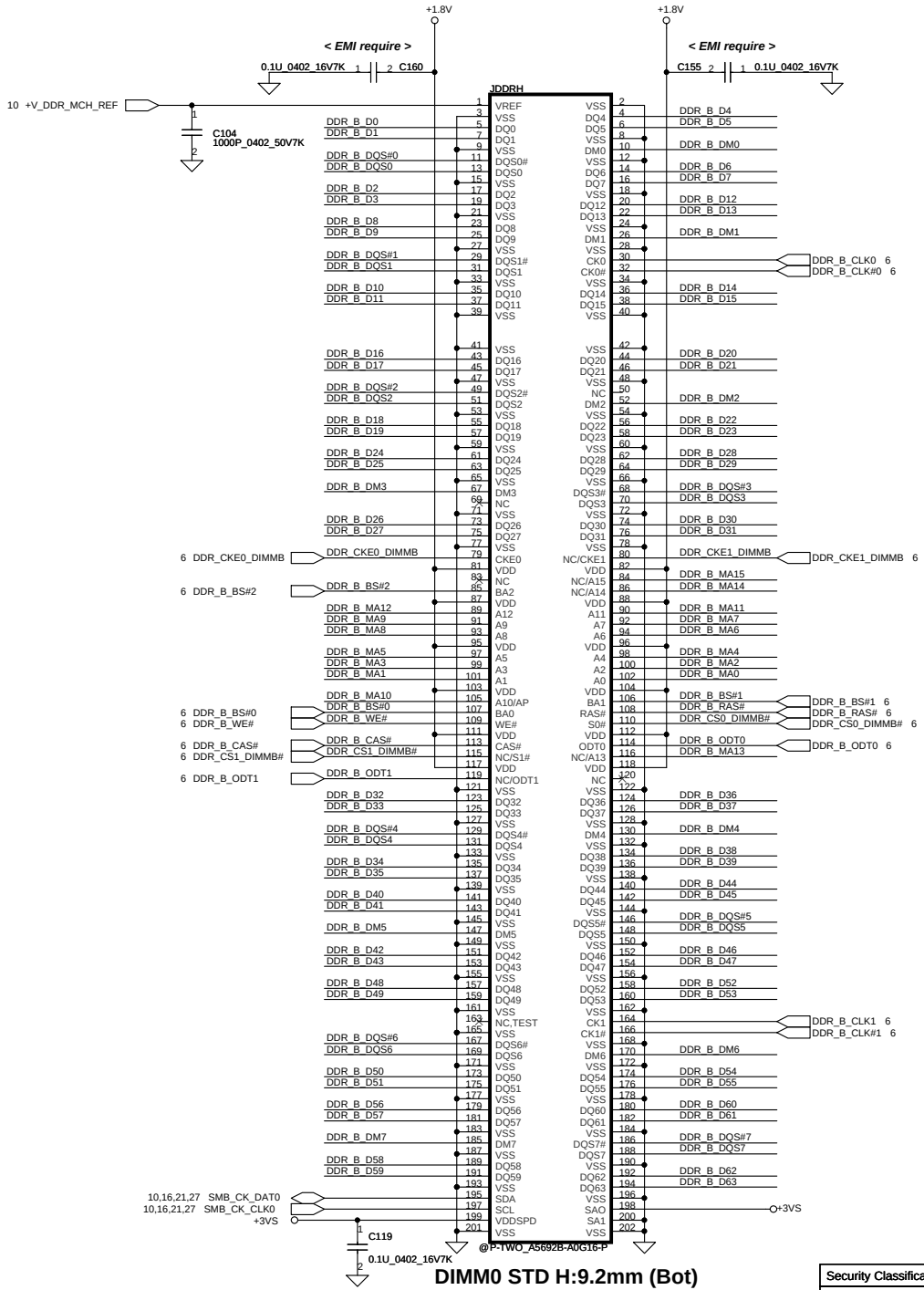
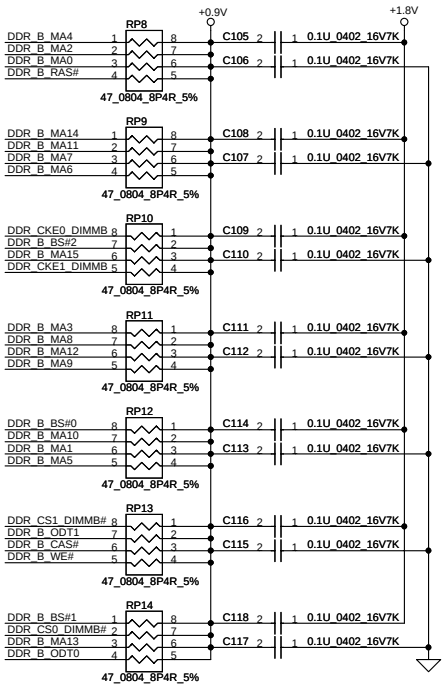
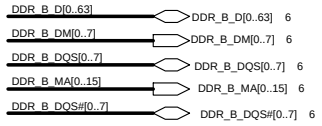


DIMM0 STD H:9.2mm (Bot)





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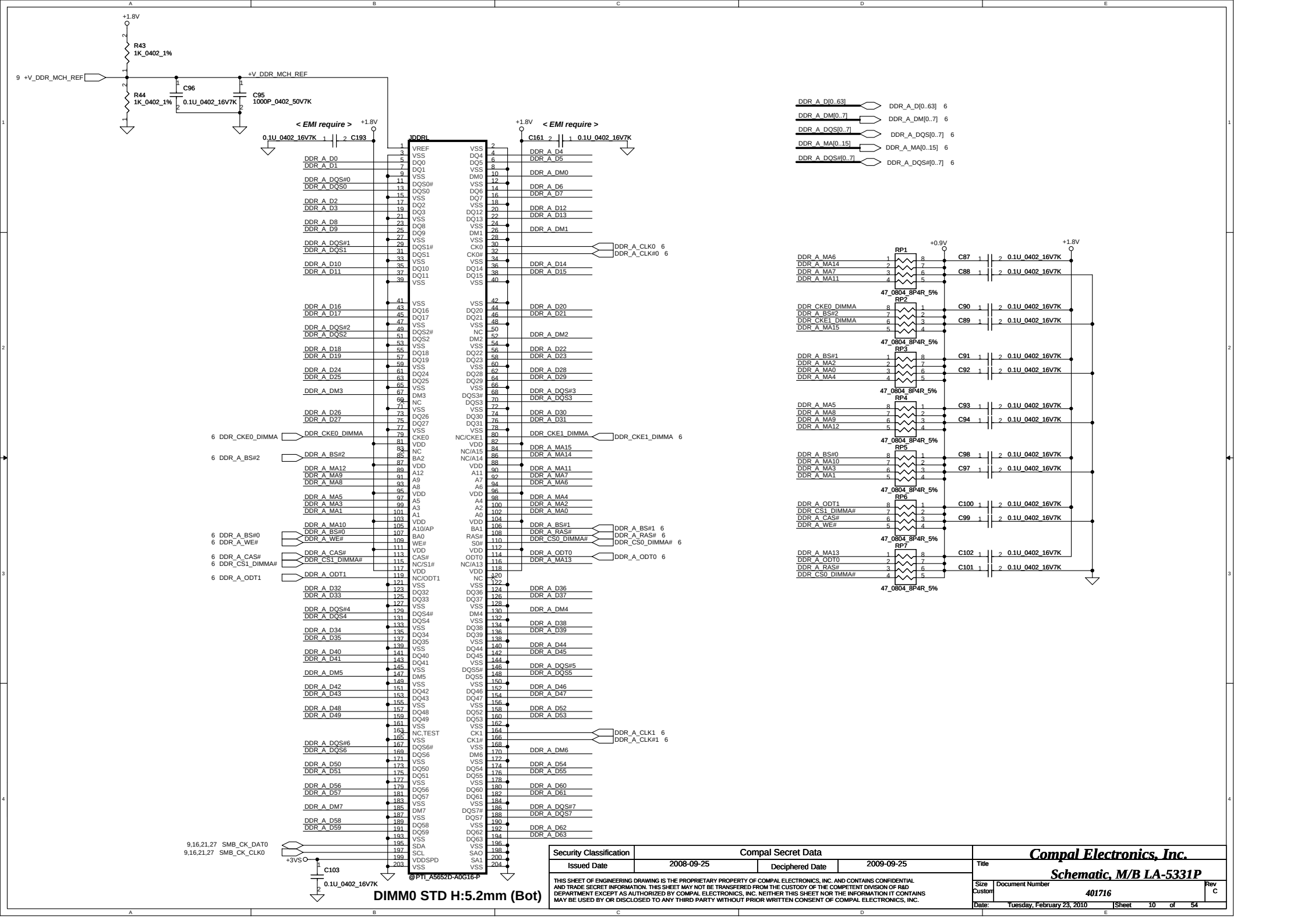

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U3B PM : RX881

PART 2 OF 6

PCIE I/F GFX

PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15] 36
PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15] 36

< From MXM VGA board >

GFX_RX	Pin	PCIE_GTX_C_MRX	Polarity inversion
GFX_RX0P/N	D4/C4	PCIE_GTX_C_MRX_N0/P0	Polarity inversion
GFX_RX1P/N	A3/B3	PCIE_GTX_C_MRX_P1/N1	
GFX_RX2P/N	C2/C1	PCIE_GTX_C_MRX_N2/P2	Polarity inversion
GFX_RX3P/N	E5/F5	PCIE_GTX_C_MRX_N3/P3	Polarity inversion
GFX_RX4P/N	G6/G5	PCIE_GTX_C_MRX_N4/P4	Polarity inversion
GFX_RX5P/N	H5/H6	PCIE_GTX_C_MRX_N5/P5	Polarity inversion
GFX_RX6P/N	J6/J5	PCIE_GTX_C_MRX_N6/P6	
GFX_RX7P/N	J7/J8	PCIE_GTX_C_MRX_N7/P7	Polarity inversion
GFX_RX8P/N	L5/L6	PCIE_GTX_C_MRX_N8/P8	Polarity inversion
GFX_RX9P/N	M8/L8	PCIE_GTX_C_MRX_N9/P9	Polarity inversion
GFX_RX10P/N	P7/M7	PCIE_GTX_C_MRX_N10/P10	Polarity inversion
GFX_RX11P/N	P5/M5	PCIE_GTX_C_MRX_N11/P11	Polarity inversion
GFX_RX12P/N	R8/P8	PCIE_GTX_C_MRX_N12/P12	Polarity inversion
GFX_RX13P/N	R6/R5	PCIE_GTX_C_MRX_N13/P13	Polarity inversion
GFX_RX14P/N	P4/P3	PCIE_GTX_C_MRX_N14/P14	Polarity inversion
GFX_RX15P/N	T4/T3	PCIE_GTX_C_MRX_N15/P15	Polarity inversion

GFX_TX	Pin	PCIE_MTX_GRX	C	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX	Polarity inversion
GFX_TX0P/N	A5/B5	PCIE_MTX_GRX_P0/N0	C120/C121	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_N0/P0	Polarity inversion
GFX_TX1P/N	A4/B4	PCIE_MTX_GRX_P1/N1	C122/C123	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_N1/P1	Polarity inversion
GFX_TX2P/N	C3/B2	PCIE_MTX_GRX_P2/N2	C124/C125	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P2/N2	
GFX_TX3P/N	D1/D2	PCIE_MTX_GRX_P3/N3	C126/C127	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_N3/P3	Polarity inversion
GFX_TX4P/N	E2/E1	PCIE_MTX_GRX_P4/N4	C128/C129	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P4/N4	
GFX_TX5P/N	F4/F3	PCIE_MTX_GRX_P5/N5	C130/C131	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P5/N5	
GFX_TX6P/N	F1/F2	PCIE_MTX_GRX_P6/N6	C132/C133	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P6/N6	
GFX_TX7P/N	H4/H3	PCIE_MTX_GRX_P7/N7	C134/C135	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P7/N7	
GFX_TX8P/N	H1/H2	PCIE_MTX_GRX_P8/N8	C136/C137	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P8/N8	
GFX_TX9P/N	J2/J1	PCIE_MTX_GRX_P9/N9	C138/C139	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P9/N9	
GFX_TX10P/N	K4/K3	PCIE_MTX_GRX_P10/N10	C140/C141	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P10/N10	
GFX_TX11P/N	K1/K2	PCIE_MTX_GRX_P11/N11	C142/C143	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P11/N11	
GFX_TX12P/N	M4/M3	PCIE_MTX_GRX_P12/N12	C144/C145	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_N12/P12	Polarity inversion
GFX_TX13P/N	M1/M2	PCIE_MTX_GRX_P13/N13	C146/C147	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P13/N13	
GFX_TX14P/N	N2/N1	PCIE_MTX_GRX_P14/N14	C148/C149	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_N14/P14	Polarity inversion
GFX_TX15P/N	P1/P2	PCIE_MTX_GRX_P15/N15	C150/C151	1	2	0.1U 0402 16V7K	PCIE_MTX_C_GRX_P15/N15	

PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] 36
PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] 36

< To MXM VGA board >

PCIE I/F GPP

GPP_RX	Pin	PCIE_PTX_C_IRX	GPP_TX	Pin	PCIE_ITX	C	1	2	0.1U 0402 16V7K	PCIE_ITX_C_PRX	
GPP_RX0P/N	AE3/AD4	27 PCIE_PTX_C_IRX_P0/N0	GPP_TX0P/N	AC1/AC2	PCIE_ITX_PRX_P0/N0	C152/C153	1	2	0.1U 0402 16V7K	PCIE_ITX_C_PRX_P0/N0	27
GPP_RX1P/N	AE2/AD3		GPP_TX1P/N	AB4/AB3							
GPP_RX2P/N	AD1/AD2	27 PCIE_PTX_C_IRX_P2/N2	GPP_TX2P/N	AA2/AA1	PCIE_ITX_PRX_P2/N2 WLAN@	C156/C157	1	2	0.1U 0402 16V7K	PCIE_ITX_C_PRX_P2/N2	27
GPP_RX3P/N	V5/W6	26 PCIE_PTX_C_IRX_P3/N3	GPP_TX3P/N	Y1/Y2	PCIE_ITX_PRX_P3/N3	C158/C159	1	2	0.1U 0402 16V7K	PCIE_ITX_C_PRX_P3/N3	26
GPP_RX4P/N	U5/U6		GPP_TX4P/N	Y4/Y3							
GPP_RX5P/N	U8/U7		GPP_TX5P/N	V1/V2							

< From New Card >
< From WLAN >
< From LAN >

< To New Card >
< To WLAN >
< To LAN >

PCIE I/F SB

SB_RX	Pin	SB_TX	Pin	PCIE	C	1	2	0.1U 0402 16V7K	SB_TX	
SB_RX0P/N	AA8/Y8	SB_TX0P/N	AD7/AE7	SB_TX0P_C/SB_TX0N_C	C162/C163	1	2	0.1U 0402 16V7K	SB_TX0P/N	20
SB_RX1P/N	AA7/Y7	SB_TX1P/N	AE6/AD6	SB_TX1P_C/SB_TX1N_C	C164/C165	1	2	0.1U 0402 16V7K	SB_TX1P/N	20
SB_RX2P/N	AA5/AA6	SB_TX2P/N	AB6/AC6	SB_TX2P_C/SB_TX2N_C	C166/C168	1	2	0.1U 0402 16V7K	SB_TX2P/N	20
SB_RX3P/N	W5/Y5	SB_TX3P/N	AD5/AE5	SB_TX3P_C/SB_TX3N_C	C169/C167	1	2	0.1U 0402 16V7K	SB_TX3P/N	20

20 SB_RX0P/N

< From SB710 : x4 PCIE A-link >

< To SB710 : x4 PCEI A-link>

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AC8 PCIE_CALRP — R55 1 2 1.27K 0402 1%
AB8 PCIE_CALRN — R56 1 2 2K 0402 1%
+1.1VS

< TX Impedance Calibration. Connect to GND >
< RX Impedance Calibration. Connect to VDDPCIE >

RS780MCR3@ RS780M_FCBGA528

U3A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

H_CADOP[0..15] → H_CADOP[0..15] 5
H_CADON[0..15] → H_CADON[0..15] 5

HT_RXCAD	Pin	H_CADO	HT_TXCAD	Pin	H_CADI
HT_RXCAD0P/N	Y25/Y24	H_CADOP0/N0	HT_TXCAD0P/N	D24/D25	H_CADIN0/P0
HT_RXCAD1P/N	V22/V23	H_CADOP1/N1	HT_TXCAD1P/N	E24/E25	H_CADIN1/P1
HT_RXCAD2P/N	V25/V24	H_CADOP2/N2	HT_TXCAD2P/N	F24/F25	H_CADIN2/P2
HT_RXCAD3P/N	U24/U25	H_CADOP3/N3	HT_TXCAD3P/N	F23/F22	H_CADIN3/P3
HT_RXCAD4P/N	T25/T24	H_CADOP4/N4	HT_TXCAD4P/N	H23/H22	H_CADIN4/P4
HT_RXCAD5P/N	P22/P23	H_CADOP5/N5	HT_TXCAD5P/N	J25/J24	H_CADIN5/P5
HT_RXCAD6P/N	P25/P24	H_CADOP6/N6	HT_TXCAD6P/N	K24/K25	H_CADIN6/P6
HT_RXCAD7P/N	N24/N25	H_CADOP7/N7	HT_TXCAD7P/N	K23/K22	H_CADIN7/P7
HT_RXCAD8P/N	AC24/AC25	H_CADOP8/N8	HT_TXCAD8P/N	F21/G21	H_CADIN8/P8
HT_RXCAD9P/N	AB25/AB24	H_CADOP9/N9	HT_TXCAD9P/N	G20/H21	H_CADIN9/P9
HT_RXCAD10P/N	AA24/AA25	H_CADOP10/N10	HT_TXCAD10P/N	J20/J21	H_CADIN10/P10
HT_RXCAD11P/N	Y22/Y23	H_CADOP11/N11	HT_TXCAD11P/N	J18/K17	H_CADIN11/P11
HT_RXCAD12P/N	W21/W20	H_CADOP12/N12	HT_TXCAD12P/N	L19/J19	H_CADIN12/P12
HT_RXCAD13P/N	V21/V20	H_CADOP13/N13	HT_TXCAD13P/N	M19/L18	H_CADIN13/P13
HT_RXCAD14P/N	U20/U21	H_CADOP14/N14	HT_TXCAD14P/N	M21/P21	H_CADIN14/P14
HT_RXCAD15P/N	U19/U18	H_CADOP15/N15	HT_TXCAD15P/N	P18/M18	H_CADIN15/P15

H_CADIP[0..15] → H_CADIP[0..15] 5
H_CADIN[0..15] → H_CADIN[0..15] 5

< From S1G3 CPU : x16 HT>

< To S1G3 CPU : x16 HT>

HT_RXCLK	Pin	H_CLKO	HT_TXCLK	Pin	H_CLKI
HT_RXCLK0P/N	T22/T23	H_CLKOP0/N0	HT_TXCLK0P/N	H24/H25	H_CLKIN0/P0
HT_RXCLK1P/N	AB23/AA22	H_CLKOP1/N1	HT_TXCLK1P/N	L21/L20	H_CLKIN1/P1

HT_RXCTL	Pin	H_CTLO	HT_TXCTL	Pin	H_CTLI
HT_RXCTL0P/N	M22/M23	H_CTLOP0/N0	HT_TXCTL0P/N	M24/M25	H_CTLIN0/P0
HT_RXCTL1P/N	R21/R20	H_CTLOP1/N1	HT_TXCTL1P/N	P19/R18	H_CTLIN1/P1

HT_RXCALP — R57 1 2 301_0402_1% — C23
HT_RXCALN — A24

HT_TXCALP — R58 1 2 301_0402_1% — B24
HT_TXCALN — B25

< Transmitter Calibration Resistor to HT_TXCALN >

0718 Place within 1" layout 1:2

RS780MCR3@RS780M_FCBGA528

0718 Place within 1" layout 1:2

NEED CHECK R57 & R58 WITH AMD

RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3	AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7	AUX1 and HPD1

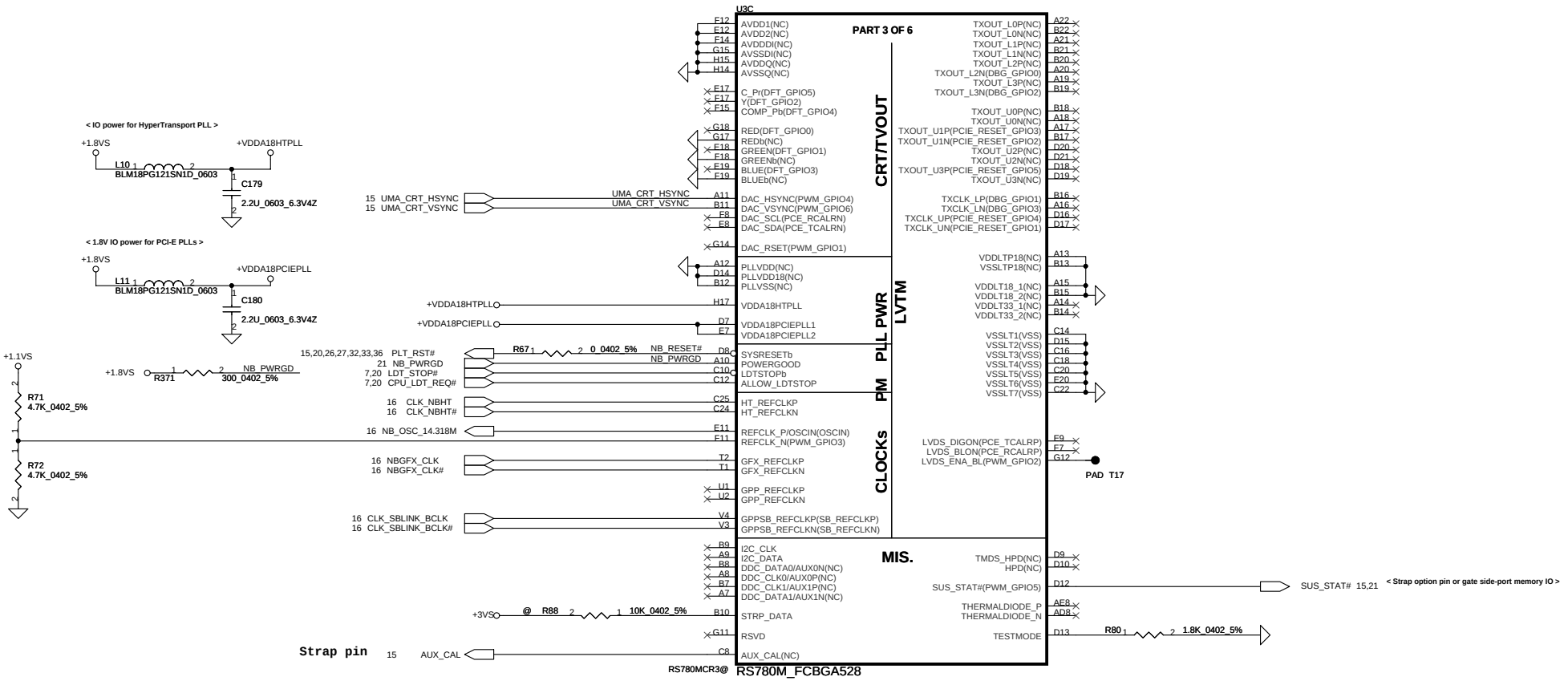
Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

Title: Schematic, M/B LA-5331P

Size	Document Number	Rev
Custom	401716	C

Date: Tuesday, February 23, 2010 Sheet 11 of 54



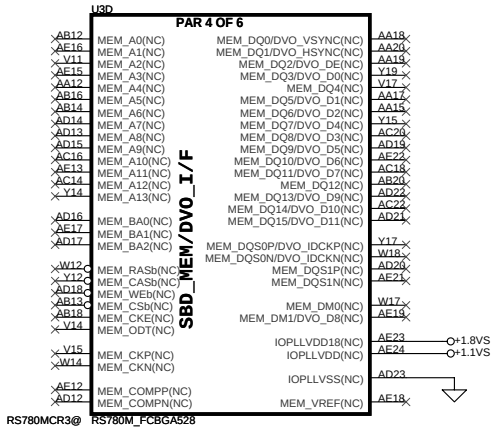
Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

Size	Document Number	Rev
Custom	401716	C

Date: Tuesday, February 23, 2010 | Sheet 12 of 54



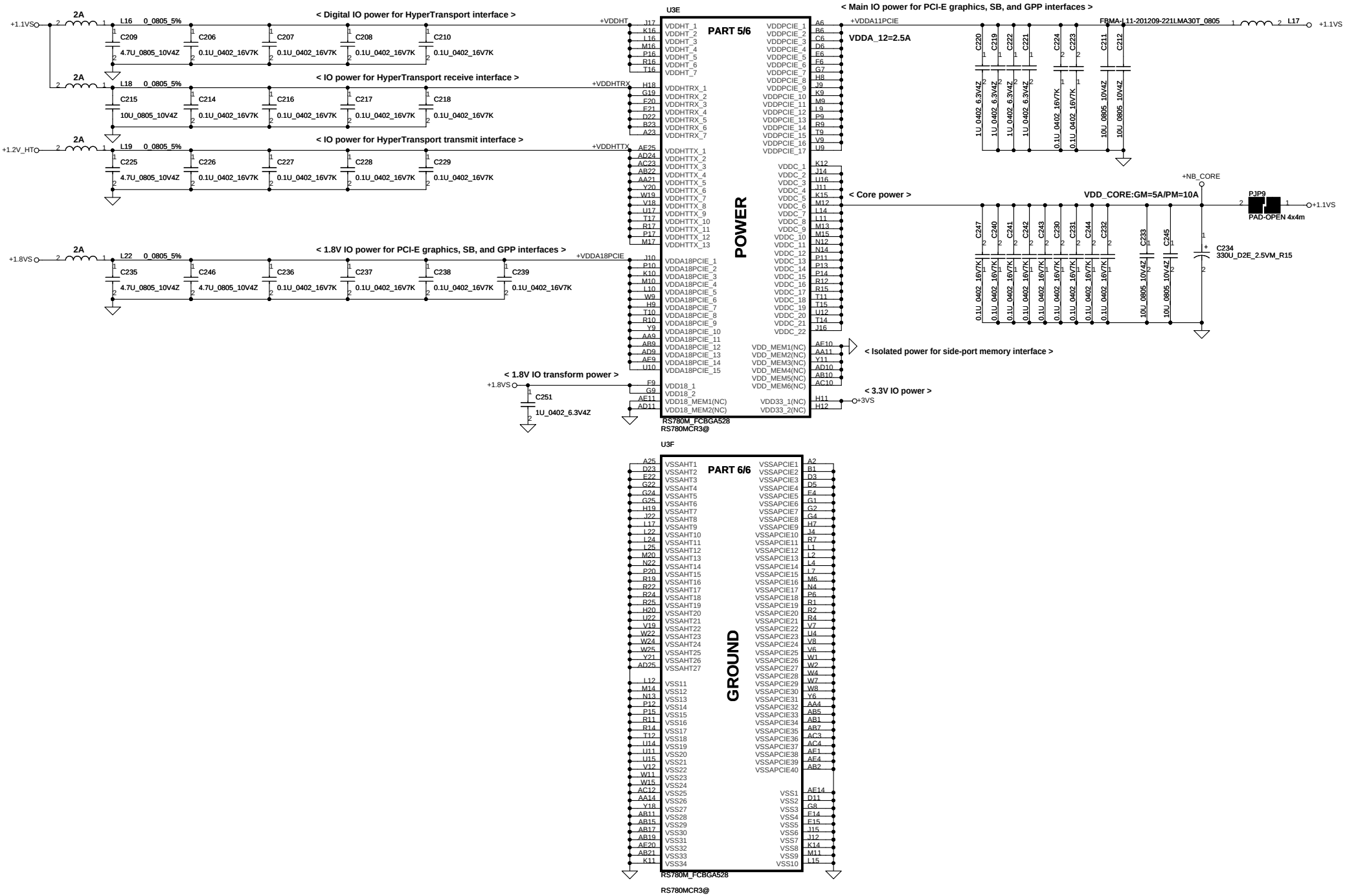
Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

Size	Document Number	Rev
Custom	401716	C

Date: Tuesday, February 23, 2010 | Sheet 13 of 54



Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.	
Title	Schematic, M/B LA-5331P
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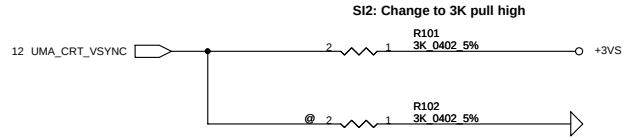
< RX881 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC:STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Enable (RX881, RS880)
0 : Disable (RX881, RS880)

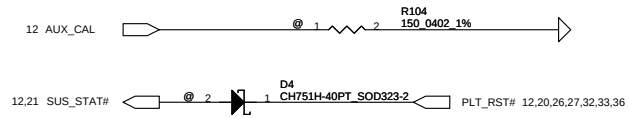
PIN: RS880--> VSYNC#

< RX881 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RX881 SUS_STAT# >



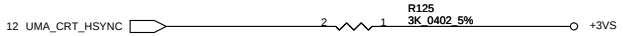
< SUS_STAT# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RX881:SUS_STAT#

< RX881 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC: STRAP_DEBUG_BUS_PCIE_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)
0 : Enable (RS780)

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Compal Electronics, Inc.		
Title: Schematic, M/B LA-5331P		
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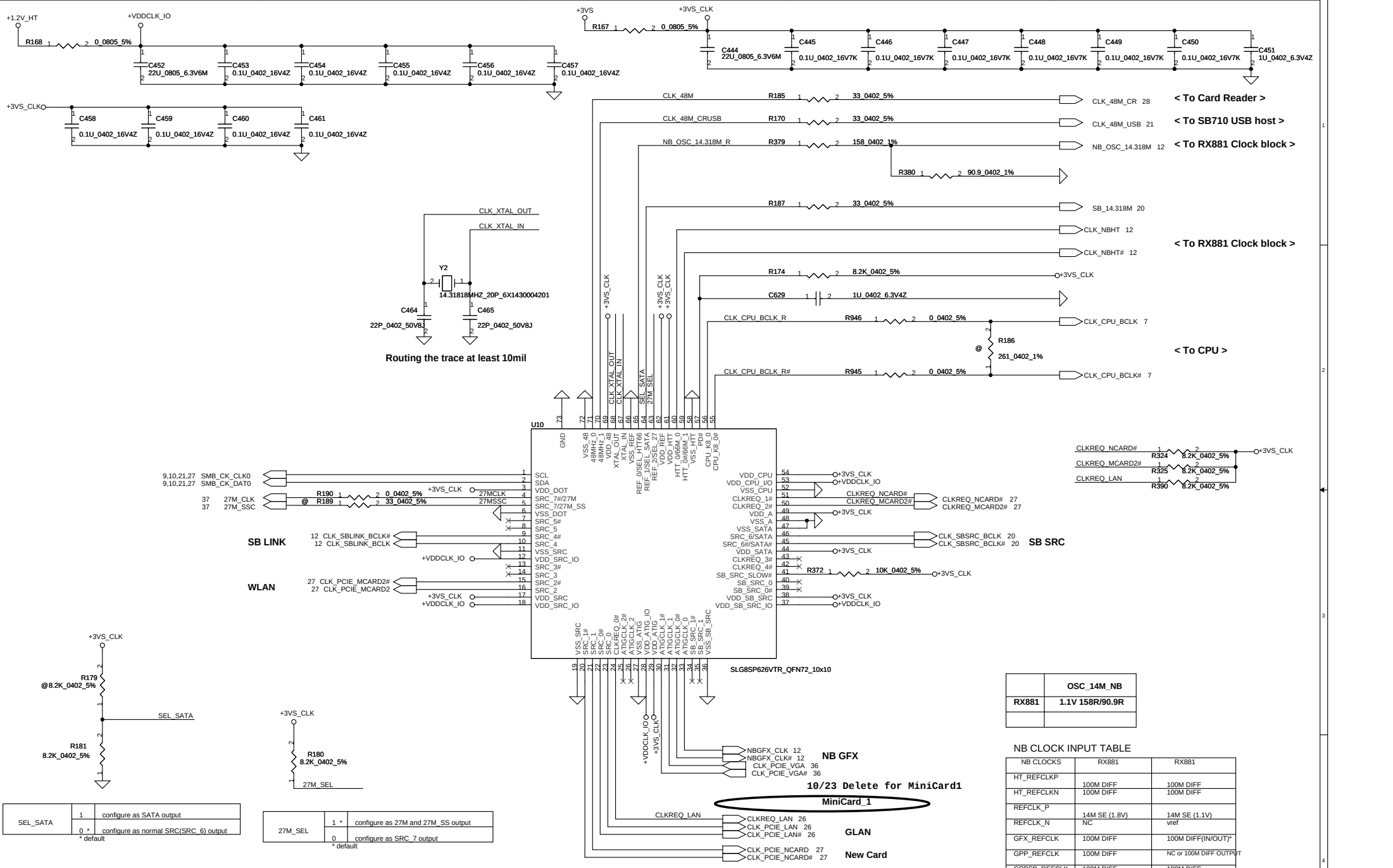

	OSC_14M_NB
RX881	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX881	RX881
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

SEL_SATA		
	1	configure as SATA output
	0 *	configure as normal SRC(SRC_6) output

* default

27M_SEL		
	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M		
	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output

* default

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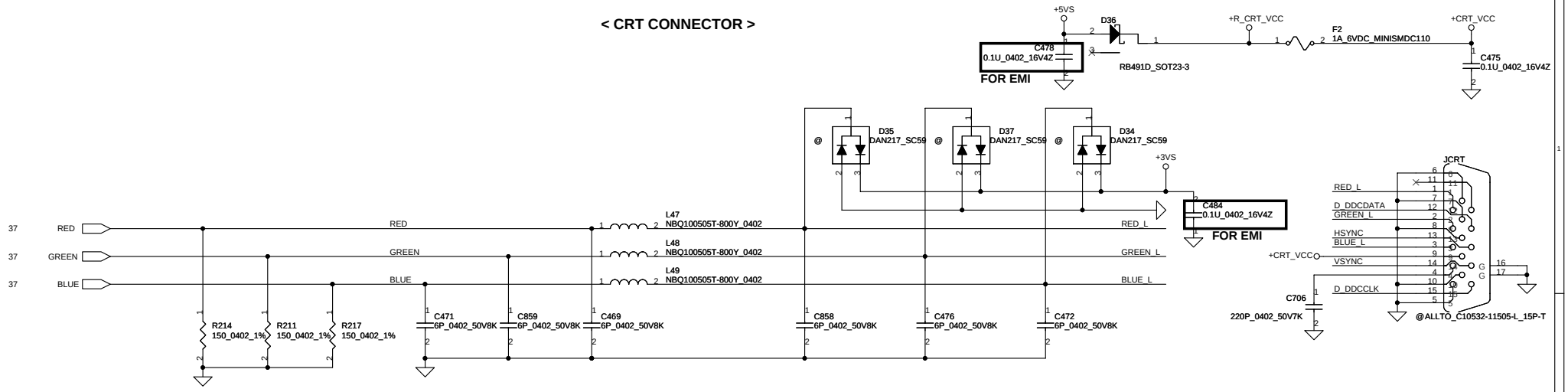
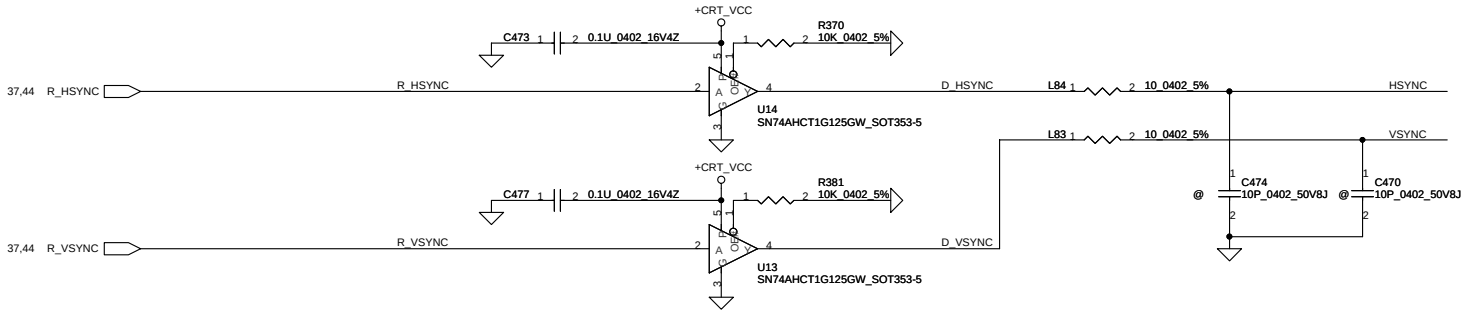
< CRT CONNECTOR >

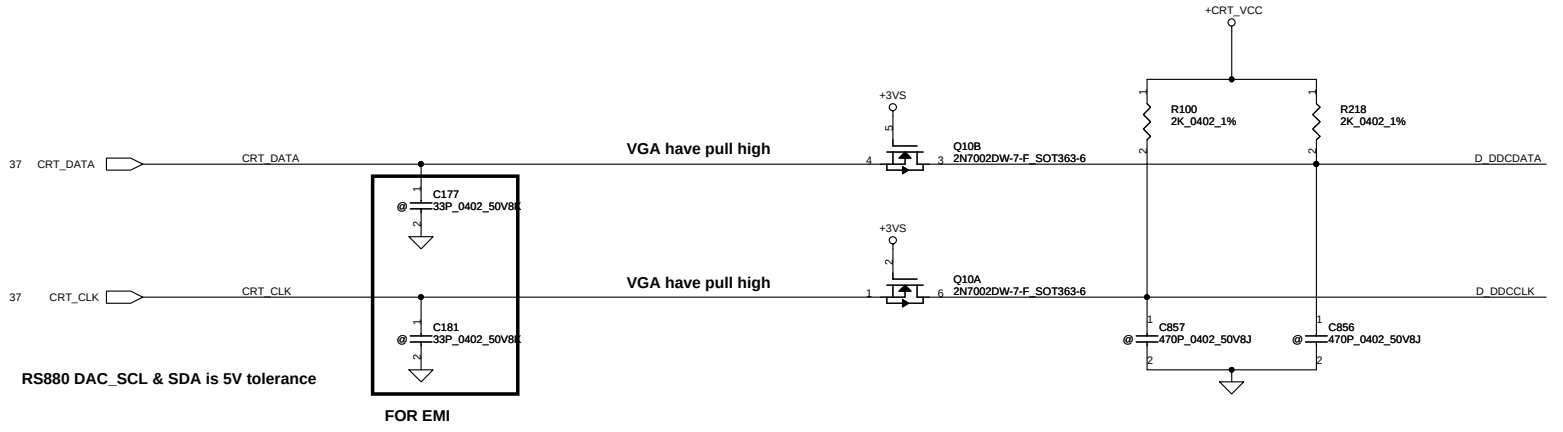


RS780 use 140 ohm, check RS880 use what value

< SYNC SIGNAL >



< Display Data Channel >



RS880 DAC_SCL & SDA is 5V tolerance

FOR EMI

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Title	Schematic, M/B LA-5331P
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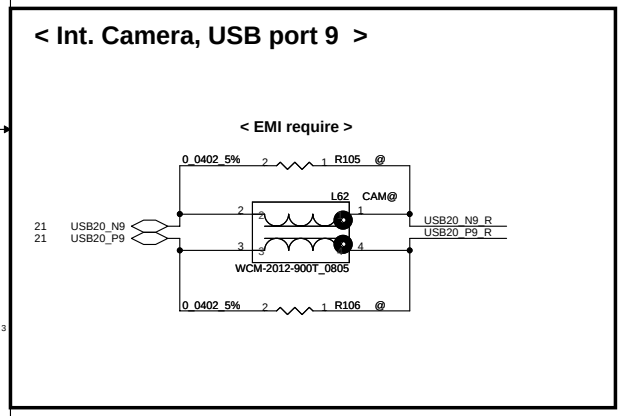
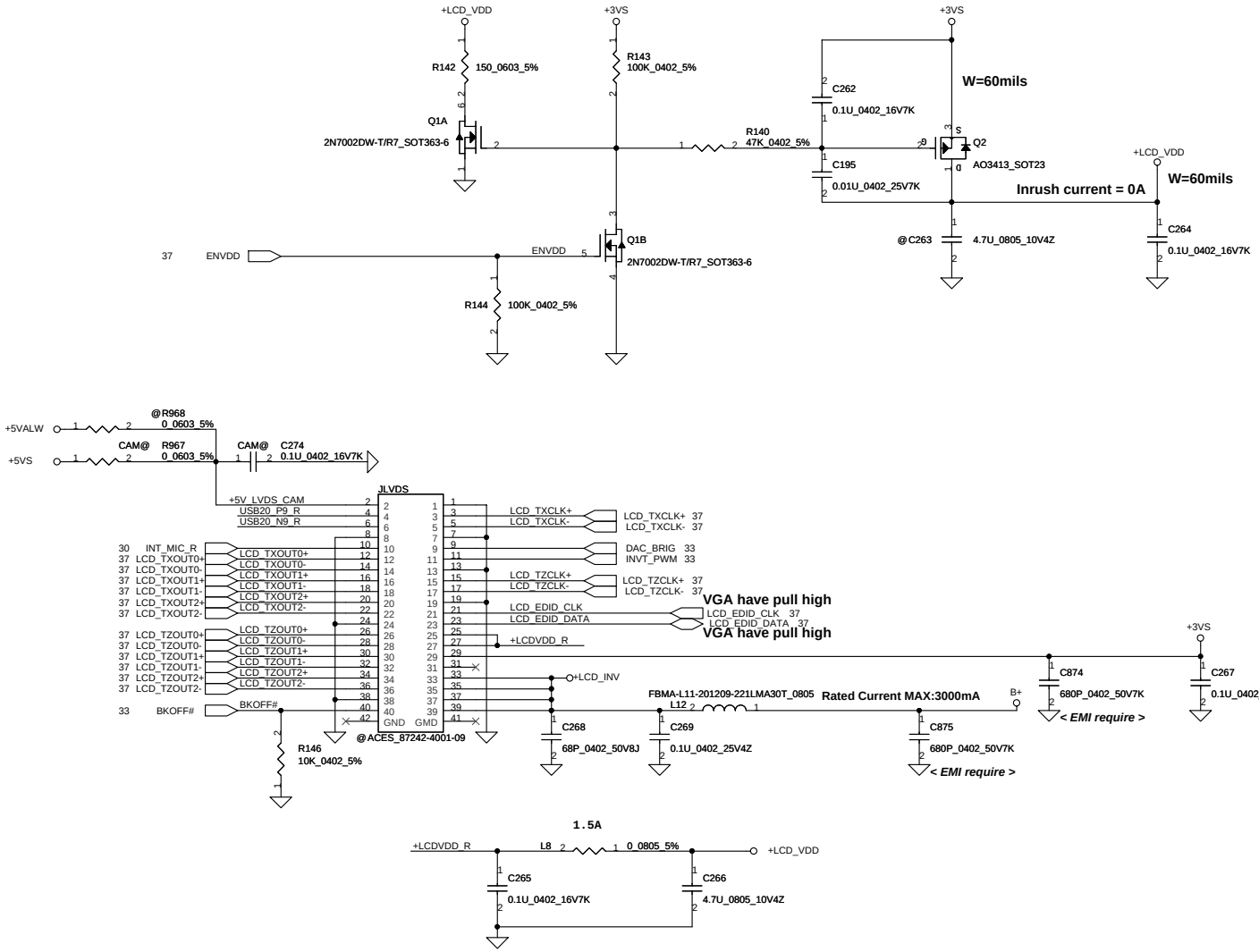
LCD/PANEL BD. Conn.





Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

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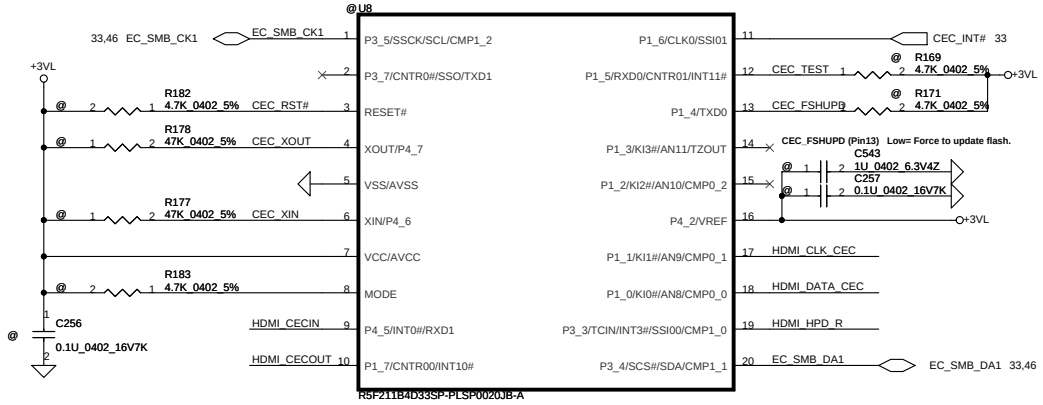
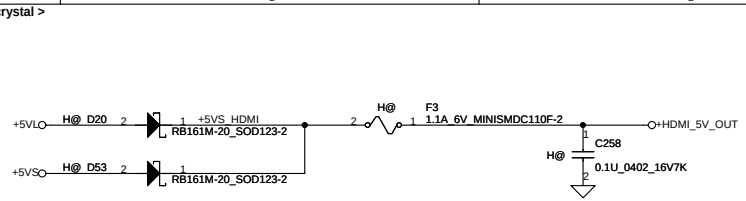
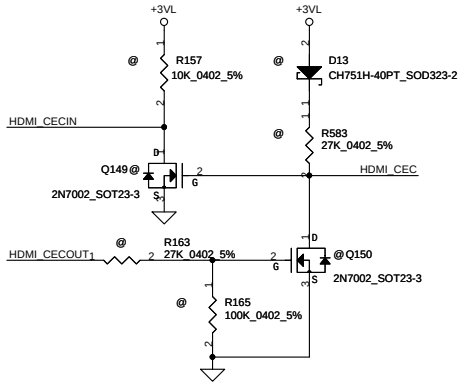
< HDMI CEC Controller >



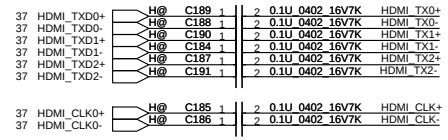
< Power, reset and crystal >



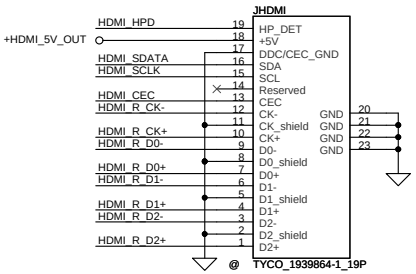
< HDMI_CEC level shift>Place MOSFET close to HDMI connector >



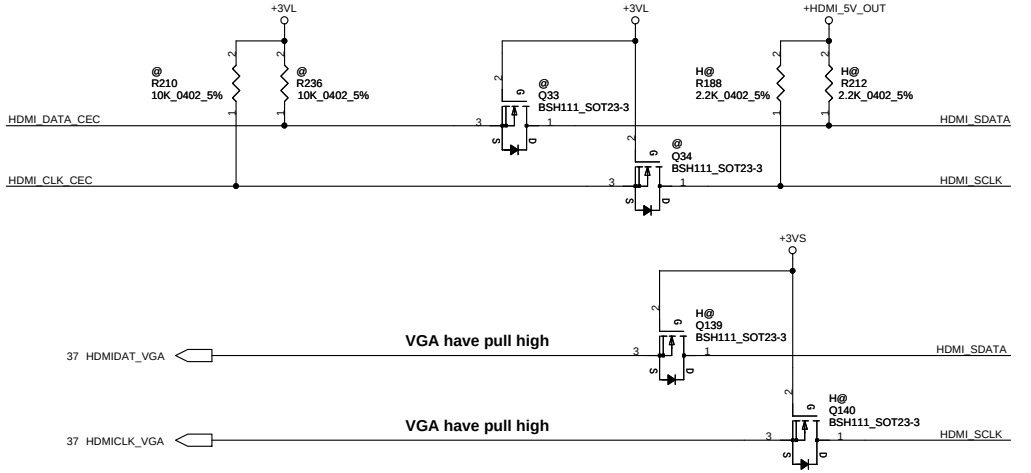
SI:Add R616~R624 for EMI requset



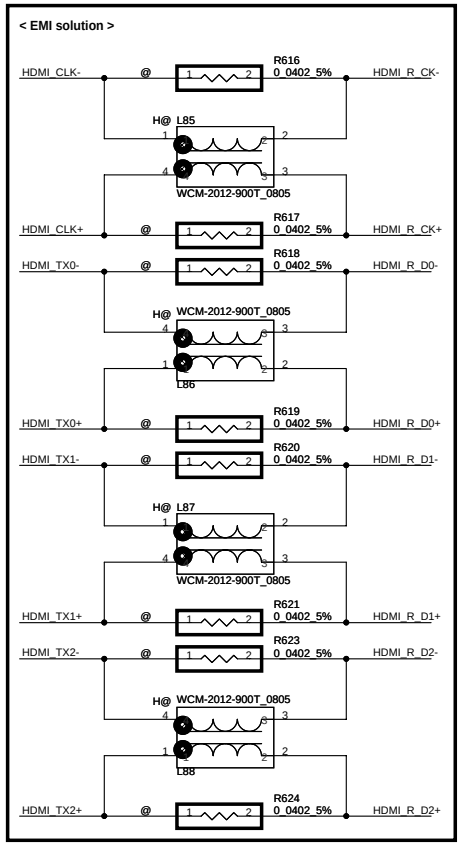
< HDMI Connector >



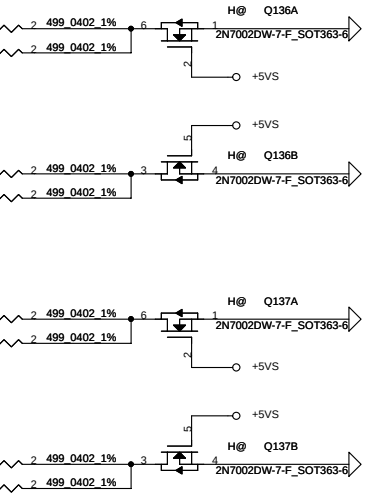
< HDMI DDC channel to device >



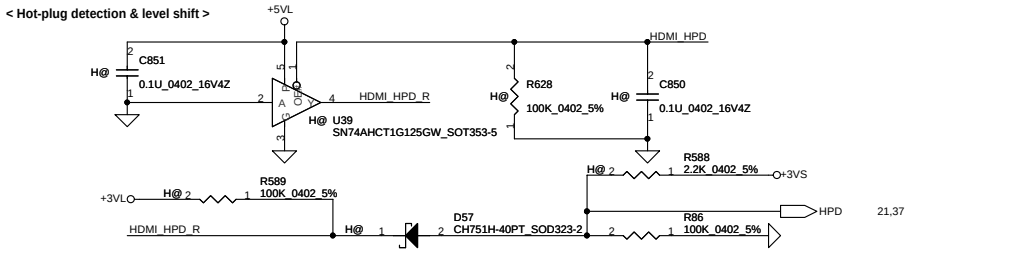
< EMI solution >



< Termination resistor >



< Hot-plug detection & level shift >



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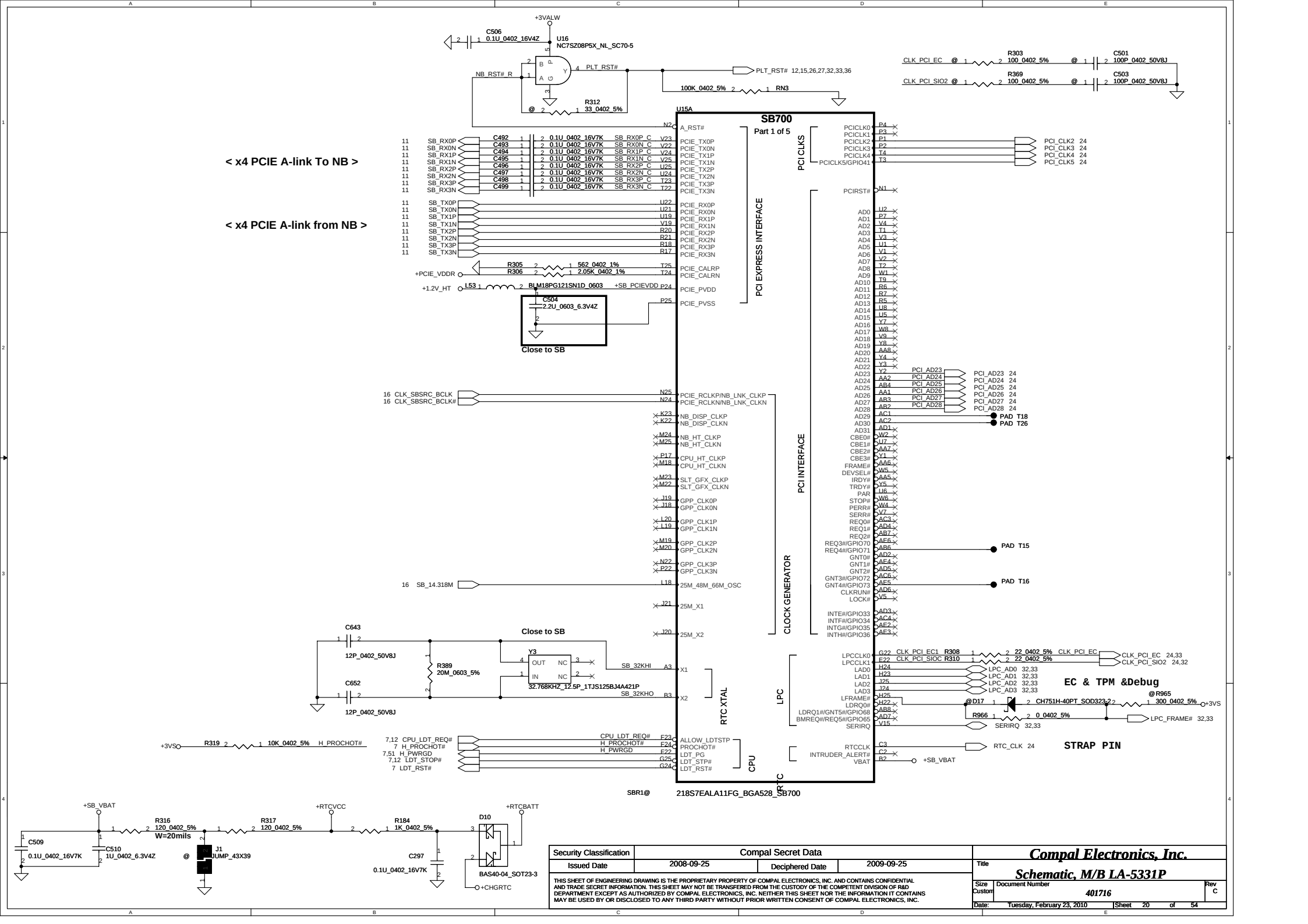

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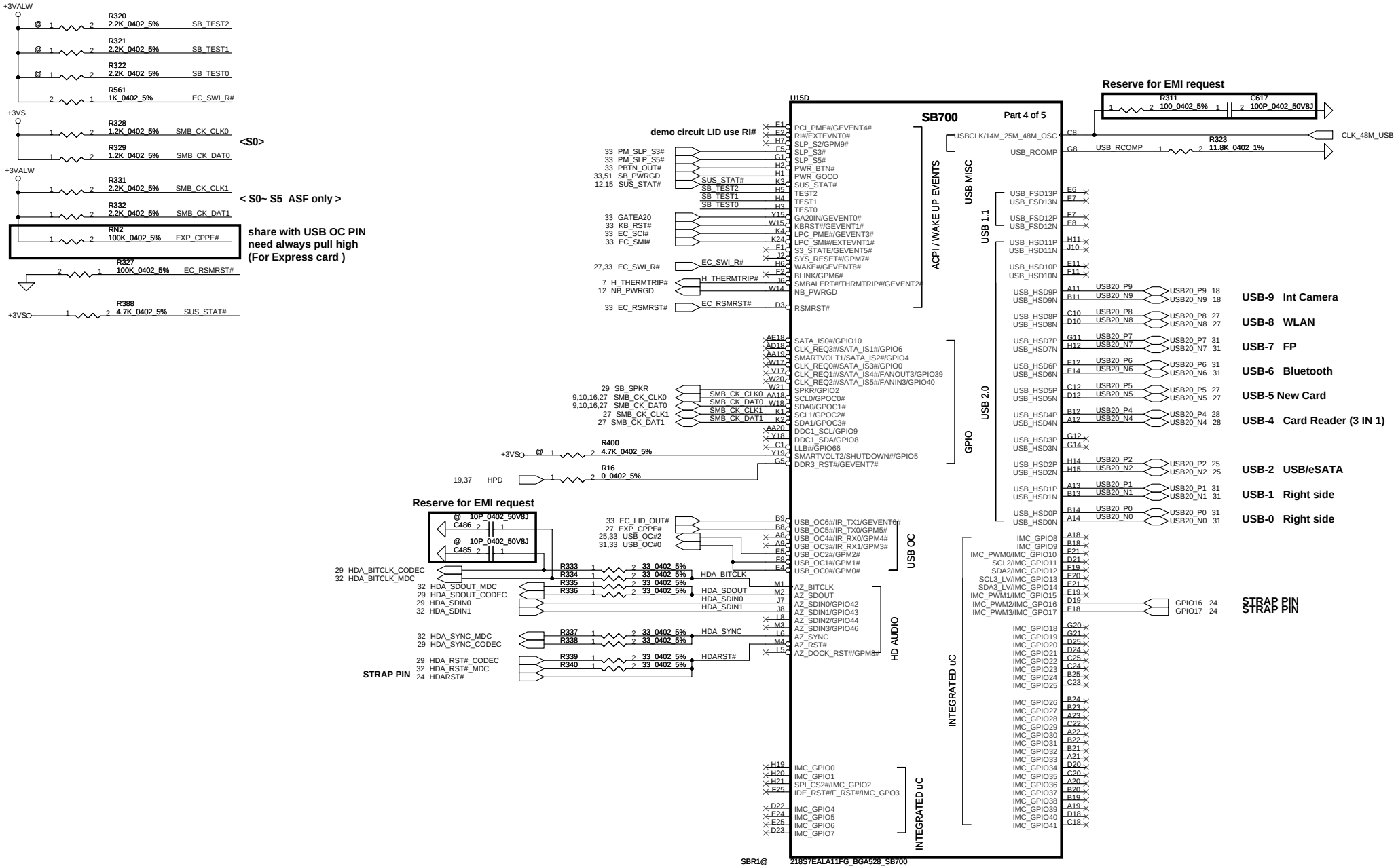

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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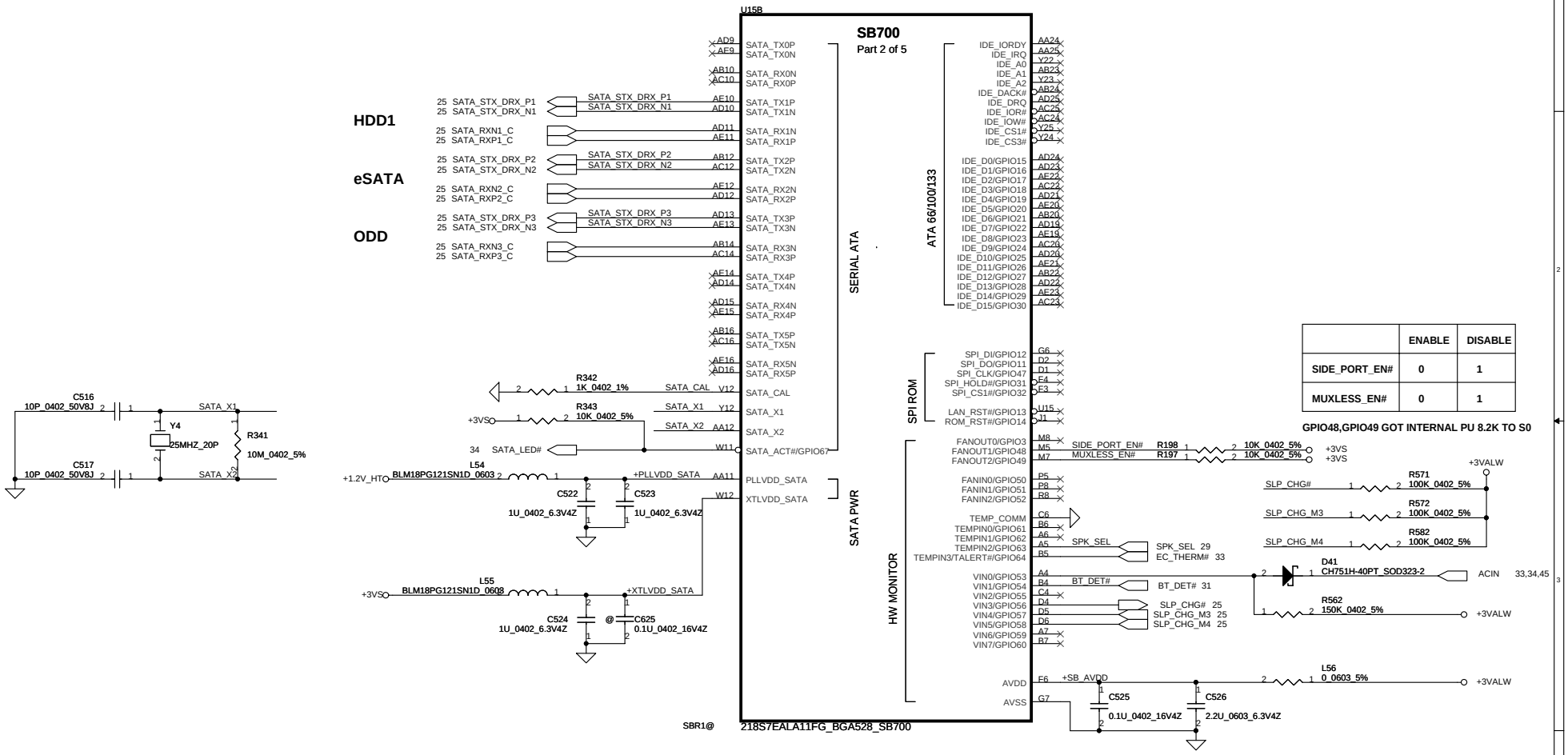

	ENABLE	DISABLE
SIDE_PORT_EN#	0	1
MUXLESS_EN#	0	1

GPIO48,GPIO49 GOT INTERNAL PU 8.2K TO S0

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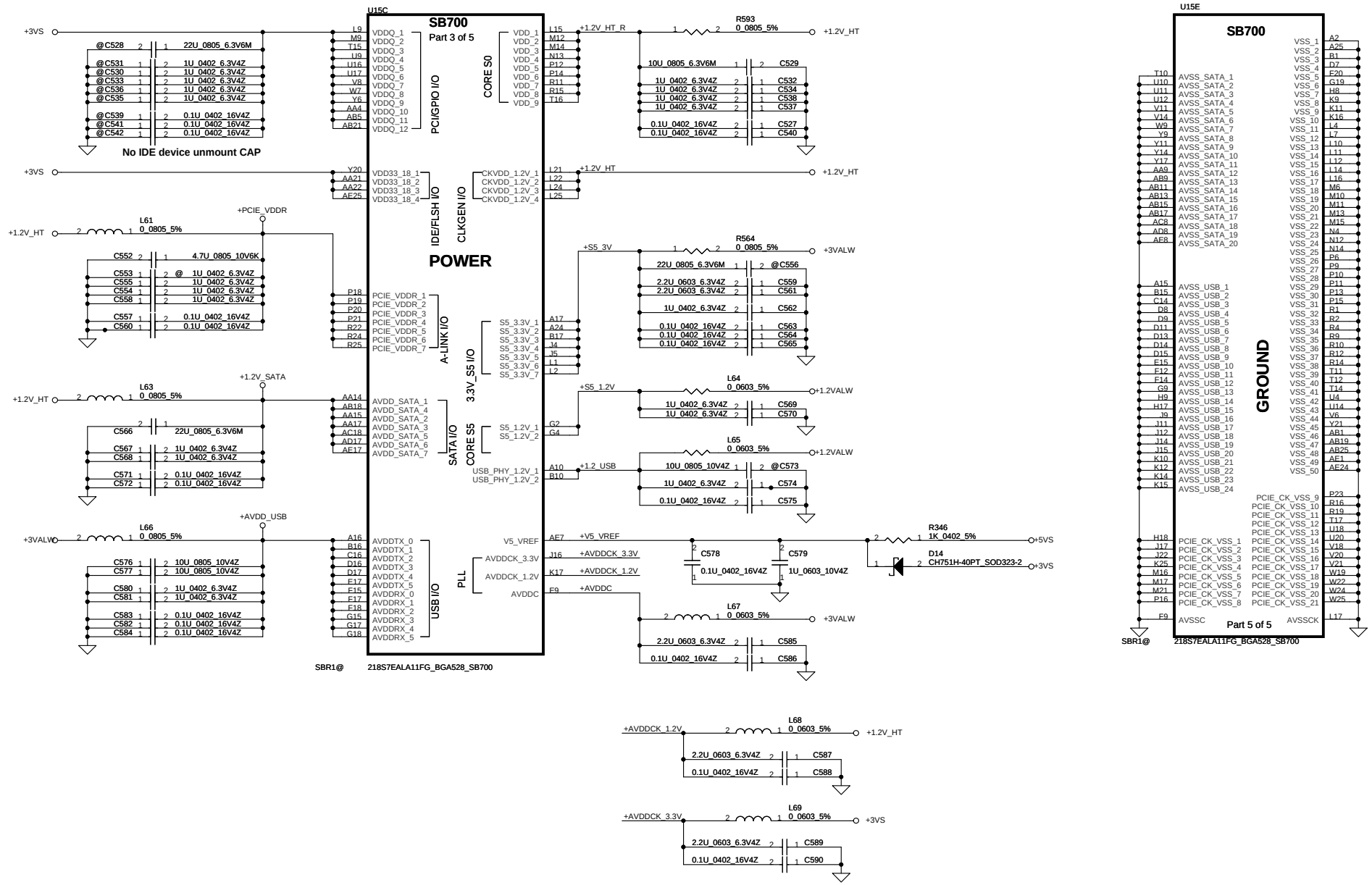

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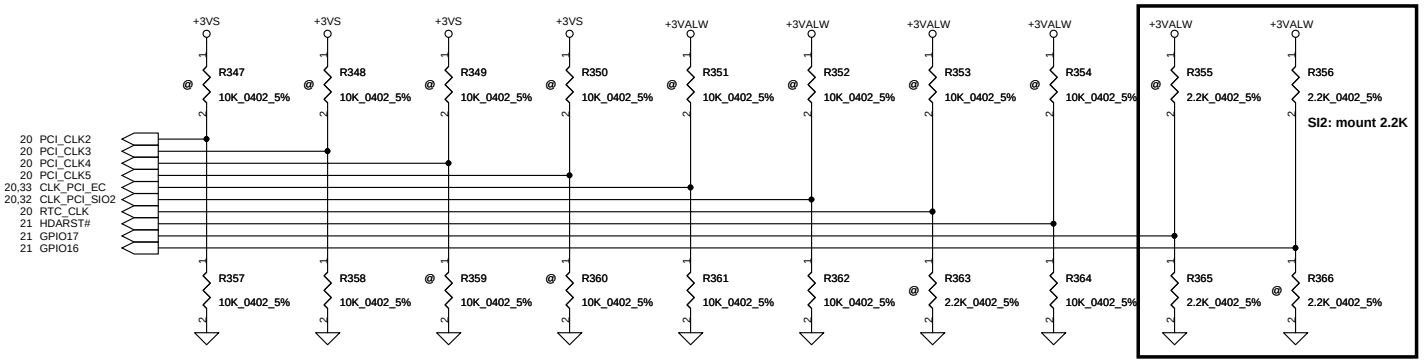
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

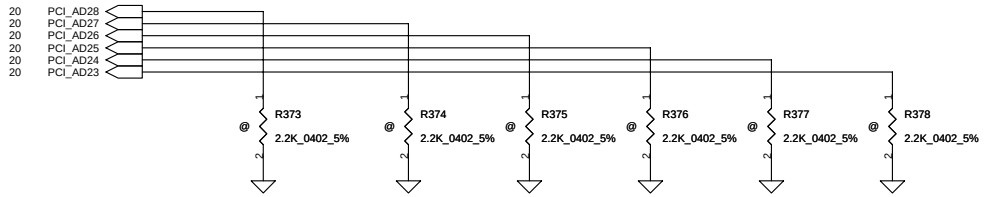


Need to confirm if SB SPI ROM will mount

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



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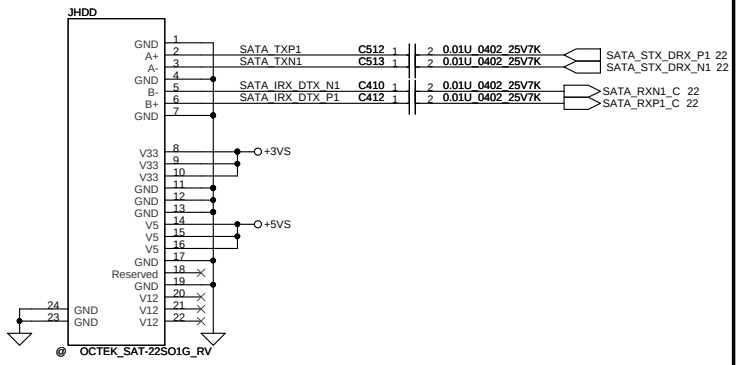
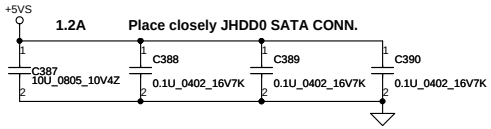
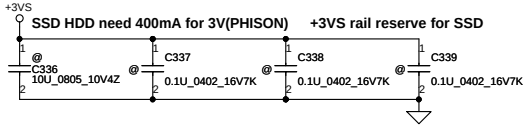
< SATA HDD1 Conn >







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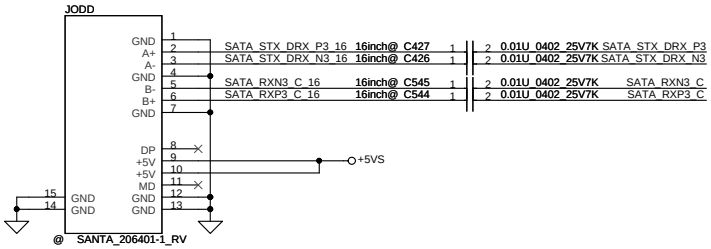
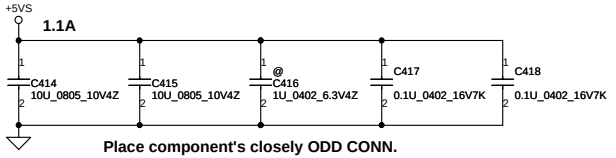
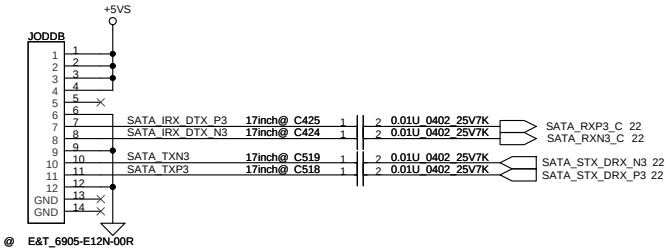


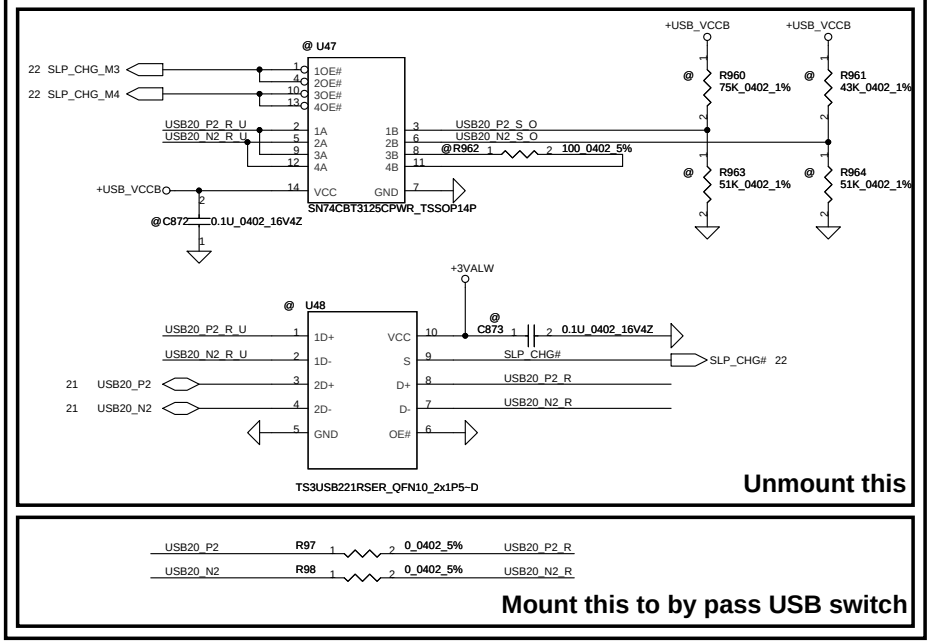


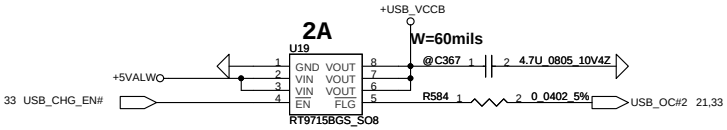
< 17" SATA ODD Conn >

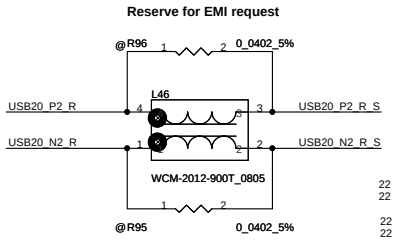


< eSATA/USB >

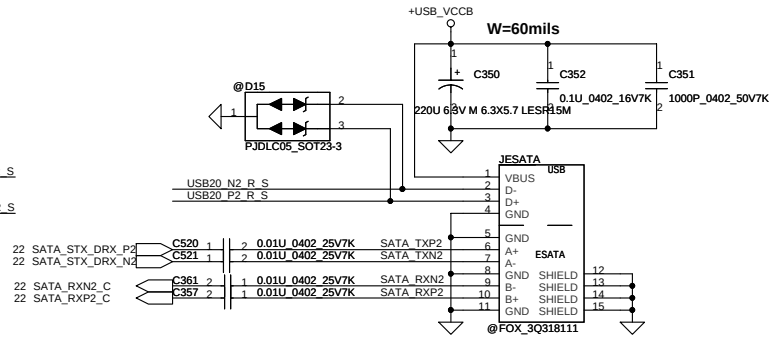
10/22 Add for USB Sleep & Charge M3/M4







eSATA/USB Conn



	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG#	FUNCTION
LOW	D=1D
HIGH	D=2D

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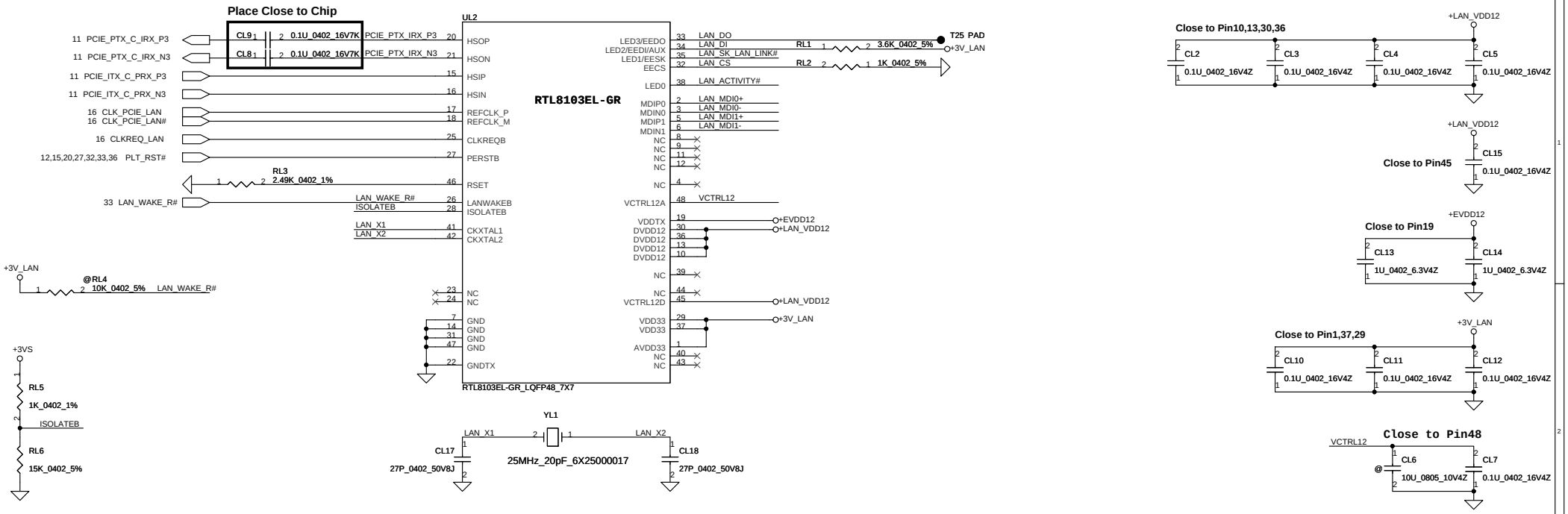

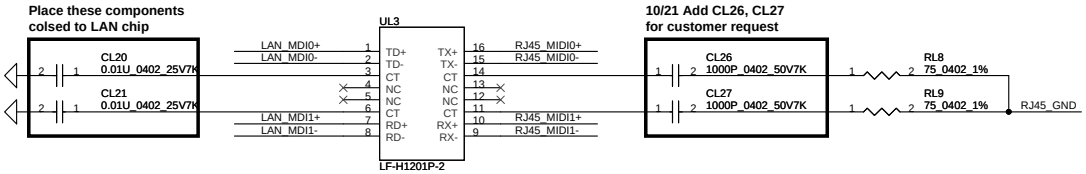

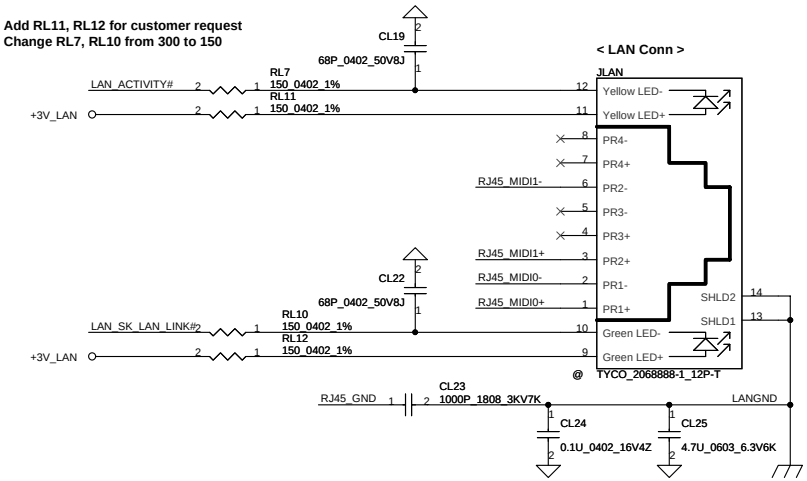

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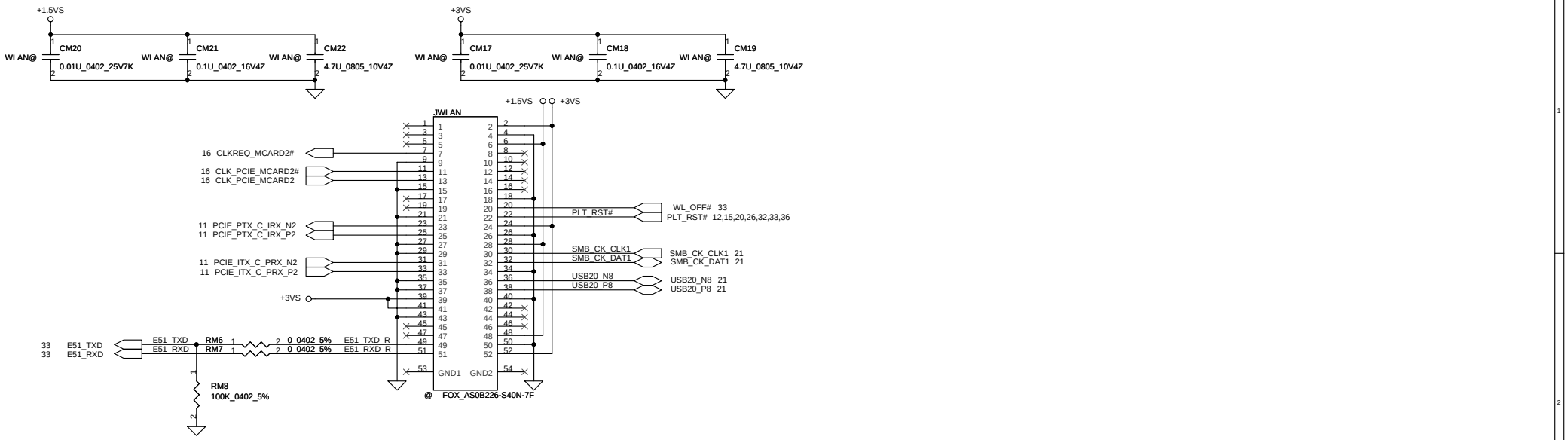
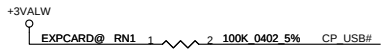
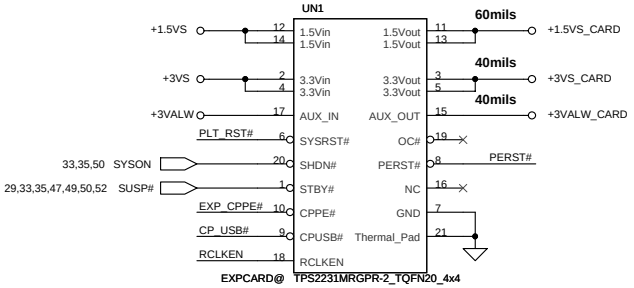
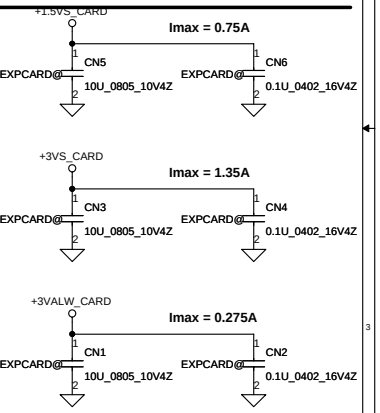
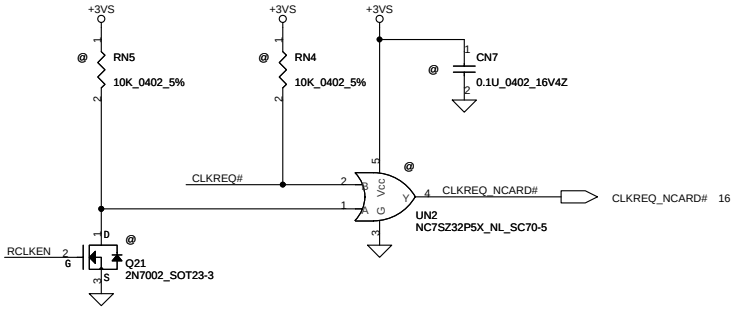
< PCIe Mini Card for WLAN >

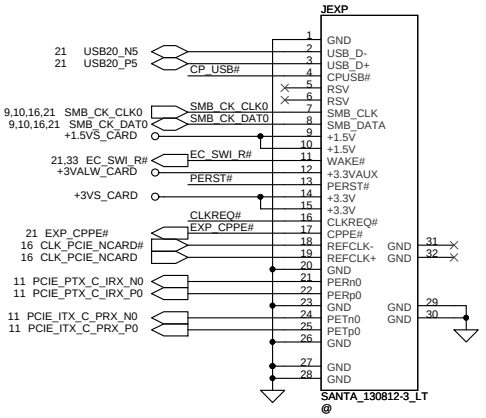




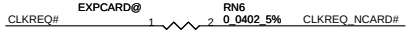








< Reserve for test >



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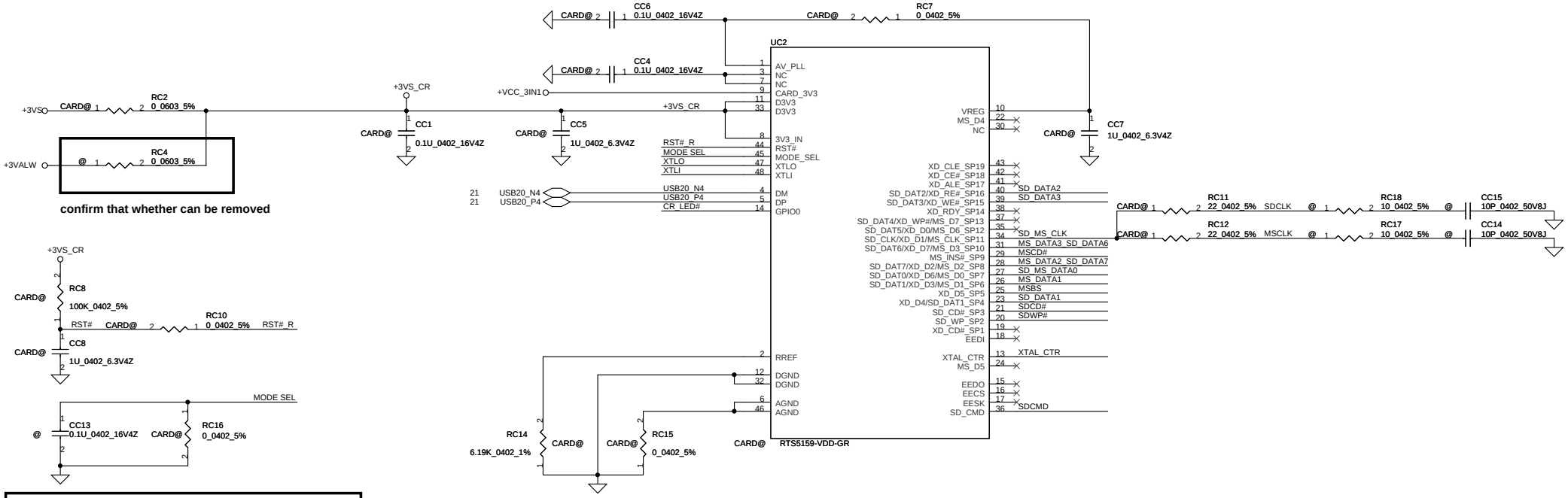
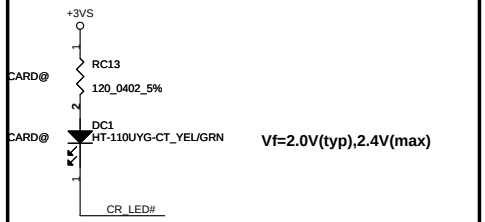
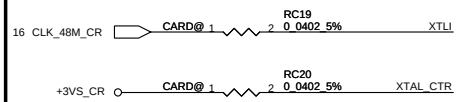


< Card Reader LED >

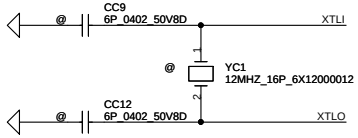


CR_LED: Low when card reader is being accessed.

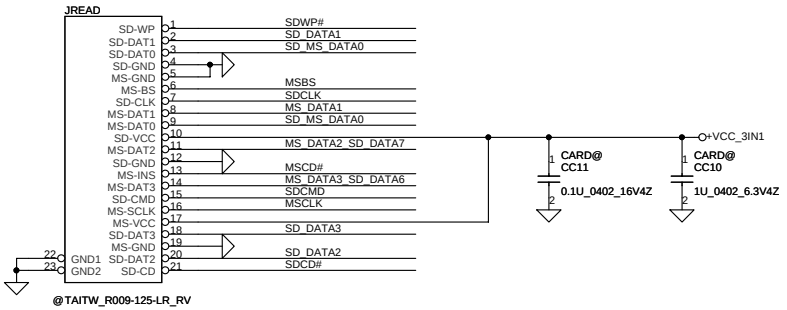
< 48MHz > Cost-down option



< 12MHz >



< 3 in 1 Card Reader >



R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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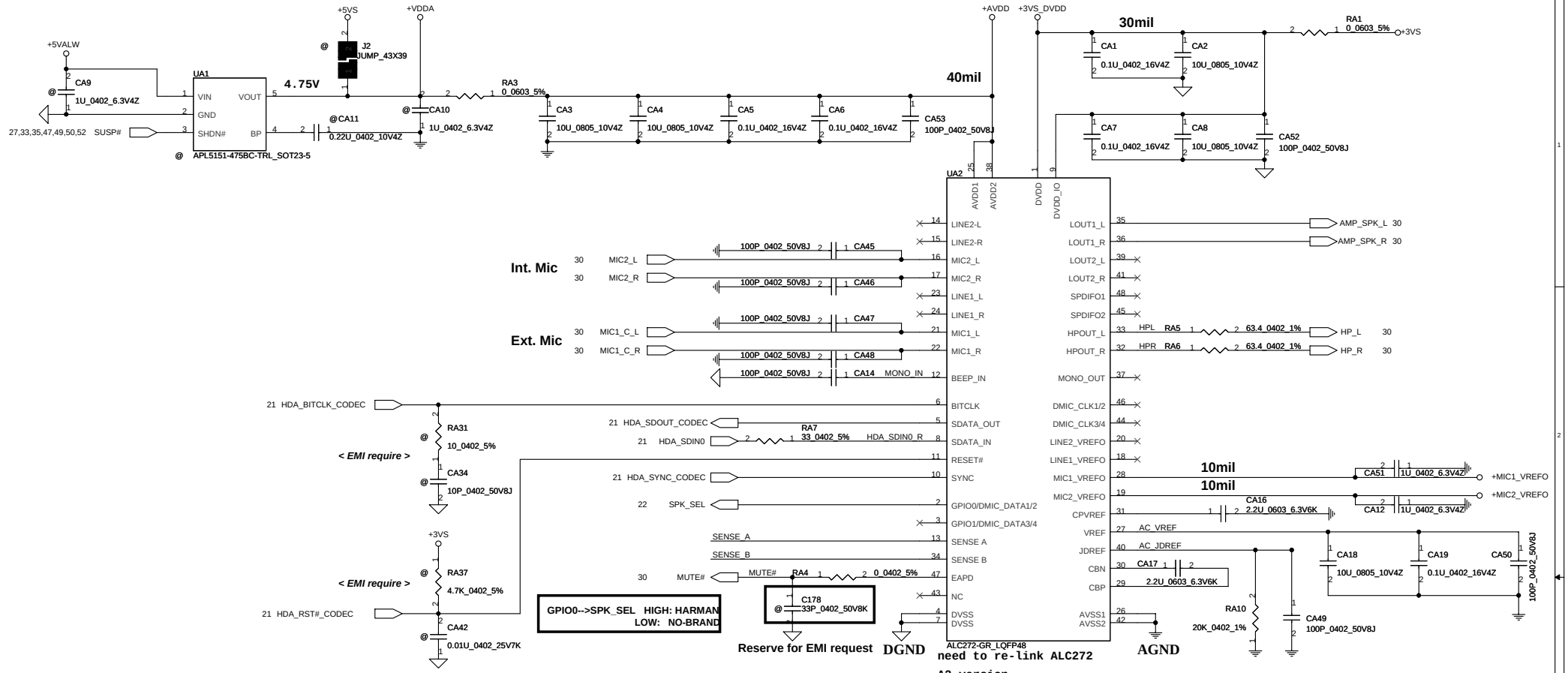
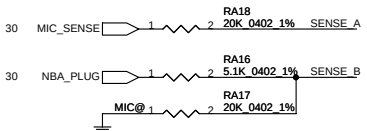
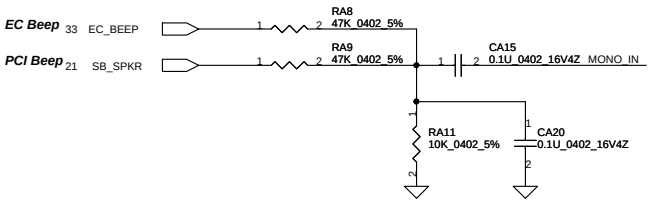


< SENSE_A & SENSE_B, place close to chip >



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

< MONO_IN SOURCE >



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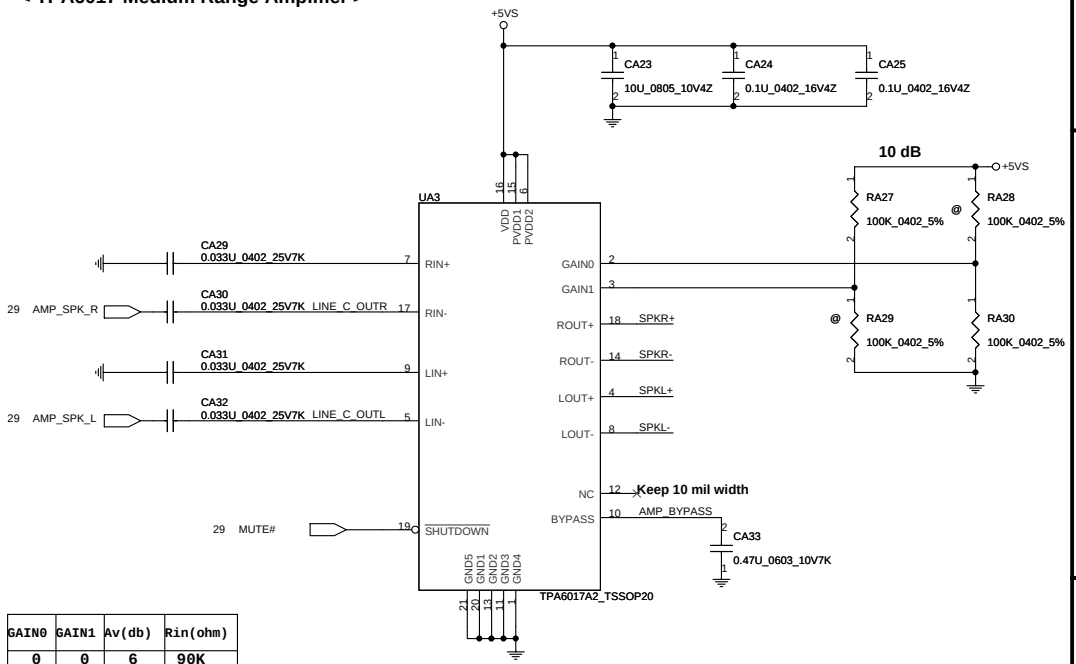
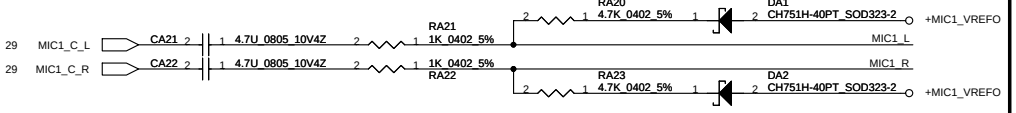
< TPA6017 Medium Range Amplifier >



GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

< Ext. Mic >



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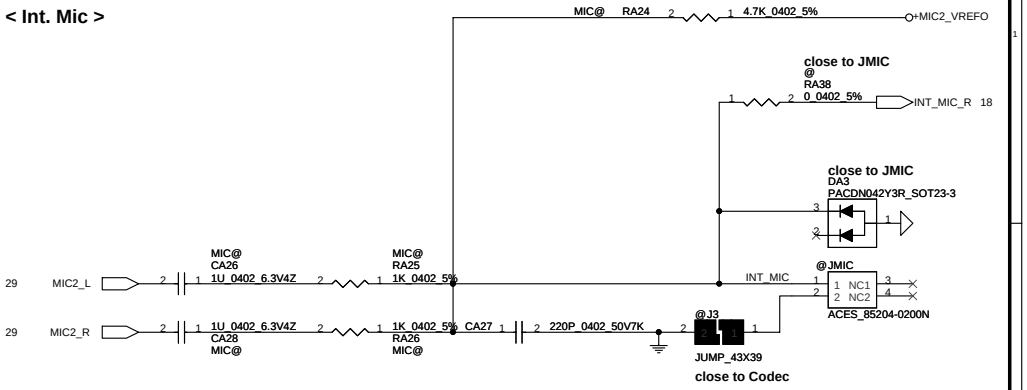
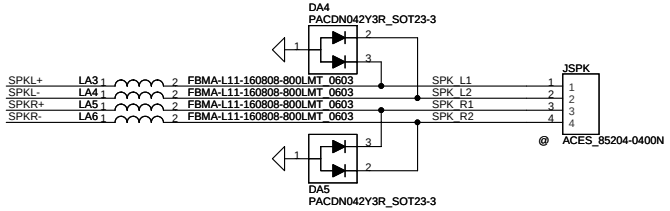
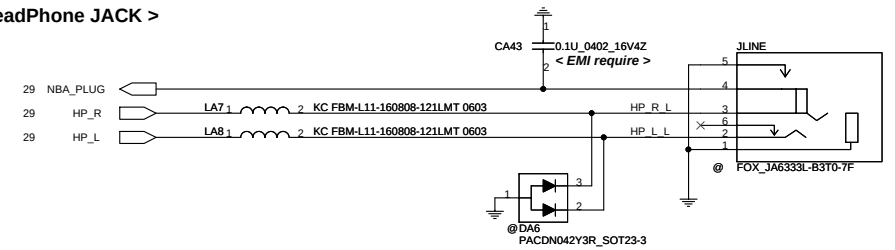


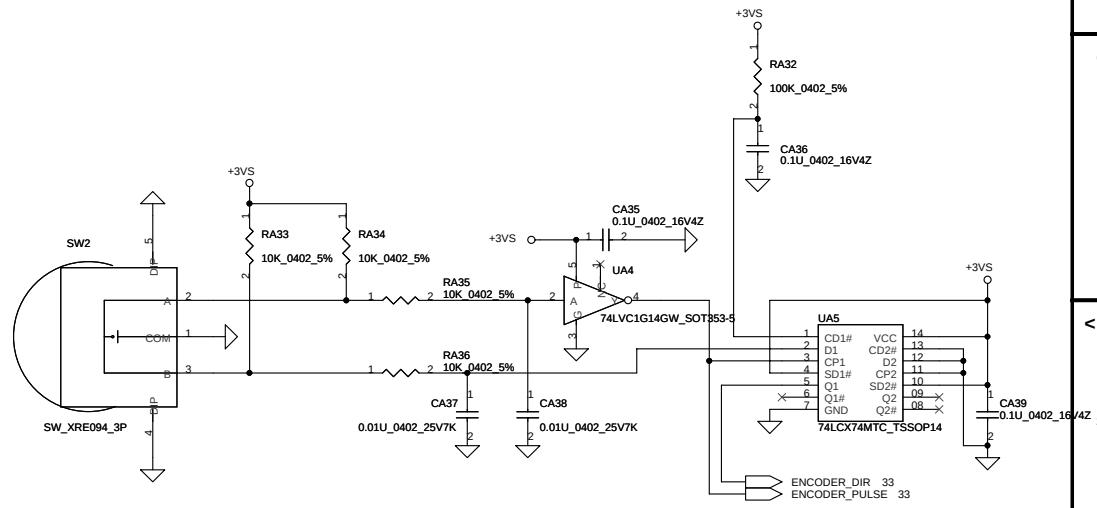
< Speaker Connector >



< HeadPhone JACK >



< Volume Control >



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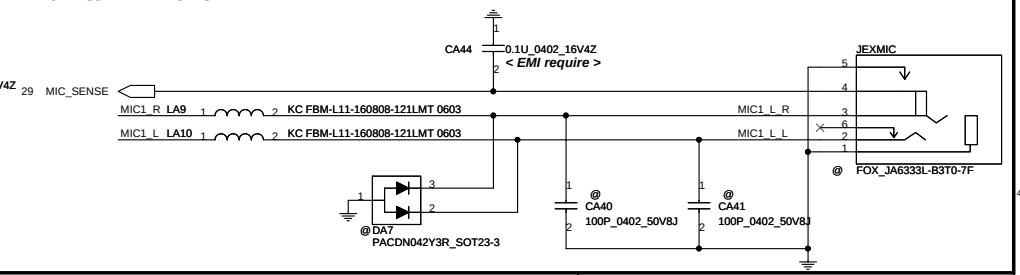

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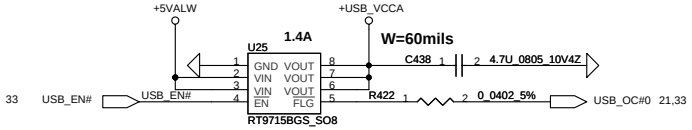
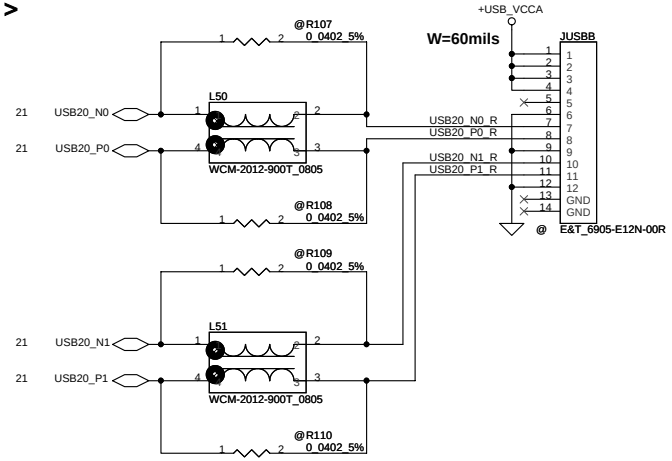
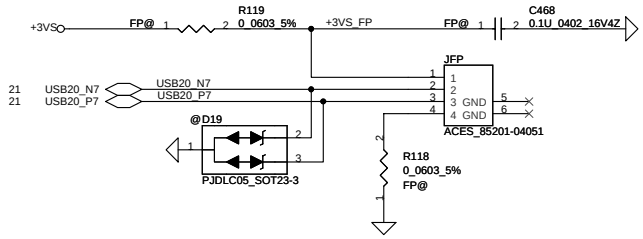
< USB Right-side Board, USB port 0,1 >



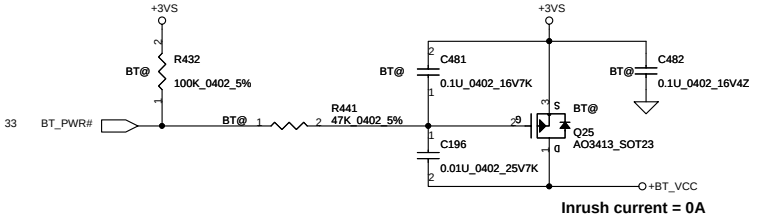
< Reserve for EMI request >



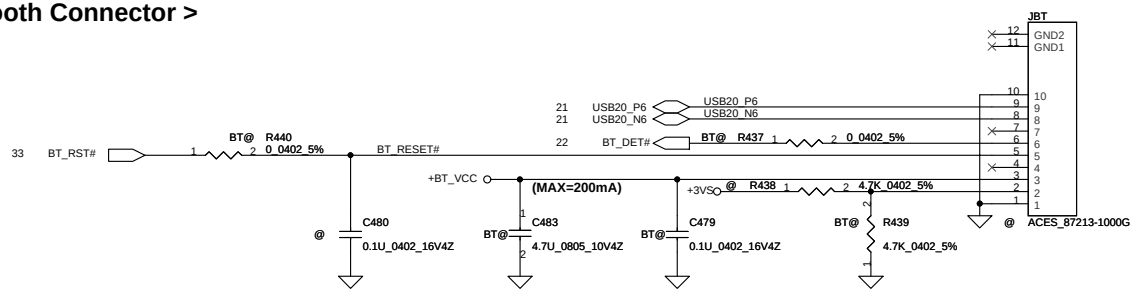
< Finger Printer, USB port 7 >



< BlueTooth Interface, USB port6 >



< Bluetooth Connector >



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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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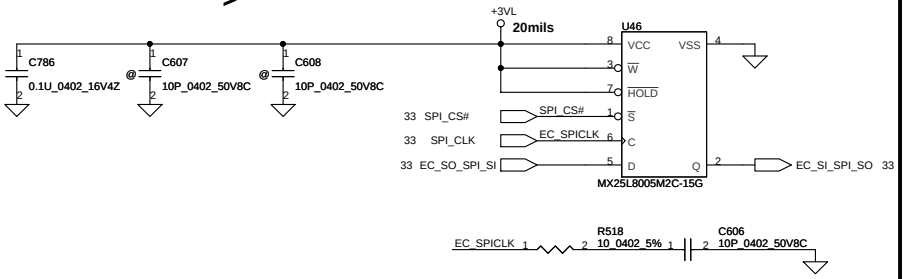
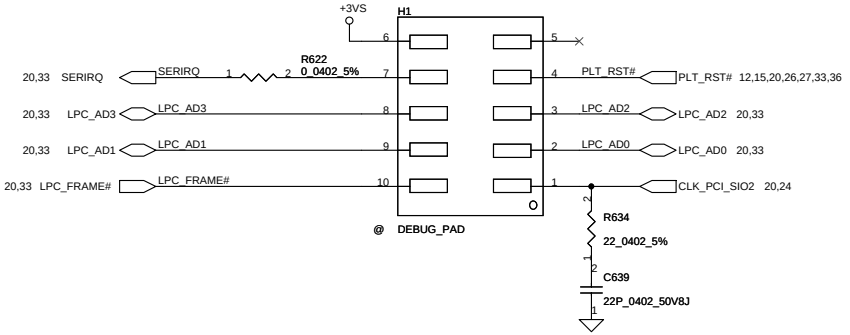
< SPI Flash 8Mb*1 >

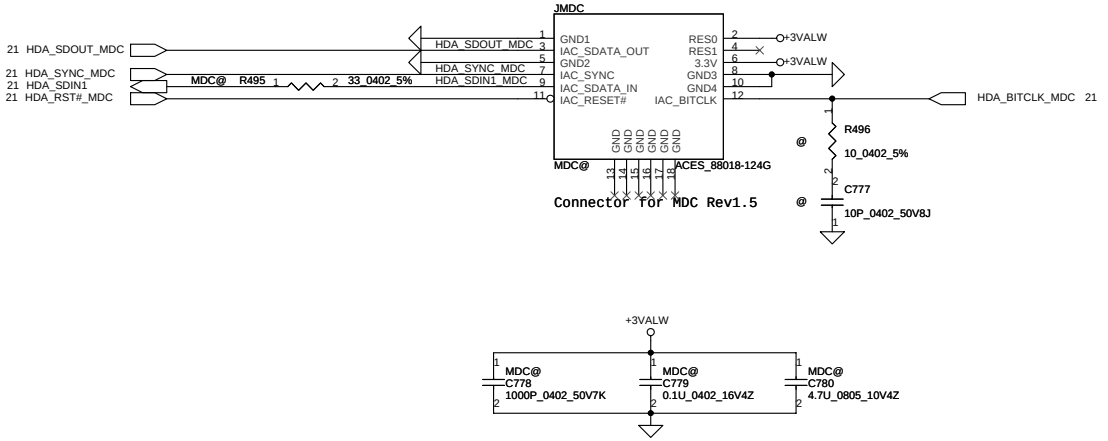


< LPC Debug Port >

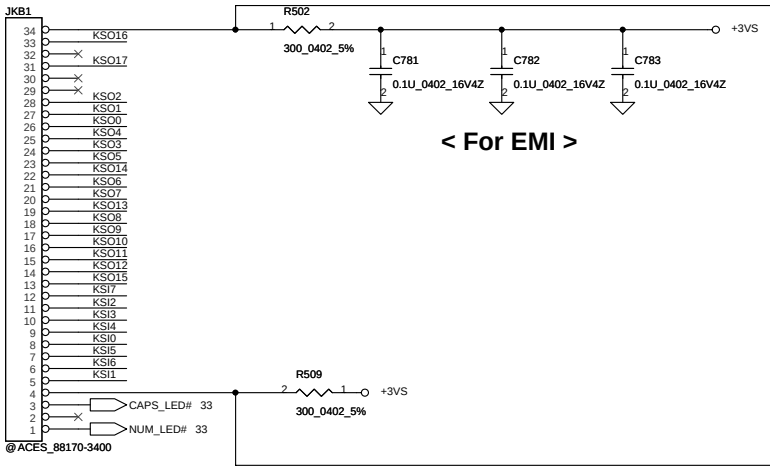
Please place the PAD under DDR DIMM.



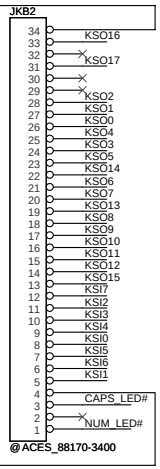
< MDC 1.5 Conn >



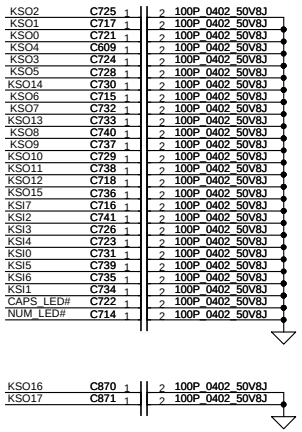
< KEYBOARD CONN 16" >



< KEYBOARD CONN 17" >



< For EMI >



KSI[0..7] KSI[0..7] 33,34

KSO[0..17] KSO[0..17] 33,34

Security Classification	Compal Secret Data		
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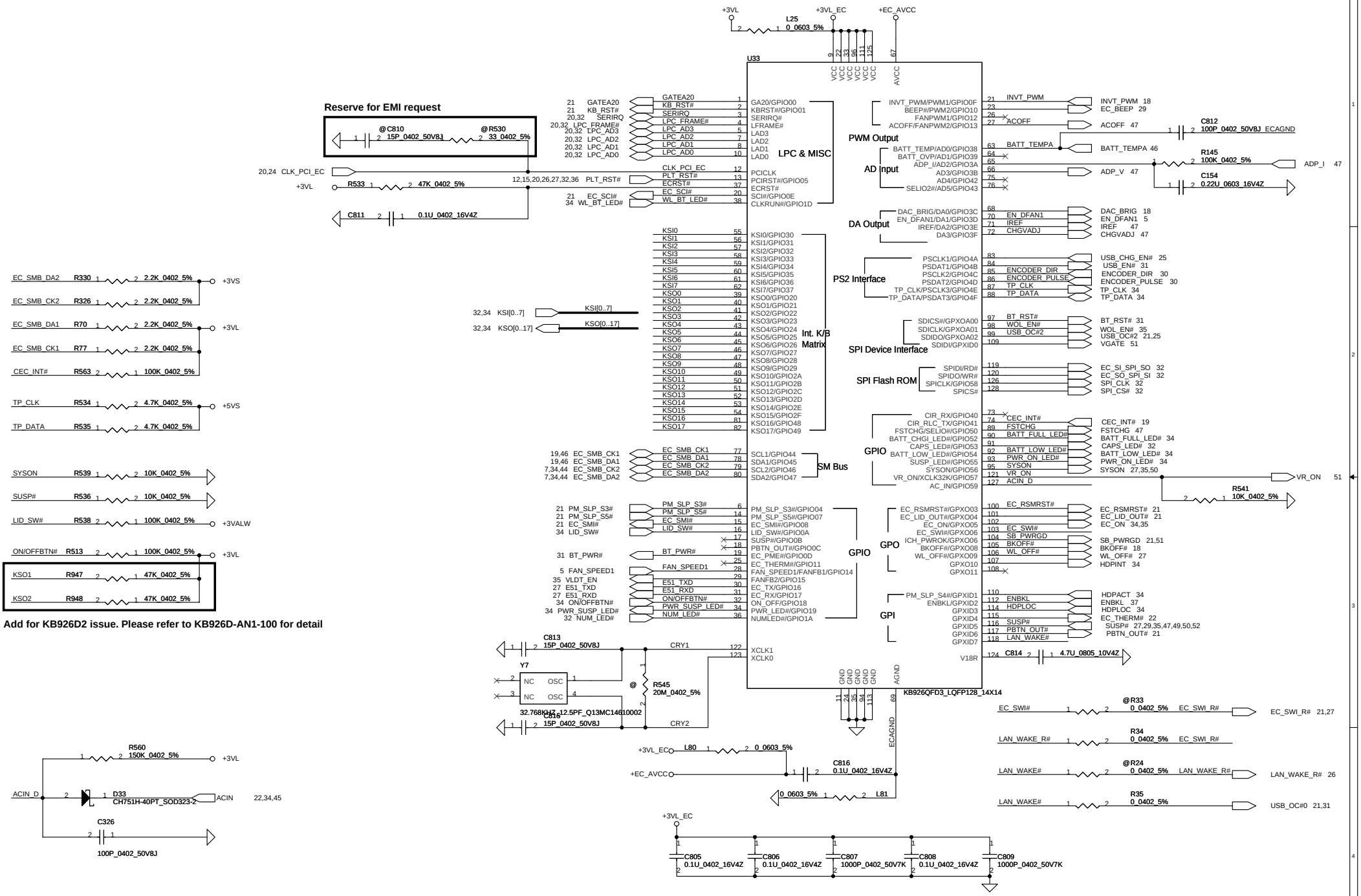

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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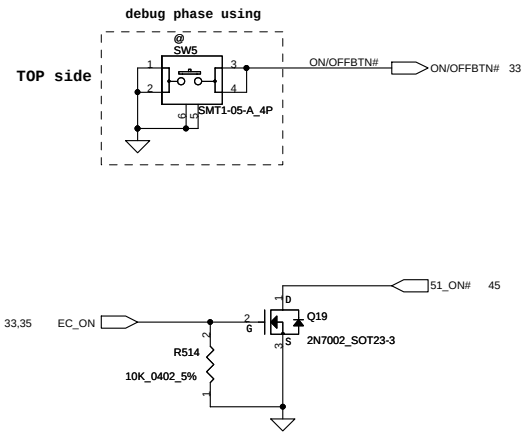
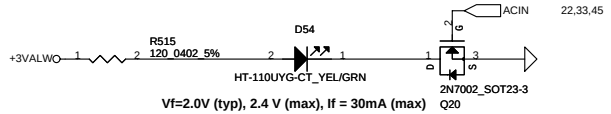
< Power Button for Debug >



< DC-IN LED >

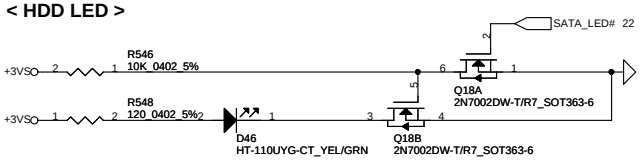


Vf=2.0V (typ), 2.4 V (max), If = 30mA (max)

< WiMAX LED >

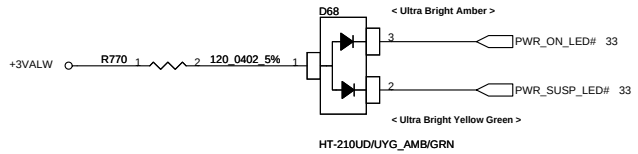
Remove WiMAX LED control circuit

< HDD LED >

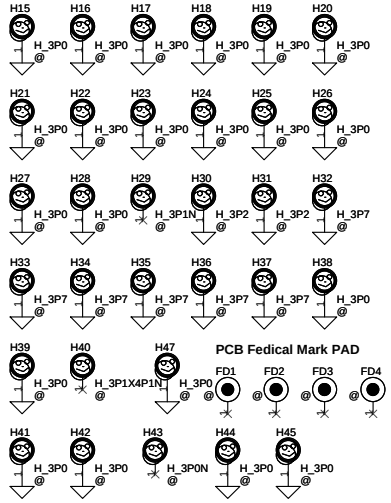


< WL&BT LED >

< POWER-ON & SUSPEND LED >

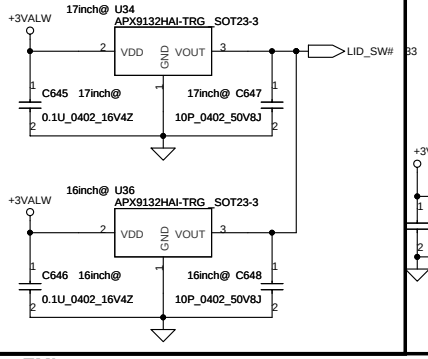


< Screw Hole >

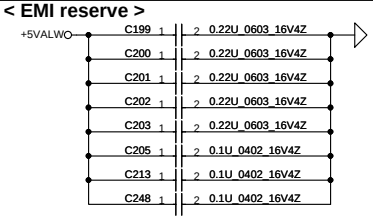


MDC: ***H30, H31***
VGA: ***H38, H39, H41***
CPU: ***H32, H33, H34, H35***
Mini Card : ***H36, H37***
Others: ***H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H25, H26, H27, H28, H29, H40, H42, H43, H47,H44***

< LID Switch >

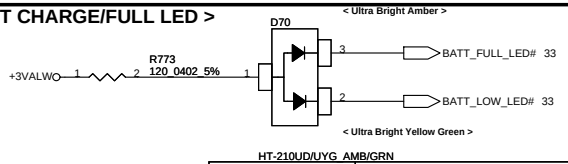


< EMI reserve >



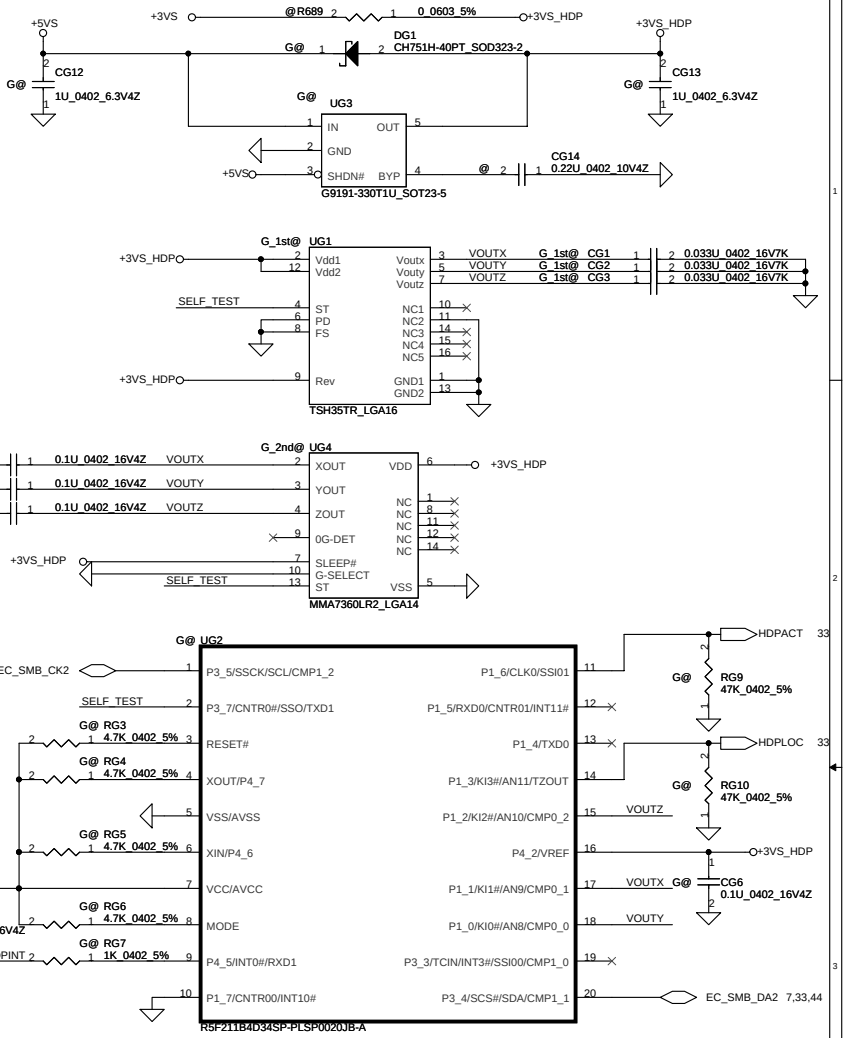
1.C199 : U19
2.C200 : PU5
3.Top side of PU12 for noise bounce.
4.C202 : U25
5.C203 : PU9
6.C205 : PU6
7.C213 : PJ5
8.C248 : Q35

< BATT CHARGE/FULL LED >

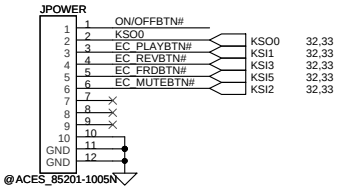


Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

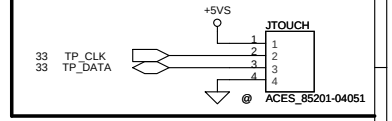
< G - Sensor >



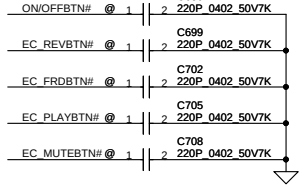
< SW/B Connector >



< Touch/B Connector >



< For EMI >



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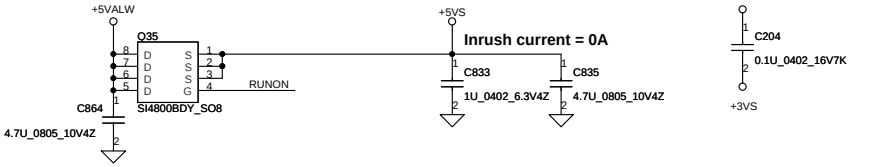
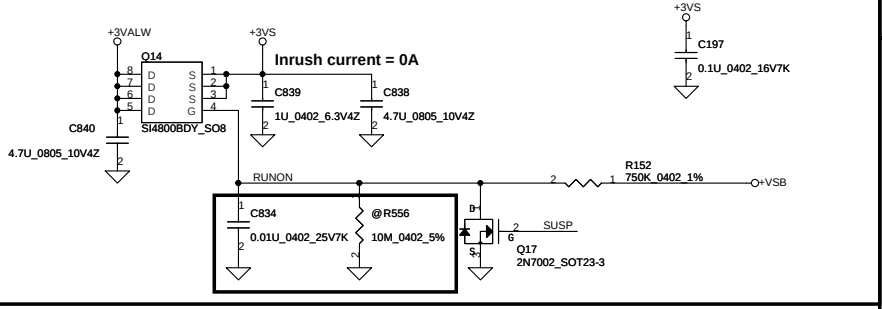
< +5VALW TO +5VS >



< close to PQ20, must EMI confirm >

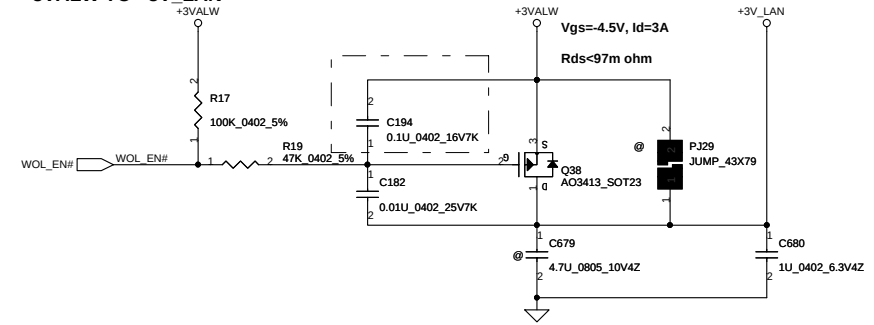
< +3VALW TO +3VS >



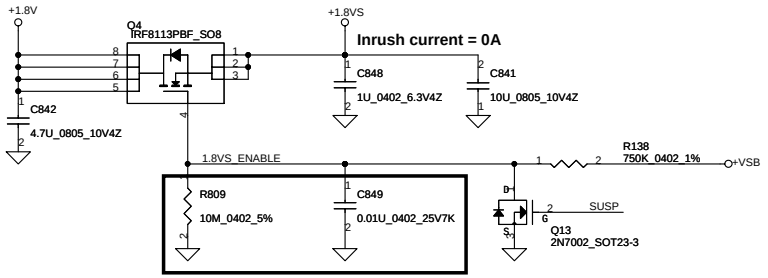
< close to PQ20, must EMI confirm >

< +3VALW TO +3V_LAN >

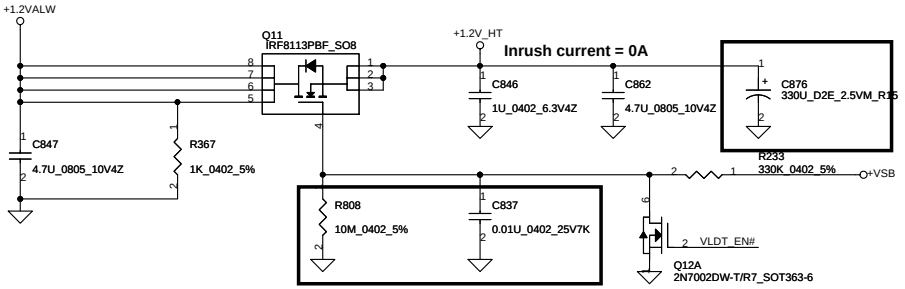
Inrush current = 0A



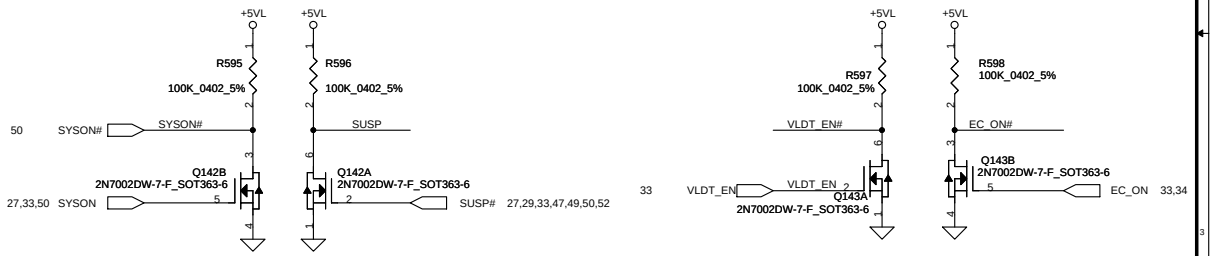
< +1.8V TO +1.8VS >



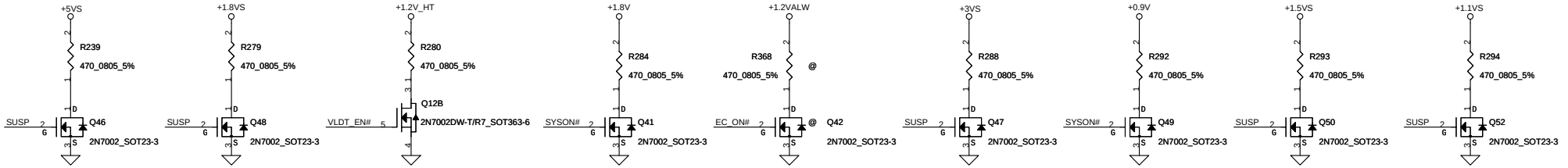
< +1.2VALW TO +1.2V_HT >



< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



< Discharge circuit >



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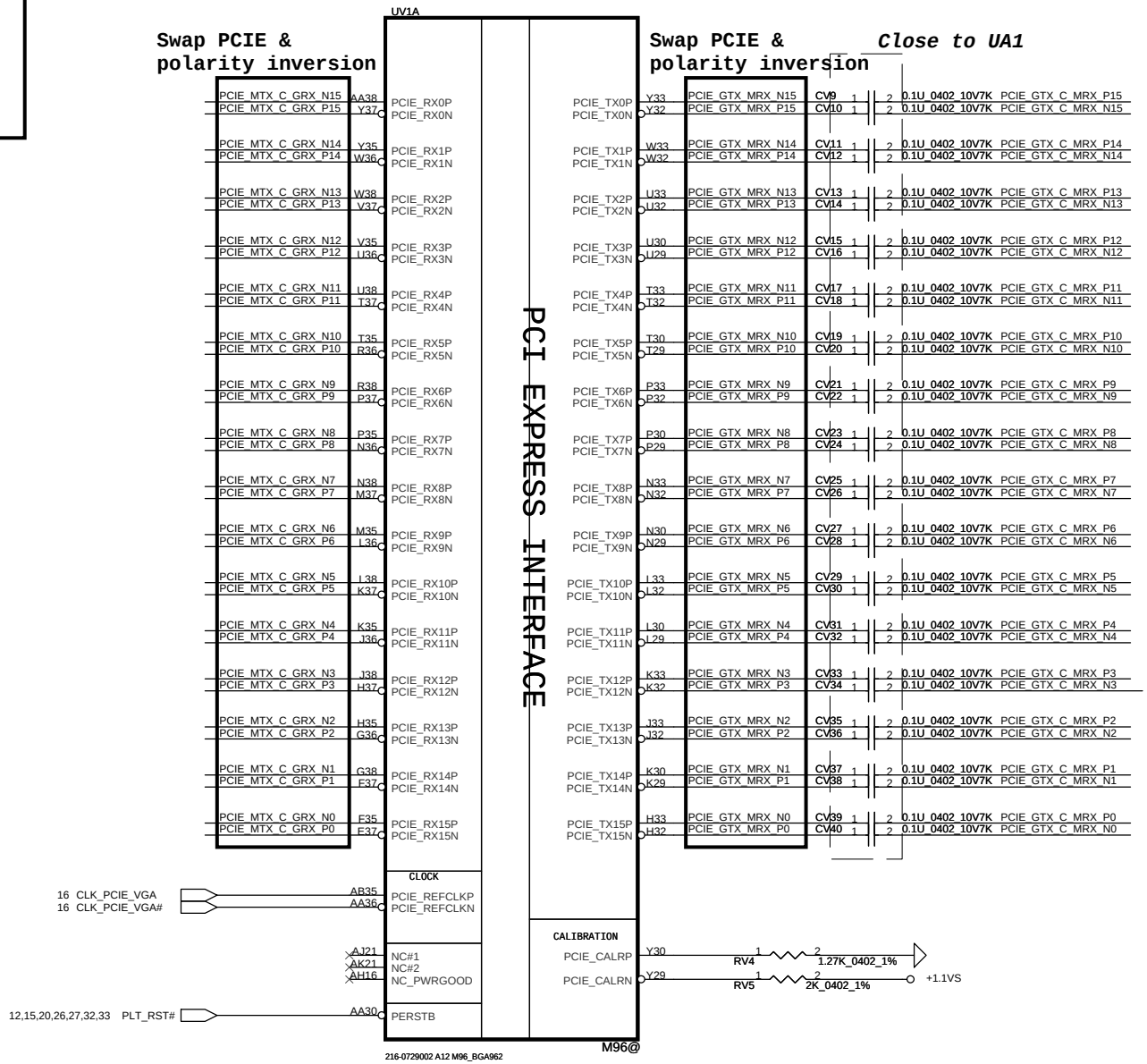
11 PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]

11 PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

11 PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]

11 PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]



Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

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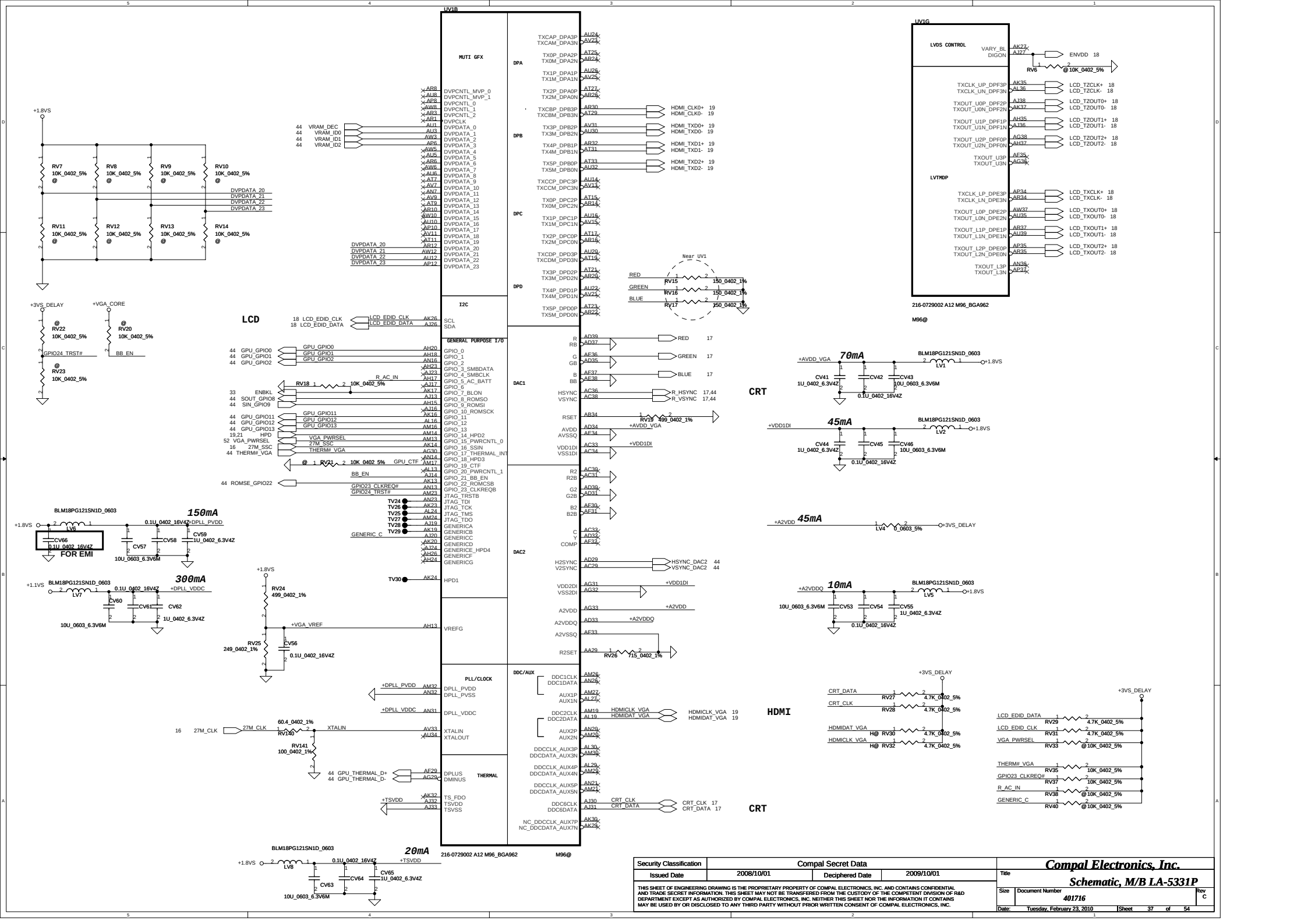

Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

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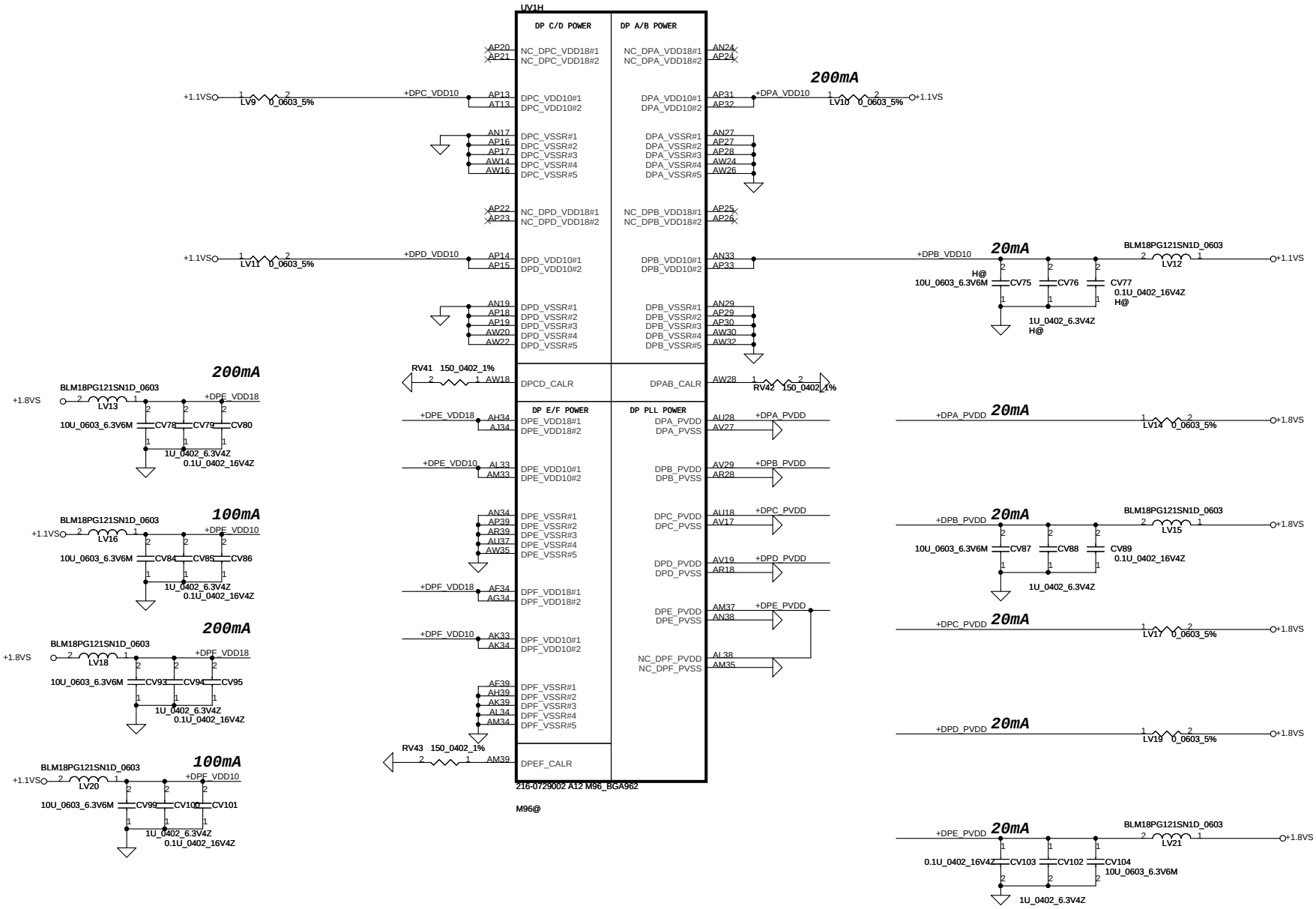

Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

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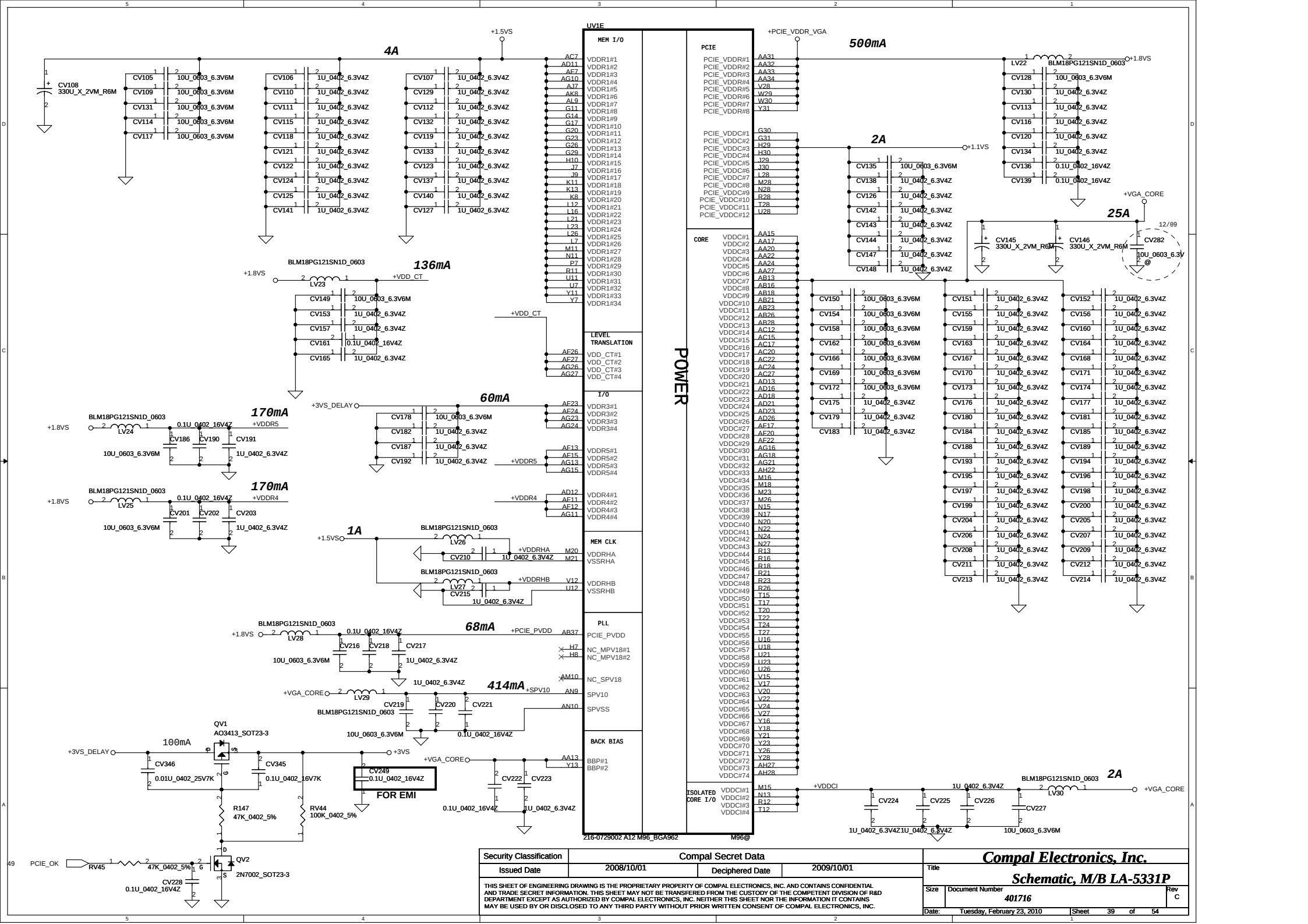

Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

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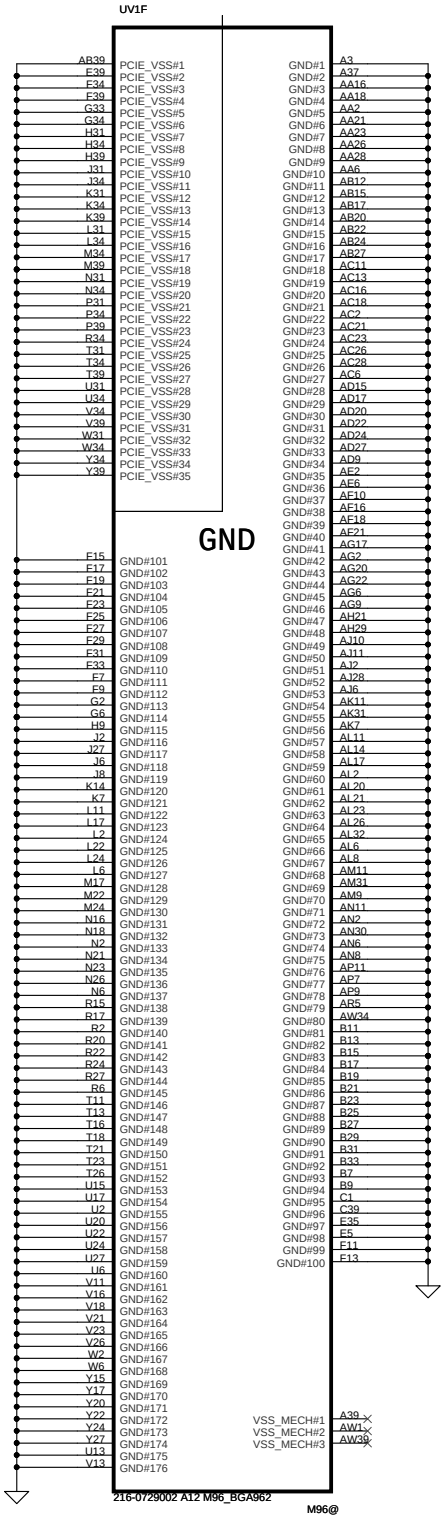

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MDA[0..63] → MDA[0..63] 42

MDB[0..63] → MDB[0..63] 43

M92-M2 uses memory group B only

UV1C

MEMORY INTERFACE A

MDA0	C37	DQA_0	MAA_0	G24	MAA0
MDA1	C35	DQA_1	MAA_1	J23	MAA1
MDA2	A35	DQA_2	MAA_2	H24	MAA2
MDA3	E34	DQA_3	MAA_3	J24	MAA3
MDA4	G32	DQA_4	MAA_4	H26	MAA4
MDA5	D33	DQA_5	MAA_5	J26	MAA5
MDA6	F32	DQA_6	MAA_6	H21	MAA6
MDA7	E32	DQA_7	MAA_7	G21	MAA7
MDA8	D31	DQA_8	MAA_8	H19	MAA8
MDA9	E30	DQA_9	MAA_9	H20	MAA9
MDA10	C30	DQA_10	MAA_10	L13	MAA10
MDA11	A30	DQA_11	MAA_11	G16	MAA11
MDA12	E28	DQA_12	MAA_12	J16	MAA12
MDA13	C28	DQA_13	MAA_13/BA2	H16	A_BA2
MDA14	A28	DQA_14	MAA_14/BA0	J17	A_BA0
MDA15	E28	DQA_15	MAA_15/BA1	H17	A_BA1
MDA16	D27	DQA_16			
MDA17	F26	DQA_17	DQMA_0	A32	DQMA#0
MDA18	C26	DQA_18	DQMA_1	C32	DQMA#1
MDA19	A26	DQA_19	DQMA_2	D23	DQMA#2
MDA20	E24	DQA_20	DQMA_3	E22	DQMA#3
MDA21	C24	DQA_21	DQMA_4	C14	DQMA#4
MDA22	A24	DQA_22	DQMA_5	A14	DQMA#5
MDA23	F24	DQA_23	DQMA_6	F10	DQMA#6
MDA24	C22	DQA_24	DQMA_7	D9	DQMA#7
MDA25	A22	DQA_25			
MDA26	F22	DQA_26	QSA_0/RDQSA_0	C34	QSA0
MDA27	D21	DQA_27	QSA_1/RDQSA_1	D29	QSA1
MDA28	A20	DQA_28	QSA_2/RDQSA_2	D25	QSA2
MDA29	F20	DQA_29	QSA_3/RDQSA_3	E20	QSA3
MDA30	D19	DQA_30	QSA_4/RDQSA_4	F16	QSA4
MDA31	E18	DQA_31	QSA_5/RDQSA_5	E12	QSA5
MDA32	C18	DQA_32	QSA_6/RDQSA_6	J10	QSA6
MDA33	A18	DQA_33	QSA_7/RDQSA_7	D7	QSA7
MDA34	F18	DQA_34			
MDA35	D17	DQA_35	QSA_0B/WDQSA_0	A34	QSA#0
MDA36	A16	DQA_36	QSA_1B/WDQSA_1	E30	QSA#1
MDA37	F16	DQA_37	QSA_2B/WDQSA_2	F26	QSA#2
MDA38	D15	DQA_38	QSA_3B/WDQSA_3	C20	QSA#3
MDA39	E14	DQA_39	QSA_4B/WDQSA_4	C16	QSA#4
MDA40	F14	DQA_40	QSA_5B/WDQSA_5	C12	QSA#5
MDA41	D13	DQA_41	QSA_6B/WDQSA_6	J11	QSA#6
MDA42	F12	DQA_42	QSA_7B/WDQSA_7	F8	QSA#7
MDA43	A12	DQA_43			
MDA44	D11	DQA_44	ODTA0	J21	ODTA0
MDA45	F10	DQA_45	ODTA1	G19	ODTA1
MDA46	A10	DQA_46			
MDA47	C10	DQA_47	CLKA0	H27	CLKA0
MDA48	G13	DQA_48	CLKA0B	G27	CLKA0#
MDA49	H13	DQA_49			
MDA50	J13	DQA_50	CLKA1	J14	CLKA1
MDA51	H11	DQA_51	CLKA1B	H14	CLKA1#
MDA52	G10	DQA_52			
MDA53	G8	DQA_53	RASA0B	K23	RASA0#
MDA54	K9	DQA_54	RASA1B	K19	RASA1#
MDA55	K10	DQA_55			
MDA56	G9	DQA_56	CASA0B	K20	CASA0#
MDA57	A8	DQA_57	CASA1B	K17	CASA1#
MDA58	C8	DQA_58			
MDA59	E8	DQA_59	CSA0B_0	K24	CSA0#_0
MDA60	A6	DQA_60	CSA0B_1	K27	
MDA61	C6	DQA_61			
MDA62	E6	DQA_62	CSA1B_0	M13	CSA1#_0
MDA63	A5	DQA_63	CSA1B_1	K16	
+MVREFDA	L18	MVREFDA	CKEA0	K21	CKEA0
		MVREFSA	CKEA1	J20	CKEA1
		NC_MEM_CALRN0	WEA0B	K26	WEA0#
		NC_MEM_CALRN1	WEA1B	L15	WEA1#
		NC_MEM_CALRN2			
		MEM_CALRP1	RSVD#1	AE28	
		NC_MEM_CALRP0	RSVD#2	AG28	
		NC_MEM_CALRP2	RSVD#3	AL31	
			RSVD#5	H23	
			RSVD#6	J19	
			RSVD#9	T8	
			RSVD#11	W8	

MAA[12..0] → MAA[12..0] 42

A_BA[2..0] → A_BA[2..0] 42

DQMA#[7..0] → DQMA#[7..0] 42

QSA[7..0] → QSA[7..0] 42

QSA#[7..0] → QSA#[7..0] 42

ODTA0 → ODTA0 42

ODTA1 → ODTA1 42

CLKA0 → CLKA0 42

CLKA0B → CLKA0# 42

CLKA1 → CLKA1 42

CLKA1B → CLKA1# 42

RASA0B → RASA0# 42

RASA1B → RASA1# 42

CASA0B → CASA0# 42

CASA1B → CASA1# 42

CSA0B_0 → CSA0#_0 42

CSA0B_1

CSA1B_0 → CSA1#_0 42

CSA1B_1

CKEA0 → CKEA0 42

CKEA1 → CKEA1 42

WEA0B → WEA0# 42

WEA1B → WEA1# 42

RSVD#1

RSVD#2

RSVD#3

RSVD#5

RSVD#6

RSVD#9

RSVD#11

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M96@

UV1D

MEMORY INTERFACE B

MDB0	C5	DQB_0	MAB_0	P8	MAB0
MDB1	C3	DQB_1	MAB_1	T9	MAB1
MDB2	E3	DQB_2	MAB_2	P9	MAB2
MDB3	E1	DQB_3	MAB_3	N7	MAB3
MDB4	F1	DQB_4	MAB_4	N8	MAB4
MDB5	F3	DQB_5	MAB_5	N9	MAB5
MDB6	F5	DQB_6	MAB_6	U9	MAB6
MDB7	G4	DQB_7	MAB_7	U8	MAB7
MDB8	H5	DQB_8	MAB_8	Y9	MAB8
MDB9	H6	DQB_9	MAB_9	W9	MAB9
MDB10	J4	DQB_10	MAB_10	AC8	MAB10
MDB11	K6	DQB_11	MAB_11	AC9	MAB11
MDB12	K5	DQB_12	MAB_12	AA7	MAB12
MDB13	L4	DQB_13	MAB_13/BA2	AA8	B_BA2
MDB14	M6	DQB_14	MAB_14/BA0	Y8	B_BA0
MDB15	M1	DQB_15	MAB_15/BA1	AA9	B_BA1
MDB16	M3	DQB_16			
MDB17	M5	DQB_17	DQMB_0	H3	DQMB#0
MDB18	N4	DQB_18	DQMB_1	H1	DQMB#1
MDB19	P6	DQB_19	DQMB_2	T3	DQMB#2
MDB20	P5	DQB_20	DQMB_3	T5	DQMB#3
MDB21	R4	DQB_21	DQMB_4	AE4	DQMB#4
MDB22	T6	DQB_22	DQMB_5	AF5	DQMB#5
MDB23	T1	DQB_23	DQMB_6	AK6	DQMB#6
MDB24	U4	DQB_24	DQMB_7	AK5	DQMB#7
MDB25	V6	DQB_25			
MDB26	V1	DQB_26	QSB_0/RDQSB_0	F6	QSB0
MDB27	V3	DQB_27	QSB_1/RDQSB_1	K3	QSB1
MDB28	Y6	DQB_28	QSB_2/RDQSB_2	P3	QSB2
MDB29	Y1	DQB_29	QSB_3/RDQSB_3	V5	QSB3
MDB30	Y3	DQB_30	QSB_4/RDQSB_4	AB5	QSB4
MDB31	Y5	DQB_31	QSB_5/RDQSB_5	AH1	QSB5
MDB32	AA4	DQB_32	QSB_6/RDQSB_6	AJ9	QSB6
MDB33	AB6	DQB_33	QSB_7/RDQSB_7	AM5	QSB7
MDB34	AB1	DQB_34			
MDB35	AB3	DQB_35	QSB_0B/WDQSB_0	G7	QSB#0
MDB36	AD6	DQB_36	QSB_1B/WDQSB_1	K1	QSB#1
MDB37	AD1	DQB_37	QSB_2B/WDQSB_2	P1	QSB#2
MDB38	AD3	DQB_38	QSB_3B/WDQSB_3	W4	QSB#3
MDB39	AD5	DQB_39	QSB_4B/WDQSB_4	AC4	QSB#4
MDB40	AF1	DQB_40	QSB_5B/WDQSB_5	AH3	QSB#5
MDB41	AF3	DQB_41	QSB_6B/WDQSB_6	AJ8	QSB#6
MDB42	AF6	DQB_42	QSB_7B/WDQSB_7	AM3	QSB#7
MDB43	AG4	DQB_43			
MDB44	AH5	DQB_44	ODTB0	T7	ODTB0
MDB45	AH6	DQB_45	ODTB1	W7	ODTB1
MDB46	AJ4	DQB_46			
MDB47	AK3	DQB_47	CLKB0	L9	CLKB0
MDB48	AF8	DQB_48	CLKB0B	L8	CLKB0#
MDB49	AF9	DQB_49			
MDB50	AG8	DQB_50	CLKB1	AD8	CLKB1
MDB51	AG7	DQB_51	CLKB1B	AD7	CLKB1#
MDB52	AK9	DQB_52			
MDB53	AL7	DQB_53	RASB0B	T10	RASB0#
MDB54	AM8	DQB_54	RASB1B	Y10	RASB1#
MDB55	AM7	DQB_55			
MDB56	AK1	DQB_56	CASB0B	W10	CASB0#
MDB57	AL4	DQB_57	CASB1B	AA10	CASB1#
MDB58	AM6	DQB_58			
MDB59	AM1	DQB_59	CSB0B_0	P10	CSB0#_0
MDB60	AN4	DQB_60	CSB0B_1	L10	
MDB61	AP3	DQB_61			
MDB62	AP1	DQB_62	CSB1B_0	AD10	CSB1#_0
MDB63	AP5	DQB_63	CSB1B_1	AC10	
	Y12	MVREFDB	CKEB0	U10	CKEB0
	AA12	MVREFSB	CKEB1	AA11	CKEB1
			WEB0B	N10	WEB0#
			WEB1B	AB11	WEB1#
	AD28	TESTEN			
	AK10	CLKTESTA			
	AL10	CLKTESTB	DRAM_RST	AH11	DRAM_RST#

MAB[12..0] → MAB[12..0] 43

B_BA[2..0] → B_BA[2..0] 43

DQMB#[7..0] → DQMB#[7..0] 43

QSB[7..0] → QSB[7..0] 43

QSB#[7..0] → QSB#[7..0] 43

ODTB0 → ODTB0 43

ODTB1 → ODTB1 43

CLKB0 → CLKB0 43

CLKB0B → CLKB0# 43

CLKB1 → CLKB1 43

CLKB1B → CLKB1# 43

RASB0B → RASB0# 43

RASB1B → RASB1# 43

CASB0B → CASB0# 43

CASB1B → CASB1# 43

CSB0B_0 → CSB0#_0 43

CSB0B_1

CSB1B_0 → CSB1#_0 43

CSB1B_1

CKEB0 → CKEB0 43

CKEB1 → CKEB1 43

WEB0B → WEB0# 43

WEB1B → WEB1# 43

DRAM_RST → DRAM_RST# 42,43

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M96@

Close to pin L18

+1.5VS

RV46 100_0402_1%

+MVREFDA

RV48 100_0402_1%

CV229 0.1U_0402_16V4Z

Close to pin L20

+1.5VS

RV50 100_0402_1%

+MVREFSA

RV52 100_0402_1%

CV231 0.1U_0402_16V4Z

+1.5VS

@RV53 243_0402_1% L27

@RV54 243_0402_1% N12

@RV55 243_0402_1% AG12

RV56 243_0402_1% M12

@RV57 243_0402_1% M27

@RV60 243_0402_1% AH12

Close to pin Y12

+1.5VS

RV47 100_0402_1%

+MVREFDB

RV49 100_0402_1%

CV230 0.1U_0402_16V4Z

Close to pin AA12

+1.5VS

RV51 100_0402_1%

+MVREFSB

RV58 100_0402_1%

CV232 0.1U_0402_16V4Z

+3VS_DELAY

@RV61 5.11K_0402_1%

TESTEN

RV62 4.7K_0402_5%

RV63 4.7K_0402_5%

RV65 1K_0402_5%

RV59 4.7K_0402_5%

+1.5VS

@RV64

CV233 0.01U_0402_16V7K

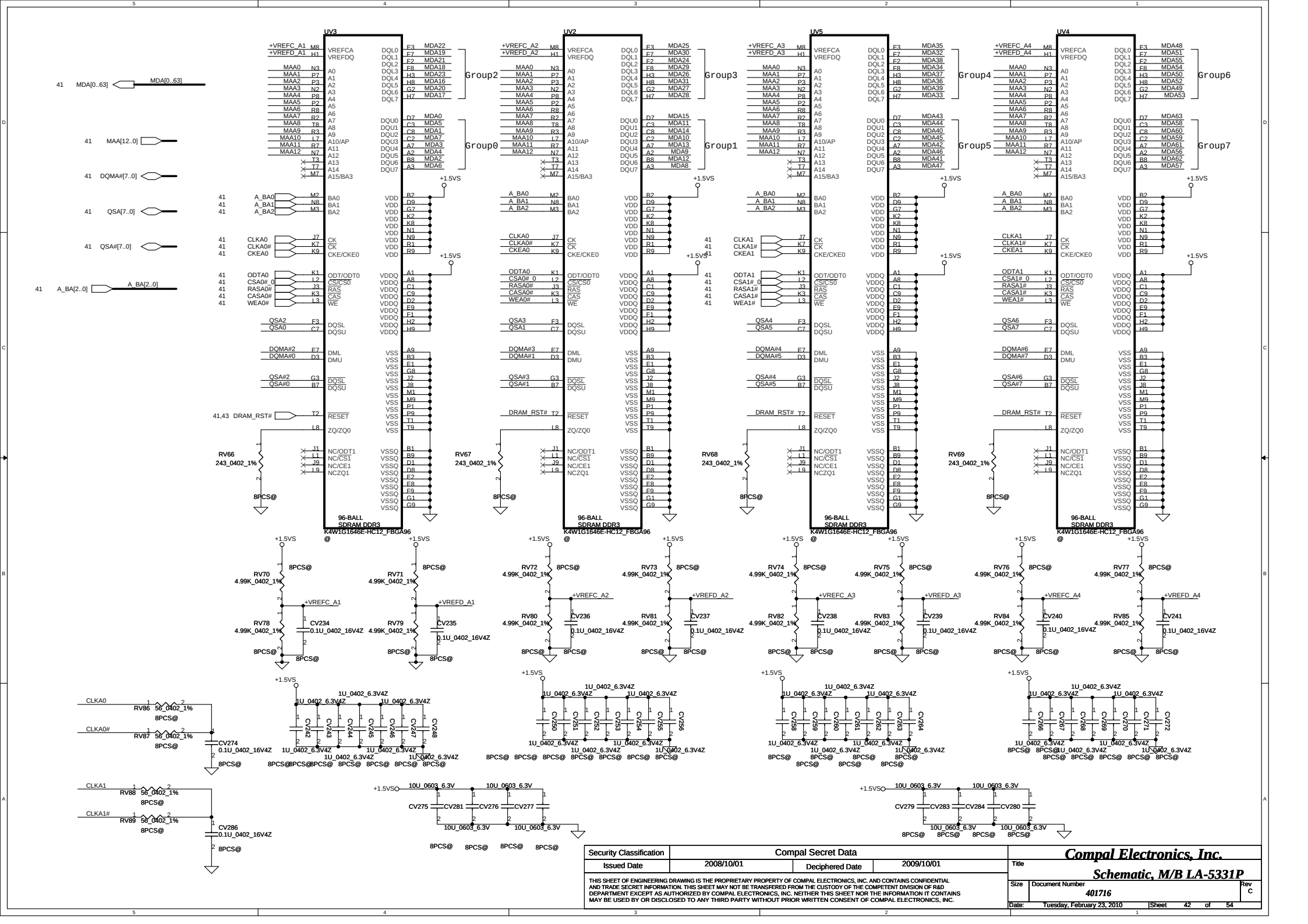
Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

Size	Document Number	Rev
	401716	C

Date: Tuesday, February 23, 2010 Sheet 41 of 54



Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

Size	Document Number	Rev
	401716	C

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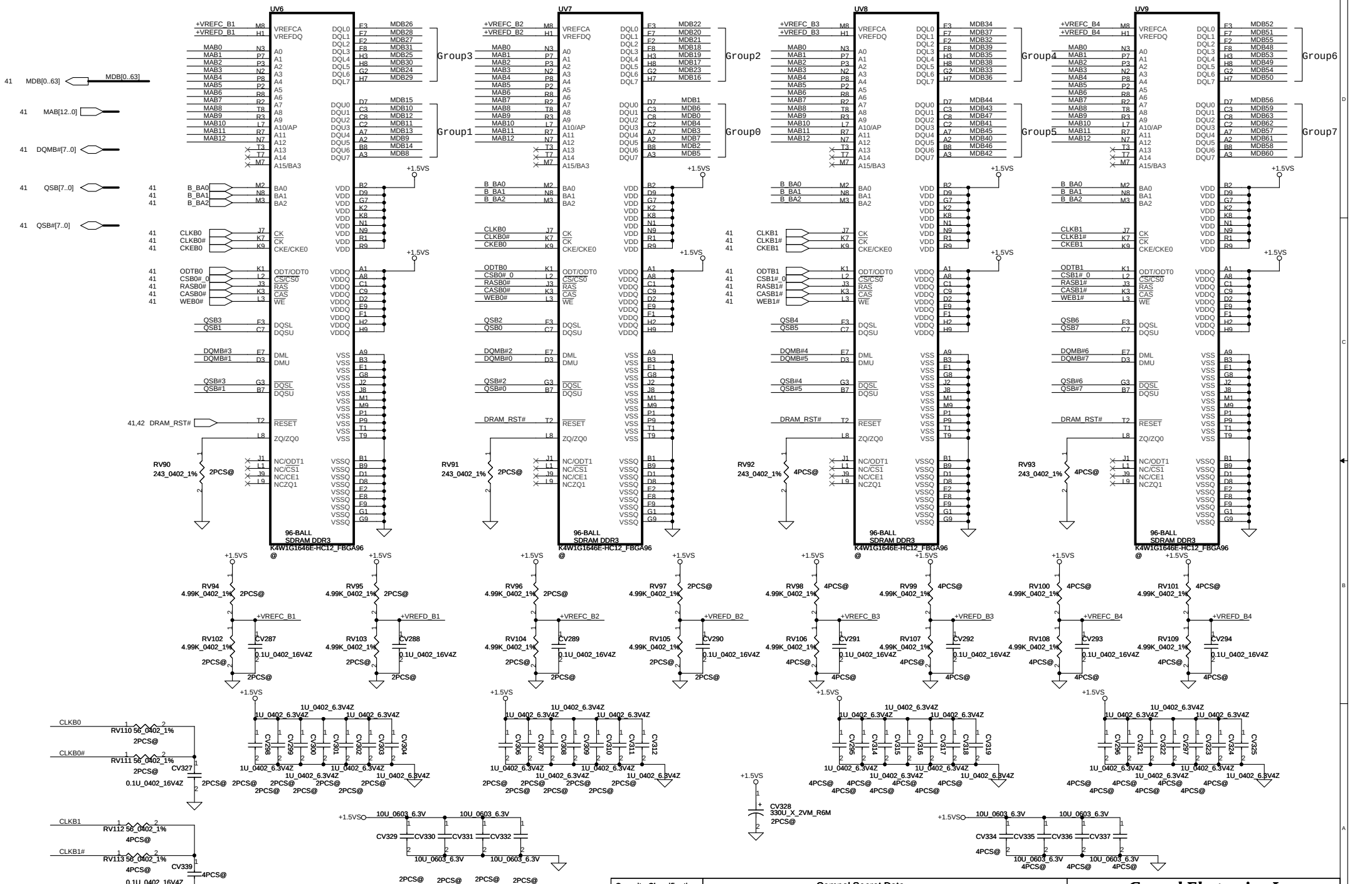

Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

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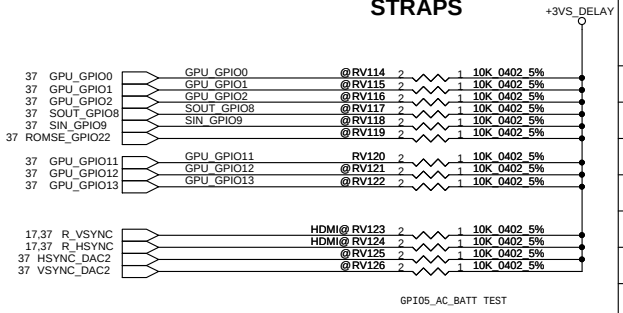
STRAPS

GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

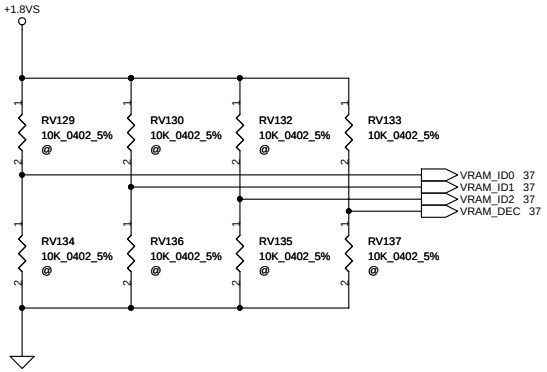
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC_DAC2 GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

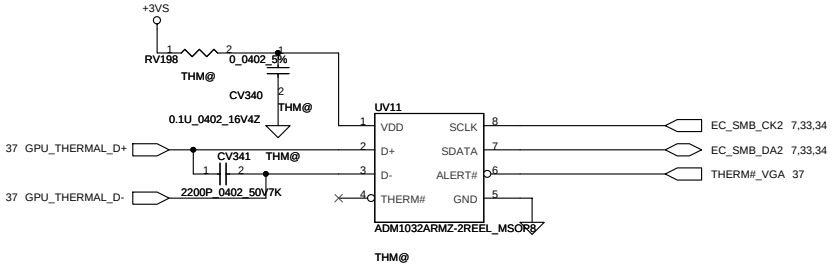
GPIO_28_TDO GPIO21_BB_EN

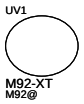


DDR3	
VRAM_DEC	1

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
		M96-M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 1
		M92-M2 XT	256M 64Mx16 (x2)	HYN H5TQ1G63BFR-12C	SA000032400	0 1 0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 0
		M96-M3	1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	0 1 1
		M92-M2 XT	256M 64Mx16 (x2)	SAM K4W1G1646E-HC12	SA000035700	1 0 1

External VGA Thermal Sensor





Security Classification	Compal Secret Data		
Issued Date	2008/10/01	Deciphered Date	2009/10/01

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

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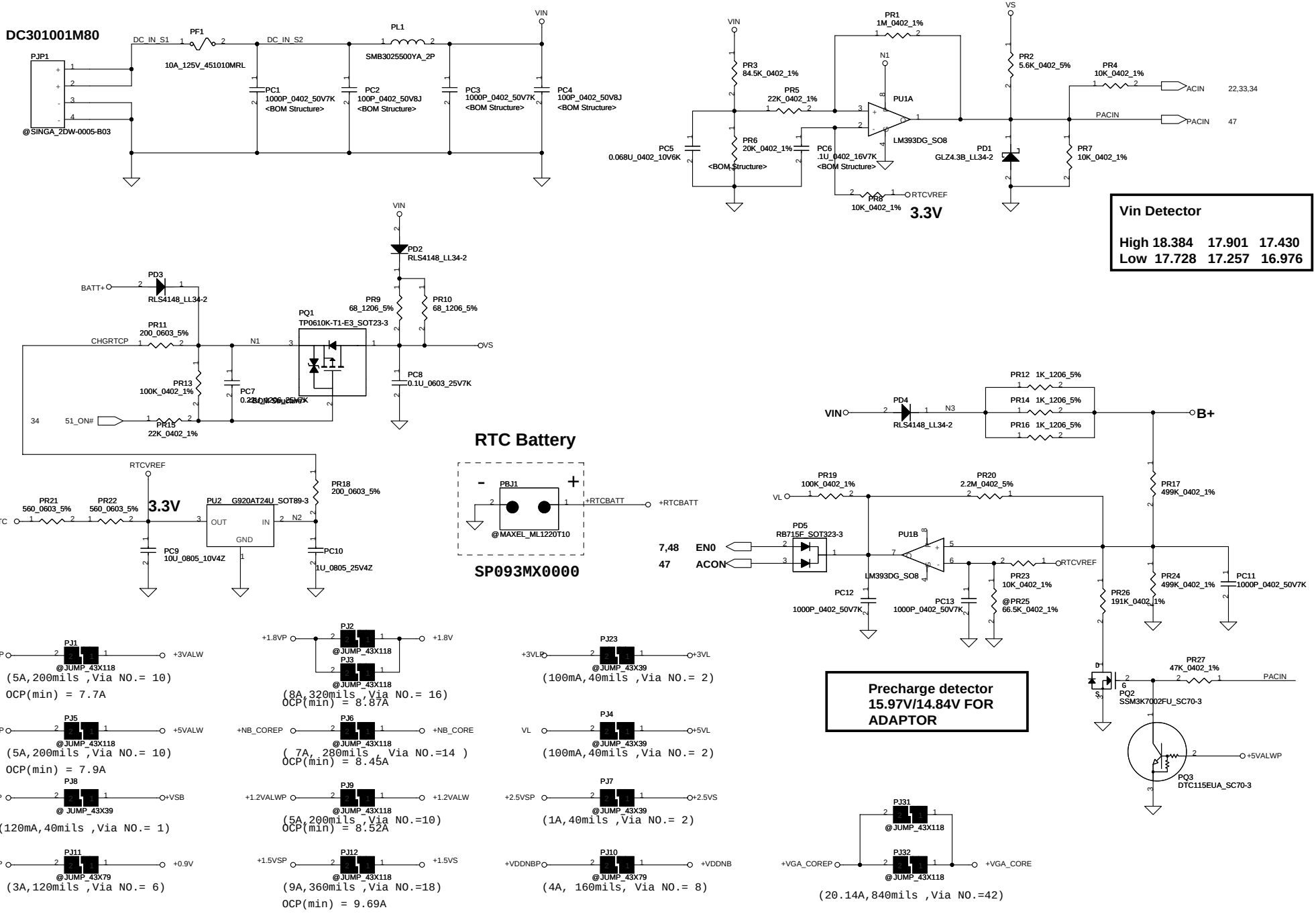

Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

Compal Electronics, Inc.

Title: Schematic, M/B LA-5331P

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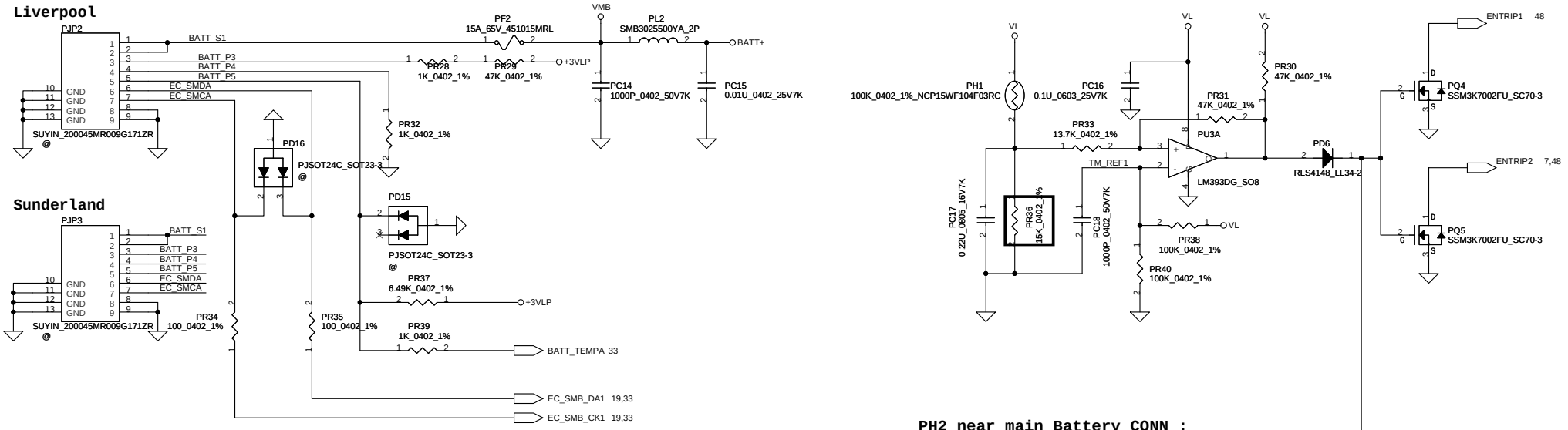
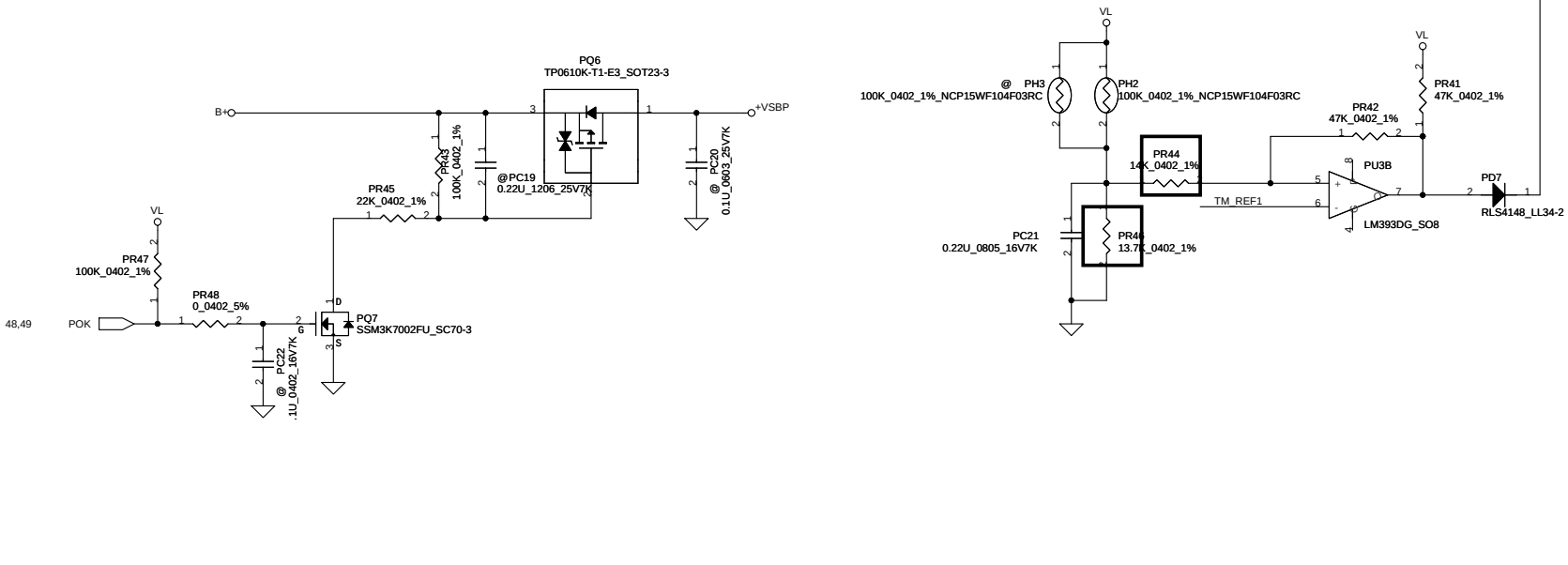
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 57 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 98 degree C
Recovery at 60 degree C



Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

Compal Electronics, Inc.

Title: Schematic, M/B LA-5331P

Size	Document Number	Rev
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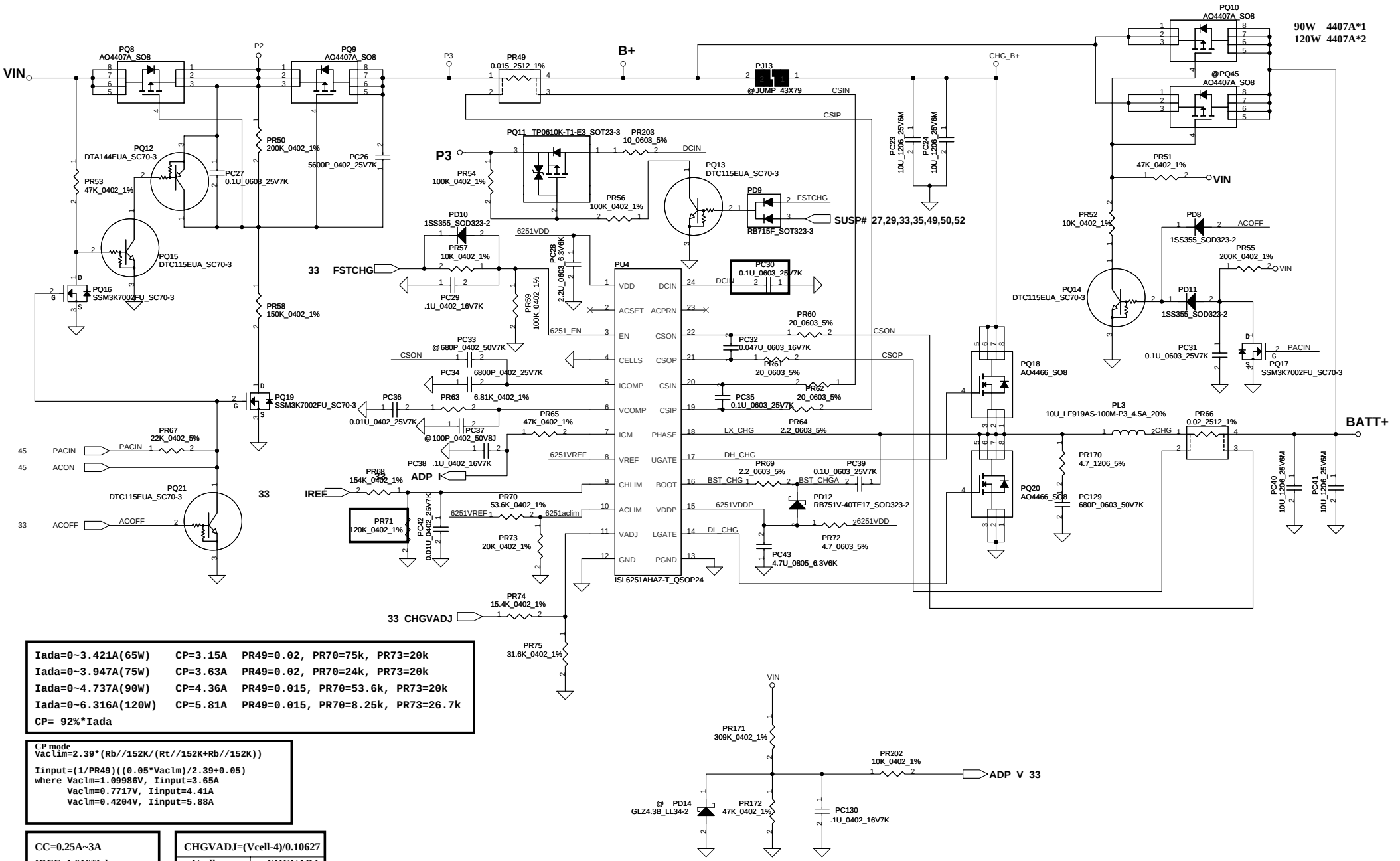

Iada=0~3.421A(65W)	CP=3.15A	PR49=0.02, PR70=75k, PR73=20k
Iada=0~3.947A(75W)	CP=3.63A	PR49=0.02, PR70=24k, PR73=20k
Iada=0~4.737A(90W)	CP=4.36A	PR49=0.015, PR70=53.6k, PR73=20k
Iada=0~6.316A(120W)	CP=5.81A	PR49=0.015, PR70=8.25k, PR73=26.7k
CP= 92%*Iada		

CP mode
Vaclim=2.39*(Rb//152K/(Rt//152K+Rb//152K))

Iinput=(1/PR49)((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.09986V, Iinput=3.65A
Vaclm=0.7717V, Iinput=4.41A
Vaclm=0.4204V, Iinput=5.88A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

Compal Electronics, Inc.

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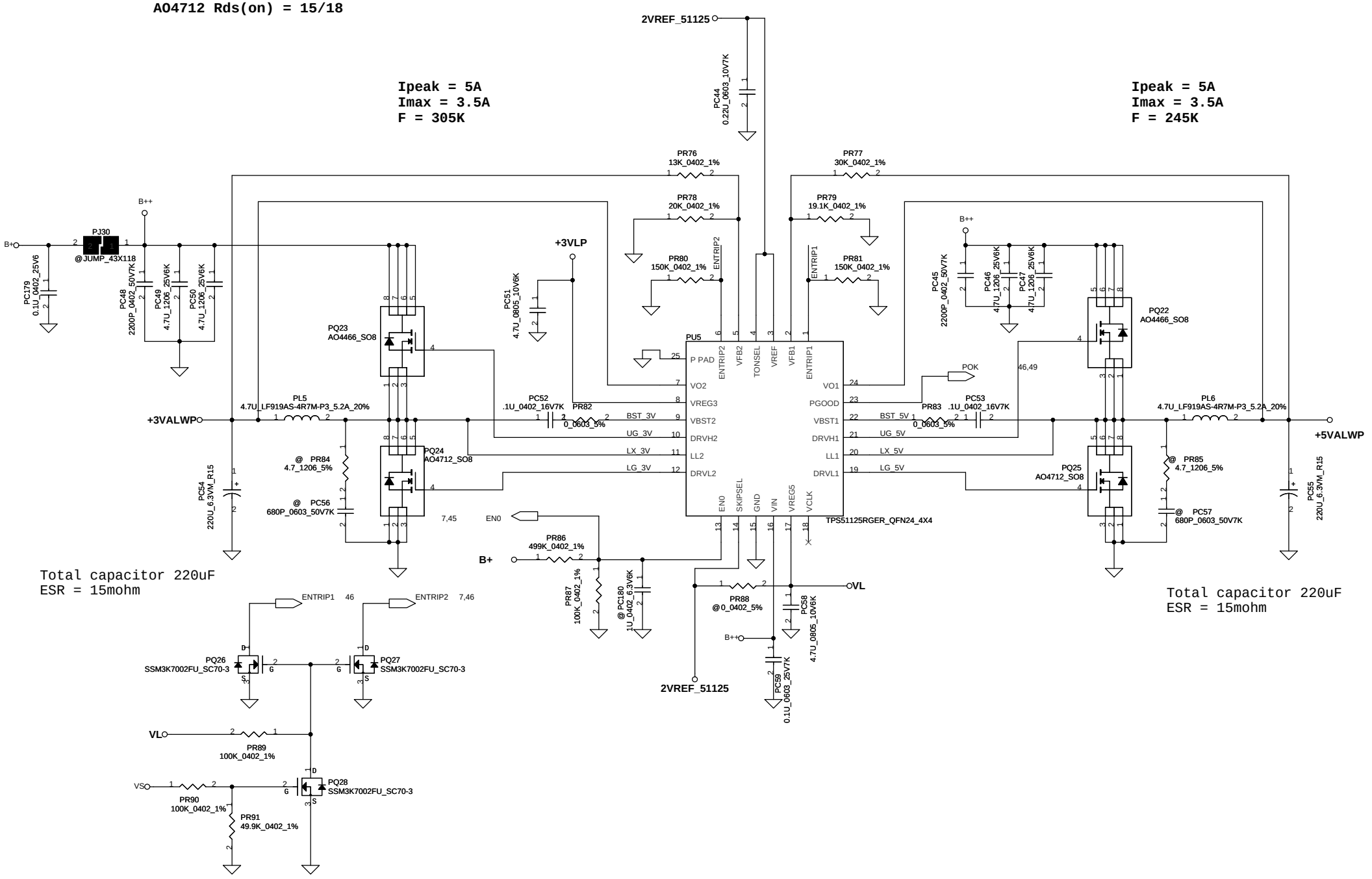
AO4712 Rds(on) = 15/18

Ipeak = 5A
Imax = 3.5A
F = 305K

Ipeak = 5A
Imax = 3.5A
F = 245K



Total capacitor 220uF
ESR = 15mohm

Total capacitor 220uF
ESR = 15mohm

Compal Electronics, Inc.

Title	Schematic, M/B LA-5331P	
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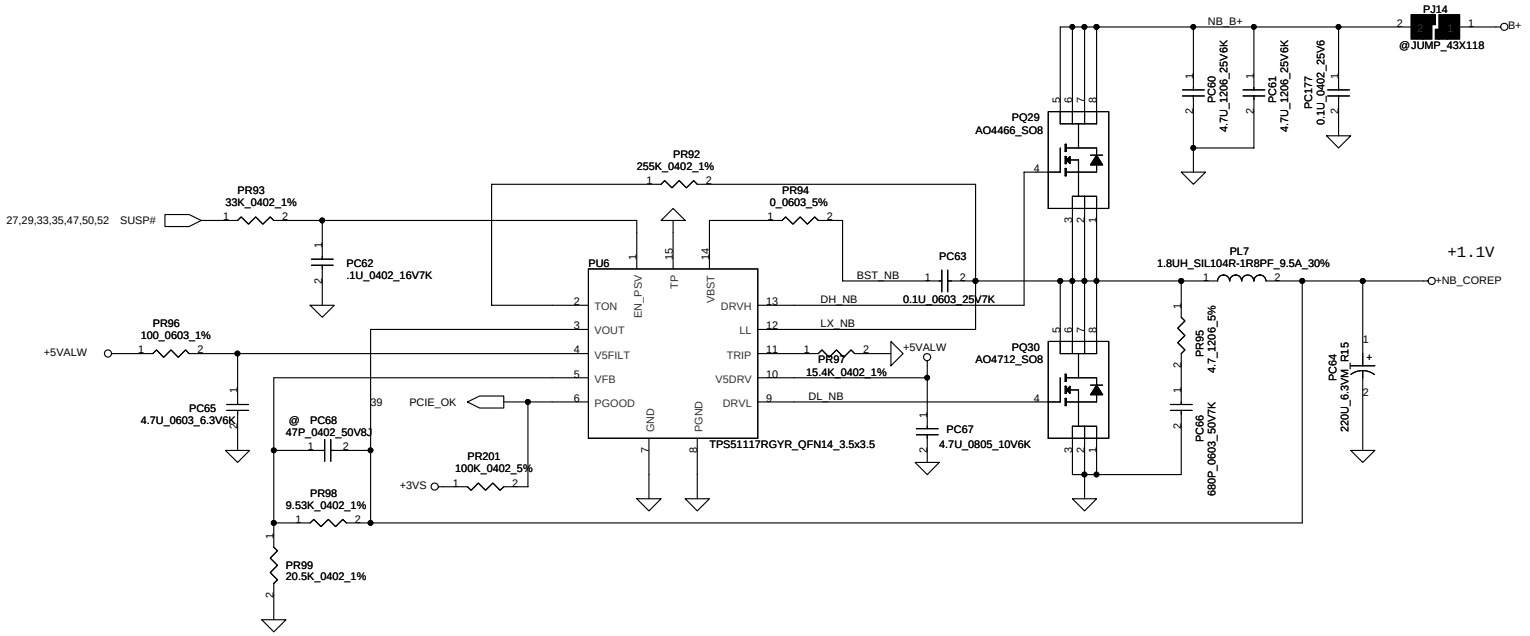
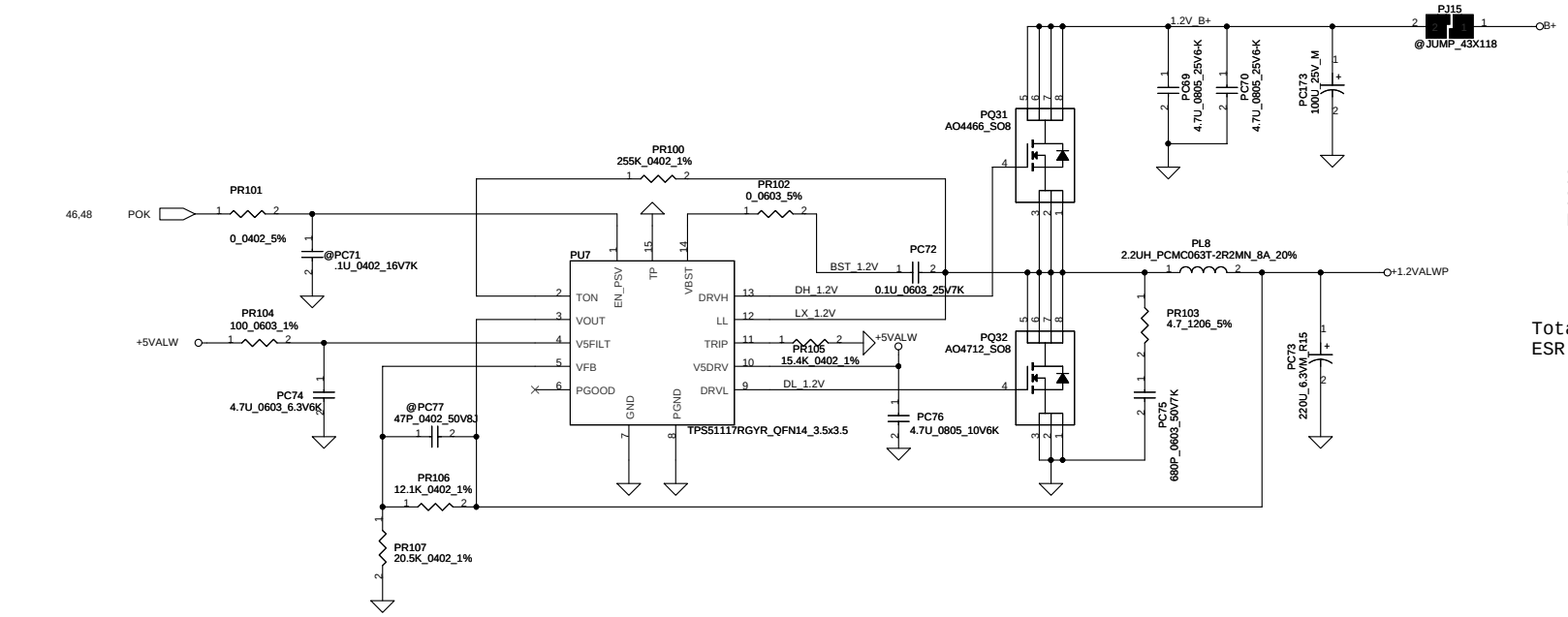


Ipeak = 7A
Imax = 4.9A
F = 315K

Total capacitor 550uF
ESR = 30mohm



Ipeak = 5A
Imax = 3.5A
F = 315K

Total capacitor 220uF
ESR = 15mohm

Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

Compal Electronics, Inc.	
Title	Schematic, M/B LA-5331P
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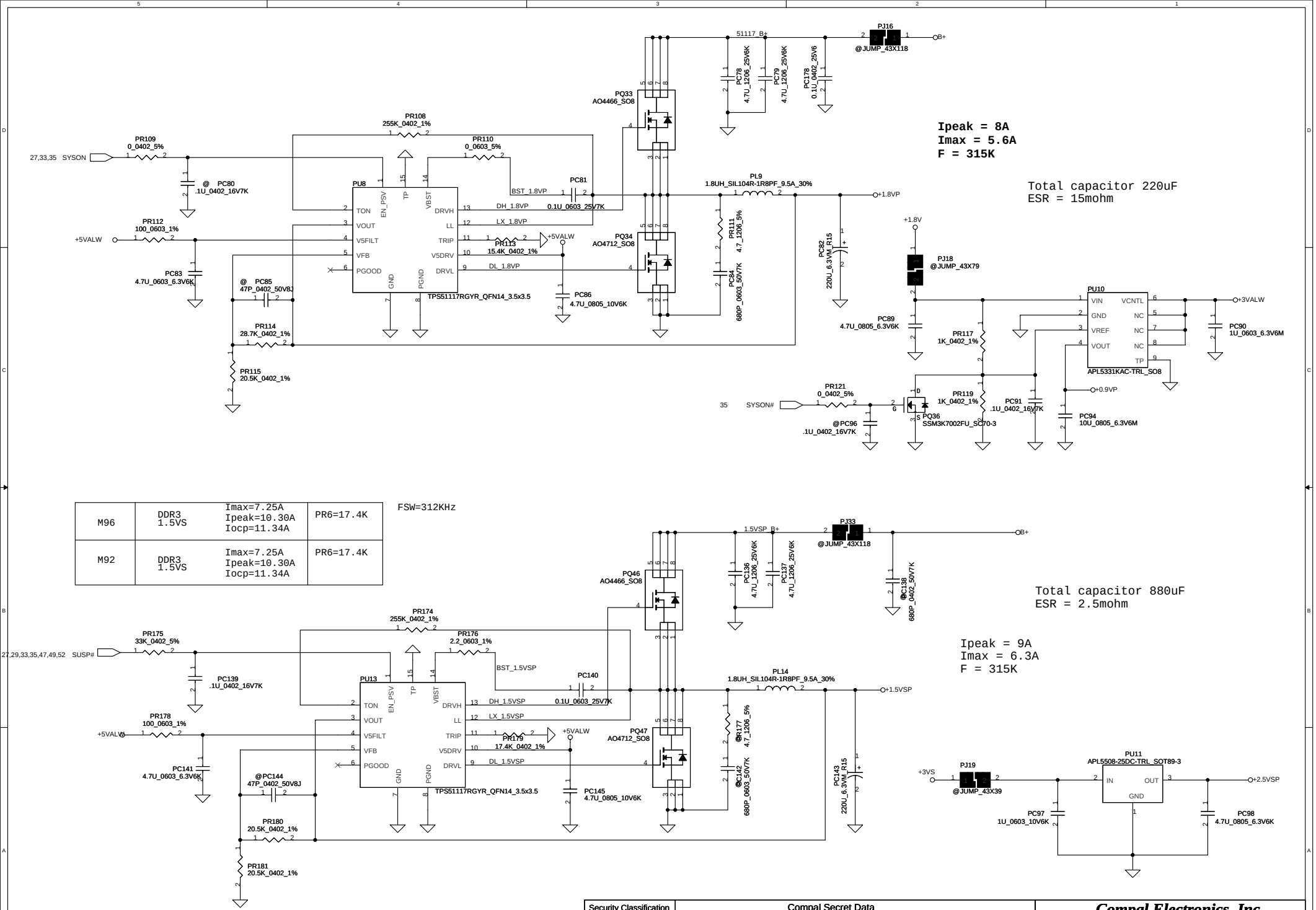

M96	DDR3 1.5VS	Imax=7.25A Ipeak=10.30A Iocp=11.34A	PR6=17.4K
M92	DDR3 1.5VS	Imax=7.25A Ipeak=10.30A Iocp=11.34A	PR6=17.4K

FSW=312KHz

Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

Compal Electronics, Inc.

Title: Schematic, M/B LA-5331P

Size	Document Number	Rev
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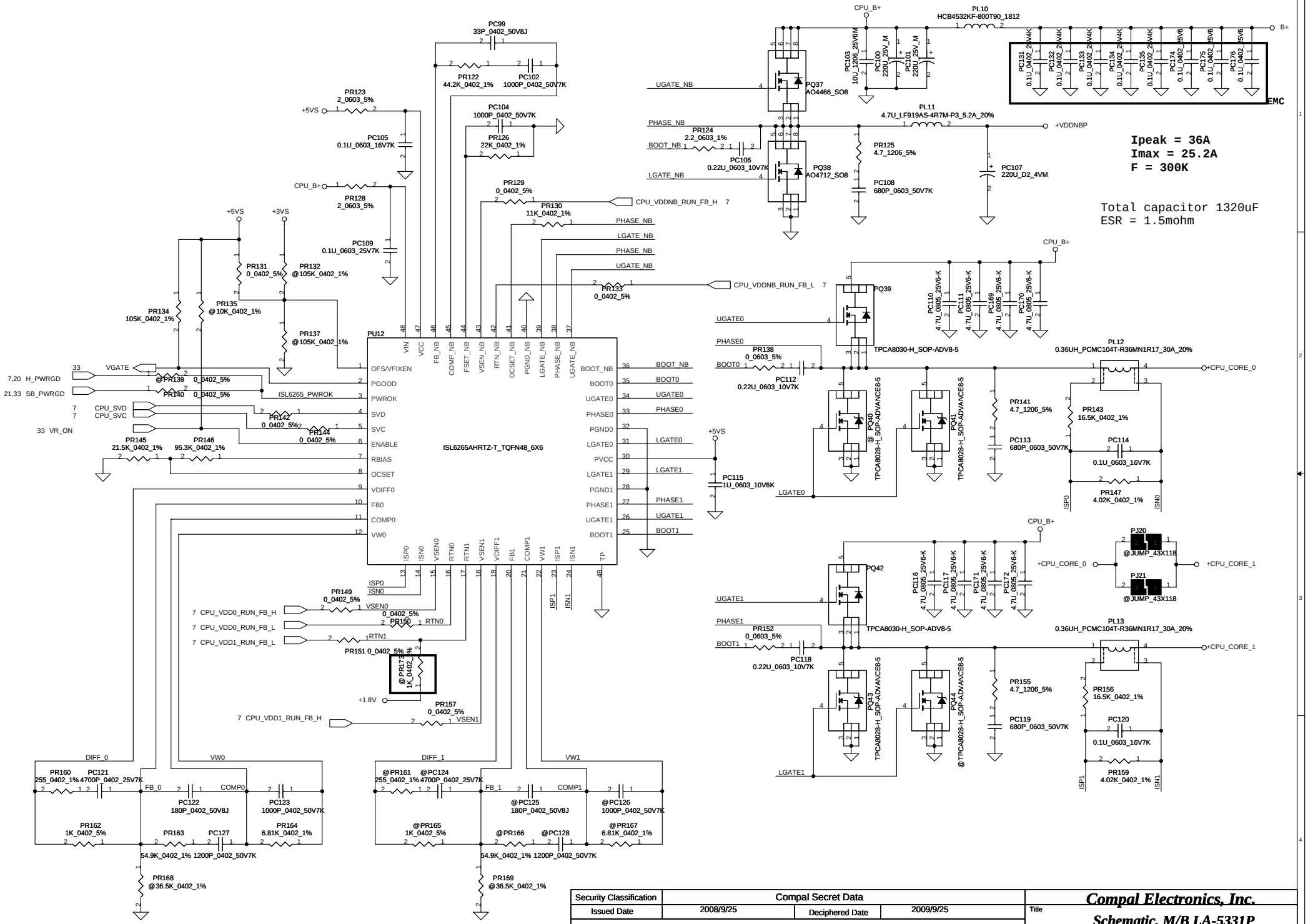
Date: Tuesday, February 23, 2010 | Sheet 50 of 54



Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

Size	Document Number	Rev
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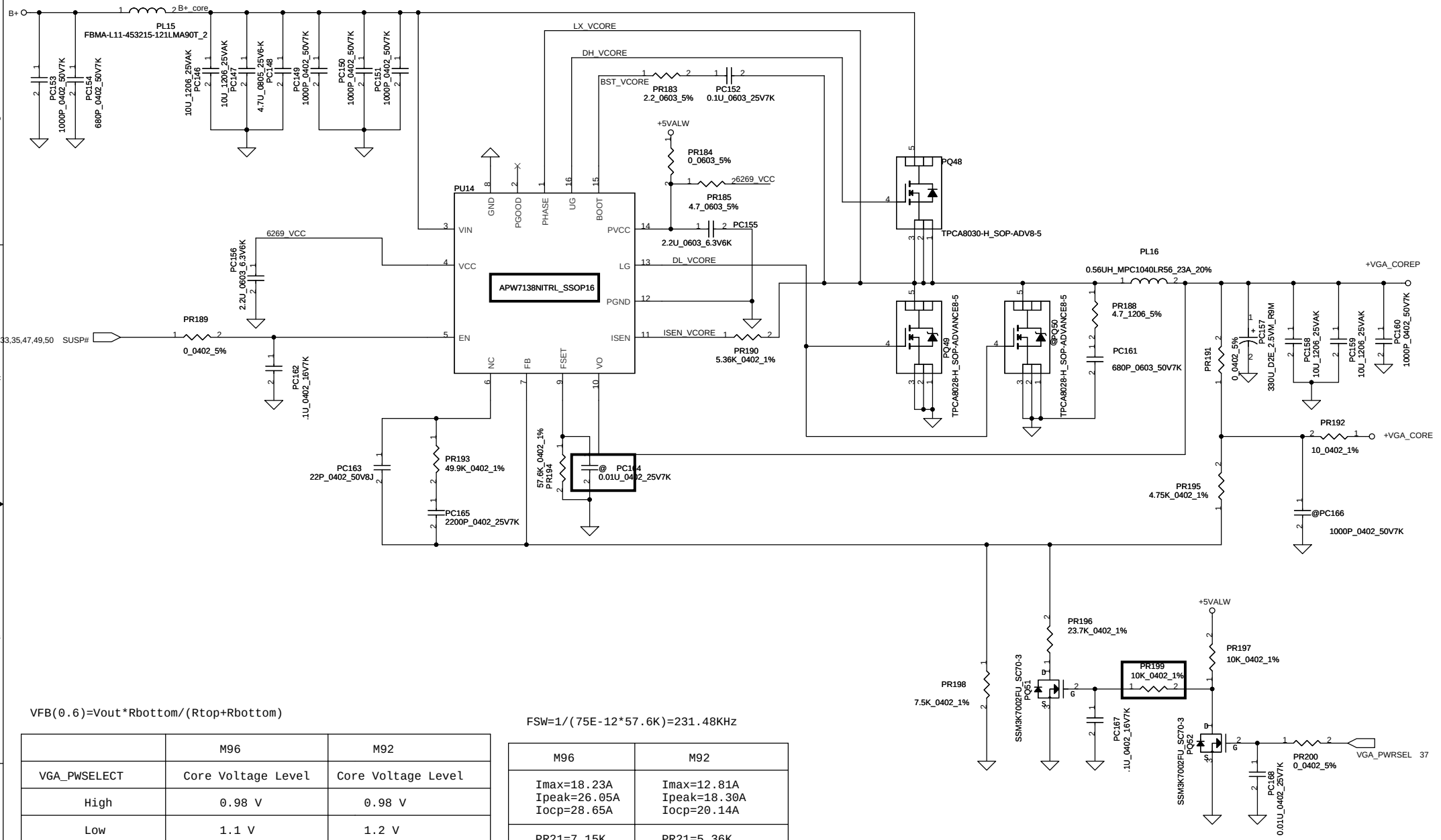
Date: Tuesday, February 23, 2010 | Sheet 51 of 54



VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

	M96	M92
VGA_PWSELECT	Core Voltage Level	Core Voltage Level
High	0.98 V	0.98 V
Low	1.1 V	1.2 V
resistor setting	PR26 = 4.75K PR30 =7.5K PR27 =23.7K	PR26 = 4.75K PR30 = 7.5K PR27 = 13K

FSW=1/(75E-12*57.6K)=231.48KHz

M96	M92
Imax=18.23A Ipeak=26.05A Iocp=28.65A	Imax=12.81A Ipeak=18.30A Iocp=20.14A
PR21=7.15K PQ5=unpop	PR21=5.36K PQ5=unpop

Security Classification	Compal Secret Data		
Issued Date	2008/10/23	Deciphered Date	2009/10/23

Compal Electronics, Inc.

Title: **Schematic, M/B LA-5331P**

Size	Document Number	Rev
Custom	401716	C

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Pre EVT modification

01. 2009/02/09 --> change UG3 to G9191-330T1U, P/N is SA000022I00
02. 2009/02/10 --> change UL3's P/N to SP050005V00
03. 2009/02/10 --> change R489 & R488 BOM structure
04. 2009/02/10 --> change R142 from 300 ohm to 150 ohm
05. 2009/02/10 --> change R143 from 1M ohm to 100K ohm
06. 2009/02/10 --> change JREAD footprint to TAITW_R009-125-LR_21P_RV-T
07. 2009/02/11 --> change +HDMI_5V_OUT circuit, add D18, R160, Q26, R557, C876 and change power
08. 2009/02/11 --> change UG1 P/N and velue to SA000039900 and TSH35TR
09. 2009/02/11 --> change location from CV2 to C706
10. 2009/02/13 --> remove WiMAX LED control circuit
11. 2009/02/17 --> remove Audio codec digital GND to analog GND net
12. 2009/02/17 --> Add JFAN1 for M96 FAN
13. 2009/02/17 --> change JTOUCH footprint
14. 2009/02/17 --> add NPTH Hole H42, H43
15. 2009/02/17 --> add CA12
16. 2009/02/17 --> change Int MIC ground to AGND between CA27 and J3
17. 2009/02/17 --> change UN1 P/N to SA00001SL20
18. 2009/02/17 --> Add JPWR1 for co-lay with JPOWER
19. 2009/02/19 --> add CA45, CA46, CA47, CA48, CA49, CA50, CA51, CA52, CA53
20. 2009/02/19 --> replace RA12, RA13, RA14 with CA54, CA55, CA56 and add CA57
21. 2009/02/19 --> Delete CV81, CV82, CV83, CV90, CV91, CV92, CV96, CV97, CV98
22. 2009/02/19 --> Change LV14, LV17, LV19 to 0 ohm
23. 2009/02/19 --> Swap M9X PCIE net & polarity inversion
24. 2009/02/19 --> Add CV345, CV346, R147 for soft start
25. 2009/02/19 --> Delete CV249, CV257, CV265, CV273, CV278, CV285, CV305, CV313, CV320, CV326, CV333, CV338
26. 2009/02/20 --> Add R189, R190 & Net：27MCLK, 27M_CLK, 27MSSC, 27M_SSC
27. 2009/02/20 --> Delete UV12, RV142, CV343, CV344, CV342, RV138, XV1, RV139
28. 2009/02/24 --> change R70, R77 from 4.7K to 2.2K
29. 2009/02/24 --> change R178 from 4.7K to 47K
30. 2009/02/26 --> change UG2 P/N to SA00003A600
31. 2009/02/27 --> change T9, T10, T11,T12, T19, T20 footprint to TPC24
32. 2009/02/27 --> Delete JFAN1
33. 2009/02/28 --> Change D36 from SC1B491D000 to SCS00002000
34. 2009/02/28 --> Change 5V camera power at JLVDS connector and add R968, R967, C274
35. 2009/02/28 --> Change SPI ROM from SST to MXIC
36. 2009/03/06 --> Change R556 BOM structure to @
37. 2009/03/06 --> Change D17, R965 BOM structure to @ and mount R966
38. 2009/03/06 --> Change RA16 from 5% to 1%

Pre DVT modification

39. 2009/03/10 --> Add ESD diode D19 for JFP
40. 2009/03/10 --> Change C686, C699, C702, C705, C708 P/N from SE074221K00 to SE074221K80
41. 2009/03/10 --> Change Y2 P/N from SJ114P3M730 to SJ114P3MG00
42. 2009/03/21 --> change R146 from 100k ohm to 10k ohm
43. 2009/03/21 --> change LAN_WAKE# & EC_SWI#
44. 2009/03/21 --> unmount USB sleep & charge, add R97 & R98
45. 2009/03/21 --> connect USB_OC#0 to LAN_WAKE# through 0 ohm (R35)
46. 2009/03/21 --> unmount HDMI CEC controller and related components.
47. 2009/03/21 --> change H42 from NPTH to PTH
48. 2009/03/21 --> change capacitor of SE068101K80 to SE071101J80
49. 2009/03/26 --> change F2 footprint to F_MINISMDC110F-2
50. 2009/03/26 --> Add R370 & R381
51. 2009/03/26 --> change R557's BOM structure from H@ to @
52. 2009/03/26 --> change R440 from 0 ohm to 100k ohm
53. 2009/03/26 --> Mount R197 and add R198
54. 2009/03/26 --> Change RA1 & RA3 P/N to SD013000080
55. 2009/04/02 --> ADD RM8
56. 2009/04/02 --> Change R440 from 100k ohm to 0 ohm and unmount C480
57. 2009/04/02 --> Change +HDMI_5V_OUT circuit, add D20, D53
58. 2009/04/14 --> Add C205、C213、C248、C478、C484、CV66、CV249 for EMI request
59. 2009/04/14 --> Mount CA54、CA55、CA56、CA57 for EMI requrest
60. 2009/04/14 --> Add C876 for Power noise issue
61. 2009/04/14 --> Add D21 for Power issue
62. 2009/04/15 --> Del TV2、TV3、TV4、TV5、TV6、TV7、TV8、TV9、TV10、TV11、TV12、TV13、TV14、TV15、TV16、TV17、TV18、TV19、TV20、TV21、TV22、TV23
63. 2009/04/17 --> Un-mount D12

Pre DVT modification

64. 2009/04/27 --> Un-mount DA6、DA7
65. 2009/04/27 --> Change C234、C876 P/N to SGA19331D00
66. 2009/04/27 --> Change RV45 P/N to SD028470280
67. 2009/04/27 --> Change RV140 P/N to SD034604A80
68. 2009/04/27 --> Un-mount R42
69. 2009/04/27 --> Mount R367
70. 2009/05/07 --> Change U25、U19 from SA005280110 to SA00002XX00
71. 2009/05/07 --> Change RA38 from LVDSSET@ to @
72. 2009/05/07 --> Change U34、U36 from SA00001NT00 to SA00001WP00
73. 2009/05/07 --> Change QV1 from SB923010020 to SB934130000
74. 2009/05/07 --> Change QV2 from SB000009610 to SB770020010

Pre PVT modification

75. 2009/05/24 --> Add H44,H45 H_3P0 for express dummy card
76. 2009/05/24 --> Change C350 from SF22001M300 to SF22001M200.
77. 2009/05/24 --> Add C178,C485,C486 for EMI request.
78. 2009/05/24 --> Del JPWR1
79. 2009/05/24 --> Del JPWR1,JCAM,R430,R428,C744,R20,R18
80. 2009/05/24 --> Change net name from USB20_N9_R_CAM & USB20_P9_R_CAM to USB20_N9_R & USB20_P9_R
81. 2009/05/24 --> Change UV2 ~ UV9 P/N & symbol to SA000035700

Pre Pre-MP modification

82. 2009/07/07 --> Change C643 & C652 to SE071120J80 .
83. 2009/07/07 --> Change C350 to SF000001H00.
84. 2009/08/06 --> Change Y7 PN from SJ100003D00 to SJ132P7KW10.
85. 2009/08/27 --> Change RV123 & RV124 BOM structure to HDMI@.
86. 2009/09/21 --> Change C9, C13, C70, C71, C83, C84, C95, C104, CL26, CL27 to SE074102K80
87. 2009/09/21 --> Change U34, U36 to SA00003GI00
88. 2009/10/02 --> Del RN2's BOM structure and move to SB side.

Pre EVT POWER modification

01. 2009/03/06 --> Mount PR95, PC66, PR170, PC129

EVT --> DVT modification

P46	add PR203 10Ohm
P46	change PR65 to 47K
P47, 48, 49, 50	PR82, 83, 94, 102, 110, 138, 152 change to SD013000080
P45	change PR36 to 13.7K
P50	change PC99 to SE071330J80
P47	change PR79 to 19.1K
P50	change PR145=21.5K, PR146=95.3K, PR143 and PR156 =16.5K, PR147 and PR159=4.02K
P49	change PR175 = 33K, PC139 to mount
P51	change PR199 = 10K
P47, 48, 49	add 3PCS Cap.=0.1uF_0402 (PC177, PC178, PC179) on B+

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HW4 Product Improvement Record (P.I.R.)

< Tigris >

< R1 for customer BOM STRUCTURE >		< R3 for mass production BOM STRUCTURE >	
RS880MN	U3	RS880MN	U3
RS880MNR1@	RS880MN R1	RS880MNR3@	RS880MN R3
RS880MC	U3	RS880MC	U3
RS880MCR1@	RS880MC R1	RS880MCR3@	RS880MC R3
RX881	U3	RX881	U3
RX881R1@	RX881 R1	RX881R3@	RX881 R3
SB710	U15	SB710	U15
SB710R1@	SB710 R1	SB710R3@	SB710 R3

< DC Jack >

DC-IN	PJP1	
16inch_45@	PJP1	
DC-IN	PJP1	
17inch_45@	PJP1	

< PCB >

PCB	ZZZ	
PCB 075 LA-5331P REV1.0 M/B		

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