LC2A Schematic

Pentium-M

945GM+ICH7

DATE: Sept. 10th Revision: 0.2

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5	Power Block
6	Yonah(1/2)-GTL/ITP-XDP
7	Yonah(2/2)-PWR/GND
8	Yonah bypass
9	Calistoga(1/6)-GTL/DMI/DDR
10	Calistoga(2/6)-DDR2 A/B CH
11	Calistoga(3/6)-VGA/LVDS/TV
12	Calistoga(4/6)-PWR
13	Calistoga(5/6)-PWR/GND
14	Calistoga(6/6)-PWR/GND
15	DDRII-SODIMM2
16	DDRII SO-DIMM B
17	ClockGen
18	TV-OUT/LVDS/CRT
19	ICH7M(1/4)_HUB,PCI,HOST
20	ICH7M(2/4)LAN,ATA,LPC,RTC
21	ICH7M(3/4)USB,GPIO,PCIE
22	ICH7-M(4/4)_POWER&GND
23	SATA/CD_ROM/G-SENSORConn.
24	USB/BlueTooth/FP
25	BCM5751M-GLAN
26	RJ-45 Connector
27	MINI_CARD SLOT-WLAN
28	R5C842-PCI/CARD BUS/OHCI
29	CARD BUS/1394
30	HD Audio Codec_ALC260D
31	AMP./Audio Jack
32	ENE-KB910L/TPM
33	BIOS/EE-Prom/TP/KB/SW
34	DC TO DC
35	PWR DCIN / Precharge
36	PWR CPU OTP
37	PWR-Battery Select
38	PWR-Charger
39	PWR-3V/5V
40	PWR-1.8V/1.5V
41	PWR-VCCPP/2.5V/0.9V
42	PWR-CPU_CORE

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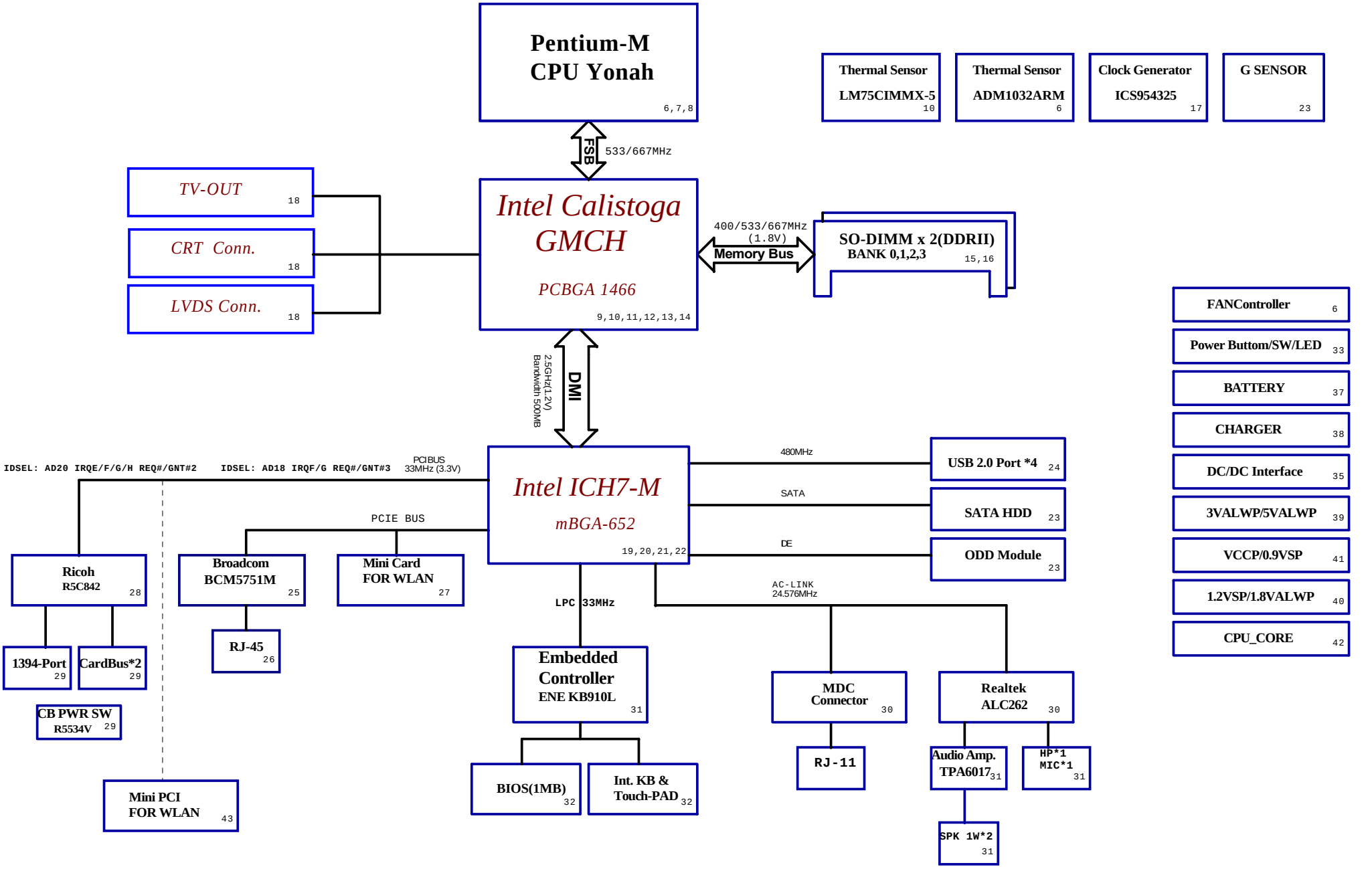
BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+0.9VS	0.9V power rail	ON	OFF	OFF
+3.3V	3.3V switched power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5V	5V always on power rail	ON	ON	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(R5C842)	AD20	2	PIRQE/PIRQF/PIRQG/PIRQH
Mini-PCI(WLAN)	AD18	3	PIRQG/PIRQH

EC SM Bus1 address

Device	Address
Main Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
ADM1032	1001 110X b

EC SM Bus2 address

Device	Address
KXP84-0200	0011 000X b
Second Battery	
LM75CIMMX-5	

ICH7 SM Bus address

Device	Address
Clock Generator (ICS954325AKLFT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 001Xb

Dip SW function

KBSEL0/1#	11:JP K/B 01:US K/B 10:UK K/B 00: Reserve
PASSWORD#	0:Override 1:Avaliable
FINGERPRINT#	0:Existence 1:Non-Existence

Function Table

Function	Japan			HK/CHINA	Comment
	Commercial	Consumer			
		LaVie	NEC Direct(Internet Retailing)		
TV-OUT	Yes	<—	<—	<—	
Bluetooth	No	Yes	<—	<—	Need BTO
PWR LED (Odekake)	No	<—	<—	<—	Not need Odekake
S/W	I/II Key	<—	<—	<—	all same
4 in 1 Card Adapter	No	Yes	<—	<—	
Finger Print	Yes (BTO)	No	Yes (BTO)	No	Need BTO
TPM	Yes	No	<—	<—	Need BTO
W-LAN	JP	JP	JP	Oversea	

Chip Reversion

Chip \ Phase	ES Phase	PP Phase	MP1 Phae	IRT
945GM	A2			
ICH7	B0			
CLK Gen	A			
KB910L	A1			
ALC262	A2			
BCM5751	C1			

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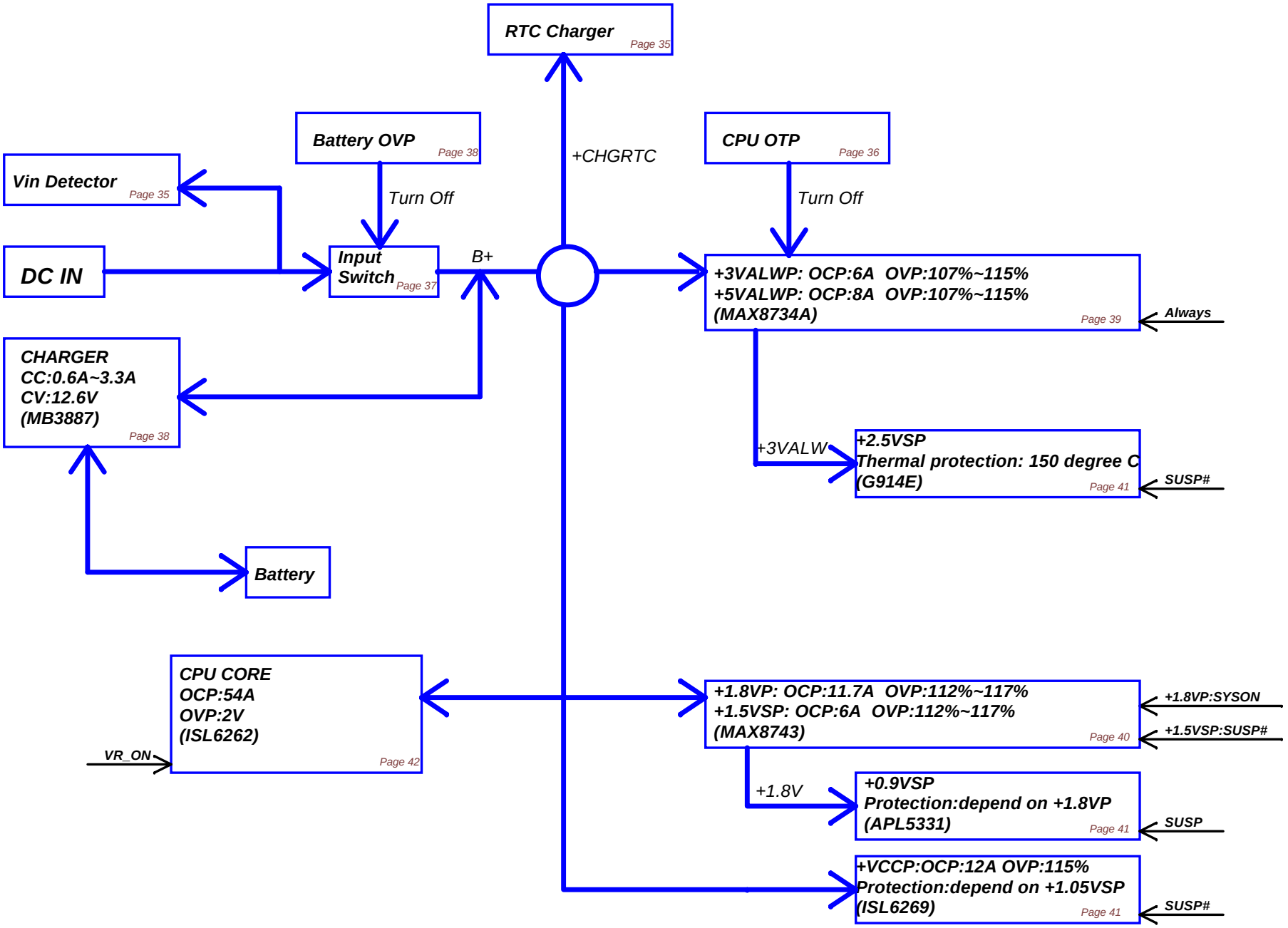
LC2a Power block



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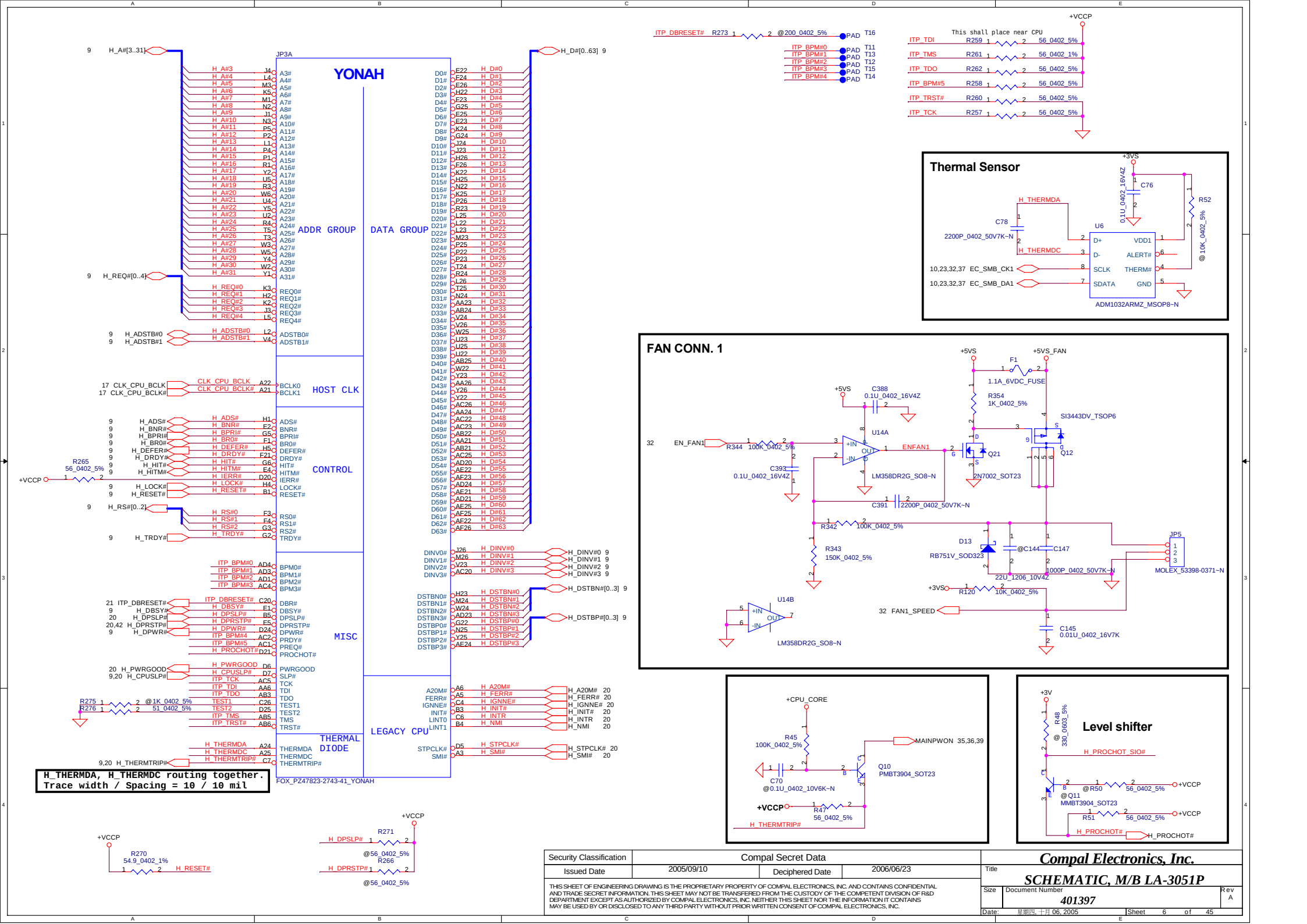

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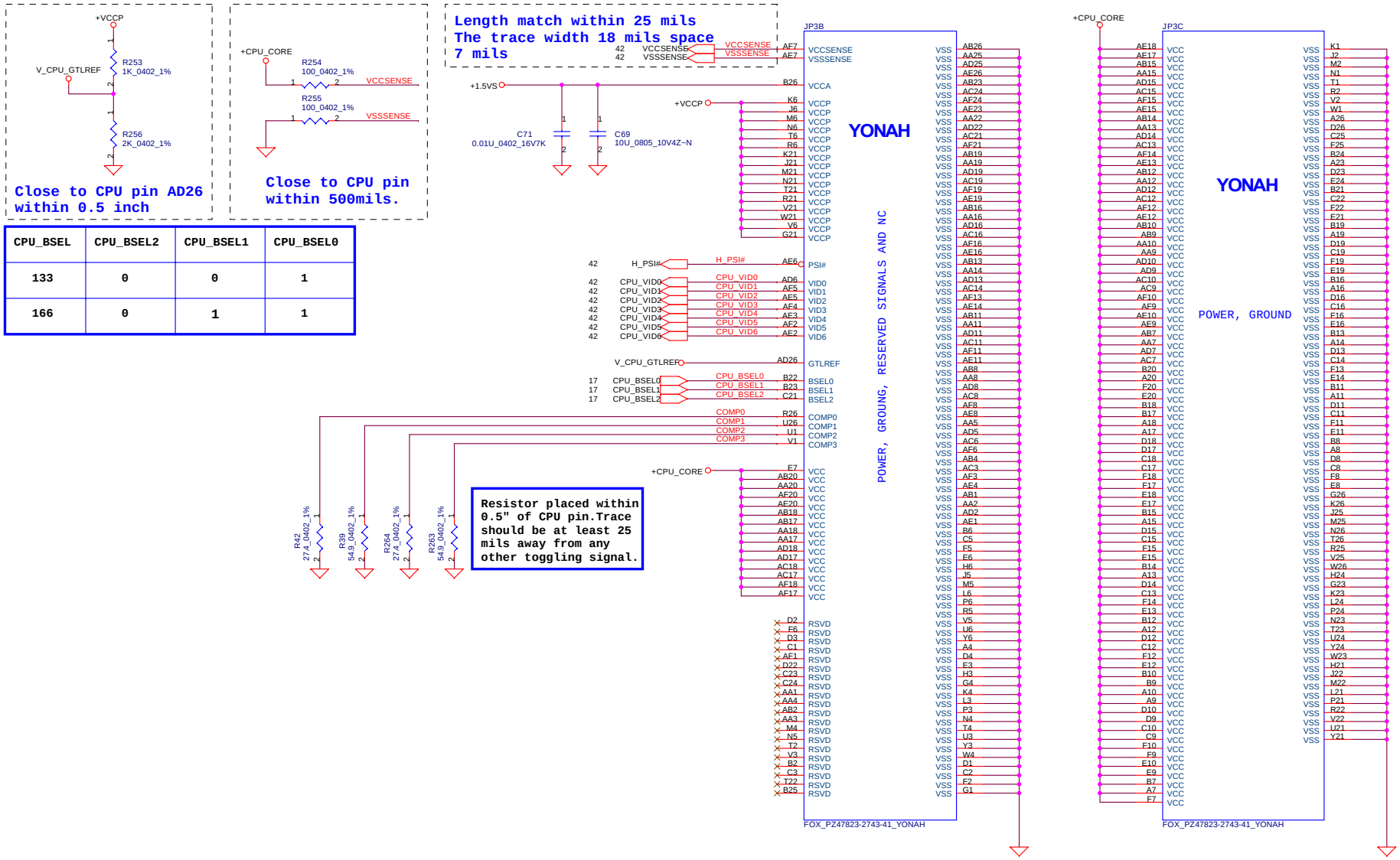

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

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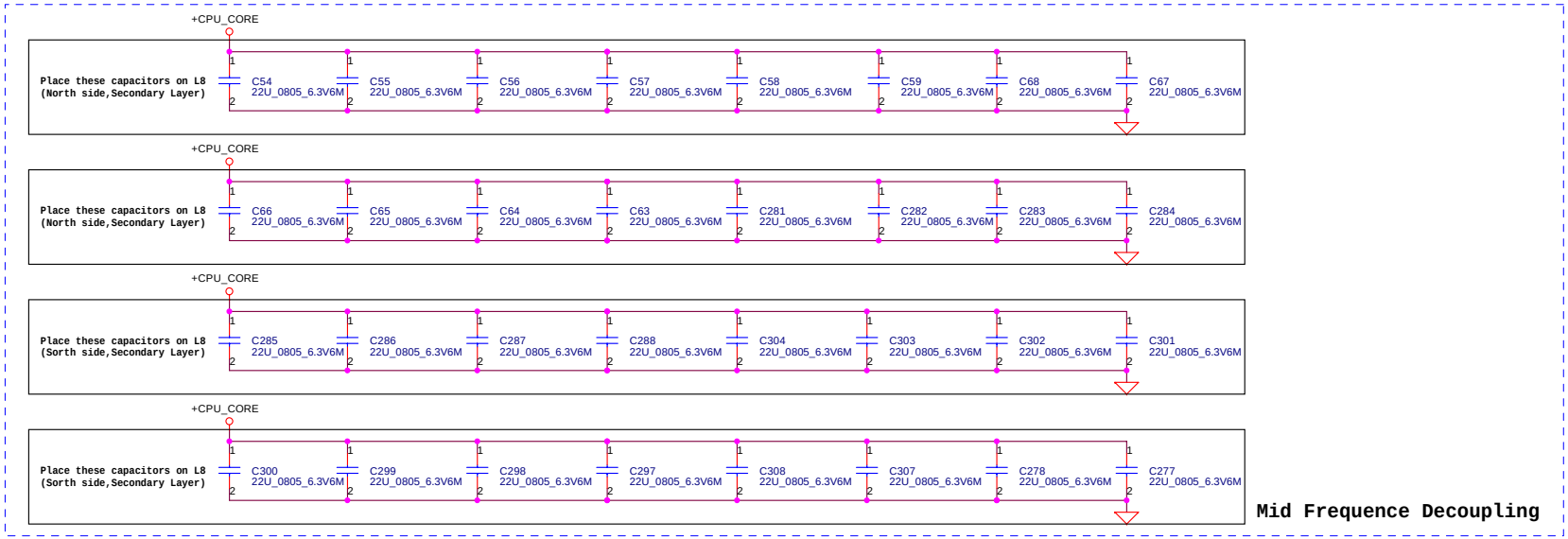
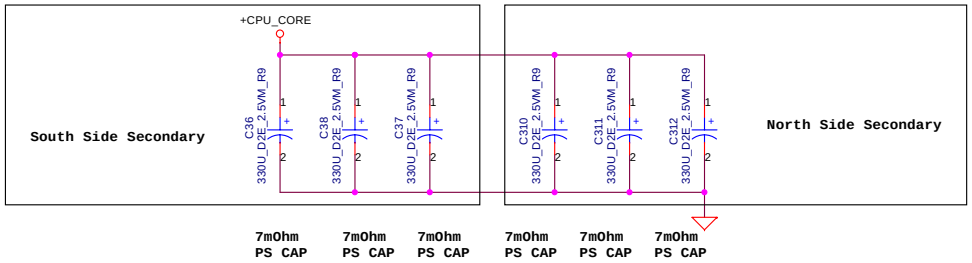
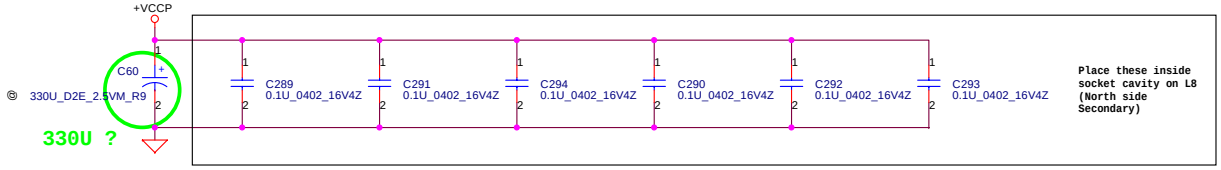




ESR <= 1.5m ohm
Capacitor > 1980uF



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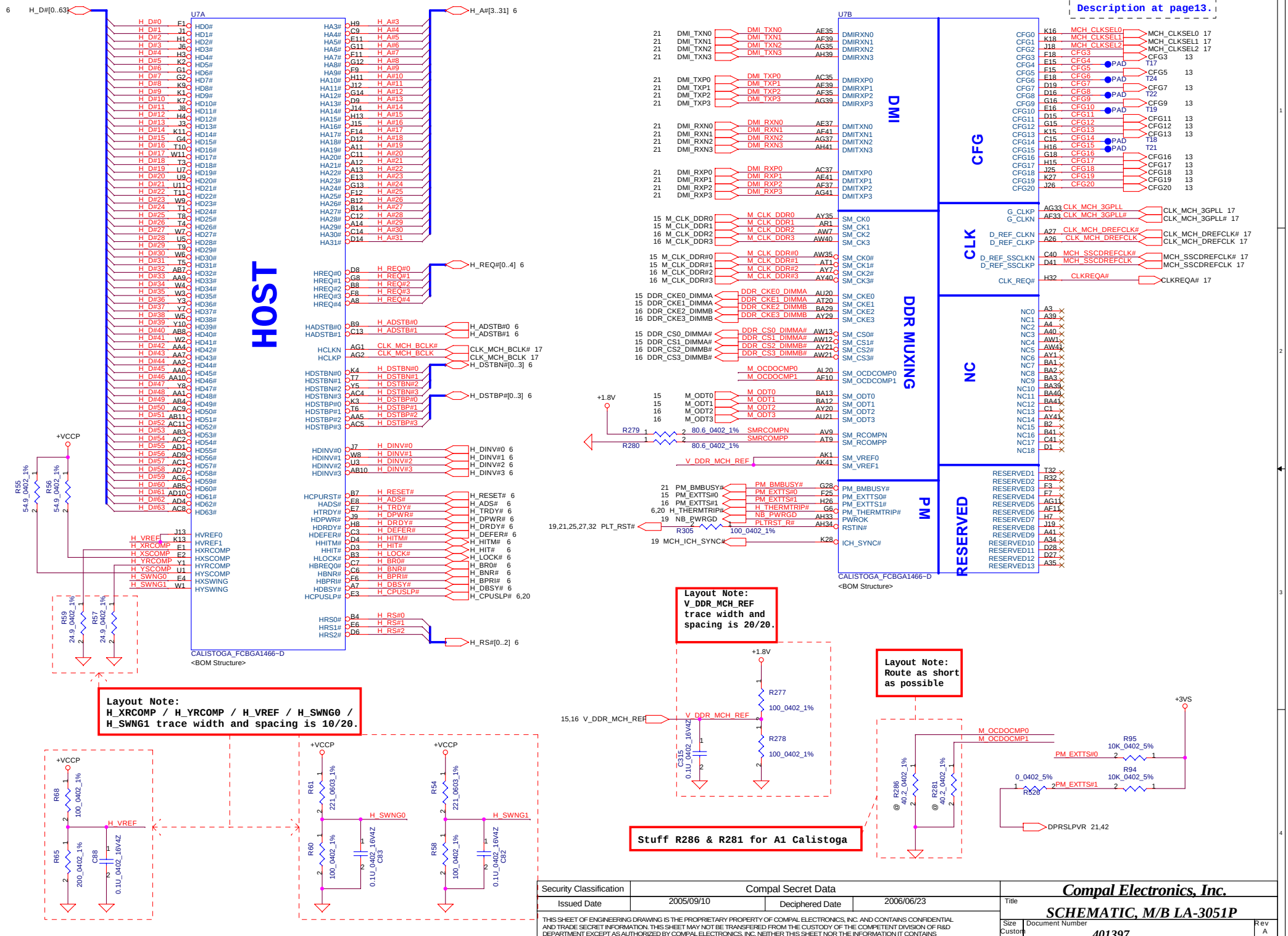

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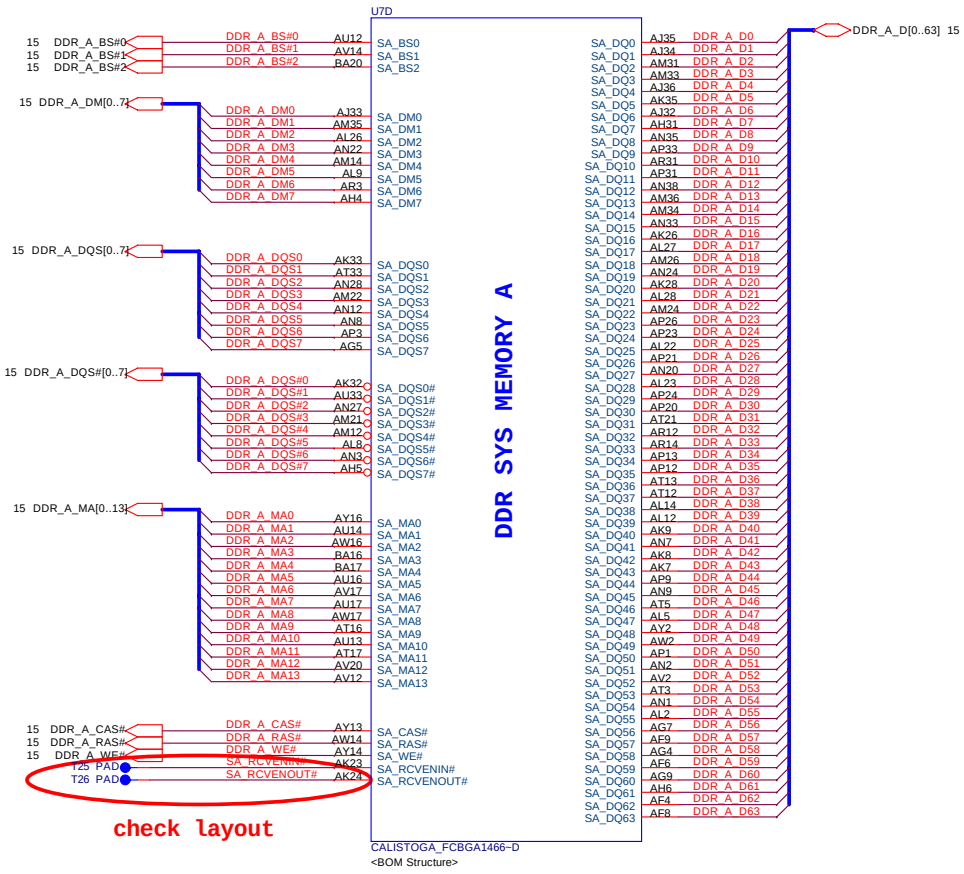

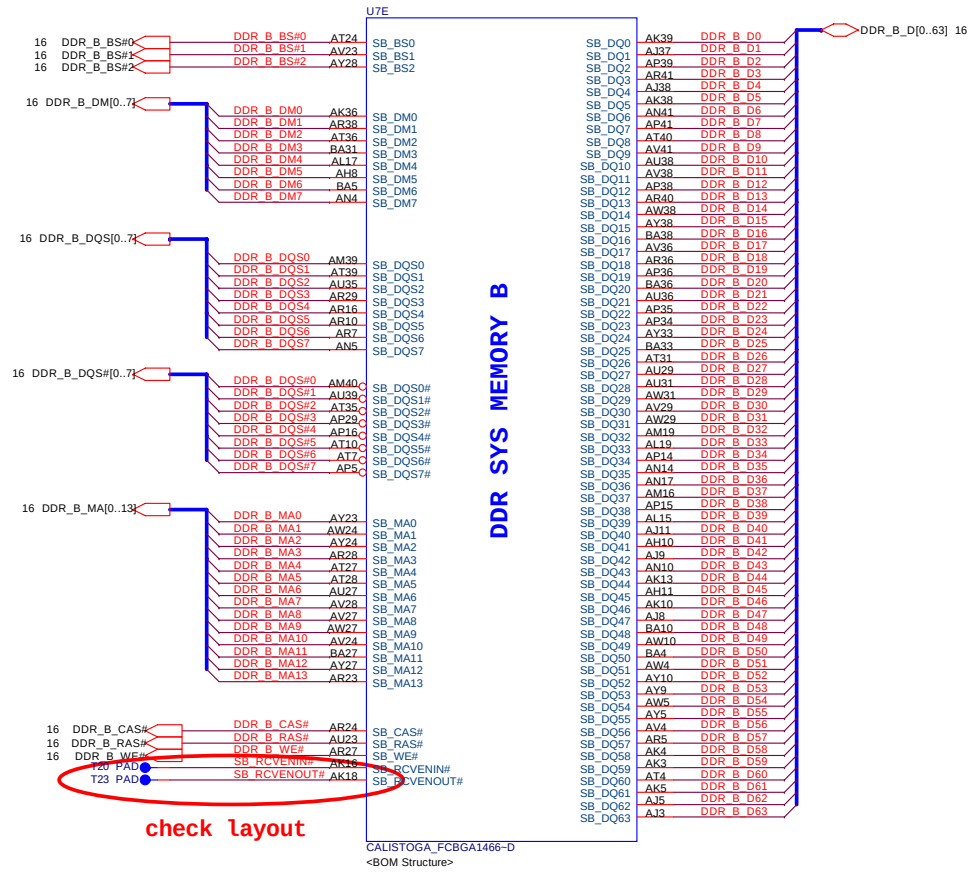

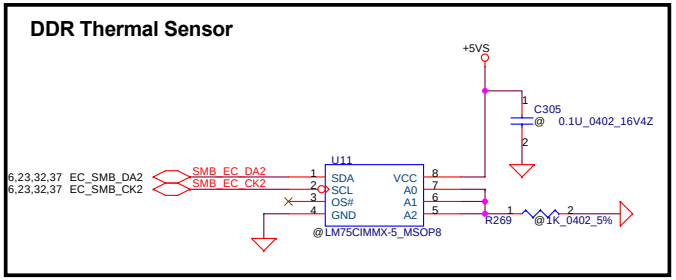

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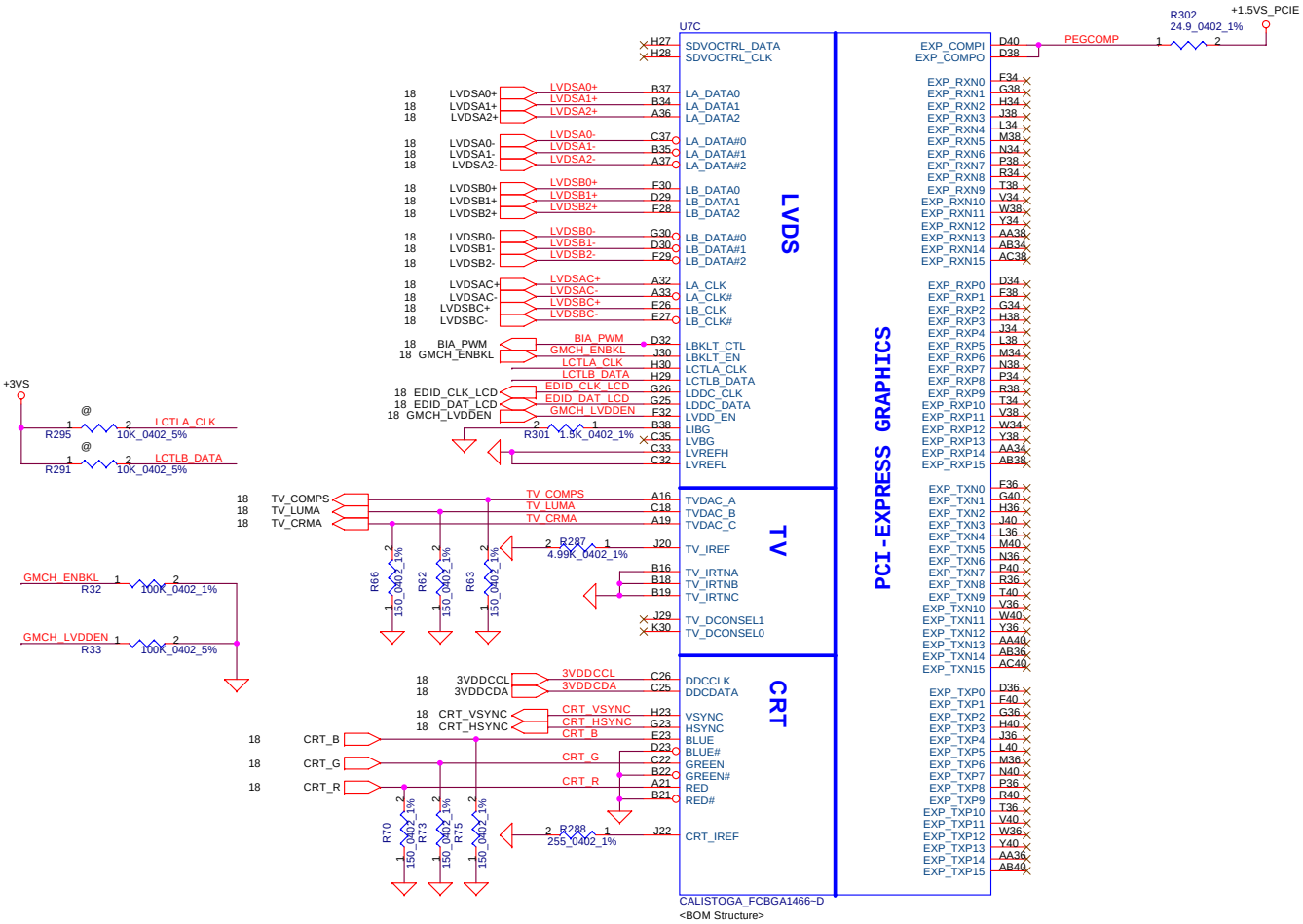

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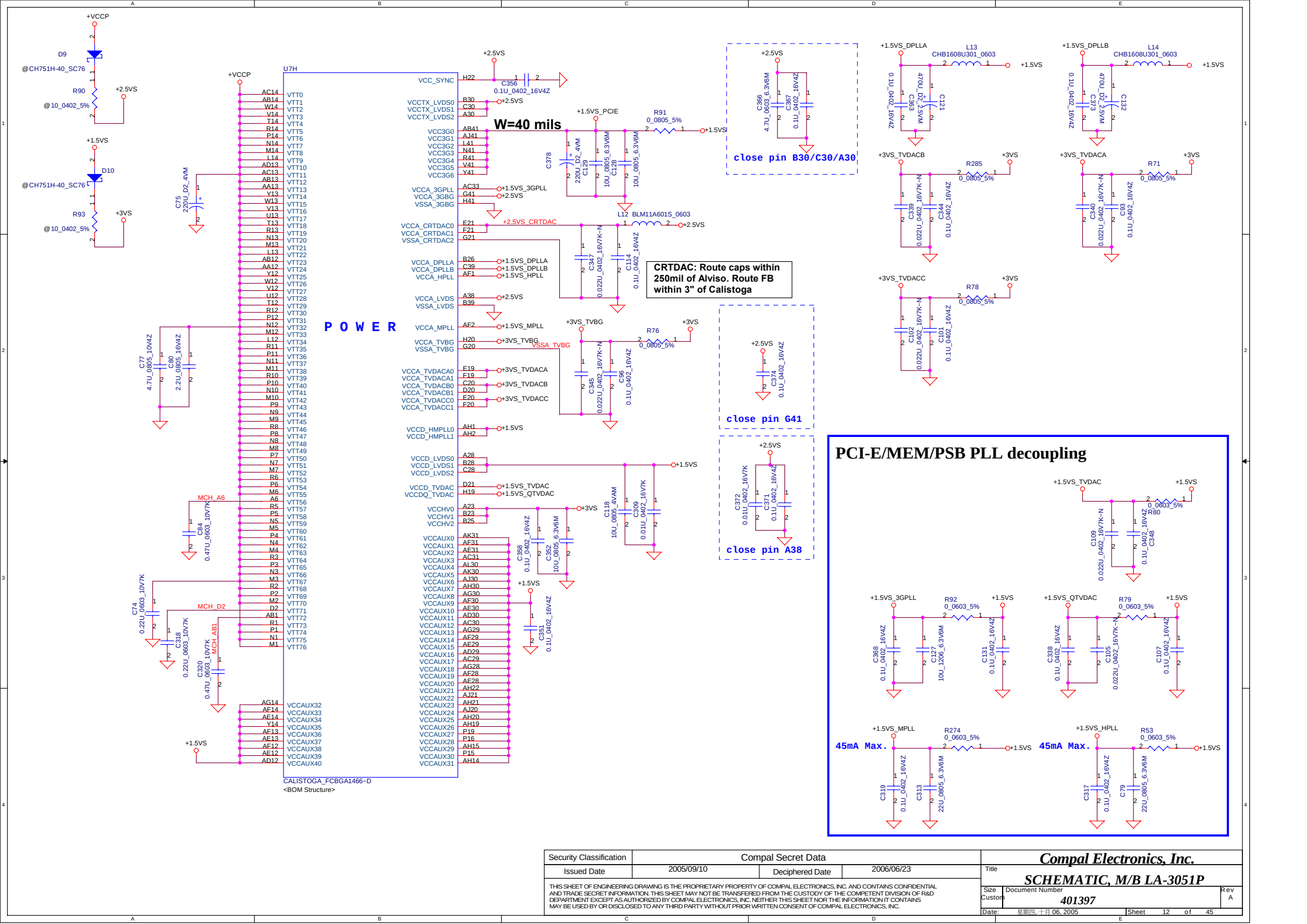

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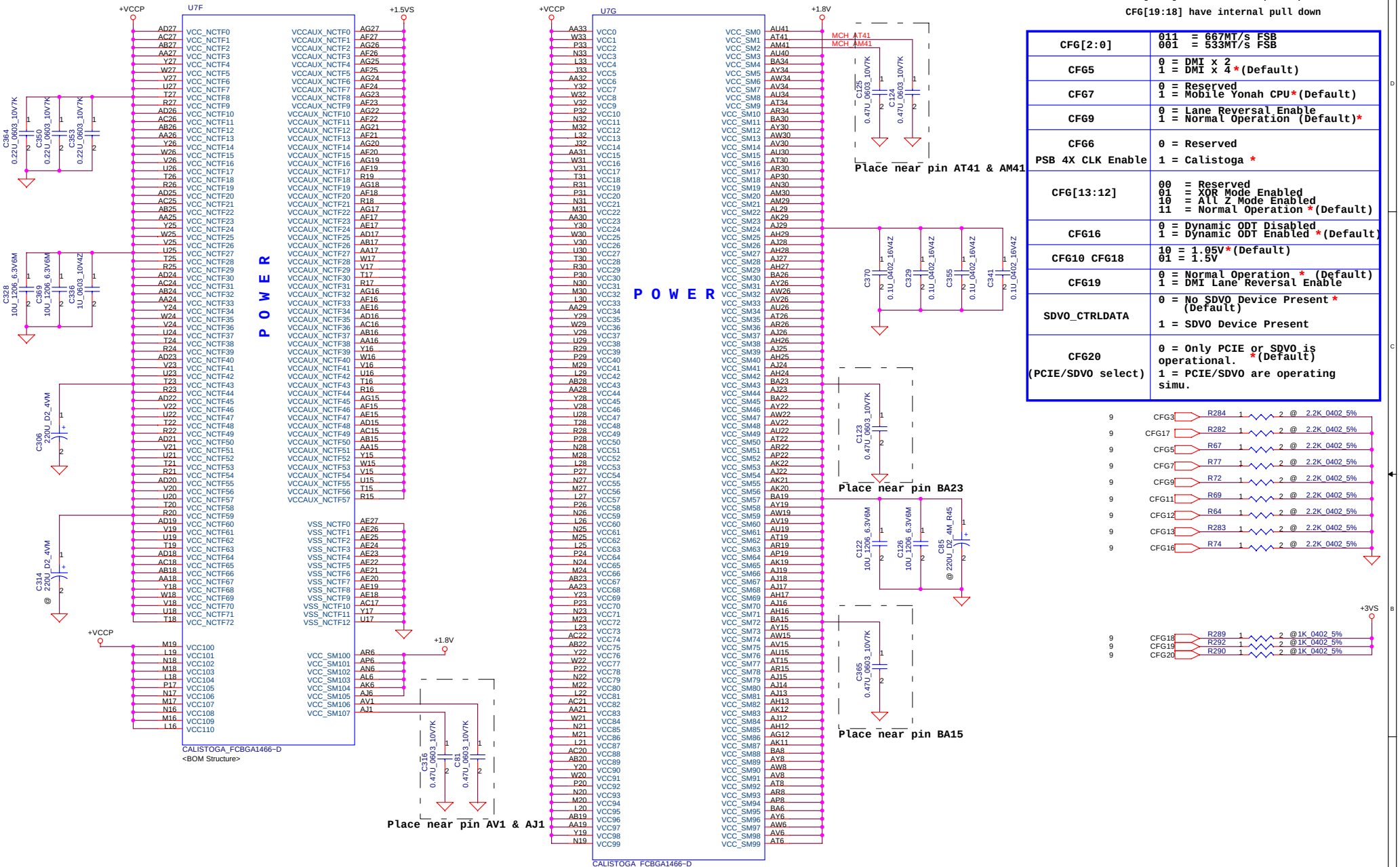
Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6 PSB 4X CLK Enable	0 = Reserved 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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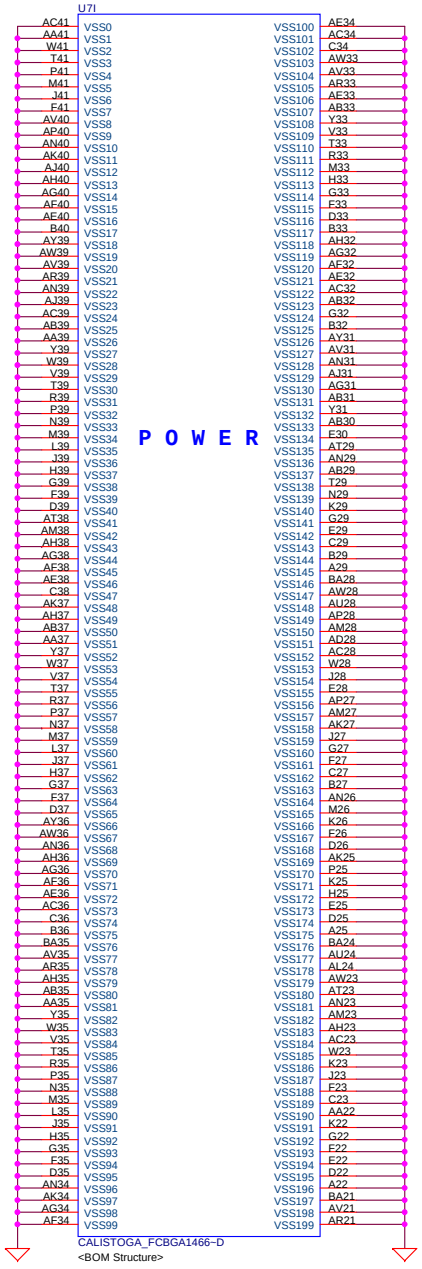

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10 DDR_A_DQS#[0..7]
10 DDR_A_D[0..63]
10 DDR_A_DM[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_MA[0..13]

Layout Note:
Place near JP41

+1.8V

2.2U_0603_6.3V6K C86
2.2U_0603_6.3V6K C116
2.2U_0603_6.3V6K C87
2.2U_0603_6.3V6K C115
2.2U_0603_6.3V6K C113
0.1U_0402_16V4Z C111
0.1U_0402_16V4Z C98
0.1U_0402_16V4Z C103
0.1U_0402_16V4Z C89

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS

0.1U_0402_16V4Z C99
0.1U_0402_16V4Z C97
0.1U_0402_16V4Z C94
0.1U_0402_16V4Z C91
0.1U_0402_16V4Z C110
0.1U_0402_16V4Z C106
0.1U_0402_16V4Z C92
0.1U_0402_16V4Z C90
0.1U_0402_16V4Z C95
0.1U_0402_16V4Z C100
0.1U_0402_16V4Z C104
0.1U_0402_16V4Z C108
0.1U_0402_16V4Z C112

+0.9VS

RP10 56_0404_4P2R_5%: DDR_A_MA5, DDR_A_MA8
RP14 56_0404_4P2R_5%: DDR_A_BS#2, DDR_CKE0_DIMMA
RP8 56_0404_4P2R_5%: DDR_A_MA1, DDR_A_MA3
RP12 56_0404_4P2R_5%: DDR_A_MA7, DDR_A_MA6
RP6 56_0404_4P2R_5%: DDR_A_RAS#, DDR_CS0_DIMMA#
RP11 56_0404_4P2R_5%: DDR_A_MA9, DDR_A_MA12
RP5 56_0404_4P2R_5%: DDR_A_BS#0, DDR_A_MA10
RP9 56_0404_4P2R_5%: DDR_A_MA4, DDR_A_MA2
RP3 56_0404_4P2R_5%: DDR_A_CAS#, DDR_A_WE#
RP7 56_0404_4P2R_5%: DDR_A_MA0, DDR_A_BS#1
RP2 56_0404_4P2R_5%: DDR_CS1_DIMMA#, M_ODT1
RP4 56_0404_4P2R_5%: M_ODT0, DDR_A_MA13
RP13 56_0404_4P2R_5%: DDR_CKE1_DIMMA, DDR_A_MA11

Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"

+1.8V

JP4 FOX_AS0A426-N8RN-7F-N

1 VREF	2 VSS		
3 VSS	4 DQ4	DDR_A_D6	
DDR_A_D4 5 DQ0	6 DQ5	DDR_A_D0	
DDR_A_D1 7 DQ1	8 VSS		
9 VSS	10 DM0	DDR_A_DM0	
DDR_A_DQS#0 11 DQS0#	12 VSS		
DDR_A_DQS0 13 DQS0	14 DQ6	DDR_A_D5	
15 VSS	16 DQ7	DDR_A_D7	
DDR_A_D2 17 DQ2	18 VSS		
DDR_A_D3 19 DQ3	20 DQ12	DDR_A_D13	
21 VSS	22 DQ13	DDR_A_D12	
DDR_A_D8 23 DQ8	24 VSS		
DDR_A_D14 25 DQ9	26 DM1	DDR_A_DM1	
27 VSS	28 VSS		
DDR_A_DQS#1 29 DQS1#	30 CK0	M_CLK_DDR0	M_CLK_DDR0 9
DDR_A_DQS1 31 DQS1	32 CK0#	M_CLK_DDR#0	M_CLK_DDR#0 9
33 VSS	34 VSS		
DDR_A_D9 35 DQ10	36 DQ14	DDR_A_D11	
DDR_A_D15 37 DQ11	38 DQ15	DDR_A_D10	
39 VSS	40 VSS		
41 VSS	42 VSS		
DDR_A_D16 43 DQ16	44 DQ20	DDR_A_D20	
DDR_A_D17 45 DQ17	46 DQ21	DDR_A_D21	
47 VSS	48 VSS		
DDR_A_DQS#2 49 DQS2#	50 NC		
DDR_A_DQS2 51 DQS2	52 DM2	DDR_A_DM2	R83 2 1 0_0402_5% PM_EXTTS#0 9
53 VSS	54 VSS		
DDR_A_D18 55 DQ18	56 DQ22	DDR_A_D23	
DDR_A_D19 57 DQ19	58 DQ23	DDR_A_D22	
59 VSS	60 VSS		
DDR_A_D29 61 DQ24	62 DQ28	DDR_A_D28	
DDR_A_D24 63 DQ25	64 DQ29	DDR_A_D25	
65 VSS	66 VSS		
DDR_A_DM3 67 DM3	68 DQS3#	DDR_A_DQS#3	
69 NC	70 DQS3	DDR_A_DQS3	
71 VSS	72 VSS		
DDR_A_D26 73 DQ26	74 DQ30	DDR_A_D31	
DDR_A_D27 75 DQ27	76 DQ31	DDR_A_D30	
77 VSS	78 VSS		
9 DDR_CKE0_DIMMA DDR_CKE0_DIMMA 79 CKE0	80 NC/CKE1	DDR_CKE1_DIMMA	DDR_CKE1_DIMMA 9
81 VDD	82 VDD		
83 NC	84 NC/A15		
10 DDR_A_BS#2 DDR_A_BS#2 85 BA2	86 NC/A14		
87 VDD	88 VDD		
DDR_A_MA12 89 A12	90 A11	DDR_A_MA11	
DDR_A_MA9 91 A9	92 A7	DDR_A_MA7	
DDR_A_MA8 93 A8	94 A6	DDR_A_MA6	
95 VDD	96 VDD		
DDR_A_MA5 97 A5	98 A4	DDR_A_MA4	
DDR_A_MA3 99 A3	100 A2	DDR_A_MA2	
DDR_A_MA1 101 A1	102 A0	DDR_A_MA0	
103 VDD	104 VDD		
DDR_A_MA10 105 A10/AP	106 BA1	DDR_A_BS#1	DDR_A_BS#1 10
10 DDR_A_BS#0 DDR_A_BS#0 107 BA0	108 RAS#	DDR_A_RAS#	DDR_A_RAS# 10
10 DDR_A_WE# DDR_A_WE# 109 WE#	110 S0#	DDR_CS0_DIMMA#	DDR_CS0_DIMMA# 9
111 VDD	112 VDD		
10 DDR_A_CAS# DDR_A_CAS# 113 CAS#	114 ODT0	M_ODT0	M_ODT0 9
9 DDR_CS1_DIMMA# DDR_CS1_DIMMA# 115 NC/S1#	116 NC/A13	DDR_A_MA13	
117 VDD	118 VDD		
9 M_ODT1 M_ODT1 119 NC/ODT1	120 NC		
121 VSS	122 VSS		
DDR_A_D37 123 DQ32	124 DQ36	DDR_A_D39	
DDR_A_D36 125 DQ33	126 DQ37	DDR_A_D38	
127 VSS	128 VSS		
DDR_A_DQS#4 129 DQS4#	130 DM4	DDR_A_DM4	
DDR_A_DQS4 131 DQS4	132 VSS		
133 VSS	134 DQ38	DDR_A_D34	
DDR_A_D35 135 DQ34	136 DQ39	DDR_A_D33	
DDR_A_D32 137 DQ35	138 VSS		
139 VSS	140 DQ44	DDR_A_D45	
DDR_A_D40 141 DQ40	142 DQ45	DDR_A_D43	
DDR_A_D44 143 DQ41	144 VSS		
145 VSS	146 DQS5#	DDR_A_DQS#5	
DDR_A_DM5 147 DM5	148 DQS5	DDR_A_DQS5	
149 VSS	150 VSS		
DDR_A_D41 151 DQ42	152 DQ46	DDR_A_D47	
DDR_A_D46 153 DQ43	154 DQ47	DDR_A_D42	
155 VSS	156 VSS		
DDR_A_D49 157 DQ48	158 DQ52	DDR_A_D52	
DDR_A_D48 159 DQ49	160 DQ53	DDR_A_D53	
161 VSS	162 VSS		
163 NC,TEST	164 CK1	M_CLK_DDR1	M_CLK_DDR1 9
165 VSS	166 CK1#	M_CLK_DDR#1	M_CLK_DDR#1 9
DDR_A_DQS#6 167 DQS6#	168 VSS		
DDR_A_DQS6 169 DQS6	170 DM6	DDR_A_DM6	
171 VSS	172 VSS		
DDR_A_D54 173 DQ50	174 DQ54	DDR_A_D51	
DDR_A_D50 175 DQ51	176 DQ55	DDR_A_D55	
177 VSS	178 VSS		
DDR_A_D61 179 DQ56	180 DQ60	DDR_A_D57	
DDR_A_D60 181 DQ57	182 DQ61	DDR_A_D56	
183 VSS	184 VSS		
DDR_A_DM7 185 DM7	186 DQS7#	DDR_A_DQS#7	
187 VSS	188 DQS7	DDR_A_DQS7	
DDR_A_D59 189 DQ58	190 VSS		
DDR_A_D58 191 DQ59	192 DQ62	DDR_A_D62	
193 VSS	194 DQ63	DDR_A_D63	
16,17 CLK_SMBDATA CLK_SMBDATA 195 SDA	196 VSS		
16,17 CLK_SMBCLK CLK_SMBCLK 197 SCL	198 SA0		
+3VS 199 VDDSPD	200 SA1		

C72 0.1U_0402_16V4Z
C73 2.2U_0603_6.3V6K

R46 10K_0402_5%
R49 10K_0402_5%

SO-DIMM A REVERSE

Top side

V_DDR_MCH_REF

Close to VREF pins of SO-DIMM

V_DDR_MCH_REF 9,16

C130 2.2U_0805_16V4Z
C133 0.1U_0402_16V4Z

Close to connect

+1.8V
R306 @100_0402_1%
V_DDR_MCH_REF
R304 @100_0402_1%
C375 @ 0.1U_0402_16V4Z

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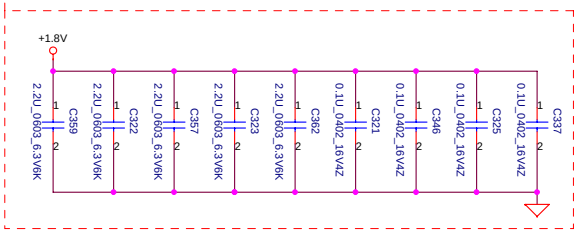
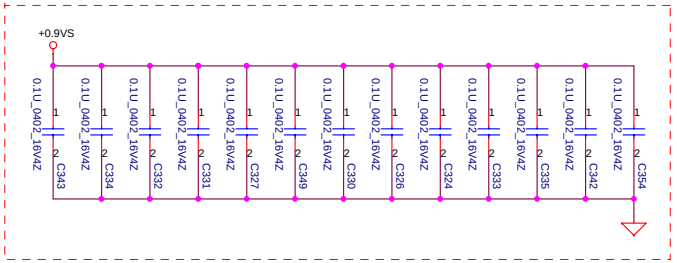
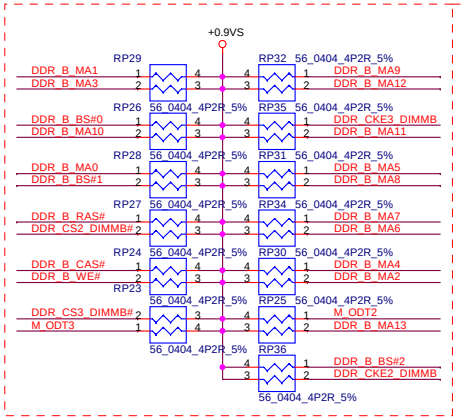
10 DDR_B_DQS#[0..7]
10 DDR_B_D[0..63]
10 DDR_B_DM[0..7]
10 DDR_B_DQS[0..7]
10 DDR_B_MA[0..13]

Layout Note:
Place near JP42

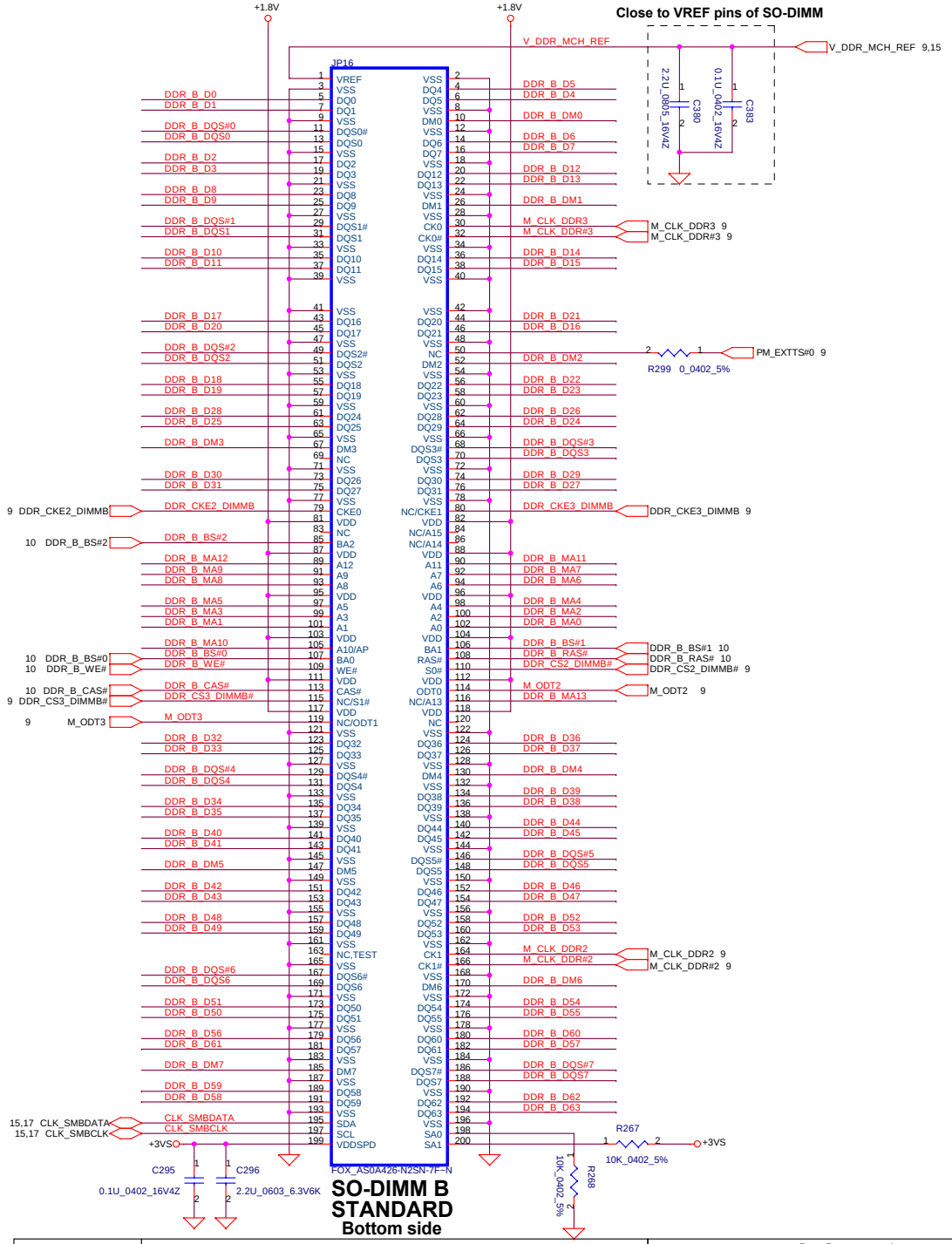


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"



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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954325

Reserved for PCI CLK when use ICS954305

ICS_CLK GEN BUG, need FSC pull down

Place crystal within 500 mils of CK410

Place near U54
Place these components near each pin within 40 mils.

LCD clock select

PCI_ICH = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

Note: pin34 have invert this logic

High:Pin18/19 = 100MHz
*Low:Pin18/19 = 96MHz

PCI_PME=SEL_PCI6

PCI_PCM	PIN27
0	CLKREQ5
1	PCICLK6

PCI_PME=SEL_PCI5

PCI_PCM	PIN22
0	CLKREQ3
1	PCICLK5

ICS954305AKLFT MLF 72P

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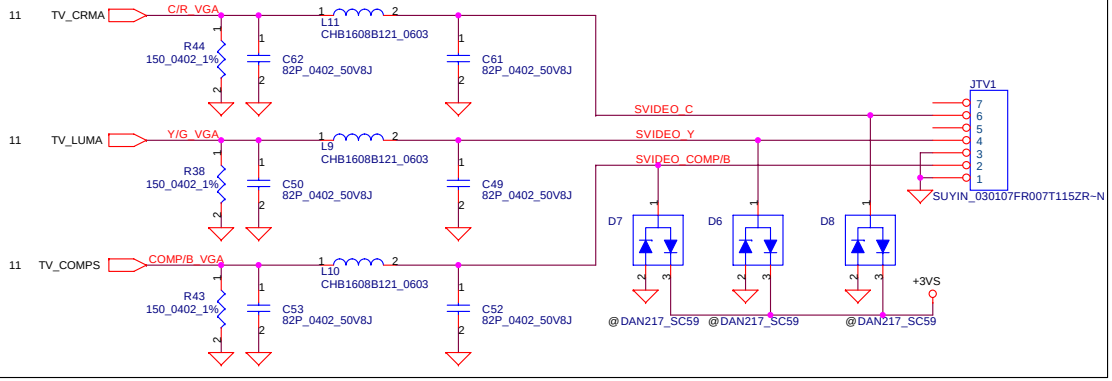
TV-OUT Connector



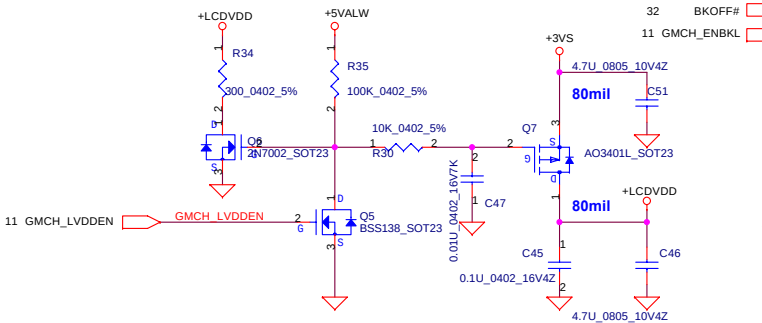
W to B Pin Define

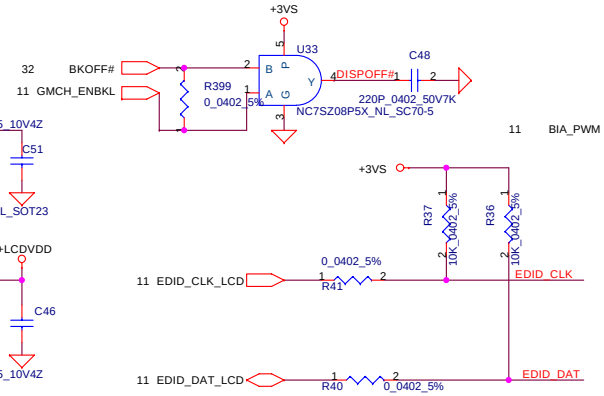
B+	1	2	B+
DISPOFF#	3	4	GND
INVT_PWM	5	6	DAC_BRIG
EDID_DAT	7	8	EDID_CLK
UTX0-	9	10	GND
UTX0+	11	12	LTX1-
GND	13	14	LTX1+
UTX1-	15	16	GND
UTX1+	17	18	LTX2-
GND	19	20	LTX2+
UTX2-	21	22	GND
UTX2+	23	24	LTX0-
GND	25	26	LTX0+
UTX3-	27	28	GND
UTX3+	29	30	LCLK-
GND	31	32	LCLK+
UCLK-	33	34	GND
UCLK+	35	36	LTX3-
LCDVDD	37	38	LTX3+
LCDVDD	39	40	+3VS

Inverter Pin Define

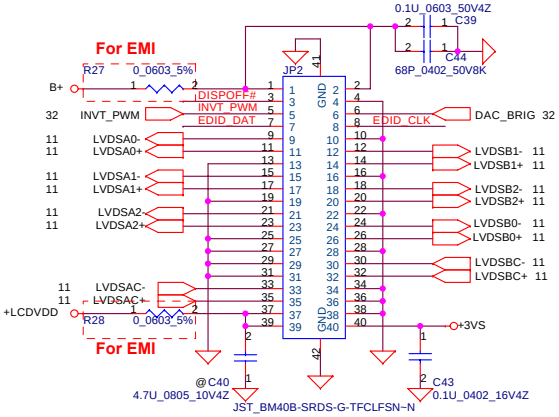
1	INV_PWR
2	INV_PWR
3	INV_PWM
4	DISOFF#
5	DAC_BRIG
6	GND
7	GND

PANEL +LCDVDD CTRL CKT

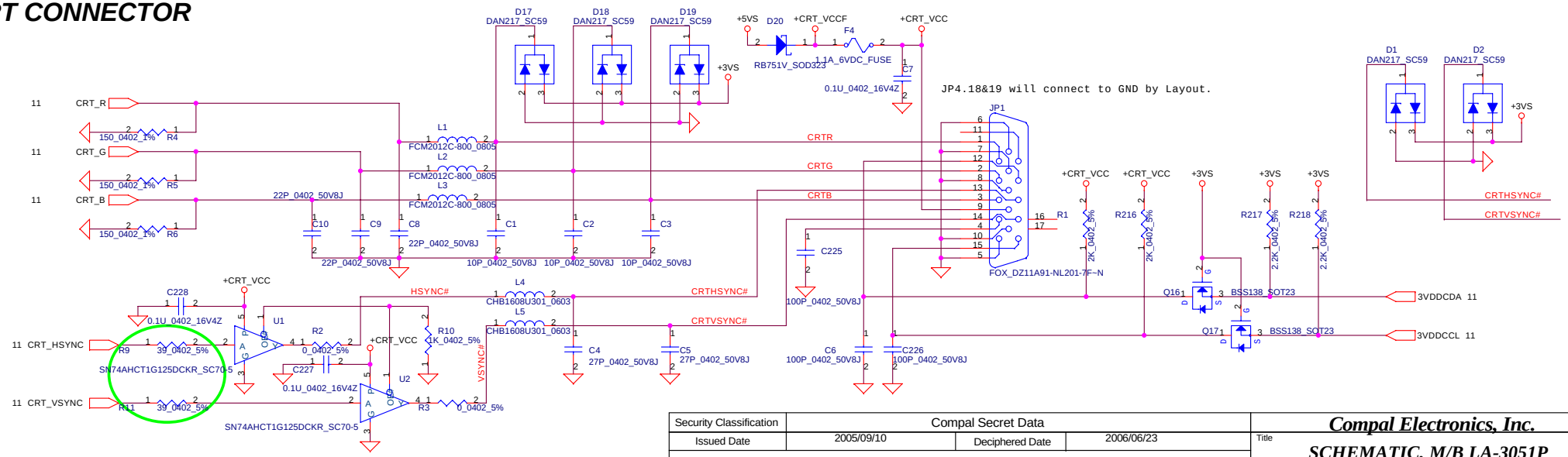




LVDS from NB



CRT CONNECTOR



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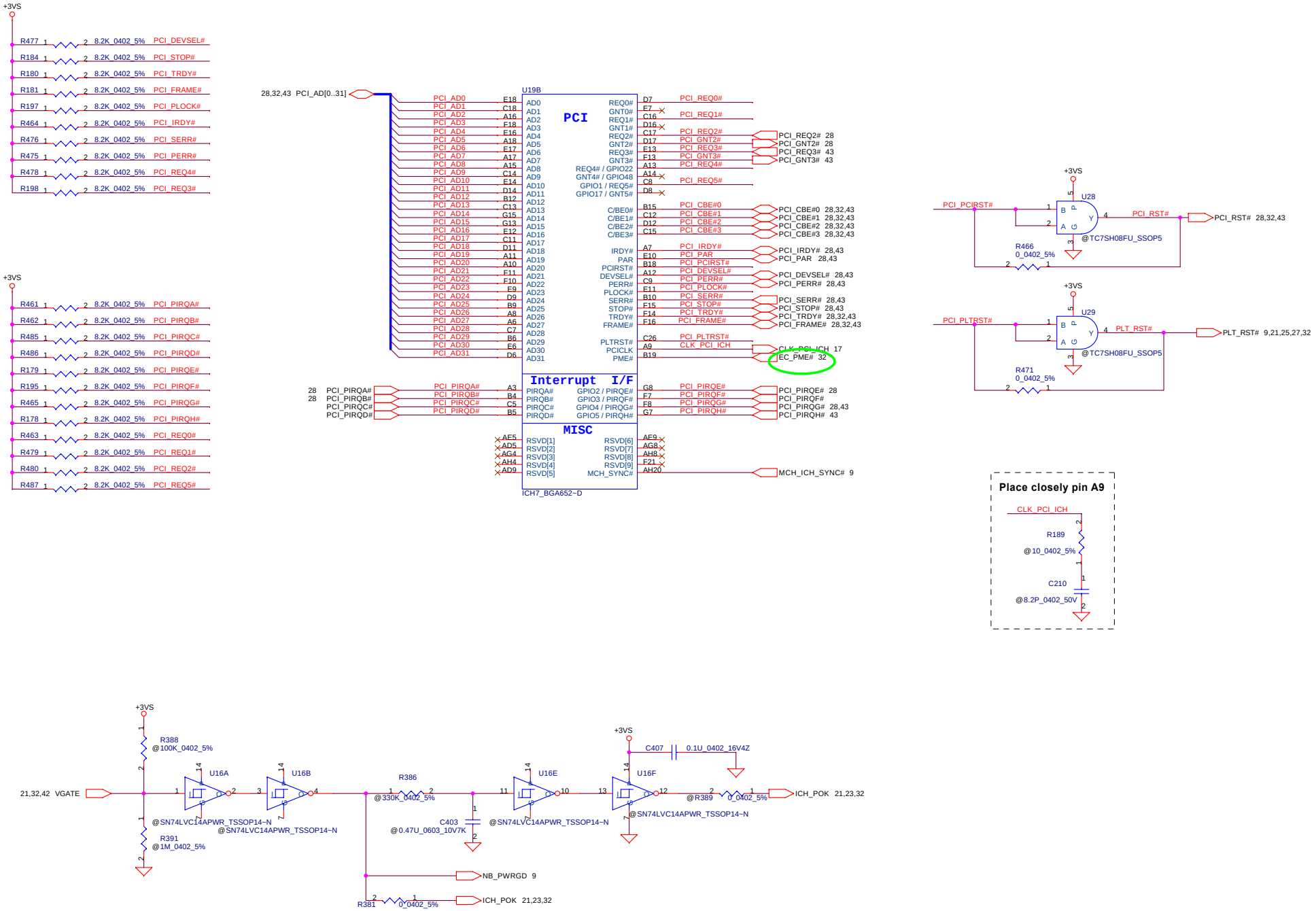

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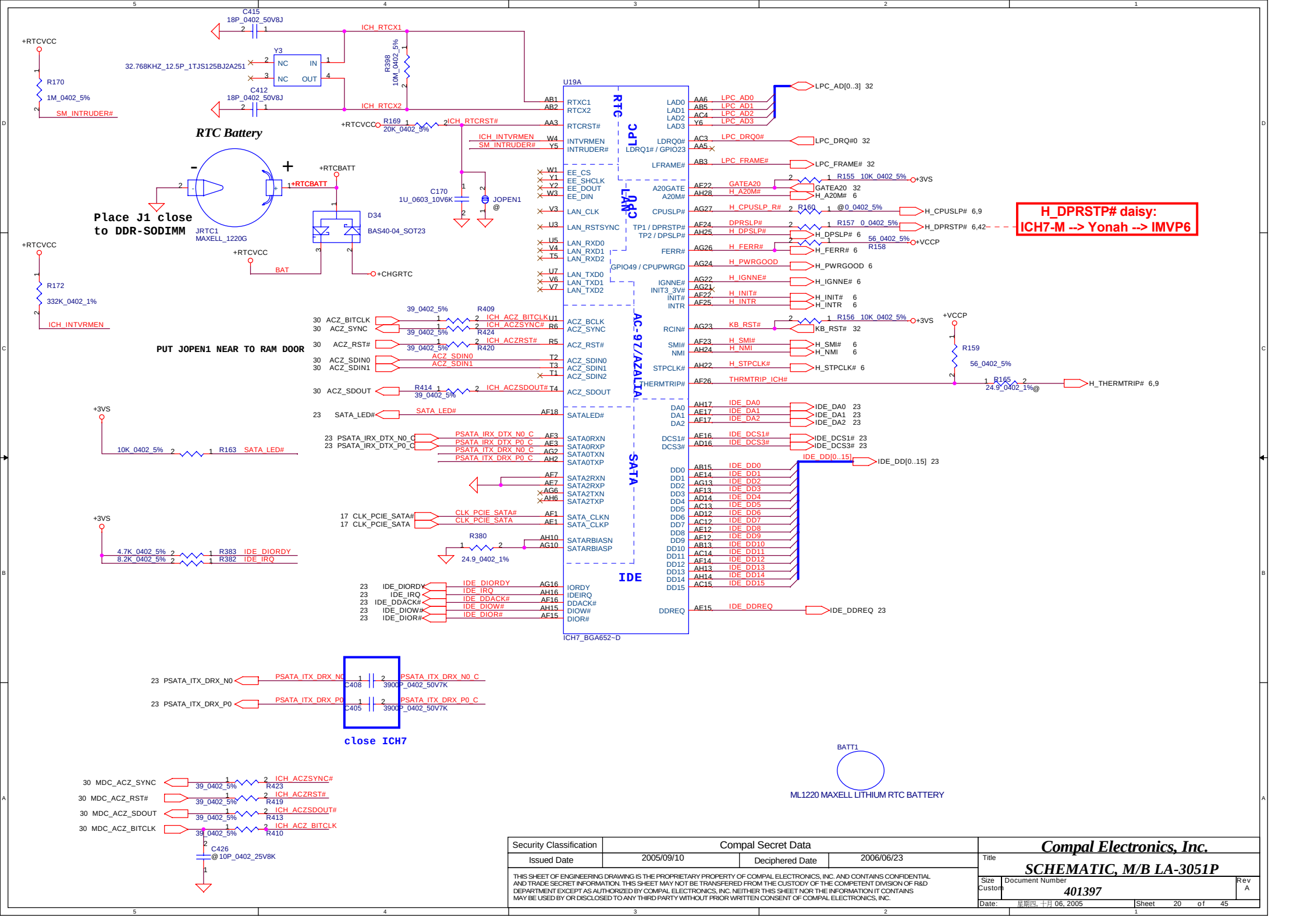
RTC Battery
Place J1 close to DDR-SODIMM
PUT JOPEN1 NEAR TO RAM DOOR
close ICH7
H_DPRSTP# daisy:
ICH7-M --> Yonah --> IMVP6
ML1220 MAXELL LITHIUM RTC BATTERY
ICH7_BGA652~D
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Compal Secret Data
Issued Date
2005/09/10
Deciphered Date
2006/06/23
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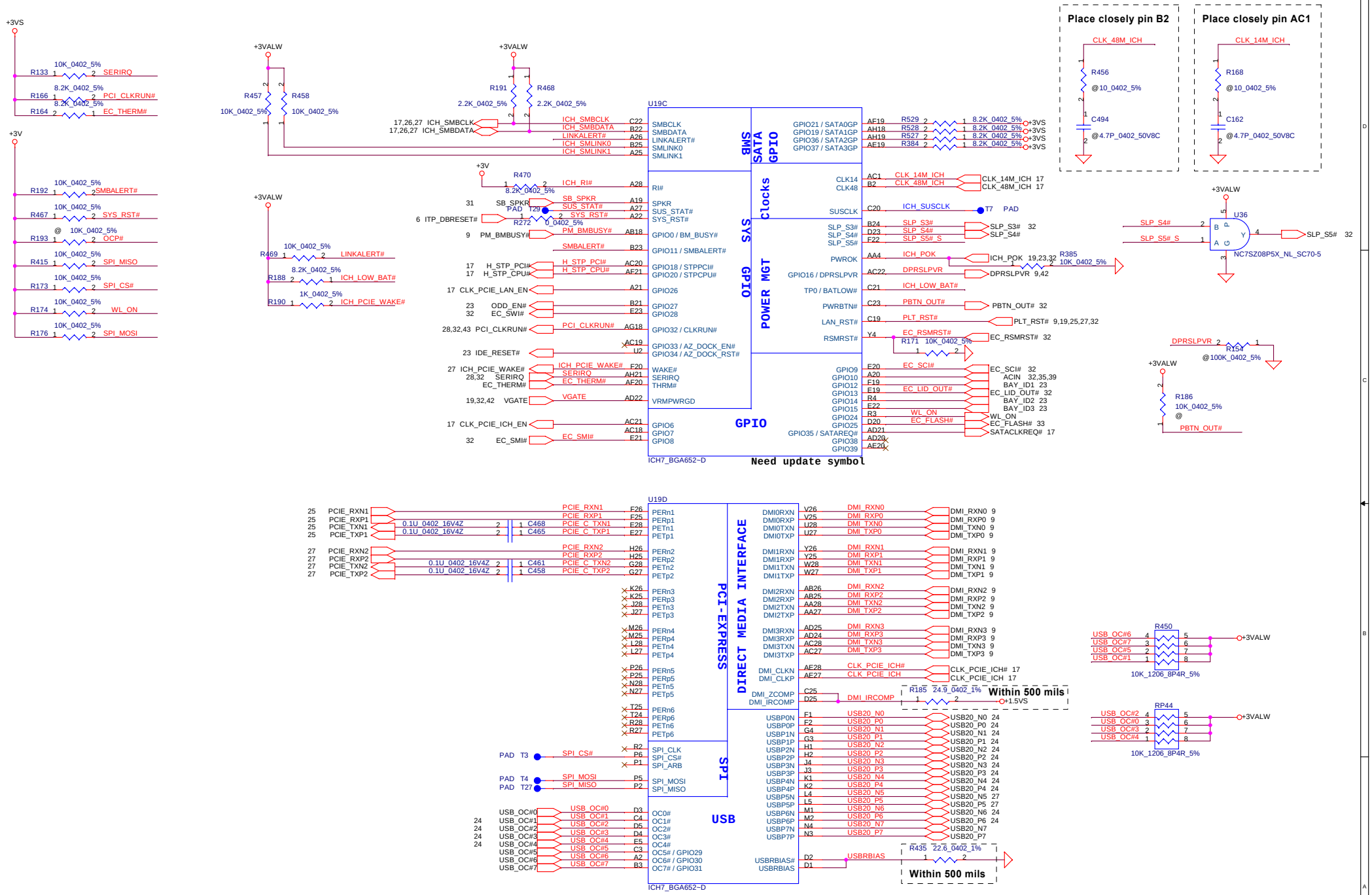

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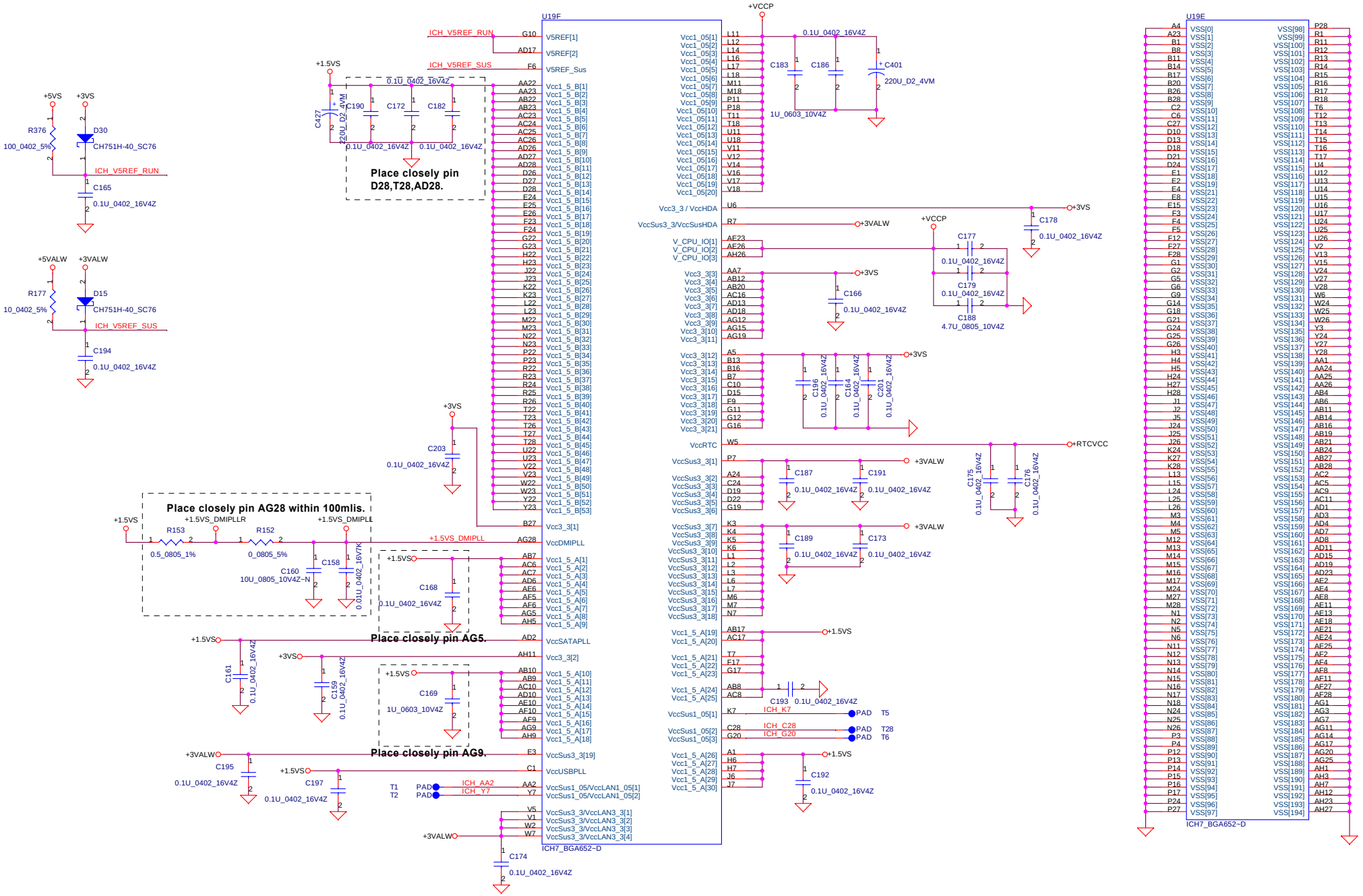

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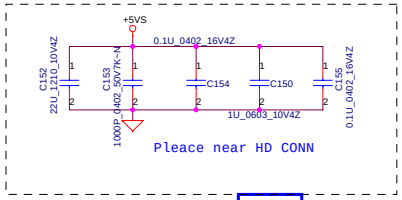
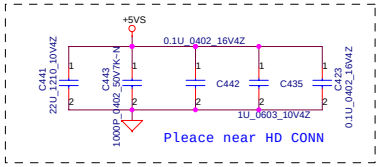
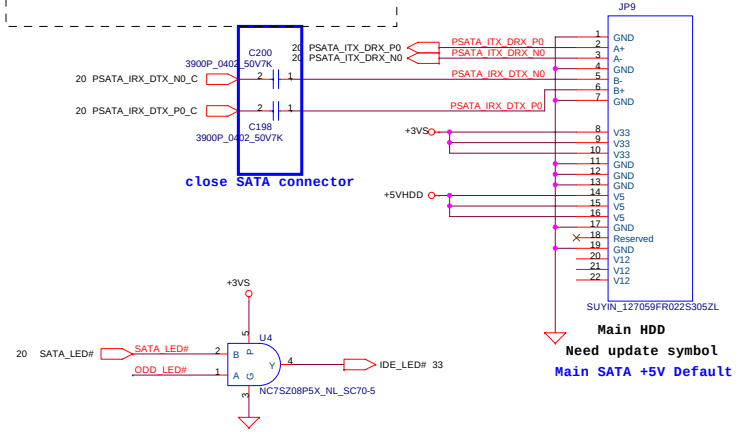
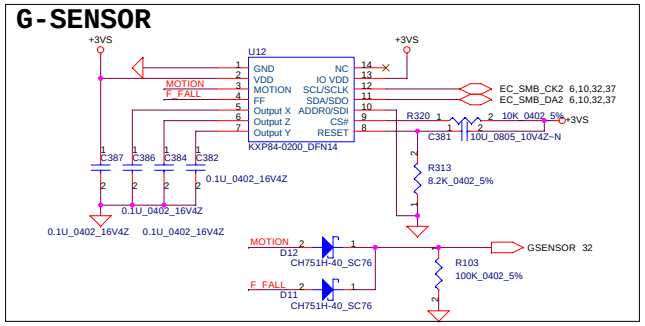
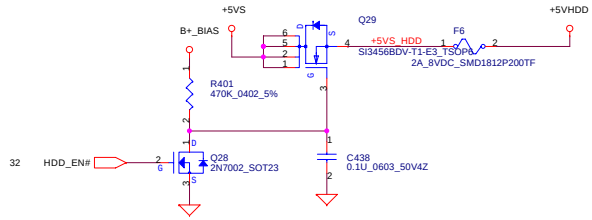
HDD CONNECTOR

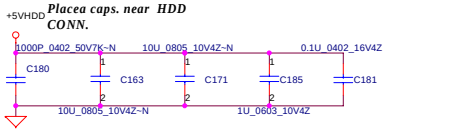


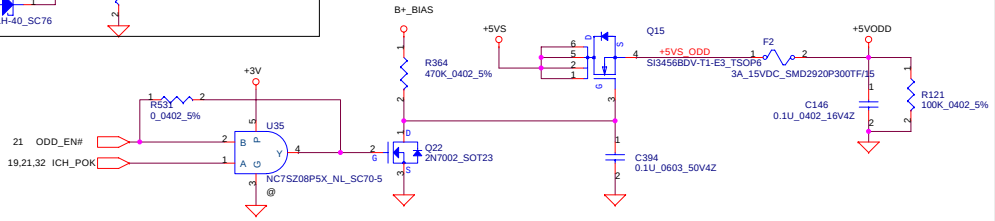


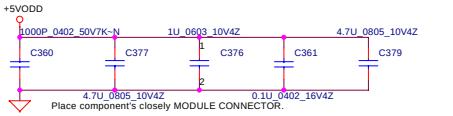


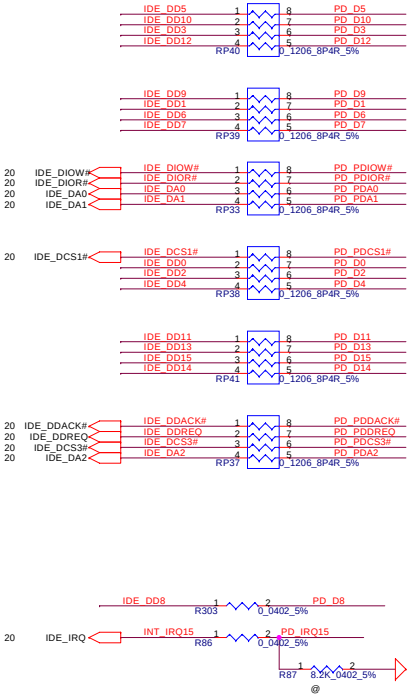


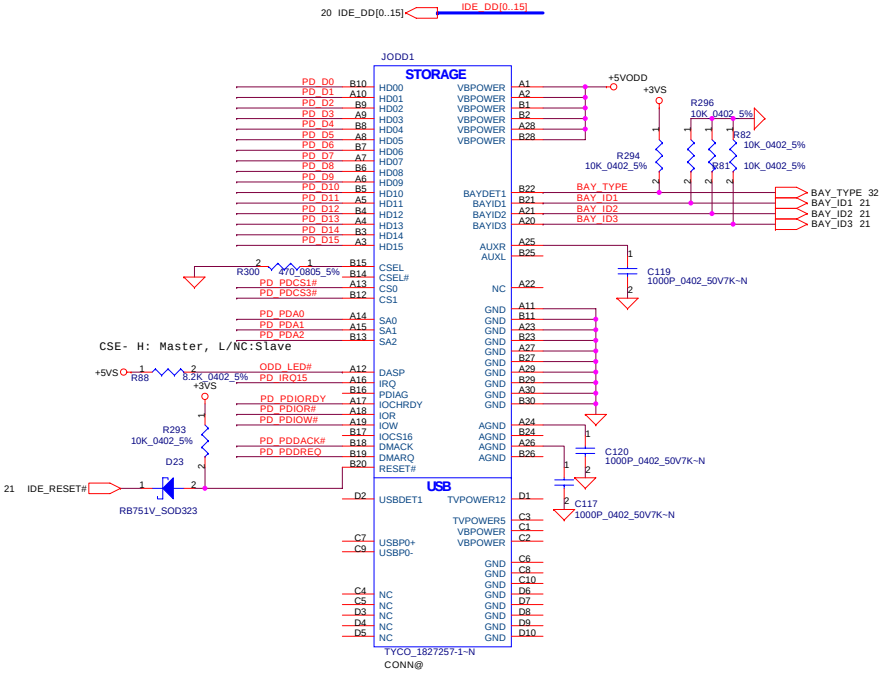


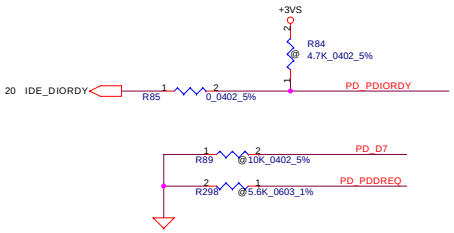












BAY TYPE- 0:Storage Device
1:2nd BATT or No pack

MODE	BAY_ID3/2/1	
Not Used	000	
CD-ROM	001	IDE
CD-RW	010	IDE
Combo	011	IDE
DVD-ROM	100	IDE
DVD-RAM	101	IDE
2nd HDD	110	IDE
Reserved	111	IDE

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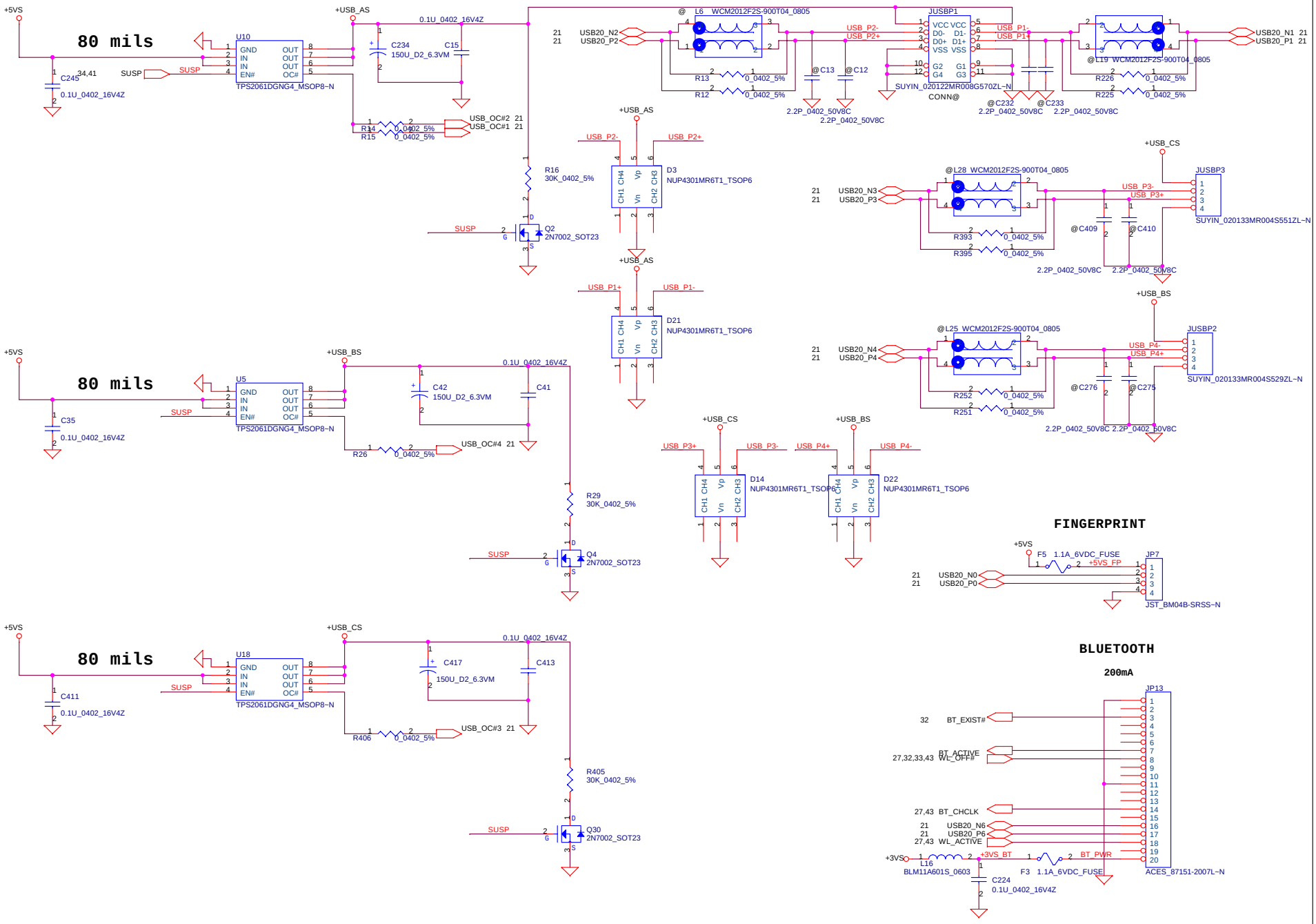

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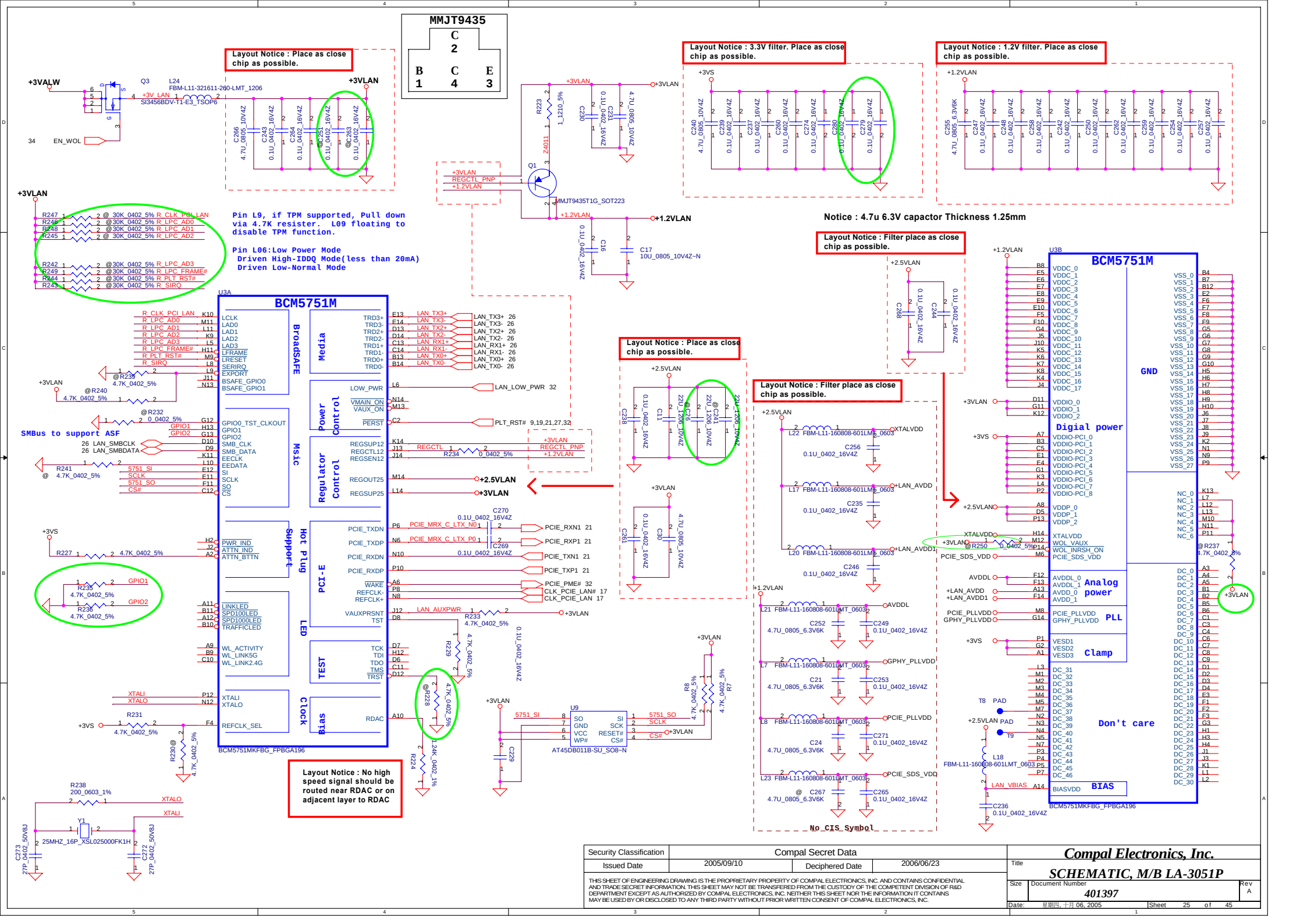
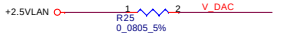
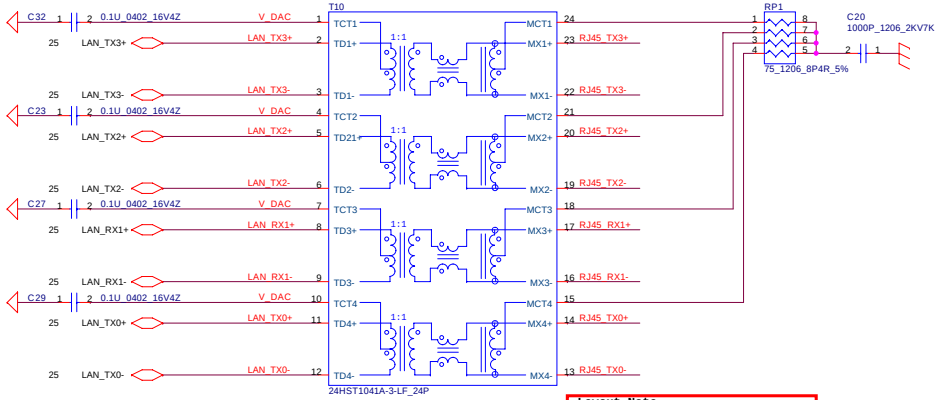
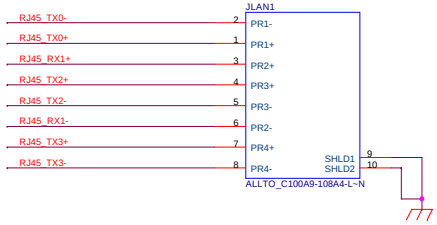
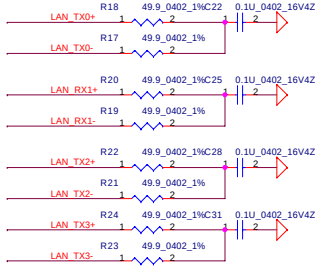




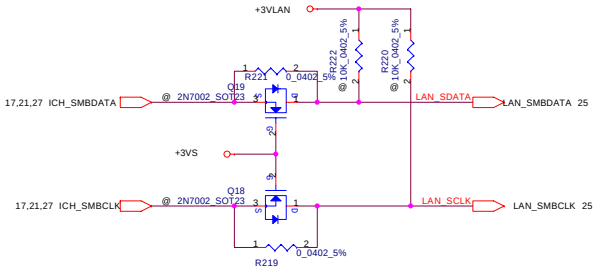


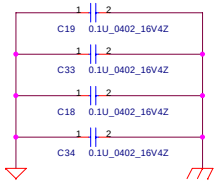
Layout Note
24HST1041A-3 pls close to conn.





All 49.9 ohm + 0.1 uF termination components close to BCM5751M





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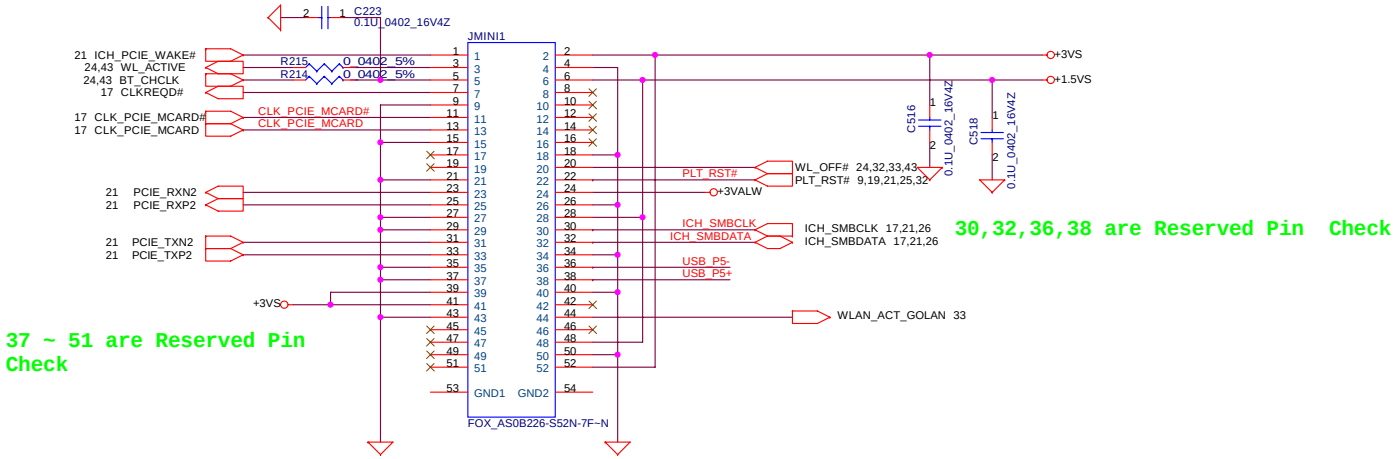

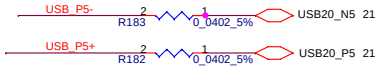

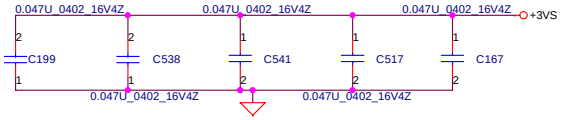

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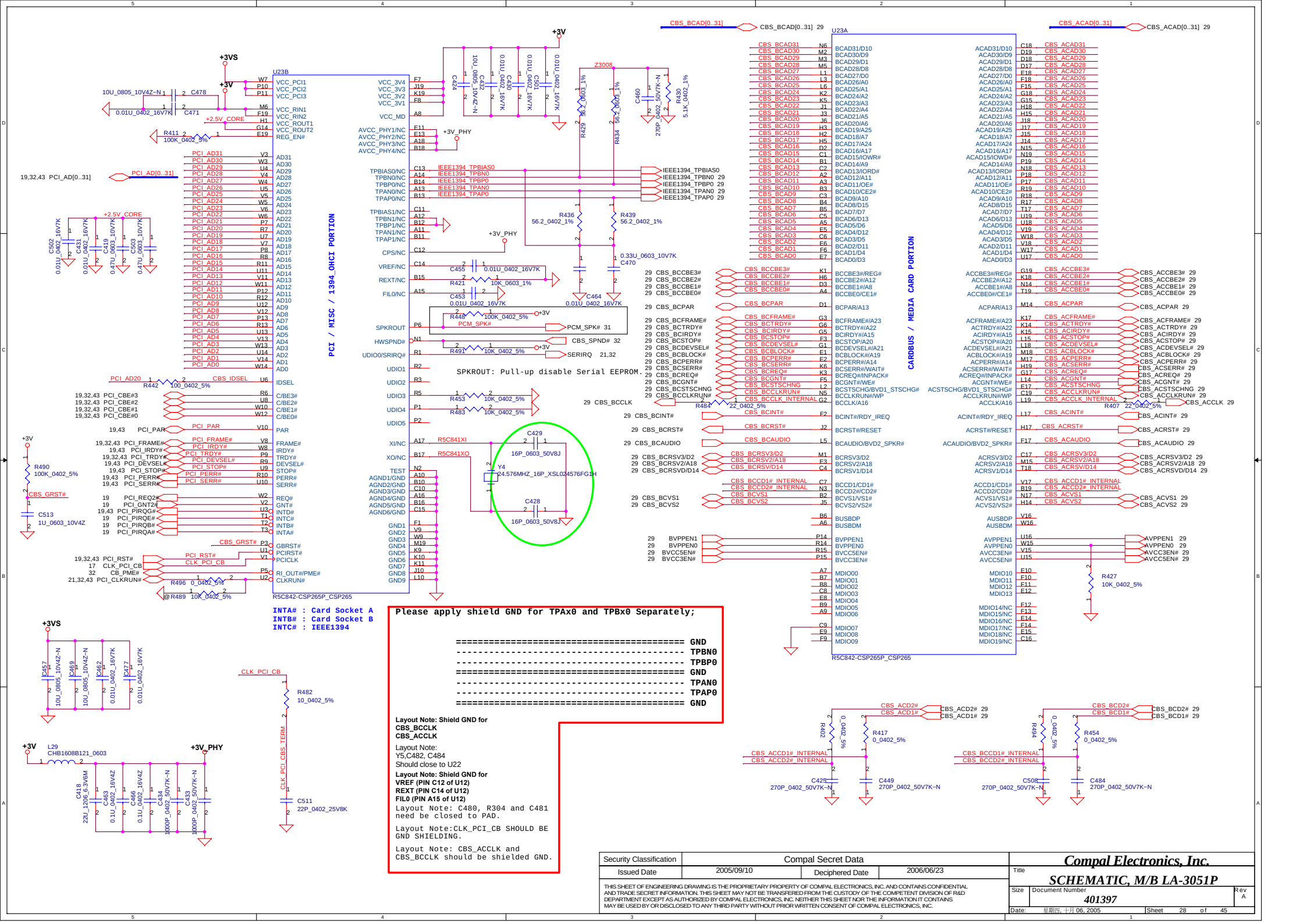

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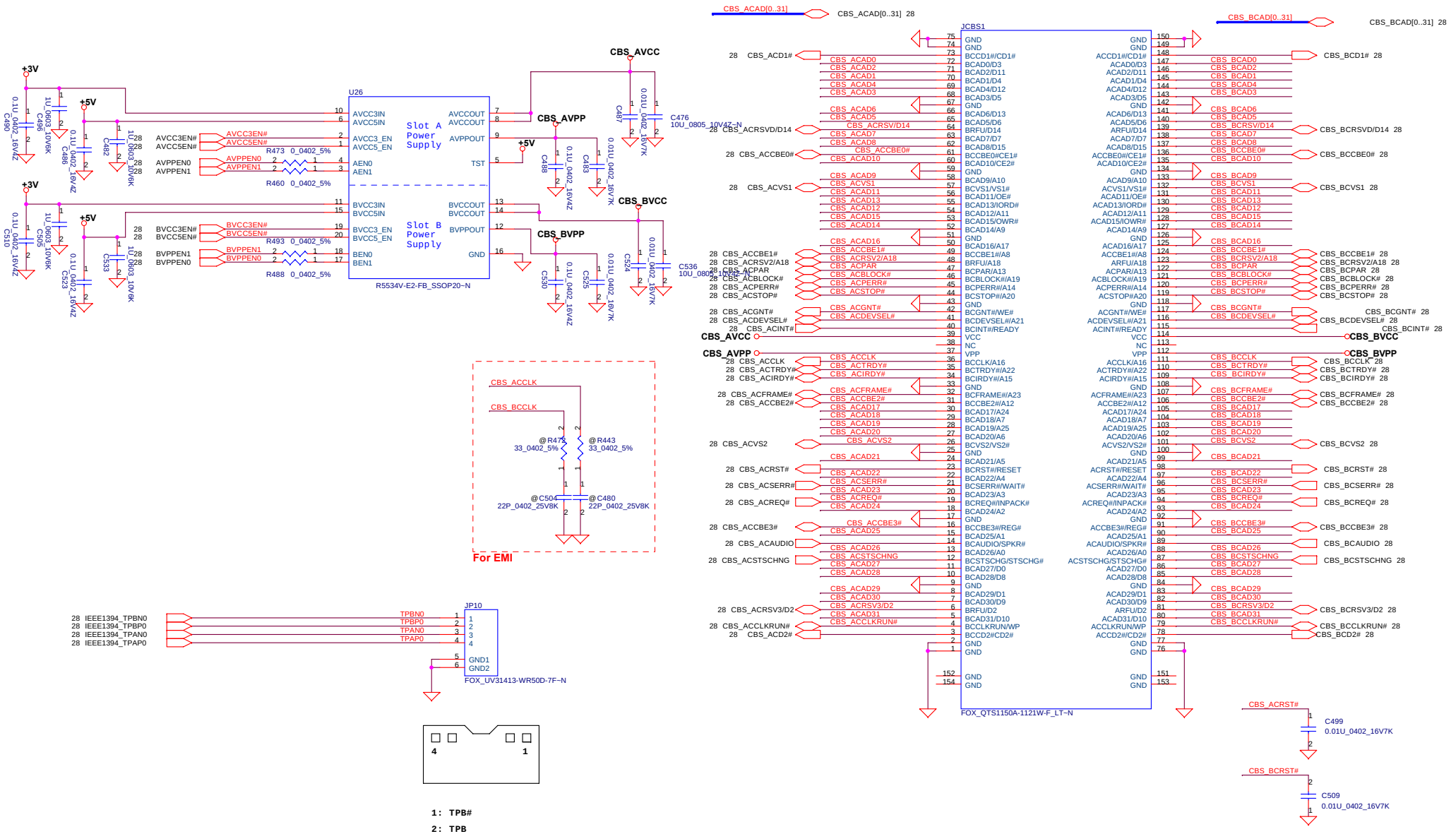

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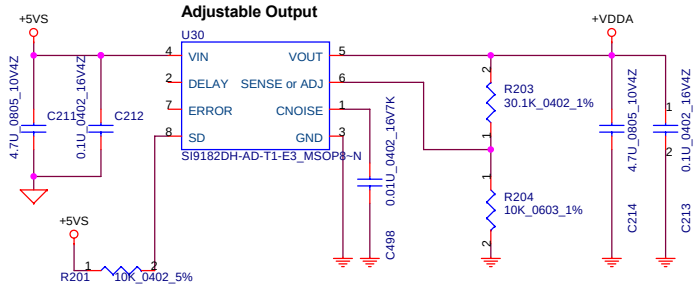
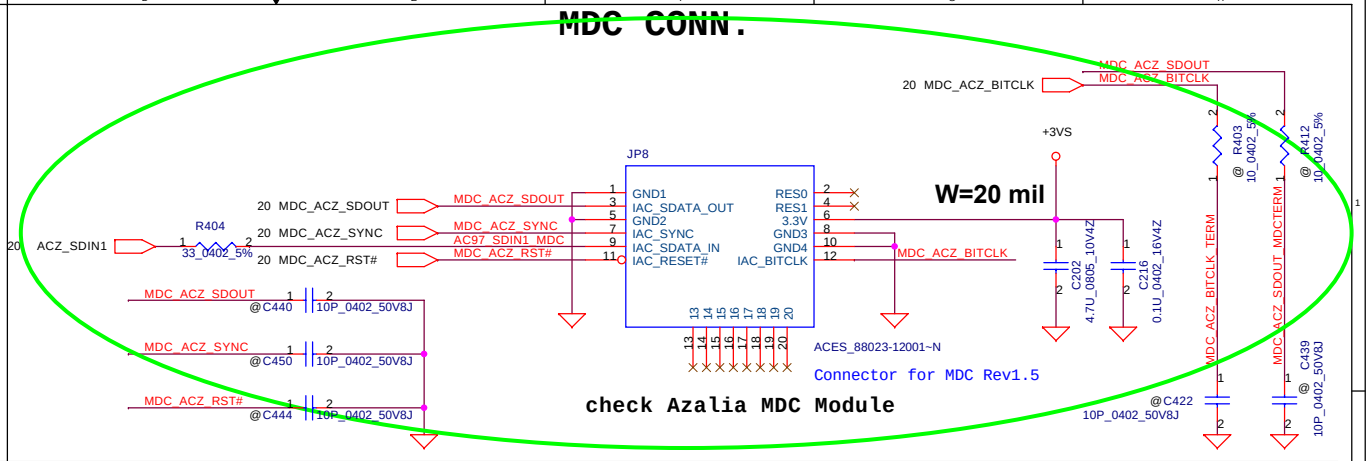
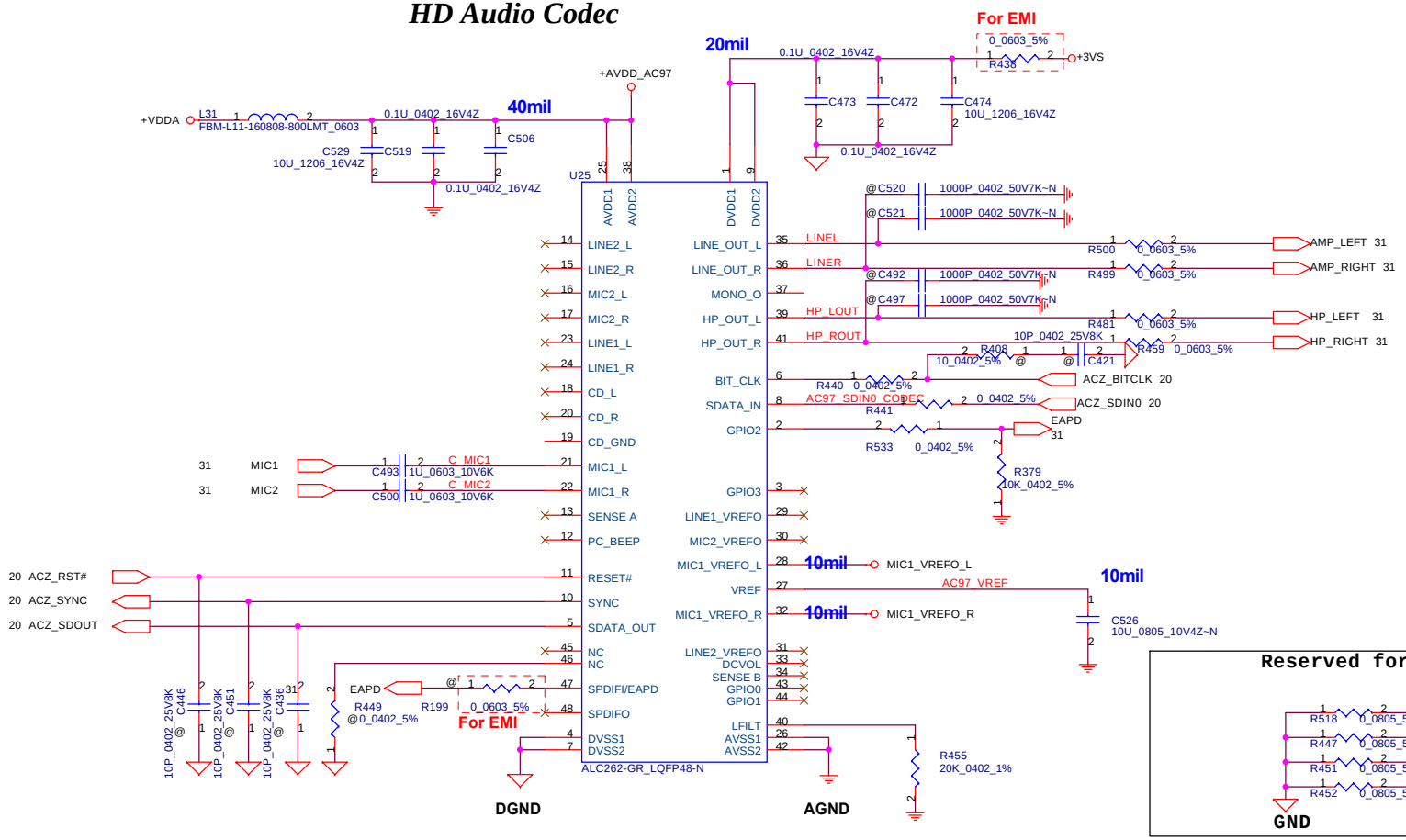




HD Audio Codec



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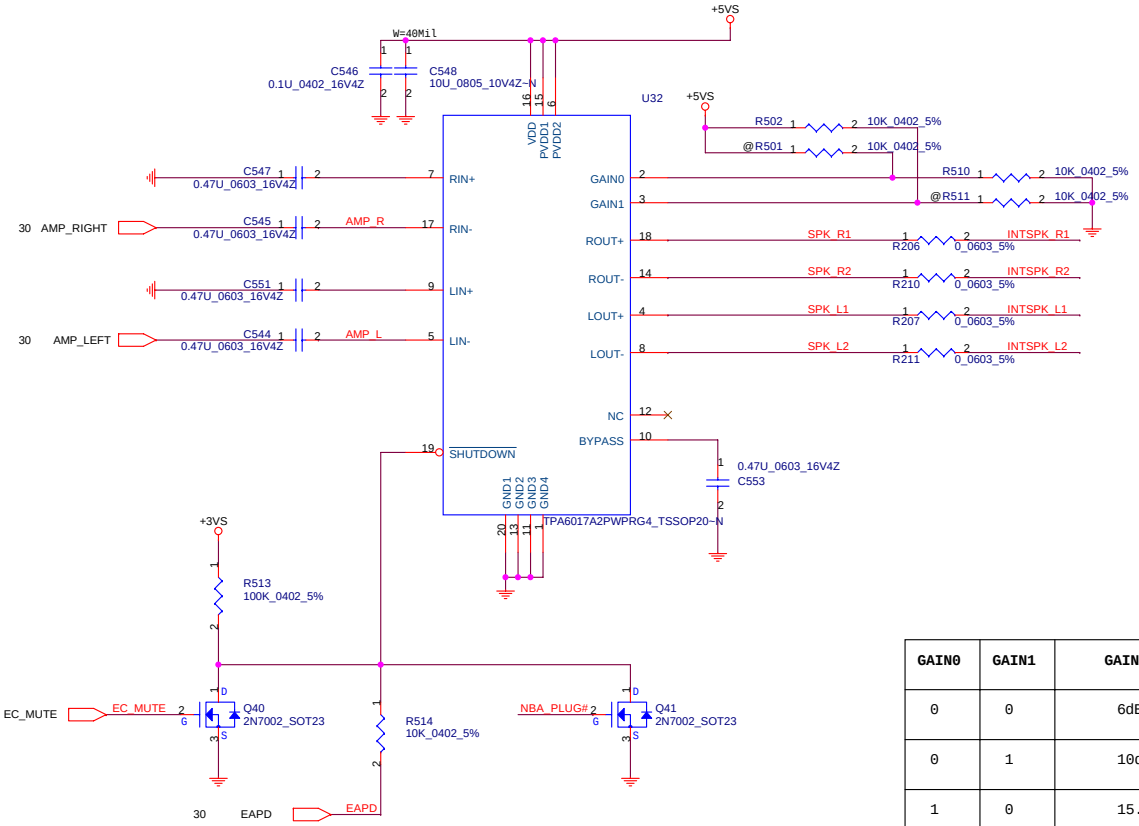
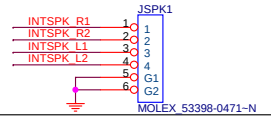


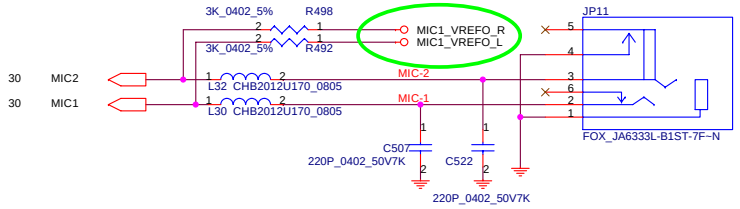
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off

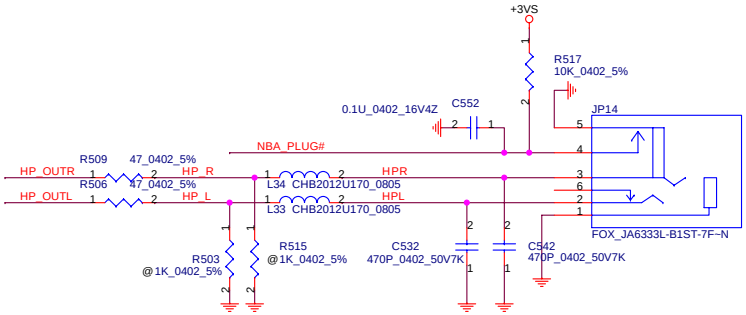
Speaker Connector

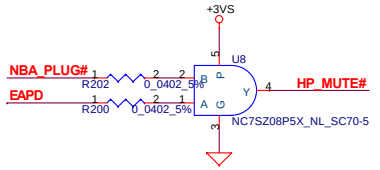


MICROPHONE IN JACK



HEADPHONE OUT JACK



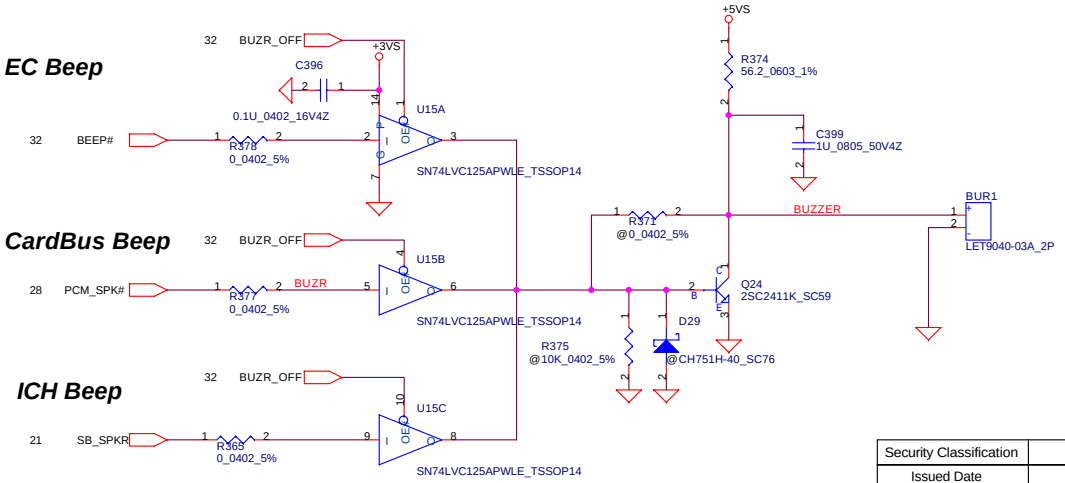


Reserve the 0 ohm resistor.
for voltage filtering

EC Beep

CardBus Beep

ICH Beep



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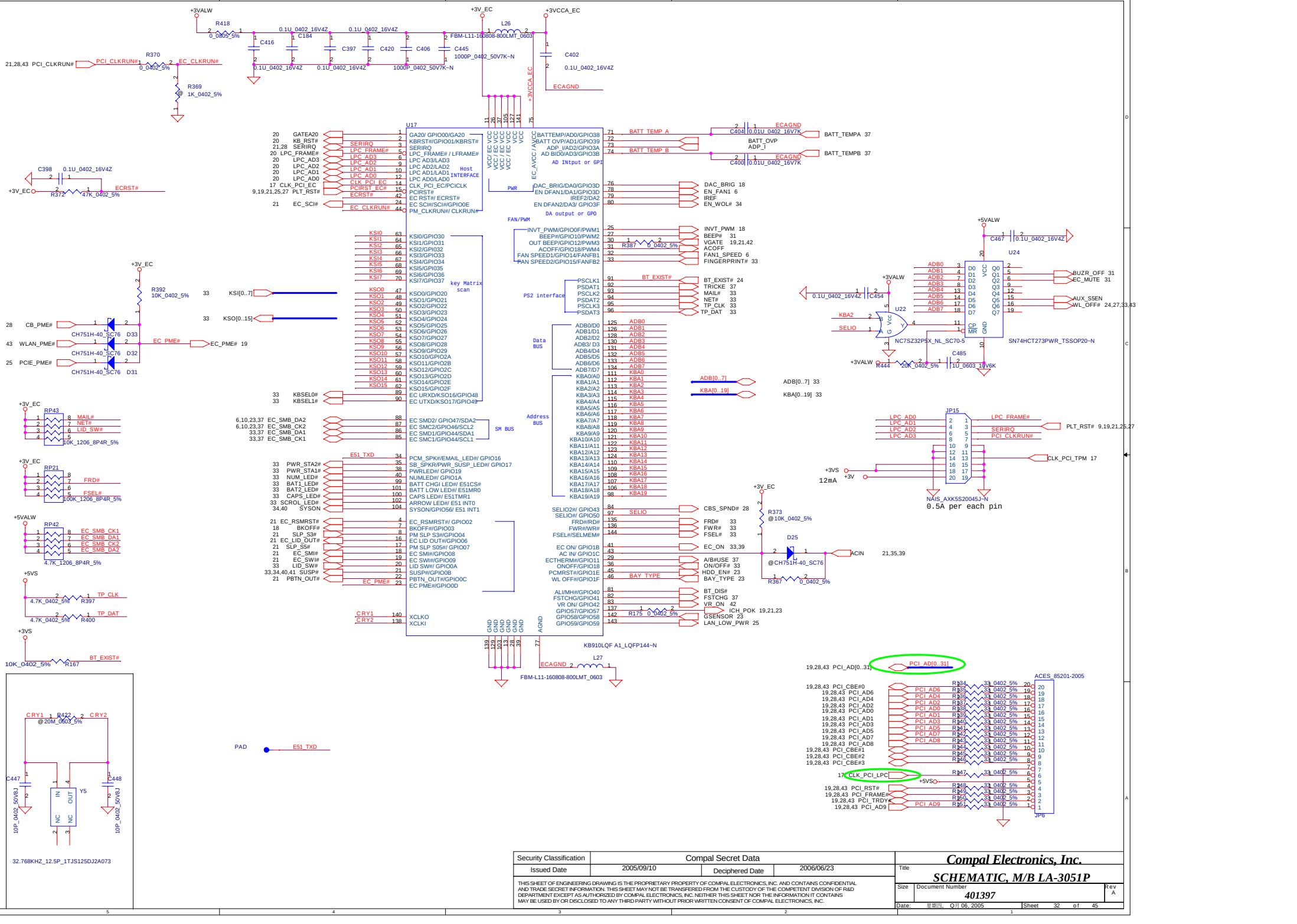
U17
KB910LQF A1_LQFP144-N
U24
SN74HCT273PWR_TSSOP20-N
JP15
NAIS_AXK5S20045J-N
0.5A per each pin
ACES_85201-2005
JP6
Y5
32.768KHZ_12.5P_1TJS125DJ2A073
PAD
E51_TXD
PCI_CLKRUN#
EC_CLKRUN#
EC_PME#
BT_EXIST#
TP_CLK
TP_DAT
SERIRQ
PLT_RST#
CLK_PCI_TPM
PCI_AD[0..31]
CLK_PCI_LPC
BATT_TEMP_A
BATT_TEMP_B
BATT_TEMPA
BATT_TEMPB
BATT_OVP
ADP_I
DAC_BRIG
EN_FAN1
IREF
EN_WOL#
INVT_PWM
BEEP#
ACOFF
FAN1_SPEED
FINGERPRINT#
BUZR_OFF
EC_MUTE
AUX_S5EN
WL_OFF#
ADB[0..7]
KBA[0..19]
KSI[0..7]
KSO[0..15]
CBS_SPND#
FRD#
FWR#
FSEL#
EC_ON
ACIN
BAY_TYPE
ICH_POK
GSENSOR
LAN_LOW_PWR
VR_ON
FSTCHG
BT_DIS#
EC_SMB_CK1
EC_SMB_DA1
EC_SMB_CK2
EC_SMB_DA2
MAIL#
LID_SW#
CB_PME#
WLAN_PME#
PCIE_PME#
EC_PME#
ECRST#
PCIRST_EC#
CLK_PCI_EC
SERIRQ
KBSEL0#
KBSEL1#
PWR_STA2#
PWR_STA1#
NUM_LED#
BAT1_LED#
BAT2_LED#
CAPS_LED#
SCROL_LED#
SYSON
BKOFF#
SLP_S3#
EC_LID_OUT#
SLP_S5#
EC_SMI#
EC_SWI#
LID_SW#
SUSP#
PBTN_OUT#
+3VALW
+3V_EC
+3VCCA_EC
+5VALW
+5VS
+3VS
ECAGND
AGND
GND
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2006/06/23
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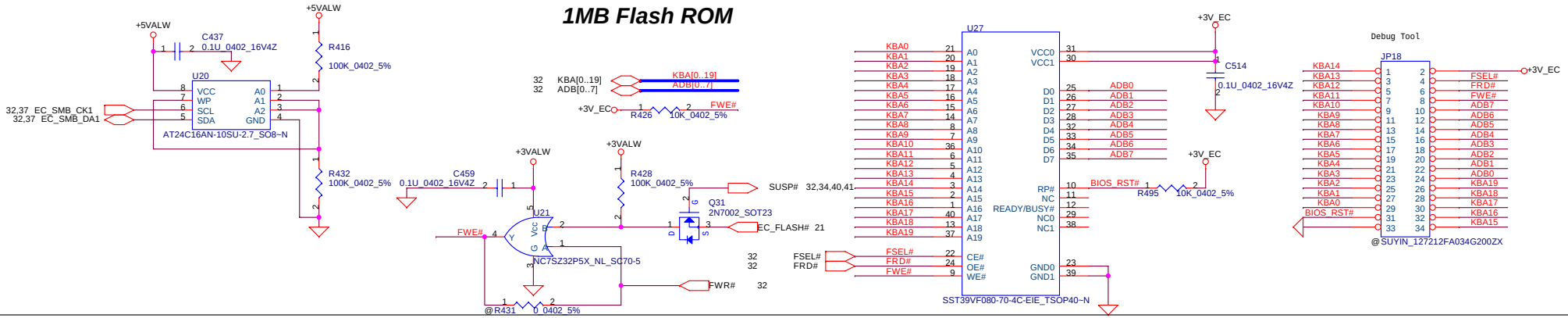
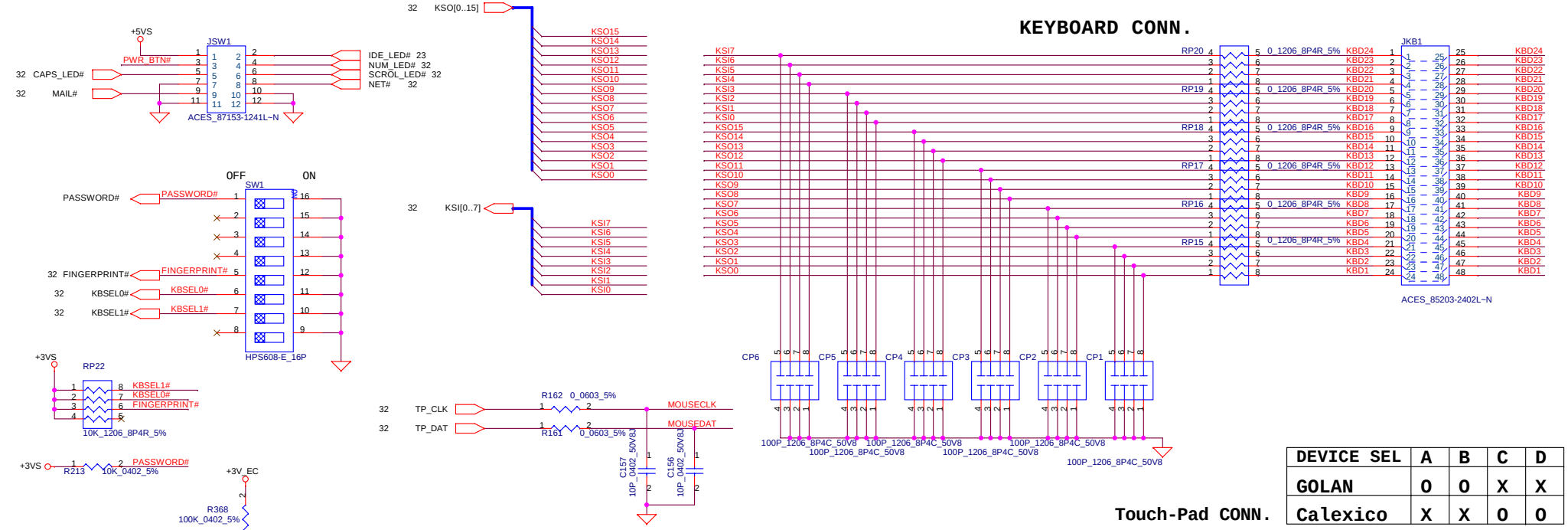
1MB Flash ROM

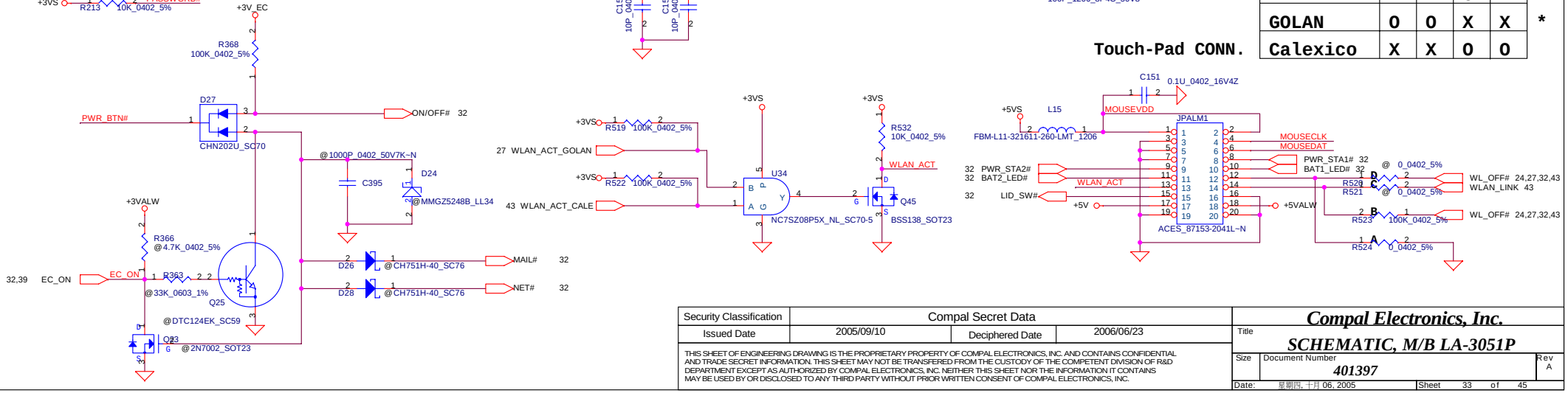


KEYBOARD CONN.



DEVICE SEL	A	B	C	D	
GOLAN	0	0	X	X	*
Calexico	X	X	0	0	

Touch-Pad CONN.



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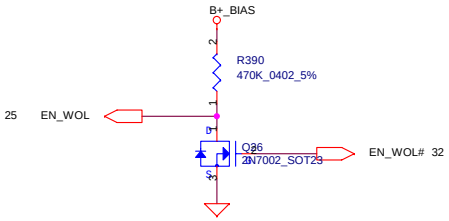

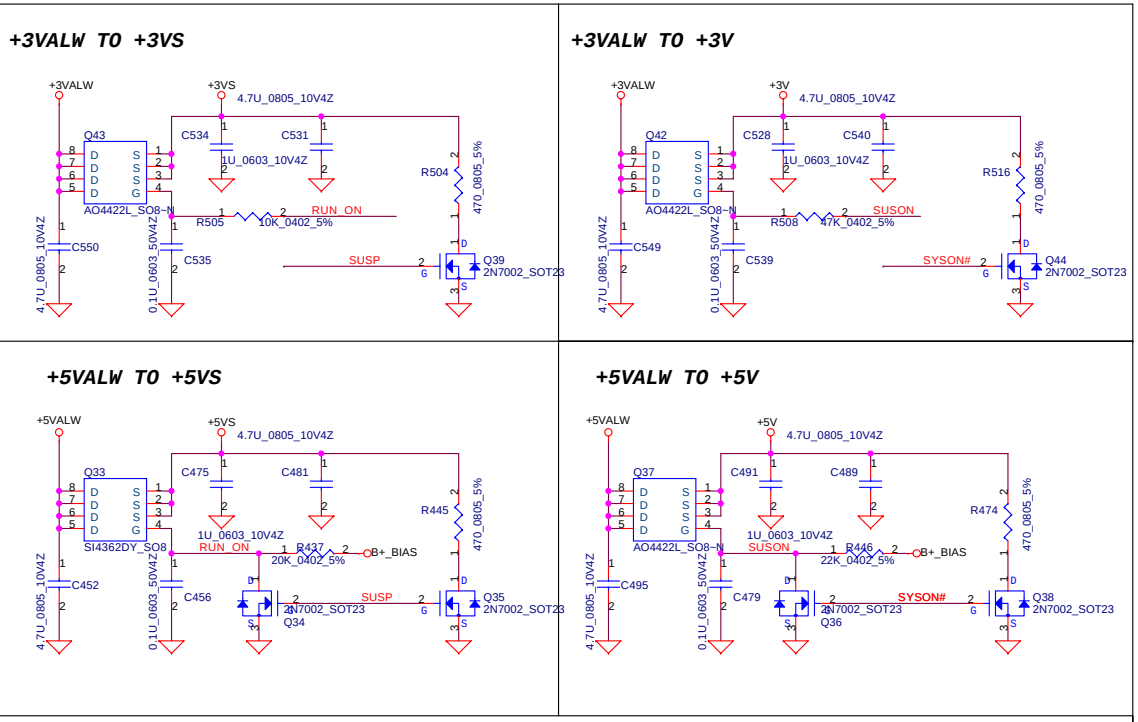

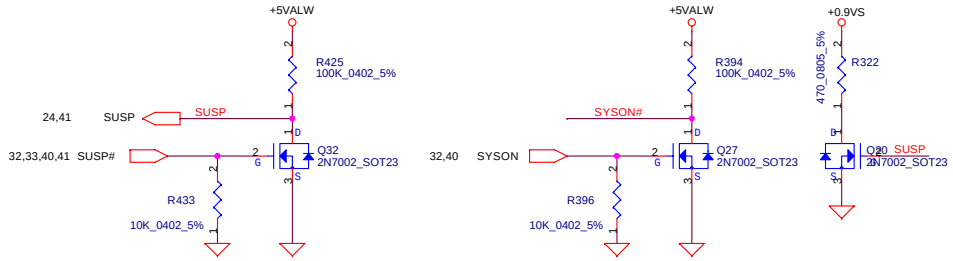

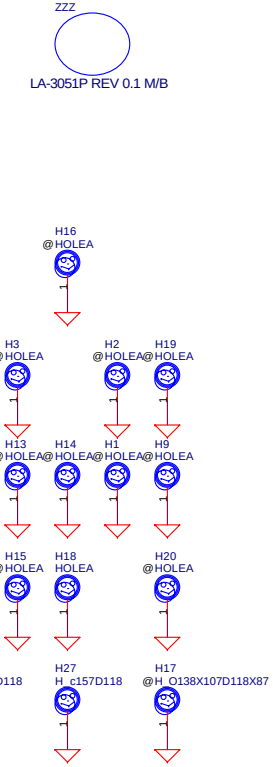

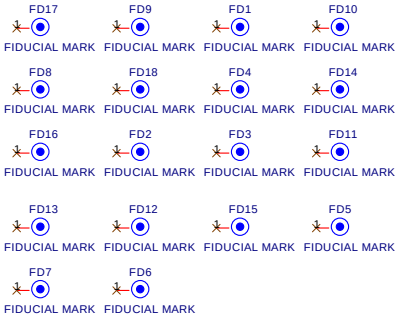

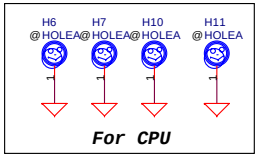

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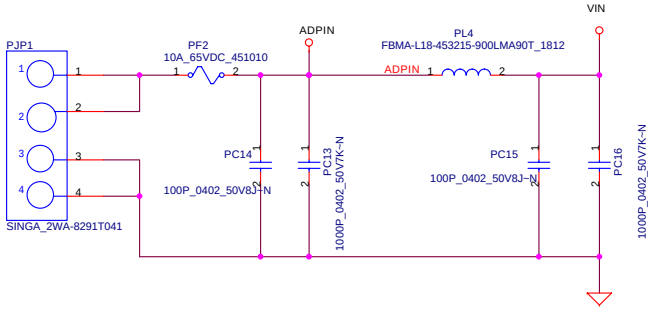
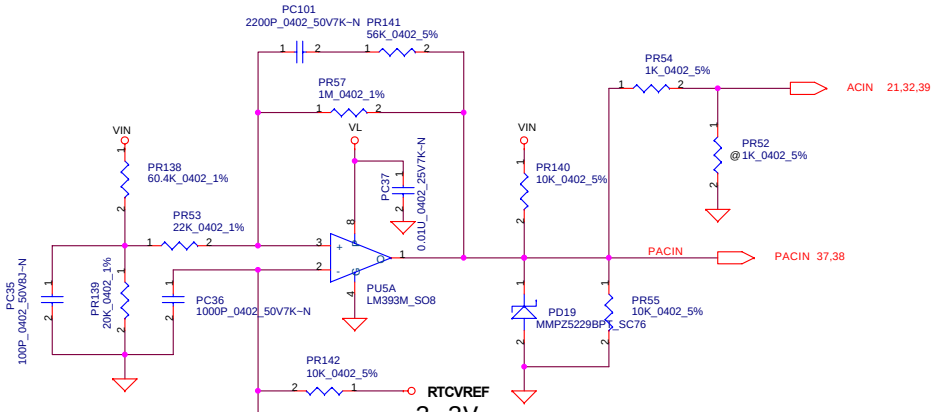
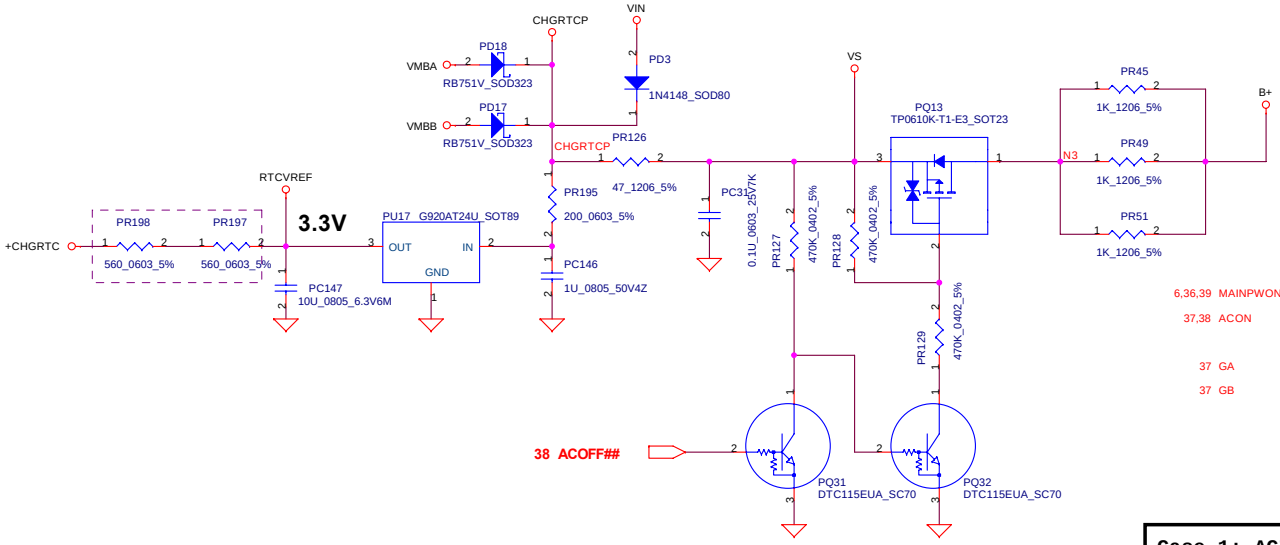
Detector

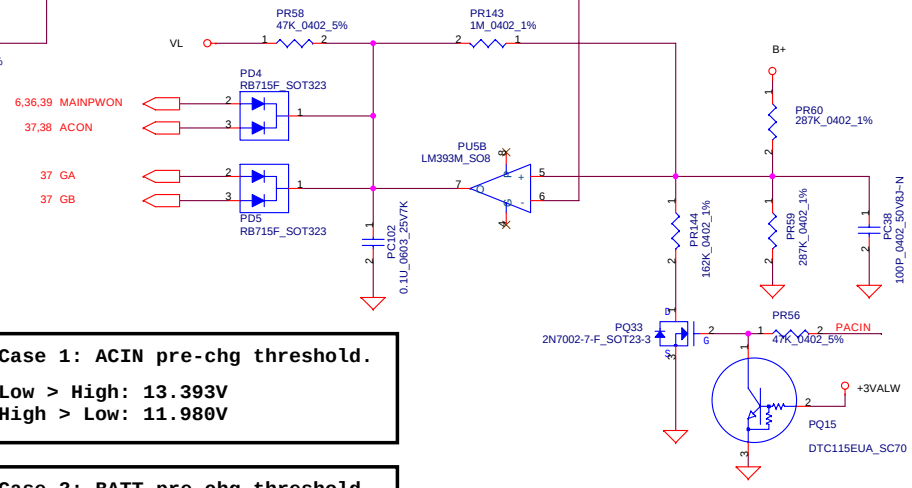
Vin Detector Threshold:

Low > High: 13.757V
High > Low: 13.160V







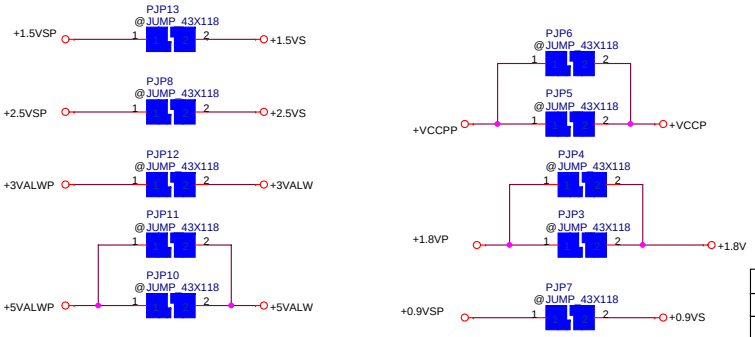


Case 1: ACIN pre-chg threshold.

Low > High: 13.393V
High > Low: 11.980V

Case 2: BATT pre-chg threshold.

Low > High: 7.547V
High > Low: 6.134V



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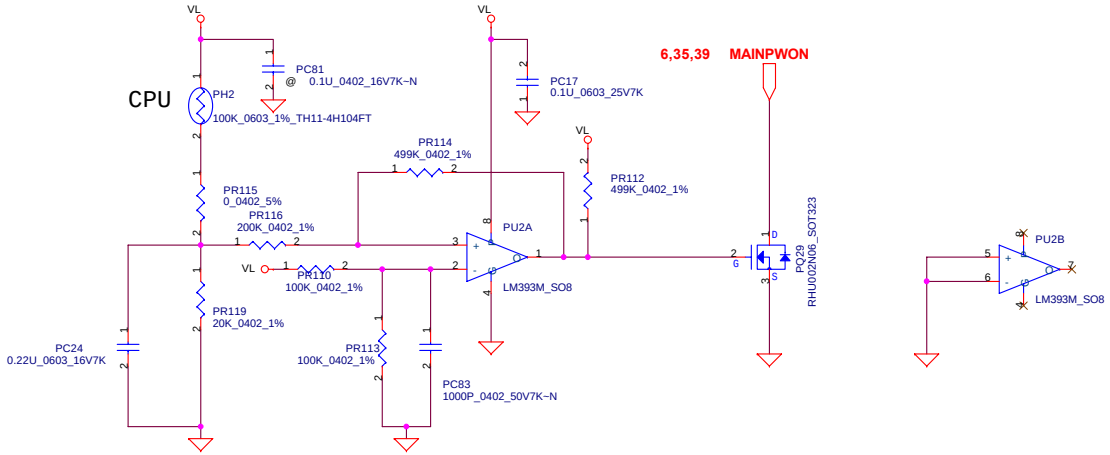
PH1 under CPU botten side :
CPU thermal protection at 86 +-3 degree C
Recovery at 51 +-3 degree C



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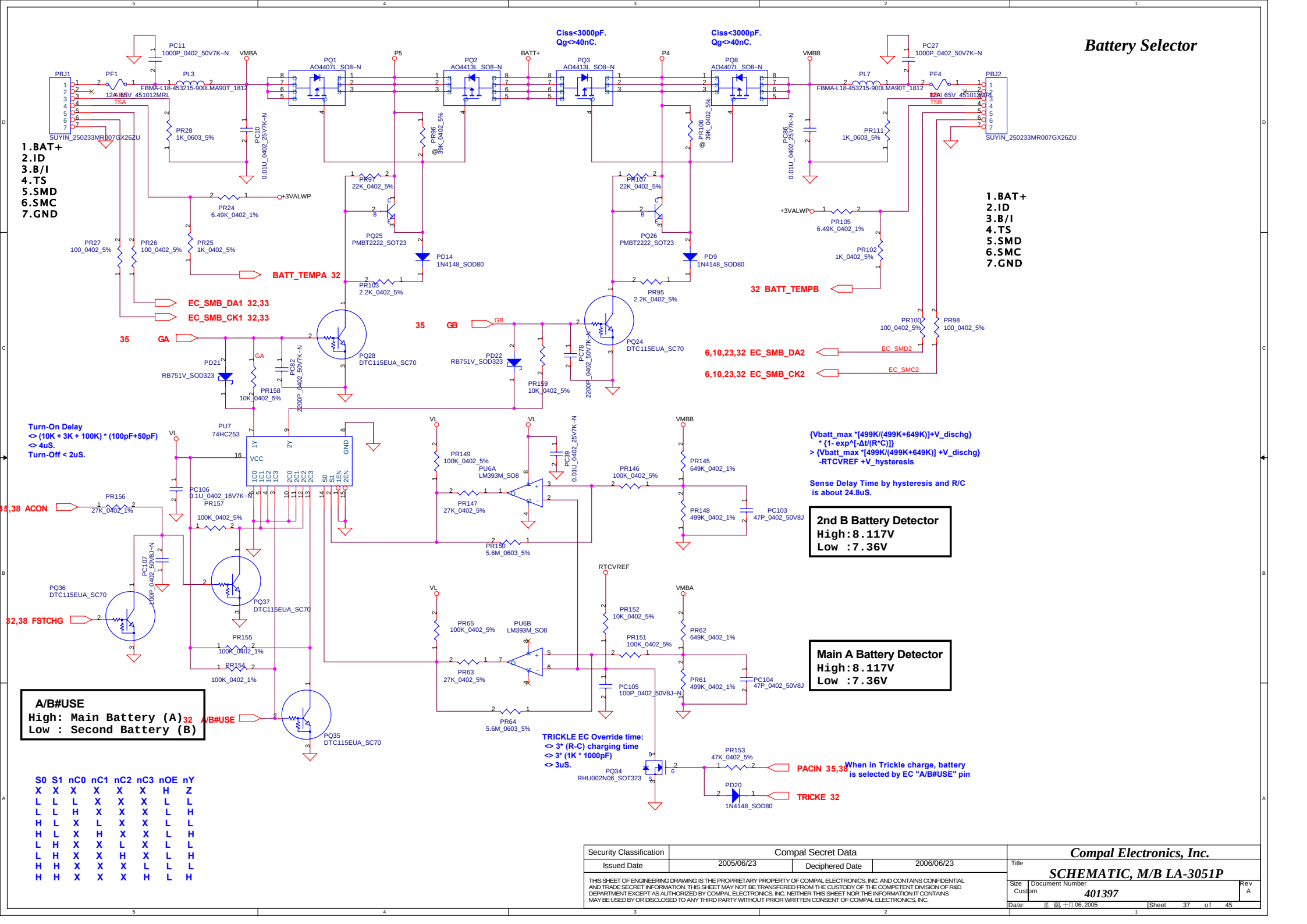
Battery Selector



S0	S1	nC0	nC1	nC2	nC3	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

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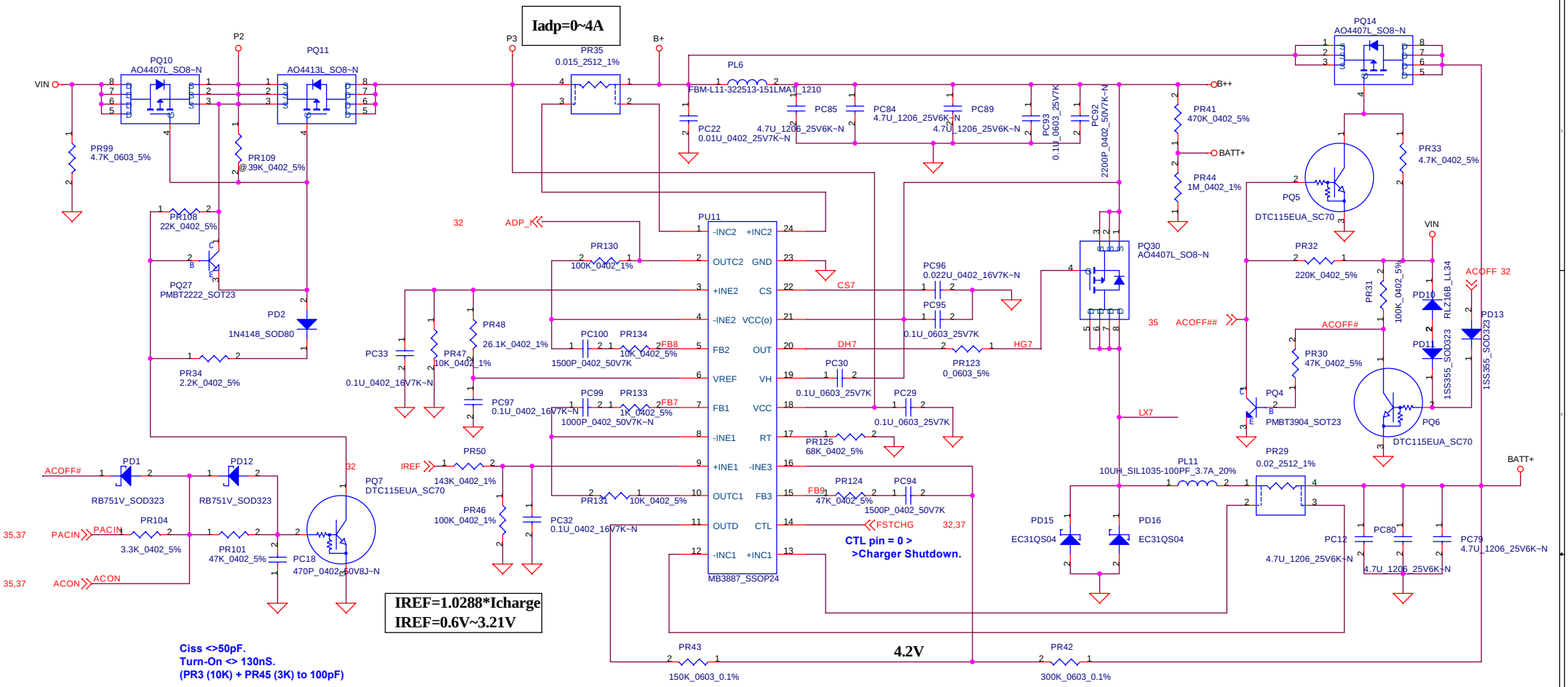

Vadp=15V

I limit: 4.61A

OVP voltage : LI
3S2P : 13.5V--> BATT_OVP= 1.5V
(BAT_OVP=0.1112 *BATT+)

D.A.C.A. (C.P.) on 75W adaptor: Take PR47= 10K
4.65A*0.015*20 = 5*PR47/(PR47+PR48)<> PR48<>26.1K

Fast charge current <> 3.3A,
3.3A*0.02*20/[(3.21V- 3.3A*0.02*20)/PR46] <> PR50
PR46 <> 143K

Trickle charge current <> 0.6A,
0.6A*0.02*20/[(0.6V- 0.6A*0.02*20)/PR46] <> PR50
PR46 <> 143K

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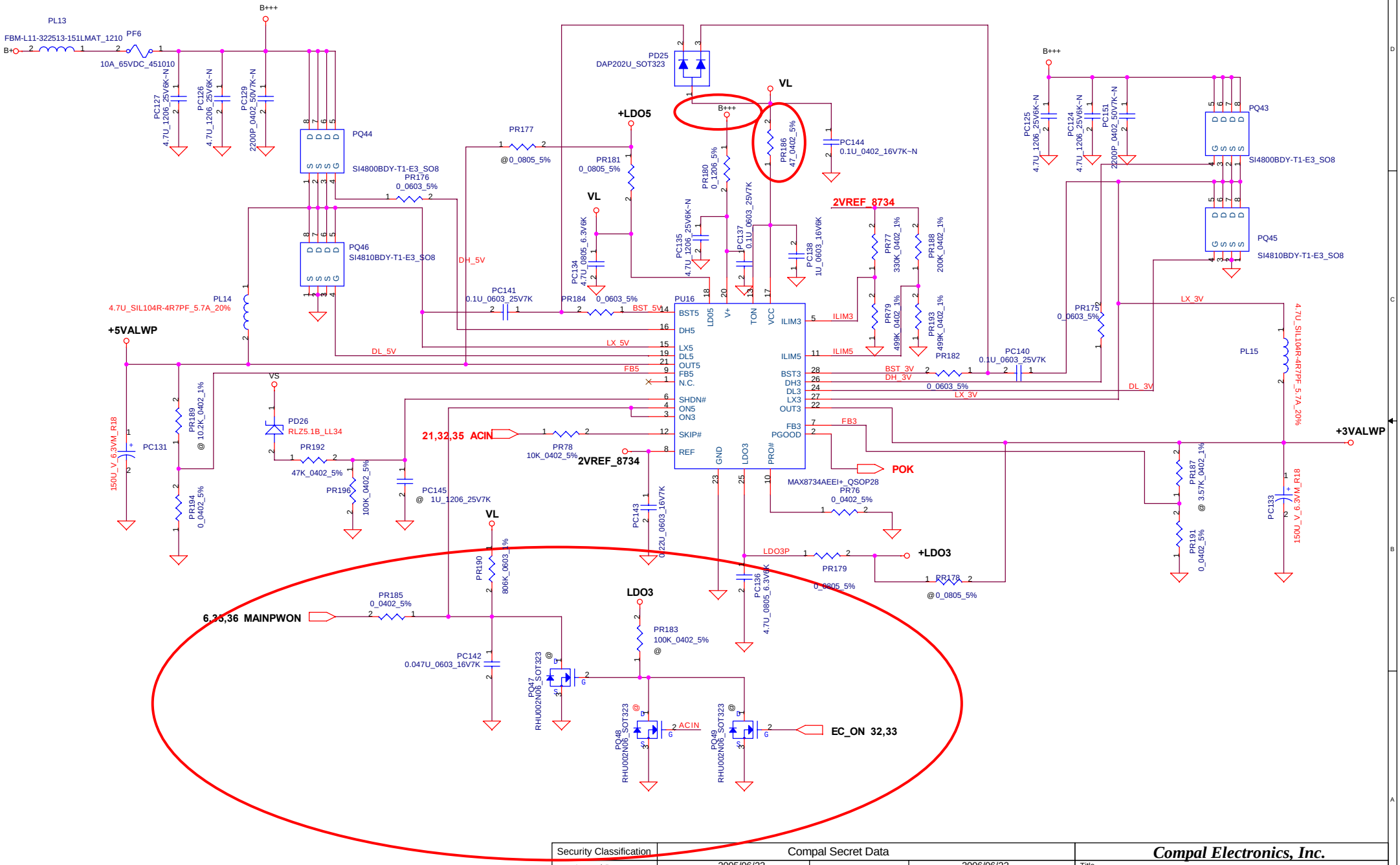
+3.3VALWP/+5VALWP



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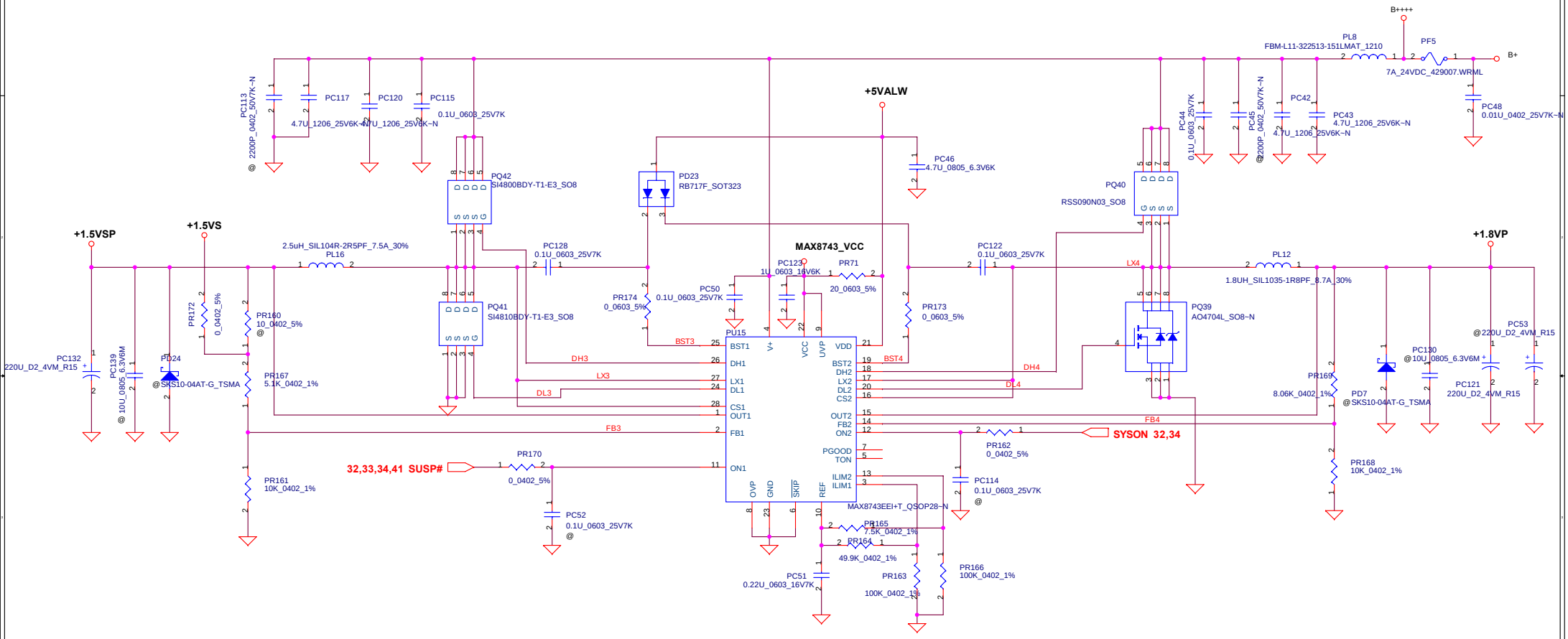

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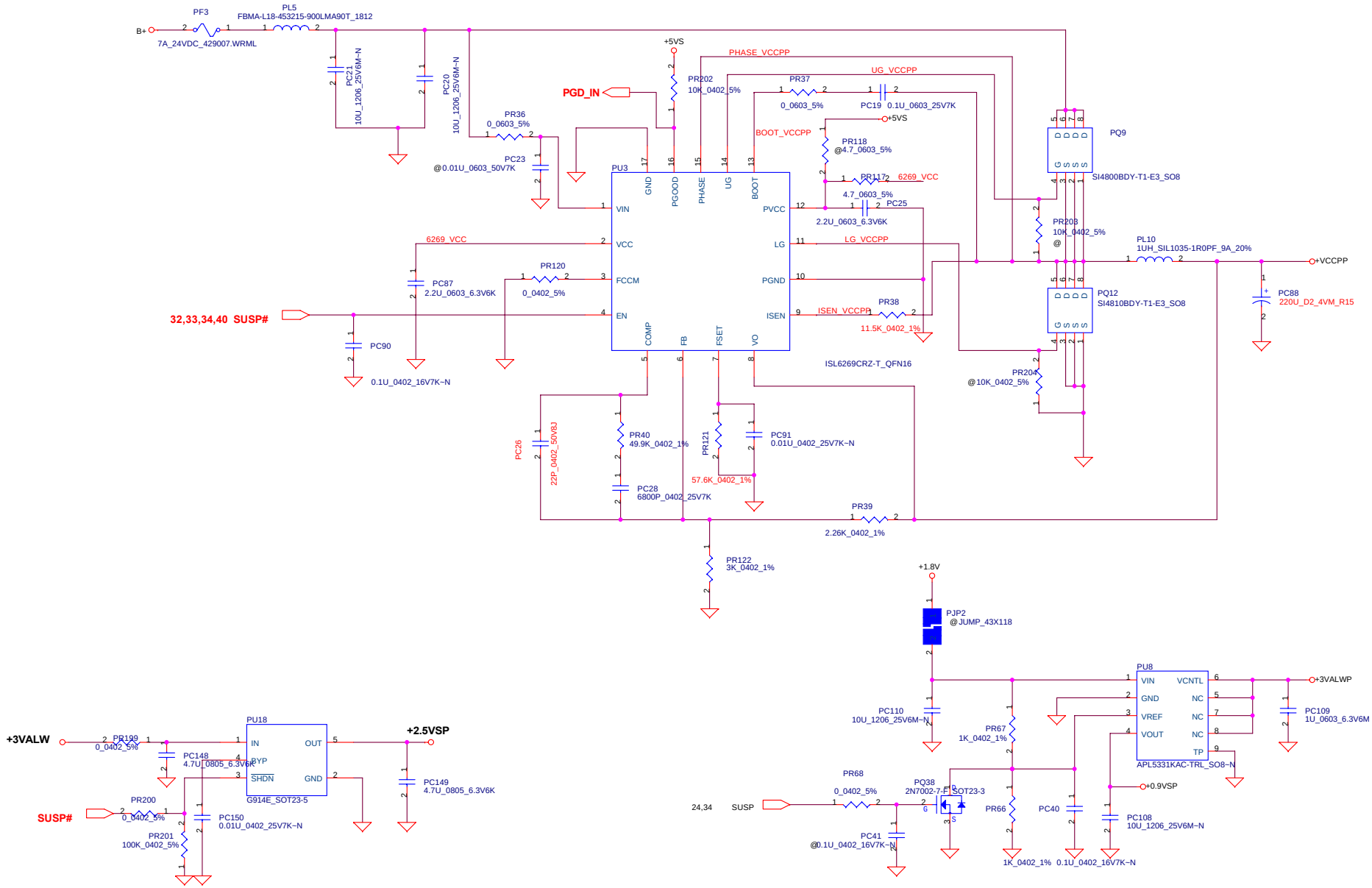

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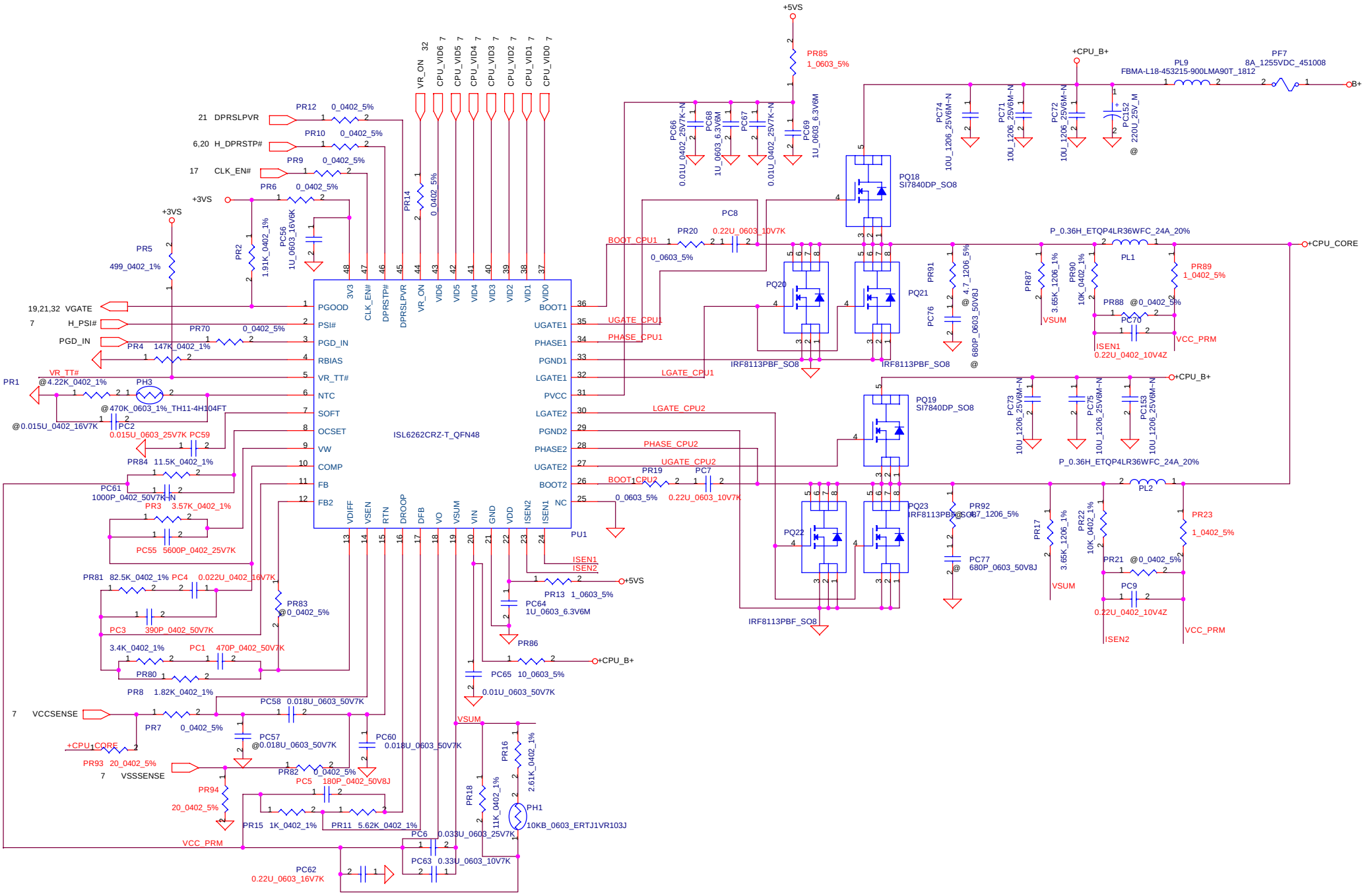

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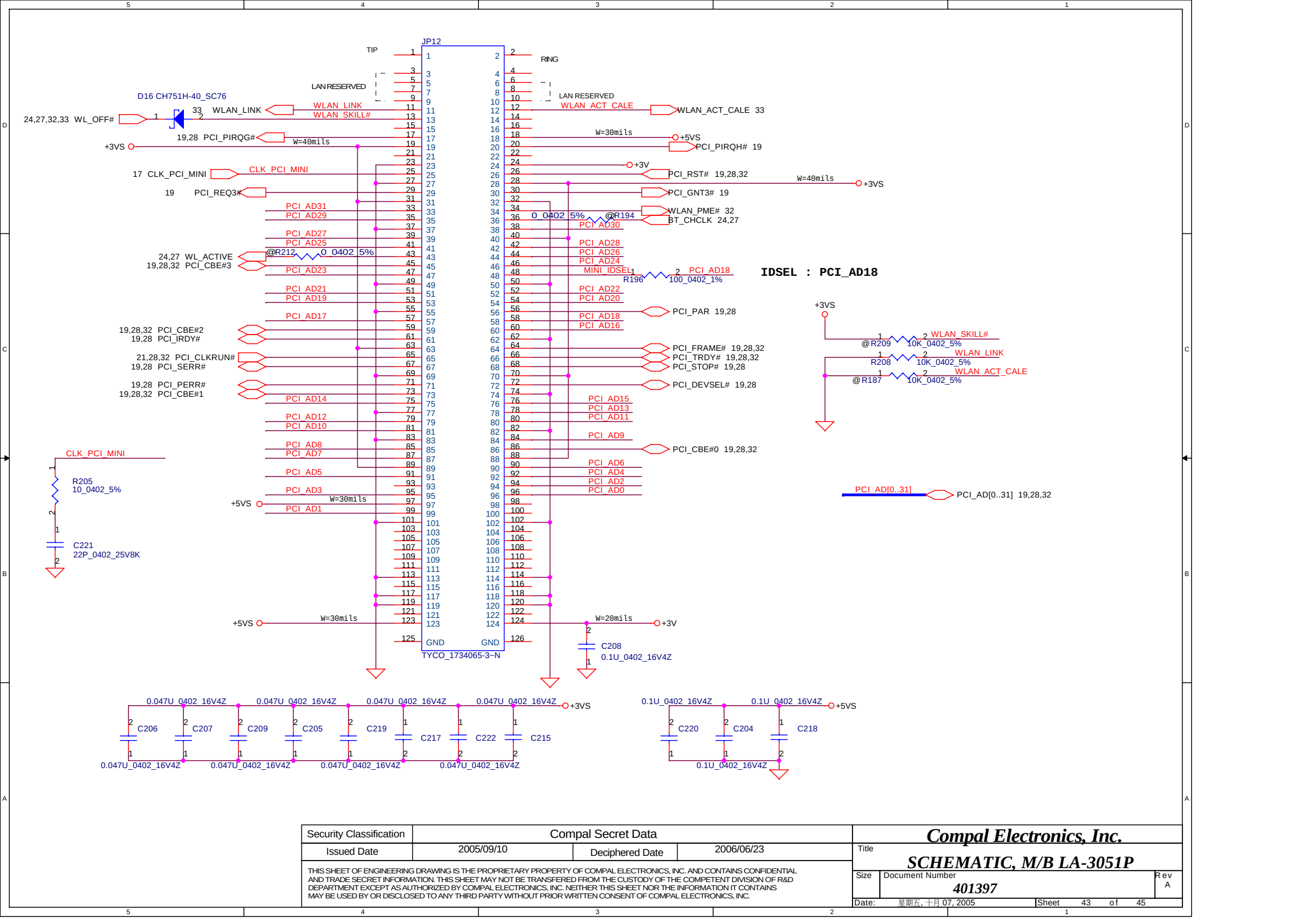

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	18	TV-OUT/LVDS/CRT	Aug. 1st	NEC	For EMI	Add D1, D2 for CRTHSYNC# & CRTVHSYNC#	0.1
2	33	BIOS/EE-Prom/TP/KB/SW	Aug. 2nd	NEC	For GALAN & CALEXICO LAN LED control	Add U33, U34, R519~524 for the LAN LED control circuit	0.1
3	9	Calistoga(1/6)-GTL/DMI/DDR	Aug. 8	INTEL	To enable faster C4 exit	Add R526 to connect PM_EXTTS1# of the GMCH and DPRSLPVR of the ICH	0.1
4	21	ICH7M(3/4)USB,GPIO,PCIE	Aug. 8	INTEL	Define GPIO STATE	Add R527~R529 PULL-HIGH	0.1
5	32	ENE-KB910L/TPM	Aug. 8	INTEL	No connect clk of debug tool	Add R530 connect to U13 pin22	0.1
6	25	BCM5751-GLAN	Aug. 8	INTEL	No connect reset signal of LAN chip	Connect to PLT_RST of ICH7	0.1
7	25	BCM5751-GLAN	Aug. 8	NEC	Change the pull high resistance	Change R7 & R8 from 1K to 4.7K	0.1
8	17	ClockGen	Aug. 11	COMPAL	ICS_CLK GEN BUG, need FSC pull down	R105 change to 0 ohm and remove R99	0.1
9	33	BIOS/EE-Prom/TP/KB/SW	Sep. 8	COMPAL	Fix the GOLAN LED incorrect light	Del U33, Add Q45,R532, change R523.1 to WL_OFF#	0.2
10	30	HD Audio Codec_ALC262	Sep. 10	NEC	Using ALC262 GPIO2 (pin2) control amplifier status	Del R199, GPIO2 Add R533,R379 and connect to EAPD	0.2
11	24	USB/BlueTooth/FP	Sep. 10	COMPAL	Change USB diode to low capacitor diode	Change D3,D14,D21,D22 to NUP4301MR6T1	0.2
12	18	TV-OUT/LVDS/CRT	Sep. 10	COMPAL	Change DISPOFF# control from EC to VBIOS	Add U33(And gate)	0.2
13	6	Yonah(1/2)-GTL/ITP-XDP	Sep. 10	EC	For EC SM bus blance	Change Thermal Sensor for SM bus2 to SM bus1	0.2
14	21	ICH7M(3/4)USB,GPIO,PCIE	Sep. 10	EC	For S4 needed	Add U36 with S5	0.2
15	24	USB/BlueTooth/FP	Sep. 14	NEC	security issue	Change :USB port0: Fingerprint & USB port6: Bluetooth	0.2
16	33	BIOS/EE-Prom/TP/KB/SW	Sep. 14	NEC	Modify the define LED to GOLAN	Take off R520,R521, mount R523,R524	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	PWR-CPU_CORE	Aug. 2	NEC	For protection	Add Fuse at CPU B+	0.1
2	35	PWR-DCIN/Precharge	Aug. 29	Compal	For VIN dector design issue at LC2	Change PC121 to 2200P and PR141 to 56K.	0.2
2	38	PWR-CHARGER	Sep. 16	Compal	Change adapter from 60W to 75W and modify the CP to 4.61A	Change PR48 to 26.1K	

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