Compal Confidential

VALGC_GD M/B Schematics Document

AMD Fs1r2 Richland Processor with DDRIII + Bolton-M3 FCH
AMD Mars XT M2

LA-A091P

2013-04-16

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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Title: Cover Page

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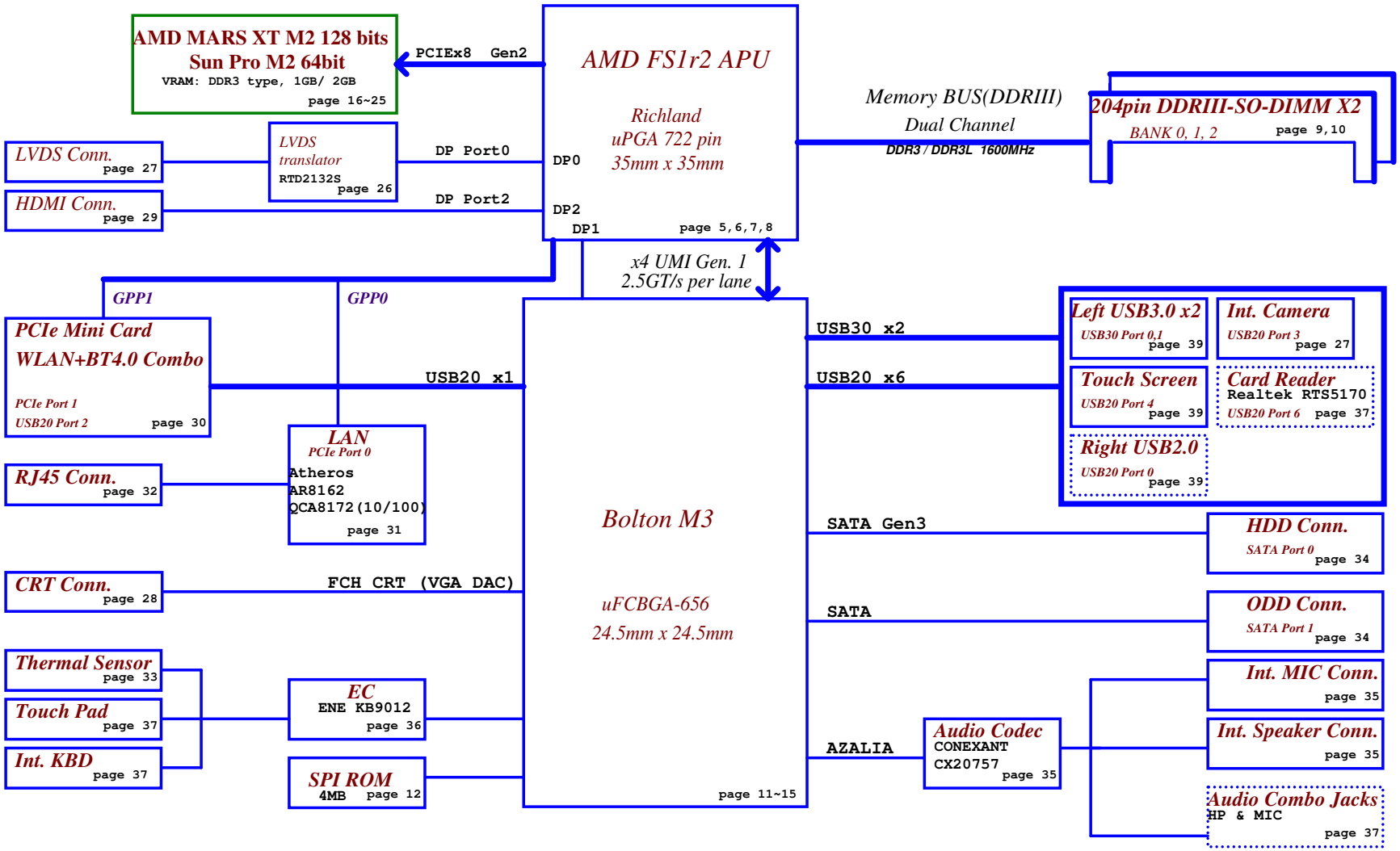
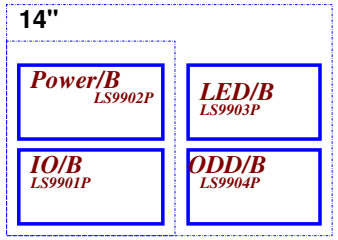


Sub-borad

15"

14"



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Title: MB Block Diagram

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW +1.1VALW	+1.5V +1.5V_APU	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +VGA_CORE +3.3VGS +1.8VGS +1.5VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.2
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Ra = R310
Rb = R311

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
SMB_EC_CK2_SUS SMB_EC_DA2_SUS	KB9012 +3VALW	X	X	X	X	X	X	X	V +1.5V	X
FCH_SCLK0 FCH_SDATA0	FCH +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS (LV shifter)	V	X	X	X	X	V	X	X	V

USB Port Table

USB 2.0	USB 3.0		Port	4 External USB Port
			0	USB Port 2.0 (Right Side)
			1	
			2	Mini Card(WLAN)
			3	Camera /
			4	Touch Screen
			5	
			6	Card Reader
			7	
			8	
			9	
	XHCI	0	10	USB 2.0 Port (Left Side)
		1	11	USB 2.0 Port (Left Side)
		2	12	
		3	13	

BOM Structure Table

BOM Structure	BTO Item
PX@	VGA circuit
14@	For 14"
15@	For 15"
45@	HDMI LOGO
CMOS@	CMOS Camera part
8162@	AR8162 LAN part
8172@	AR8172 LAN part
CMOS@	For CMOS circuit
TS@	For Touch Screen circuit
X76@	X76 Level part for VRAM
GCLK@	Ues GCLK circuit
NOGCLK@	No use GCLK circuit
GCLK302@	302 part for DIS
GCLK238@	238 part for UMA
LVDS@	LVDS circuit
PXNOGCLK@	No use GCLK circuit in GPU
LDO@	LDO mode for LAN
SWR@	SWR mode for LAN
DEBUG@	For debug
ME@	ME part
MIC@	MIC part
885N@	Unpop in KBC page
JUMP@	JUMP
TEST POINT@	TSET POINT
SHORT PAD@	SHORT PAD
EMI@	EMI part
@ESD@	Reserve for ESD
@EMI@	Reserve for EMI
@	Unpop
MARS@	VRAM CHB parts for MARS
2132S@	Panel PWM part for RTD2132S
2132R@	Panel PWM part for RTD2132R
ShareROM@	Reserve for ShareROM
Strap@	Reserve for Strap pin

USB OC MAPPING

OC#	USB Port	
0	USB20 port10,port11	USB30 port0,port1
1	USB20 port0	
2		
3		

APU PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	

FCH PCIE PORT LIST

Port	Device
1	
2	
3	
4	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_101xb
SB-TSI(default)	1001_100xb
VGA(int. thermal)	1000_001xb
RTD2132S	1010_1000b
VGA(ext. thermal)	0100_1101b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

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X76@ Mars XT VRAM STRAP

	Vendor UV5,UV6,UV7,UV8, UV9,UV10,UV11,UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
MS2G	Samsung 2048Mbits SA000068U00 128M16 K4W2G1646E-BC1A FBGA	0	0	0	NC	4.75K
MM2G	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:k	0	0	1	8.45K	2K
MH2G	Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C FBGA	0	1	0	4.53K	2K

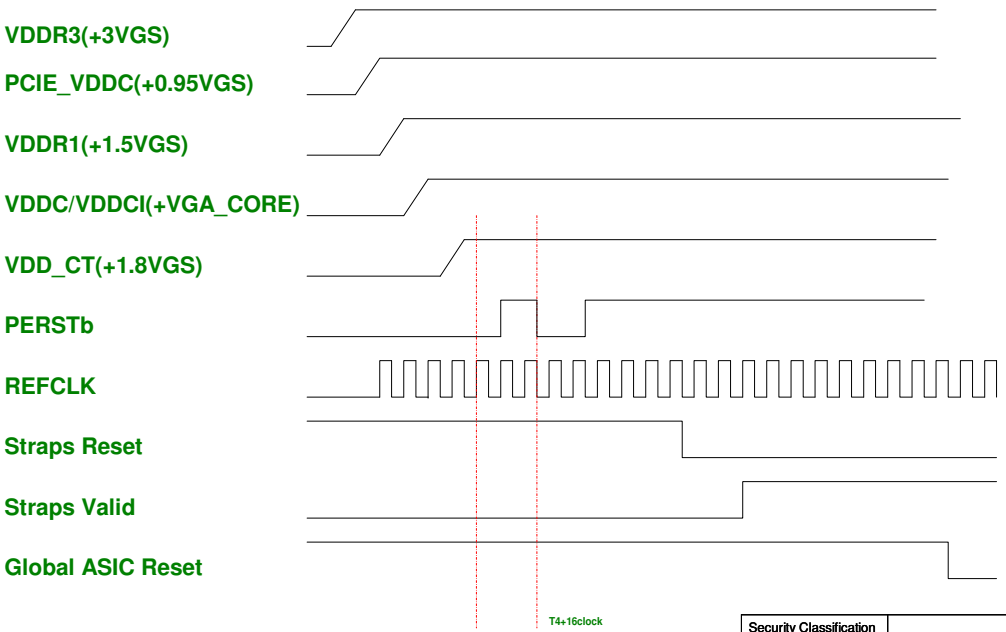
X76@ Sun PRO VRAM STRAP

	Vendor UV9,UV10,UV11,UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
SS2G	Samsung 2048Mbits SA000068R00 256M16 K4W4G1646B-HC11 FBGA	0	0	0	NC	4.75K
SM2G	Micron 2048Mbits SA000065D00 256M16 MT41K256M16HA-107G	0	0	1	8.45K	2K
SS1G	Samsung 1024Mbits SA000068U00 128M16 K4W2G1646E-BC1A FBGA	0	1	1	6.98K	4.99K
SM1G	Micron 1024Mbits SA000067500 128Mx16 MT41J128M16JT-093G:k	1	1	0	3.4K	10K
SH1G	Hynix 1024Mbits SA000065300 128M16 H5TQ2G63DFR-N0C FBGA	1	1	1	4.75K	NC

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



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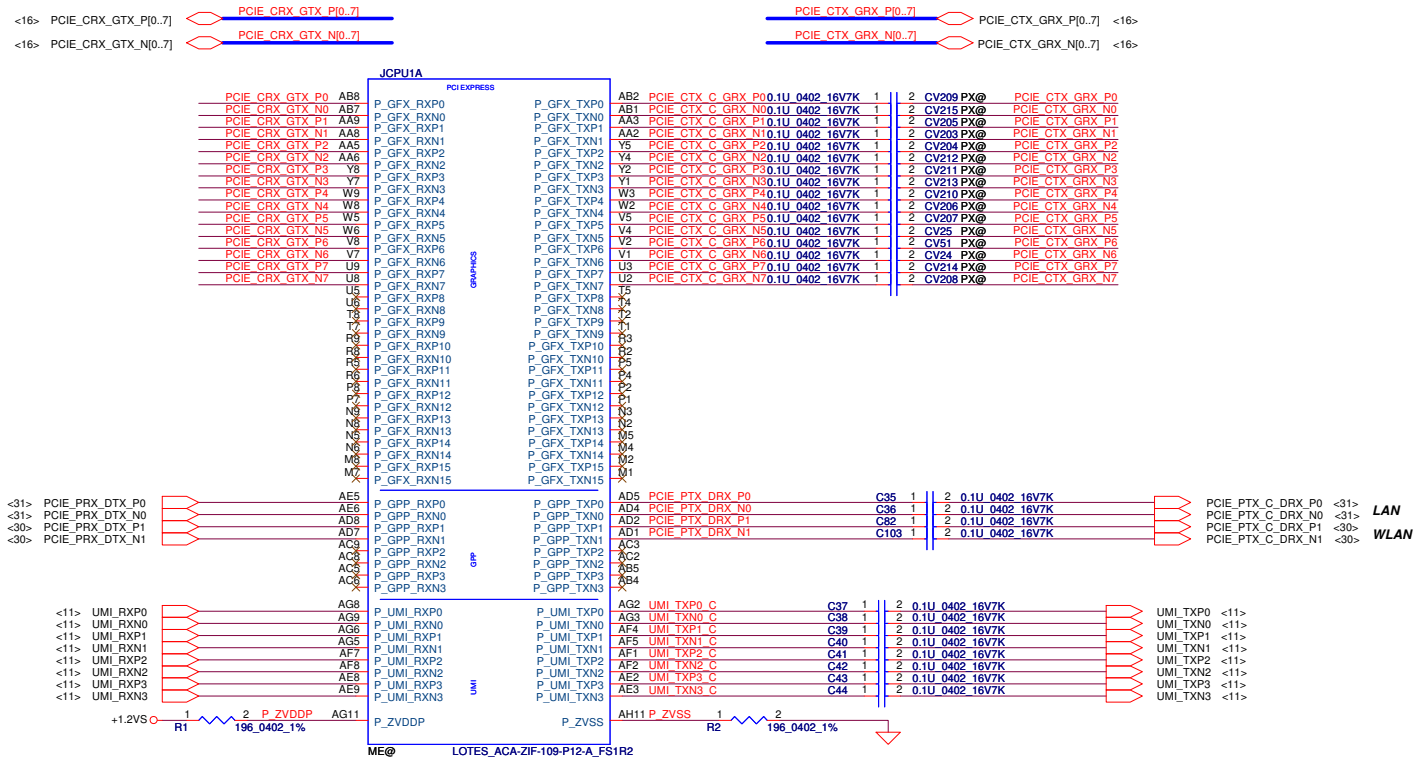

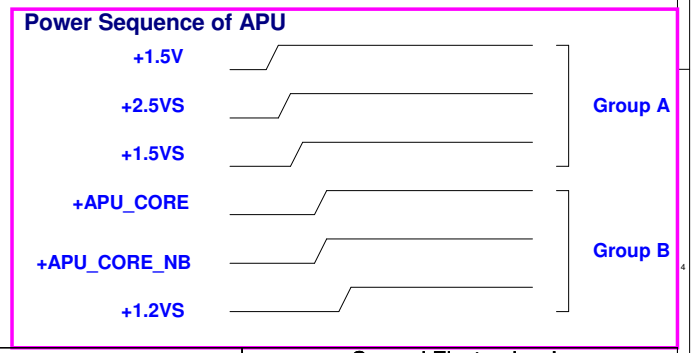

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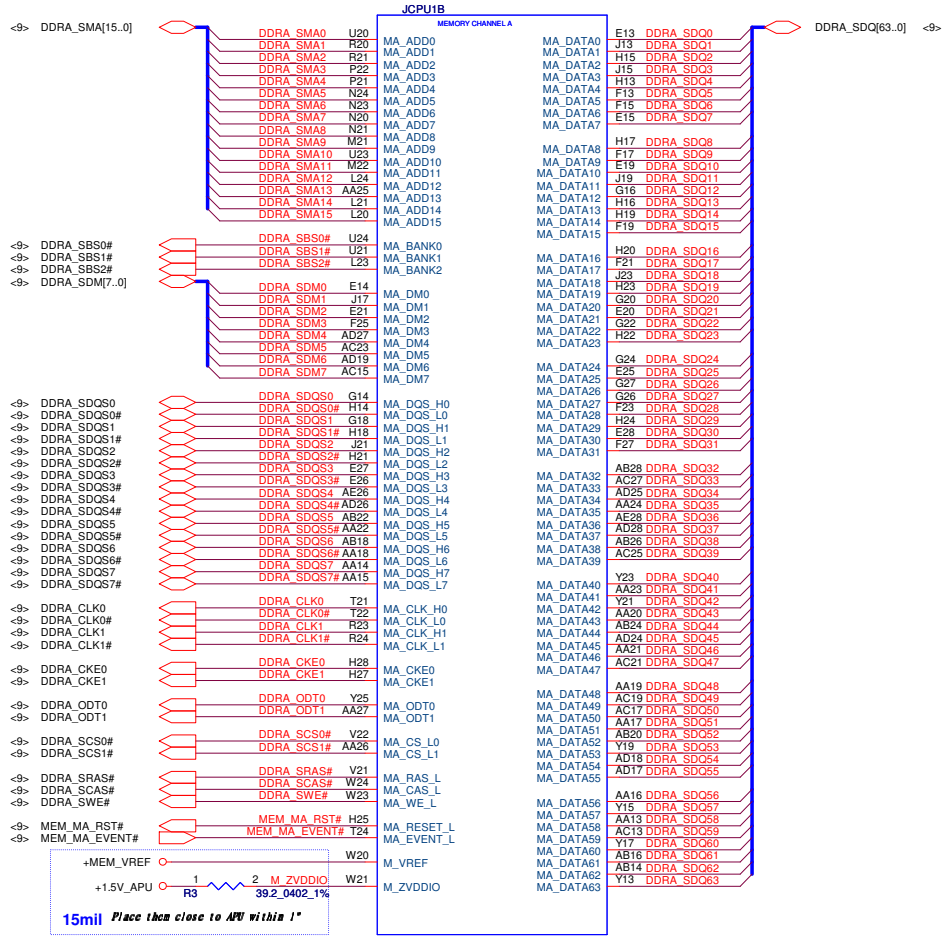
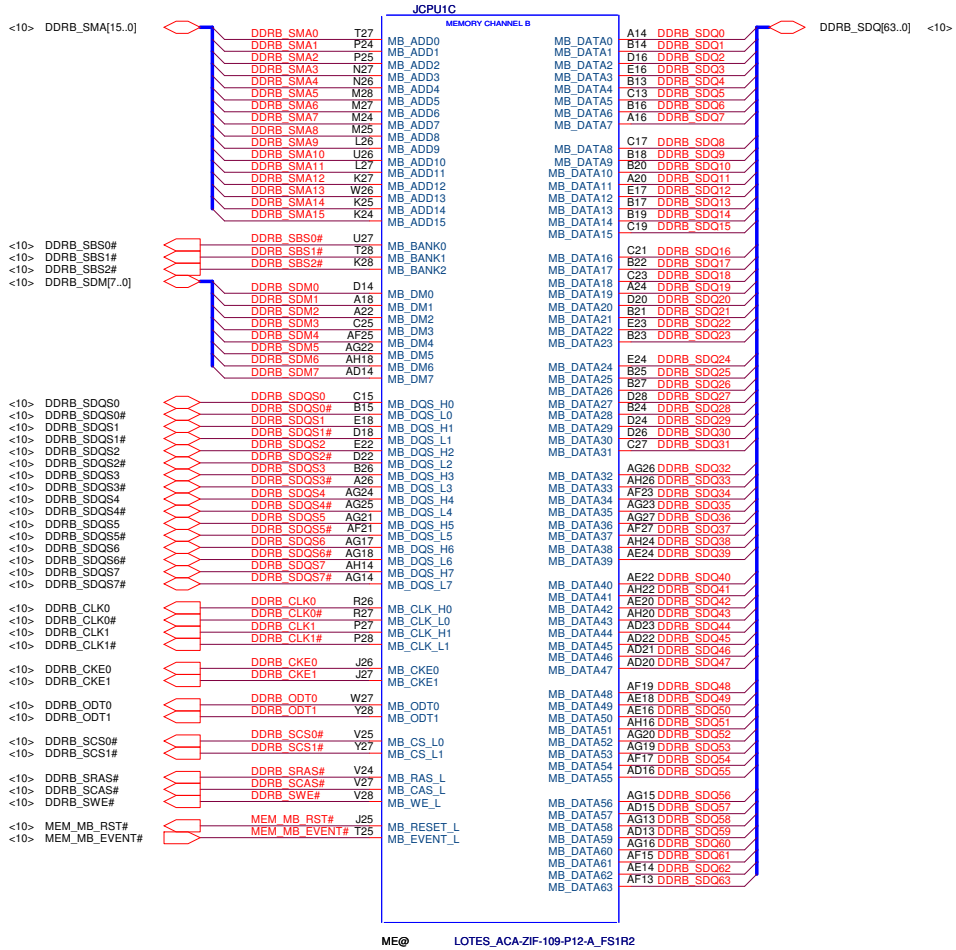
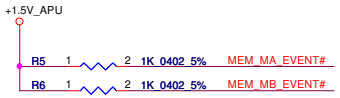
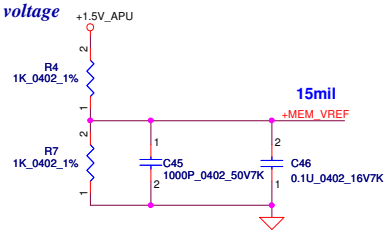




EVENT# pull high



0.75V reference voltage



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Title: FS1r2 DDRIII Memory I/F

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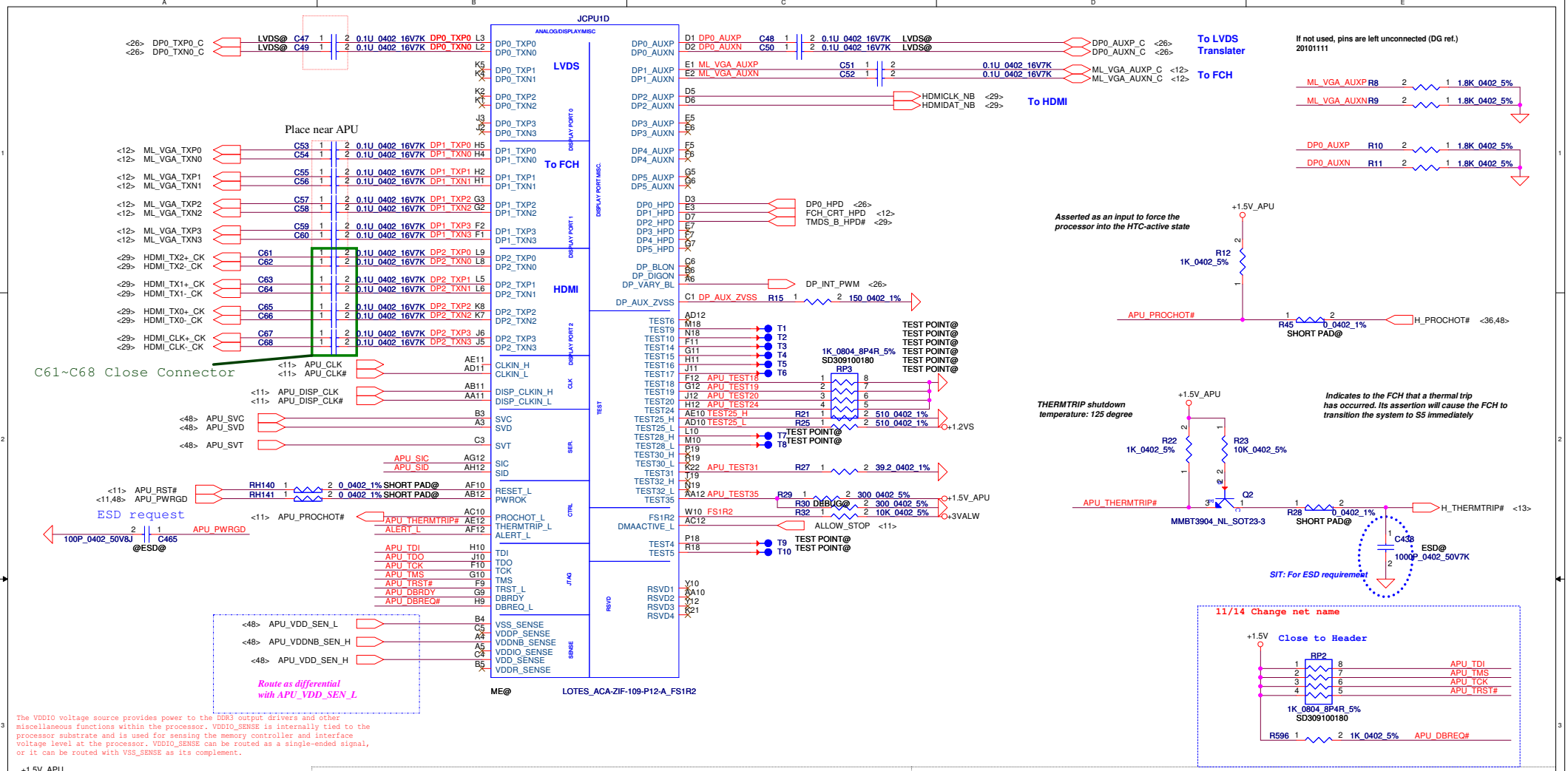
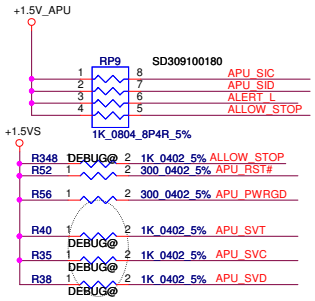
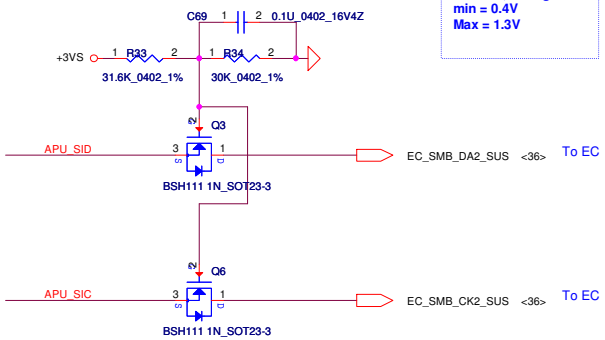


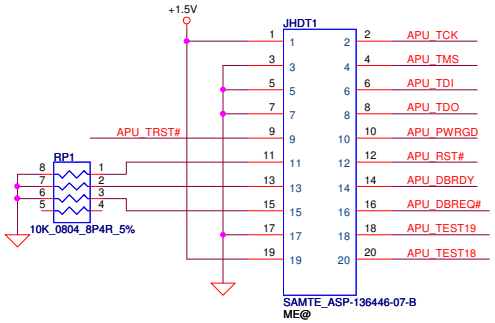
The VDDIO voltage source provides power to the DDR3 output drivers and other miscellaneous functions within the processor. VDDIO_SENSE is internally tied to the processor substrate and is used for sensing the memory controller and interface voltage level at the processor. VDDIO_SENSE can be routed as a single-ended signal, or it can be routed with VSS_SENSE as its complement.



CPU TSI interface level shift



HDT Debug conn



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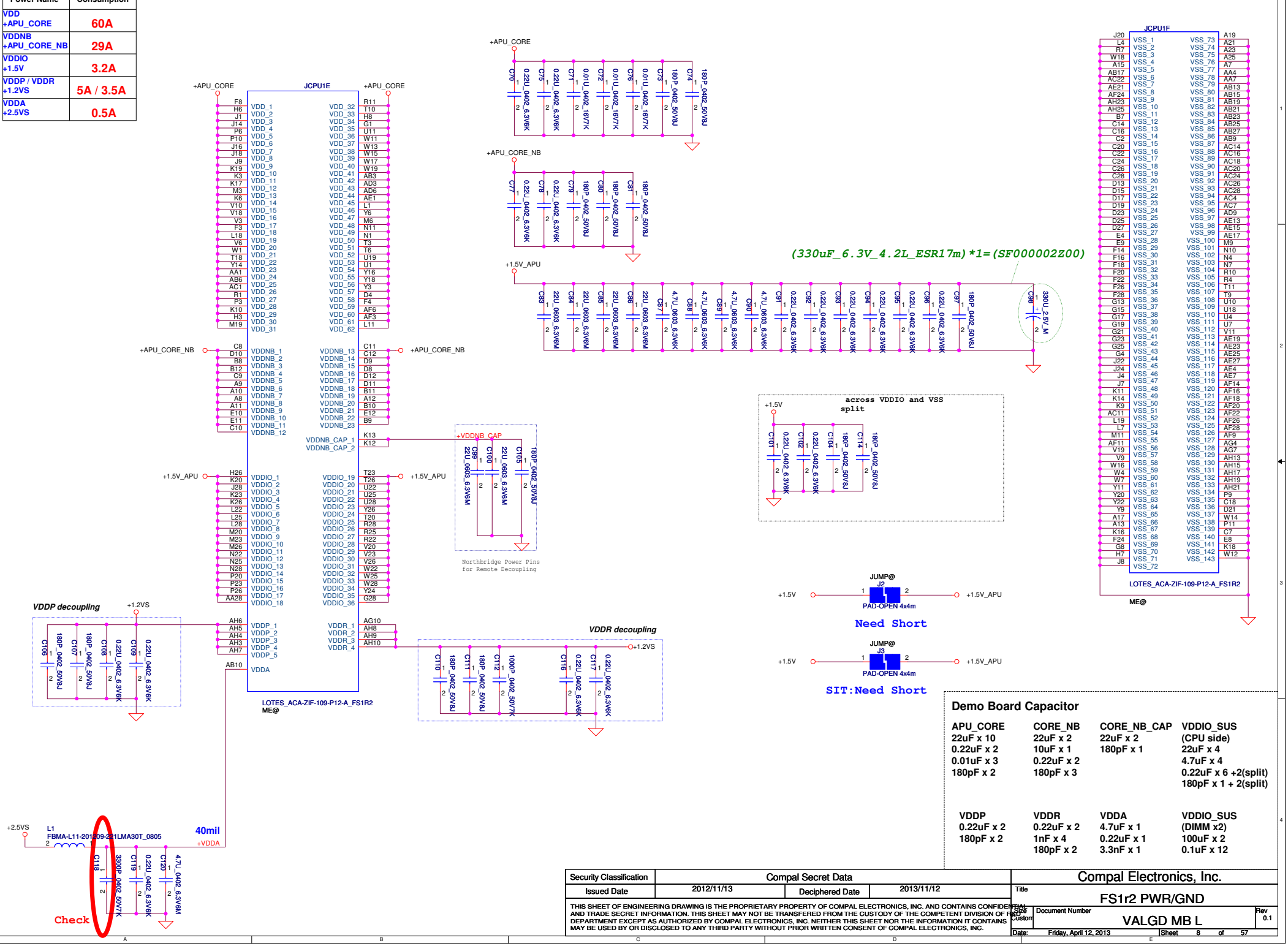
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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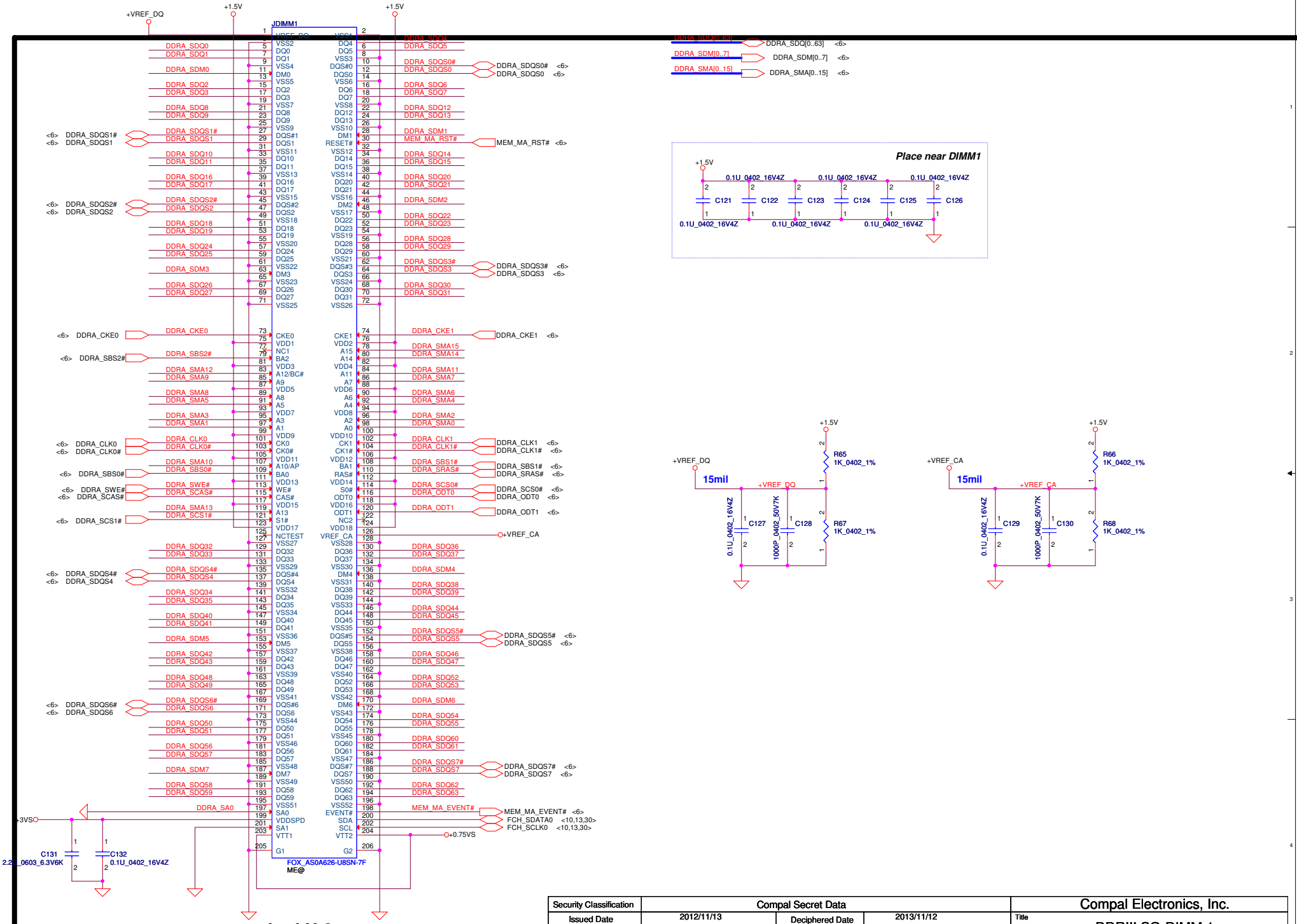

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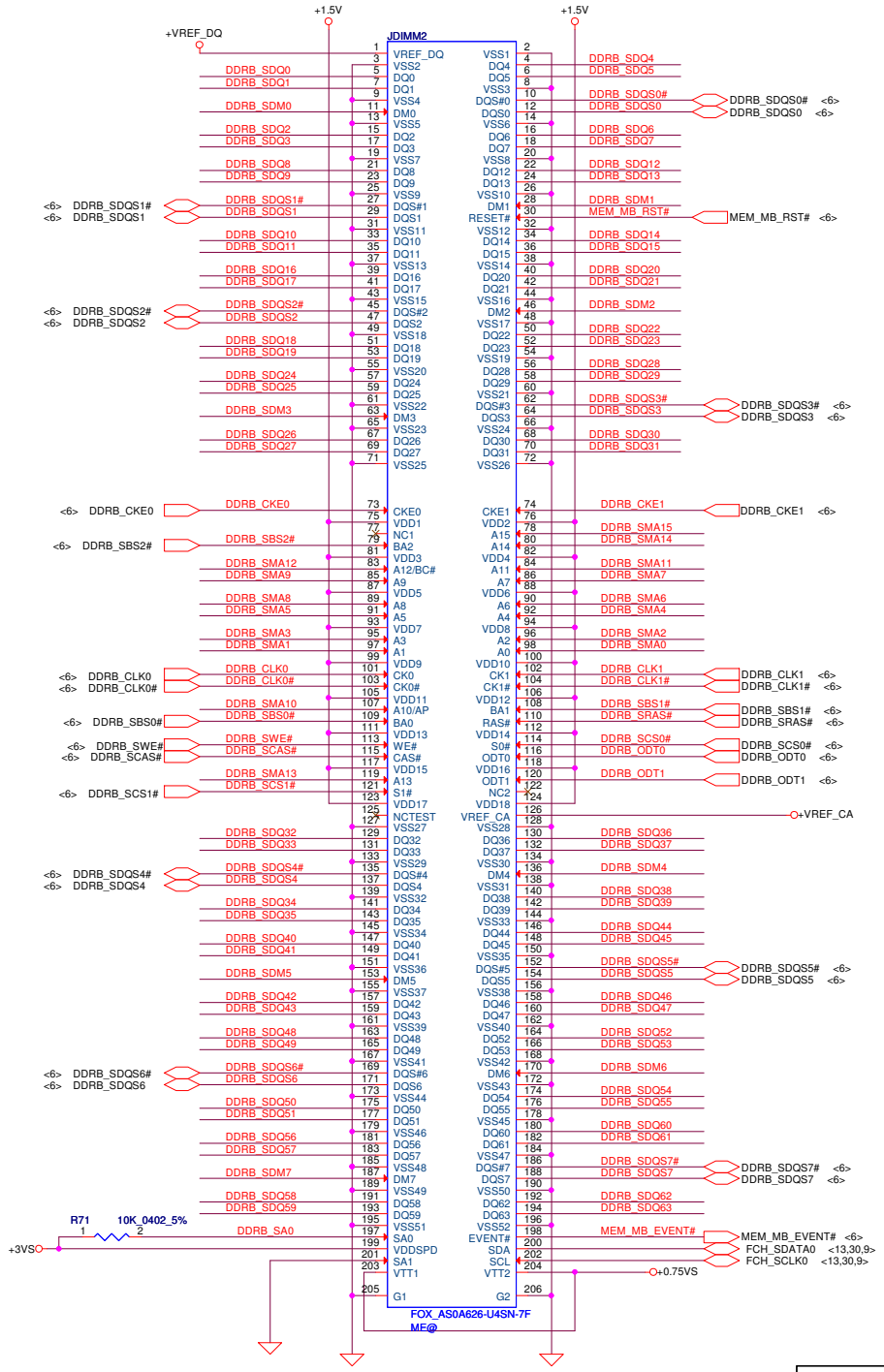

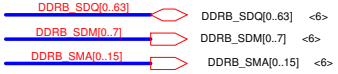

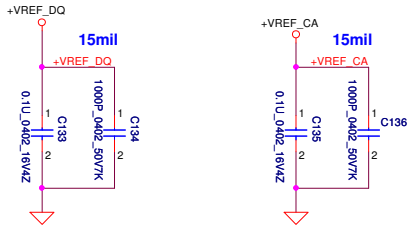

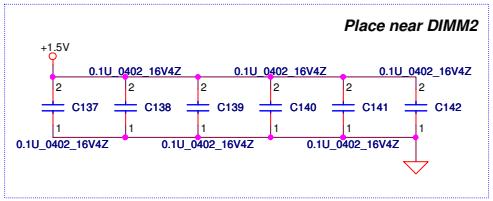

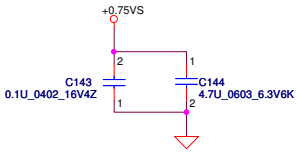

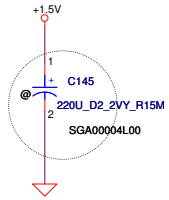

SIT:1/26 change to POLY

Standard H:4mm

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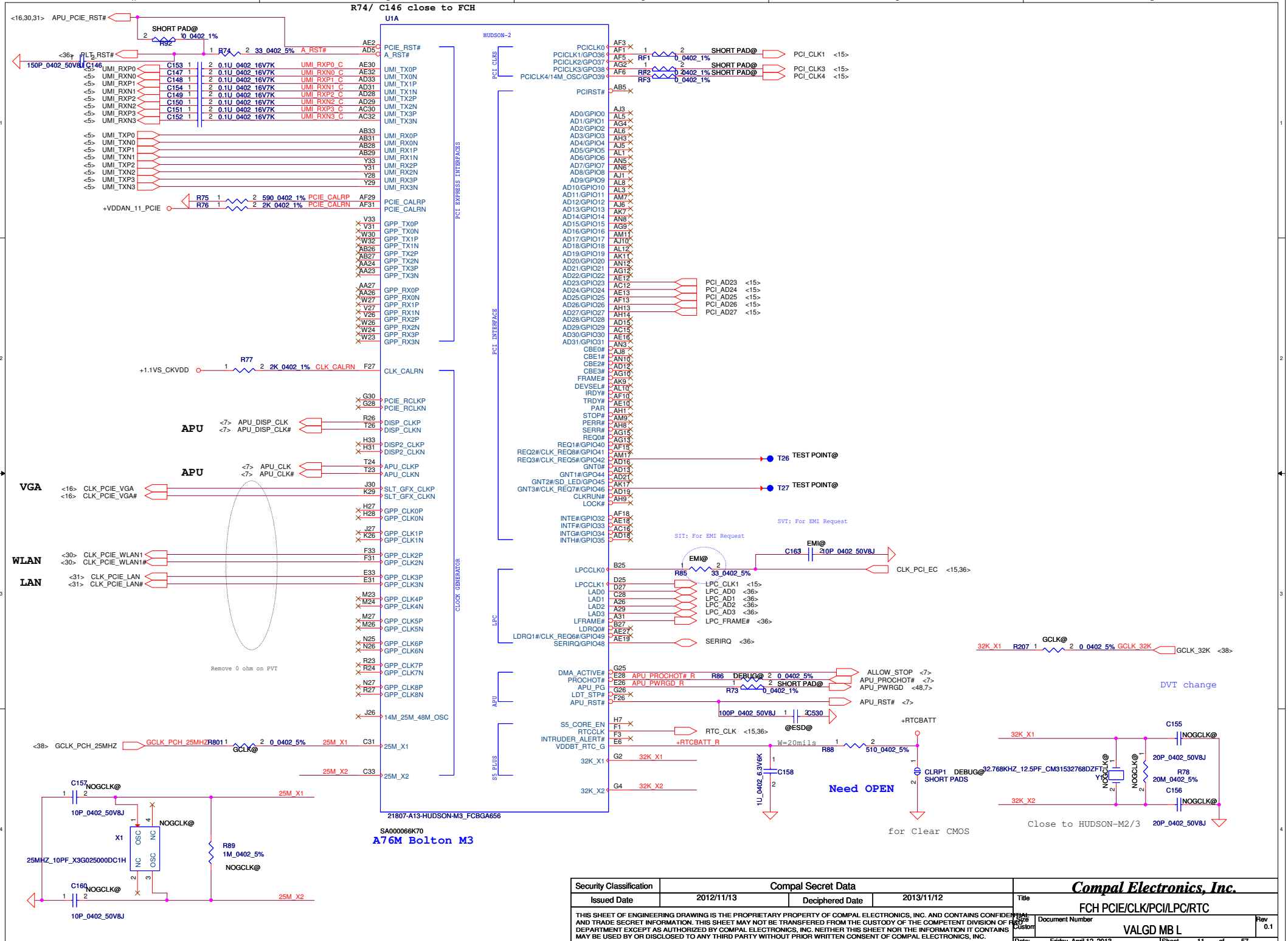
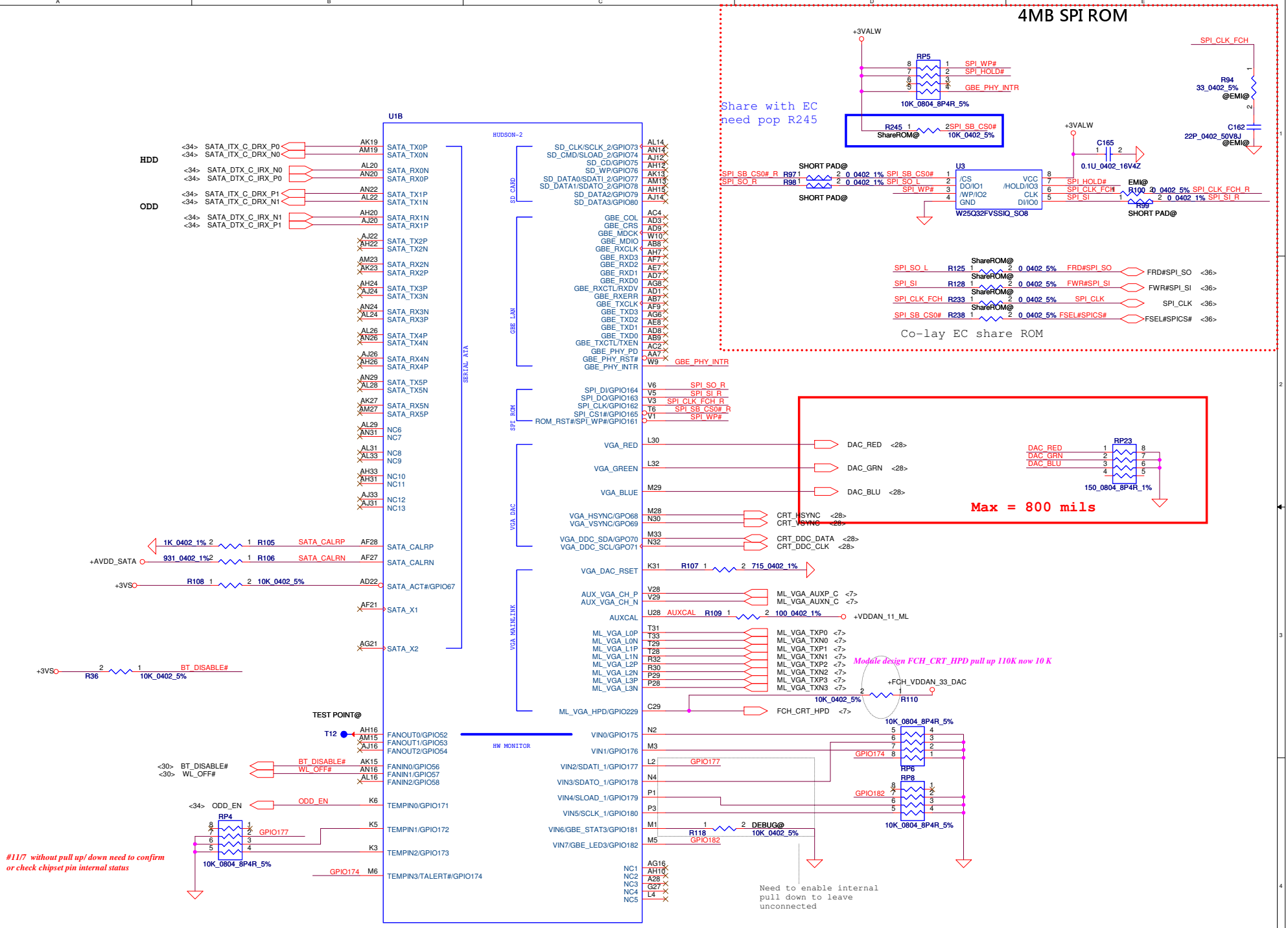

R74/ C146 close to FCH
U1A
HUDSON-2
PCIE_RST#
A_RST#
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
S5 PLUS
PCI CLKS
21807-A13-HUDSON-M3_FCBGA656
SA000066K70
A76M Bolton M3
APU
VGA
WLAN
LAN
Remove 0 ohm on PVT
TEST POINT@
SIT: For EMI Request
SVT: For EMI Request
DVT change
Need OPEN
for Clear CMOS
Close to HUDSON-M2/3
Compal Secret Data
Compal Electronics, Inc.
FCH PCIE/CLK/PCI/LPC/RTC
VALGD MB L
Issued Date 2012/11/13
Deciphered Date 2013/11/12
Rev 0.1
Sheet 11 of 57
Friday, April 12, 2013



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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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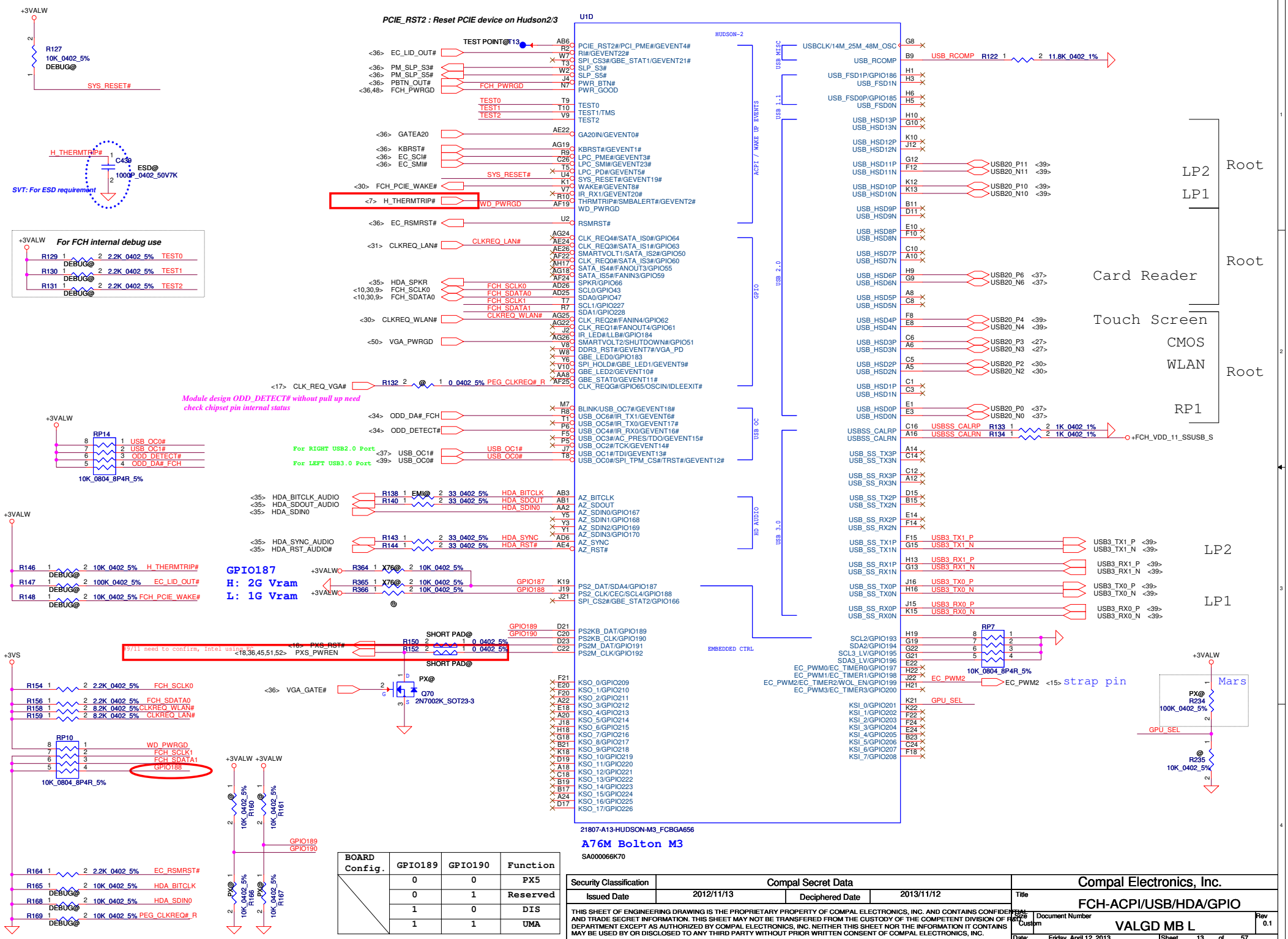
Compal Electronics, Inc.

Title: FCH SATA/SPI/VGA/HWM/SD

Size: B/25 Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 12 of 57



BOARD Config.	GPIO189	GPIO190	Function
	0	0	PX5
	0	1	Reserved
	1	0	DIS
	1	1	UMA

Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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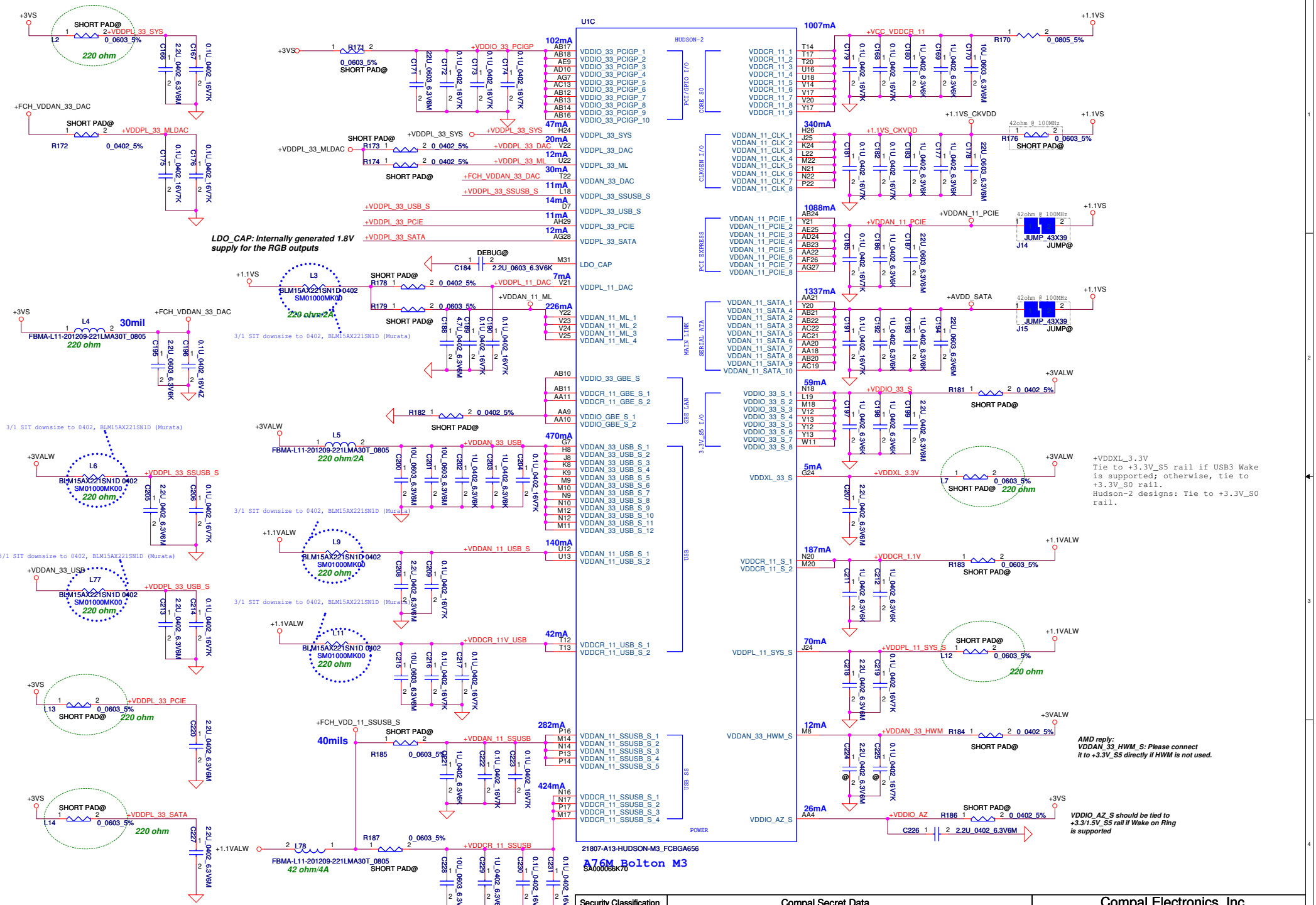
Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size: B/25 Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 13 of 57



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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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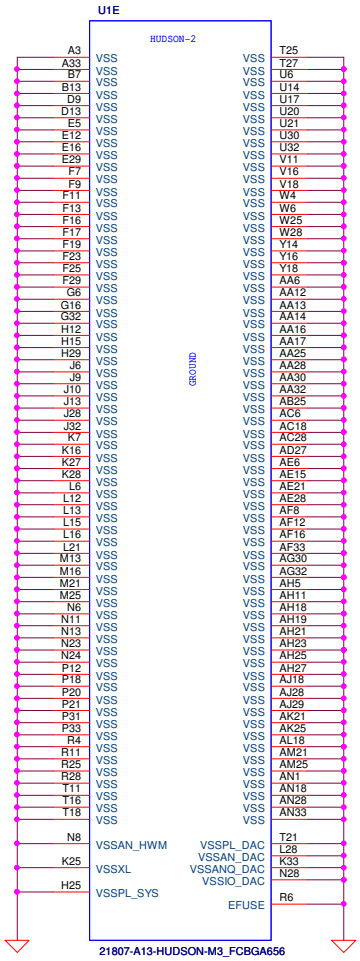
Compal Electronics, Inc.

Title: FCH PWR

Size: B/25 Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 14 of 57



A76M Bolton M3
SA000066K70

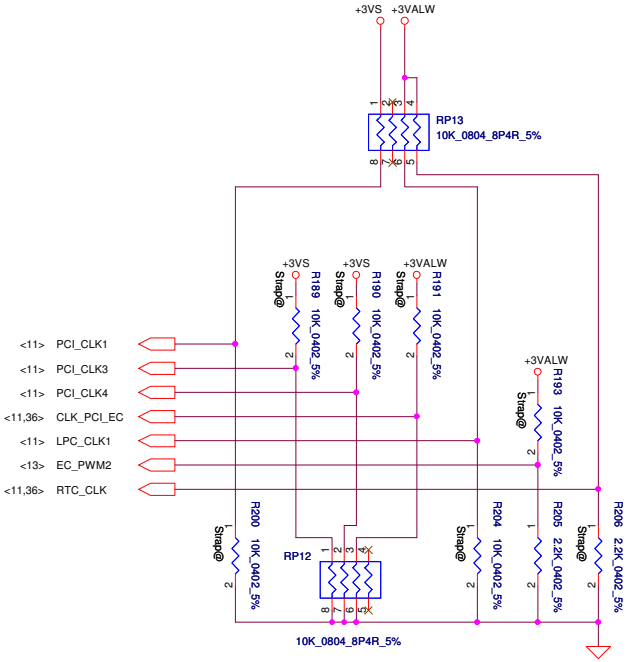
STRAP PINS

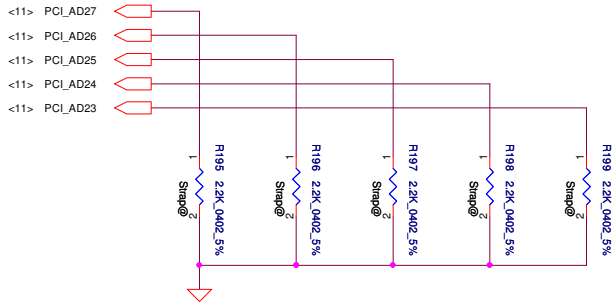
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title: FCH-VSS/Strap
				Size: B/26 Custom; Document Number: VALGD MB L; Rev: 0.1
				Date: Friday, April 12, 2013; Sheet 15 of 57

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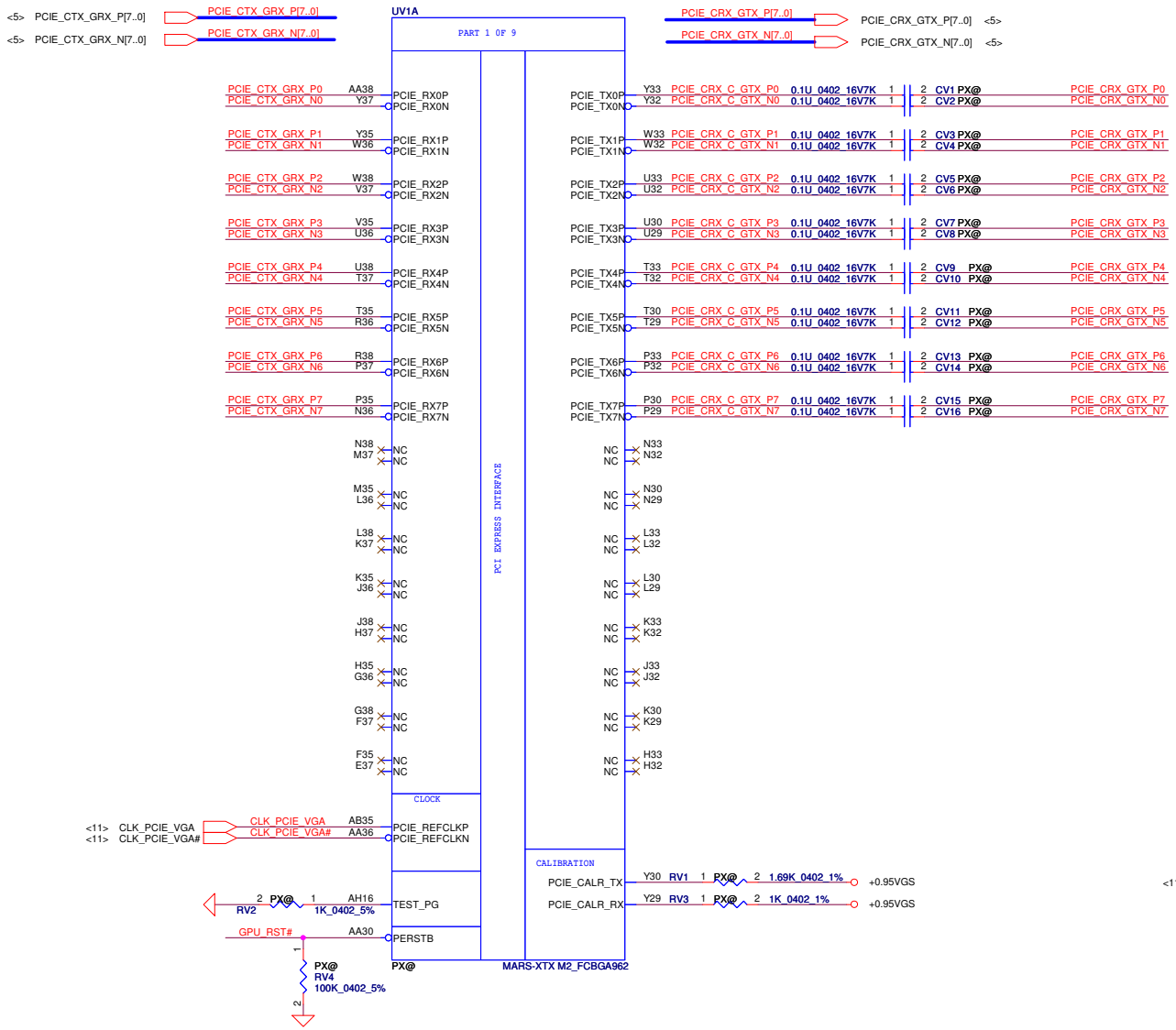
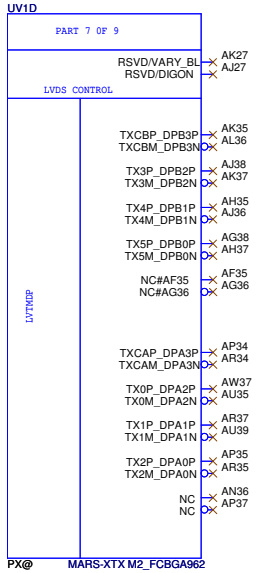
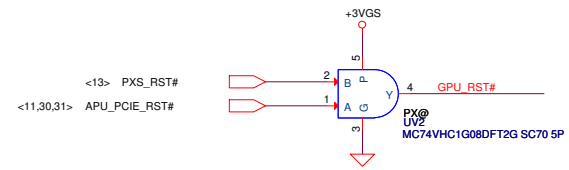


LVDS Interface





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title: ATI_MarsXT_M2_PCIE/LVDS
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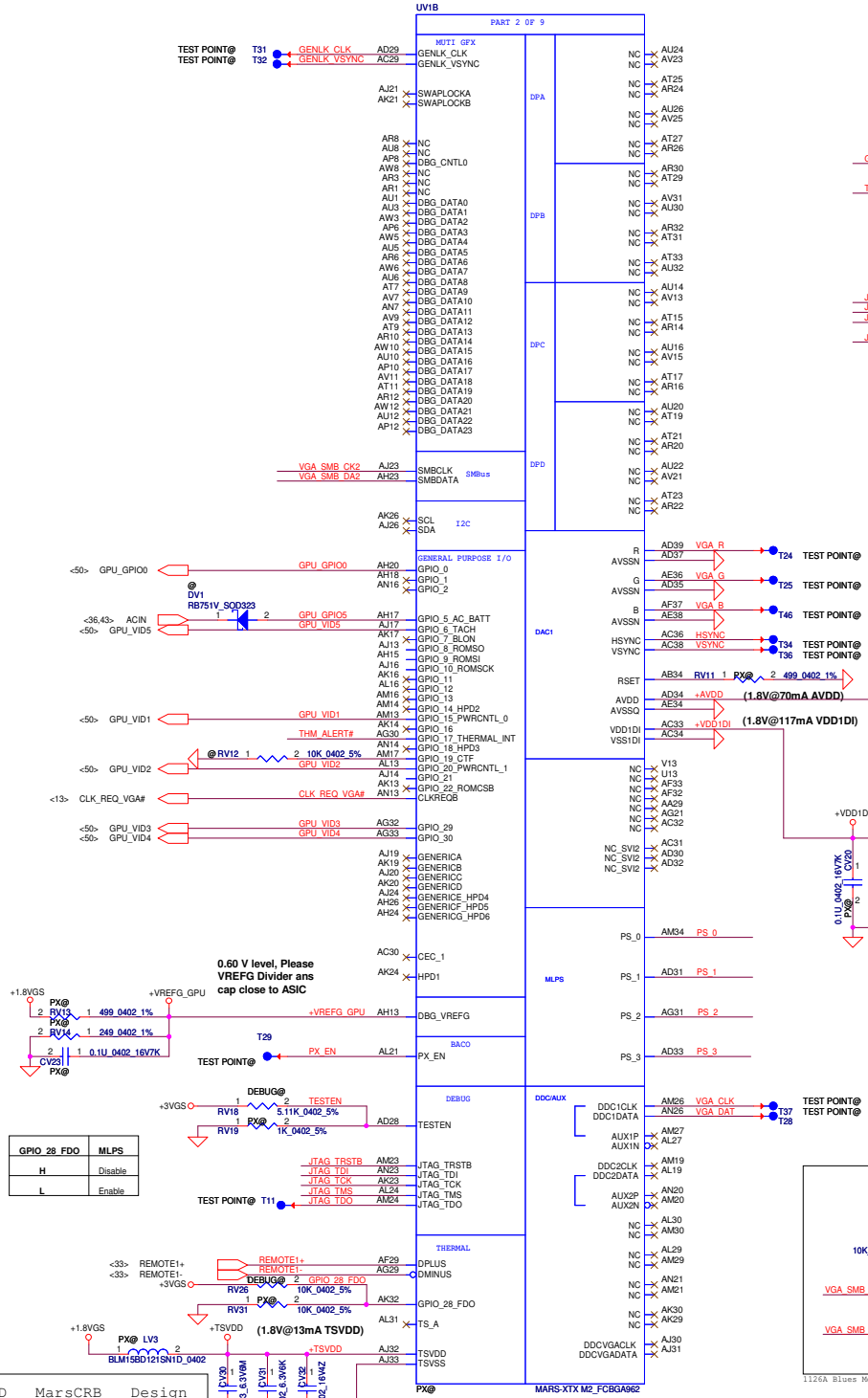
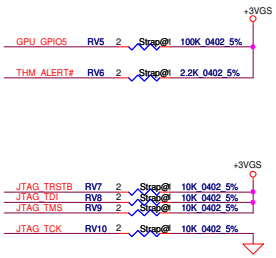
				Date: Friday, April 12, 2013; Sheet 16 of 57



GPIO_28_FDO	MLPS
H	Disable
L	Enable

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

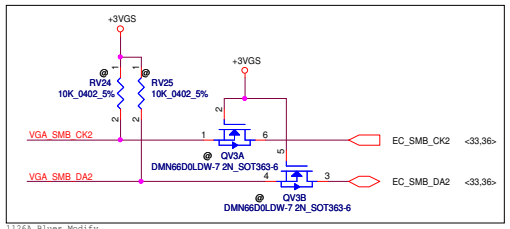
STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

DIS:+3VGS
UMA:+3VS



1126A Blues Modify

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

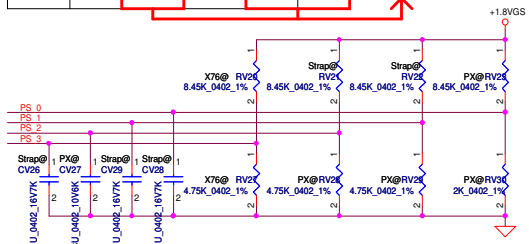
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
		NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 21



Place CLOSE VGA CHIP

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Compal Electronics, Inc.

Title: ATI_MarsXT_M2_Main_MSIC

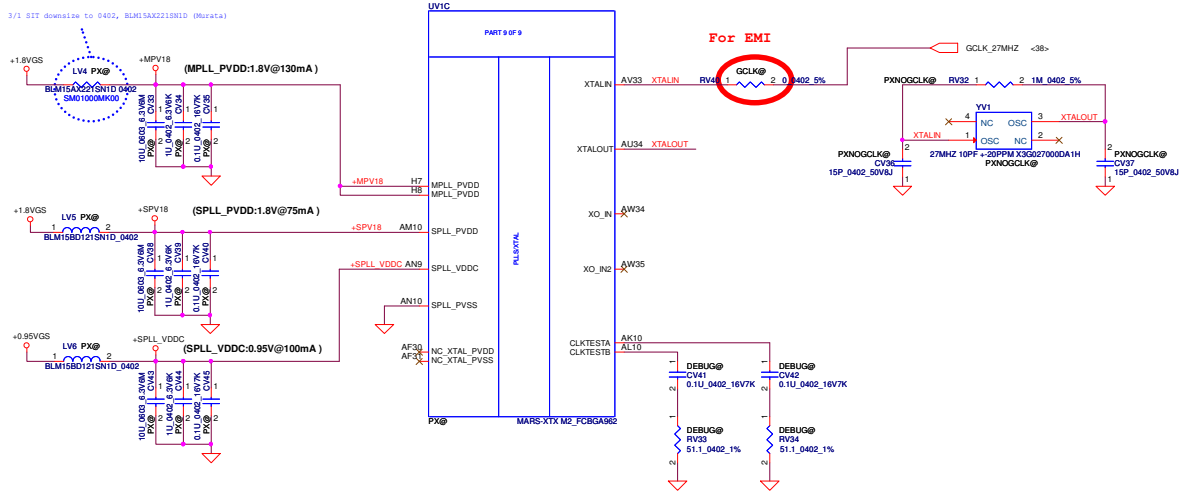
Size: C | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 17 of 57

MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

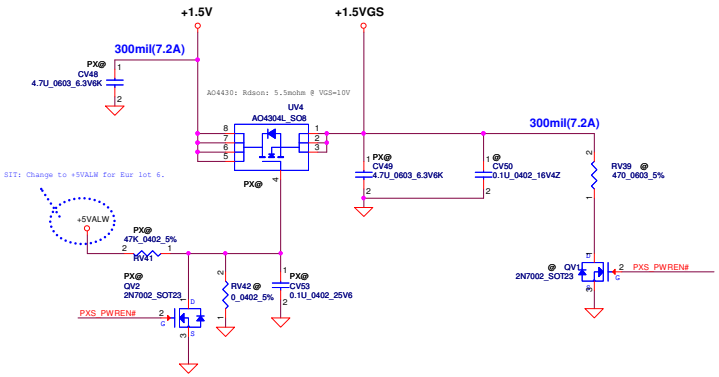
SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

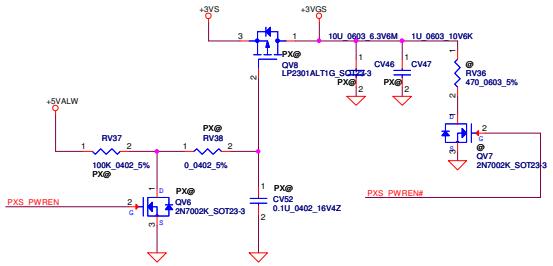


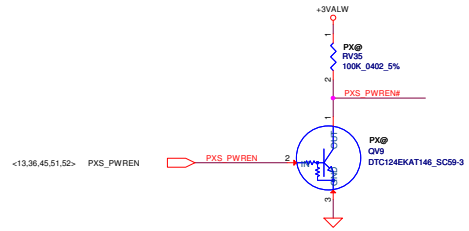
#9/11 need to confirm w/ Power team

+1.5V to +1.5VGS



+3VS to +3VGS





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+1.8VS to +1.8VGS

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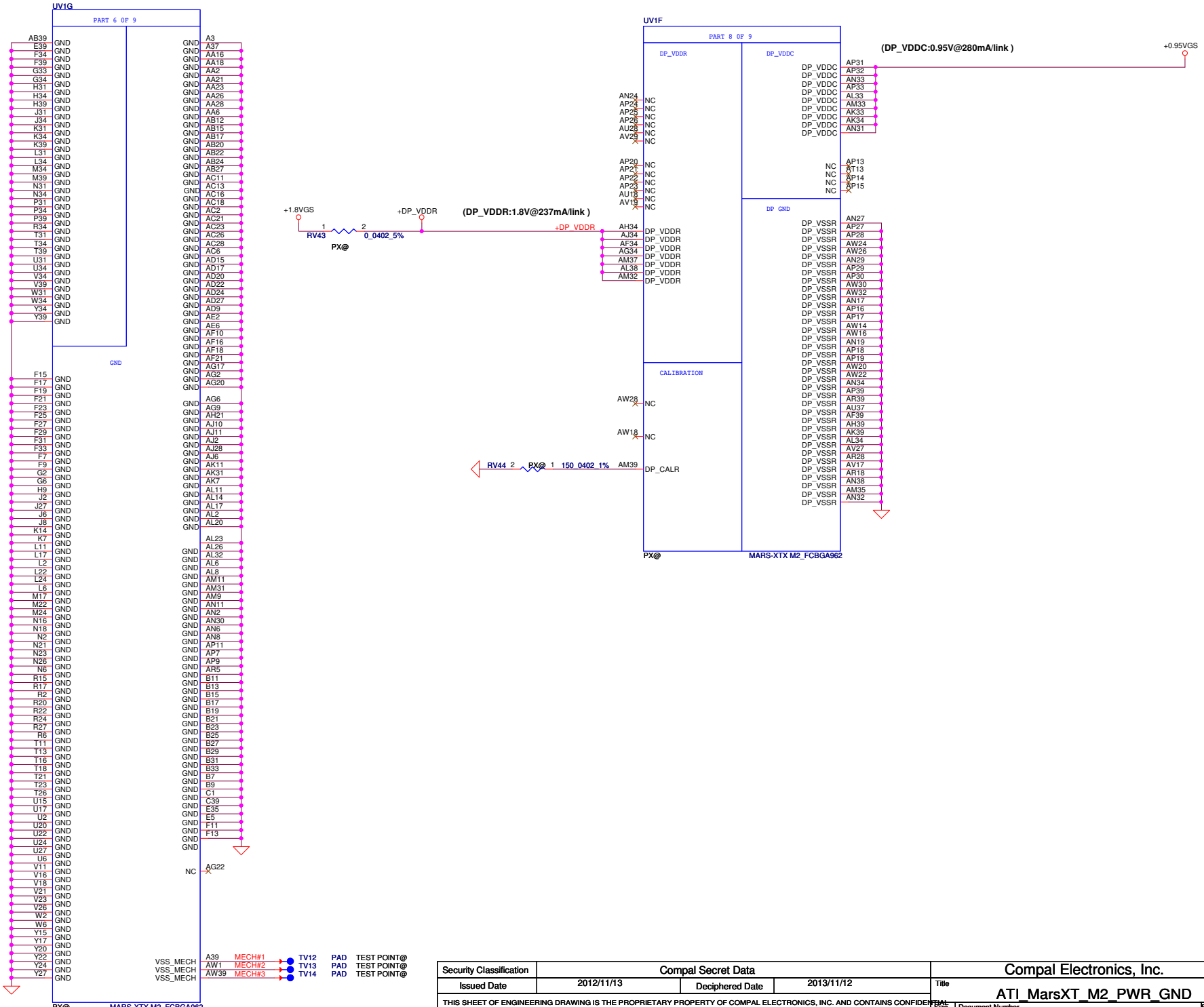
Compal Electronics, Inc.

Title: ATI_MarsXT_M2_BACO POWER

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Tuesday, April 16, 2013 | Sheet 18 of 57



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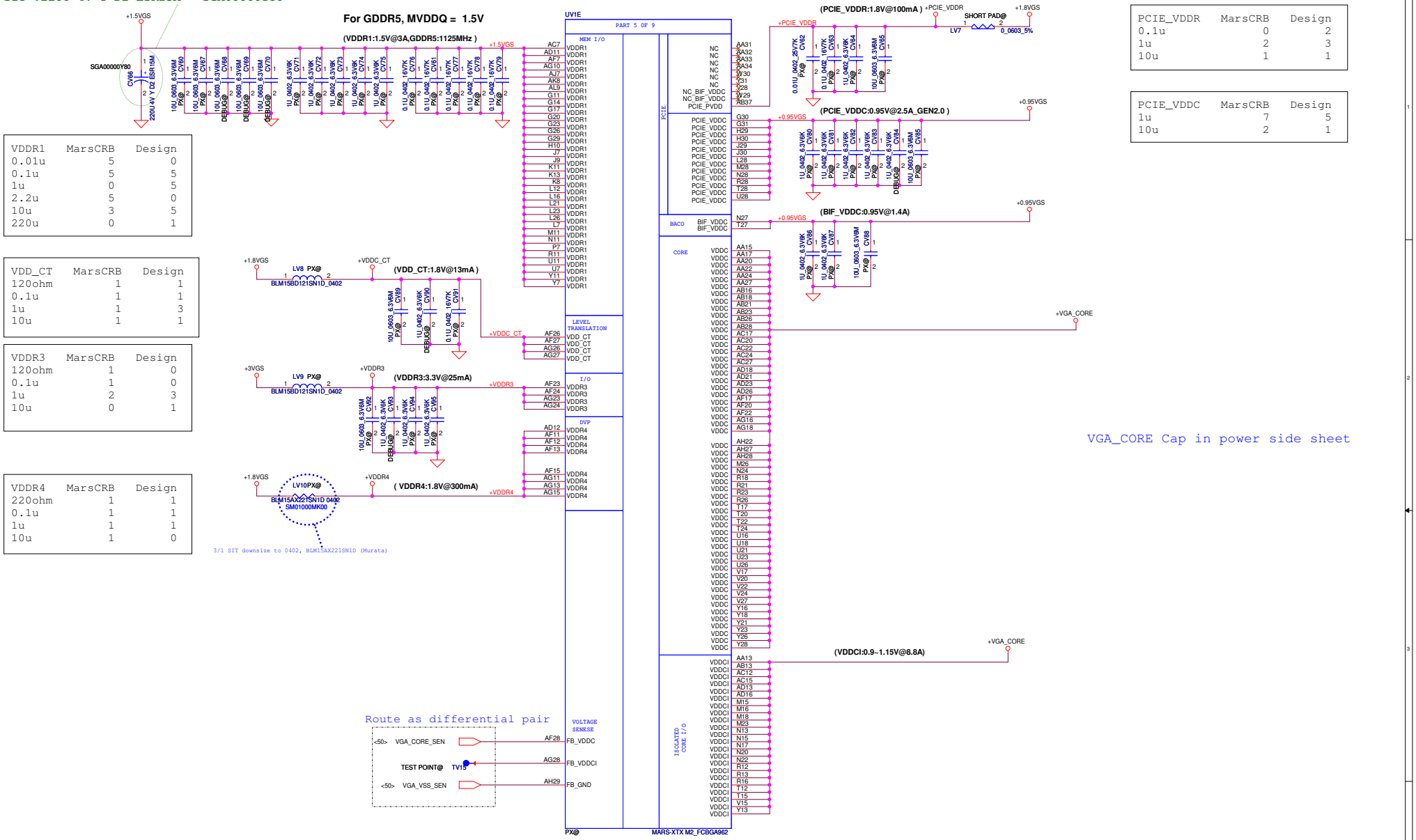
Compal Electronics, Inc.

Title: ATI_MarsXT_M2_PWR_GND

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 19 of 57

SIT :220U 4V Y D2 ESR15M = SGA00000Y80



VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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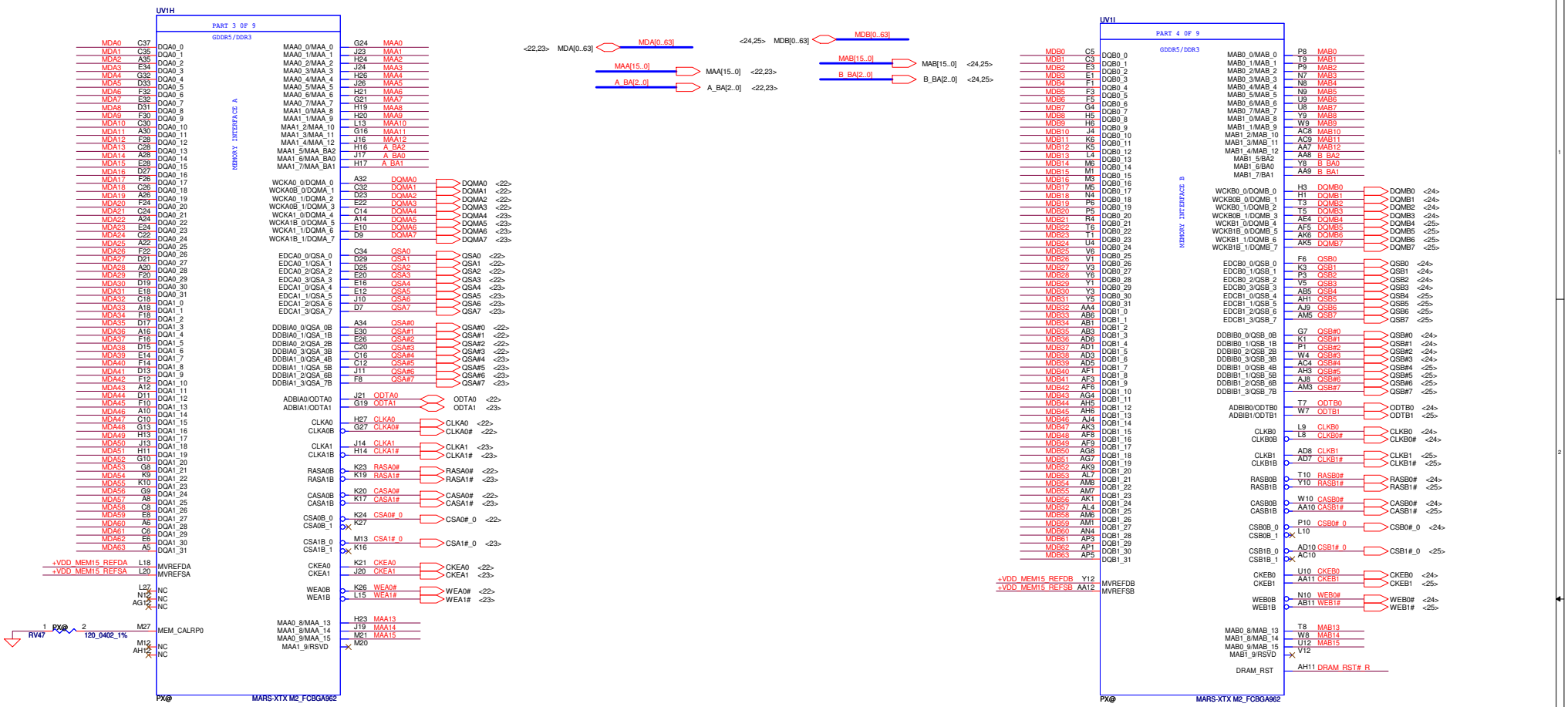
Compal Electronics, Inc.

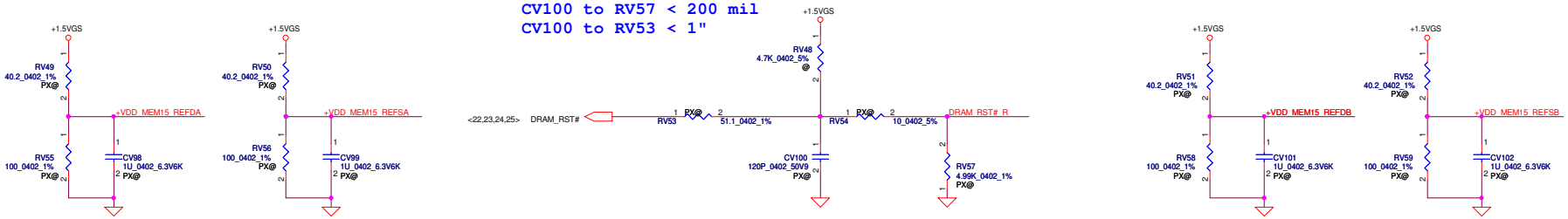
Title: ATI_MarsXT_M2_Power

Size: C | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 20 of 57



Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"



DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title: ATI_MarsXT_M2_MEM IF

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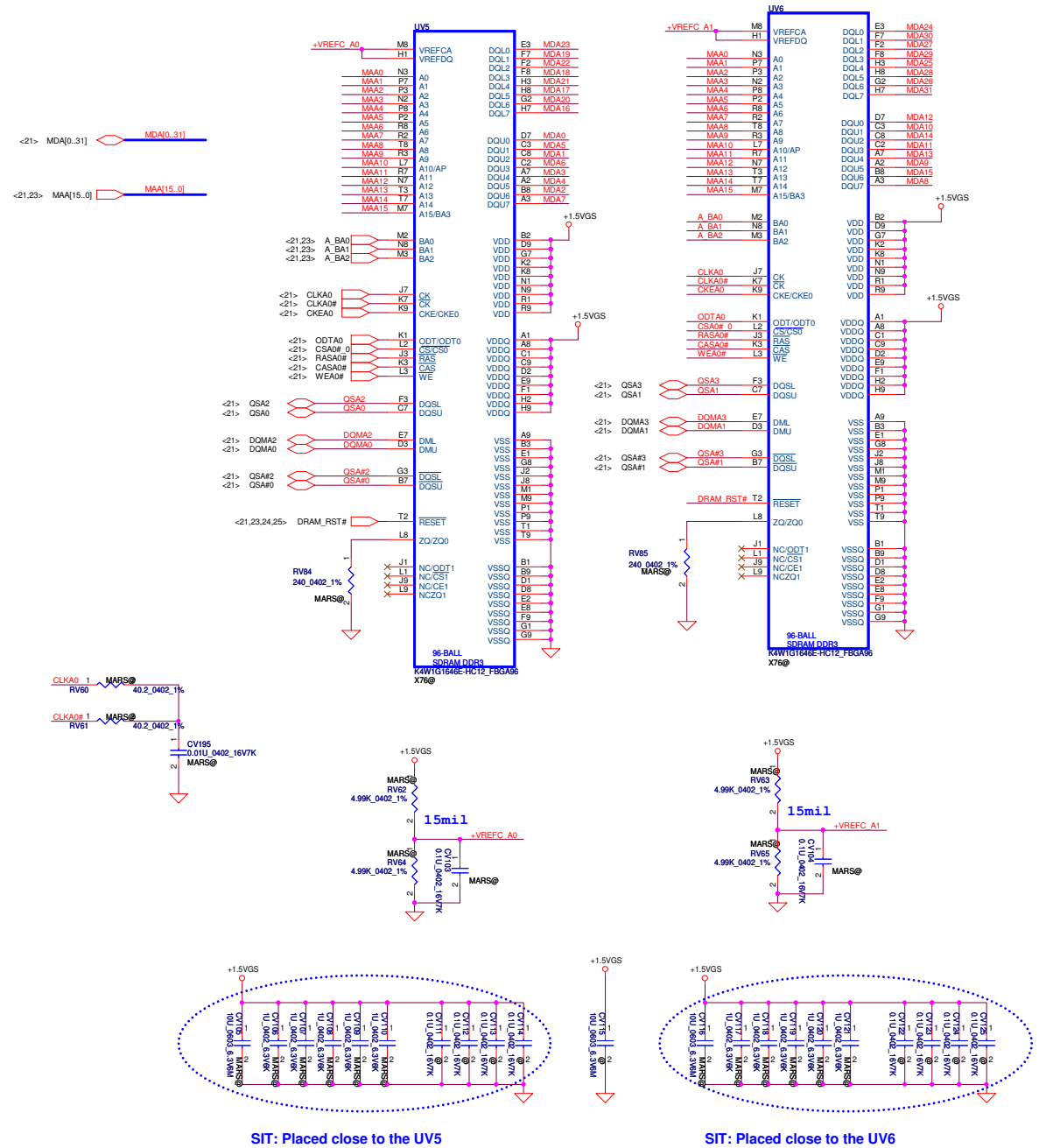

SIT: Placed close to the UV5

SIT: Placed close to the UV6

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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B0

Size: C | Document Number: VALGD MB L | Rev: 0.1

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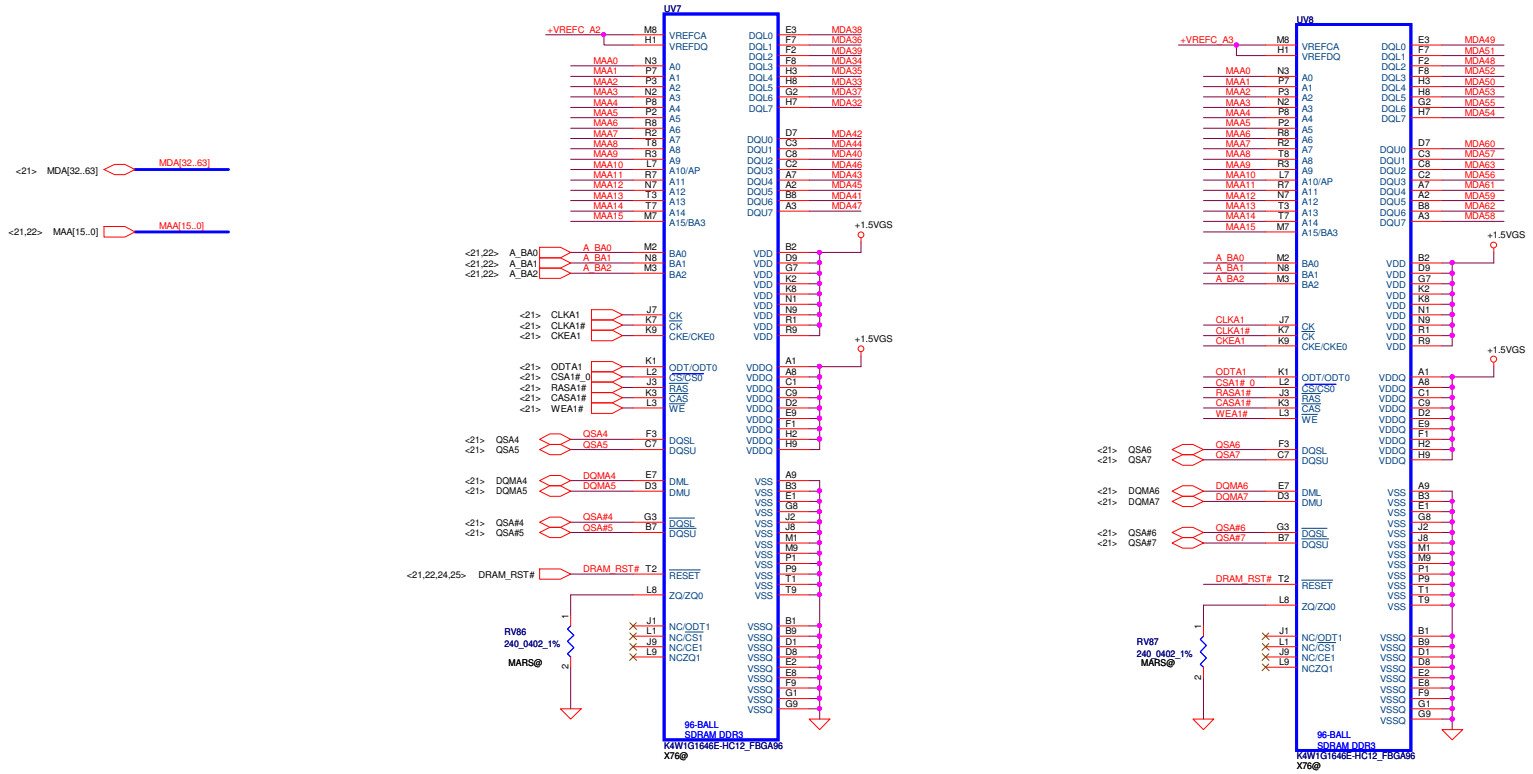

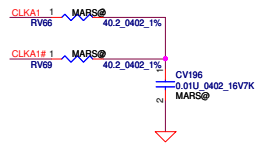

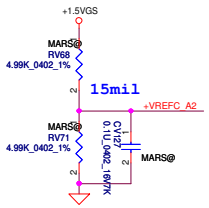

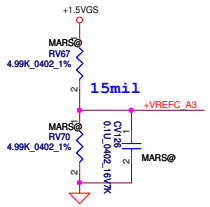

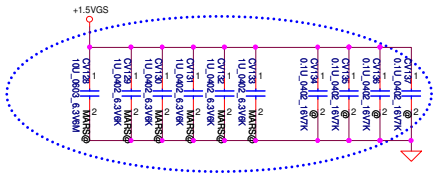

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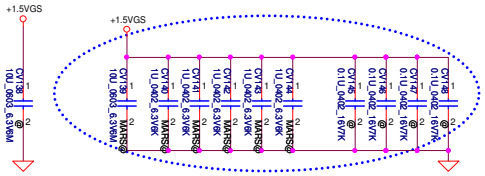

SIT: Placed close to the UV8

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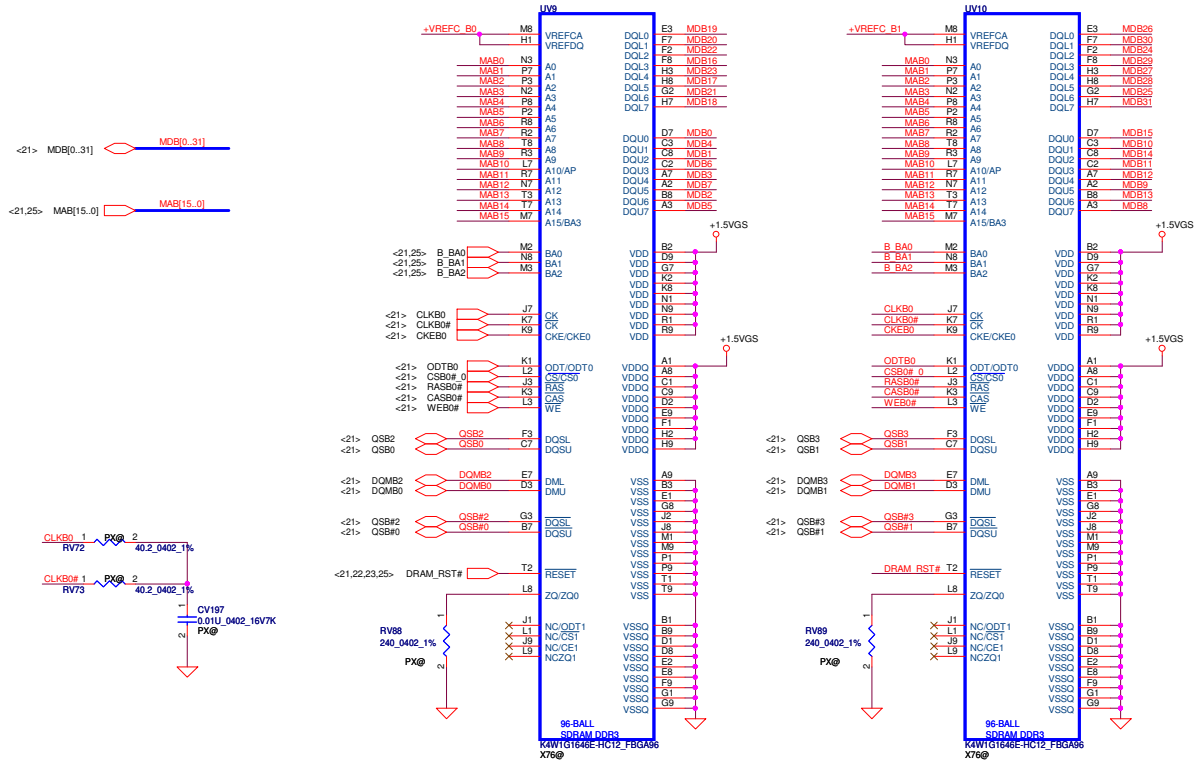
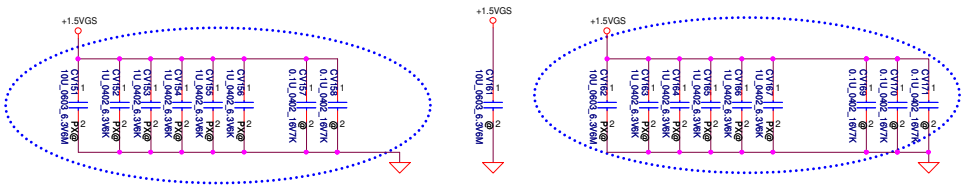
Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B1

Size	Document Number	Rev
C	VALGD MB L	0.1

Date: Friday, April 12, 2013 | Sheet 23 of 57





SIT: Placed close to the UV9

SIT: Placed close to the UV10

Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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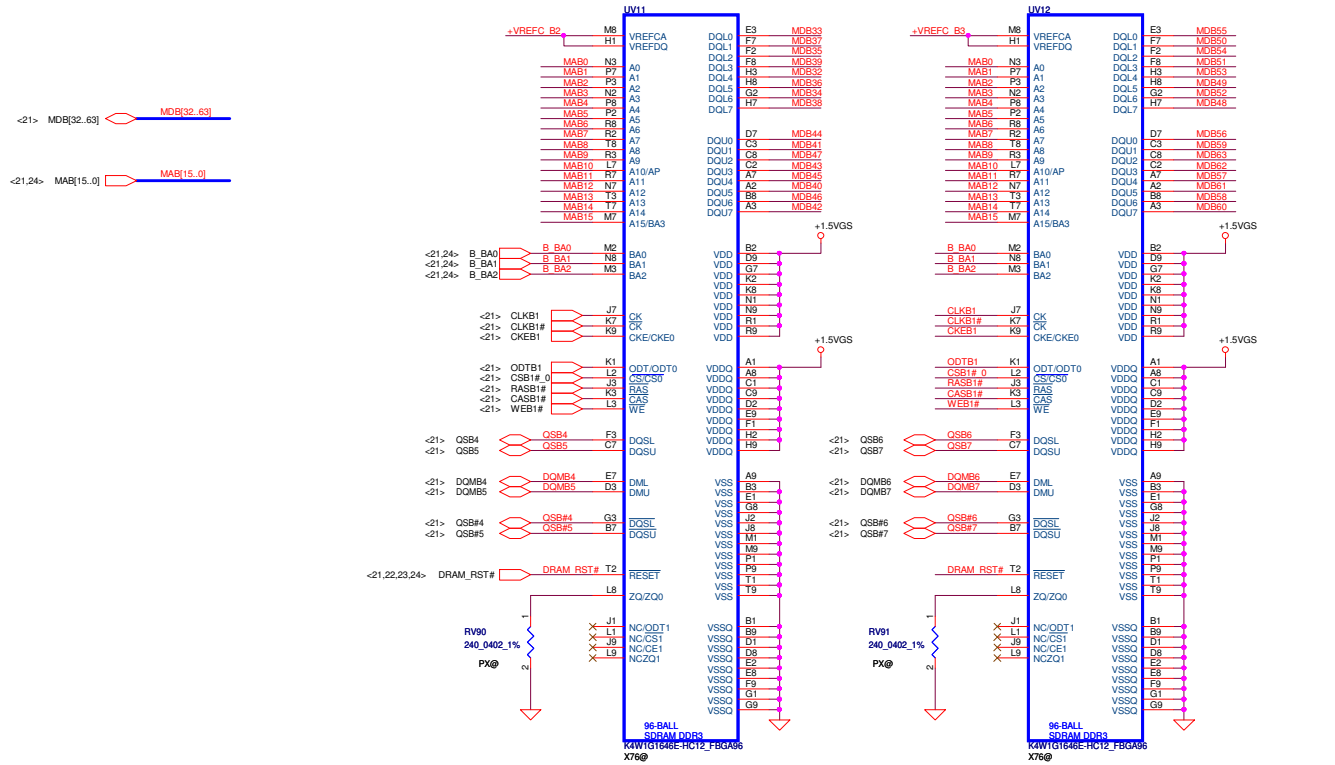
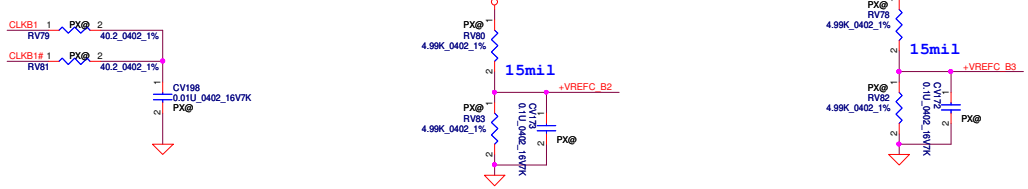
Compal Electronics, Inc.

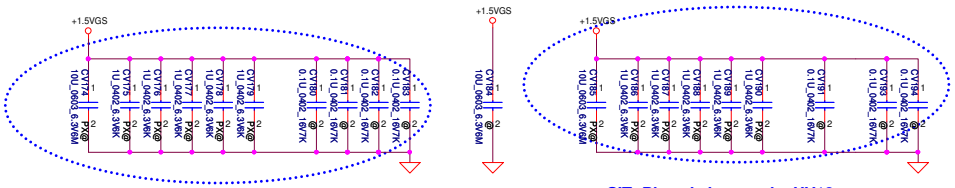
Title: ATI_Whistler_M2_VRAM_A0

Size: C | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 24 of 57







SIT: Placed close to the UV11

SIT: Placed close to the UV12

Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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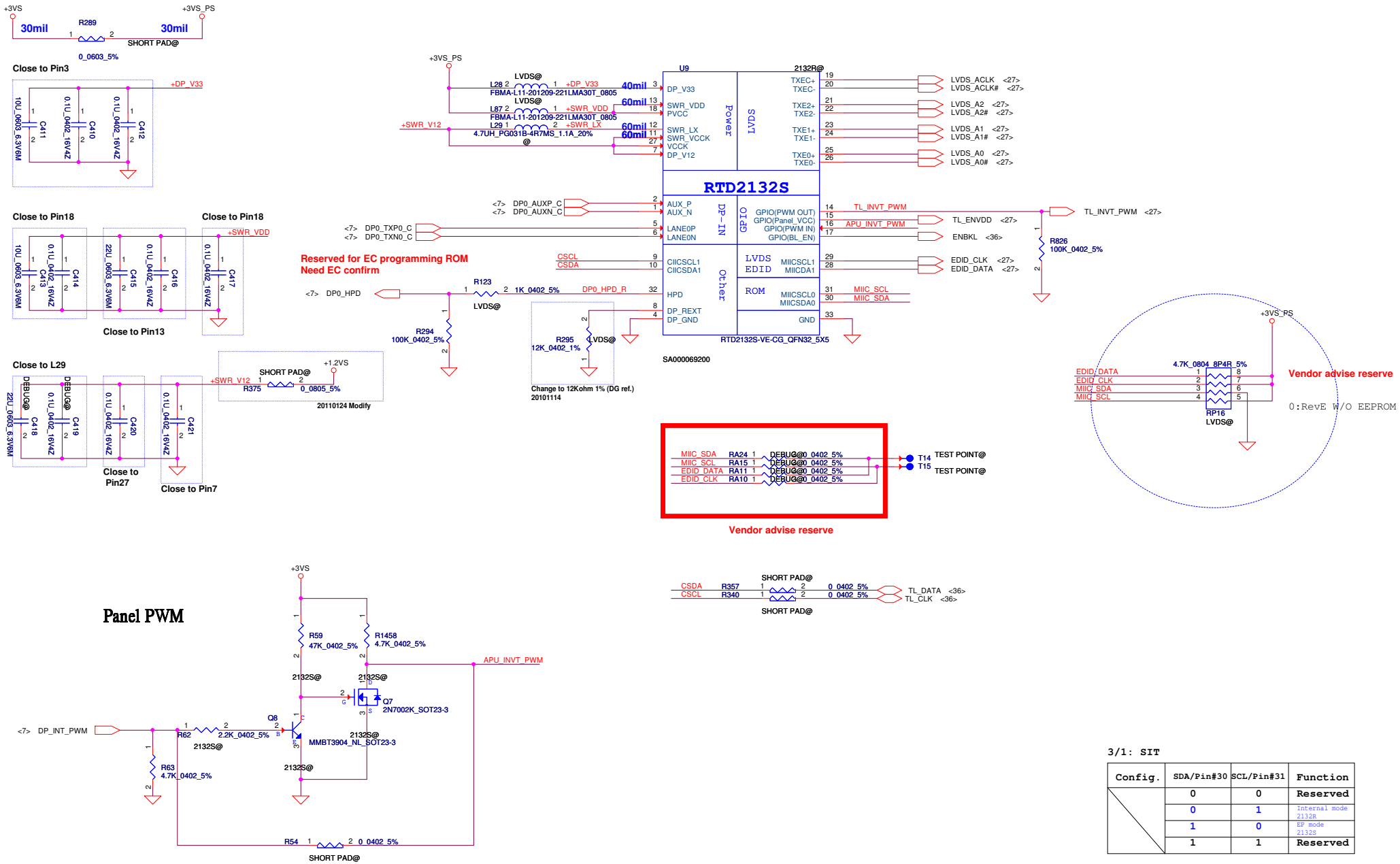
Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A1

Size: C | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 25 of 57



3/1: SIT

Config.	SDA/Pin#30	SCL/Pin#31	Function
	0	0	Reserved
	0	1	Internal mode 2132R
	1	0	EP mode 2132S
	1	1	Reserved

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/11/13	Deciphered Date 2013/11/12	Title: LVDS Translator - RTD2132S
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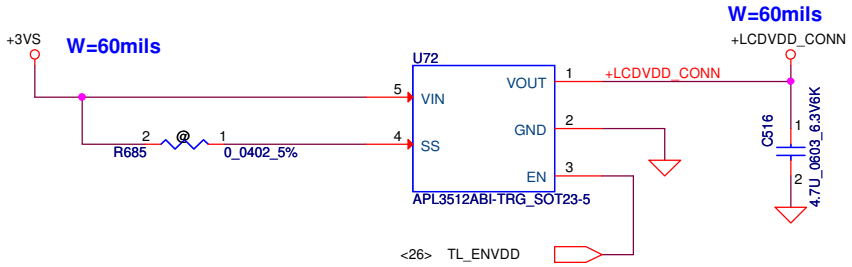
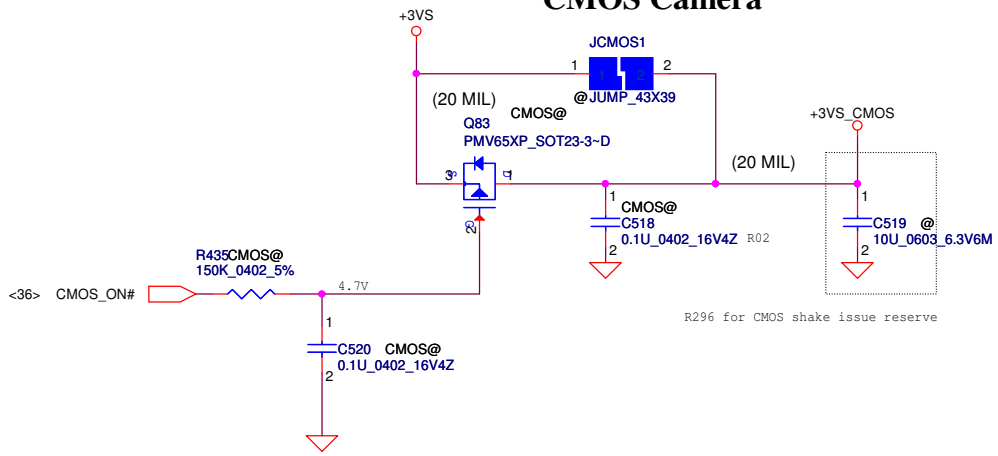
			Date: Friday, April 12, 2013; Sheet 26 of 57

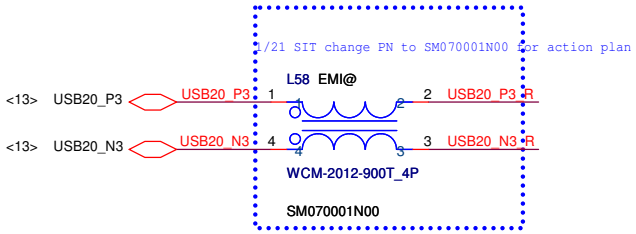
LCD POWER CIRCUIT

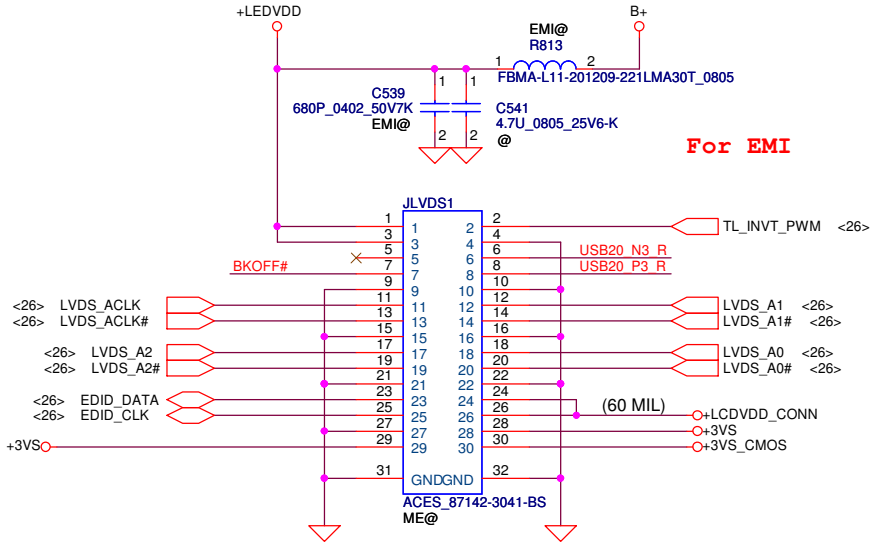


CMOS Camera



VGA LCD/PANEL BD. Conn.





Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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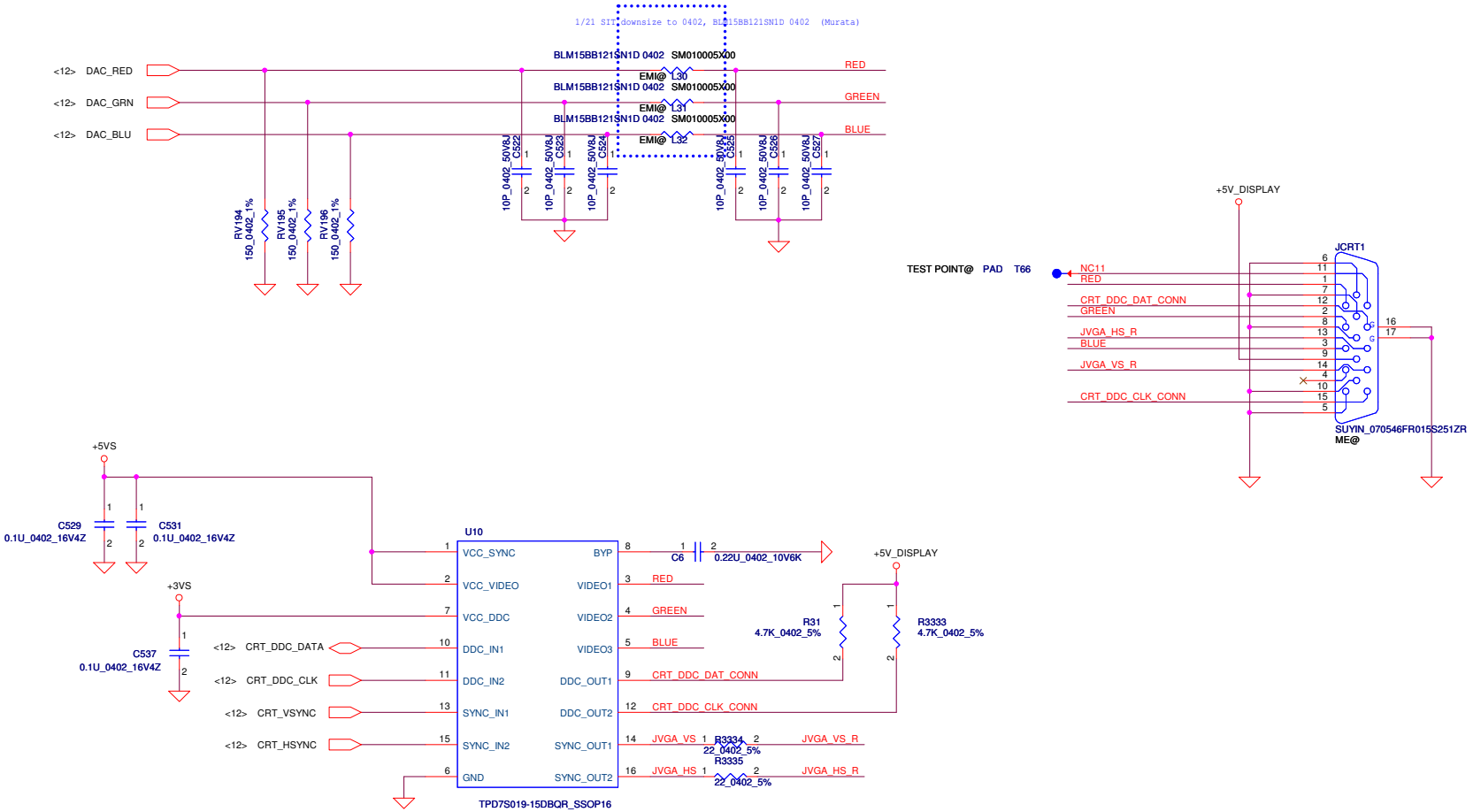
Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size: Custom | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 27 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title: CRT Connector
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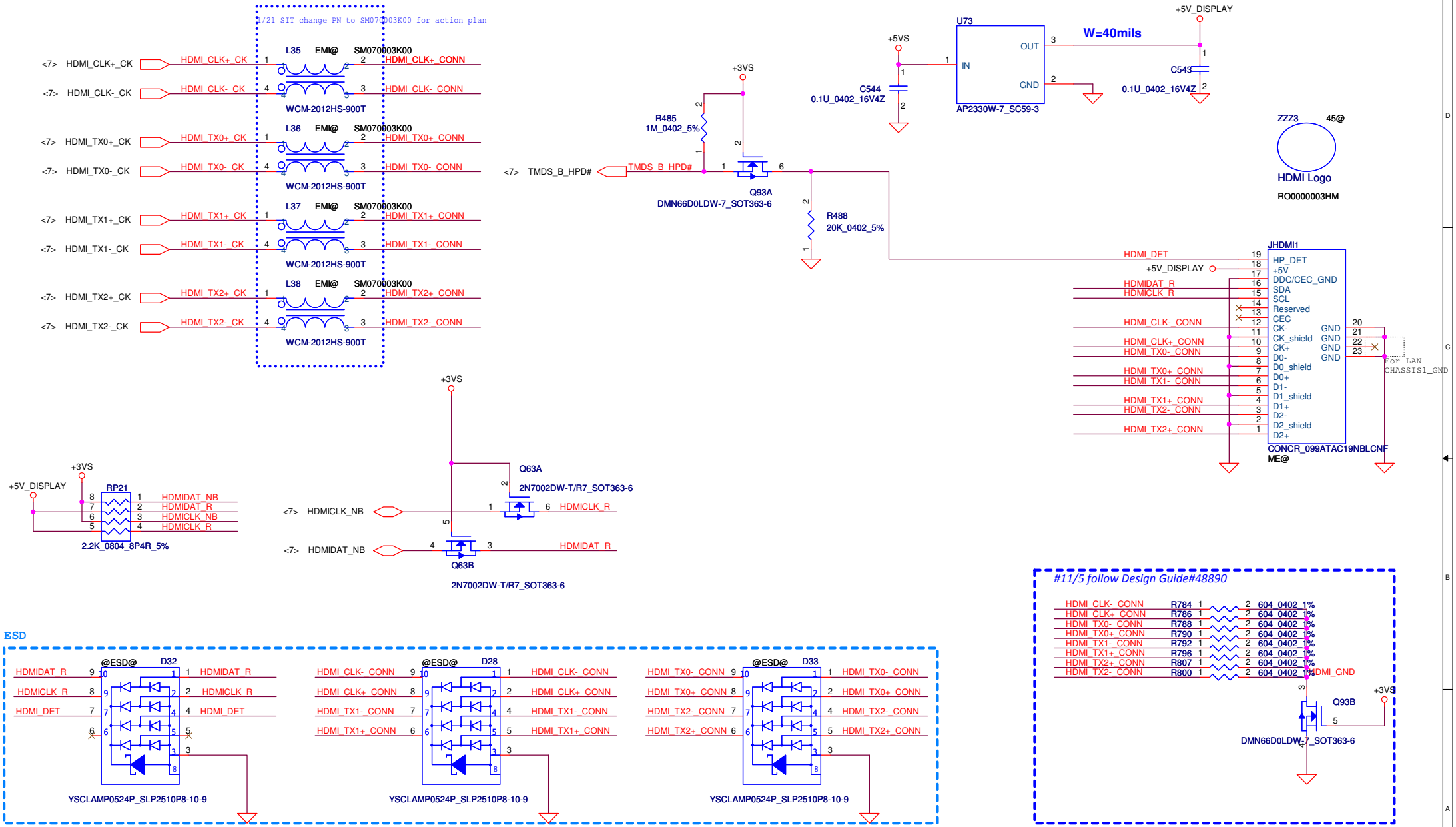
				Date: Friday, April 12, 2013 / Sheet 28 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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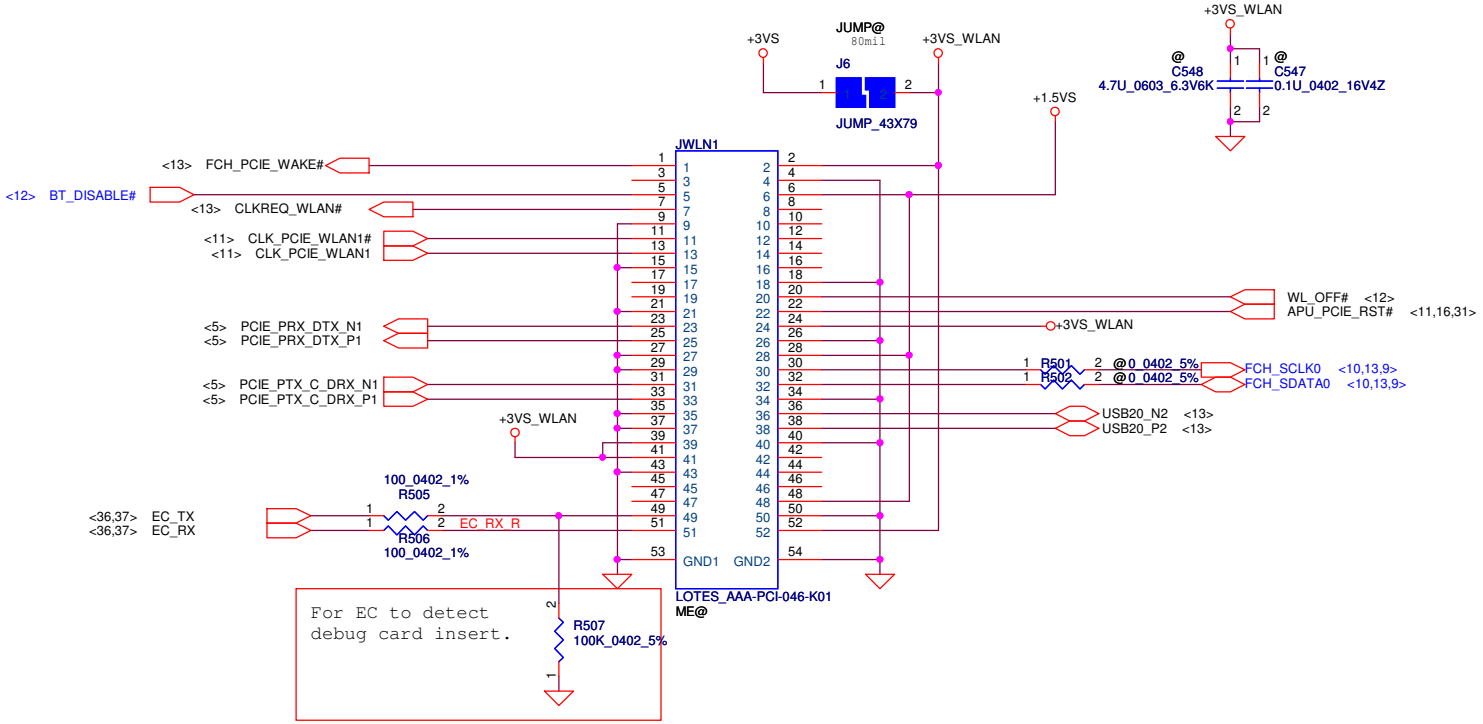
Compal Electronics, Inc.

Title: **HDMI CONN**

Size: B | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 29 of 57

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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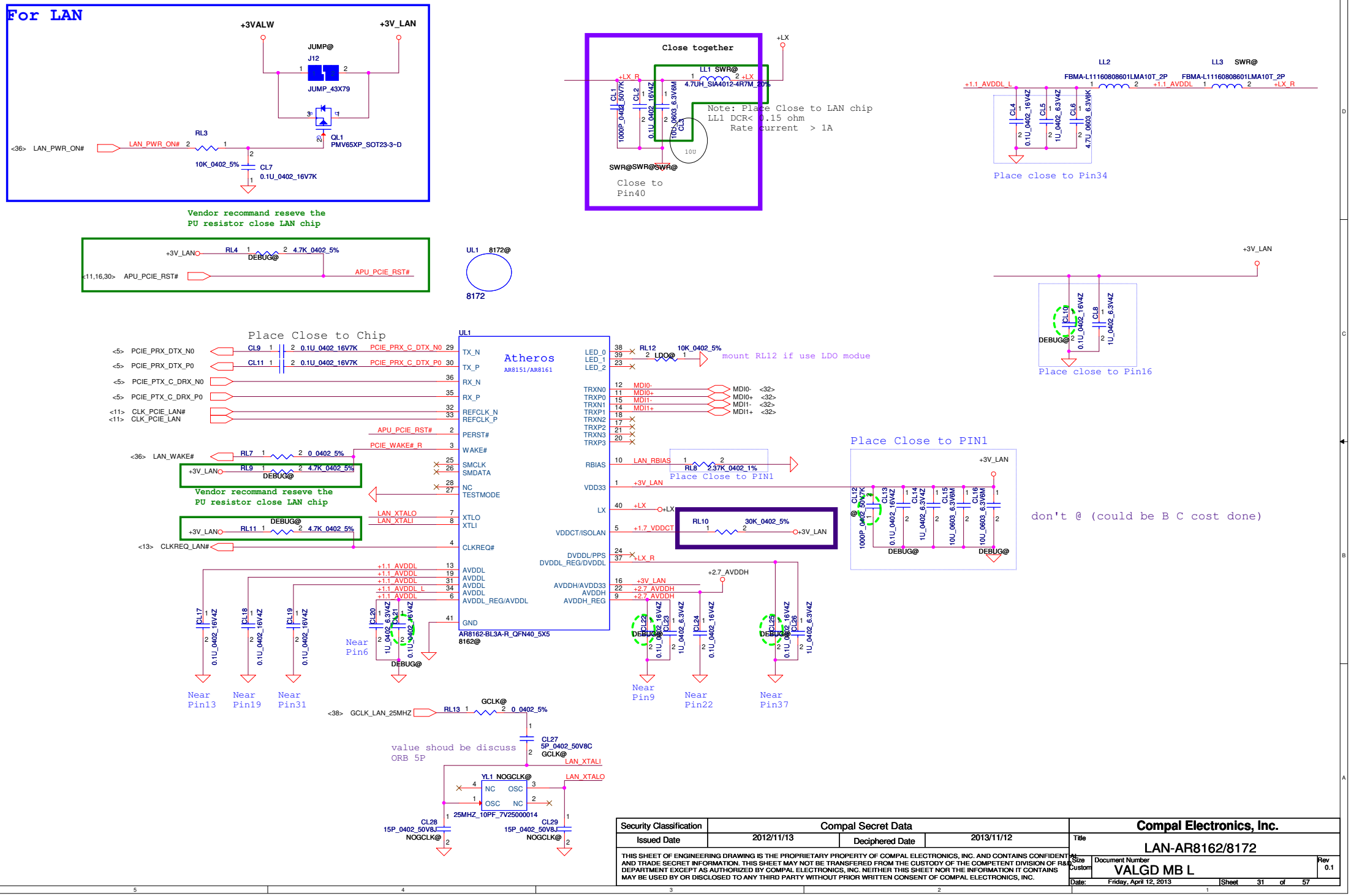
Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

Size: | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 30 of 57



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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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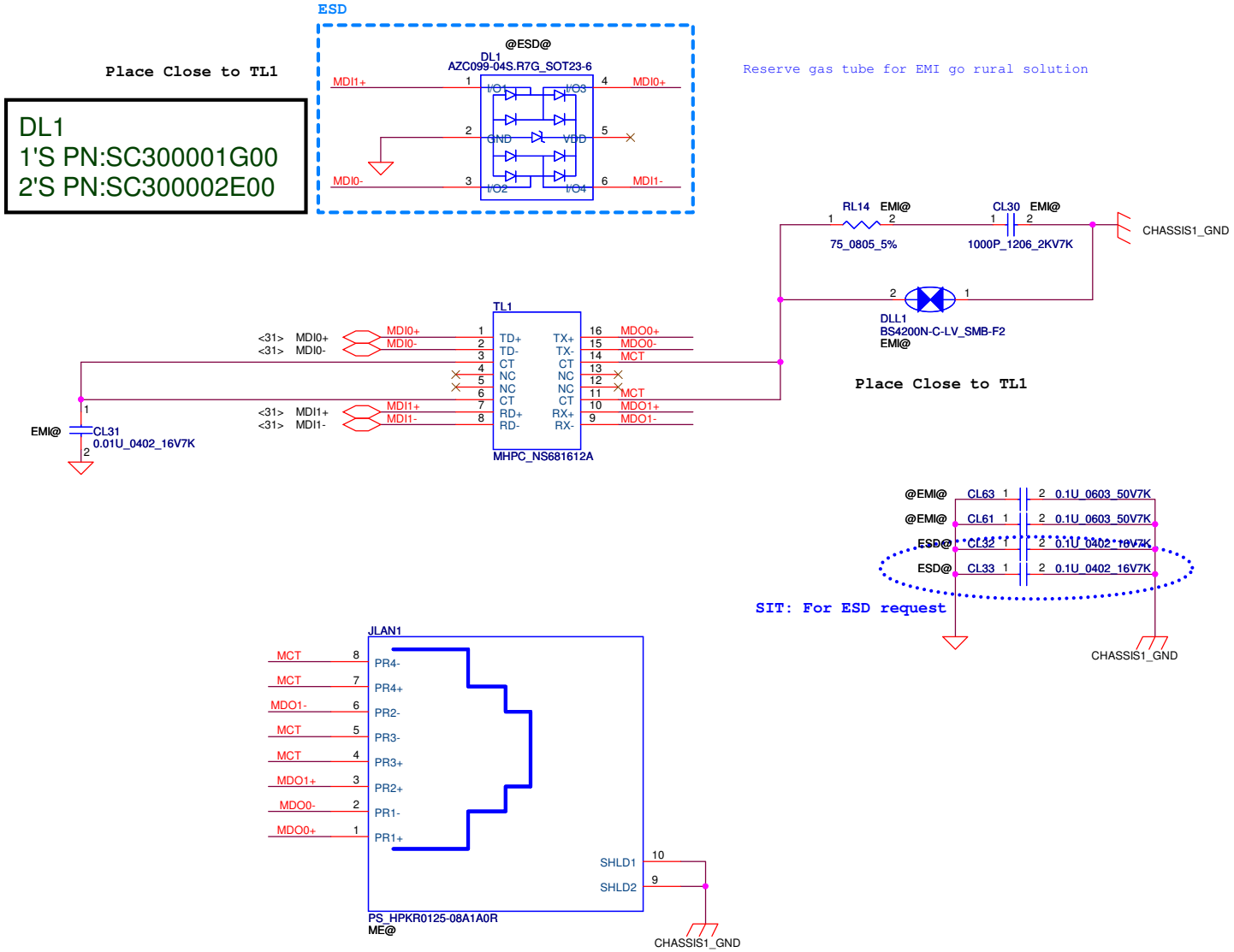
Compal Electronics, Inc.

Title: LAN-AR8162/8172

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 31 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/11/13	Deciphered Date	2013/11/12	Title: LAN_Transformer
				Size: B; Document Number: VALGD MB L; Rev: 0.1
				Date: Friday, April 12, 2013; Sheet 32 of 57

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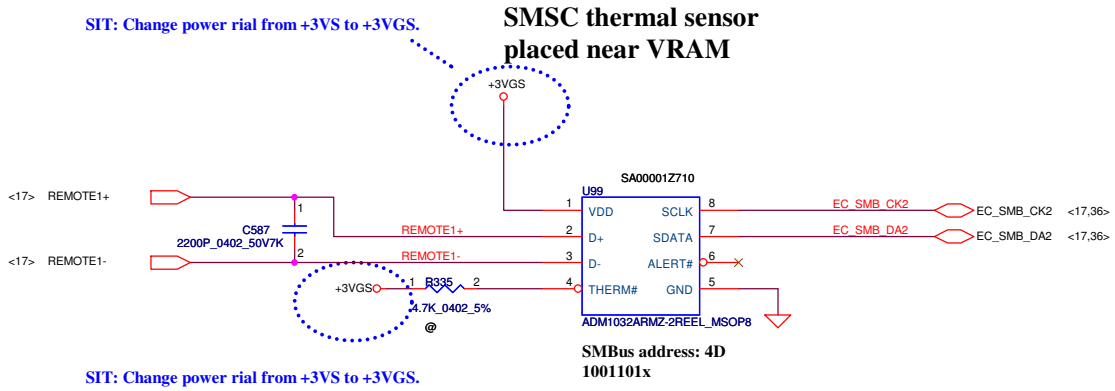
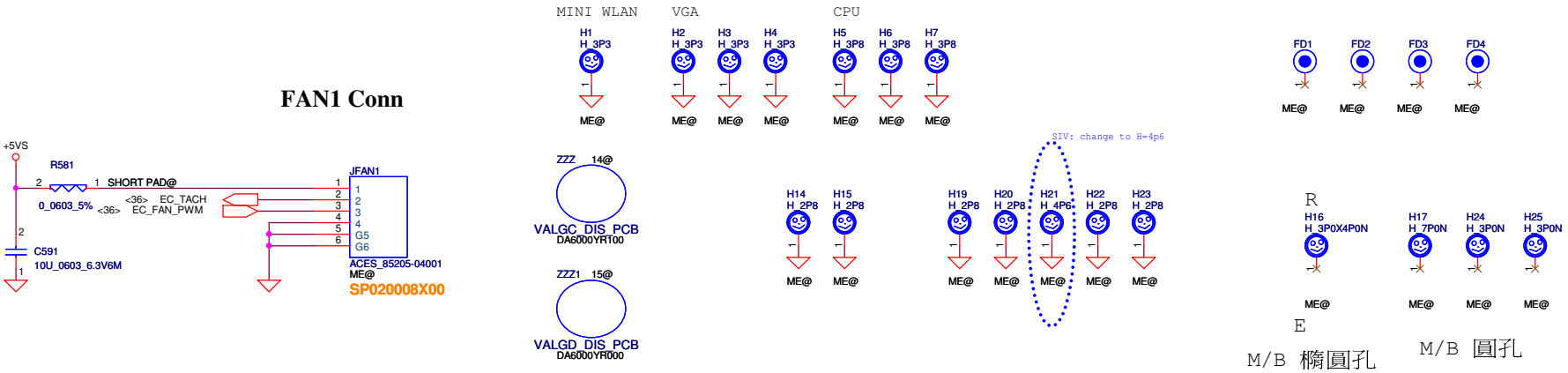
2 Channel





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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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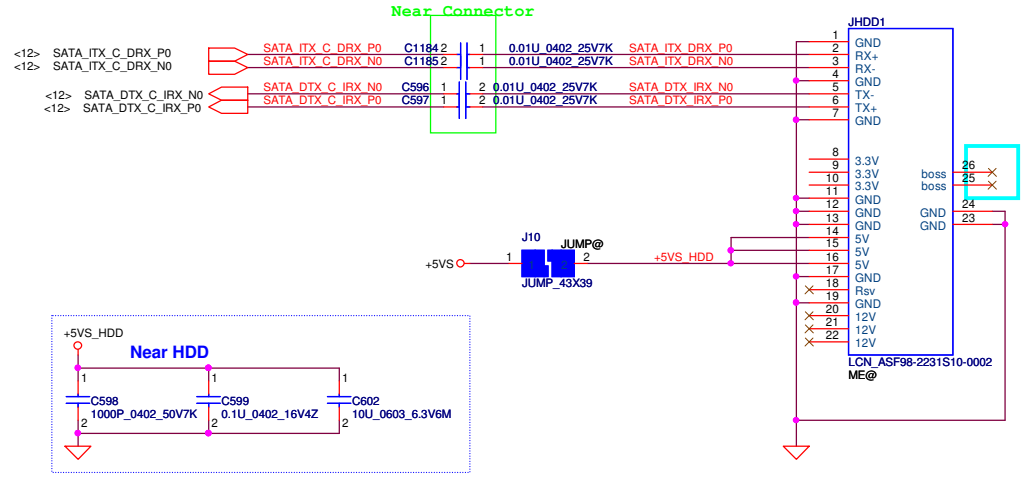
Compal Electronics, Inc.

Title: **Fintek-Thermal IC/FAN/screw**

Size: Custom | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 33 of 57

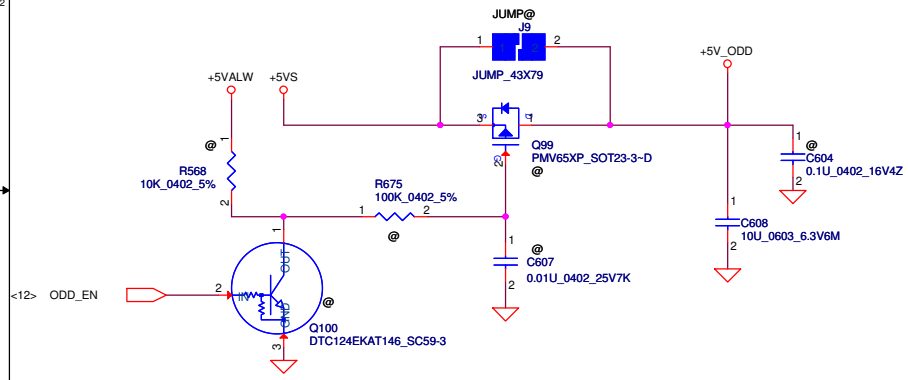
SATA HDD Conn.



SIT: 3/1 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)

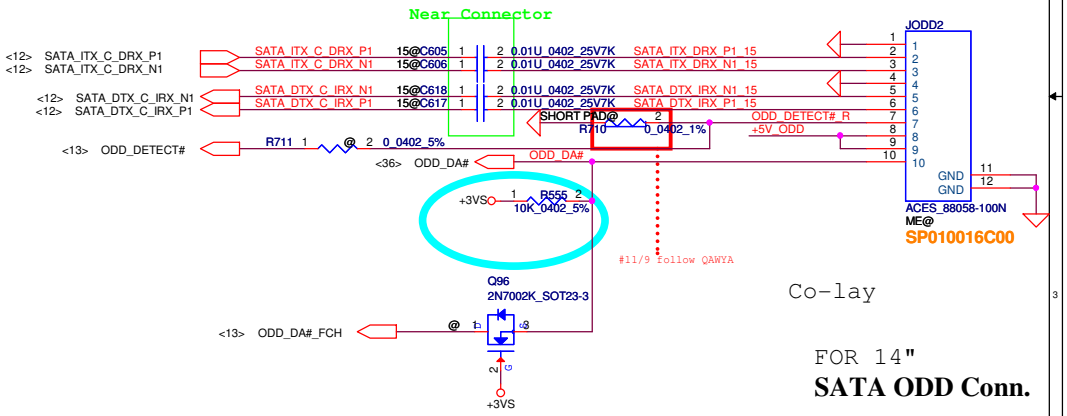
ODD Power Control

Per-MP: 4/3 un-pop ODD power control circuits



FOR 15"

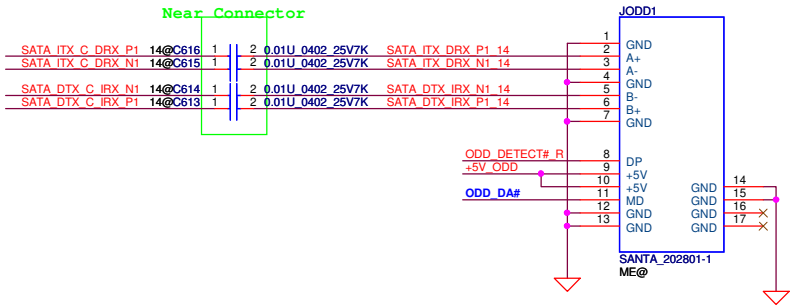
SATA ODD FFC Conn.



Co-lay

FOR 14"

SATA ODD Conn.



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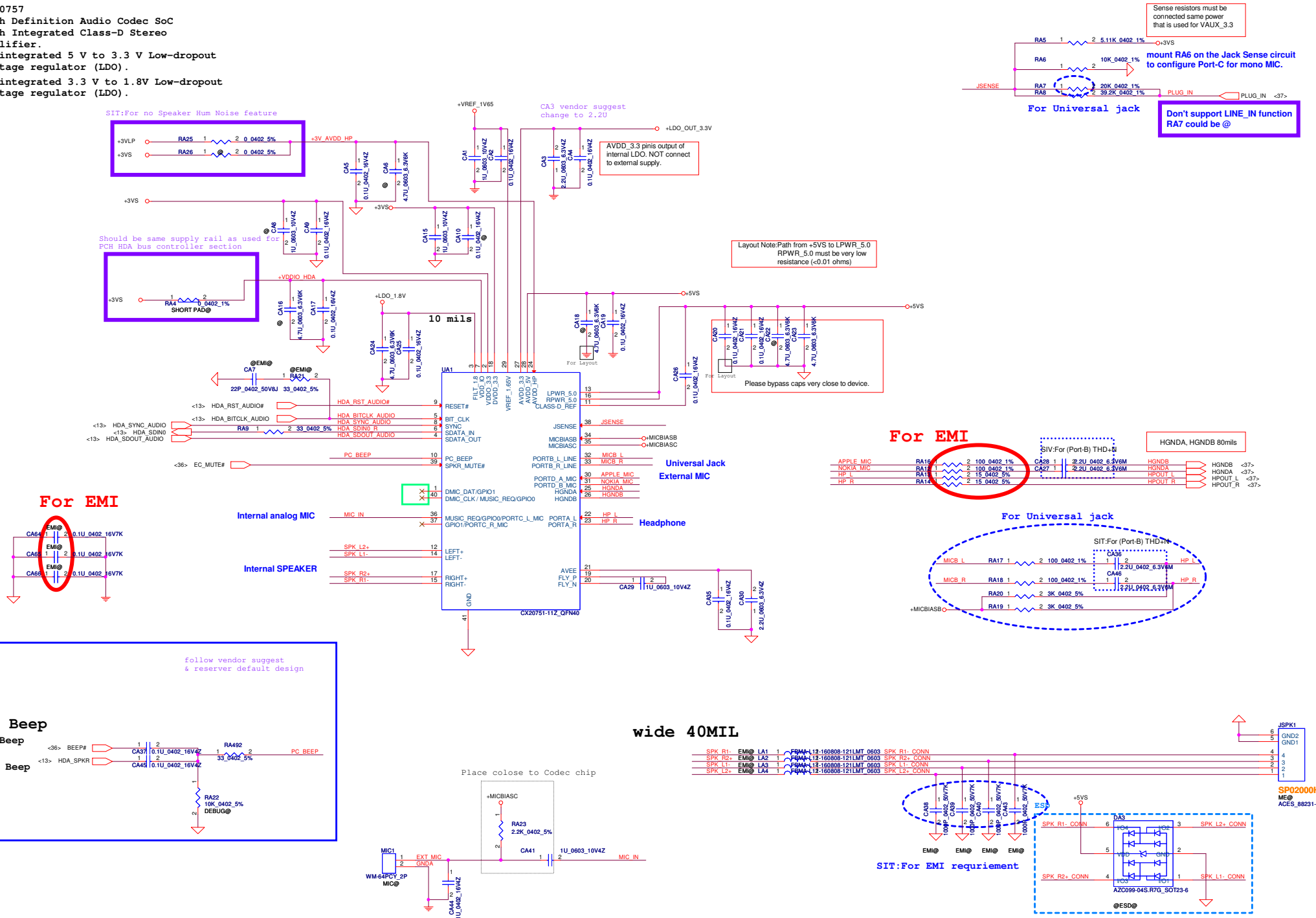
Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size: Custom | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 34 of 57

CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



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Issued Date	2012/11/13	Deciphered Date	2013/11/12

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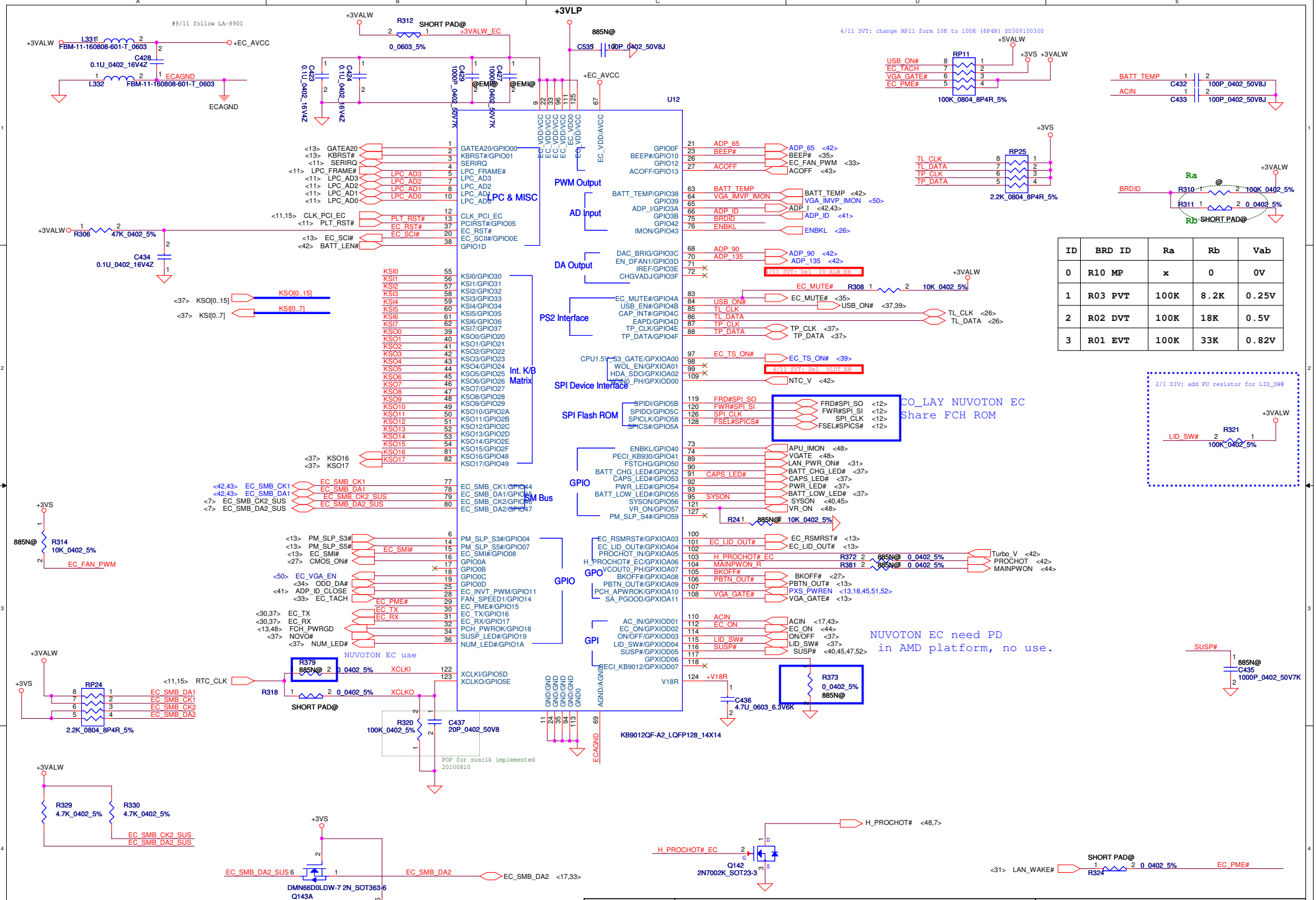
Compal Electronics, Inc.

Title: CX20757-11Z Codec

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 35 of 57



ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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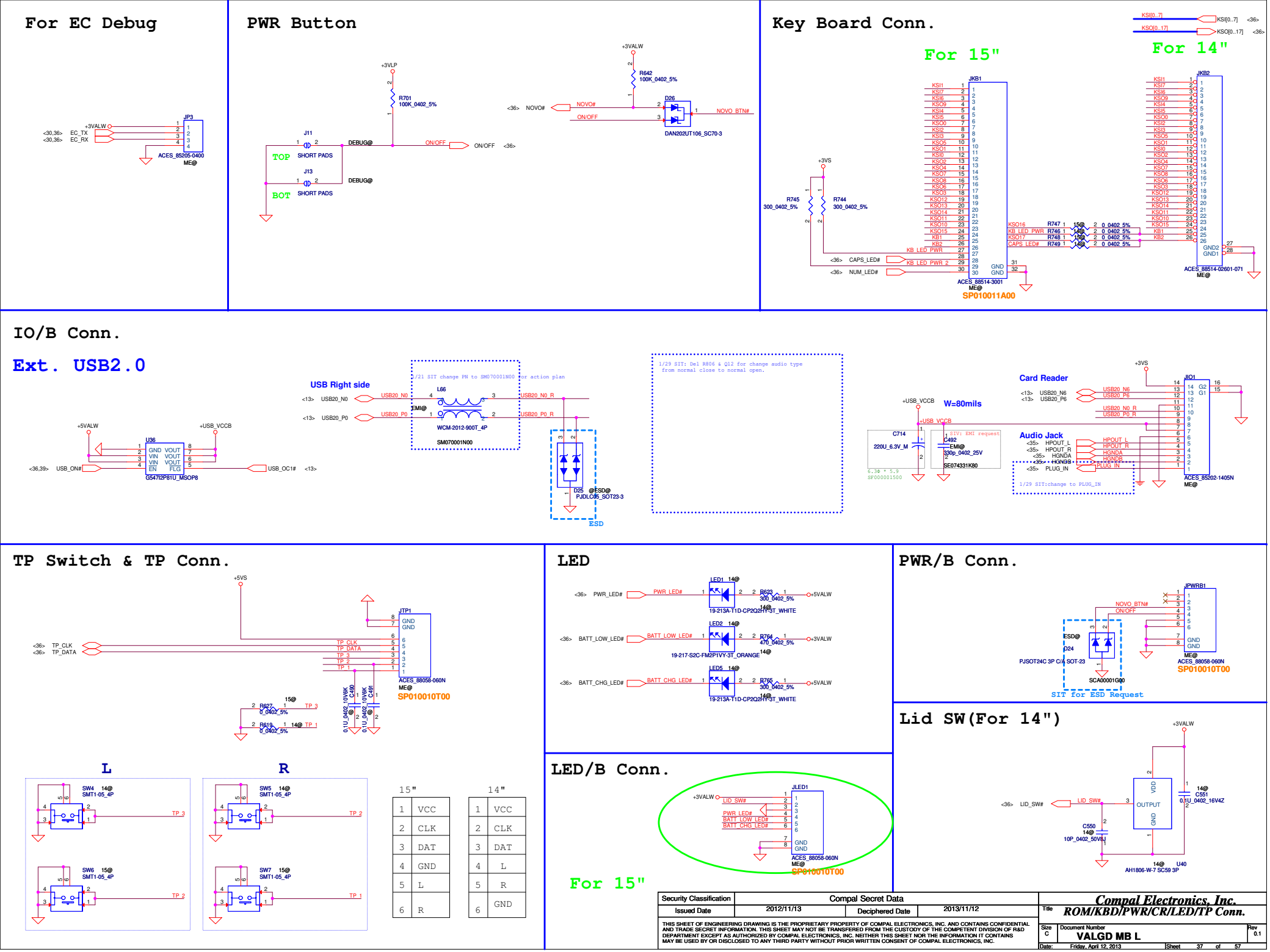
Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size: B/25 Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 36 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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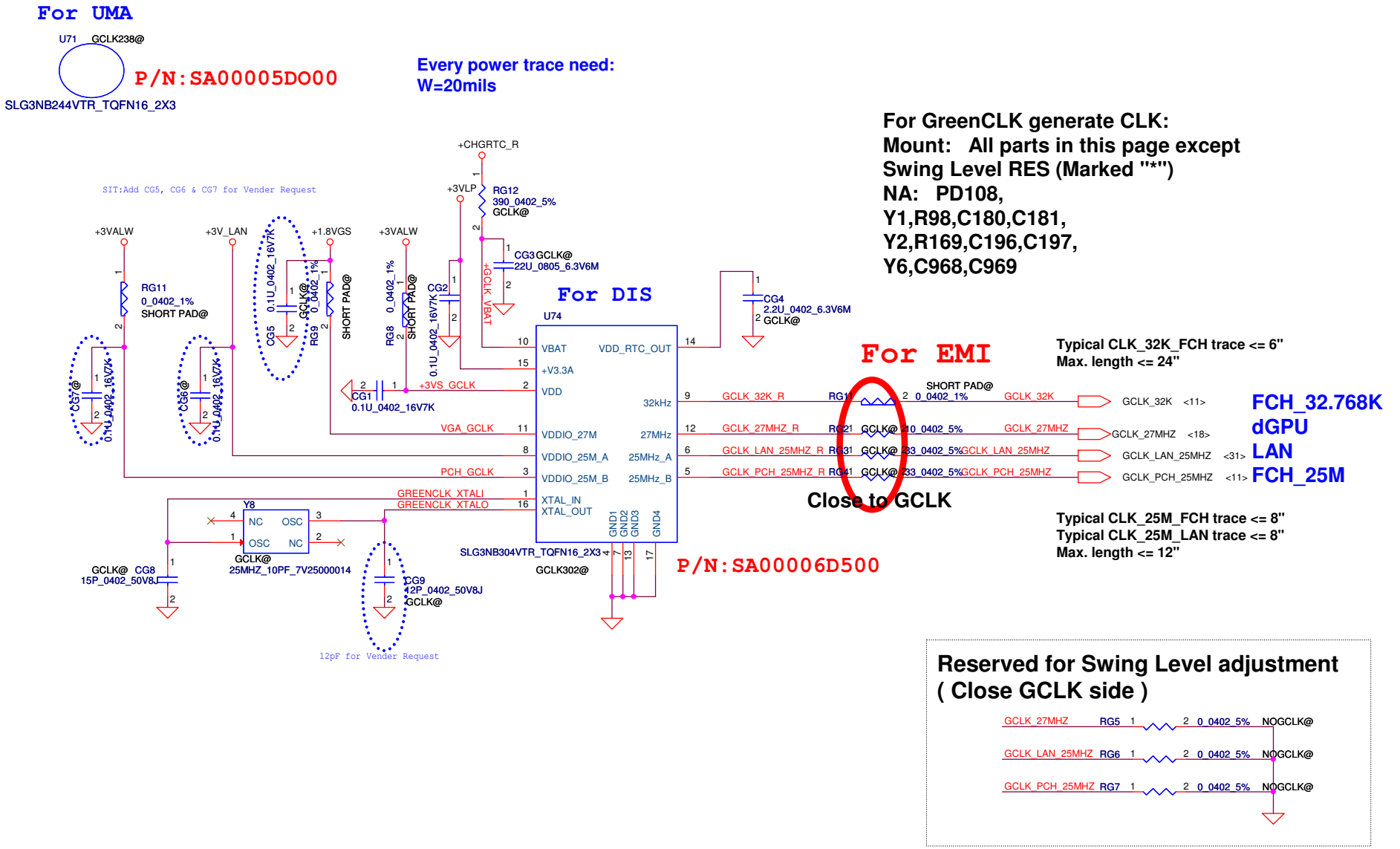
Compal Electronics, Inc.

Title: ROM/KBD/PWR/CR/LED/TP Conn.

Size: C | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 37 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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Compal Electronics, Inc.

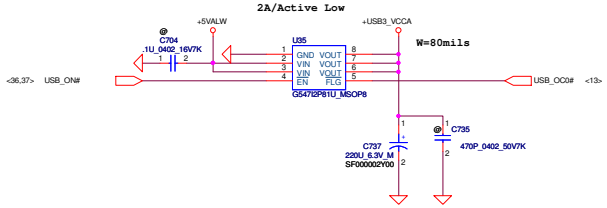
Title: GCLK

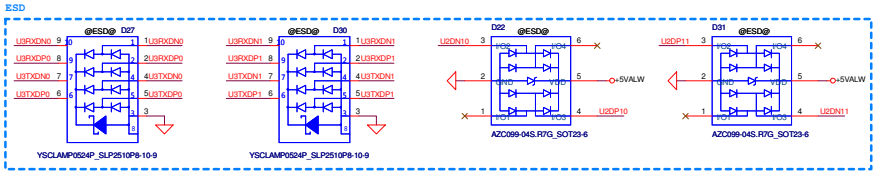
Size: B | Document Number: VALGD MB L | Rev: 0.1

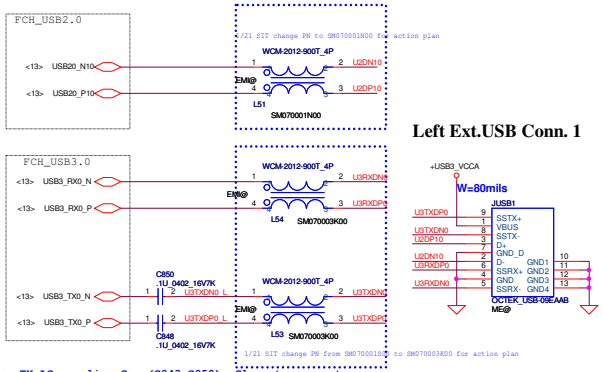
Date: Friday, April 12, 2013 | Sheet 38 of 57

Touch Screen

USB3.0

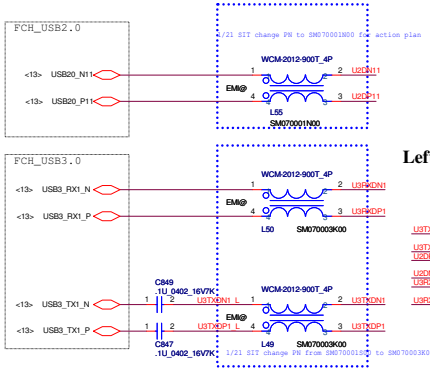




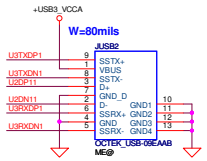


Place TX AC coupling Cap (C843~C850). Close to connector

Left Ext.USB Conn. 1



Left Ext.USB Conn. 2



Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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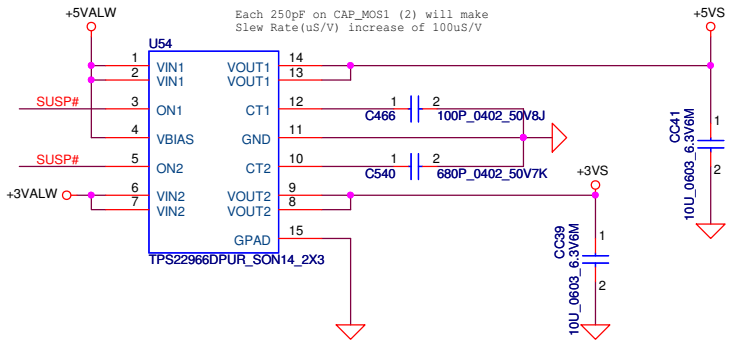
Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

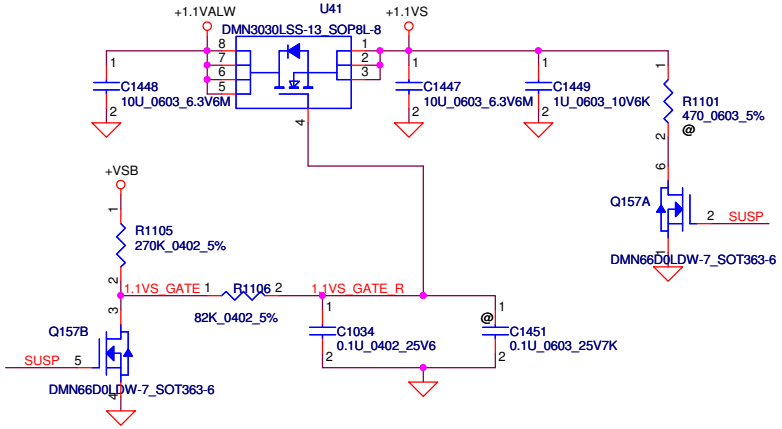
Custom | Document Number: VALGD MB L | Rev 0.1

Date: Friday, April 12, 2013 | Sheet 39 of 57

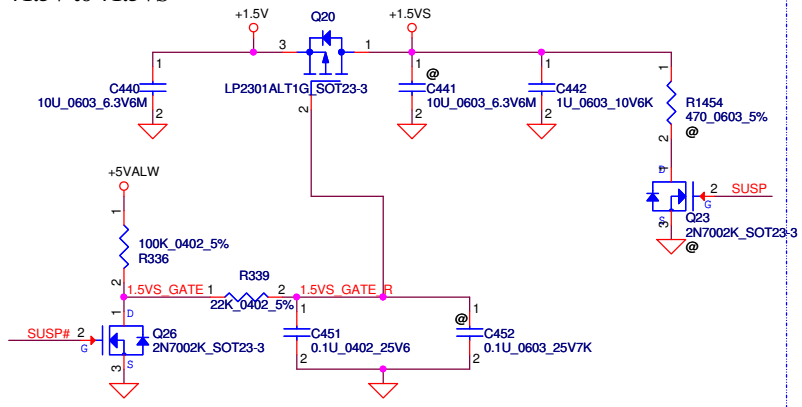
+5VALW to +5VS combine with +3VALW to +3VS

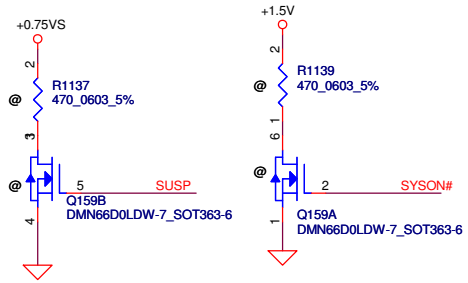


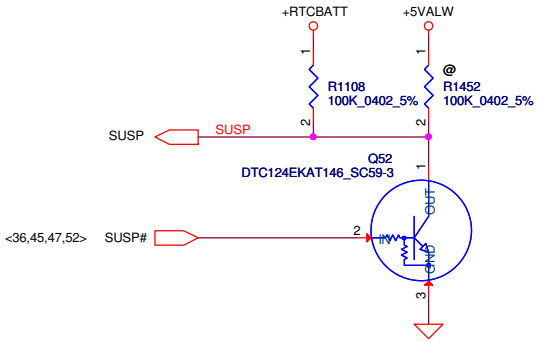
+1.1VALW TO +1.1VS (5.15A)

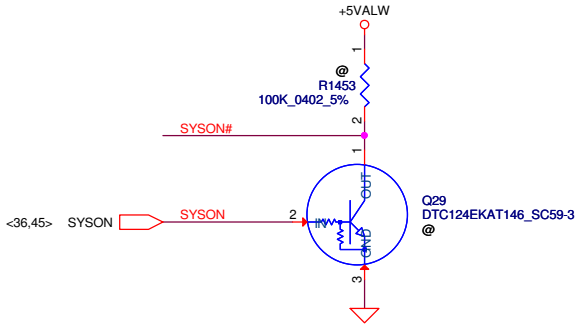


+1.5V to +1.5VS









Security Classification	Compal Secret Data		
Issued Date	2012/11/13	Deciphered Date	2013/11/12

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Compal Electronics, Inc.

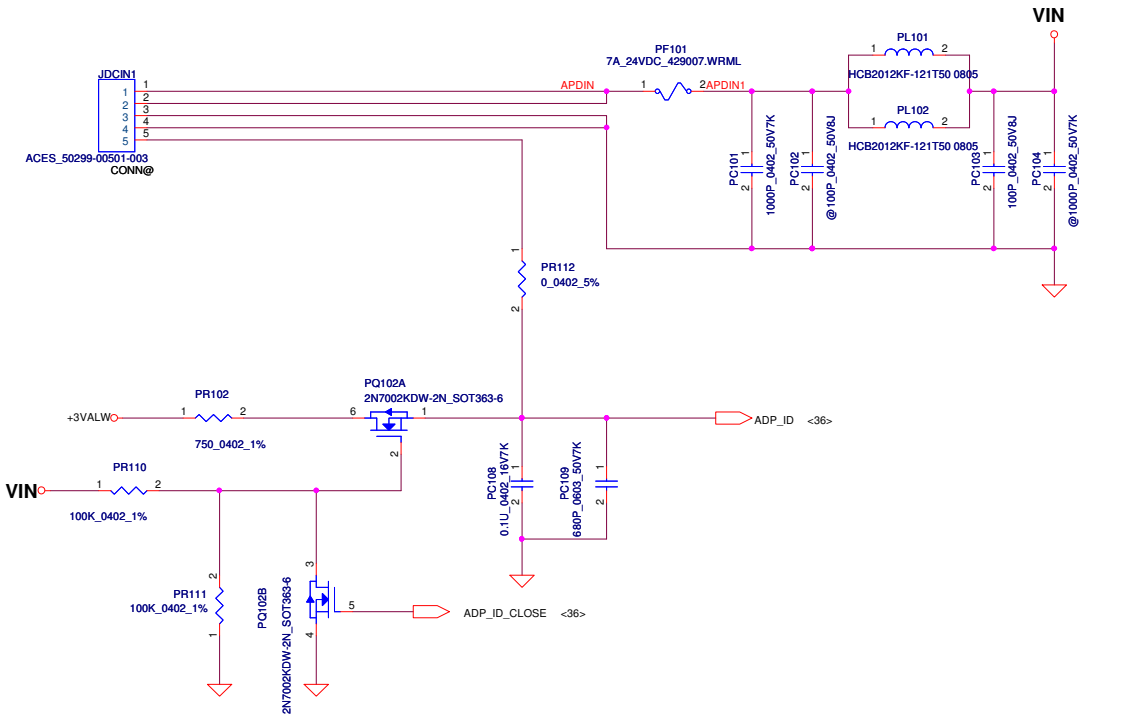
Title: DC Interface

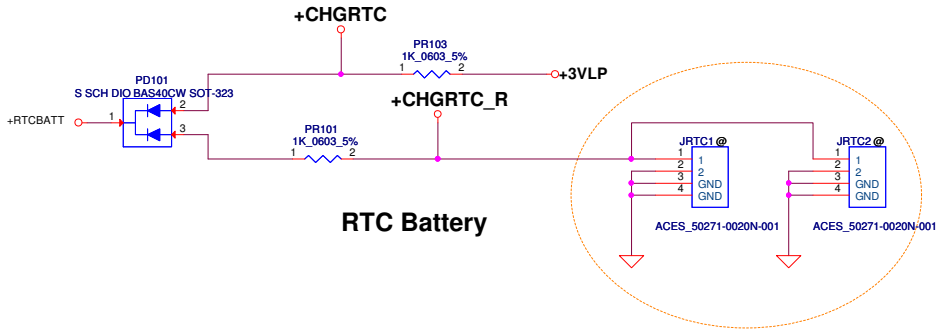
Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 40 of 57

ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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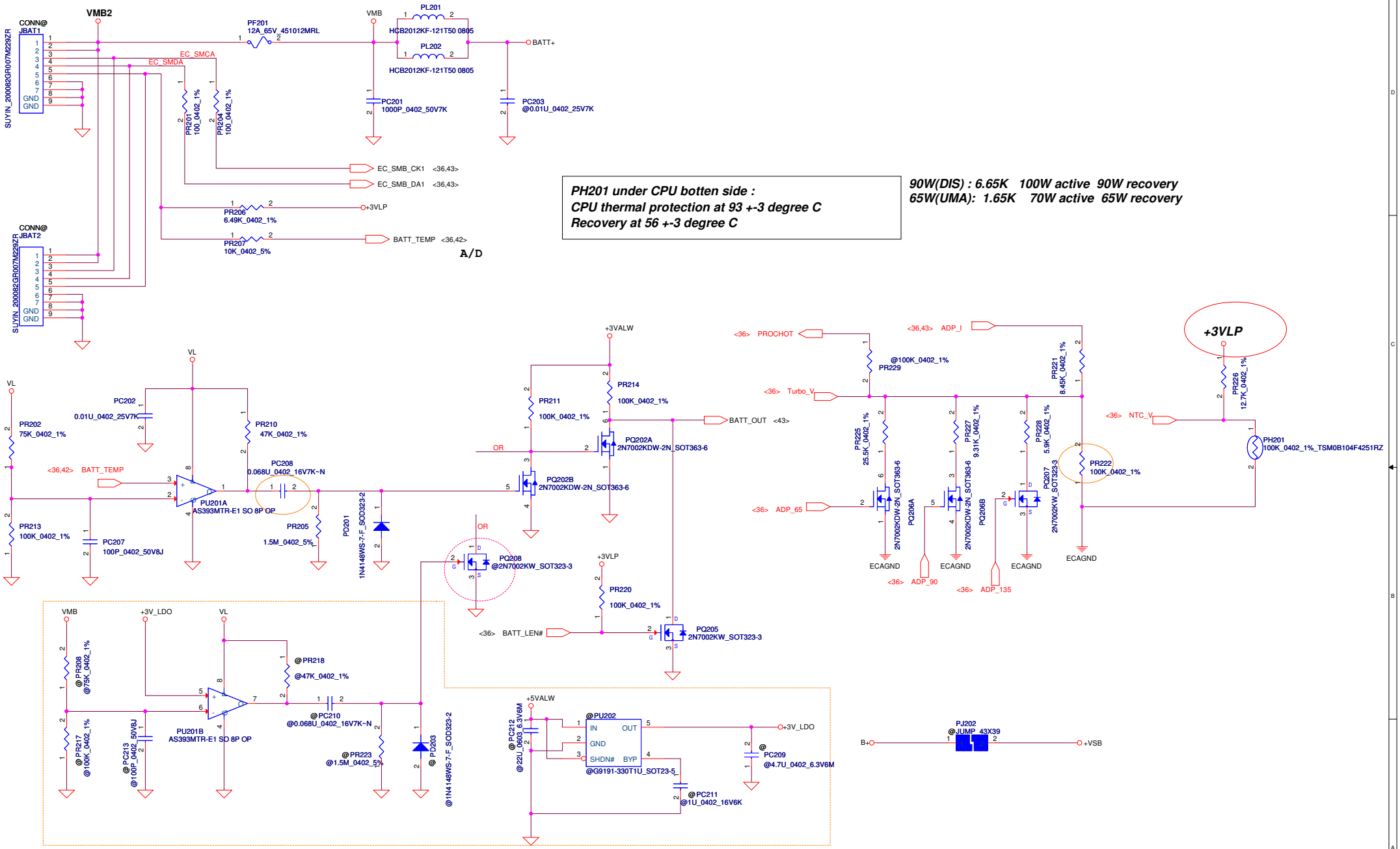
Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 41 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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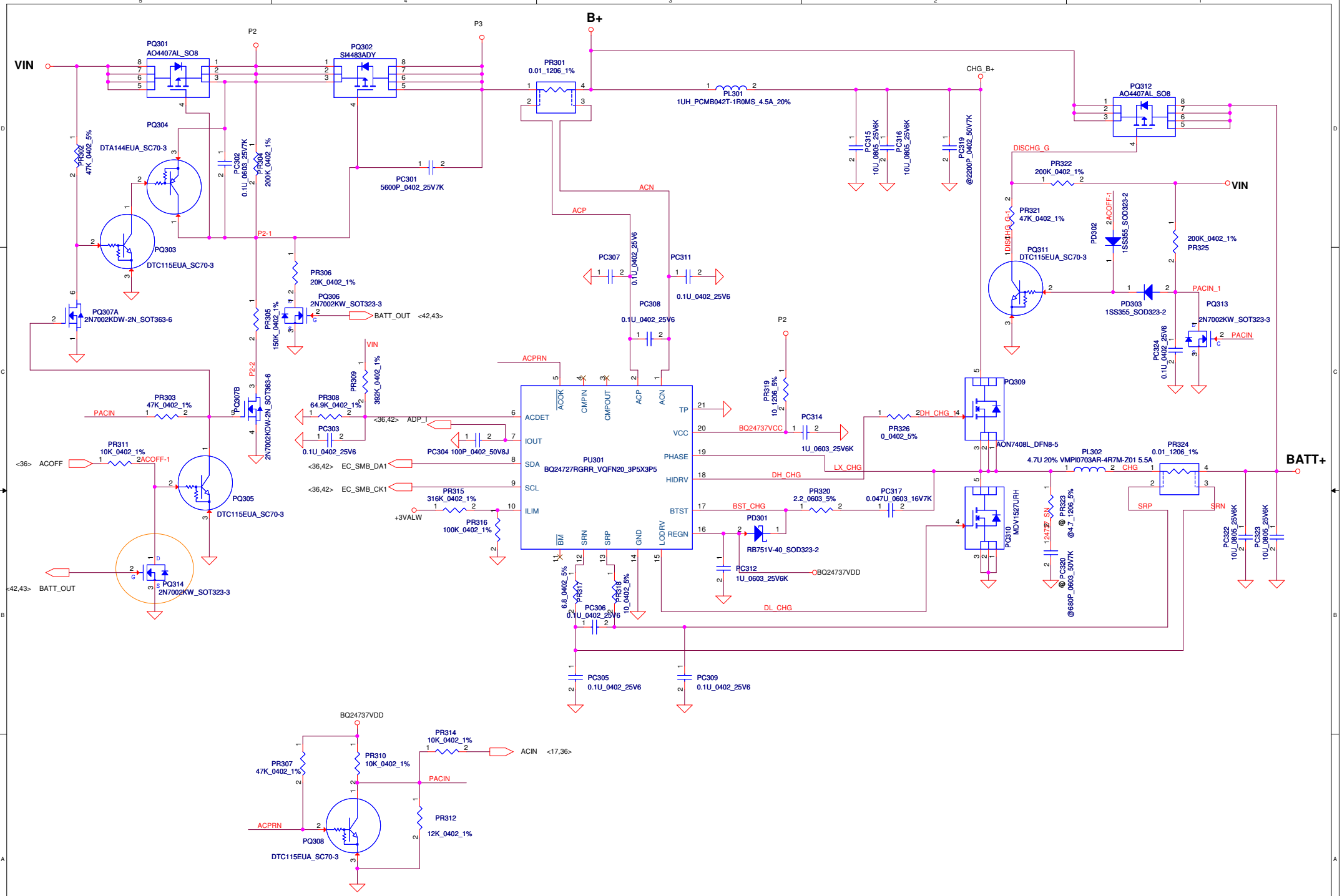
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 42 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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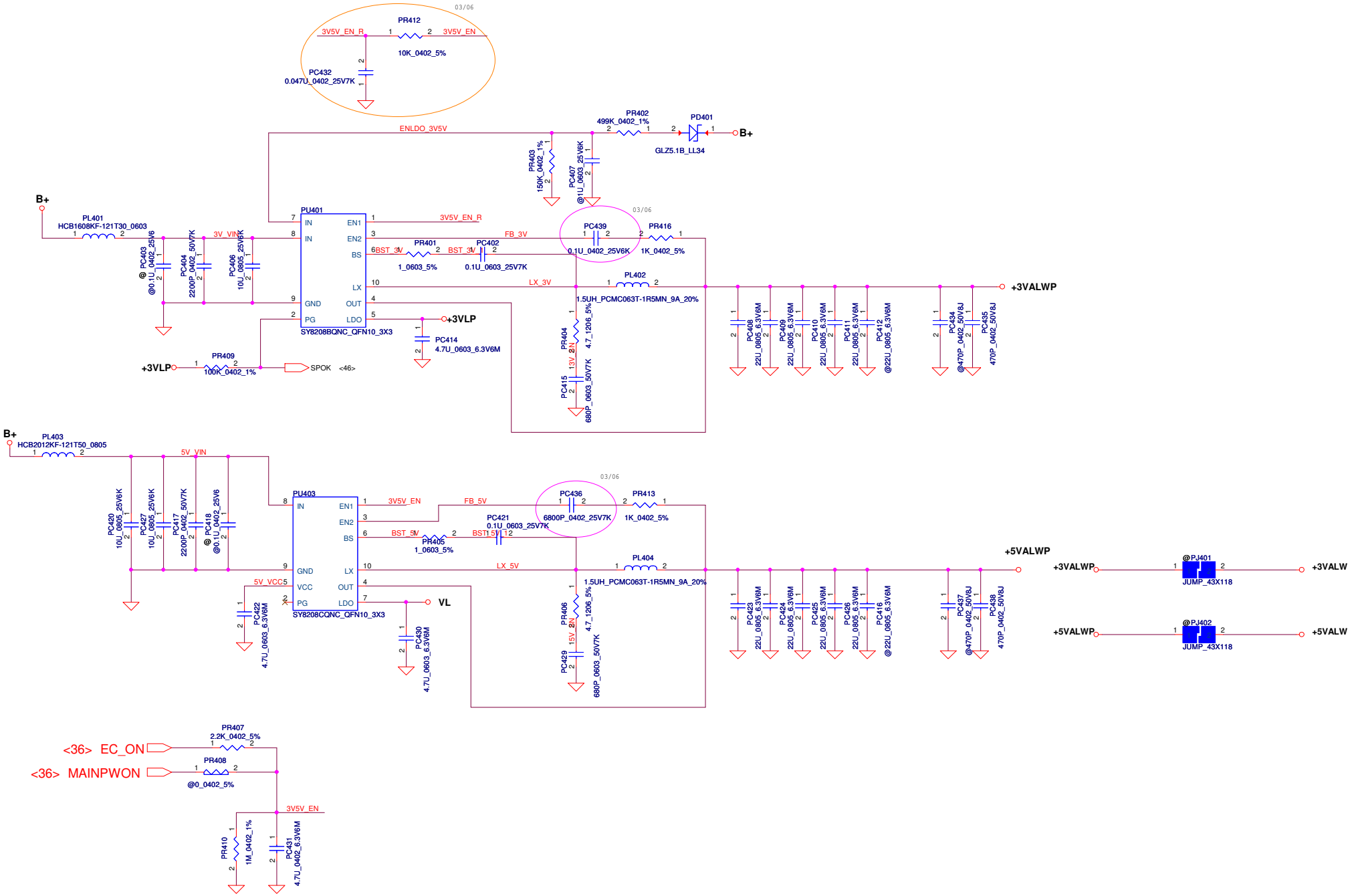
Compal Electronics, Inc.

Title: **CHARGER**

Size: Document Number: **VALGD MB L** Rev: 0.1

Date: Friday, April 12, 2013 Sheet 43 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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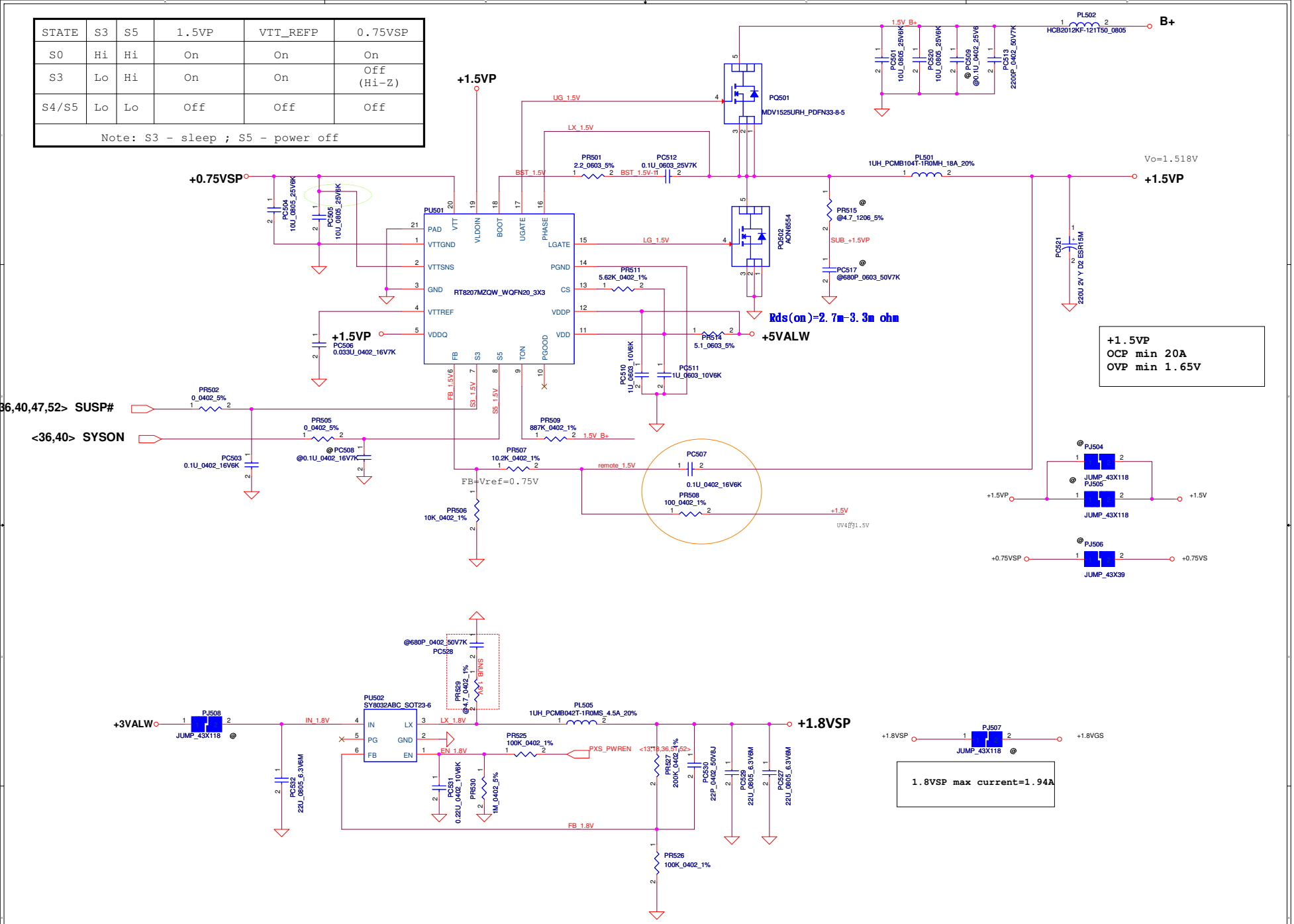
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 44 of 62

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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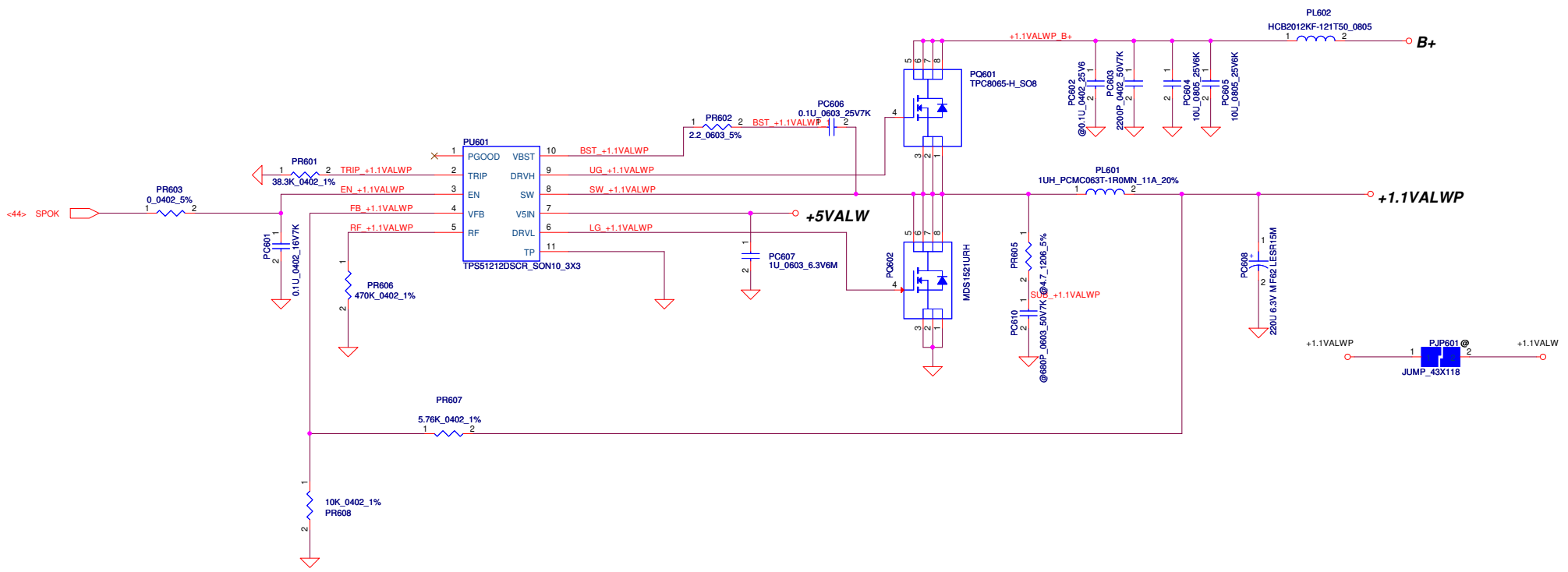
Title: +1.5VP/+1.8VSP

Size: Custom | Document Number: VALGD MB L | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 45 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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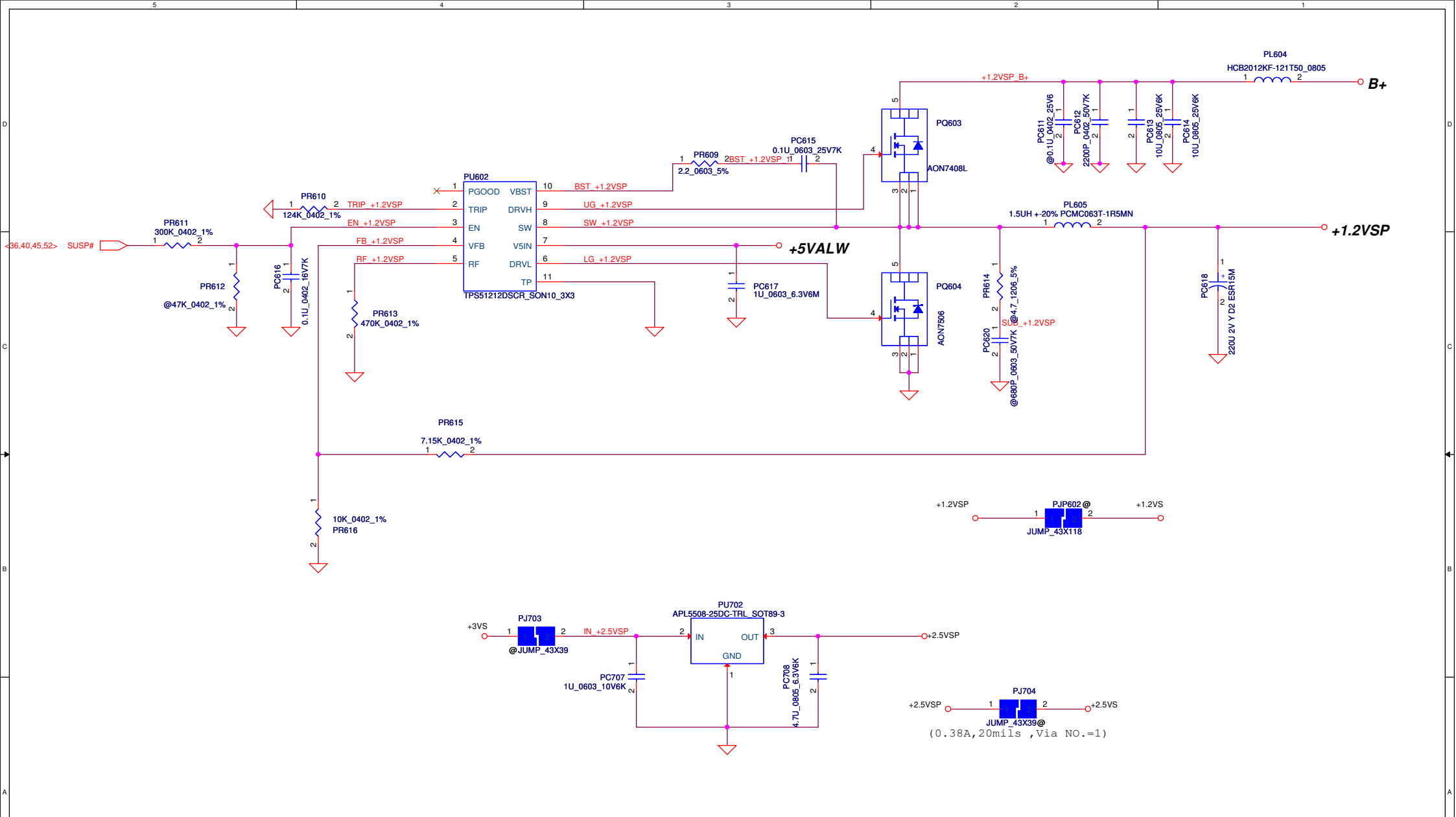
Title: **PWR +1.1VALWP**

Size: Custom | Document Number: VALGD MB L | Rev: 0.4

Date: Friday, April 12, 2013 | Sheet 46 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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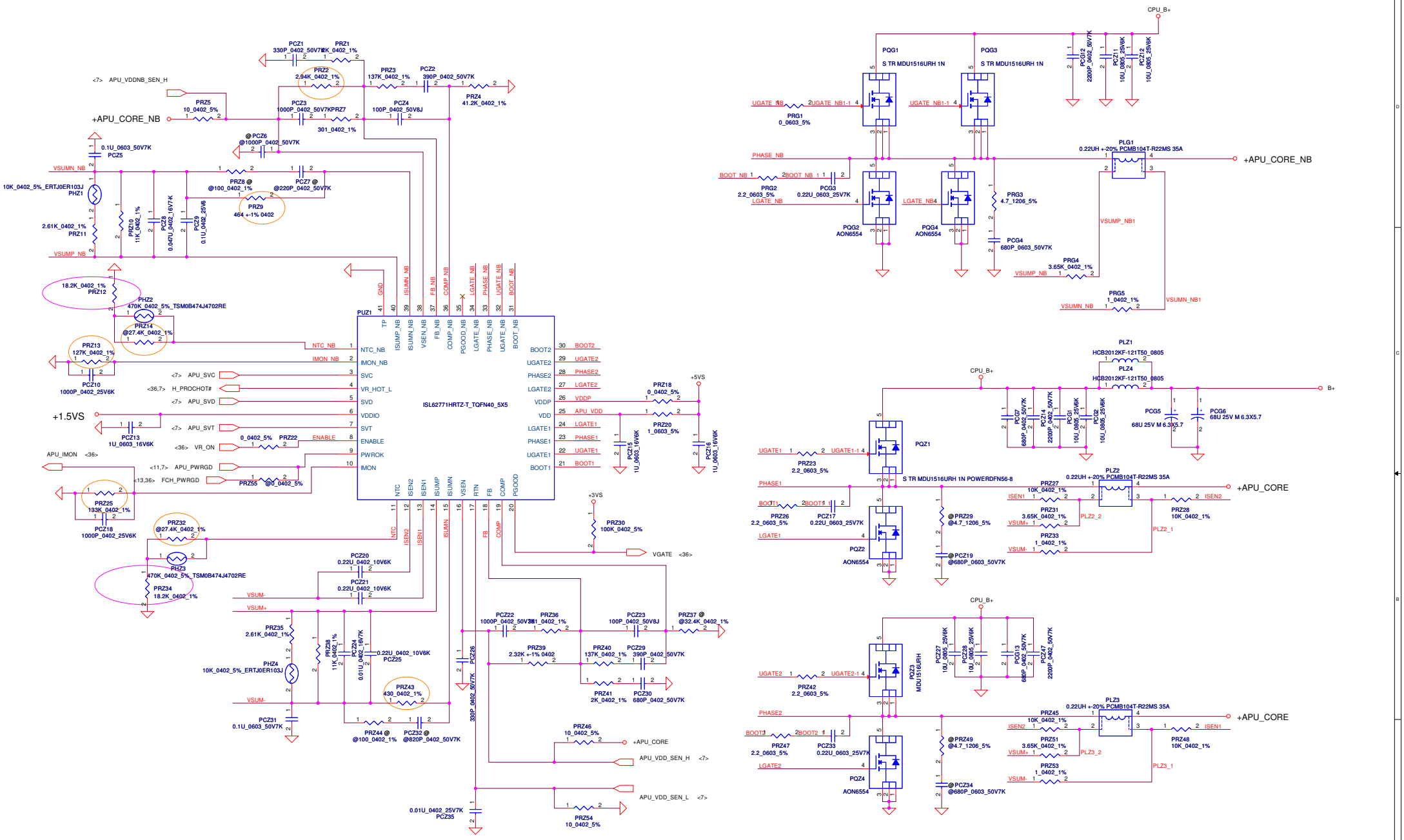
Title: **PWR +1.2VSP/2.5VSP**

Size: Custom | Document Number: **VALGD MB L** | Rev: 0.4

Date: Friday, April 12, 2013 | Sheet 47 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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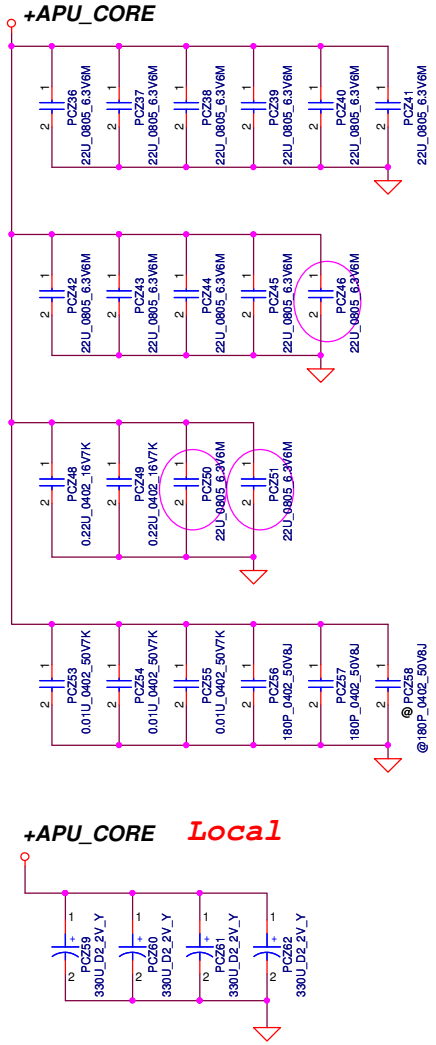
Compal Electronics, Inc.

Title: CPU_CORE/CPU_CORE_NB

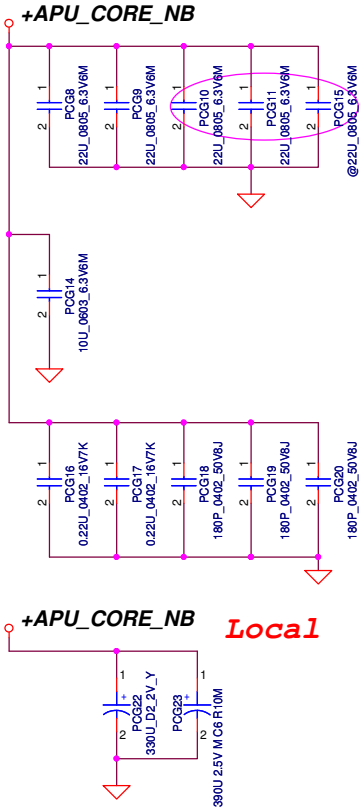
Size: Custom | Document Number: VALGD MB L | Rev: 0.3

Date: Friday, April 12, 2013 | Sheet 48 of 2

+APU_CORE



+APU_CORE_NB



	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
APU_CORE	4	10	2		3	2
APU_CORE_NB	2	2	2	1		3

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: PROCESSOR DECOUPLING
			Size: A3 / Document Number: VALGD MB L / Rev: 0.3
			Date: Friday, April 12, 2013 / Sheet 49 of 2

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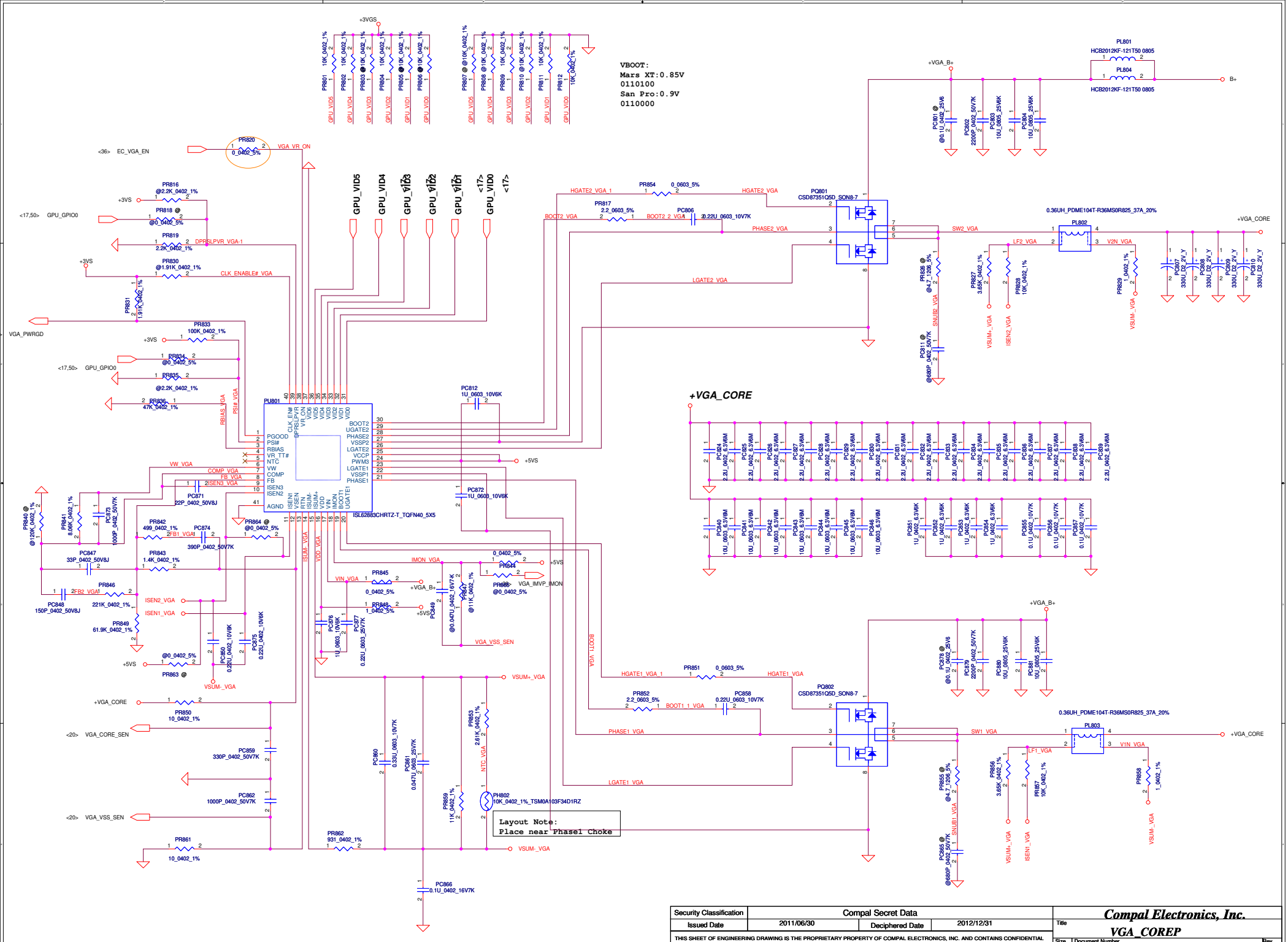

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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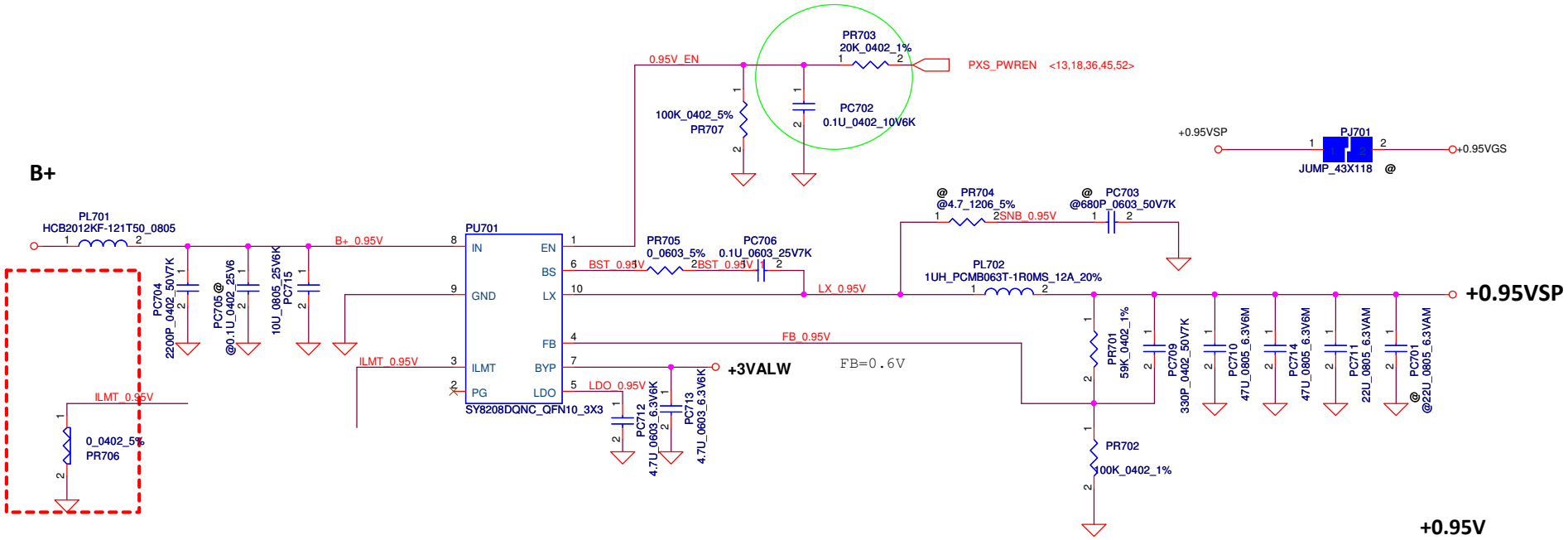
Compal Electronics, Inc.

Title: **VGA_COREP**

Size	Document Number	Rev
	VALGD MB L	1.0

Date: Friday, April 12, 2013 | Sheet 50 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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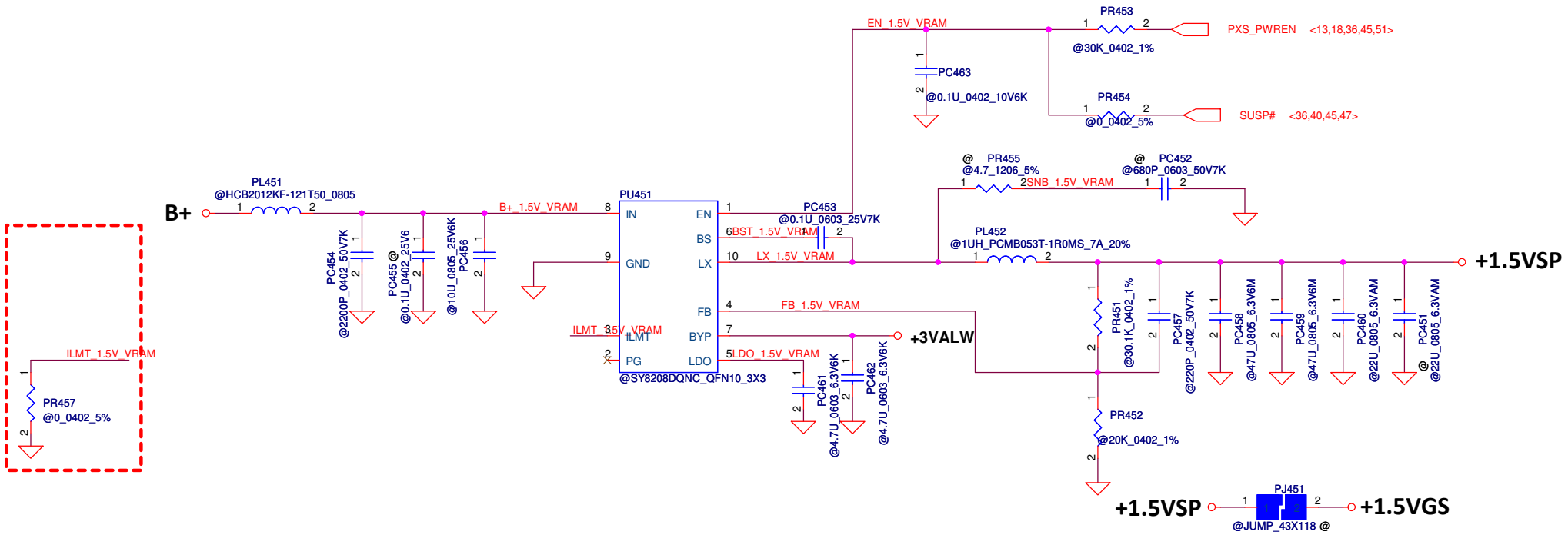
Title: **+0.95VSP**

Size: B | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 51 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

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Compal Electronics, Inc.

Title: **+1.5VSP(VRAM)**

Size: Custom | Document Number: **VALGD MB L** | Rev: 0.1

Date: Friday, April 12, 2013 | Sheet 52 of 99

Version Change List (P. I. R. List) Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P41	P41-PWR-DCIN / RTC Battery	12/11	PWR	add smart Adapter function	ADD PQ208,PQ102,PR111,PR225,PR228,PR227;Del PR973,PR974,PR972,PR975	
2	P42	P42-PWR-BATTERY CONN/OTP	12/11	PWR	add smart Adapter function	change PQ206,PR110,PR222,PR221,PC109 part number	
3	P51	P51-PWR-+0.95VSP	12/11	PWR	modify 1.5V output level	modify PR701&PR702 to 59K&100K	
4	P50	P50-PWR-+VGA_CORE	PWR	PWR	EMI rule	Add PC802 CAP	
5	P50	P50-PWR-+VGA_CORE	01/08	PWR	vender FAE requset	change VGA enable pin from SUSP# to EC_VGA_EN	
6	P45	P45-PWR-+1.5VP/+1.8VSP	01/08	PWR	0.75V can't power on	change 0.75V enable pin from SUSP to SUSP#	
7	P42	P42-PWR-BATTERY CONN/OTP	01/08	PWR	modify smart Adapter schematic	modify smart Adapter schematic	
8	P44	P44-PWR-3VALWP/5VALWP	02/23	PWR	Add RC delay for 3V power sequence	Add RC delay for 3V power sequence	
9	P48	P48-PWR-CPU_CORE/CPU_CORE_NB	02/23	PWR	modify over temperature setting	modify over temperature setting	
10	P42	P42-PWR-BATTERY CONN/OTP	02/23	PWR	Units will shut down on Optimized Battery Health mode when plug out battery	modify battery health mode schematic	
11	P45	P45-PWR-+1.5VP/+1.8VSP	02/23	PWR	VRAM transient fail	Add remote sense schematic	
12	P50	P50-PWR-+VGA_CORE	02/23	PWR	AMD change VBOOT SPEC	change Mars XT VBOOT from 1.1V to 0.85V change Sun pro VBOOT from 1.1V to 0.9V	
13	P41,42,48,50	P41,42,48,50	01/10	PWR	Add bead for cost down plan	Add bead for cost down plan	

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Version Change List (P. I. R. List) Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37		1114		1.SW3 add DEBUG@ 2.add J13		
2	38		1114		1.change netname form +3VS_VGA to +3VGS 2.change netname form +V1.05S_VCCP to +3VALW 3.remove RG10 4.change U71 P/N form SA000063300 to SA00006D500 for DIS,.change U71 P/N form SA000057I00 to SA00005D000 for UMA		
3	36		1114		1.VR_ON reserve PD 10K		
4	17		1114A		1.remove RV16,RV17		
5	27		1114A		1.reserve RV687,RV92		
6	12,30		1115		1.change netname from PCH_BT_ON# to BT_ON# 2.change netname from PCH_WL_OFF# to WL_OFF#		
7	40		1115		1.change 1.1VALW to 1.1VS circuit follow QAWYA 2. remove R1138,Q158,R1140(include discharge of 1.2VS and 2.5VS) 3.change SUSP reverse circuit follow QAWYA 4.change SYSON reverse circuit follow QAWYA 5.remove VLDT_EN reverse circuit 6.add +1.5V to +1.5VS follow QAWYA		
8	13		1116		1.change netname from LAN_CLKREQ# to CLKREQ_LAN#		
9	13		1116A		1.change netname from WLAN_CLKREQ# to CLKREQ_WLAN#		
10	13,27,30,37		1116B		1.CMOS change port from port1 to port3 2.WLAN change port form port7 to port2 3.USB(R)change port form port8 to port0		
11	35		1119C		1.change netname from +3V_PCH to +3VALW		
12	11		1119D		1.remove R84		
13	7		1119D		1.change net name from APU_VDD_RUN_FB_L toAPU_VDD_SEN_L 2.change net name from APU_VDD_SEN to APU_VDD_SEN_H 3..change net name from APU_VDDNB_SEN to APU_VDDNB_SEN_H		
14	20		1119D		1.change net name from VCCSENSE_VGA to VGA_CORE_SEN 2.change net name from VSSSENSE_VGA to VGA_VSS_SEN		
15	36		1119D		1.remove EC_VGA_EN 2.remove VGA_AC_DET		
16	34		1120A		1.reserve Q96,R711		
17	7		1120C		1.remove C159,C161,C210,C164 2.change net name from LVDS_A1 to DP0_TXP1_C 3.change net name from LVDS_A1# to DP0_TXN1_C		
18	26		1120C		1.add RP26,R241,R242		
19	26		1121C		1.remove R301,R302,R826,C422,U11		
20	27		1121C		1.remove R687		
21	19		1122		1.remove CV54,CV55,CV56,CV57,CV58,CV59		
22	20		1122		1.remove CV96,CV97		
23	36		1122A		1.remove C431,R305,C438,C439		
24	7,26,36		1123A		1.remove C113,C115,RP26,R239~242 for eDP circuit 2.add R826 3.add "ENBKL"signal 4. change EC GPIO(VGATE and EC_TS_ON)		
25	17,33,39		1126A		1. Change C736 from SGA00003000 to SE00000T780 2. Remove Q11 3. Set RV24,RV25,QV3 are 0 4. Add REMOTE1+ to UV1.AF29 & REMOTE1- to UV1.AG29		
26	38		1127		1. Change net name from +3VGS to +1.8VGS on U71 pin11		
27	27		1127A		1.Change net name from DISPOFF# to BKOFF# 2.update P04 table		
28	33		1127A		1add ZZZ for MB PCB		

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	11,18,31,38		1128		1.remove R801,R207,RV40,RL13,CL27 for GCLK circuit 2.GCLK circuit in p.38		
30	31		1128		1.remove GCLK@ in RL3,CL7,QL1 2.change LL1 P/N to SHI00008W00		
31	37		1128		1.change U40 P/N to SA00005LN00		
32	28		1128A		1.change RP22 to RV94~RV96		
33	32		1128B		1.change CL30 P/N to SE067102K80		
34	11		1128B		1.change CLK_PCIE_LAN/CLK_PCIE_LAN# form port0 to port3 2.change CLK_PCIE_WLAN1/CLK_PCIE_WLAN1# from port1 to port2		
35	28		1128B		1.add R3334,R3335		
36	26		1129		1.add RA10,RA11,RA15,RA24,R1459,R1460		
37	36,41		1129		1.add signal"ADP_ID_CLOSE"for smart adapter function		
38	32,33		1130		1.remove OPT@ of C587 2.change from @EMI@ to EMI@ for CL30		
39	5,16		1130		1.change cap form .22u to .1u for PCIE Gen2		
40	35		1130		1.change shot pad to .1u for CA64~CA66		
41	39		1204		1.change JTS1 conn to SP010013W10		
42	12,30		1204A		1.remove BT_ON#,add BT_DISABLE#		
43	07		1204A		1.RP9.4 connect to +1.5V_APU,R348.1 connect to +1.5VS for leakage issue		
44	11,18,31,38		1204B		1.add R801,R207,RV40,RL13,CL27 for GCLK circuit 2.add GCLK circuit in p.38		
45	36		1205		1.change net name form NOVO# to EC_FAN_PWM in EC 2.change net name form EC_FAN_PWM to NOVO# in EC 3.change net name form ENBKL to APU_IMON in EC 4.change net name form APU_IMON to ENBKL in EC		
46	38		1206		1.change RG2 to 10ohm,RG3 to 33ohm,RG4 to 33ohm 2.U74.2 change from +3V_LAN to +3VALW		
47	39		1206A		1.change C736 to SE00000PL00(0805 package)		
48	38		1210		1.add GCLK@ in RG2,RG3,RG4		
49	55,56		1210A		1.add P55,P56		
50	03,12,33,37,39		1212		1.update BOM Structure Table 2.change U3 symbol to SA00003K820 3.change U35,U36 symbol to SA00003TV00 4.change U99 P/N to SA00001Z710		
51	41~52		1213		1.update PWR circuit for BOM		
52	20		1220		1.change LV7 BOM structure from PX@ to SHORT PAD@		
53	40		1220		1.remove @ in Q157A		
54	20		1224		1.add TEST POINT@ to TV15		
55	18		1224		1.change net name from PXS_PWREN to PXS_PWREN# in QV2.2		
56	28		1224		1.remove C528 based on LA-9901 DVT schematic		
57	37		1224		1.change JKB1 from SP01000WK00 to SP010011A00 2.change JTP1,JPWRB1 from SP010014M10 to SP010010T00		
58	34		1224		1.change JODD2 from SP01001FJ00 to SP010016C00		

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
59	35		1224		1.change JSPK1 from SP02000RR00 to SP02000H700		
60	37		1224		1.change JLED1 from SP01001A900 to SP010010T00		
61	33		1225		1.change U99 from SA00001Z710 to SA000067P00		
62	24,25		1225		1.change CHB form PX@ to MARS@		
63	26		1225		1.change Panel PWM circuit 2132R@		
63	29		1225		1.change Q93 & Q95 to Q93A & Q93B		
64	27		0105		1.Change BID R311=>18K		
65	35		0107		1.RA12,RA16 change to 100-ohm., RA13, RA14 to 15-ohm, ADD CA27,CA28 to 1uF		
65	36		0108		1.add PXS_PWREN & EC_VGA_EN		
66	14 ,34		0108		1.Change R177 ,180 & R550 from 0805 short pad to Jumper (J14, J15, & J10)		
66	35		0110		1.RA22=>DEBUG@ for Beep 2. CA28 CA27=>2.2u for THD+N		
67	27, 32 and 37		0110		1.R813=>220 ohm Bead 2.Add C492 for EMI request 3.DLL1=>EMI@		
68	33		0111		1.ADD ZZZ & ZZZ1 for 14"_DIS & 15"_DIS pcb		
69	12		0114		1.ADD GPIO54 for RTD2132R@ 2.change U99		
70	33		0116		1.change H21 from 2P8 to 4P6 2.change U99 to 1001101x (4D)		
71	39		0116		1.add C737 &C735@ for USB droop (follow Intel)		
72			0121		1.change D24 to SCA00001G00 for ESD request		
73	28		0121		1.L30, L31 & L32 downsize to 0402,SM010005X00		
74	39		0121		1/21 L51,L55,L58 &L66 change PN to SM070001N00 for action plan		
75	29		0121		1/21 L35,L36,L37 &L38(HDMI) L49,L50,L53 & L54(USB3) change PN from SM070001S00 to SM070003K00 for action plan		
76	10		0126		SIT: change C145 from OS-Con to POLY		
77	37		0129		1/29 SIT: Del R806 & Q12 for change audio type from normal close to normal open.		
78	36		0201		2/1 SIV: add PU resistor for LID_SW#		
79	35		0221		1.upgrade capacitors of CA36 & CA46 from 1uF to 2.2uF/X5R 2.AVDD_HP connect to standby power rail (+3VLP) for prevent speaker hum noise issue.		
80	20		0221		1.Change Cap of CV66 to 220U 4V Y D2 ESR15M = SGA00000Y80 for PWR request		
81	38		0221		1.add CG5 on 1.8VGS for GCLK 2.reserve CG6 & CG7 for vender request.		
82	22~25		0221		1. p22 & p23==>Channel B Mars@ 2.p24 & p25==>ChannelA PX@		
83	35		0225		1. add speaker bypass Cap CA38,CA39,CA40 & CA43 for EMI requirement		
84	07		0226		1. add C438 100pF on H_THERMTRIP# for ESD requirement		
85	34		0301		SIT: 3/1 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)		
86	34		0301		Del CV168 ,CV159,CV160 &CV189 for VRAM body size issue		
87	37		0301		change C492, SE00000FD80 to SE074331K80 by Sourcer requiremrnt.		
88			0301		LV4,LV10,L3,L6,L9,L11& L77 Downsize to 0402 BLM15AX221SN1D (Murata) ,SM01000MK00 by Sourcer requiremrnt.		
89	36		0301		Add R311=8.2K for SIT		
90	11		0301		Change R85 from 0 ohm short pad @ to 33 ohm EMI@		

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
91	26		0301		1.add R1461 for RTD2132R ,MIIC_SDA :MIIC_SCL=0 : 1		
92	35		0301		1.Change +VDDIO_HDA power rail from +3VALW to +3VS.		
93	26		0304		1.add R1462 for RTD2132R ,MIIC_SDA :MIIC_SCL=0 : 1 2.Del RP16.3 & RP16.4		
94	12,13		0304		1.Change R367 from 10K to 100K. 2.Change R234 from 10K to 100K		
94	32		0305		1.add CL32 & CL33 for ESD request.		
95	32		0306		1.add R236 & R237 (LVDS_SEL) for C build only.		
96	8		0306		1.add J3 for 1.5V		
96	33		0306		1.Change Power rail of the U99 from +3VS to +3VGS.		
97	12		0306		1.Change Power rail of the GPIO54 from +3VALW to +3VS.		
98	12		0307		1.Change +1.5GVS enable pin from +VSB to +5Valw for Eup lot 6.		
99	12,36		0311		1.Change BOM structure of R367 & R368 to @,2132S only 2.R237 & R236 =>@		
Pre-MP 100	33		0311		1.Change U99 to SA00001Z710		
Pre-MP 101	12,36 & 26		0403		1.Reduce part count for RTD2132R only		
Pre-MP 102	12,36 & 26		0403		1.Reduce part count for RTD2132R only		
Pre-MP 103	34		0403		1.ODD Power Control cuicuits =>@		
Pre-MP 104	33		0410		1.Change H17 form H_8P0N to H_7P0N SD309100280		
Pre-MP 105	36		0410		1.Change RP11 form SD309100280(10K) to SD309100300(100K)		
Pre-MP 106	18		0410		1.Change RV41 to 47K for Erp Lot6		
Pre-MP 107	18		0410		1.Change RV37 from 20Kto 100K ,RV38 from 20K to 0 ohm.		
Pre-MP 108	18		0410		1.Change RV37 from 20Kto 100K ,RV38 from 20K to 0 ohm.		
Pre-MP 109	36		0411		1.Del Net VLDT_EN & 1V_ALW_EN		
Pre-MP 110	7, 13		0412		1.change C438 from 100p to 1000p. 2. add C439, 1000p for ESD request.		

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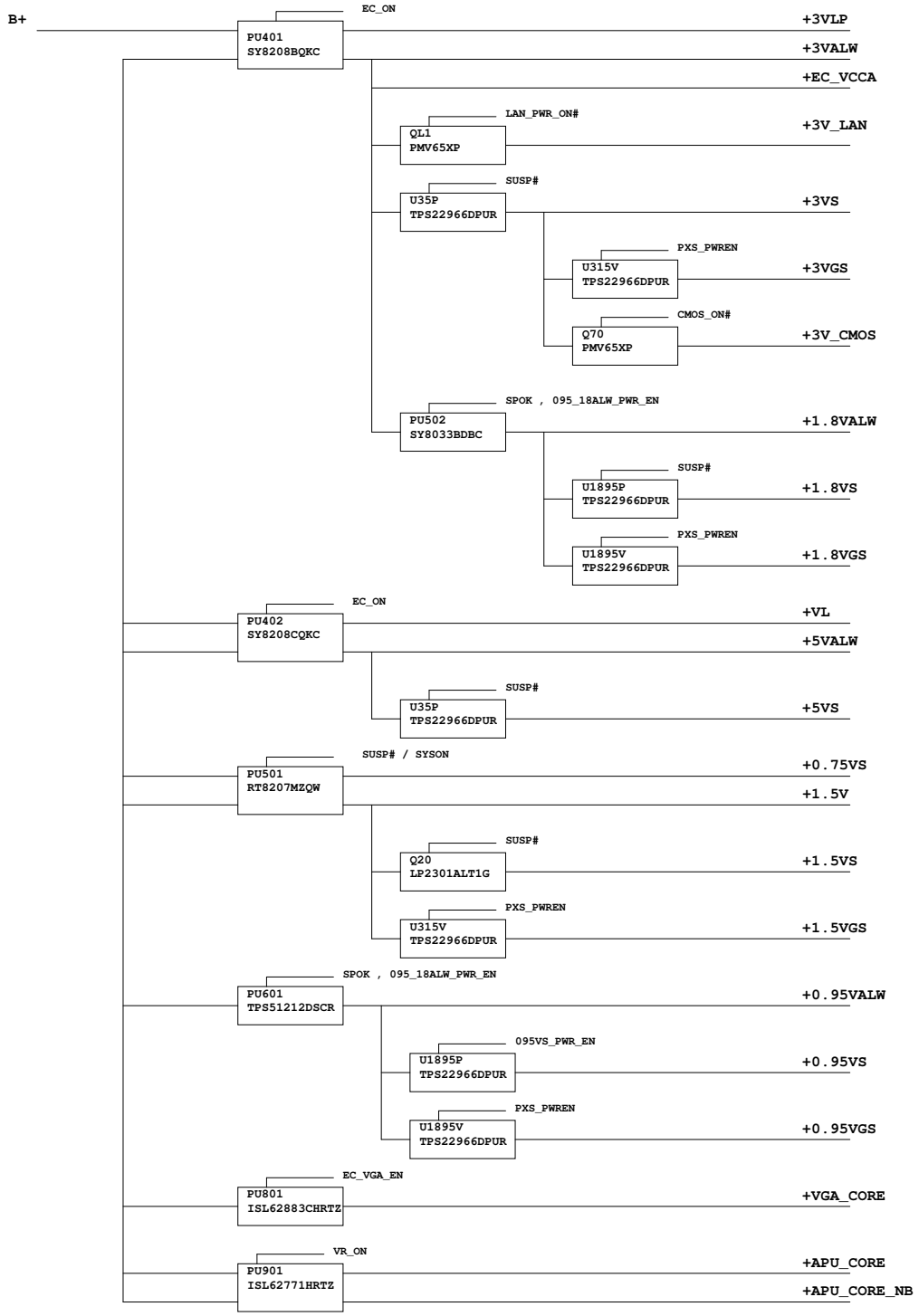

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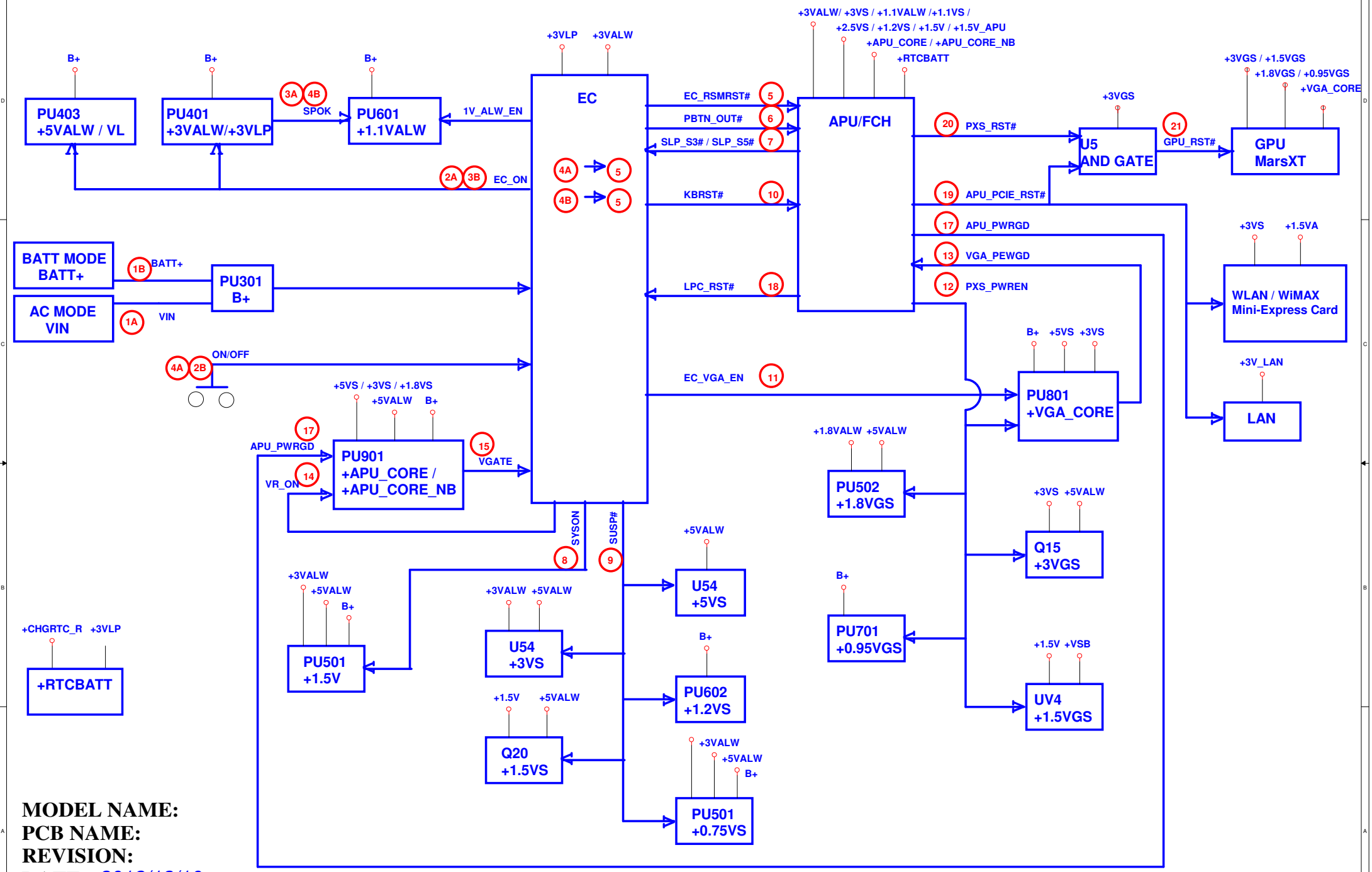

MODEL NAME:
PCB NAME:
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