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PWWAA

Marseille LC

L-A6841P REV 0.1 Schematic

Intel Penryn/ Cantiga/ ICH9M
2010-07-22 Rev. 0.1

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Date: Monday, August 16, 2010	Sheet 1 of 44	

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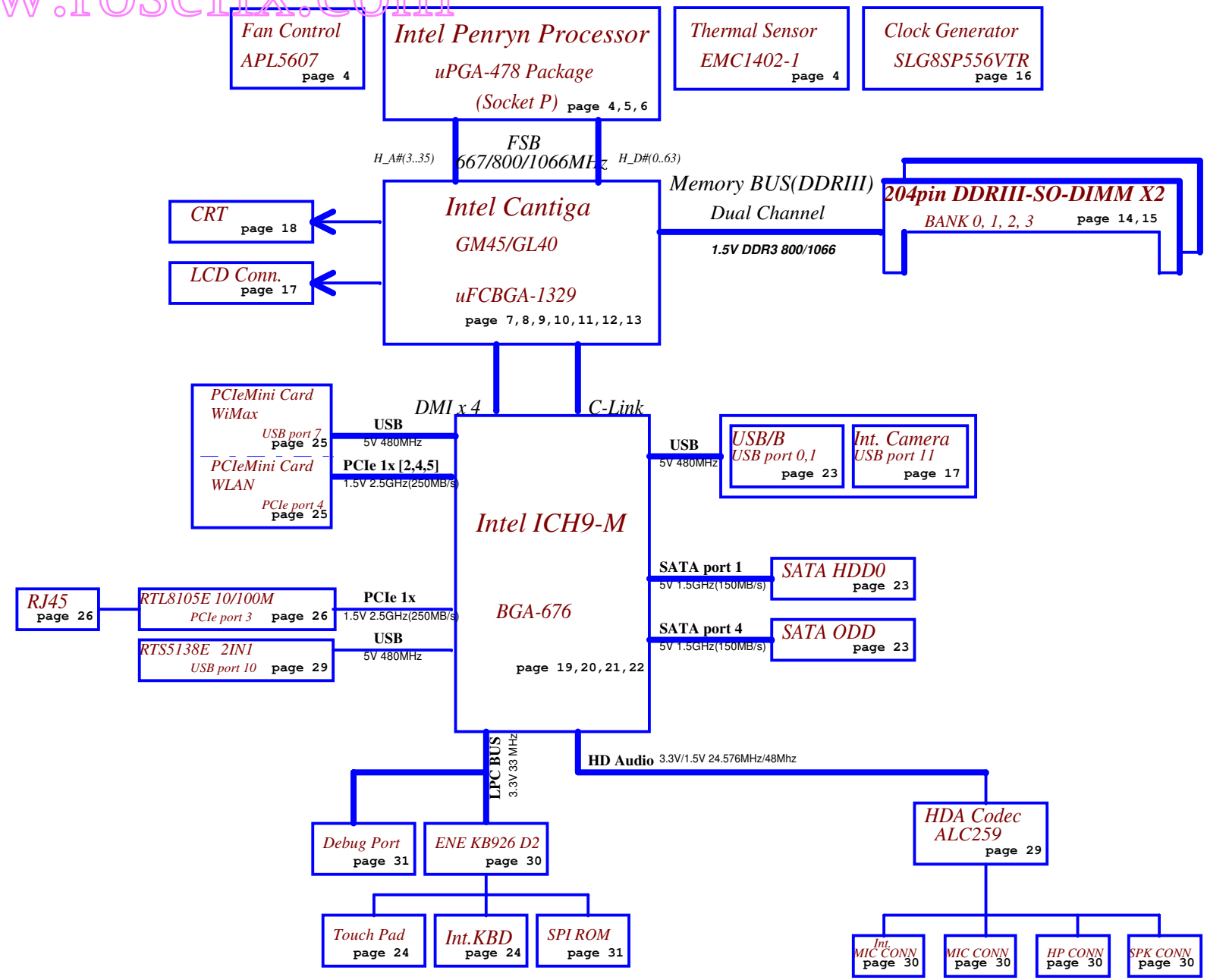
Model Name : PWWAA
File Name : LA-6841P



Power/B page 24

RTC CKT. page 20

DC/DC Interface CKT. page 33

Power Circuit DC/DC page 34,35,36,37,38,39,40

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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5 power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for SB	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	Card Reader		Camera	WLAN	Energy Star
description			(X)	Always	Always
explain			Camera	WLAN	Energy Star
BTO			CAM@	WLAN@	

External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D2	
+3VL	Smart Battery	0001 011X b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D2	
+3VS	CPU THM Sen SMSC SMC1402	1001 101Xb

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb

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Title: Notes List

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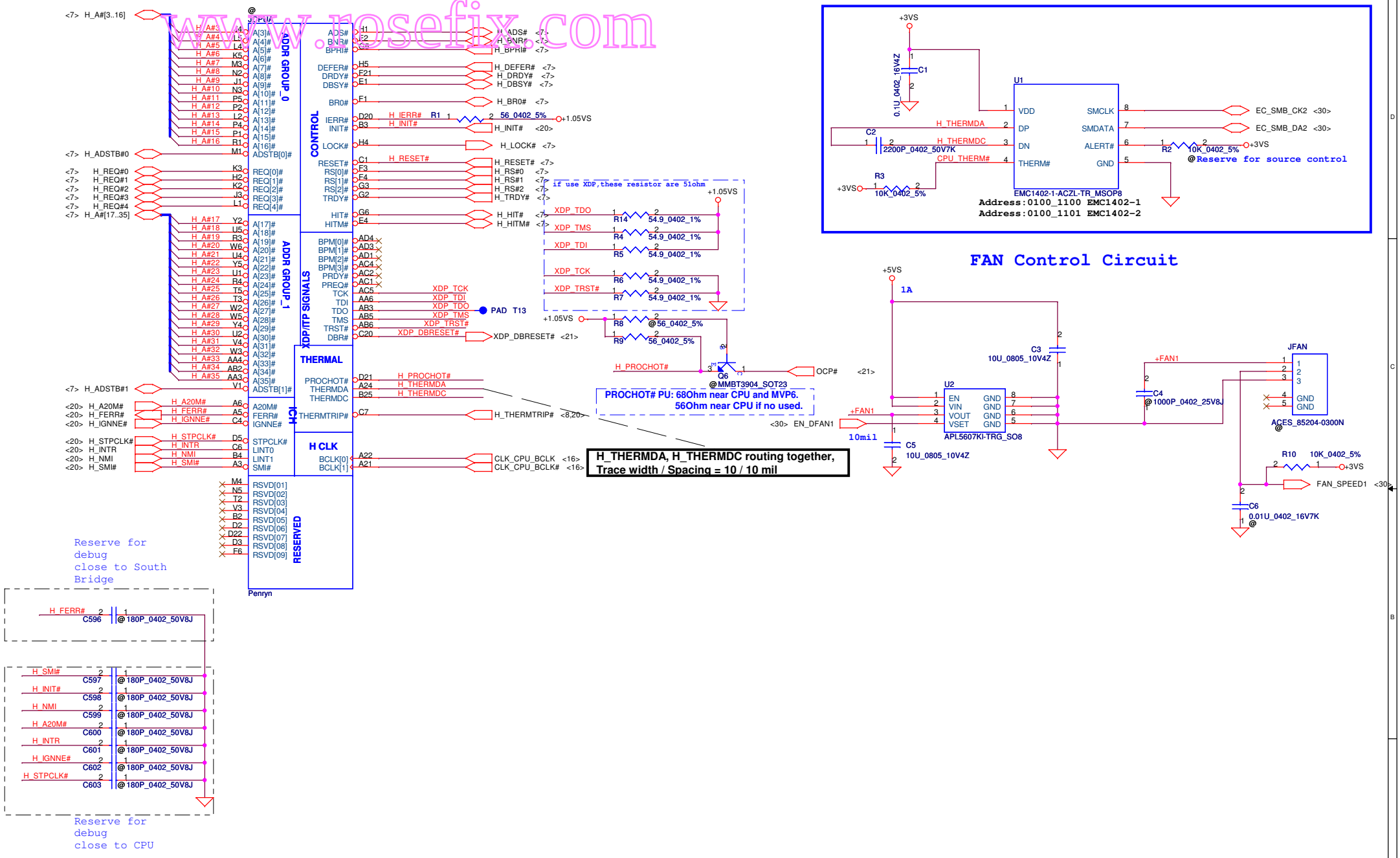

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Title: Penryn(1/3)-AGTL+/THM/FAN

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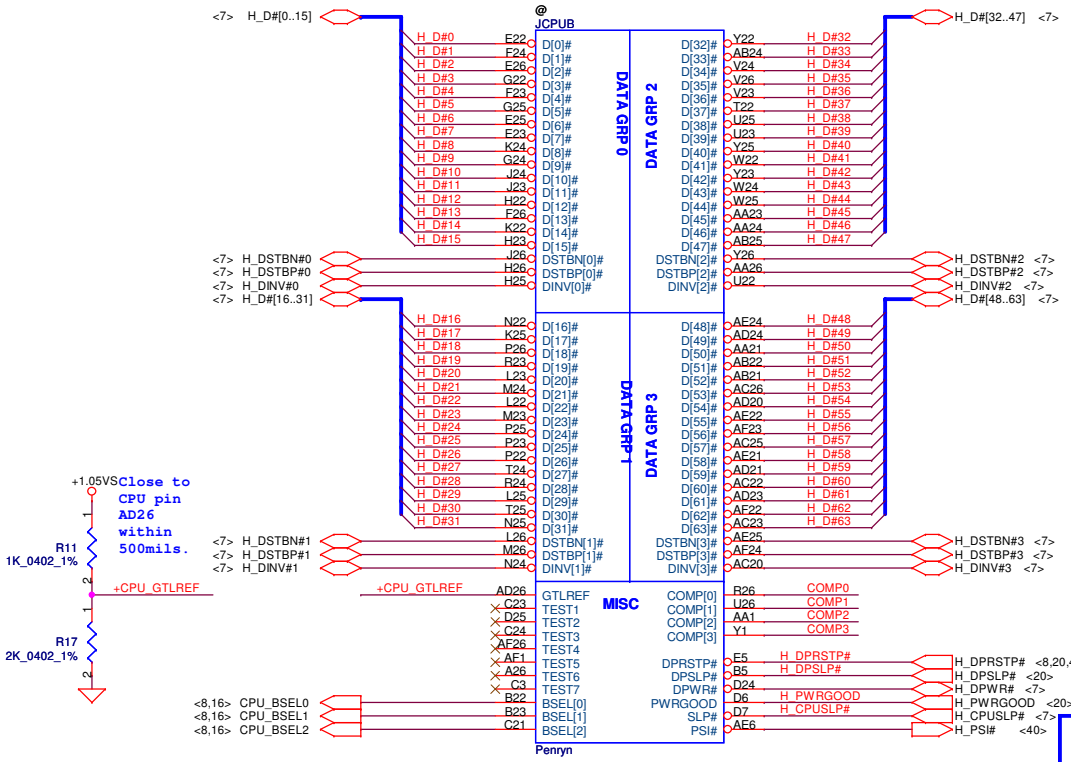
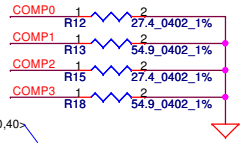


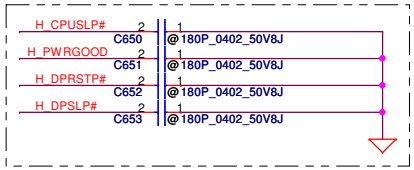
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 5 mils.



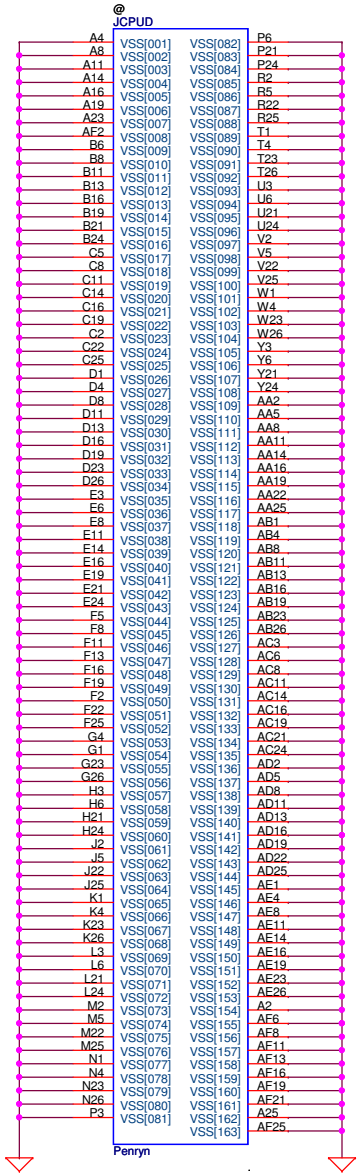
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Reserve for debug close to CPU



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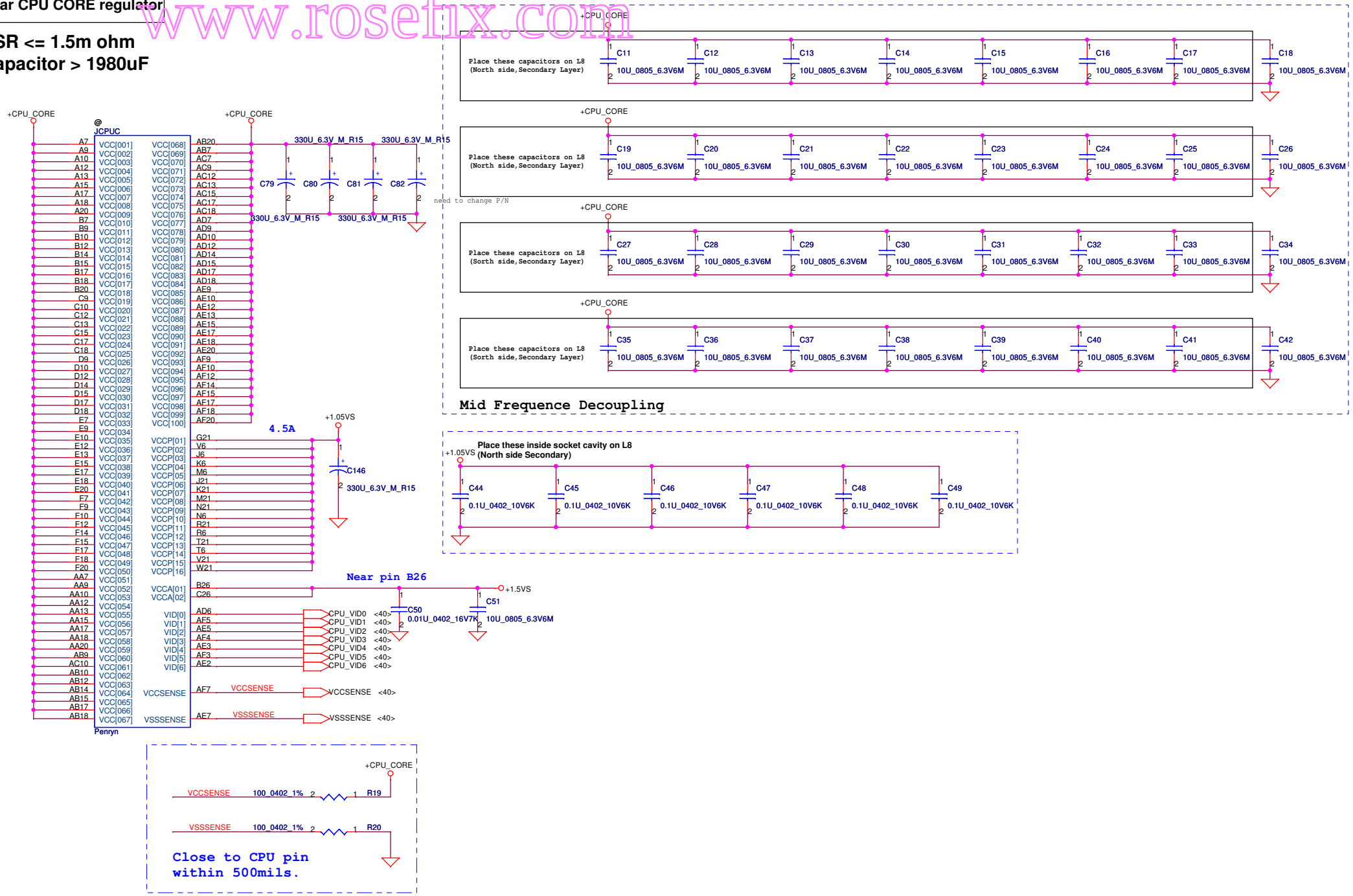
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



Length match within 25 mils.
The trace width/space/other is 14/7/25.

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Compal Electronics, Inc.

Title: Penryn(3/3)-PWR/Bypass

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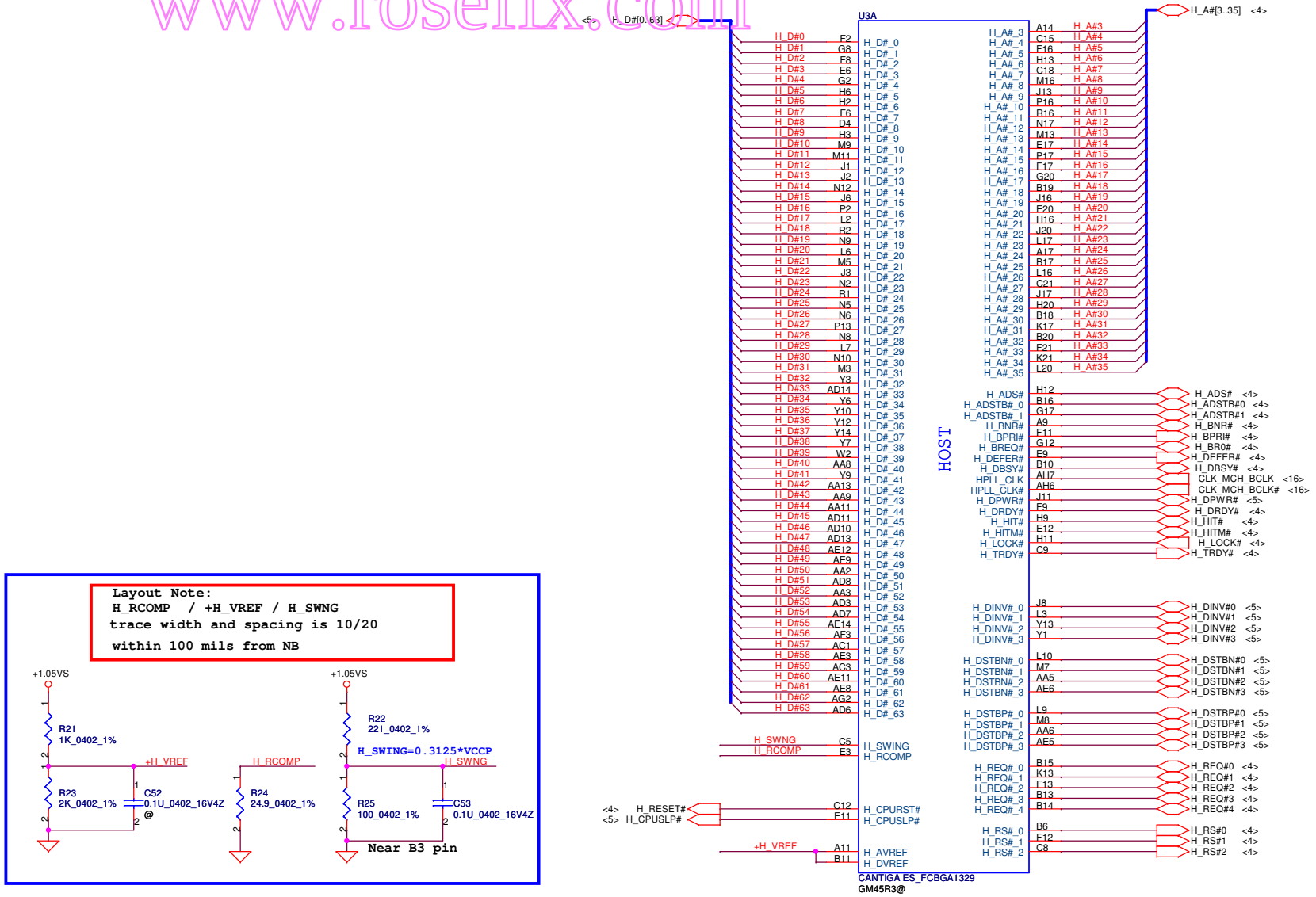

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Compal Electronics, Inc.

Title: Cantiga GMCH(1/7)-GTL

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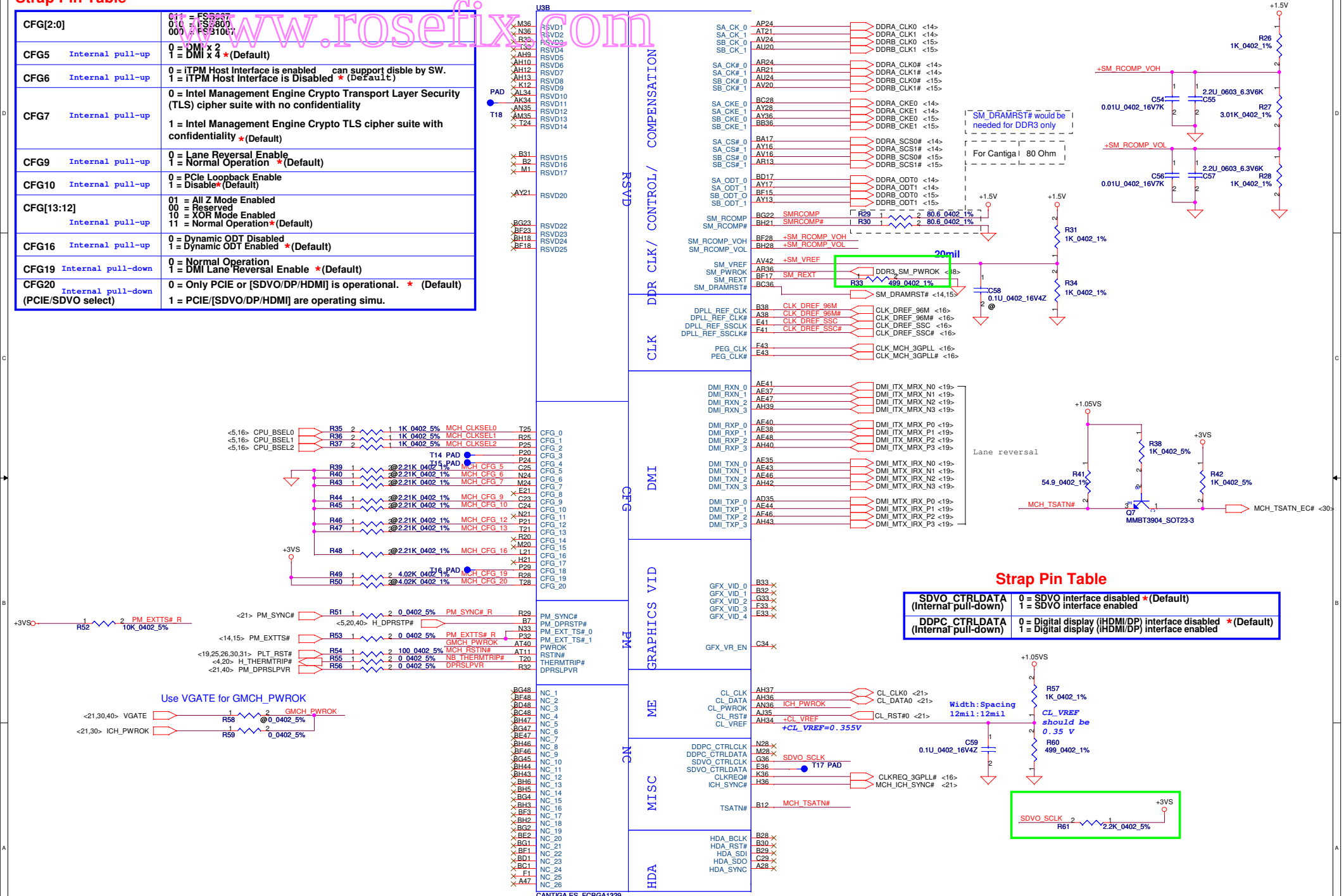
Strap Pin Table

CFG[2:0]		011 = FS2667 010 = FS2800 000 = FS3106
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled * (Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.



Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled *(Default) 1 = Digital display (iHDMI/DP) interface enabled

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Title: Cantiga GMCH(2/7)-GTL

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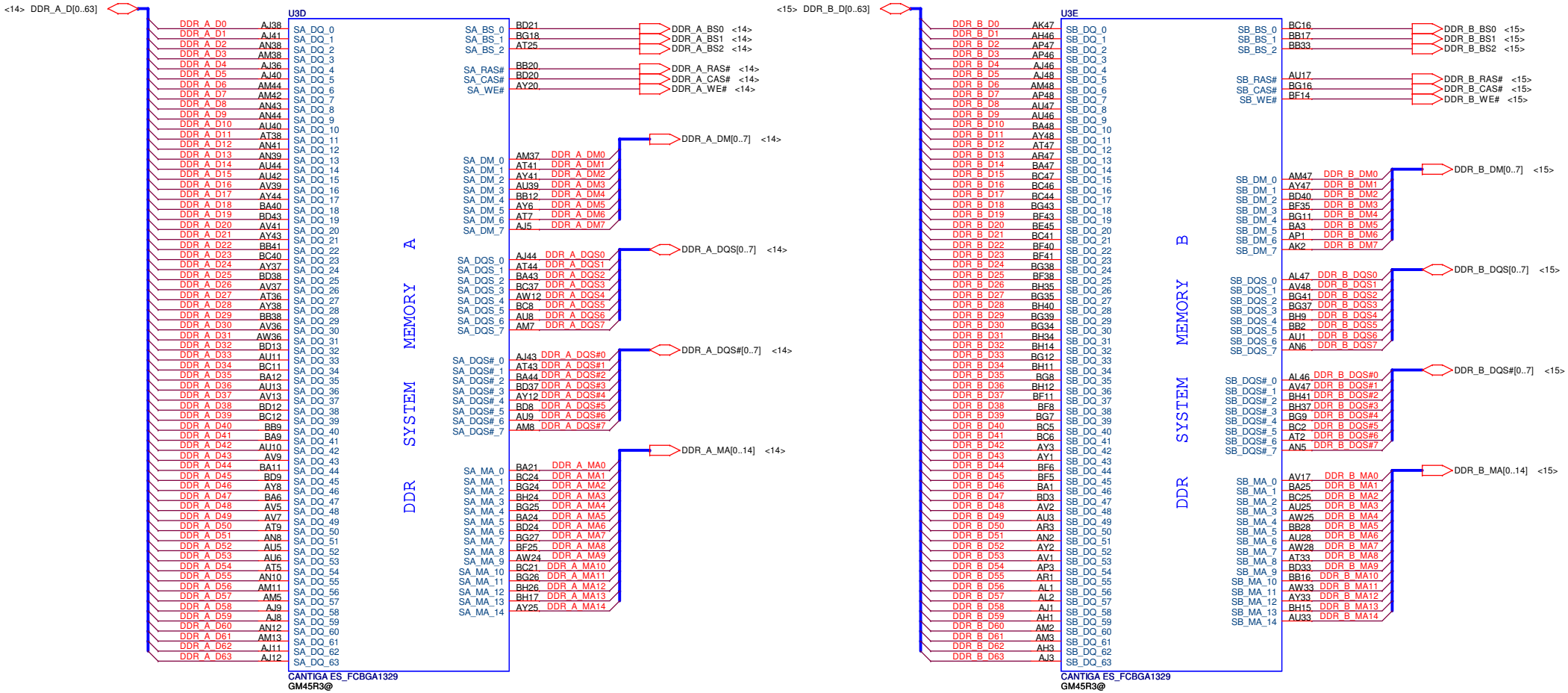

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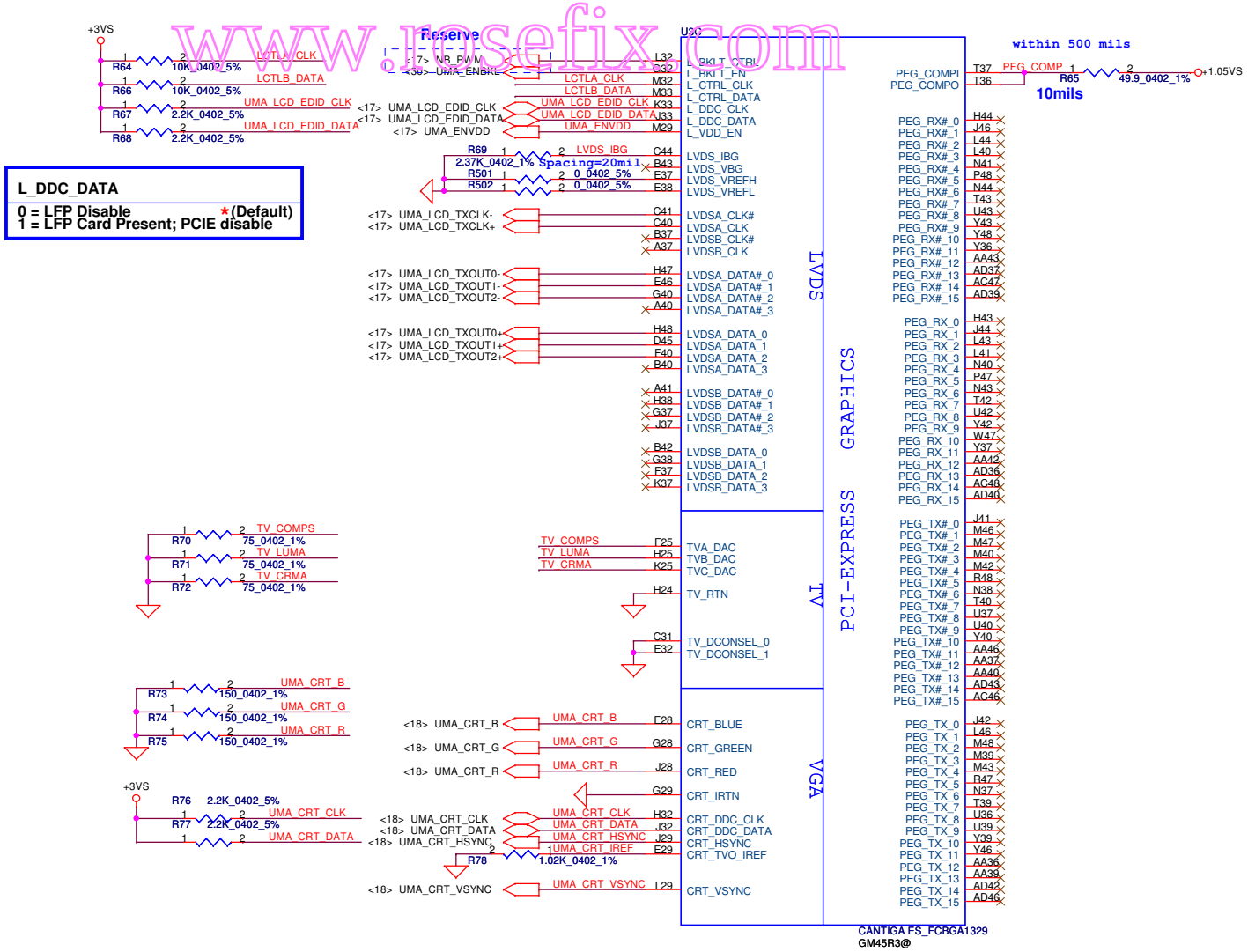

L_DDC_DATA

0 = LFP Disable *(Default)
1 = LFP Card Present; PCIE disable

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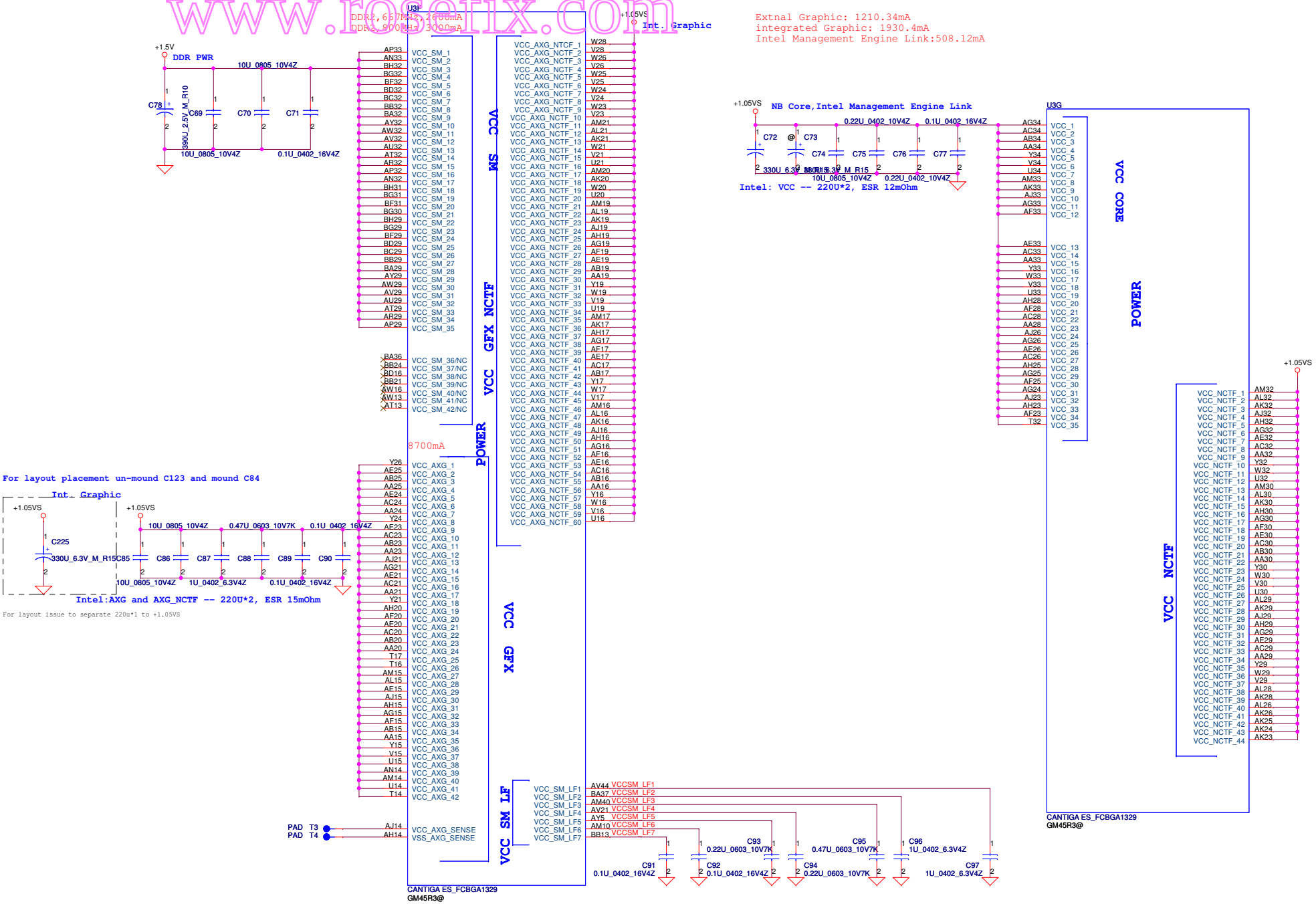
DDR2,667MHz,2600mA
DDR3,800MHz,3000mA

Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA
Intel Management Engine Link:508.12mA



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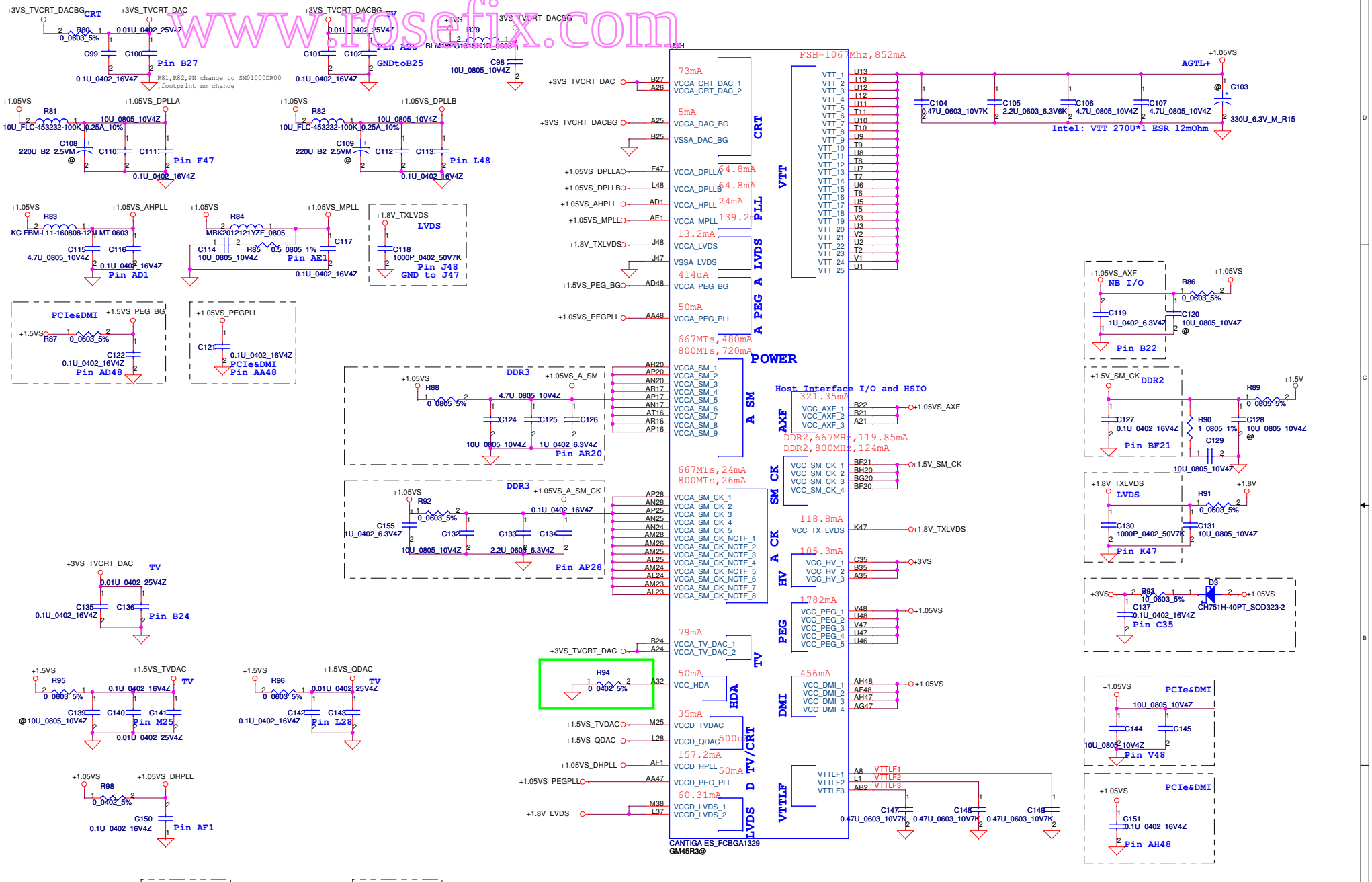

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Title: Crestline GMCH (6/7)-VCC

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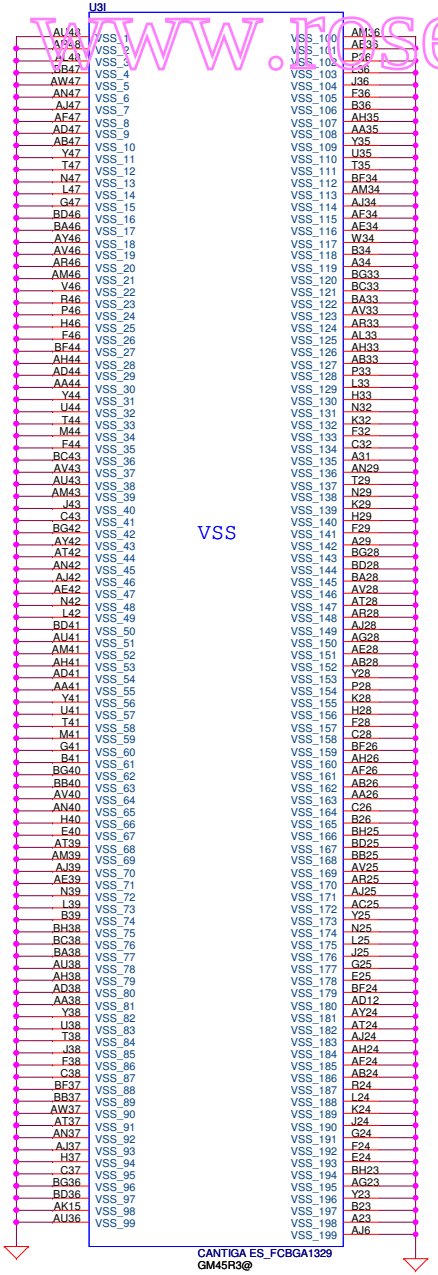

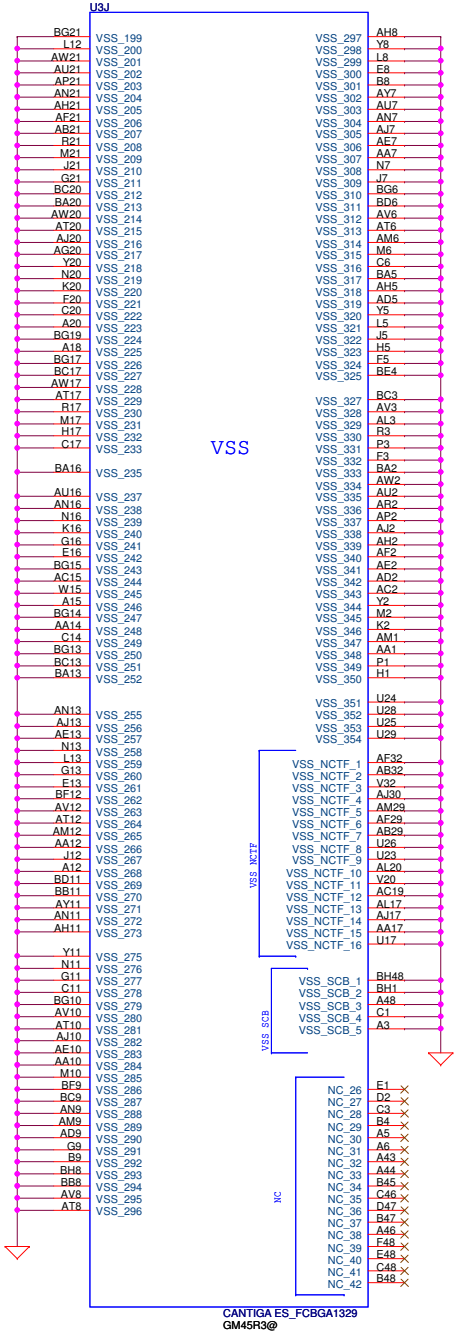

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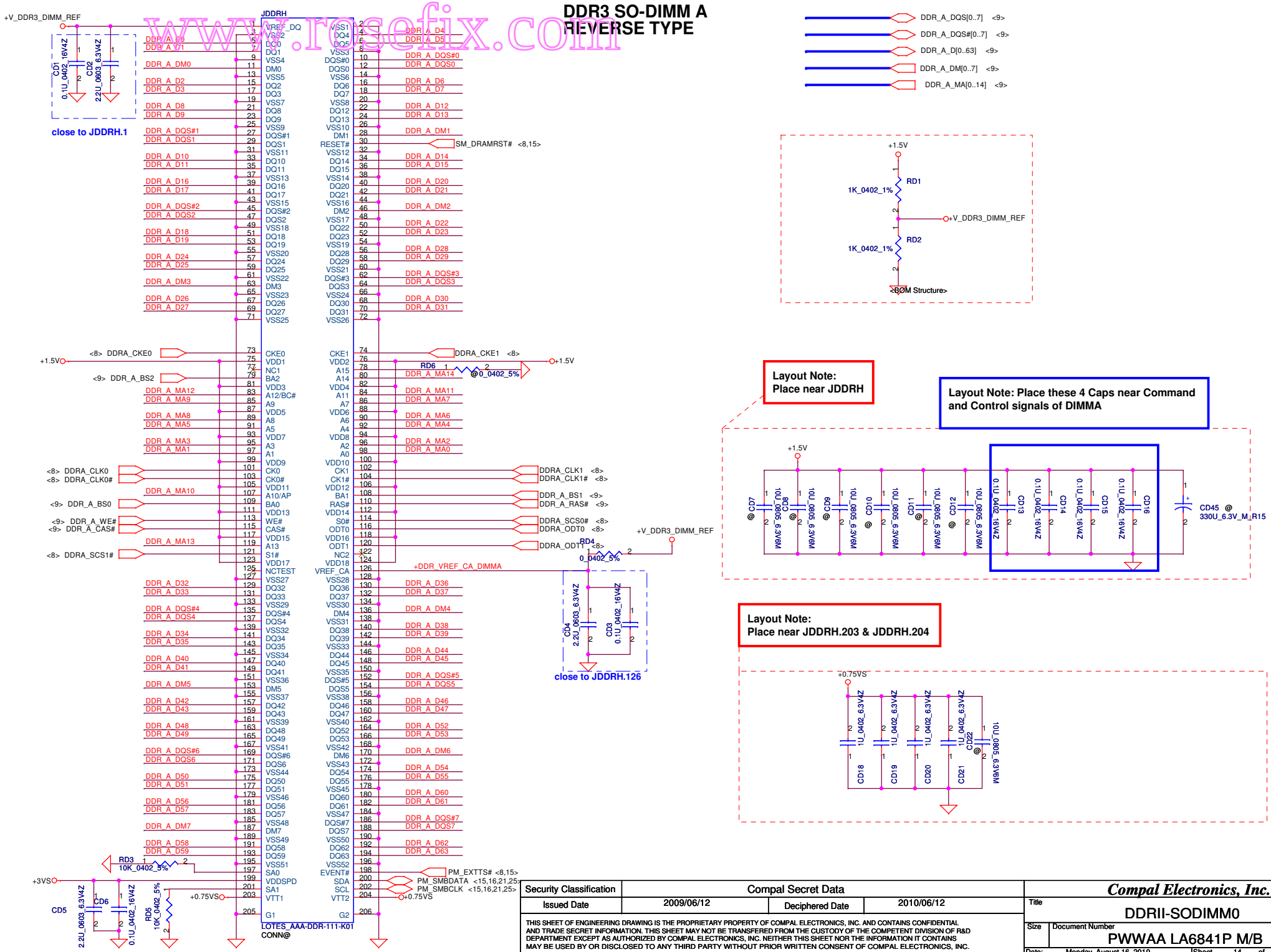
DDR3 SO-DIMM A
REVERSE TYPE



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Title: DDRII-SODIMM0

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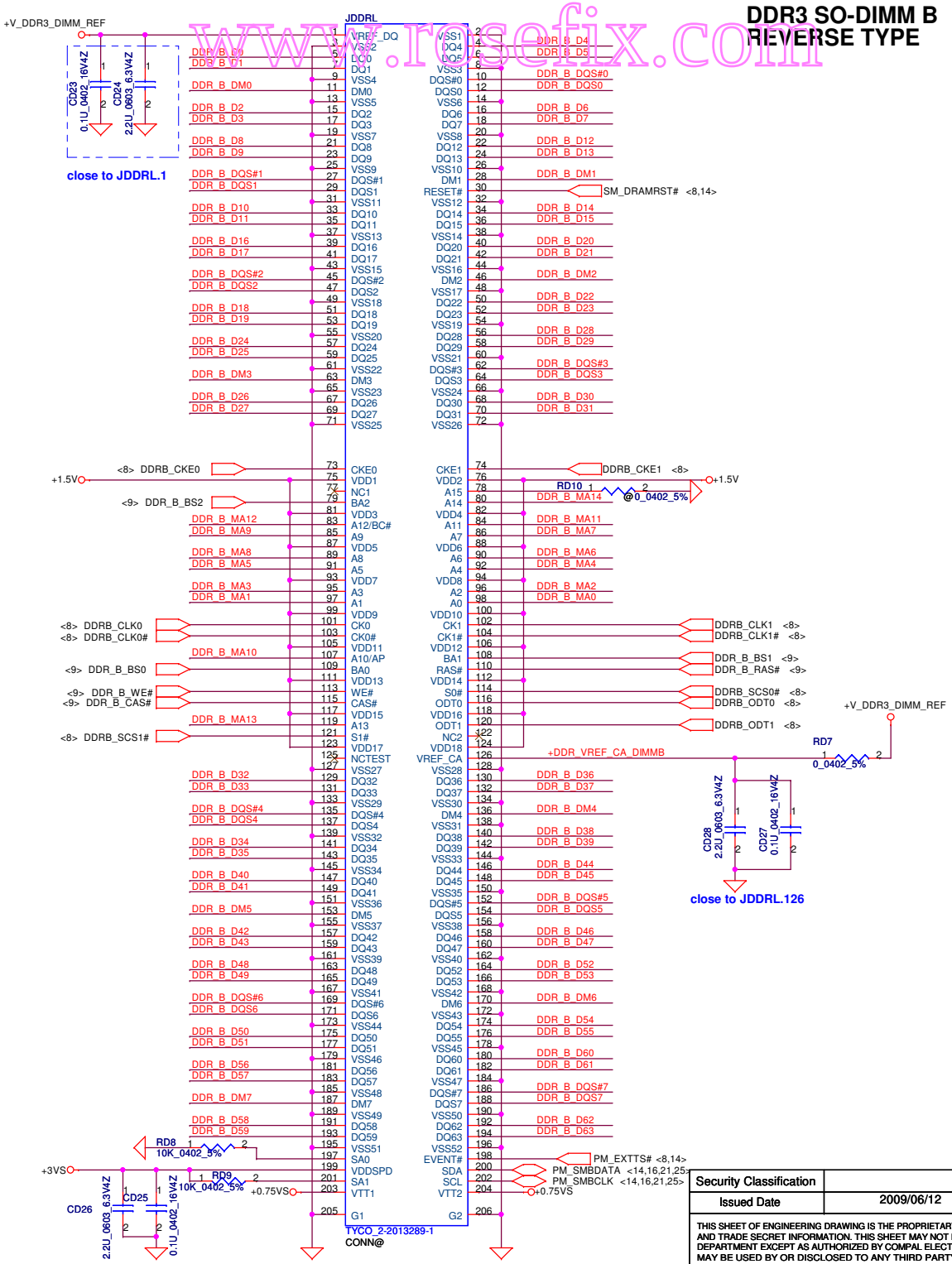
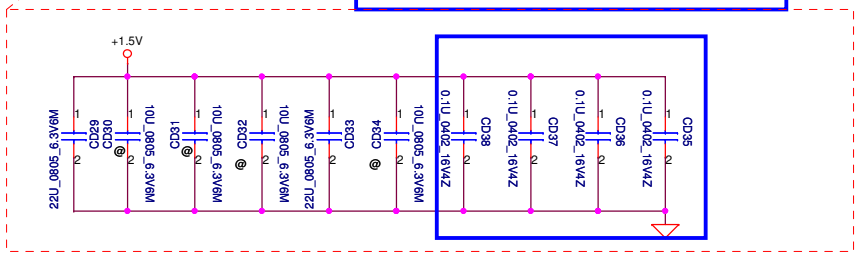
DDR3 SO-DIMM B
REVERSE TYPE

DDR_B_DQS[0..7] <9>
DDR_B_DQS#[0..7] <9>
DDR_B_D[0..63] <9>
DDR_B_DM[0..7] <9>
DDR_B_MA[0..14] <9>

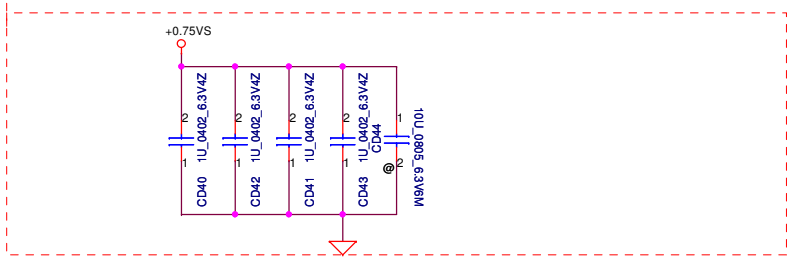


Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDDRL.203 & JDDRL.204



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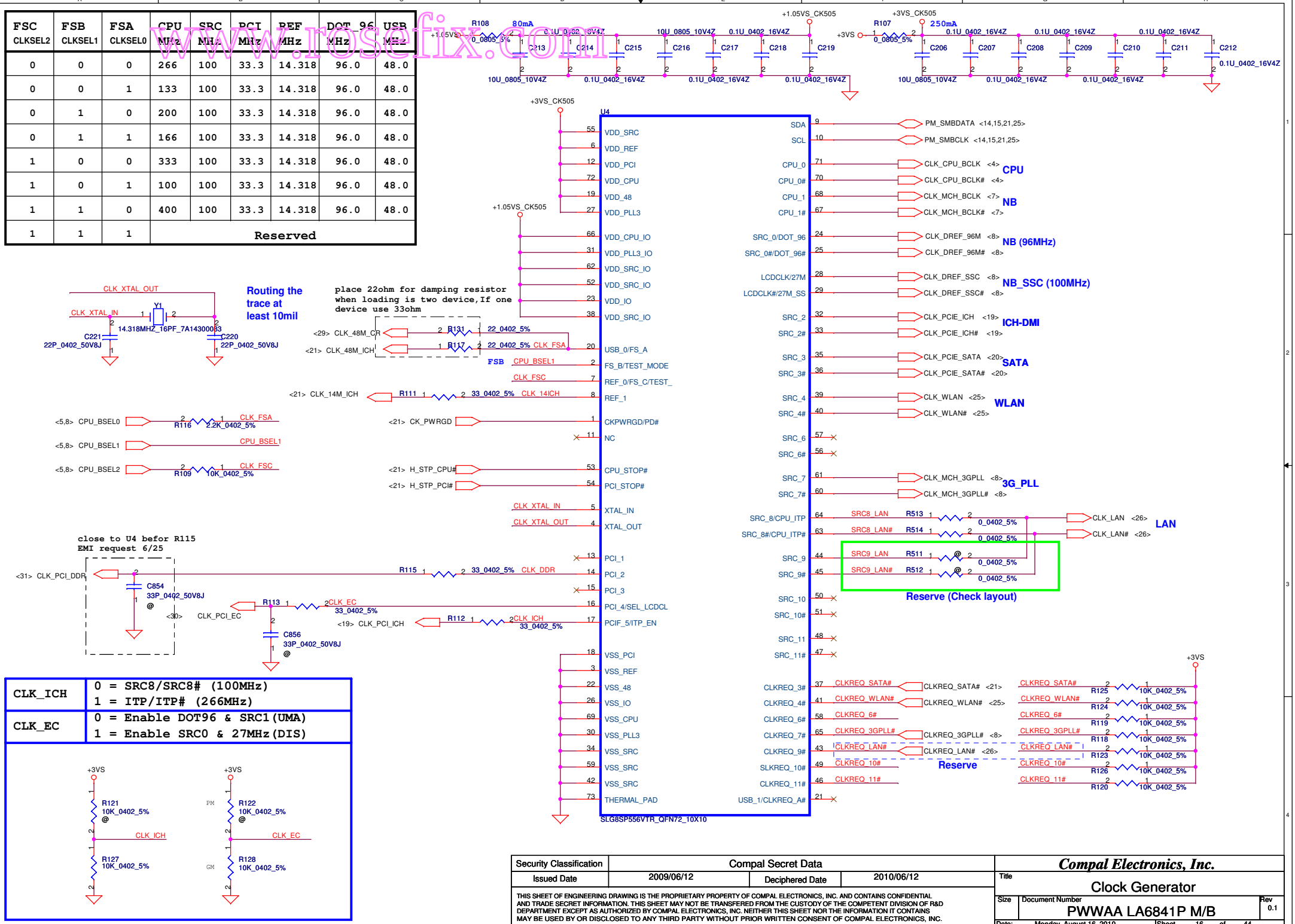
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



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Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: Clock Generator

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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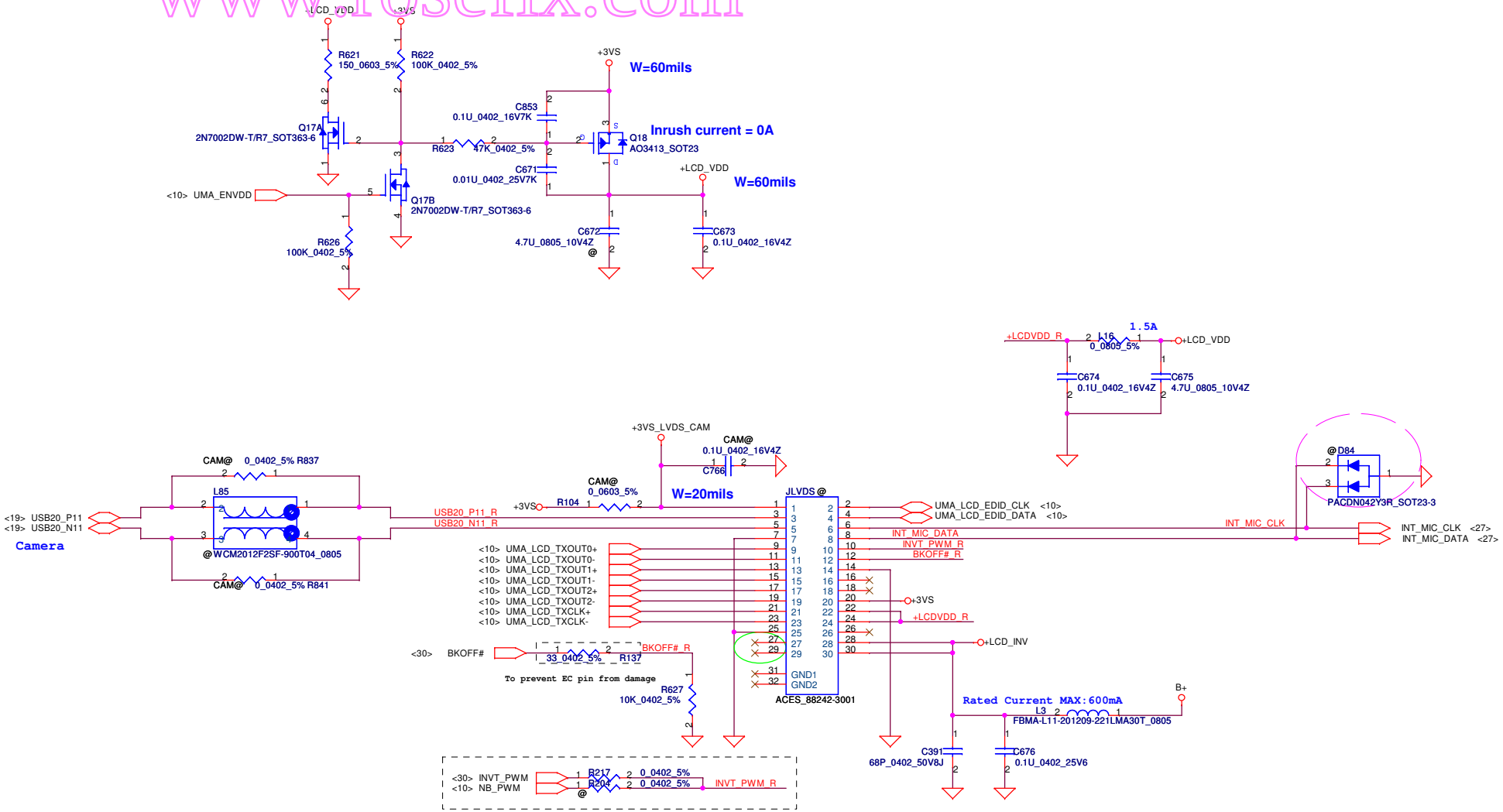
LCD/PANEL BD. Conn.



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Compal Electronics, Inc.

Title: NB9M GDDR2A

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CRT CONNECTOR

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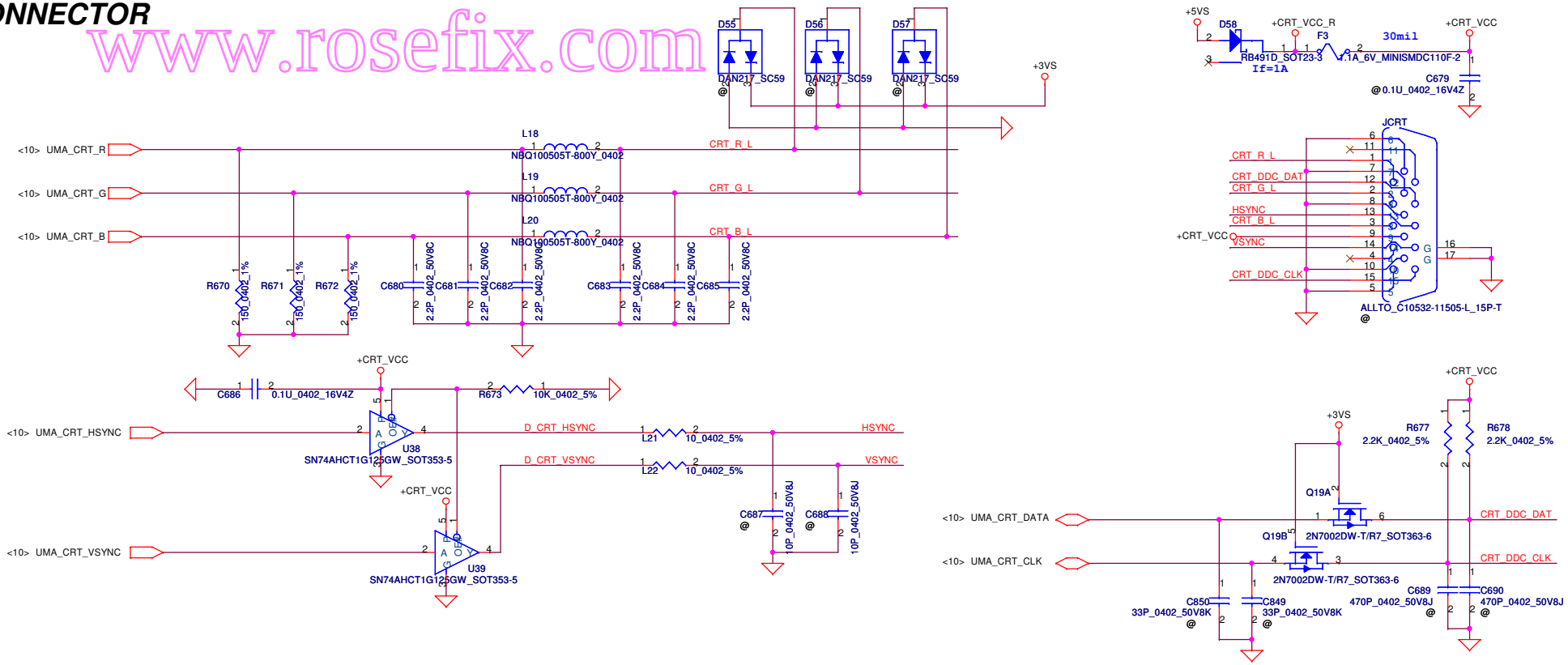

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Compal Electronics, Inc.

Title: CRT\TV\LVDS

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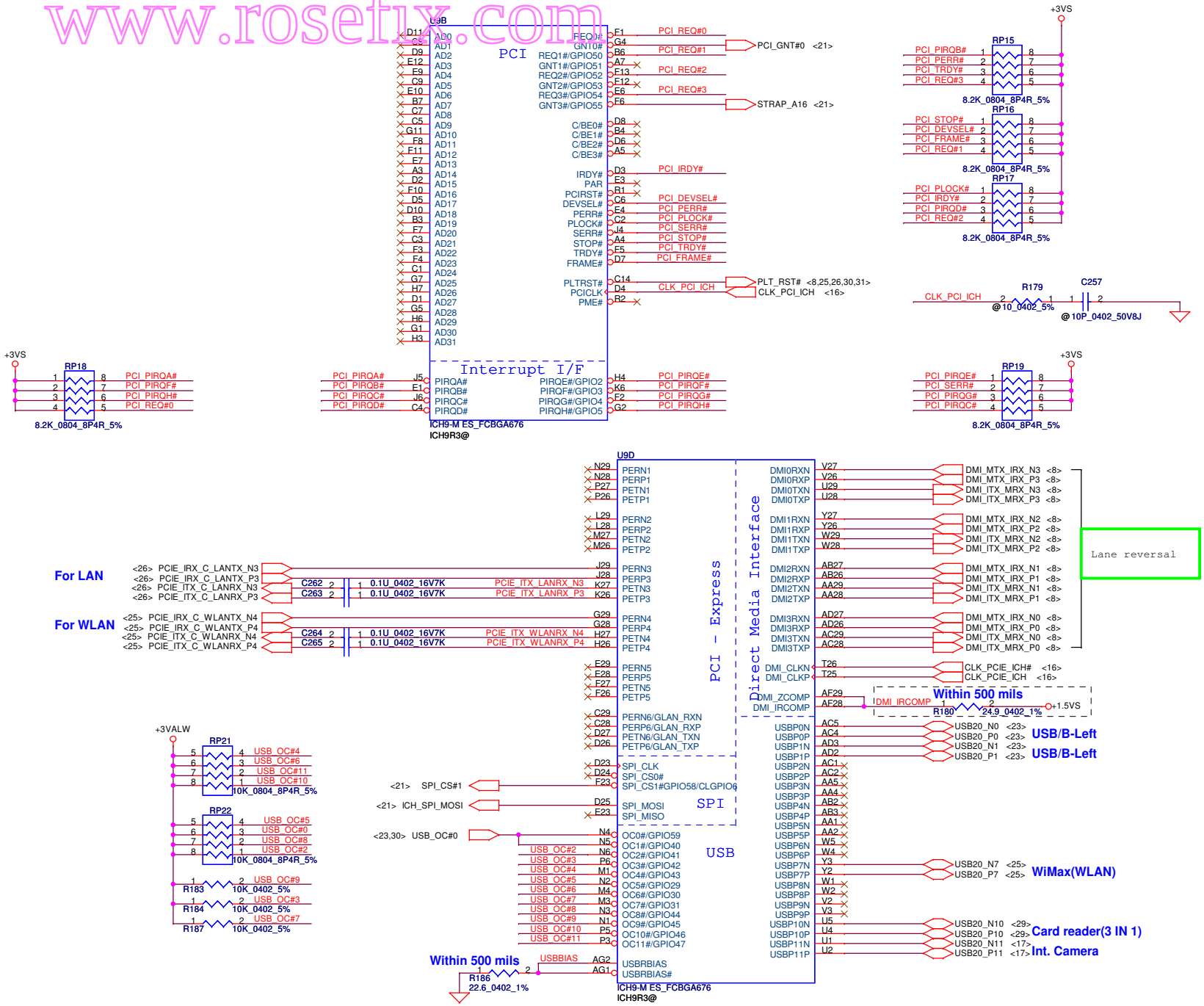

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Compal Electronics, Inc.

Title: ICH9M(1/4)-PCI

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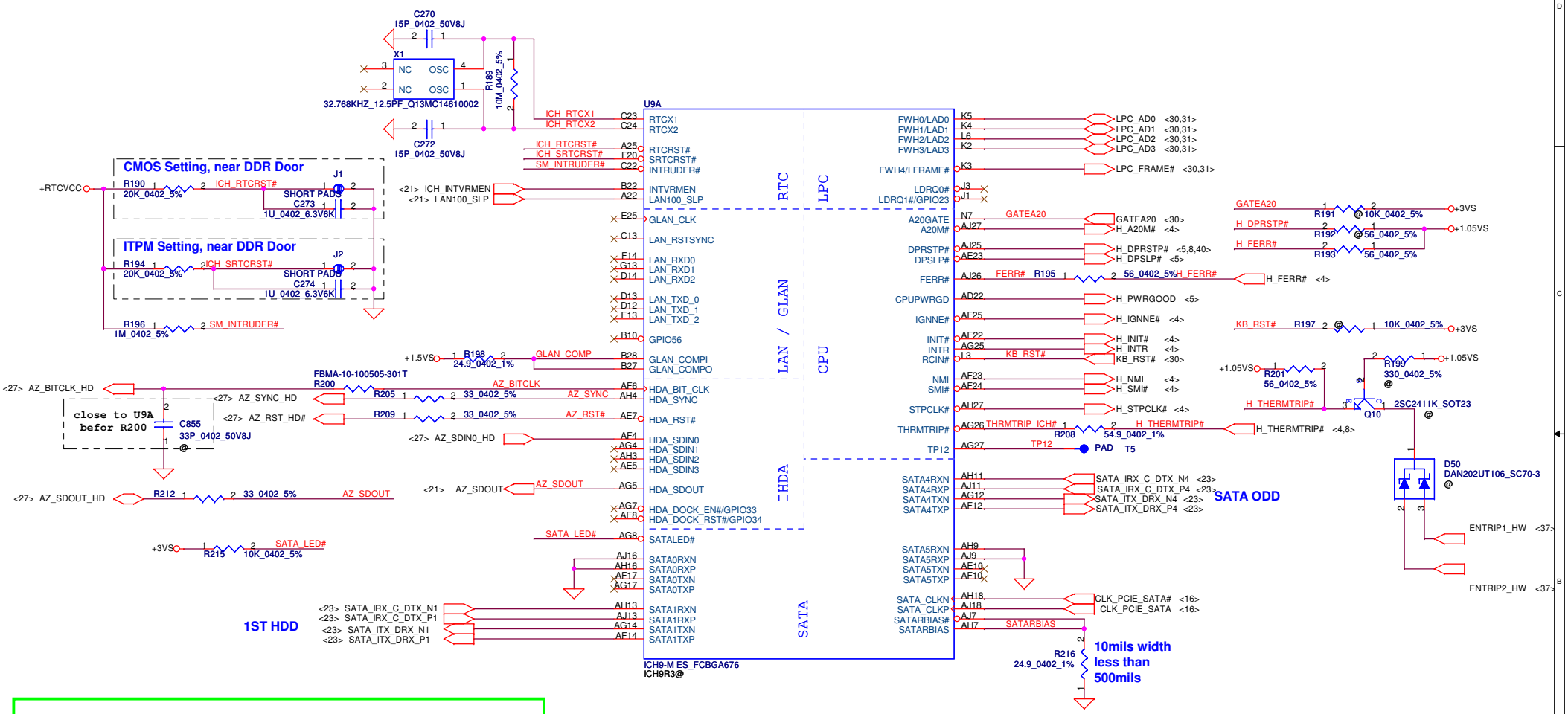

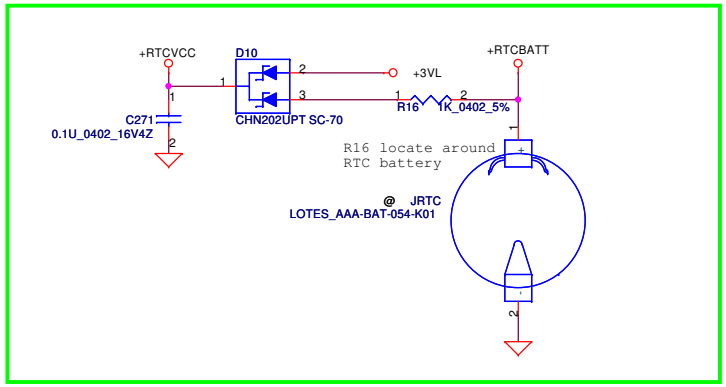

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Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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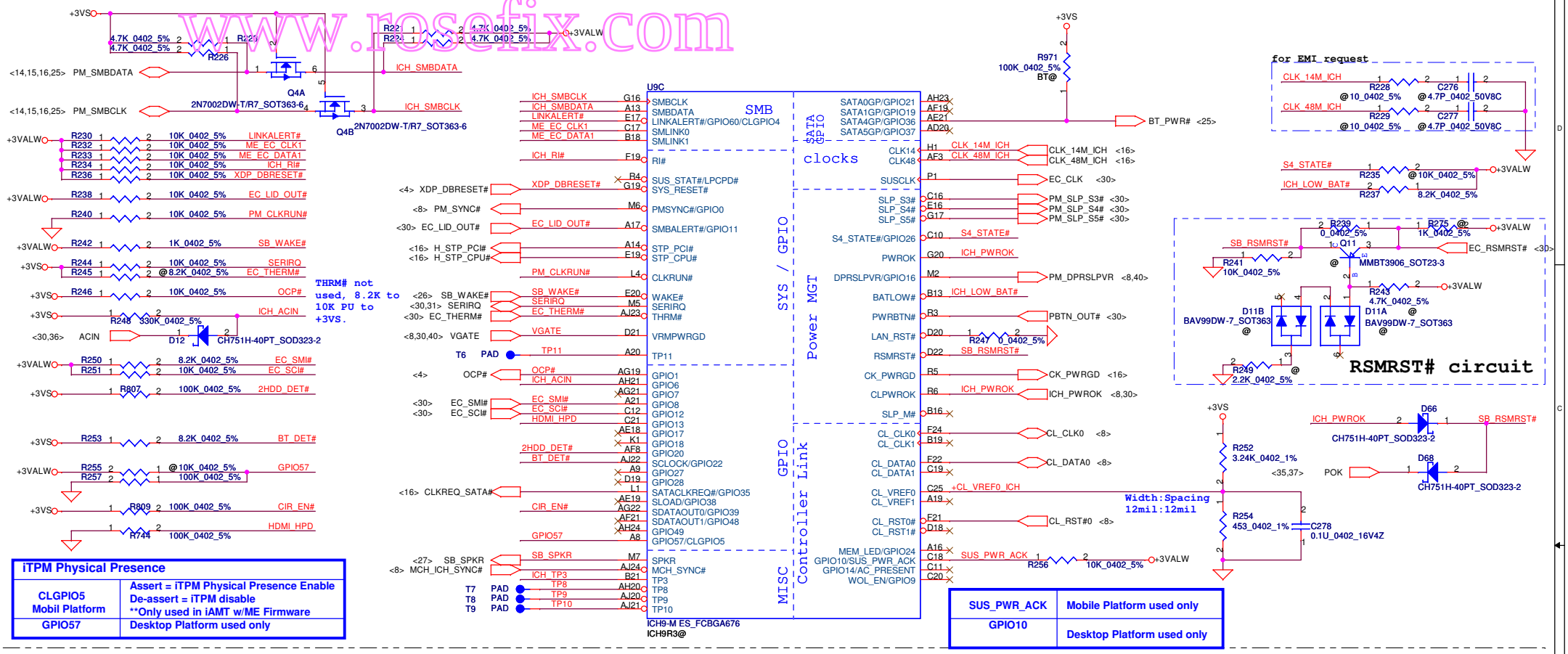
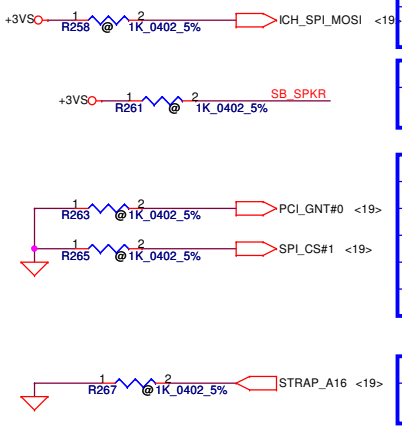


iTPM Physical Presence	
CLGPIO5 Mobil Platform	Assert = iTPM Physical Presence Enable De-assert = iTPM disable **Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

SUS_PWR_ACK	Mobile Platform used only
GPIO10	Desktop Platform used only

ICH9M Strap Pin

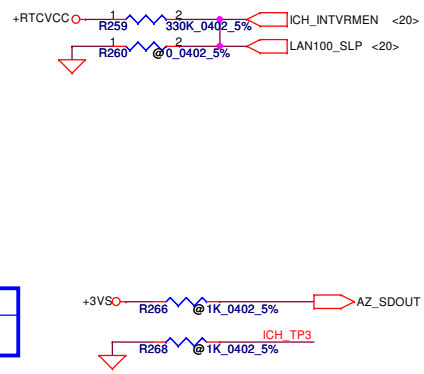


Internal TPM Strap(Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size | Document Number: PWWAA LA6841P M/B | Rev 0.1

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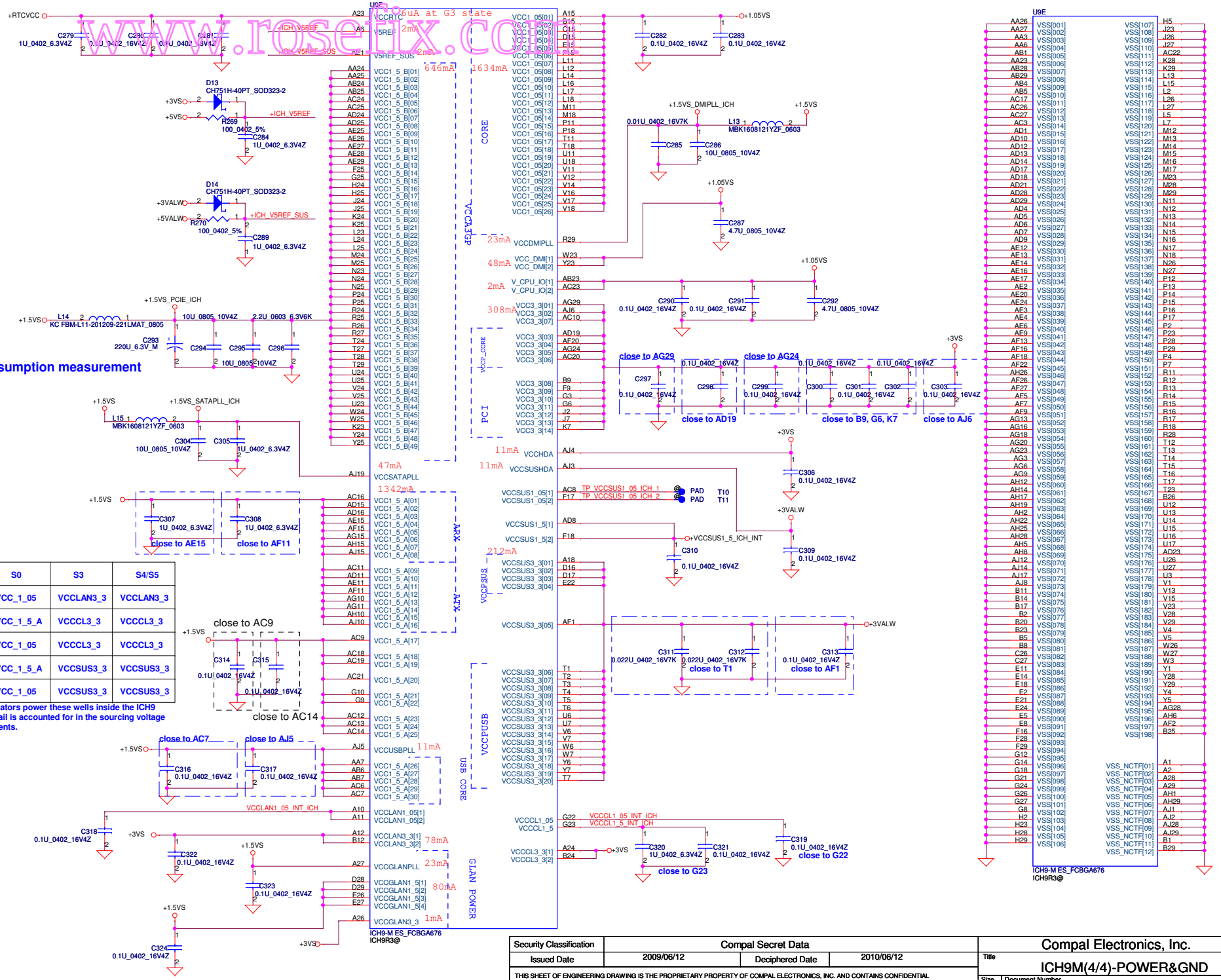

Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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SATA HDD Conn.

Place closely JHDD SATA CONN.

+5VS 1.2A

C697 10U_0805_10V4Z, C698 0.1U_0402_16V4Z, C699 0.1U_0402_16V4Z, C700 0.1U_0402_16V4Z

JHDD — SANTA_191201-1 CONN@ (this is temp. footprint)

Pin	Signal	Capacitor	Value	Net
2	SATA_ITX_C_DRX_P1	C713	0.01U_0402_25V7K	SATA_ITX_DRX_P1 <20>
3	SATA_ITX_C_DRX_N1	C715	0.01U_0402_25V7K	SATA_ITX_DRX_N1 <20>
5	SATA_IRX_DTX_N1	C717	0.01U_0402_25V7K	SATA_IRX_C_DTX_N1 <20>
6	SATA_IRX_DTX_P1	C719	0.01U_0402_25V7K	SATA_IRX_C_DTX_P1 <20>

V33 V33 V33 → +3VS; V5 V5 V5 → +5VS

SATA ODD Conn

Place components close to ODD CONN.

+5VS 1.1A

C721 10U_0805_10V4Z, C722 10U_0805_10V4Z, C723 @ 1U_0402_6.3V4Z, C724 0.1U_0402_16V4Z, C725 0.1U_0402_16V4Z

JODD — SANTA_206401-1_RV CONN@

Pin	Signal
2	SATA_ITX_C_DRX_P4_ODD
3	SATA_ITX_C_DRX_N4_ODD
5	SATA_IRX_DTX_N4_ODD
6	SATA_IRX_DTX_P4_ODD

DP +5V +5V MD → +5VS

Capacitor	Value	Net
C733	0.01U_0402_25V7K	SATA_ITX_DRX_P4 <20>
C734	0.01U_0402_25V7K	SATA_ITX_DRX_N4 <20>
C735	0.01U_0402_25V7K	SATA_IRX_C_DTX_N4 <20>
C736	0.01U_0402_25V7K	SATA_IRX_C_DTX_P4 <20>

+5VALW — U42 G528_SO8 — 1.4A — +USB_VCCA W=60mils

<30> USB_EN# — USB_OC#0 <19,30>

C693 1000P_0402_50V7K For EMI request

C752 4.7U_0805_10V4Z @

USB Conn

+USB_VCCA

C84 220U_6.3V_M, C63 0.1U_0402_16V4Z, C64 1000P_0402_50V7K

<19> USB20_N0 <19> USB20_P0 — @WCM2012F2SF-900T04_0805 L87 — <BOM Structure> 0402_5% — USB20_N0_R USB20_P0_R

JUSB1 @ ALLTOP C107L8-10405-L — W=60mils

D65 @ PJDLC05_SOT23-3

<19> USB20_N1 <19> USB20_P1 — @WCM2012F2SF-900T04_0805 L86 — R842 — USB20_N1_R USB20_P1_R

C60 0.1U_0402_16V4Z, C61 1000P_0402_50V7K

JUSB2 @ ALLTOP C107L8-10405-L — W=60mils

D62 @ PJDLC05_SOT23-3

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Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB

Size | Document Number: PWWAA LA6841P M/B | Rev 0.1

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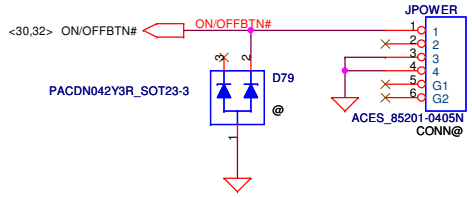
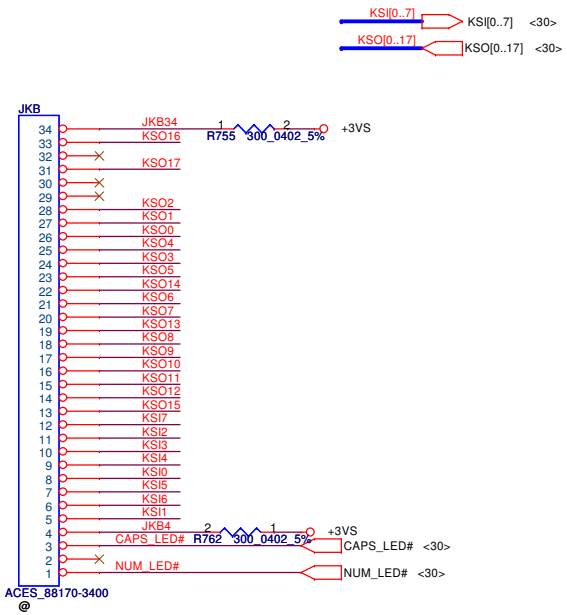
POWER/B Connector

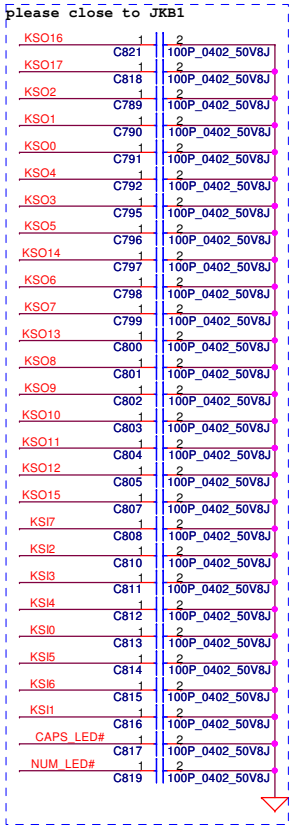
Check footprint and pin define



KEYBOARD CONN

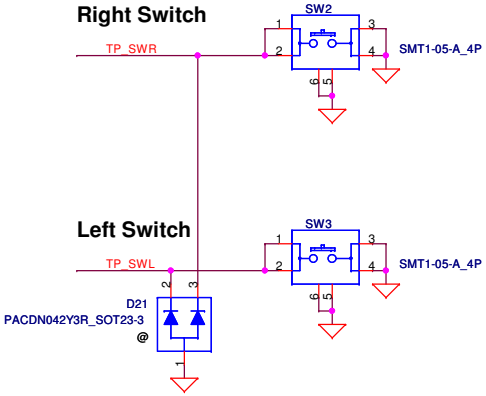


please close to JKB1



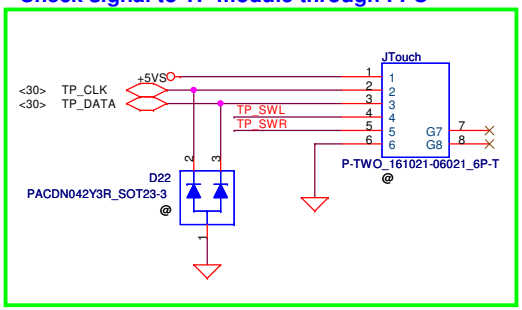
Touch/B Connector

Right Switch



Left Switch

Check signal to TP module through FFC



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Compal Electronics, Inc.

Title: USB/BT/FP/Int. Cam

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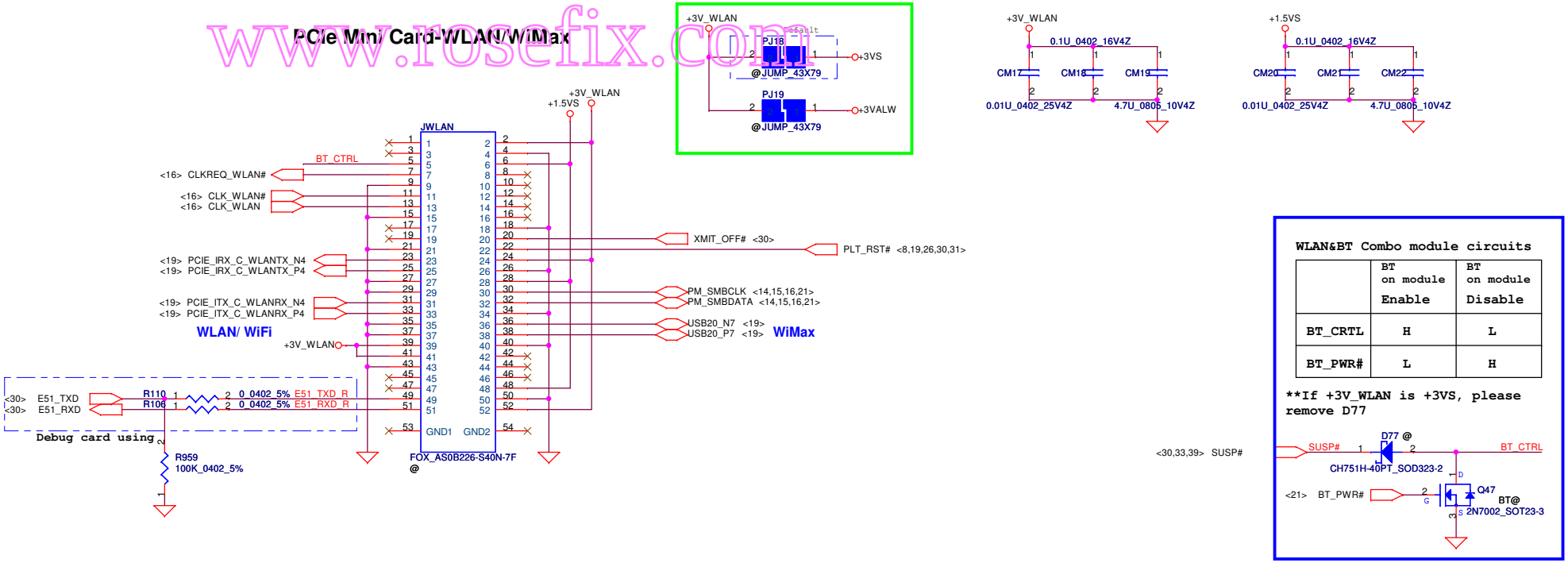
PCIe Mini Card-WLAN/WiMax



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove D77

Add BT_CTRL for WLAN & BT Combo module at DVT

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Compal Electronics, Inc.

Title: PCIe-WLAN/HDDVD/NAND/NEW

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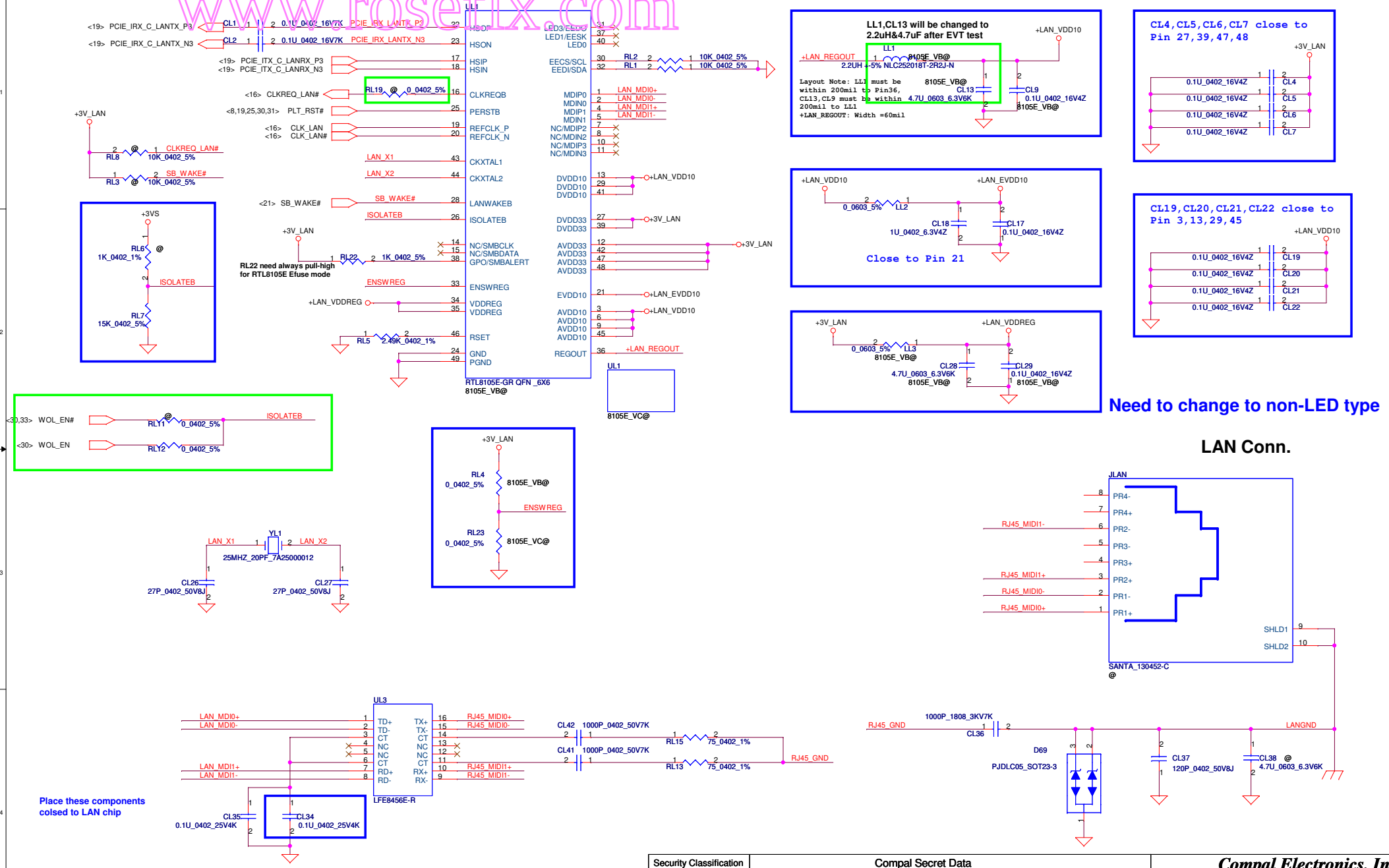

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Compal Electronics, Inc.

Title: **RTL8105E 10/100 LAN**

Size: Custom | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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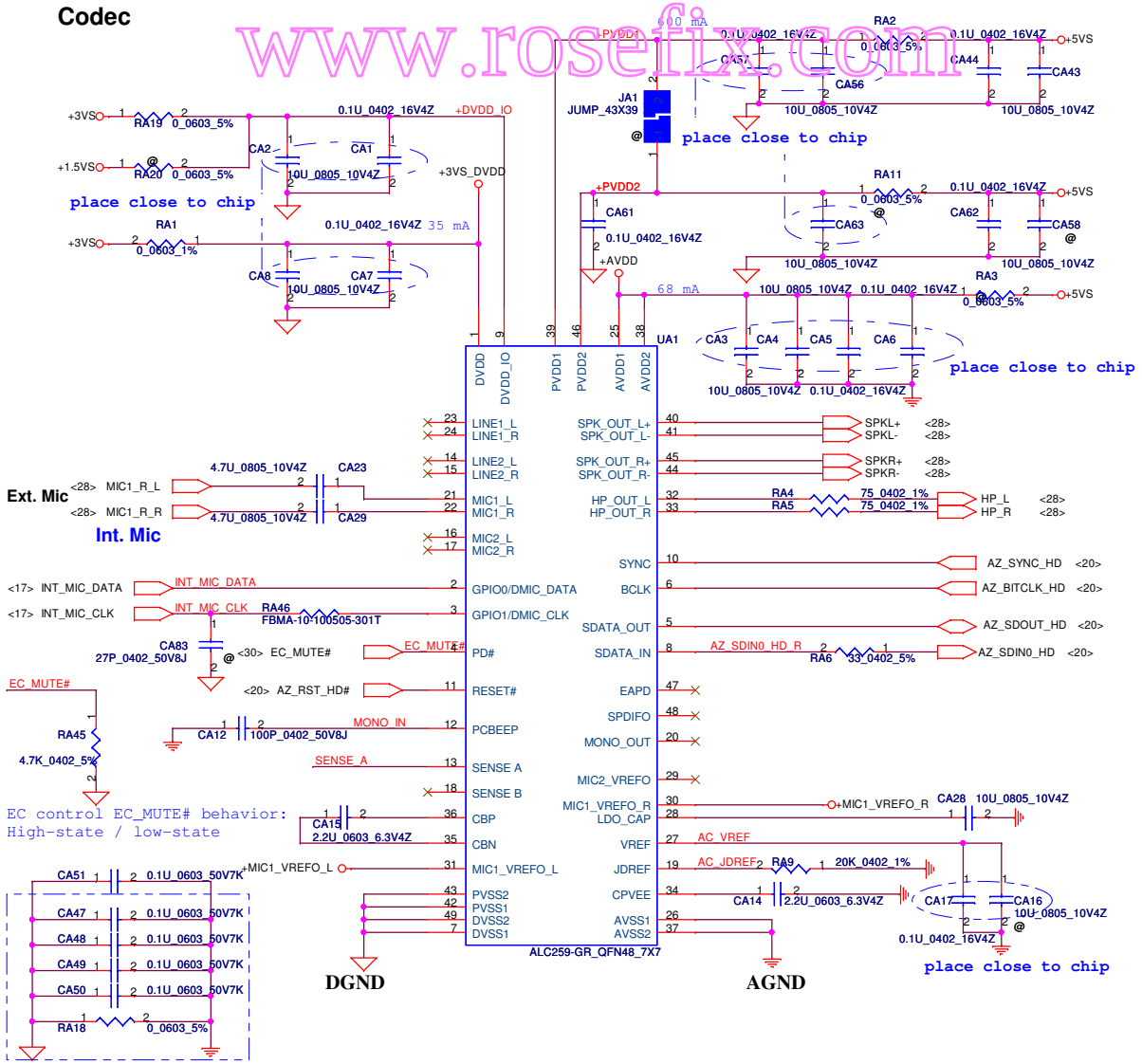
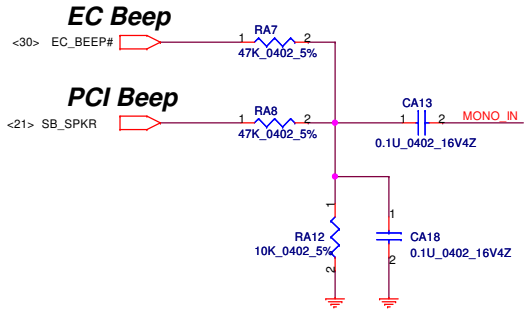
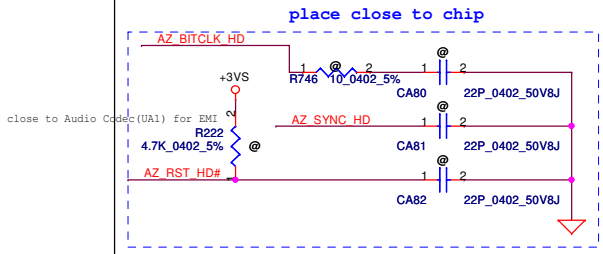
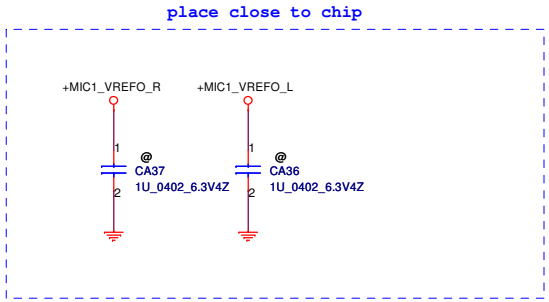
Codec



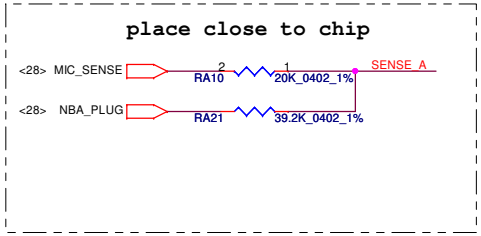
Beep sound







Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



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Compal Electronics, Inc.

Title: HD CODEC ALC272

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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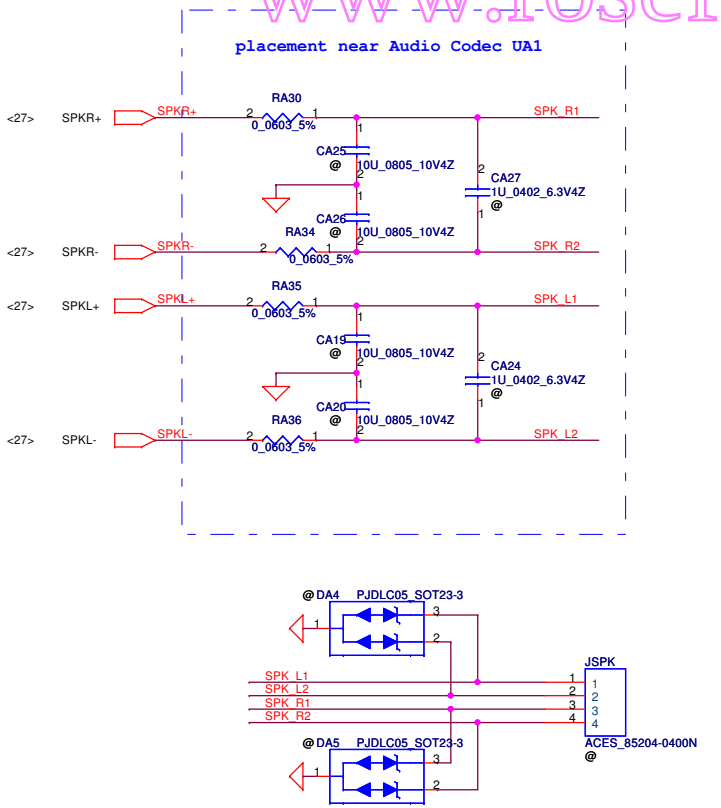
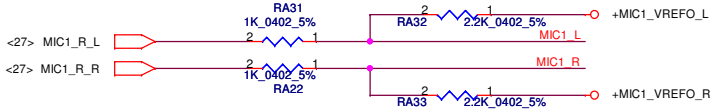
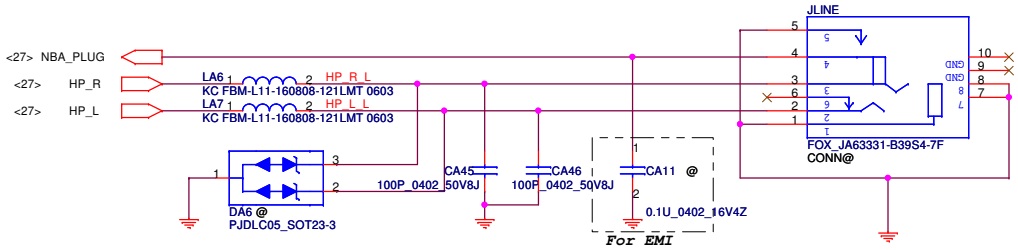
Speaker Connector



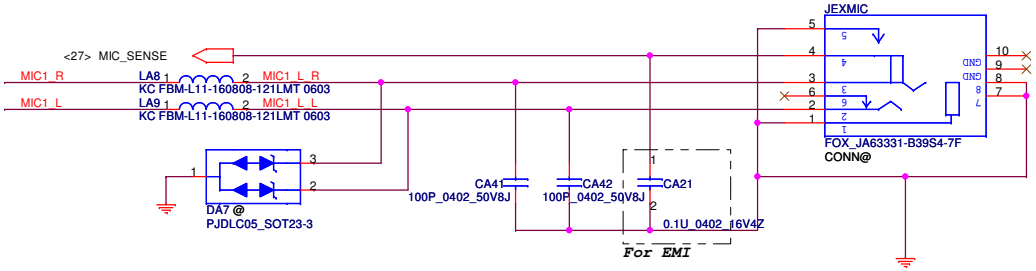
Ext. Mic



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



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Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: AUDIO AMP/MIC/SPK/VR

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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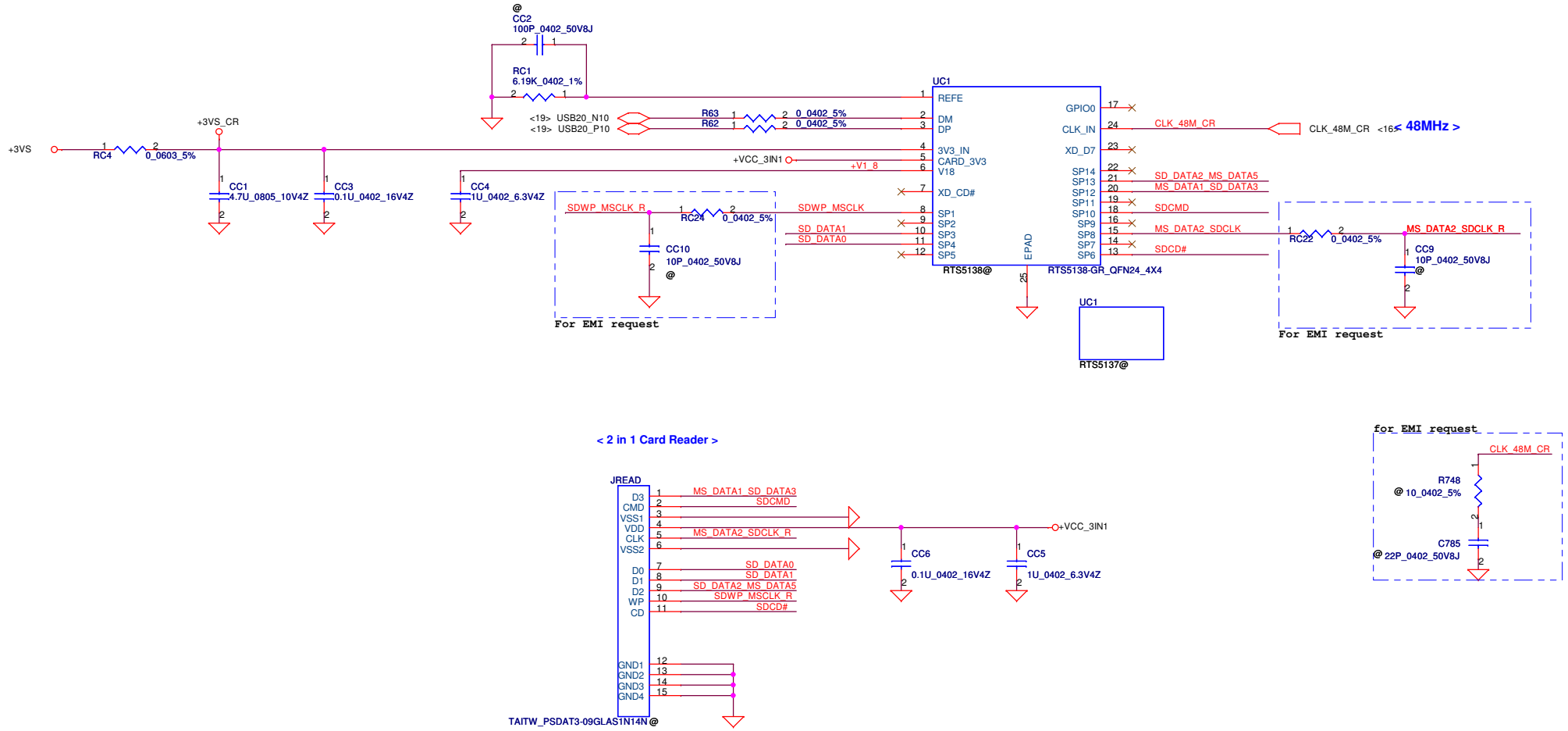

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Issued Date	2009/10/01	Deciphered Date	2010/10/01

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Compal Electronics, Inc.

Title: **RTS5138 Card Reader**

Size: Custom | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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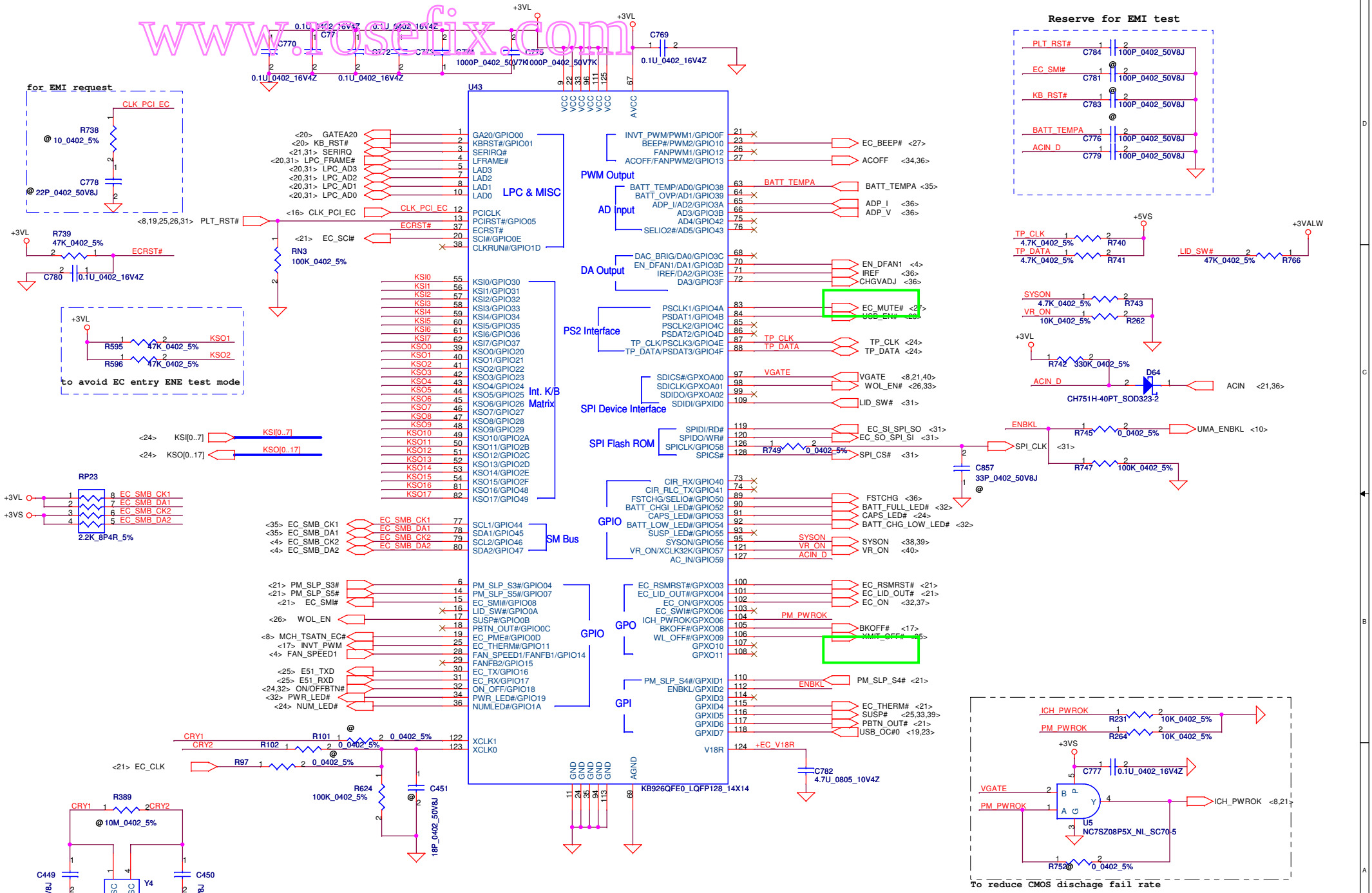

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Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: ENE-KB926 RevD2

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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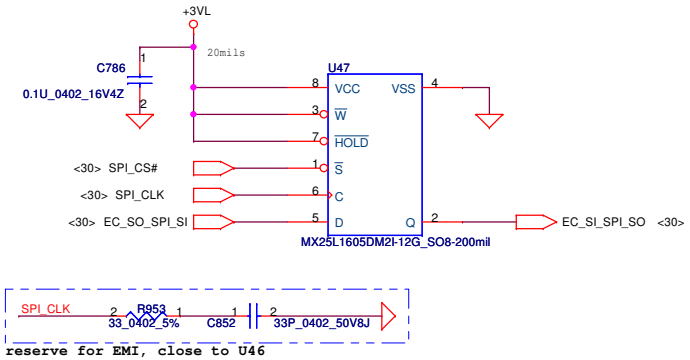
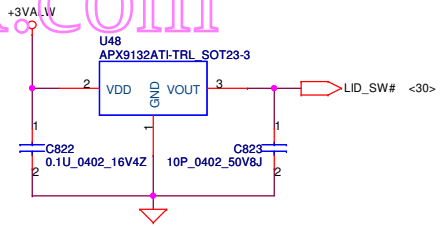
SPI Flash (16Mb*1)

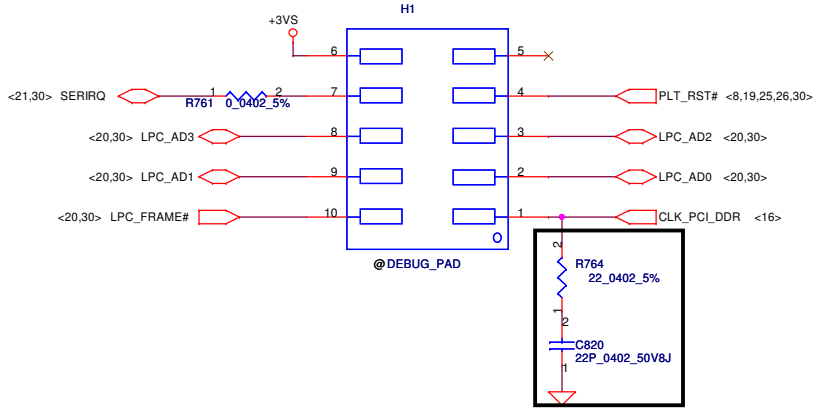


Lid SW

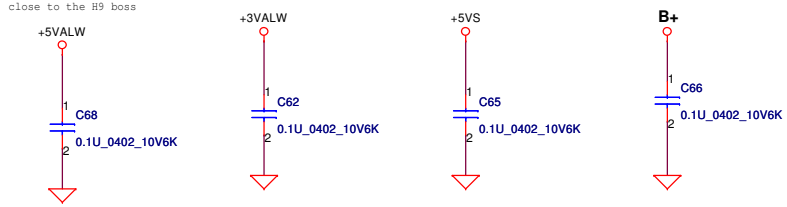


LPC Debug Port

Please place the PAD under DDR DIMM.



for EMI



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Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: SPI ROM/TP/KB/Debug

Size | Document Number: PWWAA LA6841P M/B | Rev: 0.1

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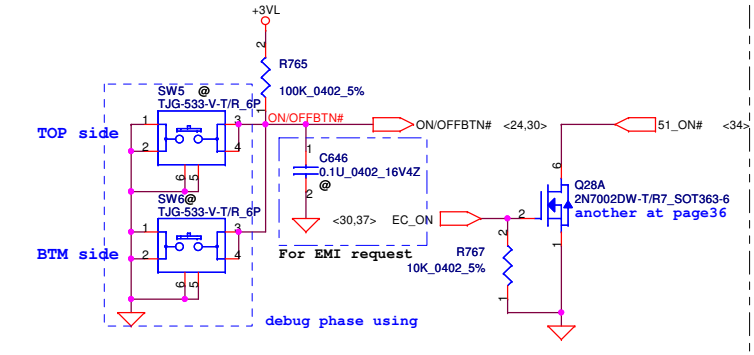
Power Button



ISCD

PCB

ZZZ
DAZ0HE00100

DC-IN

PJP1
PJP1
45@

NB_GL40_R3

U3
CANTIGA GL40
GL40R3@

NB_GL40_R1

U3
CANTIGA GL40
GL40R1@

NB_GM45_R1

U3
CANTIGA GM45
GM45R1@

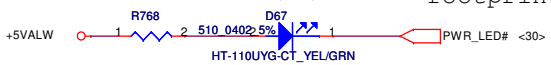
SB_R1

U9
ICH9-M ES
ICH9R1@

DC-IN LED

Vf=2.0V(typ),2.4V(max)
If=30mA(max)

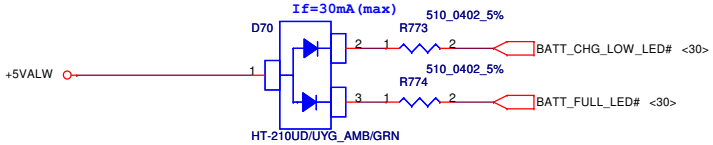
footprint is SC510UYG000



BATT CHARGE/FULL LED

Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

footprint is SC510UDG000



Screw Hole

H5 H_3P0 @
H6 H_3P0 @
H8 H_3P0 @
H9 H_3P0 @
H10 H_3P0 @
H11 H_3P0 @
H12 H_3P0 @
H13 H_3P0 @
H14 H_3P0 @
H2 H_2P7x3P2N @
H26 H_2P7N @

CPU

H36 H_3P7 @
H33 H_3P7 @
H34 H_3P7 @
H35 H_3P7 @

SB

H15 H_5P0N @
H16 H_5P0N @

MINI CARD

H18 H_3P3 @
H19 H_3P3 @

PCB Fedical Mark PAD

FD1 @
FD2 @
FD3 @
FD4 @

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS

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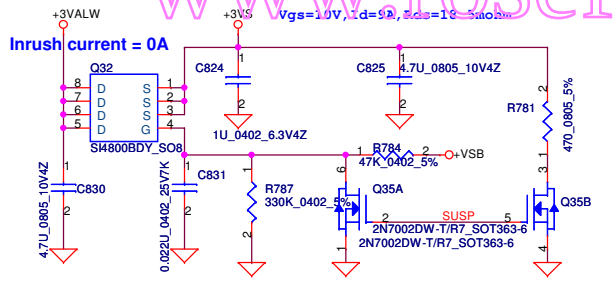
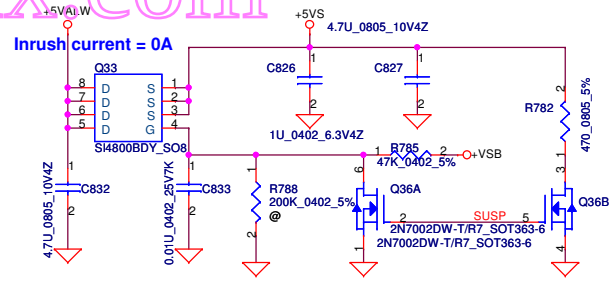
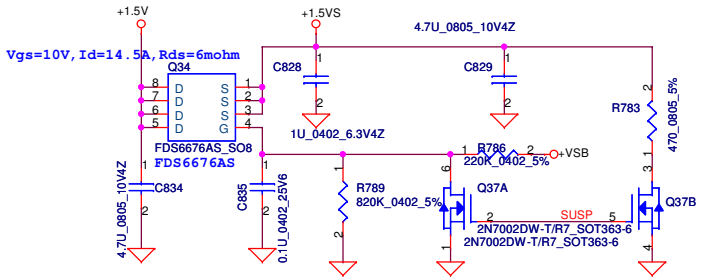
+3VALW TO +3VS



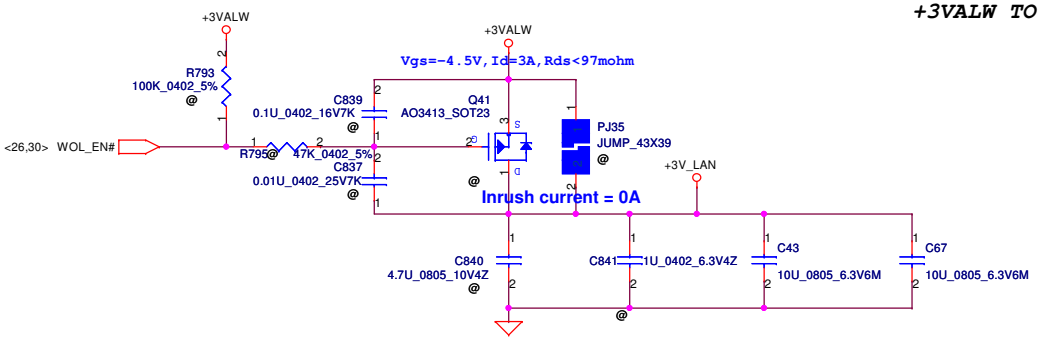
+5VALW TO +5VS



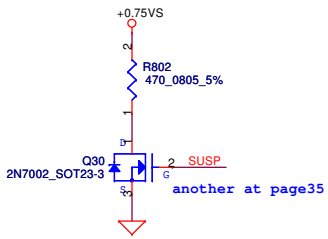
+1.5V to +1.5VS

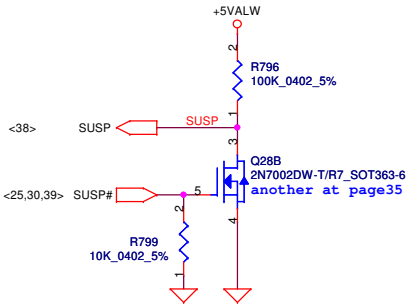


+3VALW TO +3V_LAN



+3VALW TO +3V_SB





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Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: PSWAA LA6511P M/B | Rev: 0.1

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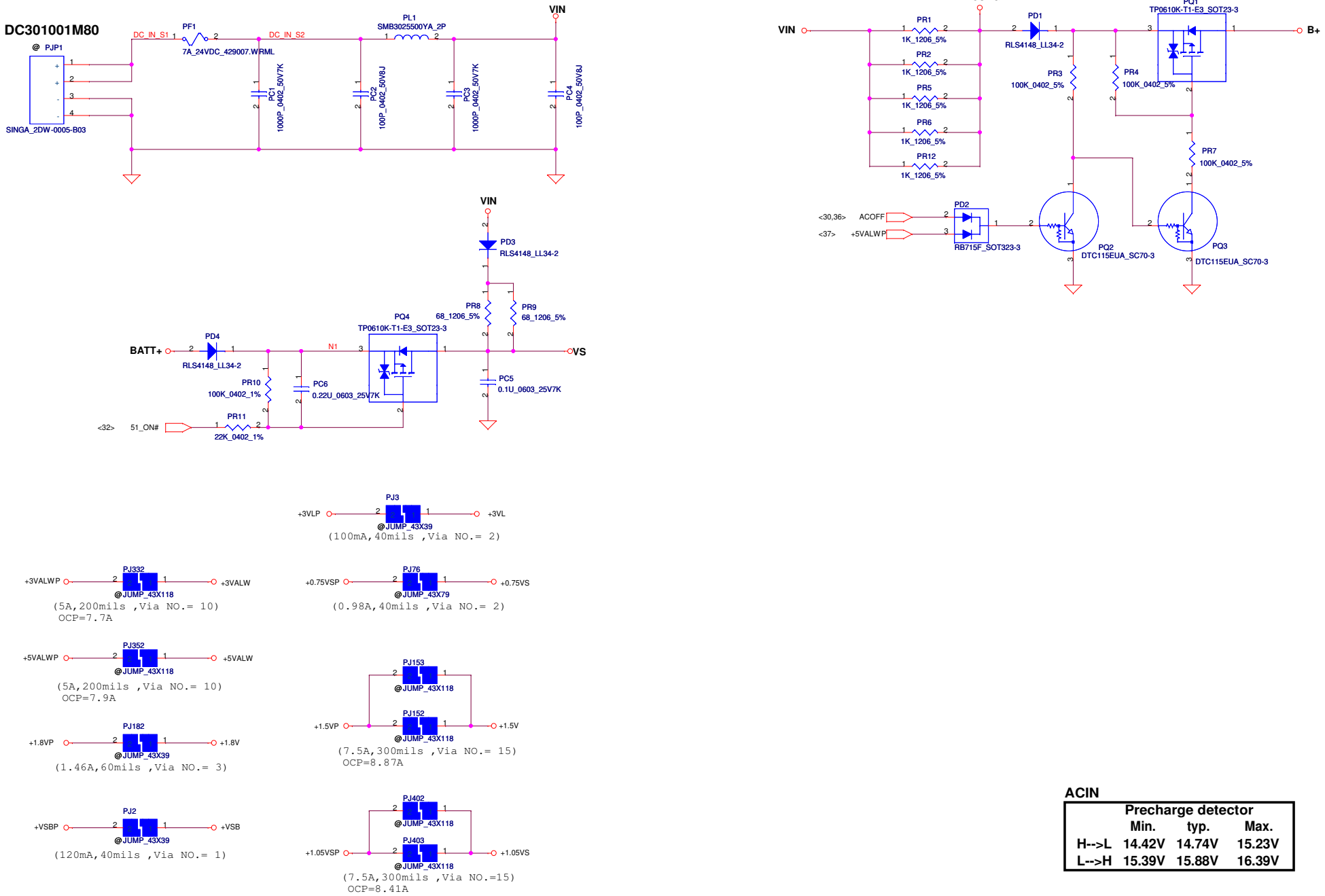

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size | Document Number: KSWAA | Rev: 0.1

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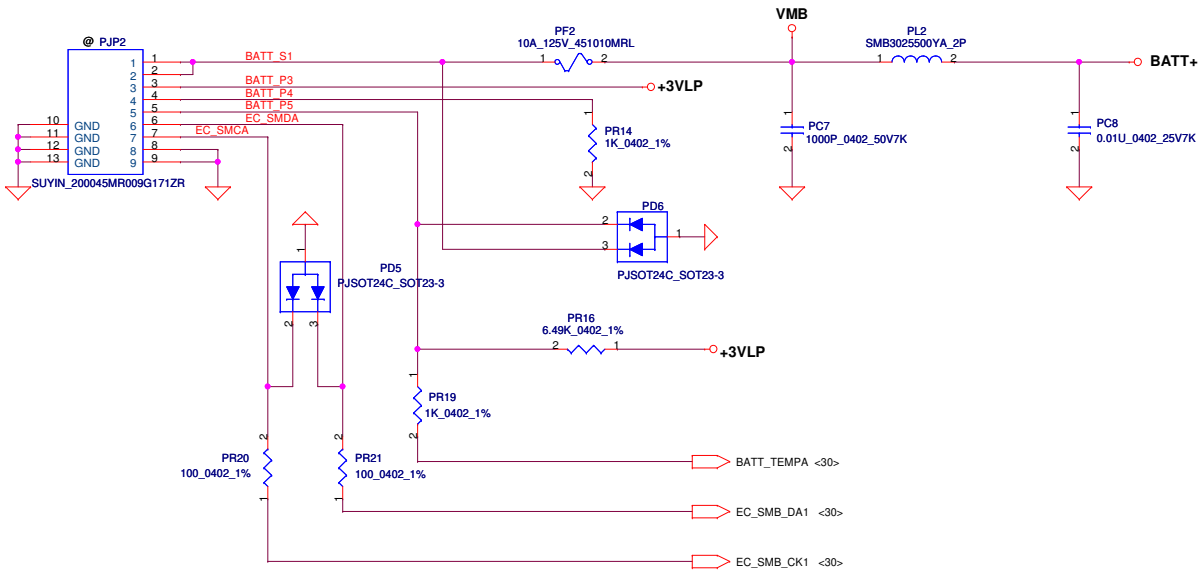
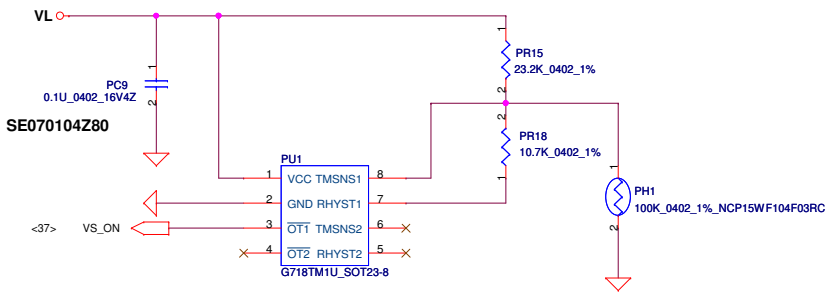


PH1 under CPU botten side :

CPU thermal protection at 90 degree C

Recovery at 56 degree C



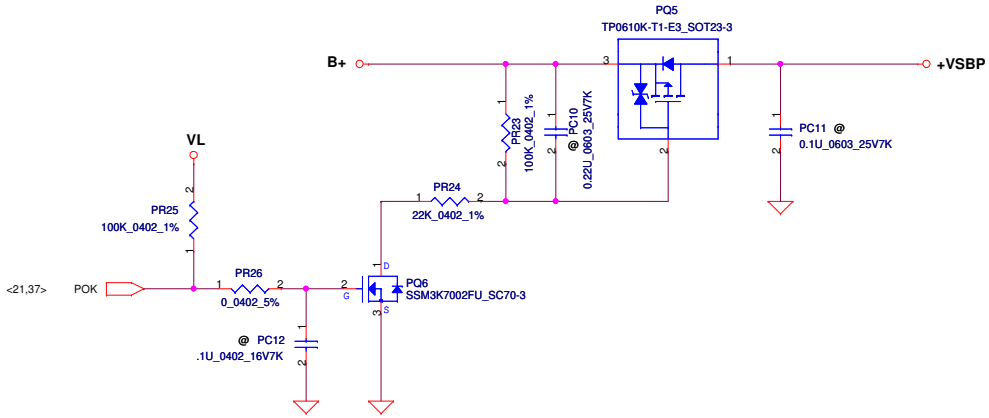
Rset = 3 * Rtmh

Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.79K, Rtml at 56C = 26.1K

Rset = 3 * 7.79K = 23.37K ==> 23.2K

Rhyst = (23.2K * 26.1K) / (3 * 26.1K - 23.2K) = 10.99K ==> 10.7K



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Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number: KSWAA | Rev: 0.1

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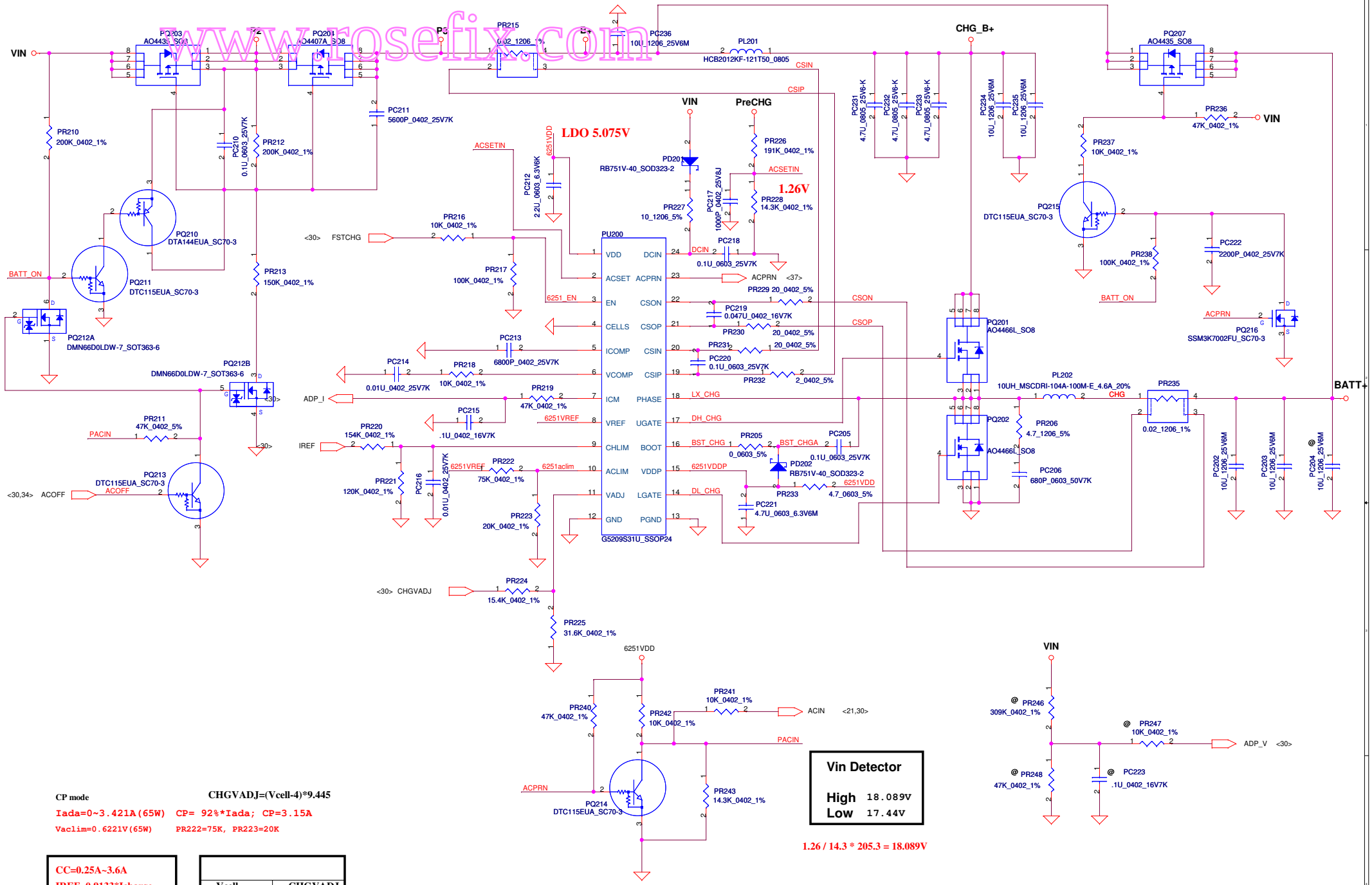

Vin Detector

High	18.089V
Low	17.44V

1.26 / 14.3 * 205.3 = 18.089V

CP mode

Iada=0~3.421A(65W) CP= 92%*Iada; CP=3.15A

Vaclim=0.6221V(65W) PR222=75K, PR223=20K

CHGVADJ=(Vcell-4)*9.445

CC=0.25A~3.6A

IREF=0.9133*Icharge

IREF=0.228V~3.29V

VCHLIM need over 95mV

Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: Huron river | Rev: 0.1

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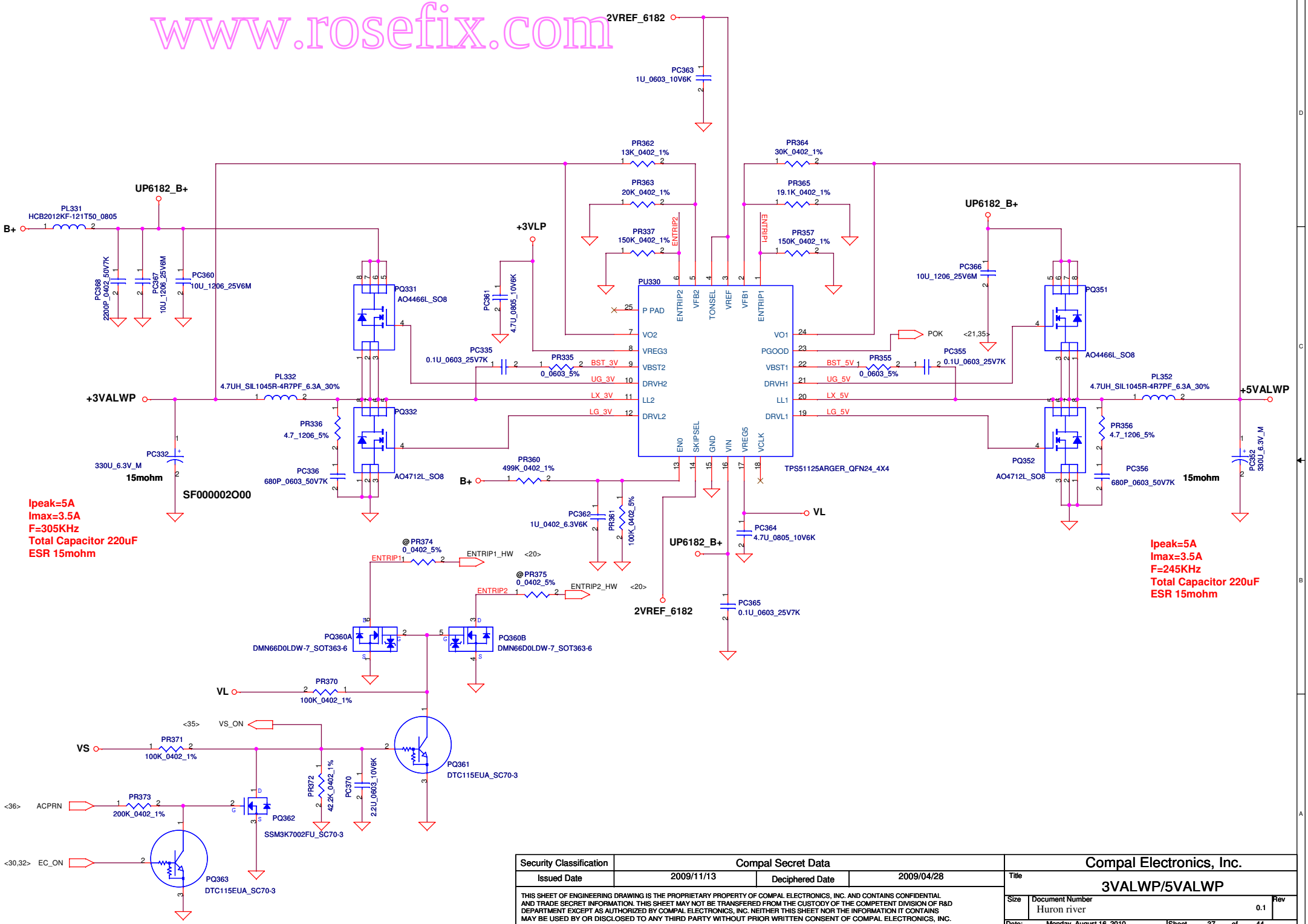

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size | Document Number: Huron river | Rev: 0.1

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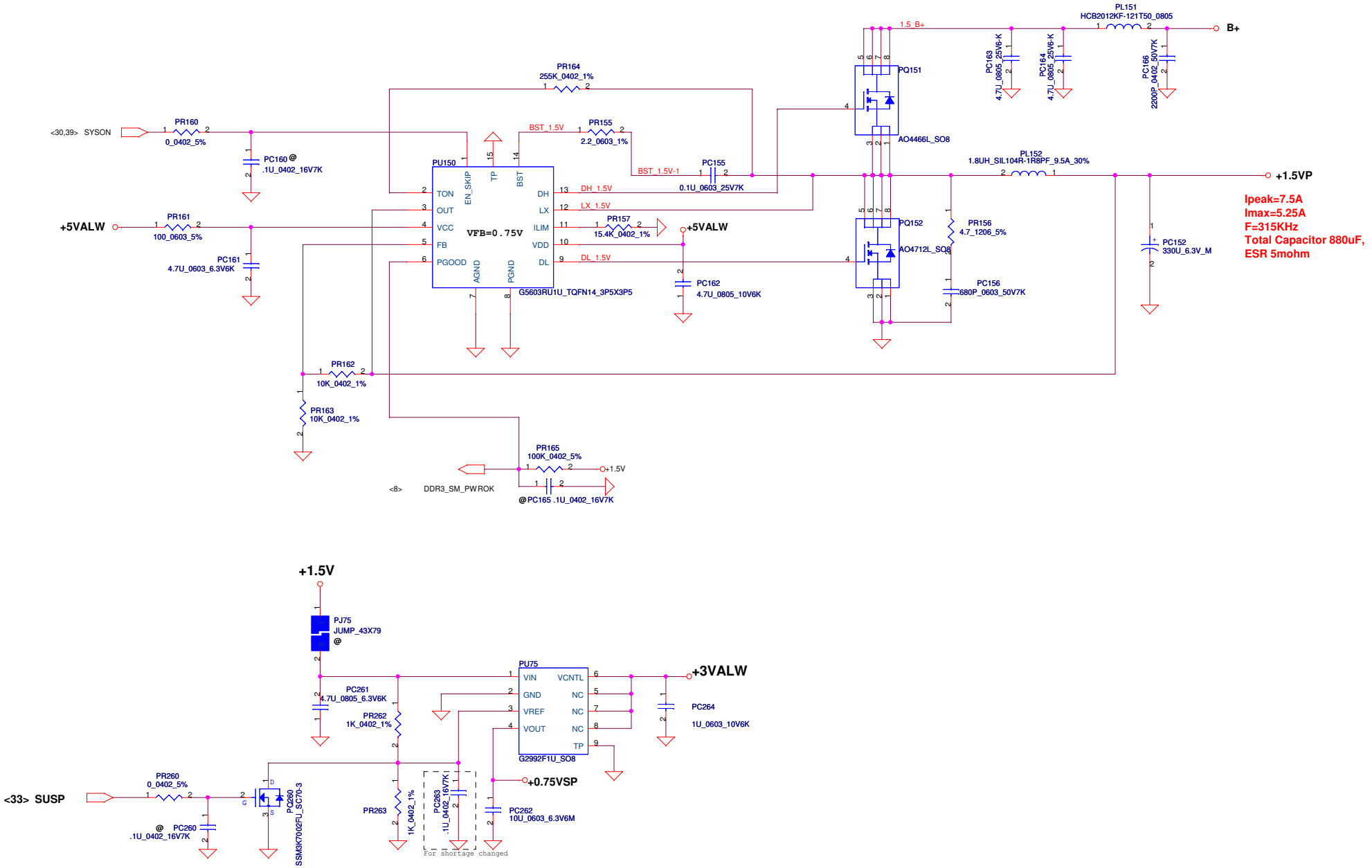

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: 1.8V / 1.5V / 0.75V

Size | Document Number: KSWAA | Rev: 0.1

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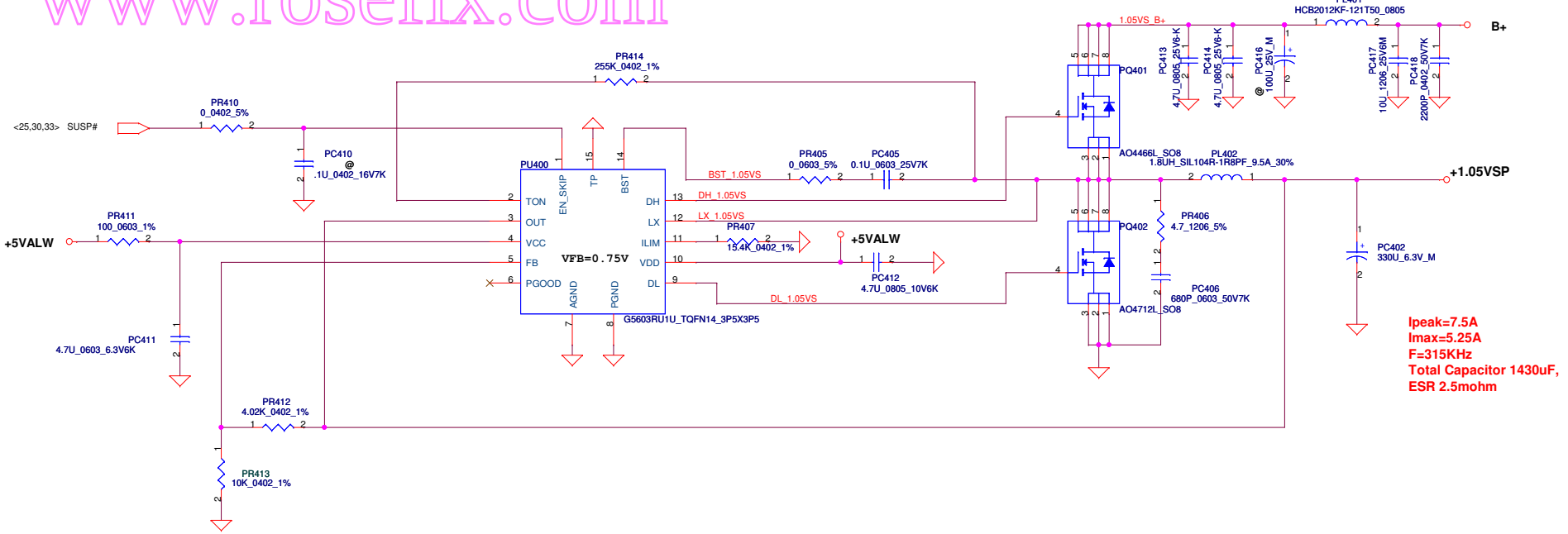

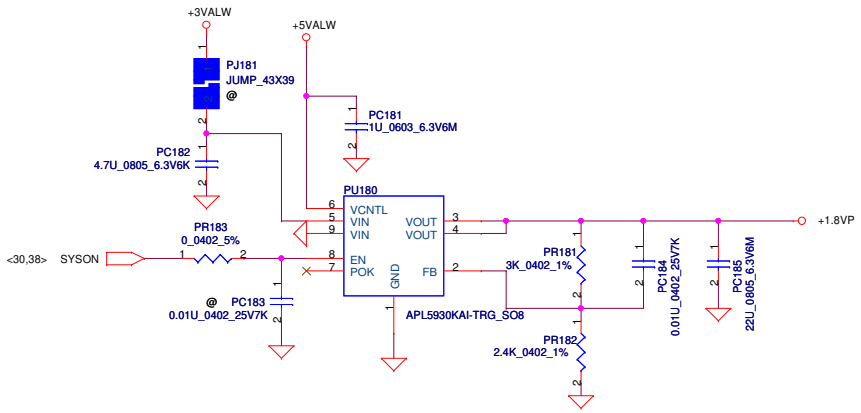

Security Classification	Compal Secret Data		
Issued Date	2009/06/12	Deciphered Date	2010/06/12

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Compal Electronics, Inc.

Title: 1.05V / 1.8V

Size | Document Number: KSWAA | Rev: 0.1

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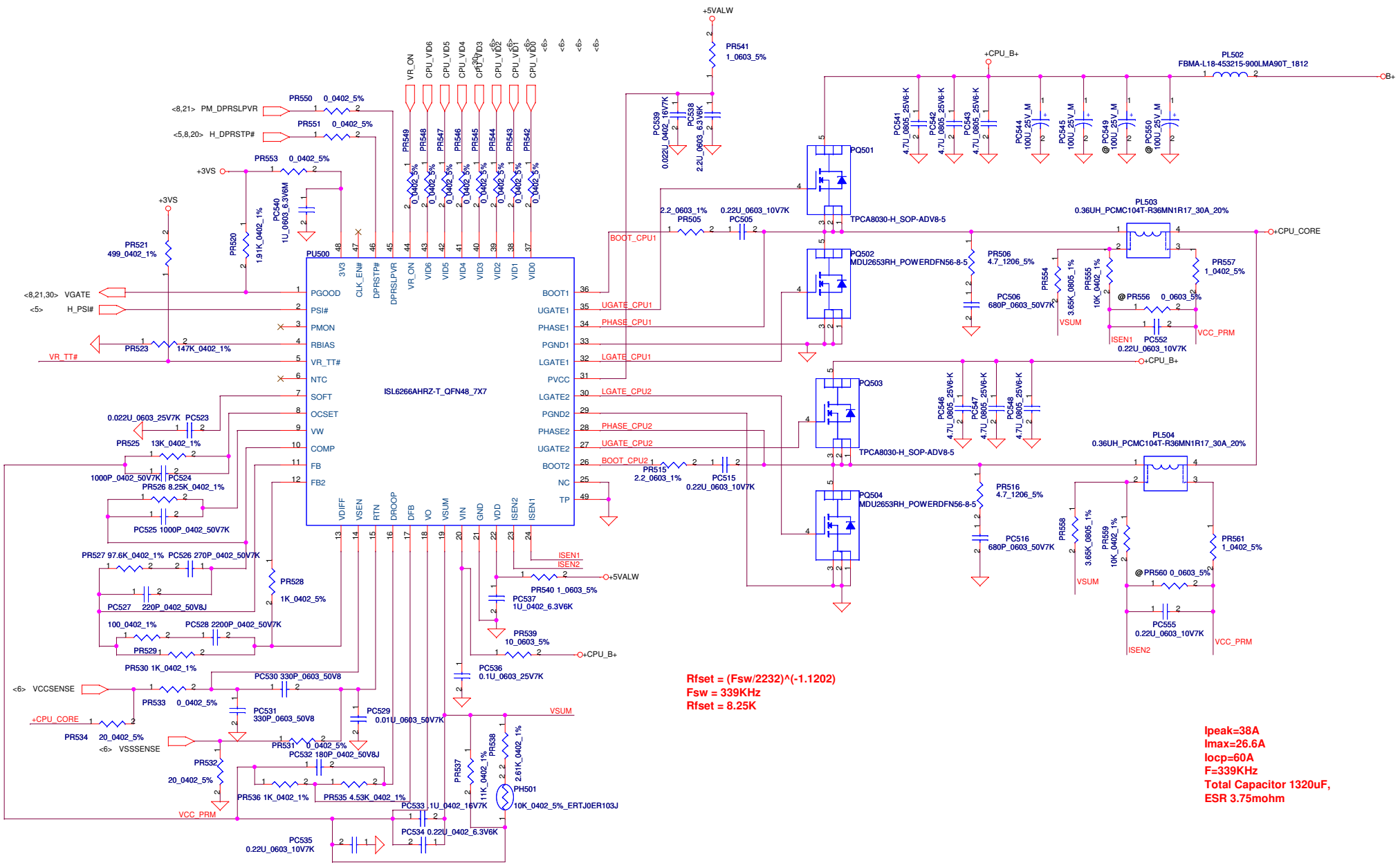

Rfset = (Fsw/2232)^(-1.1202)
Fsw = 339KHz
Rfset = 8.25K

Ipeak=38A
Imax=26.6A
Iocp=60A
F=339KHz
Total Capacitor 1320uF,
ESR 3.75mohm

Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

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Title: +CPU_CORE

Size: Custom | Document Number: KSWAA | Rev: 0.1

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PIR (Product Improve Record)

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REVISION CHANGE: 0.1 TO 0.2 EVT

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	07/23	32	Change R768,R773 from 120 ohm to 510 ohm	for changed 5mA LED
2.	07/23	32	Chage LED power rail from +3valw to +5valw	for changed 5mA LED
3.	07/23	23	del. L86,L87 EMI component	for EMI request
4.	07/23	31	Add 1PCS(C62) 0.1uF_0402 on +3Valw-->GND	for EMI request
5.	07/23	31	Add 1PCS(C65) 0.1uF_0402 on +5Vs-->GND	for EMI request
6.	07/23	31	Add 0.1uF_0402(C66) on B+-->GND close to H8	for EMI request
7.	07/23	28	JLINE and JEXMIC change from DC2300006300 to DC230004L00	for SMT DFx request
8.	07/27	30	change R742 from +3VALW to +3VL	for LED no function issue
9.	07/27	8	add test pad ON U3.E36,U3.AK34	for ATE request
10.	07/27	33	change part number of Q30 (SB770020010)	for Reduce BOM part type
11.	07/27	32	Change D67(power on LED) from SC510UYG000 to SC500009D00	for changed 5mA LED
12.	07/27	32	Change D70(DC in LED) from SC510UDG000 to SC500009800	for changed 5mA LED
13.	07/29	14	un-mount CD7,CD8,CD9,CD10,CD11,CD12,CD30,CD31,CD32,CD34,and mount(22uF) CD29,CD33	for design change
14.	07/29	11	For +1.5V ,C78 from 330uF to 390u (SF000002O00)	for design change
15.	07/29	12	Change R82 and R81 from inductor to Bead	for design change
16.	07/29	15	+0.75VS filter un-mount CD22 and CD44	for design change
17.	08/03	25	un-mount D77	for If +3V_WLAN is +3VS, please un-mount D77

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PIR (Product Improve Record)

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REVISION CHANGE: 0.2 TO 0.3 Pre-MP

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	08/09	29	Change net V1_8 to +v1_8	for power trace
2.	08/09	32	add R774	for LED control
3.	08/12	32	un-mount SW5 and SW6	for Pre-MP do need power SW
4.	08/12	20	add R16 (for RTC battery)	for design change
5.	08/13	26	add D69 and un-mount CL38	for EMI request
6.	08/13	26	CL37 from 0.1uF to 120pF	for EMI request
7.	08/13	26	add CL35	for EMI request
8.	08/13	27	add CA51	for EMI request
9.	08/13	33	add C67 and C43	for EMI request

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REVISION CHANGE: 0.1 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

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Title: PIR

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Version Change List (P. I. R. List) for Power Circuit

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Page #	Item Title	Solution Description
PVT : modification from EVT		
P35	mount ESD diode	mount PD5, PD6
P36	EMI request	add PC236 10uF
P37	EMI request	add PC367 10uF, PC368 2200pF
P37	change 3/5V IC main source	change PU330 to UP6182
P38	EMI request	add PC166 2200pF
P39	EMI request	add PC417 10uF, PC418 2200pF
P40	adjust loadine	change PR535 to 3.09K
P34	unify source	change PD1 to SC11N414880
P36	unify source	change PQ216 to SB000009610
P37	unify source	change PQ362 to SB000009610
P40	unify source	change PL502 to SM010020720
P40	turn on speed too quick	change PQ502, PQ504 to MDU2653RH
P37	change cap to 330uF with same price	change PC332, PC352 to SF000002000
P38	change cap to 330uF with same price	change PC152 to SF000002000
P39	change cap to 330uF with same price	change PC402 to SF000002000
P36	EMI request to mount snubber circuit, ISN caps	add PR206, PC206; PC234, PC235
P37	EMI request to mount snubber circuit	add PR336, PC336; PR356, PC356
P38	EMI request to mount snubber circuit & boost resistor	add PR156, PC156; change PR155 to 2.2ohm
P39	EMI request to mount snubber circuit	add PR406, PC406
P40	EMI request to mount snubber circuit	add PR506, PC506; PR516, PC516
PreMP : modification from PVT		
P34	increase precharge design margin	add PR12 1K
P35	change OTP setting	change PR15 to 23.2K, PR18 to 10.7K
P35	change source	chagne PC9 to SE070104Z80
P37	change 3/5V IC main source	change PU330 to TPS51125A
P38	change 0.75V IC main source	change PU75 to G2992
P40	adjust loadine	change PR535 to 4.53K
P40	adjust transient stability	change PR527 to 220pF

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