

COMPAL CONFIDENTIAL

MODEL NAME : IAQ20

PCB NO : LA-3751P (DA800008Y0L)

BOM P/N : 46149031L0121

Converse

**uFCPGA Mobile Merom
Intel Crestline + ICH8M**

21-05-2007

REV : 0.1(X00)

@ : Nopop Component

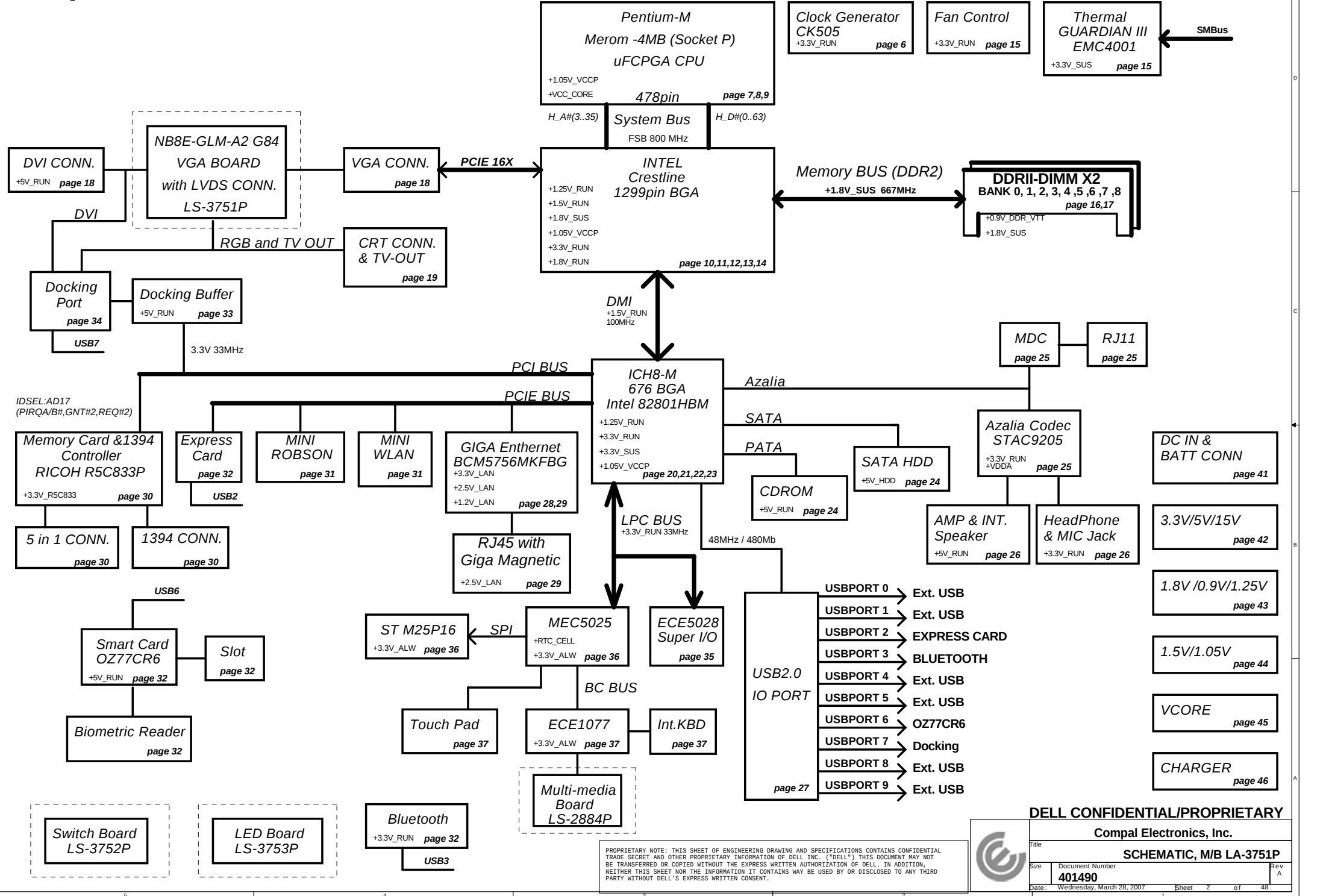
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +1.25V_RUN +0.9V_DDR_VTT +1.05V_VCCP +VCC_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQC, D
Docking	AD24	REQ#0 / GNT#0	PIRQA

ICH8-M	USB PORT#	DESTINATION
	0	Rear Right Bottom
	1	Rear Right Top
	2	EXPRESS CARD
	3	Bluetooth
	4	Rear Left Bottom
	5	Rear Left Top
	6	OZ77CR6/Smart Card Reader
	7	Docking
	8	Side Bottom
	9	Side Top
OZ77CR6	UPD+/D-, pin 16/17	ICH8-M
	DPD+/D-, pin 18/19	Biometric Reader
	EGATED+/D-, pin 20/21	SMART CARD

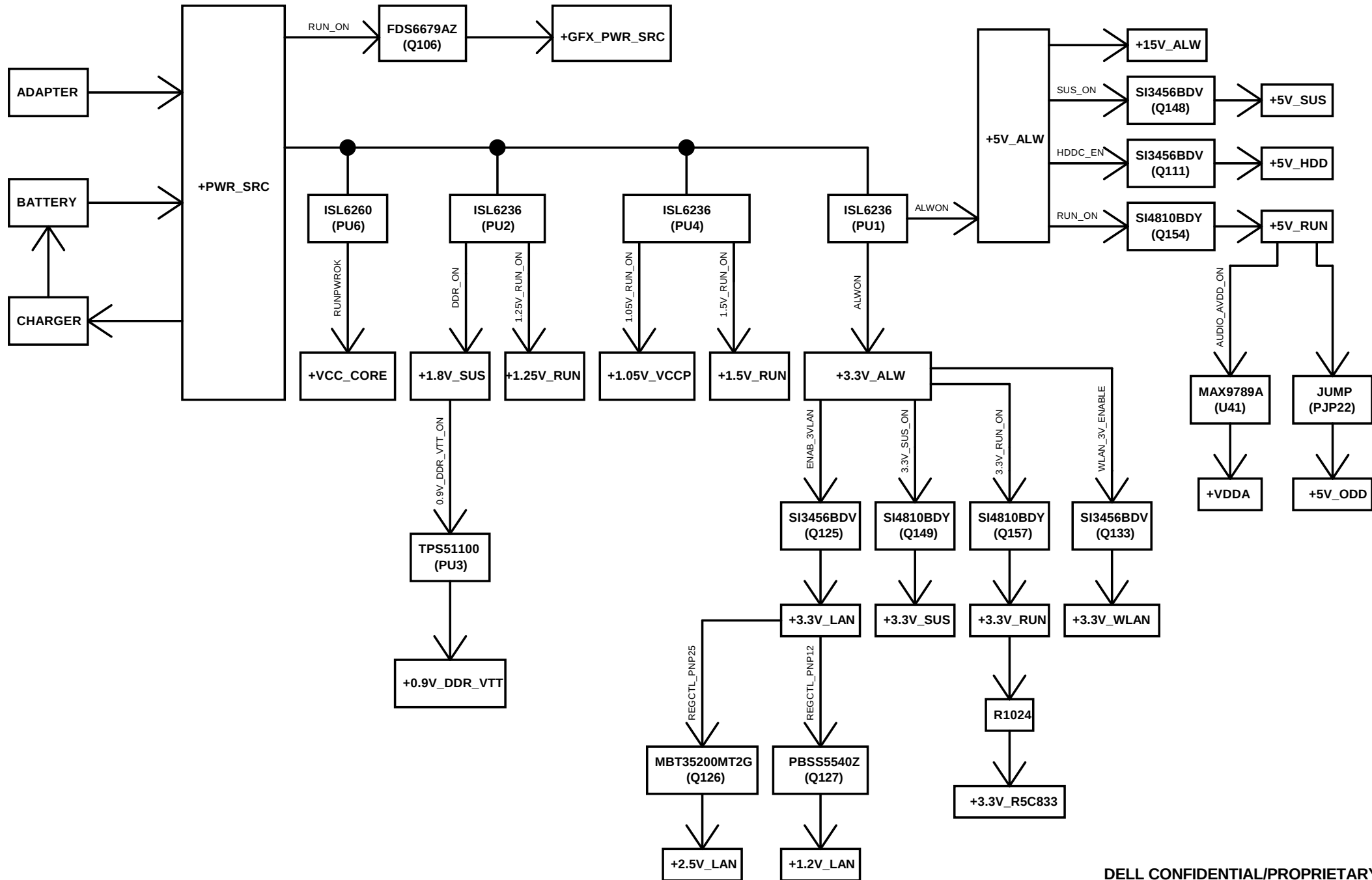
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD 1- Robson
Lane 2	MINI CARD 2- WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	GIGA LAN

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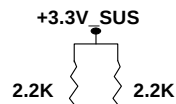
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ICH8-M

AJ26 ICH_SMBCLK
AD19 ICH_SMBDATA



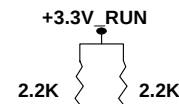
B6 D7
BCM5756
SMBUS Address [C8]

11 9
EXPRESS CARD
SMBUS Address [TBD]

32 30
MINI WLAN
SMBUS Address [TBD]

2N7002
2N7002

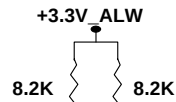
MEM_SCLK
MEM_SDATA



197 195
DIMMA
SMBUS Address [A0]
197 195
DIMMB
SMBUS Address [A4]
30 32
MINI ROBSON
SMBUS Address [TBD]

SIO
MEC5025

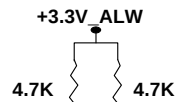
8 LCD_SMBCLK
7 LCD_SMBDAT



+3.3V_ALW

8 10
Graphic BTB CONN inverter
SMBUS Address [58]

100 THRM_SMBCLK
99 THRM_SMBDAT

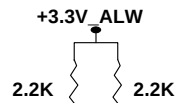


+3.3V_ALW

12 11
GUARDIAN EMC4001
SMBUS Address [2F]

9 10
CHARGER ISL88731
SMBUS Address [12]

112 PBAT_SMBCLK
111 PBAT_SMBDAT

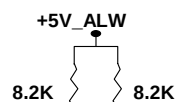


+3.3V_ALW



3 4
BATTERY Connector
SMBUS Address [16]

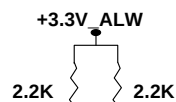
6 DOCK_SMBCLK
5 DOCK_SMBDAT



+5V_ALW

39 40
DOCKING
SMBUS Address [C4, 72, 70, 48]

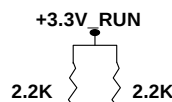
13 CKG_SMBCLK
12 CKG_SMBDAT



+3.3V_ALW

2N7002
2N7002

CLK_SCLK
CLK_SDATA



+3.3V_RUN

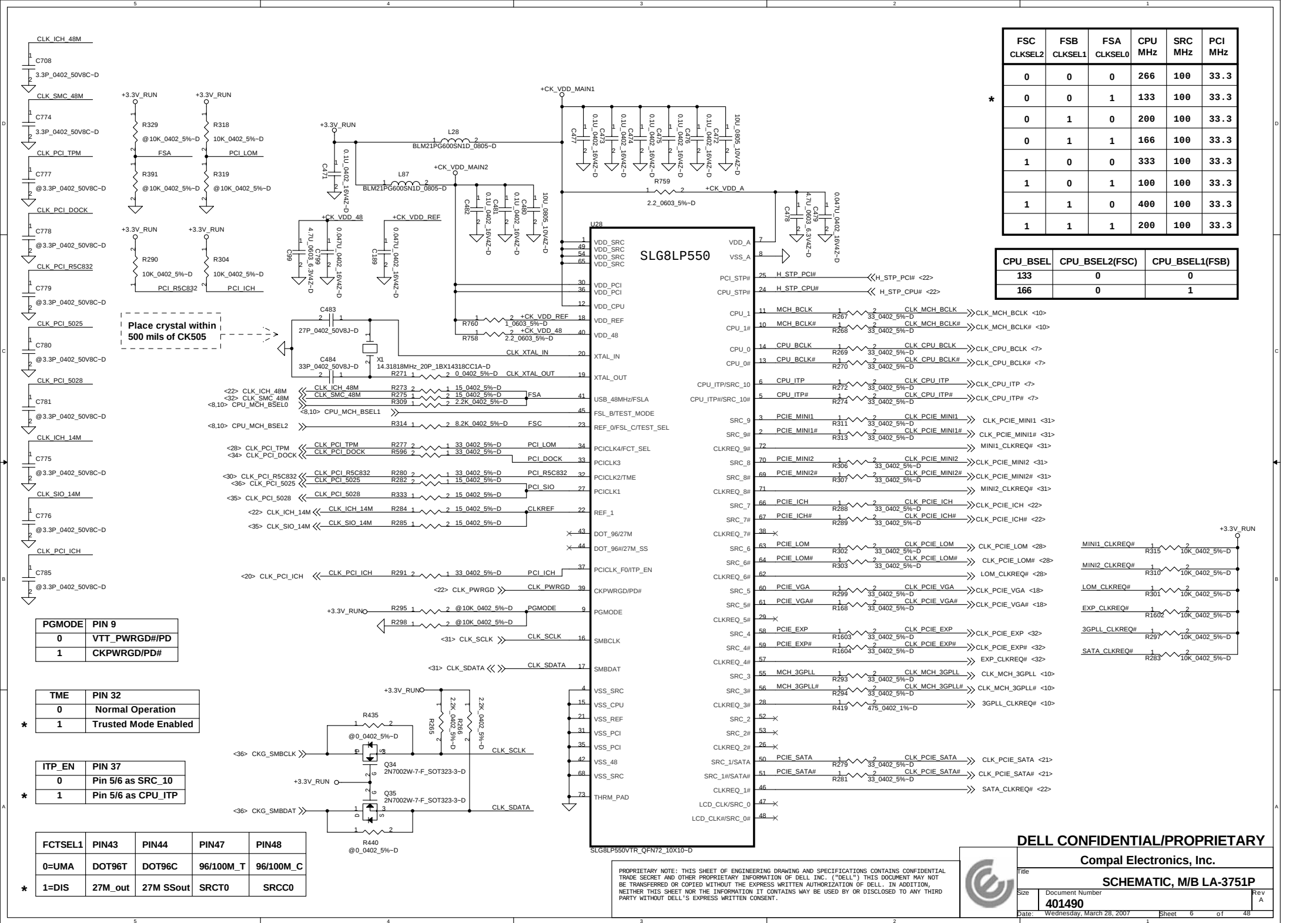
16 17
CLOCK GENERATOR
SMBUS Address [D2]

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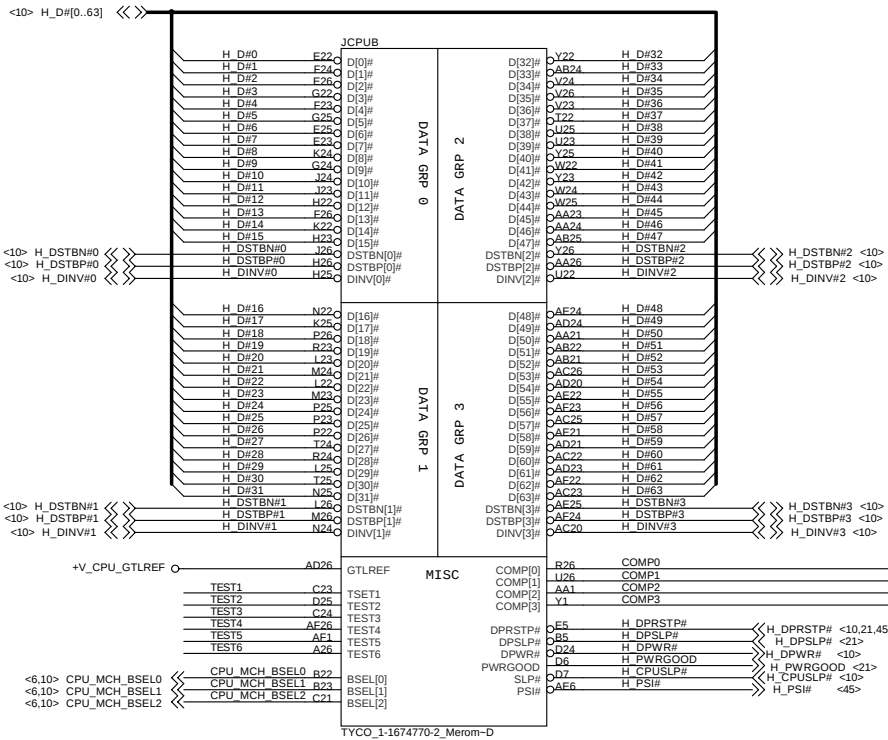
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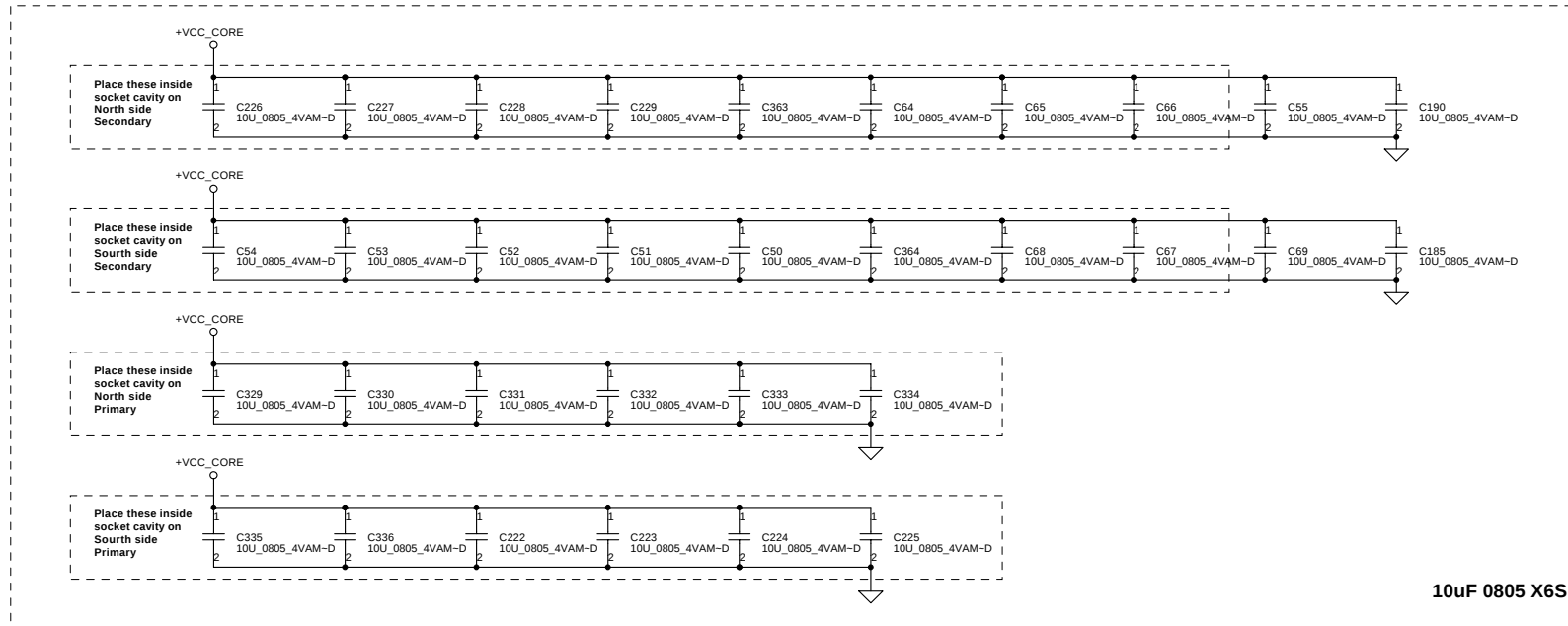
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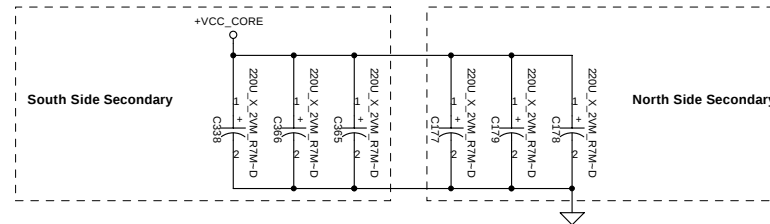




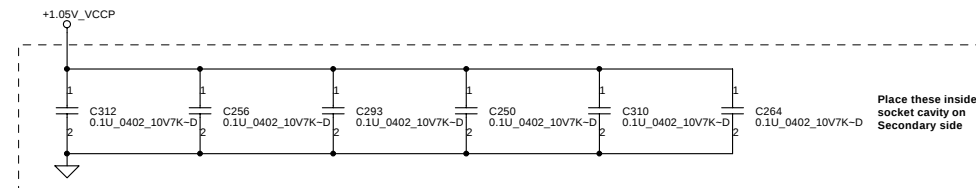
High Frequency Decoupling



Near VCORE regulator.



ESR <= 1.5m ohm

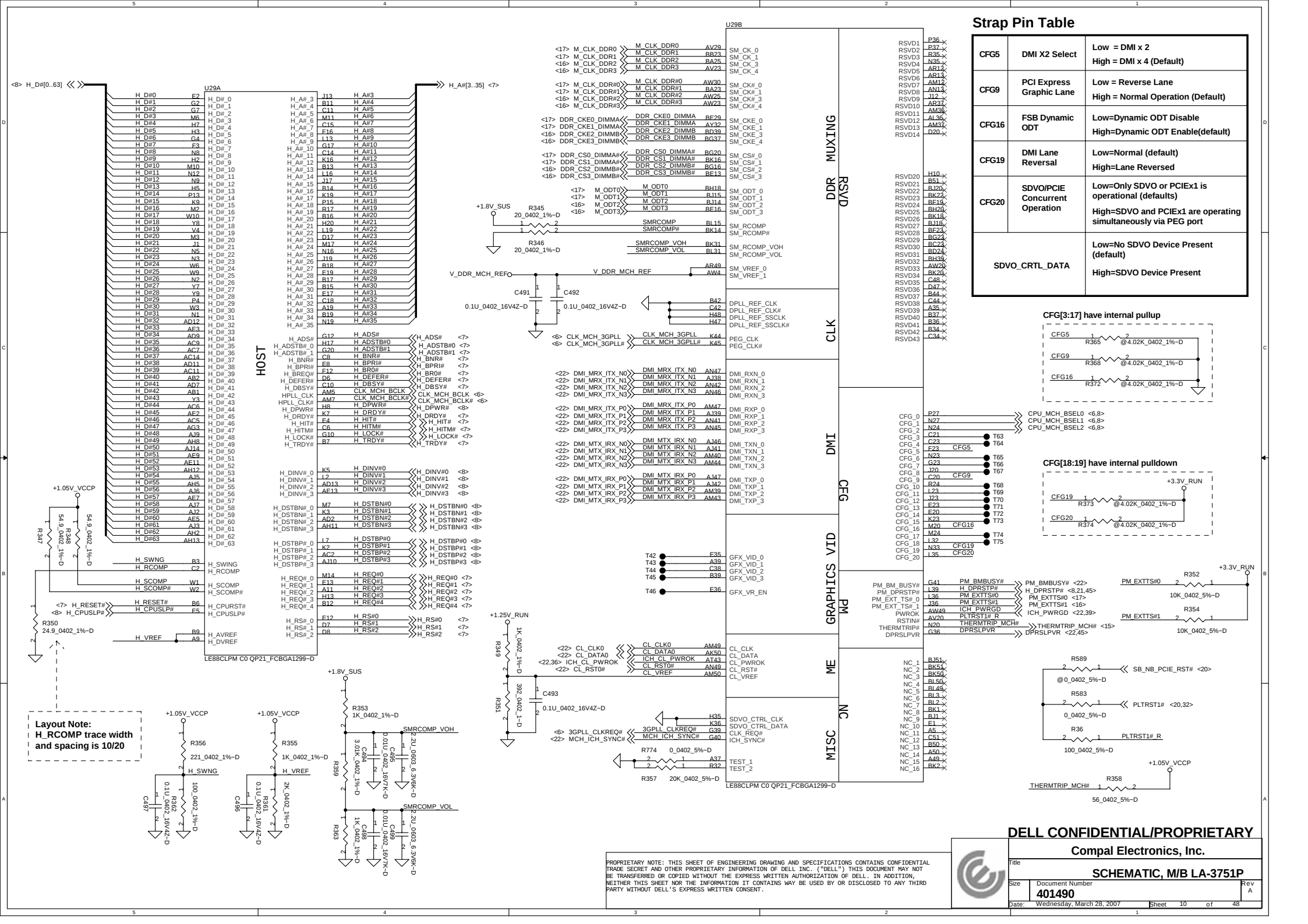


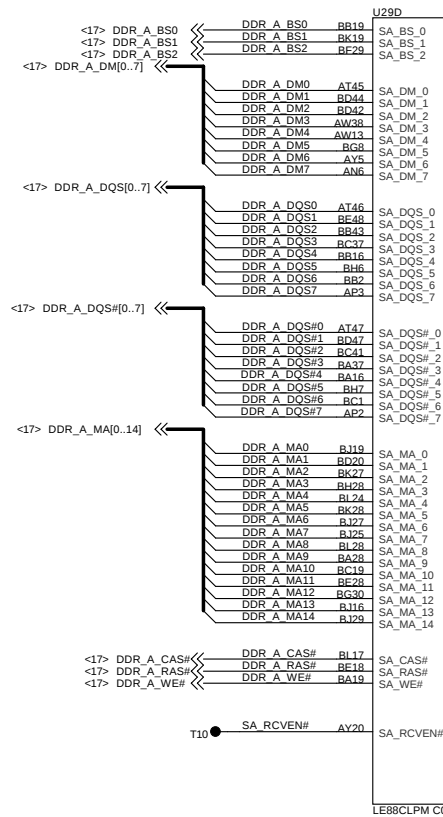
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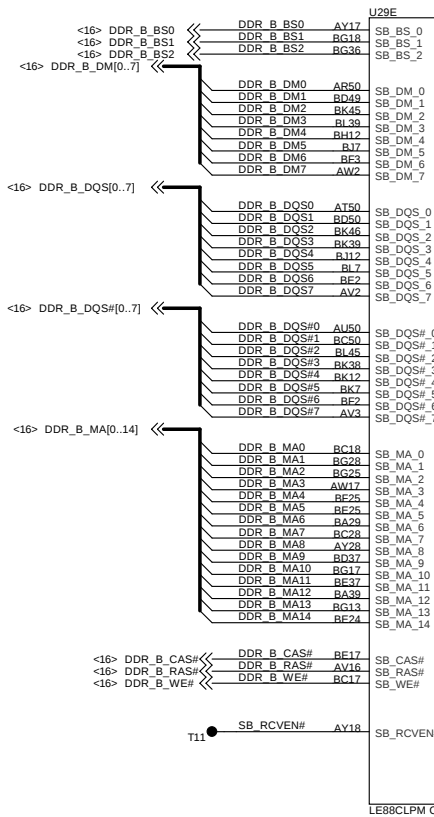
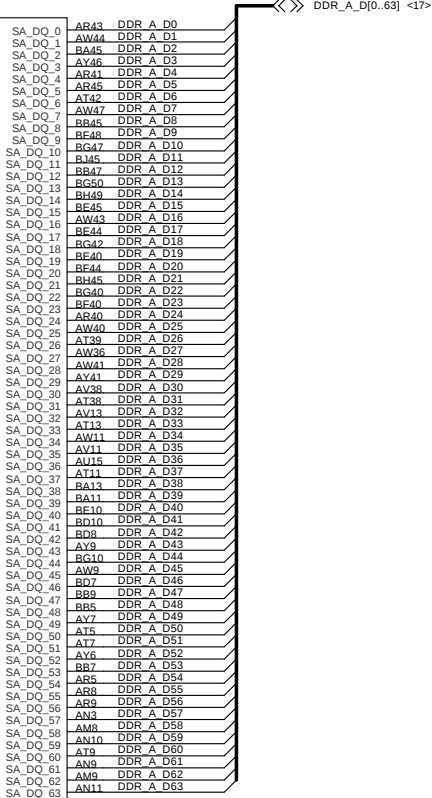
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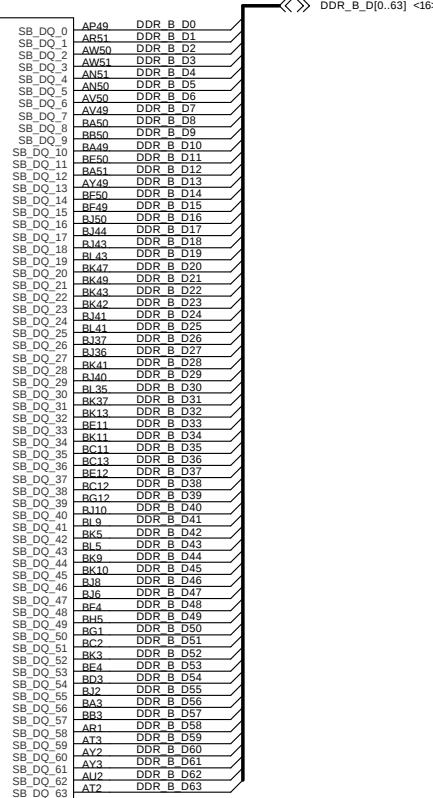




DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

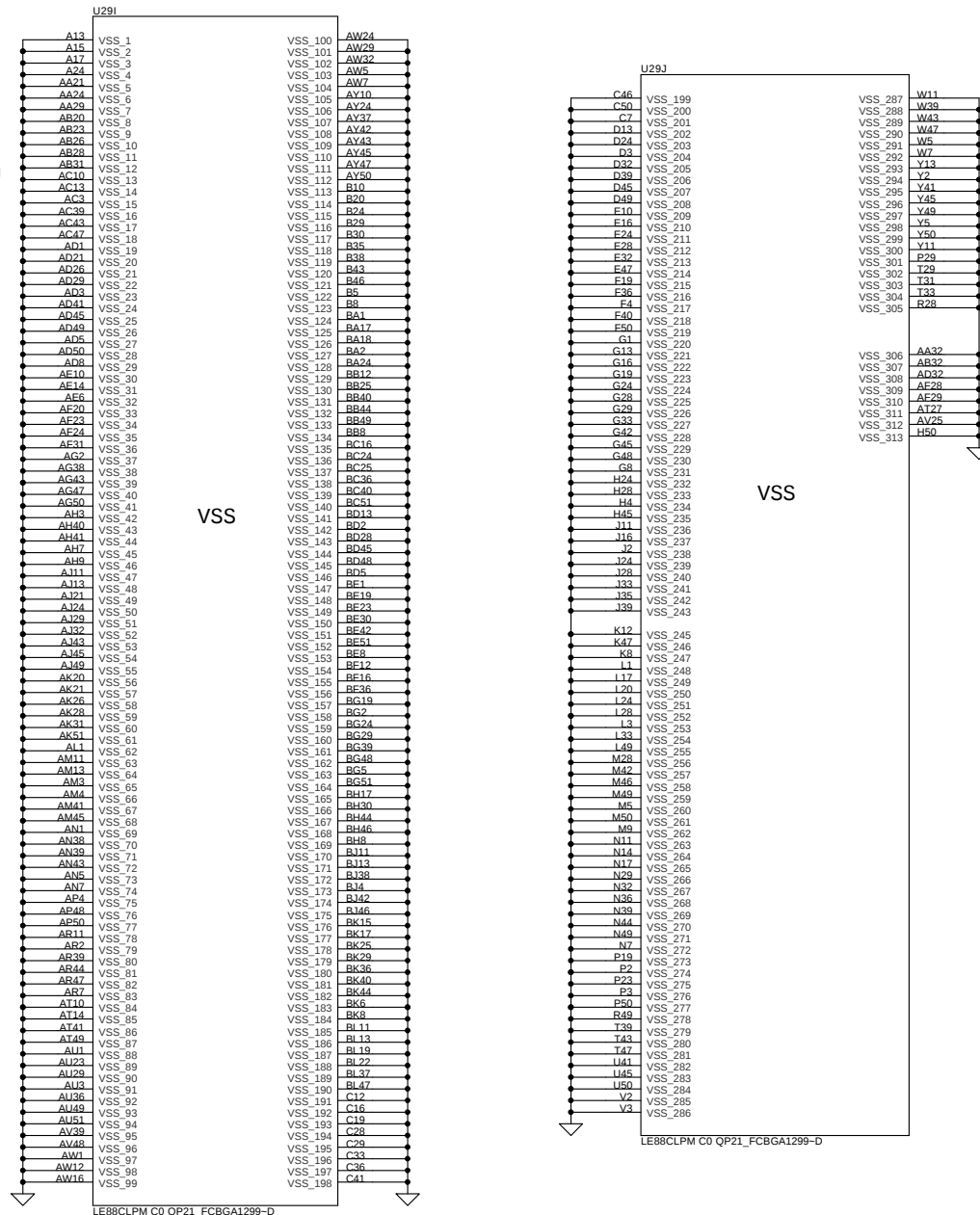
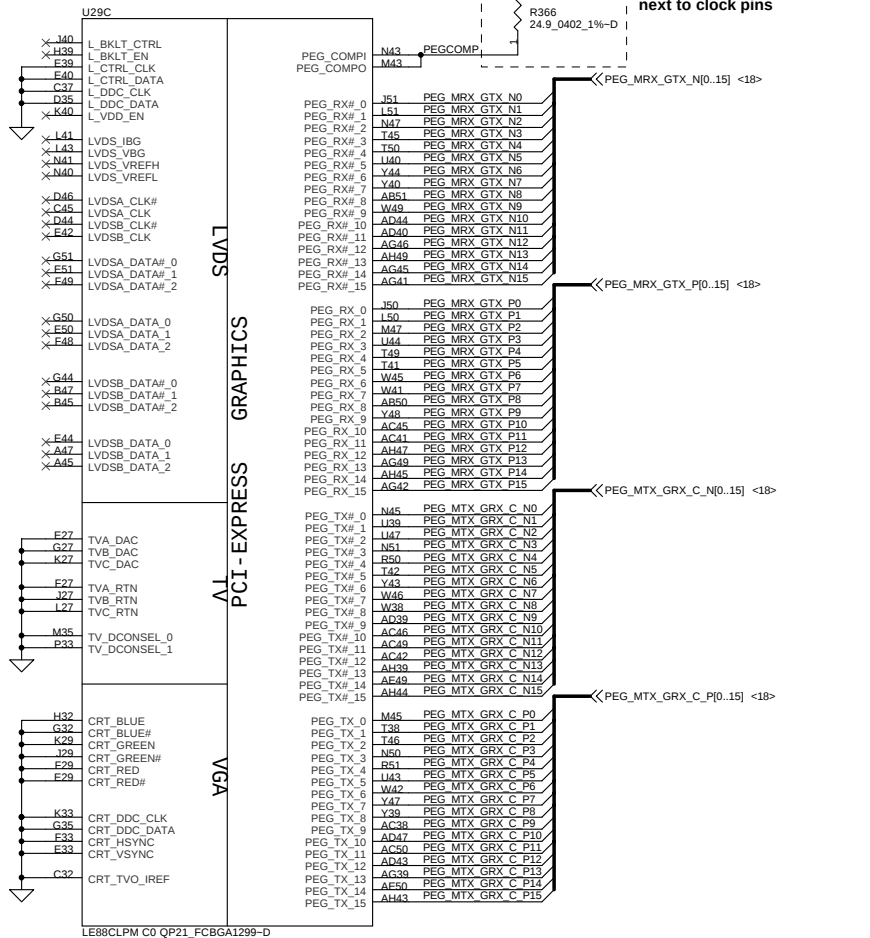


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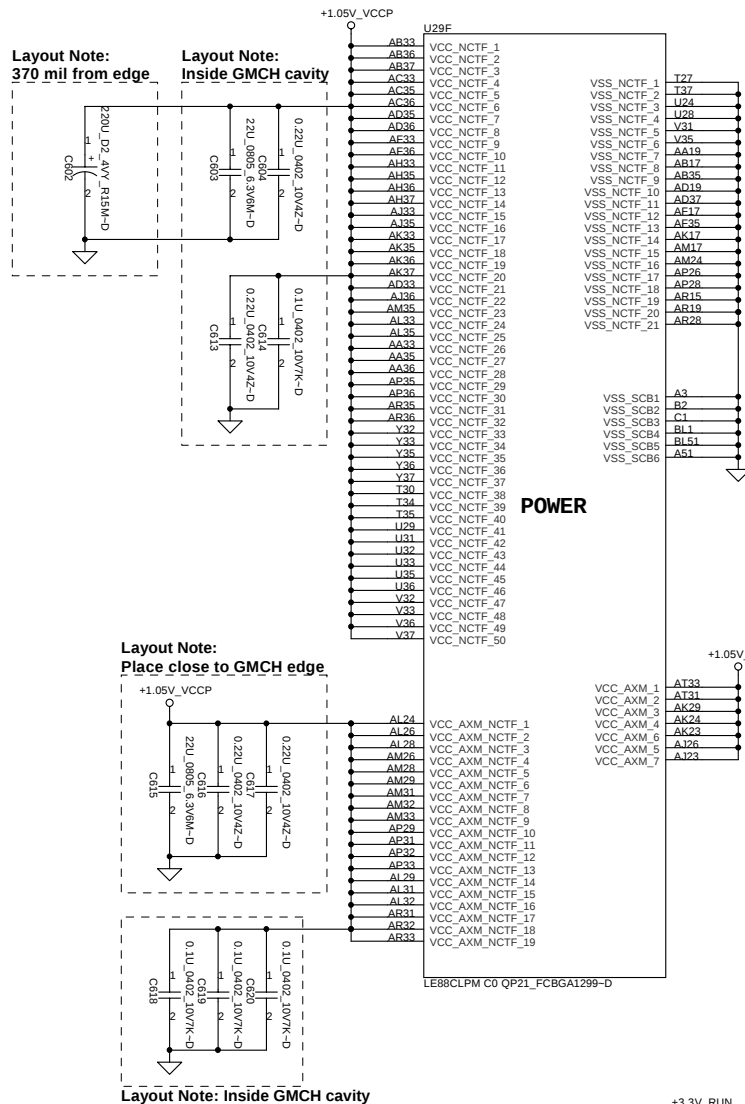
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Size Document Number 401490 Rev A

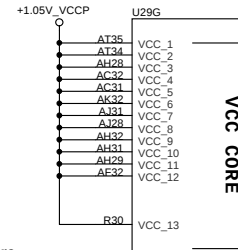
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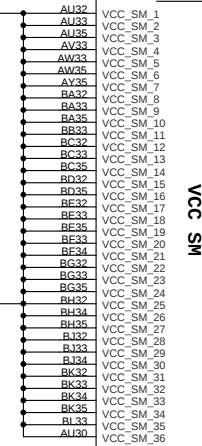


Layout Note:
Place C901 where LVDS and DDR2 taps

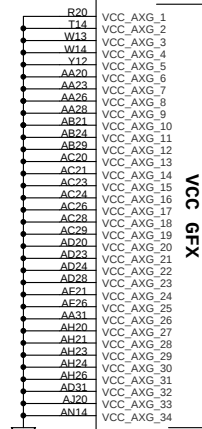
Layout Note:
Place on the edge



POWER



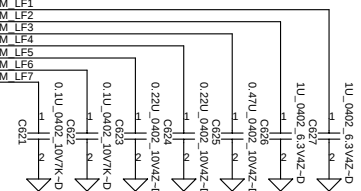
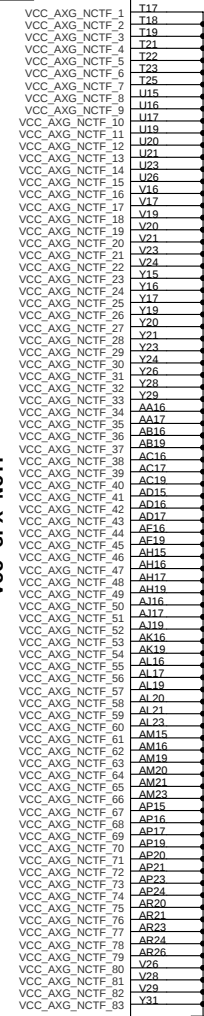
VCC SM



VCC GFX

VCC GFX NCTF

VCC SM LF



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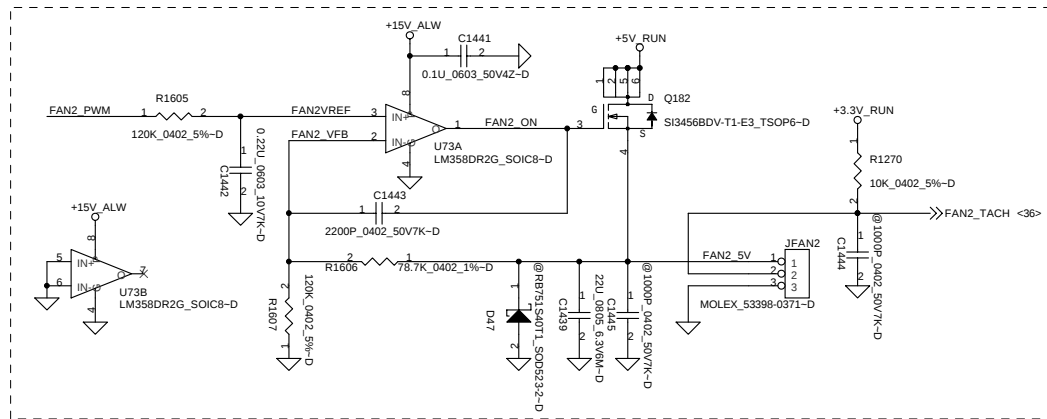
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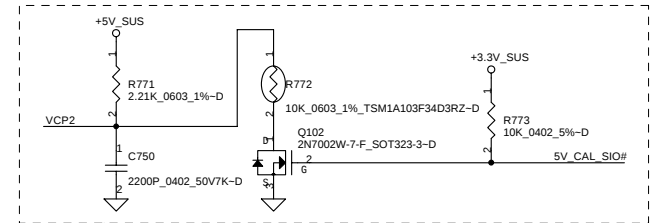
VGA fan control and Tachometer



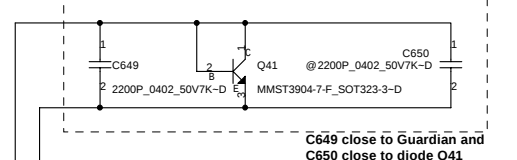
$$VSET = \frac{R438}{R436+R438} \times 3.3V = 0.865V$$

$$VSET = \left(\frac{Tp-70}{21} \right) \Rightarrow Tp = 88.2\text{ C}$$

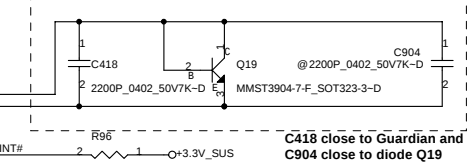
Place close to JDIMA



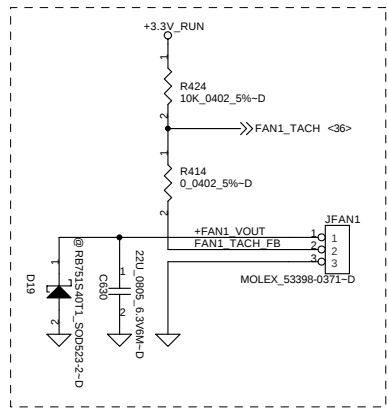
Place Q41 close to JDIMMB
REM_DIODE3_N, REM_DIODE3_P routing together.
Trace width / Spacing = 10 / 10 mil



Diode circuit at DP4/DN4 is used for skin temp sensor
(placed optimally between CPU, MCH and GPU)

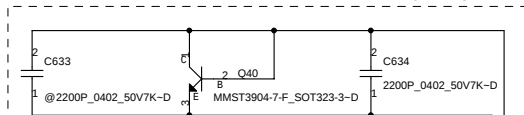


Main fan control and Tachometer



Place under CPU

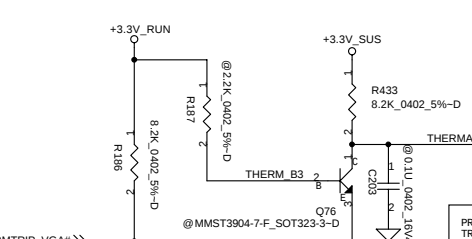
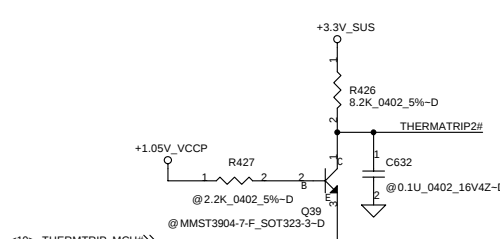
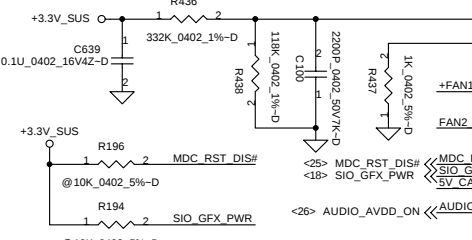
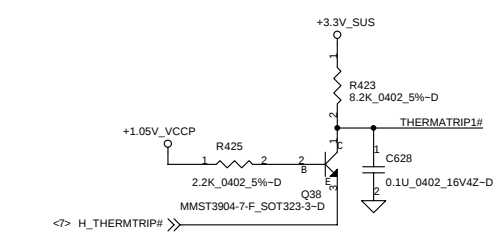
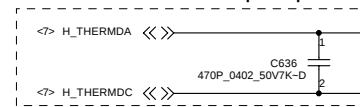
Place C633 close to the Q40 as possible



Place C634 close to the Guardian pins as possible



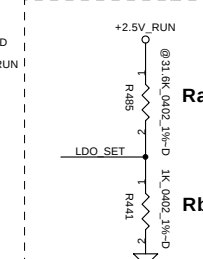
Place C636 close to Guardian pin as possible



SMBus address: 2F



Voltage margining circuit for LDO output



For Vmargin, stuff Ra=31.6K and Rb=30K
For production, stuff Rb=1K only

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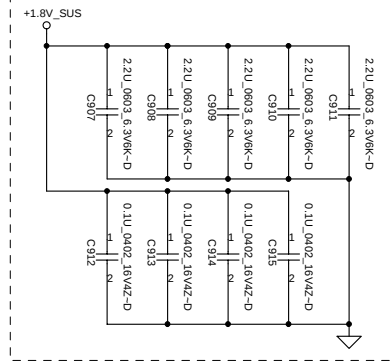
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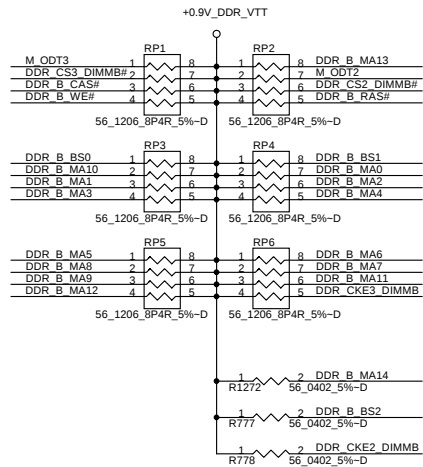
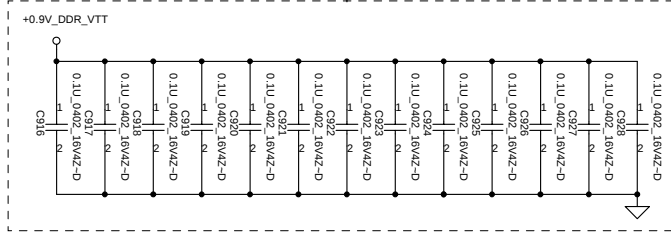
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Layout Note:
Place near JDIMB

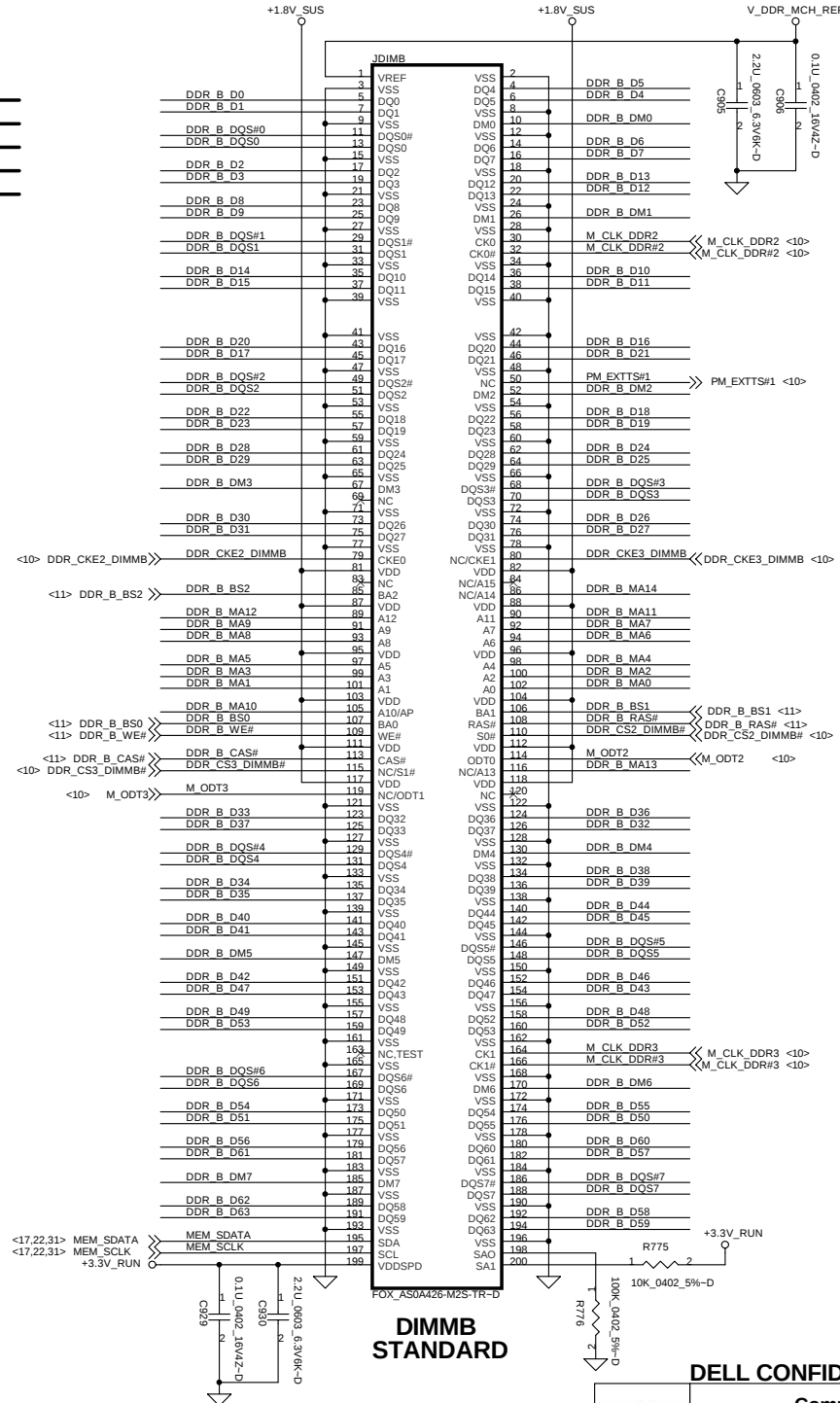


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistors close to JDIMB

<11> DDR_B_D[0..63] <<>>
<11> DDR_B_DM[0..7] <<>>
<11> DDR_B_DQS[0..7] <<>>
<11> DDR_B_DQS#[0..7] <<>>
<11> DDR_B_MA[0..14] <<>>



**DIMB
STANDARD**

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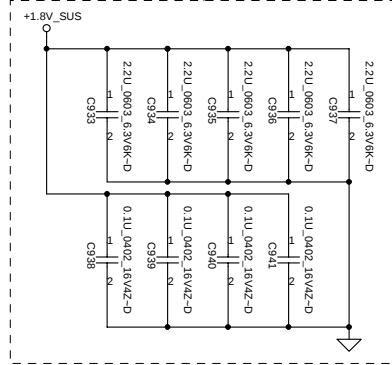
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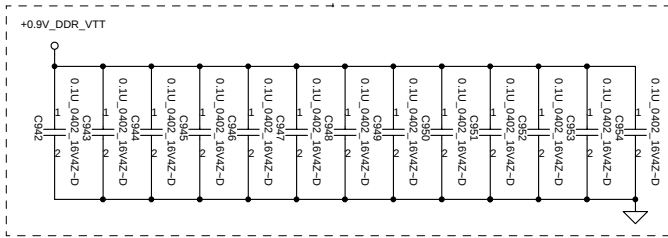
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Layout Note:
Place near JDIMA

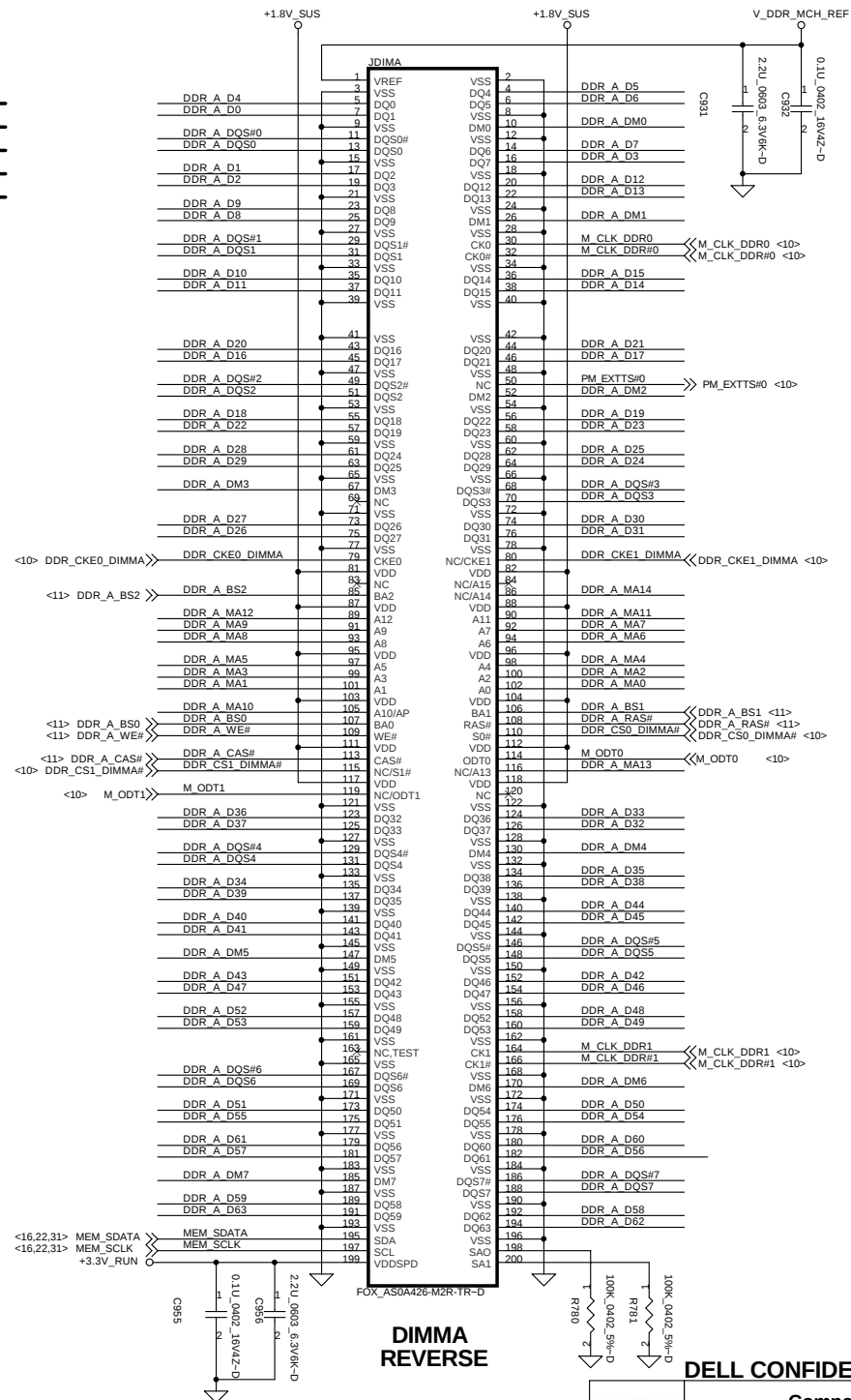
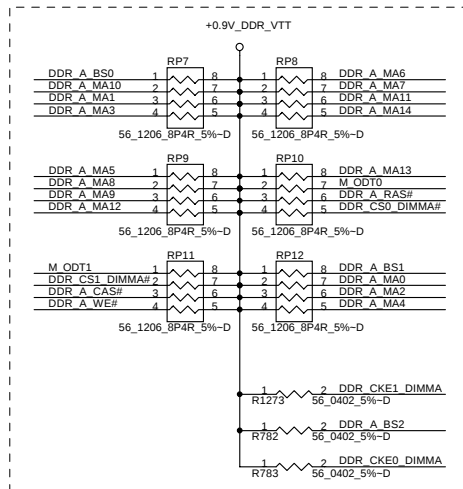


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



<11> DDR_A_D[0..63] <<>
<11> DDR_A_DQS[0..7] <<>
<11> DDR_A_DQS#0[0..7] <<>
<11> DDR_A_DM[0..7] <<>
<11> DDR_A_MA[0..14] <<>

Layout Note:
Place these resistors close to JDIMA



**DIMMA
REVERSE**

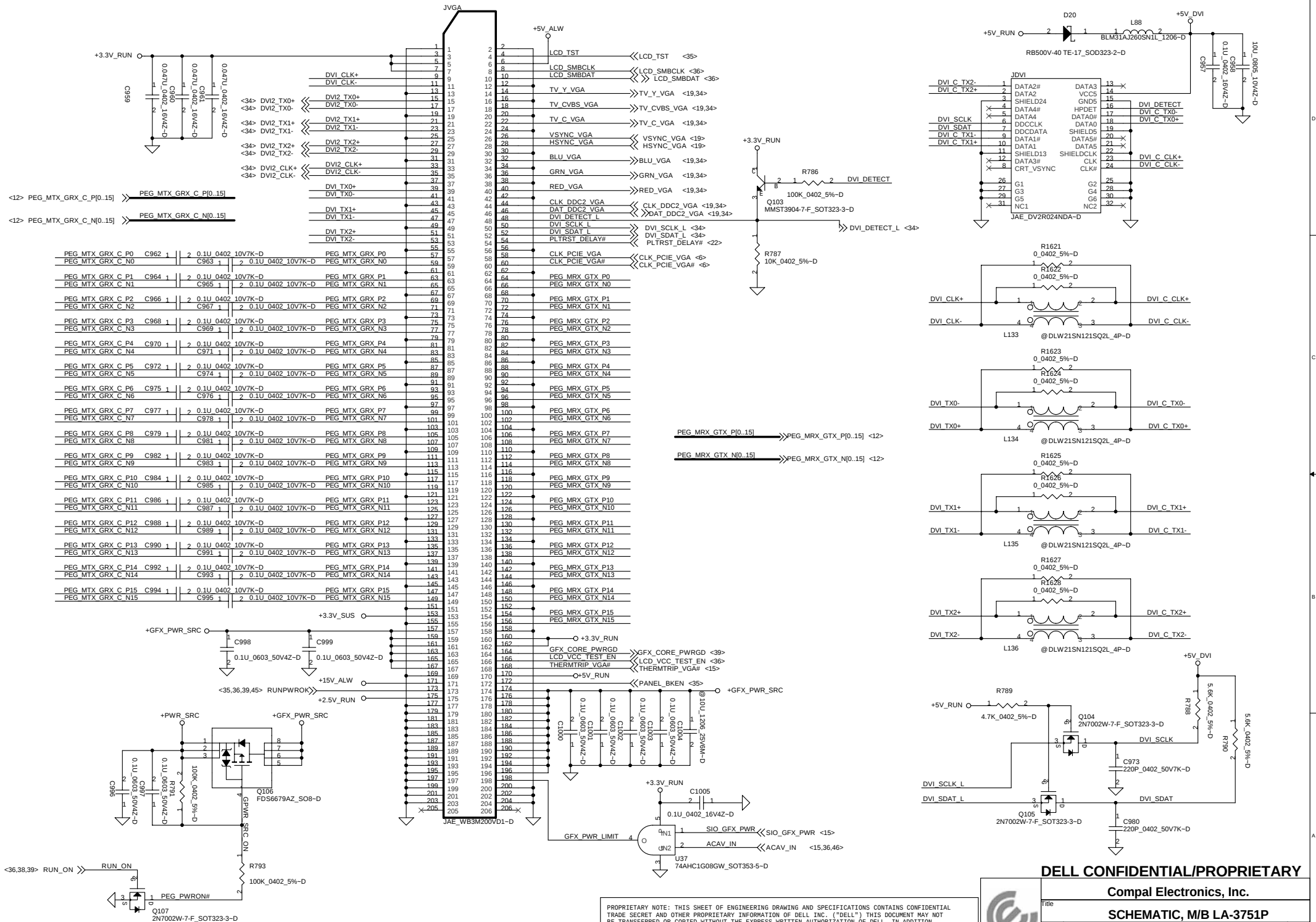
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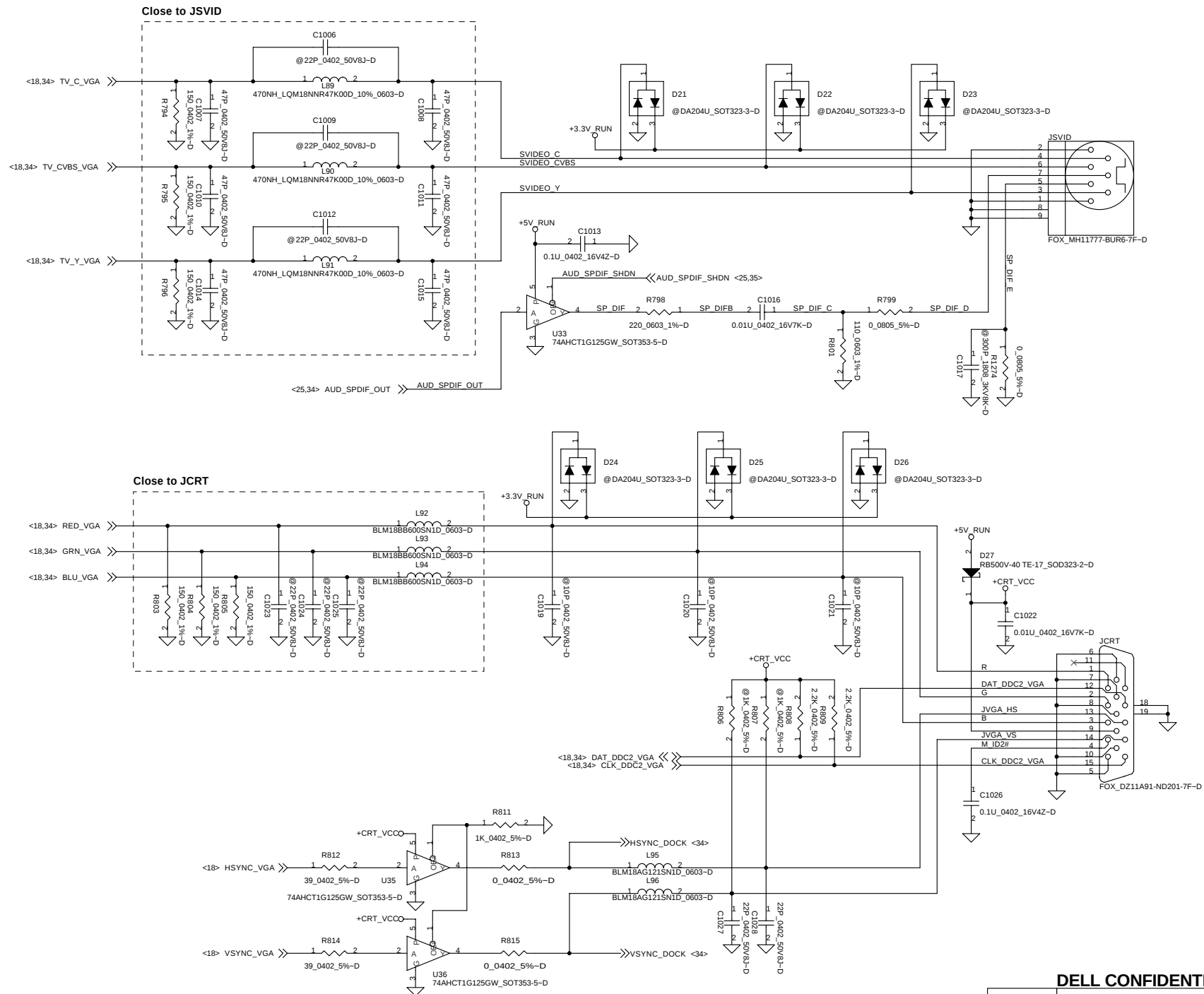


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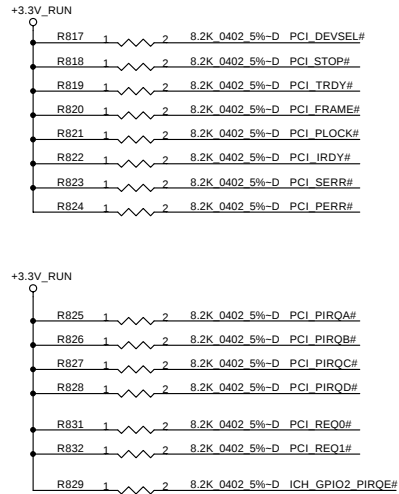
Compal Electronics, Inc.

SCHEMATIC, M/B LA-3751P

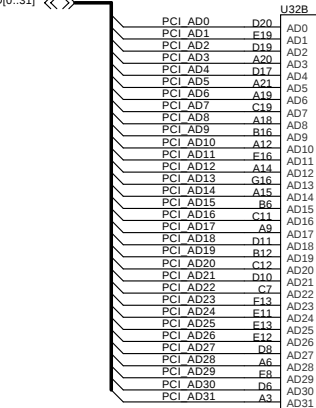
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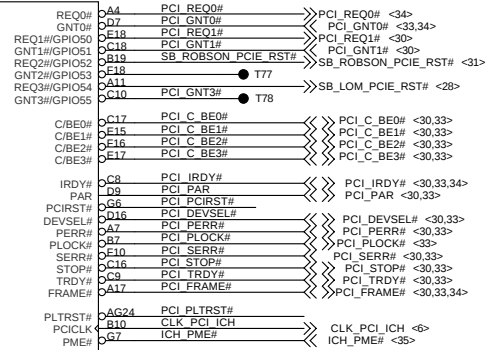
Sheet 19 of 48



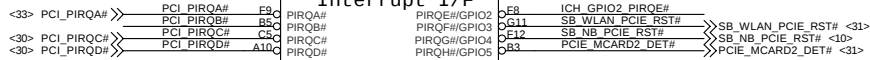
<30,33> PCI_AD[0..31] <<>



PCI

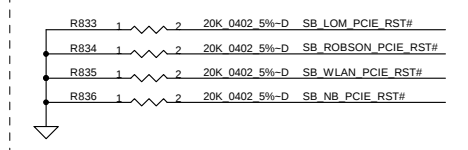


Interrupt I/F



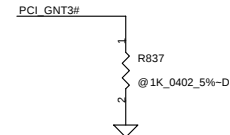
NH82801HEM B1 QN24_BGA676-D

BIOS should not enable the internal GPIO pull up resistor

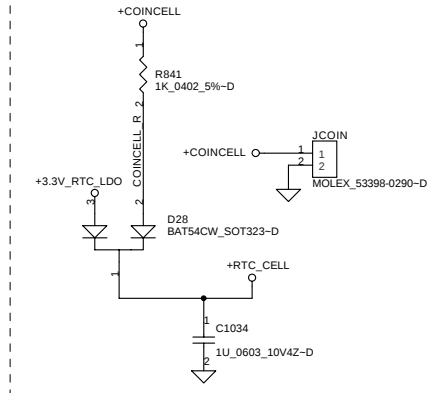


A16 away override strap.

PCI_GNT3#	Low = A16 swap override enabled. High = Default.
-----------	---



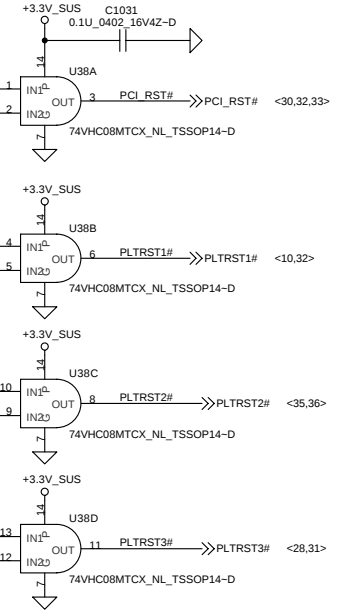
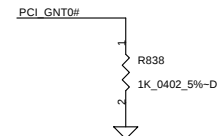
COIN CELL RTC BATTERY



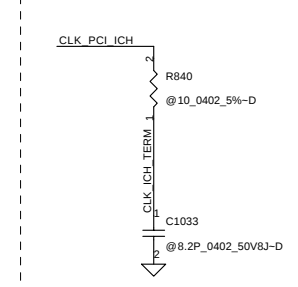
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BOOT BIOS STRAP

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC



Place close to pin U32.B10



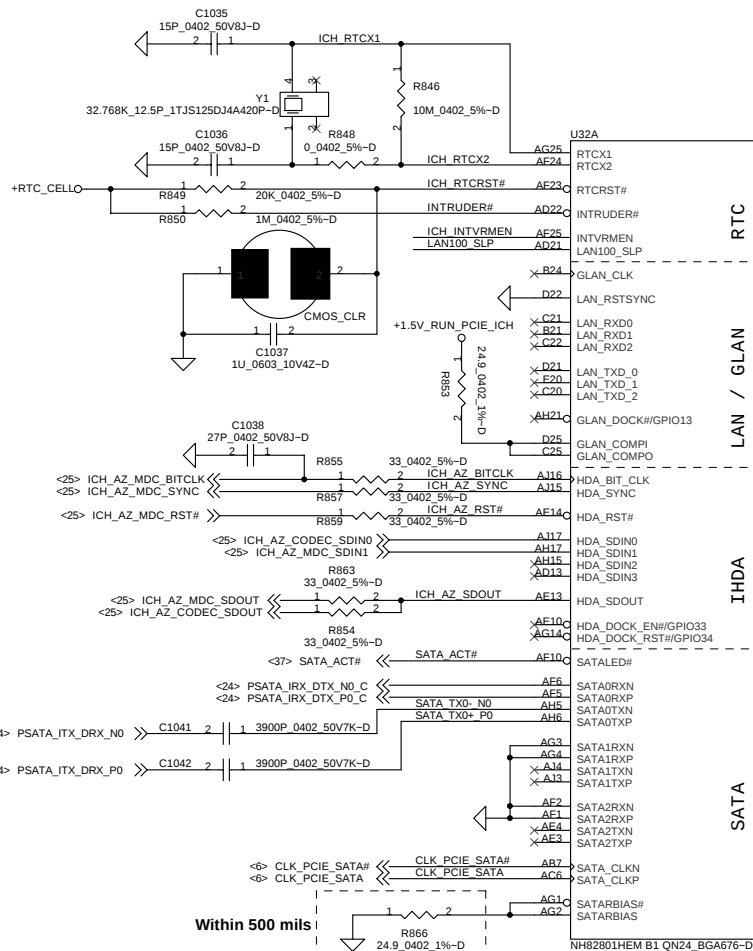
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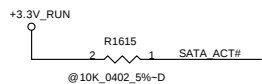
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ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
--------------	---



ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
----------------	---

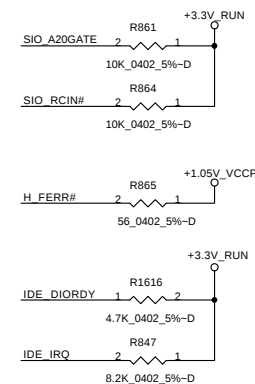
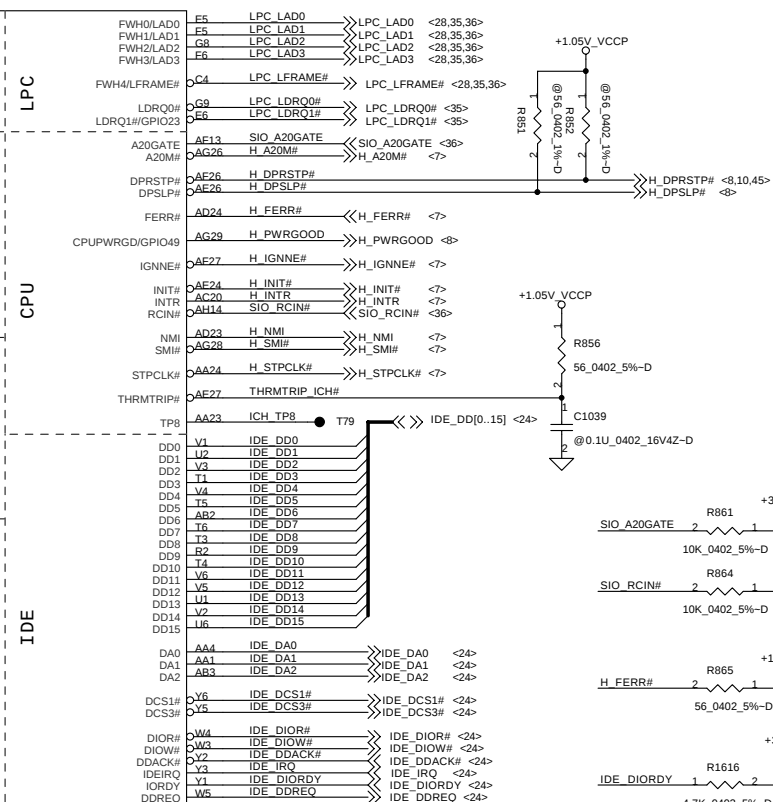
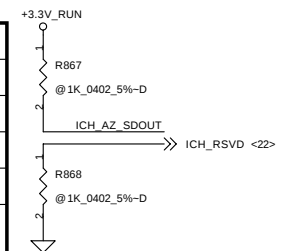


<25> ICH_AZ_CODEEC_BITCLK << R862 ICH_AZ_BITCLK
 1 2
 33_0402_5%-D
 1
 C1040
 27P_0402_50V8J-D
 2

<25> ICH_AZ_CODEEC_SYNC << R858 ICH_AZ_SYNC
 1 2
 33_0402_5%-D

<25> ICH_AZ_CODEEC_RST# >> R860 ICH_AZ_RST#
 1 2
 33_0402_5%-D

XOR Chain Entrance STRAP		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



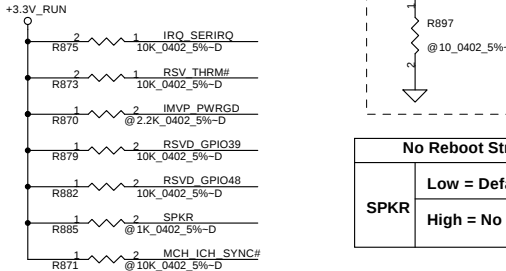
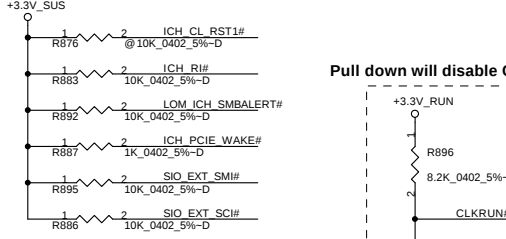
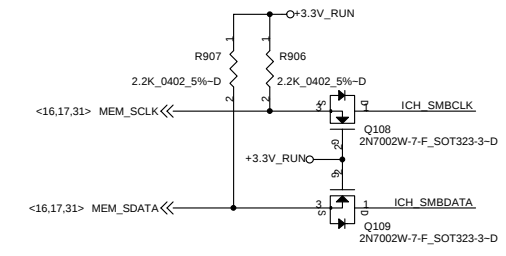
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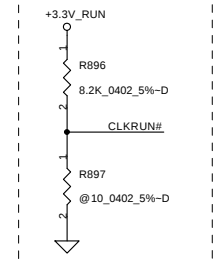
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	101.100

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Pull down will disable CLKRUN#



No Reboot Strap	
SPKR	Low = Default High = No Reboot

No Reboot Strap

SPKR

Low = Default
High = No Reboot

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#

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MCH_ICH_SYNC#

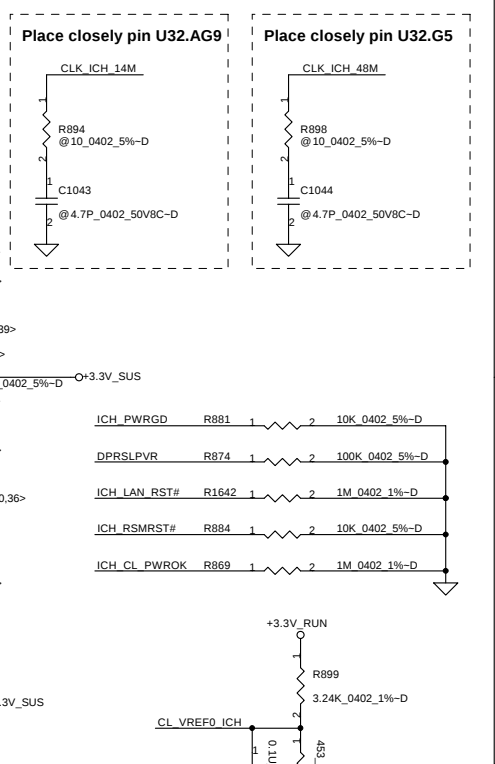
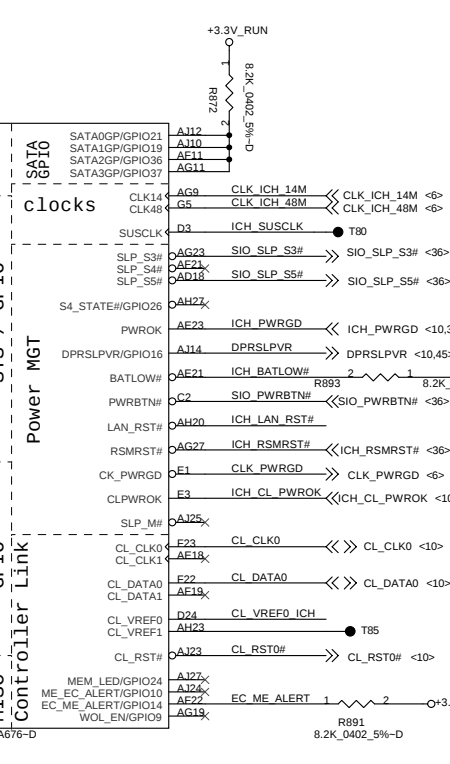
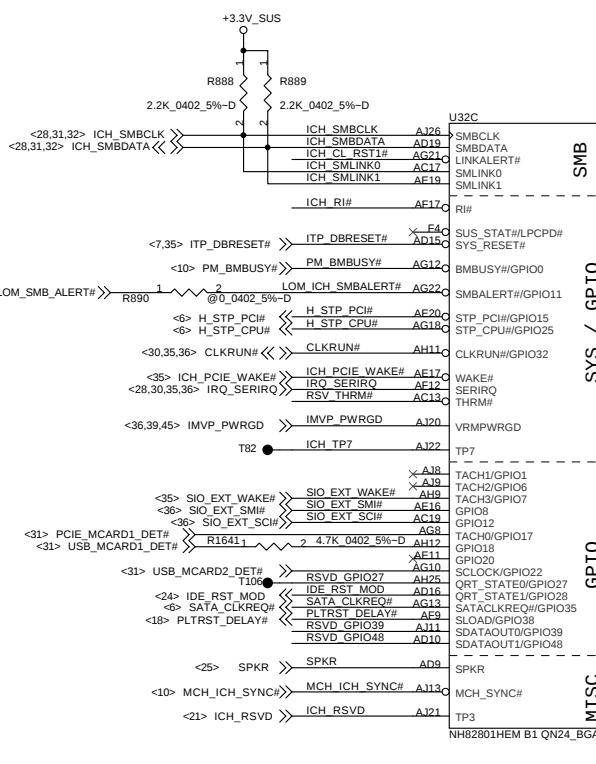
MCH_ICH_SYNC#

MCH_ICH_SYNC#

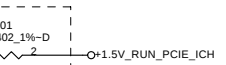
MCH_ICH_SYNC#

MCH_ICH_SYNC#

MCH_ICH_SYNC#



Place R901 within 500 mil of the ICH8-M and avoid routing next to clock pins



- >Rear Right Bottom
- >Rear Right Top
- >Express Card
- >Bluetooth
- >Rear Left Bottom
- >Rear Left Top
- >OZ77CR6
- >Docking
- >Side Bottom
- >Side Top

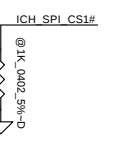
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Date: Wednesday, March 28, 2007
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MINI ROBSON (Mini Card 1)---

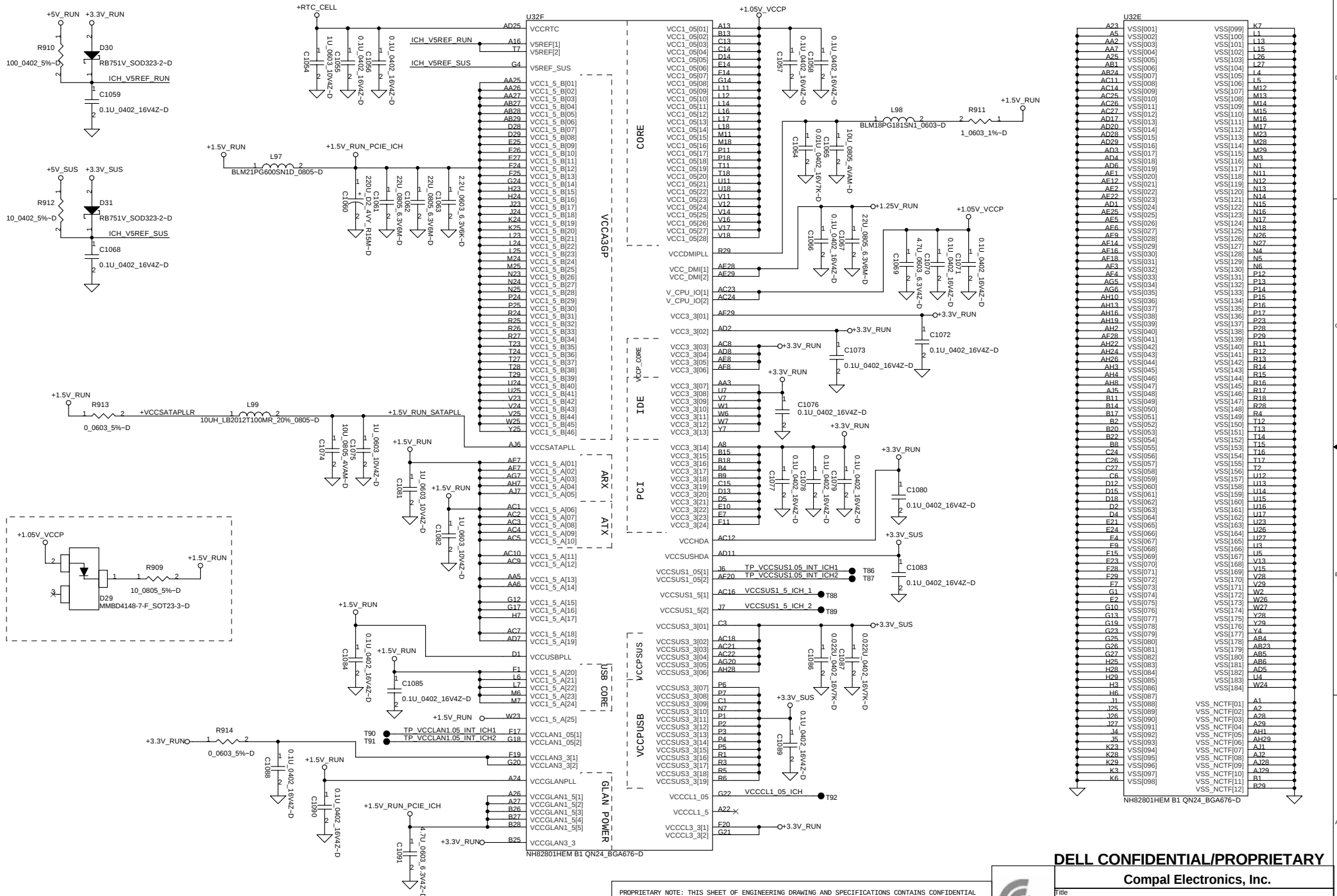
MINI WLAN (Mini Card 2)---

EXPRESS CARD ----

GIGA LAN --->



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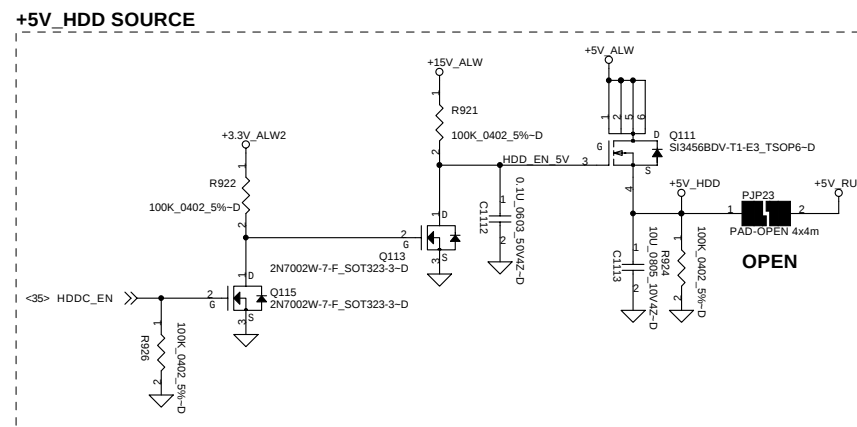
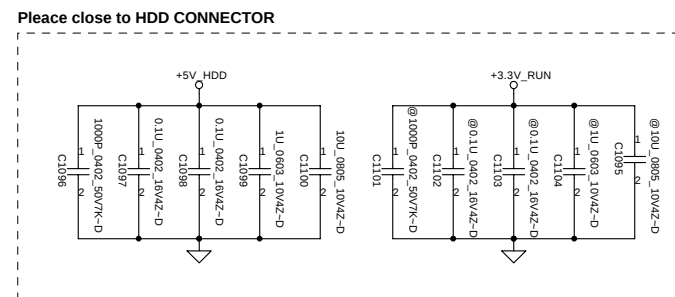
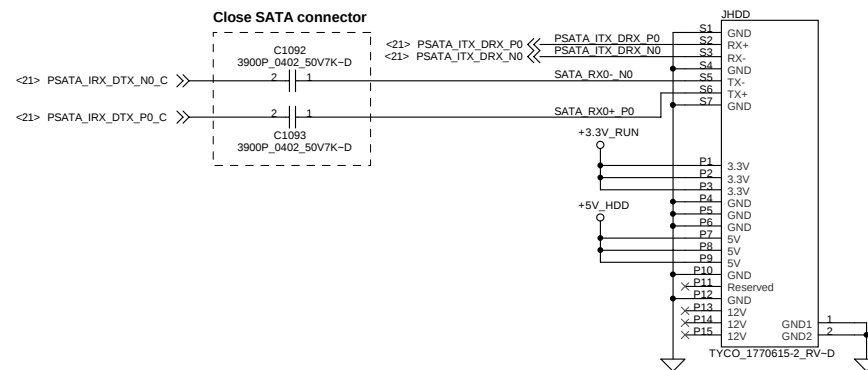
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The schematic shows a control line for the audio amplifier. A pull-up resistor R947 (100K) connects the line to +5V_AMPVCC. A pull-down resistor R948 connects the line to ground (0_0402_5%-D). The node is labeled 'AUD_AMP MUTE#' and is connected to the 'AUDIO_AVDD ON' pin of the audio codec.

The schematic diagram illustrates the power supply section of the BLM21PG6005N1D_0805-D. It features a +5V_RUN0 input connected to a network of capacitors (C1139, C1141, C1140, C1143, C1142) and an inductor (L104) leading to a +5V_AMPVCC output. The capacitors are all 10µF/42-D type.

INT_SPK_R1 1
 INT_SPK_R2 2
 INT_SPK_L1 3
 INT_SPK_L2 4

JSPK
 1
 2
 3
 4

MOLEX_53398-0490-D

INT SPK L2
INT SPK L1
INT SPK R2
INT SPK R1

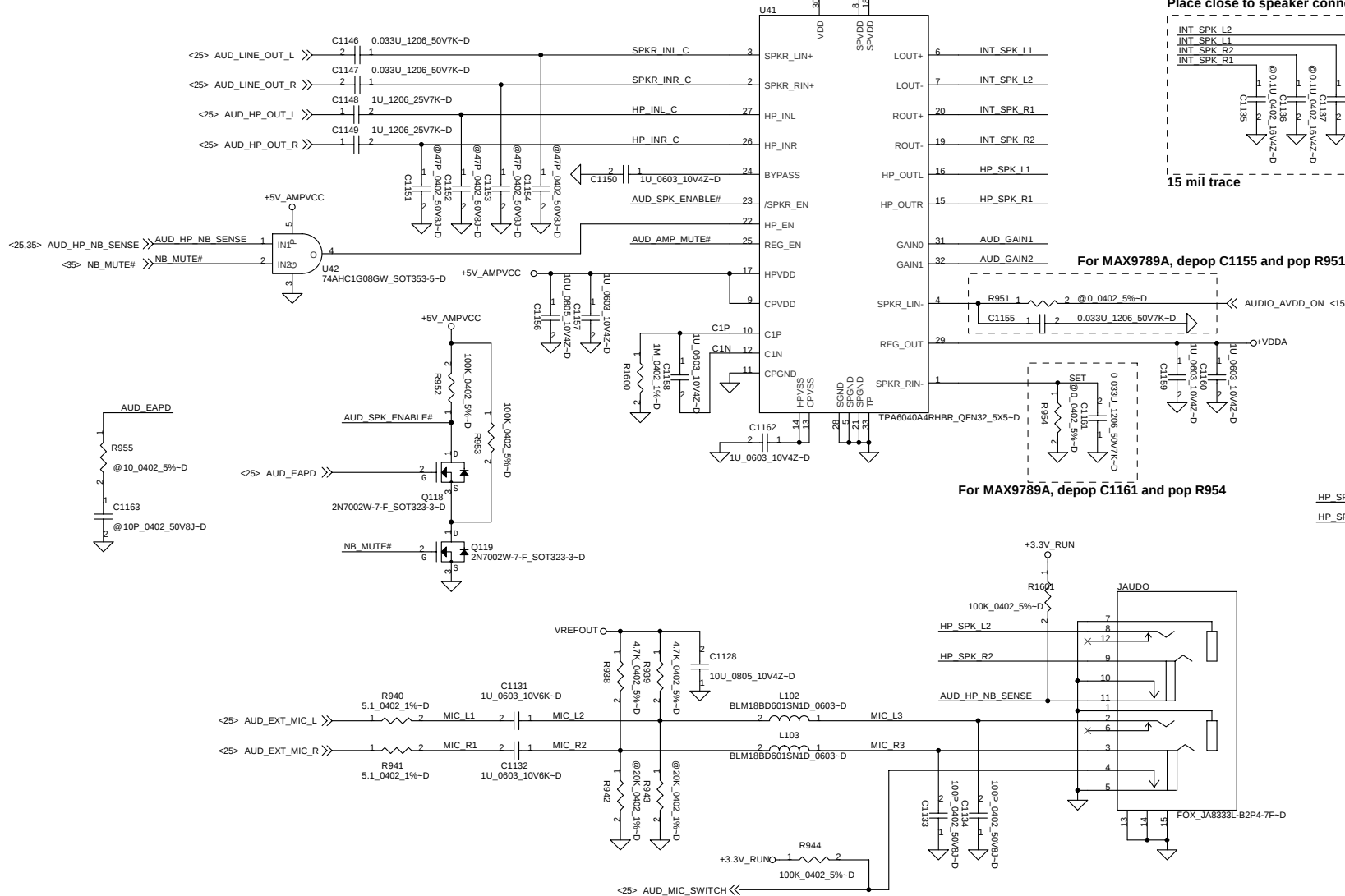
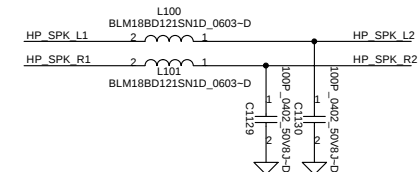
0.1uF
0.01uF
16V4Z-D

C1135
C1136
C1137
C1138
C1139

15 mil trace

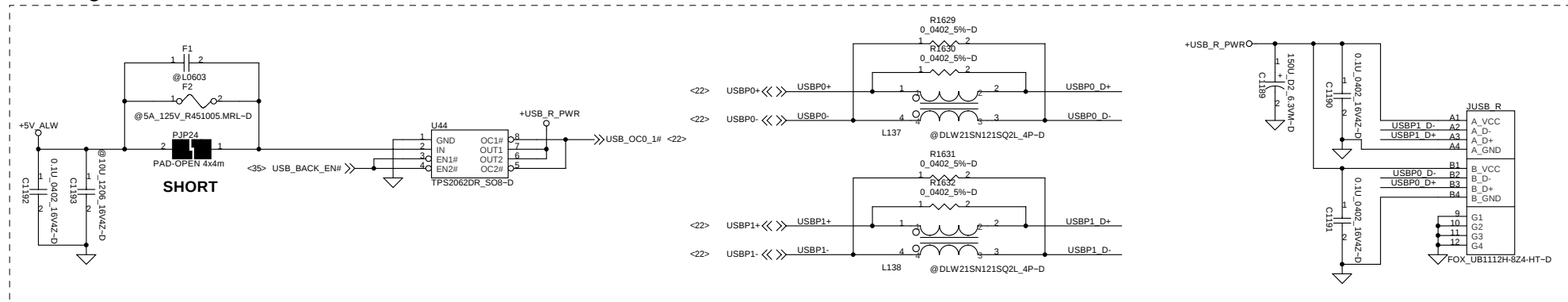
For MAX9789A, depop C1161 and pop R954

	GAIN1	GAIN2	AV(inv)	INPUT IMPEDANCE
	0	0	6dB	82K ohm
	0	1	10dB	66K ohm
	1	0	15.6dB	45K ohm
*	1	1	21.6dB	26K ohm

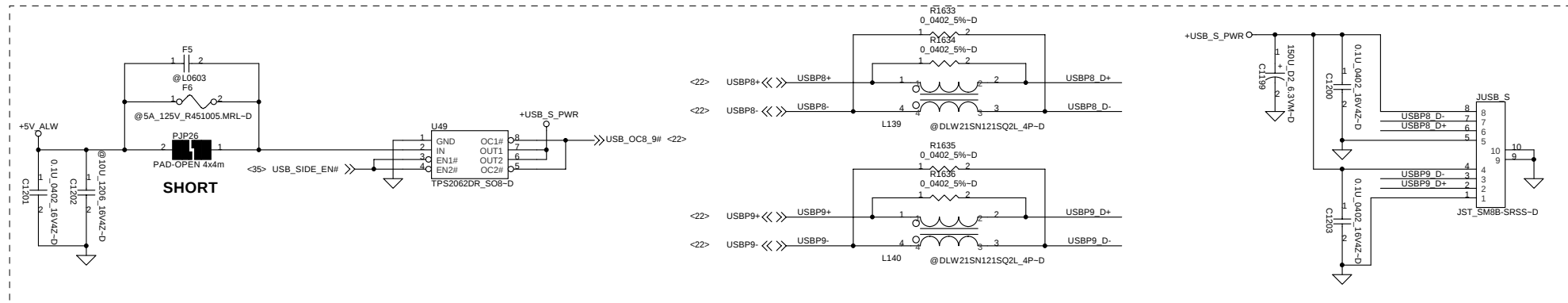


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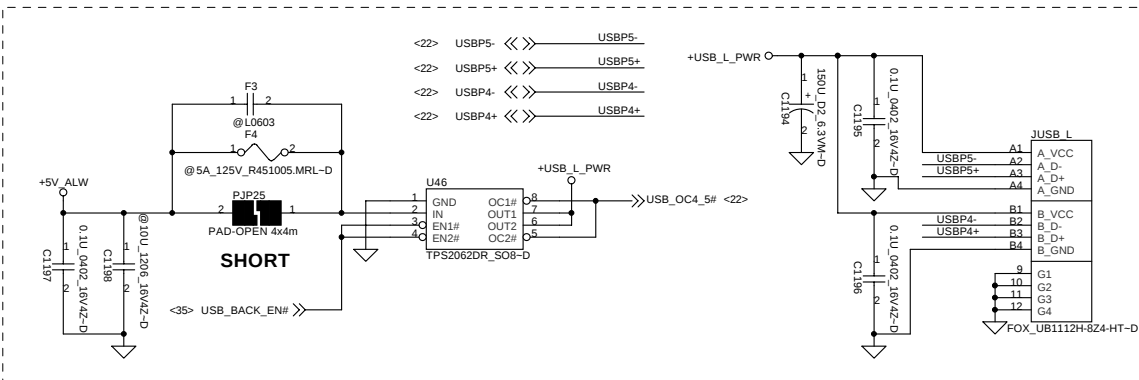
Rear Right USB Port



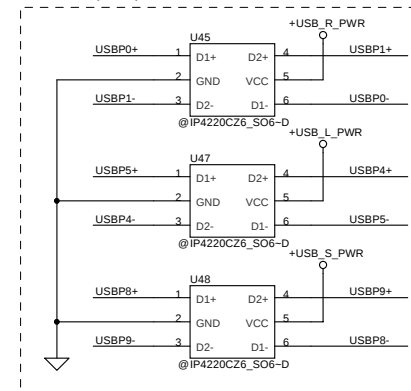
Side USB Port



Rear Left USB Port



Place U45, U47, U48 as close as USB connector



USB PORT#	DESTINATION
0	JUSB_R (Rear Right Bottom)
1	JUSB_R (Rear Right Top)
4	JUSB_L (Rear Left Bottom)
5	JUSB_L (Rear Left Top)
8	JUSB_S (Side Bottom)
9	JUSB_S (Side Top)

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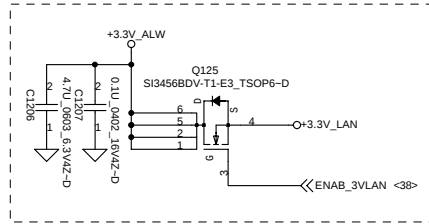
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Size Document Number 401490 Rev A

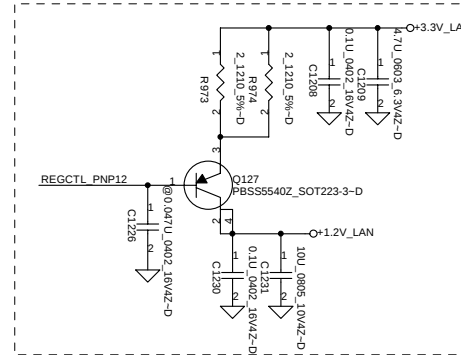
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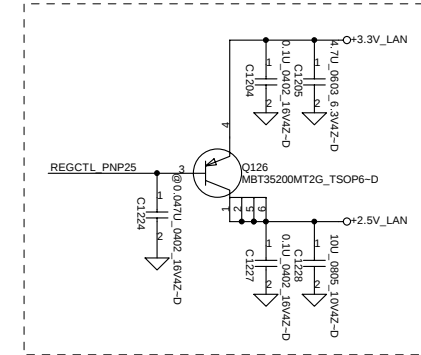
+3.3V_LAN SOURCE



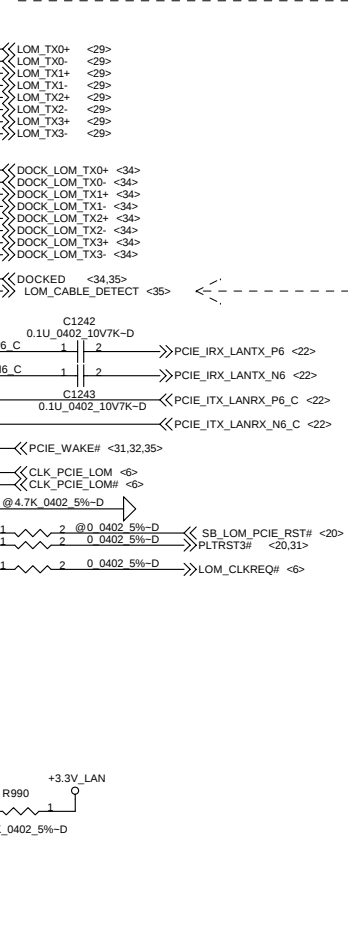
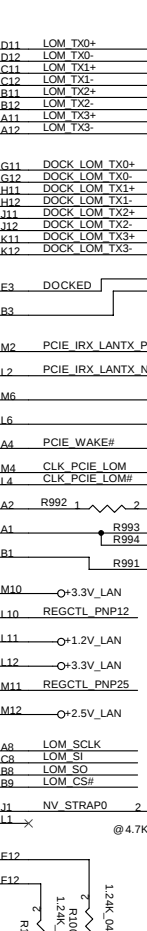
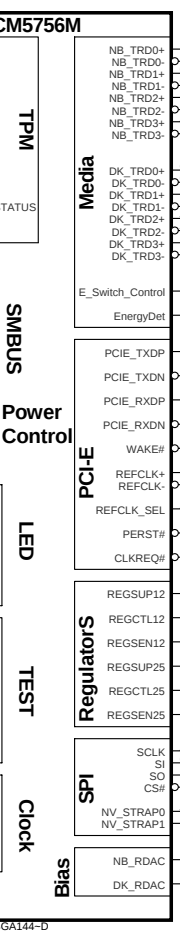
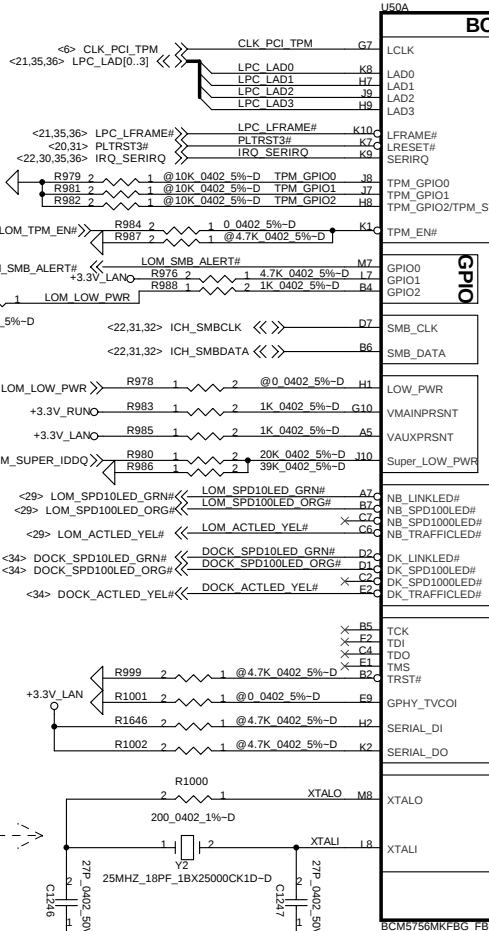
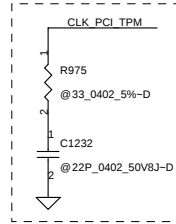
+1.2V_LAN Regulator Control



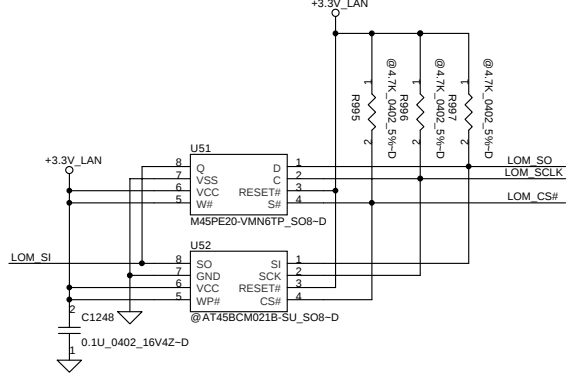
+2.5V_LAN Regulator Control



Place close to pin G7

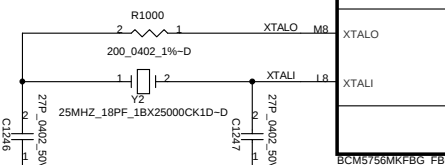


LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOW_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIOC defined by the GPIO mapping



	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Auto-Sense Mode (Default)	0	0	0	0	0	0
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

Drive level should be at least 300uW Max. power



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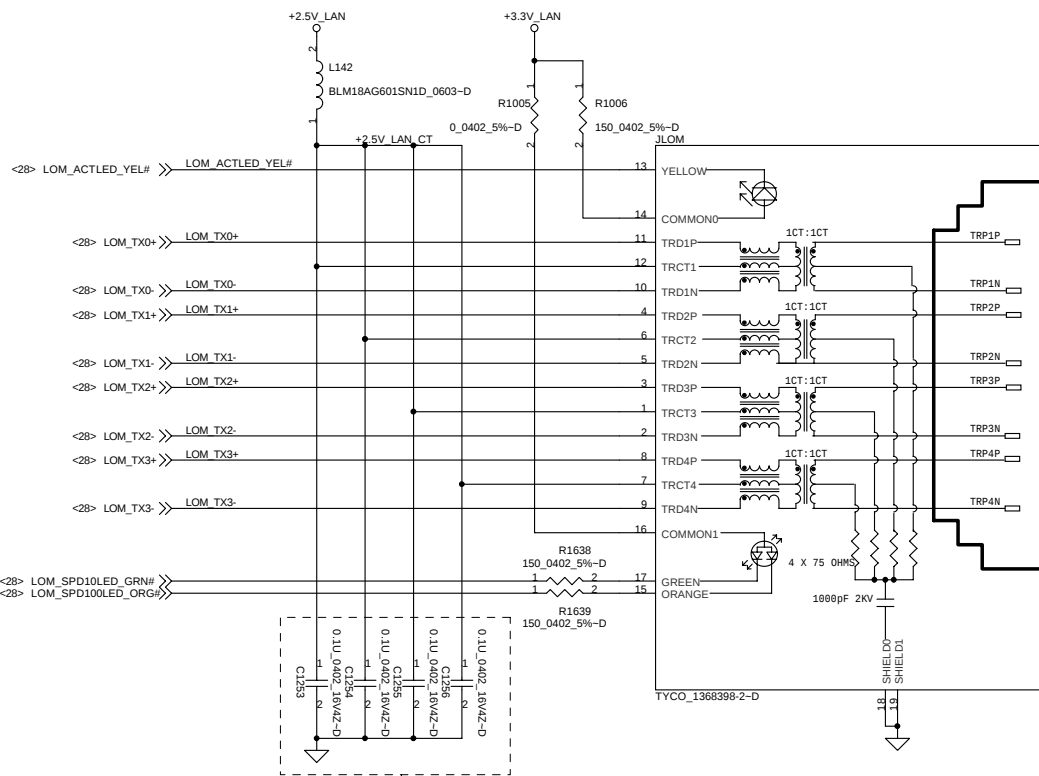
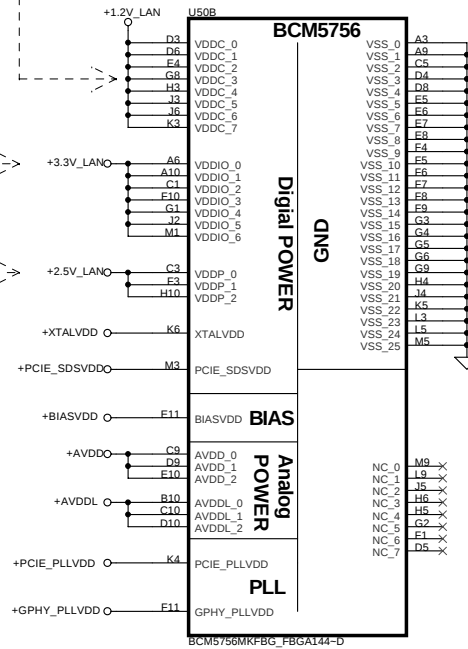
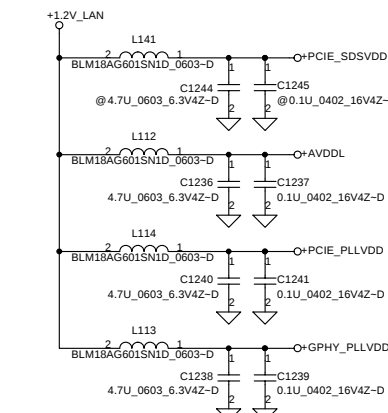
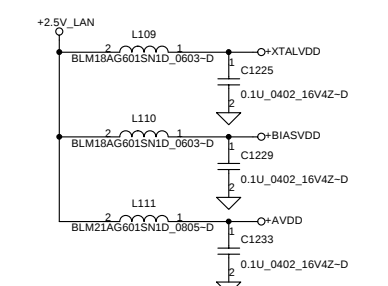
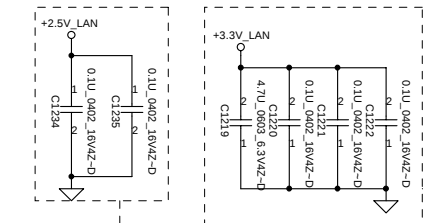
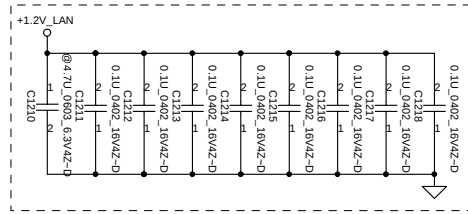
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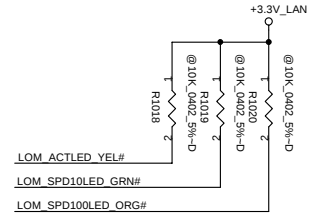
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Place as close as U50 as possible



Place these caps as close to the center tap pins of the mag/connector



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The schematic diagram illustrates the JMINI1 connector and its associated circuitry. The connector pins are numbered 1 through 54. The diagram shows the following connections and components:

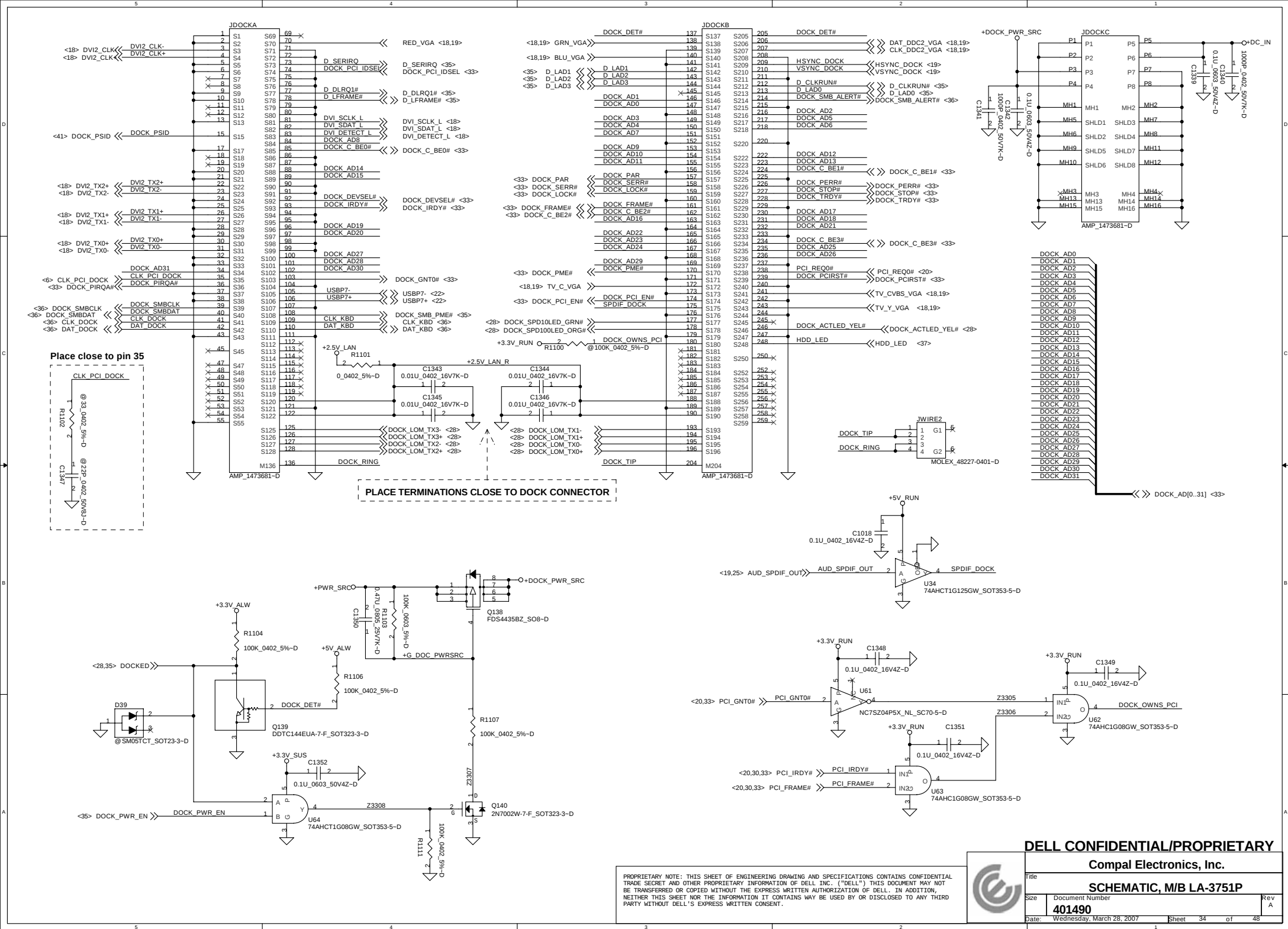
- Power Supply:**
 - +3.3V_RUN:** Connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, and 53.
 - +1.5V_RUN:** Connected to pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, and 54.
- Signal Connections:**
 - PCIE_WAKE#:** Connected to pin 1.
 - MINI1_CLKREQ#:** Connected to pin 3.
 - CLK_PCIE_MINI1#:** Connected to pins 5 and 7.
 - PCIE_IRX_ROBSONTX_N1:** Connected to pin 23.
 - PCIE_IRX_ROBSONTX_P1:** Connected to pin 25.
 - PCIE_ITX_ROBSONRX_N1_C:** Connected to pin 31.
 - PCIE_ITX_ROBSONRX_P1_C:** Connected to pin 33.
 - PCIE_MCARD2_DET#:** Connected to pin 41.
 - ROBSON_RADIO_DIS#:** Connected to pin 35.
 - ROBSON_PLTRST3# R:** Connected to pin 20.
 - ROBSON_SCLK:** Connected to pin 28.
 - ROBSON_SDATA:** Connected to pin 32.
 - SB_ROBSON_PCIE_RST#:** Connected to pin 20.
 - MEM_SCLK:** Connected to pin 16.
 - MEM_SDATA:** Connected to pin 16.
 - USB_MCARD2_DET#:** Connected to pin 41.
- Resistors:**
 - R1067:** 100K 0402 5%-D, connected between +3.3V_RUN and pin 41.
 - R1065:** 0 0402 5%-D, connected between pin 20 and PLTRST3#.
 - R1059:** 0 0402 5%-D, connected between pin 20 and SB_ROBSON_PCIE_RST#.
 - R1643:** 0 0402 5%-D, connected between pin 28 and MEM_SCLK.
 - R1644:** 0 0402 5%-D, connected between pin 32 and MEM_SDATA.
 - R1610:** 0 0402 5%-D, connected between pin 41 and USB_MCARD2_DET#.
 - R1068:** 100K 0402 5%-D, connected between pin 41 and +3.3V_RUN.
- Capacitors:**
 - C1293:** 220 0805, 6.3V6M-D, connected between +3.3V_RUN and ground.
 - C1297:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1298:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1299:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1294:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1295:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1296:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1297:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1298:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
 - C1299:** 33p 0402, 50V6A-D, connected between +3.3V_RUN and ground.
- Other Components:**
 - T96:** A temperature sensor or diode connected to pin 41.
 - GND1, GND2:** Ground connections for the connector.

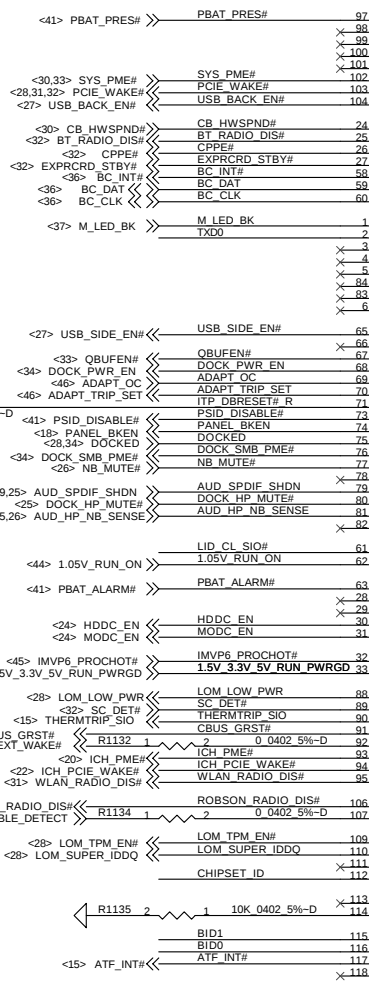
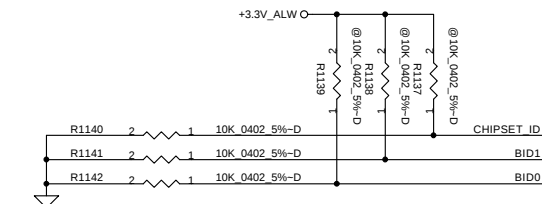
The diagram is labeled with the part number **TYCO_1775838-1-D** at the bottom.

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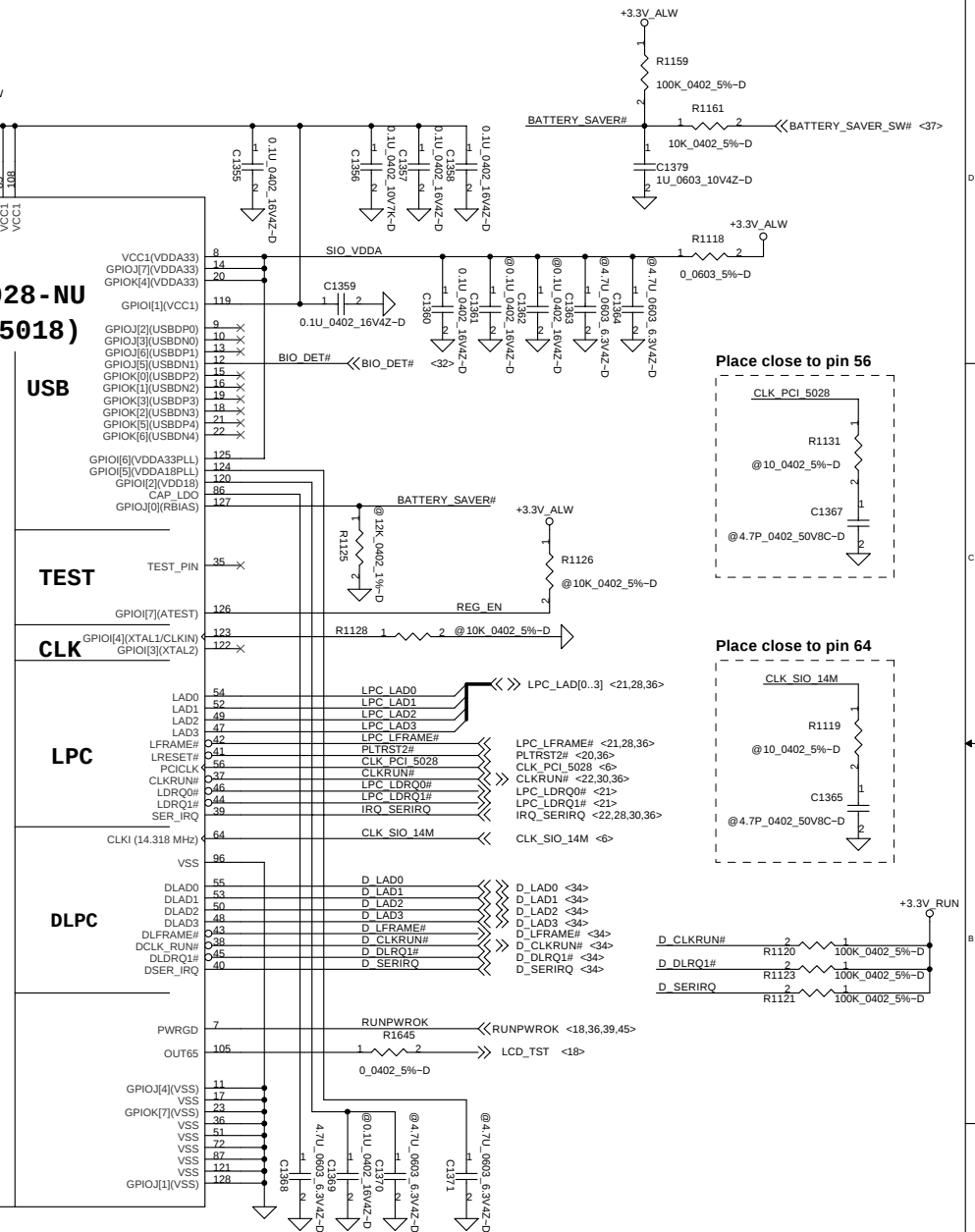
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REV	BID1	BID0
X00	0	0
X01	0	1



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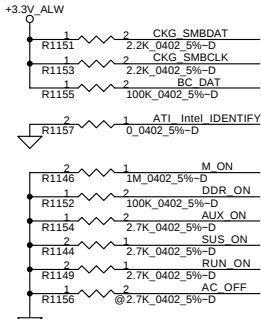
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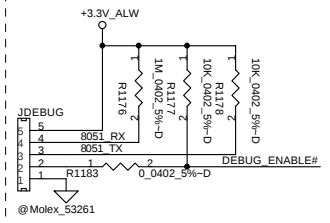
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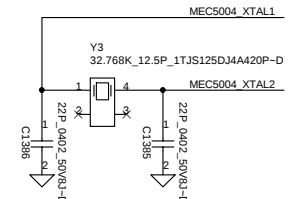
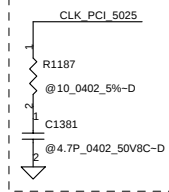
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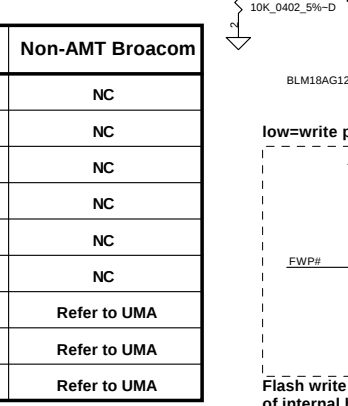
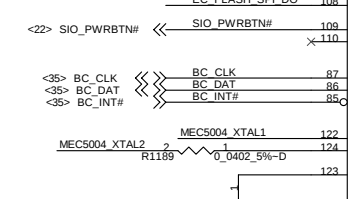
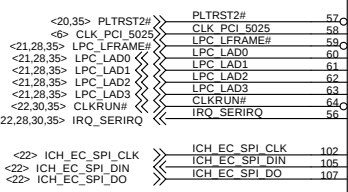
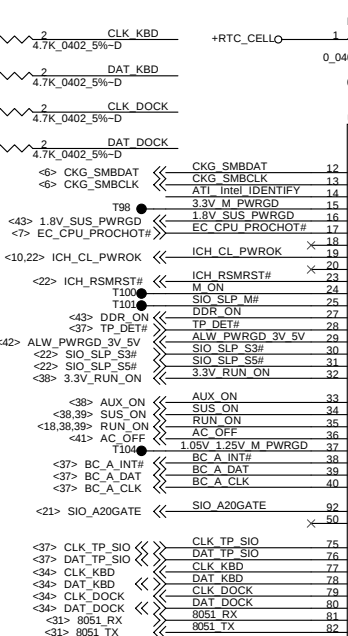
R1752 no stuff when doing flash recovery



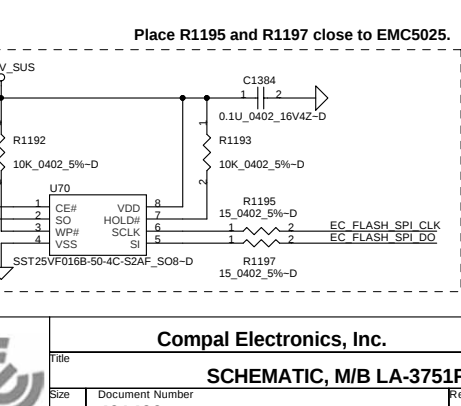
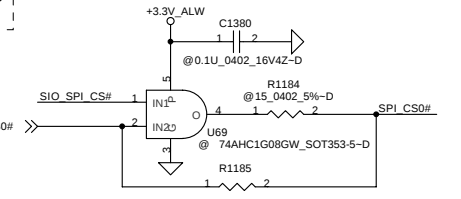
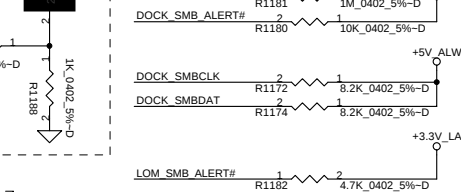
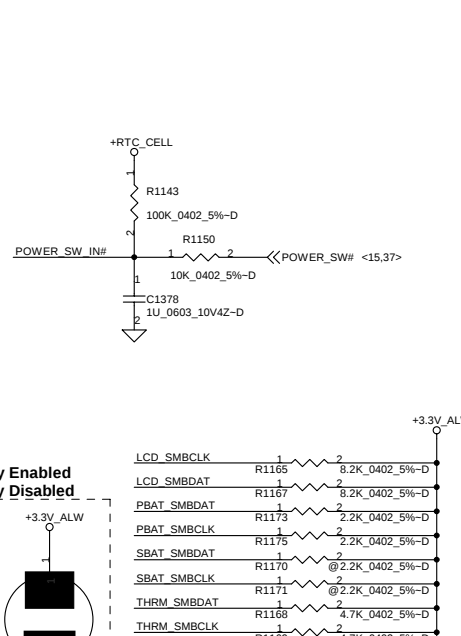
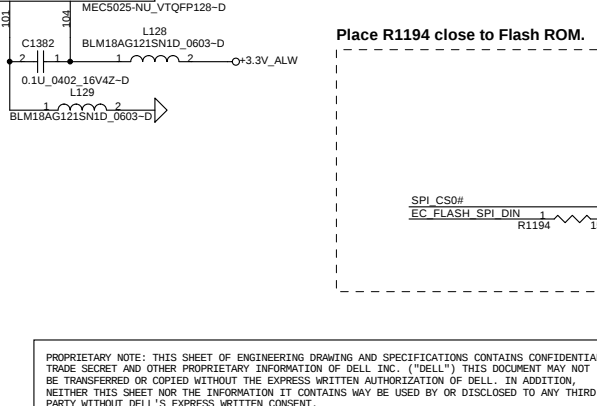
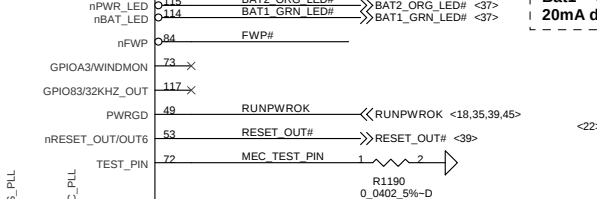
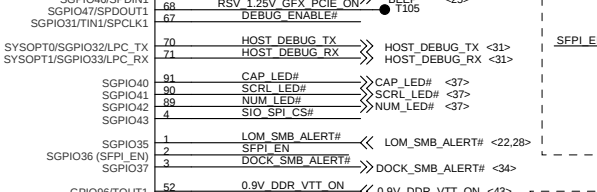
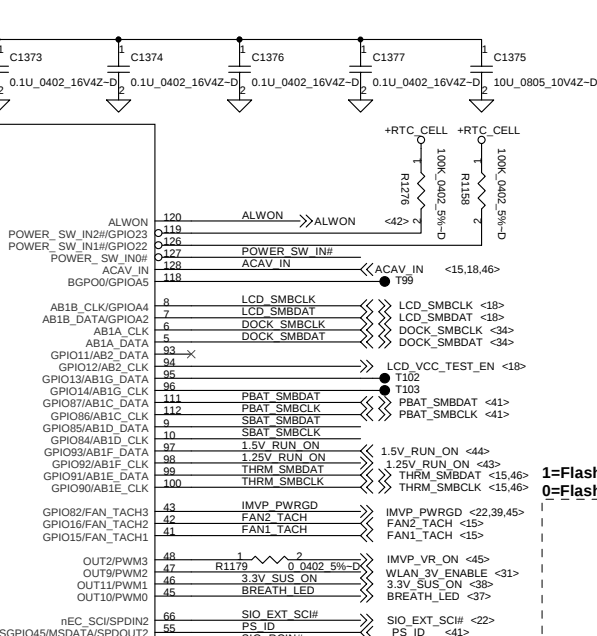
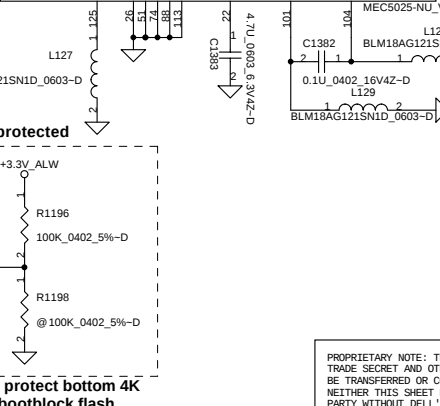
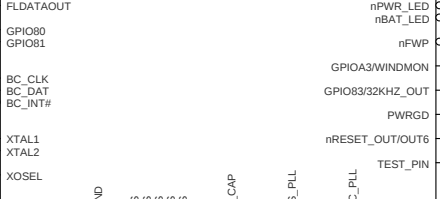
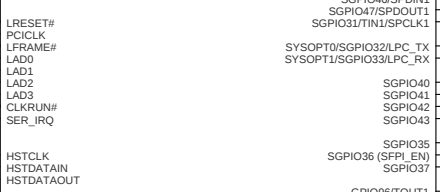
Place close to pin 58



Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
CH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA
LOM_LOW_PWR	NC	Refer to UMA
LOM_CABLE_DETECT	NC	Refer to UMA



Flash write protect bottom 4K of internal bootblock flash



1=Flash Recovery Enabled
0=Flash Recovery Disabled

Bat2 = Amber LED
Bat1 = Green LED
20mA drive pins

Place R1194 close to Flash ROM.

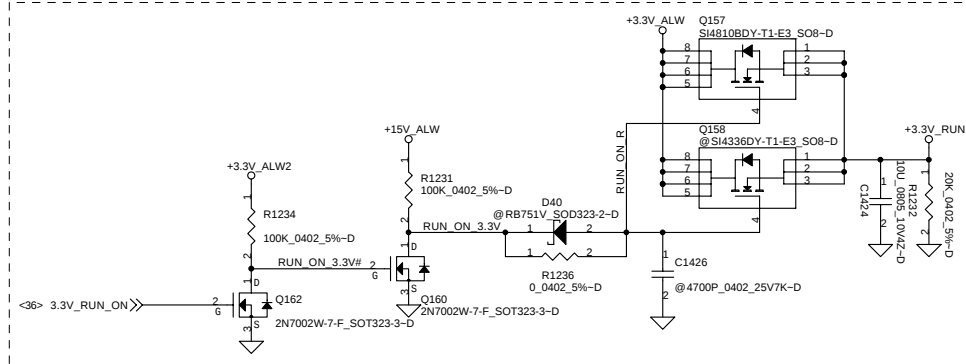
Place R1195 and R1197 close to EMC5025.

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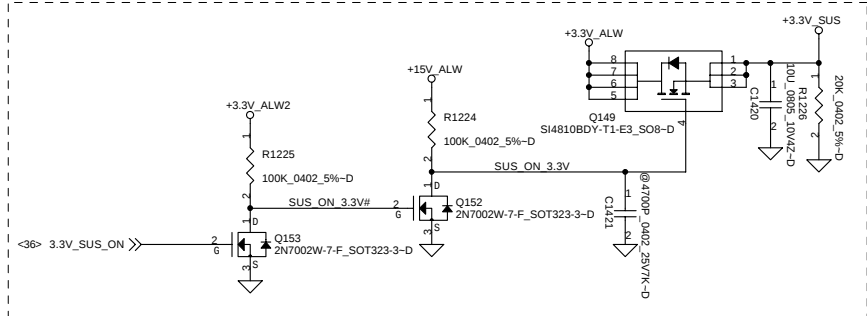


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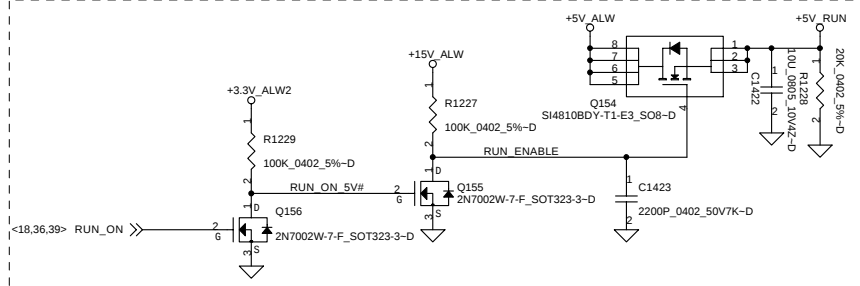
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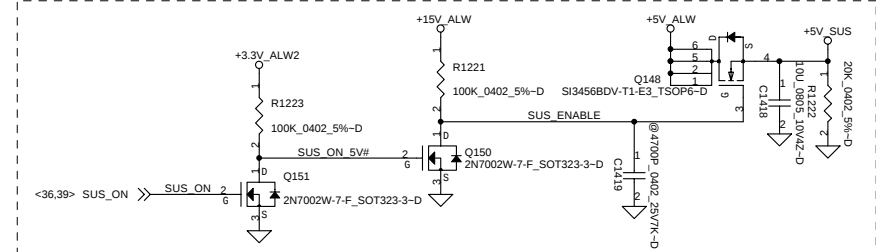
+3.3V_SUS Source



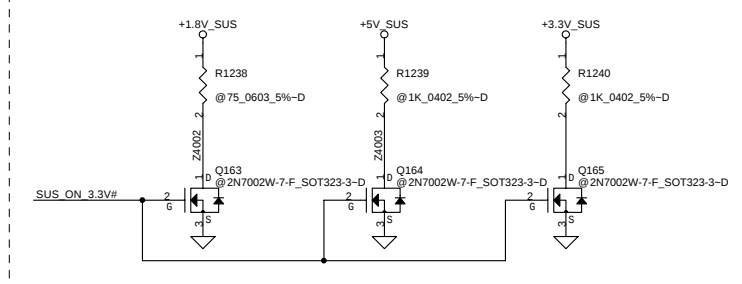
+5V_RUN Source



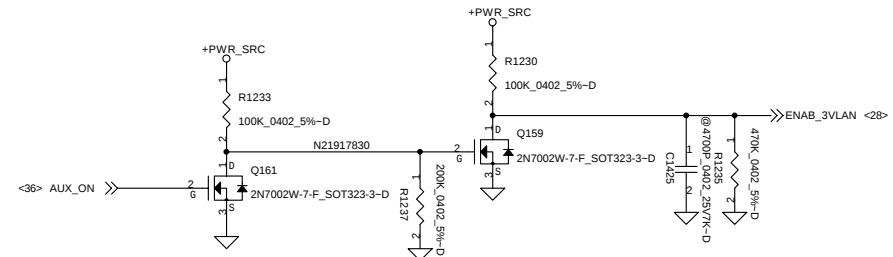
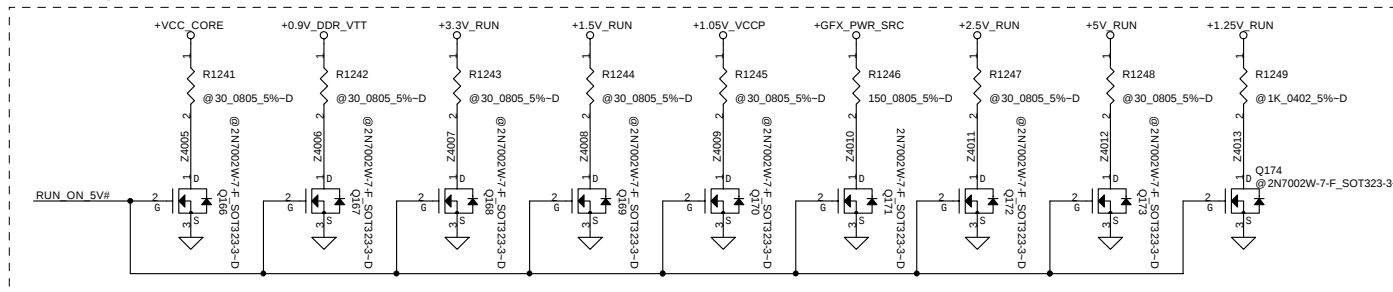
+5V_SUS Source



Discharg Circuit



Discharg Circuit



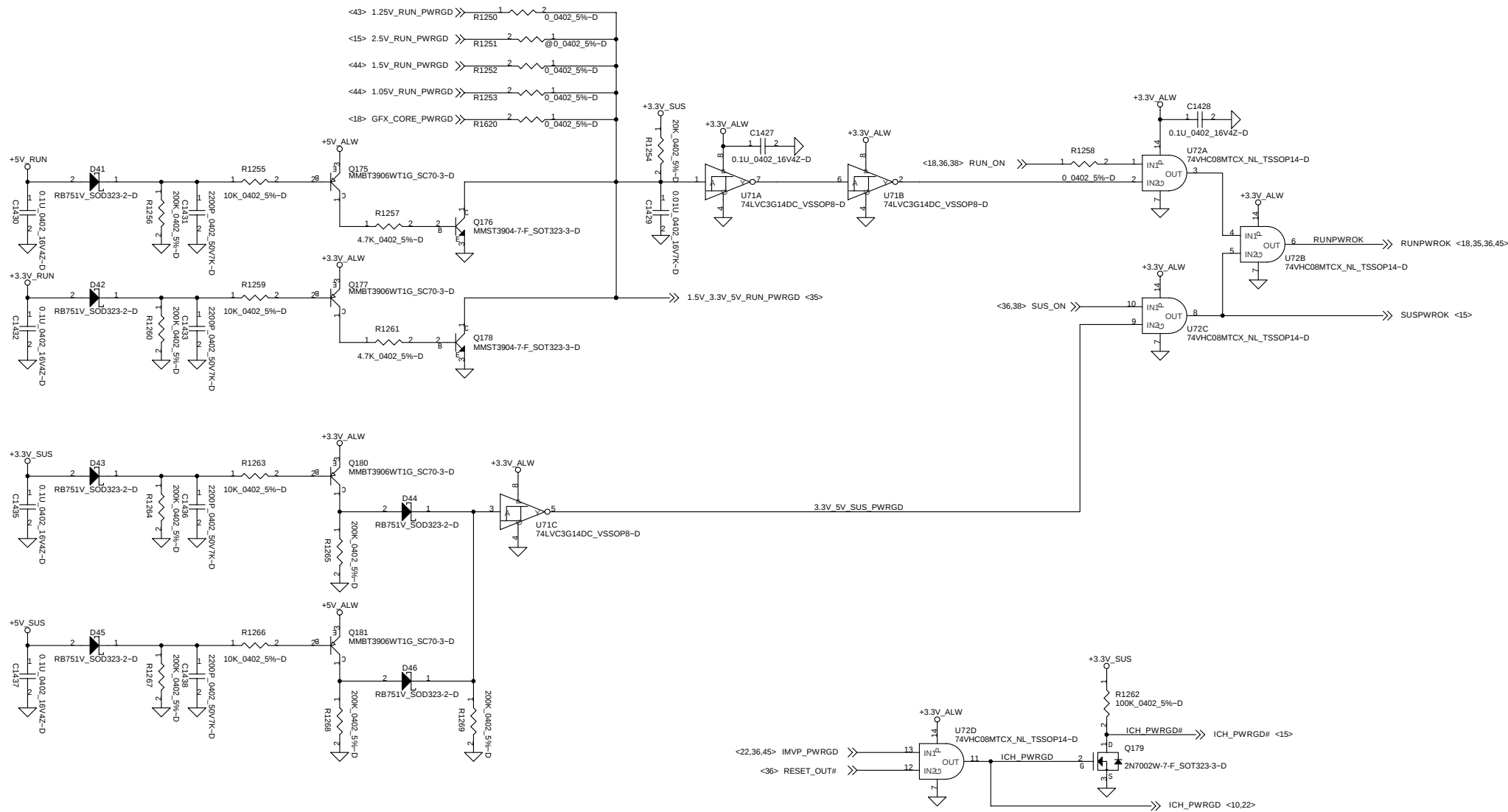
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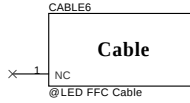
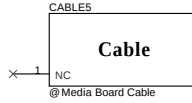
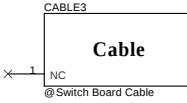
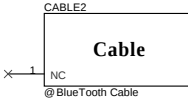
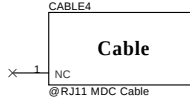
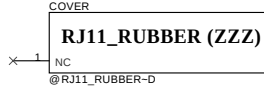
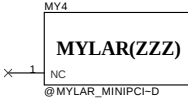
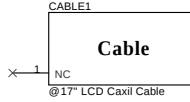
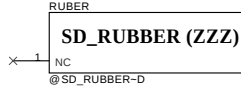
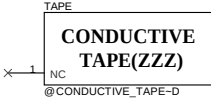
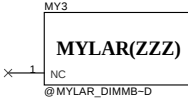
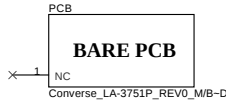
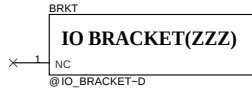
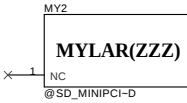
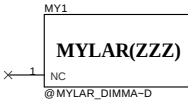
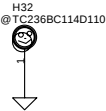
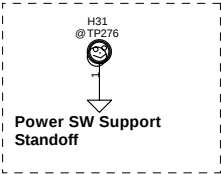
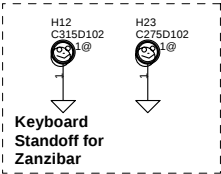
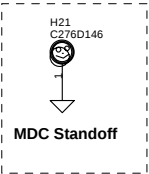
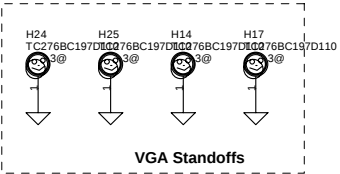
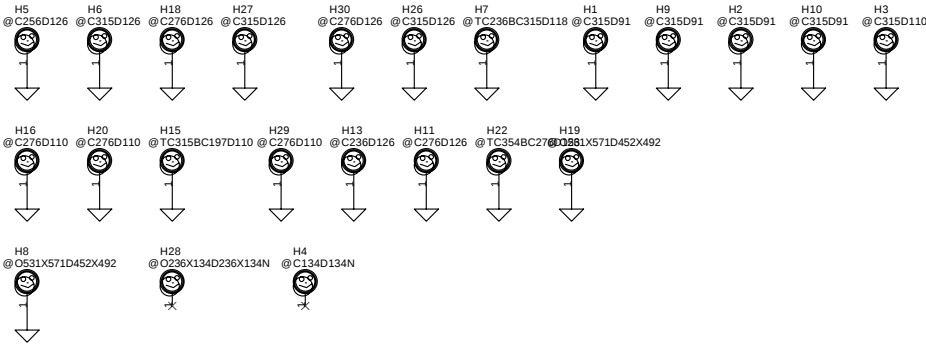
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Fiducial Mark

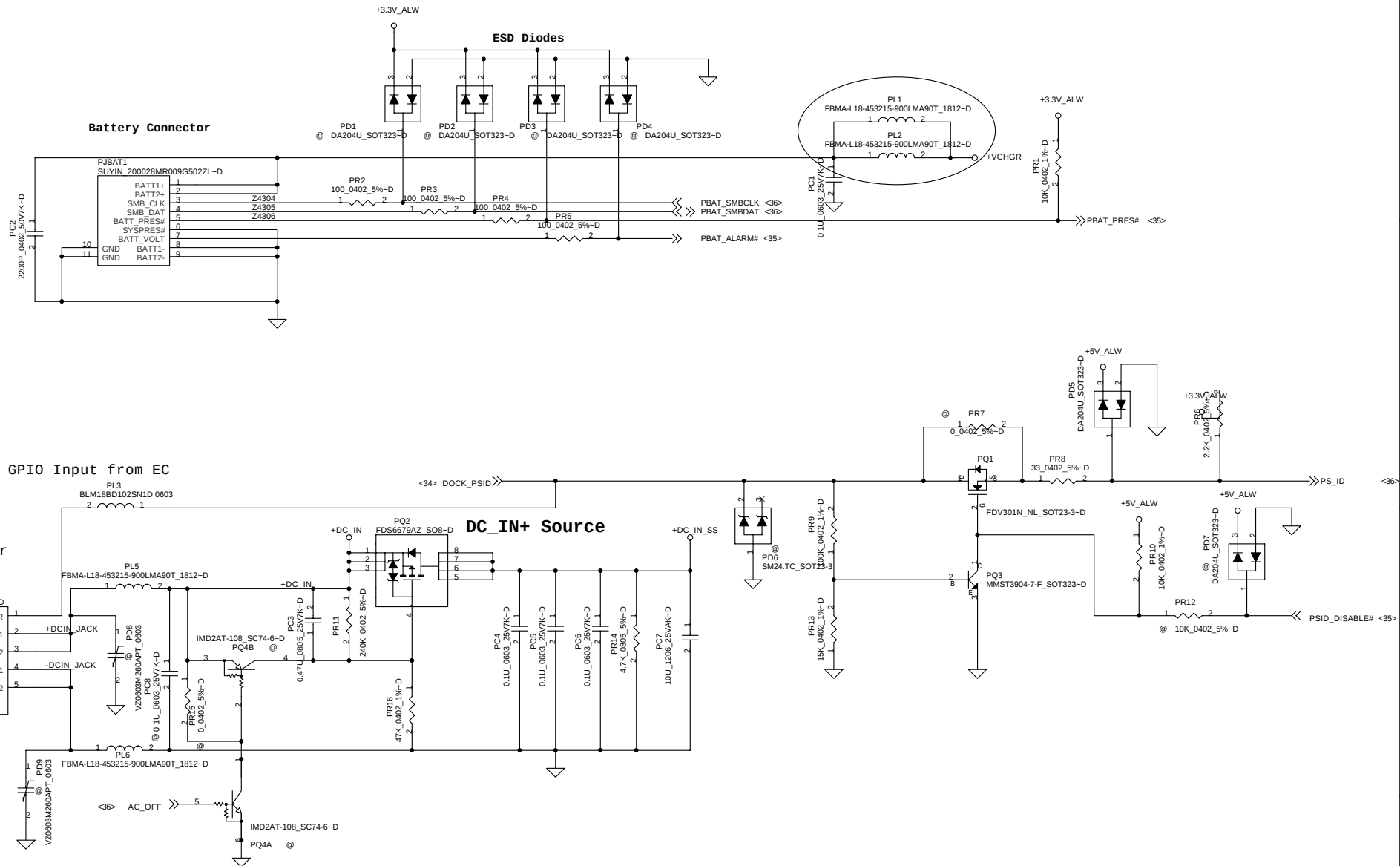


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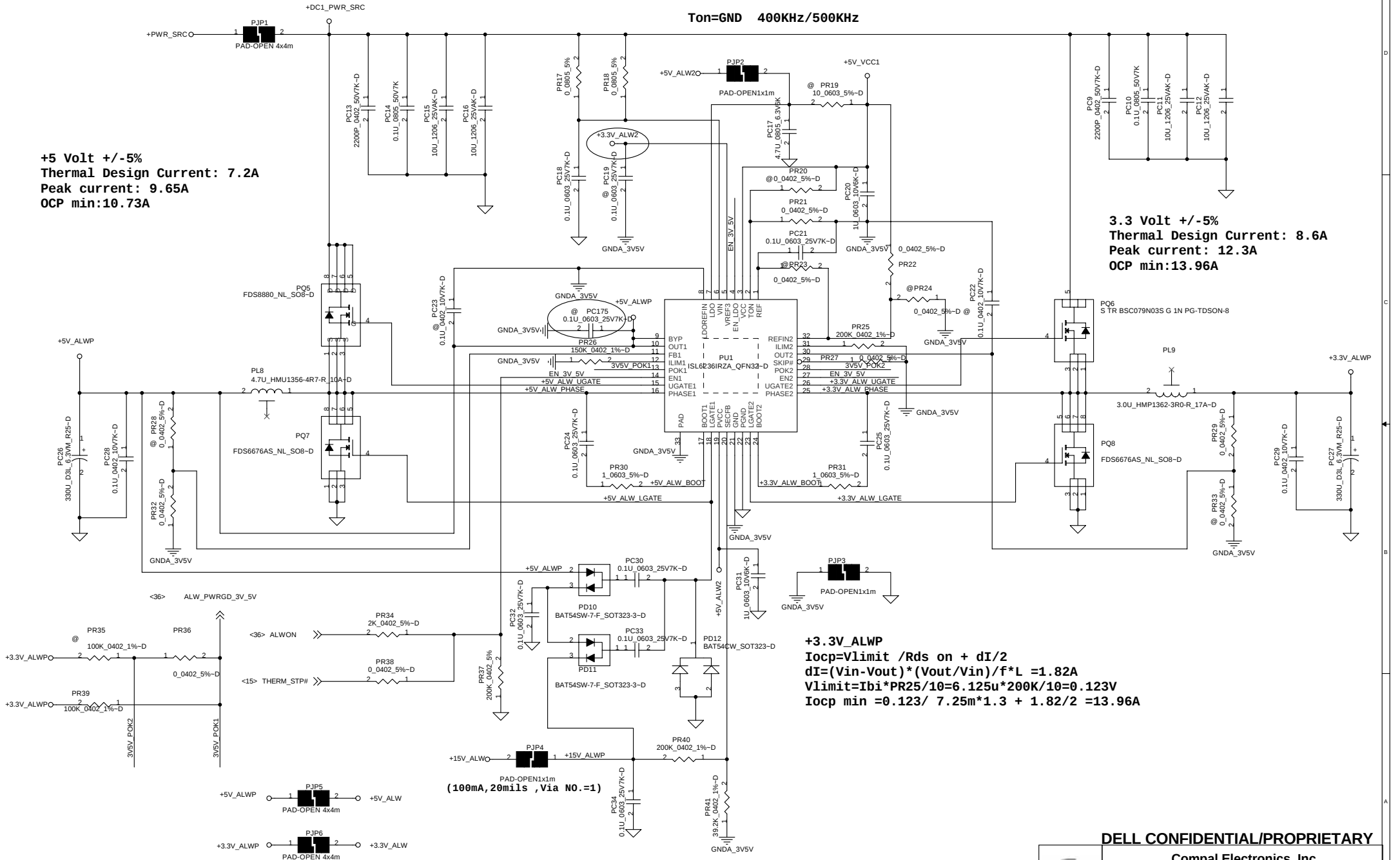
+5V_ALWP
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 1.96A$
 $V_{limit} = I_{bi} * PR26 / 10 = 6.125u * 150K / 10 = 0.92V$
 $I_{ocp\ min} = 0.92 / 7.25m * 1.3 + 1.96 / 2 = 10.73A$

+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/+15V_SUBW00FERP

Ton=GND 400KHz/500KHz

+5 Volt +/-5%
Thermal Design Current: 7.2A
Peak current: 9.65A
OCp min:10.73A

3.3 Volt +/-5%
Thermal Design Current: 8.6A
Peak current: 12.3A
OCp min:13.96A



+3.3V_ALWP
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 1.82A$
 $V_{limit} = I_{bi} * PR25 / 10 = 6.125u * 200K / 10 = 0.123V$
 $I_{ocp\ min} = 0.123 / 7.25m * 1.3 + 1.82 / 2 = 13.96A$

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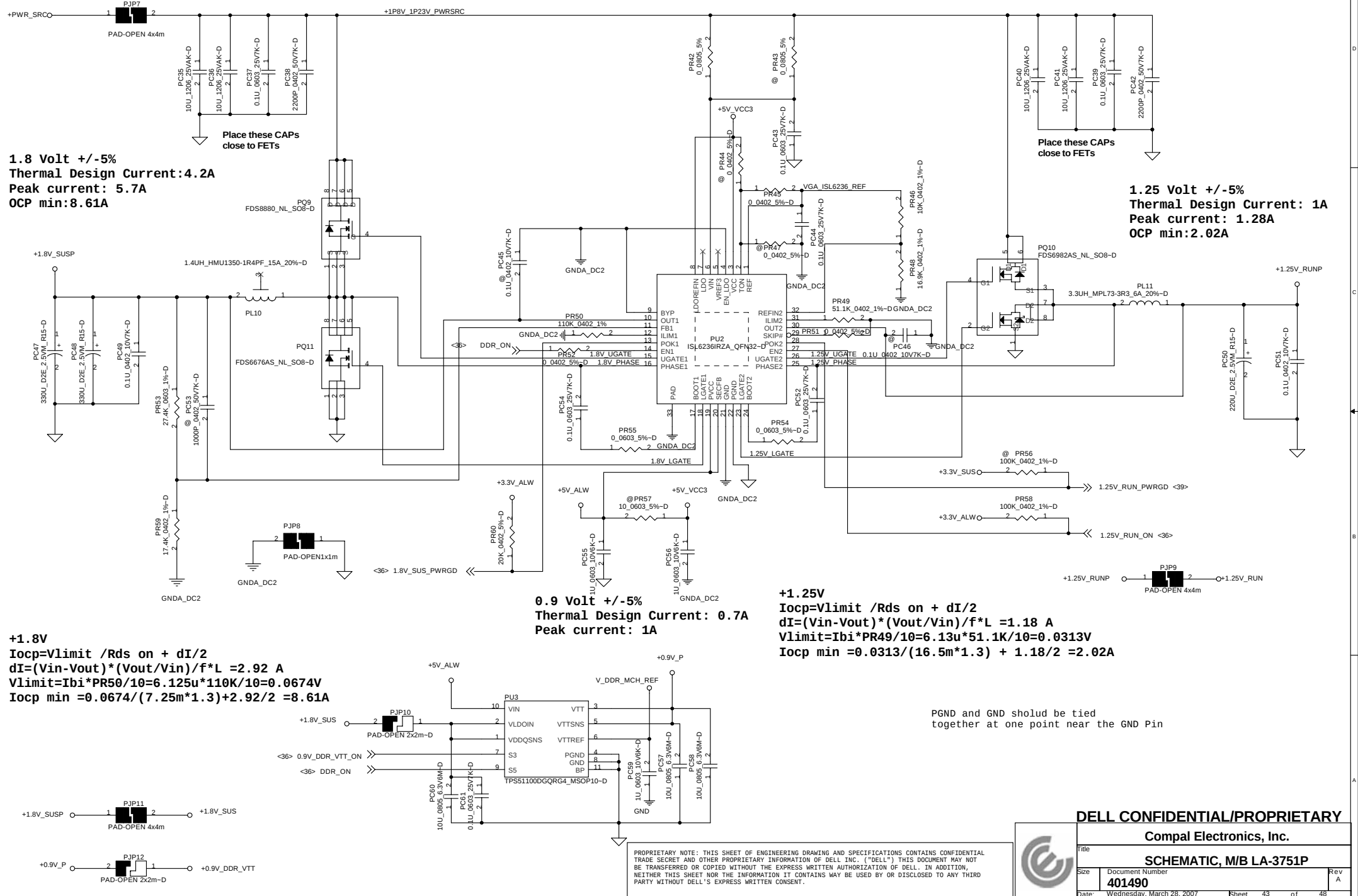
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1.8V/1.25V/0.9V VTT

Ton=REF 400KHz/300KHz



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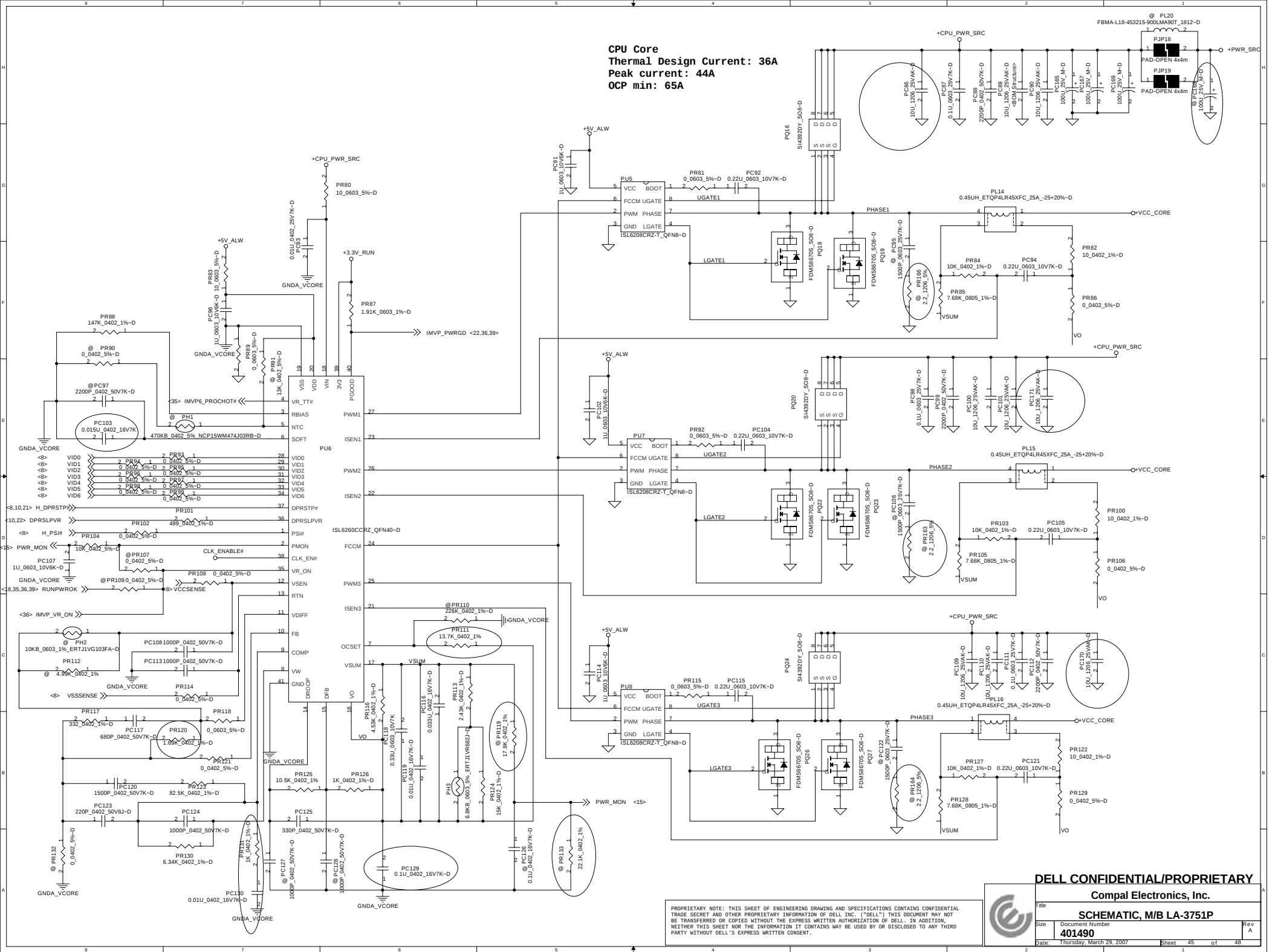
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CPU Core
Thermal Design Current: 36A
Peak current: 44A
OCP min: 65A



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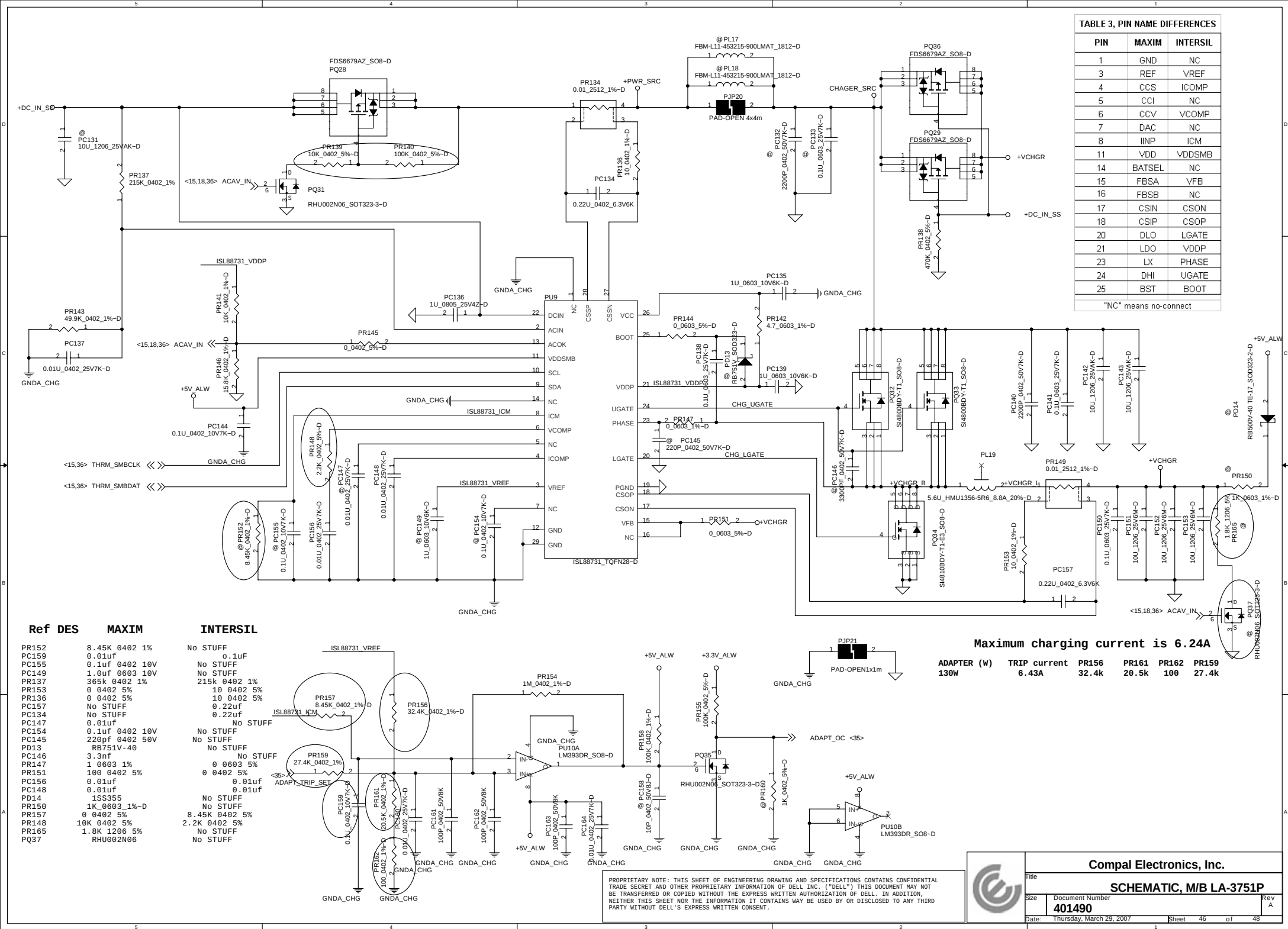
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