Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel Crestline + ICH8-M core logic IBT00 LA-3262P Discrete VGA (M64)

2007-08-02 **REV:1A**

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Title: *Cover Sheet*

Size: Custom | Document Number: *LA3262P_DIS_M64* | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 1 of 57

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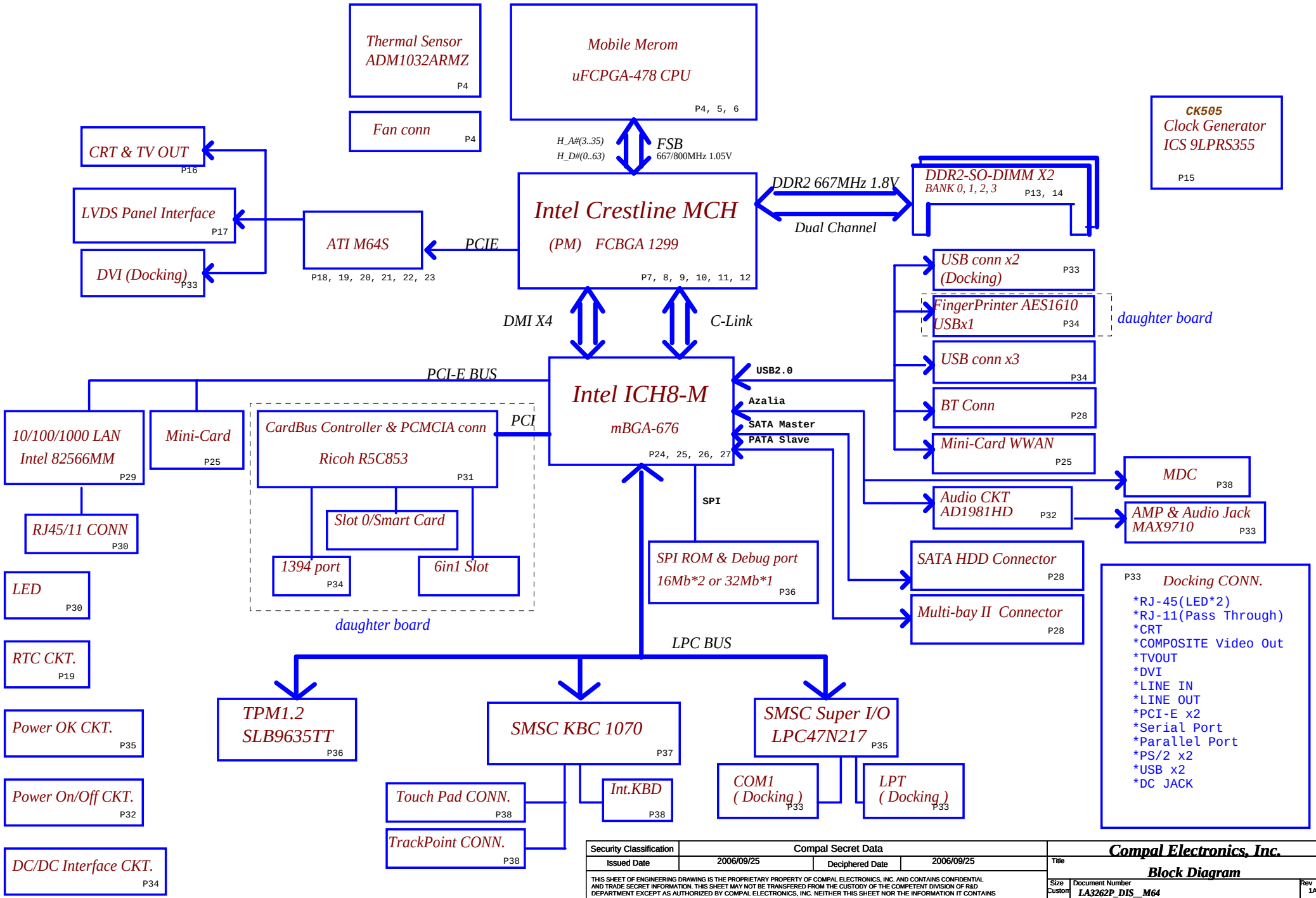
File Name : LA-3262P

Chimay Discrete



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Title: **Block Diagram**

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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/ Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up0 (Right side)
1	Fingerprint
2	Reserve
3	WWAN
4	Walk-up1 (Left Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Reserve
8	Docking
9	Docking

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass strorage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

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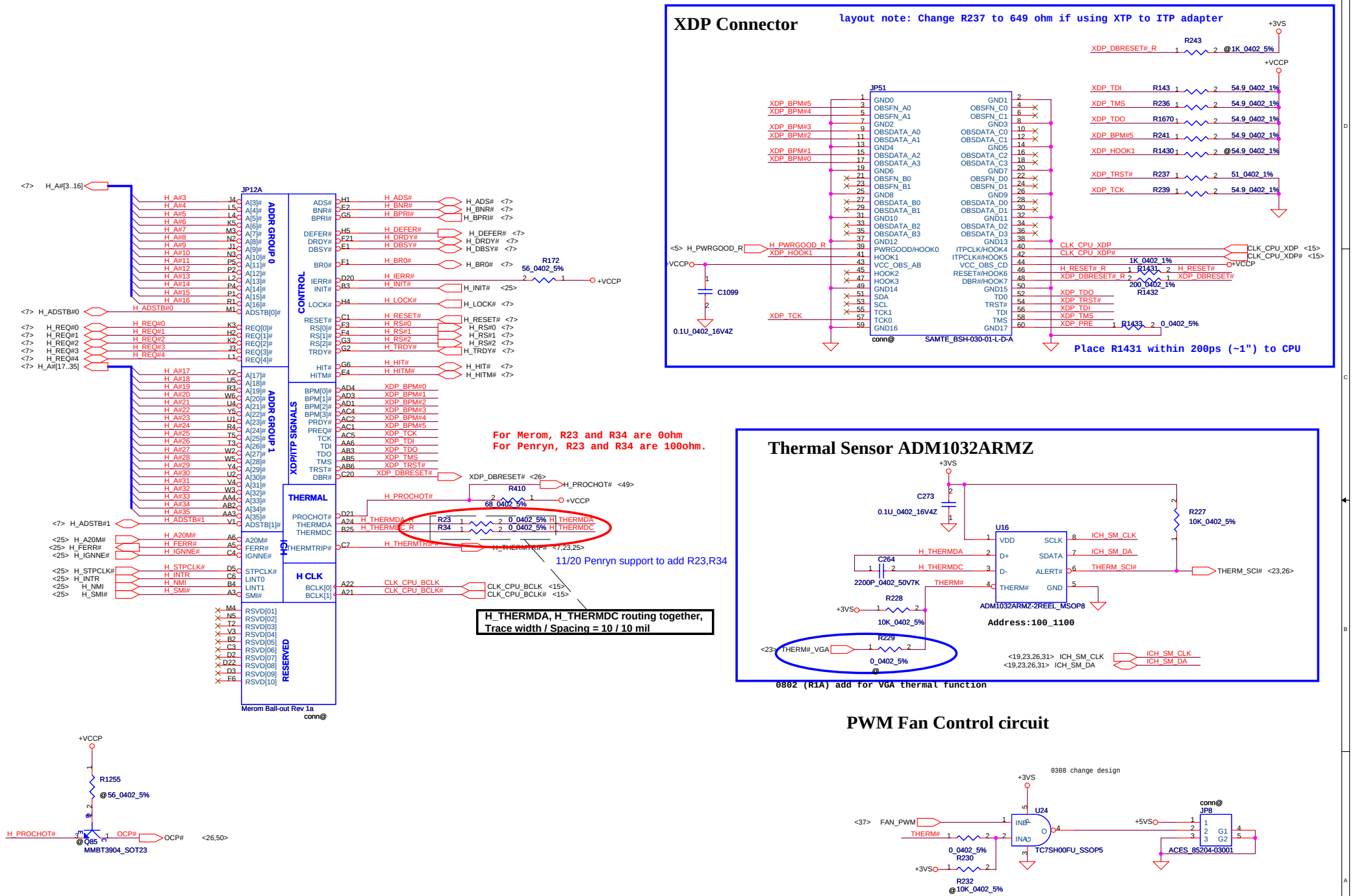

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Title: Merom(1/3)-AGTL+/XDP

Size: Custom | Document Number: LA3262P_DIS__M64 | Rev: 1A

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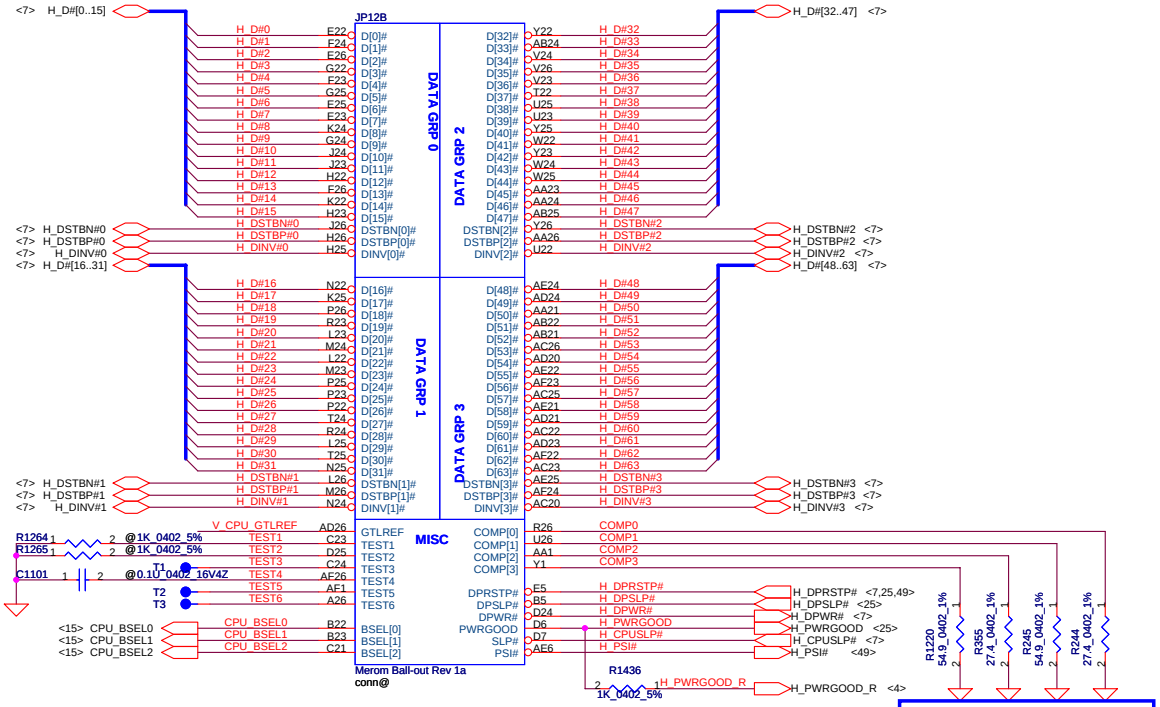
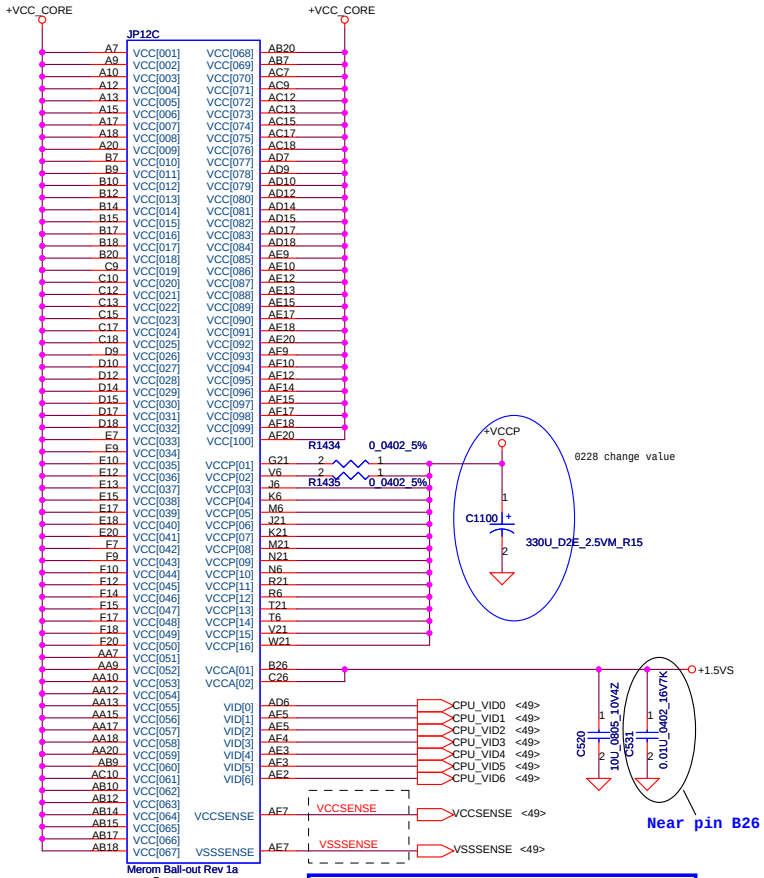


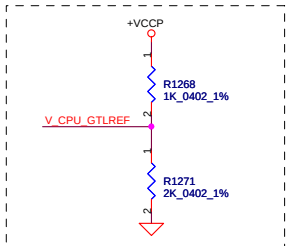
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

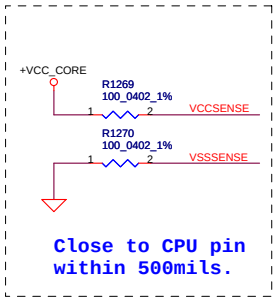
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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Title: **Merom(2/3)-AGTL+/PWR**

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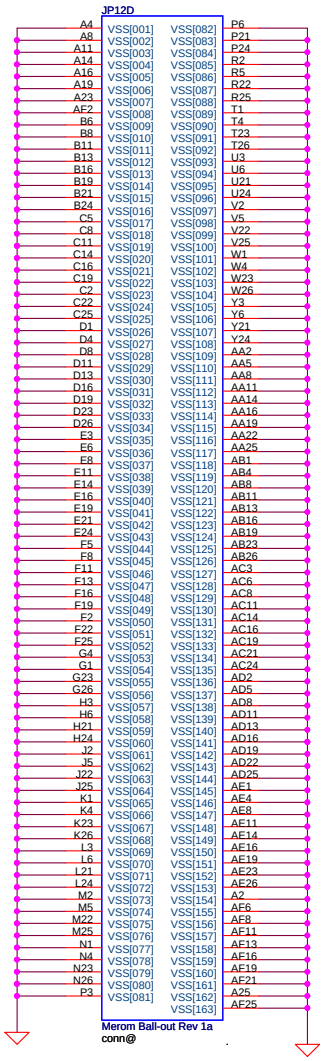
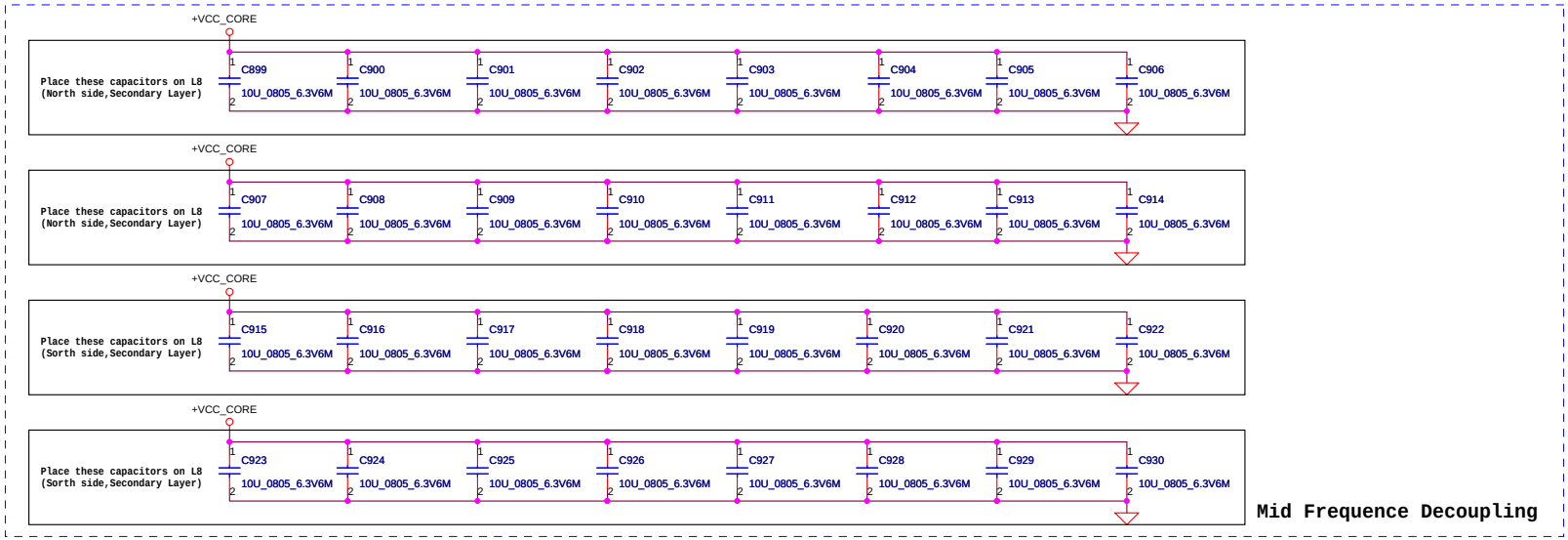
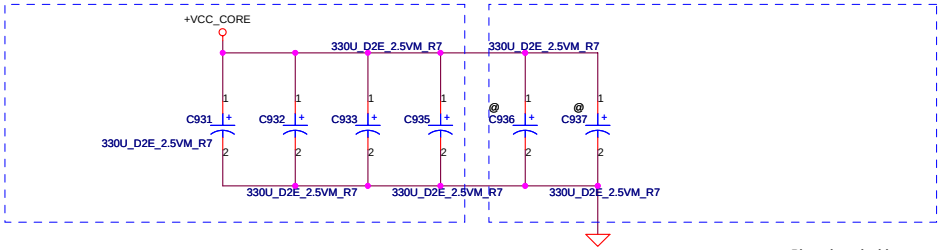


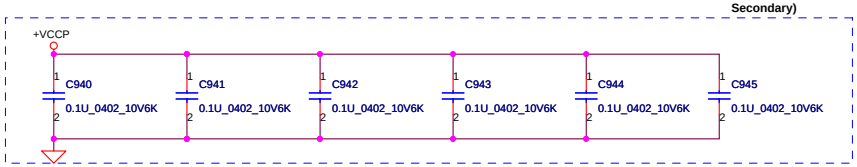


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



Place these inside socket cavity on L8 (North side Secondary)



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Title: **Merom(3/3)-GND&Bypass**

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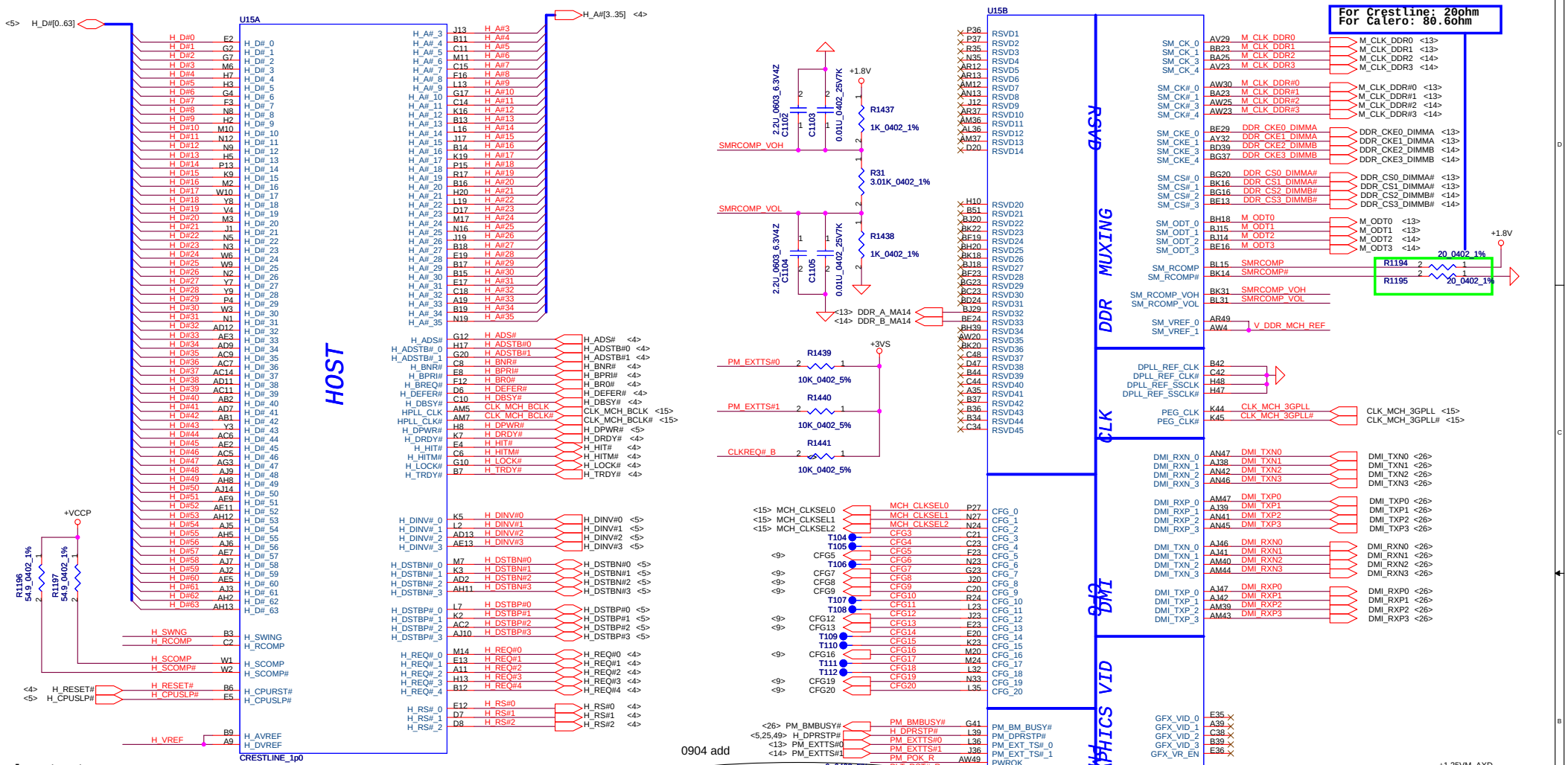
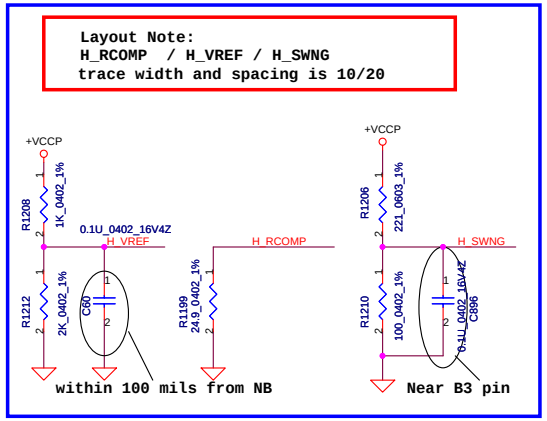
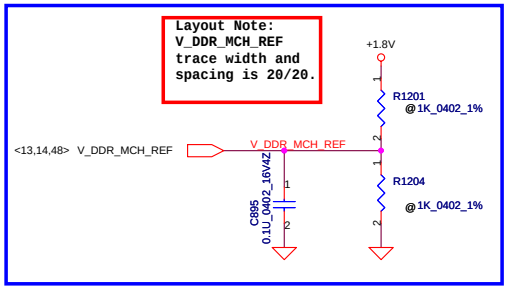


layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces





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Title: **CRESTLINE(1/6)-AGTL+/DMI/DDR2**

Size	Document Number	Rev
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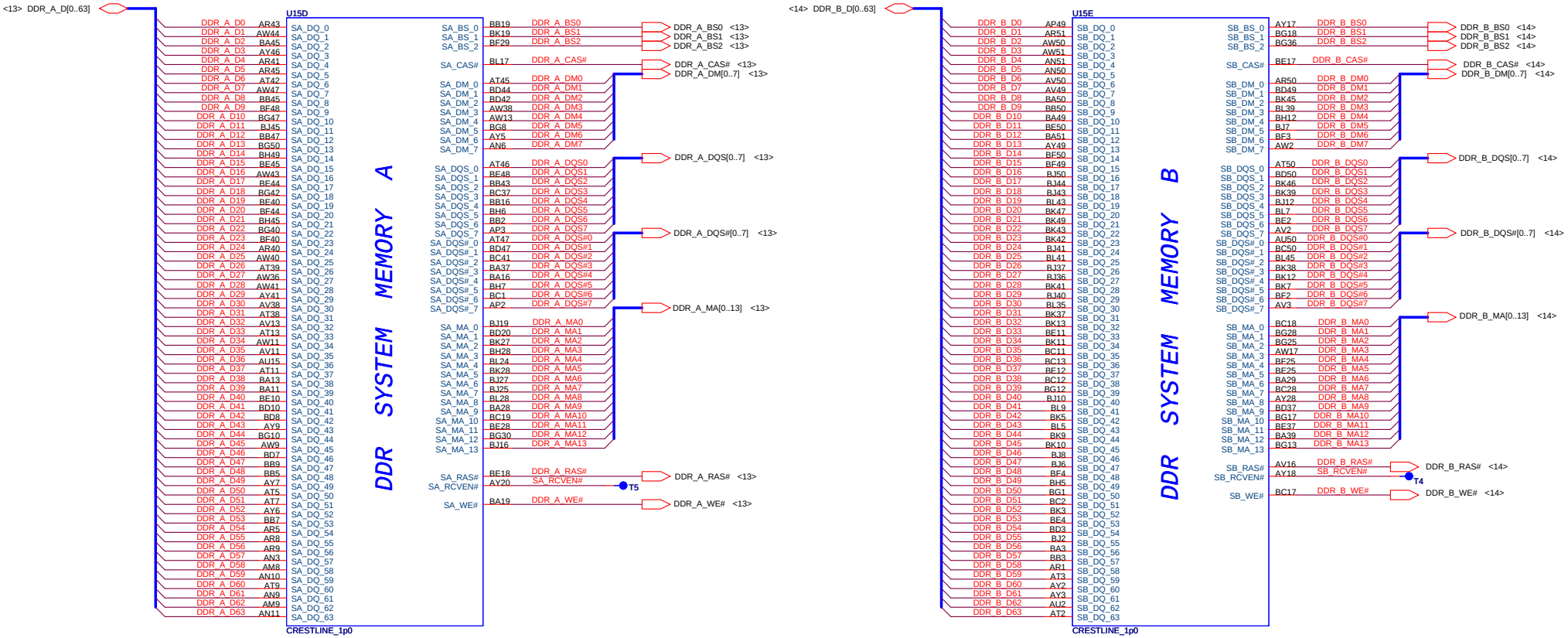

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Title: **CRESTLINE((2/6)-DDR2 A/B CH**

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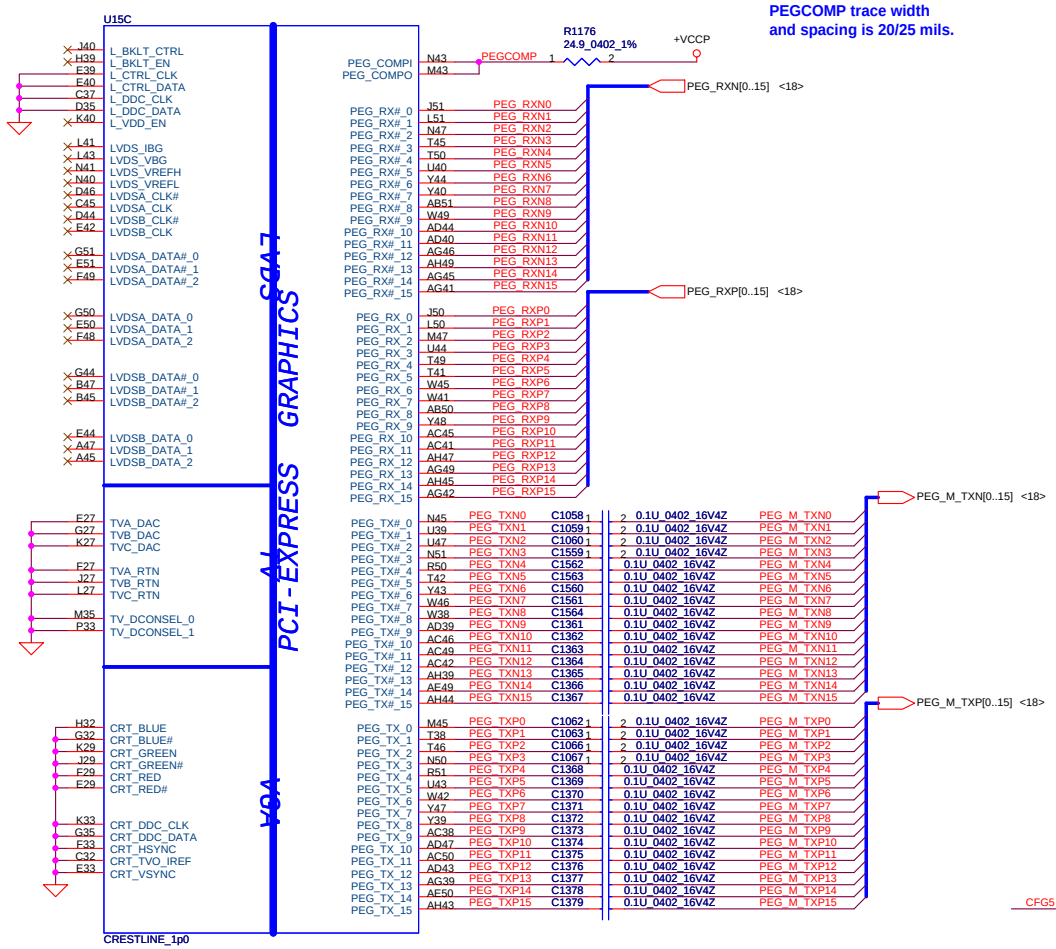
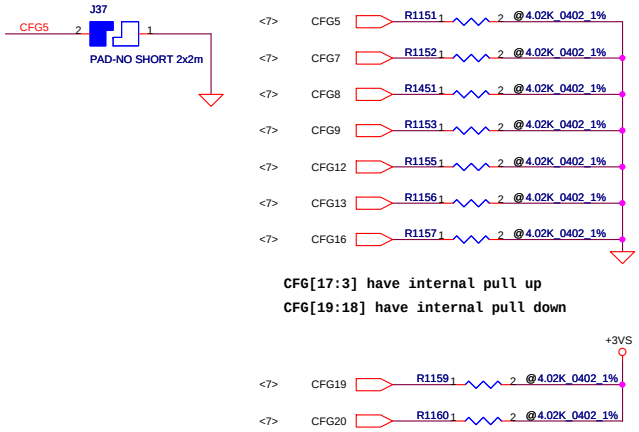


Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



CFG[17:3] have internal pull up

CFG[19:18] have internal pull down

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Title: CRESTLINE((3/6)-VGA/LVDS/TV

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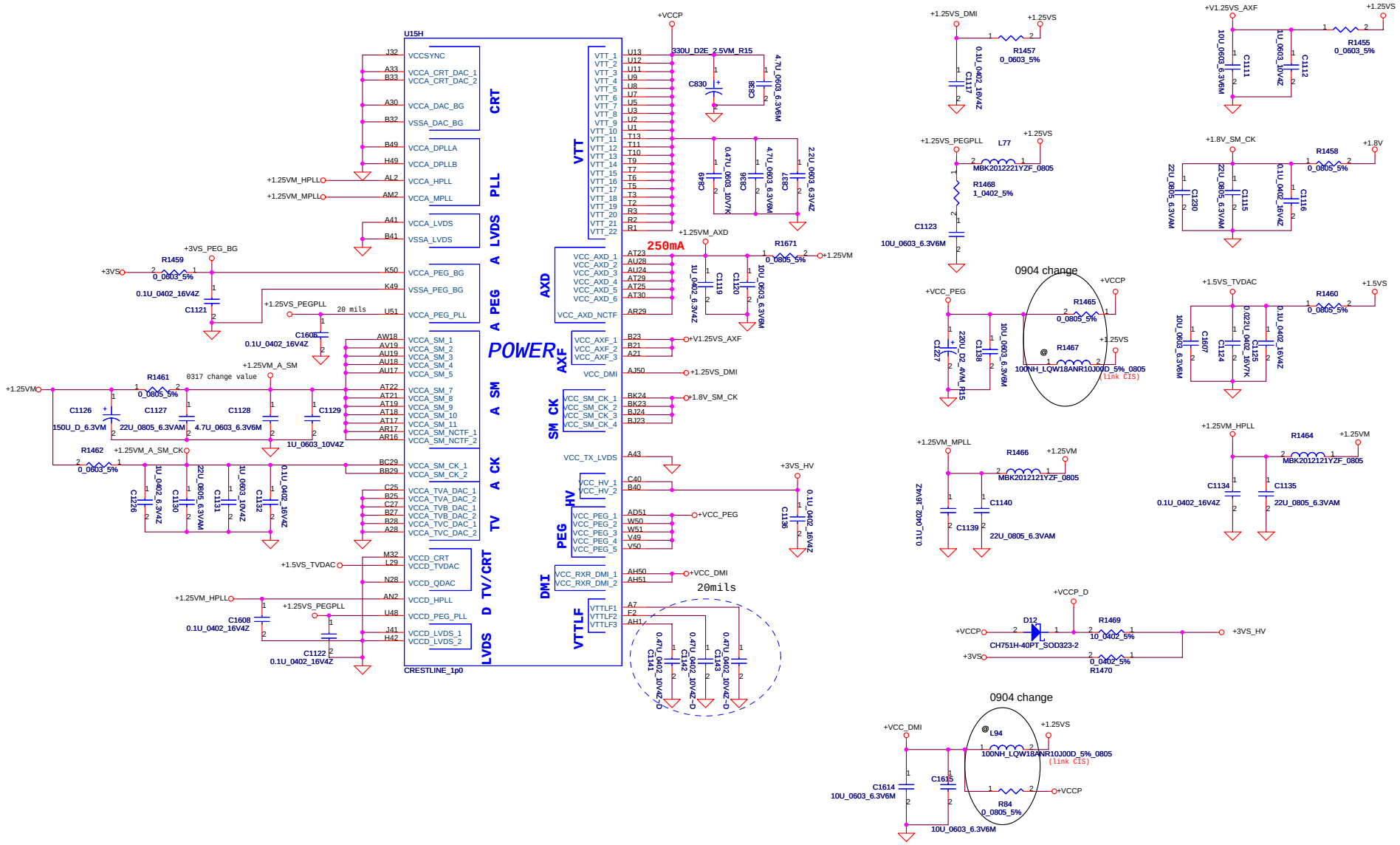

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Title: **CRESTLINE(4/6)-PWR**

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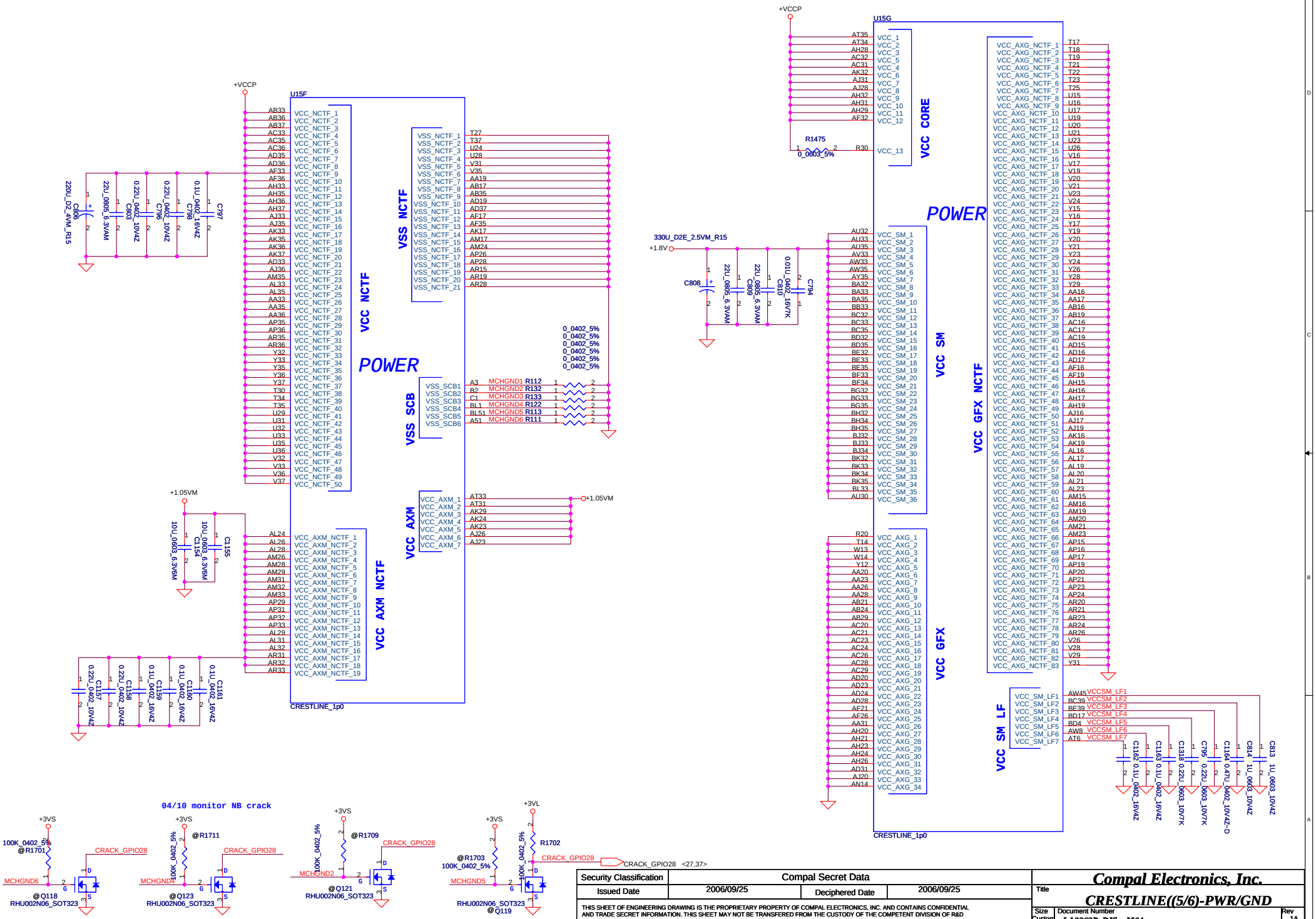
U15F
U15G
POWER
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE_1p0
+VCCP
+1.05VM
+1.8V
+3VS
+3VL
330U_D2E_2.5VM_R15
220U_D2_4VM_R15
04/10 monitor NB crack
CRACK_GPIO28
MCHGND6
MCHGND4
MCHGND2
MCHGND5
RHU002N06_SOT323
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CRESTLINE((5/6)-PWR/GND
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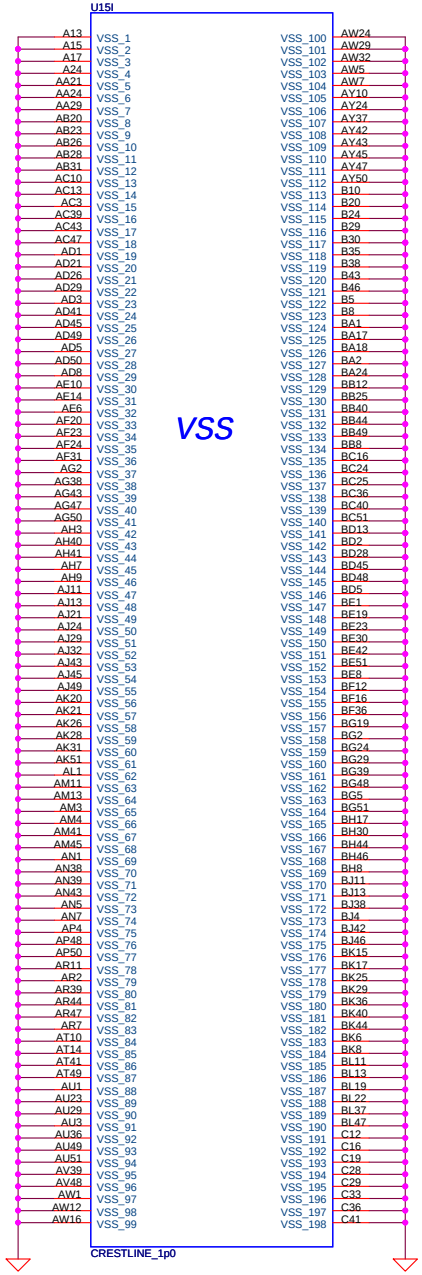

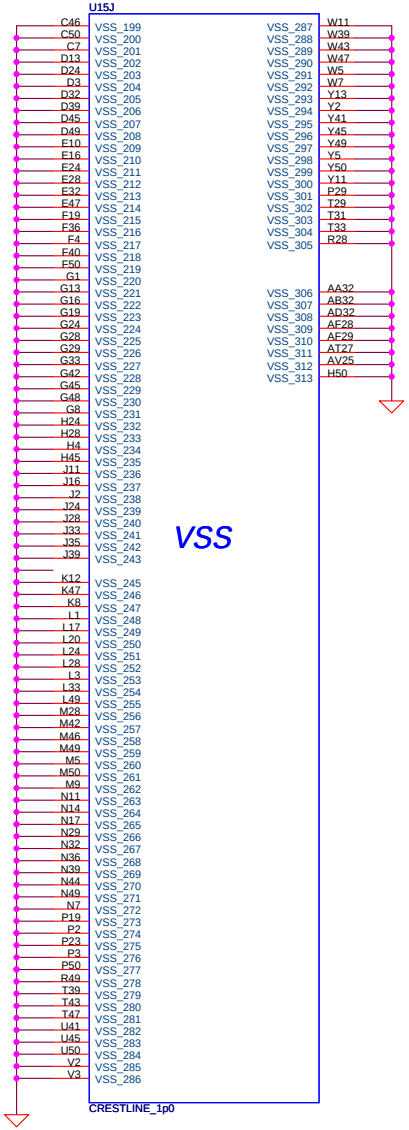

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Title: **CRESTLINE((6/6)-PWR/GND**

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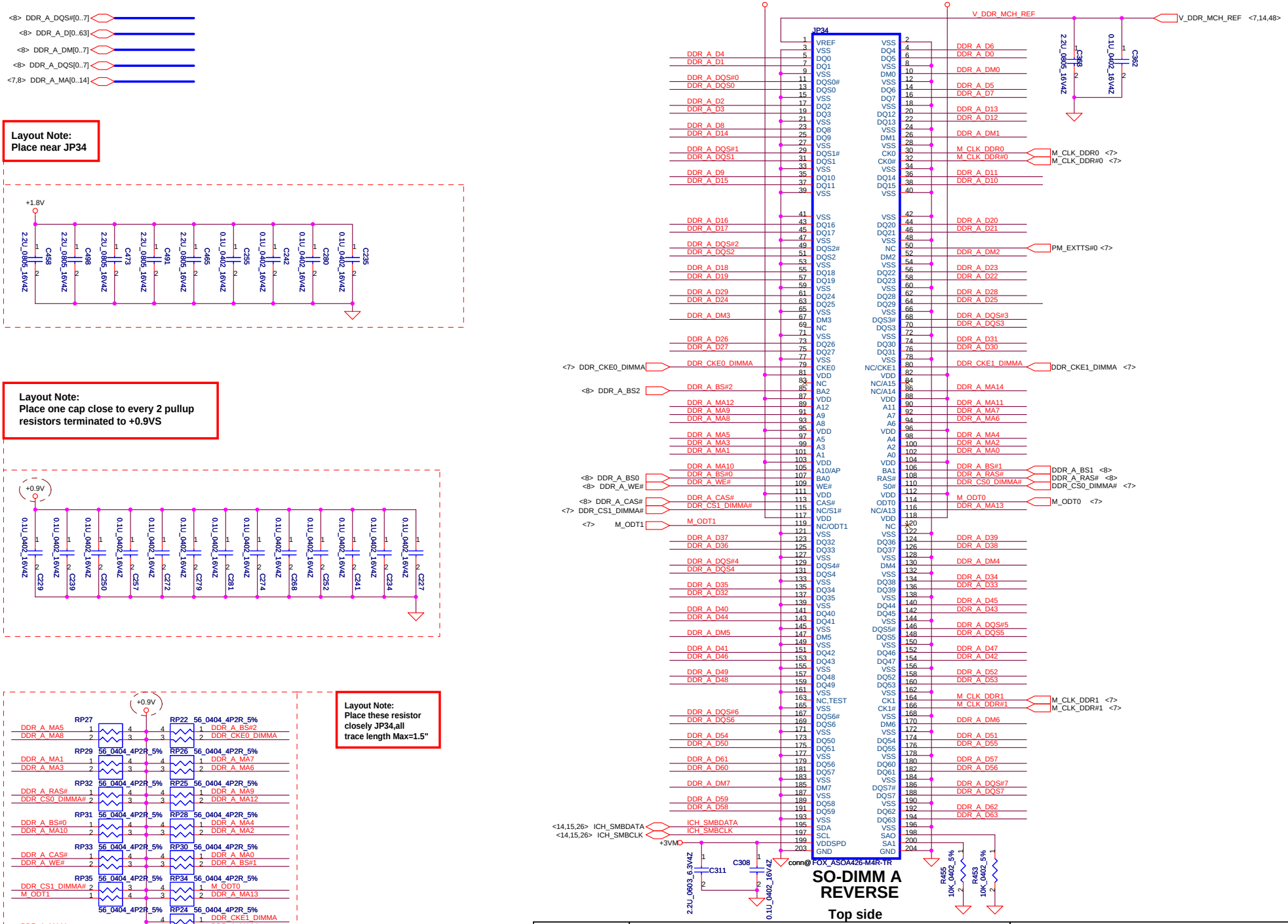

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Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT1**

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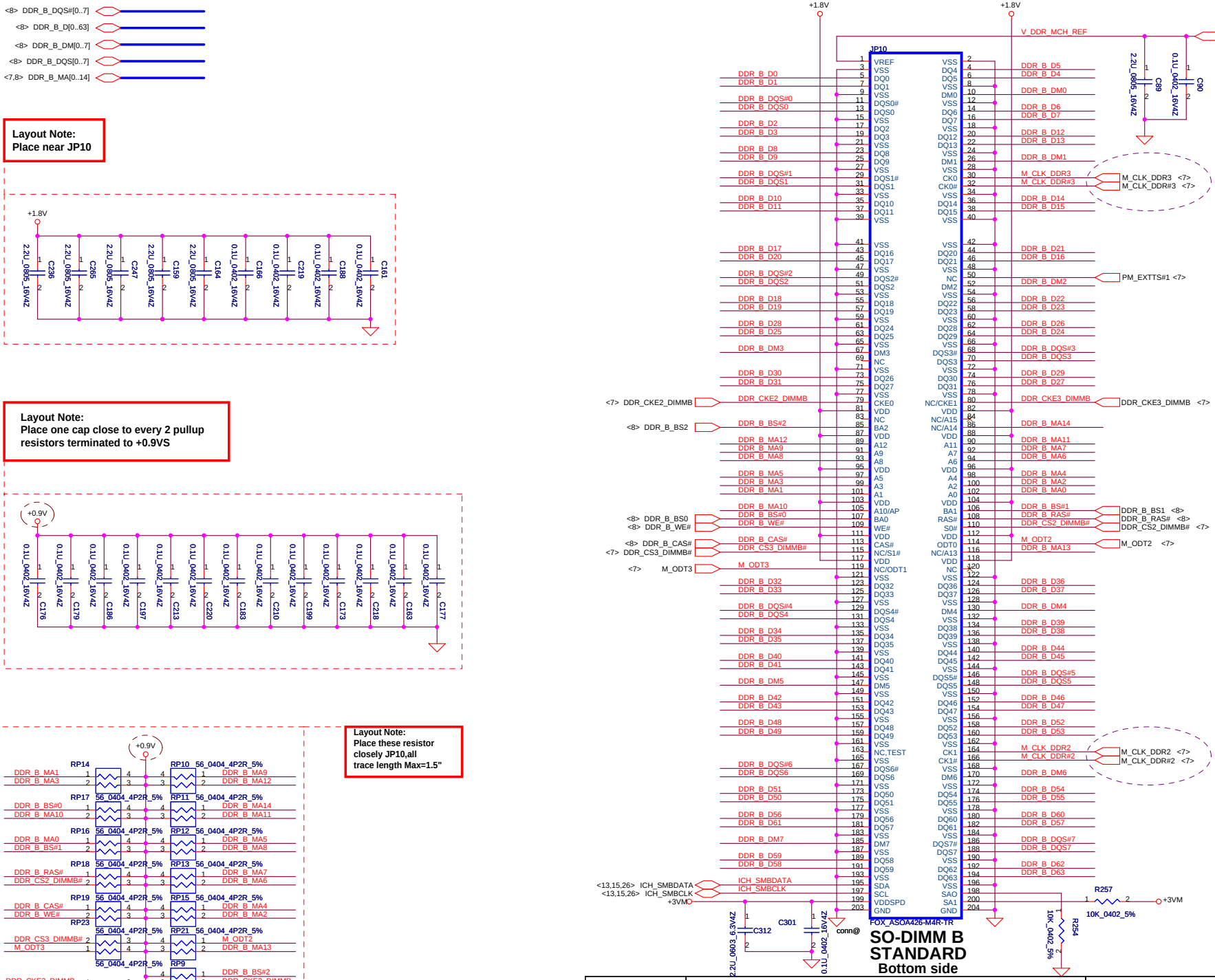

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Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

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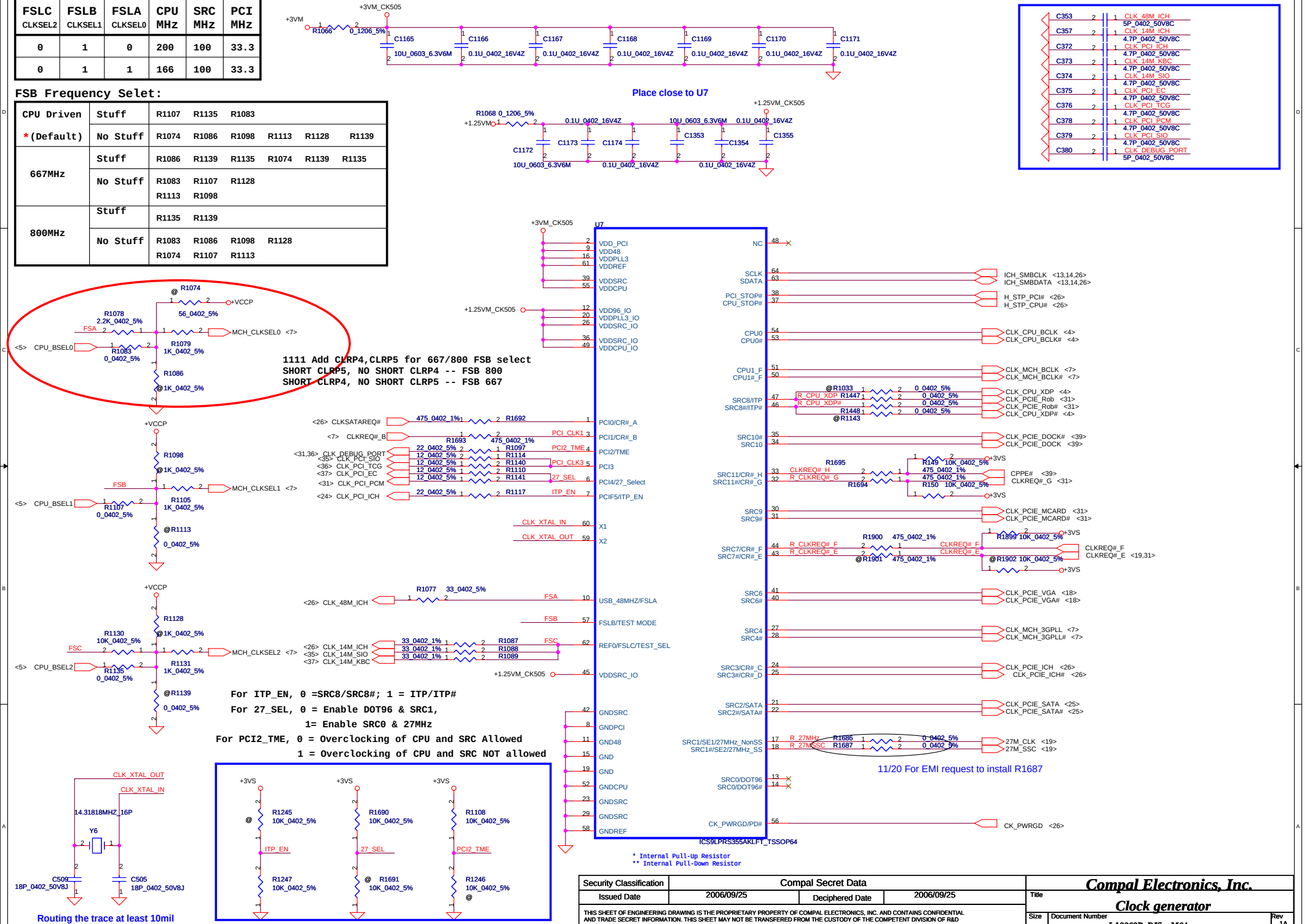
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Compal Electronics, Inc.

Title: **Clock generator**

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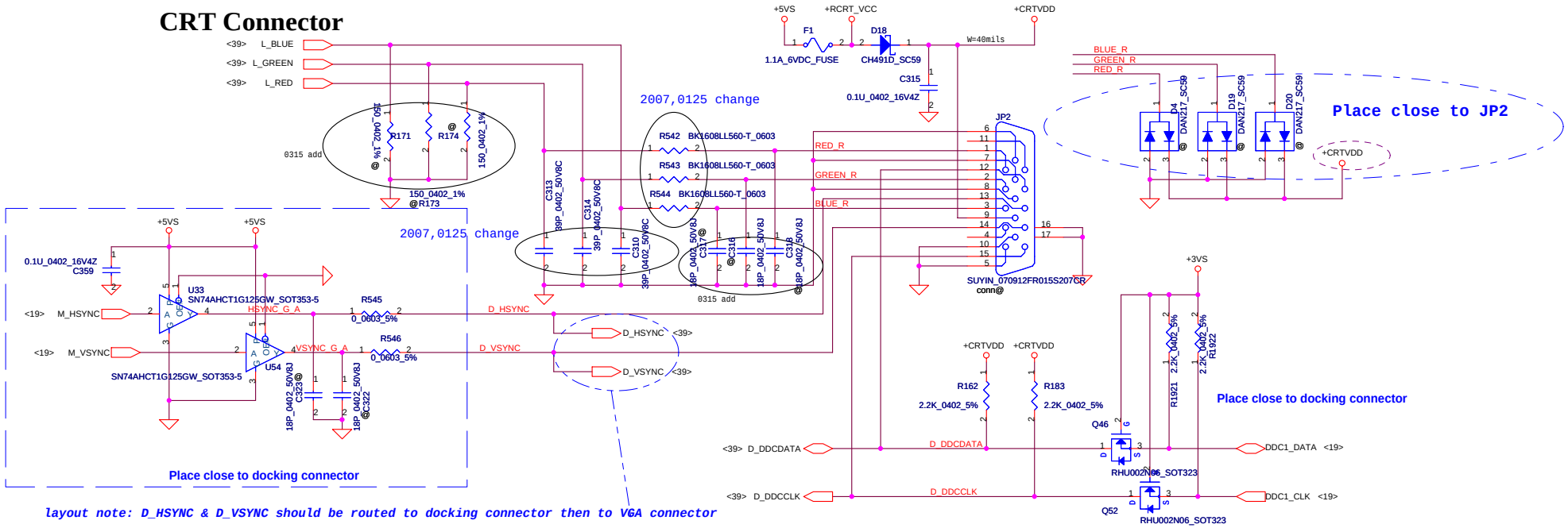
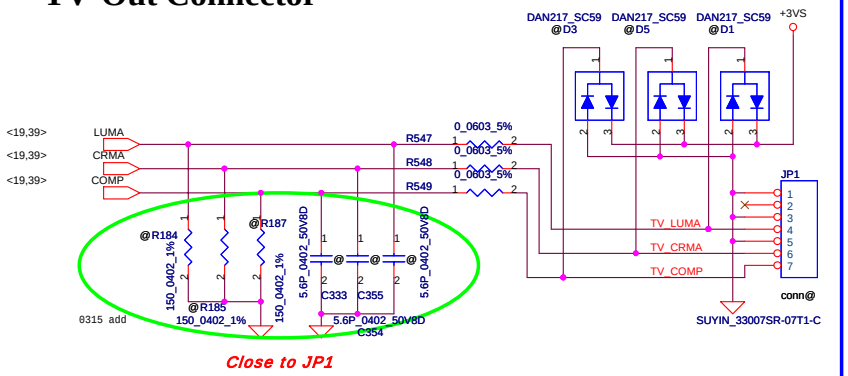
CRT Connector



layout note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector

TV-Out Connector



Close to JP1

layout note: TV-out signals should be routed to JP30 then to JP1

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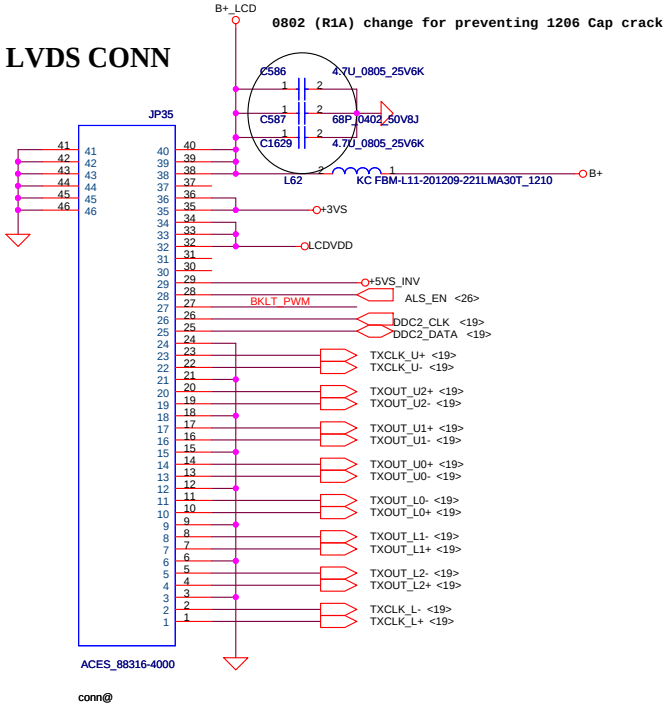
Compal Electronics, Inc.

Title: **CRT & TVout Connector**

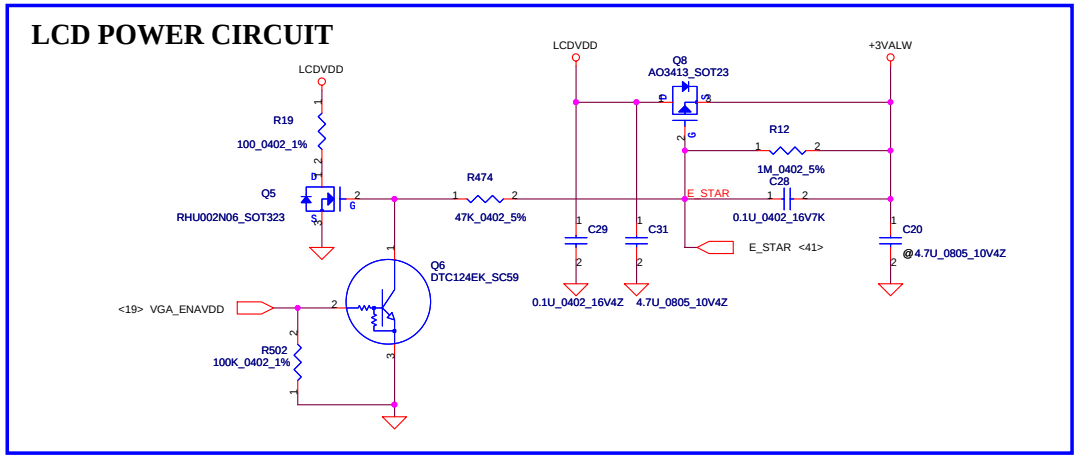
Size | Document Number: *LA3262P_DIS__M64* | Rev: 1A

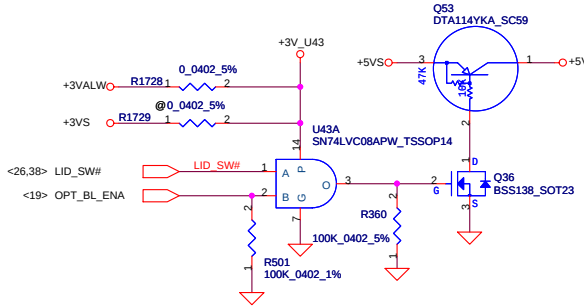
Date: Tuesday, August 21, 2007 | Sheet 16 of 57

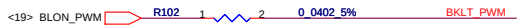
LVDS CONN



LCD POWER CIRCUIT







Support 3V inverter

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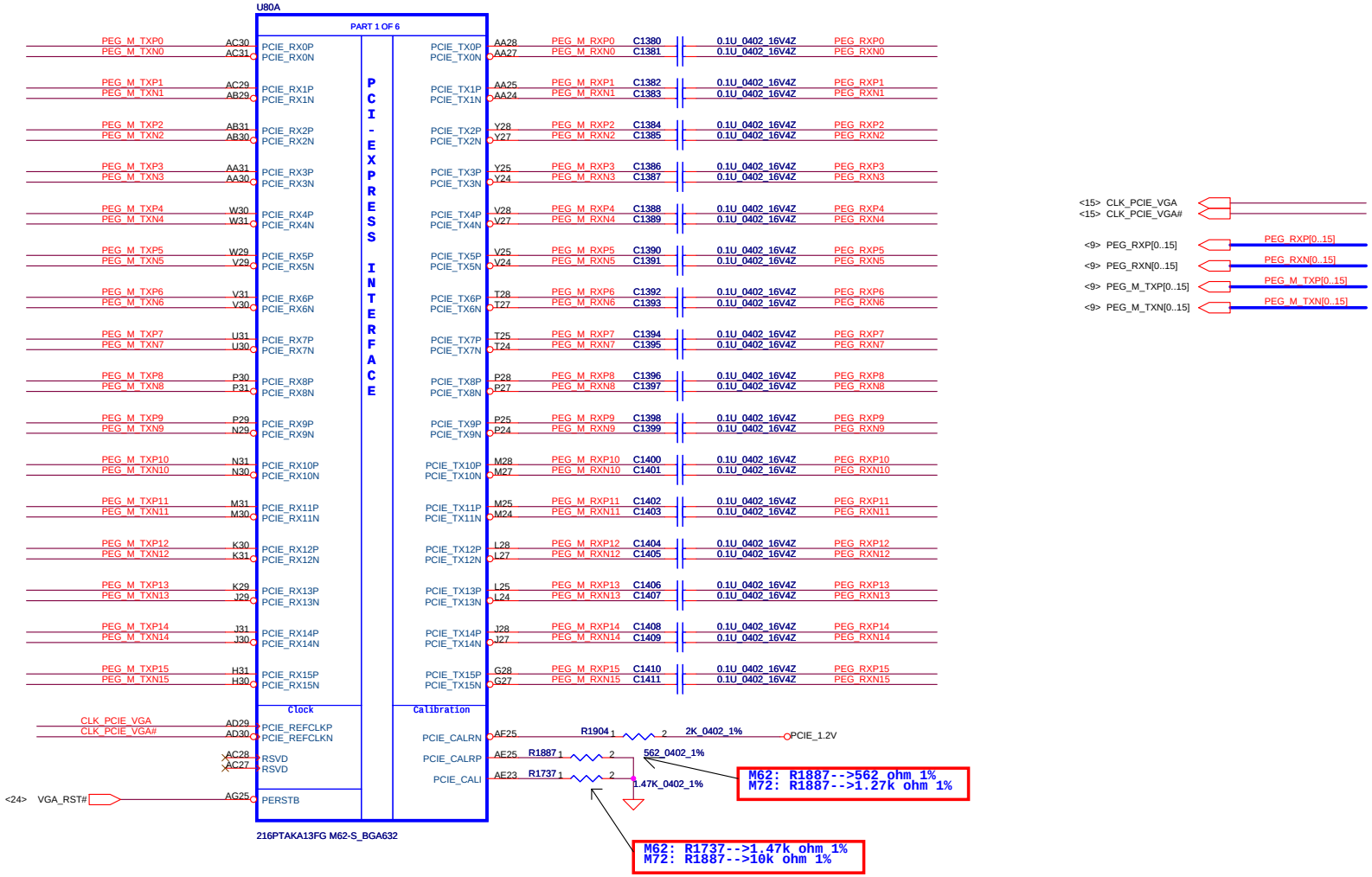
Compal Electronics, Inc.

Title: **LCD CONN.**

Size: | Document Number: *LA3262P_DIS__M64* | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 17 of 57



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Compal Electronics, Inc.

Title: **M62-S PCIE interface**

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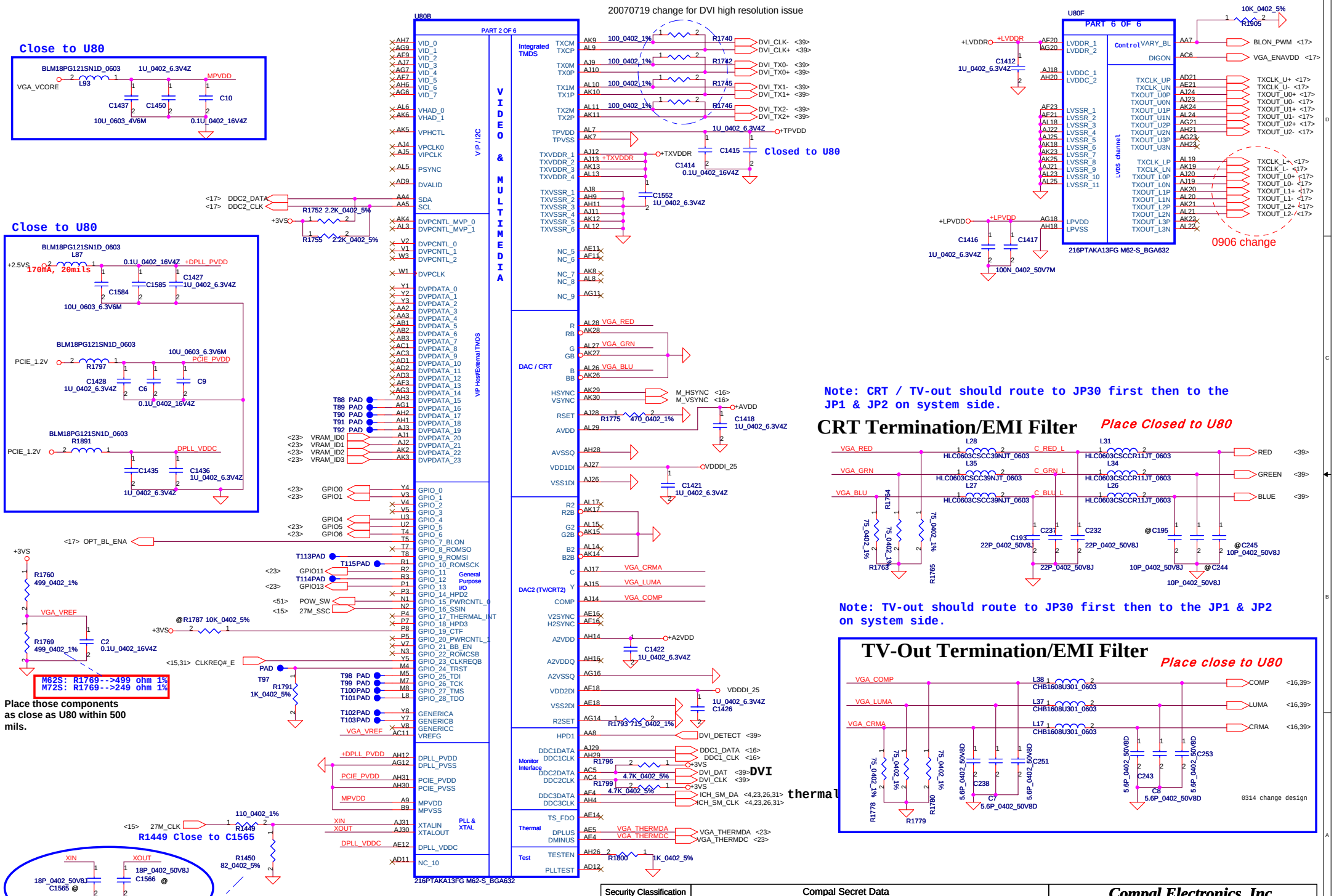
Date: Tuesday, August 21, 2007 | Sheet 18 of 57



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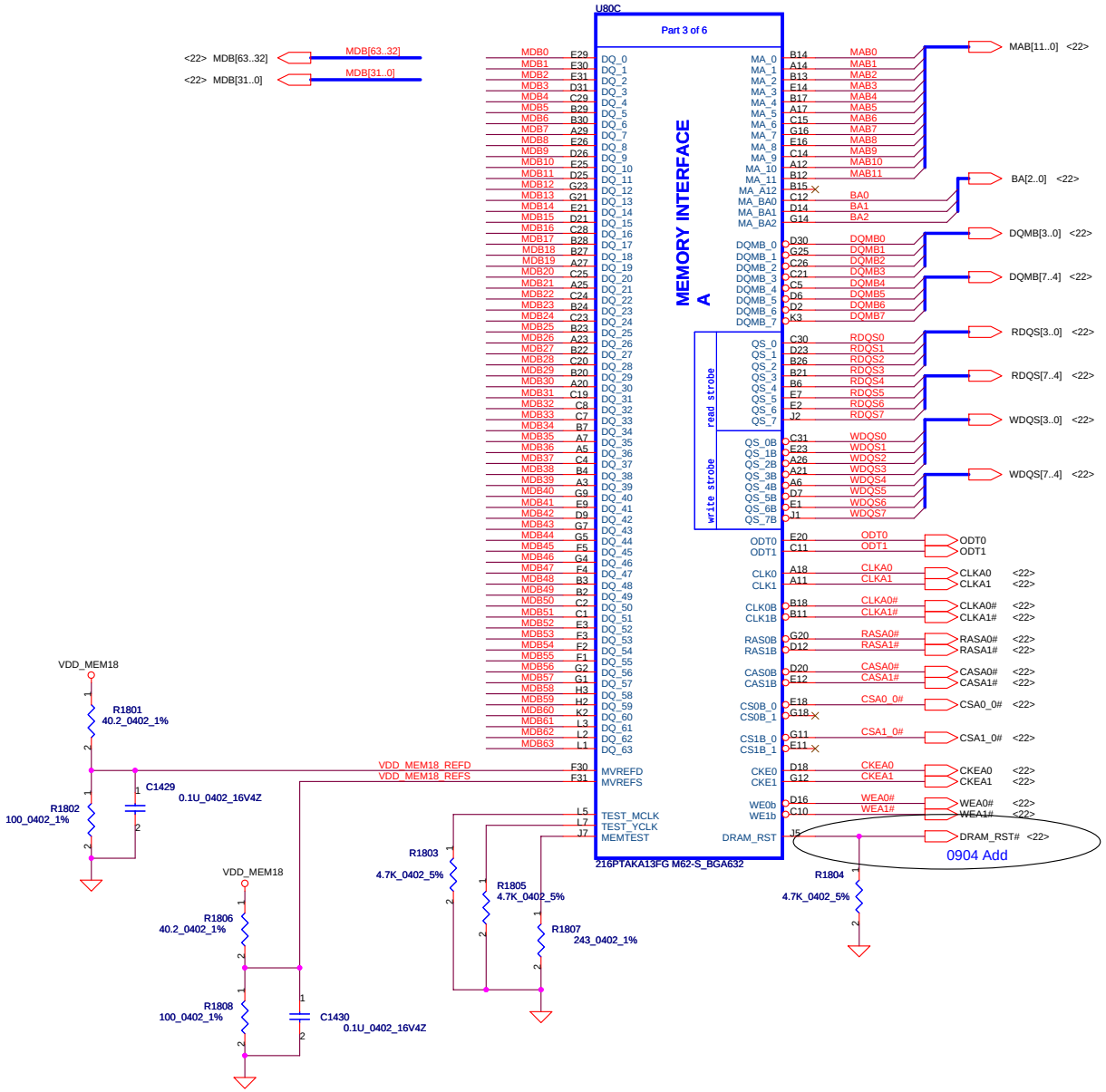
Compal Electronics, Inc.

Title: **M62-S CRT/LVDS/TV-OUT**

Size: | Document Number: *LA3262P_DIS_M64* | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 19 of 57



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Compal Electronics, Inc.

Title: **M62-S MEM**

Size | Document Number: *LA3262P_DIS__M64* | Rev: 1A

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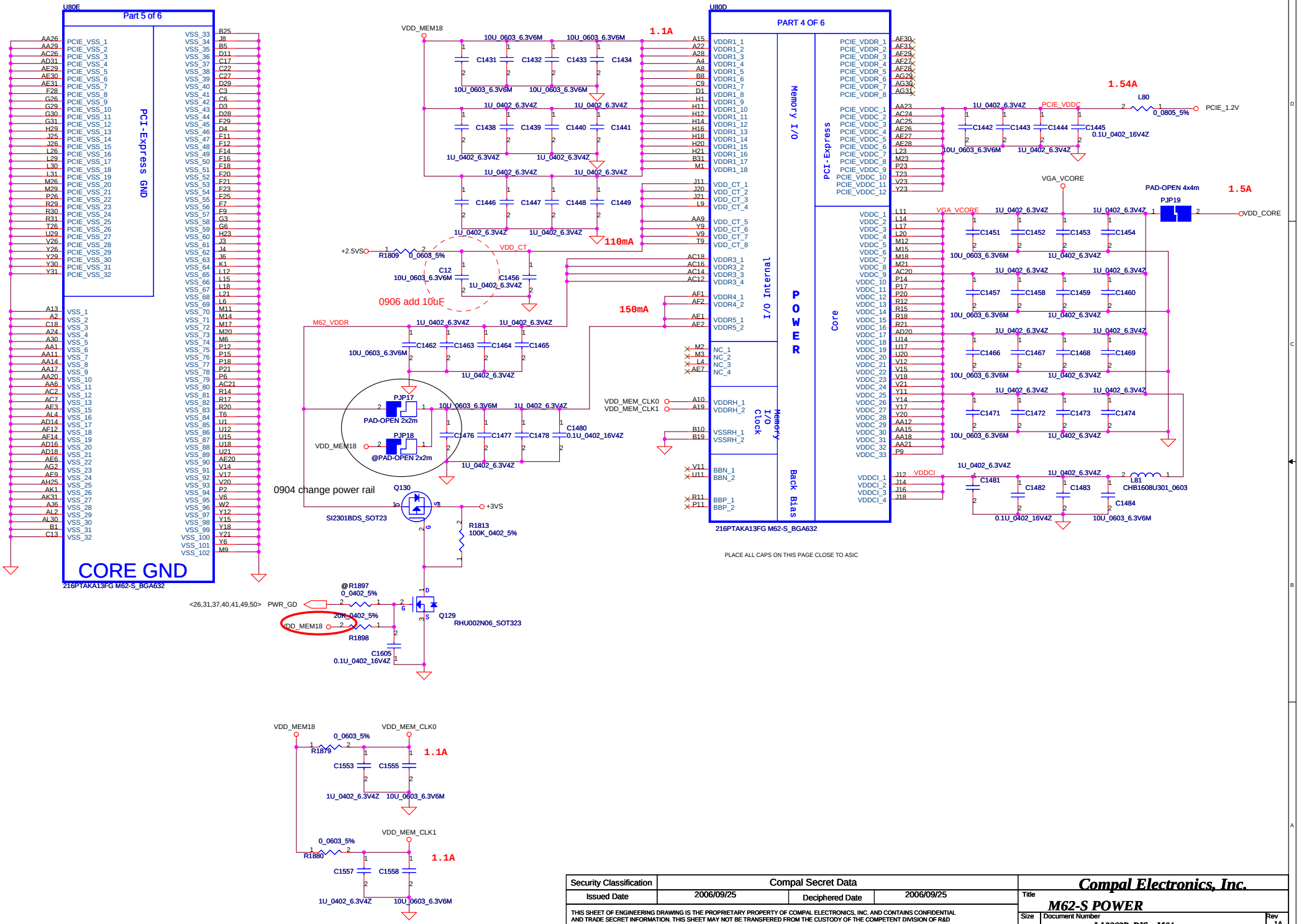

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Compal Electronics, Inc.

Title: **M62-S POWER**

Size | Document Number: LA3262P_DIS__M64 | Rev: 1A

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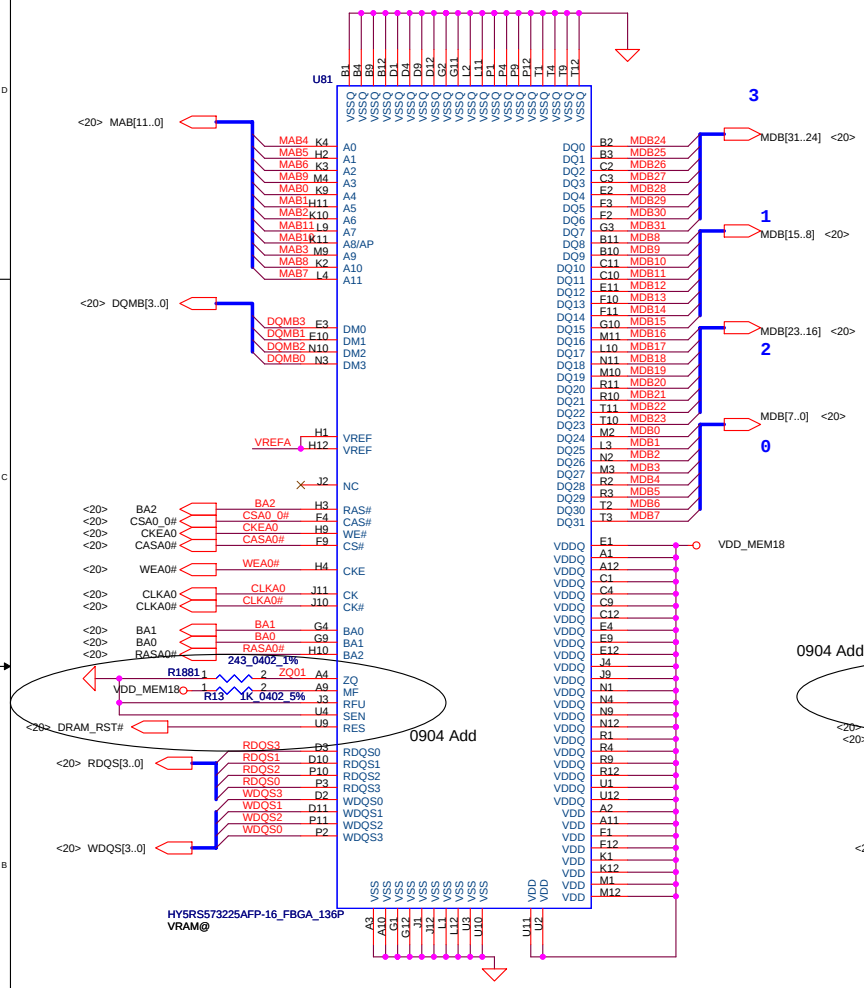
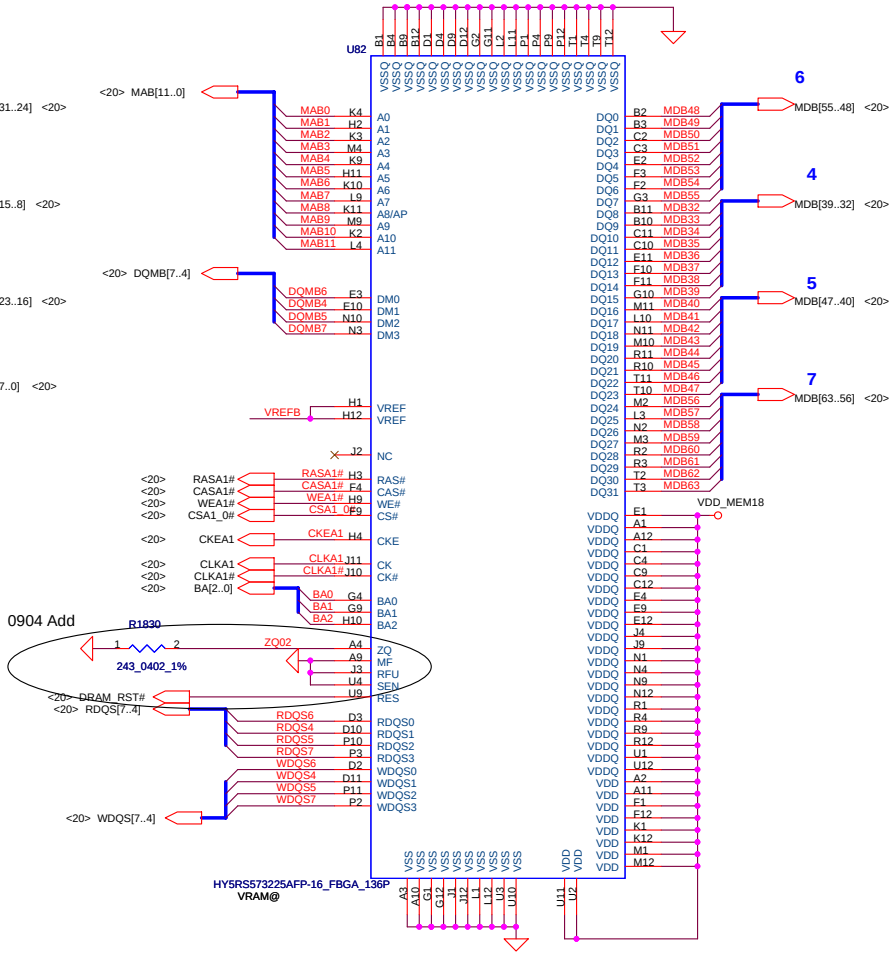
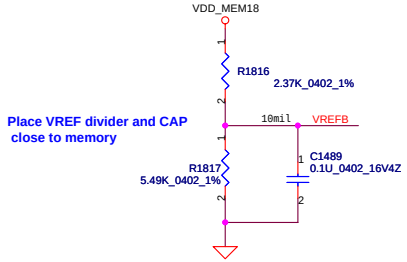
DDR3 VRAM: 8Mx32/16Mx32 FBGA_136P 2 pcs

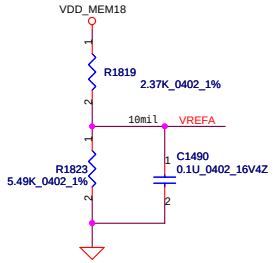


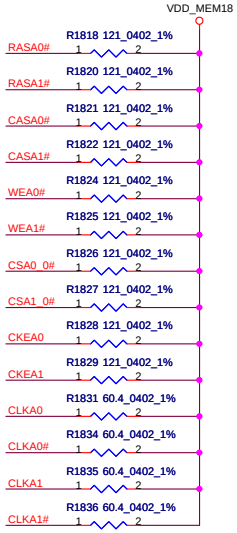




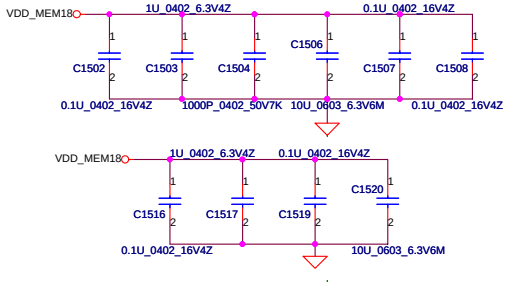
Place VREF divider and CAP close to memory

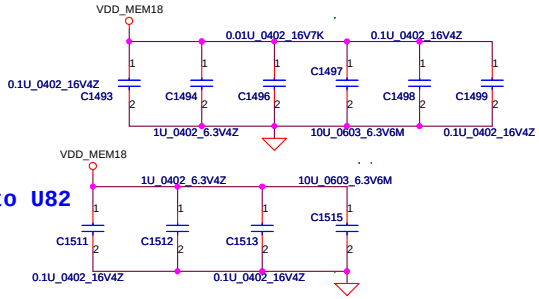
Place VREF divider and CAP close to memory





Place close to U81





Place close to U82

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Compal Electronics, Inc.

Title: **M62-S VRAM**

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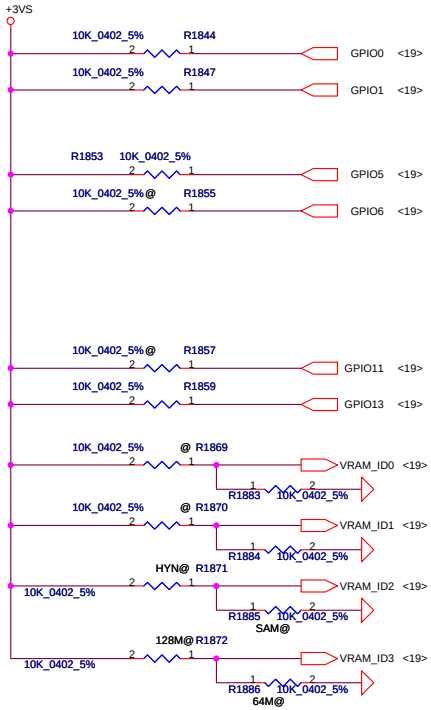
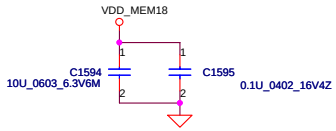


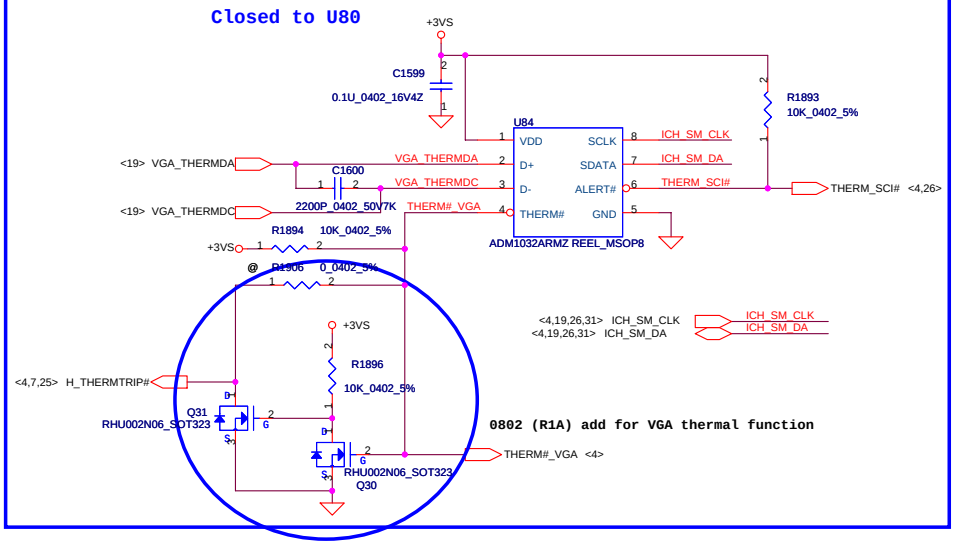
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
TX_PWRS_ENB	GPIO0	FULL SWING internal pull down	1
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable internal pull down	1
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible internal pull down	0
PLL_IBIAS_RD	GPIO[6:5]	Bias Currentfor the PCIE PHY PLL	GPIO6-->0 GPIO5-->1
ROMIDCFG[3:0] internal pull down	GPIO [9,13,12,11]		
		No ROM , with 128M frame buffer	0 0 0 X
		No ROM , with 64M frame buffer	0 1 0 X
VRAM_ID[0:3]	DVPDATA (20,21,22,23)		VRAM_ID 0, 1, 2, 3
		Samsung 8Mx32 1.8V	0 0 0 0
		Samsung 16Mx32 1.8V	0 0 0 1
		Hynix 8Mx32 1.8V	0 0 1 0
		Hynix 16Mx32 1.8V	0 0 1 1

Closed to U80

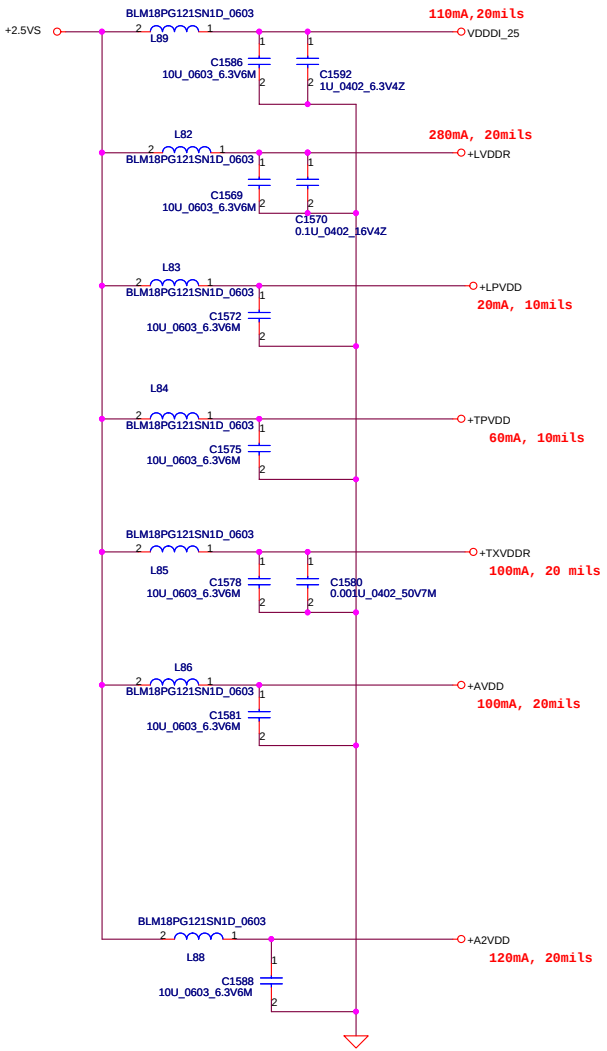


VGA Thermal Sensor ADM1032ARMZ

Closed to U80



Closed to U80



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Compal Electronics, Inc.

Title: **M62-S Filters / Strap**

Size | Document Number: LA3262P_DIS__M64 | Rev 1A

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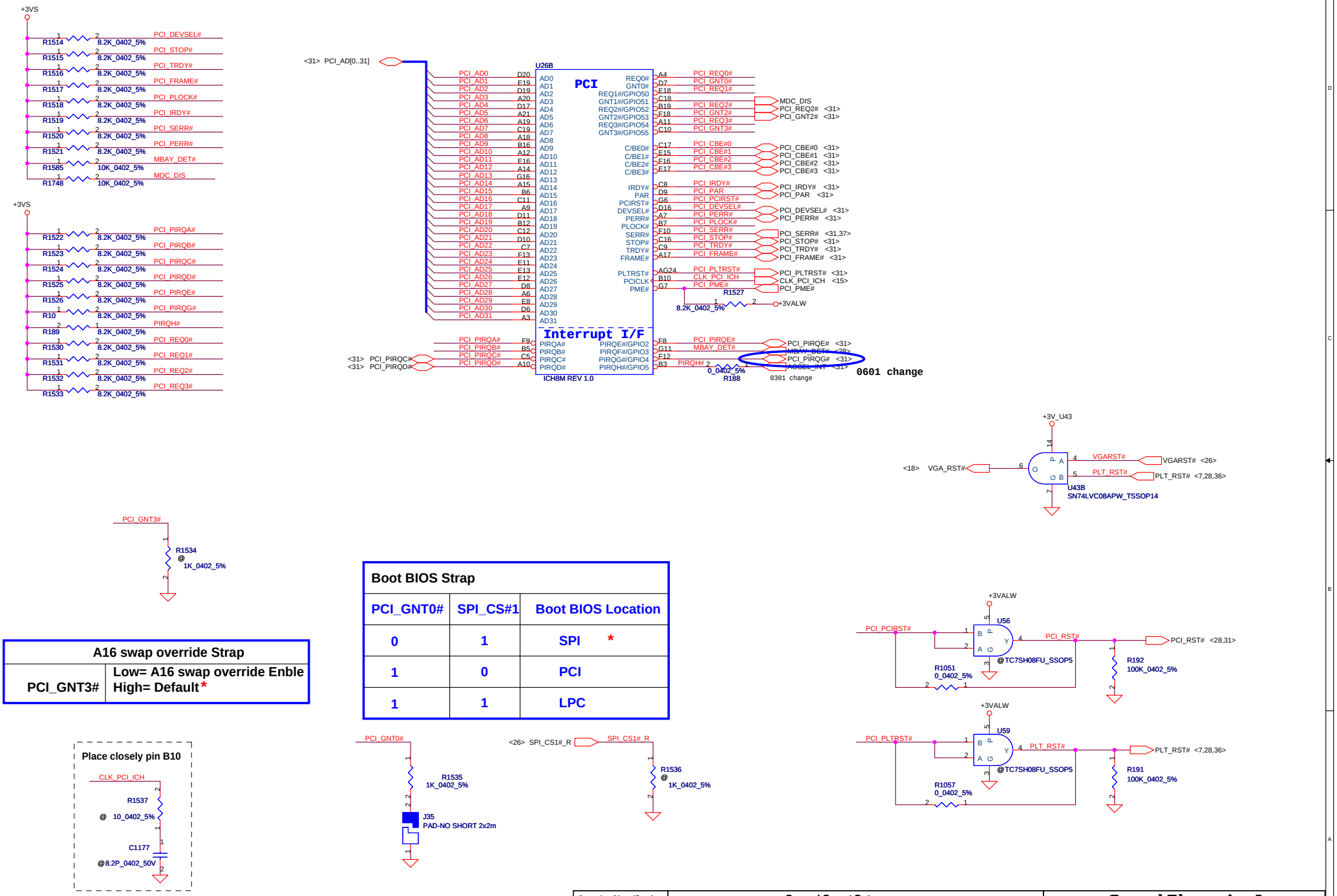

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default*

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Compal Electronics, Inc.

Title: ICH8(1/4)-PCI/INT

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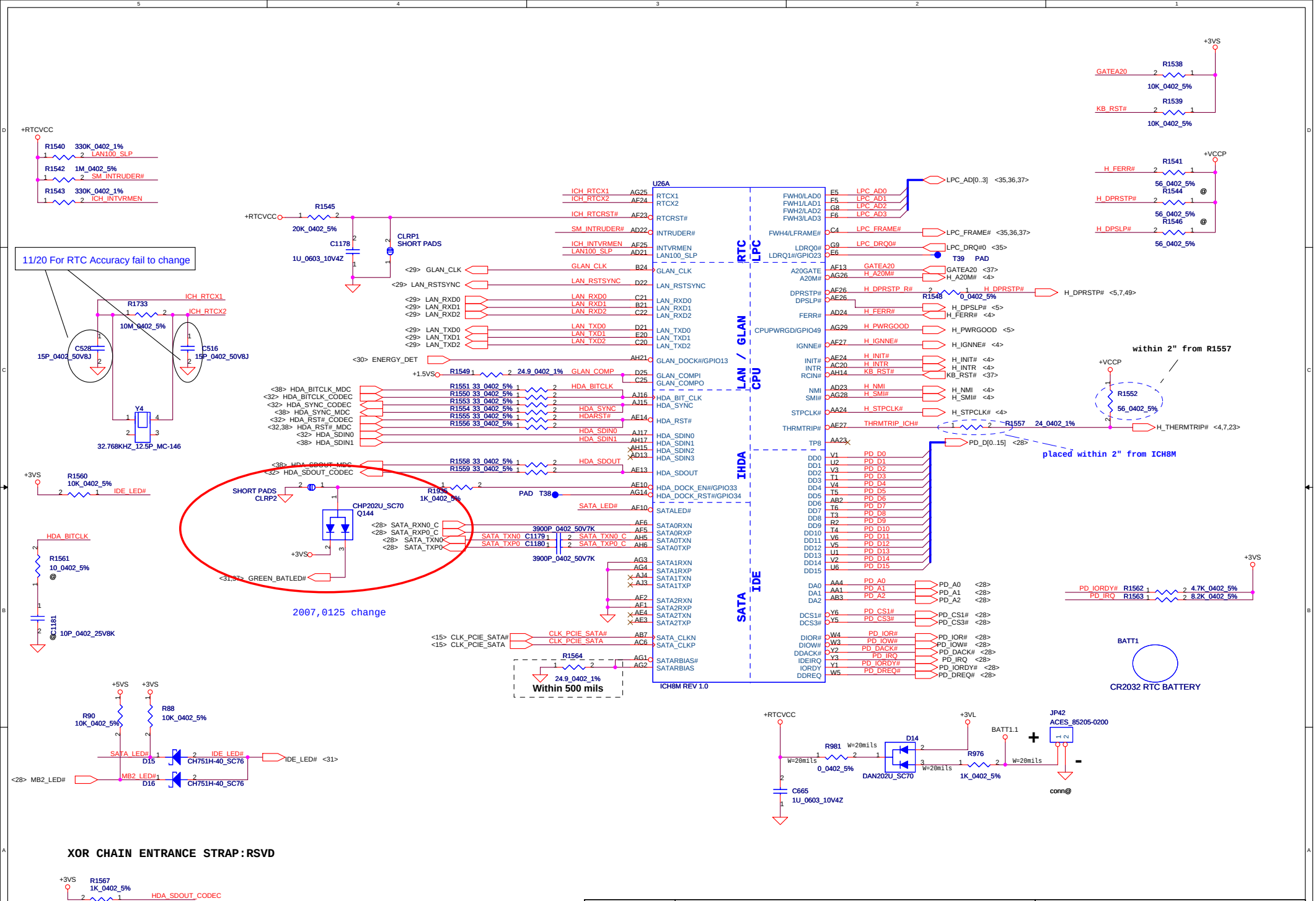

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Compal Electronics, Inc.

Title: **ICH8(2/4)_LAN,HD,IDE,LPC**

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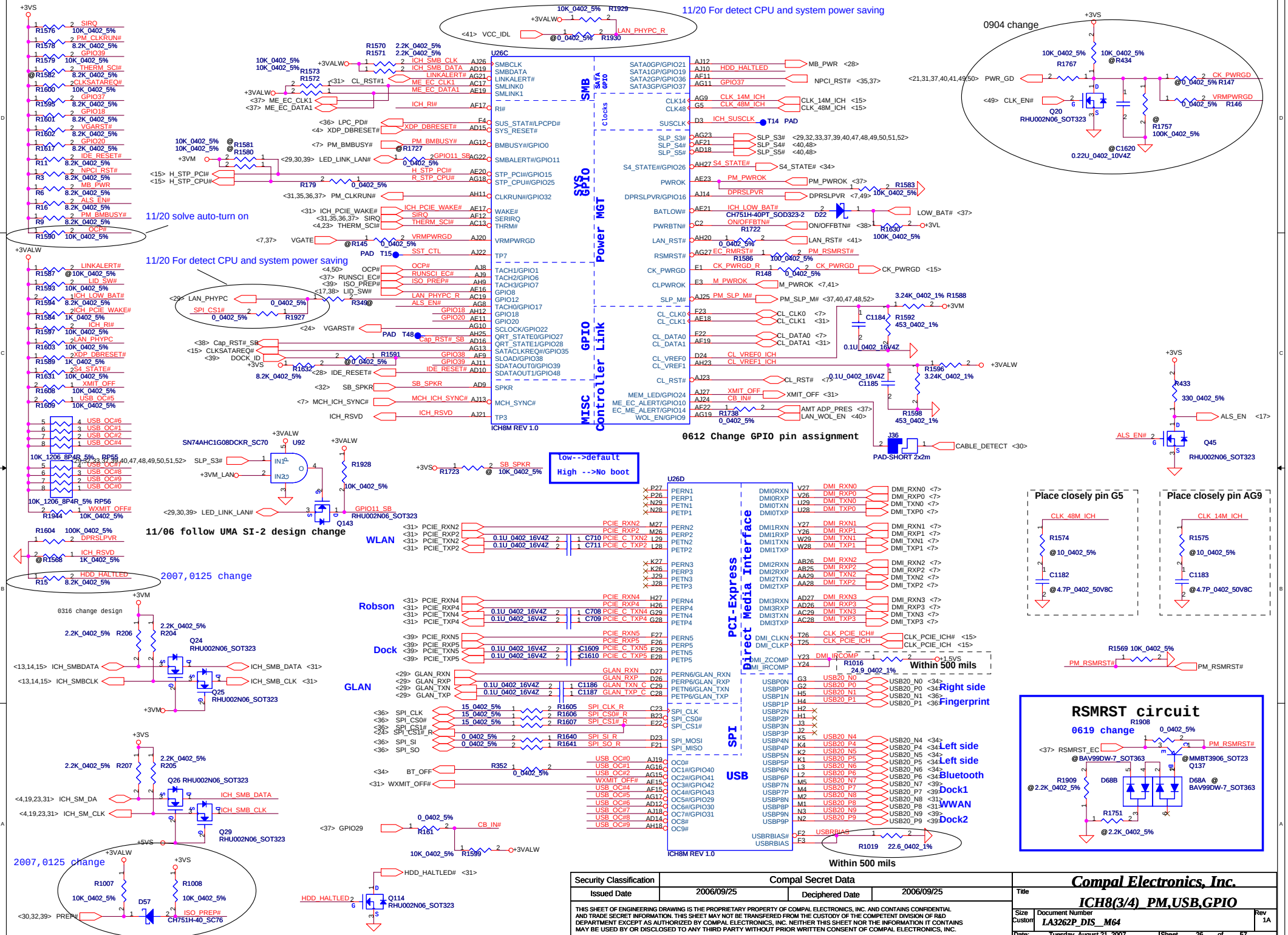
11/20 For detect CPU and system power saving
0904 change
11/20 solve auto-turn on
11/20 For detect CPU and system power saving
0612 Change GPIO pin assignment
11/06 follow UMA SI-2 design change
2007,0125 change
0316 change design
2007,0125 change
low-->default
High -->No boot
Place closely pin G5
Place closely pin AG9
RSMRST circuit
0619 change
Within 500 mils
Right side
Fingerprint
Left side
Left side
Bluetooth
Dock1
WWAN
Dock2
Within 500 mils
U26C
ICH8M REV 1.0
U26D
ICH8M REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
GPIO Controller Link
MISC
PCI-Express Direct Media Interface
SPI
USB
WLAN
Robson
Dock
GLAN
PAD-SHORT 2x2m
SN74AHC1G08DCKR_SC70
Compal Electronics, Inc.
ICH8(3/4)_PM,USB,GPIO
LA3262P_DIS__M64
Tuesday, August 21, 2007
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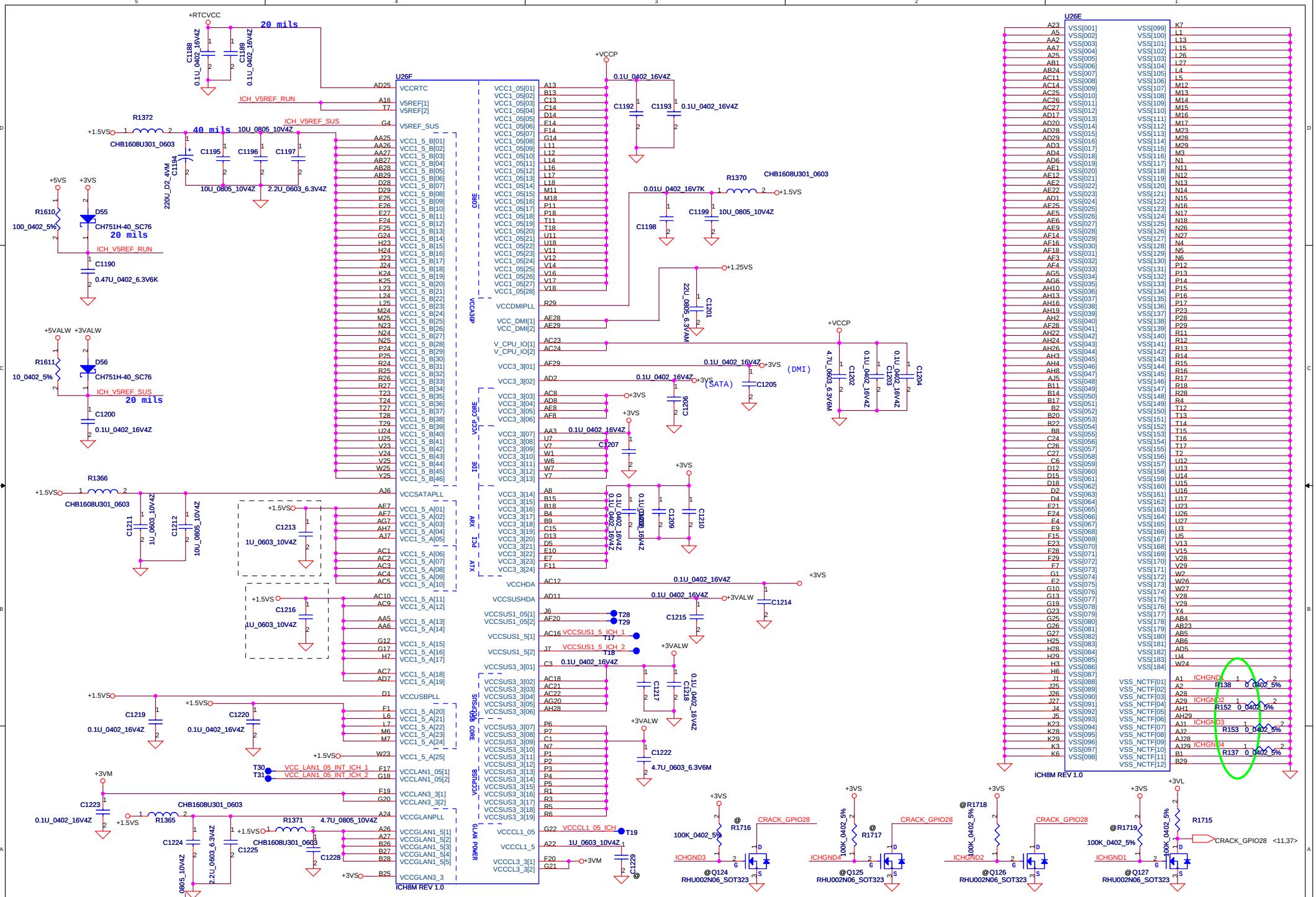

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Compal Electronics, Inc.

Title: **ICH8(4/4)_POWER&GND**

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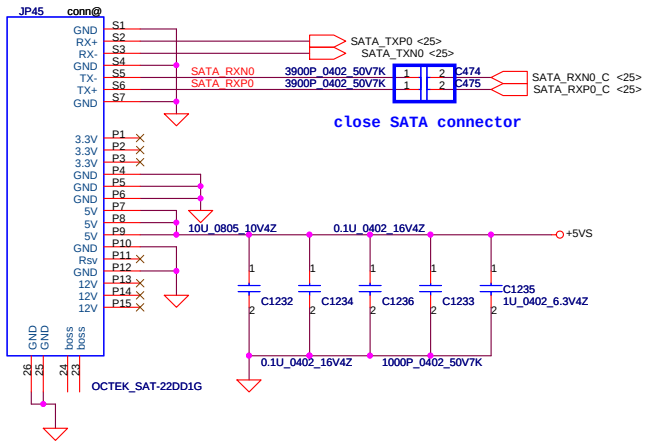
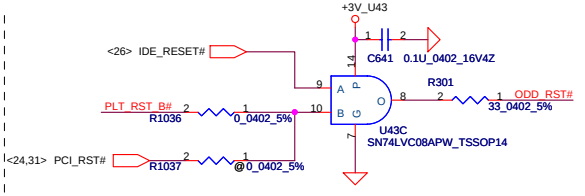
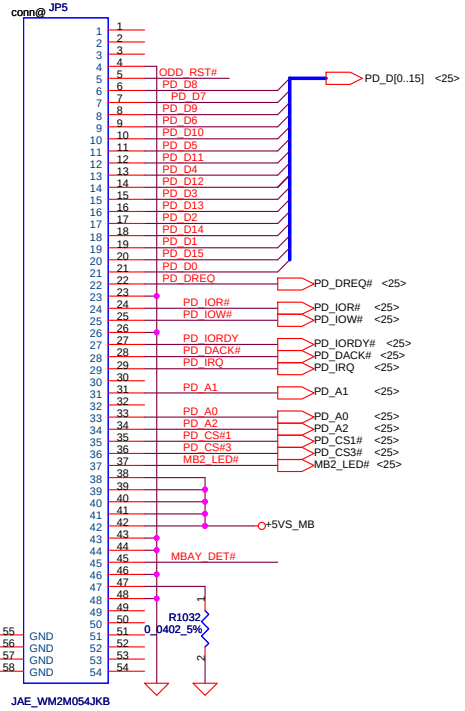
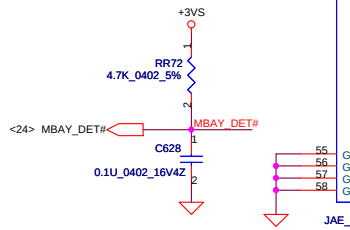
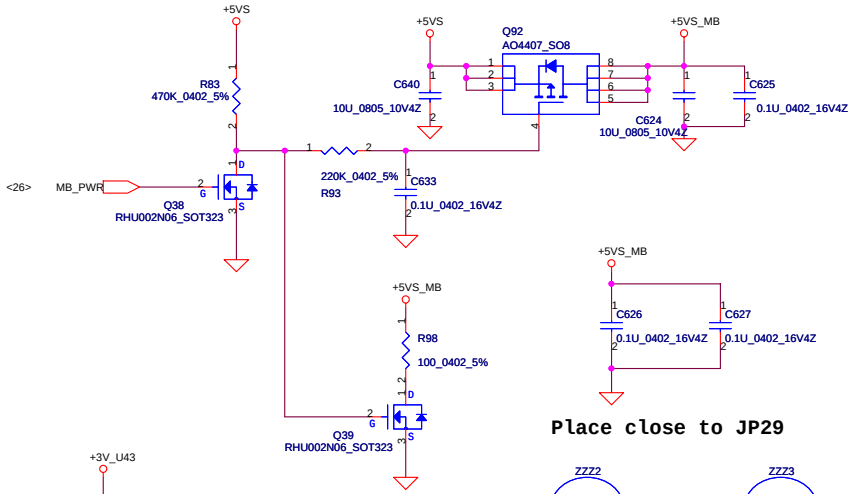
Multi Bay II connector

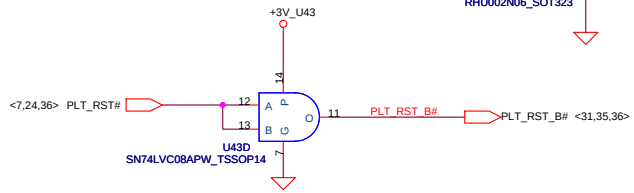












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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Compal Electronics, Inc.

Title: **HDD & CDROM**

Size	Document Number	Rev
Custom	LA3262P_DIS_M64	1A

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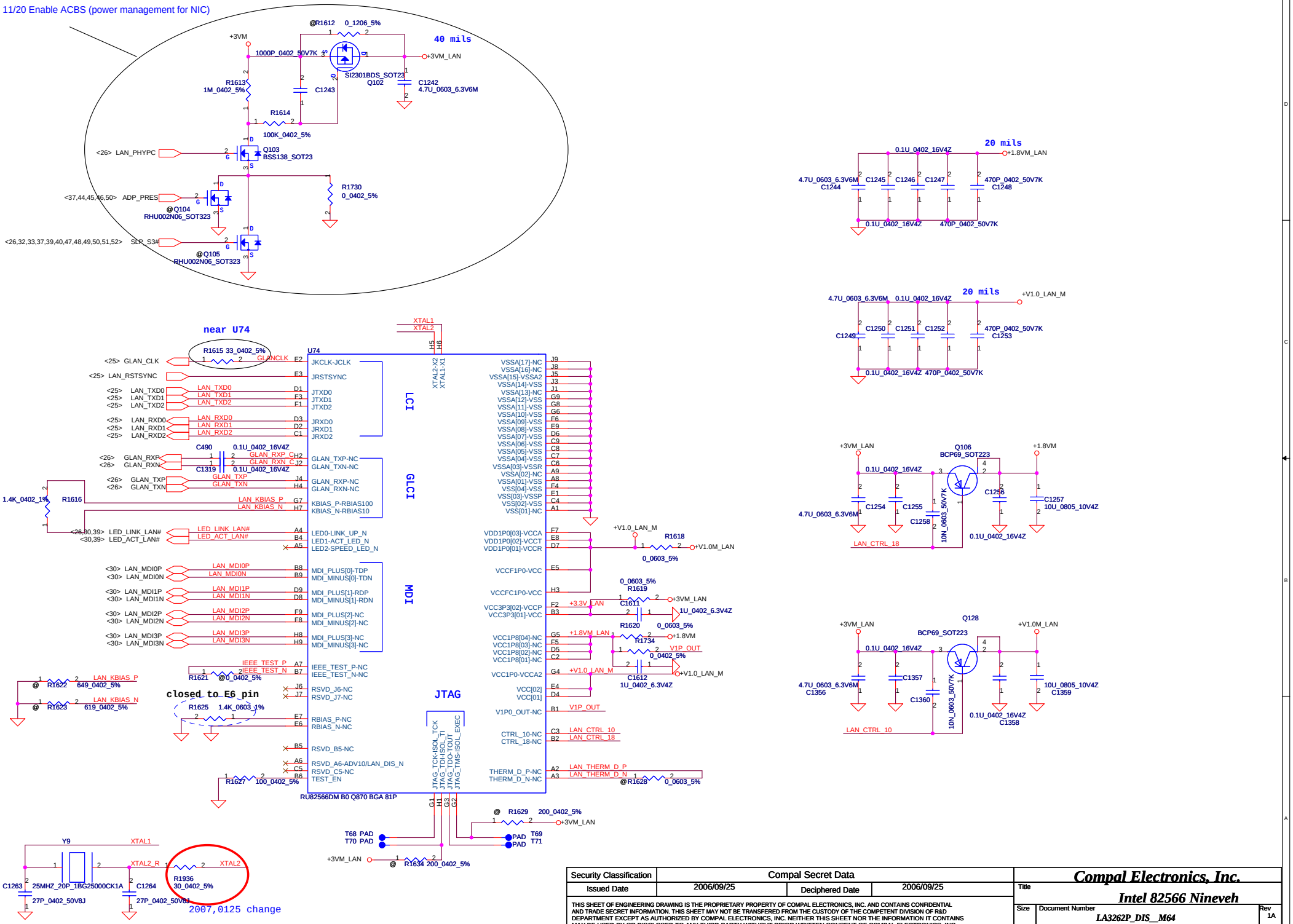
11/20 Enable ACBS (power management for NIC)



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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Compal Electronics, Inc.

Title: **Intel 82566 Nineveh**

Size	Document Number	Rev
	LA3262P_DIS__M64	1A

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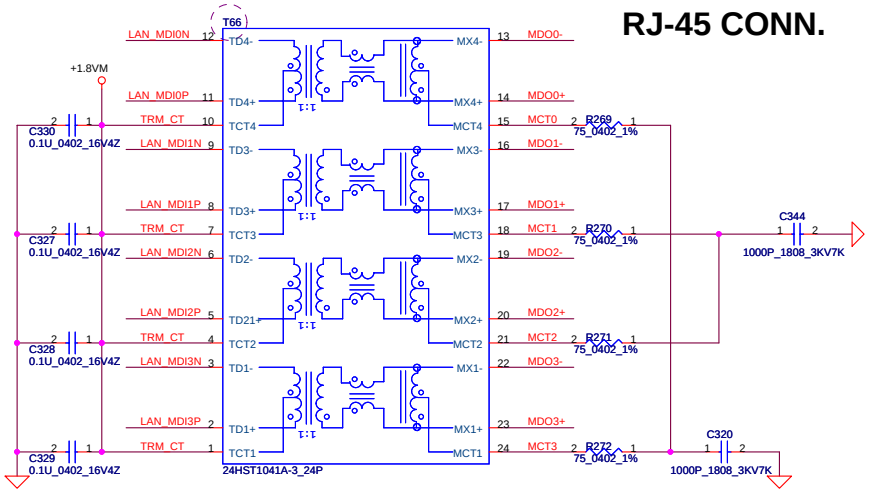
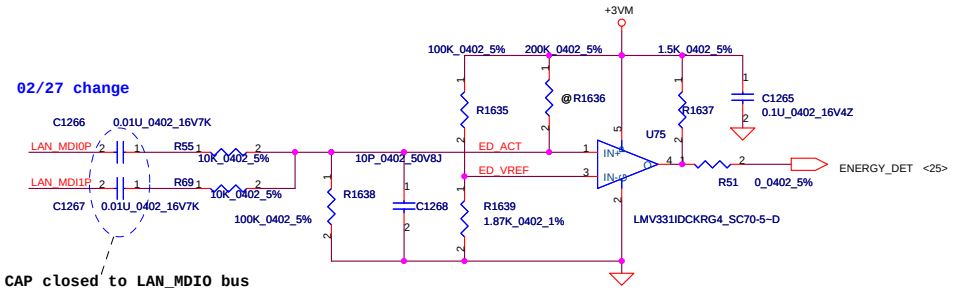
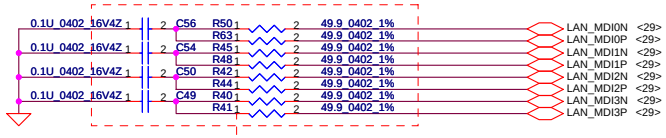
RJ-45 CONN.

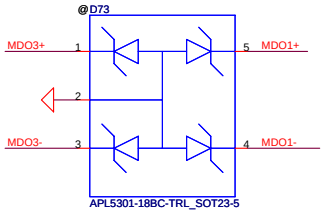


LAN ENERGY DET

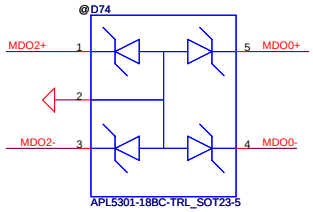


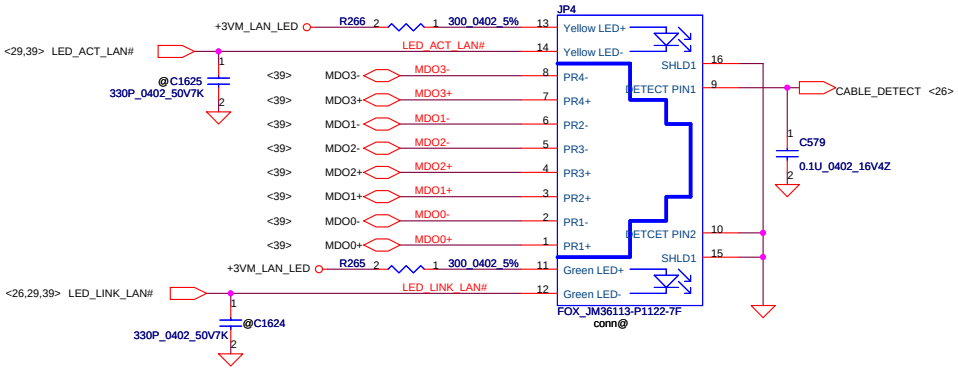


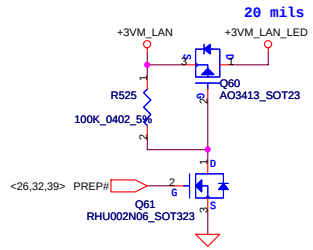
Layout Notice : Place termination as close as Intel 82566 as possible



Note: MDO[3..0]+/- signals should route to JP4 first then to JP30.







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Compal Electronics, Inc.

Title: **Magnetic & RJ45/RJ11**

Size | Document Number: LA3262P_DIS__M64 | Rev: 1A

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B/B connector with PCI / LED / FIR / SC interface

0915 Change 1394 signals

JP13 — ACES_88394-1A71

0622 change to support AMT

0731 Install R1383 and no install R1382, do not support wake on WWAN card

0811 Isolate SLOT power from SYSTEM power.

Mini-Express Card---WLAN

0824 Add +1.5VS_WLAN

0811 Isolate SLOT power from SYSTEM power.

0821 Install R1364

0906 Remove debug resistors

0906 Remove debug resistors

0612 change power plane

0627 Add 0 ohm on PIN 42,46

0821 Change +3VS to +3VS_WLAN

0627 PIN37,43 connected to GND
PIN39,41 connected to +3VS

0811 No install R1418,R1358,R1359,R1360

0906 Remove debug resistors

JP44 — MOLEX 67910-0002 52P

0811 HP request

Mini-Express Card--WWAN

JP46 — MOLEX 67910-0002 52P

U72 — S DIO(BR) NUP4301MR6T1 TSOP-6

JP50 — TAITW_PMPAT6-06GLBS7N14N0

0821 Change +3VS to +3VS_WWAN

0811 Pins 37 and 43 connect to GND and remove +1.5VS

0821 Delete SW1,C986,R521,D65,R200

2007,0125 change

0811 Reserve for SIM card does not meet rise time and a pull-up resistor is needed.

ACCELEROMETER

0313 change design

U64 — LIS3LV02DL-TR_LGA16

0619 Follow ST Demo circuit

0619 Follow ST Demo circuit

Must be placed in the center of the system.

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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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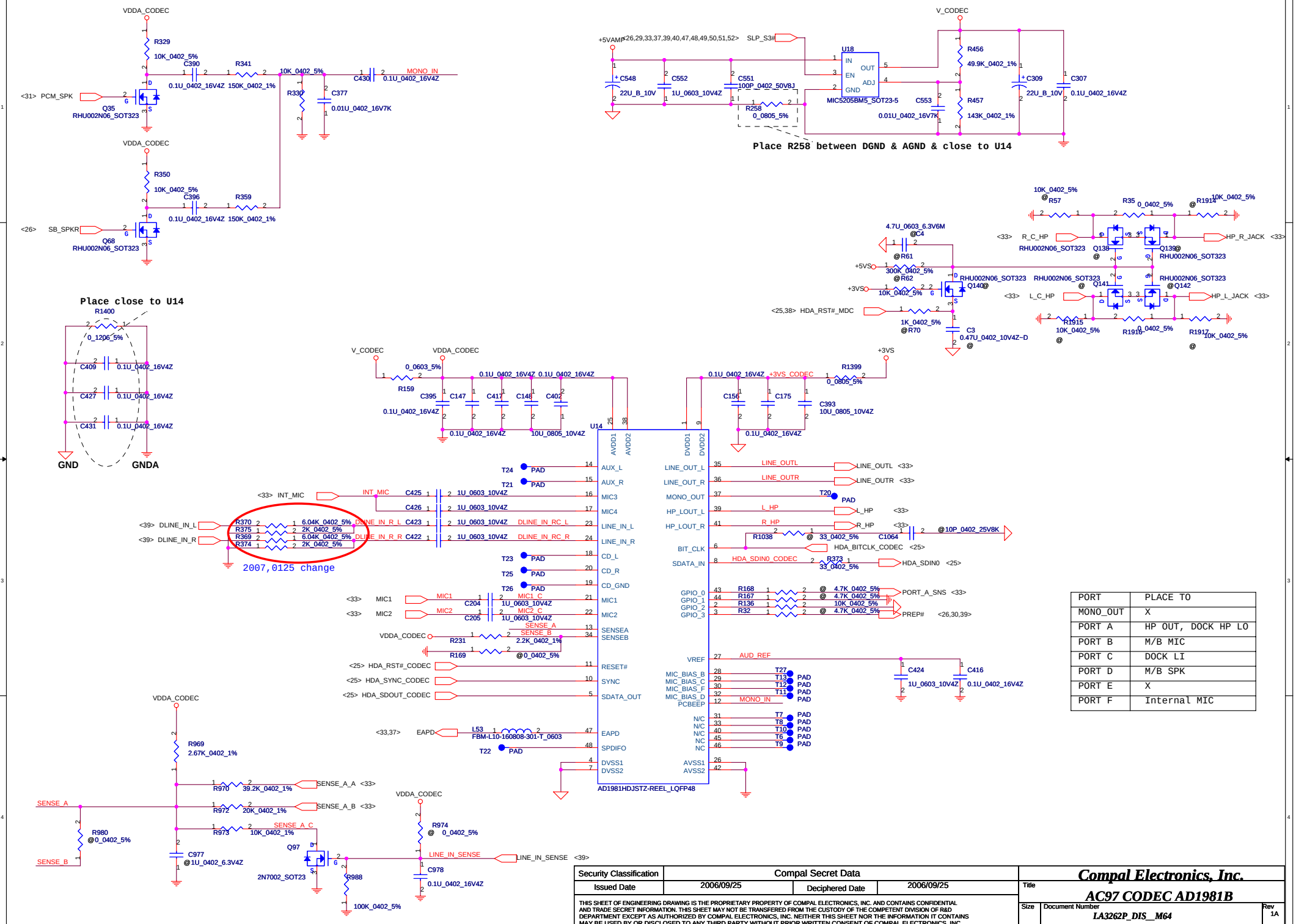
Compal Electronics, Inc.

Title: Mini-Card/Mini-PCI/Accelerometer

Size: | Document Number: LA3262P_DIS__M64 | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 31 of 57



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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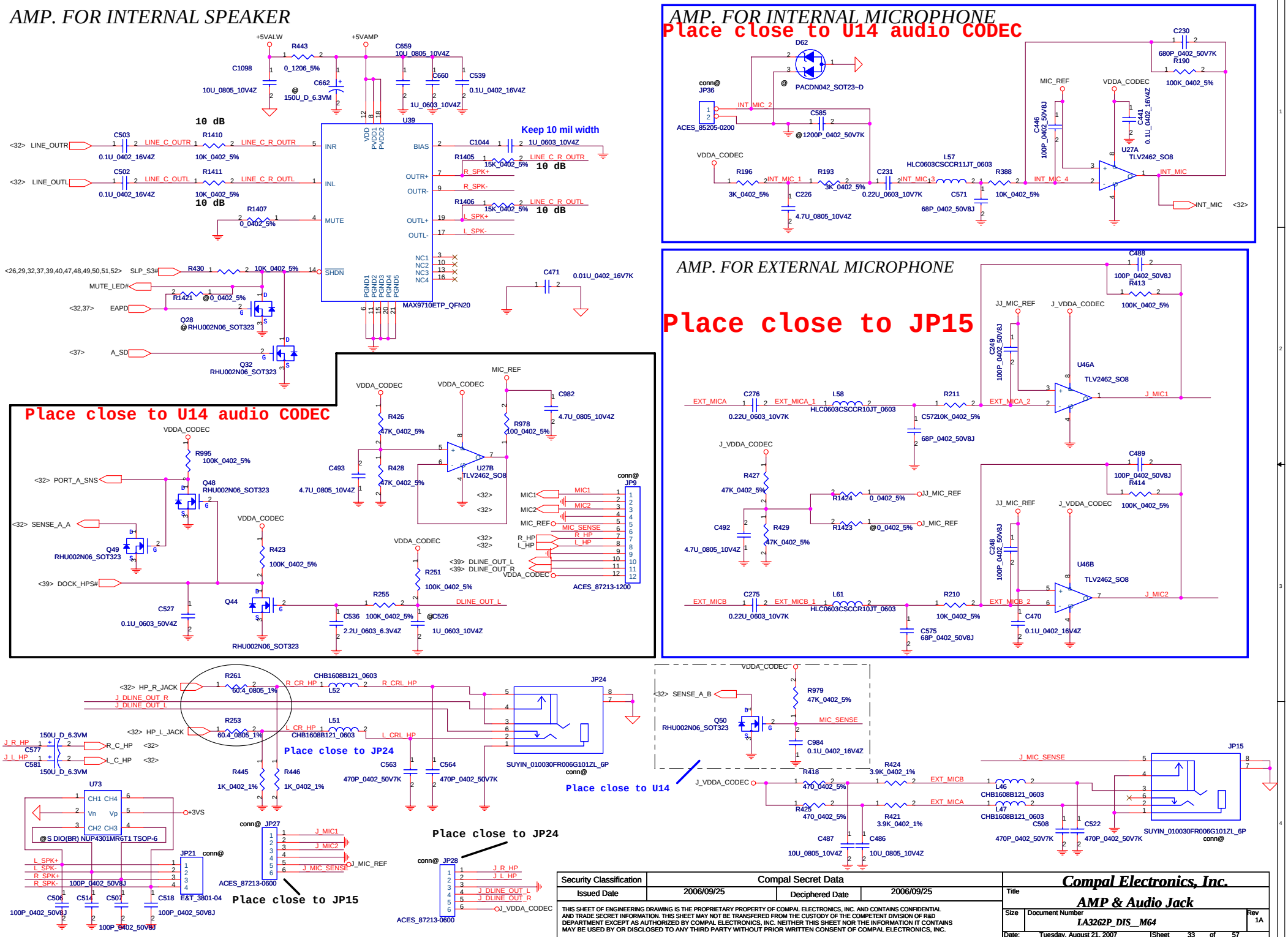
Compal Electronics, Inc.

Title: **AC97 CODEC AD1981B**

Size | Document Number: LA3262P_DIS__M64 | Rev 1A

Date: Tuesday, August 21, 2007 | Sheet 32 of 57


AMP. FOR INTERNAL SPEAKER
AMP. FOR INTERNAL MICROPHONE
Place close to U14 audio CODEC
AMP. FOR EXTERNAL MICROPHONE
Place close to JP15
Place close to U14 audio CODEC
Place close to JP24
Place close to U14
Place close to JP24
Place close to JP15
MAX9710ETP_QFN20
ACES_85205-0200
PACDN042_SOT23-D
TLV2462_SO8
ACES_87213-1200
SUYIN_010030FR006G101ZL_6P
ACES_87213-0600
E&T_3801-04
@S DIO(BR) NUP4301MR6T1 TSOP-6
Security Classification
Compal Secret Data
Issued Date
2006/09/25
Deciphered Date
2006/09/25
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Compal Electronics, Inc.
Title
AMP & Audio Jack
Size
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1A
Date:
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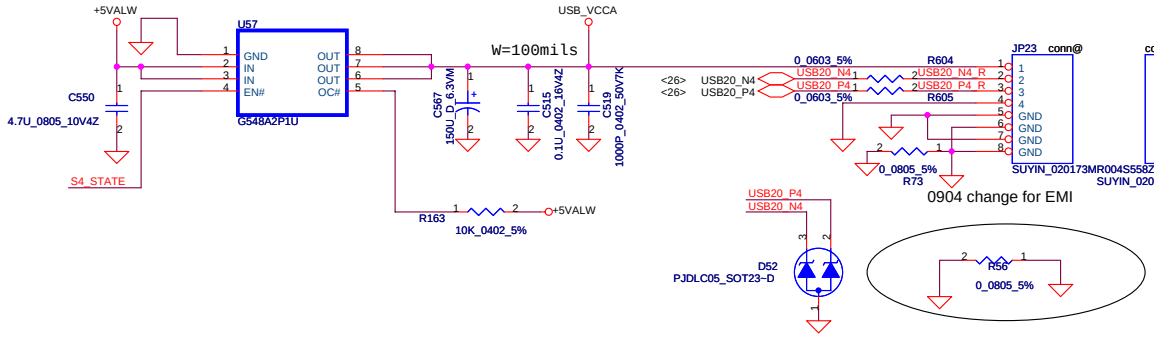
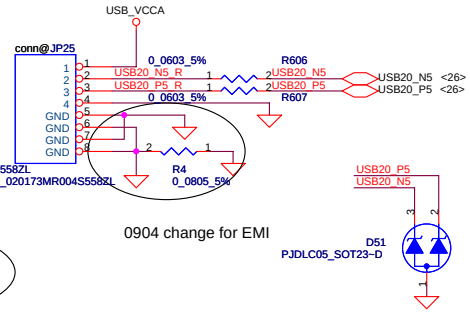
33
of
57

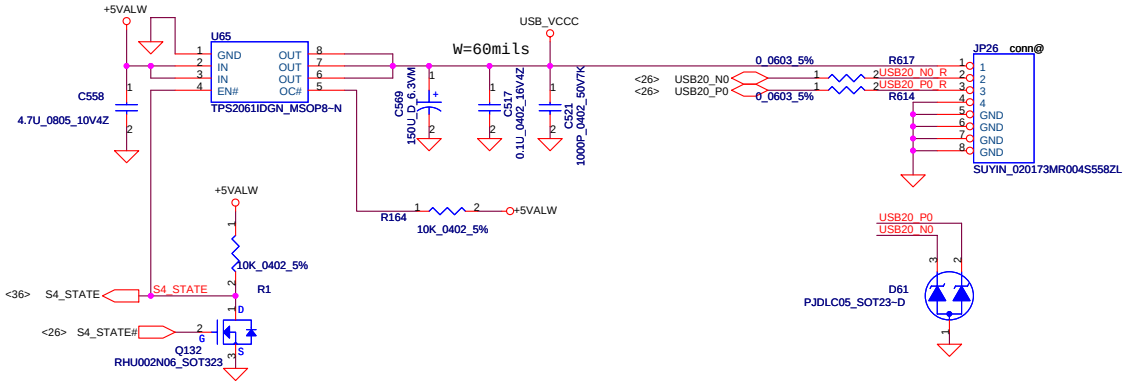
Left side USB CONNECTOR 0



Left side USB CONNECTOR 1

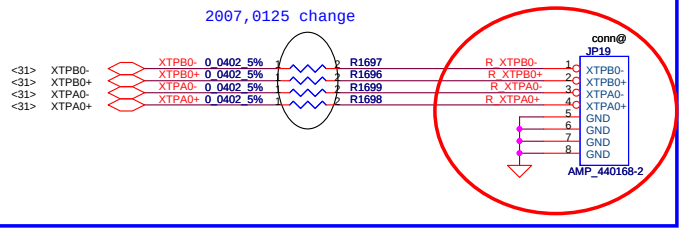


Right side USB CONNECTOR 0

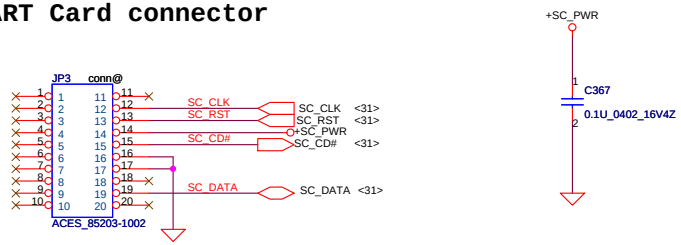


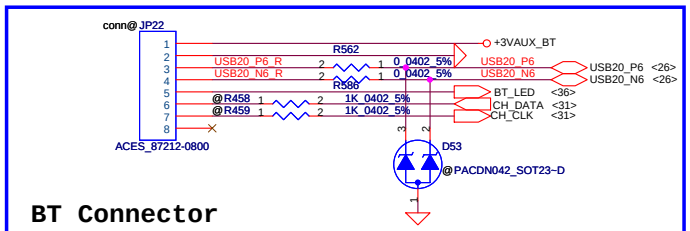
1394 connector

11/06 fix DB2 1394 can not detect issue

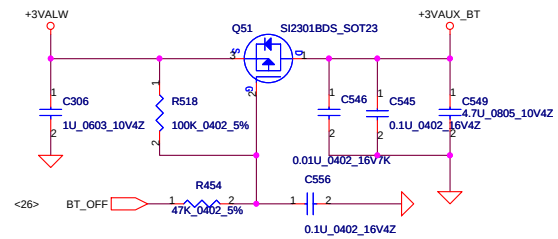


SMART Card connector





BT Connector



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Compal Electronics, Inc.

Title: **USB & BT Connector**

Size: | Document Number: LA3262P_DIS__M64 | Rev: 1A

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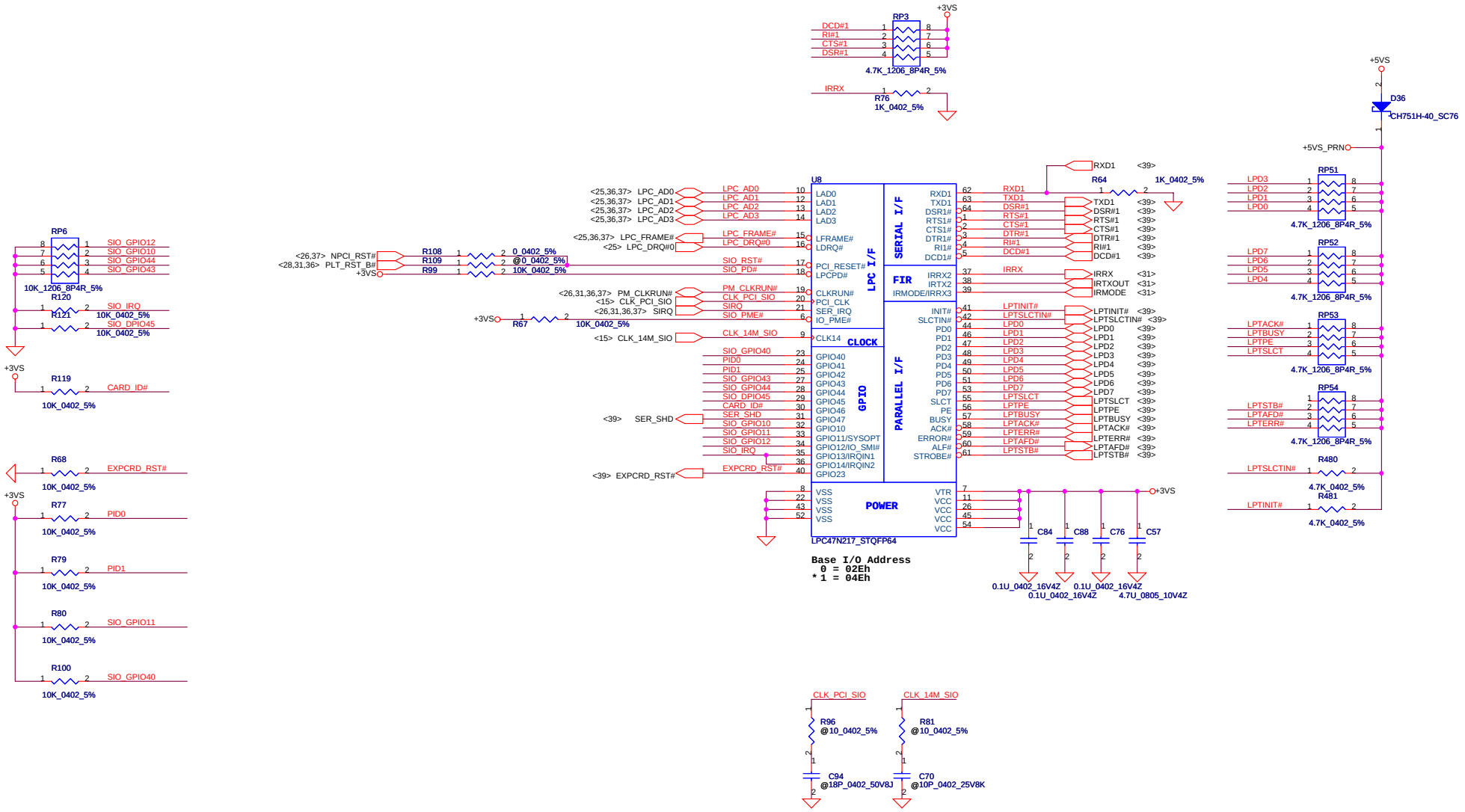

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Compal Electronics, Inc.

Title: **SUPER I/O LPC47N217**

Size: | Document Number: *LA3262P_DIS__M64* | Rev: 1A

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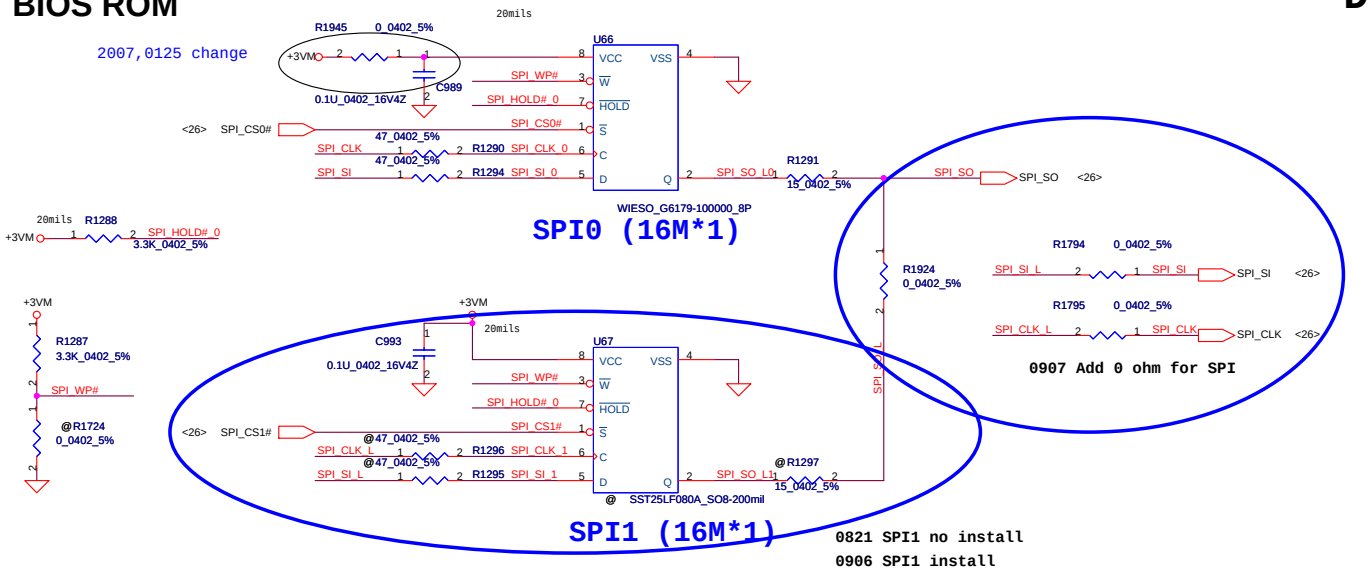
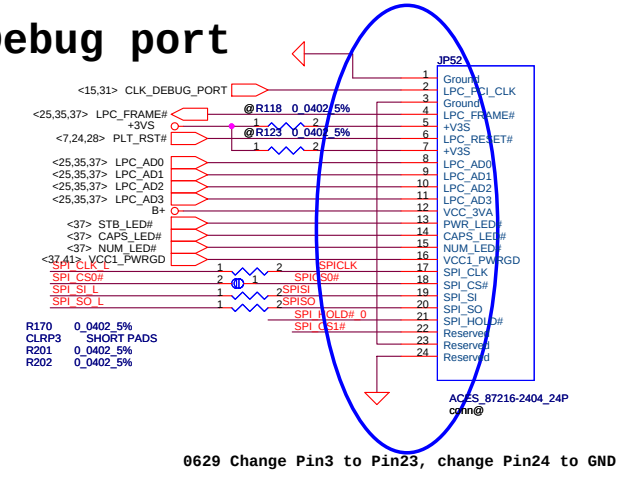
BIOS ROM

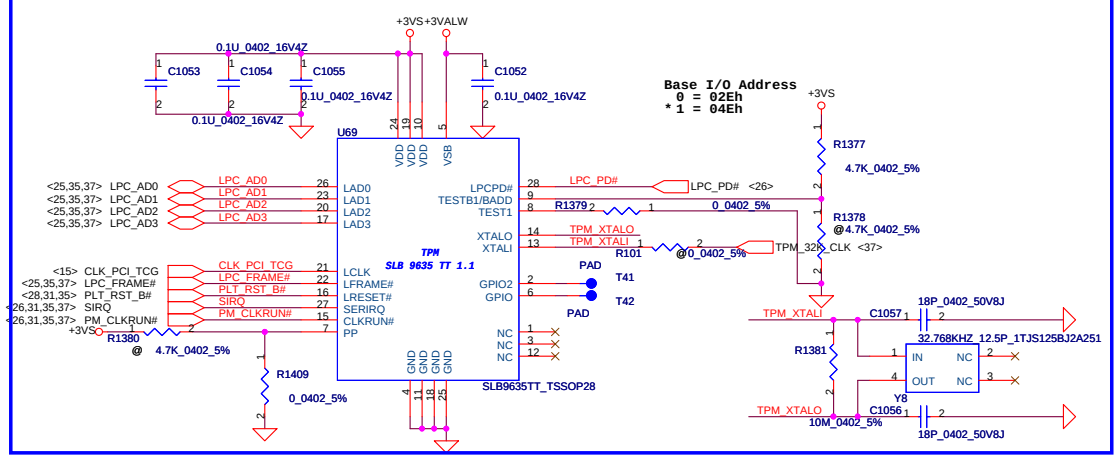
2007,0125 change



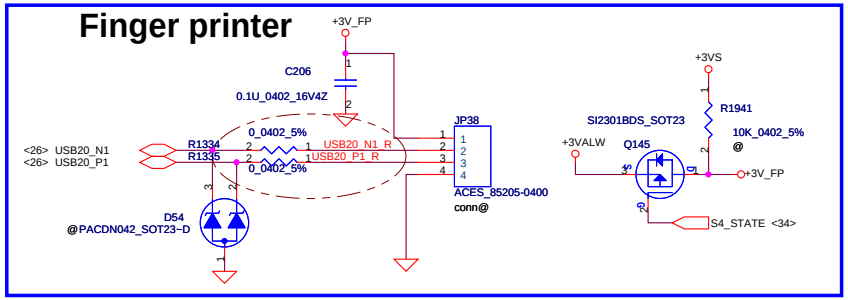
Debug port



TPM1.2

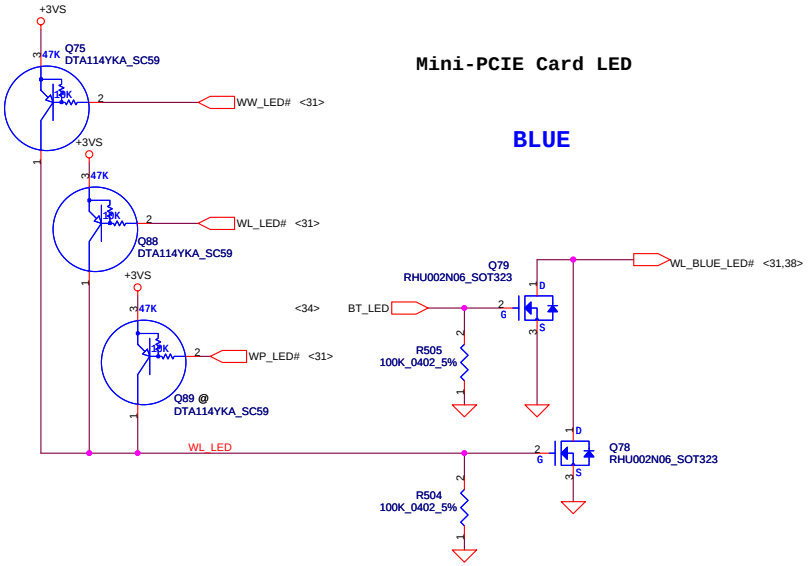


Finger printer



Mini-PCIE Card LED

BLUE



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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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Compal Electronics, Inc.

Title: **TCG/BIOS ROM/PS2/LED/SW**

Size	Document Number	Rev
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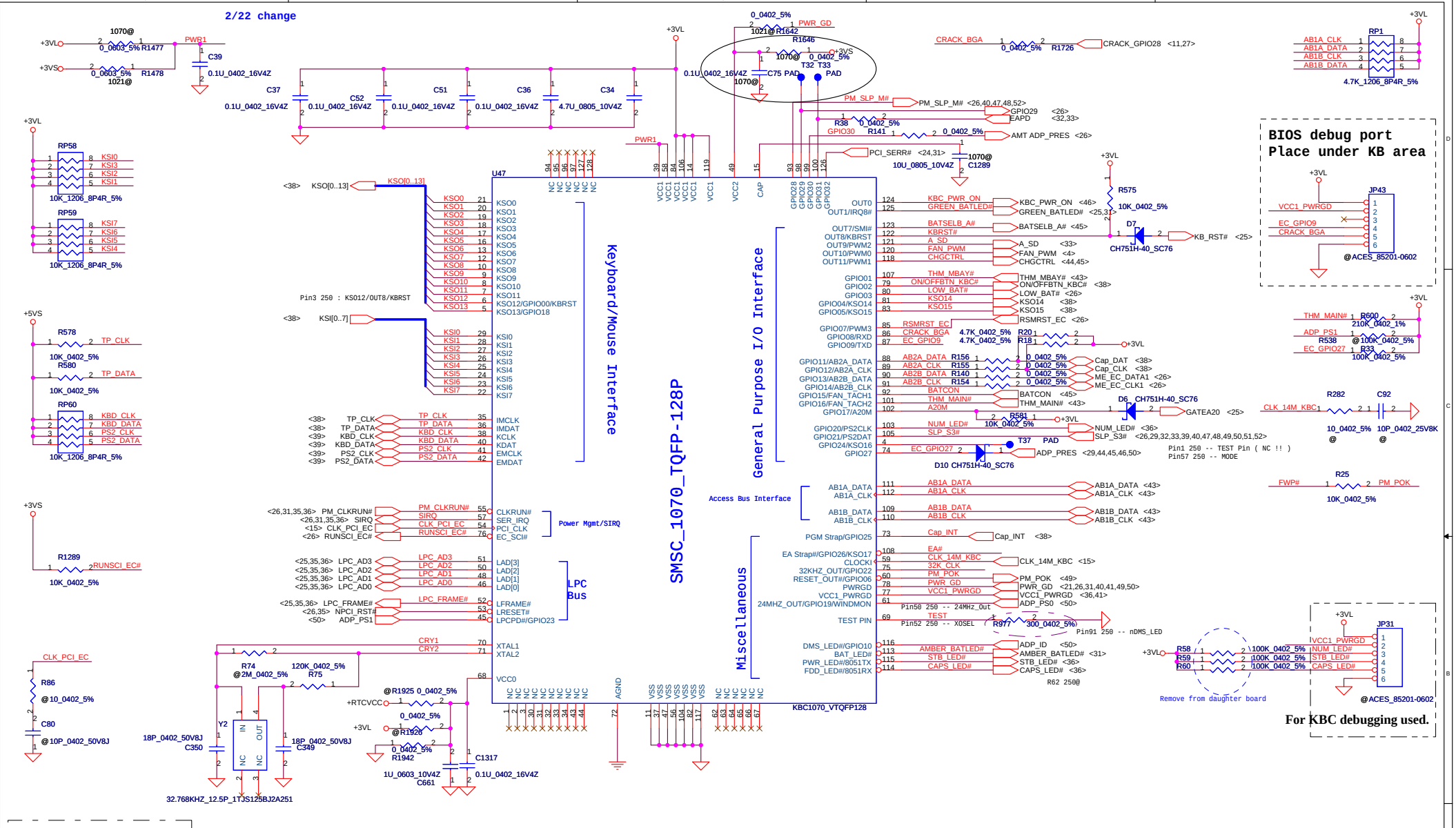

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Compal Electronics, Inc.

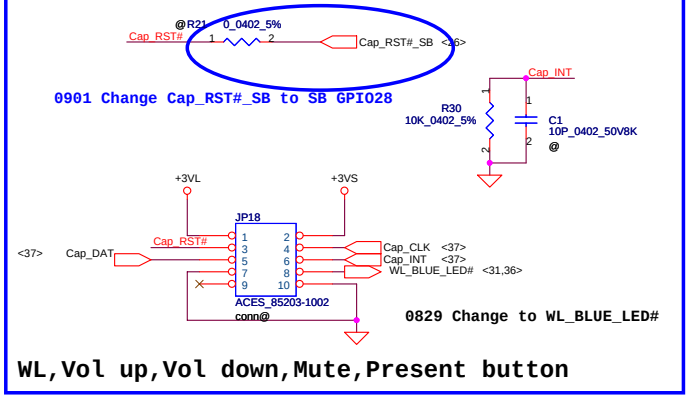
Title: LPC47N1021

Size: | Document Number: LA3262P_DIS__M64 | Rev: 1A

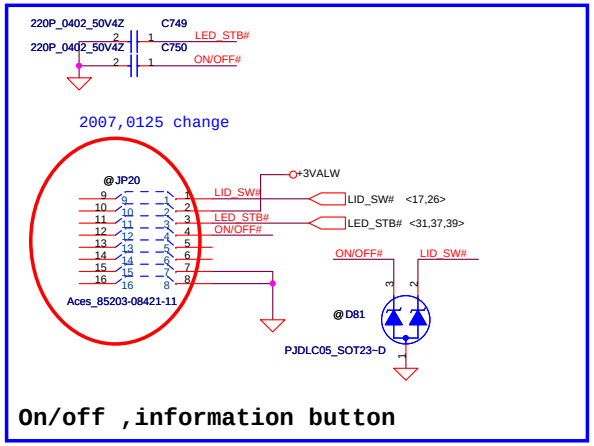
Date: Tuesday, August 21, 2007 | Sheet 37 of 57

SWITCH BOARD.

0622 change

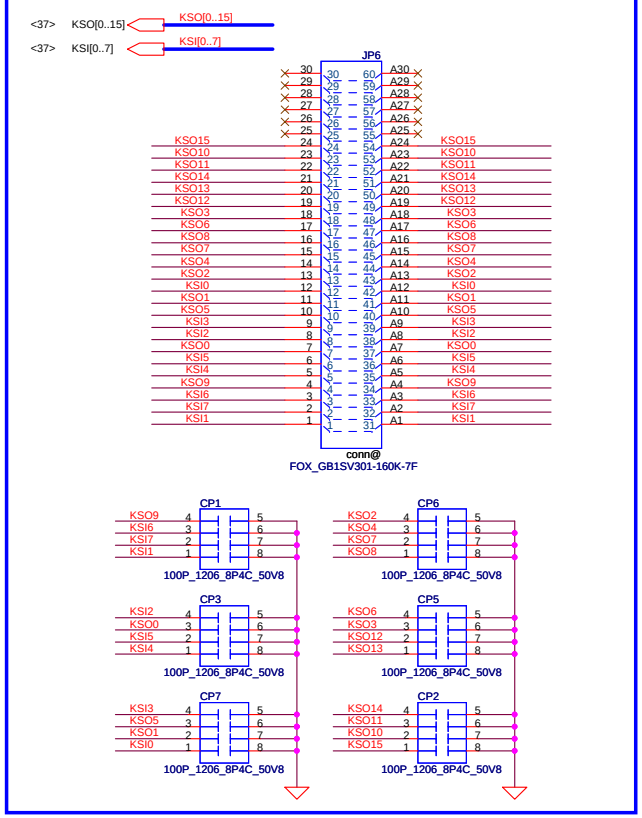


WL,Vol up,Vol down,Mute,Present button



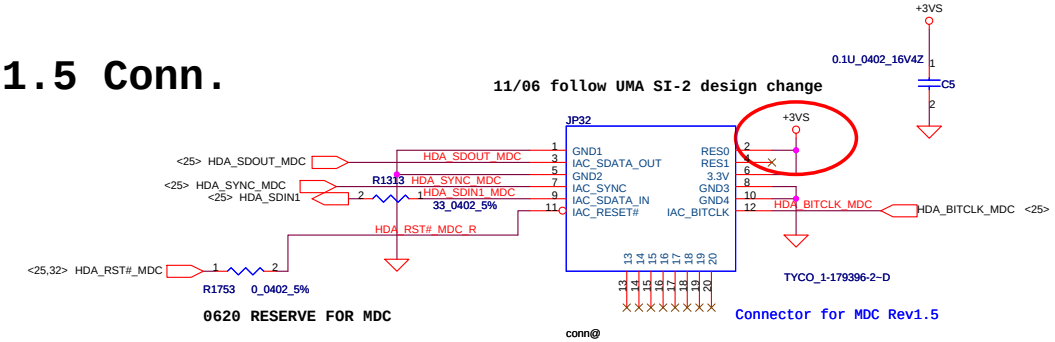
On/off ,information button

INT_KBD CONN.

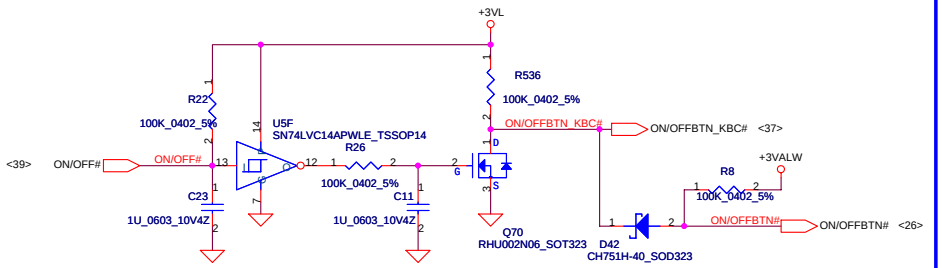


MDC 1.5 Conn.

11/06 follow UMA SI-2 design change

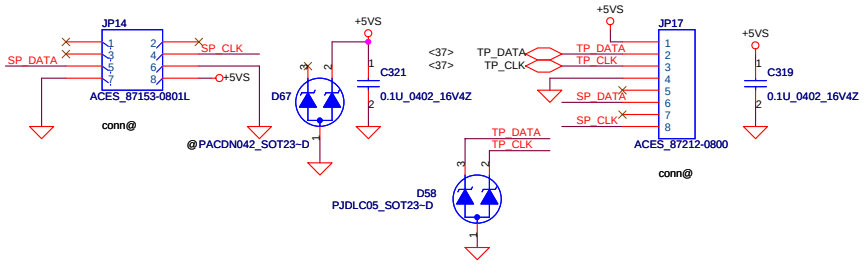


Power button



TrackPoint CONN.

T/P BOARD.



Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

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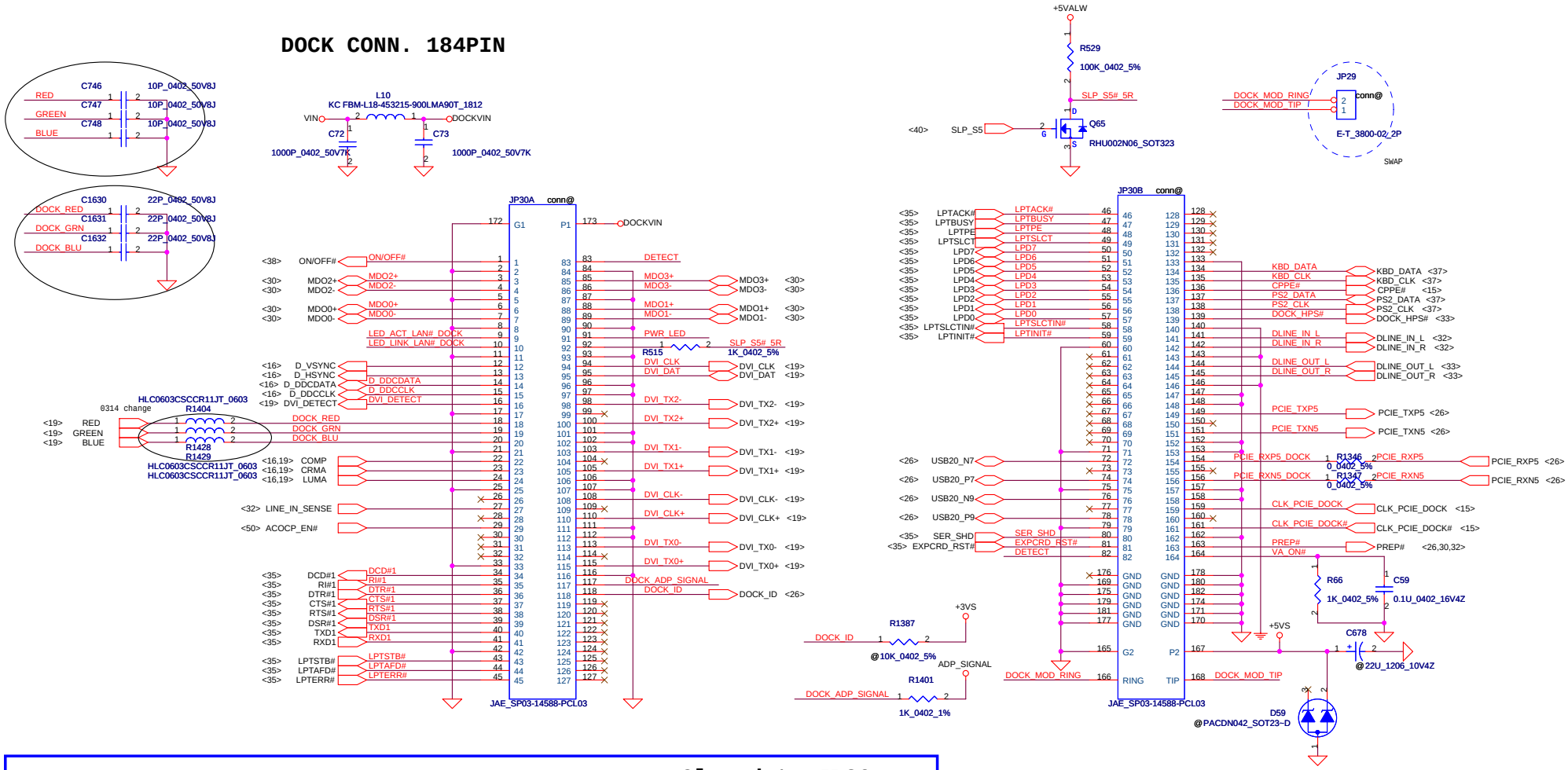
Compal Electronics, Inc.

Title: MDC/KBD/ON_OFF/LID

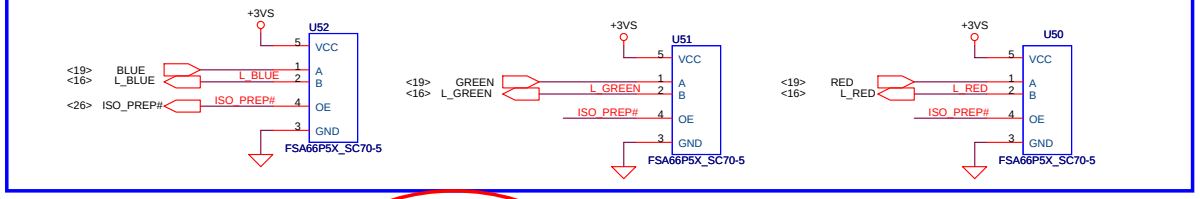
Size | Document Number: LA3262P_DIS__M64 | Rev: 1A

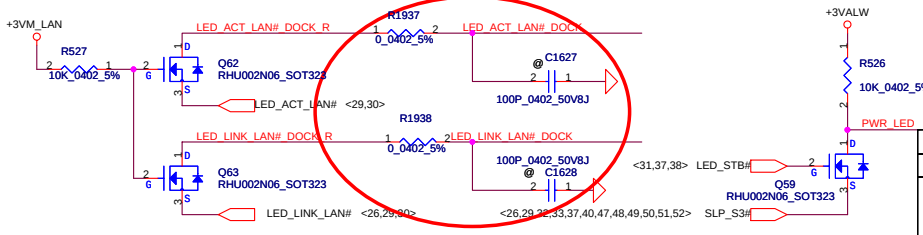
Date: Tuesday, August 21, 2007 | Sheet 38 of 57

DOCK CONN. 184PIN



Closed to JP30





Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

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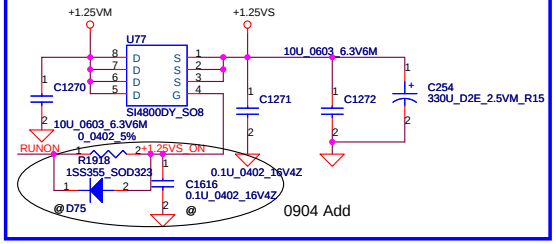
Compal Electronics, Inc.

Title: **Docking CONN.**

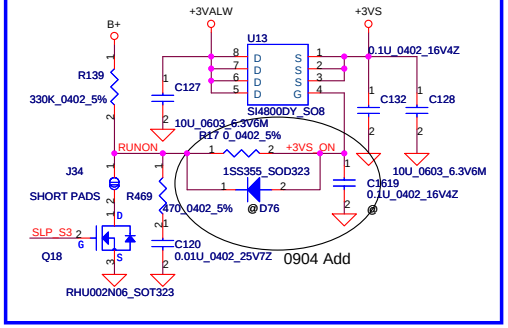
Size: | Document Number: LA3262P_DIS__M64 | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 39 of 57

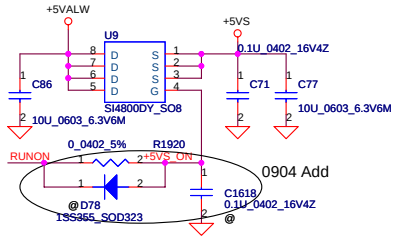
+1.25VM to +1.25VS Transfer



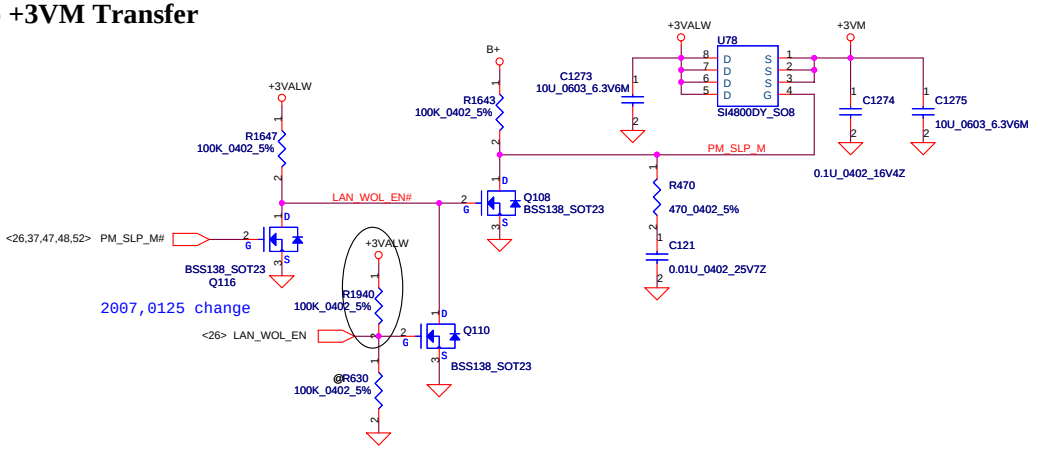
+3VALW to +3VS Transfer



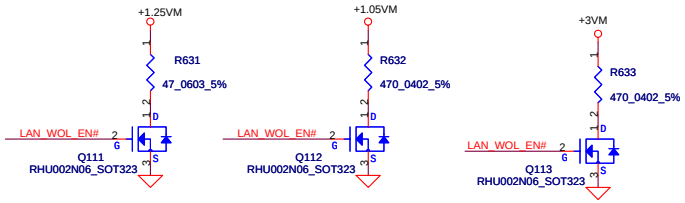
+5VALW to +5VS Transfer



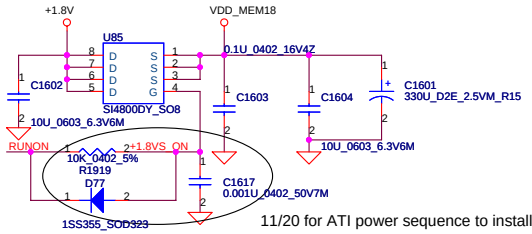
+3VALW to +3VM Transfer



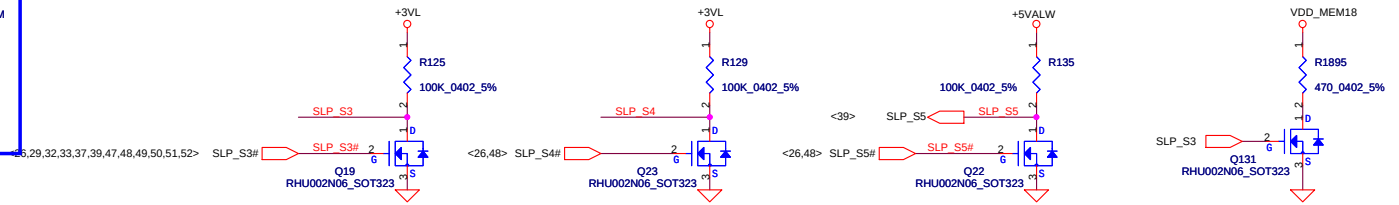
Discharge circuit-2 for V-M

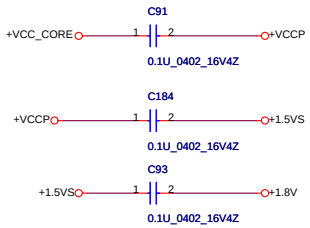


+1.8V to VDD_MEM18 Transfer

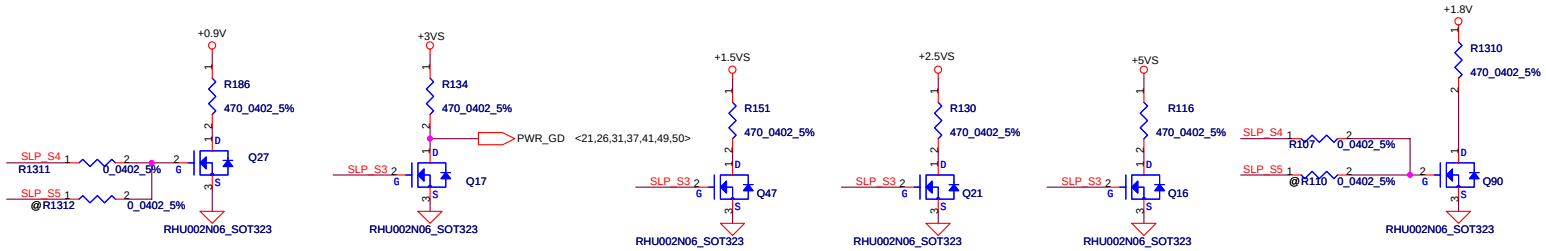


11/20 for ATI power sequence to install





Discharge circuit-1



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Issued Date	2006/09/25	Deciphered Date	2006/09/25

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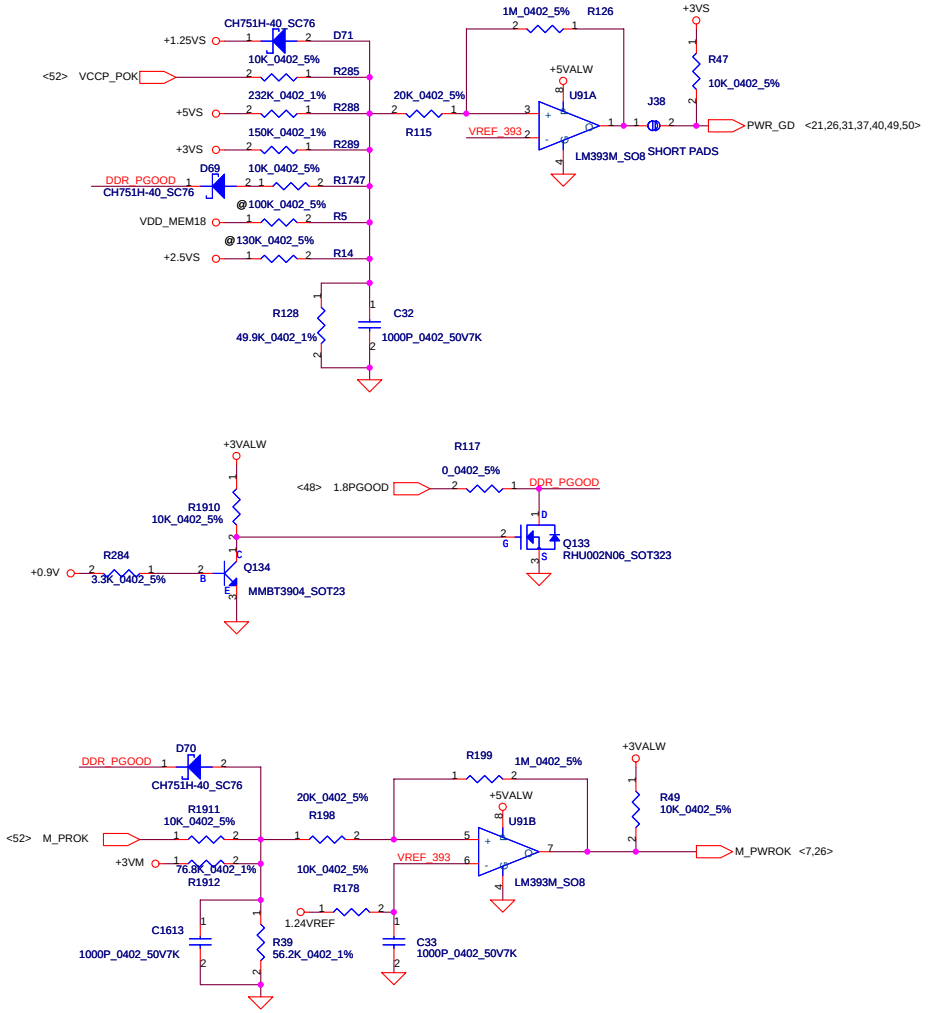
Compal Electronics, Inc.

Title: **DC/DC Circuits**

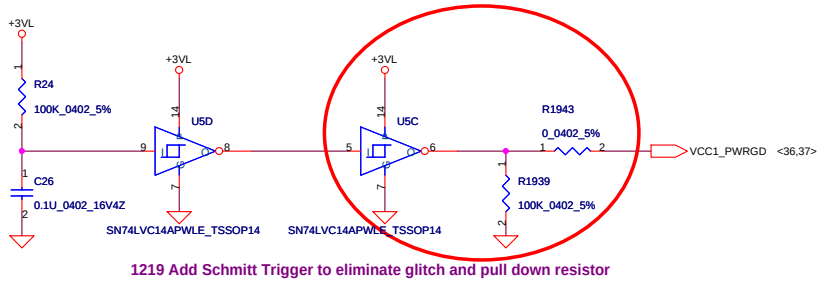
Size | Document Number: *LA3262P_DIS__M64* | Rev 1A

Date: Tuesday, August 21, 2007 | Sheet 40 of 57

PWR_OK circuit

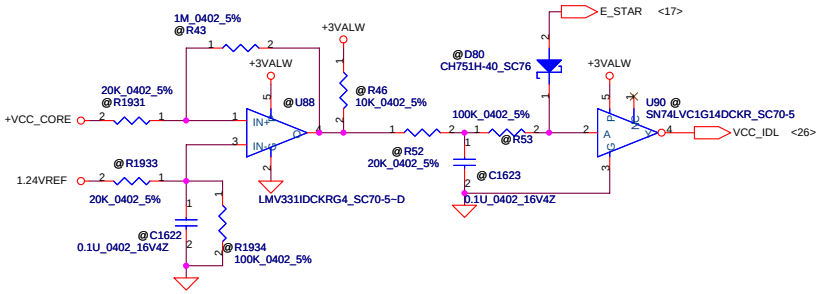


KBC PWR_OK circuit



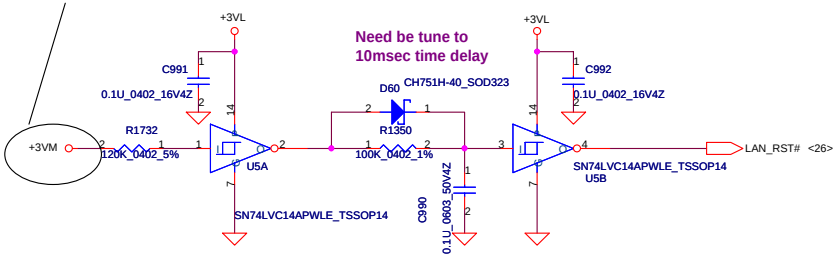
1219 Add Schmitt Trigger to eliminate glitch and pull down resistor

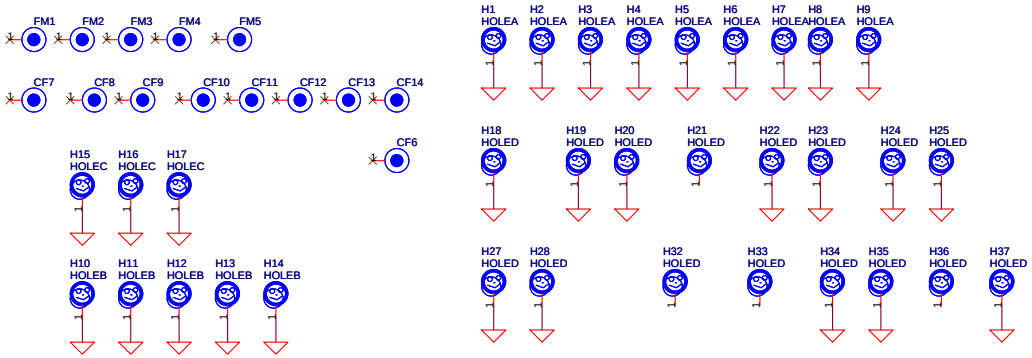
Energy Star for CPU 1114 Add



LAN_RST circuit

11/20 Enable ACBS (power management for NIC)





Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

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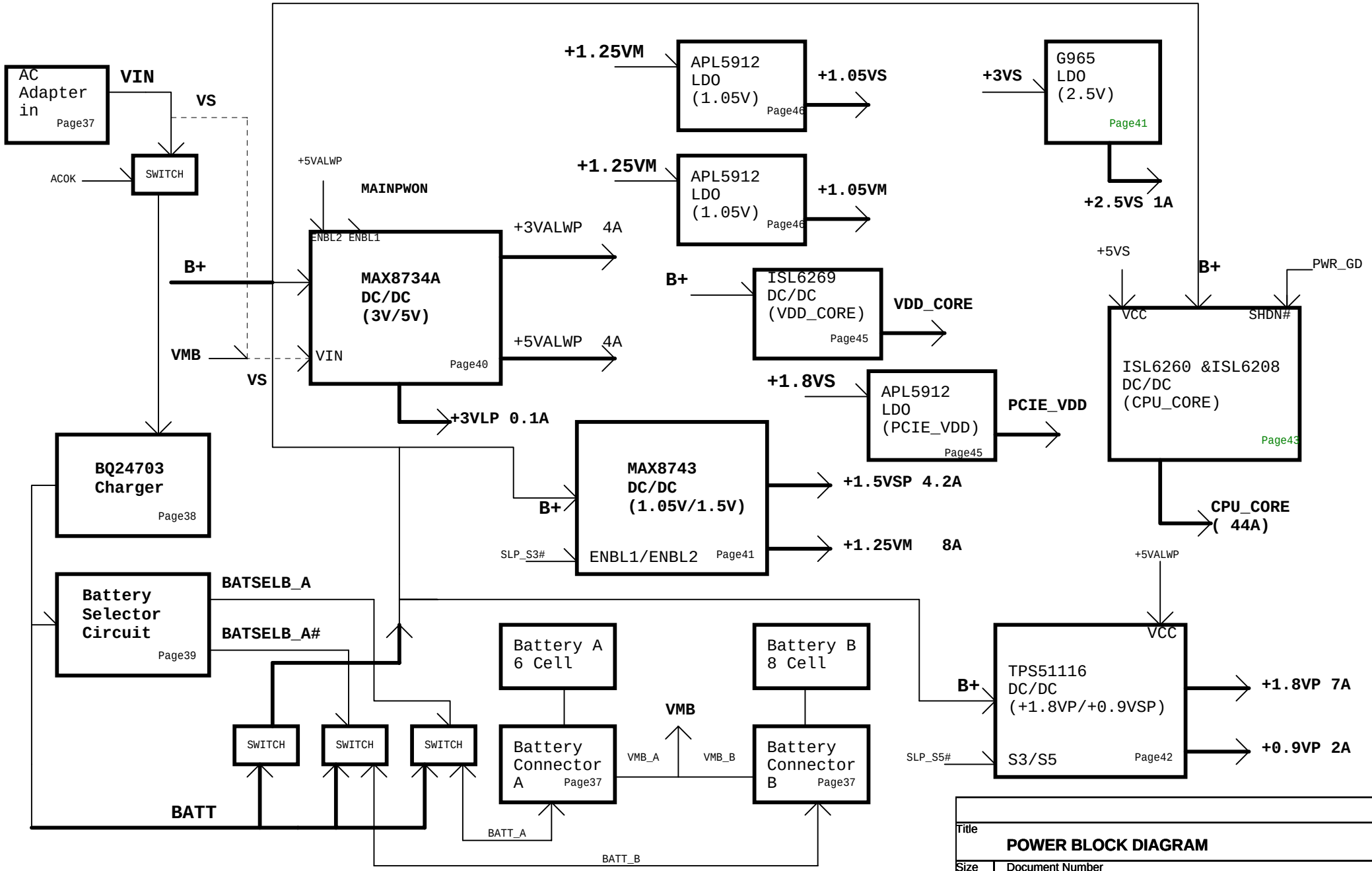
Compal Electronics, Inc.

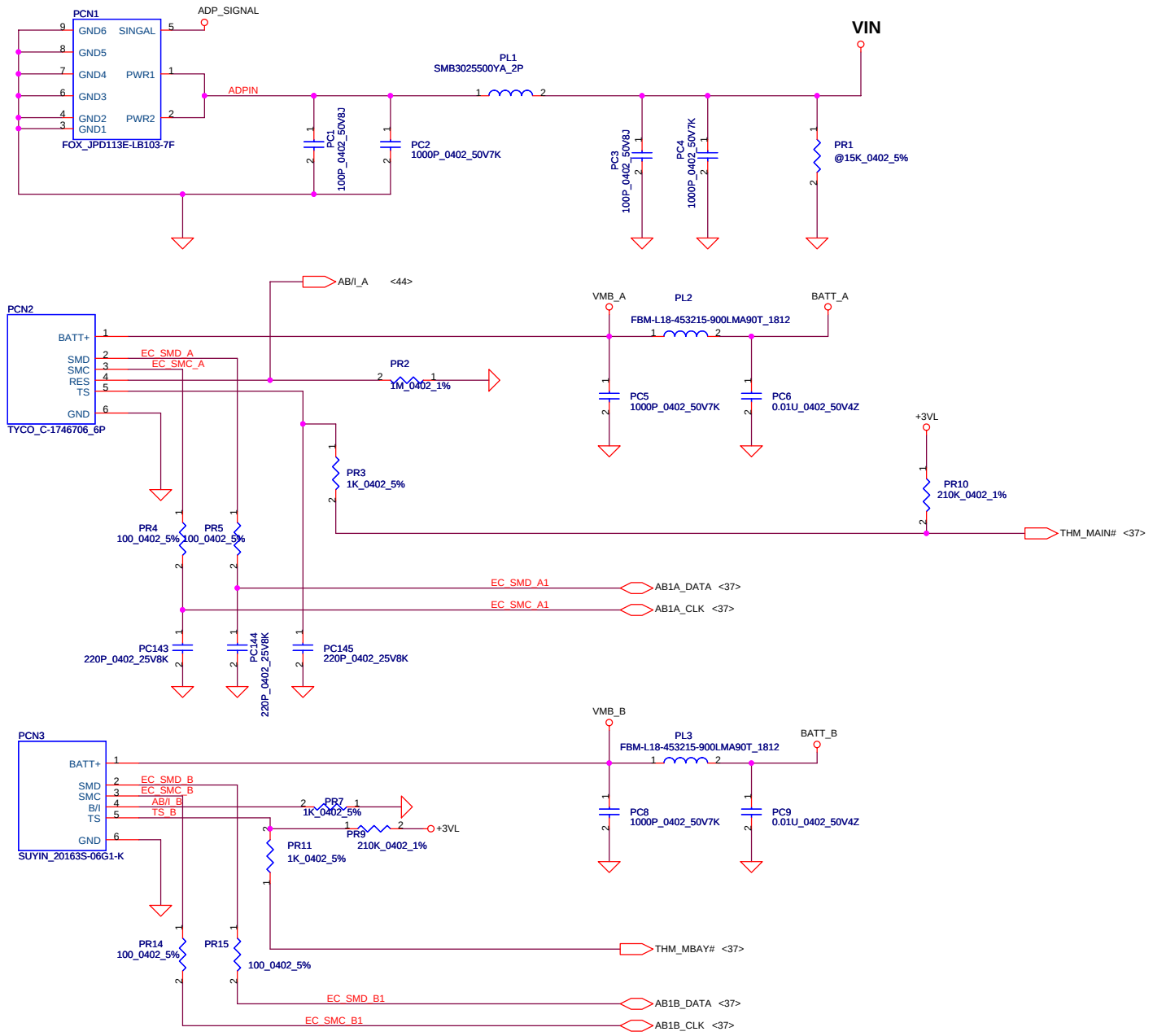
Title: **POK CKT**

Size | Document Number: LA3262P_DIS__M64 | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 41 of 57



Title	POWER BLOCK DIAGRAM	
Size	Document Number	Rev
Date: Tuesday, August 21, 2007	Sheet 42 of 57	



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Issued Date	2005/03/10	Deciphered Date	2006/03/10

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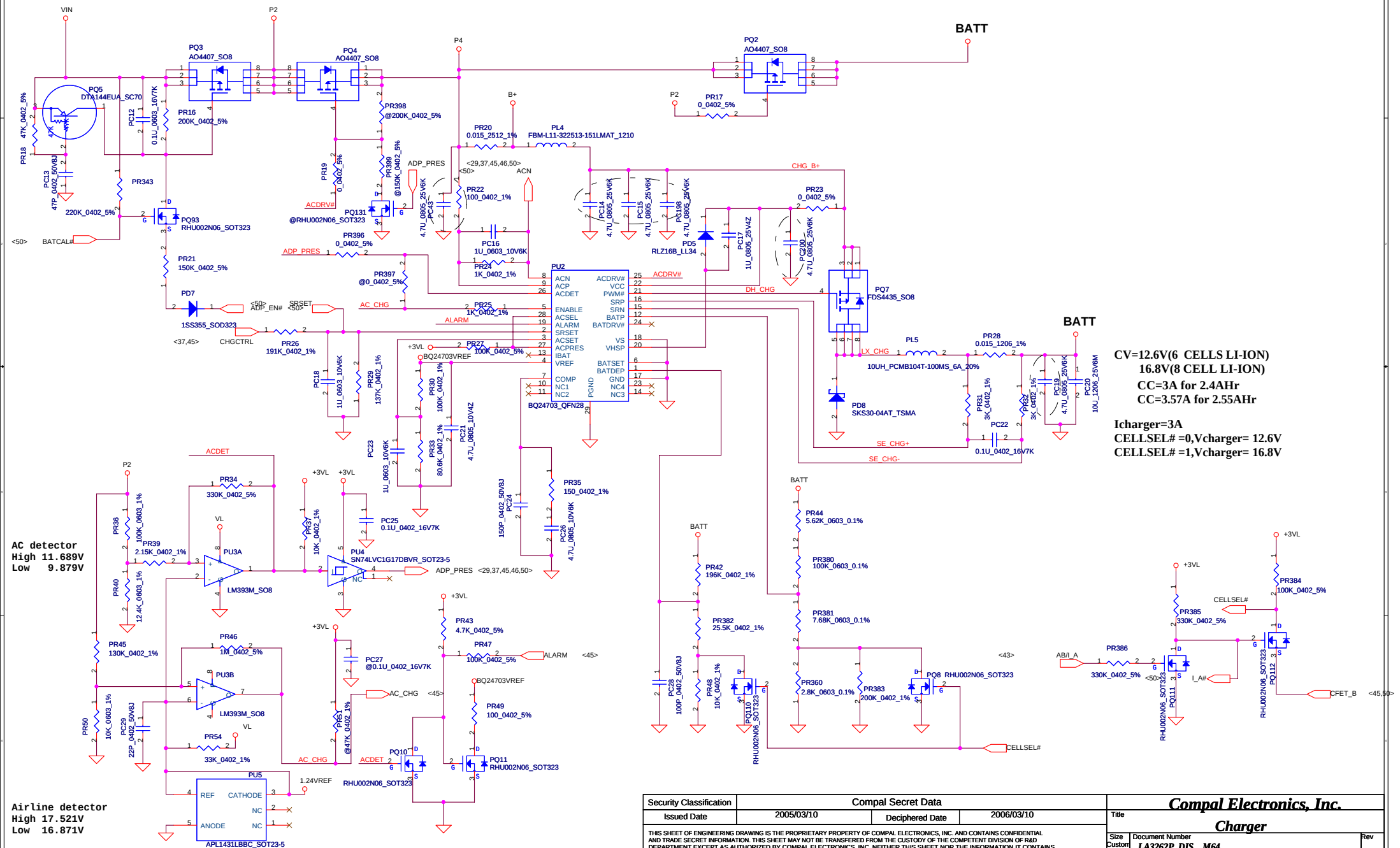
Compal Electronics, Inc.

Title: **BATTERY CONN**

Size: Custom | Document Number: *LA3262P_DIS__M64* | Rev

Date: Tuesday, August 21, 2007 | Sheet 43 of 57



CV=12.6V(6 CELLS LI-ION)
16.8V(8 CELL LI-ION)
CC=3A for 2.4AHr
CC=3.57A for 2.55AHr

Icharger=3A
CELLSEL# =0,Vcharger= 12.6V
CELLSEL# =1,Vcharger= 16.8V

AC detector
High 11.689V
Low 9.879V

Airline detector
High 17.521V
Low 16.871V

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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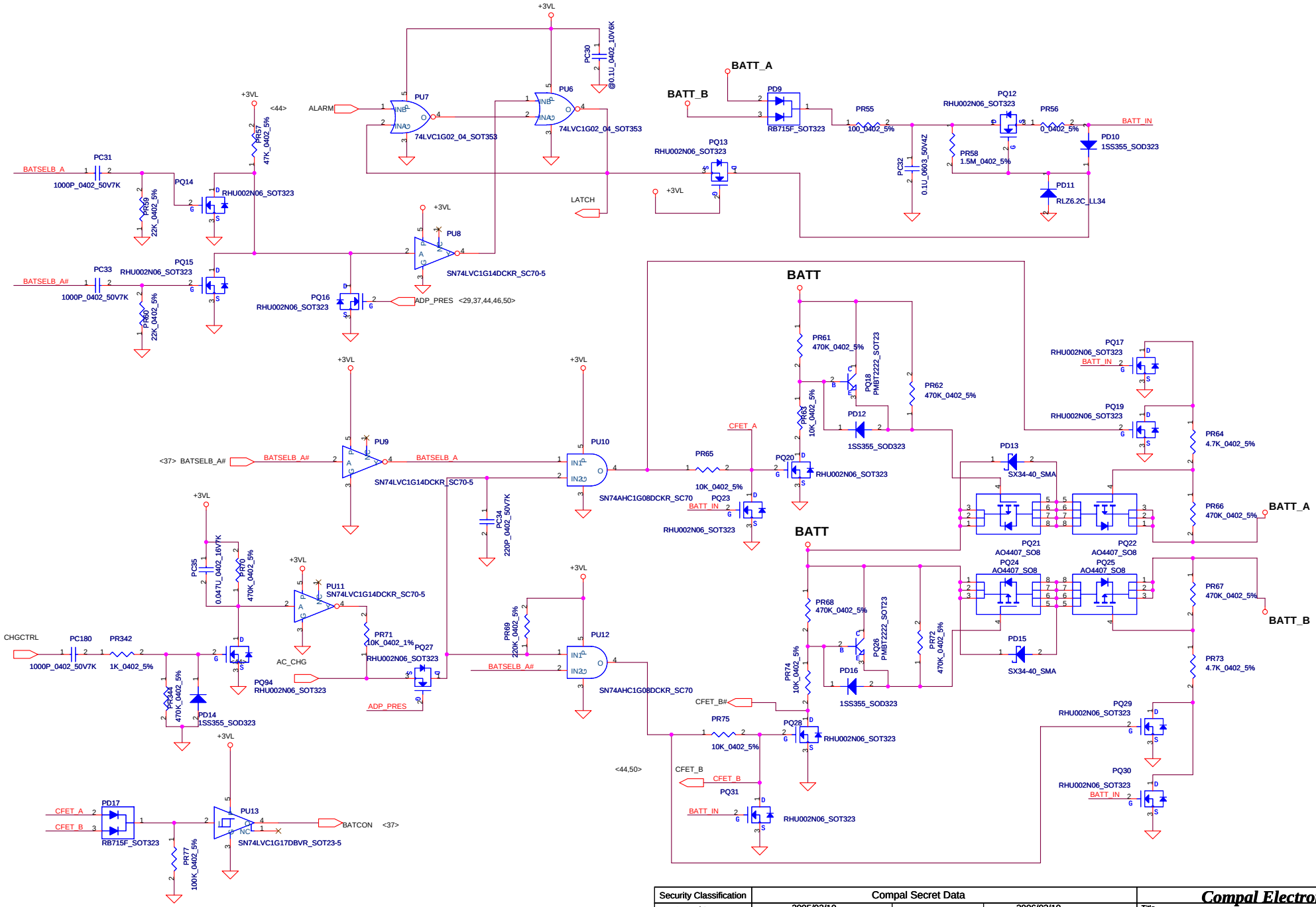
Compal Electronics, Inc.

Title: **Charger**

Size: Custom | Document Number: *LA3262P_DIS__M64* | Rev

Date: Tuesday, August 21, 2007 | Sheet 44 of 57



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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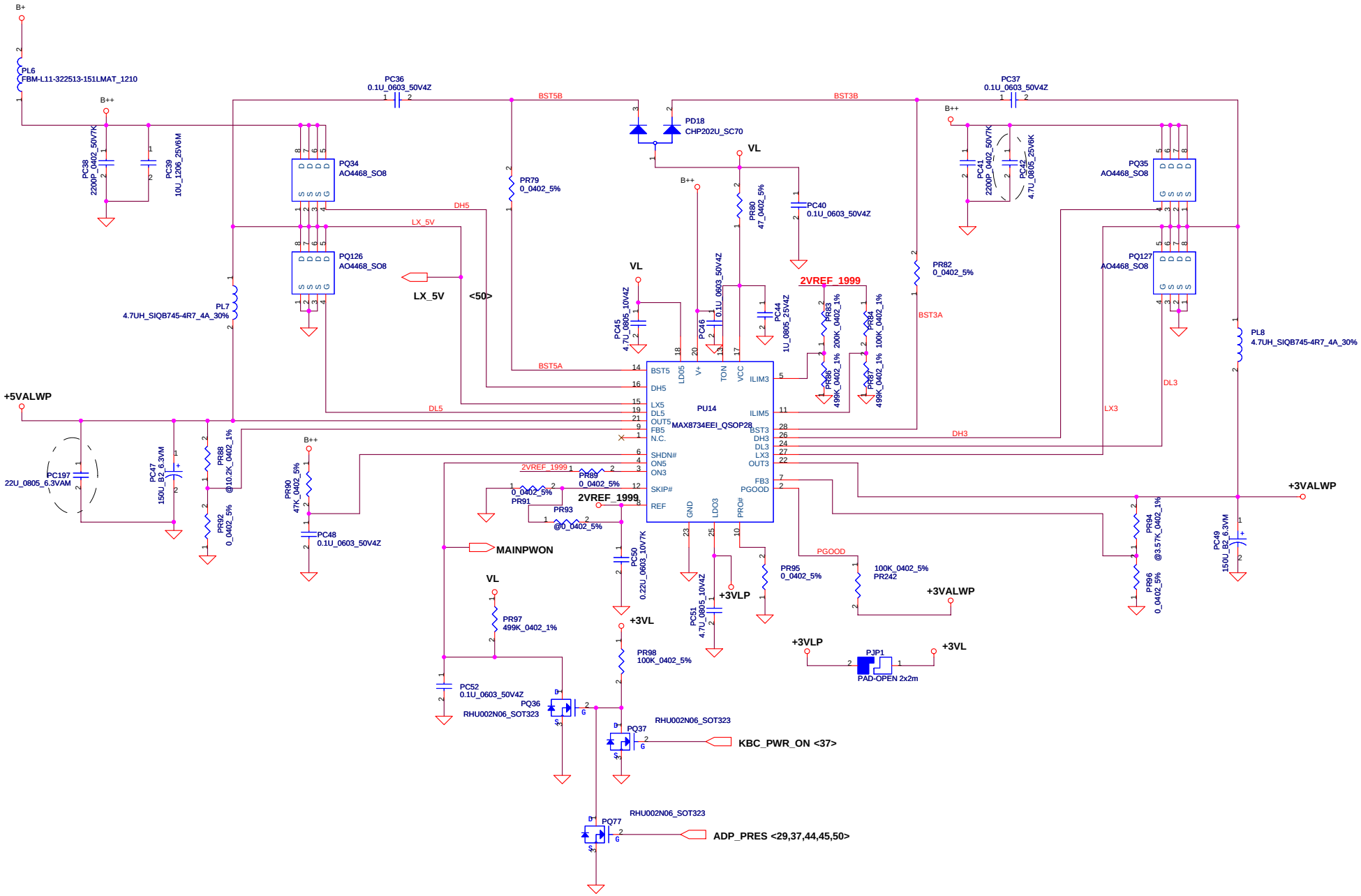
Compal Electronics, Inc.

Title: **Battery selector**

Size: Custom | Document Number: LA3262P_DIS_M64 | Rev

Date: Tuesday, August 21, 2007 | Sheet 45 of 57

+3.3V/+5V



Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2006/03/01

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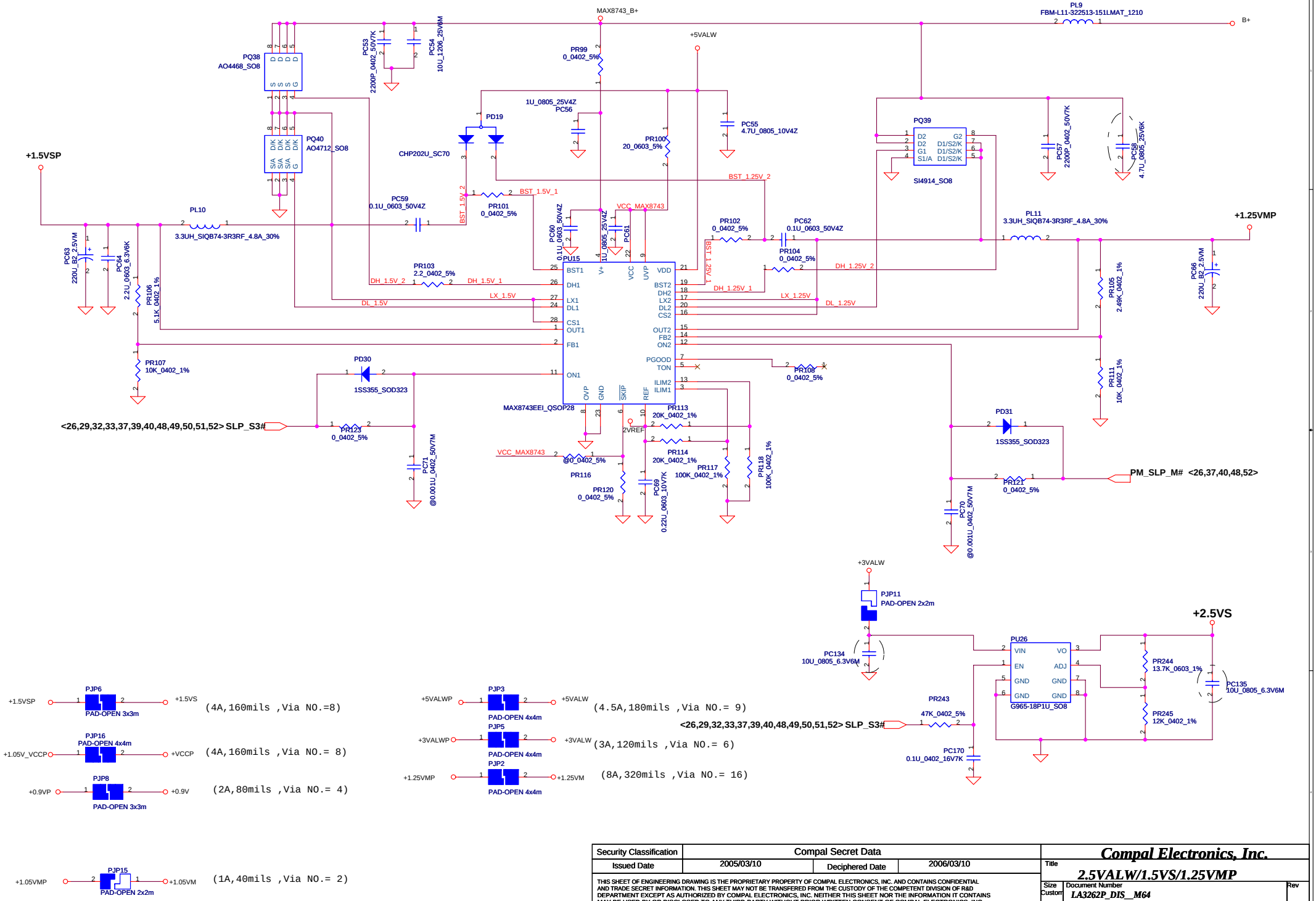
Title: 3.3V / 5V

Size: B | Document Number: LA3262P_DIS__M64 | Rev: 1A

Date: Tuesday, August 21, 2007 | Sheet 46 of 57



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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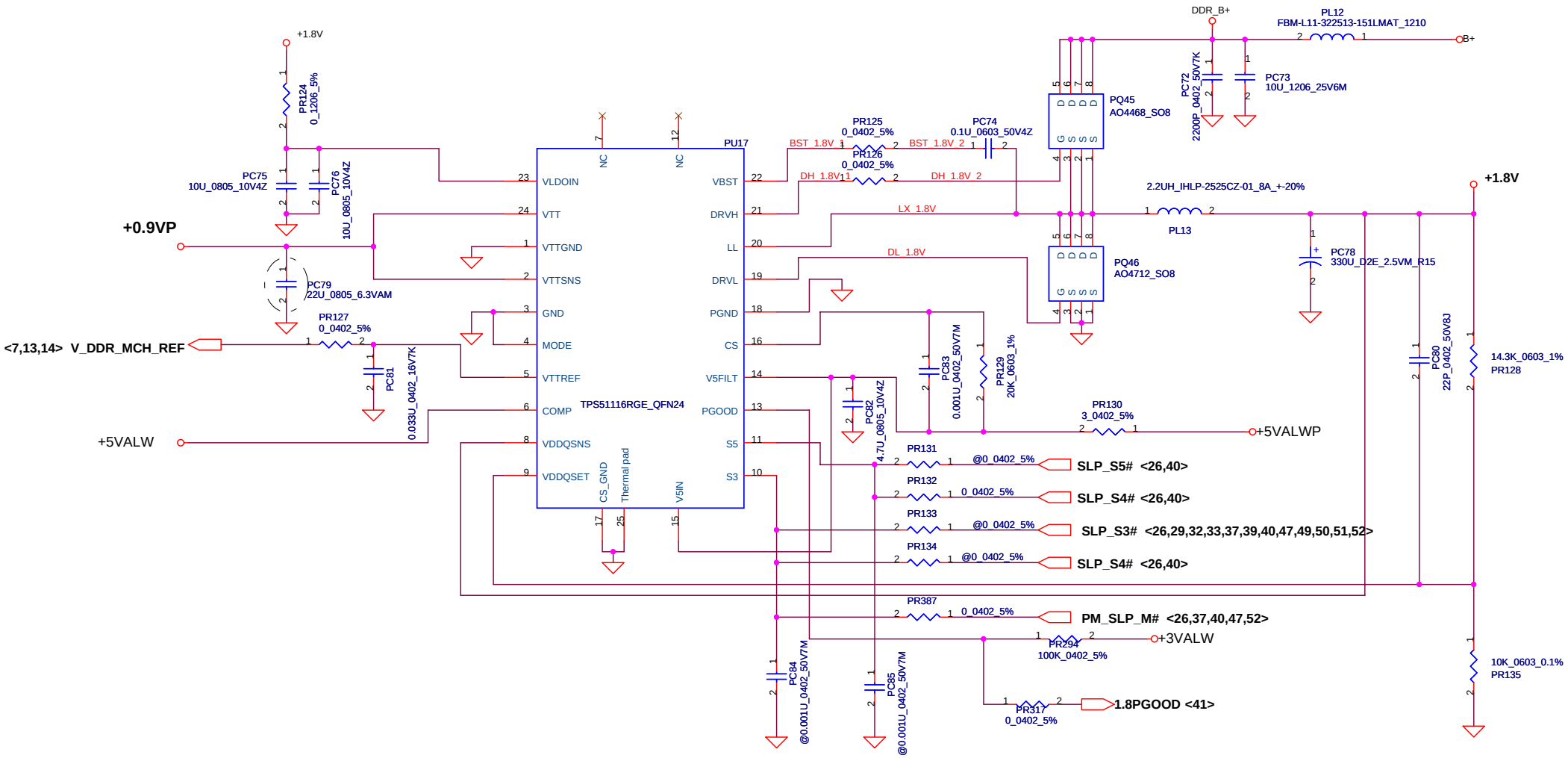
Compal Electronics, Inc.

Title: **2.5VALW/1.5VS/1.25VMP**

Size: Custom | Document Number: LA3262P_DIS__M64 | Rev

Date: Tuesday, August 21, 2007 | Sheet 47 of 57



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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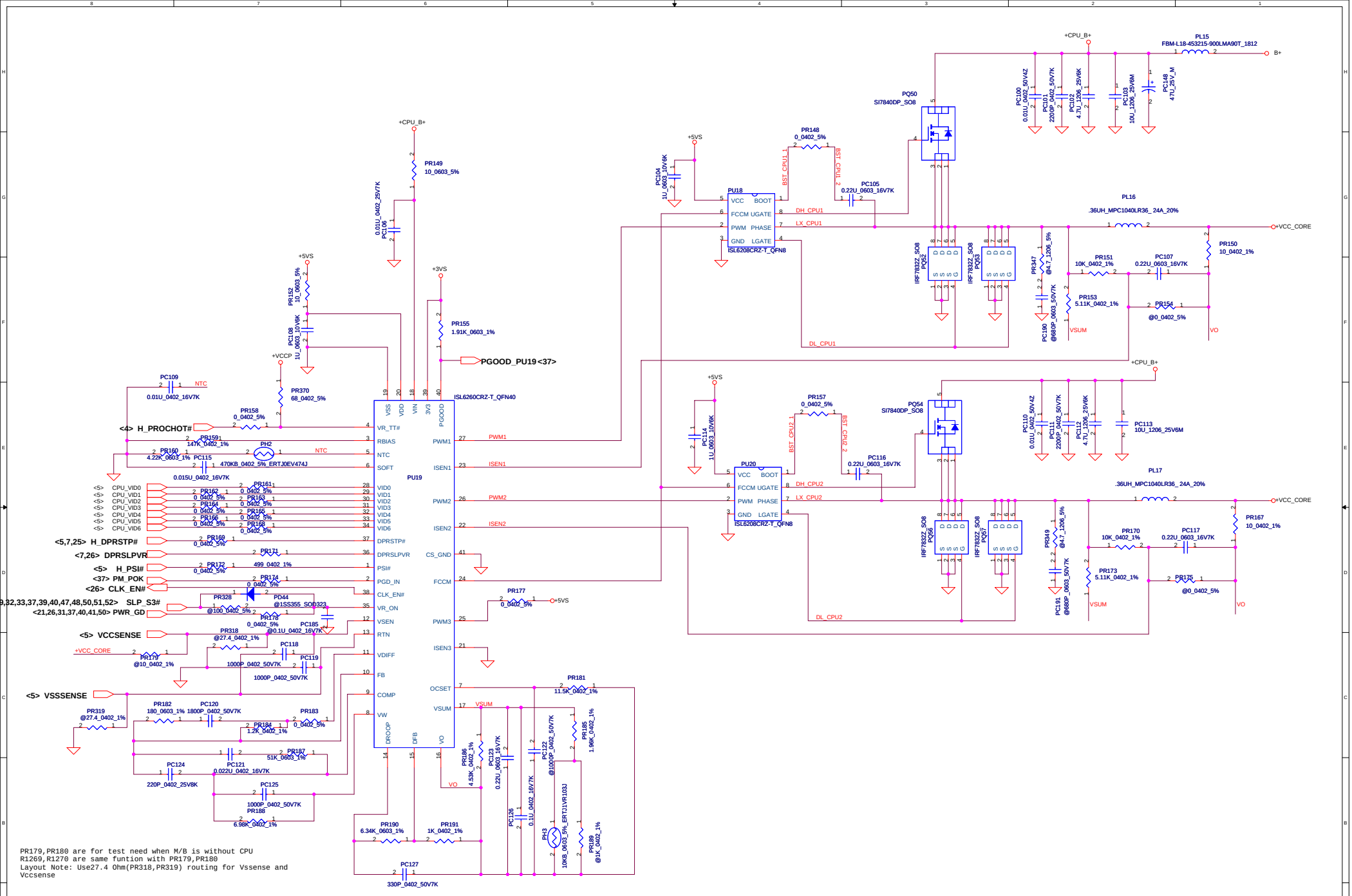
Compal Electronics, Inc.

Title: **1.8V/0.9VS**

Size: B | Document Number: LA3262P_DIS__M64 | Rev

Date: Tuesday, August 21, 2007 | Sheet 48 of 57



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
C	LA3262P_DIS__M64	

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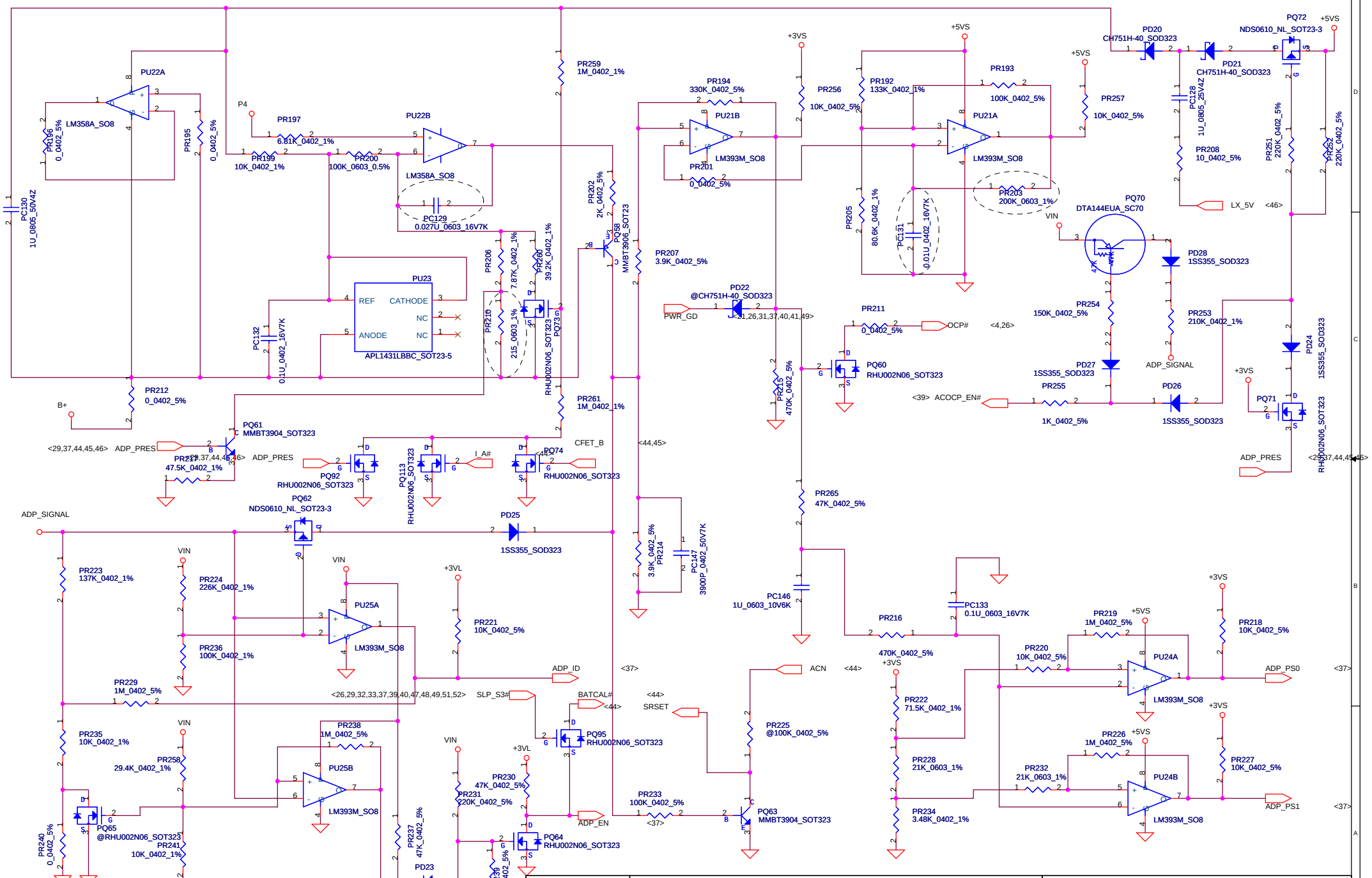

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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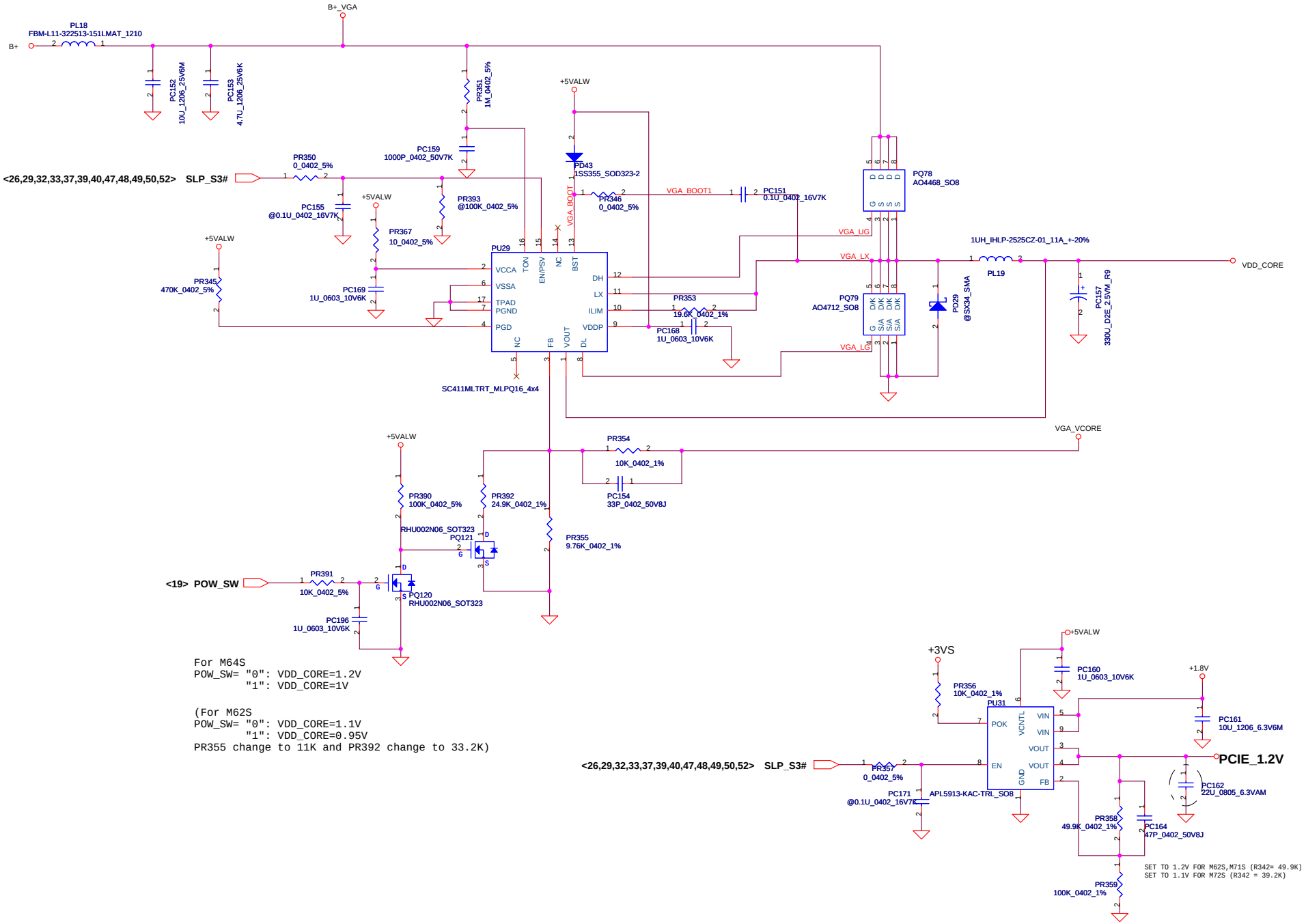
2005.8.20

Compal Electronics, Inc.

Title: **ADP_OCP**

Size: Custom | Document Number: *LA3262P_DIS__M64* | Rev

Date: Tuesday, August 21, 2007 | Sheet 50 of 57



For M64S
POW_SW= "0": VDD_CORE=1.2V
"1": VDD_CORE=1V

(For M62S
POW_SW= "0": VDD_CORE=1.1V
"1": VDD_CORE=0.95V
PR355 change to 11K and PR392 change to 33.2K)

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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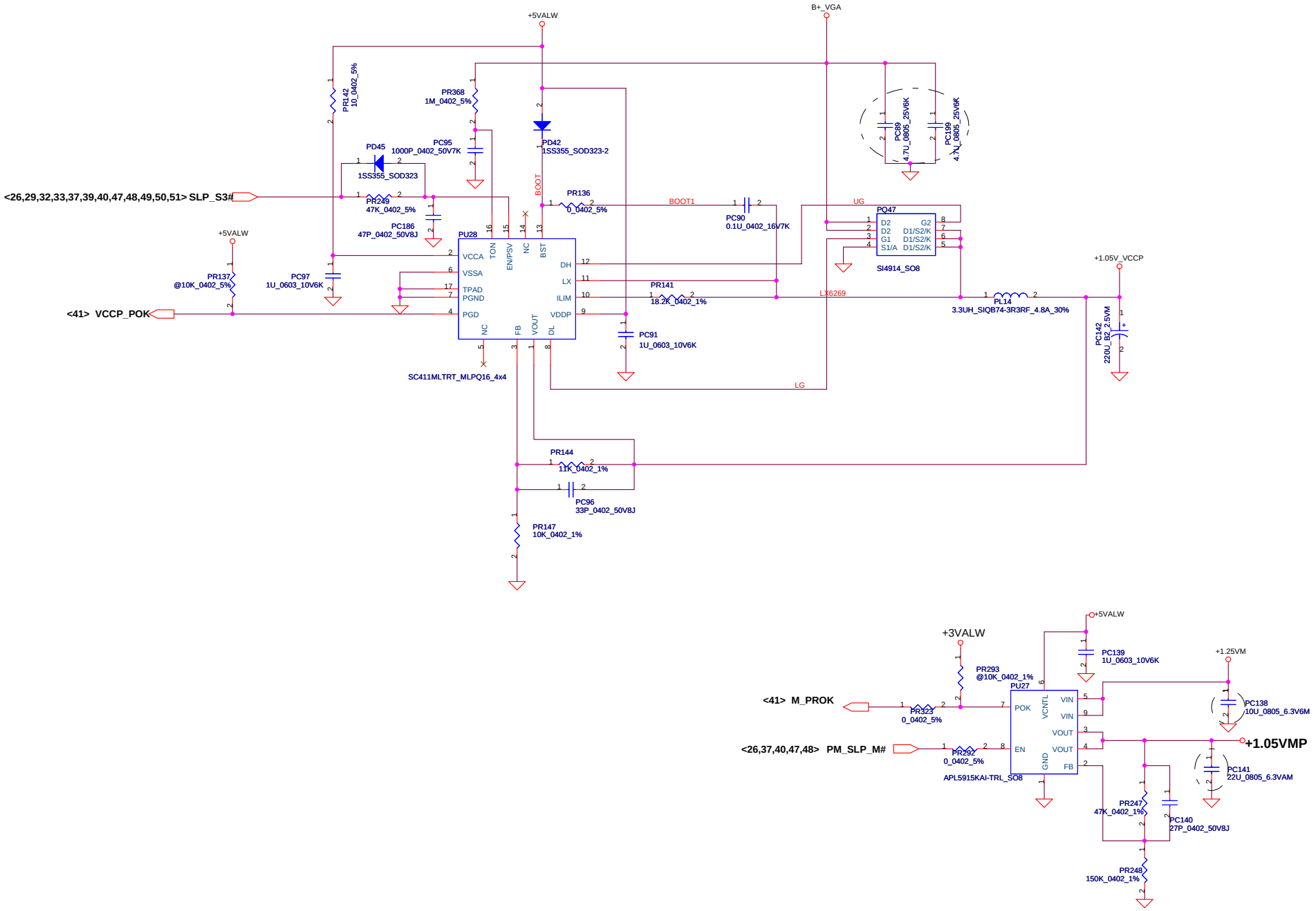
Compal Electronics, Inc.

Title: **VDD_CORE**

Size: Custom | Document Number: *LA3262P_DIS__M64* | Rev

Date: Tuesday, August 21, 2007 | Sheet 51 of 57



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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Compal Electronics, Inc.

Title: **+1.25VMP/+1.05V_VCCP**

Size: Custom | Document Number: *LA3262P_DIS__M64* | Rev

Date: Tuesday, August 21, 2007 | Sheet 52 of 57

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as 1uf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2
14	44	Charger	2007/3/1	PWR Francis H	Reserve circuit for testing Energy STAR	Reserve PR397, PR398, PR399 and PQ131 Add PR396 as 0 ohm.	PV
15	51	VDD_CORE /PCIE_VDD	2007/3/1	PWR Francis H	MOSFET change for M64s (original design is for M72)	Change PQ78 from IRF7413Z to AO4468 Change PQ79 from IRF8113 to AO4712 Change PR353 from 6.81K to 19.6K	PV
16	50	ADP_OCP	2007/4/12	HP R.L.	Fine tune system OCP setting for battery spec	Change PR210 from 422 to 215 Change PC129 from .22u to .027u Change PR203 from 604K to 200K Change PC131 from .027u to .01u	MV
17	44 46 47 48 51 52	Charger 3.3V/5V 1.5VS/1.25VM +1.25VMP/ 1.8V/0.9V VDD_CORE /PCIE_VDD +1.25VMP/ +1.05V_VCCP	2007/7/30	HP R.L.	Change some MLCCs size from 1206 to 0805	1. Change PC14 from 10u_1206 to 4.7u_0805 Add PC198 as 4.7u_0805 2. Change PC89 from 10u_1206 to 4.7u_0805 Add PC199 as 4.7u_0805 3. Change PC15, PC19, PC42 and PC58 from 4.7u_1206 to 4.7u_0805 4. Change PC79, PC141, PC162 and PC197 from 22u_1206 to 22u_0805 5. Change PC134, PC135 and PC138 from 10u_1206 to 10u_0805	MP
18	44	Charger	2007/7/30	TI	For TI's suggestion, add 4.7u at VCC pin	Add PC200 as 4.7u_0805	MP

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2006.09.11>	1		Dseign issue (Lost VRAM RST pin)	20, 22	Add DRAM_RST# from VGA to VRAM	0.2
	2		Dseign issue (LVDS channel error)	19	Swapped LVDS upper and lower channel	0.2
	3		Dseign issue (HSYNC & VSYNC error)	19	Swapped VSYNC & HSYNC each other	0.2
	4		isolate ESD to CPU core via USB and 1394 conn's pin	34	Add R4, R73 and R56	0.2
	5		Follow ATI design suggestion for VDDR4, VDDR5	21	change and reserve two jopens for +1.8VS and +3VS power rails	0.2
	6		Follow ATI design suggestion for DPLL_VDDC	21	delete R1892	0.2
	7		follow ATI power sequence	40	Add +1.25VS, +3VS, +5VS and VDD_MEM18 delay circuits.	0.2
<2006.10.14>	1		RGB signal EA failed and CRT display garbage	16, 19	Change CRT circuit from MAX9511 to RLC circuit.	0.3
	2		RGB signal EA failed and CRT display garbage	39	Change CRT circuit from MAX9511 to RLC circuit. Add Q/Switch circuit.	0.3
	3		follow ATI power sequence	21	install R1898 aand C1605, uninstall R1897	0.3
	4		Increase VDD_MEM18 via holes	23	VDD_MEM18 no power noise, remove 1206 size resister.	0.3
	5		Cancel Kill switch function on Chimay	28	uninstall JP53, R1906, R1736 and Q136	0.3
	6		change 1394 bus route on board	31	re-define JP13 pins' assignment	0.3
	7		implement one 4MB SPI chip	36	add R1794, R1795, R1924	0.3
	8		implement 30pins KBC connector	38	re-define KBC connector JP6 pins assignment	0.3
<2006.11.20>	1		HP request, support Penryn CPU	4	Add R23, R34	0.4
	2		For Intel ES2 Crestline thermtrip pin.	7	Add R2	0.4
	3		For EMI request enable 27MHz_SSC	15	install R1687	0.4
	4		For Intel ES2 NB 800/667M Hz issue	15	Add CLRP4, CLRP5 to select FSB speed.	0.4
	5		For RTC Accuracy fail to change	25	Change C528, C516 to 15pf	0.4
	6		For detect CPU and system power saving	26	Add some components	0.4
	7		Solve auto-turn on	26	install R1590 pull up to +3valw, uninstall R1727	0.4
	8		Enable ACBS (power management for NIC)	29	install Q102, uninstall R1612, Q104, Q105	0.4
	9		Enable ACBS (power management for NIC)	30	Change R1639 value to 1.87k	0.4

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2006.11.20>	10		Add Energy Star for CPU schematics	41	reserve R1931, R1934, R1933, C1622, U88, U90, R43, R46, R52, R53, C1623, D80	0.4
	11		Enable ACBS (power management for NIC)	41	Change R1732 pin2 from +3VM_Lan to +3VM	0.4
	12		HP request	38	MDC power change to +3vs	0.4
	13		Follow ATI power sequence	40	Install D77, C1617, change R1919 to 10K	0.4
<2007.01.25>	1		For HP request	40	Add R1940 and pull up +3valw	0.5
	2		For 3VL/VCC1_PWRGD glitch change	41	Add U5C and R1939 pull down	0.5
	3		For KBC VCC2 connection to 3VS	37	install R1646, C75	0.5
	4		For HP request	25	Add Q144 and R1935 instead of D75	0.5
	5		For HP request to install BGA CRACK components	27 12		0.5
	6		For solving Power wireset interfere Fan	38	change JP20 connector Footprint	0.5
	7		For Intel Crestline thermtrip shutdowm	7	Reserve 0.1uf *1 for THERMTRIP#	0.5
	8		For possible Leak during ACBS on PREP# signal	26	Change pull up to +3valw	0.5
	9		For HP request to change Line-in BOM	32	R370, R369 change to 6.04k, R374, R375 change to 2.00k	0.5
	10		For SIM connector supply chain	31	SIM connector footprint change	0.5
	11		For LMV331 supply chain, change to LMV393	41	change U76 & U86 to U91	0.5
	12		For EMI changes for VGA CRT	16	Install C310,C313,C314,R542,R543,R544	0.5
	13		For EMI changes for LED_LAN_DOCK	33	Add R1805,R1806	0.5
	14		For HP request, change R1780.1 to UIM_PWR	31	change R1780.1 to UIM_PWR	0.5
	15		For Intel NIC crystal design	29	Add R1936 30ohm value	0.5
	16		For G-Sensor LED	26	HDD_HALTLED (R15) pull down	0.5
	17		For Intel new design	26	Remove pull ups for STP_PCI# and STP_CPU# uninstall R1581, R1580	0.5
	18		For HP request	36	Add CLRP6 for SPI ROM	0.5
	19		For VGA wavy isse	17	Change C586 to 10uf_1206, add C1629 10uf_1206	0.5

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.02.14> 1		Add FP power supply circuit for Vista	41	reserve R1931, R1934, R1933, C1622, U88, U90, R43, R46, R52, R53, C1623, D80	0.4
2		Enable ACBS (power management for NIC)	41	Change R1732 pin2 from +3VM_Lan to +3VM	0.4
3		HP request	38	MDC power change to +3vs	0.4
4		Follow ATI power sequence	40	Install D77, C1617, change R1919 to 10K	0.4
5		For HP request	40	Add R1940 and pull up +3valw	0.5
6		For 3VL/VCC1_PWRGD glitch change	41	Add U5C and R1939 pull down	0.5
7		For KBC VCC2 connection to 3VS	37	install R1646, C75	0.5
8		For HP request	25	Add Q144 and R1935 instead of D75	0.5
		For HP request to install BGA CRACK components	27 12		0.5
		For solving Power wireset interfere Fan	38	change JP20 connector Footprint	0.5
		For Intel Crestline thermtrip shutdowm	7	Reserve 0.1uf *1 for THERMTRIP#	0.5
		For possible Leak during ACBS on PREP# signal	26	Change pull up to +3valw	0.5
9		For HP request to change Line-in BOM	32	R370, R369 change to 6.04k, R374, R375 change to 2.00k	0.5
10		For SIM connector supply chain	31	SIM connector footprint change	0.5
11		For LMV331 supply chain, change to LMV393	41	change U76 & U86 to U91	0.5
12		For EMI changes for VGA CRT	16	Install C310,C313,C314,R542,R543,R544	0.5
13		For EMI changes for LED_LAN_DOCK	33	Add R1805,R1806	0.5
14		For HP request, change R1780.1 to UIM_PWR	31	change R1780.1 to UIM_PWR	0.5
15		For Intel NIC crystal design	29	Add R1936 30ohm value	0.5
16		For G-Sensor LED	26	HDD_HALTLED (R15) pull down	0.5
17		For Intel new design	26	Remove pull ups for STP_PCI# and STP_CPU# uninstall R1581, R1580	0.5
18		For HP request	36	Add CLRP6 for SPI ROM	0.5
19		For VGA wavy isse	17	Change C586 to 10uf_1206, add C1629 10uf_1206	0.5

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<2007.08.02>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Solve VGA can not thermal shutdown and KB dissolve	4	Add R229 (non-install) and contact to THERM#_VGA	1A
2		prevent Cap crack to change Cap size	17	C1629 & C586 size change from 1206 to 0805	1A
3		Solve VGA can not thermal shutdown and KB dissolve	23	Add R1906 (non-install) and R1896 install Add Q30 & Q31	1A
4		Prevent GPIO33 leakage	25	Change Q144 to CHP202U_SC70	1A
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