

Compal Confidential

Lotus M/B Schematics Document

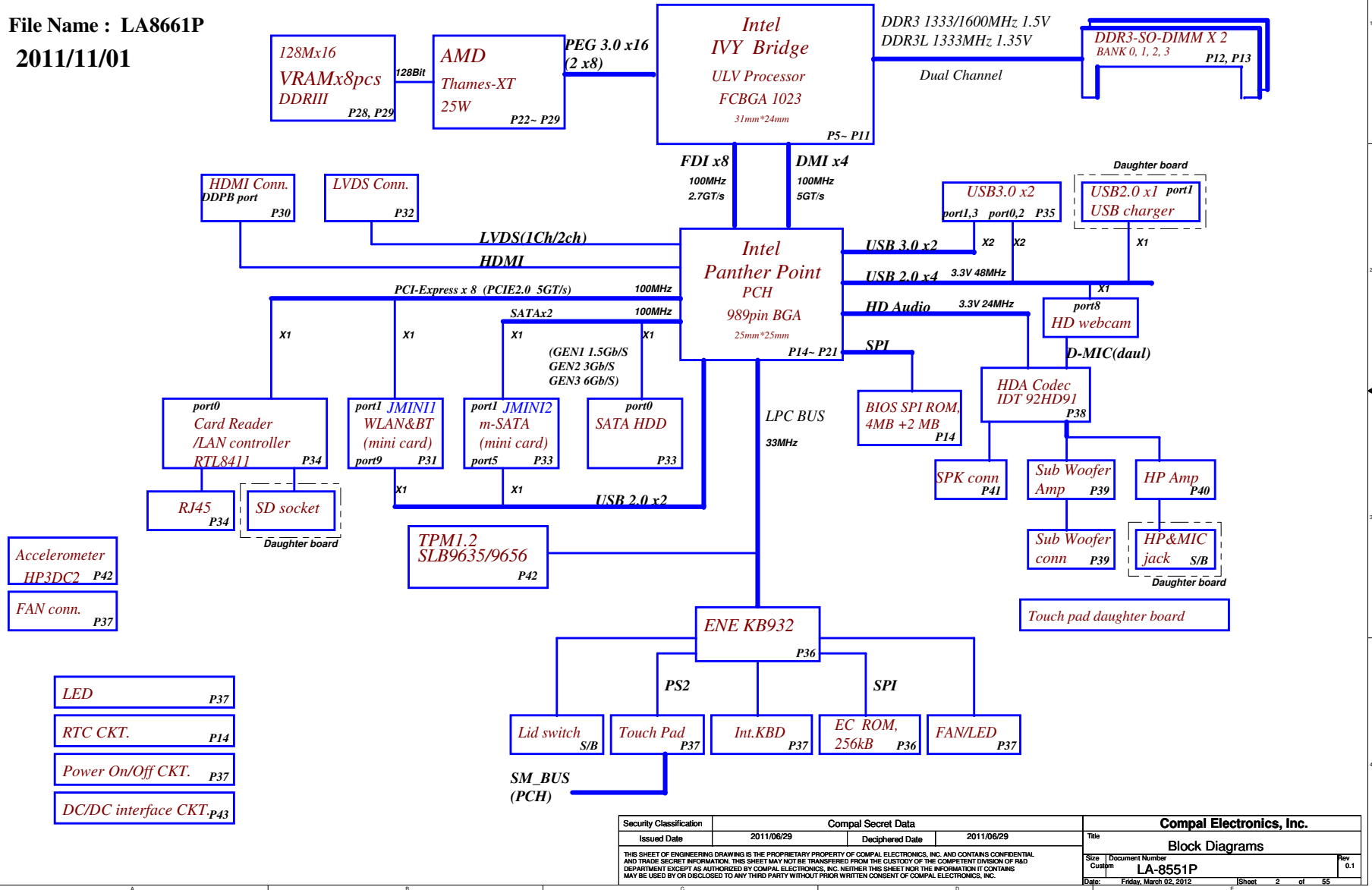
14": Elise; 15.6" Exige

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2011/10/27
Version 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title		
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				Size	Document Number	Rev
				Custom	LA-8551P	0.1
				Date:	Friday, March 02, 2012	Sheet 1 of 55

2011/11/01



QAU30/50 (LA-8661P Ver:0.1)

Volatge Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+SVALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+3VALW_EC	+3VALW always to KBC	ON	ON	ON
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+SVALW	+SVALWP to +SVALW power rail	ON	ON	ON
+5V_PCH	+SVALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON
+5VS	+SVALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+VGA_CORE	GPU power	PX	OFF	OFF
+3VGS	GPU power	PX	OFF	OFF
+1.8VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF
+1.0VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	SATA, JHDD1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

BY SKU			
TPM	9635@	9656@	
CPU	CPUUMA1@	CPUUMA2@	CPUDIS@
VRAM	X76@	H2G@	M2G@ S2G@

Option	@	CONN@	USB30@	PX@	UMA@	DIS@	THA@
UMA	X	X	V	X	V	X	X
DIS	X	X	V	V	X	V	V

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CRK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CRK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CRK2 EC_SMB_DA2	KB930							V		V	V
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	PCIE LAN CARD READER	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	mini WLAN	CLKOUTFLEX2	None
	CLKOUT_PCIE2	None	CLKOUTFLEX3	DGPU_PRSENT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :
 : means Digital Ground
 : means Analog Ground

Project ID	30UMA@	30DIS@	50UMA@	50DIS@
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PCB	LA-8661P	LA-8662P
	PX@	UMA@

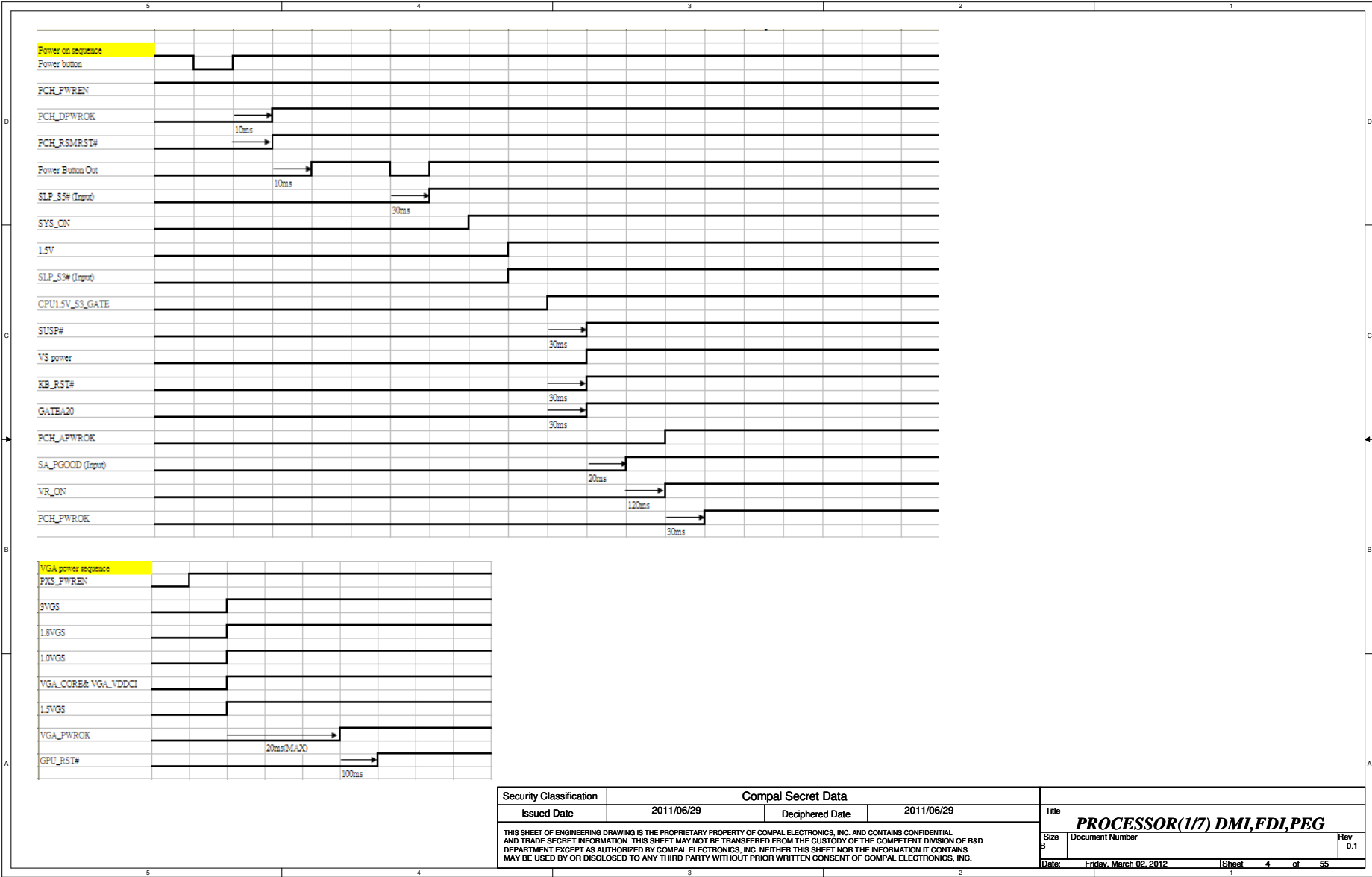
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (left Side)
		1	USB2.0 (right Side)
		2	USB2.0 (left Side)
	UHCI1	3	None
		4	None
		5	None
		6	None
EHCI2	UHCI3	7	None
		8	Camera
	UHCI4	9	Mini Card(WLAN& BT)
		10	None
		11	None
		12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	USB3.0 (left Side)
	4	None

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				Document Number
				LA-8661P
				Date: Friday, March 02, 2012
				Sheet 3 of 56

Rev 0.1



UCPU1 CPUIDIS01@
I5-2467M CPU
SA00004X000

UCPU1 CPUIDIS02@
I5-2367M CPU
SA000051H20

UCPU1 CPUIDIS03@
I5-2367M CPU
SA000051H20

UCPU1 CPUIDIS04@
I5-3317U CPU
SA00005K600

UCPU1 CPUUMA3@
I5-2367M CPU
SA000051H20

UCPU1 CPUUMA4@
17W 1.7GHz GT2 ES2 QBP7
SA00005B010

UCPU1 CPUUMA5@
17W 1.7GHz no only ES2 QBTQ
SA00005B020

UCPU1 CPUUMA1@
17W 1.5GHz GT2 ES2 QBP8
SA00005AZ10

UCPU1 CPUUMA2@
17W 1.5GHz no only ES2 QBTQ
SA00005AZ20

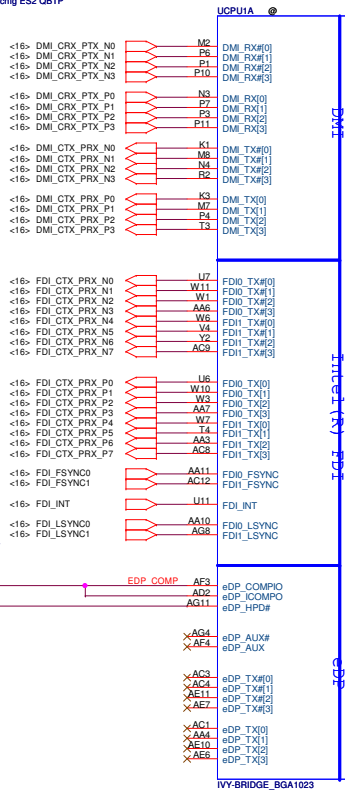
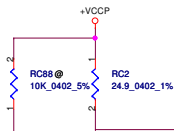
Sandy Bridge:
Intel Core I5-2467M: SA00004X000 (4619HY32L01)

Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QBTQ: SA00005AZ20 (4619HZ32L02)

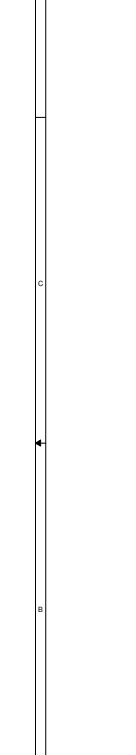
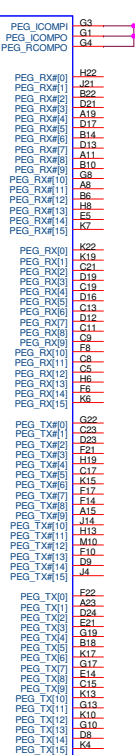
PEG_ICOMPI and RCOMPO signals should be
shorted and routed
with - max length = 500 mils - typical
impedance = 43 mohms
PEG_ICOMPO signals should be routed with -
max length = 500 mils
- typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals
should be shorted near balls
and routed with typical
impedance <25 mohms

NOTE: eDP_COMPIO and eDP_ICOMPO
should not be left floating even if Internal
Graphic is disabled since they are shared
with other interfaces

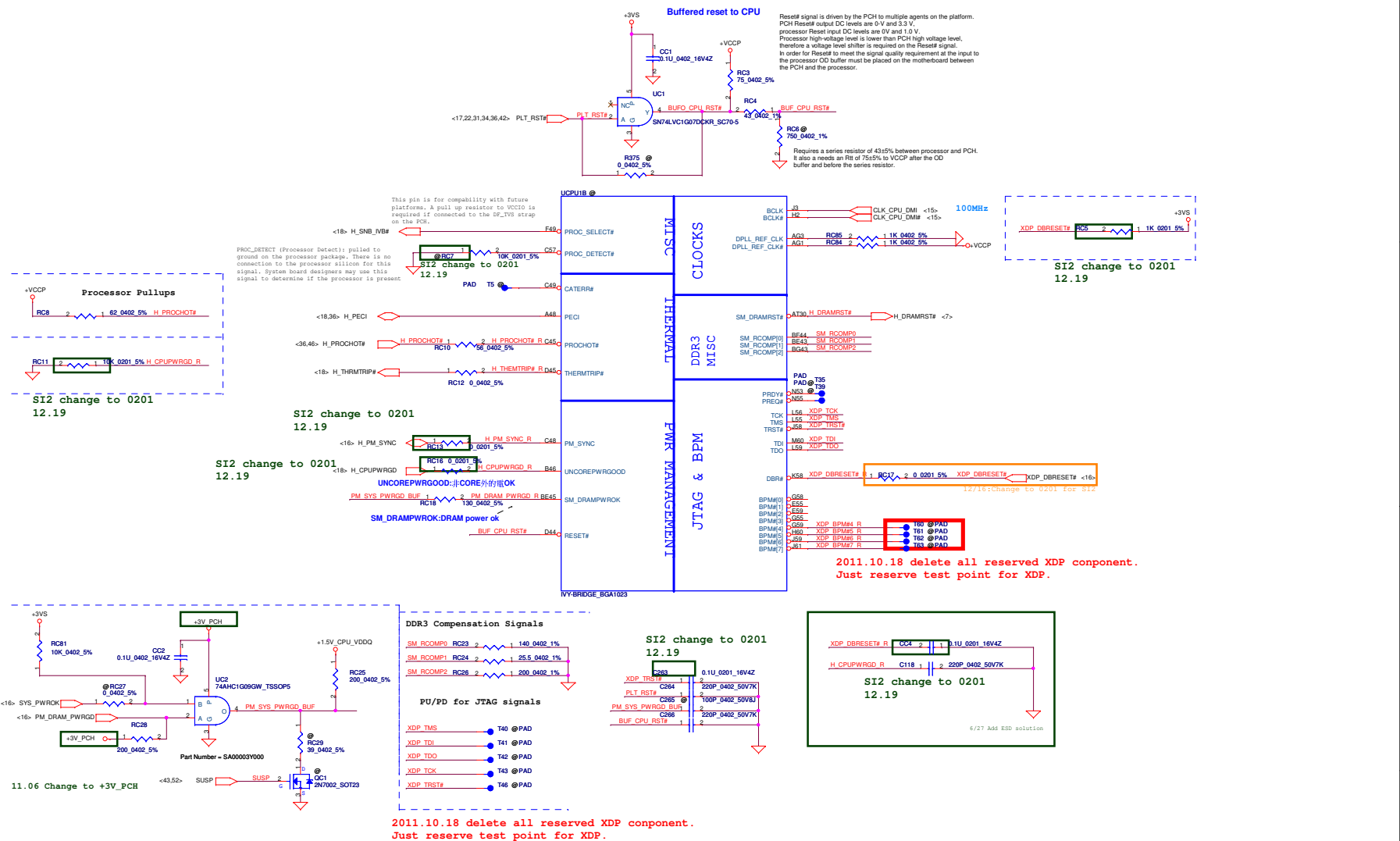


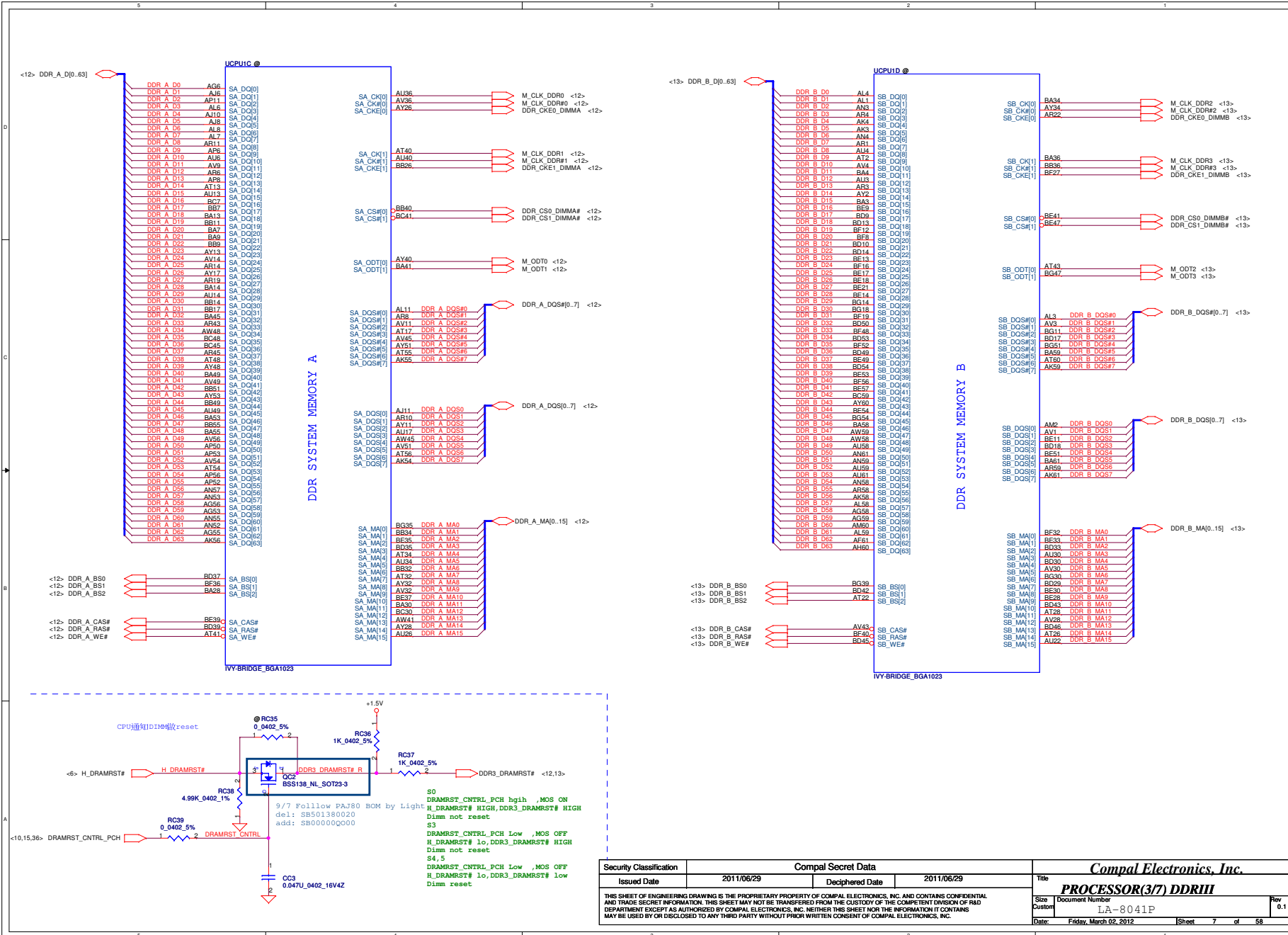
PCI EXPRES -- GRAPHICS



10/05 Change to 0.22uF.
Typ- suggest 220nF. The change in AC capacitor
value from 180nF to 265nF is to enable
compatibility with future platforms having PCIe
Gen3 (8GT/s)

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				Custom	LA-8661P
				Date:	Friday, March 02, 2012
				Sheet	5 of 58
				Rev	0.1

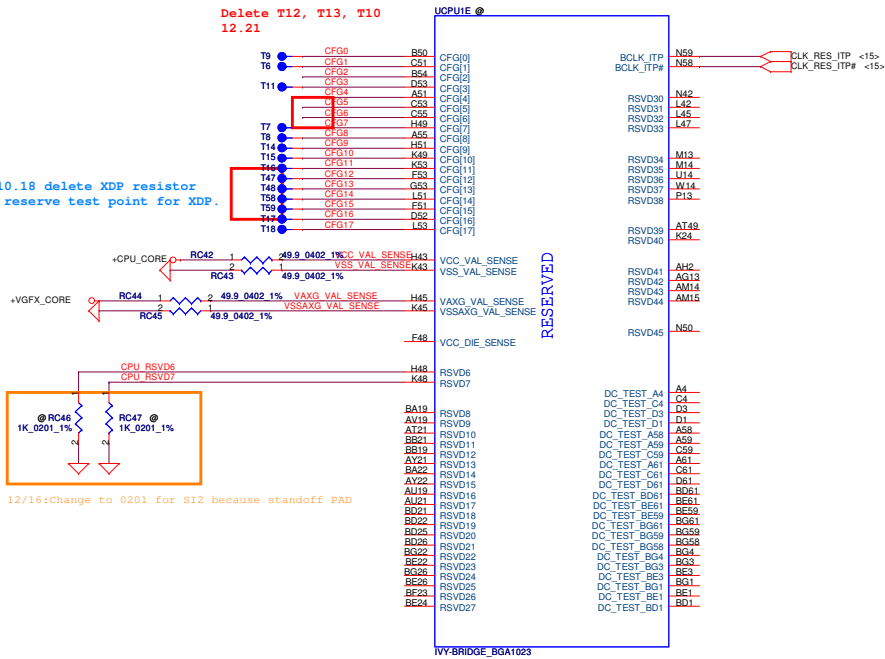




Change to part G.

Delete T12, T13, T10
12.21

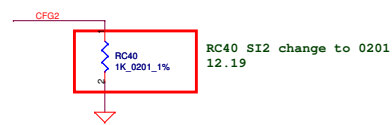
2011.10.18 delete XDP resistor
just reserve test point for XDP.



CFG Straps for Processor

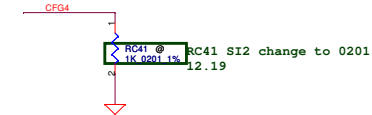
PEG bus is reversed, need to PD.

11.01



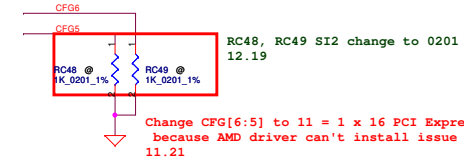
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	---



Display Port Presence Strap

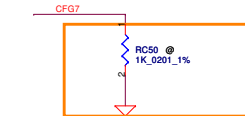
CFG4	★ 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
------	---



PCIe Port Bifurcation Straps

CFG[6:5]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express ★
----------	---

12/16: Change to 0201 for SI2 because standoff PAD



PEG DEFER TRAINING

CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	--

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				Custom	LA-8661P
				Date	Friday, March 02, 2012
				Sheet	6 of 58
				Rev	0.1

POWER

UCPU1F

+CPU_CORE

- A26 VCCQ[1]
- A29 VCCQ[2]
- A31 VCCQ[3]
- A34 VCCQ[4]
- A35 VCCQ[5]
- A38 VCCQ[6]
- A39 VCCQ[8]
- A42 VCCQ[9]
- C26 VCCQ[10]
- C27 VCCQ[11]
- C32 VCCQ[12]
- C34 VCCQ[13]
- C37 VCCQ[14]
- C39 VCCQ[15]
- D42 VCCQ[16]
- D32 VCCQ[17]
- D34 VCCQ[18]
- D37 VCCQ[19]
- D39 VCCQ[20]
- D42 VCCQ[21]
- E26 VCCQ[22]
- E28 VCCQ[23]
- E32 VCCQ[24]
- E34 VCCQ[25]
- E37 VCCQ[26]
- F25 VCCQ[27]
- F26 VCCQ[28]
- F28 VCCQ[29]
- F32 VCCQ[30]
- F34 VCCQ[31]
- F37 VCCQ[32]
- F38 VCCQ[33]
- F42 VCCQ[34]
- H25 VCCQ[35]
- H26 VCCQ[36]
- H29 VCCQ[37]
- H32 VCCQ[38]
- H34 VCCQ[39]
- H35 VCCQ[40]
- H37 VCCQ[41]
- H38 VCCQ[42]
- H40 VCCQ[43]
- J25 VCCQ[44]
- J26 VCCQ[45]
- J28 VCCQ[46]
- J29 VCCQ[47]
- J32 VCCQ[48]
- J34 VCCQ[49]
- J35 VCCQ[50]
- J37 VCCQ[51]
- J40 VCCQ[52]
- J42 VCCQ[53]
- K26 VCCQ[54]
- K27 VCCQ[55]
- K29 VCCQ[56]
- K32 VCCQ[57]
- K34 VCCQ[58]
- K35 VCCQ[59]
- K37 VCCQ[60]
- K39 VCCQ[61]
- K42 VCCQ[62]
- L25 VCCQ[63]
- L28 VCCQ[64]
- L33 VCCQ[65]
- L36 VCCQ[66]
- L40 VCCQ[67]
- N26 VCCQ[68]
- N30 VCCQ[69]
- N34 VCCQ[70]
- N38 VCCQ[71]

CORE SUPPLY

PEG IO AND DDR IO

- VCCQ[1] AF46
- VCCQ[3] AG46
- VCCQ[4] AG50
- VCCQ[5] AG51
- VCCQ[6] AJ17
- VCCQ[7] AJ21
- VCCQ[8] AJ25
- VCCQ[9] AJ43
- VCCQ[10] AJ47
- VCCQ[11] AK50
- VCCQ[12] AK51
- VCCQ[13] AL14
- VCCQ[14] AL15
- VCCQ[15] AL16
- VCCQ[16] AL20
- VCCQ[17] AL22
- VCCQ[18] AL26
- VCCQ[19] AL45
- VCCQ[20] AL48
- VCCQ[21] AM16
- VCCQ[22] AM17
- VCCQ[23] AM21
- VCCQ[24] AM43
- VCCQ[25] AM47
- VCCQ[26] AN20
- VCCQ[27] AN42
- VCCQ[28] AN45
- VCCQ[29] AN48
- VCCQ[30] AA14
- VCCQ[31] AA15
- VCCQ[32] AB17
- VCCQ[33] AB20
- VCCQ[34] AC18
- VCCQ[35] AD16
- VCCQ[36] AD19
- VCCQ[37] AD21
- VCCQ[38] AE14
- VCCQ[39] AE15
- VCCQ[40] AE16
- VCCQ[41] AE18
- VCCQ[42] AE20
- VCCQ[43] AG15
- VCCQ[44] AG16
- VCCQ[45] AG17
- VCCQ[46] AG20
- VCCQ[47] AG21
- VCCQ[48] AJ14
- VCCQ[49] AJ15

+VCCP

+VCCP

+VCCP

+VCCP

+VCCP

+VCCP

+VCCP

+VCCP

+CPU CORE

VV-BRIDGE_BGA1023

BC22 VCCP_PWRCTRL_R 10K 0402 5%

choose low or high

RC53

+1.05VS_VCCPQ

AN22

RC54 0.0805_5%

CC73 10_0402_6.3V6K

CPU EDS descript as follow:
For Chief River platforms this pin
should not be used.

A44 H CPU_SVIDALRT#

B43 H CPU_SVIDCLK

C44 H CPU_SVIDA1

RC57 1 2 43 0402 1%

RC58 1 2 0 0402 5%

RC59 1 2 0 0402 5%

VR_SVID_ALRT# <54>

VR_SVID_CLK <54>

VR_SVID_DAT <54>

F43 VCCSENSE_R RC81 1 2 0 0402 5%

G43 VSSSENSE_R RC82 1 2 0 0402 5%

RC60 100_0402_1%

RC63 1 2 10_0402_1%

AN16 VCCIO_SENSE_R

AN17 VSS_SENSE_VCCIO

RC66 10_0402_1%

RC63 1 2 10_0402_1%

RC66 10_0402_1%

RC63 1 2 10_0402_1%

RC66 10_0402_1%

RC63 1 2 10_0402_1%

RC66 10_0402_1%

RC63 1 2 10_0402_1%

RC66 10_0402_1%

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RC63 1 2 10_0402_1%

RC66 10_0402_1%

RC63 1 2 10_0402_1%

RC66 10_0402_1%

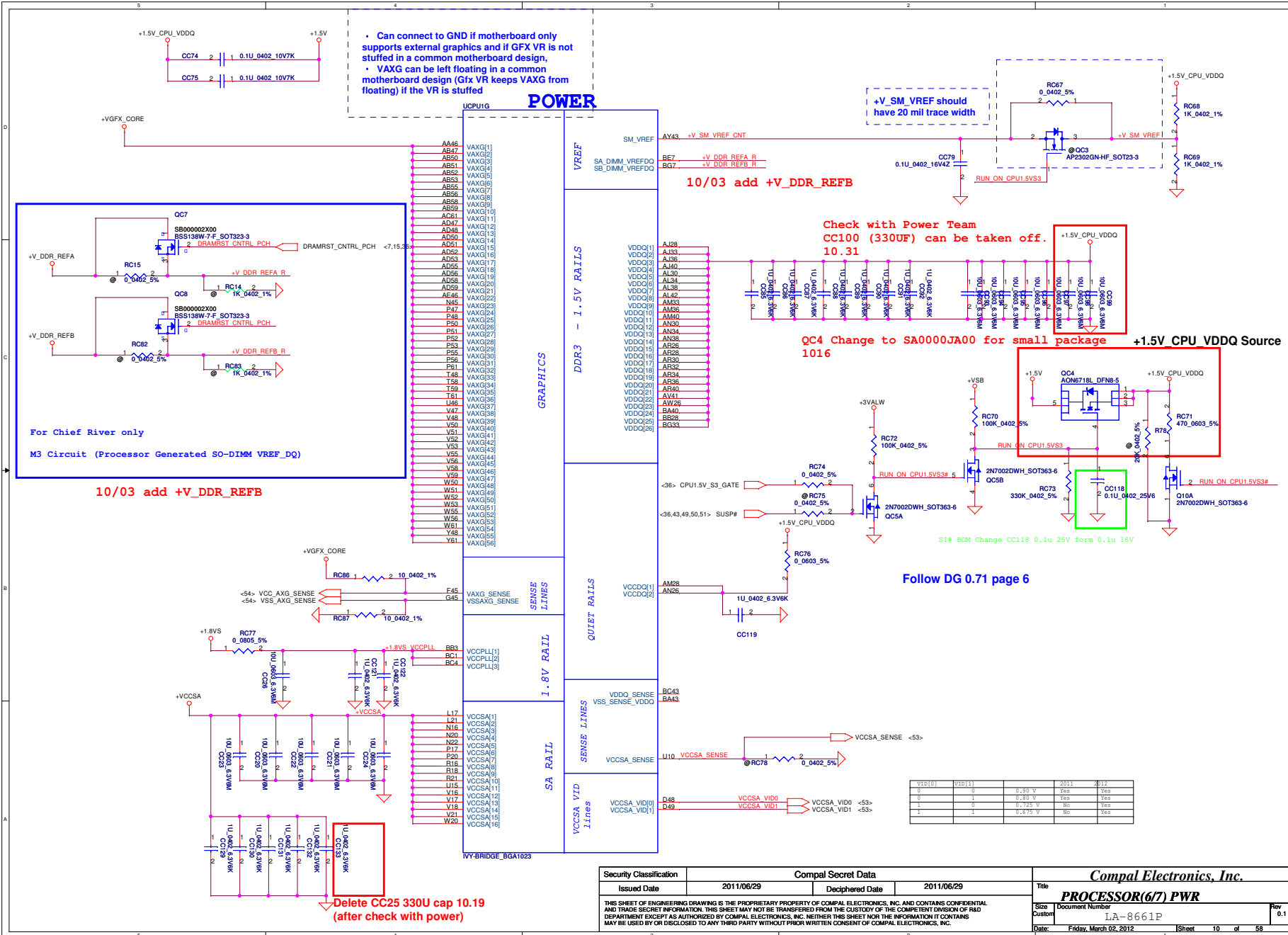
10/05 mount.
(follow check list)

Place the PU
resistors close to CPU

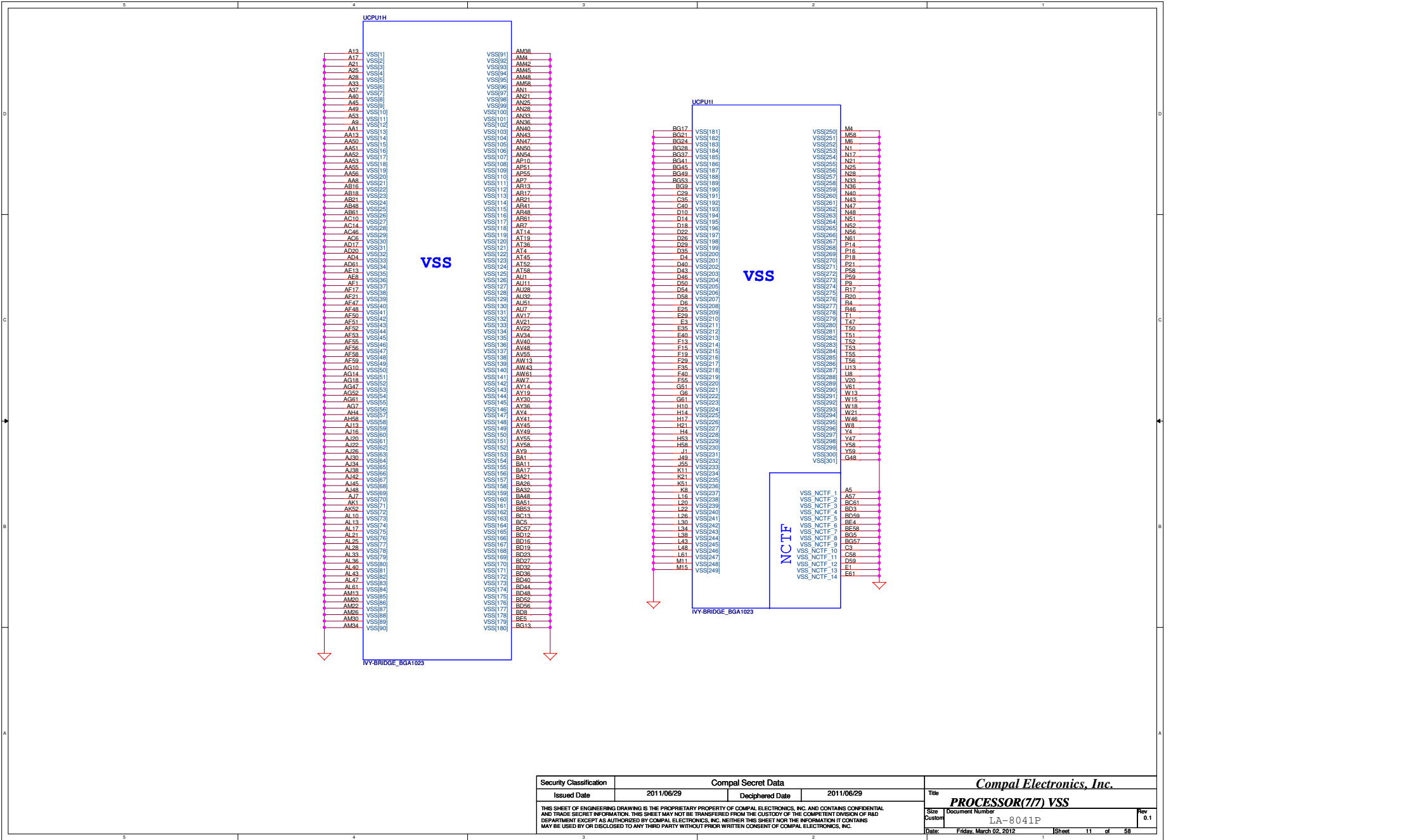
Place the PU
resistors close to VR

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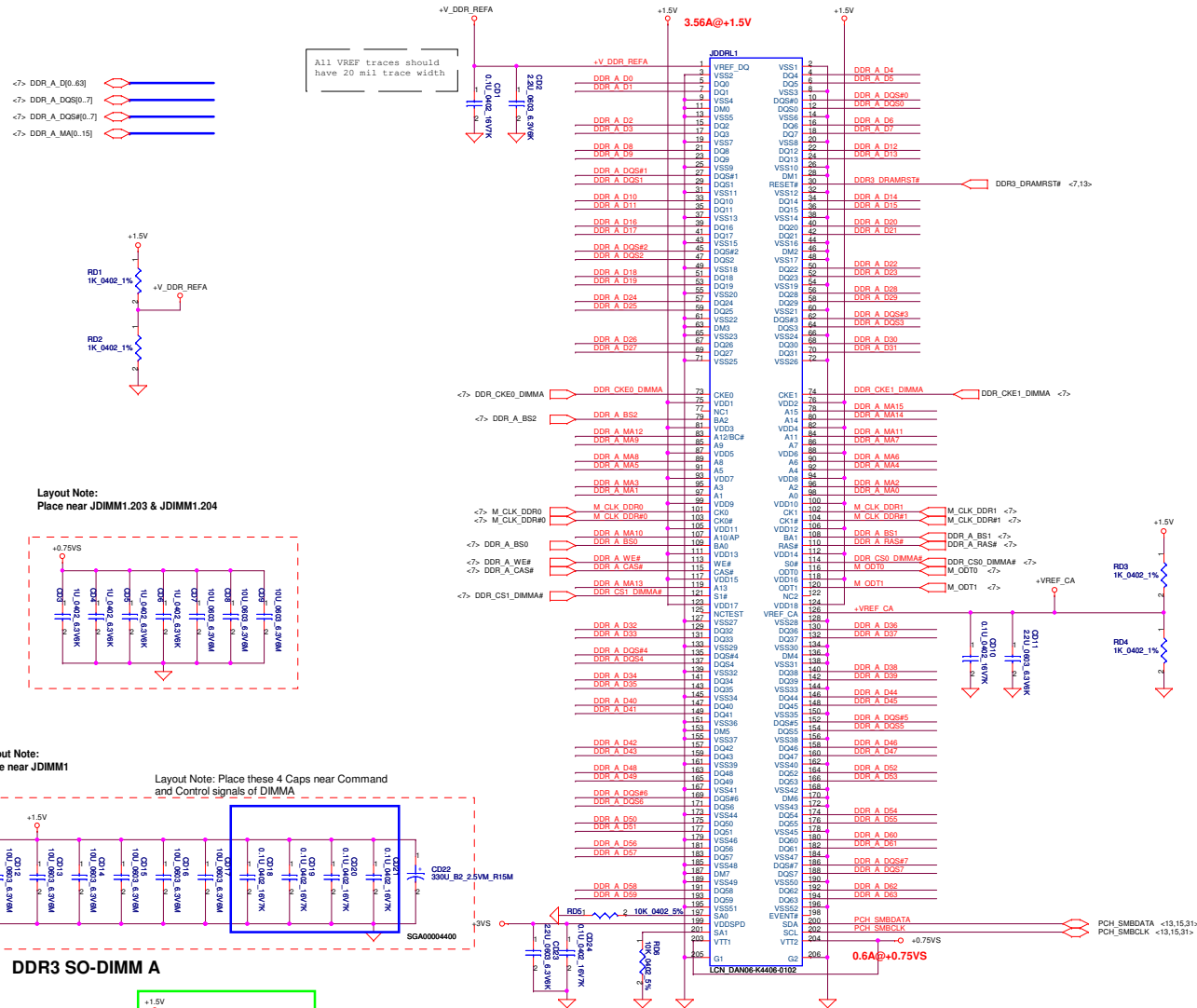
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PROCESSOR(S/7) PWR,BYPASS	
Size	Document Number
Custom	LA-8661P
Date	Friday, March 02, 2012
Sheet	9 of 58
Rev	0.1



VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes



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				Document Number	LA-8041P
				Date	Friday, March 02, 2012
				Sheet	11 of 58

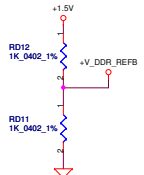
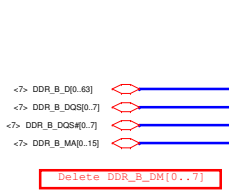
DDR3 SO-DIMM A

Standard
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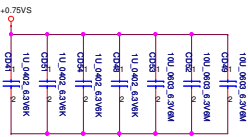
DDR3 SO-DIMM B

10/03 change to +V_DDR_REFB



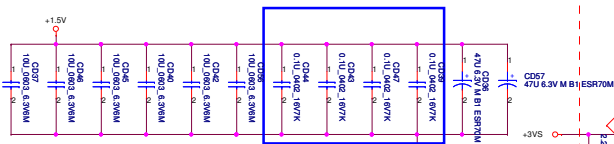
10/03 change to +V_DDR_REFB

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

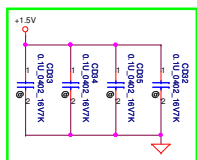


Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



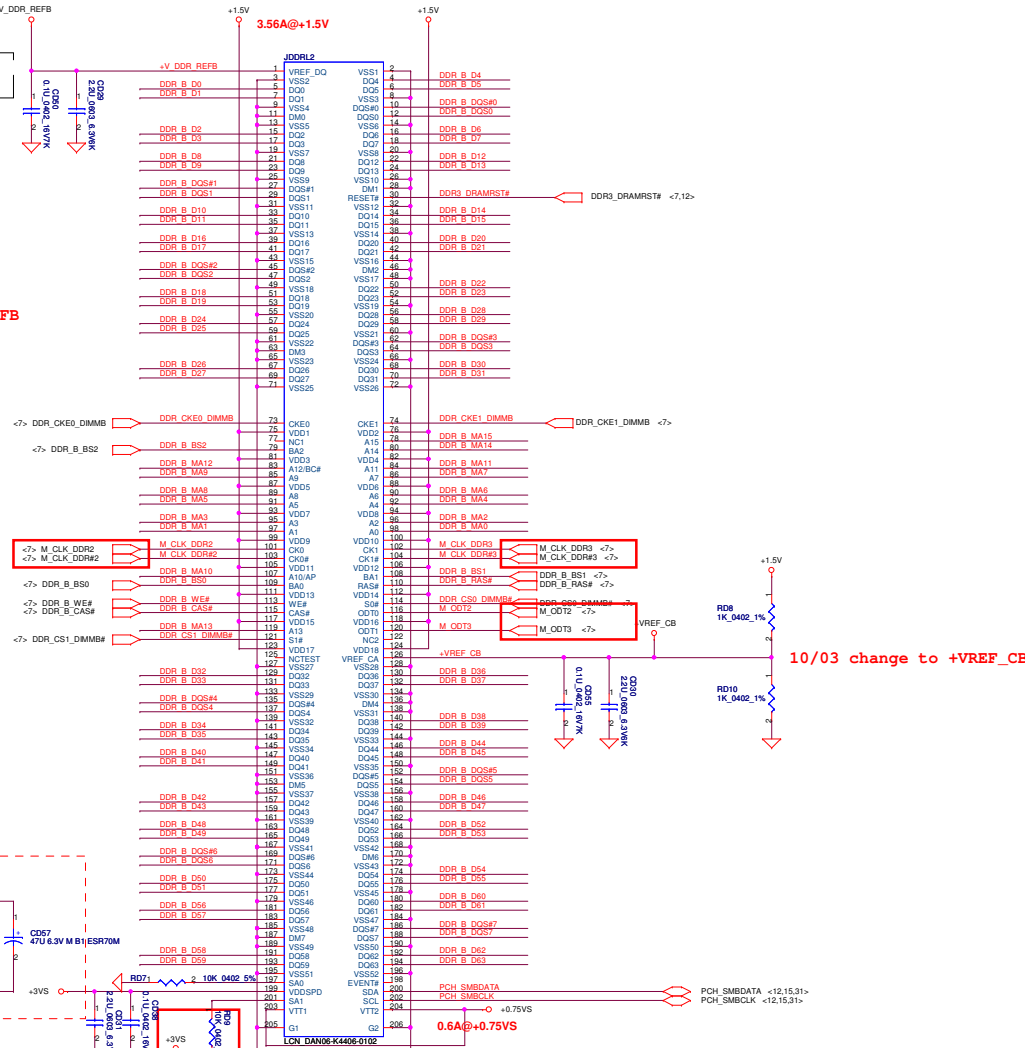
DDR3 SO-DIMM B



SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

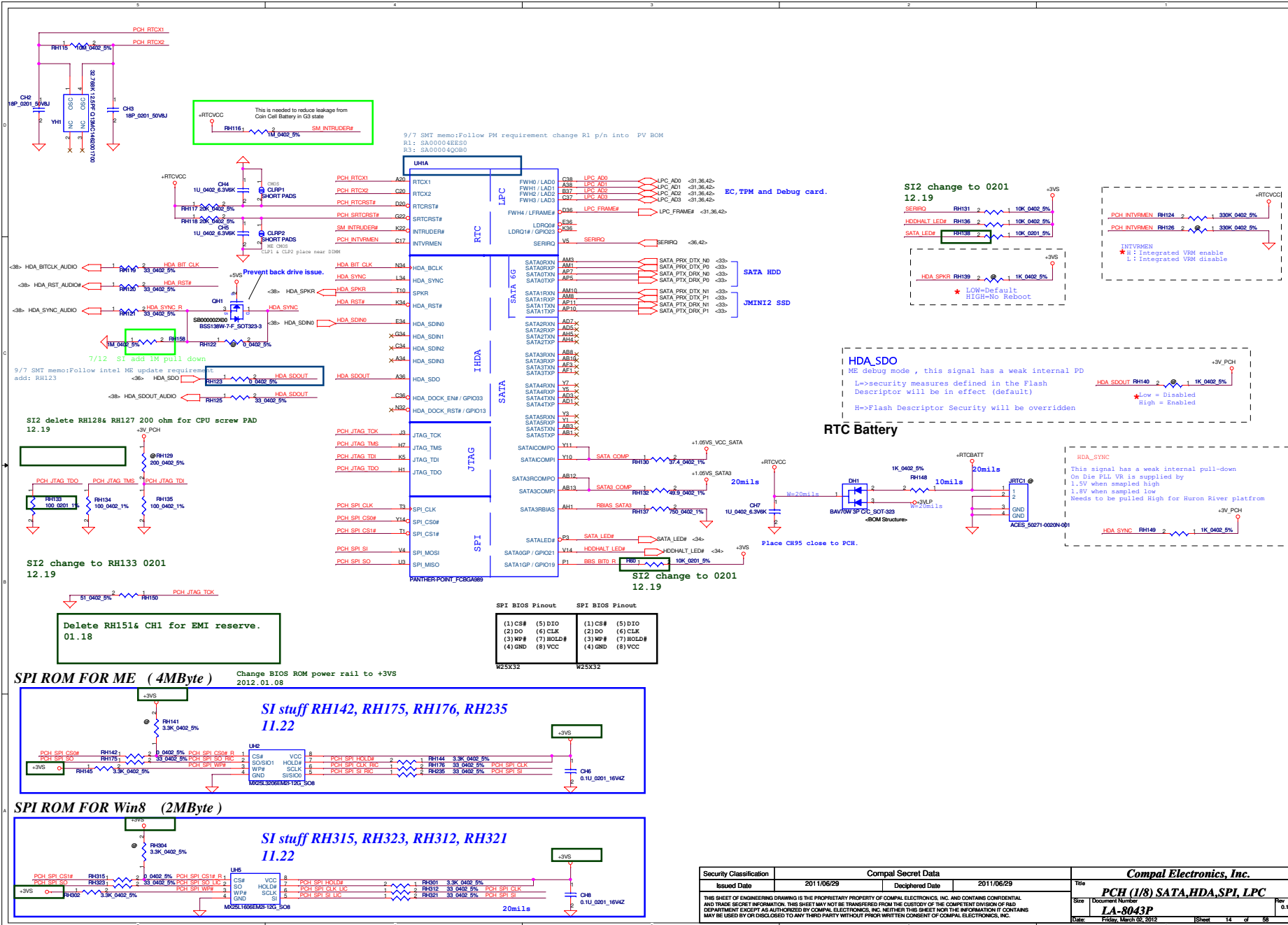
10/05 change to PH.

Standard
<Address(SA1,SA0):10>



10/03 change to +VREF_CB

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Size	Document Number	LA-8661P		Rev	0.1
Date	Friday, March 02, 2012	Sheet	13	of	58

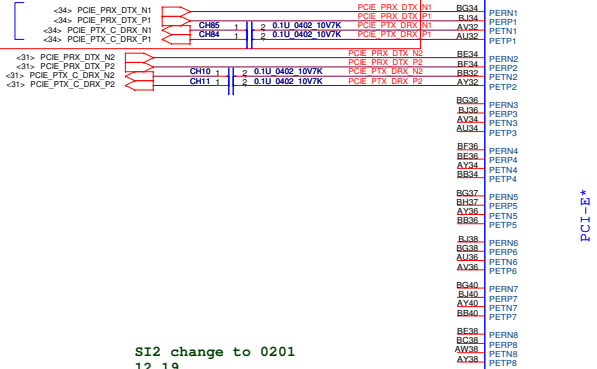


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title
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				LA-8043P
			Date:	Issued: 14 of 58

10/03 change to PCIe port1.

PCIE LAN/Card Reader

Mini card WLAN



SI2 change to 0201
12.19

PCIE LAN/Card Reader

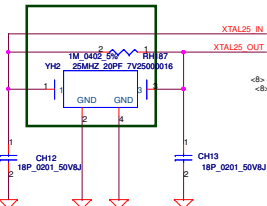
MiniWLAN

SI2 change to 0201
12.19

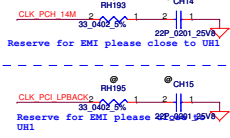
SI2 change to 0201
12.19

SI2 change to 0201
12.19

Change WL_OFF# to GPIO45 (pull-high) +3V_PCH
2012.01.04



SI2 YH2 change to SJ10000DJ00
12.19



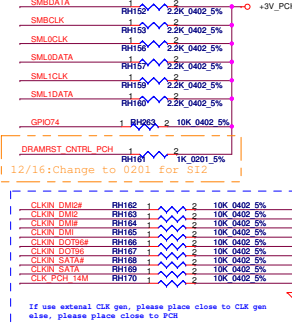
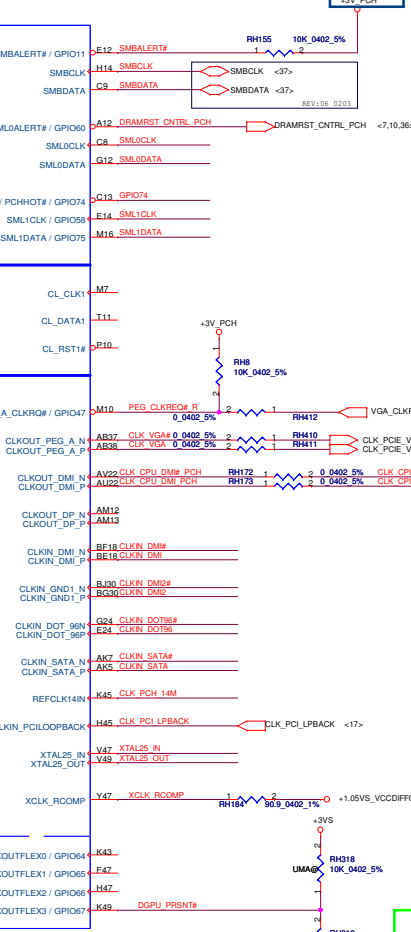
UHB

PCIE*

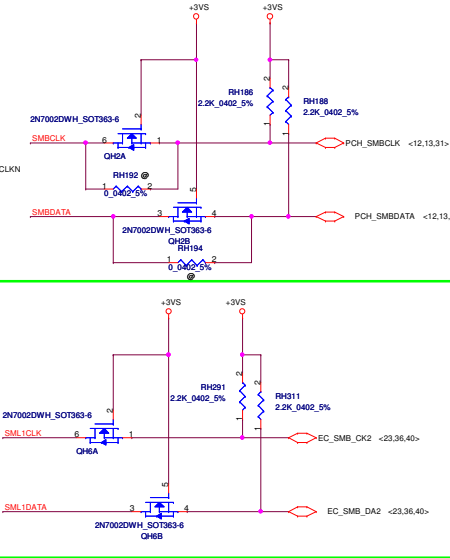
CLOCKS

Controller Link

CLOCKS

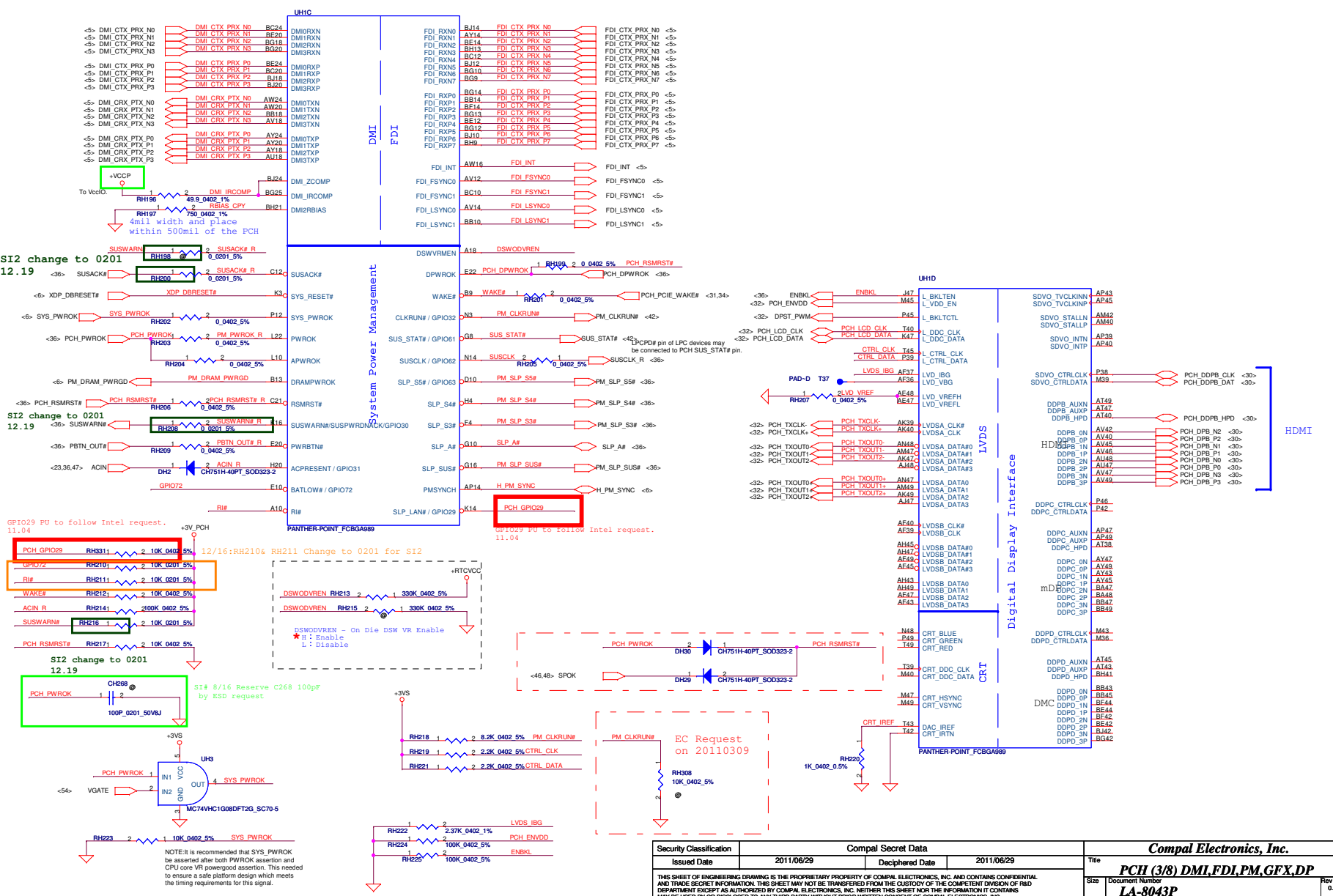


If use external CLK gen, please place close to CLK gen also, please place close to PCH

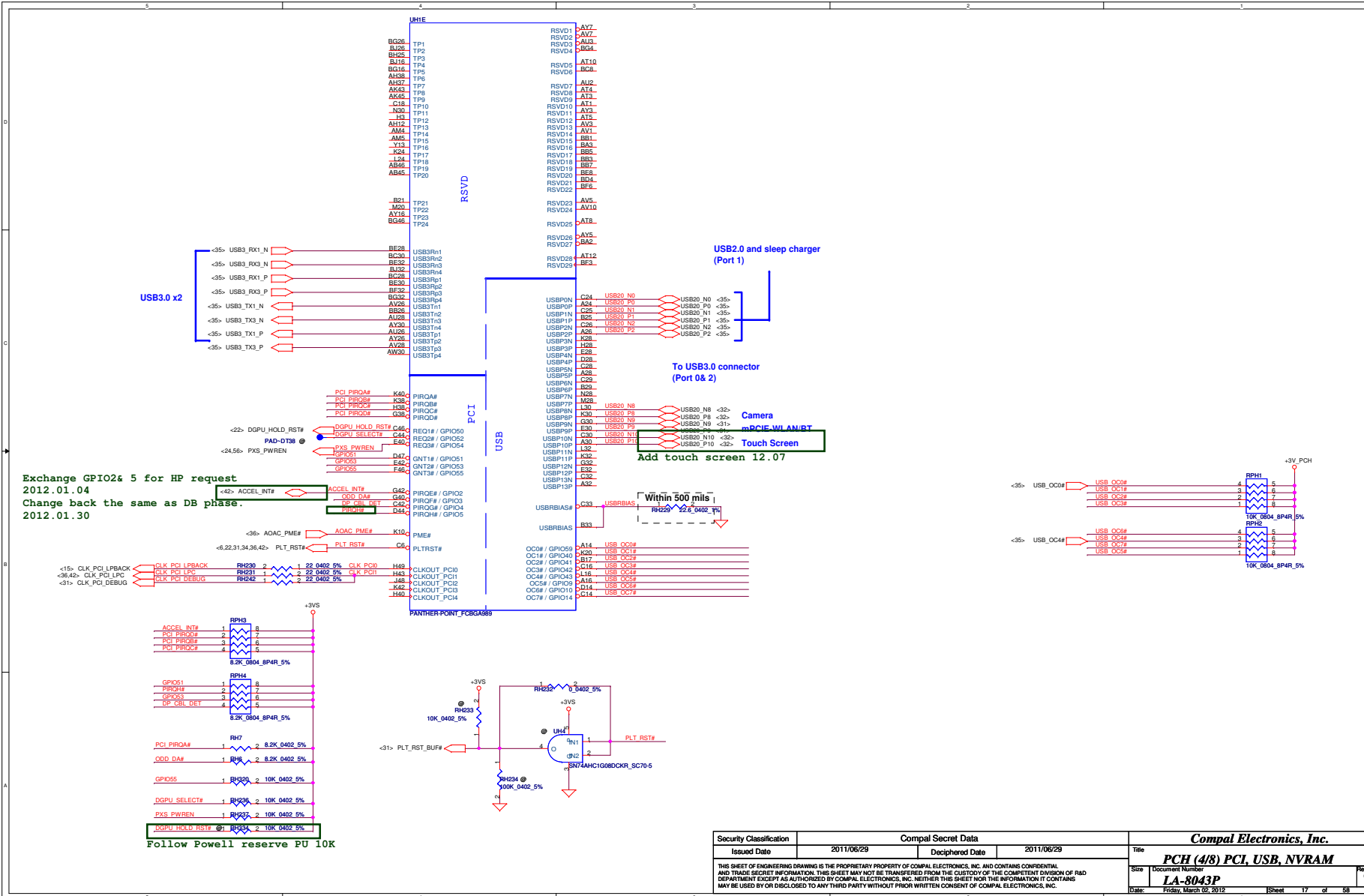


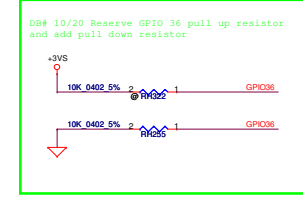
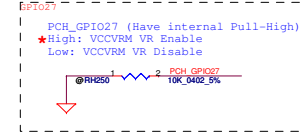
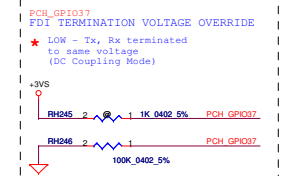
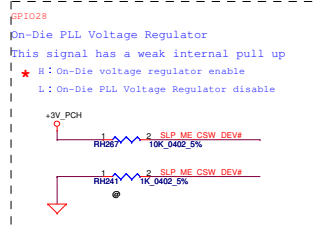
SI# 8/8 Add SML1CLK/SML1DATA for EC detect Thermal

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				LA-8043P	Rev 0.1
				Date	Friday, March 02, 2012
				ISheet	15 of 58

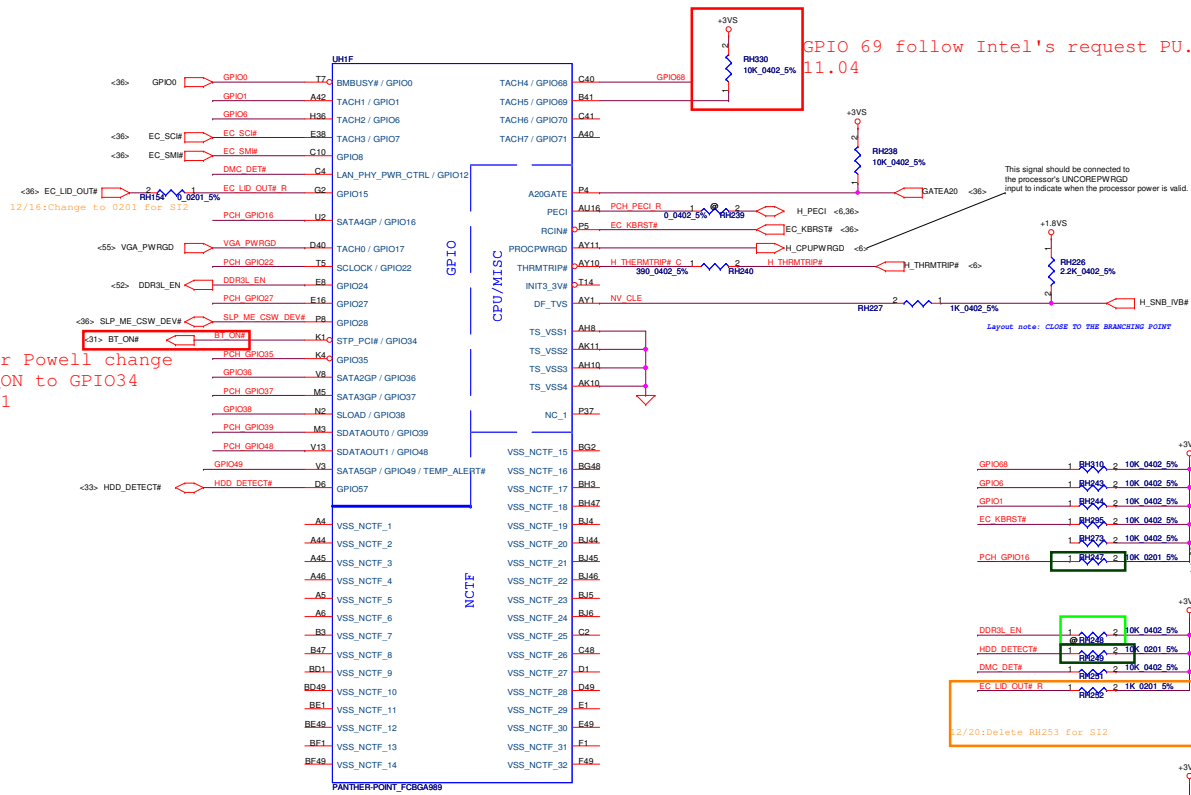


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	PCH (3/8) DMI,FDI,PM,GFX,DP	
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				LA-8043P	0.1
				Date	Sheet
				Friday, March 02, 2012	18 of 58





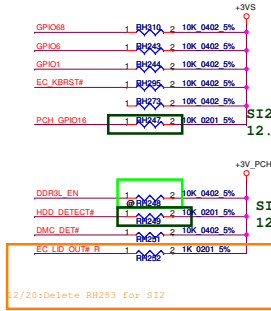
Refer Powell change
 BT_ON to GPIO34
 10.21



GPIO 69 follow Intel's request PU.
 11.04

This signal should be connected to the processor's UNCOREPWGRD input to indicate when the processor power is valid.

Layout note: CLOSE TO THE BRANCHING POINT



SI2 change to 0201
 12.19

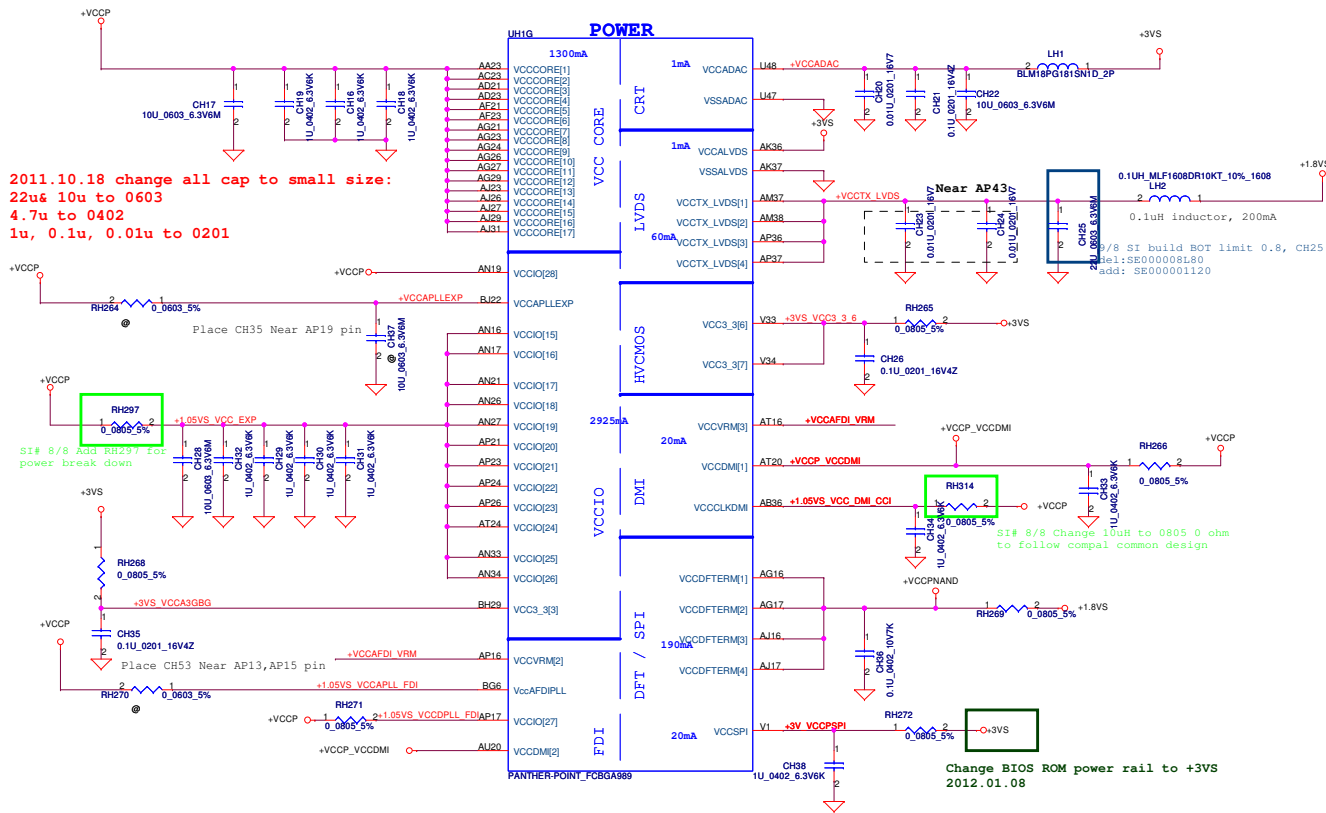
SI2 change to 0201
 12.19

SI2 change to 0201
 12.19

Refer Powell change
 BT_ON to GPIO34
 10.21

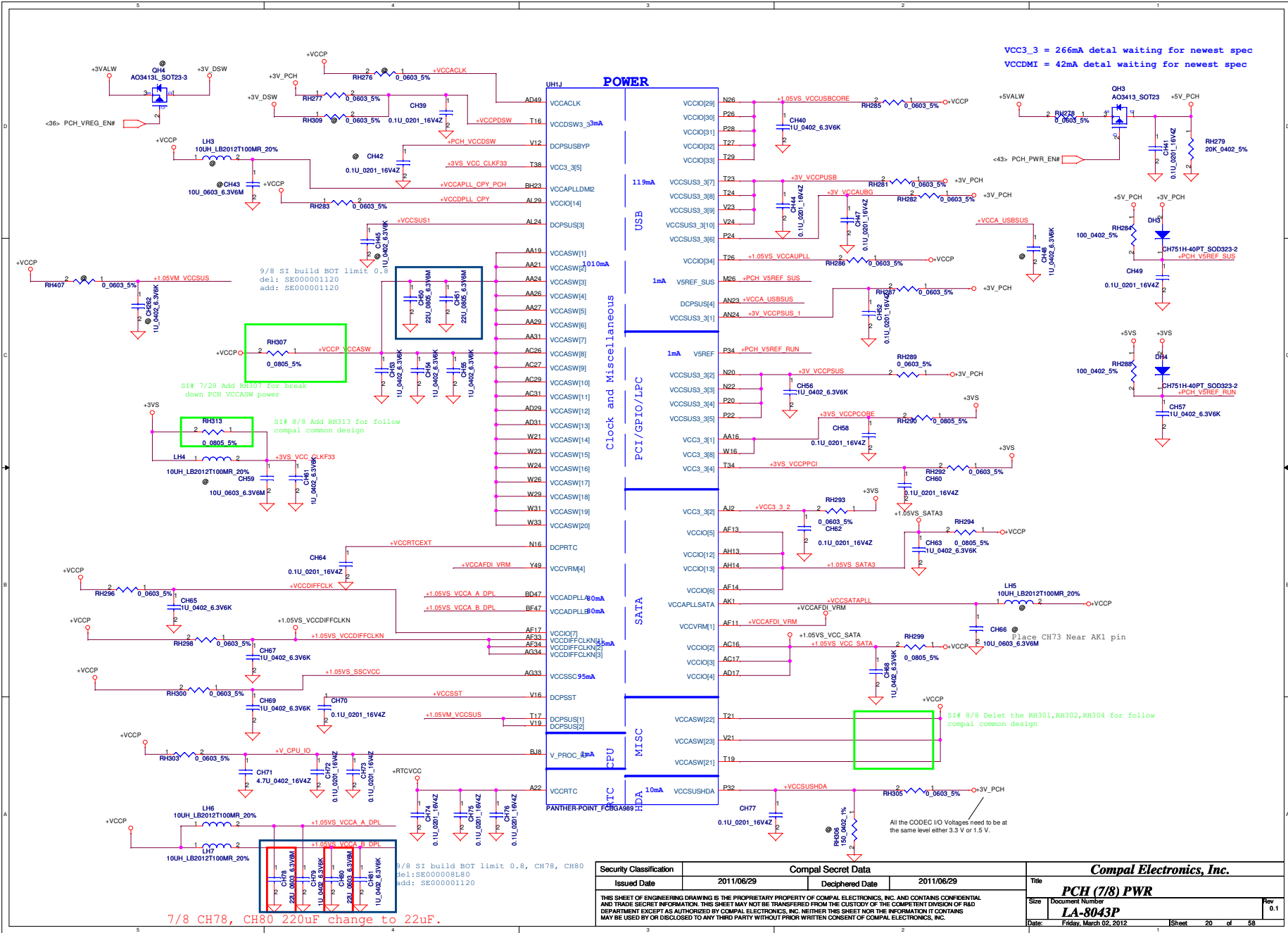
SI# 8/8 change PCH_WAN_RADIO_OFF#
 to PCH_GPIO15

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				Date	Salisbury, March 03, 2012
				Sheet	18 of 58



PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_IVDS	1.8	0.06

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				LA-8043P	Rev 0.1
				Date	Friday, March 02, 2012
				Sheet	19 of 58



7/8 CH78, CH80 220uF change to 22uF.

UHH		
H5	VSS[0]	
AA17	VSS[80]	AK38
AA2	VSS[81]	VSS[81]
AA5	VSS[82]	AK42
AA33	VSS[83]	AK46
AB11	VSS[84]	VSS[84]
AB14	VSS[85]	AL16
AB38	VSS[86]	AL17
AB4	VSS[87]	AL2
AB43	VSS[88]	AL21
AB5	VSS[89]	AL23
AB7	VSS[90]	AL26
AC19	VSS[91]	AL27
AC2	VSS[92]	AL31
AC21	VSS[93]	AL33
AC24	VSS[94]	AL34
AC33	VSS[95]	AL48
AC45	VSS[96]	AM11
AD10	VSS[97]	AM14
AD11	VSS[98]	AM36
AD12	VSS[99]	AM39
AD13	VSS[100]	AM43
AD19	VSS[101]	AM45
AD24	VSS[102]	AM46
AD26	VSS[103]	AM7
AD27	VSS[104]	AN2
AD33	VSS[105]	AN29
AD34	VSS[106]	AN3
AD36	VSS[107]	AN31
AD37	VSS[108]	AP12
AD38	VSS[109]	AP19
AD39	VSS[110]	AP28
AD4	VSS[111]	AP30
AD40	VSS[112]	AP32
AD42	VSS[113]	AP4
AD43	VSS[114]	AP38
AD45	VSS[115]	AP4
AD46	VSS[116]	AP42
AD5	VSS[117]	AP46
AD6	VSS[118]	AP5
AD8	VSS[119]	AR2
AE2	VSS[120]	AR46
AE3	VSS[121]	AT11
AE10	VSS[122]	AT13
AE12	VSS[123]	AT18
AE14	VSS[124]	AT22
AE16	VSS[125]	AT26
AE19	VSS[126]	AT28
AE24	VSS[127]	AT30
AE27	VSS[128]	AT32
AE28	VSS[129]	AT34
AE29	VSS[130]	AT39
AE31	VSS[131]	AL42
AE38	VSS[132]	AT46
AF4	VSS[133]	AT7
AF40	VSS[134]	AL24
AF5	VSS[135]	AL30
AF6	VSS[136]	AV16
AF7	VSS[137]	AV20
AF8	VSS[138]	AV24
AG2	VSS[139]	AV30
AG31	VSS[140]	AV38
AG46	VSS[141]	AV4
AH11	VSS[142]	AV43
AH3	VSS[143]	AV9
AH36	VSS[144]	AW14
AH39	VSS[145]	AW18
AH40	VSS[146]	AW2
AH42	VSS[147]	AW22
AH46	VSS[148]	AW28
AH7	VSS[149]	AW32
AJ19	VSS[150]	AW34
AJ21	VSS[151]	AW36
AJ24	VSS[152]	AW40
AJ33	VSS[153]	AW46
AJ34	VSS[154]	AV11
AK12	VSS[155]	AV12
AK3	VSS[156]	AV22
	VSS[157]	AY28
	VSS[158]	

PANTHER-POINT_FCBGA989

UHH		
AY4	VSS[159]	
AY42	VSS[160]	VSS[259]
AY46	VSS[161]	VSS[260]
AY8	VSS[162]	VSS[261]
B11	VSS[163]	VSS[262]
B15	VSS[164]	VSS[263]
B19	VSS[165]	VSS[264]
B23	VSS[166]	VSS[265]
B27	VSS[167]	VSS[266]
B31	VSS[168]	VSS[267]
B35	VSS[169]	VSS[268]
B39	VSS[170]	VSS[269]
B43	VSS[171]	VSS[270]
B47	VSS[172]	VSS[271]
B51	VSS[173]	VSS[272]
B55	VSS[174]	VSS[273]
B59	VSS[175]	VSS[274]
B63	VSS[176]	VSS[275]
B67	VSS[177]	VSS[276]
B71	VSS[178]	VSS[277]
B75	VSS[179]	VSS[278]
B79	VSS[180]	VSS[279]
B83	VSS[181]	VSS[280]
B87	VSS[182]	VSS[281]
B91	VSS[183]	VSS[282]
B95	VSS[184]	VSS[283]
B99	VSS[185]	VSS[284]
BC14	VSS[186]	VSS[285]
BC18	VSS[187]	VSS[286]
BC22	VSS[188]	VSS[287]
BC26	VSS[189]	VSS[288]
BC30	VSS[190]	VSS[289]
BC34	VSS[191]	VSS[290]
BC38	VSS[192]	VSS[291]
BC42	VSS[193]	VSS[292]
BC46	VSS[194]	VSS[293]
BD46	VSS[195]	VSS[294]
BD50	VSS[196]	VSS[295]
BD54	VSS[197]	VSS[296]
BD58	VSS[198]	VSS[297]
BD62	VSS[199]	VSS[298]
BD66	VSS[200]	VSS[299]
BD70	VSS[201]	VSS[300]
BD74	VSS[202]	VSS[301]
BD78	VSS[203]	VSS[302]
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BD118	VSS[213]	VSS[312]
BD122	VSS[214]	VSS[313]
BD126	VSS[215]	VSS[314]
BD130	VSS[216]	VSS[315]
BD134	VSS[217]	VSS[316]
BD138	VSS[218]	VSS[317]
BD142	VSS[219]	VSS[318]
BD146	VSS[220]	VSS[319]
BD150	VSS[221]	VSS[320]
BD154	VSS[222]	VSS[321]
BD158	VSS[223]	VSS[322]
BD162	VSS[224]	VSS[323]
BD166	VSS[225]	VSS[324]
BD170	VSS[226]	VSS[325]
BD174	VSS[227]	VSS[326]
BD178	VSS[228]	VSS[327]
BD182	VSS[229]	VSS[328]
BD186	VSS[230]	VSS[329]
BD190	VSS[231]	VSS[330]
BD194	VSS[232]	VSS[331]
BD198	VSS[233]	VSS[332]
BD202	VSS[234]	VSS[333]
BD206	VSS[235]	VSS[334]
BD210	VSS[236]	VSS[335]
BD214	VSS[237]	VSS[336]
BD218	VSS[238]	VSS[337]
BD222	VSS[239]	VSS[338]
BD226	VSS[240]	VSS[339]
BD230	VSS[241]	VSS[340]
BD234	VSS[242]	VSS[341]
BD238	VSS[243]	VSS[342]
BD242	VSS[244]	VSS[343]
BD246	VSS[245]	VSS[344]
BD250	VSS[246]	VSS[345]
BD254	VSS[247]	VSS[346]
BD258	VSS[248]	VSS[347]
BD262	VSS[249]	VSS[348]
BD266	VSS[250]	VSS[349]
BD270	VSS[251]	VSS[350]
BD274	VSS[252]	VSS[351]
BD278	VSS[253]	VSS[352]
BD282	VSS[254]	
BD286	VSS[255]	
BD290	VSS[256]	
BD294	VSS[257]	
BD298	VSS[258]	

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				LA-8043P	
				Date:	Friday, March 02, 2012
				Sheet	21 of 58
				Rev	0.1

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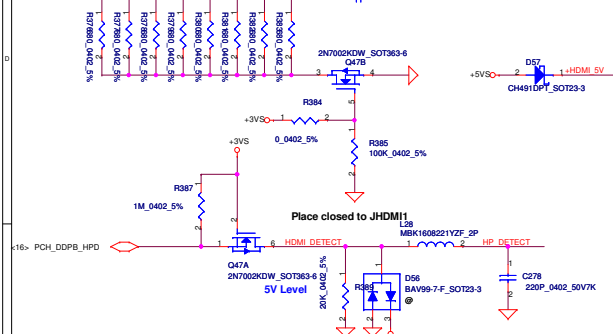
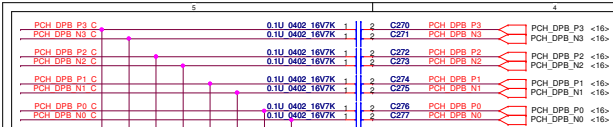
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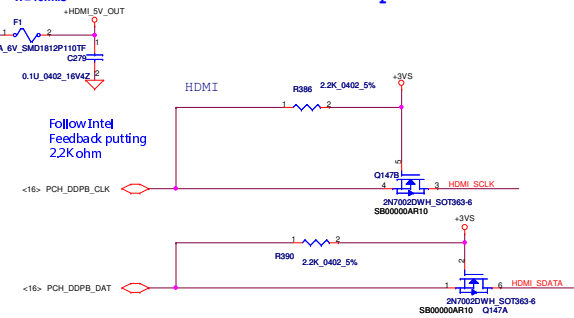
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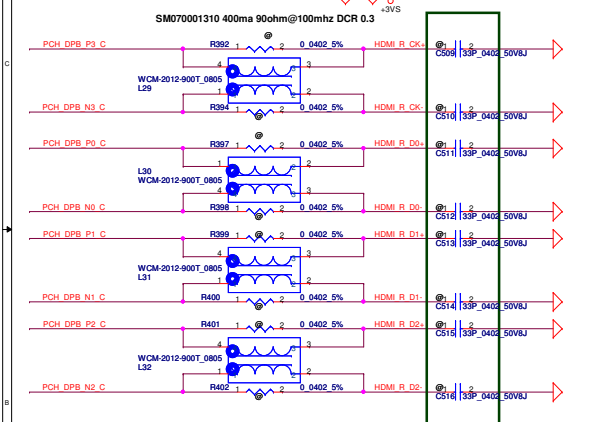
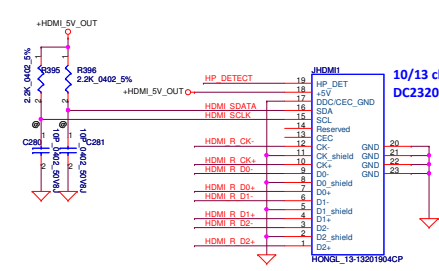
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Del HDMI Repeater PS8271



5V PULL UP IN CONNECTER SIDE



Follow EMI request add 33pF cap to GND.
11.02

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	HDMI Conn
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				Date	Friday, March 02, 2012
				Sheet	30 of 58

R73 pull high, and stuff R100
12.07

WLAN

WL_OFF# Change from PCH GPIO55 to GPIO46.
(pull-high change from +3VS to +3V_PCH)
12.07

For Wireless LAN

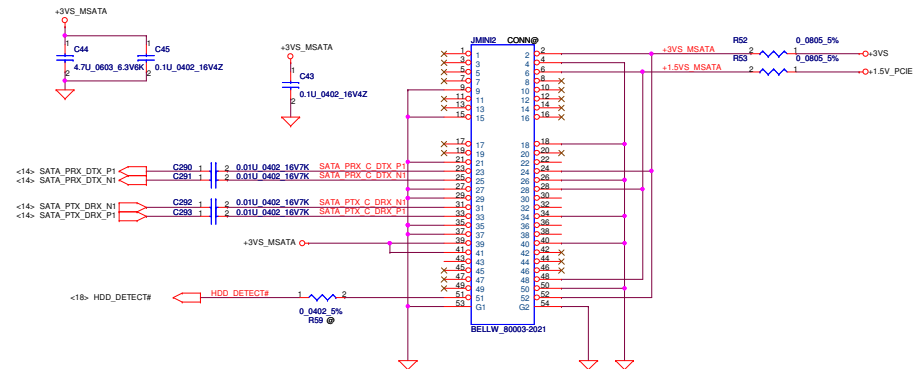
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Compal Electronics, Inc.	
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				Rev 0.1	
				LA-8042P	
				Date:	Friday, March 02, 2012
				Sheet	31 of 58

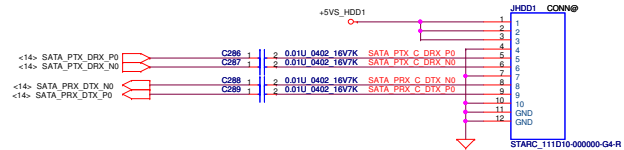
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Issued Date	2011/06/29	Deciphered Date	2011/06/29			
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					LA-8042P	0.1
Date:				Friday, March 02, 2012	Sheet	32 of 58

mSATA Conn

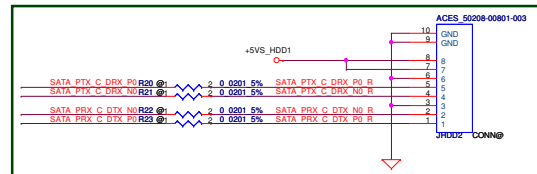
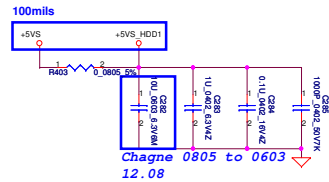


Exchange port 0 & port 1 for SI as customer request
11.30

Change footprint to Starconn (PAD is bigger)
11.30



SATA connector



Co-layout for wire type connector

01.16

Change connector to ACES_50376

01.31

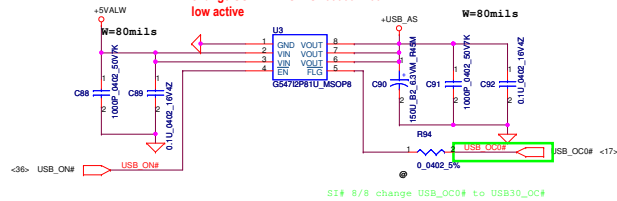
Change connector to ACES_50208 because current limit issue

02.06

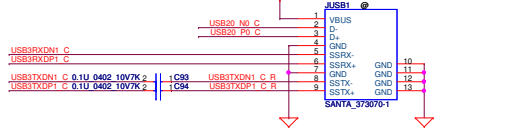
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	mSATA Connector
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				Rev	PC-042A-02 05/10
				Checked	GK / JG

USB3.0

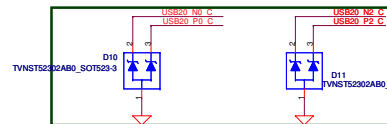
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



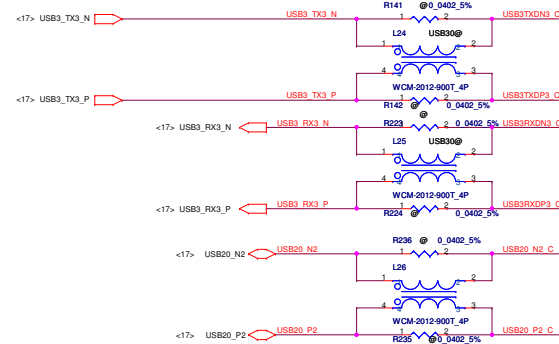
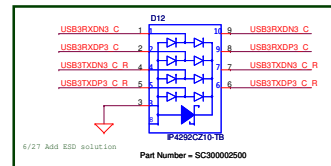
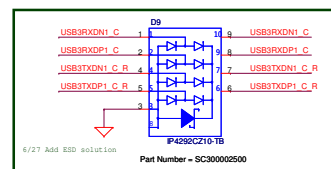
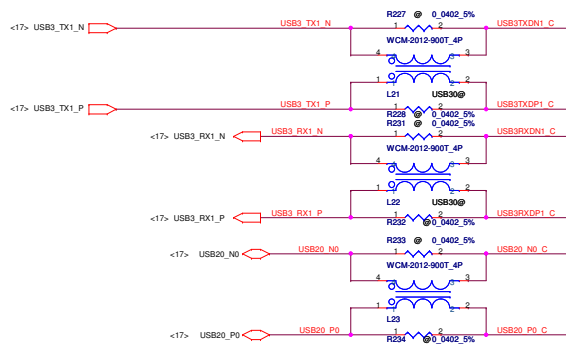
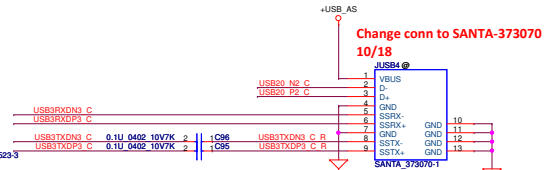
Change conn to SANTA-373070
10/18



Change P/N from SCA00000T00 to SCA00001L00
11.01
Change P/N to SCA00001W00 for smaller size, 10*10 choke
02.13

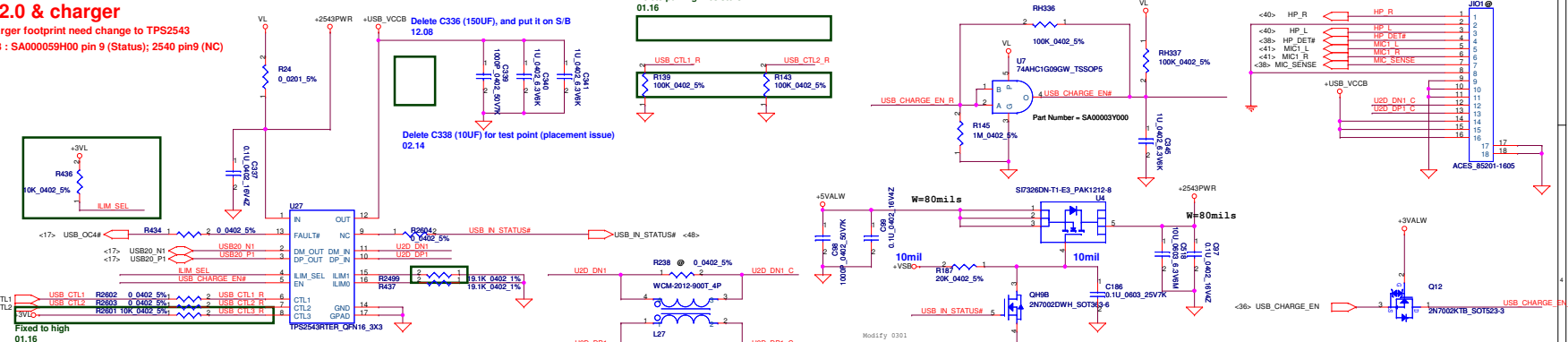


Change conn to SANTA-373070
10/18



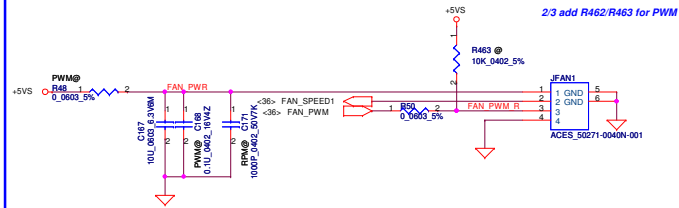
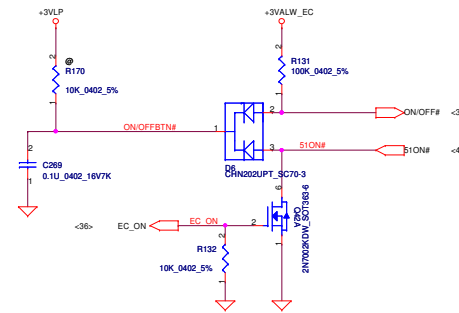
USB2.0 & charger

USB charger footprint need change to TPS2543
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)

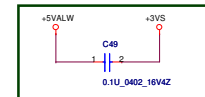
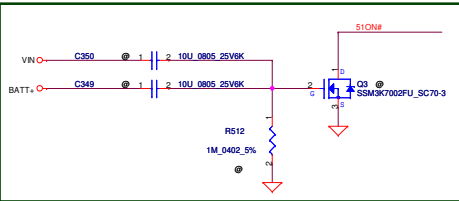


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	USB Con & Daughter Con
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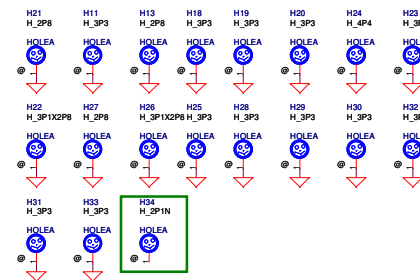
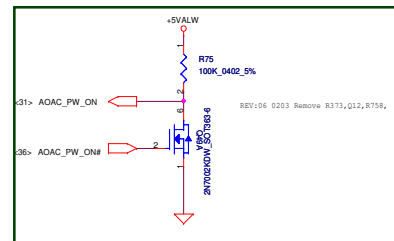
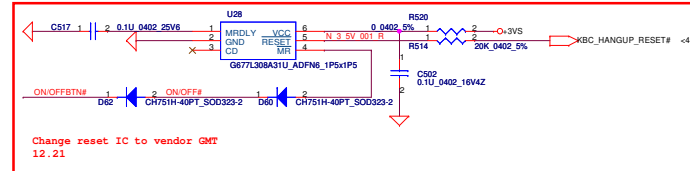
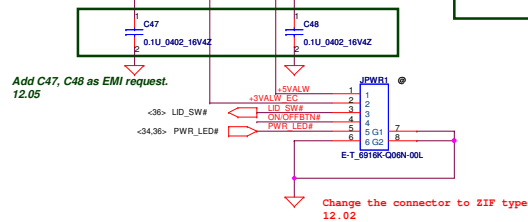
PWM Fan Control circuit



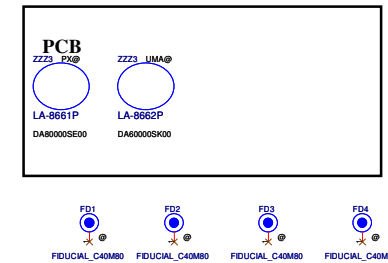
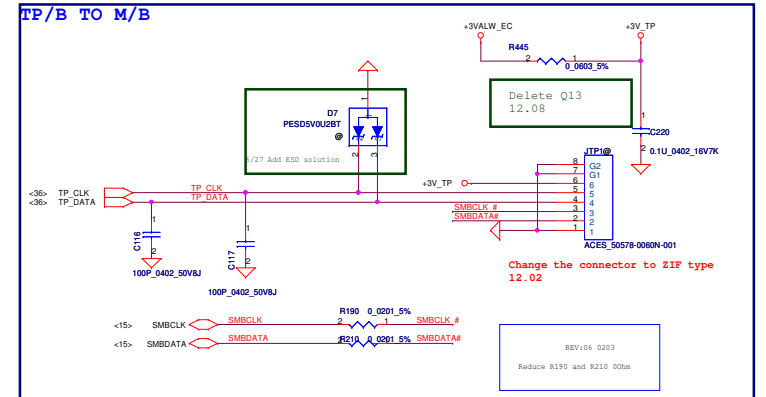
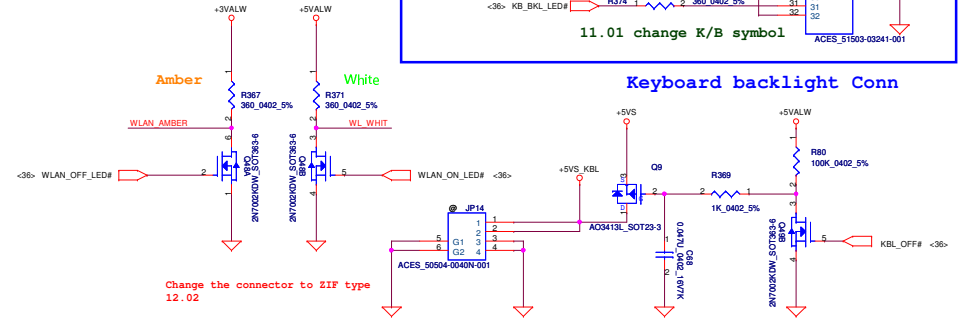
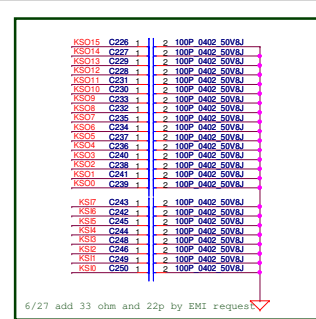
Follow thermal (FAN) design guide, pull-high 10K
12.05



Add C49 as EMI request.
12.05



12/15: Add NPTH H34



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	KB/TPLED/FAN/Screw/Gsensor	
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				Custom	LA-8041P	
				Date:	Saturday, March 03, 2012	Sheet

Notes:

- Keep PVDD supply and speaker traces routed on the DGND plane.
- Keep away from AGND and other analog signals

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Follow EMI request, reserve cap.
11.03

Correct CA508 circuitry.
12.05

Place C208 close to Coder

Follow EMI request, reserve cap.
11.03

SB Beep

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, change C12 to 0.1uF

CA11

If Sense_B is un-used, then pull high
Sense_B to AVDD by 10Kohm resistor

HP Jack

Ext MIC

Internal SPKR(front stereo speaker

9/27 LDO TPS793475DBVR for audio power

-401

1

402_2

6

0

2

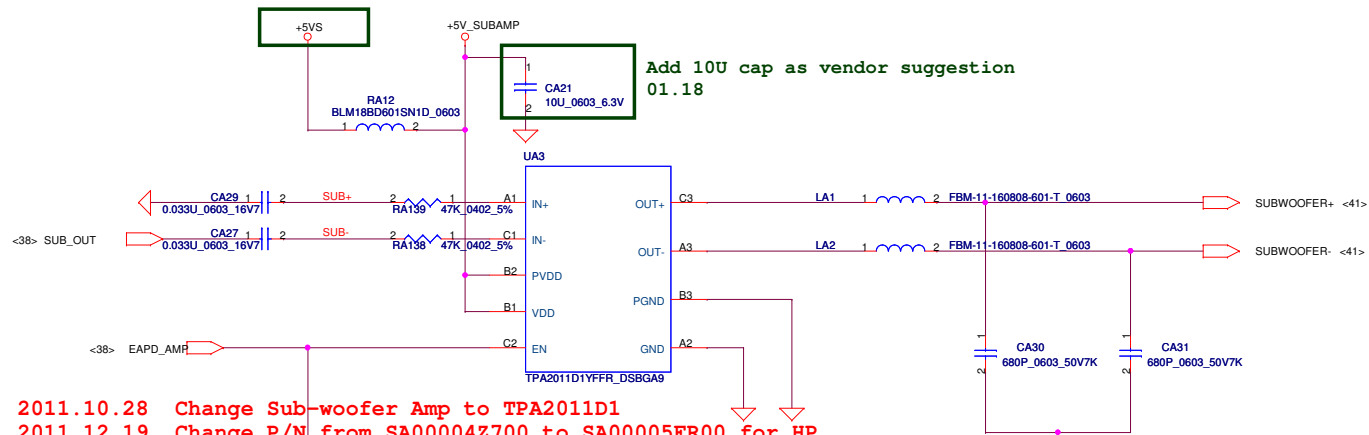
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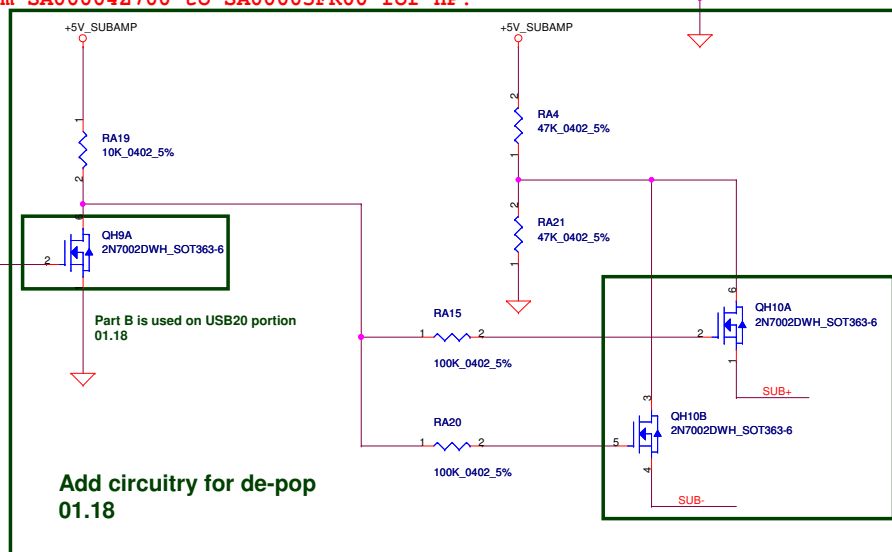
1

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Issued Date	2011/06/29	Deciphered Date	2011/06/29
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title
			Audio IDT 92HD91	
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				Rev 0.1



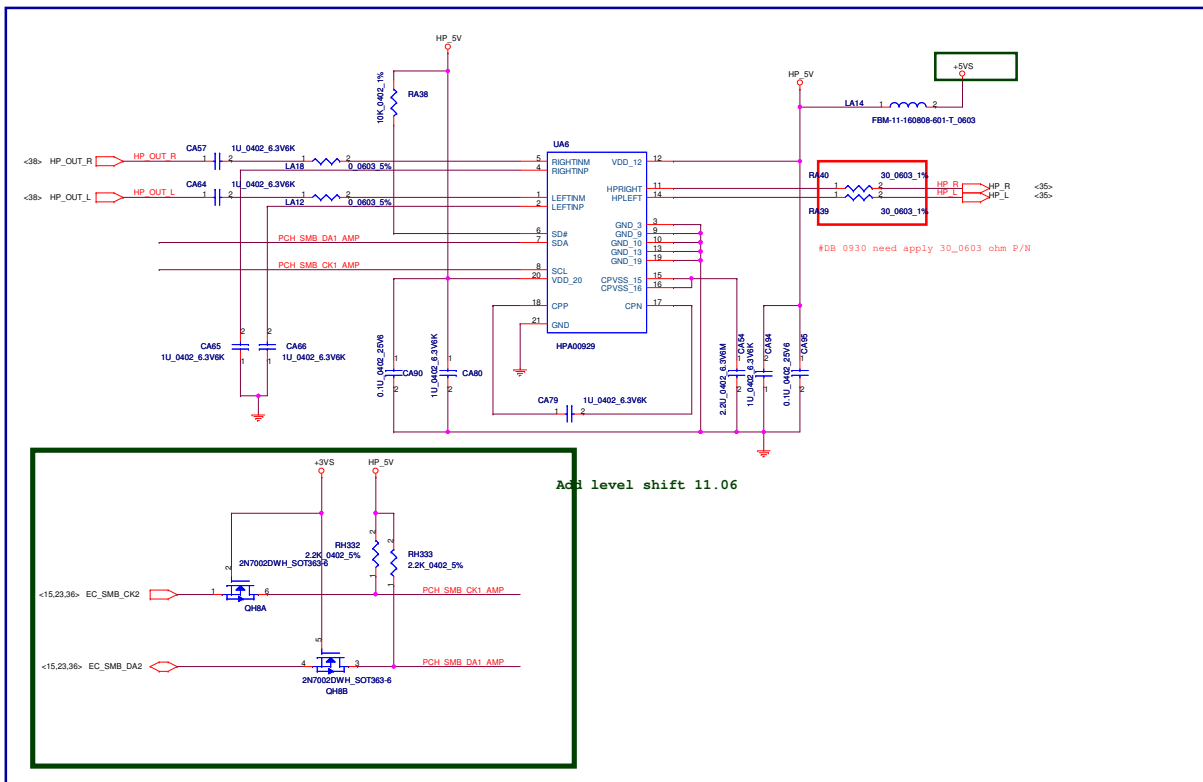
2011.10.28 Change Sub-woofer Amp to TPA2011D1
 2011.12.19 Change P/N from SA00004Z700 to SA00005FR00 for HP.



QH10 must change to BJT before SMT
 (Footprint is compatible from BJT & MOTFET)
 01.18
 BJT P/N: SB00000VH00

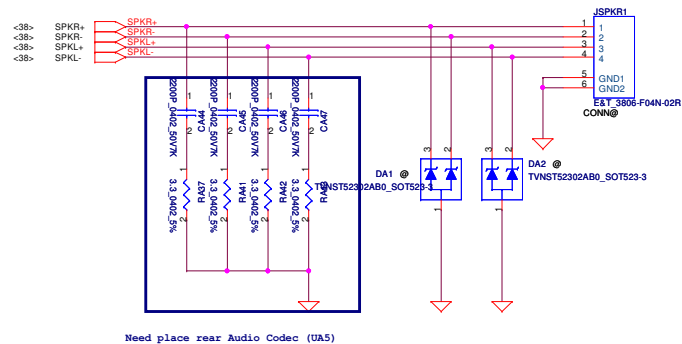
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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				Size	Document Number
				B	Rev 0.1
Date: Friday, March 02, 2012		Sheet 39 of 58			

Headphone amplifier

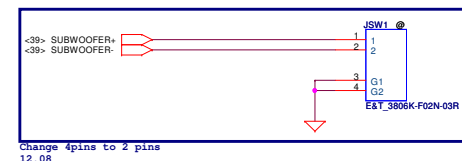
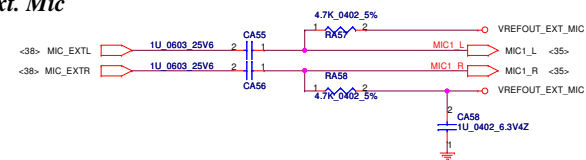


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Audio SPK/HP Amplifier
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				Date:	Wednesday, March 07, 2012
				Sheet	40 of 58

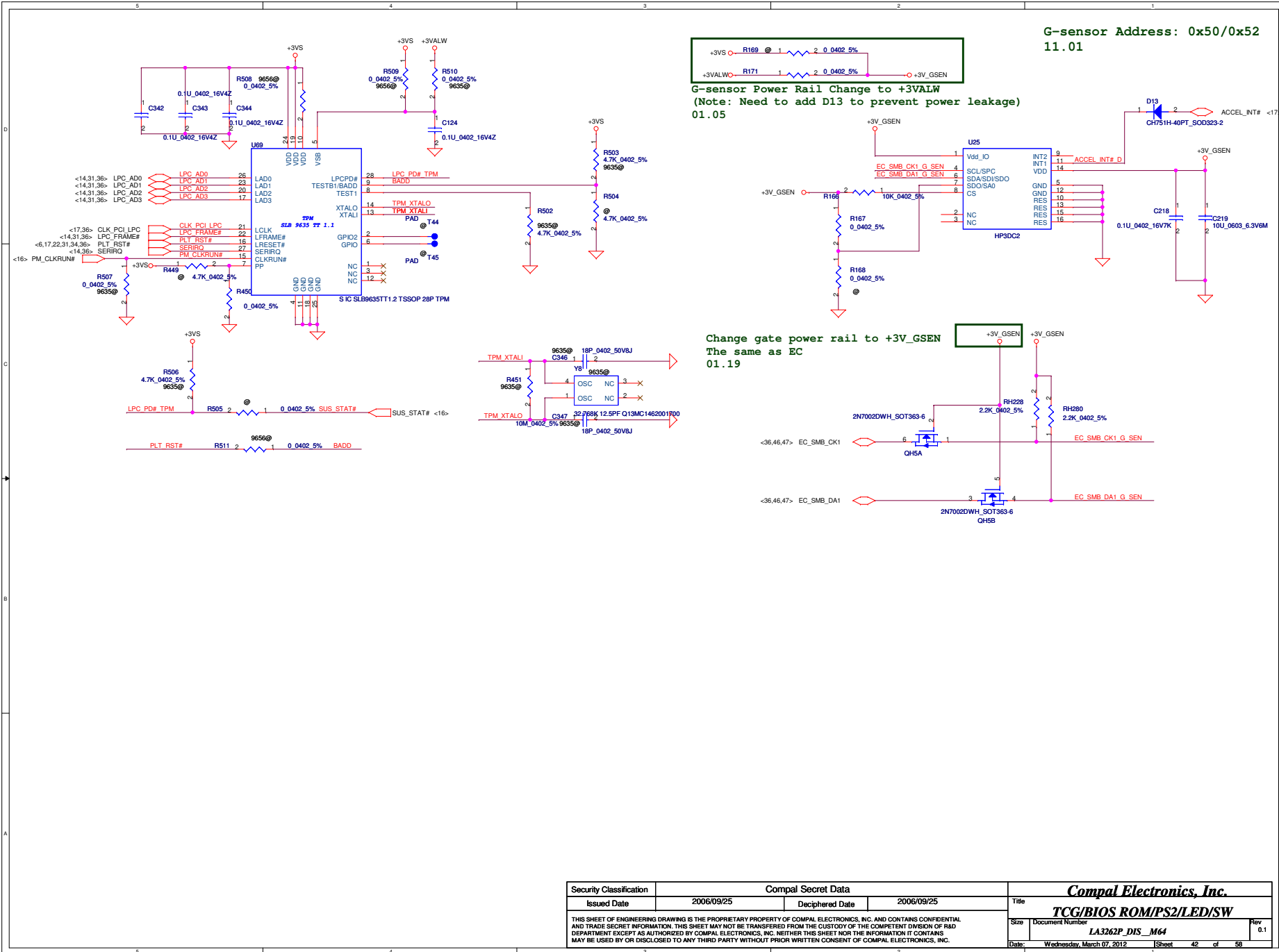
Front Speaker Connector 1

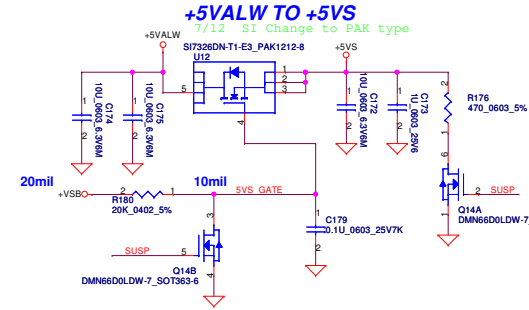


Ext. Mic



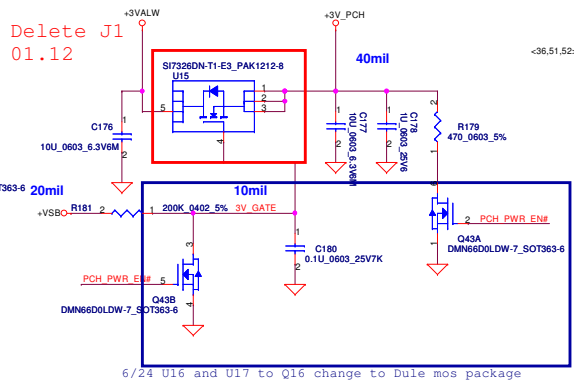
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title	Audio SPK Conn/Jack/MIC
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				Customer	PAV10
				Date:	Friday, March 02, 2012





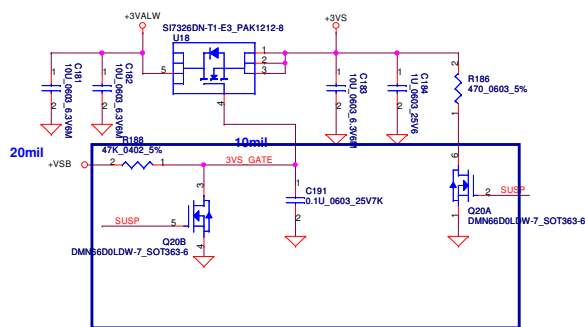
10.21 Change to PAK type
 +3VALW TO +3VALW(PCH AUX Power)
 Short J1 for PCH VCCSUS3.3

Delete J1
 01.12

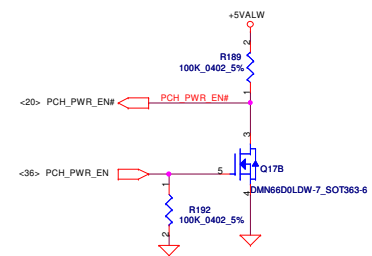
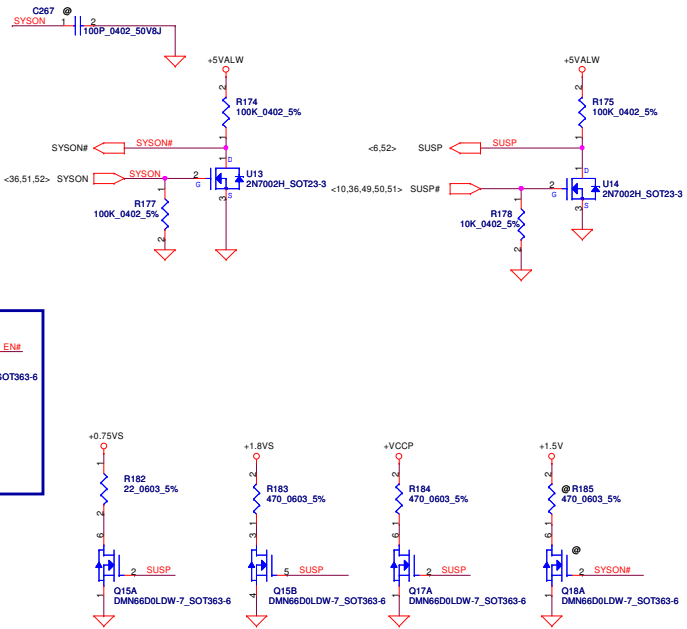


6/24 U16 and U17 to Q16 change to Dule mos package

+3VALW TO +3VS

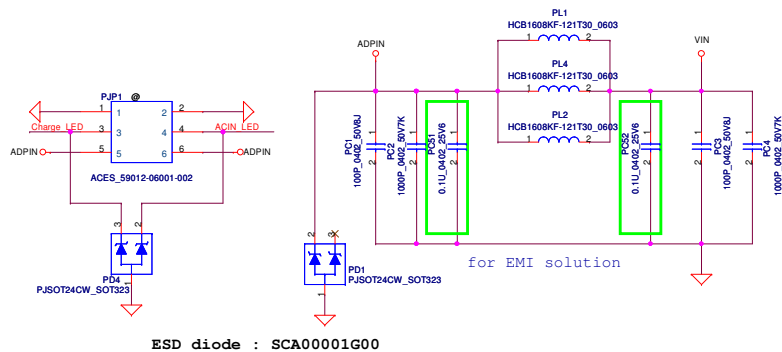


6/24 Q20 and Q21 to Q20 change to Dule mos package

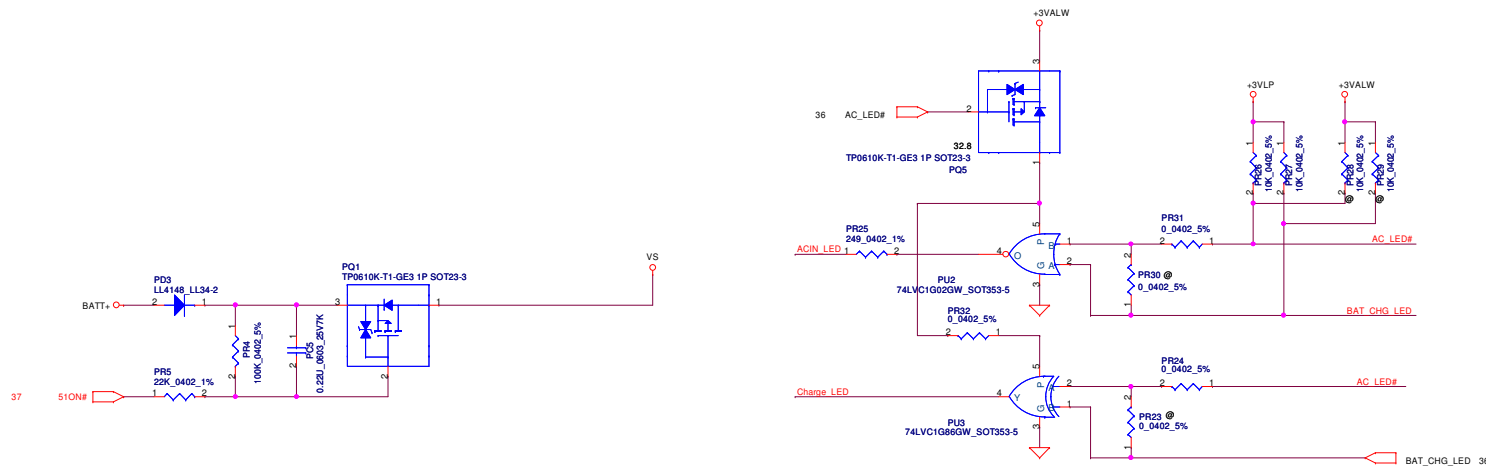


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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				Custom	LA-8661P
				Date:	Friday, March 02, 2012
				Sheet	43 of 58
				Rev	0.1

	QA260 Strap pin Table		@:un_install	
	Netname	setting	BOM config	
CPU	CFG2	1	RC40 @	1: Normal Operation; Lane # definition matchessocket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @	1 : Disabled; No Physical Display Portattached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @	H : Integrated VRM enable L : Integrated VRM disable
	HDA_SPKR	L	RH139 @	H:No Reboot L:Default
	HDA_SYNC	H	RH149	This signal has a weak internal pull-downOn Die PLL VR is supplied by H:1.5V when smapled high L:1.8V when sampled low Needs to be pulled High for Huron River platfrom
	HDA_SDOUT	L	RH140 @	ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @	On Die DSW VR Enable H : Enable L : Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @	On-Die PLL Voltage Regulator This signal has a weak internal pull up H : On-Die voltage regulator enable L : On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246	FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
	GPIO27	H	RH250 @	PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable

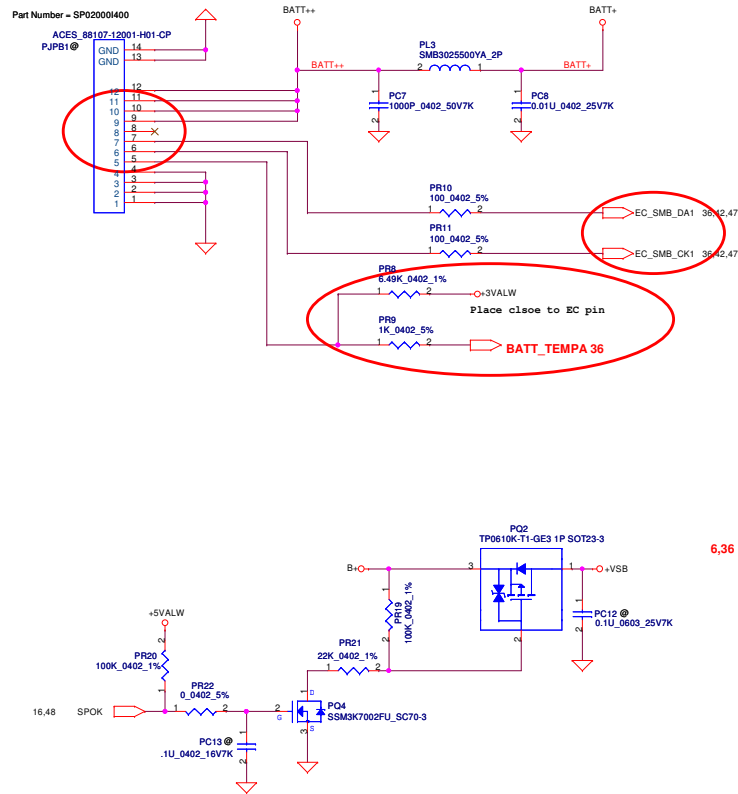


KBC output		Input to Battery		
AC_LED#	BAT_CHG_LED	ACIN_LED	Charge_LED	LED Status
0	0	1	0	White LED light
0	1	0	1	Amber LED light
1	0	0	0	X (don't care)
1	1	0	0	X (don't care)



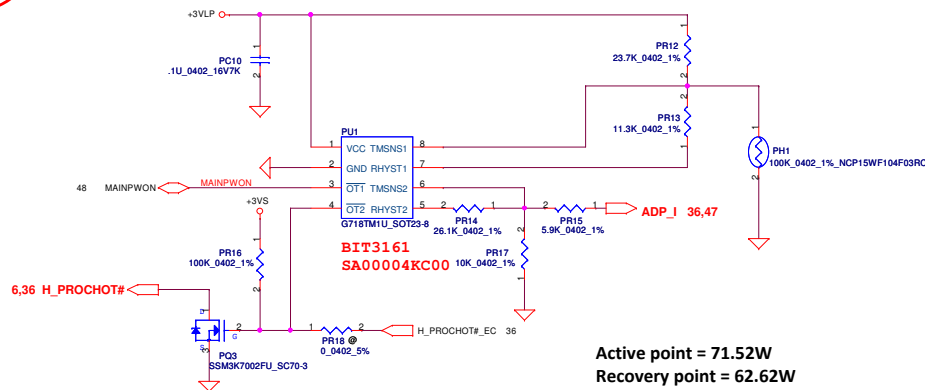
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/10/03	Deciphered Date	2014/12/31	Title	PWR- DCIN / Vin Detector
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				Document Number	LA-8551P
				Date	Saturday, March 03, 2012
				Sheet	45 of 59

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

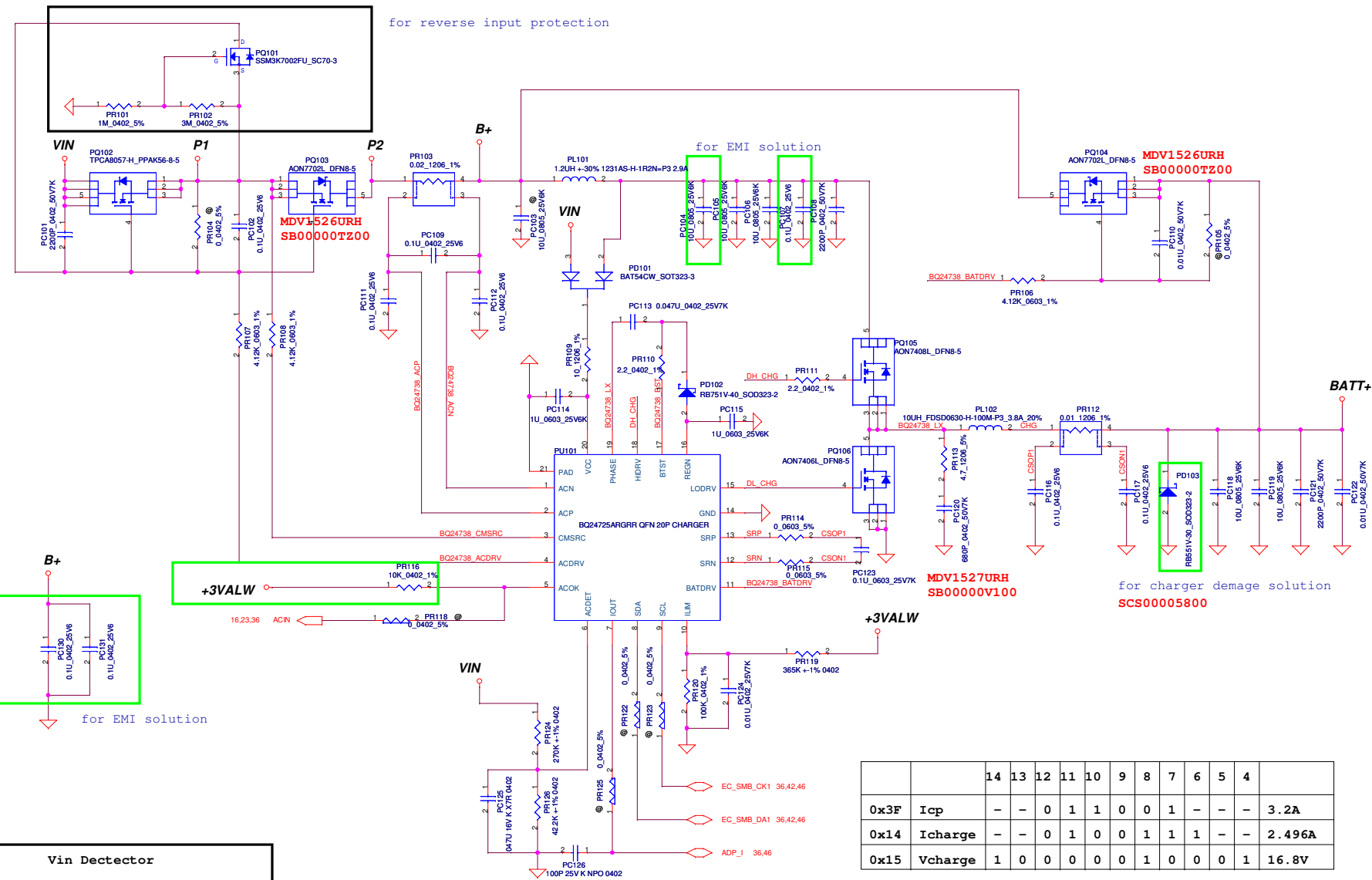


PH1 under CPU bottom side :
CPU thermal protection at 90 +3 degree C
Recovery at 56 +3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset * Rtml) / (3 * Rtml - Rset)
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



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Title	PWR- BATTERY CONN		
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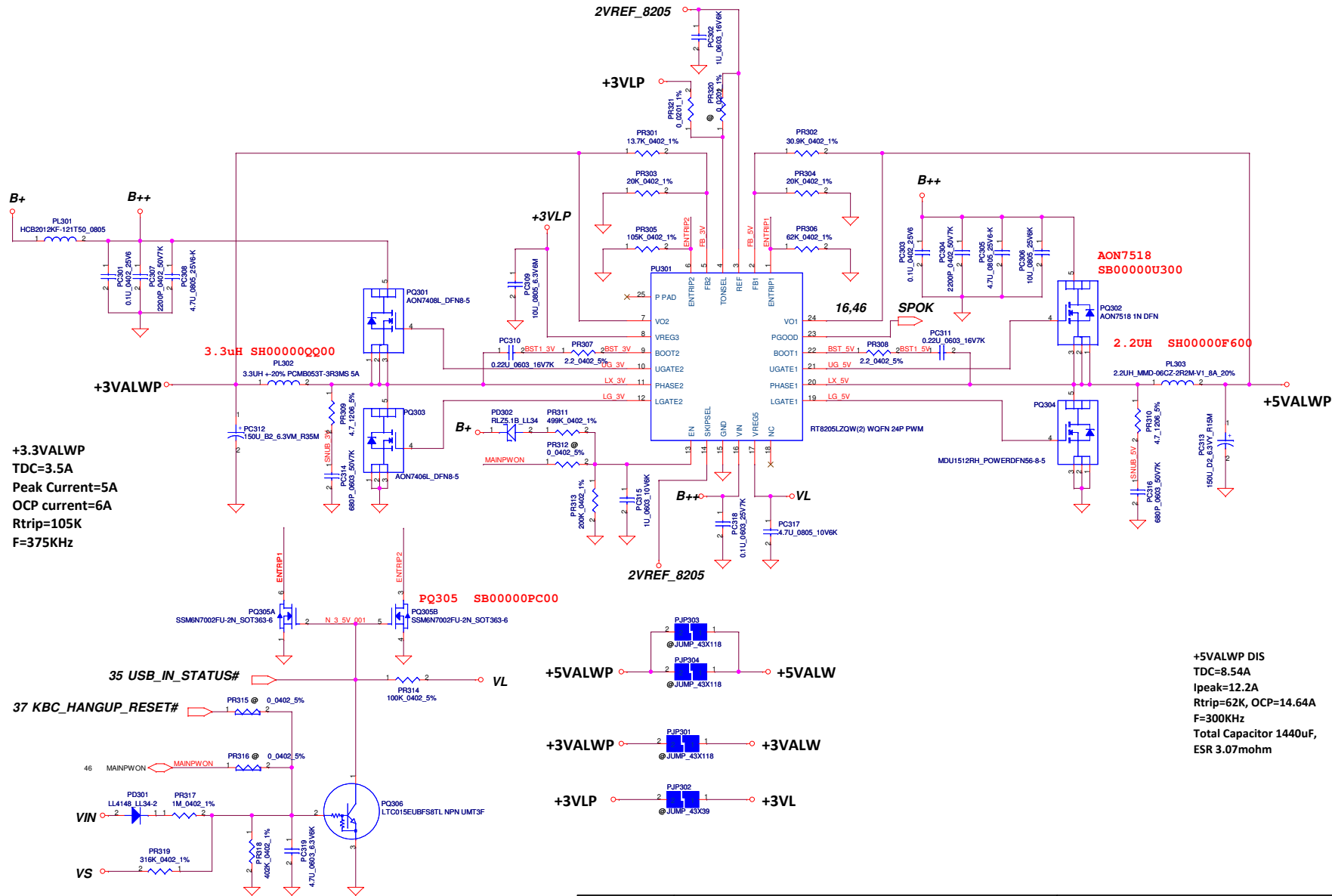


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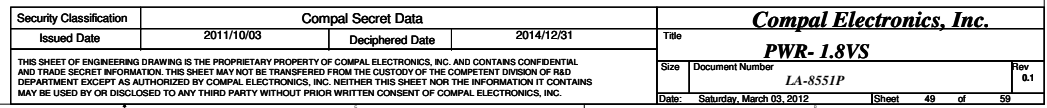
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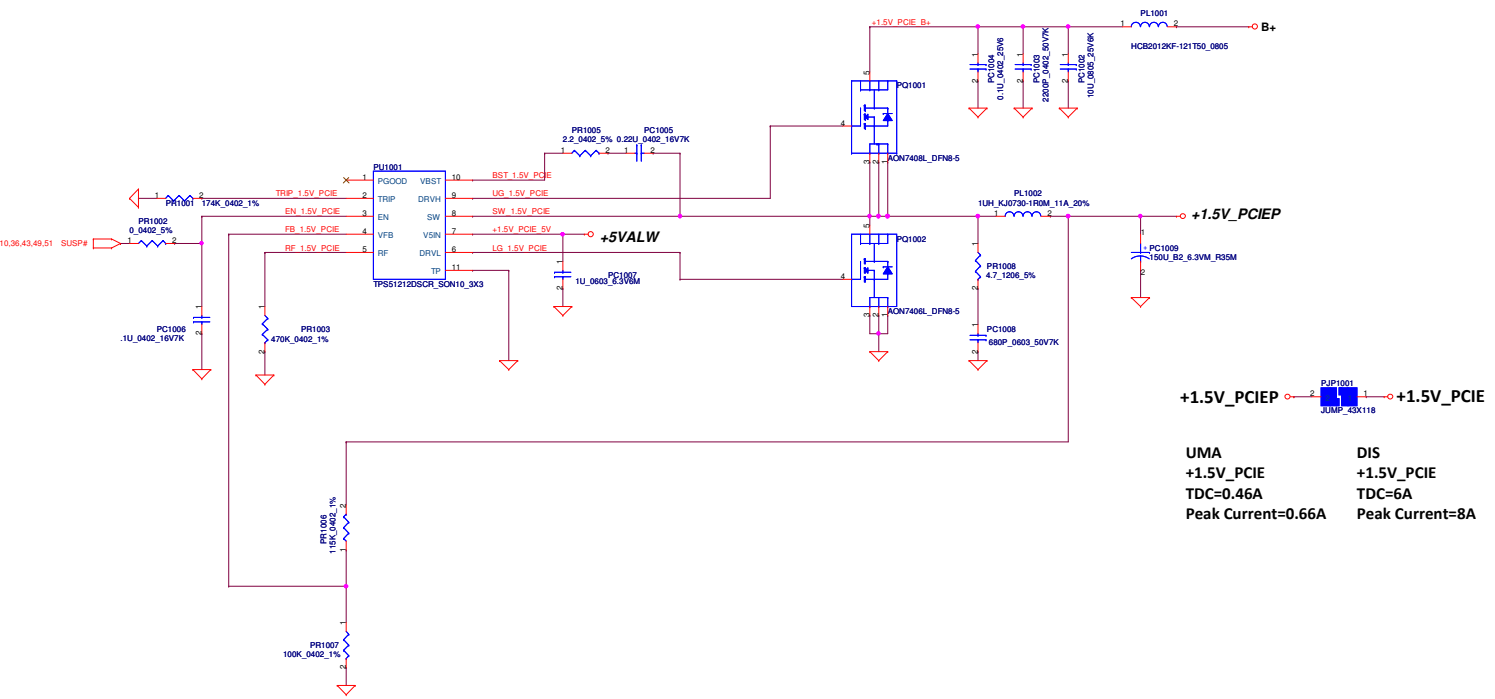
PWR- CHARGER

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				Document Number	LA-8551P
				Date	Saturday, March 03, 2012
				Sheet	46 of 59



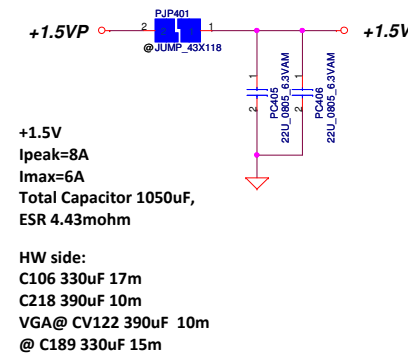
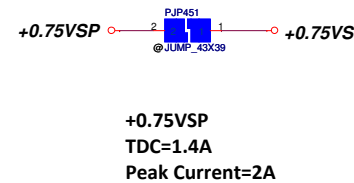
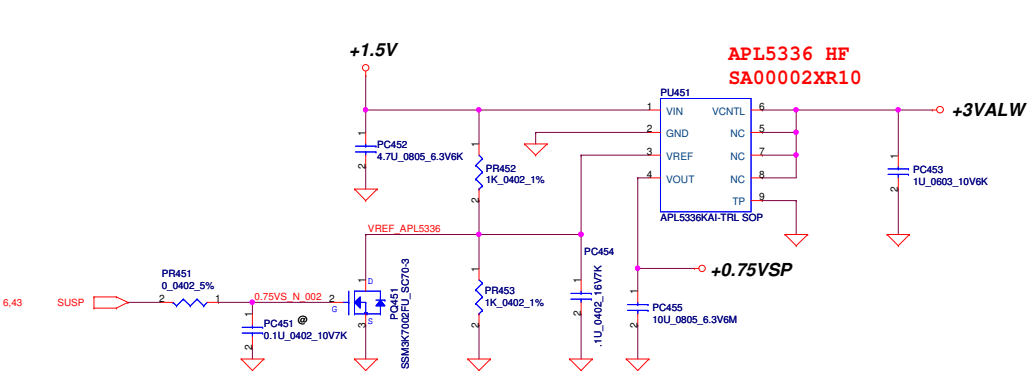
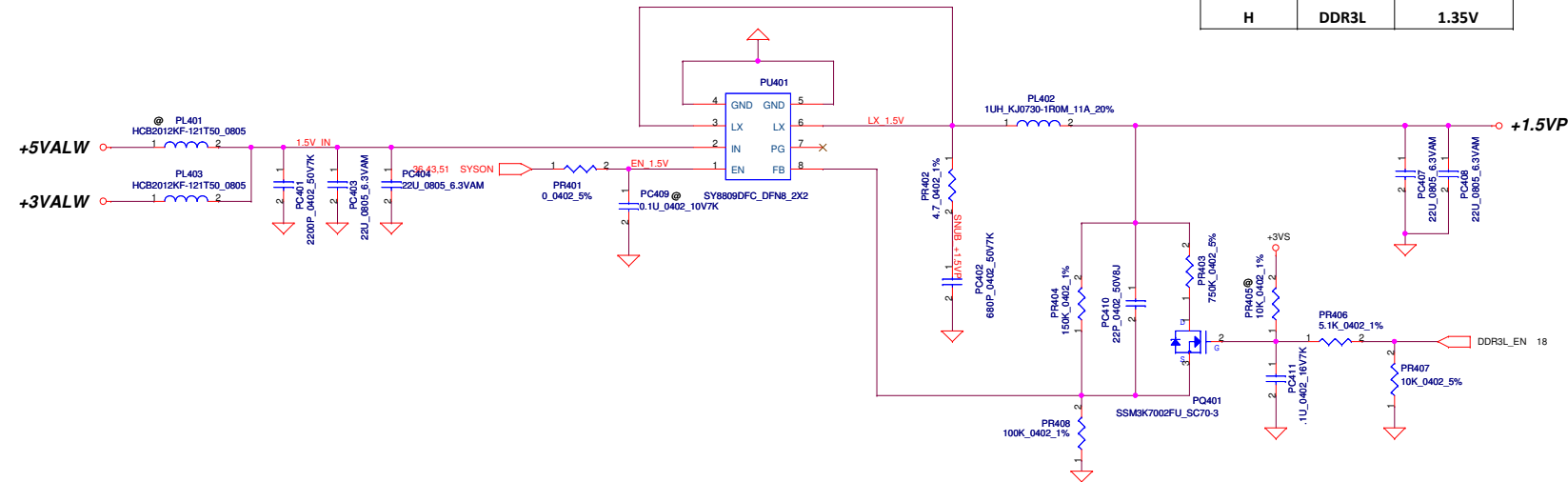


UMA
+1.5V_PCIE
TDC=0.46A
Peak Current=0.66A

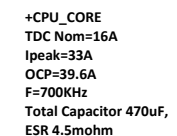
DIS
+1.5V_PCIE
TDC=6A
Peak Current=8A

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Size	C	Document Number	LA-8551P	Rev	0.1
Date		Saturday, March 03, 2012		Sheet	50 of 50

DDR3L_EN		1.5VP
L	DDR3	1.5V
H	DDR3L	1.35V



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				Size	Rev
				Customer	0.1
				Date	Sheet
				Saturday, March 03, 2012	52 of 59

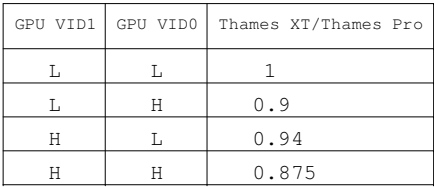


+GFX_CORE
TDC=21.5A
Ipeak=33A
OCP=39.6A
F=700KHz
Total Capacitor 470uF
ESR 4.5mohm

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Date:	Saturday, March 03, 2012	Sheet	54	of	59



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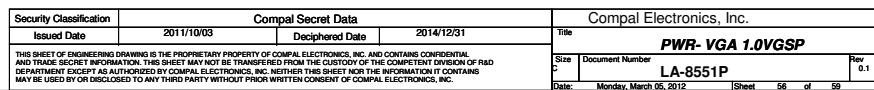


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PWR- VGA_VDDC

LA-8551I

Date: Wednesday, March 07, 2012 Sheet 55 of 59



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	change PC111 to 0402	2011/11/28		For layout space		
2	47	remove PR121	2011/11/28		0ohm, not needed		
3	47	change PR124 to 270K, PR126 to 42.2K	2011/11/28		change Vin detector setting		
4	47	change PC125 to 0.047uF	2011/11/28				
5	47	change PR125 to 0ohm, PC126 to 100pF	2011/11/28		FAE review recommand		
6	47	change PR119 to 365K	2011/11/28		modify charge Ilimit to 3.54A		
7	47	change PR111 to 0ohm	2011/11/28				
8	47	add PL101	2011/11/28				
9	46	delete PD5, PD6	2011/11/28		imbedded battery, ESD diode is not needed		
10	46	SMC, SMD exchange	2011/11/28				
11	46	delete pin8 and pin5, add battery temp sense at pin5.	2011/11/28		EC request to need one detect pin if SMB communication fail.		
12	47	change PQ302 to AON7518	2011/11/28				
13	50, 52	change PU1001, PU401 from SY8036HDBC to SY8036LDB	2011/11/28				
14	53	change PU651 from SY8037DCC to SY8037ADCC	2011/11/28				
15	52	add PQ401, PR406, PR407, PC411	2011/11/28				
16	56	change PR1055 to 28.7K	2011/11/28		for correct 1.0V voltage		
17	54	change PL202, PL204 to SH00000PP00, 0.12uH	2011/11/28				
18	54	change PU201 to RT8167, SA00005AU00	2011/11/28				
19	54	change PQ201, PQ203 to AON7518, SB00000U300	2011/11/28				
20	54	change PQ202, PQ204 to FDMS0308AS, SB00000U400	2011/11/28				
21	55	change PL802 to 0.36uH, SH00000HD00	2011/11/28				
22	52	change PU401 to SY8809DFC	2011/11/29				
23	45, 48	change PD2, PD301 DIO CD4148WN-1 1206	2011/11/29		For cost and layout space		
24	51	add PC511, PC512	2011/12/11				
25	54	change PL201 to 0805, and add PL203	2011/12/11				
26	48	add PR320	2011/12/11		tune frequency		
27	55	change PC813, PC814, PC815, PC816 tp 330uF 9m	2011/12/11				
28	47	change PQ101 to SB000009610	2011/12/11				
29	54	change PR210, PR214, PR261, PR264 to 3.3K; PR222 to 15.8K; PR255 to 10.5K; PC202, PC209 to 270p; PC223 to 220p; PC227 to 560p; PR224, PR254 to 1.82K; PR207 to 127K	2011/12/11		Fine tune CPU, GFX transient		
30	47, 54	change PR111, PR110, PR216, PR249 to 2.2 ohm	2011/12/12		For EMI solution		
31	53, 56	change PL602, PL1052 to SH00000MMW00	2011/12/12		For crack issue		
32	55	change PL802 to SH00000HQ00	2011/12/12		For thermal solution		
33	48	change PL303 to SH00000CN00	2011/12/12		For thermal solution		
34	47	change PR114, PR115 to 0 ohm	2011/12/14		Prevent charger damaged by negative output voltage		
35	54	change PR207 to 66.5K	2011/12/14		For GFX GT2 current limit		
36	54	change PR237 to 23.7K +-1% 0402	2011/12/23				
37	54	change PR241 to 1/16W 0 +-5% 0402	2011/12/23				
38	54	change PR242 to 23.7K +-1% 0402	2011/12/23				
39	47	change PQ103, PQ104 to SB00000TZ00	2011/12/23				
40	47, 48	change PQ106, PQ303 to SB00000H700	2011/12/23				
41	54	change PR210, PR261, PR264 to 3.3K +-1% 0402	2011/12/23				
42	53	change PL651 to SY8037CDCC	2012/1/11		For latch mode		
43	57	change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/11		For height limit		
44	46	Delete PC11	2012/1/12		For ME request		

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				Document Number	LA-8551P
				Date:	Saturday, March 03, 2012
				Sheet	58 of 59

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	47	change PR114 to 10, PR115 to 6.8ohm, add PD103	2012/1/30		For Charger issue		
46	47	Add PC130, PC131, PC104, PC107	2012/1/30		For EMI solution		
47	48	Add PR321	2012/1/30		Choose working frequency to improve efficiency and thermal		
48	50	change 1.5VPCIE Circuit	2012/1/30		Change input voltage form 5V to 19V to slove thermal issue		
49	52	Add PL403	2012/1/30		Choose input voltage to slove thermal issue		
50	54	Change PR224 to 1.58Kohm, PC209 to 220PF, PC202 to 390PF, PR222 to 16.9Kohm, PR237 to 21.5K	2012/1/30		Base on SI layout, FAE review recommand value		
51	48	change PL303 to SH00000F600	2012/1/30		For thermal issue		
52	45	Delete PD2, PR2, FR3, PC6	2012/1/30		For Layout space		
53	47, 48, 54	Change PQ302, PQ201, PQ203 to AON7514	2012/1/30		For efficiency		
54	51	Delete PJP501	2012/1/30		For Layout space		
55	55	Change PC813, PC814, PC815 to 470uF, delete PC816 Change PL802 0.36uF to 13*13*3.5 size	2012/1/30		For thermal issue		
56	55	Add PC820, PC821, PC822	2012/1/30		For VGA transient voltage		
57	57	Change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/30		For ME request		
58	47	change PQ102 to TPCA8057	2012/1/30				
59	54	change PC223 to 560pF, PC227 to 220pF	2012/2/17		For FAE suggesstion		
60	48	change PQ302 to AON7518	2012/2/17		For efficiency		
61	55	change PL802 to 13*13*3 size	2012/2/17		For thermal solution		
62	47	change PR114, PR115 to 0 ohm, PD103 to SCS00005800	2012/2/17		For HP and soucer request		
63	54	change PC201 to 330uF	2012/2/17		For acoustic solution		
64	45	change LED circuit	2012/2/23				
65	48	change PL303 to 3.3uH 10*10*3H, PC313 to 150U_B2_6.3VM_R35M, remove 5V output jumper	2012/2/23		For thermal solution		
66	53	change PU651 to SY8037DDCC	2012/2/23		For ULV CPU and latch mode		
67	55	change FR812 and FR816 power to +3VGS	2012/2/23		For leakage issue		
68	45	change LED circuit	2012/2/29				
69	54	change PC209 to 390pF, PR237 to 13.3Kohm, PR254 to 1.13Kohm, PR255 to 16.2Kohm, PR242 to 6.65Kohm	2012/2/29		Base on PV layout		
70	45	change PL1, PL2 to 0603 size, add PL4	2012/2/29		EMI request		

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					LA-8551P	0.1
				Date:	Saturday, March 03, 2012	Sheet 59 of 59

