

Compal Confidential

PAWGE Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M3L + GPU RobsonXT

2011-11-21

REV: 1.0

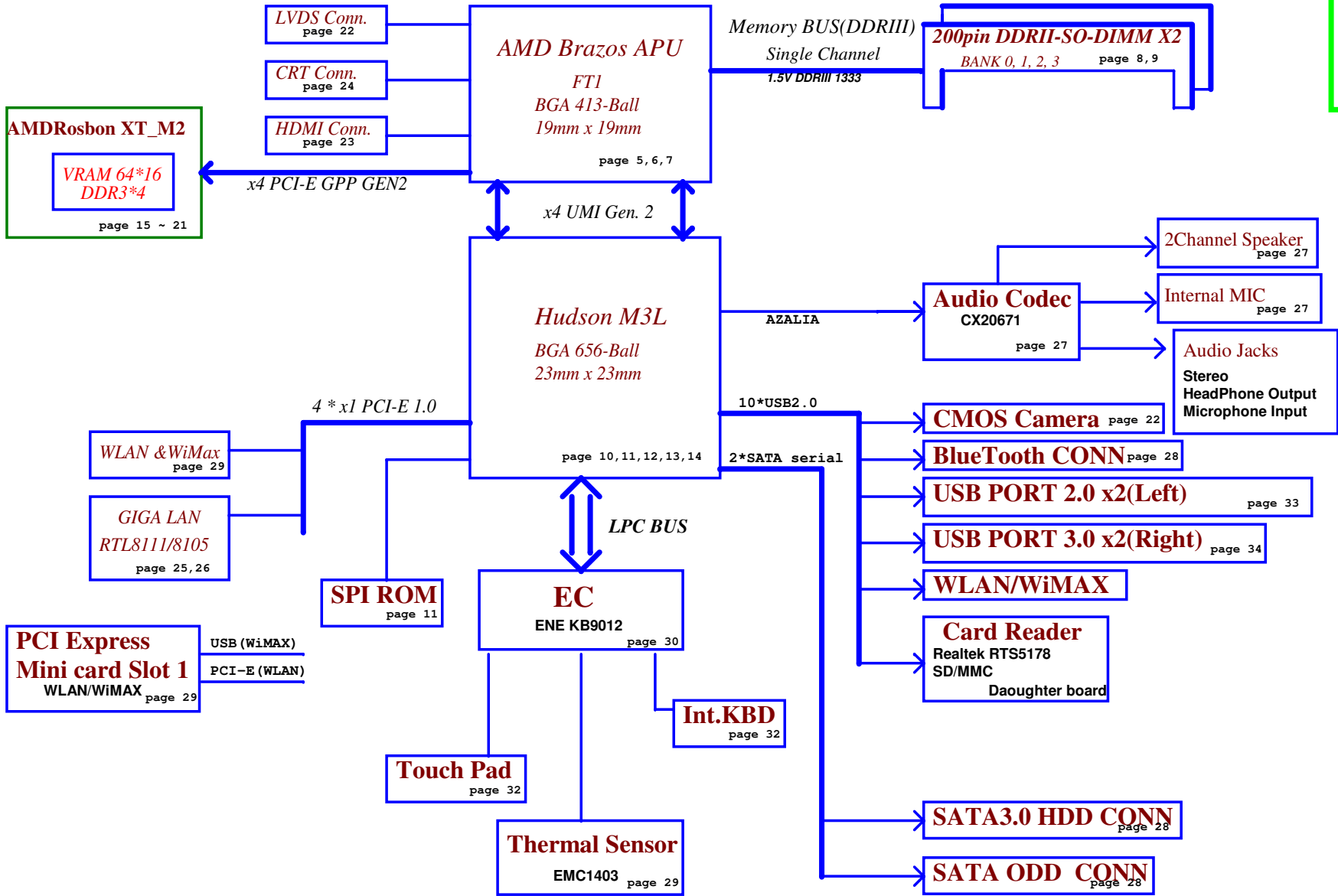
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QIWG5

LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B

QIWG6

LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B
LS7984P LED/B
LS7985P ODD/B



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	EMC1412-2 (dGPU)	1111-100xb	F8H
			EMC1403-2(DDR,WLAN)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M3L USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB
Port1	Right USB
Port2	Mini-PCIE
Port3	USB Camera
Port4	NC
Port5	CardReader
Port6	BT
Port7	NC
Port8	NC
Port9	NC
Port10	Left USB1
Port11	Left USB2
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M3L SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

UMA@ : UMA only
PX@ : DIS muxluss PX 4.0
Robson@ : Robson GPU
GIGA@ : RTL8111 1000
8105@ : RTL8105 10/100
DIMM@ : DIMM select
CMOS@ : USB camera
BT@ : BT function
ME@ : ME components
X76@, H1G@, H512@, S1G@, S512@ : VRAM
45@ : 45 Level
HDMI@ : HDMI function
non HDMI@ : HDMI function

AN@ : Apple + Nokia ear phone combo
A@ : Apple ear phone
PCB@ : PCB PN
14@ : 14"
15@ : 15"
BBH@ : BBH
nonBBH@@ : nonBBH@

Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VGS)

PCIE_VDDC(1.0V)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

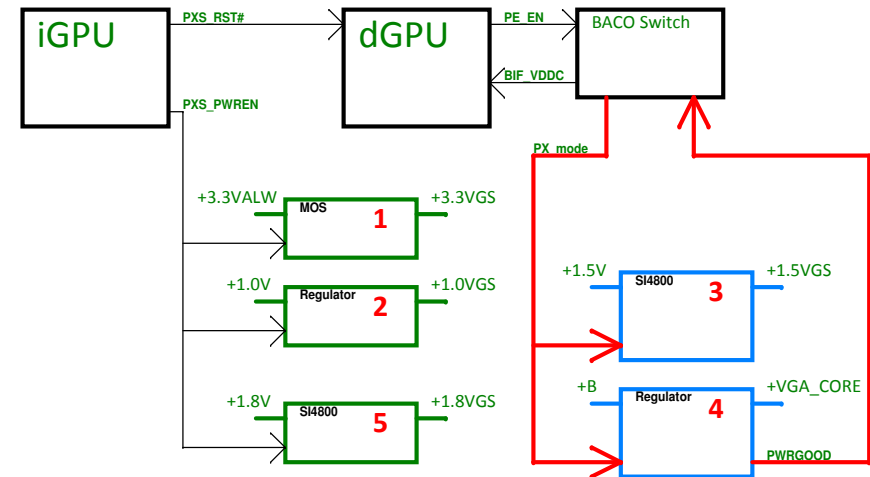
Without BACO option :

PXS_RST# : Low -> Reset dGPU ; High -> Normal operation
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

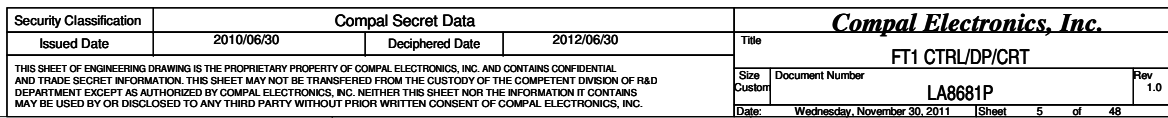
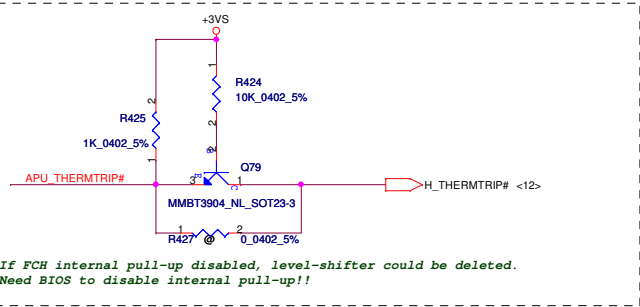
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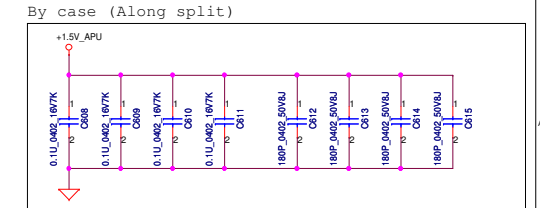
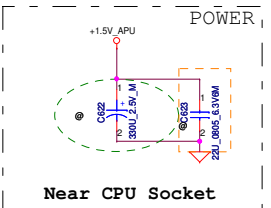
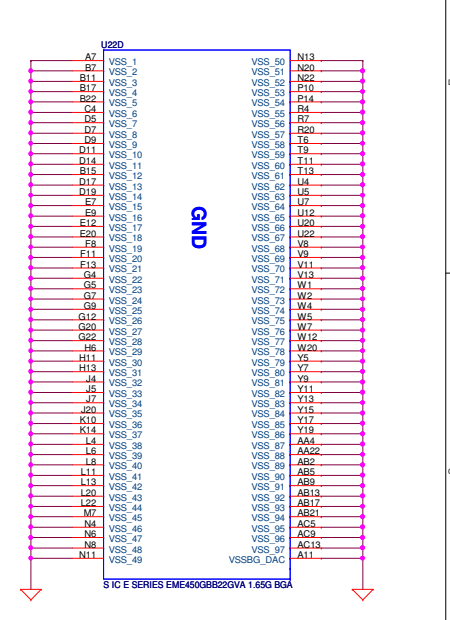
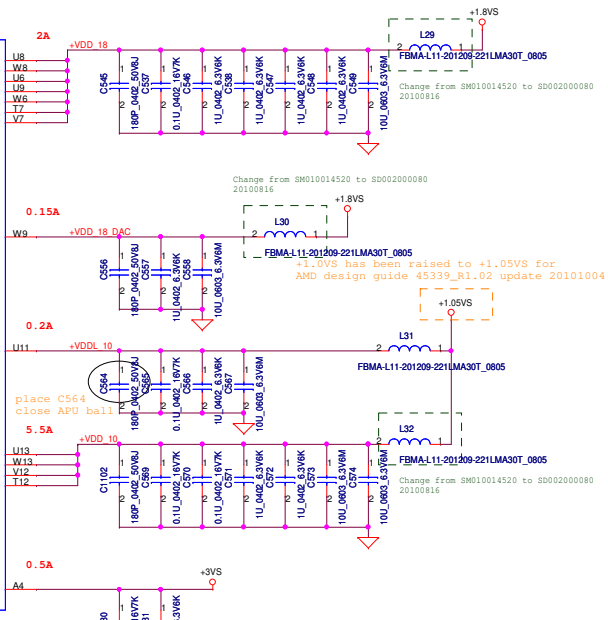
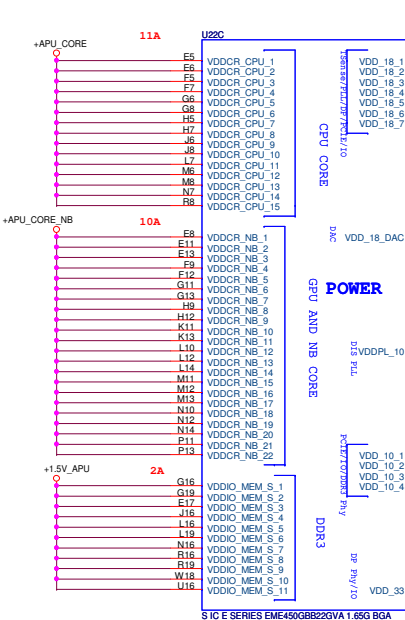
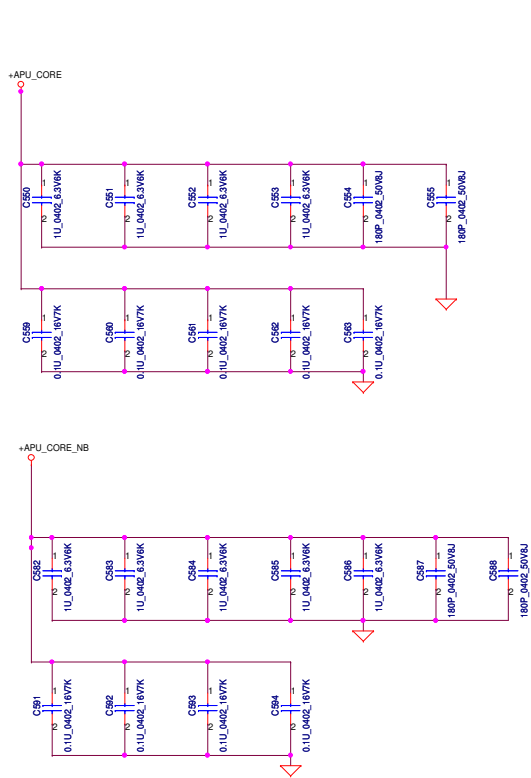
PXS_RST# : High -> Normal operation (dGPU is not reset on BACO mode)
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

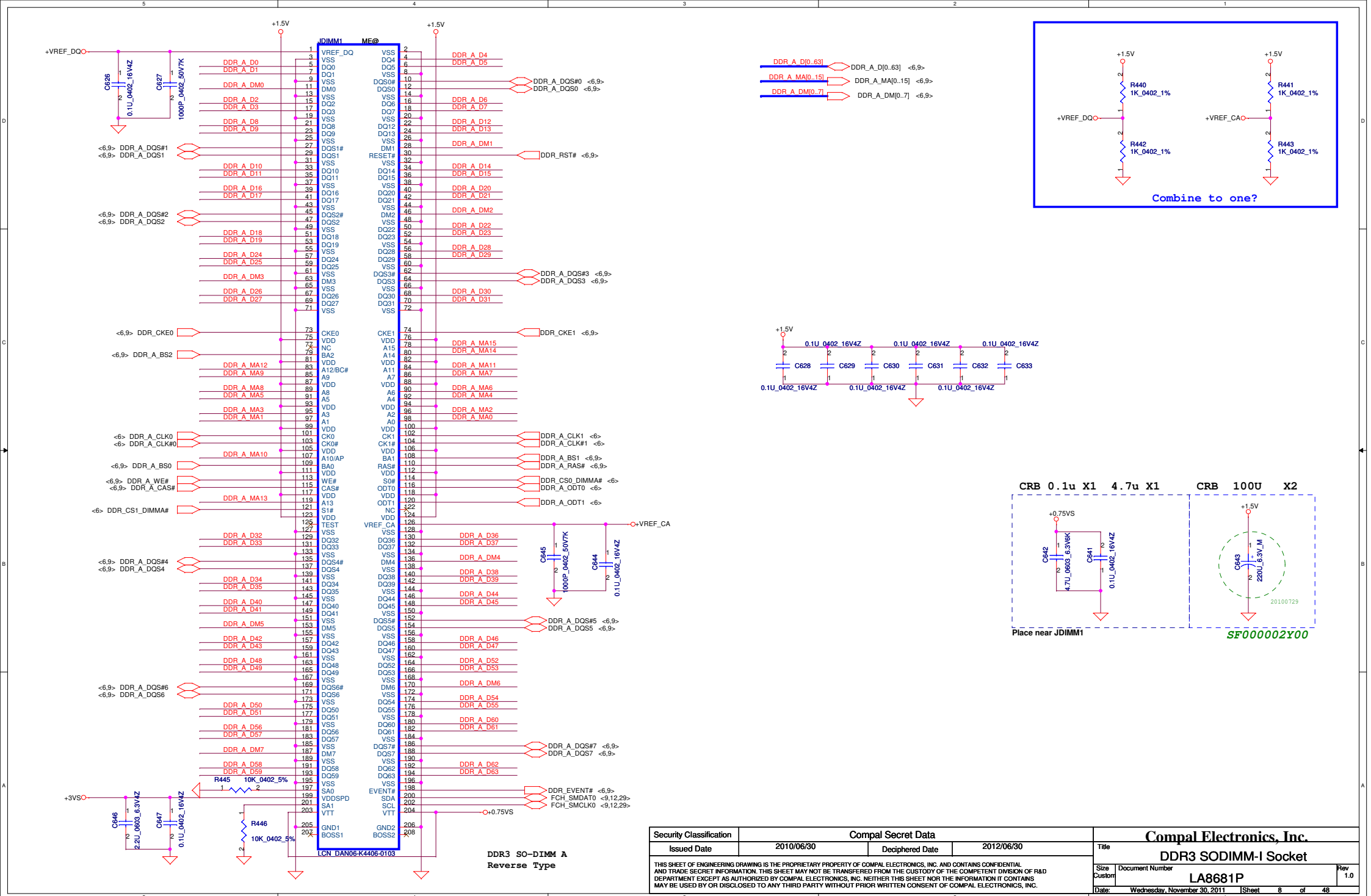


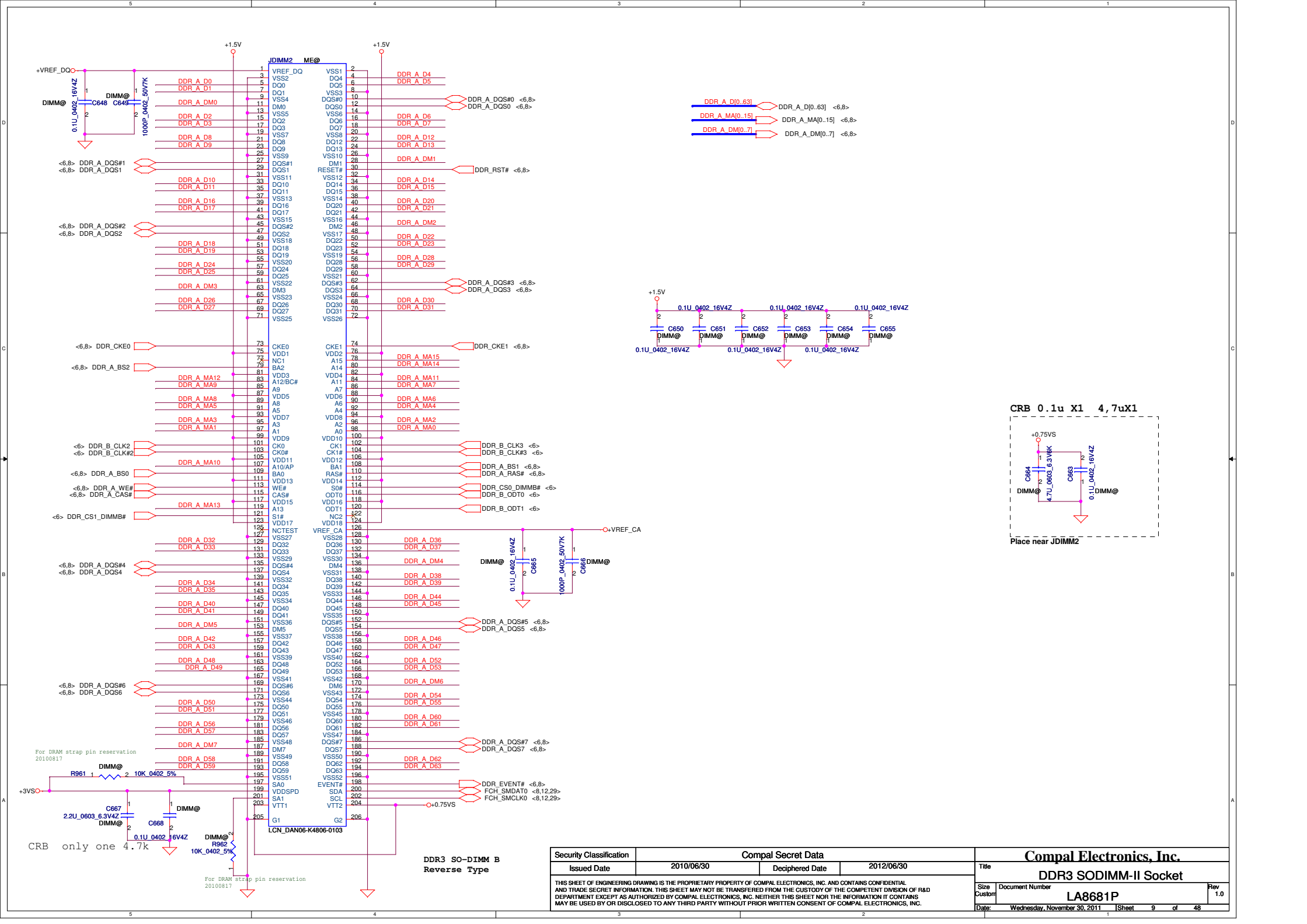
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C146 place close to FCH

C146 1 2 150P_0402_50V8J

LAN

WLAN

VGA

WLAN

LAN

S IC 218-0755091 A13 HUDSON-M3L FCBGA 656P C38

APU_PCIE_RST #: Reset PCIe device on APU

MC74VHC1G08DFT2G SC70 5P

APU_PCIE_RST# C

APU_PCIE_RST# <15,29>

R692/ C790 close to FCH

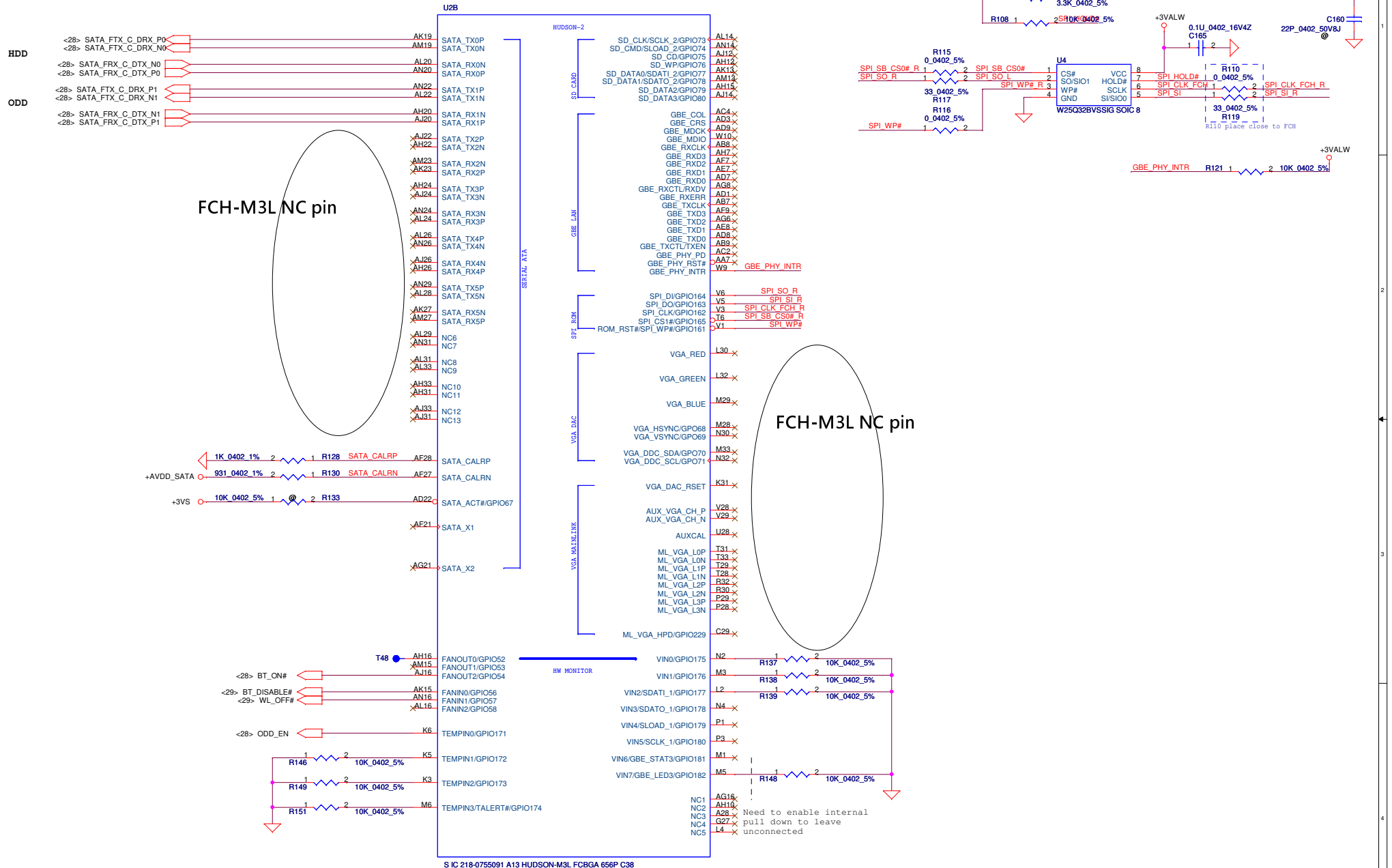
Module design have reserve GPIO44,45 for
VGA power enable and reset

change to 510 Ohm

for Clear CMOS

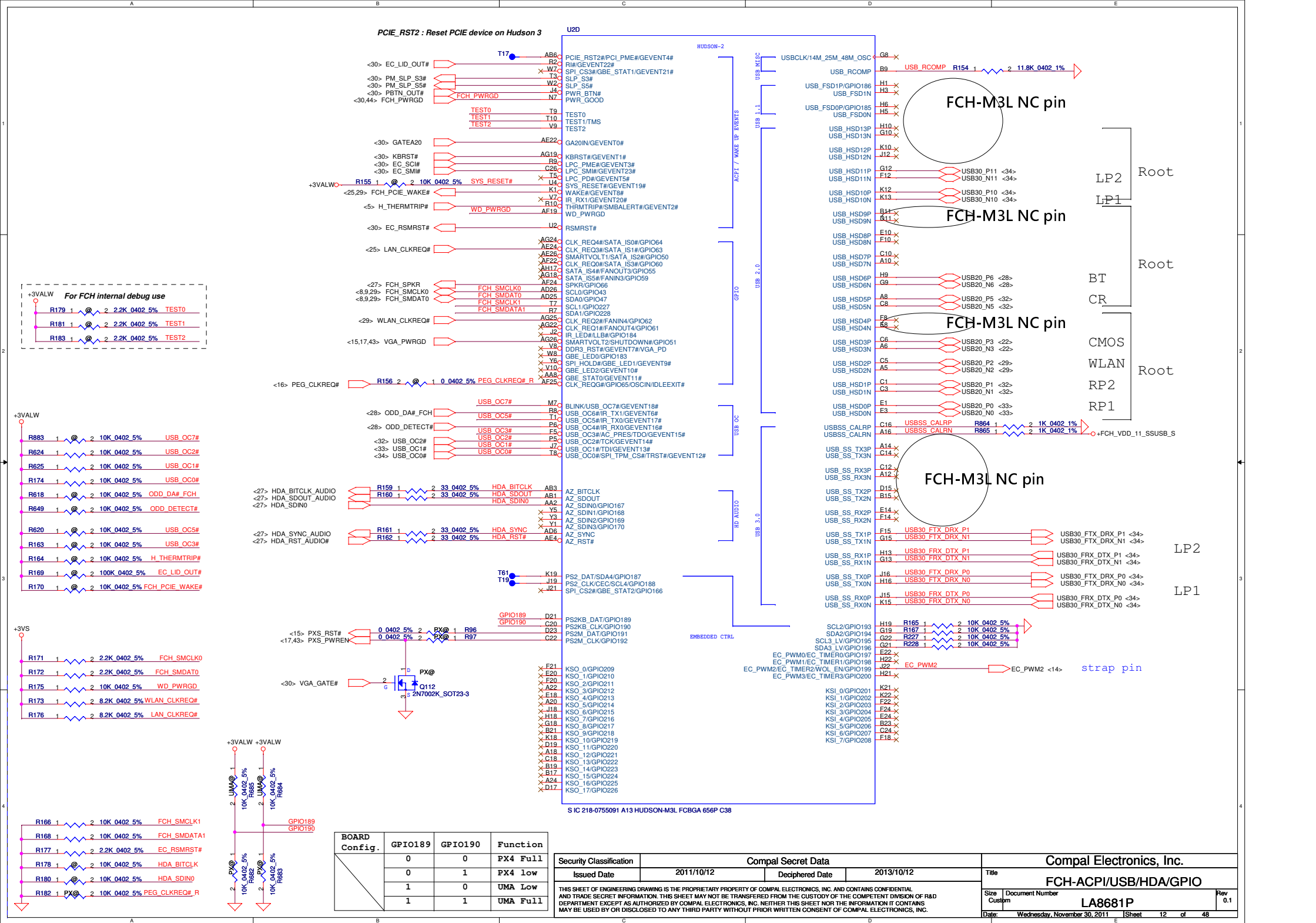
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								FCH PCIE/CLK/PCI/LPC/RTC	
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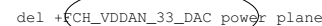
4MB SPI ROM & Non-share ROM.



S I C 218-0755091 A13 HUDSON-M3L FCBGA 656P C38

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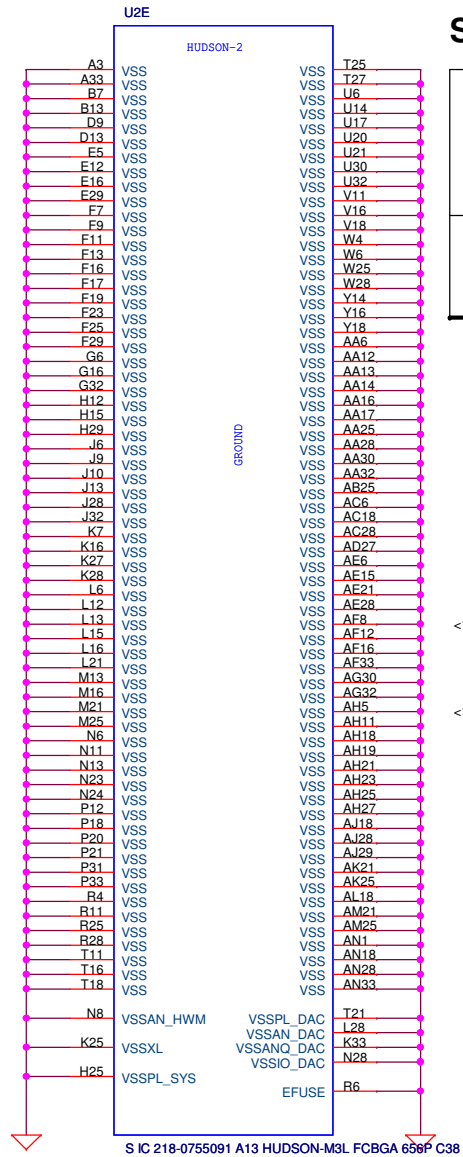
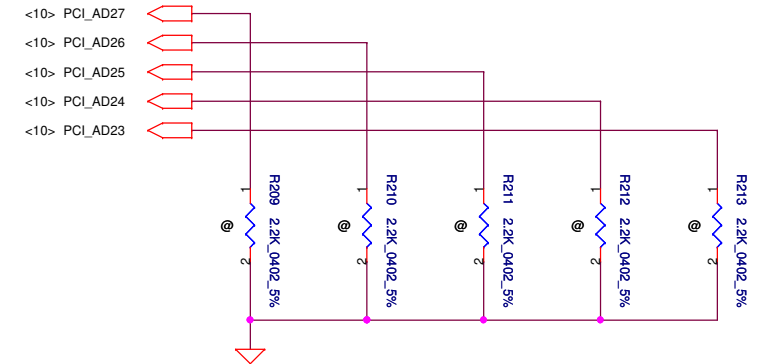
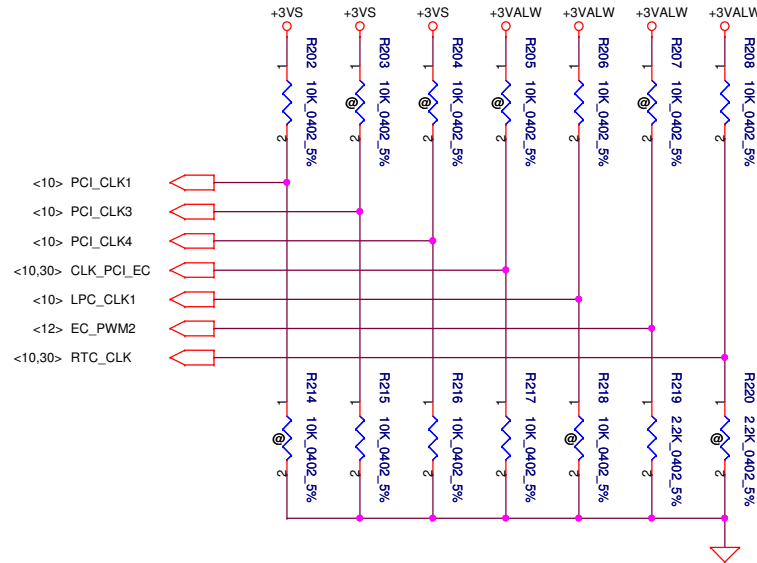
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

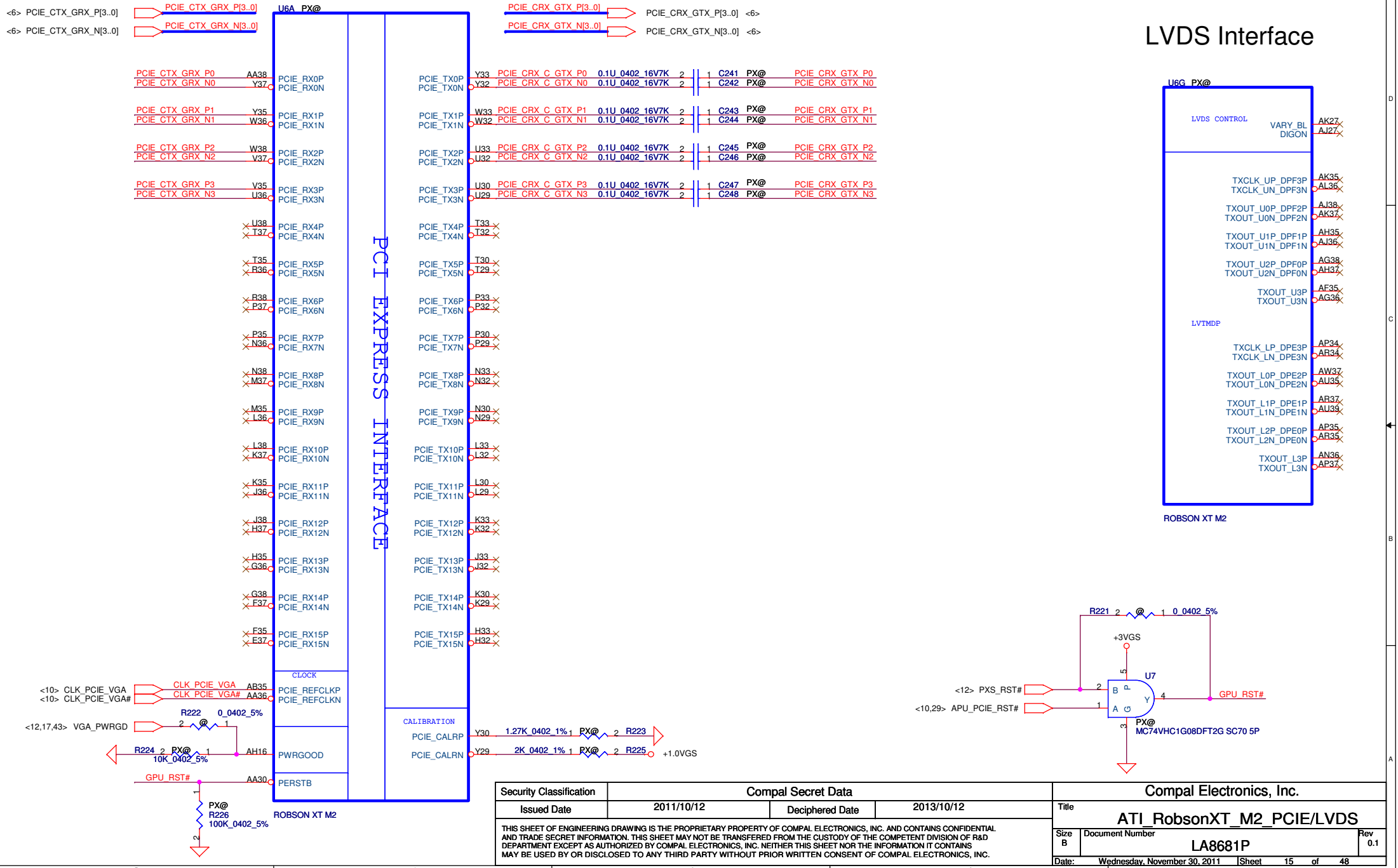
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



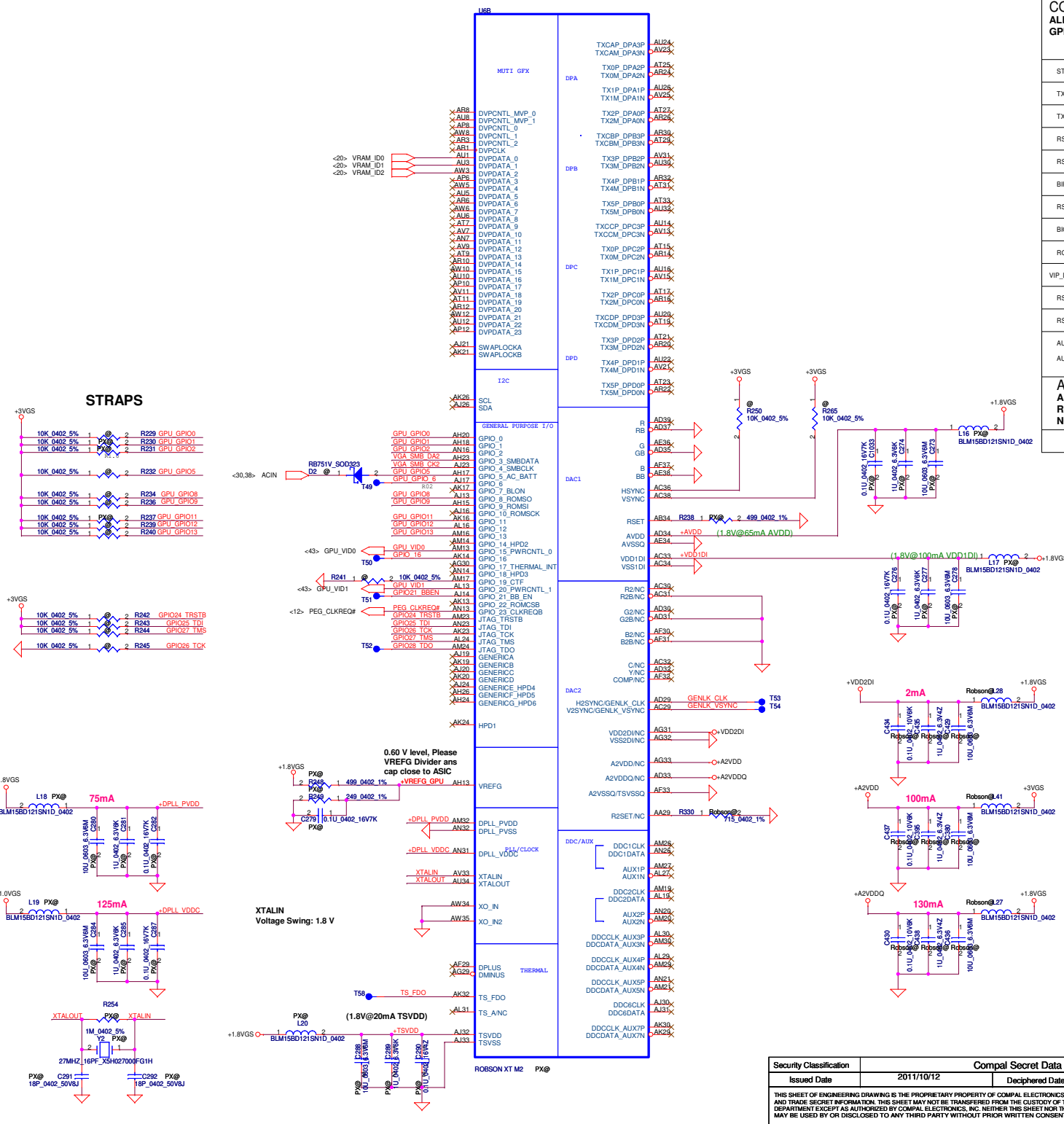
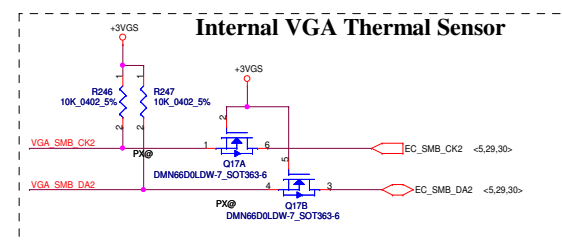
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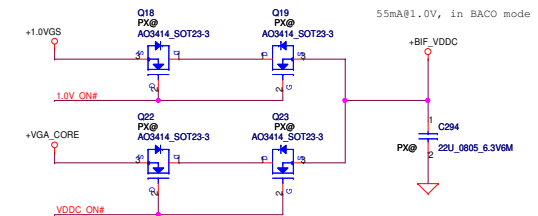
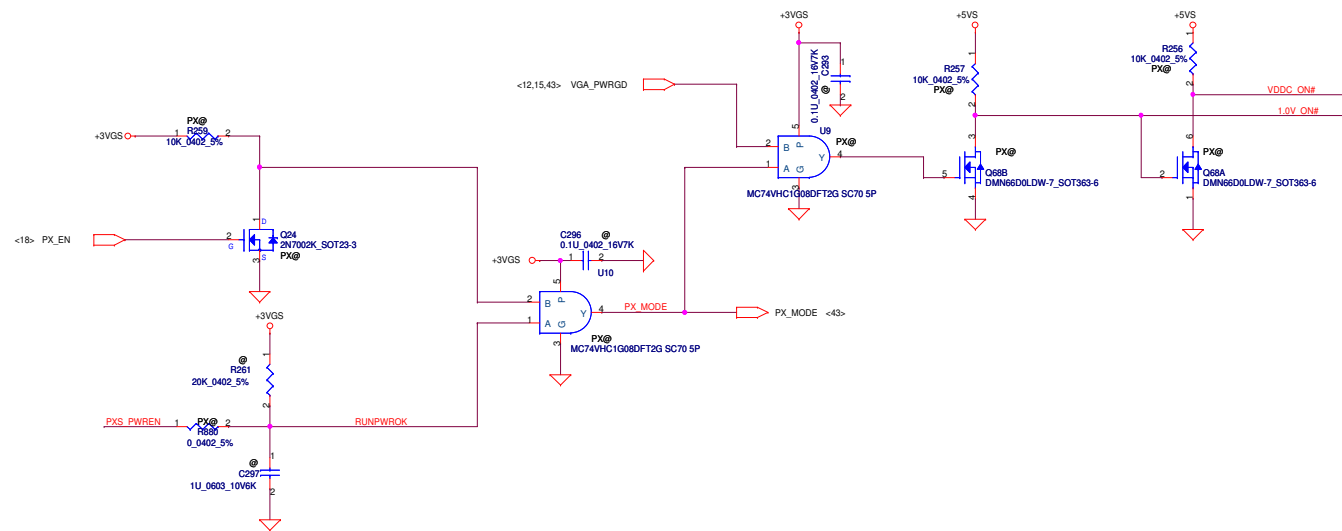
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CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET					
0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE					
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing		X	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable		X	
RSVD	GPIO2	Advertises PCIe speed when compliance test 0: 2.5Gt/s 1: 5Gt/s		0	
RSVD	GPIO8	RESERVED		0	
BIF_VGA_DIS	GPIO9	VGA ENABLED		0	
RSVD	GPIO21	RESERVED		0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable		X	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX	
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0	
RSVD	H2SYNC			0	
RSVD	GENERICC			0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11	
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET					
GPIO21 H2SYNC GENERICC GPIO2 GPIO8					

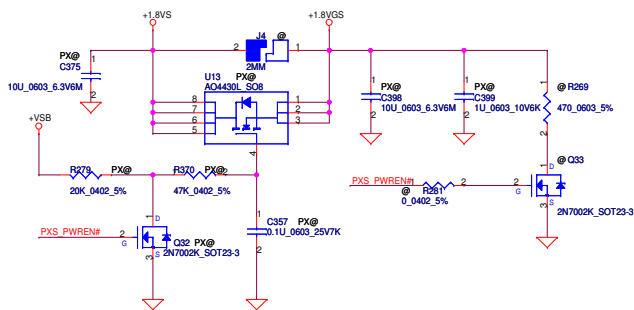
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



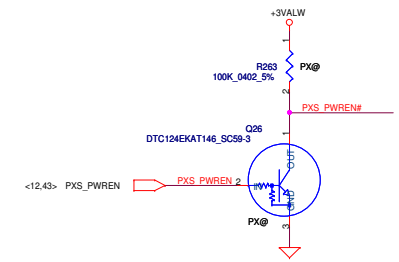
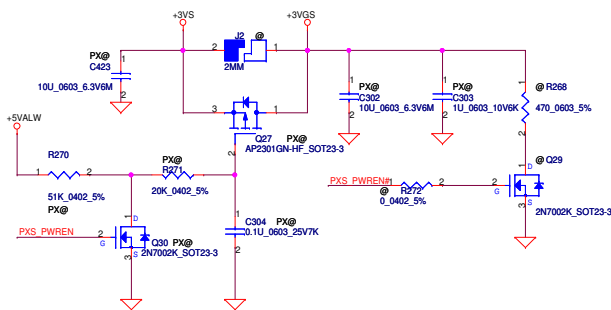
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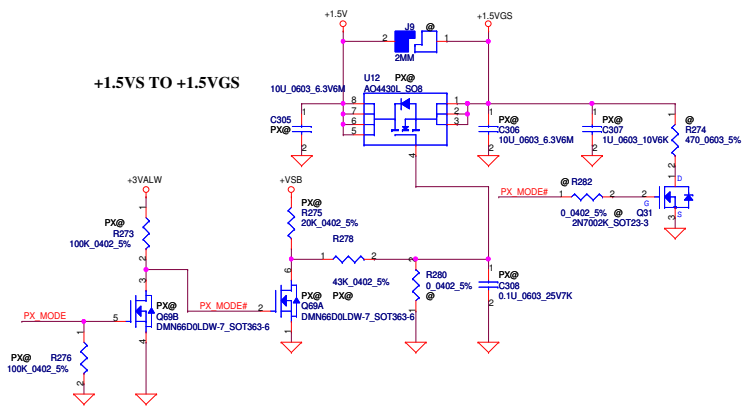
+1.8VS TO +1.8VGS



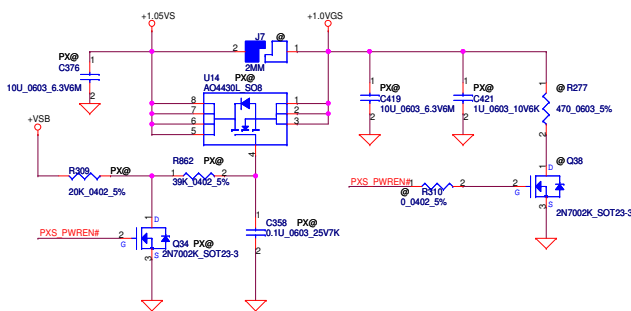
+3.3VS TO +3.3VGS



+1.5VS TO +1.5VGS



+1.0VS TO +1.0VGS



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

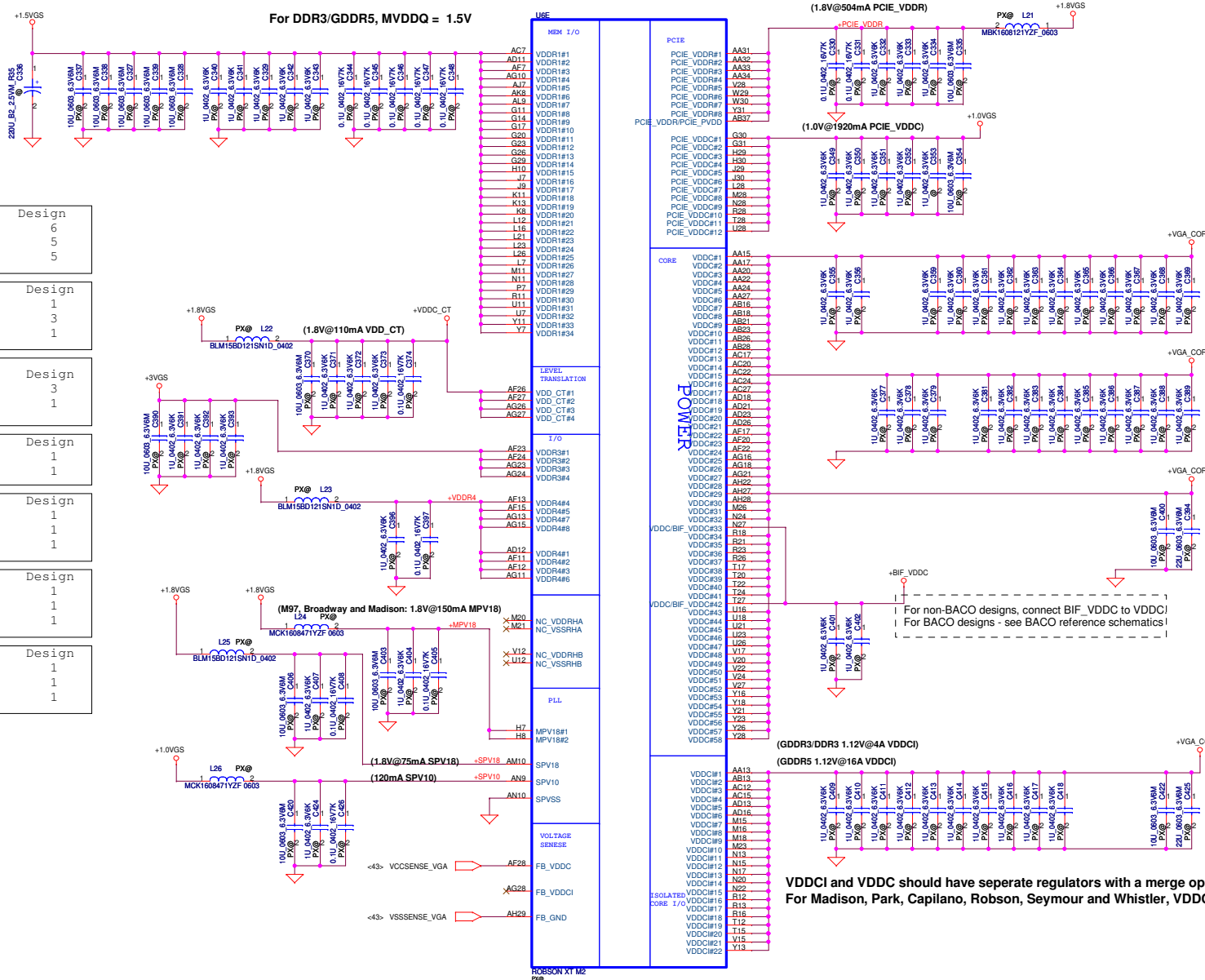
VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1



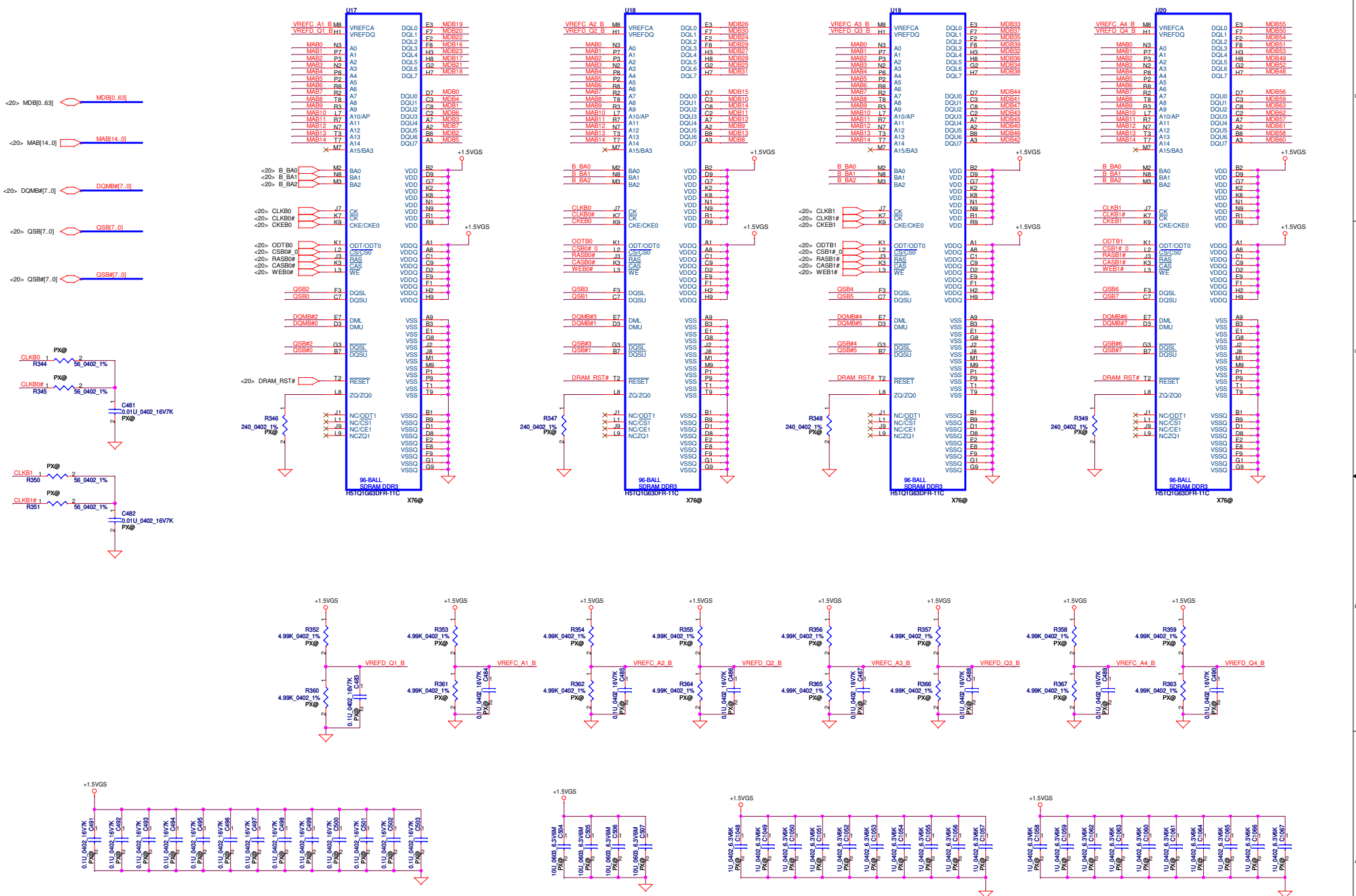
PCIe_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

PCIe_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

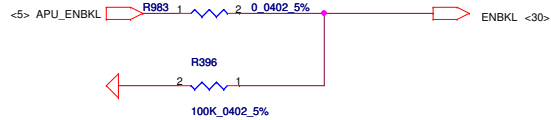
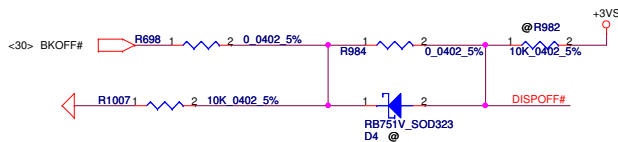
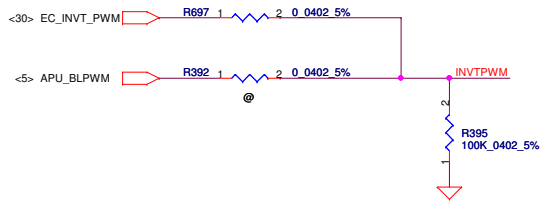
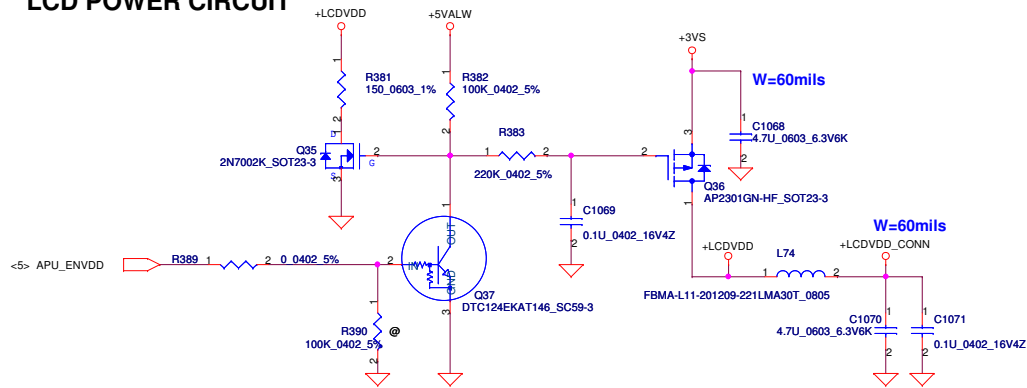
VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

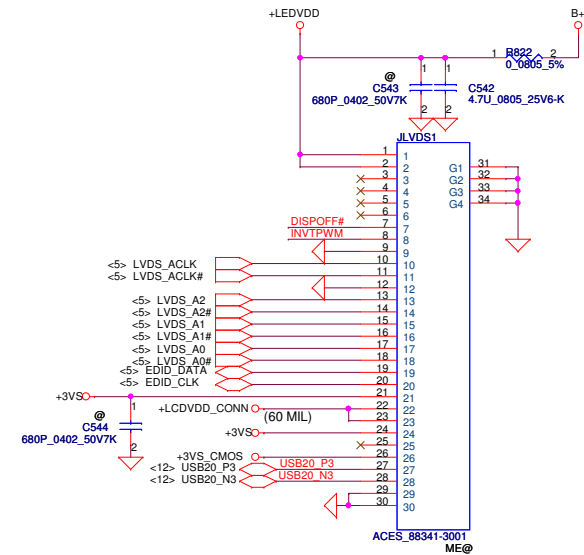
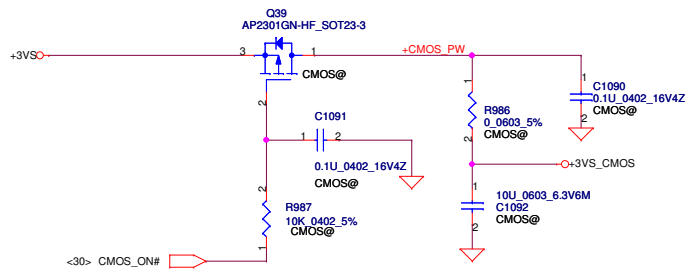
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Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title	ATI RobsonXT M2 MEM IF
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					LA8681P
Date:		Wednesday, November 30, 2011		Sheet	20 of 48



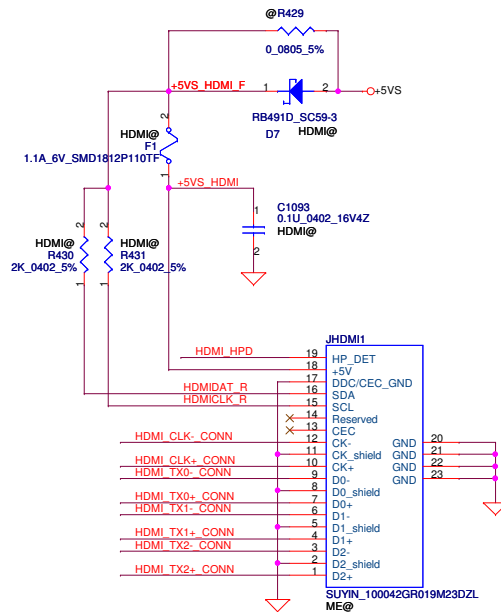
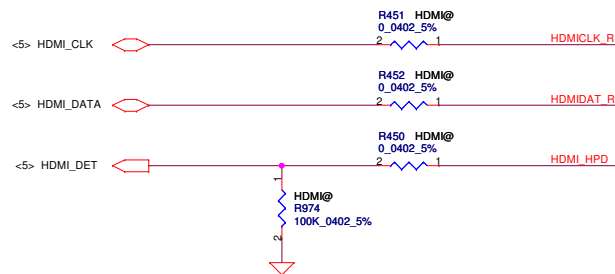
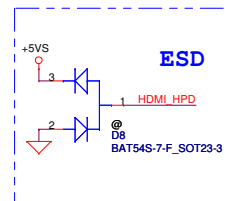
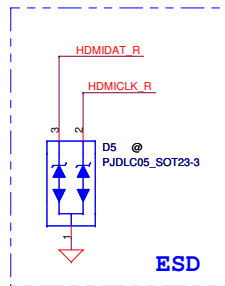
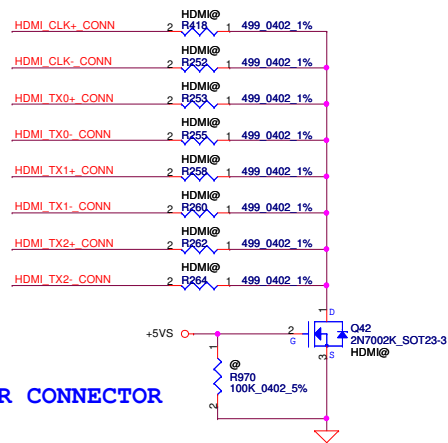
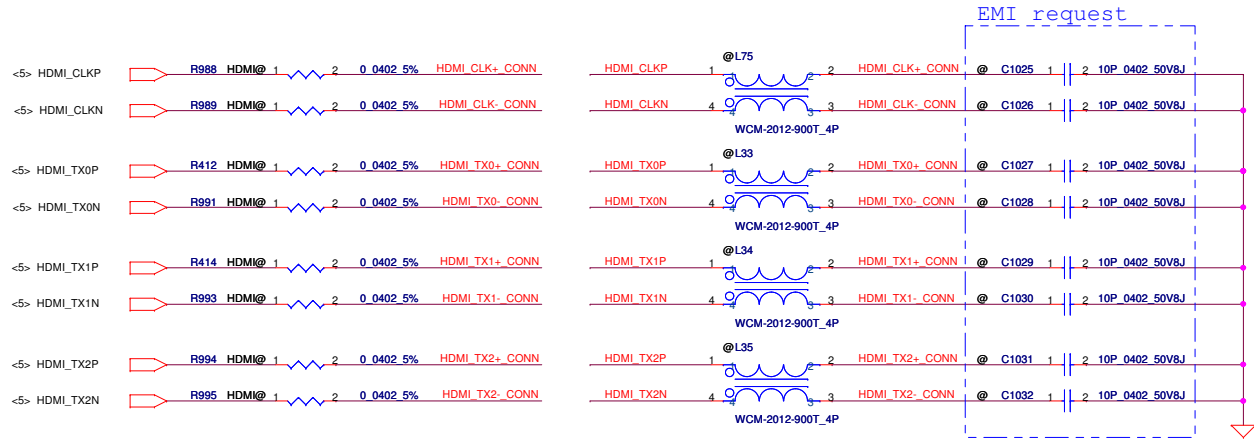
LCD POWER CIRCUIT



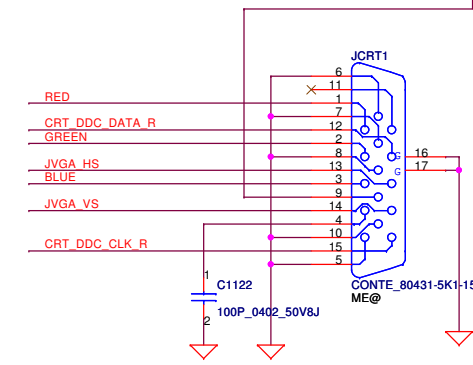
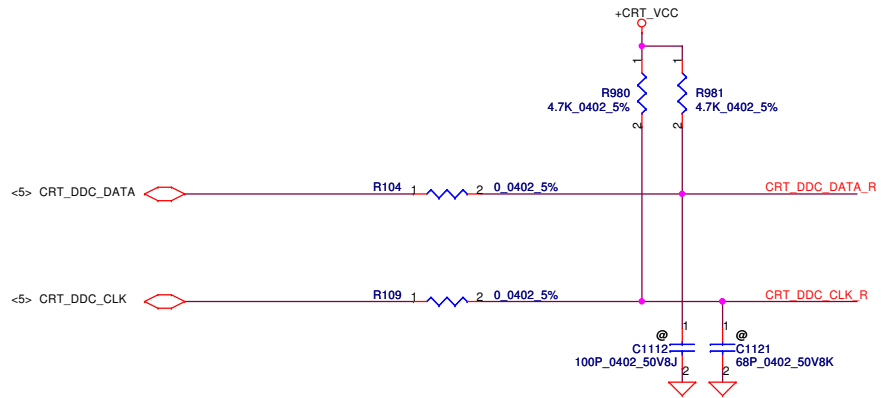
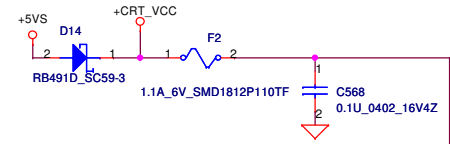
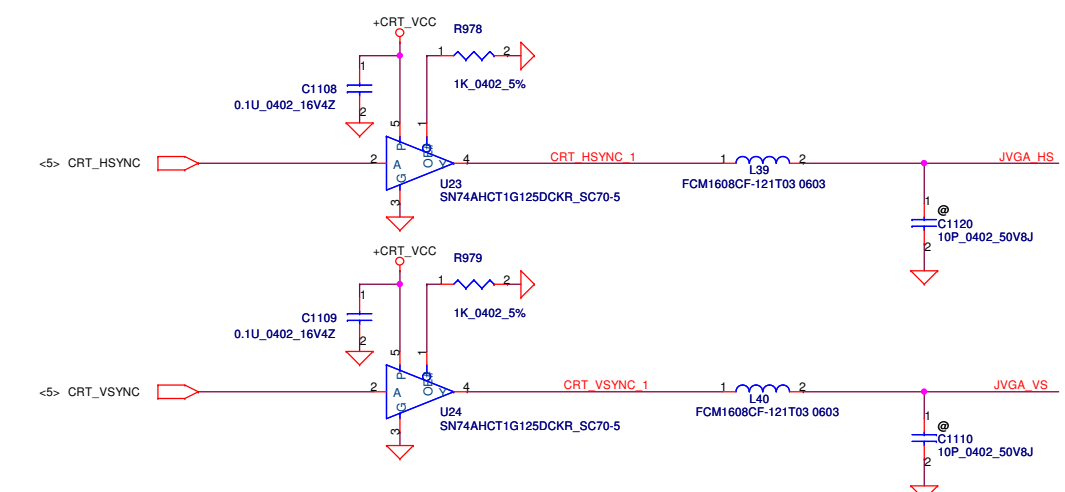
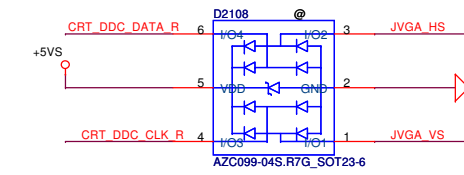
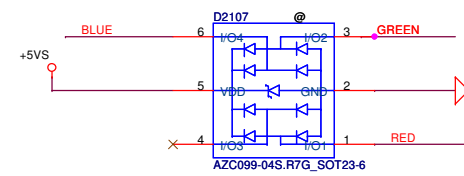
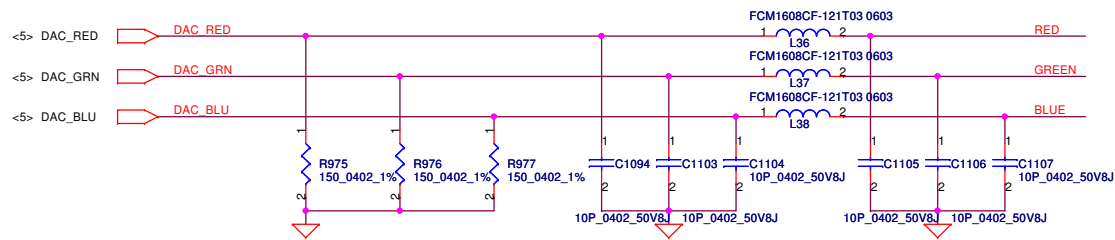
CMOS Camera



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					Size B	Document Number	LA8681P	Rev 0.1
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2011/10/12				2013/10/12				Title			
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								Document Number			
								Custom			
								LA8681P			
								Date			
								Wednesday, November 30, 2011			
								Sheet 23 of 48			
								Rev 0.1			

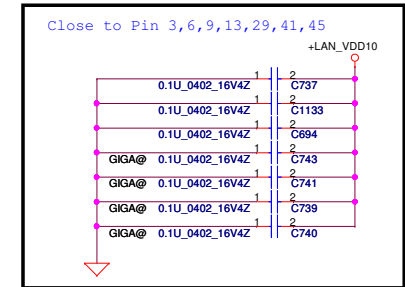


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Issued Date	2011/10/12	Deciphered Date	2013/10/12	CRT Connector	
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				Date: Wednesday, November 30, 2011	Sheet 24 of 48

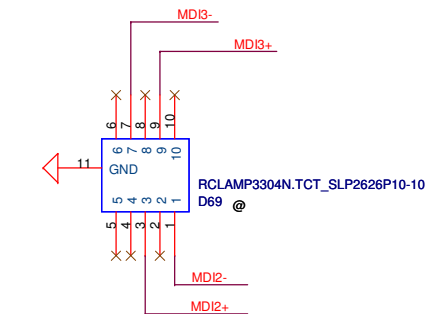
Compal Electronics, Inc.

CRT Connector

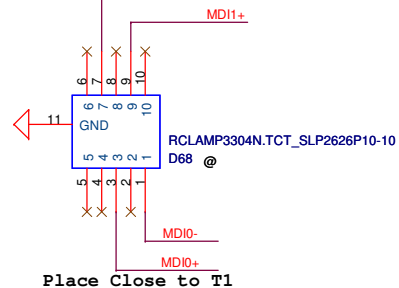
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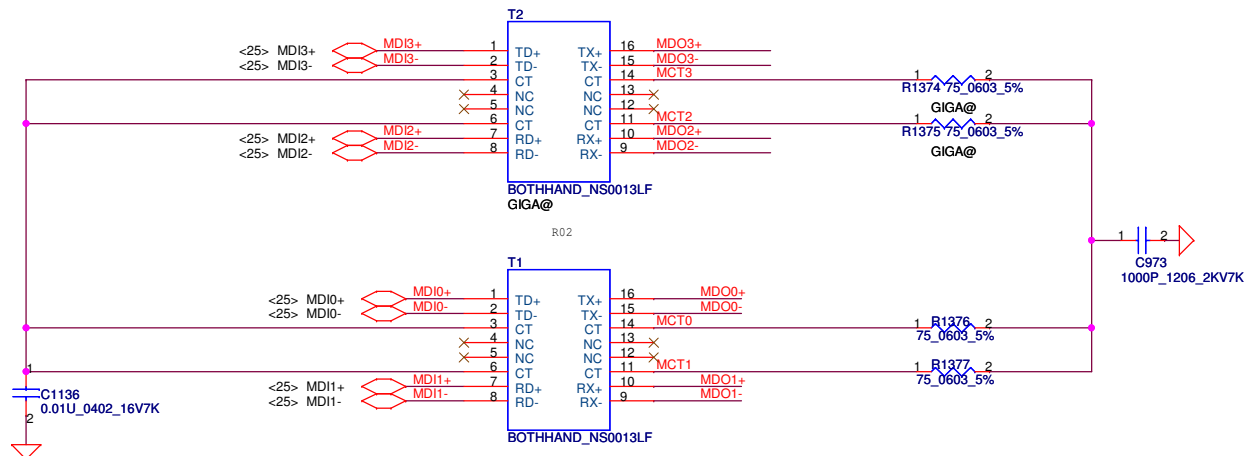
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Place Close to T2

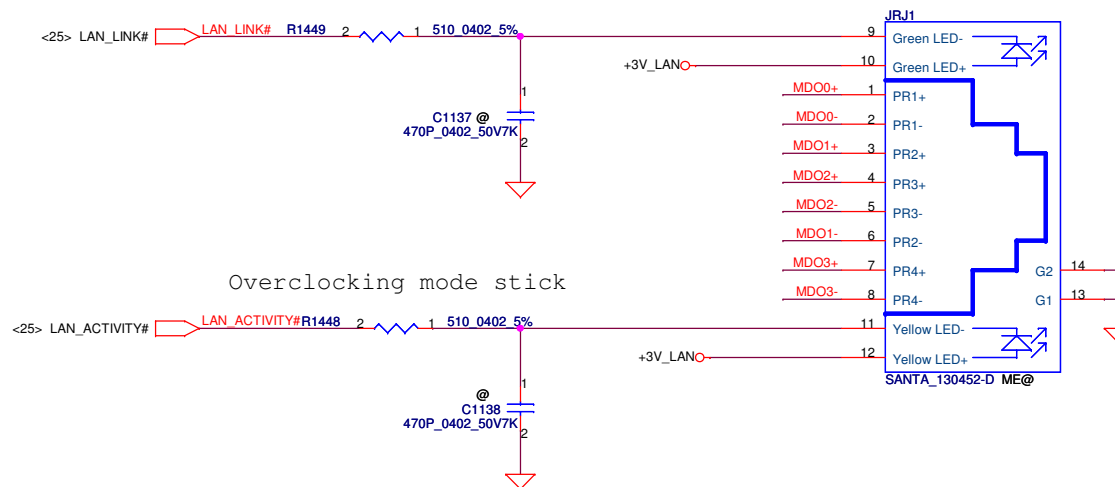


Place Close to T1

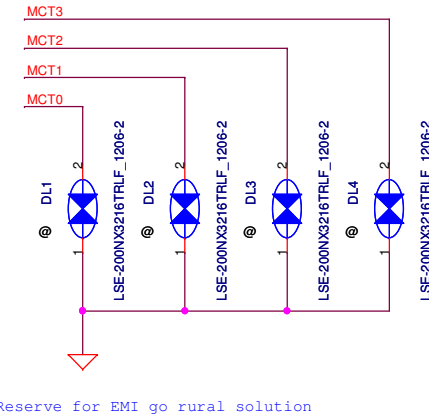


Reserve gas tube for EMI go rural solution

Place Close to T1,T2



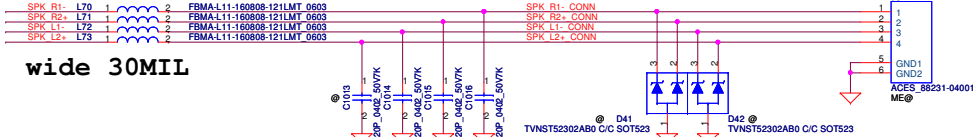
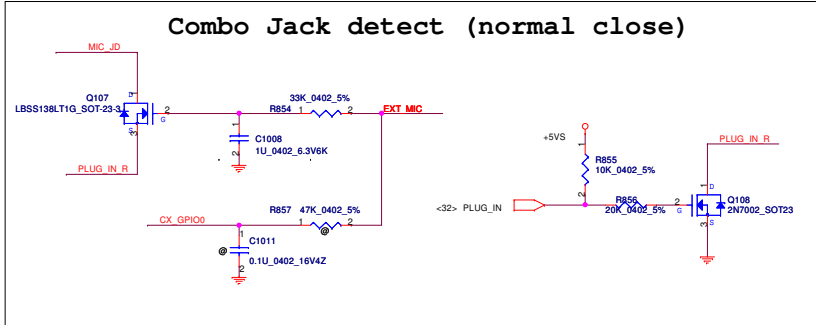
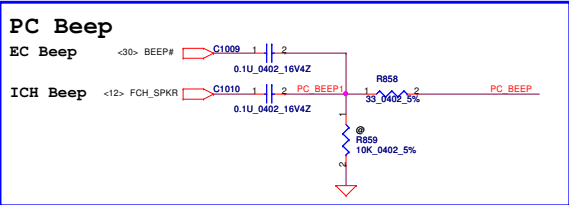
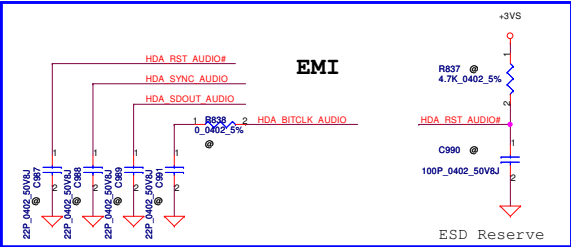
Overclocking mode stick



Reserve for EMI go rural solution

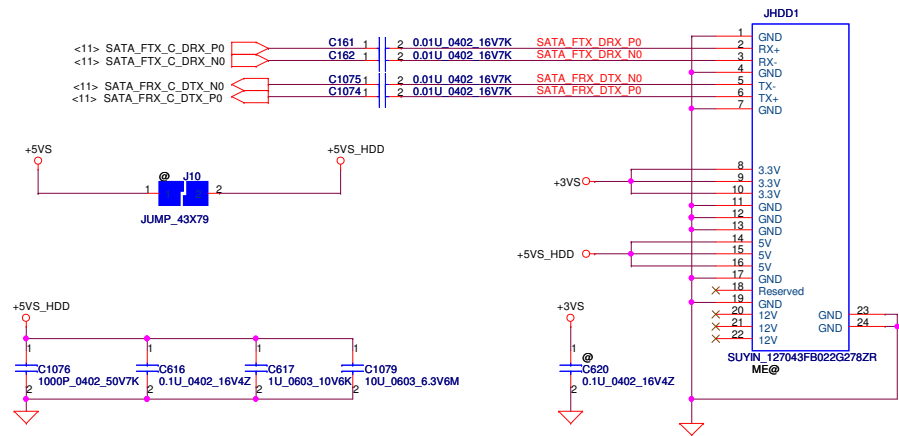
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Issued Date		2011/06/15		Deciphered Date		2012/07/11		Title			
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						Size	Document Number			Rev	
						A	LA-7984P			0.1	
						Date:	Wednesday, November 30, 2011		Sheet	26	of

An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).

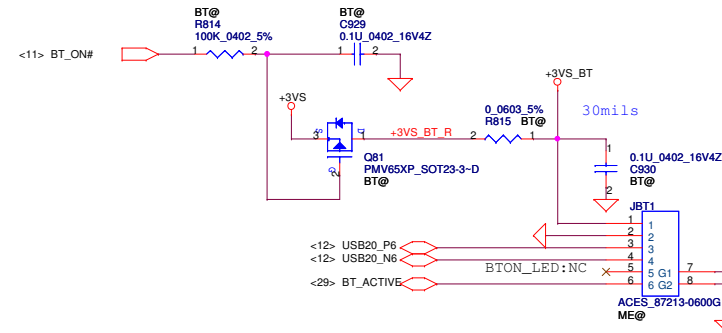


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Size	Document Number			Rev
Custom				0.1
Date:	Wednesday, November 30, 2011	Sheet	27	of 48

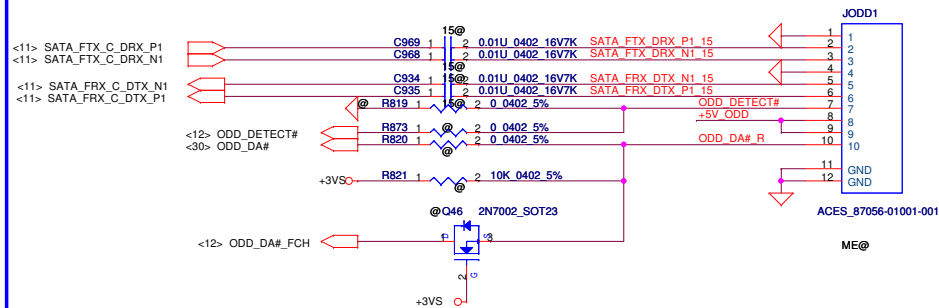
HDD CONN



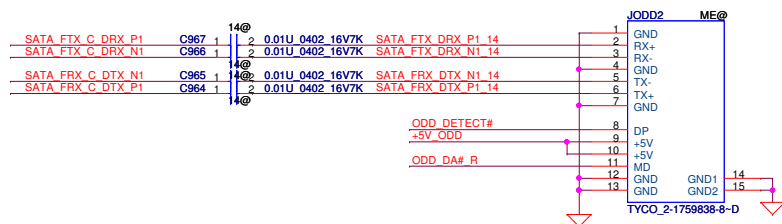
BT MODULE CONN



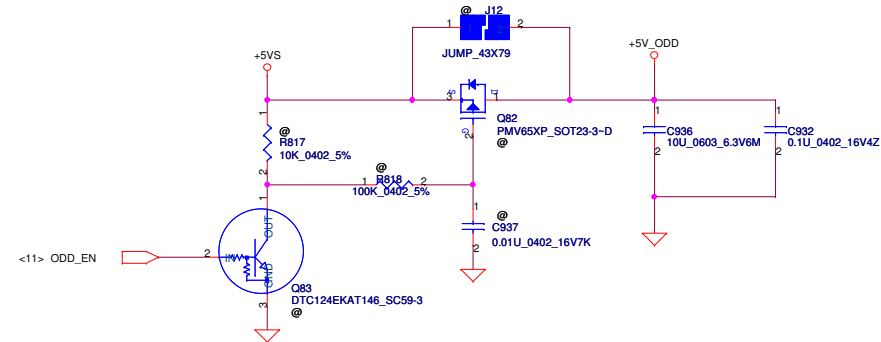
ODD CONN 15"



ODD CONN 14"

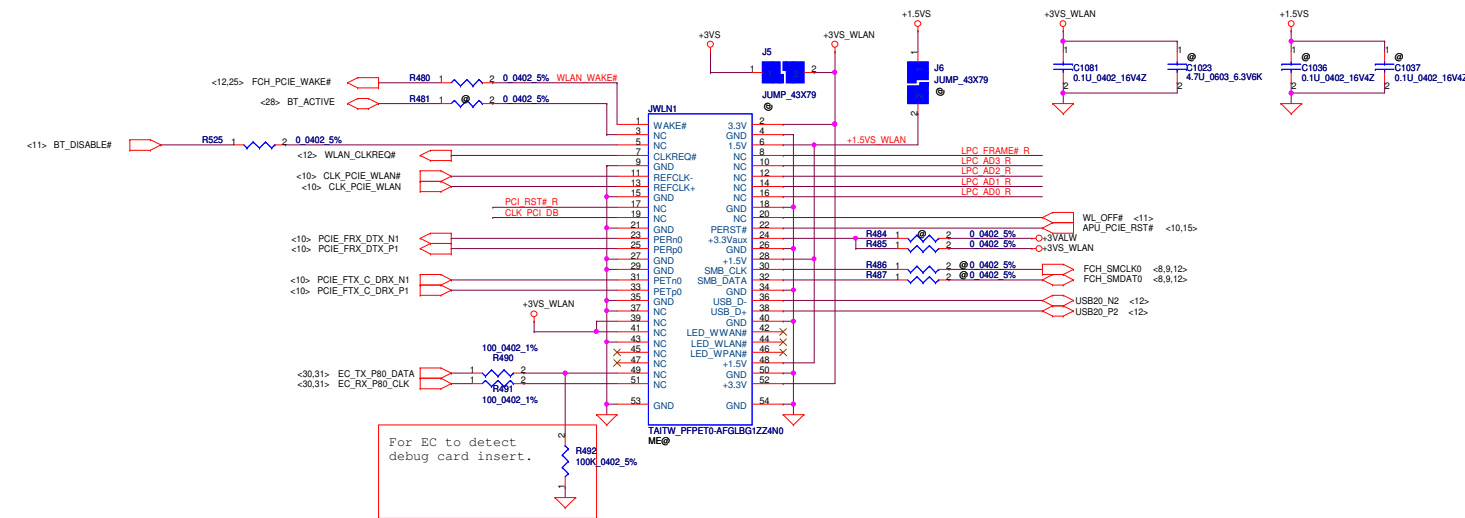


short J12, no zero power ODD function

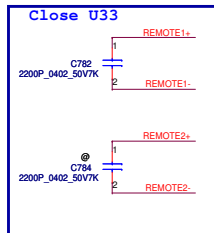
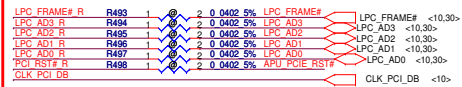


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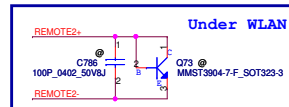
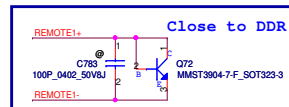
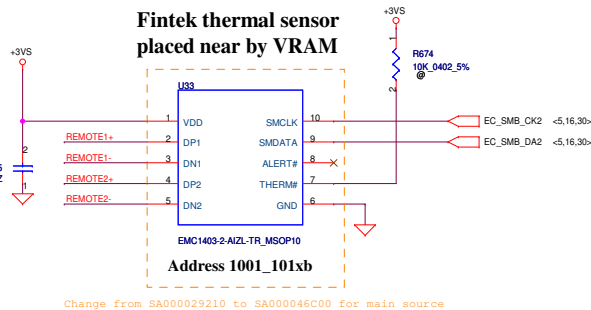
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

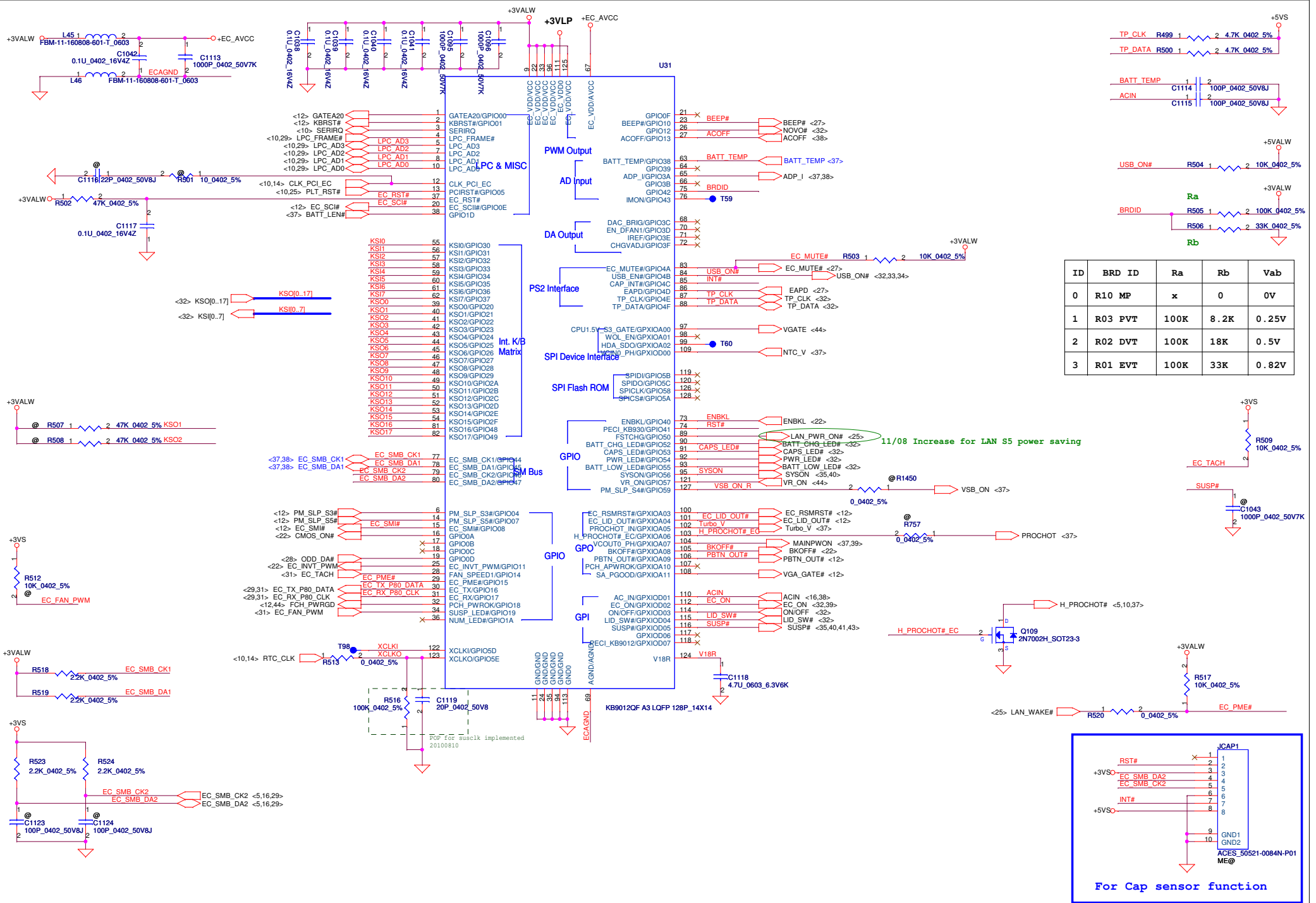


Fintek thermal sensor
placed near by VRAM

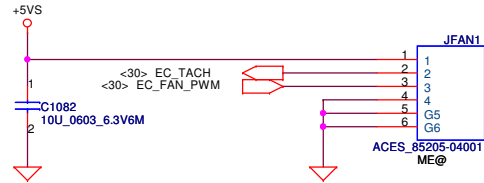


REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

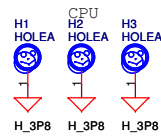
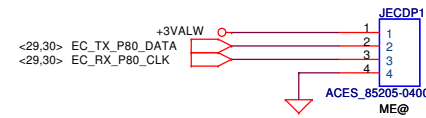
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				Size Document Number
				LA8681P
				Rev 0.1
				Date: Wednesday, November 30, 2011 Sheet 29 of 48



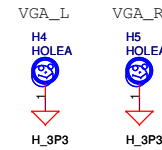
FAN CONN



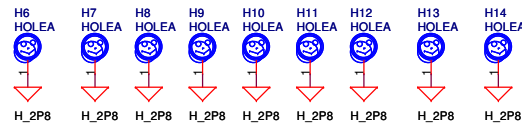
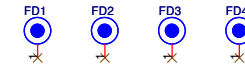
EC DEBUG PORT



A

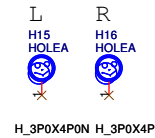


B



D

M/B 橢圓孔



M/B 圓孔



2P8 * 9 pcd

E

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Power Button

TOP Side

Bottom Side

3VLP

3VALW

R701 100K_0402_5%

RS35 100K_0402_5%

SW3 SW3 SMT1-05 4P

J13

R720 0.0402_5%

SHORT PADS

D24

DAN202U1106_SC70-3

Q106 2N7002_SCOT23-3

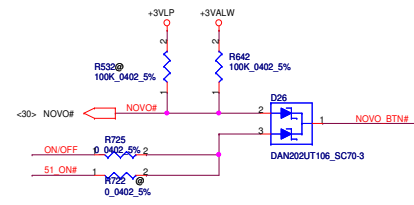
RS41 10K_0402_5%

EC_ON

ON/OFFBTN#

ON/OFF <30>

51_ON <36>



FOR 14"

Pin	Function	Pin	Function
KSQ0..7	<30>	KS11..1	KS12..1
KSQ0..17	<30>	KS12..1	KS13..1
KSQ2 C940 1	2 @ 100P 0402 50V8U	KS13..1	KS14..1
KSQ15 C942 1	2 @ 100P 0402 50V8U	KS14..1	KS15..1
KSQ4 C944 1	2 @ 100P 0402 50V8U	KS15..1	KS16..1
KSQ8 C946 1	2 @ 100P 0402 50V8U	KS16..1	KS17..1
KSQ13 C948 1	2 @ 100P 0402 50V8U	KS17..1	KS18..1
KSQ12 C950 1	2 @ 100P 0402 50V8U	KS18..1	KS19..1
KSQ11 C952 1	2 @ 100P 0402 50V8U	KS19..1	KS20..1
KSQ10 C954 1	2 @ 100P 0402 50V8U	KS20..1	KS21..1
KSQ3 C956 1	2 @ 100P 0402 50V8U	KS21..1	KS22..1
KSQ4 C958 1	2 @ 100P 0402 50V8U	KS22..1	KS23..1
KSQ0 C960 1	2 @ 100P 0402 50V8U	KS23..1	KS24..1
KSQ0 C962 1	2 @ 100P 0402 50V8U	KS24..1	KS25..1
		KS25..1	KS26..1
		KS26..1	KS27..1
		KS27..1	KS28..1
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		KS90..1	KS91..1
		KS91..1	KS92..1
		KS92..1	KS93..1
		KS93..1	KS94..1
		KS94..1	KS95..1
		KS95..1	KS96..1
		KS96..1	KS97..1
		KS97..1	KS98..1
		KS98..1	KS99..1
		KS99..1	KS100..1
		KS100..1	KS101..1
		KS101..1	KS1

The diagram shows the JPWRB1 ME@ component with the following connections:

- +5VALW** connected to pin 1.
- NOVO BTN# ON/OFFBTN#** connected to pin 2.
- D25 @ PJSOT24C 3P C/A SOT-23** connected to pin 3.
- E-T-7182C-F04N-00R** connected to pin 4.
- G1** connected to pin 5.
- G2** connected to pin 6.

White LED1 14@

<30> PWR_LED# PWR_LED# 1 2 2 R644 14@ 300 5402.5% 3VSWALV

19-213A-T1D-CP2Q2HY-3T_WHITE

BATT_LOW_LED# **Orange** LED2 14@

<30> BATT_LOW_LED# BATT_LOW_LED# 1 2 2 R764 14@ 300 5402.5% 3VSWALV

2nd source SC500005910 S
LED L7ST-C191KFT-K5-A 0603 GRANT-191UD05_AMBER

BATT_CHG_LED# **White** LED3 14@

<30> BATT_CHG_LED# BATT_CHG_LED# 1 2 2 R755 14@ 300 5402.5% 3VSWALV

19-213A-T1D-CP2Q2HY-3T_WHITE

White LED4 14@

<30> CAPS_LED# CAPS_LED# 1 2 2 R8 14@ 300 5402.5% 3VSWALV

19-213A-T1D-CP2Q2HY-3T_WHITE

Pin connection diagram for the ACES 51524-0100N-01T ME0. The diagram shows a 16-pin connector on the left and a 16-pin header on theright. Pin 1 is HP_OUTR, Pin 2 is HP_OUTL, Pin 3 is EXT_MIC, and Pin 4 is PLUG_IN. Pins 5-8 are USB0_N1, USB0_P1, USB0_N5, and USB0_P5 respectively. Pins 9-16 are CX_GPIO0, MICBIASB, R90VANG0, R90VANG1, R90VANG2, R90VANG3, R90VANG4, and R90VANG5. The diagram also shows connections to JCR1, GND, and ME0.

LED B/D Conn

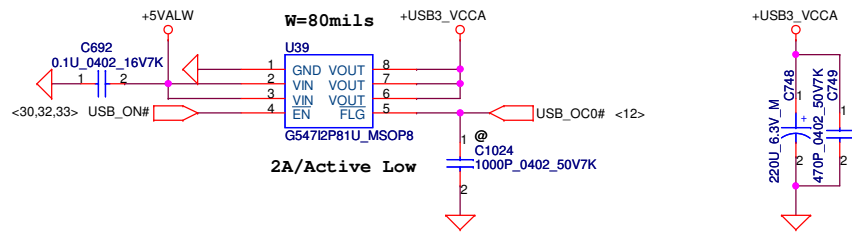
Signal	Pin
5V	1
5V	2
LED SW#	3
PWR LED#	4
BATT LOW LED#	5
BATT CHG LED#	6
CAPS LED#	7
SW R	8
SW L	9
GND	10
GND	11
GND	12

ACES 8805S-12CN
ME®

[illegible]

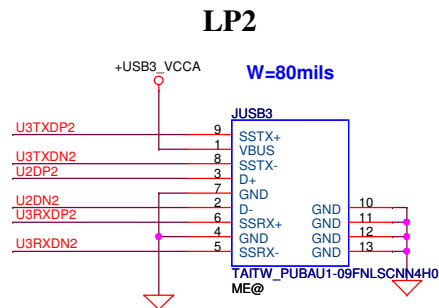
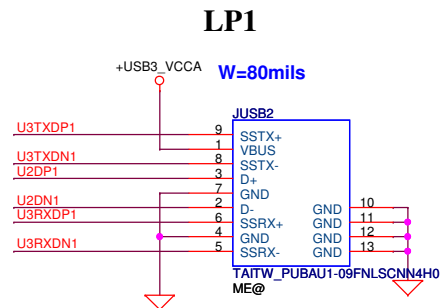
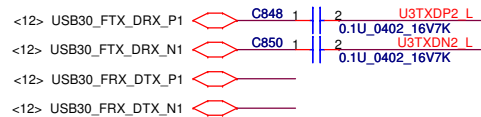
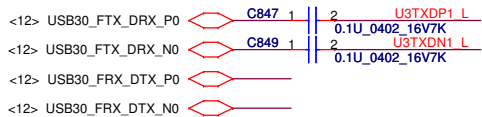
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Date:					Wednesday, November 20, 2013 10:58 AM		

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					Size B	Document Number	LA8681P	Rev 0.1
					Date:	Wednesday, November 30, 2011	Sheet 33	of 48

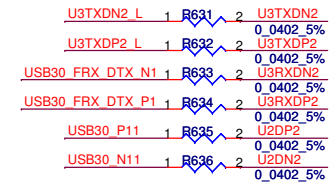
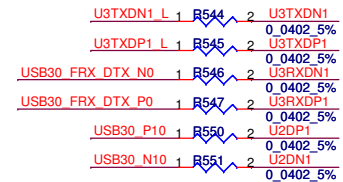
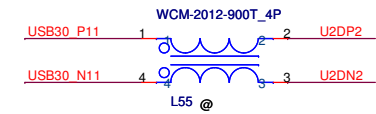
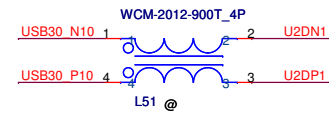
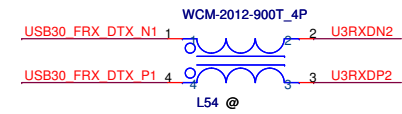
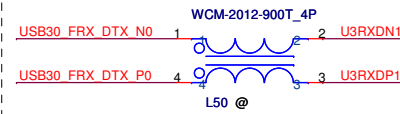
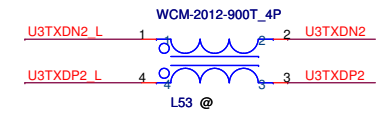
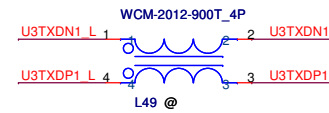
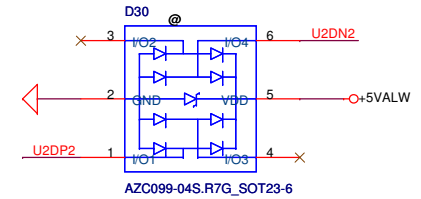
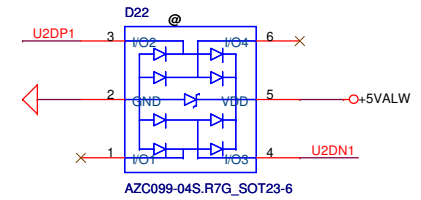
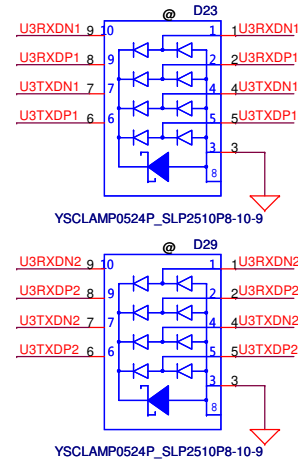


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<12> USB30_P10

<12> USB30_N11
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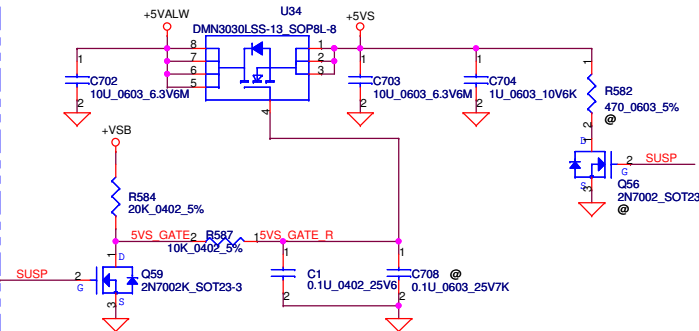


For EMI/ESD request

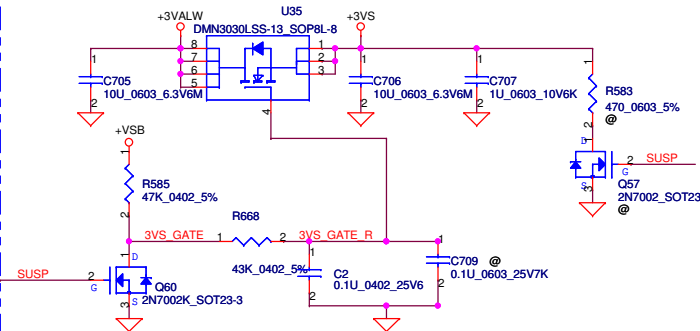


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				LA8681P	
				Date:	Wednesday, November 30, 2011
				Sheet	34 of 48

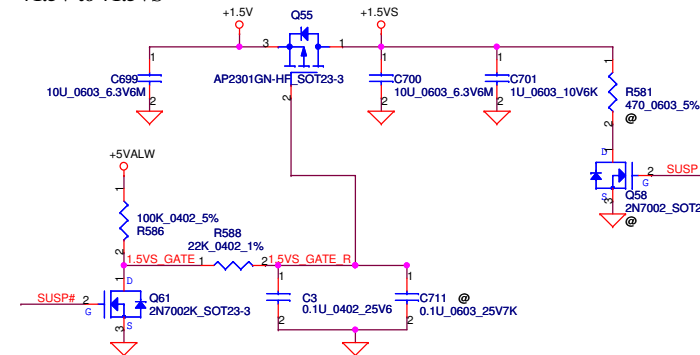
+5VALW TO +5VS



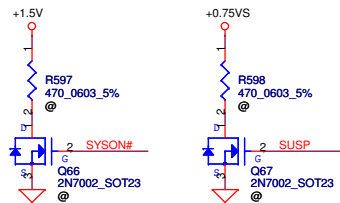
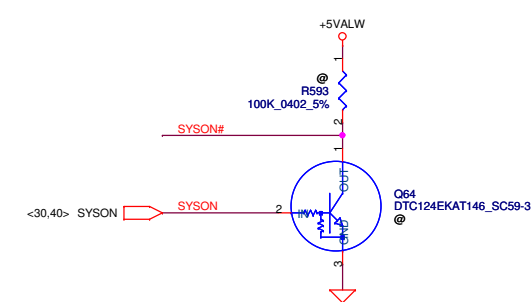
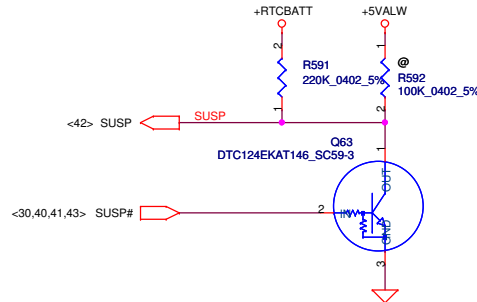
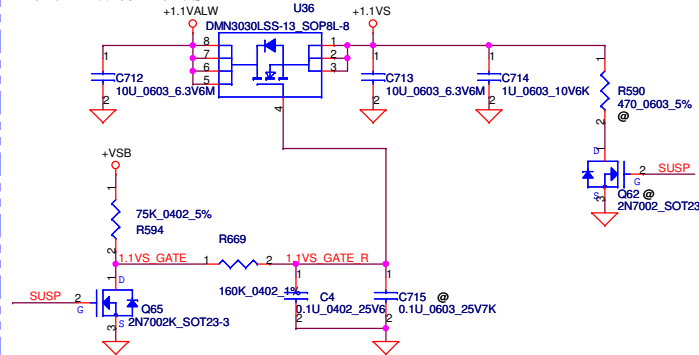
+3VALW TO +3VS



+1.5V to +1.5VS



+1.1VALW to +1.1VS

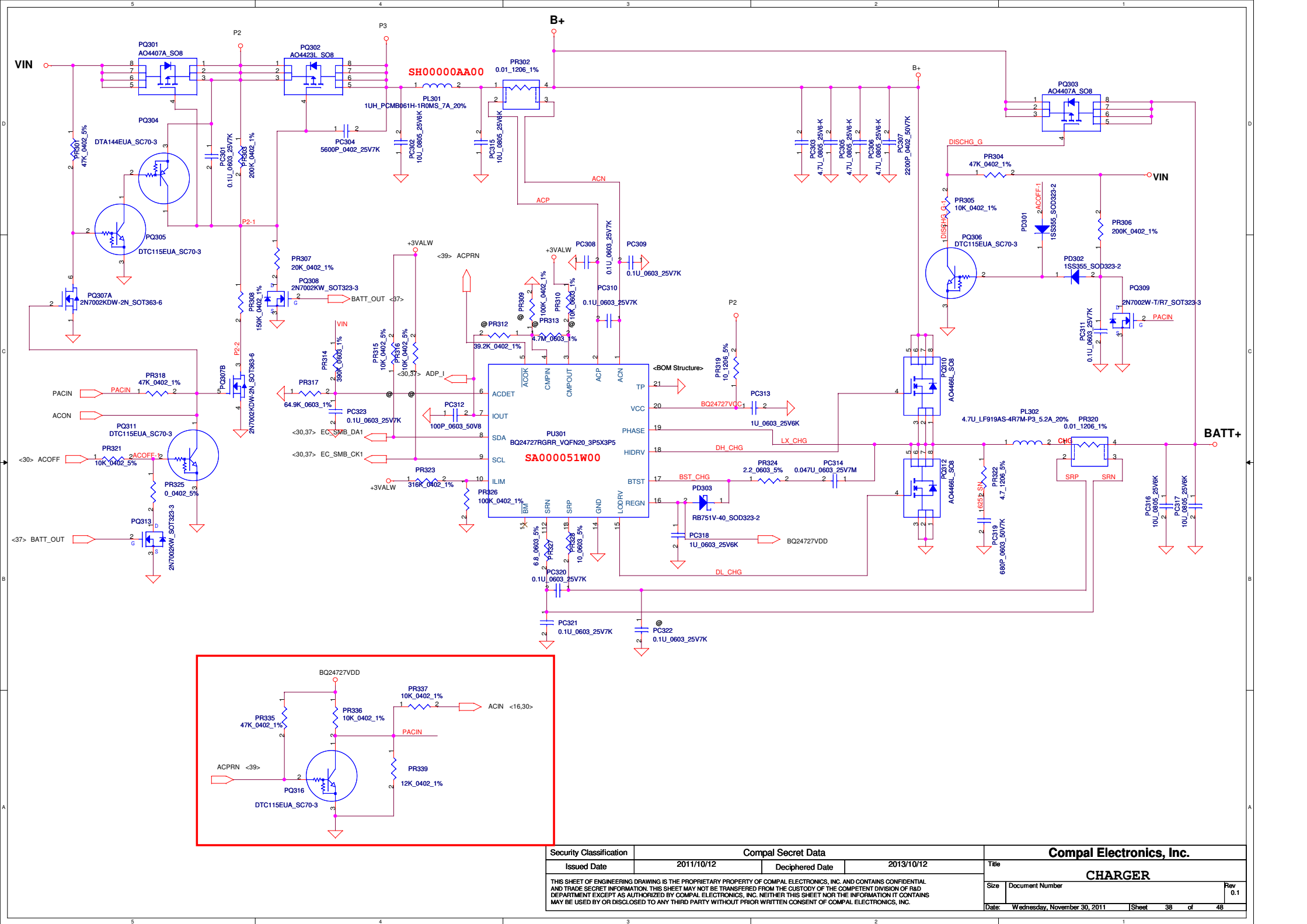


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										Rev 0.1	
										Date: Wednesday, November 30, 2011	
										Sheet 35 of 48	

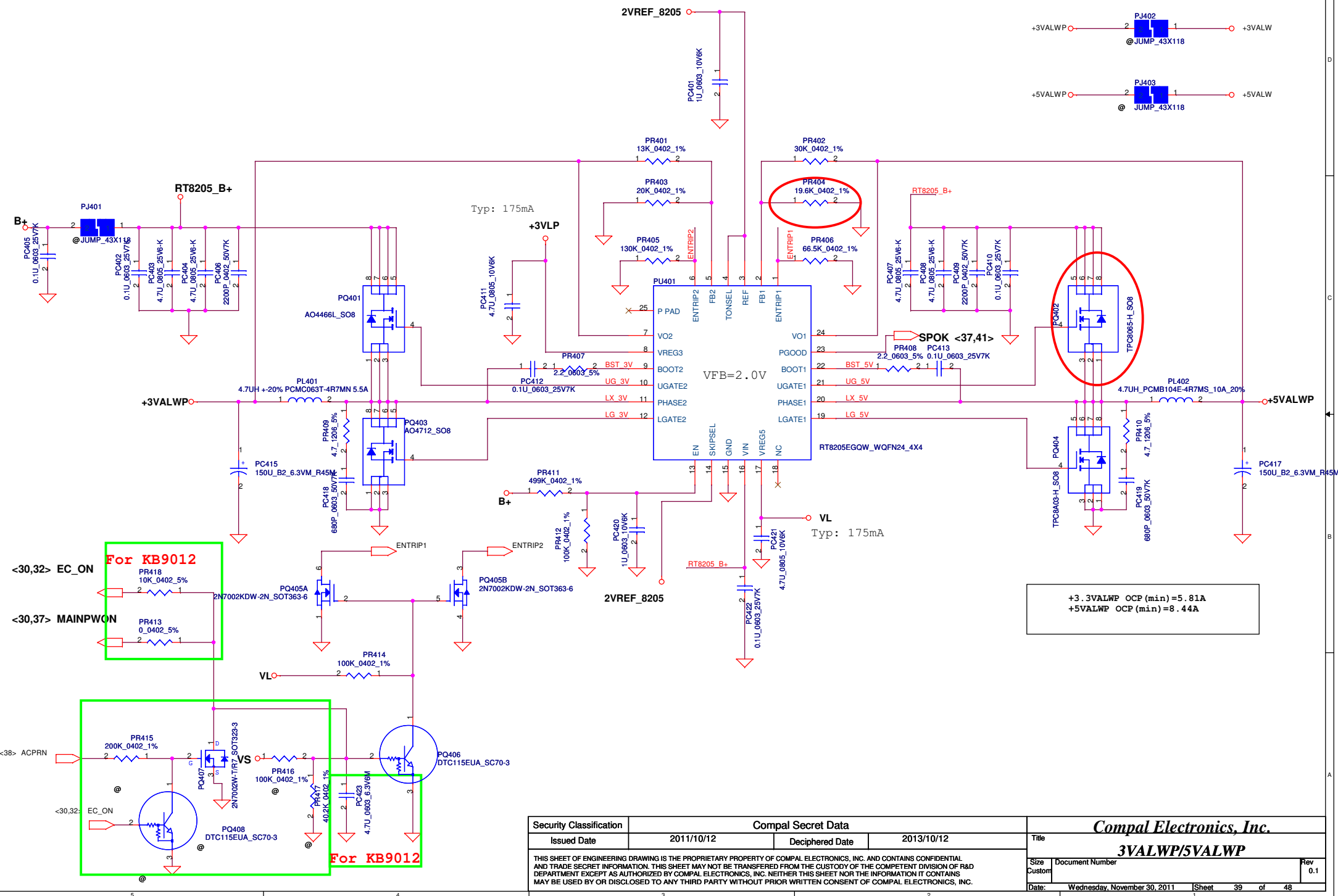
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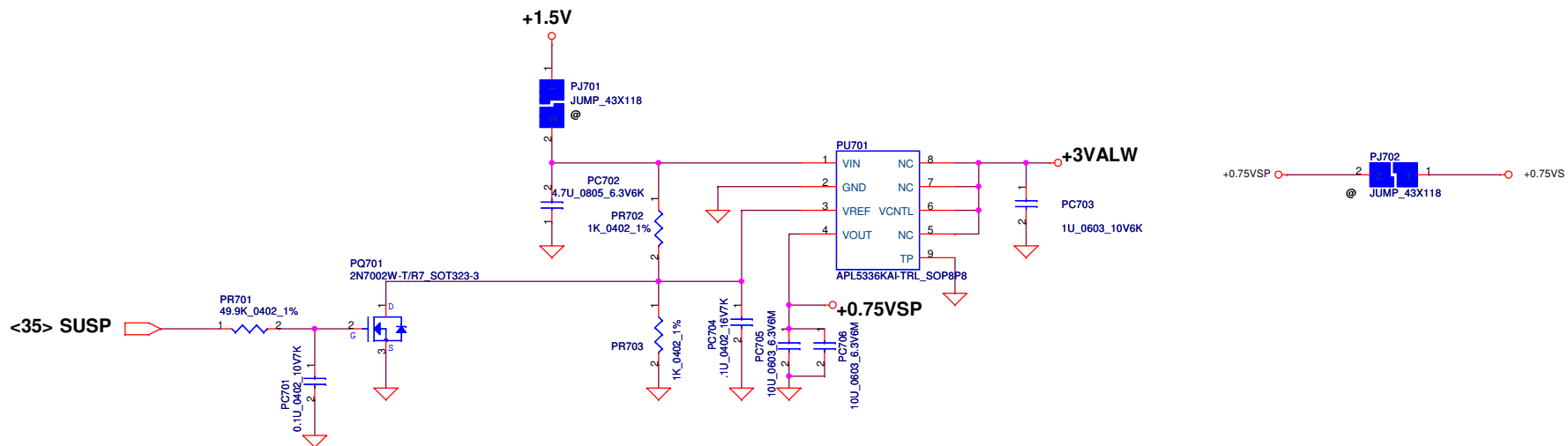


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				Custom			0.1
				Date:	Wednesday, November 30, 2011		Sheet

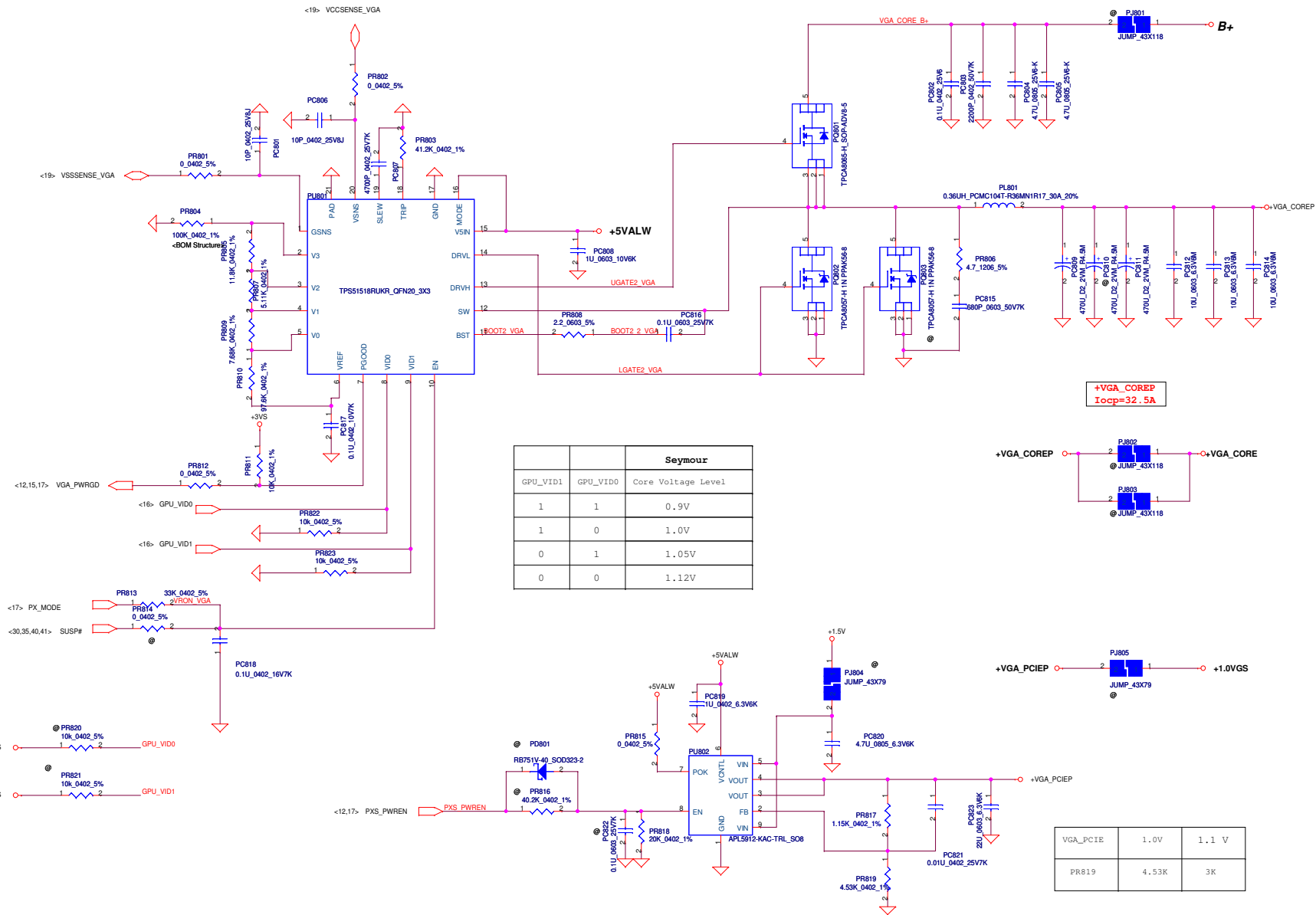


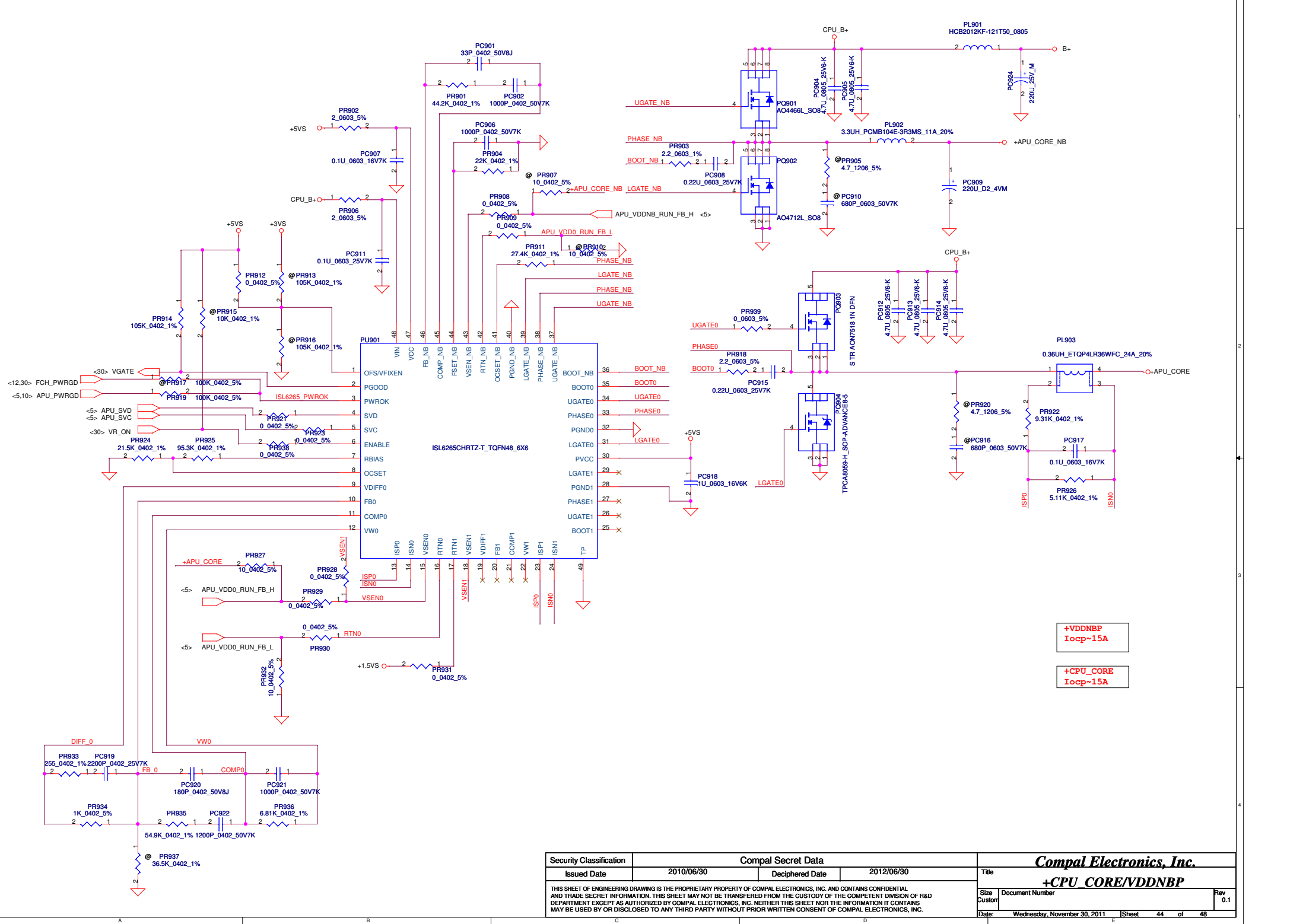
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO





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Size	Custom	Document Number		Rev	0.1
Date:	Wednesday, November 30, 2011	Sheet	42	of	48





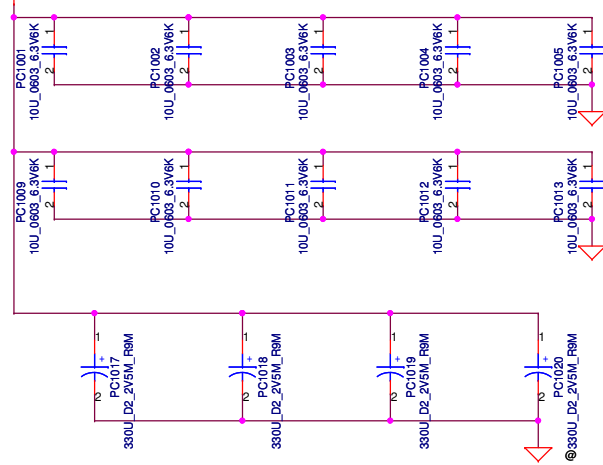
+VDDNB
Iocp~15A

+CPU_CORE
Iocp~15A

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				Date:	Wednesday, November 30, 2011
				Sheet	44 of 48
				Rev	0.1

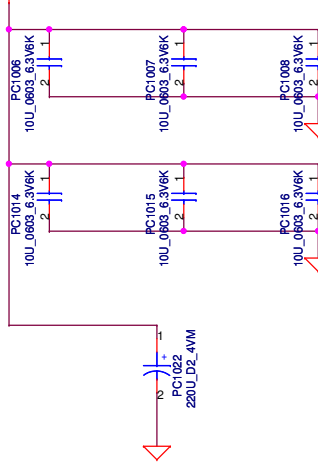
+CPU_CORE

+APU_CORE

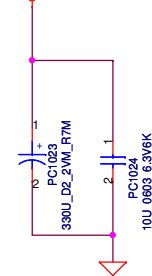


+CPU_CORE_NB

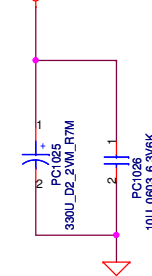
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+1.05VS



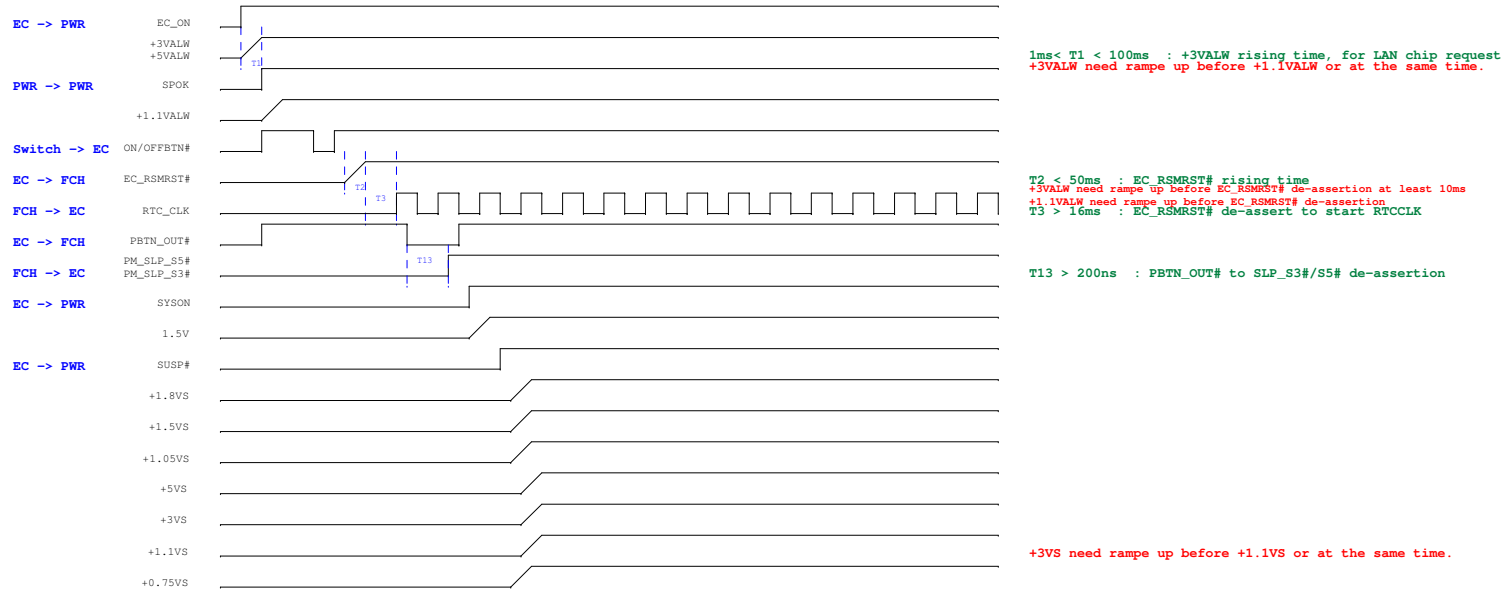
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				Date:	Tuesday, November 29, 2011
				Sheet	45 of 48
				Rev	0.1

Item	Reason for change	PG#	Modify List	Date	Phase
1	(CPU CORE/VDDNBP)...VR_ON增加PR938				
2	0402 0 欧姆				
3	APU_CORE_NB....PC1021拿掉				
4					
5					
6					
7					
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13					
14					
15					
16					
17					

QAWGE Power Sequence (AC mode)



DIS sequence

