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QHRAE

Superior 10AS/10ASG

LA-7213P REV 1.0 Schematic

AMD Llano FS1 Processor / Hudson M2/M3
Whistler Pro

2011-04-30 Rev 1.0

Security Classification	Compal Secret Data		
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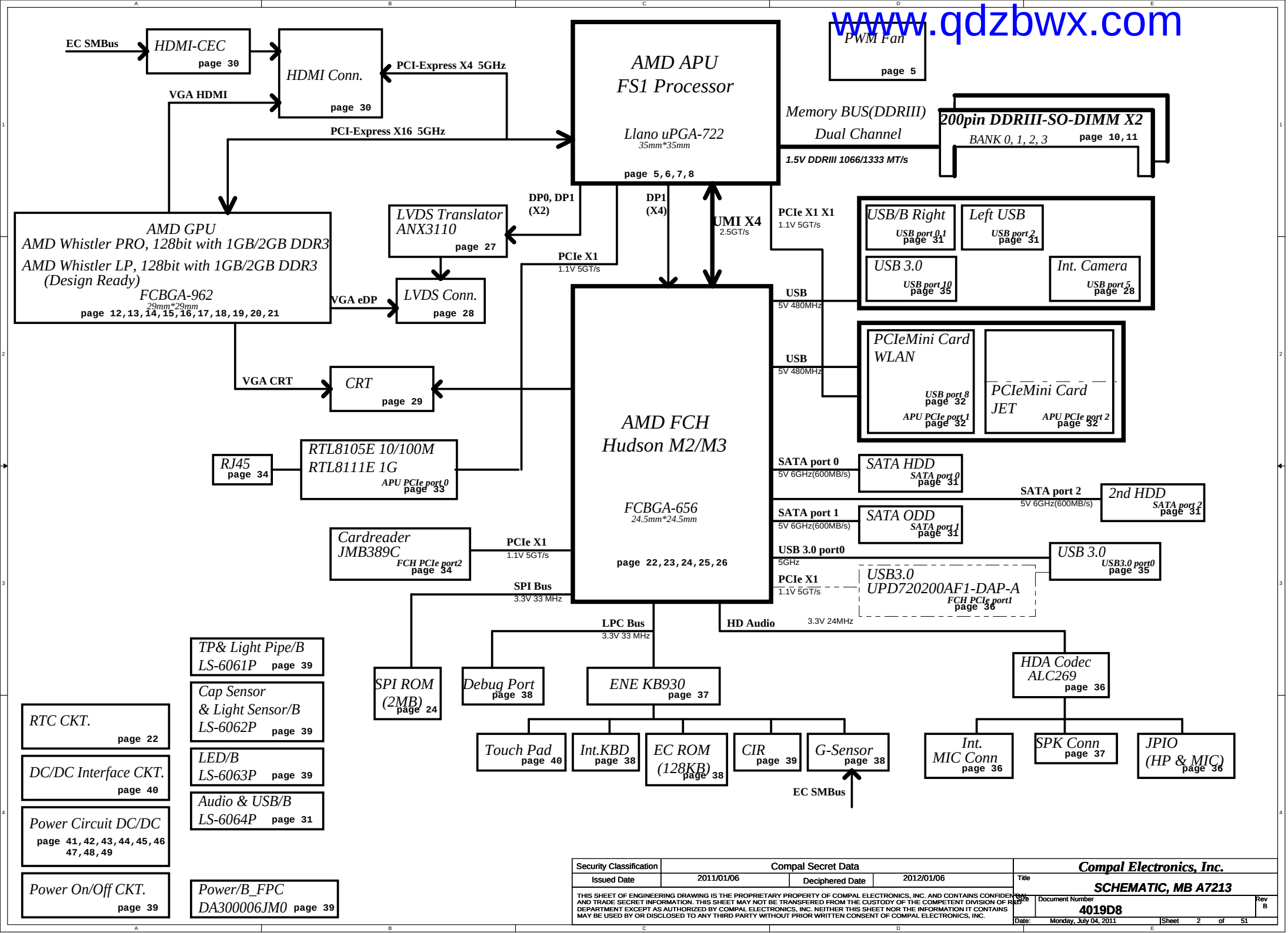

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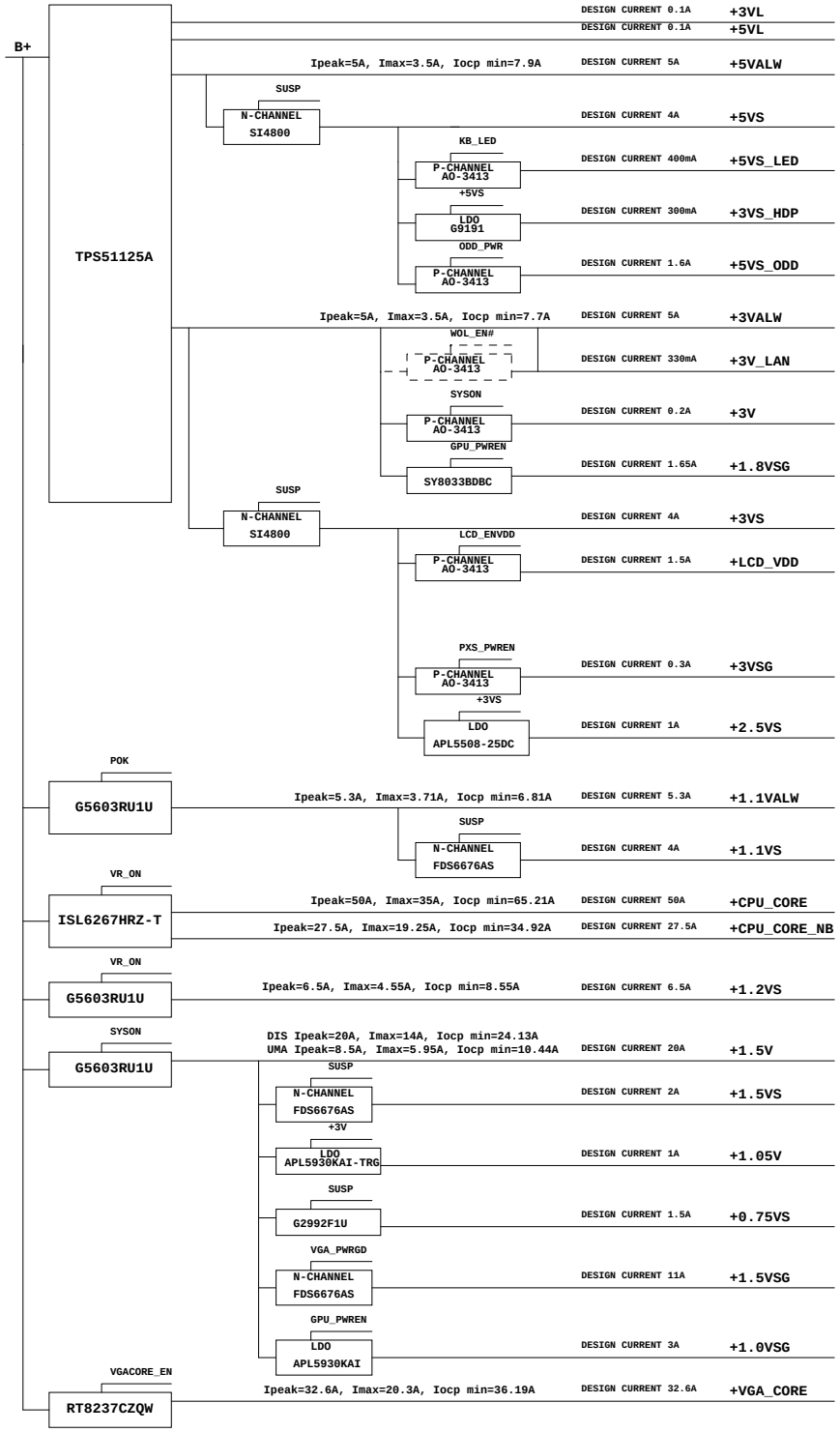

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VSG +1.8VSG +1.5VSG +1.0VSG
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress	Discrete	COMMON	CEC	UMA	PowerXpress	Discrete
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function		LAN		CIR	KB Light
description		LAN		CIR	KB Light
explain		10/100M	GIGA	CIR	KB Light
BTO		8105E@	8111E@	CIR@	KBL@

Function		G-SENSOR	Cam & Mic	Panel		
description		G-SENSOR	Cam & Mic	Panel (DIS@)		
explain		G-SENSOR	Cam & Mic	3D LVDS	eDP	Non-3D & EDP
BTO		GSENSOR@	CAM@	3D@+NOEDP@	EDP@	NO3D@+NOEDP@

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		Renesas USB3.0	FCH		EC	
description	PowerXpress (PXS@)		Renesas USB3.0	FCH		EC	
explain	BACO mode	Non-BACO	Renesas USB3.0	Hudson-M2	Hudson-M3	KB-930	KB-9012
BTO	BACO@	NOBACO@	RENE@	M2@	M3@	KB930@	KB9012@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	CPU Thermal Sensor	98 H	1001 1001 b
+3VS	GPU Thermal Sensor	41 H	0100 0001 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b
+3VS	3D - Bootloader	C0 H	1100 0000 b
+3VS	3D - Slave	C0 H	1100 0000 b

STATE / SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

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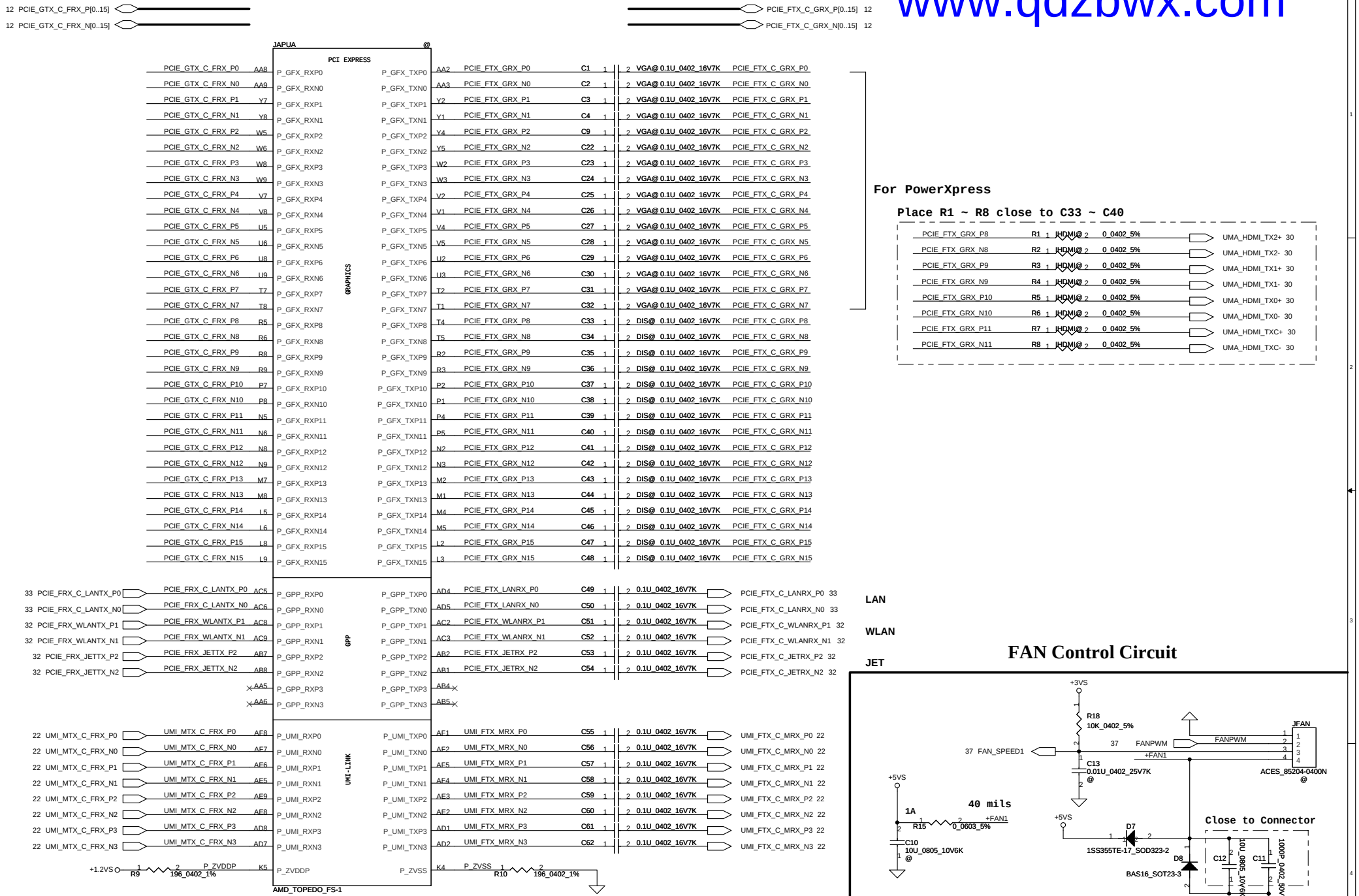

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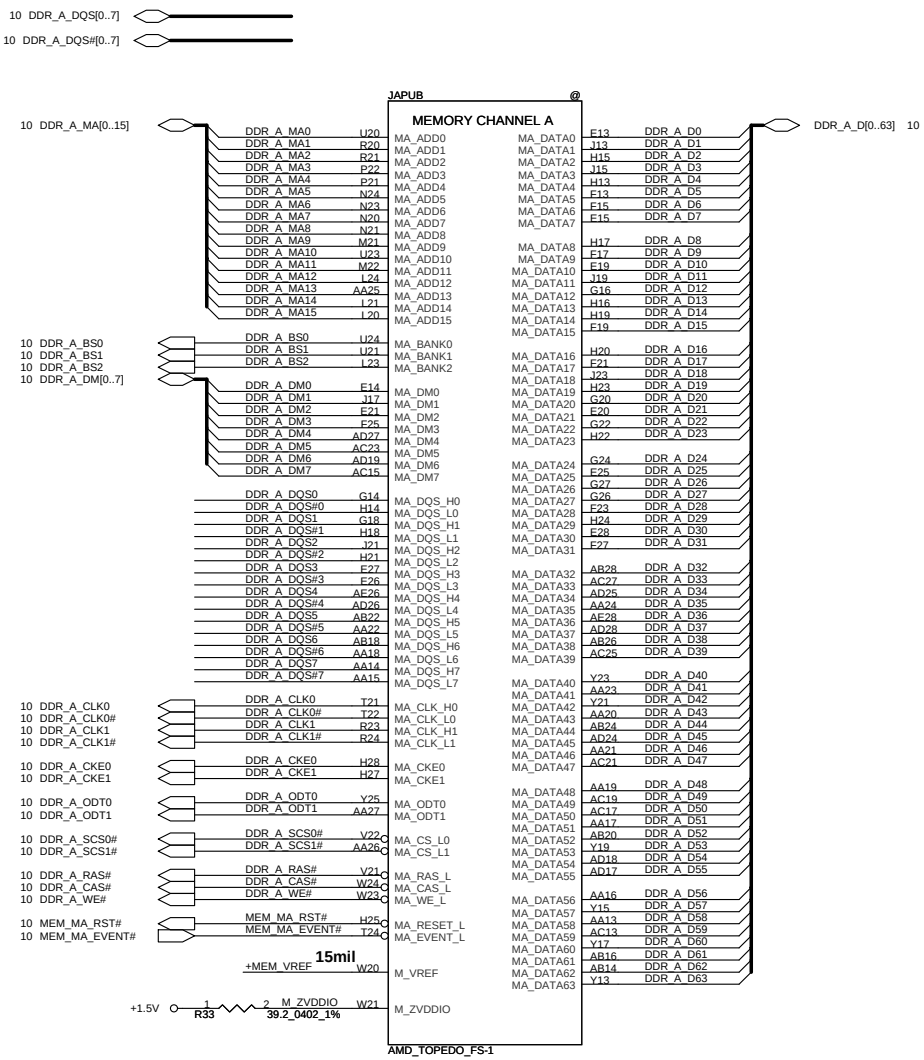
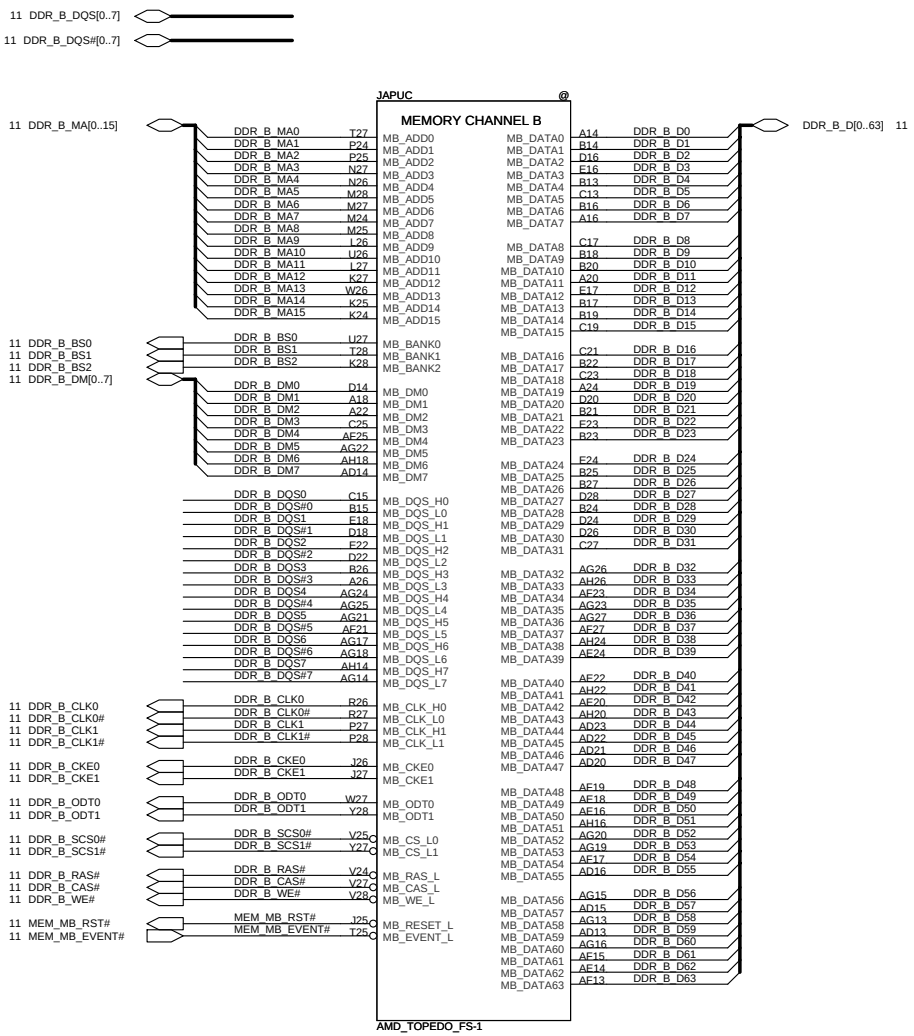
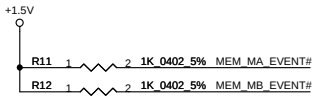
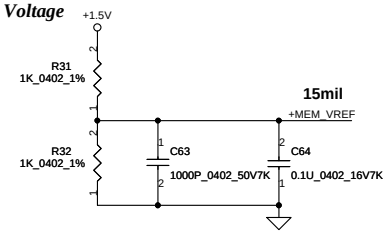




EVENT# pull high



0.75V Reference Voltage



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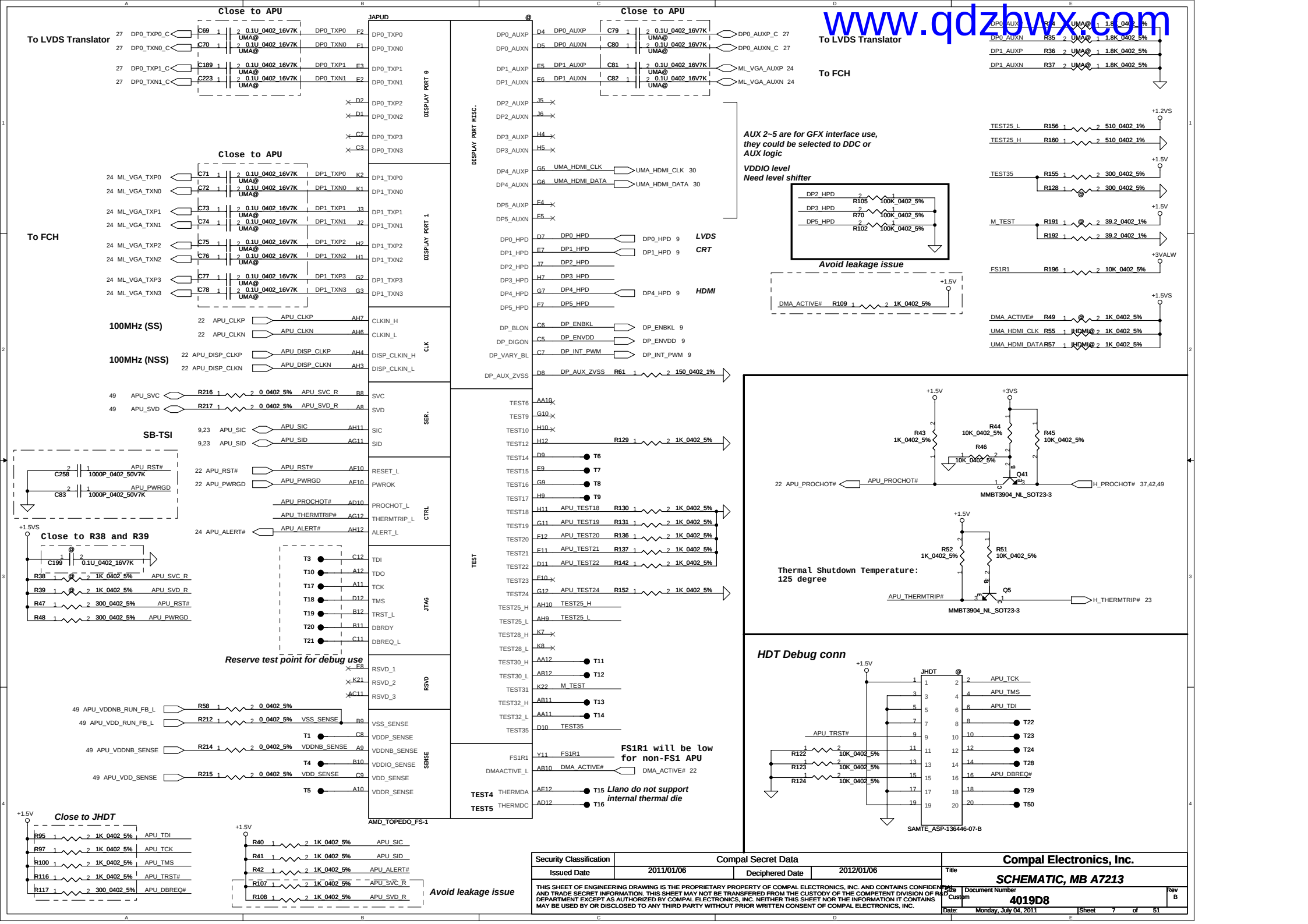

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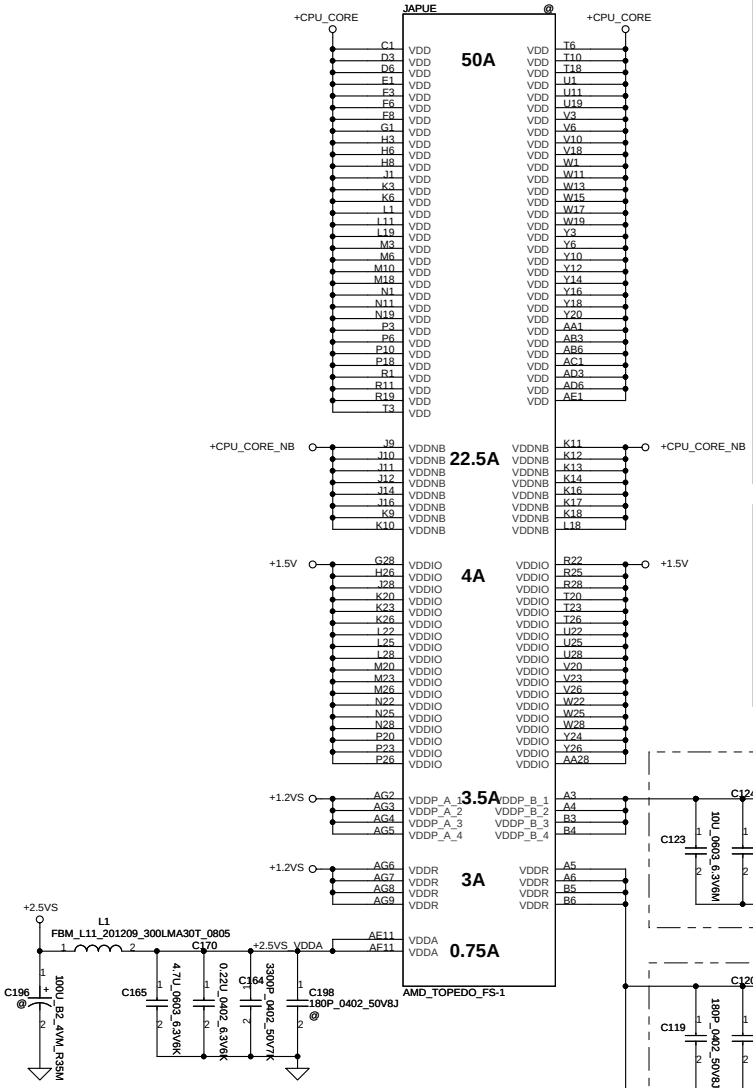
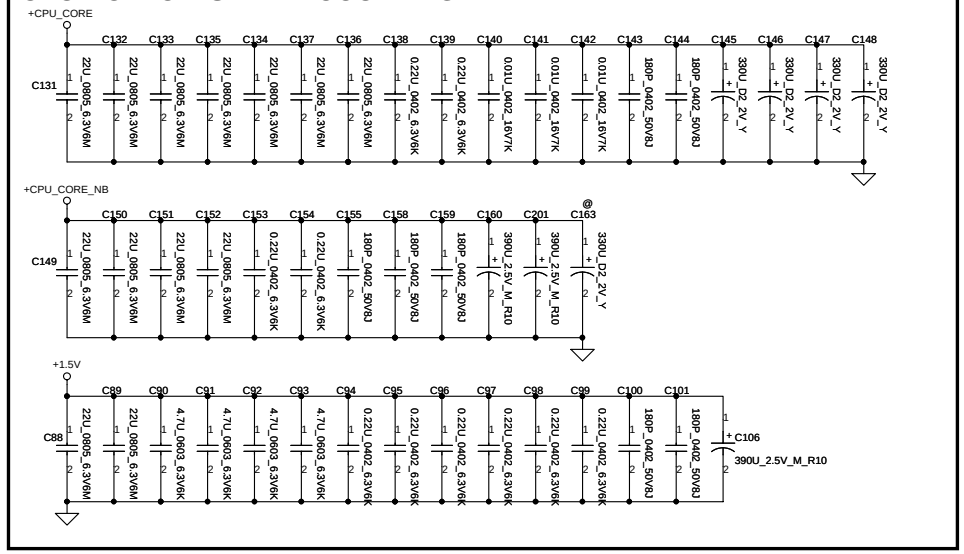
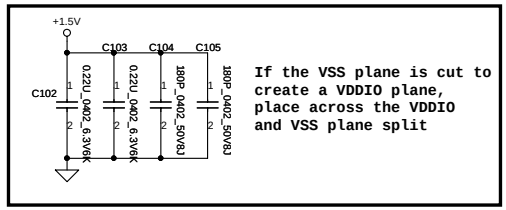


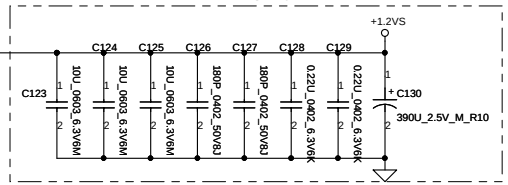
CPU BOTTOM SIDE DECOUPLING



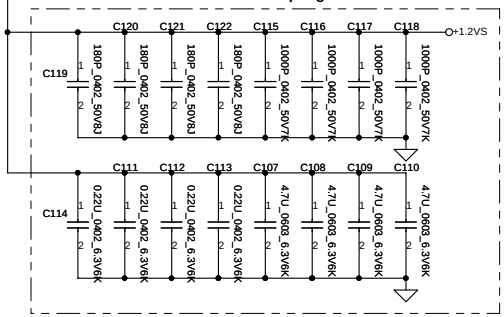


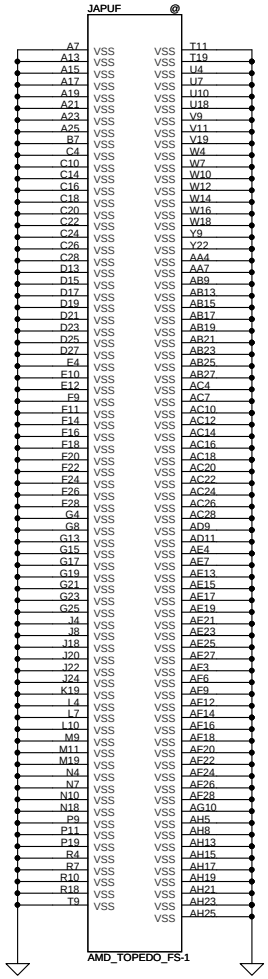
If the VSS plane is cut to create a VDDIO plane, place across the VDDIO and VSS plane split

VDDP Decoupling



VDDR Decoupling





CRB Decoupling Capacitor (include PWM side) :

VDD:	VDDNB:	VDDIO:	VDDP/R_PWM:	VDDP:	VDDR:	VDDA:
470uF x 6	470uF x 4	680uF x 1	470uF x 2	10uF x 3	4.7uF x 4	100uF x 1
22uF x 9	22uF x 6	330uF x 1	10uF x 1	0.22uF x 2	0.22uF x 4	4.7uF x 1
0.22uF x 2	0.22uF x 2	22uF x 2		180pF x 2	1nF x 4	0.22uF x 1
0.01uF x 3	180pF x 3	4.7uF x 4			180pF x 4	3.3nF x 1
180pF x 2		0.22uF x 8				
		180pF x 4				

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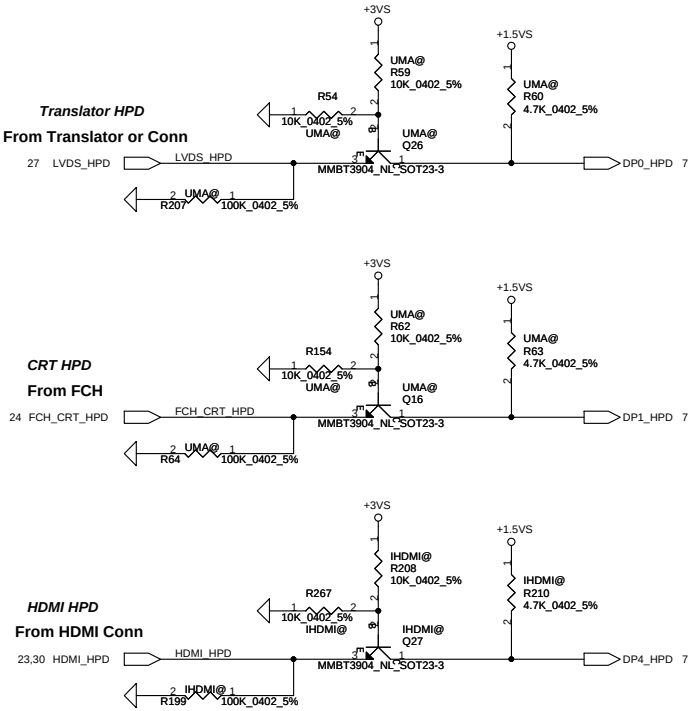
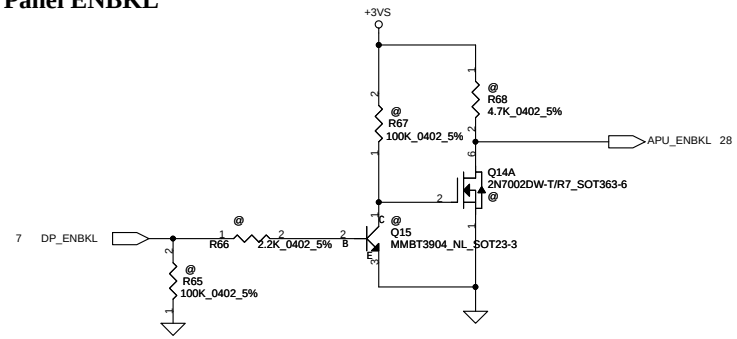
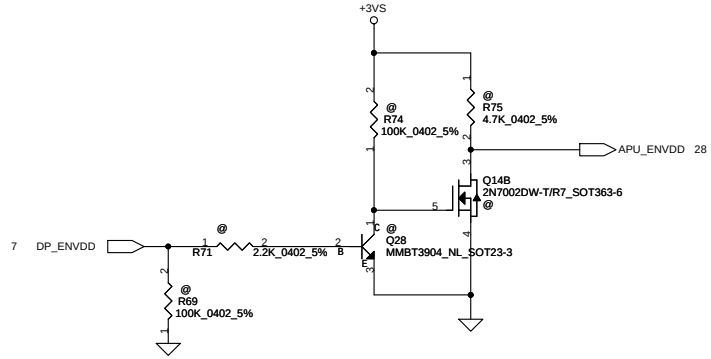
HPD



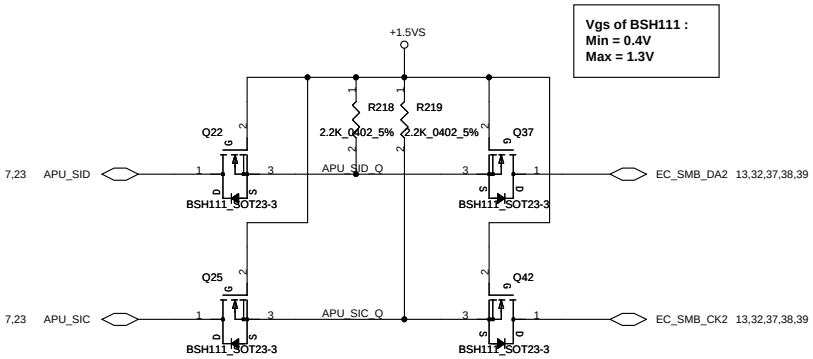
Panel ENBKL



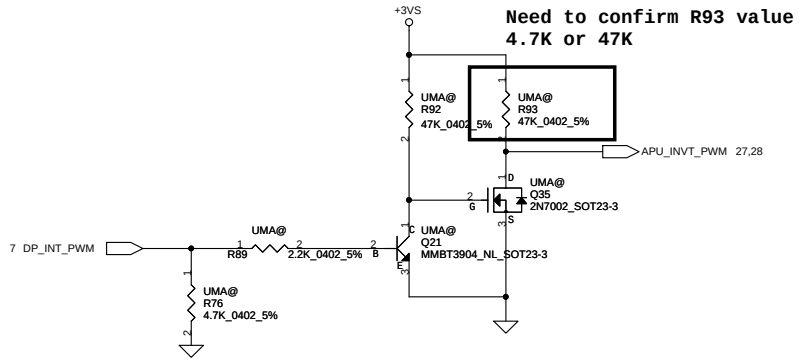
Panel ENVDD



SB-TSI



Panel PWM



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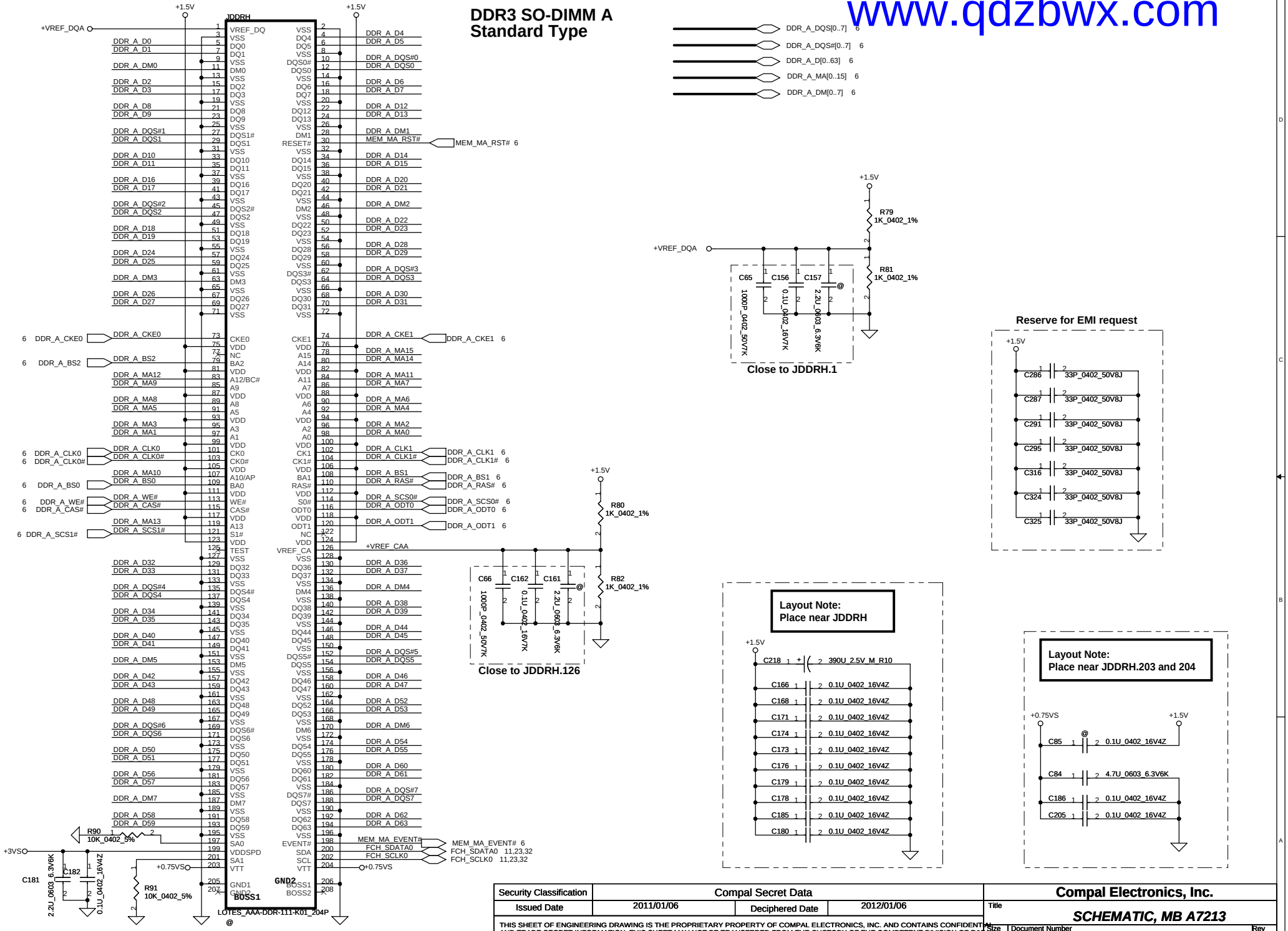
DDR3 SO-DIMM A
Standard Type



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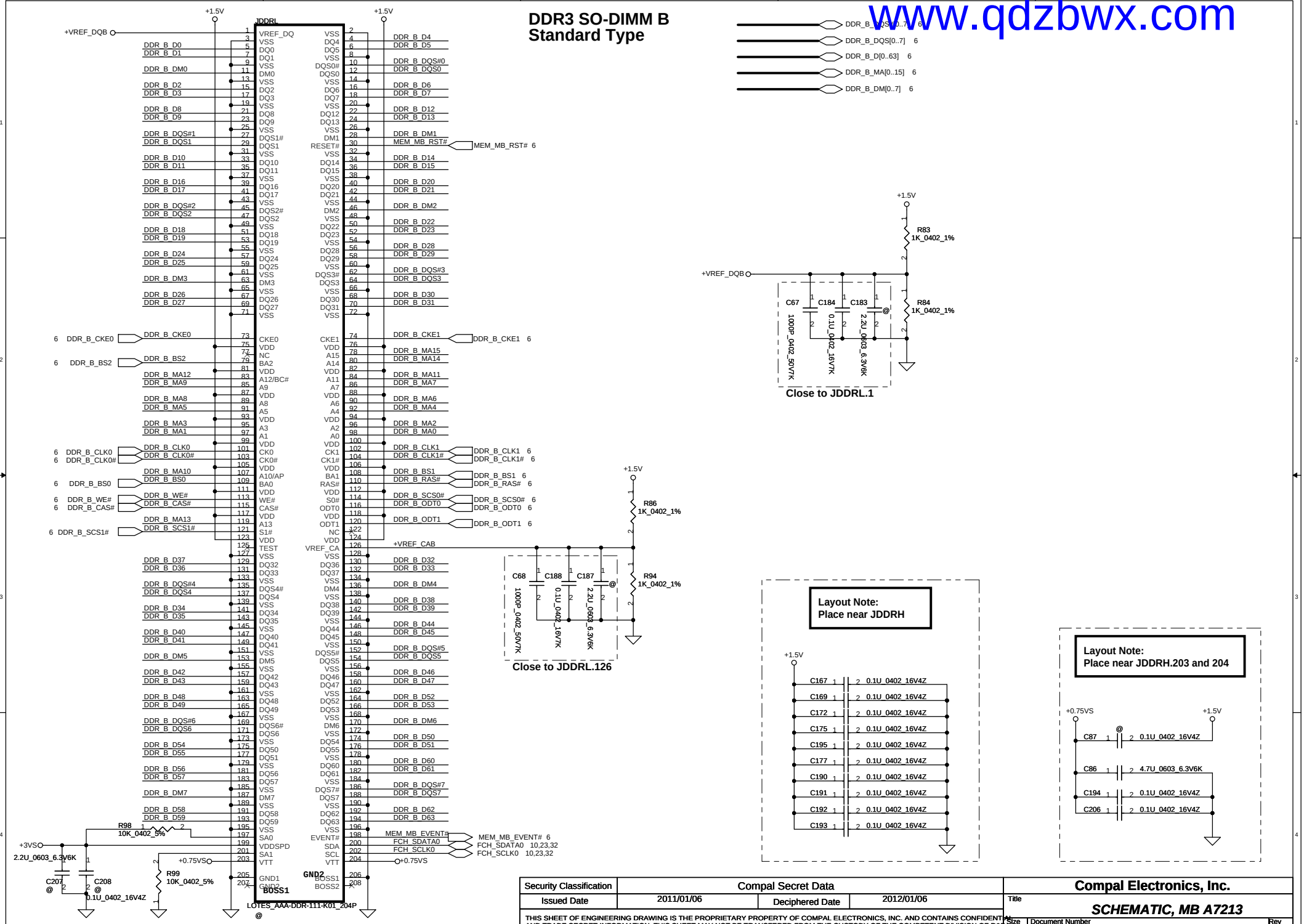

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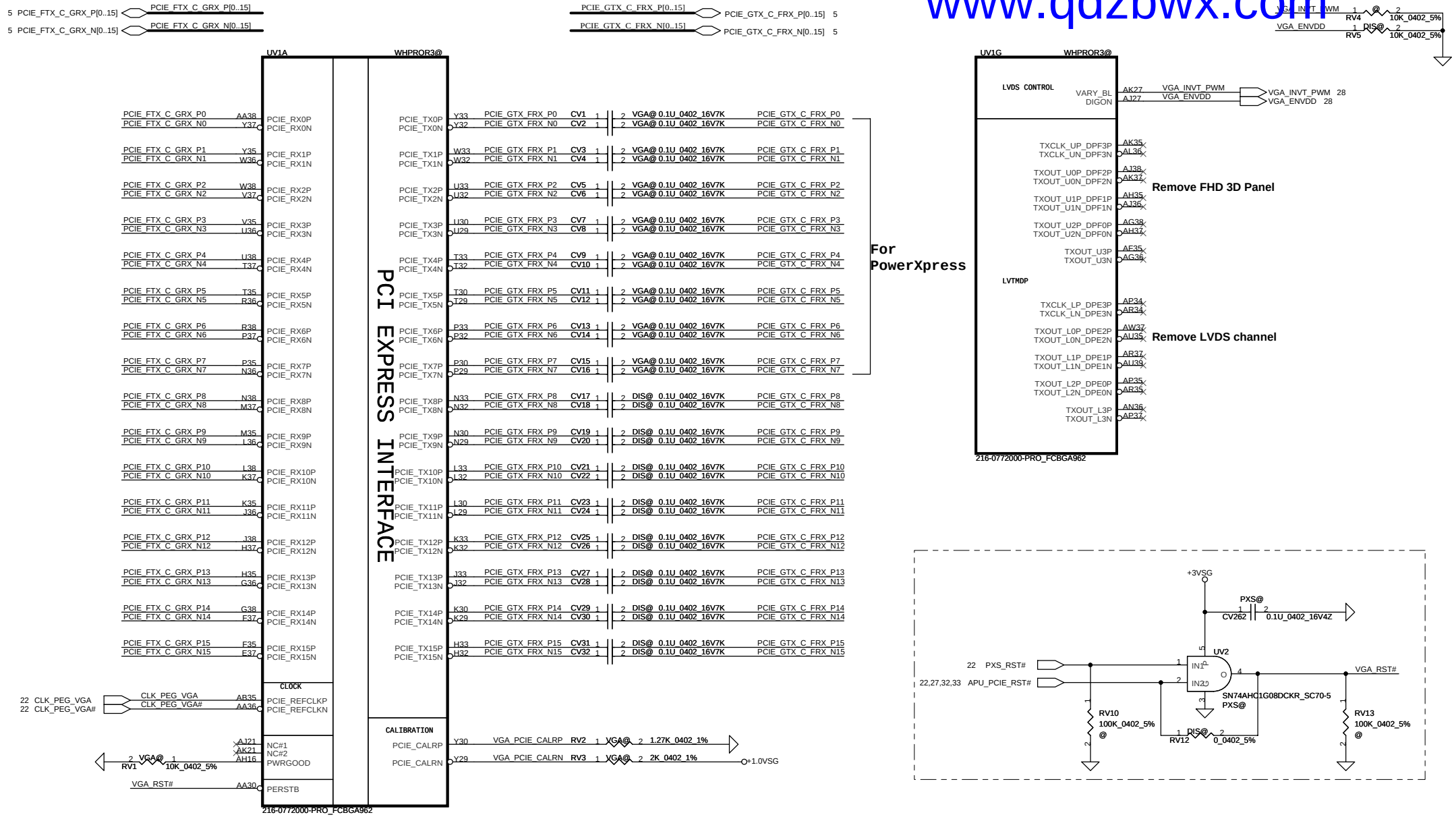

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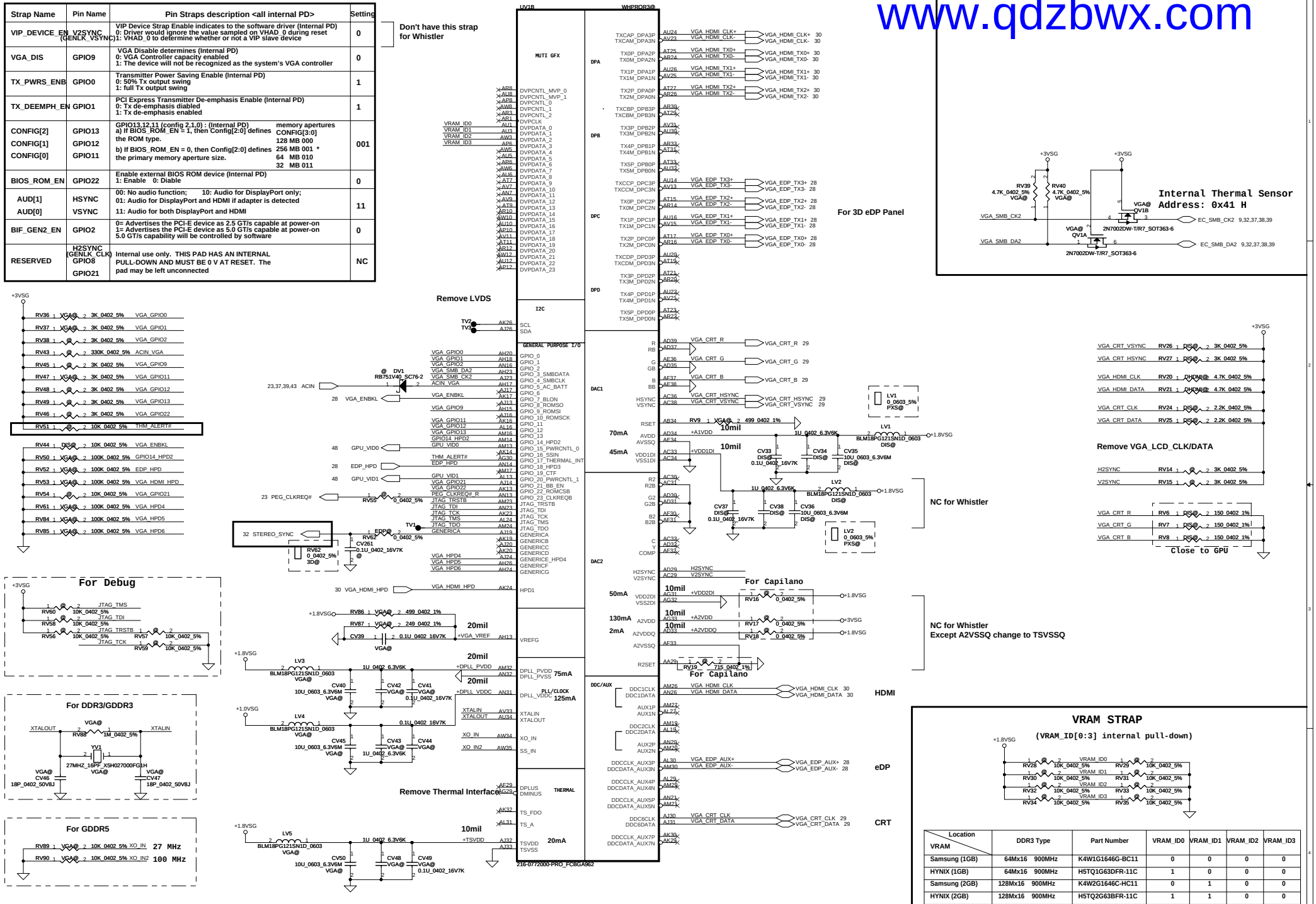
Strap Name	Pin Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN_V2SYNC (GENLK_VSYNC)		VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 256 MB 001 * b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010 32 MB 011	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 1: Enable 0: Diable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	NC

Don't have this strap for Whistler



VRAM \ Location	DDR3 Type	Part Number	VRAM_ID0	VRAM_ID1	VRAM_ID2	VRAM_ID3
Samsung (1GB)	64Mx16 900MHz	K4W1G1646G-BC11	0	0	0	0
HYNIX (1GB)	64Mx16 900MHz	H5TQ1G63DFR-11C	1	0	0	0
Samsung (2GB)	128Mx16 900MHz	K4W2G1646C-HC11	0	1	0	0
HYNIX (2GB)	128Mx16 900MHz	H5TQ2G63BFR-11C	1	1	0	0

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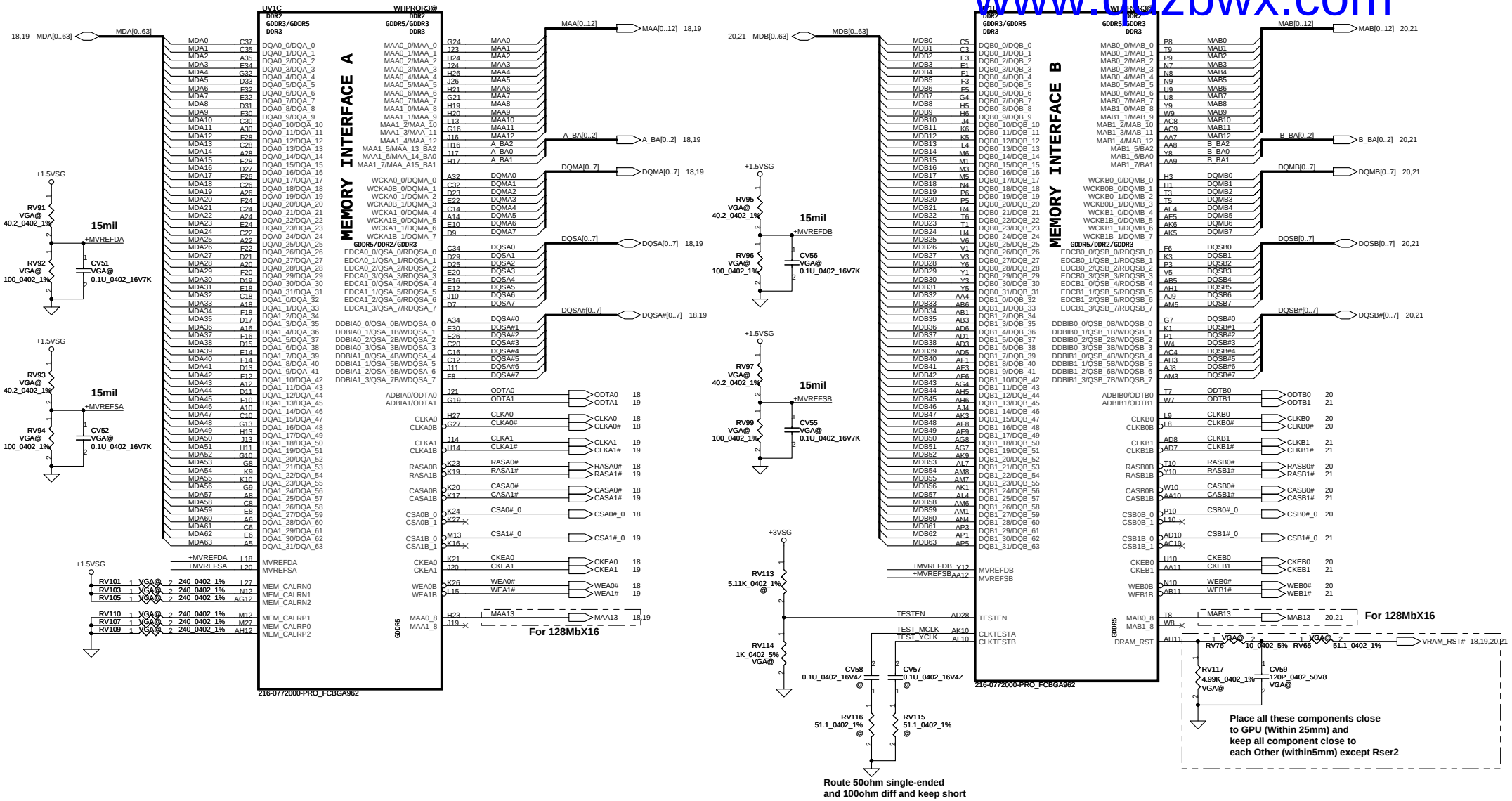

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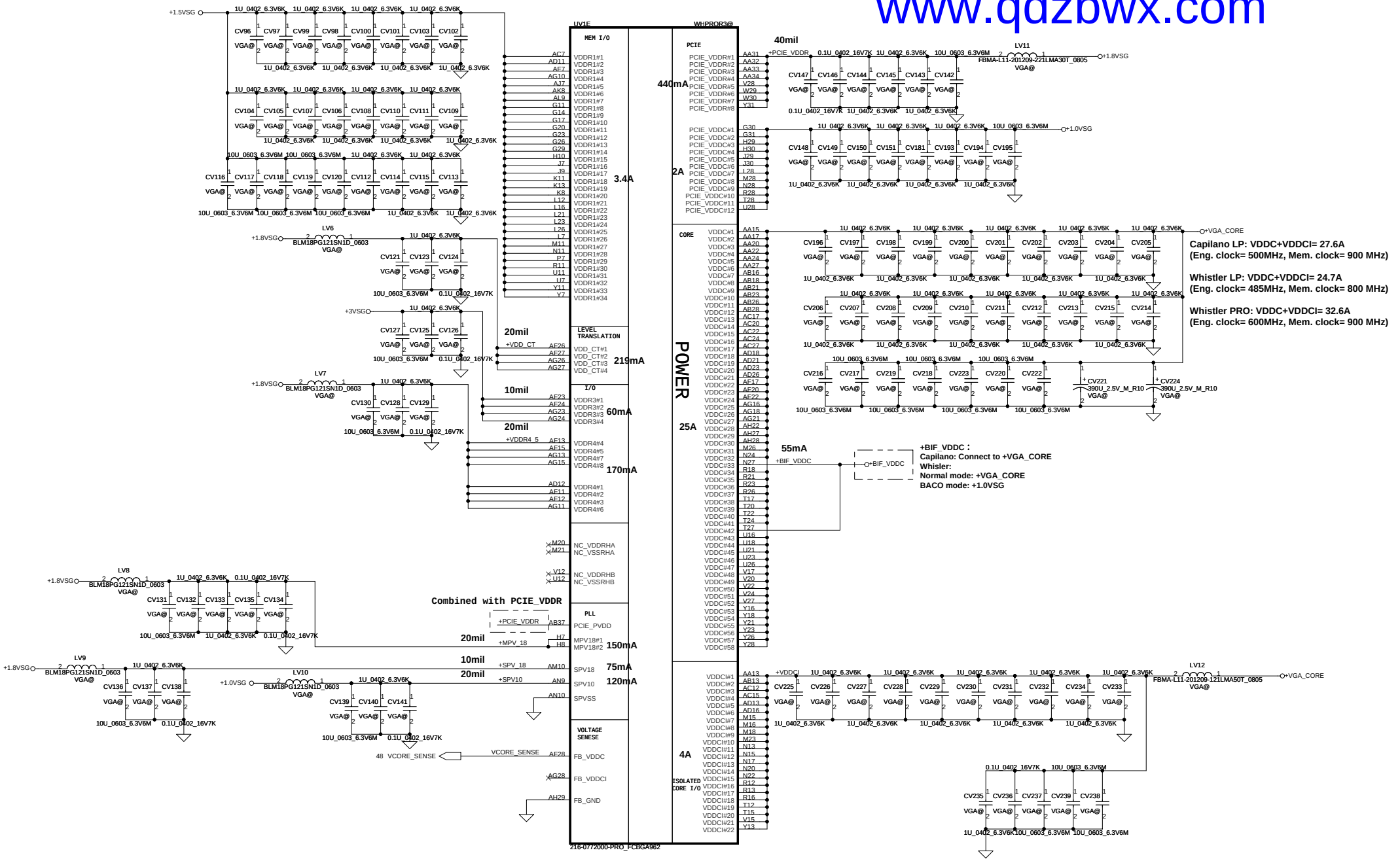

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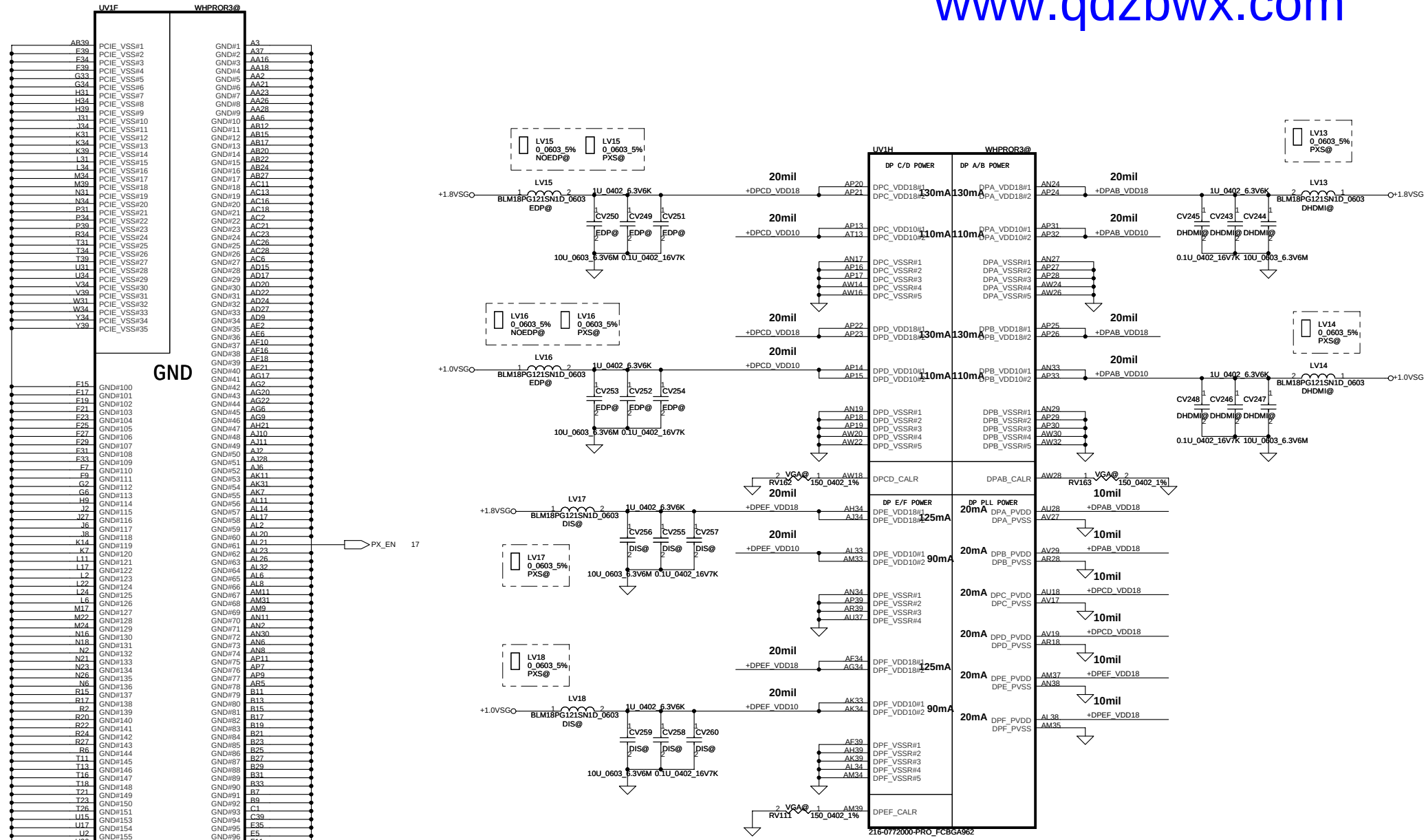

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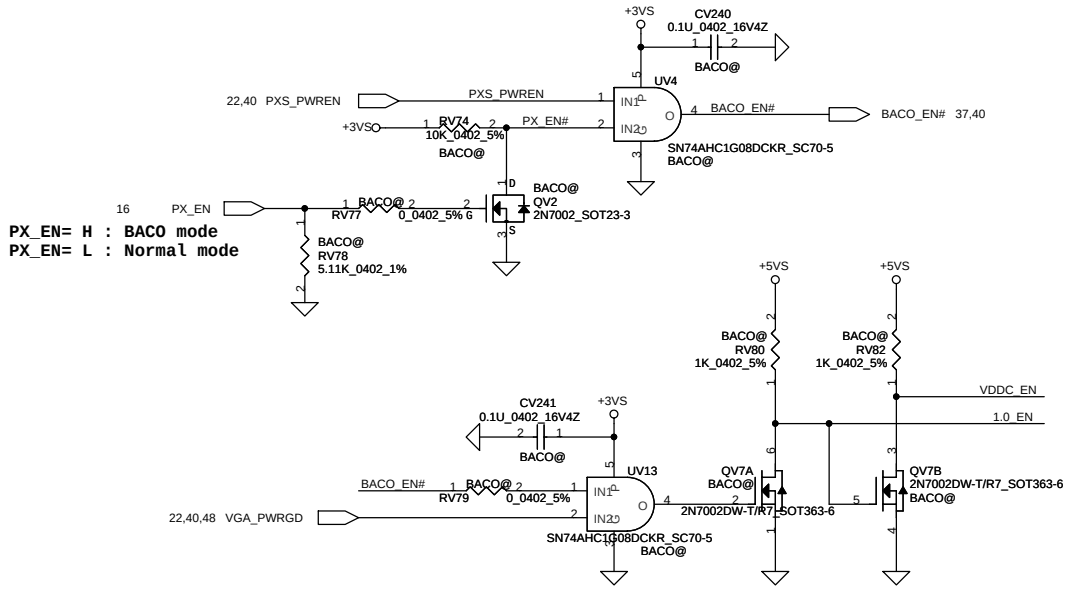

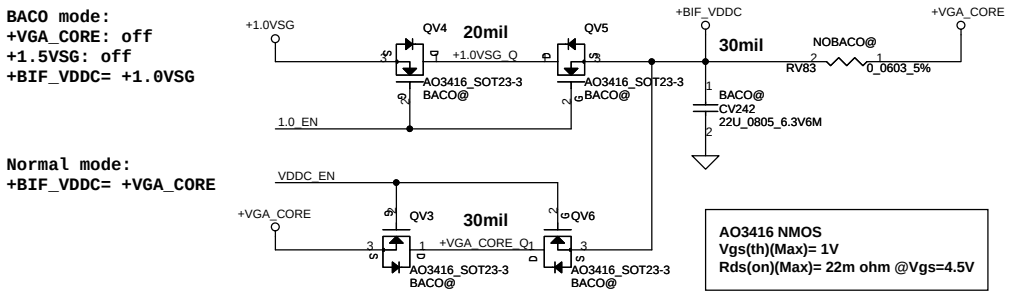

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Memory Partition A - Lower 32 bits

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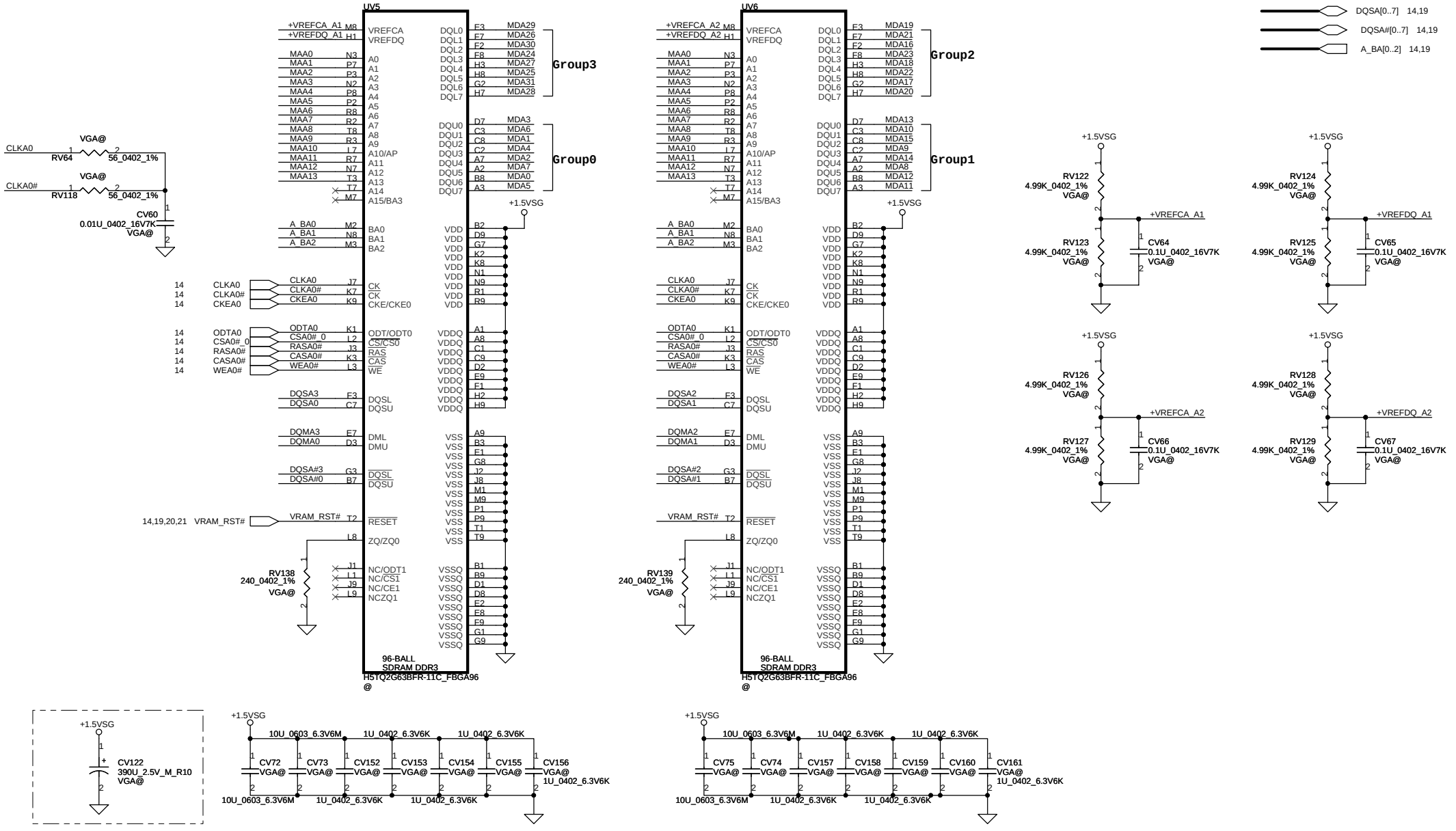
MDA[0..63] 14,19
MAA[0..13] 14,19
DQMA[0..7] 14,19
DQSA[0..7] 14,19
DQSA#[0..7] 14,19
A_BA[0..2] 14,19



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Memory Partition A - Upper 32 bits

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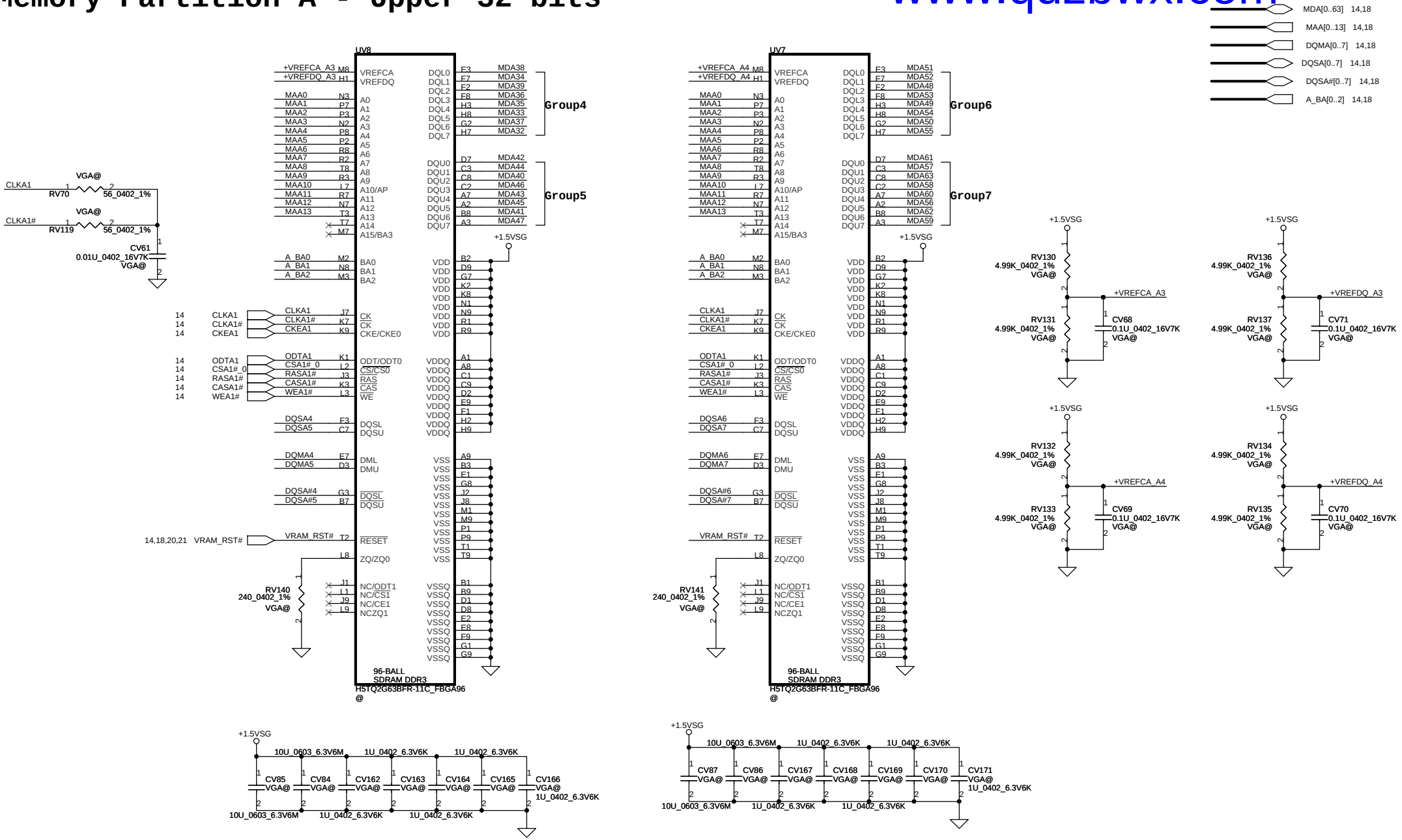

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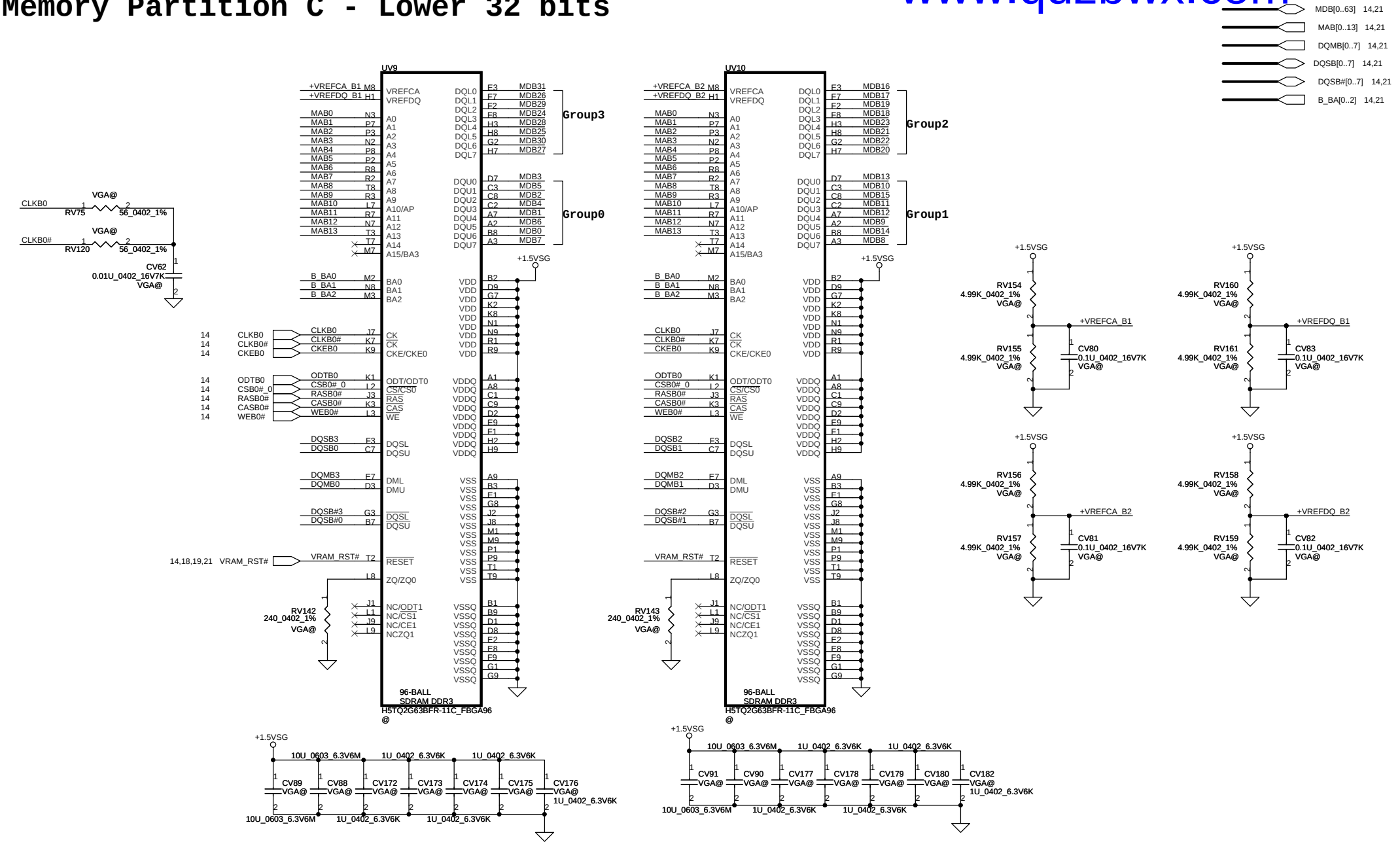
Memory Partition C - Lower 32 bits

www.qdzbwx.com



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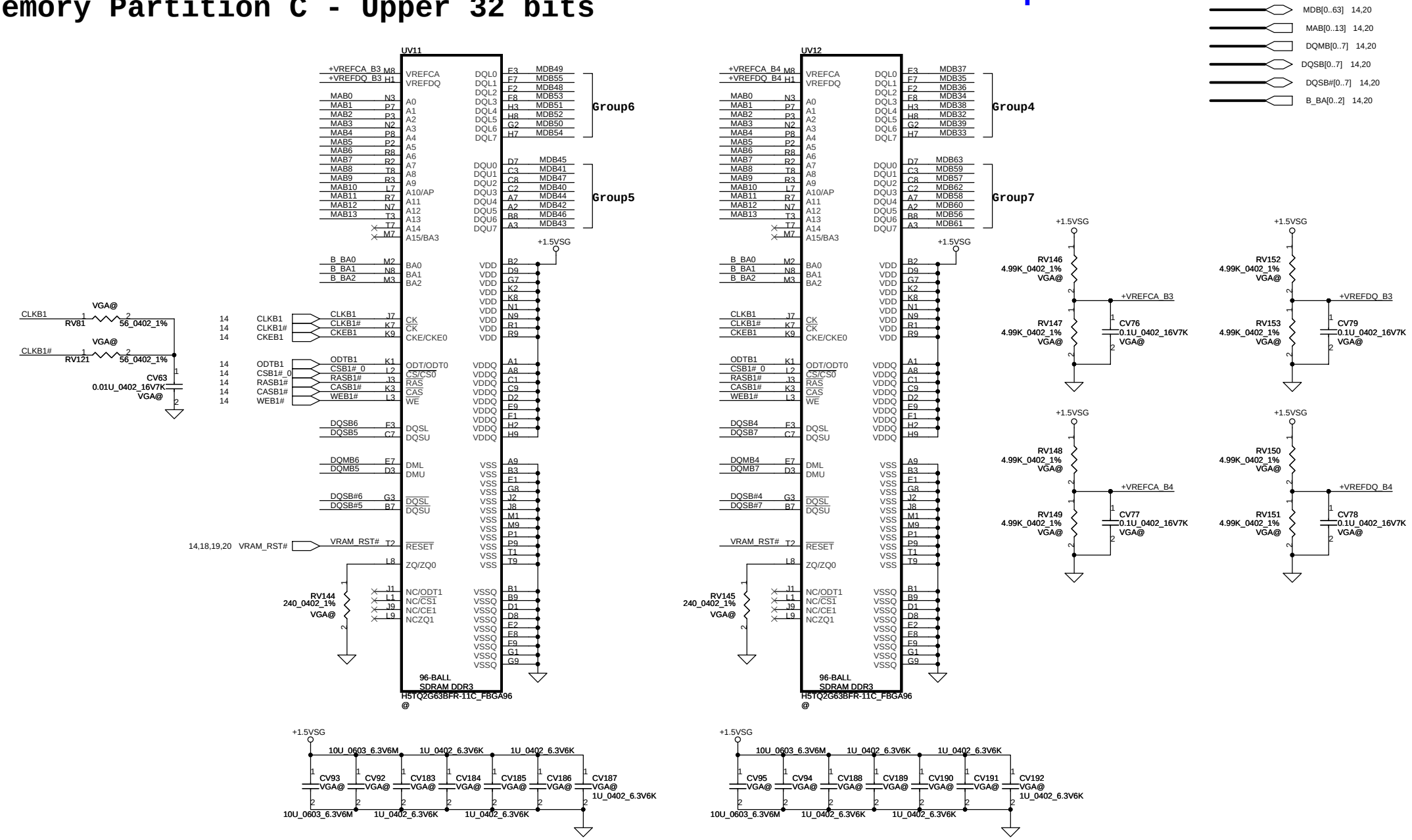
Memory Partition C - Upper 32 bits



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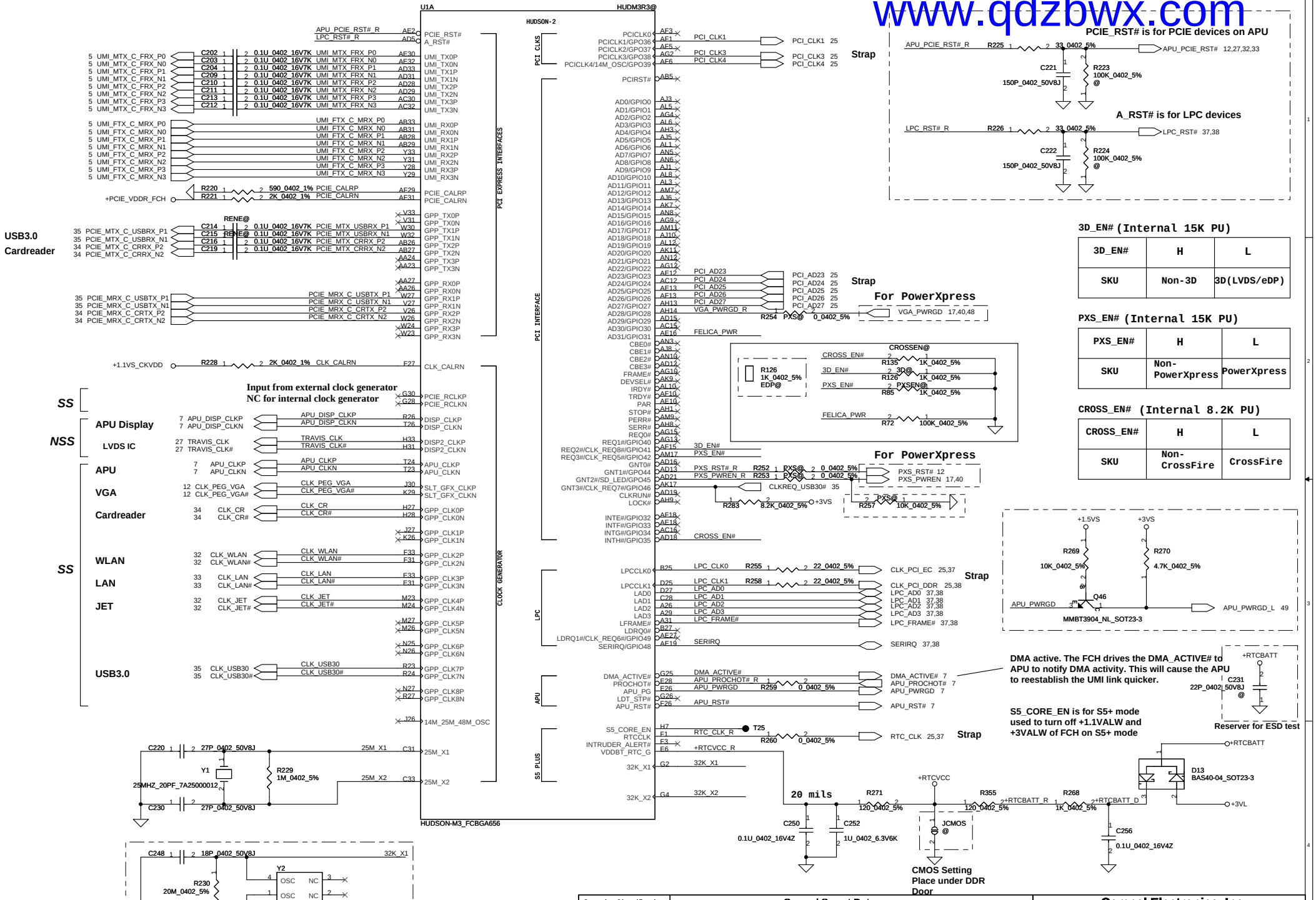

3D_EN#	H	L
SKU	Non-3D	3D(LVDS/eDP)

PXS_EN#	H	L
SKU	Non-PowerXpress	PowerXpress

CROSS_EN#	H	L
SKU	Non-CrossFire	CrossFire

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PCIE_RST2# is for PCIE devices on FCH

U1D HUDM3R3@ HUDSON-2

R227 100K_0402_5% C19 150P_0402_50V8J R222 33_0402_5%

34,35 FCH_PCIE_RST# — FCH_PCIE_RST#_R — PCIE_RST2#/PCI_PME#/GEVENT4# (AB6)

37 EC_LID_OUT# — EC_LID_OUT# — RI#/GEVENT22# (R2) — T68 (W7)

37 SLP_S3# — SLP_S3# — SPI_CS3#/GBE_STAT1/GEVENT21# (T3)

37 SLP_S5# — SLP_S5# — SLP_S3# (W2)

37 PBTN_OUT# — PBTN_OUT# — SLP_S5# (J4)

37 FCH_PWRGD — FCH_PWRGD — PWR_BTN# (N7)

PWR_GOOD

TEST0 (T9) TEST1 (T10) TEST2 (V9)

+3VS R301 8.2K_0402_5% PEG_CLKREQ# VGA@ R295 1K_0402_5%

37 GATEA20 — GATEA20 — GA20IN/GEVENT0# (AE22)

37 KB_RST# — KB_RST# — KBRST#/GEVENT1# (AG19)

37 EC_SCI# — EC_SCI# — LPC_PME#/GEVENT3# (R9)

37 EC_SMI# — EC_SMI# — LPC_SMI#/GEVENT23# (C26)

T69 (T5) LPC_PD#/GEVENT5# (U4)

33,35 FCH_PCIE_WAKE# — FCH_PCIE_WAKE# — SYS_RESET#/GEVENT19# (K1) — T67 (V7)

WAKE#/GEVENT8# (R10)

7 H_THERMTRIP# — H_THERMTRIP# — IR_RX1/GEVENT20# (AF19)

+3VS R279 10K_0402_5% — WD_PWRGD — THRMTRIP#/SMBALERT#/GEVENT2#

WD_PWRGD (U2)

37 EC_RSMRST# — EC_RSMRST# — RSMRST#

32 CLKREQ_JET# — CLKREQ_JET# — CLK_REQ4#/SATA_IS0#/GPIO64 (AG24)

33 CLKREQ_LAN# — D17 RB751V40_SC76-2 — CLKREQ_LAN#_R — CLK_REQ3#/SATA_IS1#/GPIO63 (AE24)

R361 0_0402_5% — CLKREQ_CR# — SMARTVOLT1/SATA_IS2#/GPIO50 (AE26) — CLK_REQ0#/SATA_IS3#/GPIO60 (AE22)

SATA_IS4#/FANOUT3/GPIO55 (AH17) SATA_IS5#/FANIN3/GPIO59 (AG18)

SPKR/GPIO66

36 FCH_SPKR — FCH_SPKR (AF24)

10,11,32 FCH_SCLK0 — FCH_SCLK0 — SCL0/GPIO43 (AD26)

10,11,32 FCH_SDATA0 — FCH_SDATA0 — SDA0/GPIO47 (AD25)

FCH_SCLK1 — SCL1/GPIO227 (T7)

FCH_SDATA1 — SDA1/GPIO228 (R7)

32 CLKREQ_WLAN# — CLKREQ_WLAN# — CLK_REQ2#/FANIN4/GPIO62 (AG25)

CLK_REQ1#/FANOUT4/GPIO61 (AG22) T30 (J2) IR_LED#/LLB#/GPIO184 (AG26)

SMARTVOLT2/SHUTDOWN#/GPIO51 (V8)

DDR3_RST#/GEVENT7#/VGA_PD

25 VGA_PD — R292 0_0402_5% — VGA_PD_FCH — GBE_LED0/GPIO183 (W8) T65 (Y6)

HDMI_HPD_FCH_R — SPI_HOLD#/GBE_LED1/GEVENT9# (V10)

GBE_LED2/GEVENT10# (AA8)

GBE_STAT0/GEVENT11#

13 PEG_CLKREQ# — PEG_CLKREQ# — CLK_REQG#/GPIO65/OSCIN/IDLEEXIT# (AF25)

35 USB30_SMI# — USB30_SMI# — BLINK/USB_OC7#/GEVENT18# (M7)

USB_OC6#/IR_TX1/GEVENT6# (R8)

31 ODD_PLUGIN# — ODD_DA#_FCH — USB_OC5#/IR_TX0/GEVENT17# (T1)

USB_OC4#/IR_RX0/GEVENT16# (P6)

37 USB_OC3# — USB_OC3# — USB_OC3#/AC_PRES/TDO/GEVENT15# (F5)

34 CR_CPPE# — CR_CPPE# — USB_OC2#/TCK/GEVENT14# (P5)

32,35,37 USB_OC1# — USB_OC1# — USB_OC1#/TDI/GEVENT13# (J7)

31,37 USB_OC0# — USB_OC0# — USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12# (T8)

36 AZ_BITCLK_HD — R320 33_0402_5% — HDA_BITCLK — AZ_BITCLK (AB3)

36 AZ_SDOUT_HD — R321 33_0402_5% — HDA_SDOUT — AZ_SDOUT (AB1)

36 AZ_SDIN0_HD — AZ_SDIN0_HD — AZ_SDIN0/GPIO167 (AA2)

AZ_SDIN1/GPIO168 (V5) AZ_SDIN2/GPIO169 (Y3) AZ_SDIN3/GPIO170 (Y1)

36 AZ_SYNC_HD — R322 33_0402_5% — HDA_SYNC — AZ_SYNC (AD6)

36 AZ_RST_HD# — R323 33_0402_5% — HDA_RST# — AZ_RST# (AE4)

+3VALW

R421 10K_0402_5% CR_CPPE#

R293 10K_0402_5% VGA_PD_FCH

R278 10K_0402_5% H_THERMTRIP#

R288 10K_0402_5% FCH_SCLK1

R289 10K_0402_5% FCH_SDATA1

R272 10K_0402_5% EC_LID_OUT#

R276 10K_0402_5% FCH_PCIE_WAKE#

RENE@ R306 10K_0402_5% USB30_SMI#

R318 10K_0402_5% USB_OC0#

R319 10K_0402_5% USB_OC1#

R436 330K_0402_5% ACIN_FCH#

R332 10K_0402_5% USB_OC3#

CIR@ R442 1K_0402_5% — T26 (K19) T27 (J19) — CIR_EN# (J21)

PS2_DAT/SDA4/GPIO187 PS2_CLK/CEC/SCL4/GPIO188 SPI_CS2#/GBE_STAT2/GPIO166

ACIN_FCH# (D21) C20 D23 C22

PS2KB_DAT/GPIO189 PS2KB_CLK/GPIO190 PS2M_DAT/GPIO191 PS2M_CLK/GPIO192

Change to low active for AC_IN LED issue

13,37,39,43 ACIN — Q191 2N7002_SOT23-3

KSO_0/GPIO209 (F21) KSO_1/GPIO210 (E20) KSO_2/GPIO211 (F20) KSO_3/GPIO212 (A22) KSO_4/GPIO213 (F18) KSO_5/GPIO214 (A20) KSO_6/GPIO215 (J18) KSO_7/GPIO216 (H18) KSO_8/GPIO217 (G18) KSO_9/GPIO218 (B21) KSO_10/GPIO219 (K18) KSO_11/GPIO220 (D19) KSO_12/GPIO221 (A18) KSO_13/GPIO222 (C18) KSO_14/GPIO223 (B19) KSO_15/GPIO224 (B17) KSO_16/GPIO225 (A24) KSO_17/GPIO226 (D17)

+3VS

R286 2.2K_0402_5% FCH_SCLK0

R287 2.2K_0402_5% FCH_SDATA0

R291 8.2K_0402_5% CLKREQ_WLAN#

R290 8.2K_0402_5% CLKREQ_JET#

R281 8.2K_0402_5% CLKREQ_CR# — R282 1K_0402_5%

R284 8.2K_0402_5% CLKREQ_LAN#_R

Set cardreader clock as free-running

R280 100K_0402_5% EC_RSMRST#

R324 10K_0402_5% HDA_BITCLK

R325 10K_0402_5% AZ_SDIN0_HD

+3VALW

For FCH internal debug use (Internal 10K pull-down)

R273 2.2K_0402_5% TEST0

R274 2.2K_0402_5% TEST1

R275 2.2K_0402_5% TEST2

HUDSON-M3_FCBGA656

ACPI / WAKE UP EVENTS — GPIO — HD AUDIO — USB OC — USB MISC — USB 1.1 — USB 2.0 — USB 3.0 — EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC (G8)

USB_RCOMP (B9) — R329 11.8K_0402_1%

USB_FSD1P/GPIO186 (H1) USB_FSD1N (H3)

USB_FSD0P/GPIO185 (H6) USB_FSD0N (H5)

USB_HSD13P (H10) USB_HSD13N (G10)

USB_HSD12P (K10) USB_HSD12N (J12)

USB_HSD11P (G12) USB_HSD11N (F12)

USB_HSD10P (K12) — USB20_P10 — USB20_P10 32 — USB 3.0 (For Hudson M3 only)

USB_HSD10N (K13) — USB20_N10 — USB20_N10 32

USB_HSD9P (B11) USB_HSD9N (D11) — Remove Felica

USB_HSD8P (E10) — USB20_P8 — USB20_P8 32 — WLAN (BT)

USB_HSD8N (F10) — USB20_N8 — USB20_N8 32

USB_HSD7P (C10) USB_HSD7N (A10) — Remove Finger Printer

USB_HSD6P (H9) USB_HSD6N (G9) — Remove 3G/TV #1

USB_HSD5P (A8) — USB20_P5 — USB20_P5 28 — Int. Camera

USB_HSD5N (C8) — USB20_N5 — USB20_N5 28

USB_HSD4P (F8) USB_HSD4N (E8)

USB_HSD3P (C6) USB_HSD3N (A6) — Remove TV #2

USB_HSD2P (C5) — USB20_P2 — USB20_P2 31 — USB-Left

USB_HSD2N (A5) — USB20_N2 — USB20_N2 31

USB_HSD1P (C1) — USB20_P1 — USB20_P1 31 — USB-Right2

USB_HSD1N (C3) — USB20_N1 — USB20_N1 31

USB_HSD0P (E1) — USB20_P0 — USB20_P0 31 — USB-Right1

USB_HSD0N (E3) — USB20_N0 — USB20_N0 31

Hudson-M2/M3 OHCI (DEV-20, FUN-5)

Hudson-M2 OHCI (DEV-22, FUN-0) EHCI (DEV-22, FUN-2)

Hudson-M3 XHCI (DEV-16, FUN-0) XHCI (DEV-16, FUN-1)

Hudson-M2/M3 OHCI (DEV-19, FUN-0) EHCI (DEV-19, FUN-2)

Hudson-M2/M3 OHCI (DEV-18, FUN-0) EHCI (DEV-18, FUN-2) <Support Wakeup>

USBSS_CALRP (C16) — USBSS_CALRP — R330 1K_0402_1% M3@ — +VDDANCR_11_SSUSB

USBSS_CALRN (A16) — USBSS_CALRN — R334 1K_0402_1% M3@

USB_SS_TX3P (A14) USB_SS_TX3N (C14)

USB_SS_RX3P (C12) USB_SS_RX3N (A12)

USB_SS_TX2P (D15) USB_SS_TX2N (B15)

USB_SS_RX2P (E14) USB_SS_RX2N (F14)

USB_SS_TX1P (F15) USB_SS_TX1N (G15)

USB_SS_RX1P (H13) USB_SS_RX1N (G13)

USB_SS_TX0P (J16) — USB30_TX0P — USB30_TX0P 35 — USB 3.0 (For Hudson M3 only)

USB_SS_TX0N (H16) — USB30_TX0N — USB30_TX0N 35

USB_SS_RX0P (J15) — USB30_RX0P — USB30_RX0P 35

USB_SS_RX0N (K15) — USB30_RX0N — USB30_RX0N 35

Hudson-M3 XHCI (DEV-16, FUN-0) XHCI (DEV-16, FUN-1)

SCL2/GPIO193 (H19) — R326 10K_0402_5% — +3VALW

SDA2/GPIO194 (G19) — R328 10K_0402_5%

SCL3_LV/GPIO195 (G22) — FCH_SIC — APU_SIC 7,9

SDA3_LV/GPIO196 (G21) — FCH_SID — R338 0_0402_5% — APU_SID 7,9 — SB-TSI

R343 0_0402_5%

EC_PWM0/EC_TIMER0/GPIO197 (F22)

EC_PWM1/EC_TIMER1/GPIO198 (H22)

EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 (J22) — EC_PWM2 — EC_PWM2 25 — Strap

EC_PWM3/EC_TIMER3/GPIO200 (H21)

KSI_0/GPIO201 (K21) KSI_1/GPIO202 (K22) KSI_2/GPIO203 (F22) KSI_3/GPIO204 (F24) KSI_4/GPIO205 (E24) KSI_5/GPIO206 (B23) KSI_6/GPIO207 (C24) KSI_7/GPIO208 (F18)

Place R425 and C363 close to FCH for ESD

+3VALW R312 10K_0402_5% @ — +3VS R311 10K_0402_5%

ODD_DA#_FCH — R425 0_0402_5% — ODD_DA#_Q — Q208 2N7002_SOT23-3 — ODD_DA# 31

C379 0.1U_0402_16V4Z

+3VS CEC@ Q192 — R331 10K_0402_5% @ — +3VALW

9,30 HDMI_HPD — 2N7002_SOT23-3 — CEC@ R419 0_0402_5% — HDMI_HPD_FCH_R

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

Internal PU 10K

USB_OC1# is for USB port2

USB_OC0# is for USB port0 and port1

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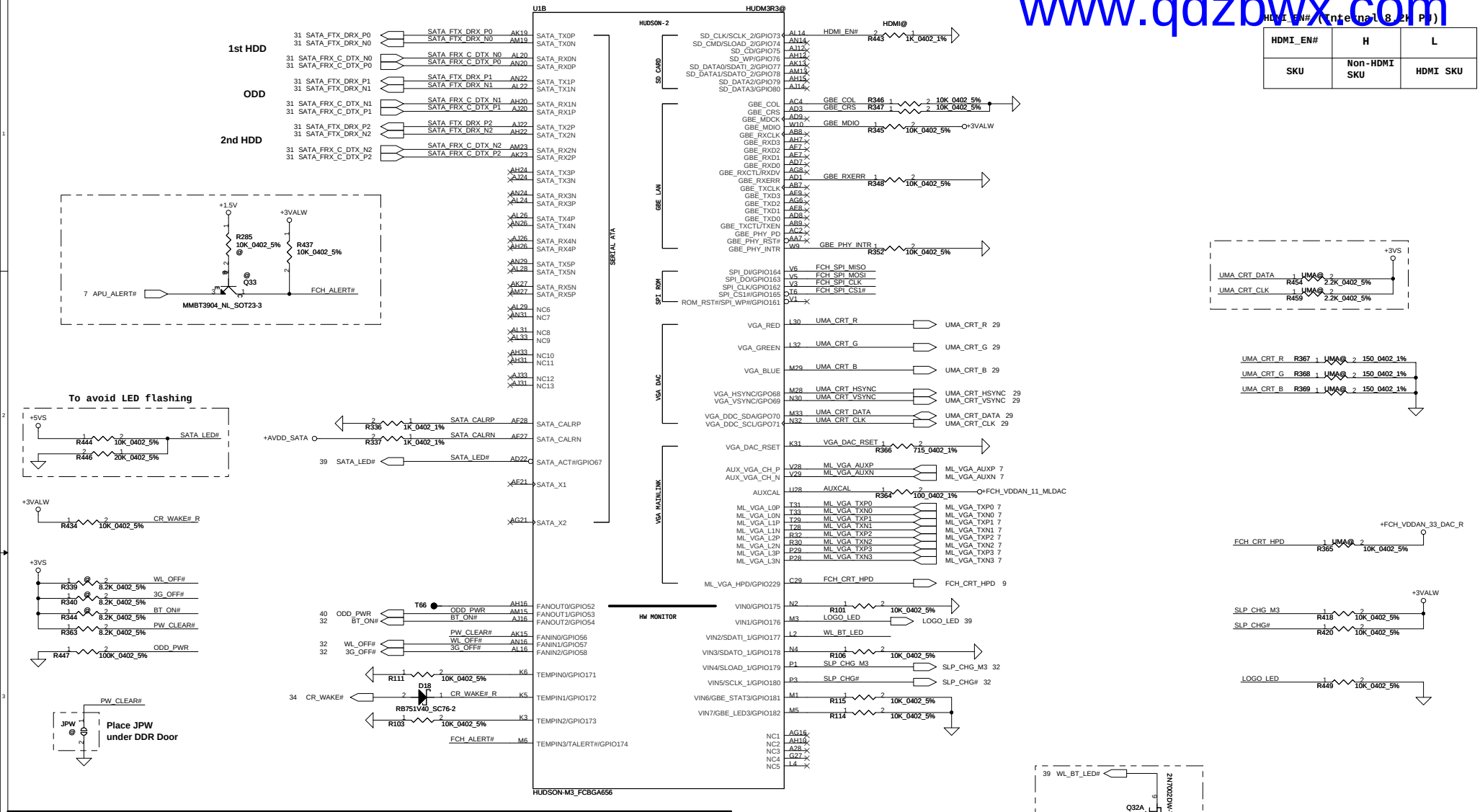
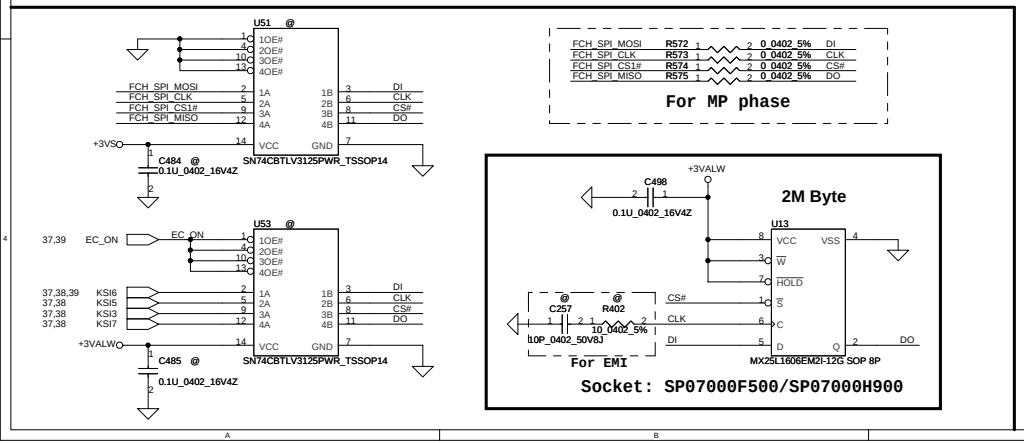
HDMI_EN# (Internal 8 K PU)		
HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU





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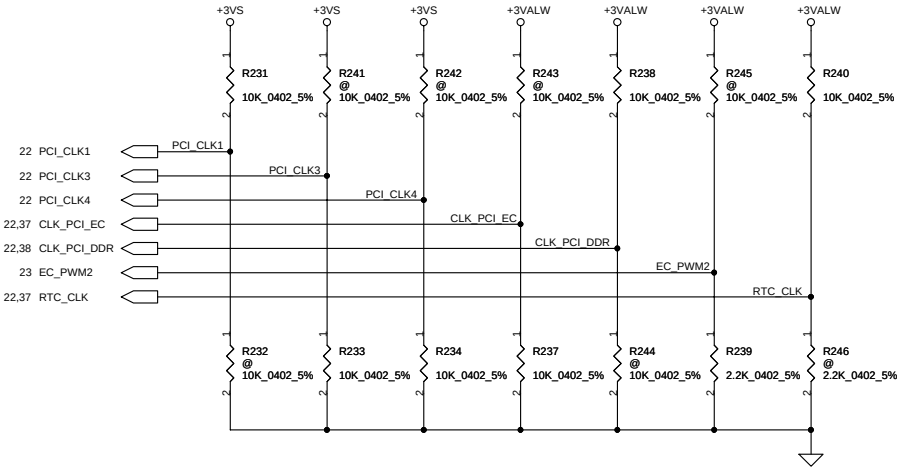
STRAP PINS

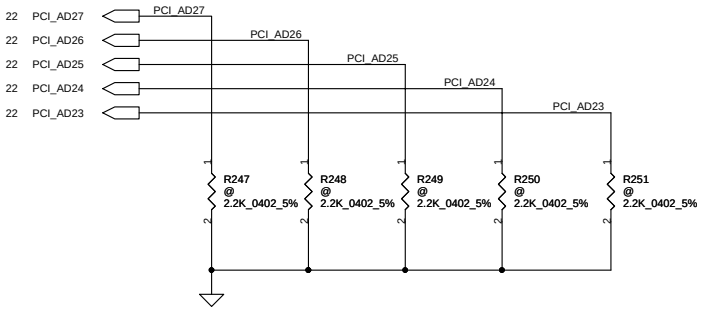
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



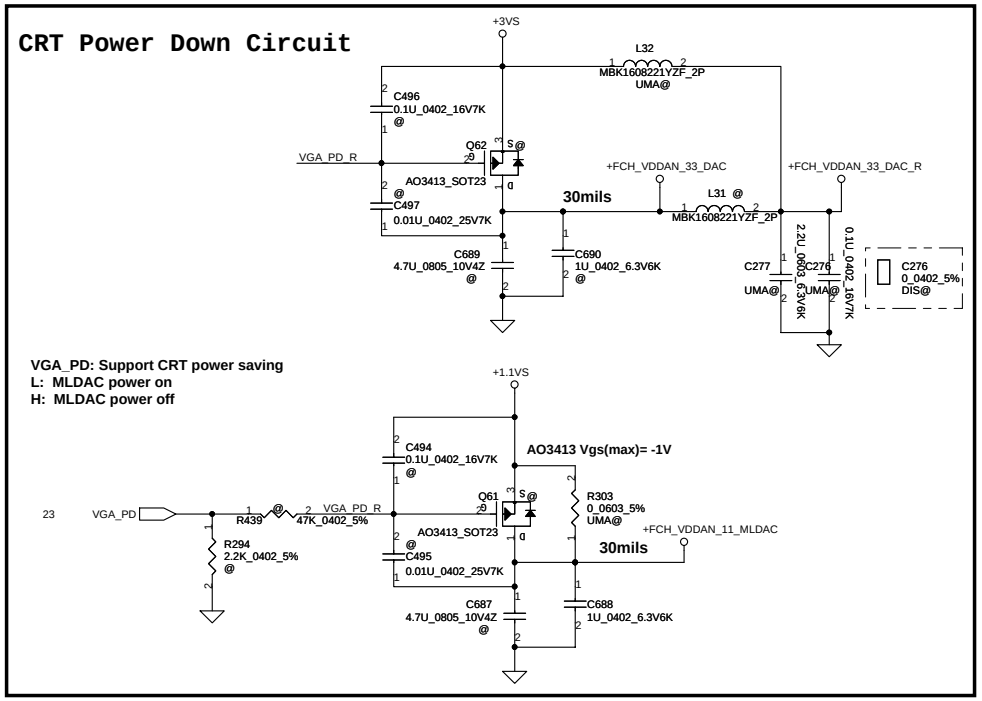
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



CRT Power Down Circuit



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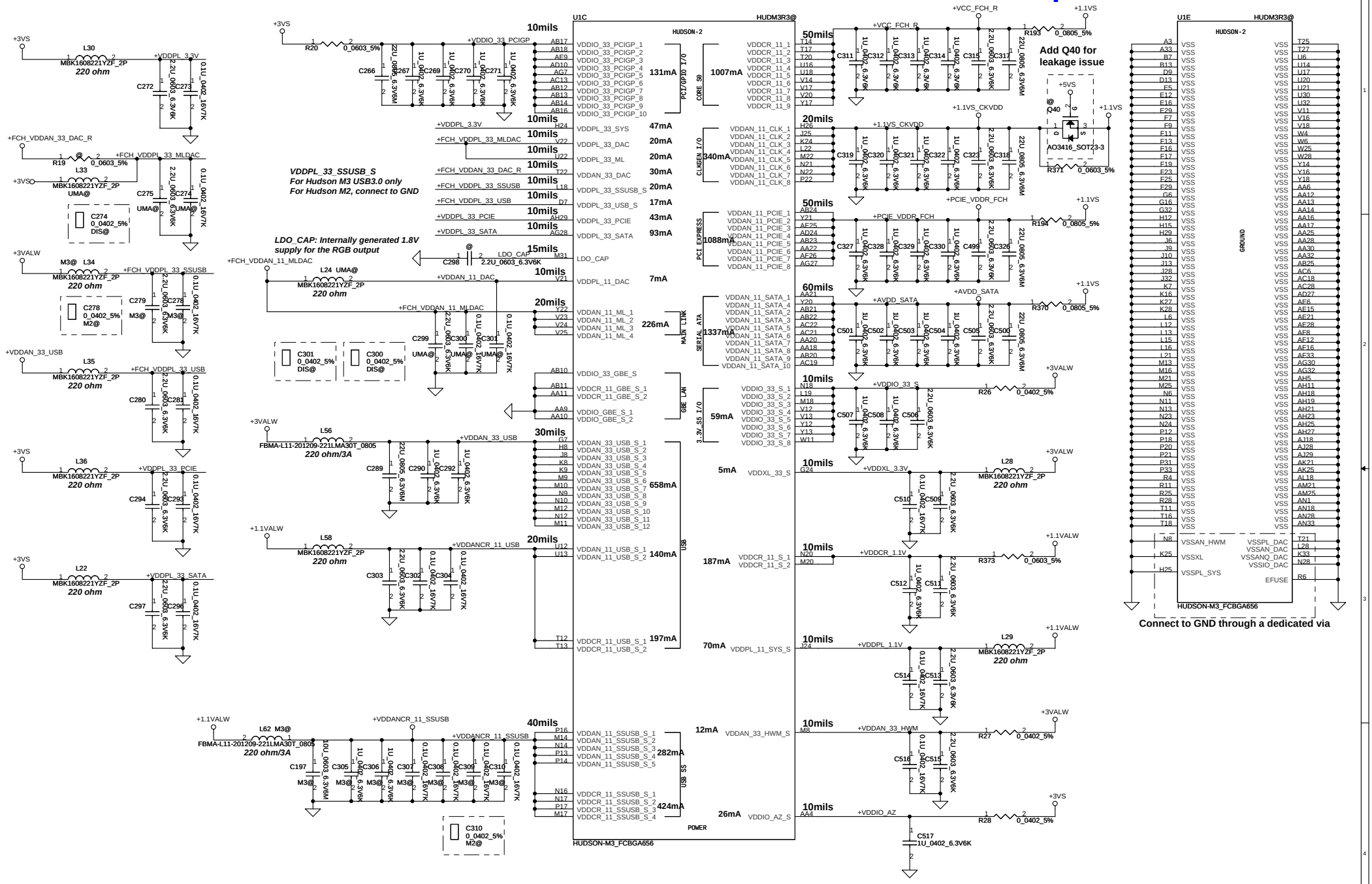

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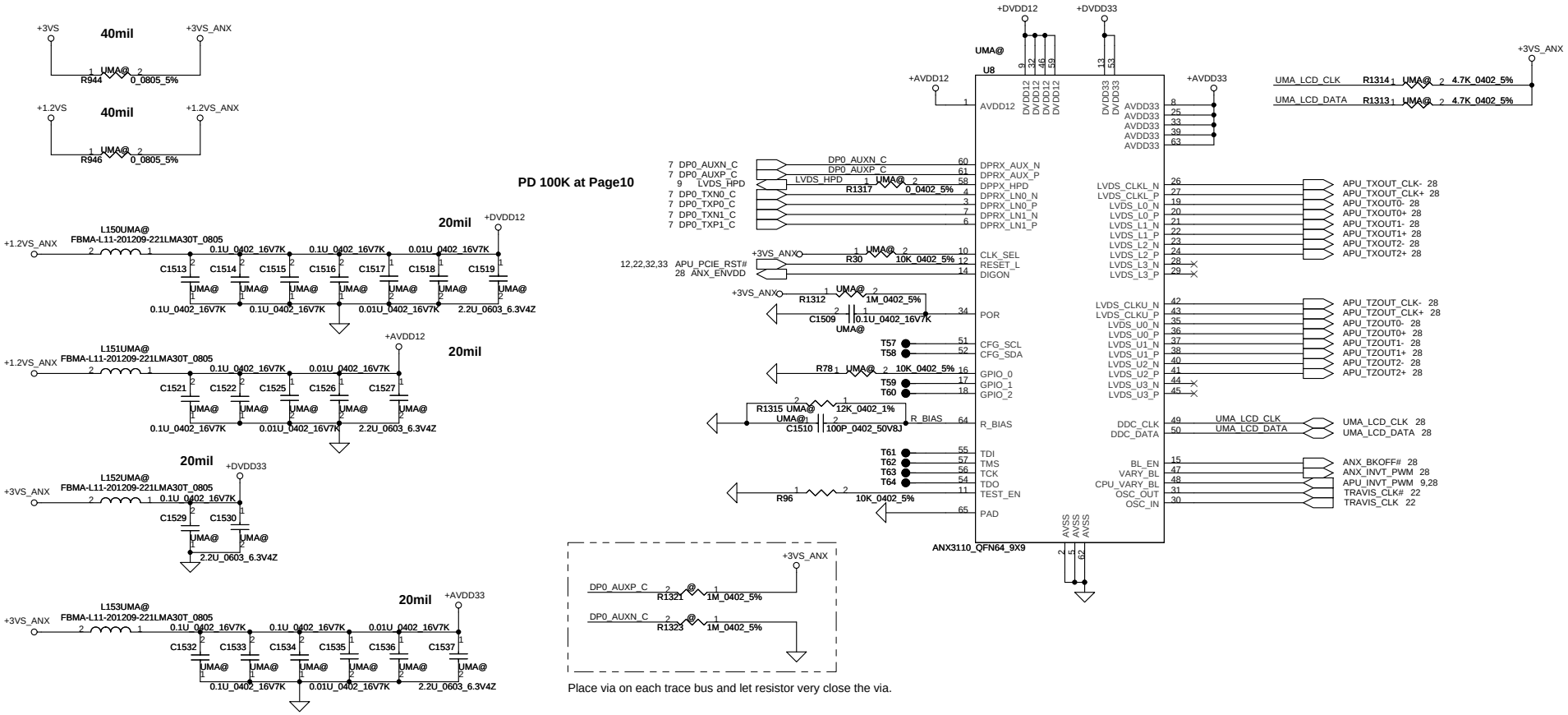

Place via on each trace bus and let resistor very close the via.

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For UMA & PowerXpress

27 APU_TXOUT0+	RD262	0_0402_5%	LVDS_TXOUT0+	
27 APU_TXOUT0-	RD263	0_0402_5%	LVDS_TXOUT0-	
27 APU_TXOUT1+	RD265	0_0402_5%	LVDS_TXOUT1+	
27 APU_TXOUT1-	RD264	0_0402_5%	LVDS_TXOUT1-	
27 APU_TXOUT2+	RD298	0_0402_5%	LVDS_TXOUT2+	
27 APU_TXOUT2-	RD277	0_0402_5%	LVDS_TXOUT2-	
27 APU_TXOUT_CLK+	RD297	0_0402_5%	LVDS_TXCLK+	
27 APU_TXOUT_CLK-	RD296	0_0402_5%	LVDS_TXCLK-	
27 APU_TZOUT0+	RD268	0_0402_5%	LVDS_TZOUT0+	
27 APU_TZOUT0-	RD267	0_0402_5%	LVDS_TZOUT0-	
27 APU_TZOUT1+	RD269	0_0402_5%	LVDS_TZOUT1+	
27 APU_TZOUT1-	RD266	0_0402_5%	LVDS_TZOUT1-	
27 APU_TZOUT2+	RD302	0_0402_5%	LVDS_TZOUT2+	
27 APU_TZOUT2-	RD278	0_0402_5%	LVDS_TZOUT2-	
27 APU_TZOUT_CLK+	RD301	0_0402_5%	LVDS_TZCLK+	
27 APU_TZOUT_CLK-	RD303	0_0402_5%	LVDS_TZCLK-	
27 UMA_LCD_CLK	RD300	0_0402_5%	LVDS_EDID_CLK	
27 UMA_LCD_DATA	RD299	0_0402_5%	LVDS_EDID_DATA	
9,27 APU_INVT_PWM	RD332	0_0402_5%	LED_PWM	
9 APU_ENVDD	RD350	0_0402_5%	LCD_ENVDD	
9 APU_ENBKL	RD357	0_0402_5%	EC_ENBKL	EC_ENBKL 37

Close to LVDS Connector

To prevent EC pin damage

RD449 0_0402_5%
LED_PWM — DD29 RB751V40_SC76-2 — LED_PWM_D — RD144 47K_0402_5%

37 BKOFF# — DD30 RB751V40_SC76-2 — BKOFF#_D — RD113 10K_0402_5%

Reserve for EMI request

23 USB20_N5 — RD78 0_0402_5% — USB20_N5_R
23 USB20_P5 — LD55 WCM-2012-900T_0805 — USB20_P5_R
RD96 0_0402_5%

EC PWM

37 INVT_PWM — RD387 0_0402_5% — LED_PWM

For DISCRETE

Remove LVDS channel

12 VGA_INVT_PWM	RD349	0_0402_5%	LED_PWM
12 VGA_ENVDD	RD355	0_0402_5%	LCD_ENVDD
13 VGA_ENBKL	RD358	0_0402_5%	EC_ENBKL

Close to LVDS Connector

Remove DISCRETE for 3D LVDS Panel

Remove 3D LVDS Panel

DISCRETE for 3D eDP Panel

13 VGA_EDP_TX0+	CD880	0.1U_0402_16V7K	LVDS_TXOUT0+	
13 VGA_EDP_TX0-	CD881	0.1U_0402_16V7K	LVDS_TXOUT0-	
13 VGA_EDP_TX1+	CD882	0.1U_0402_16V7K	LVDS_TXOUT1+	
13 VGA_EDP_TX1-	CD883	0.1U_0402_16V7K	LVDS_TXOUT1-	
13 VGA_EDP_TX2+	CD884	0.1U_0402_16V7K	LVDS_TXOUT2+	
13 VGA_EDP_TX2-	CD885	0.1U_0402_16V7K	LVDS_TXOUT2-	
13 VGA_EDP_TX3+	CD886	0.1U_0402_16V7K	LVDS_TXCLK+	
13 VGA_EDP_TX3-	CD887	0.1U_0402_16V7K	LVDS_TXCLK-	

Close to LVDS1 Connector

13 VGA_EDP_AUX+	CD888	0.1U_0402_16V7K	LVDS_EDID_CLK
13 VGA_EDP_AUX-	CD889	0.1U_0402_16V7K	LVDS_EDID_DATA

Close to LVDS Connector

LCD/PANEL BD. Conn.

+3VS — RD388 CAM@ 0_0603_5% — +3VS_LVDS_CAM — CD229 CAM@ 0.1U_0402_16V4Z — W=20mils

JLVDS @ — ACES_87242-4001-09

USB20_P5_R	3	
USB20_N5_R	5	
LVDS_TXOUT0+	9	LVDS_TXCLK+
LVDS_TXOUT0-	11	LVDS_TXCLK-
LVDS_TXOUT1+	13	LVDS_TZCLK+
LVDS_TXOUT1-	15	LVDS_TZCLK-
LVDS_TXOUT2+	17	LVDS_EDID_CLK
LVDS_TXOUT2-	19	LVDS_EDID_DATA
	21	INT_MIC_CLK
LVDS_TZOUT0+	23	INT_MIC_DATA
LVDS_TZOUT0-	25	LCD_ENVDD
LVDS_TZOUT1+	27	LED_PWM_D
LVDS_TZOUT1-	29	+3VS_LVDSDDC
LVDS_TZOUT2+	31	
LVDS_TZOUT2-	33	
BKOFF# D	35	
	37	
	39	GMD
	41	

+LCD_INV — +LCD_INV

DD84 YSLC05CH_SOT23-3 — INT_MIC_CLK 36, INT_MIC_DATA 36

3A — CD226 0.1U_0402_16V4Z — CD227 4.7U_0805_10V4Z — +LCD_VDD

+3VS — RD209 EDP@ 100K_0402_5% — LVDS_EDID_DATA
RD256 EDP@ 100K_0402_5% — LVDS_EDID_CLK

For LVDS Translator

27 ANX_INVT_PWM	RD333	0_0402_5%	LED_PWM	
27 ANX_ENVDD	RD351	0_0402_5%	LCD_ENVDD	
27 ANX_BKOFF#	RD360	0_0402_5%	EC_ENBKL	

RD107 150_0603_5% UMA@ — RD108 100K_0402_5% UMA@ — RD120 100K_0402_5% EDP@ — RD109 47K_0402_5% UMA@ — RD112 100K_0402_5% UMA@

QD1A 2N7002DW-T/R7_SOT363-6 UMA@ — QD1B 2N7002DW-T/R7_SOT363-6 UMA@ — LCD_ENVDD

LCDPWR_GATE — CD228 0.1U_0402_16V7K UMA@ — CD229 0.01U_0402_25V7K UMA@ — QD17 AO3413_SOT23 UMA@ — +LCD_VDD — CD233 0.1U_0402_16V4Z UMA@ — W=80mils

+3VS — +5VS — EDP@ CD251 0.1U_0402_16V7K — QD23 AO3413_SOT23 EDP@ — +LCD_VDD — W=80mils

RD101 150_0603_5% EDP@ — RD119 47K_0402_5% EDP@ — CD233 0.1U_0402_16V4Z EDP@ — CD229 0.01U_0402_25V7K EDP@ — QD1 2N7002DW-T/R7_SOT363-6 EDP@

RD107 150_0603_5% NO3D@ — RD108 100K_0402_5% NO3D@ — RD109 47K_0402_5% NO3D@ — CD228 0.1U_0402_16V7K NO3D@
QD1 2N7002DW-T/R7_SOT363-6 NO3D@ — CD229 0.01U_0402_25V7K NO3D@ — CD233 0.1U_0402_16V4Z NO3D@
QD17 AO3413_SOT23 NO3D@

RD1440 0_0603_5% UMA@

+3VS_LVDSDDC — RD143 EDP@ 0_0402_5% — EDP_HPD 13
RD1440 NOEDP@ 0_0603_5% — +3VS

For EMI — CD231 680P_0402_50V7K — NOEDP@ CD232 0.1U_0402_16V4Z

CD232 0.1U_0402_16V4Z UMA@

+LCD_INV — CD234 68P_0402_50V8J — LD2 FBMA-L11-201209-221LMA30T_0805 — CD235 0.1U_0402_25V6 — B+

For EMI — B+ — CD235 @ — CD268 @ — CD489 @ — CD490 @ — 0.1U_0402_25V6

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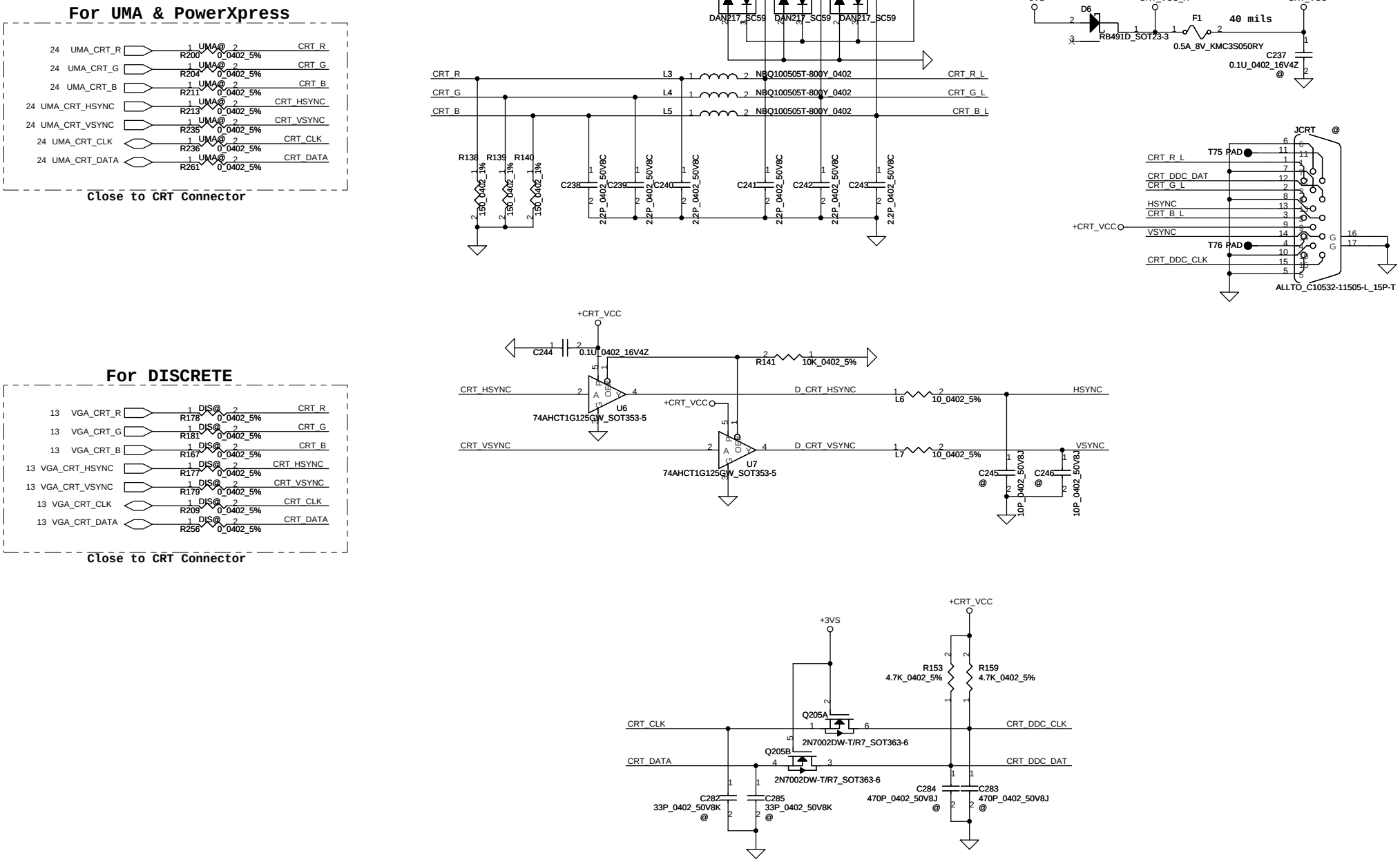
CRT CONNECTOR



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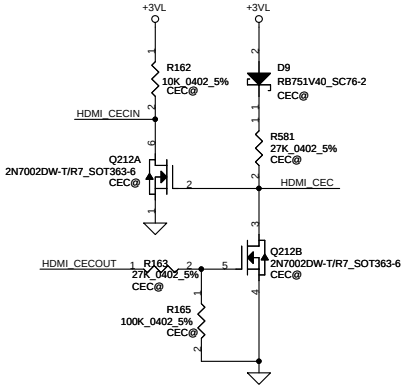
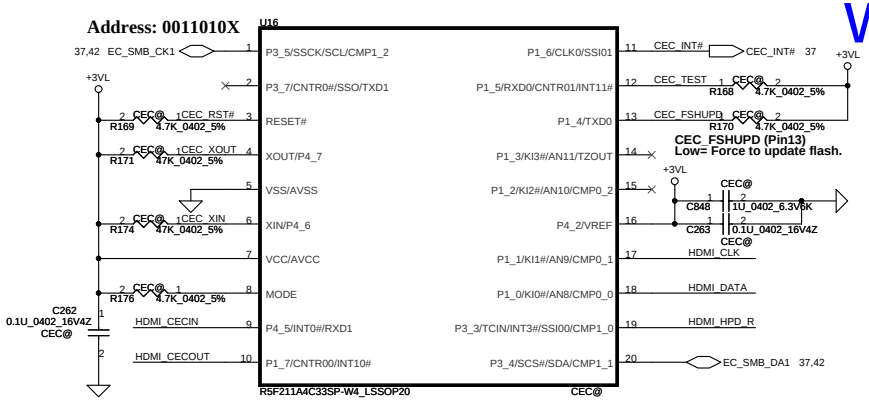
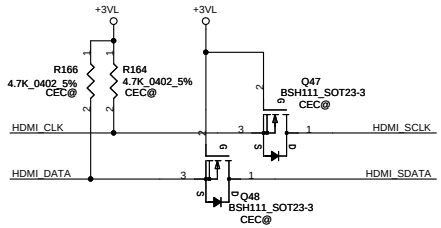
HDMI CEC Controller







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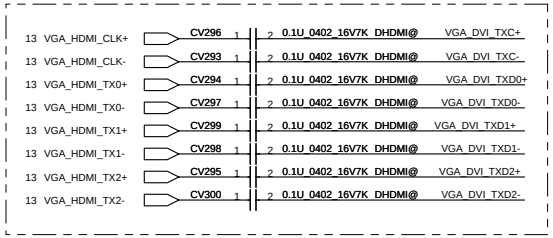

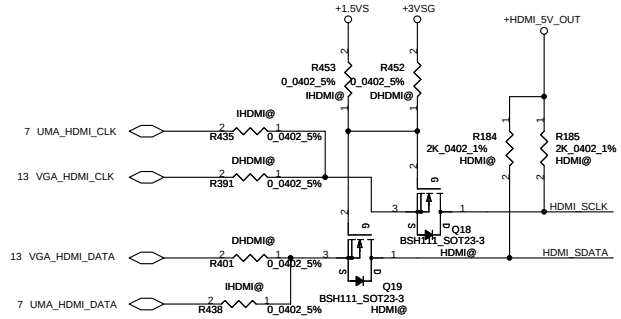

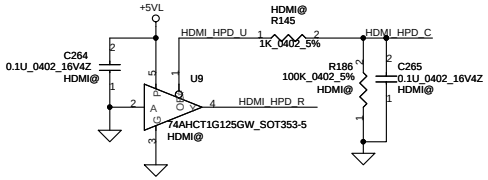

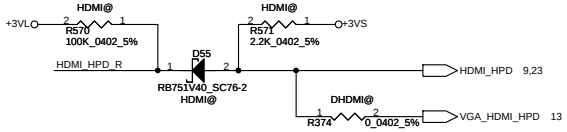

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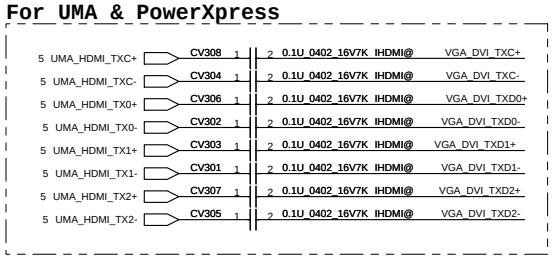
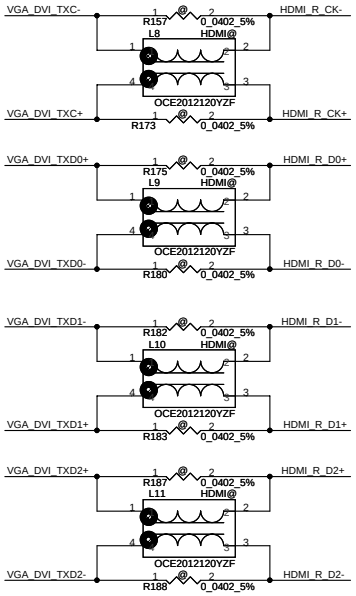
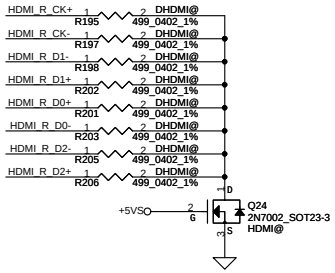
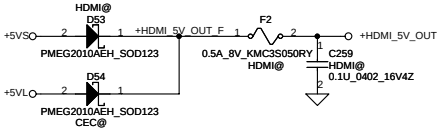
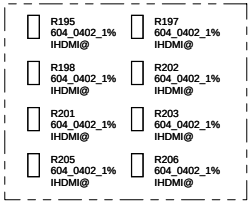


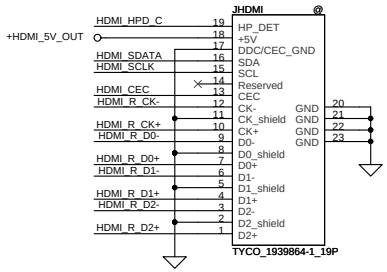








HDMI Connector



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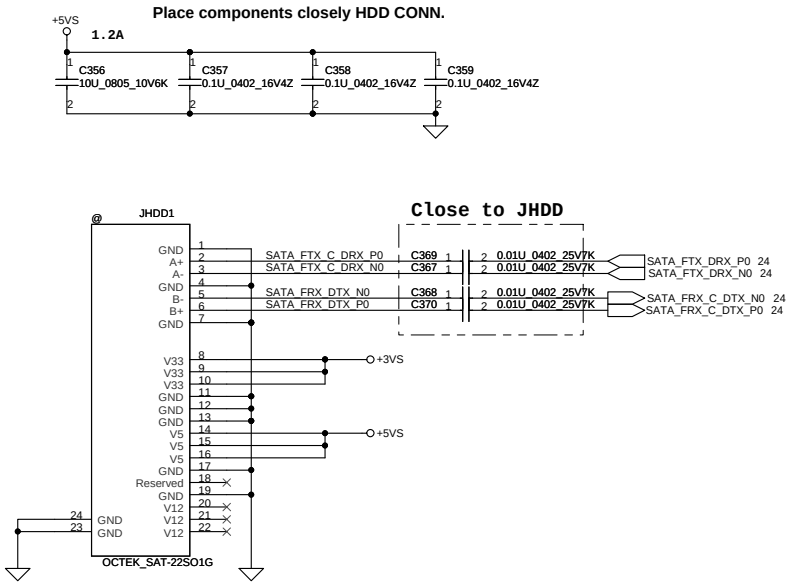
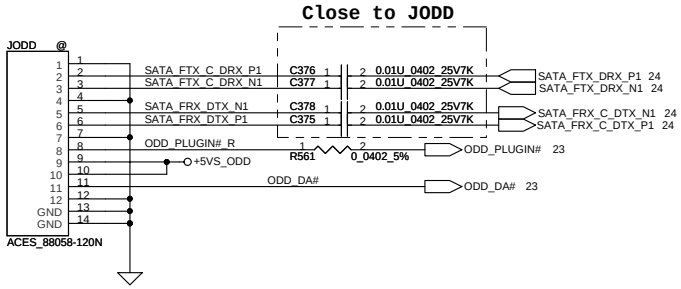
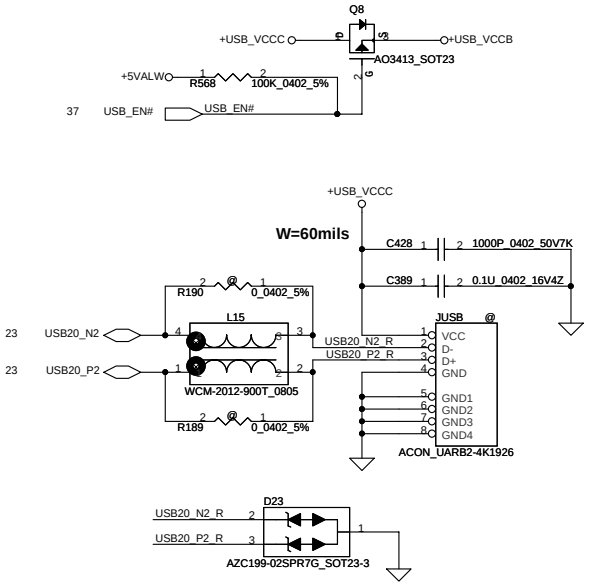
SATA HDD Conn.



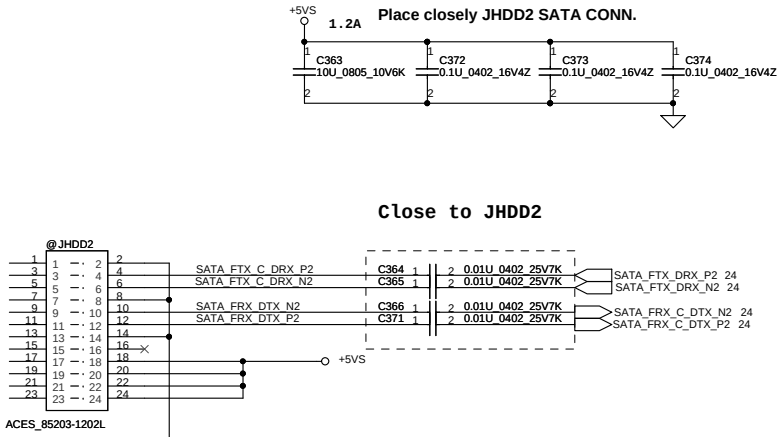
SATA ODD Conn.



USB Board@ Left Side

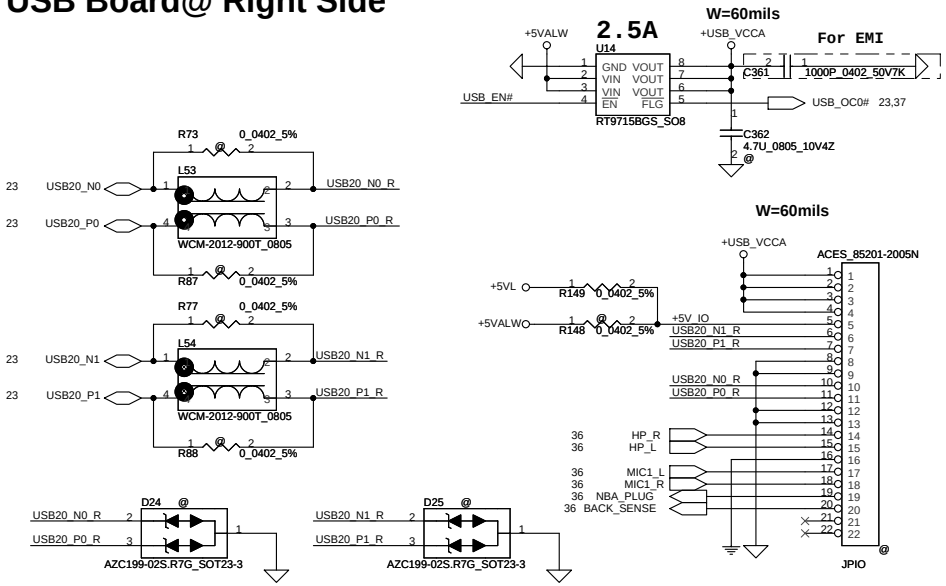


SATA 2nd HDD Conn.



Confirm SSD need 3V or not.

USB Board@ Right Side



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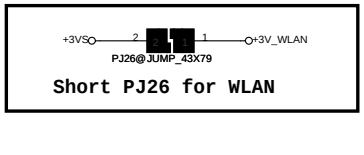
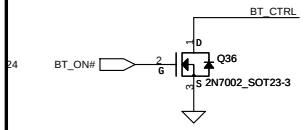
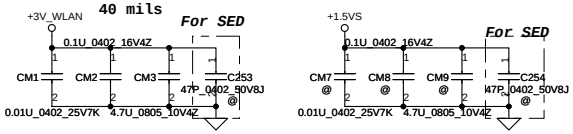
Slot 1 Half PCIe Mini Card-WLAN

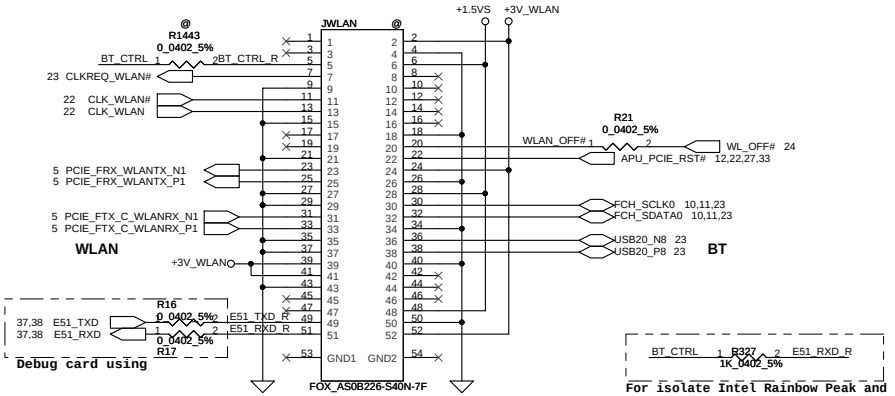


WLAN&BT Combo module circuits



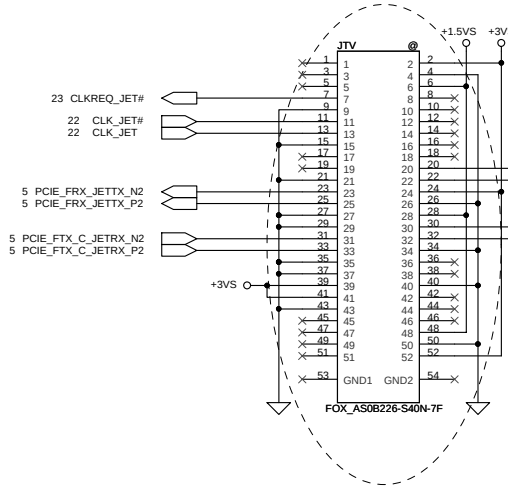
	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H



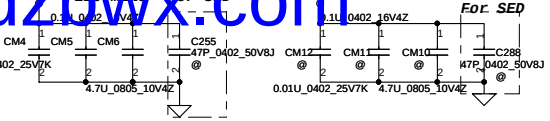


Slot 2 Half PCIe Mini Card- JET

Remove 3G/TV tuner

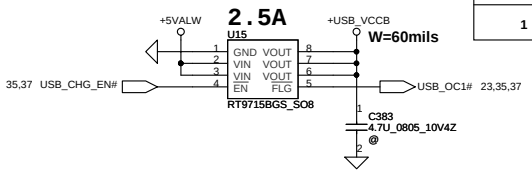


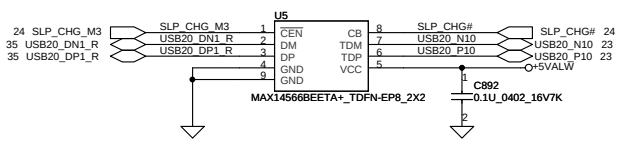
Need to double check JET pin define



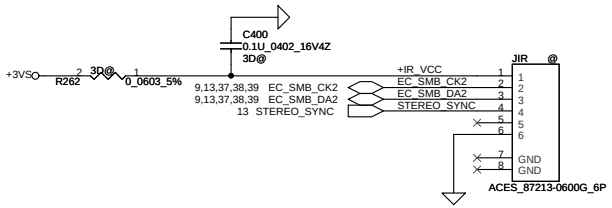
USB Sleep & Charge: Auto-Mode Mode3

MAX14566B		
CB SLP_CHG#	CEN# SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM





IR Emitter Connector



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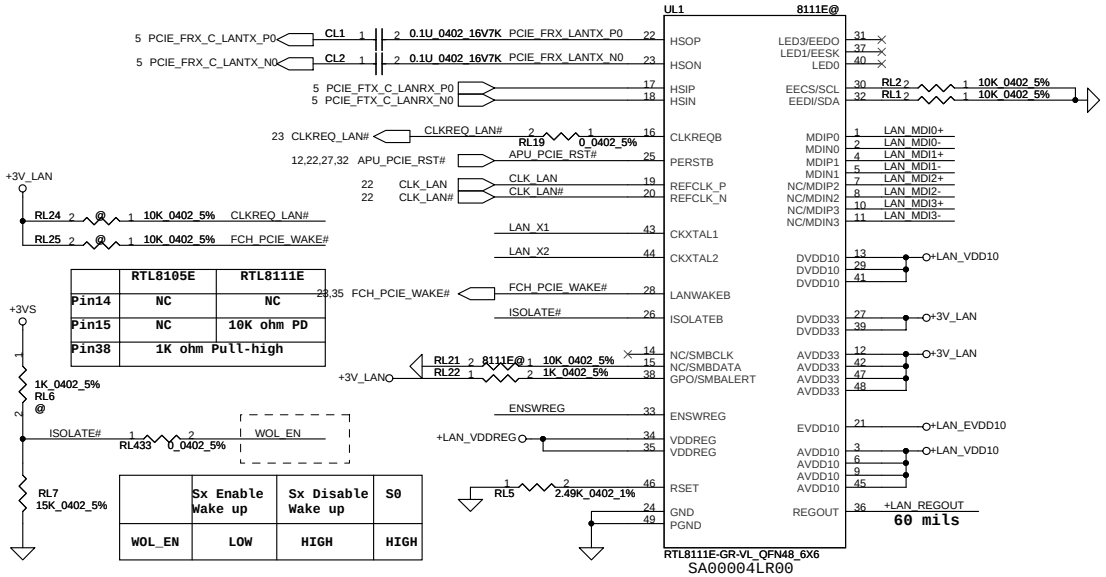
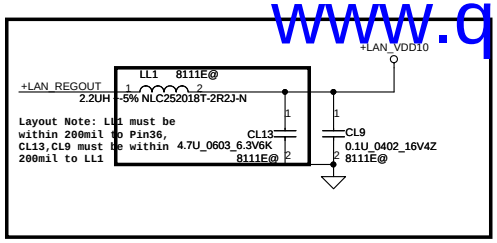
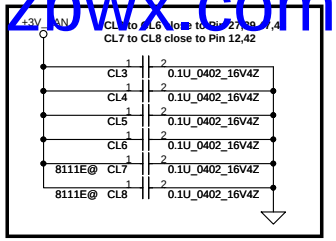
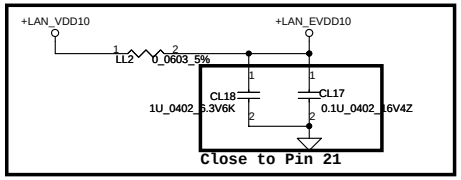


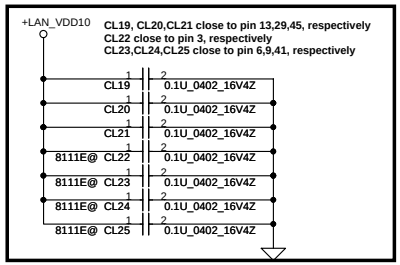
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

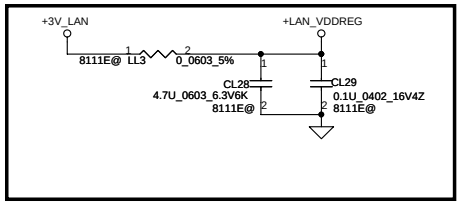
	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN	LOW	HIGH	HIGH

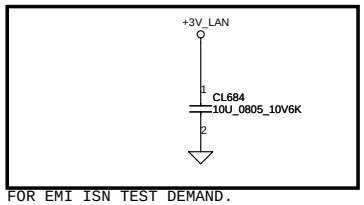






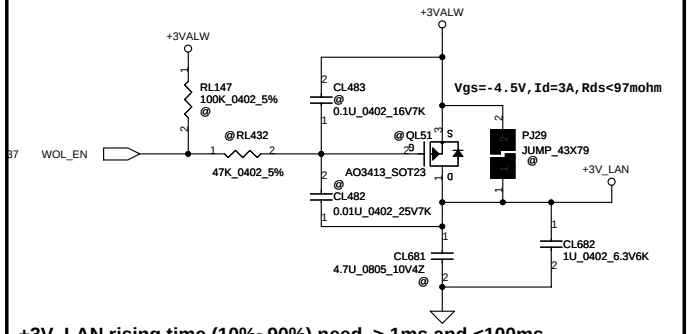




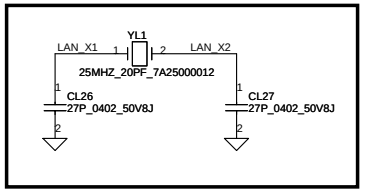


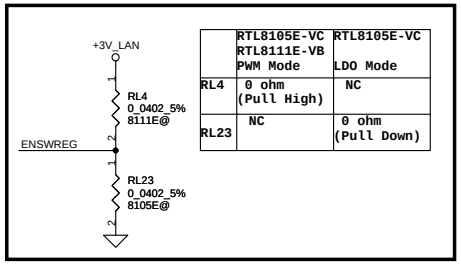
FOR EMI ISN TEST DEMAND.

+3VALW TO +3V_LAN



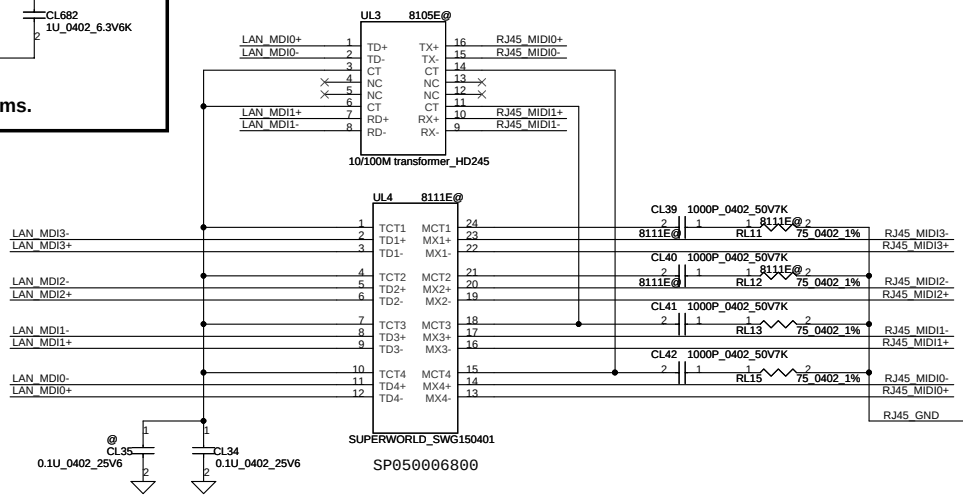
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.





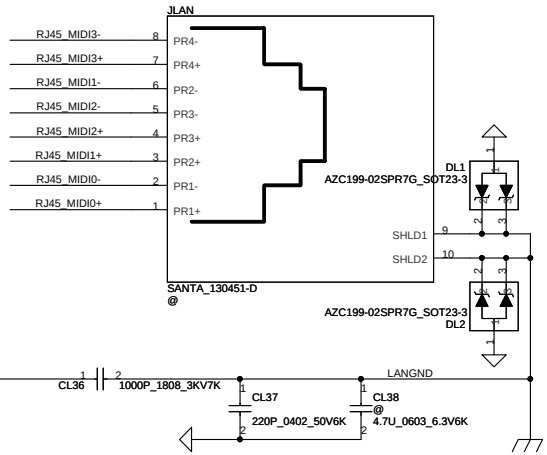
	RTL8105E-VC RTL8111E-VB PWM Mode	RTL8105E-VC LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

SP050006W00

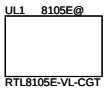


SP050006800

LAN Conn.



For P/N and footprint
Please place them to ISPD page



SA00003PO30

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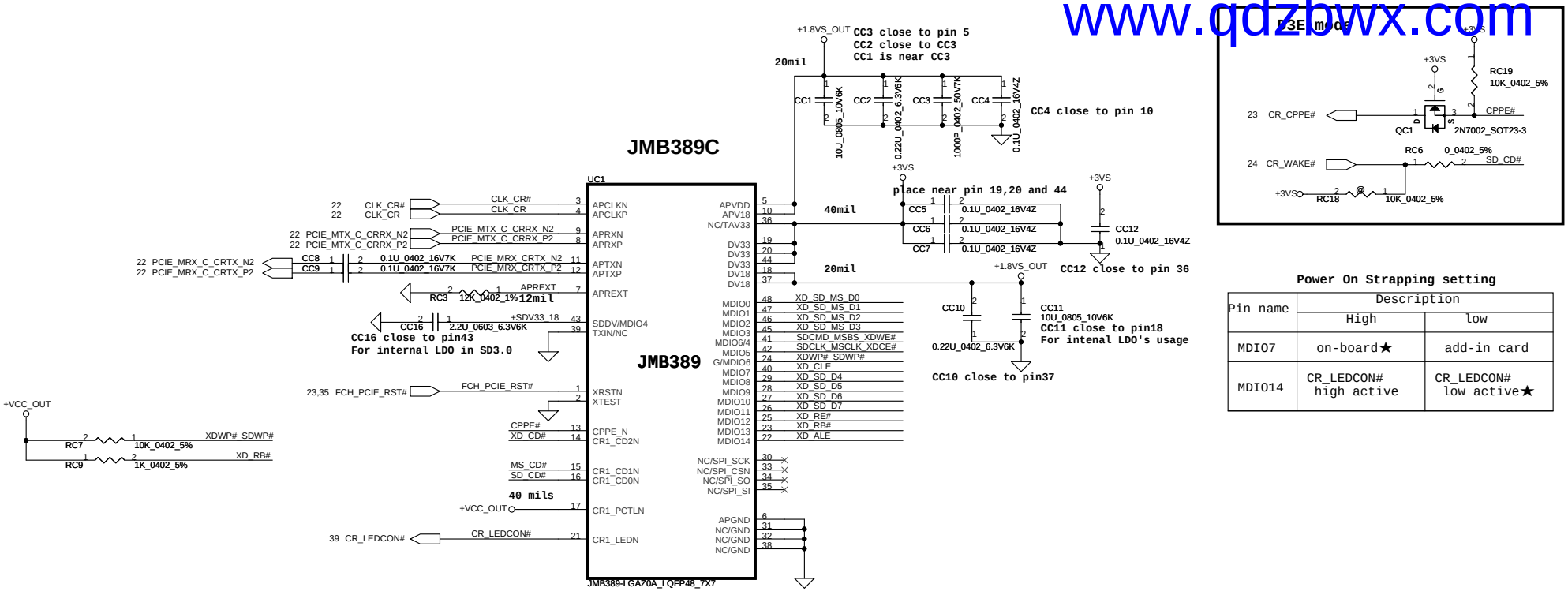
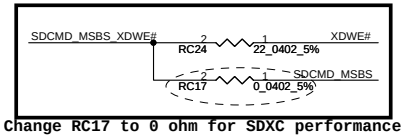


Power On Strapping setting

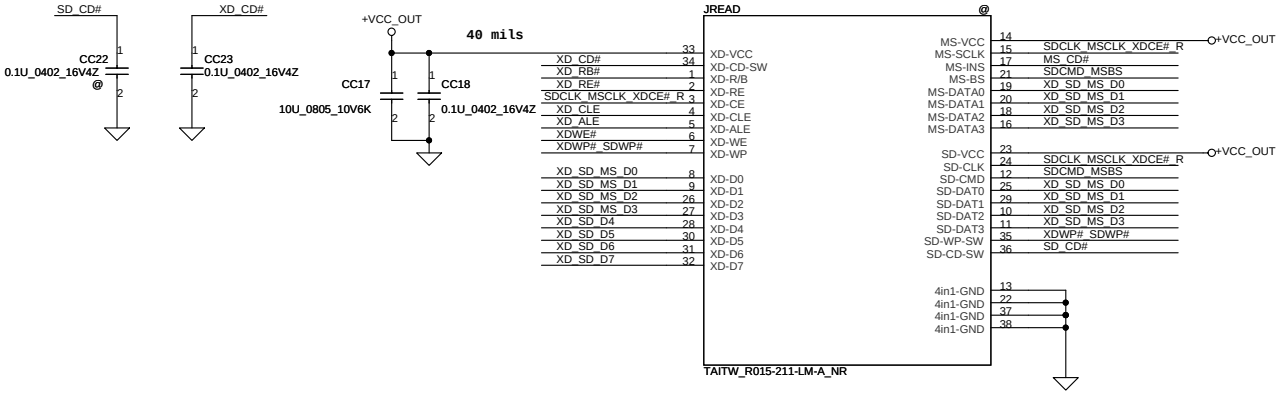
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LEDCON# high active	CR_LEDCON# low active★

Add RC24 and RC17 close to UC1 for xD issue

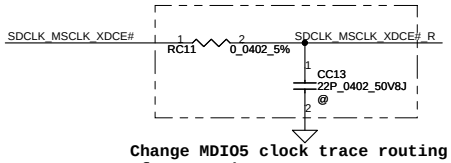


Change RC17 to 0 ohm for SDXC performance low issue

5 in 1 Card Reader



Reserved for EMI,close to UC1.42



Change MDIO5 clock trace routing for SDHC issue

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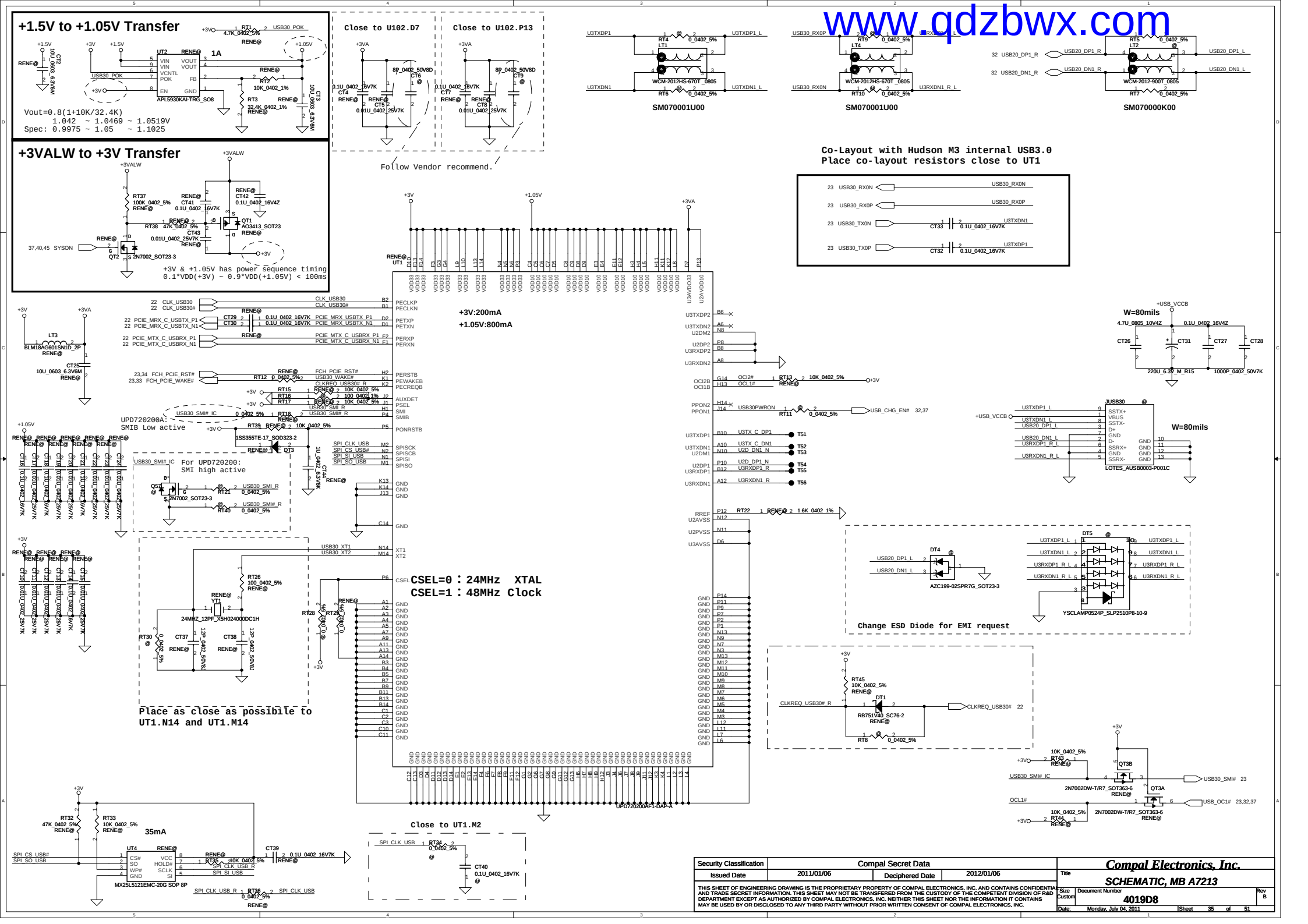

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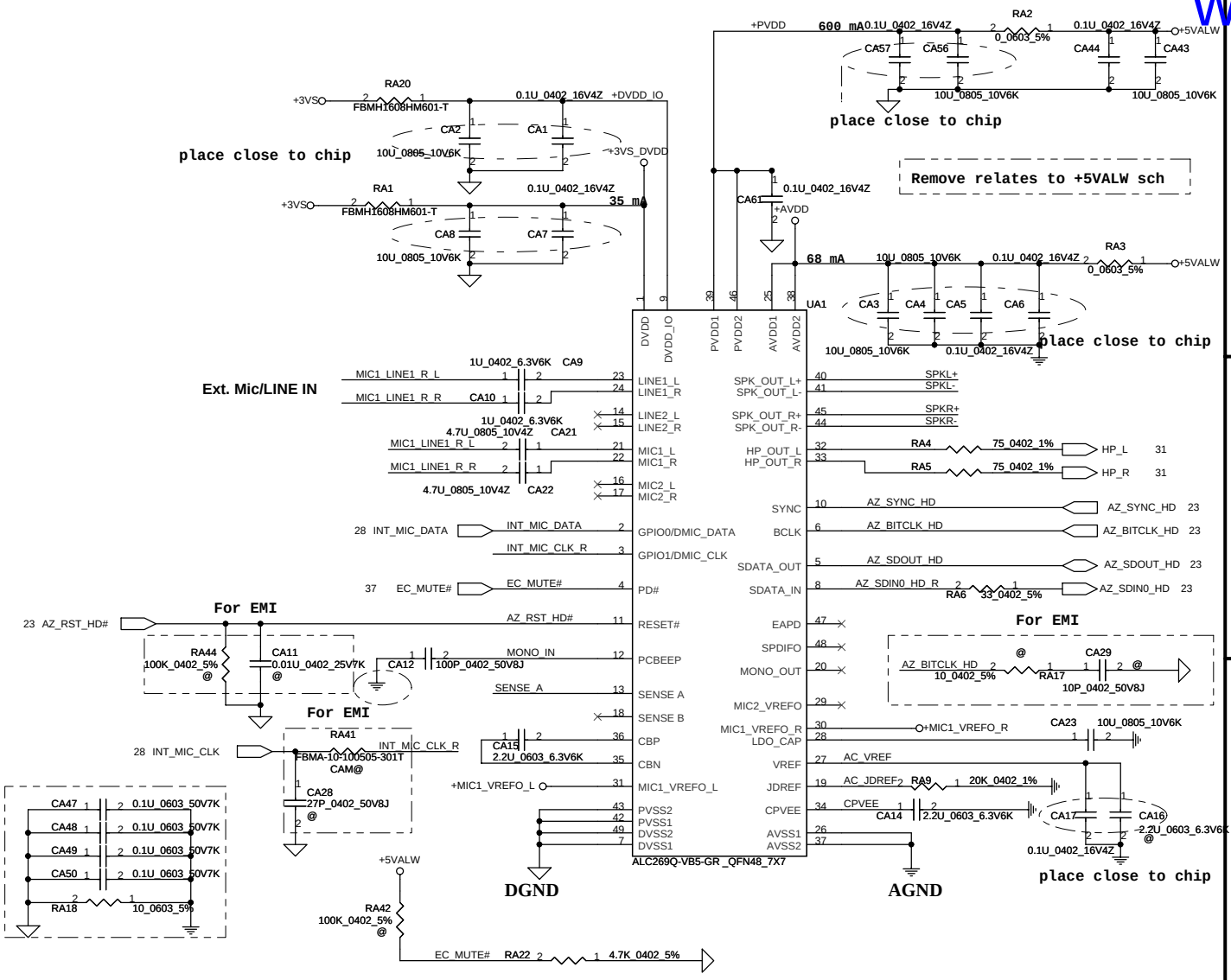
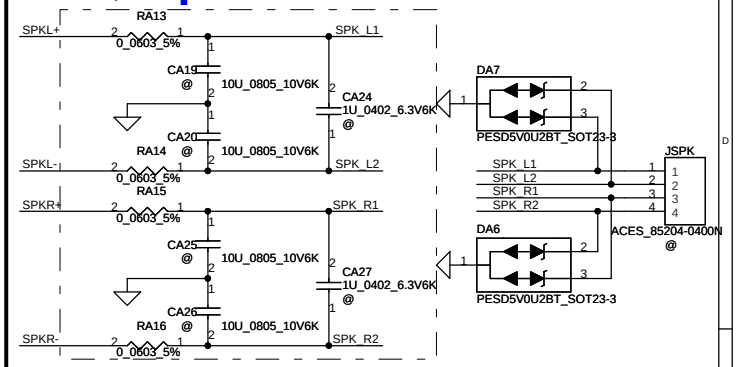
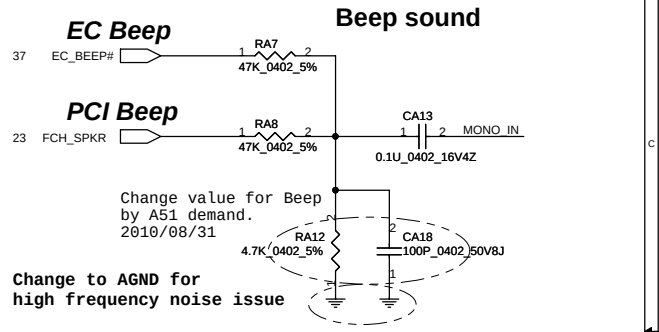


Speaker Connector

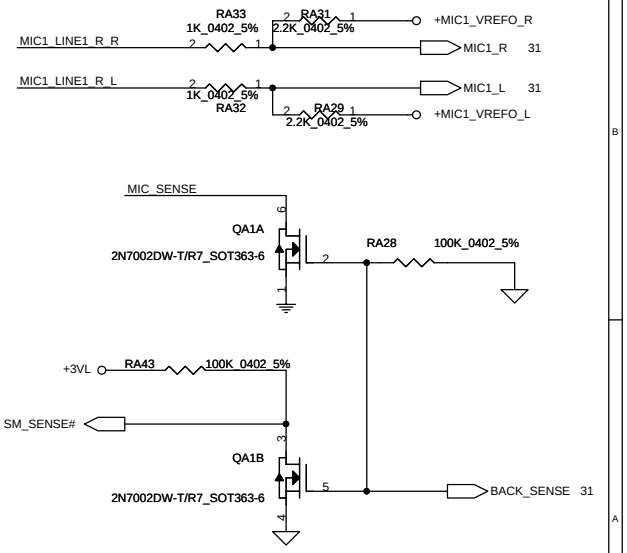
placement near Audio Codec



Beep sound

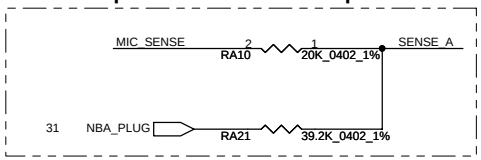


Ext.MIC/LINE IN JACK



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

place close to chip



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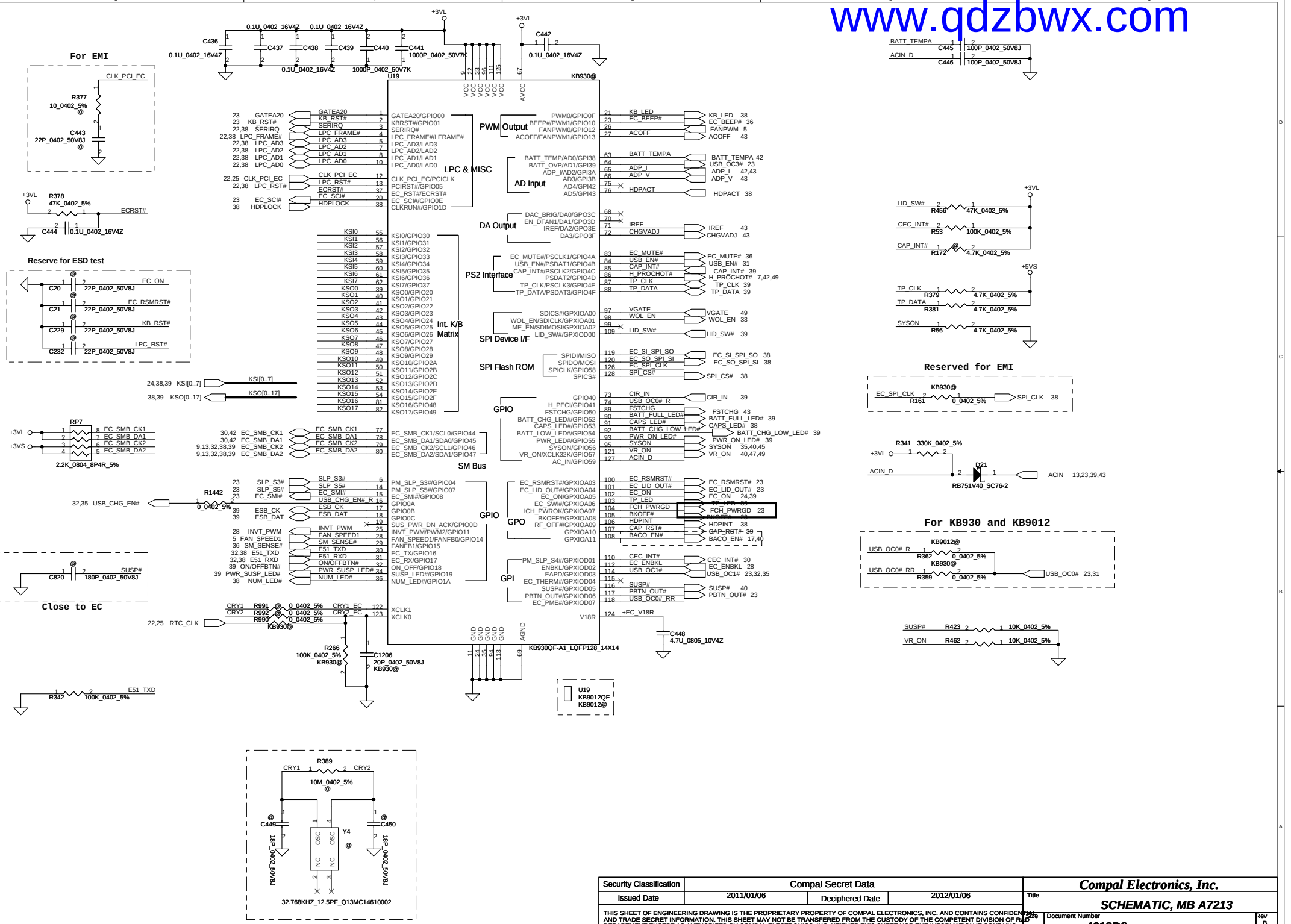

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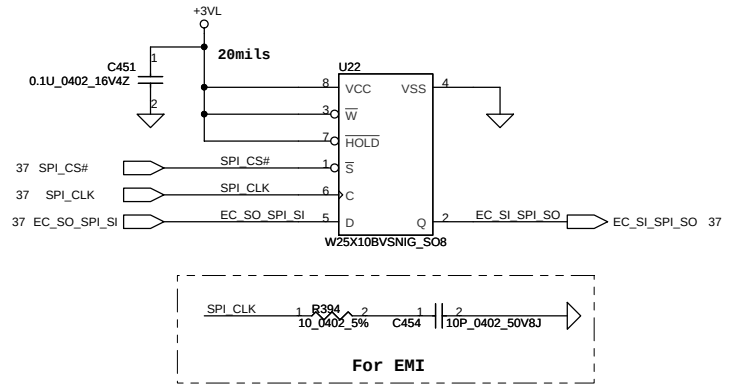
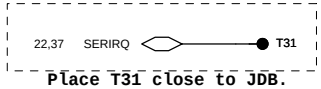
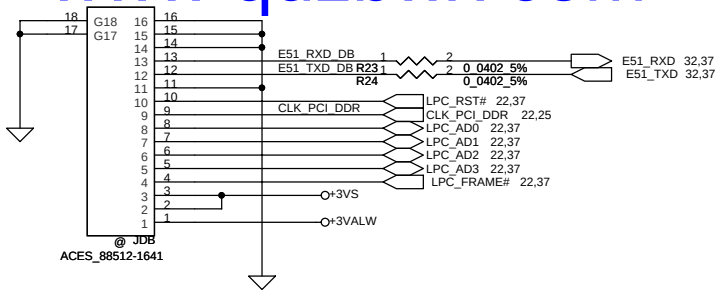
SPI Flash (128KB)



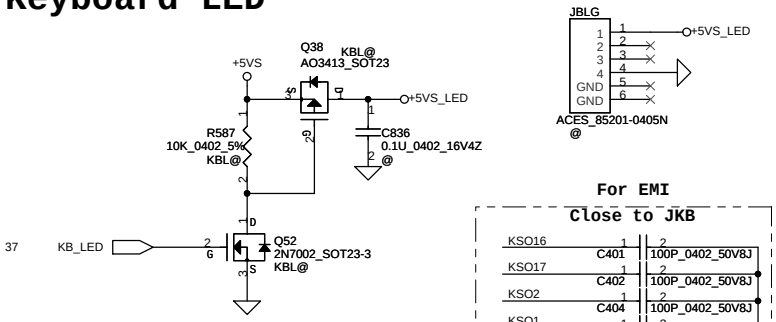
LPC Debug Port

Place JDB under DDR DIMM.

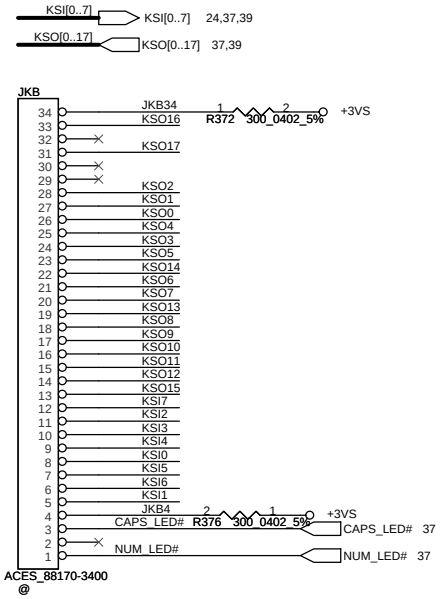




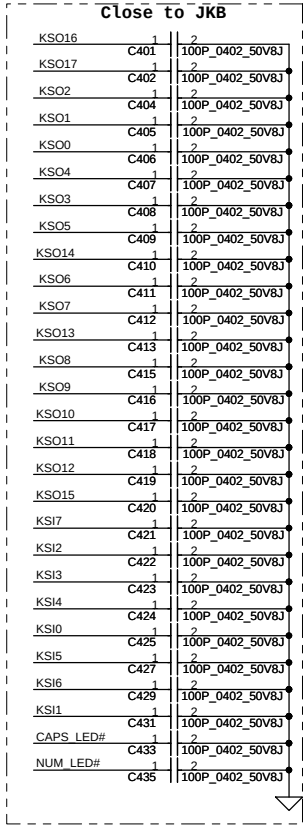
Keyboard LED



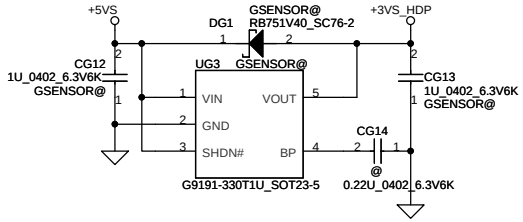
KEYBOARD CONN.



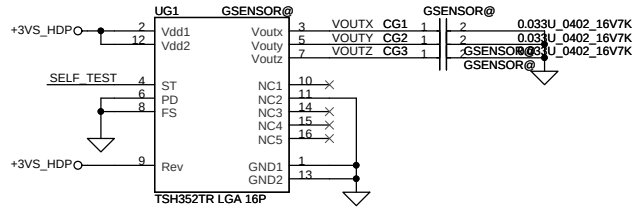
For EMI
Close to JKB

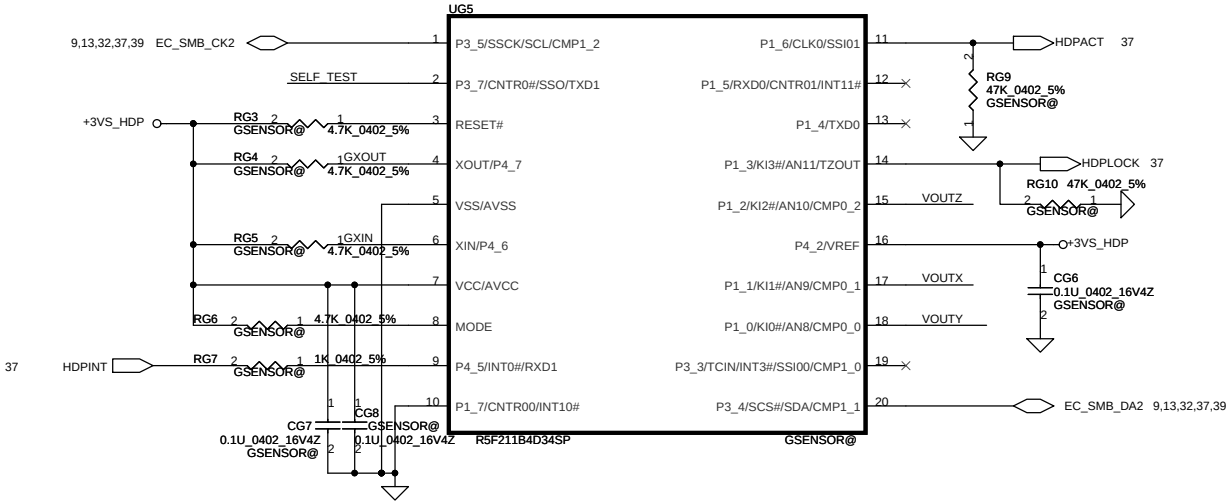


G-Sensor



Place UG1 on TOP Layer





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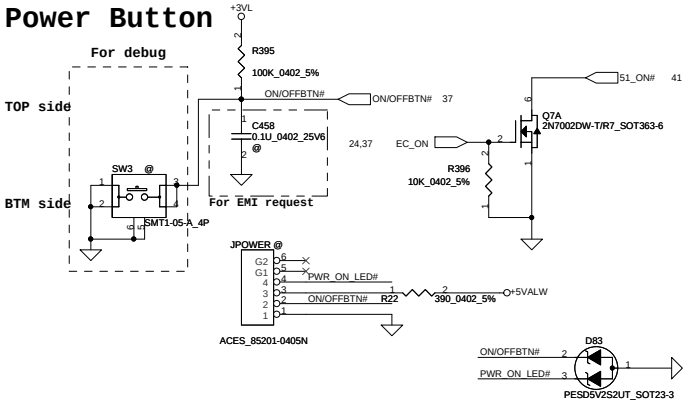
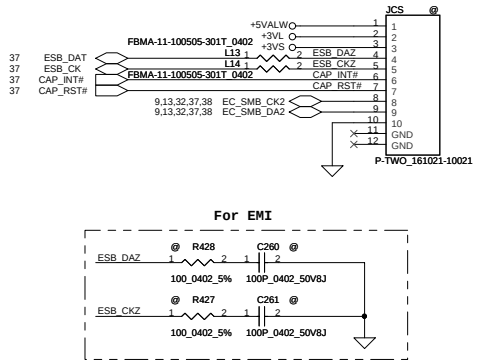
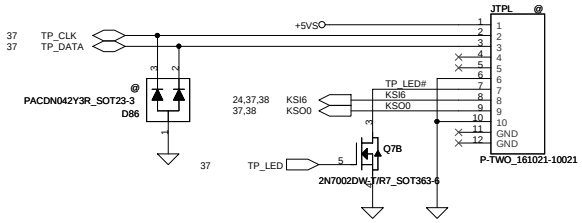
Power Button



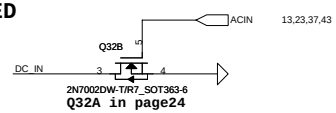
Caps Sensor/Light Sensor Conn.



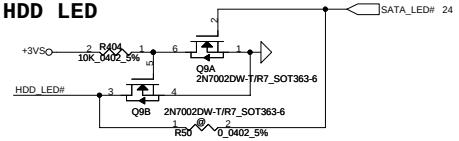
Touchpad & Light Pipe Connector

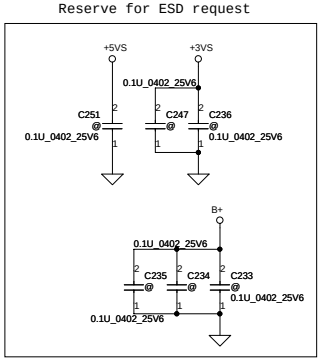


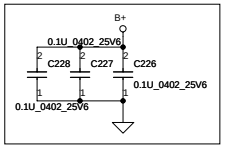
DC-IN LED

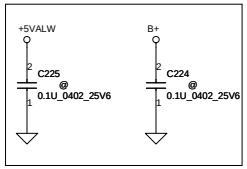


HDD LED

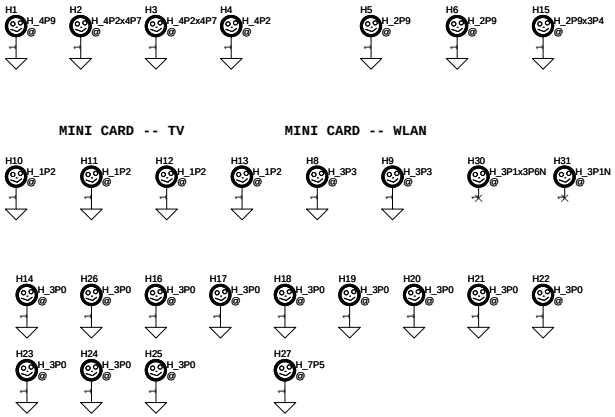




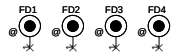




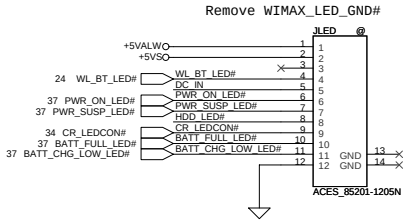
Screw Hole



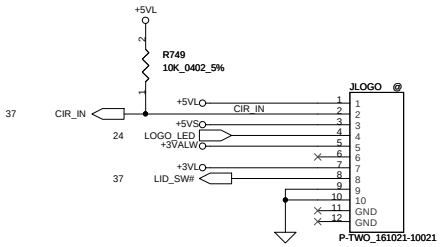
PCB Fedical Mark PAD



LED/B Connector



LOGO/B Connector



ISPD

WHPROR3@
SA00004C790

UV1 WHPROR1@
SA00004C780
216-0810005 A11 WHISTLER PRO

ZZZ
DAZ0K600100
PCB LA-7213P

U1 HUDM3R1@
SA000043I60
218-0755022 A13 HUDSON-M3

PJP1 45@
DC30100AA00
PJP1

HUDM3R3@
SA000043I70

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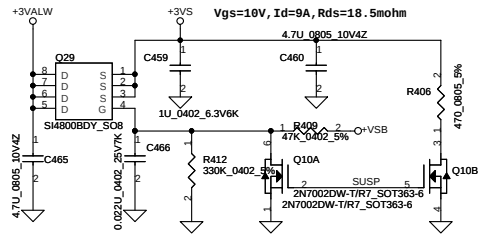
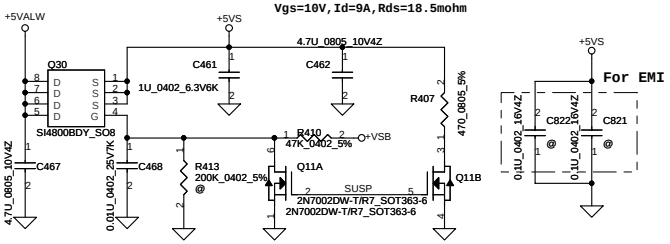
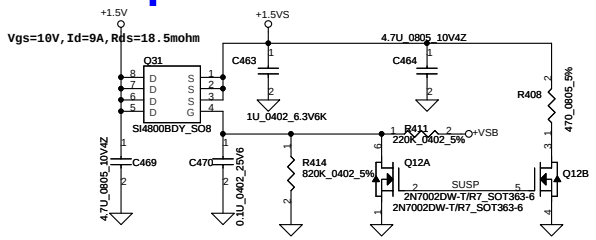
+3VALW TO +3VS



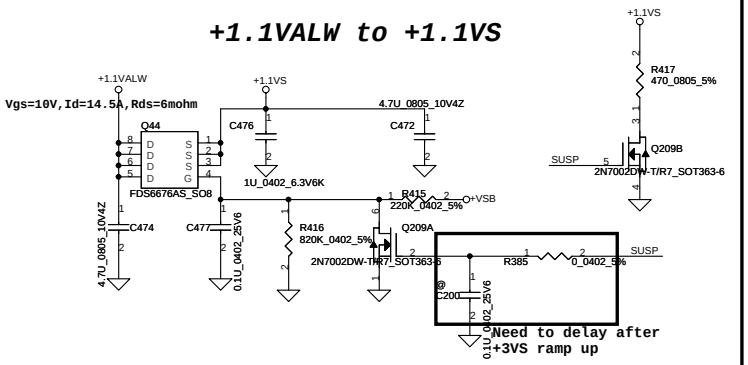
+5VALW TO +5VS

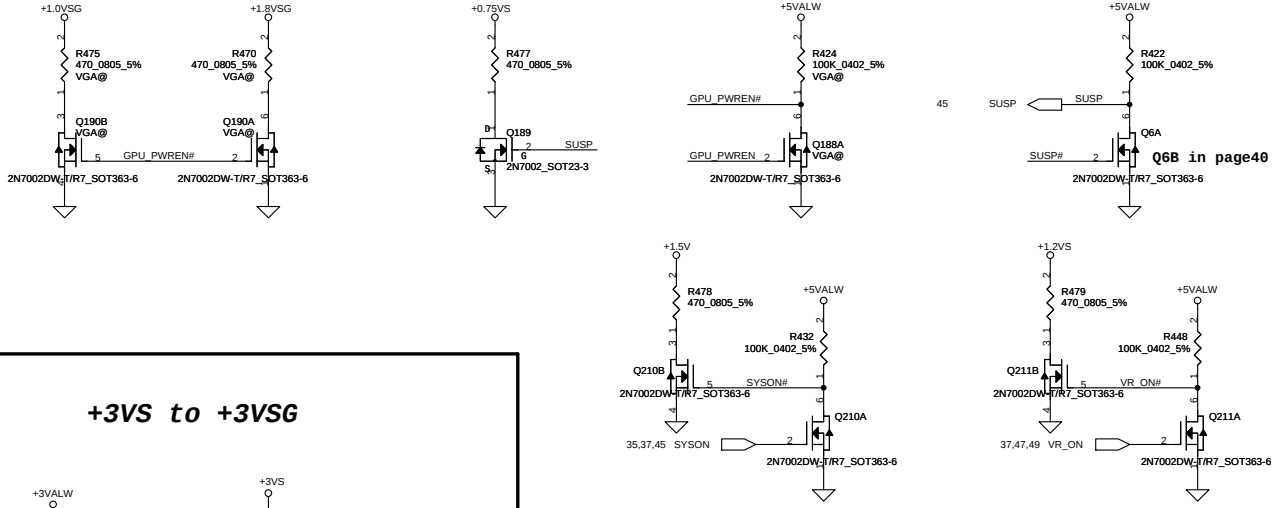


+1.5V TO +1.5VS

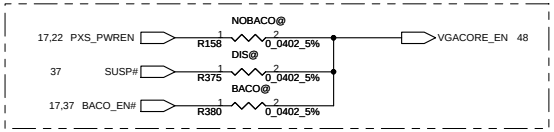


+1.1VALW to +1.1VS

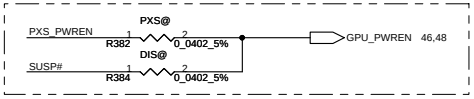




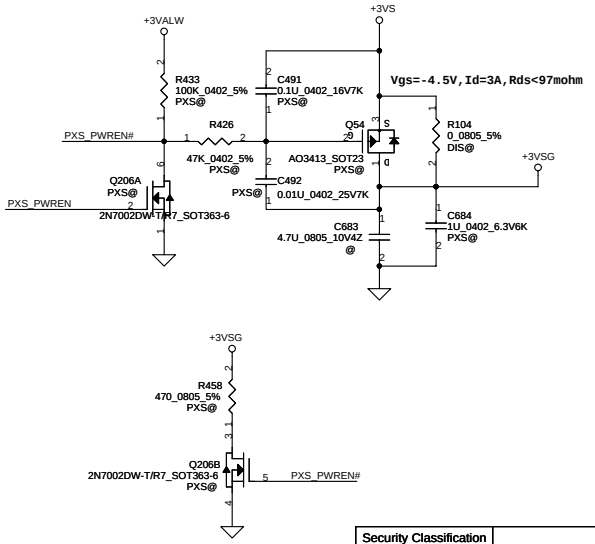
For +VGA_CORE power enable



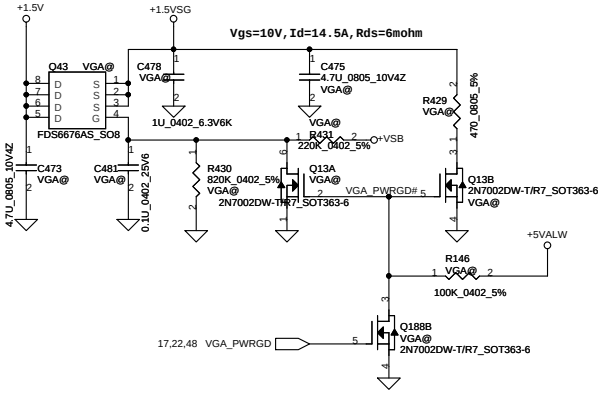
For GPU power enable



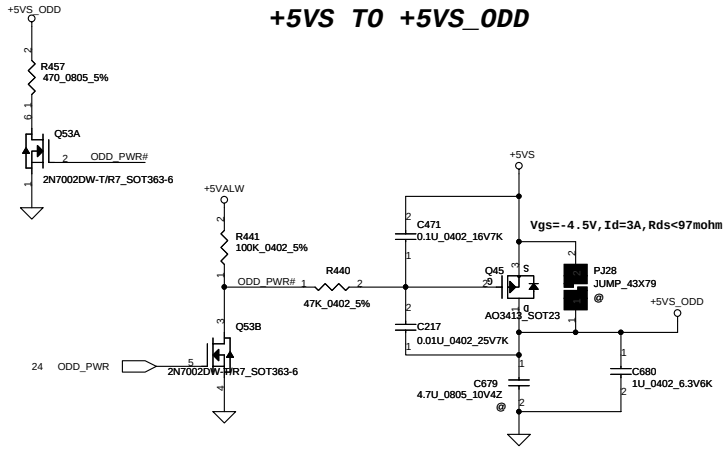
+3VS to +3VSG



+1.5V to +1.5VSG



+5VS TO +5VS_ODD



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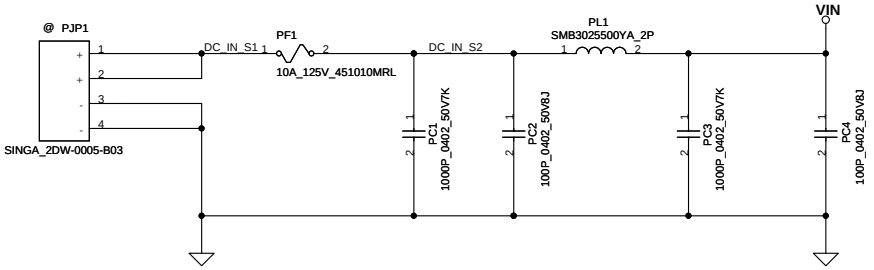
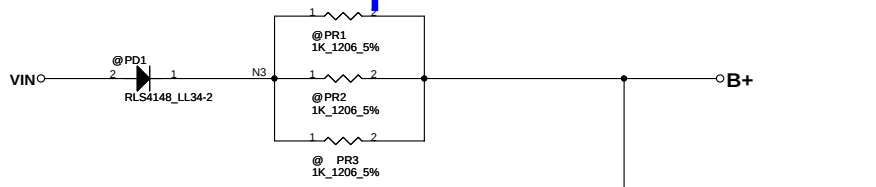
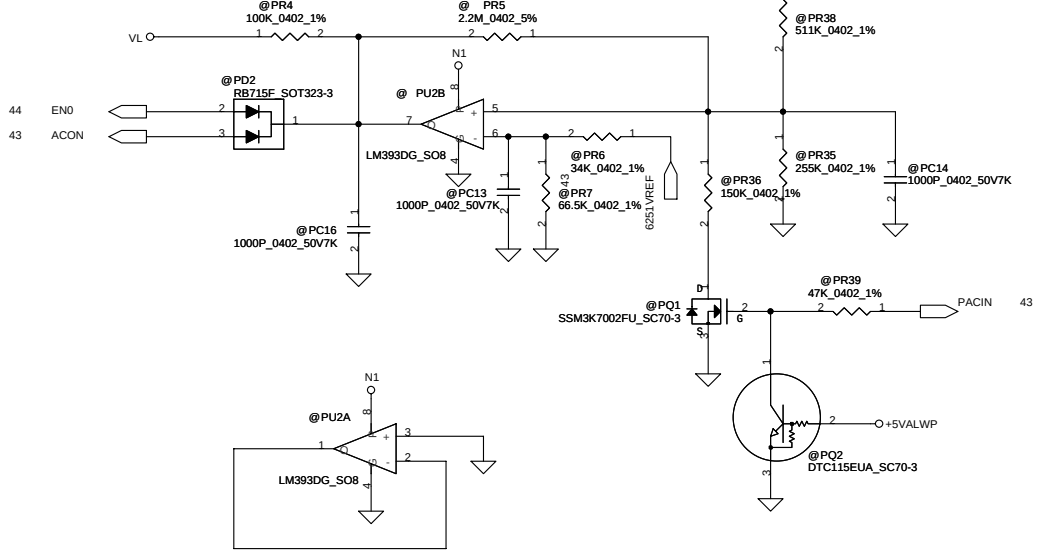
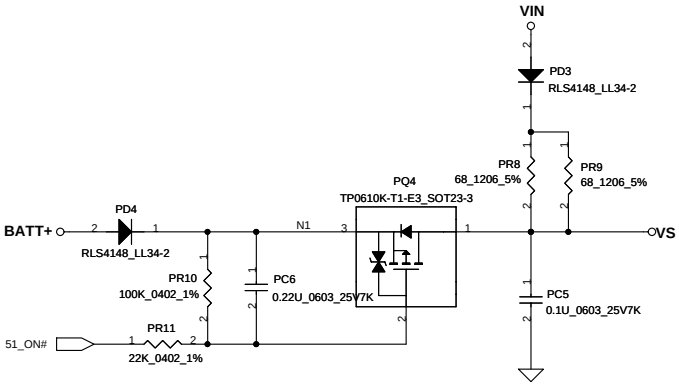
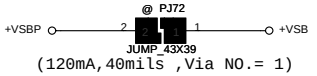




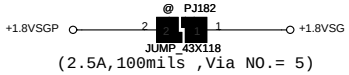




(100mA,40mils ,Via NO.= 2)



(120mA,40mils ,Via NO.= 1)



(2.5A,100mils ,Via NO.= 5)

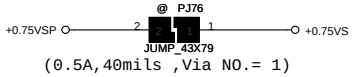
(6.5A,260mils ,Via NO.= 13)
OCP=8.55A

(5A,200mils ,Via NO.= 10)
OCP=7.7A

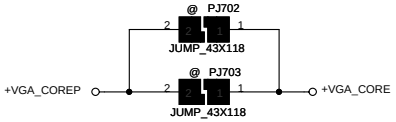
(5A,200mils ,Via NO.= 10)
OCP=7.9A

(5.3A,212mils ,Via NO.= 11)
OCP=6.81A

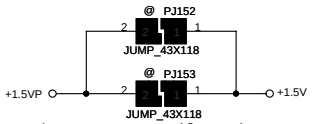
(3A,120mils ,Via NO.= 6)



(0.5A,40mils ,Via NO.= 1)

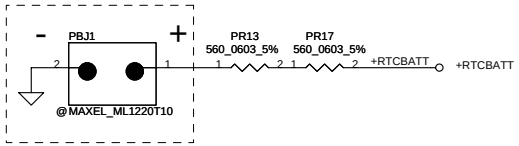


(32.6A,1288mils ,Via NO.= 65)
OCP= 36.19A



(DIS 20A, 800mils ,Via NO.= 40,
OCP=24.13A)
(UMA 8.5A, OCP=10.44A)

RTC Battery



SP093MX0000

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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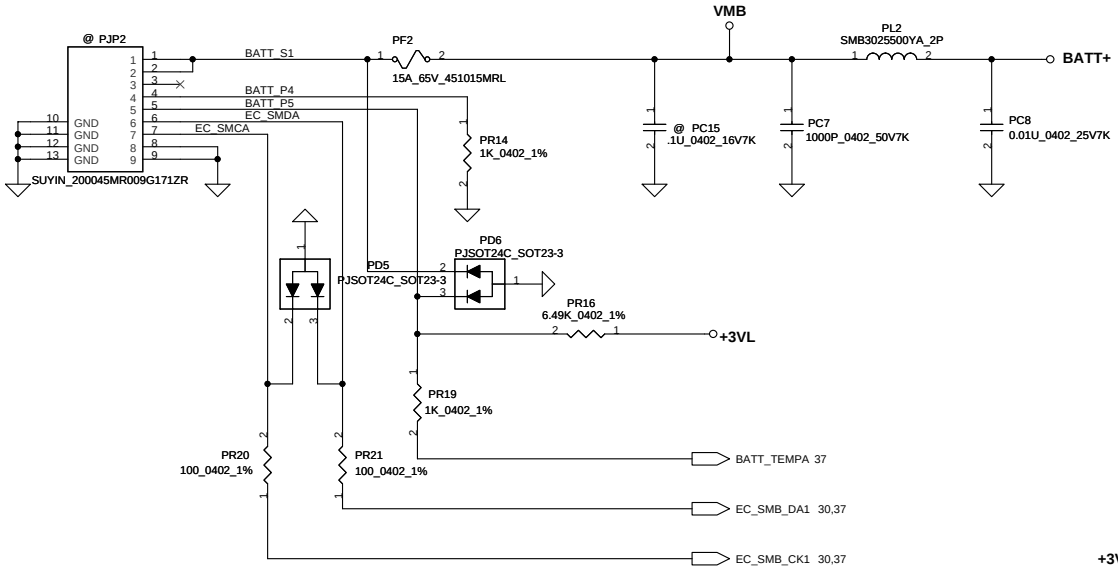
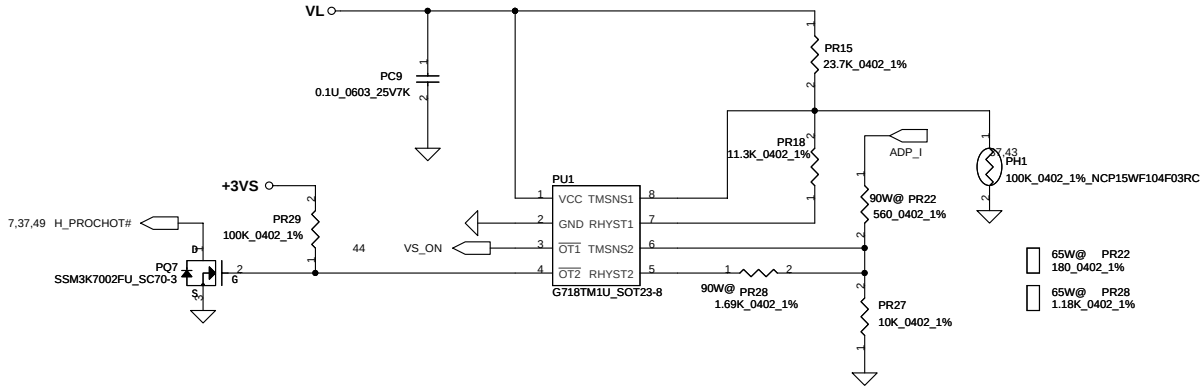
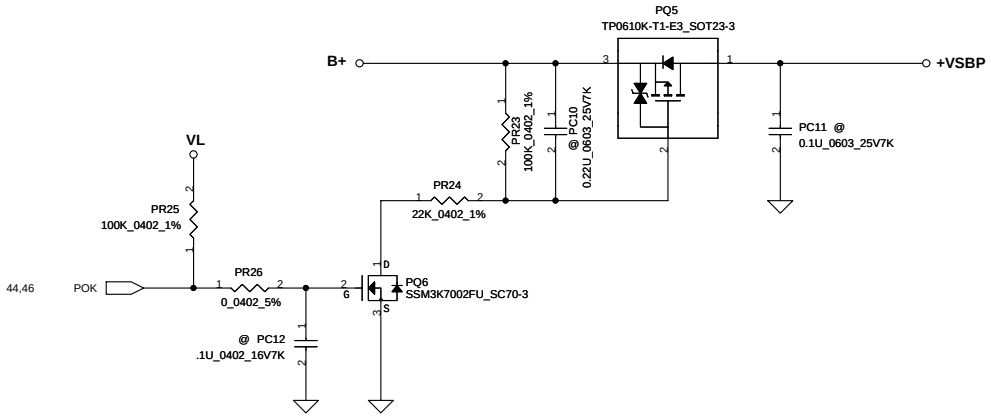


PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
Rset = 3 * 7.87K = 23.61K ==> 23.7K
Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K





Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.5V	62.44W	1.3V

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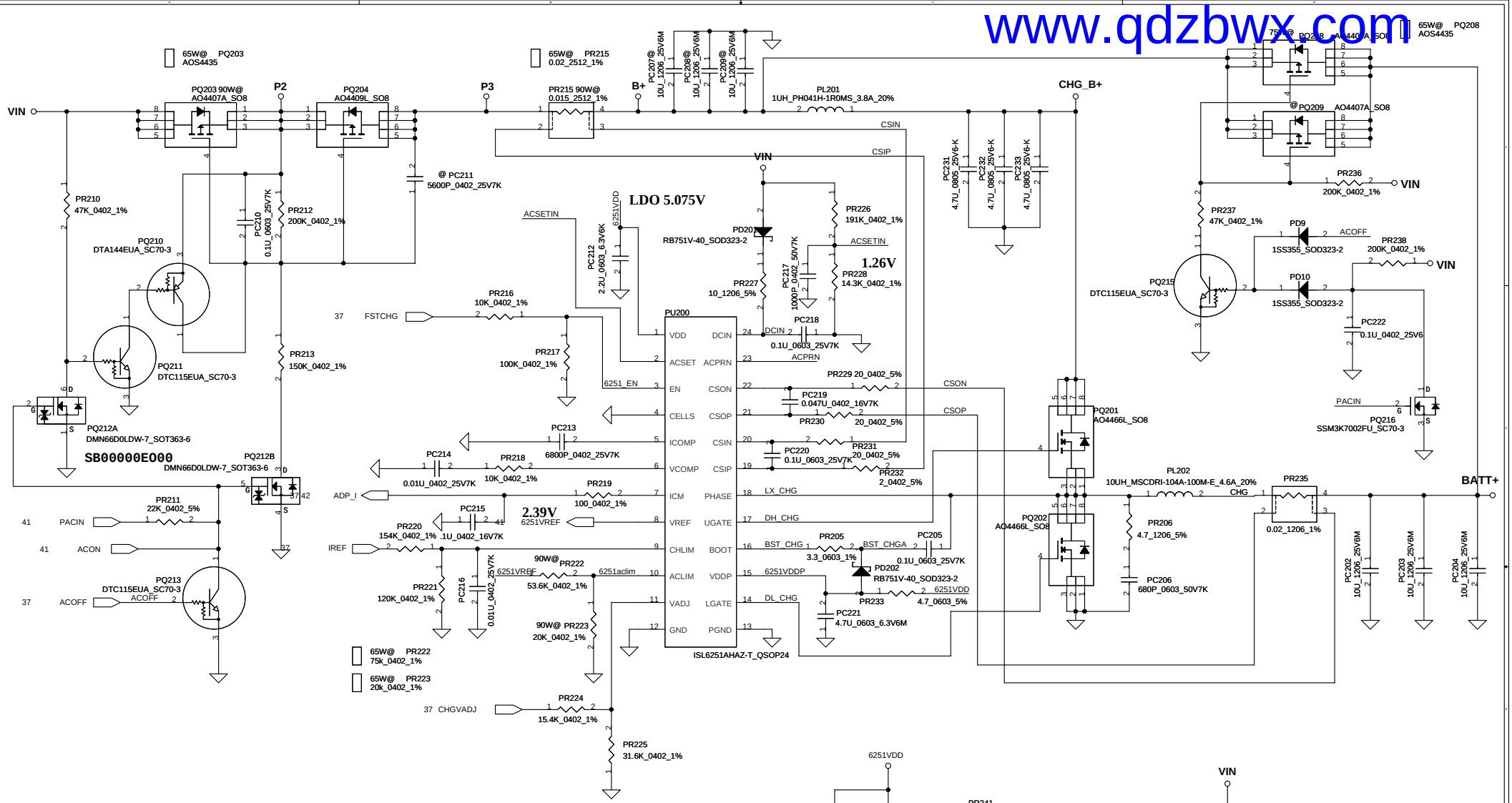

CC=0.25A~3.6A
IREF=0.9133*Icharge
IREF=0.228V~3.288V
VCHLIM need over 88mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

CP mode CP= 92%*Iada

UMA
Iada=0~3.421A(65W) CP=3.147A
Vaclim=0.619V(65W) PR222=75k, PR223=20k, PR215=0.02

DIS
Iada=0~4.74A(90W) CP=4.36A
Vaclim=0.735V(90W) PR222=53.6k, PR223=20k, PR215=0.015

Vin Detector

High	18.089V
Low	17.44V

1.26 / 14.3 * 205.3 = 18.089V

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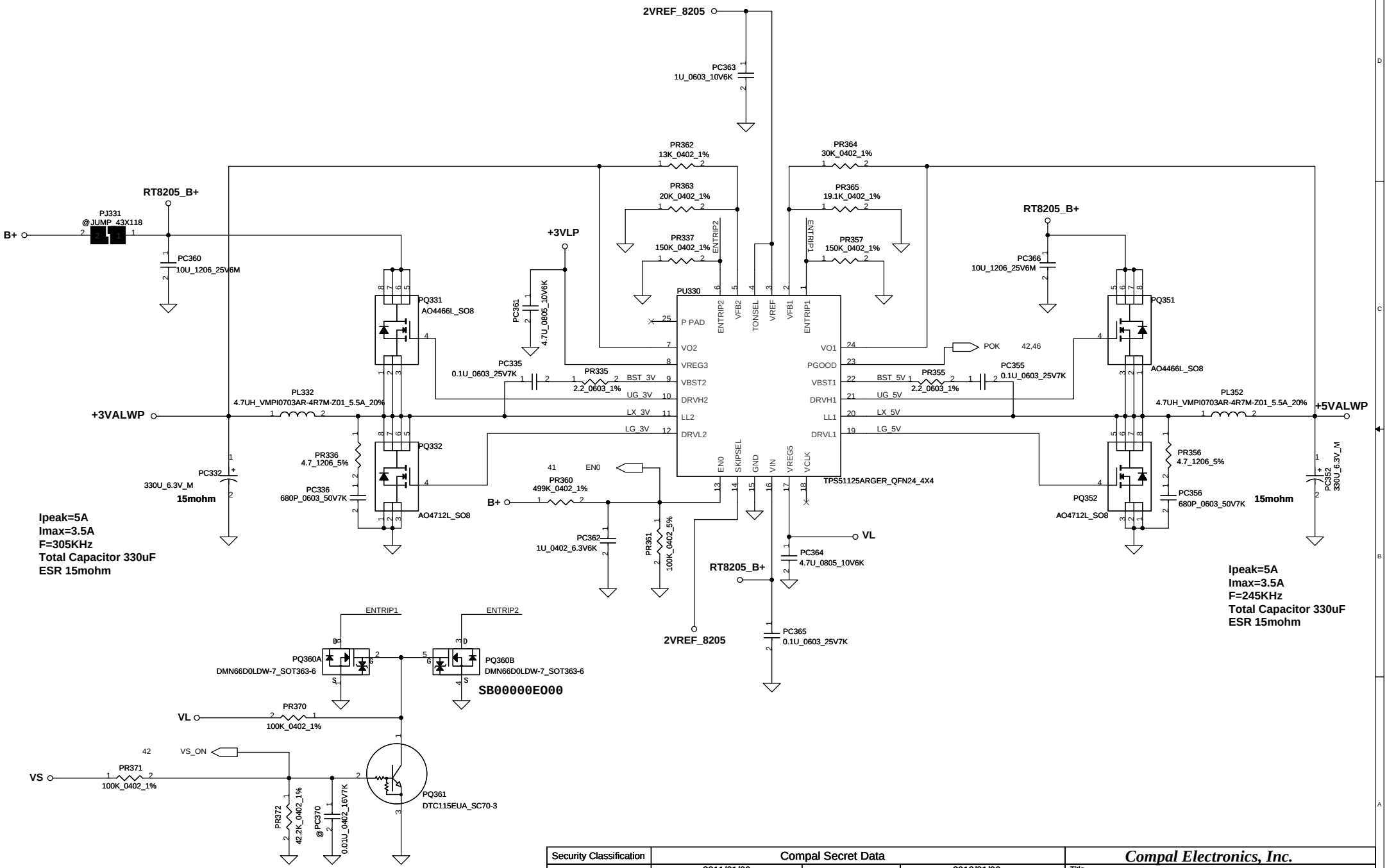

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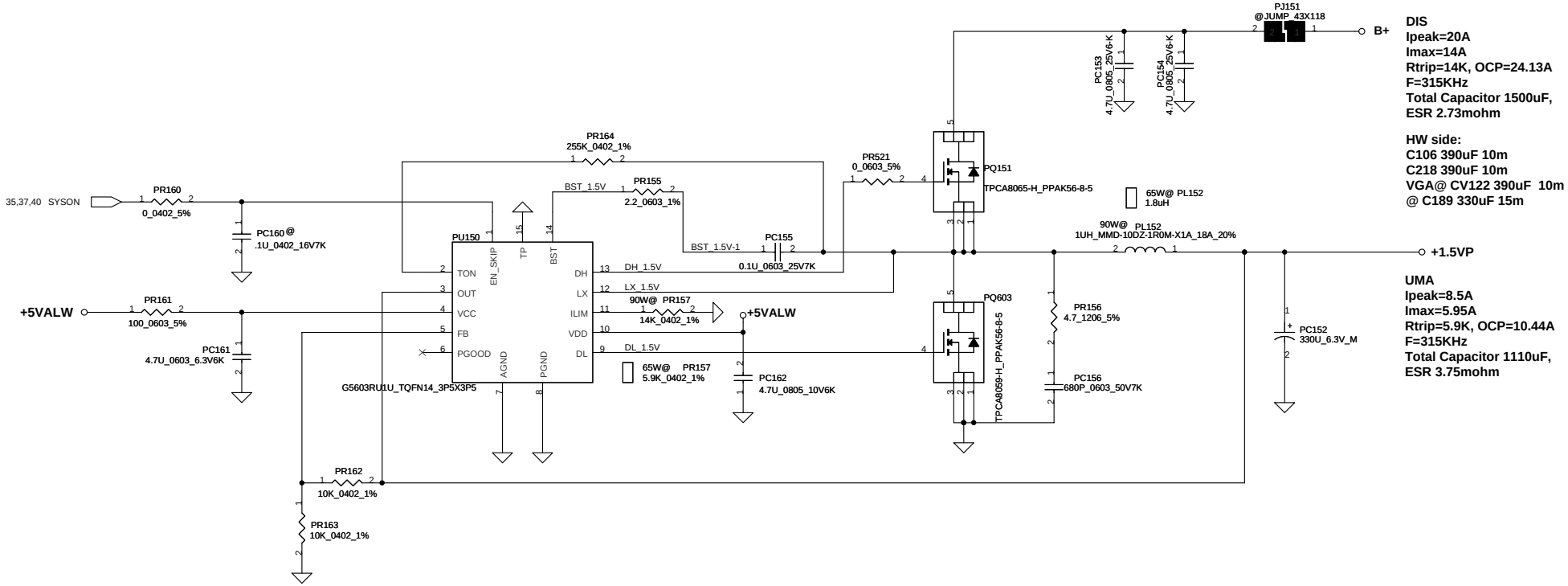

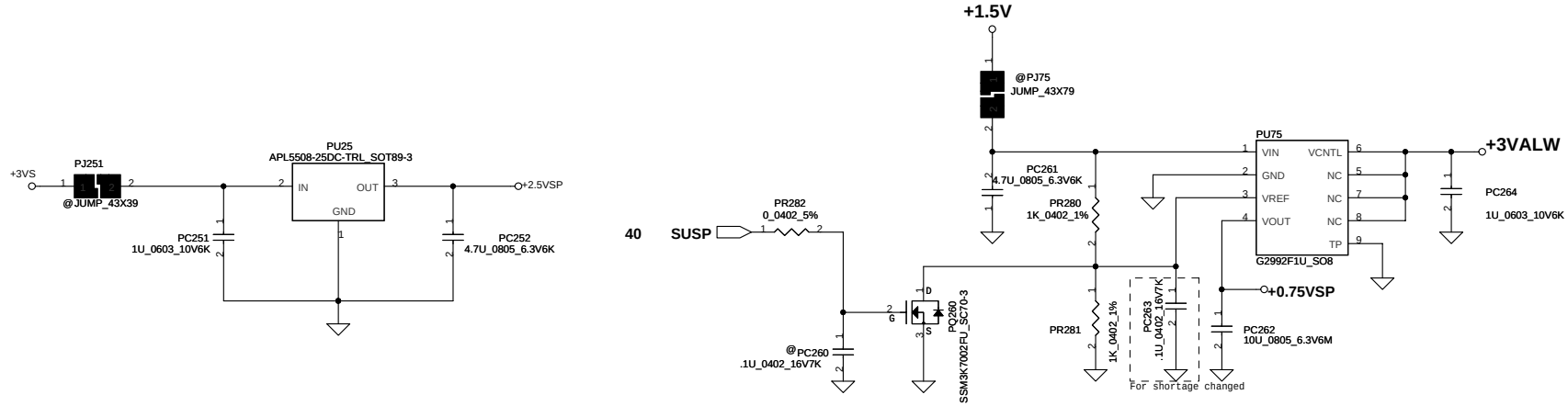

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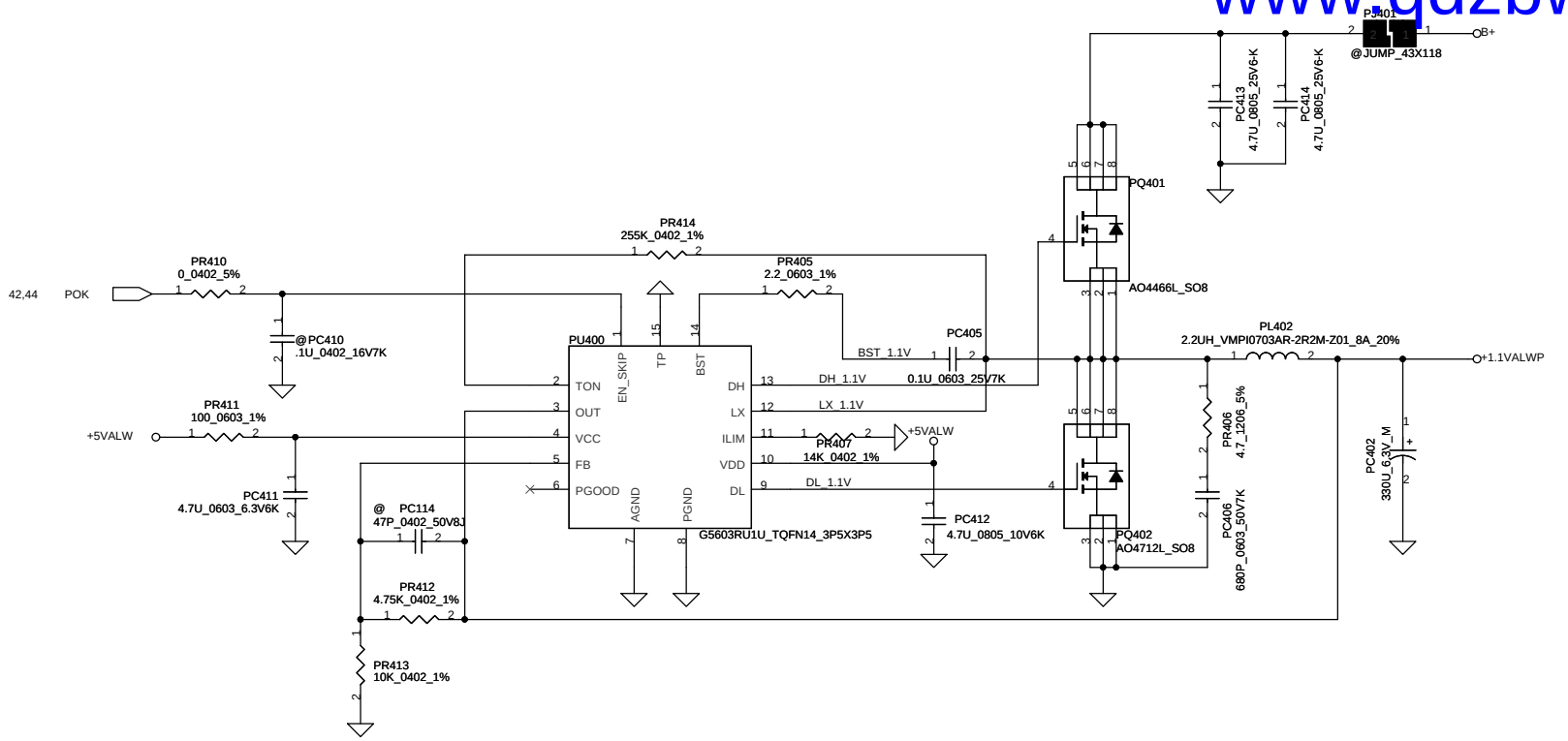
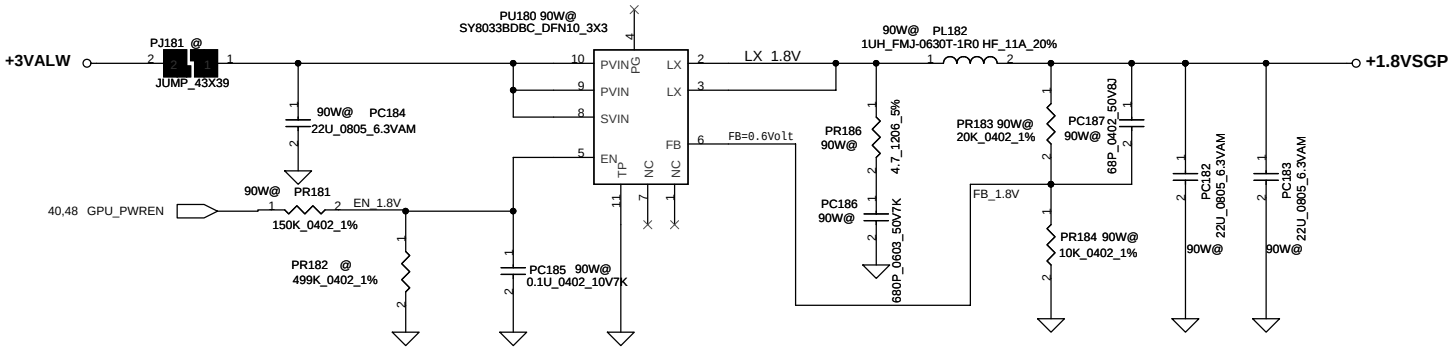


Ipeak=5.3A
Imax=3.71A
Rtrip=14K, OCP=6.64A
F=315KHz
Total Capacitor 330uF,
ESR 15mohm



Ipeak=2.5A
ILIM = 4A
F=1MHz
Total Capacitor 44uF,

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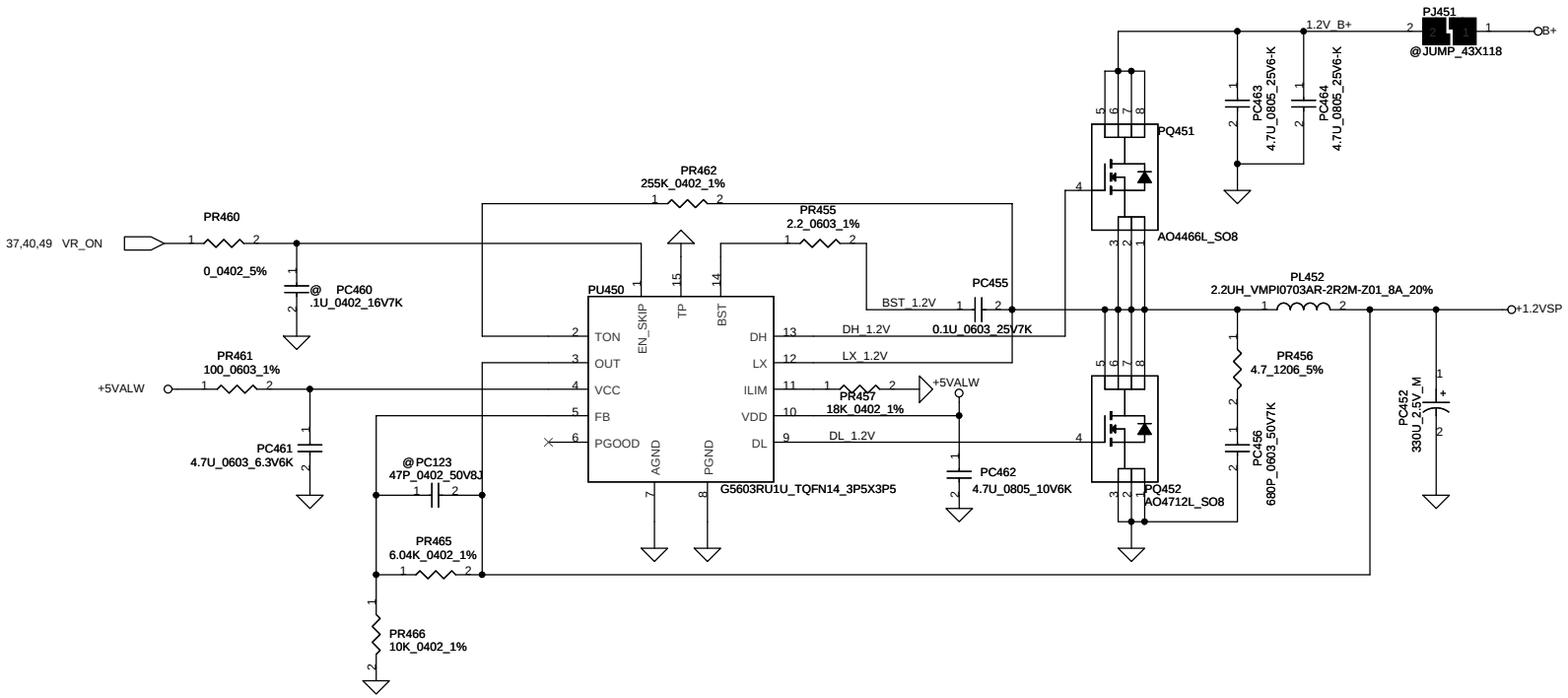

Ipeak=6.5A
Imax=4.55A
Rtrip=18K, OCP=8.37A
F=315KHz
Total Capacitor 720uF,
ESR 6mohm

HW side:
C130 390uF 10m

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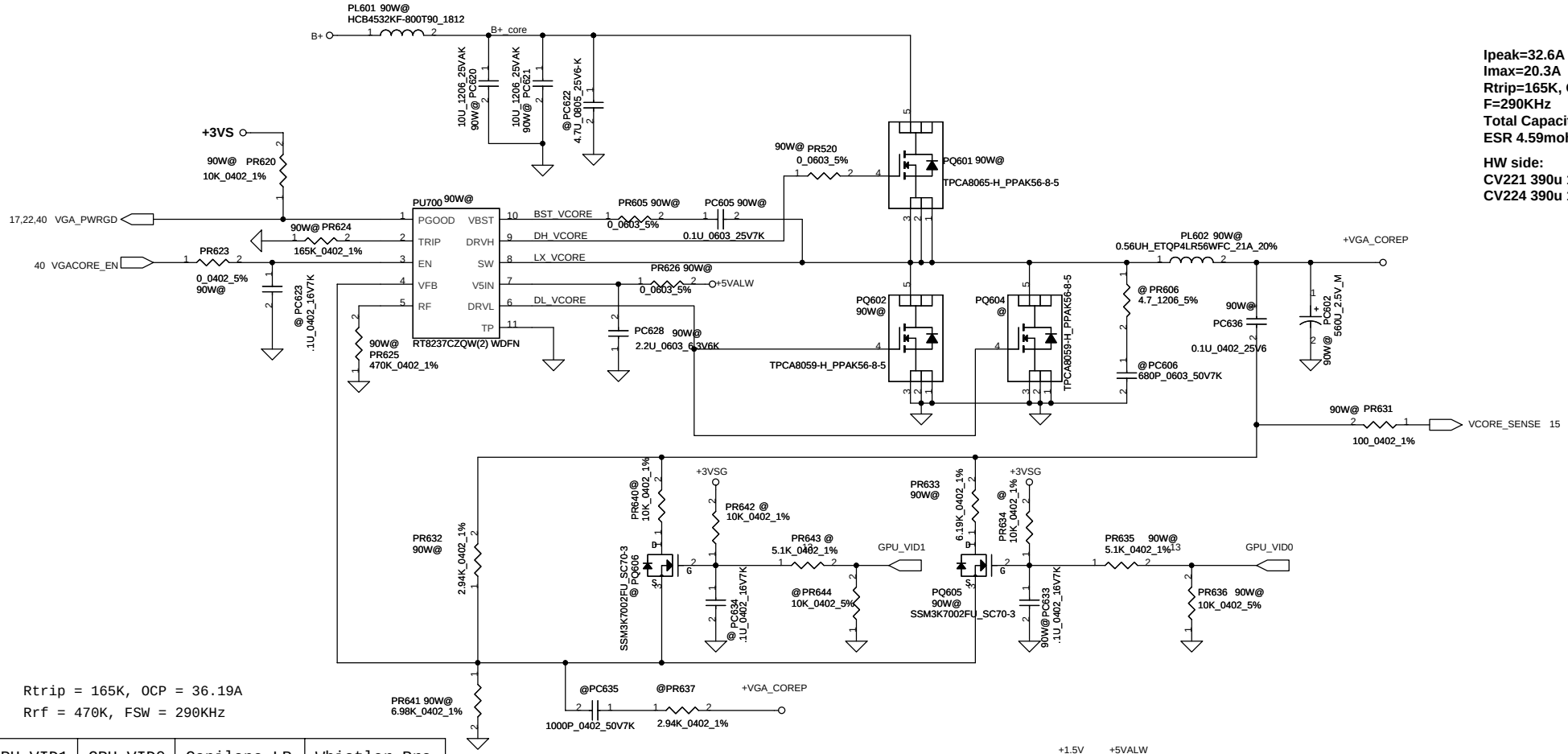
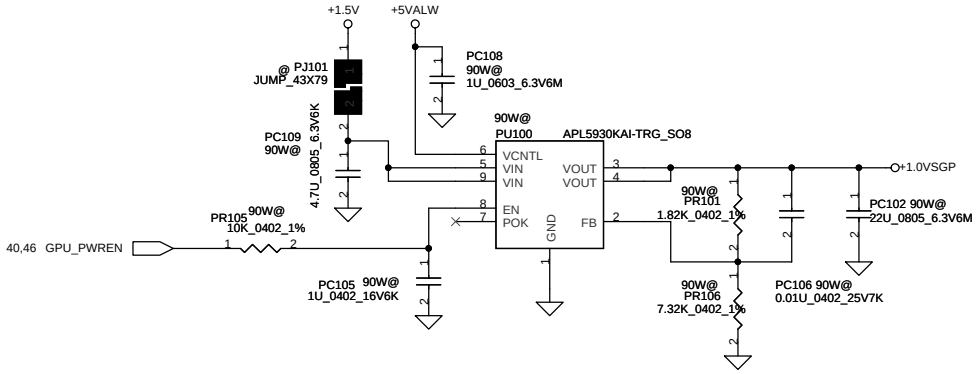


Ipeak=32.6A
Imax=20.3A
Rtrip=165K, OCP=36.19A
F=290KHz
Total Capacitor 1220uF,
ESR 4.59mohm

HW side:
CV221 390u 17m
CV224 390u 17m

Rtrip = 165K, OCP = 36.19A
Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Capilano LP	Whistler Pro
X	L	1	1
X	H	0.9	0.9
H	L		
H	H		



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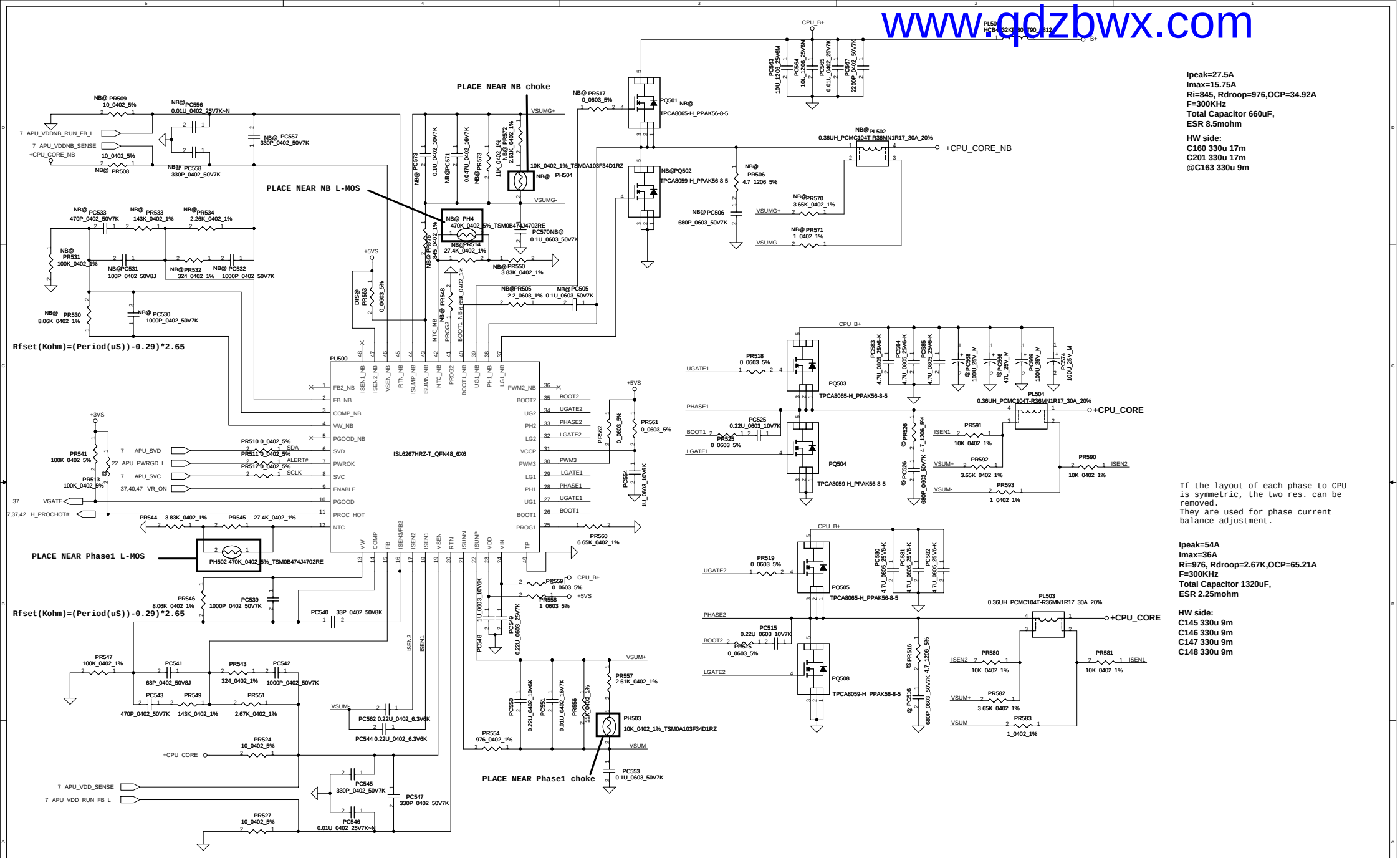

Ipeak=27.5A
Imax=15.75A
Ri=845, Rdroop=976,OCP=34.92A
F=300KHz
Total Capacitor 660uF,
ESR 8.5mohm

HW side:
C160 330u 17m
C201 330u 17m
@C163 330u 9m

If the layout of each phase to CPU is symmetric, the two res. can be removed.
They are used for phase current balance adjustment.

Ipeak=54A
Imax=36A
Ri=976, Rdroop=2.67K,OCP=65.21A
F=300KHz
Total Capacitor 1320uF,
ESR 2.25mohm

HW side:
C145 330u 9m
C146 330u 9m
C147 330u 9m
C148 330u 9m

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2011/03/30	42	Change PR22 to 180Ω,PR28 to 1.18KΩ	For 65W SKU
			Change PR22 to 523Ω,PR28 to 3KΩ	For 90W SKU
		43	Change PC217 to SE074102K80,PR236 to 200KΩ,PR237 to 47KΩ PR205 to 3.3Ω,PR235 to SD00000S120,Add PR206,PC206, Delete PC211	Circuit modify
			Change PR222 to 53.6KΩ,PR223 to 20KΩ,Delate PQ209	For 90W SKU
			Change PR222 to 75KΩ	For 65W SKU
		44	Change PR335,PR355 to 2.2Ω,PC332,PC352 to SF000002080 ,PL332,PL352 to SH00000KN00,Add PR336,PR356,PC336,PC356	Circuit modify
		45	Change PR155 to 2.2Ω,PC152 to SF000002080, Add PR156,PC156,PR521,Delete PC260	Circuit modify
			Change PR157 to 5.9KΩ,PL152 to SH00000IP00	For 90W SKU
			Change PR157 to 14KΩ,PL152 to SH00000CN00	For 65W SKU
		46	Change PR405 to 2.2Ω,PC402 to SF000002080,Add PR406,PC406 Change PR407 to 14KΩ,PL402 to 2.2UH 7*7	Circuit modify
		47	Change PR455 to 2.2Ω,PR457 to 18KΩ,PL452 to 2.2UH 7*7 Add PR456,PC456	Circuit modify
		48	Change PR624 to 165KΩ,PR631 to 100Ω,Delete PR630, Add PC636,PR520	Circuit modify
		49	Change PR505 to 2.2Ω,PR560 to 6.65KΩ,PR551 to 2.67KΩ Change PH503,PH504 to SL200000W00,PC569,PC574 to SF000003W00 Add PC506,PR506,PR517,PR518,PR519	Circuit modify

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HW PIR (Product Improve Record)

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QHRAE LA-7213P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

Item	Date	Page	Solution	Request
1.	3/17	P23	Remove level-shifter for ODD_PLUGIN#	ODD has internal 1K pull-down
2.	3/17	P34	Add level-shifter for CR_CPPE#	For leakage issue
3.	3/17	P23	Change HDMI_HPD to GEVENT10# and reserve GEVENT19#	GEVENT9# has issue
4.	3/17	P24	Change LOGO_LED to GPIO176 and WL_BT_LED to GPIO177	For LED flash issue after power-on
5.	3/24	P10	Add C295,C316,C324,C325	For EMI test
6.	3/28	P39	Reserve C20,C21,C229,C231~C236,C247,C251	For ESD test)
7.	3/29	P38	Change LPC debug port to 16pins connector	To support new debug card
8.	3/30	P07	Add R70,R102,R105	Pull-down for unused HPD port

REVISION CHANGE: 0.2 TO 1.0

Item	Date	Page	Solution	Request
1.	4/15	P31	Reserve D24, D25	
2.	4/27	P22	Change R257 form 100k to 10k for leakage issue.	
3.	4/27	P37	Add BACO_EN# to EC	To inform EC GPU thermal sensor status

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