Model Name : VIUS1
File Name : LA-9611P
BOM P/N:

Compal Confidential

M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

GPU AMD

2012-02-18

REV:0.4

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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Title: Cover Sheet

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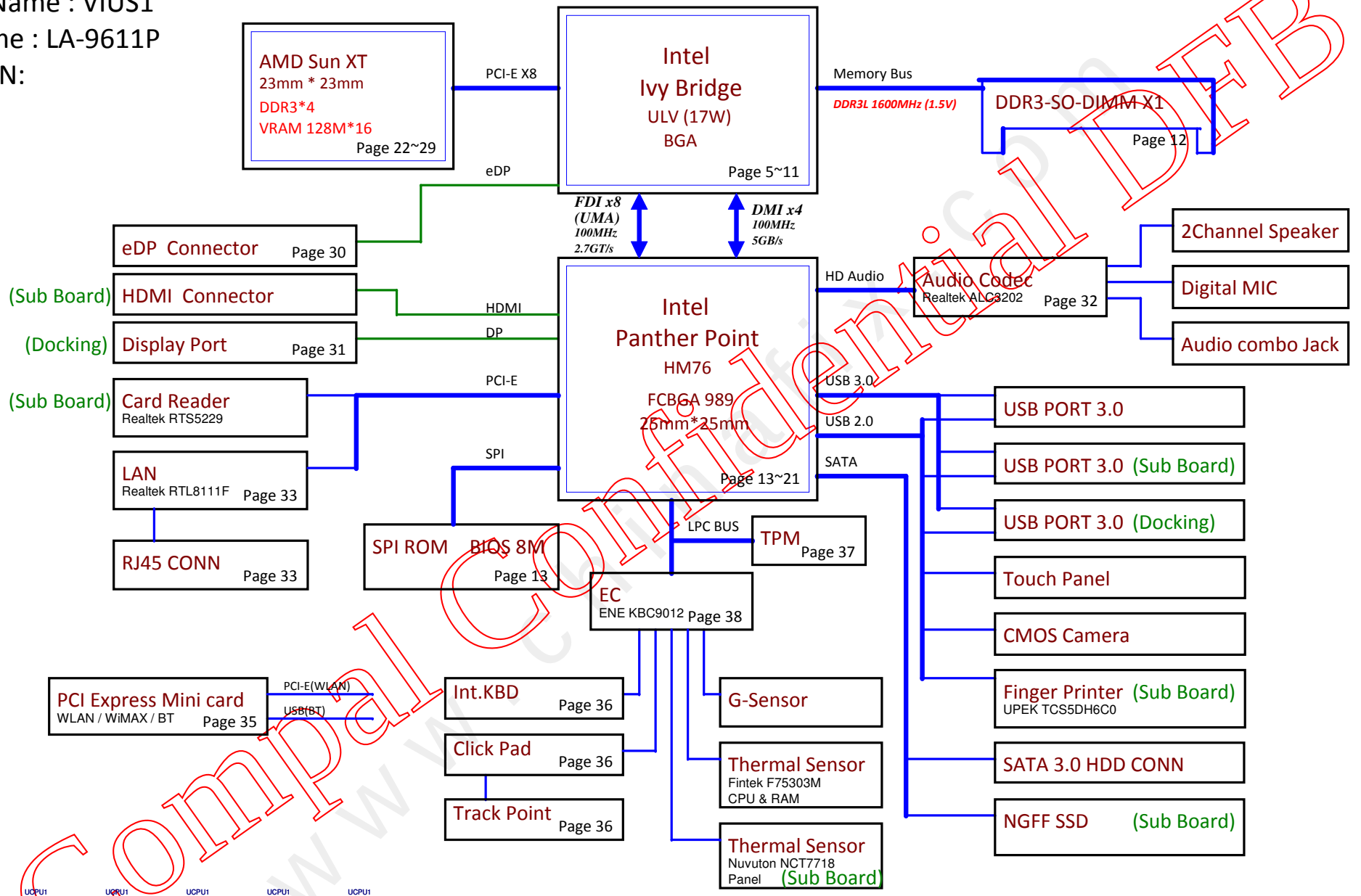
File Name : LA-9611P
BOM P/N:



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Title: Block Diagram

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	~~+3VM~~ ~~+1.05VM~~ (SBA Only)
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB 3.0 Port (I/O Board)
		1	USB 3.0 Port (MB)
	UHCI1	2	USB 3.0 Port (Docking)
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Touch Panel
		9	(Test point)
	UHCI5	10	Mini Card (WLAN/BT)
		11	FPR
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
Unprop	@
AMD	DIS@
Intel UMA	UMA@
VRAM Option	X76@
TPM	TPM@
AOAC	AOAC@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

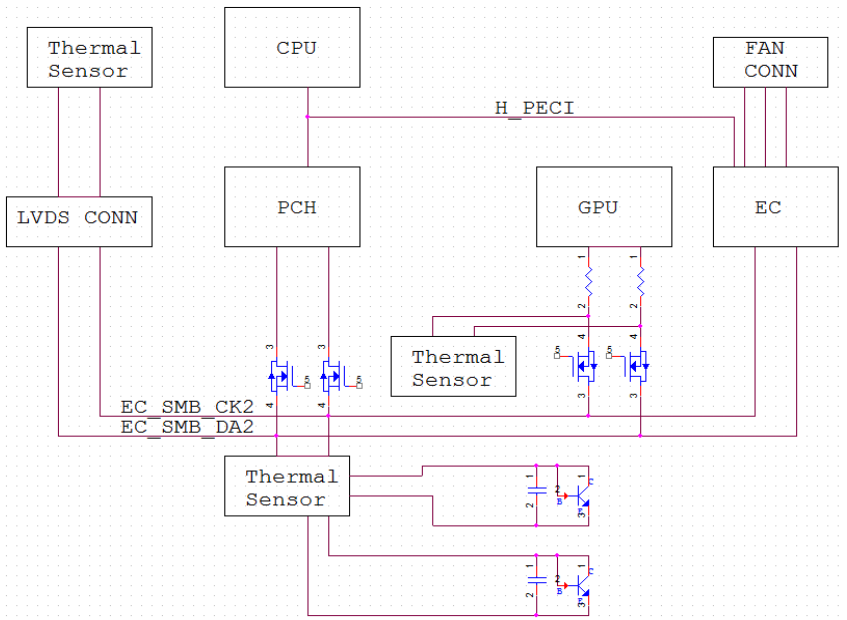
Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X



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Title: Notes List

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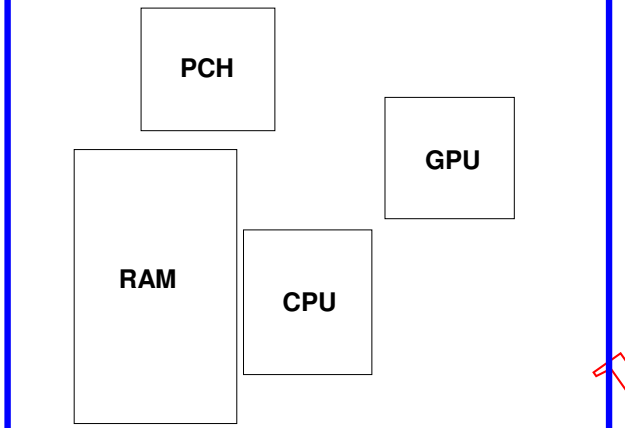
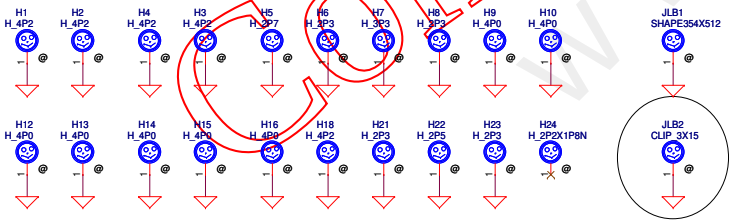
MB Bottom view





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Title: Screw Hole

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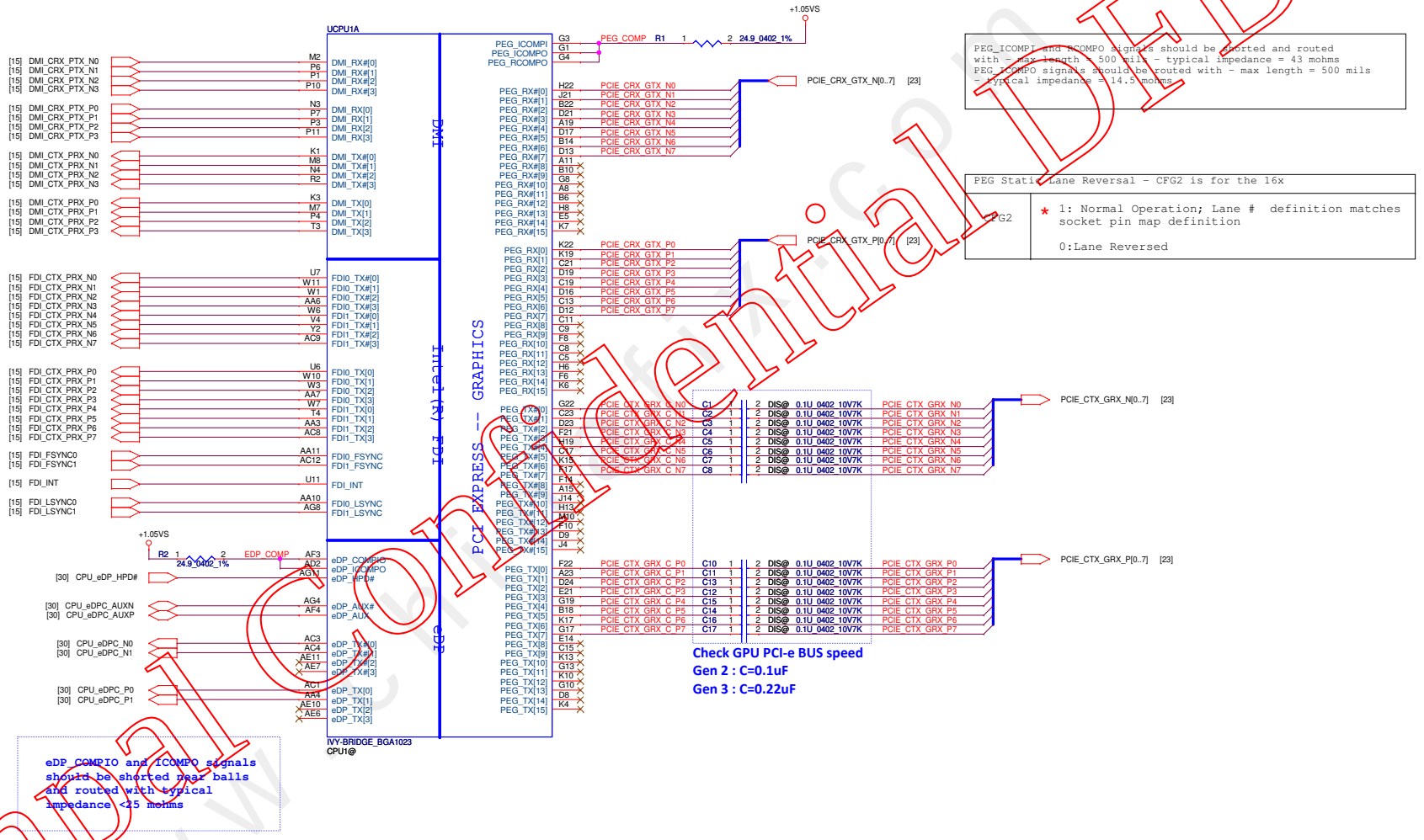

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Compal Electronics, Inc.			
Title: PROCESSOR(1/7) DMI,FDI,PEG			
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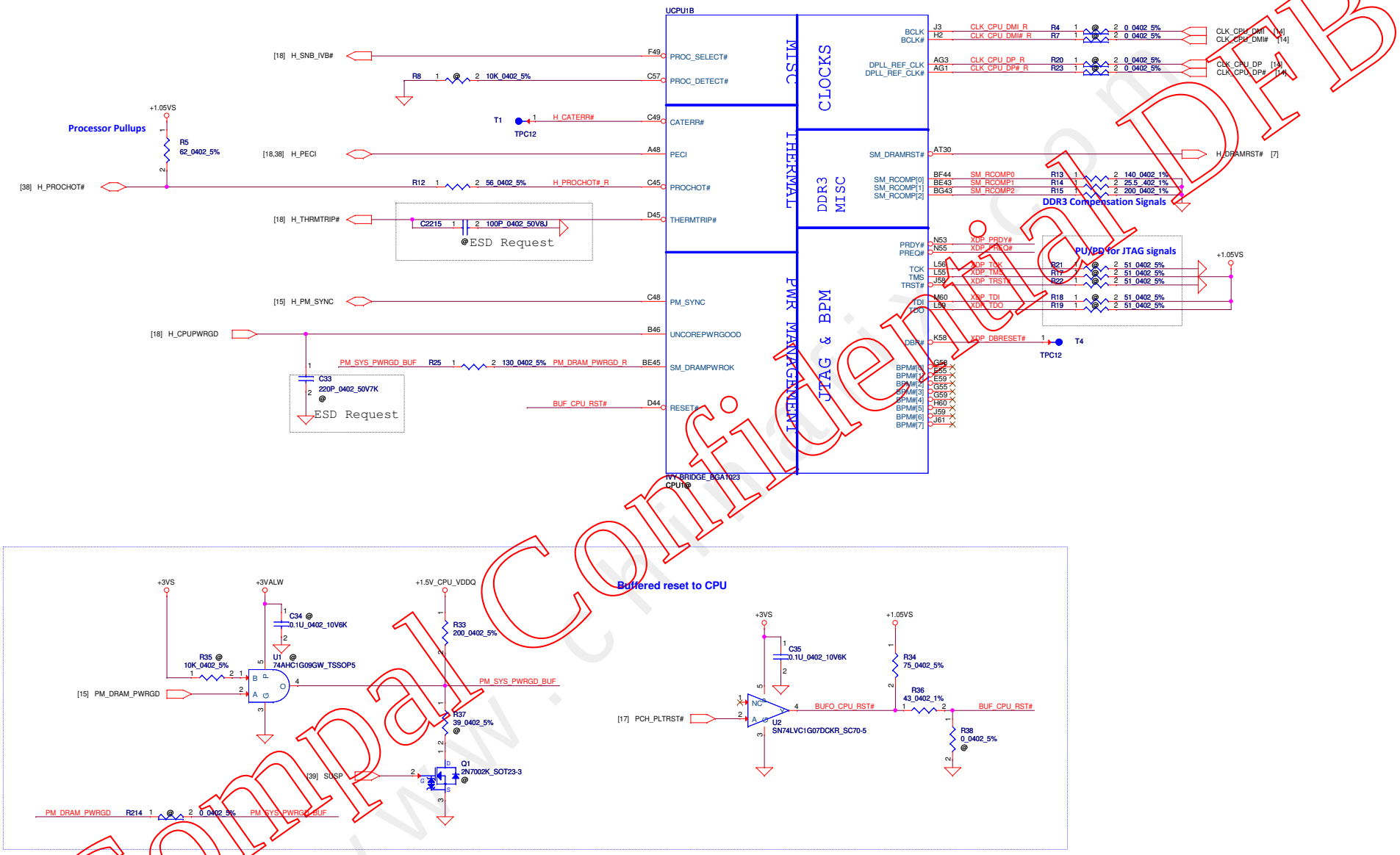

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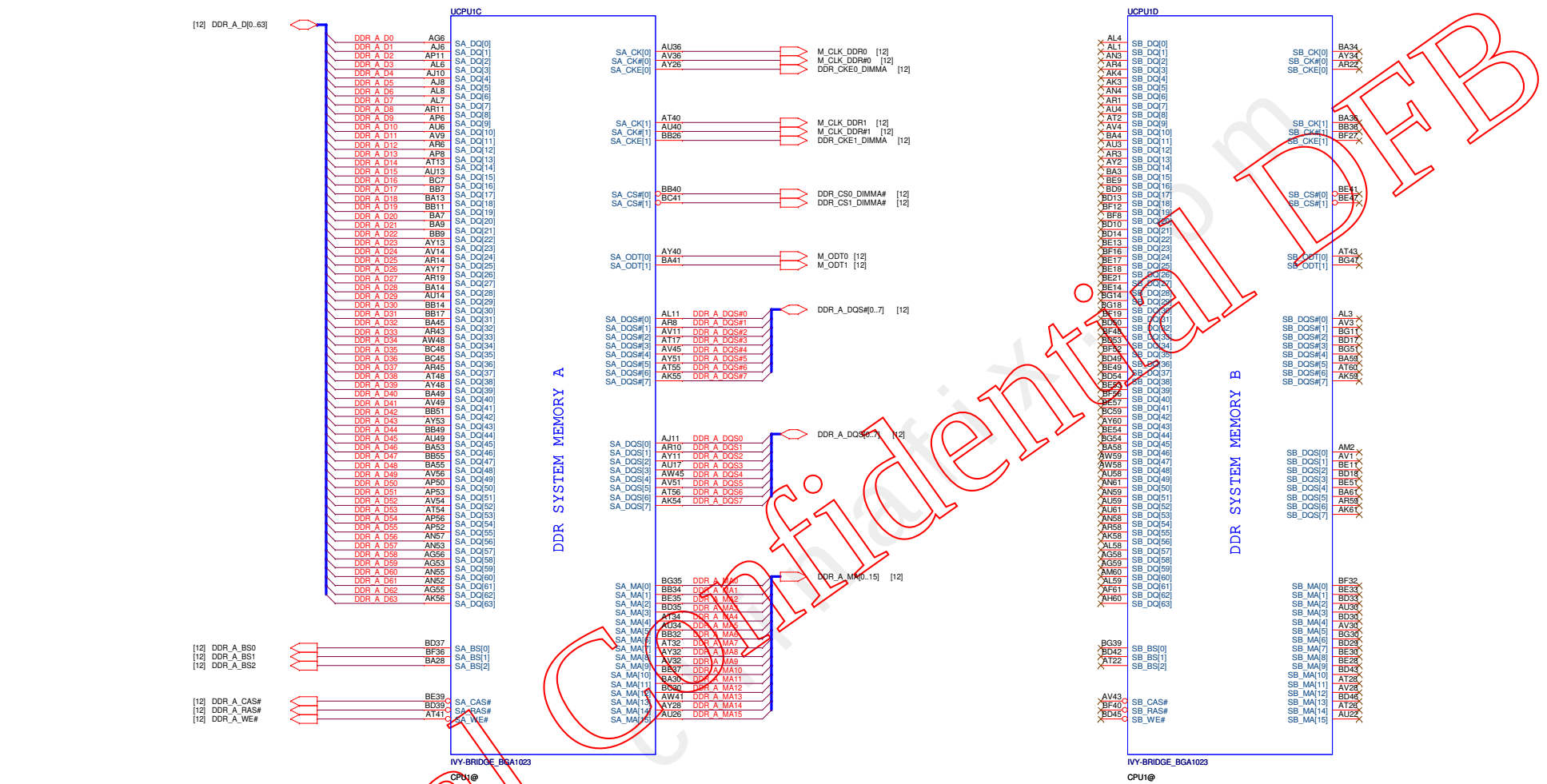
Issued Date	2011/07/12	Deciphered Date	2012/07/01

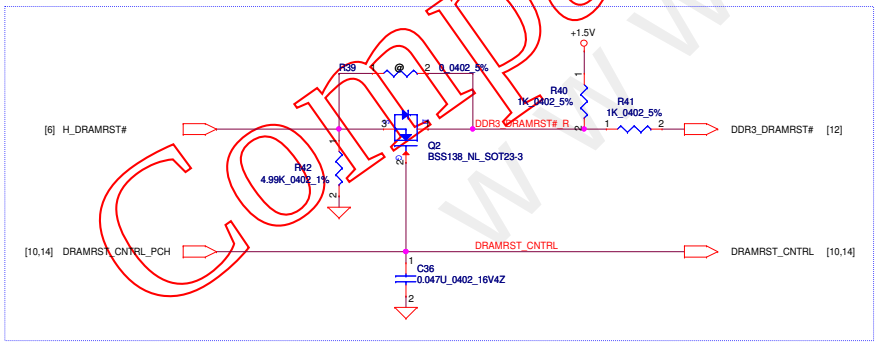
Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: LA-9611P | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 6 of 53





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

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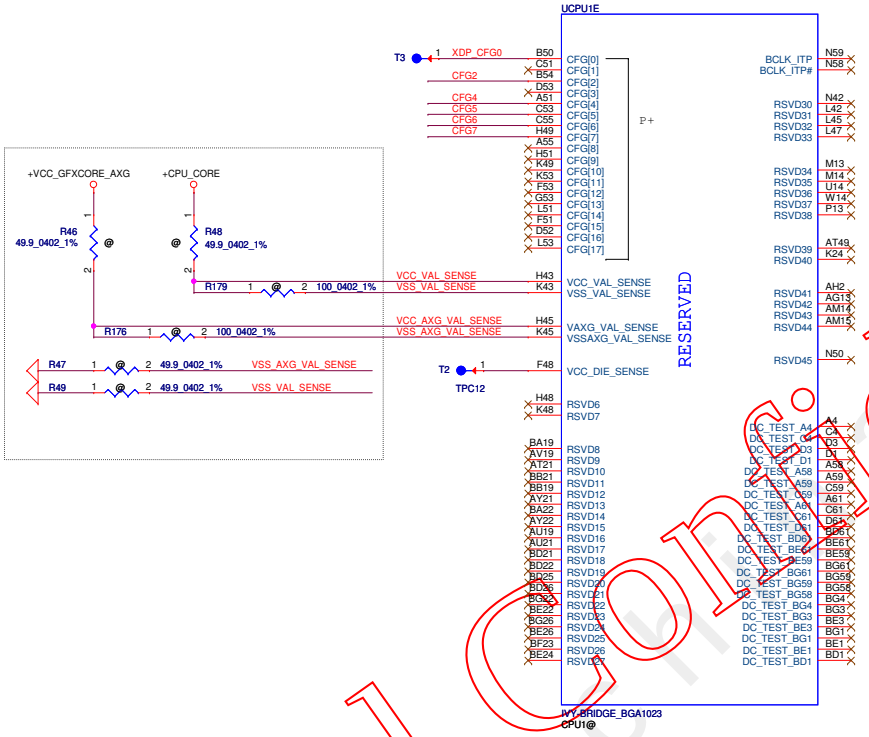
Date: Tuesday, February 26, 2013 | Sheet 7 of 53



CFG Straps for Processor

CFG2

R45 1K_0402_1% @

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4

R50 1K_0402_1%

Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG5
CFG6

R52 @ 1K_0402_1%
R51 1K_0402_1%

PCIE Port Bifurcation Straps

CFG[6:5]	– 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved * – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express*

CFG7

@ R53 1K_0402_1%

PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

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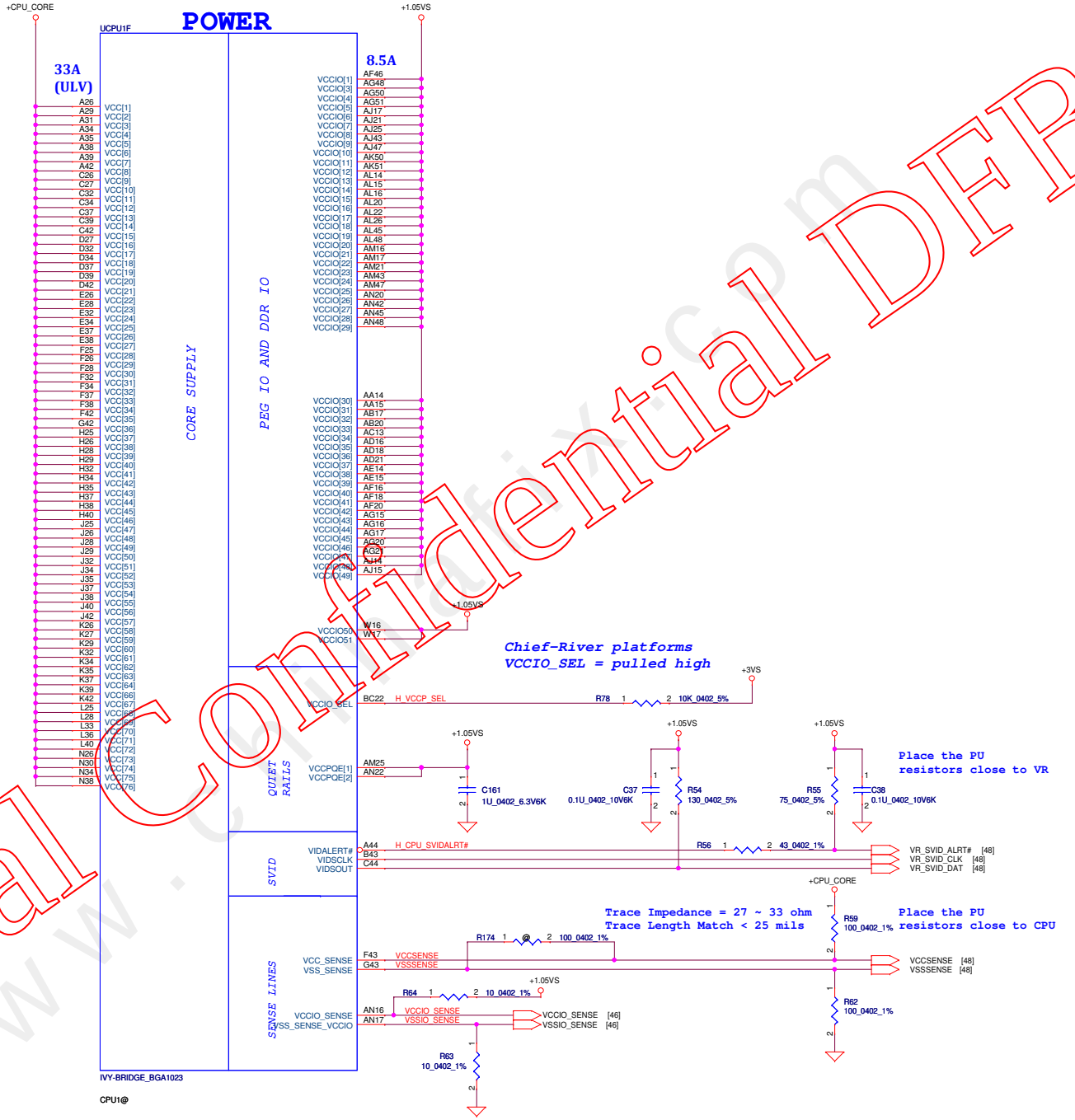
Date: Tuesday, February 26, 2013 | Sheet 8 of 53



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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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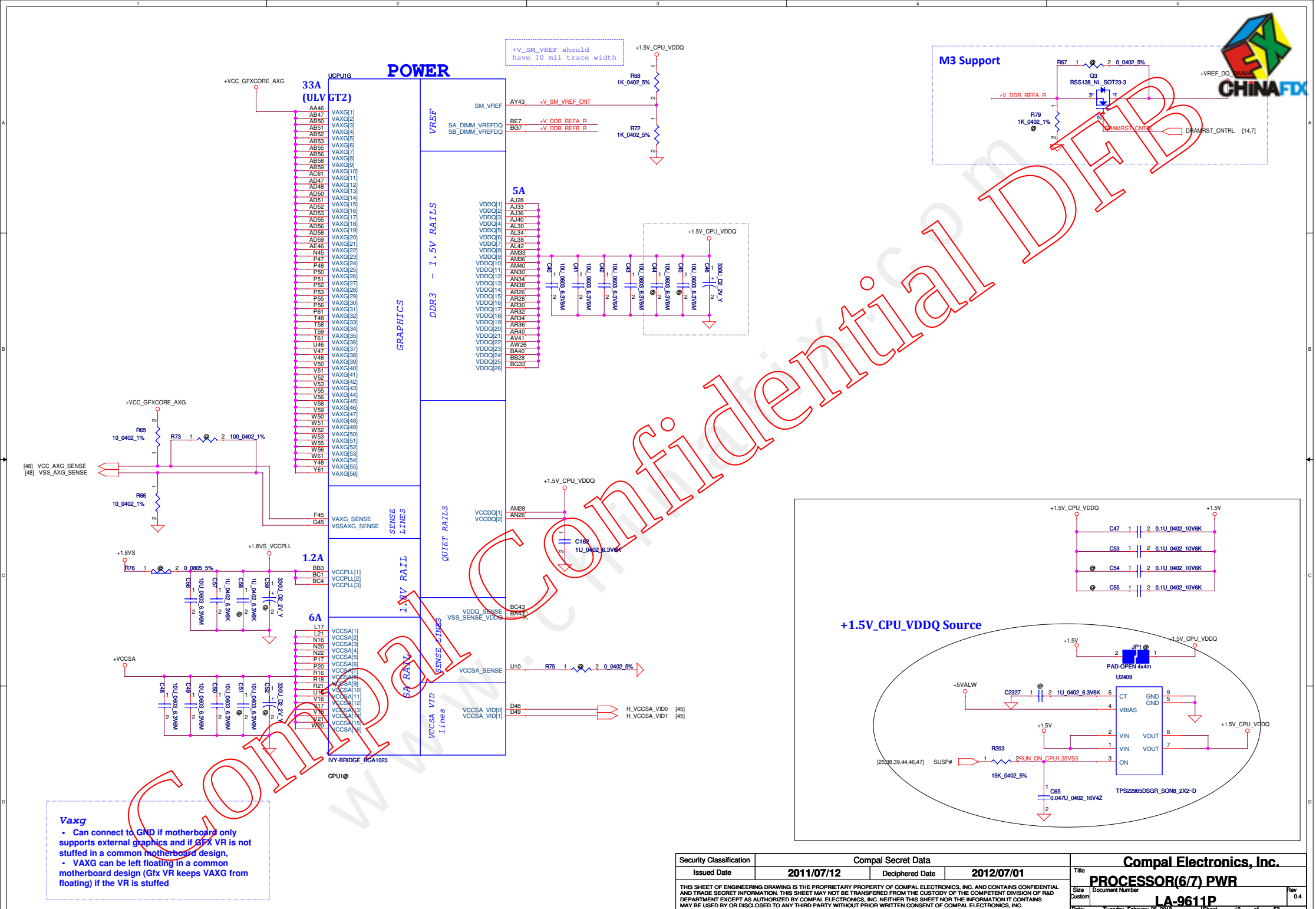
POWER



M3 Support

+1.5V_CPU_VDDQ Source

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	PROCESSOR(6/7) PWR		
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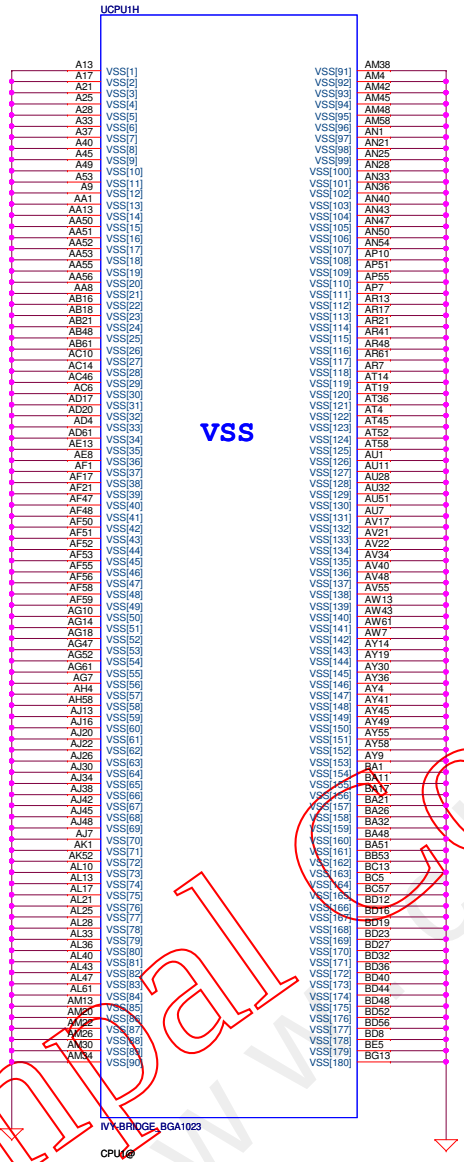
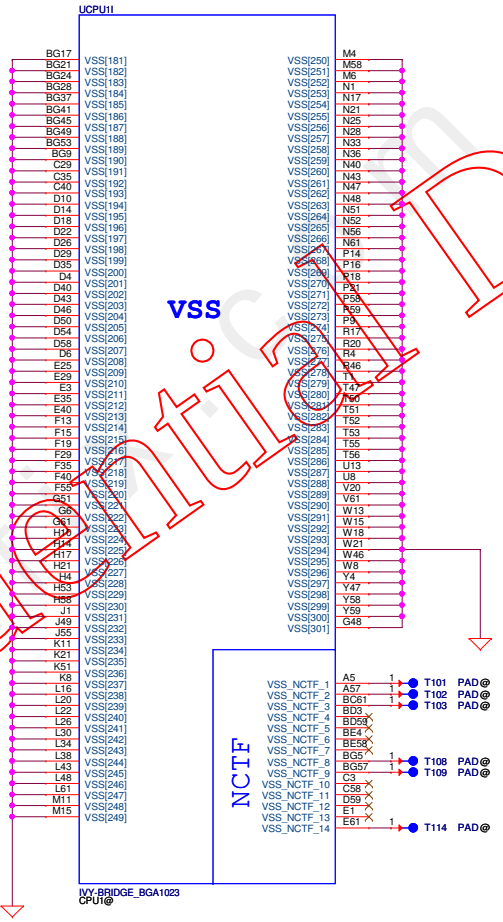
Date: Tuesday, February 26, 2013	Sheet 10 of 53		





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

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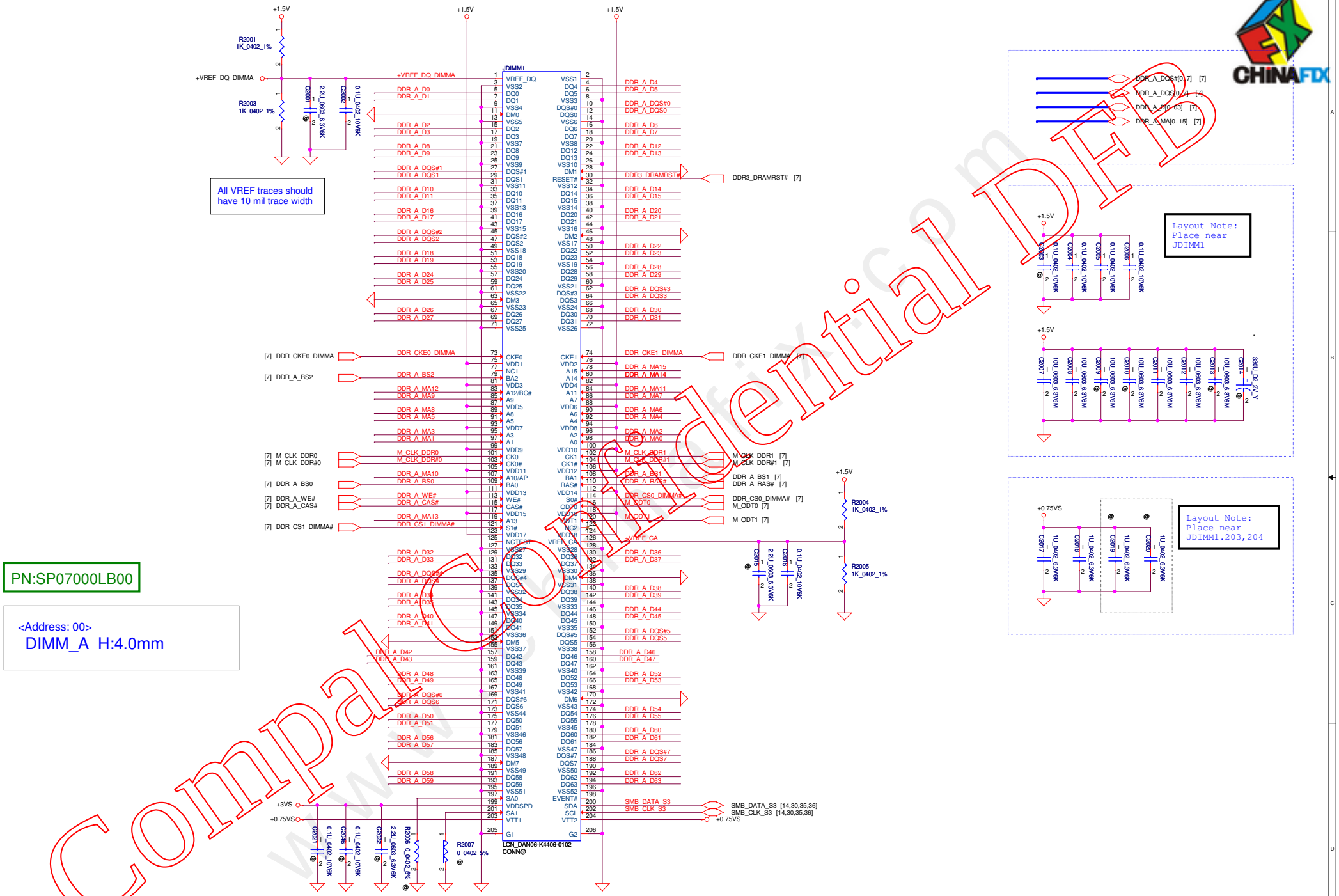
Date: Tuesday, February 26, 2013 | Sheet 11 of 53



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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: DDRIII DIMMA

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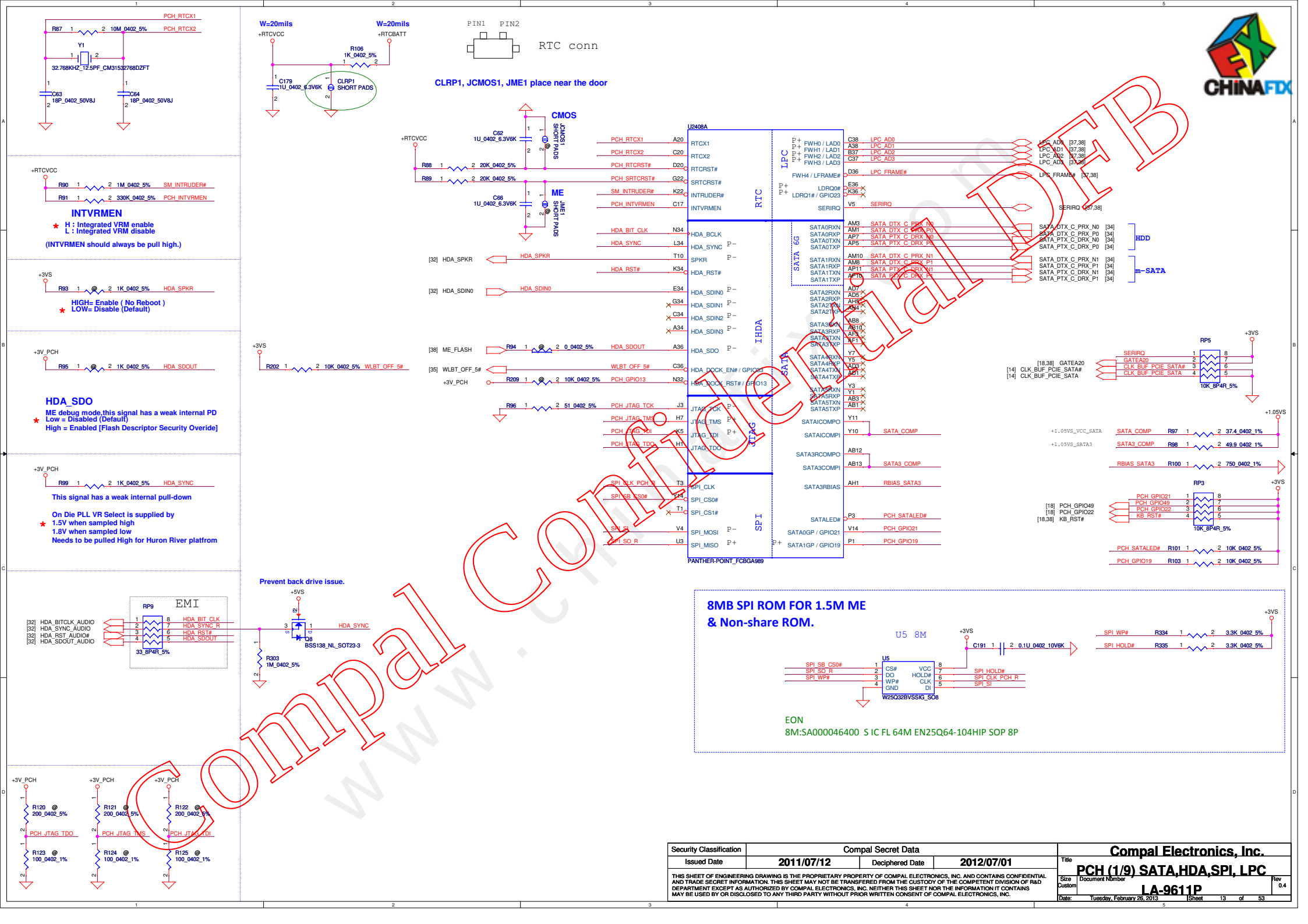

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

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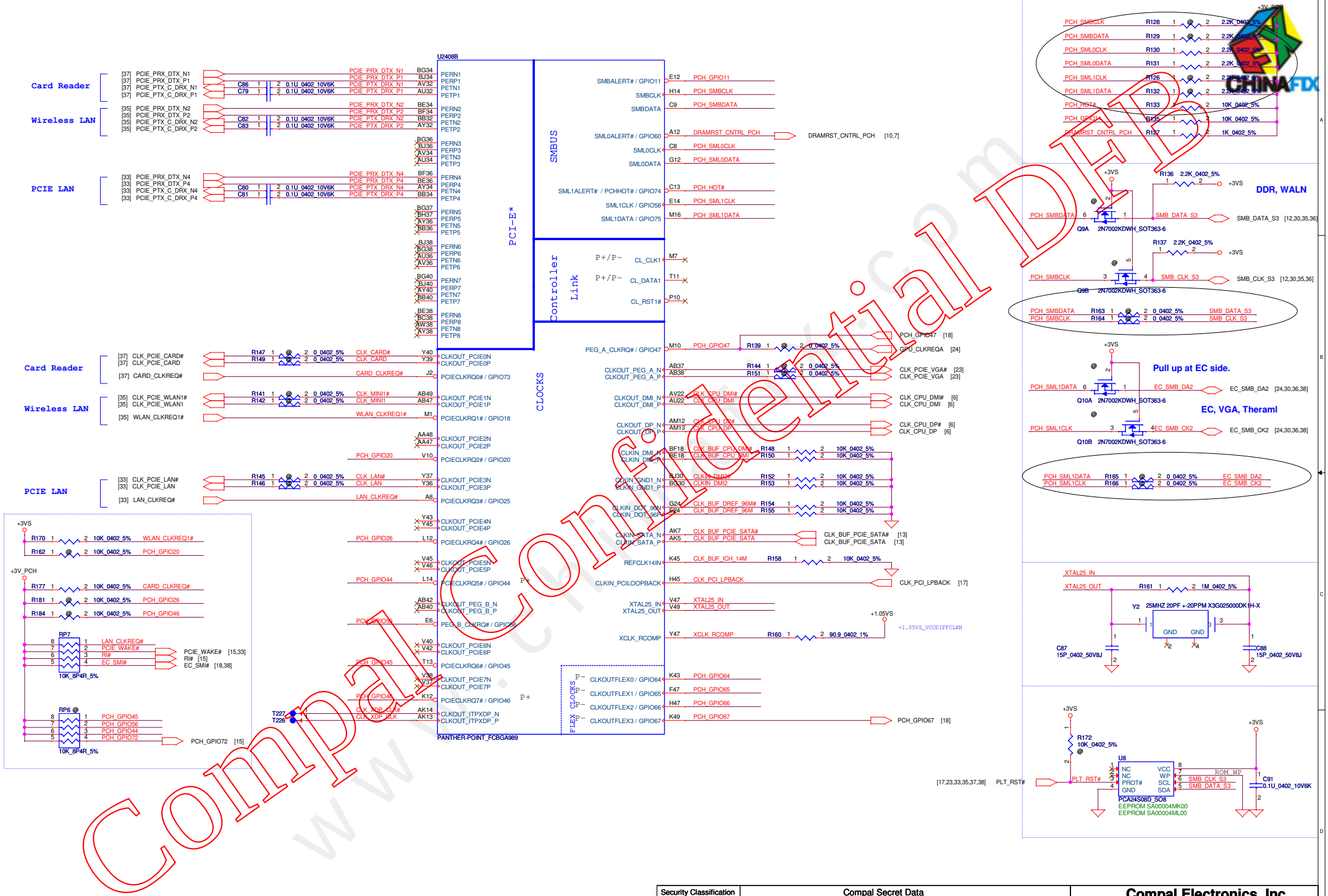
Date: Tuesday, February 26, 2013 | Sheet 13 of 53



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Title: PCH (2/8) PCIE, SMBUS, CLK

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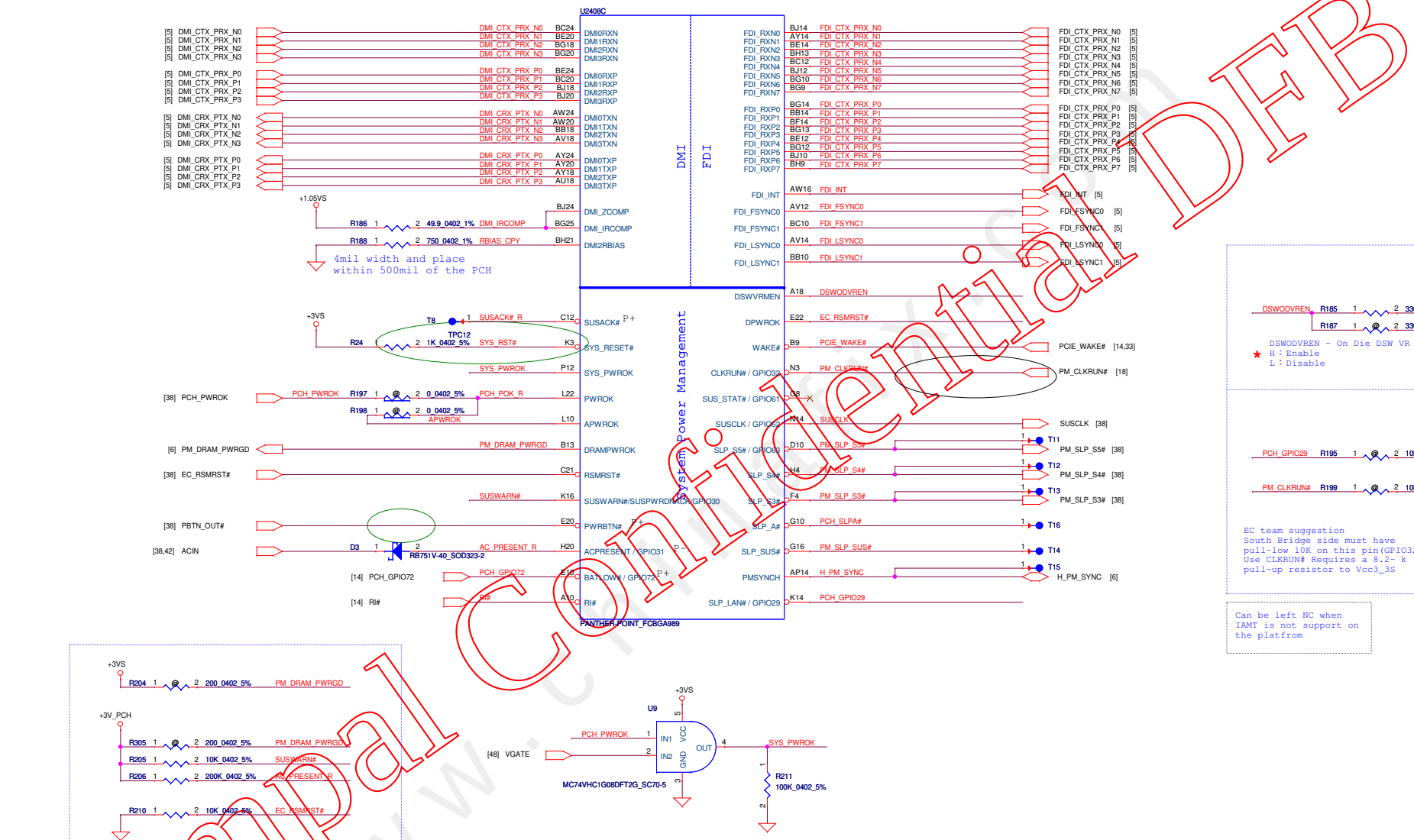
Date: Tuesday, February 26, 2013 | Sheet 14 of 53



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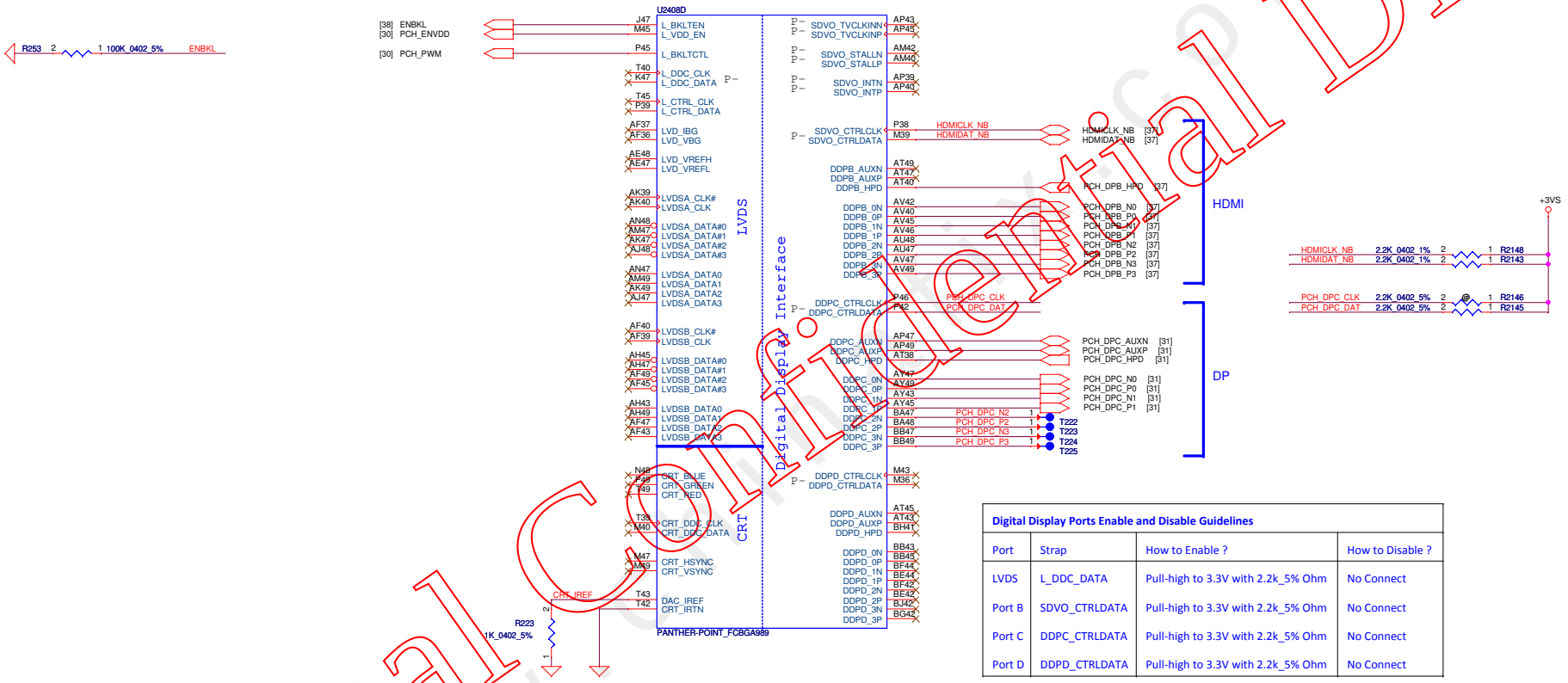
Compal Electronics, Inc.			
Title	PCH (3/8) DMI,FDI,PM,		
Size Custom	Document Number LA-9611P		Rev 0.4
Date: Tuesday, February 26, 2013	Sheet 15 of 53		



Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable ?	How to Disable ?
LVDS	L_DDC_DATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect
Port B	SDVO_CTRLDATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect
Port C	DDPC_CTRLDATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect
Port D	DDPD_CTRLDATA	Pull-high to 3.3V with 2.2k_5% Ohm	No Connect

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

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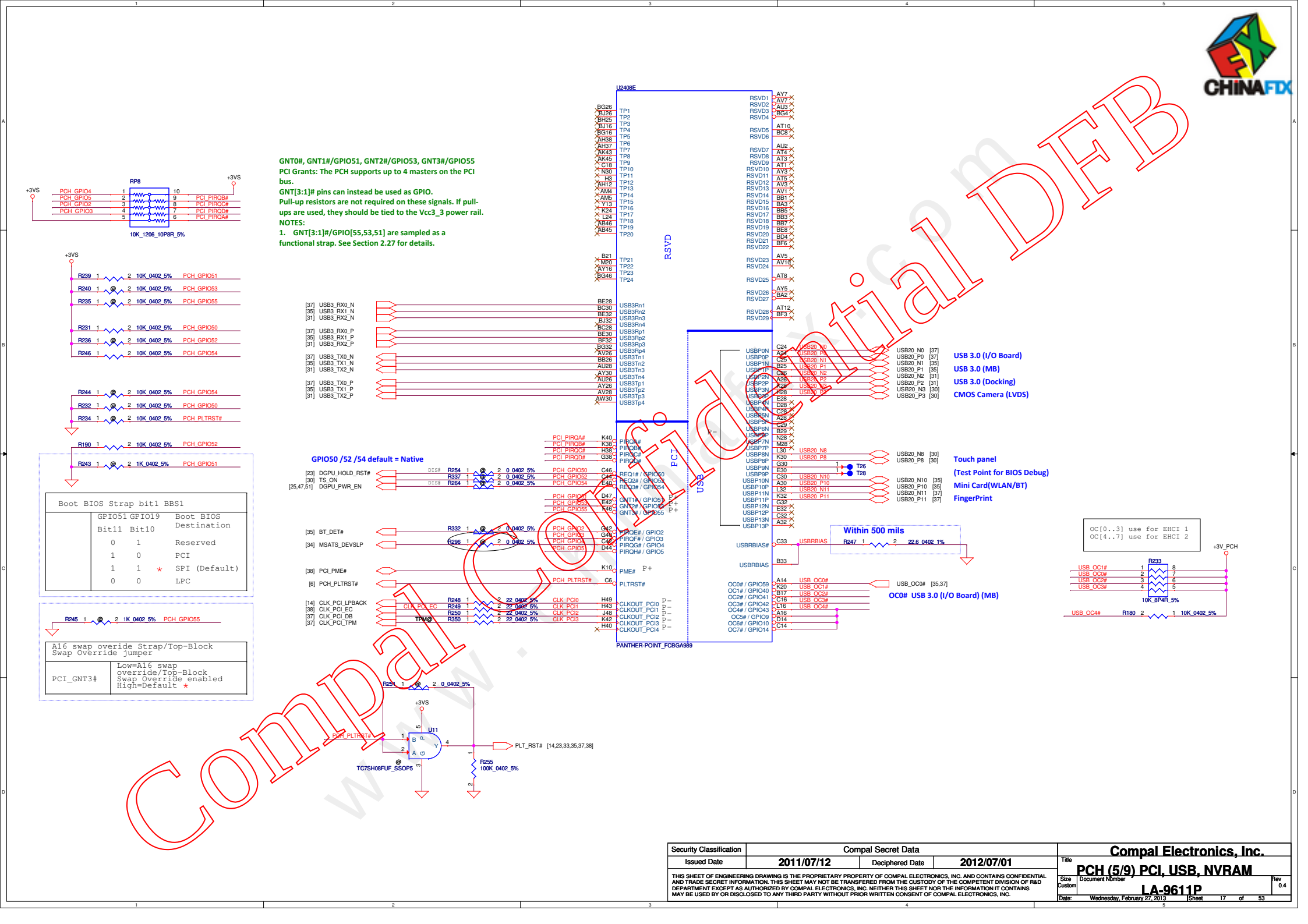

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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

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Date: Wednesday, February 27, 2013 | Sheet 17 of 53

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R265 1 @ 2 1K_0402_5% PCH_GPIO28

R274 1 @ 2 1K_0402_5% EC_SMI#

+3VS
R280 1 @ 2 10K_0402_5%
R282 1 @ 2 10K_0402_5% WLBT_OFF_51#

+3V_PCH
R288 1 @ 2 10K_0402_5%
R290 1 @ 2 10K_0402_5% PCH_GPIO24

+3VS
R285 1 @ 2 10K_0402_5%
R284 1 @ 2 10K_0402_5% PCH_GPIO37

+3V_PCH +3VS RP4
1 8 PCH_GPIO0
2 7 PM_CLKRUN# PM_CLKRUN# [15]
3 6 PCH_GPIO28
4 5 PCH_GPIO47 PCH_GPIO47 [14]
10K_8P4R_5%

+3VS
R266 1 @ 2 10K_0402_5% DOCK_PRSNT#
R344 1 @ 2 10K_0402_5% EC_SCI#
R275 1 @ 2 10K_0402_5% PCH_GPIO16
R268 1 @ 2 10K_0402_5% DGPU_PWROK
R346 1 @ 2 10K_0402_5% PCH_GPIO34
R283 1 @ 2 10K_0402_5% PCH_GPIO35
R287 1 @ 2 10K_0402_5% PCH_GPIO39
R289 1 @ 2 10K_0402_5% PCH_GPIO48

+3V_PCH
R293 1 2 100K_0402_5% PCH_GPIO27
R271 1 2 10K_0402_5% PCH_GPIO12
R273 1 2 1K_0402_5% PCH_GPIO15

R292 1 @ 2 10K_0402_5% PCH_GPIO57

U2408F

[30] TS_INT# PCH_GPIO0 T7 BMBUSY# / GPIO0
TS_INT# A42 TACH1 / GPIO1
[31] DOCK_PRSNT# DOCK_PRSNT# H36 TACH2 / GPIO6
[38] EC_SCI# EC_SCI# E38 TACH3 / GPIO7
[14,38] EC_SMI# EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
[38] EC_WAKE# R178 1 @ 2 0_0402_5% PCH_GPIO15 G2 GPIO15
PCH_GPIO16 U2 SATA4GP / GPIO16
[38,47] DGPU_PWROK DGPU_PWROK D40 TACH0 / GPIO17
[13] PCH_GPIO22 PCH_GPIO22 T5 SCLOCK / GPIO22
PCH_GPIO24 E8 GPIO24
PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
PCH_GPIO34 K1 STP_PCI# / GPIO34
PCH_GPIO35 K4 GPIO35
[35] WLBT_OFF_51# WLBT_OFF_51# V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
PCH_GPIO38 N2 SLOAD / GPIO38
PCH_GPIO39 M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
[13] PCH_GPIO49 PCH_GPIO49 V3 SATA5GP / GPIO49 / TEMP_ALERT#
PCH_GPIO57 D6 GPIO57

GPIO

T22 1 A4 VSS_NCTF_1
T24 1 A44 VSS_NCTF_2
T26 A45 VSS_NCTF_3
T28 A46 VSS_NCTF_4
T30 1 A5 VSS_NCTF_5
T32 1 A6 VSS_NCTF_6
T34 1 B3 VSS_NCTF_7
T36 B47 VSS_NCTF_8
T38 1 BD1 VSS_NCTF_9
T40 1 BD49 VSS_NCTF_10
T42 1 BE1 VSS_NCTF_11
T44 1 BE49 VSS_NCTF_12
T46 1 BF1 VSS_NCTF_13
T48 1 BF49 VSS_NCTF_14

NCTF

VSS_NCTF_15 BG2 1 T18
VSS_NCTF_16 BG48 1 T19
VSS_NCTF_17 BH3 1 T20
VSS_NCTF_18 BH47 1 T21
VSS_NCTF_19 BJ4 1 T23
VSS_NCTF_20 BJ44 1 T25
VSS_NCTF_21 BJ45 1 T27
VSS_NCTF_22 BJ46 1 T29
VSS_NCTF_23 BJ5 1 T31
VSS_NCTF_24 BJ6 1 T33
VSS_NCTF_25 C2 1 T35
VSS_NCTF_26 C48
VSS_NCTF_27 D1 1 T39
VSS_NCTF_28 D49
VSS_NCTF_29 E1 1 T43
VSS_NCTF_30 E49
VSS_NCTF_31 F1 1 T47
VSS_NCTF_32 F49

PANTHER-POINT_FCBGA989

CPU/MISC

C40 TS_PRSNC# TS_PRSNC# [30]
B41 PCH_GPIO69
C41 PCH_GPIO70
A40 PCH_GPIO71
P4 A20GATE GATEA20 [13,38]
AU16 PCH_PECI_R R267 1 @ 2 0_0402_5% H_PECI H_PECI [38,6]
P5 RCIN# KB_RST# KB_RST# [13,38]
AY11 H_CPUPWRGD H_CPUPWRGD [6]
AY10 R278 1 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# [6]
T14 INIT3_3V
AY1 DF_TVS

INIT3_3V
This signal has weak internal PU, can't pull low.

Intel schematic review recommand.

AH8 TS_VSS1
AK11 TS_VSS2
AH10 TS_VSS3
AK10 TS_VSS4
P37 NC_1

TS_PRSNC# R256 1 2 10K_0402_5%
PCH_GPIO71 5 4
PCH_GPIO70 6 3
PCH_GPIO69 7 2
TS_INT# 8 1
RP10 10K_8P4R_5%

+1.8VS
R226 2.2K_0402_5%
DF_TVS R229 1 2 1K_0402_5% H_SNB_IVB# [6]

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA

+3VS
R259 10K_0402_5% @
R330 10K_0402_5% UMA@
R311 10K_0402_5% UMA@
PCH_GPIO69
PCH_GPIO38
PCH_GPIO67
PCH_GPIO67 [14]
Connect to RP10
R329 10K_0402_5% DIS@
R286 10K_0402_5% DIS@

(MB_ID_2)
(MB_ID_1)
(MB_ID_0)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

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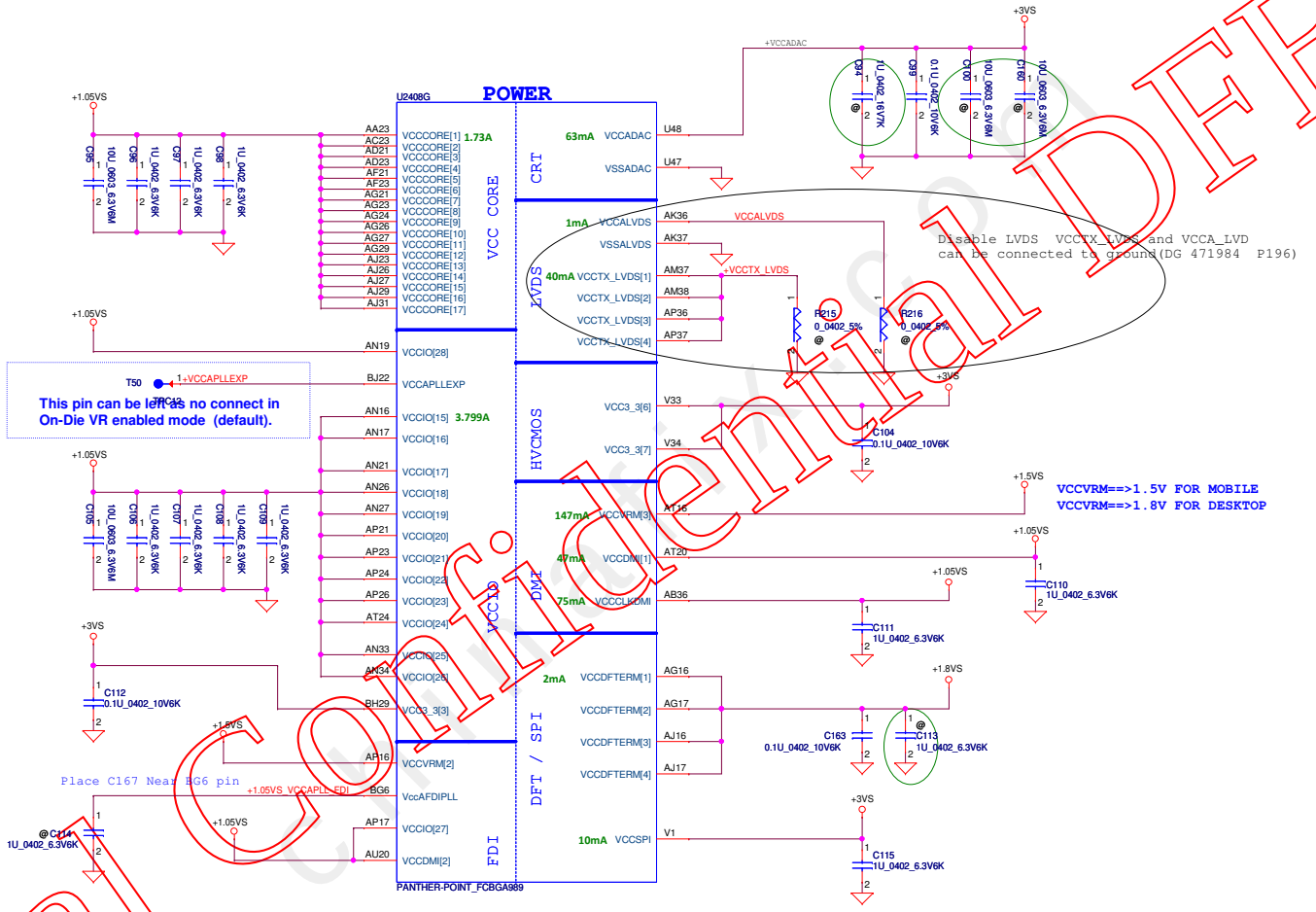

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-9611P | Rev: 0.4

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VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

Have internal VRM

If platform does not support Deep S4/S5 then tie to VccSus3_3.

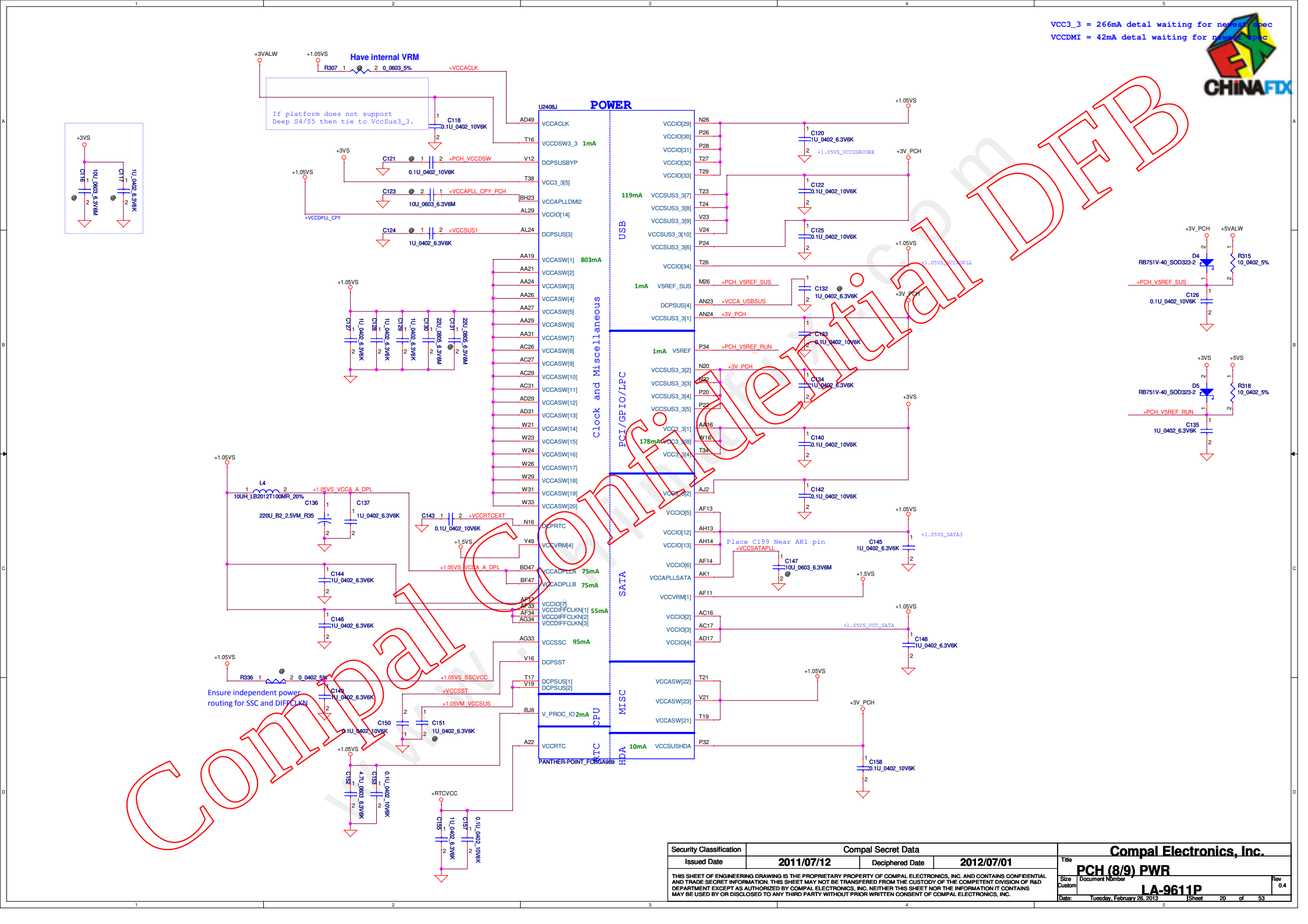
Ensure independent power routing for SSC and DIFFCLKN

Place C199 Near AK1 pin

POWER

U2408J

PANTHER-POINT_FCBGA989



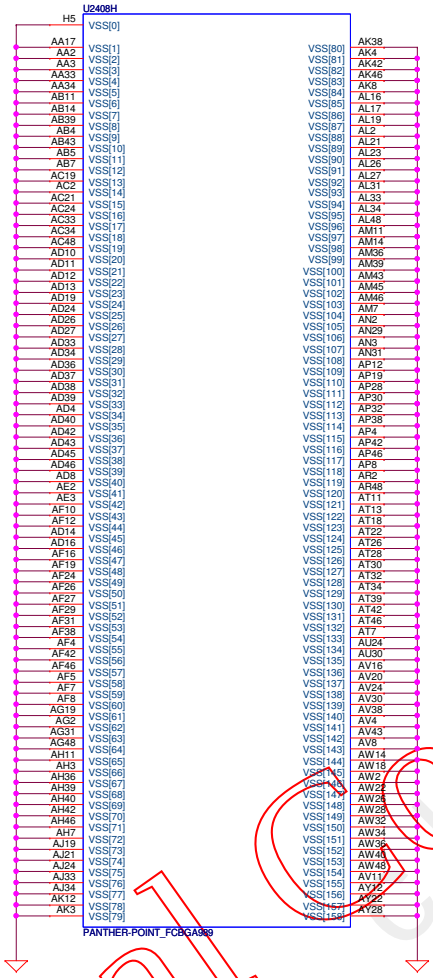
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-9611P | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 20 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size: Custom | Document Number: **LA-9611P** | Rev: 0.4

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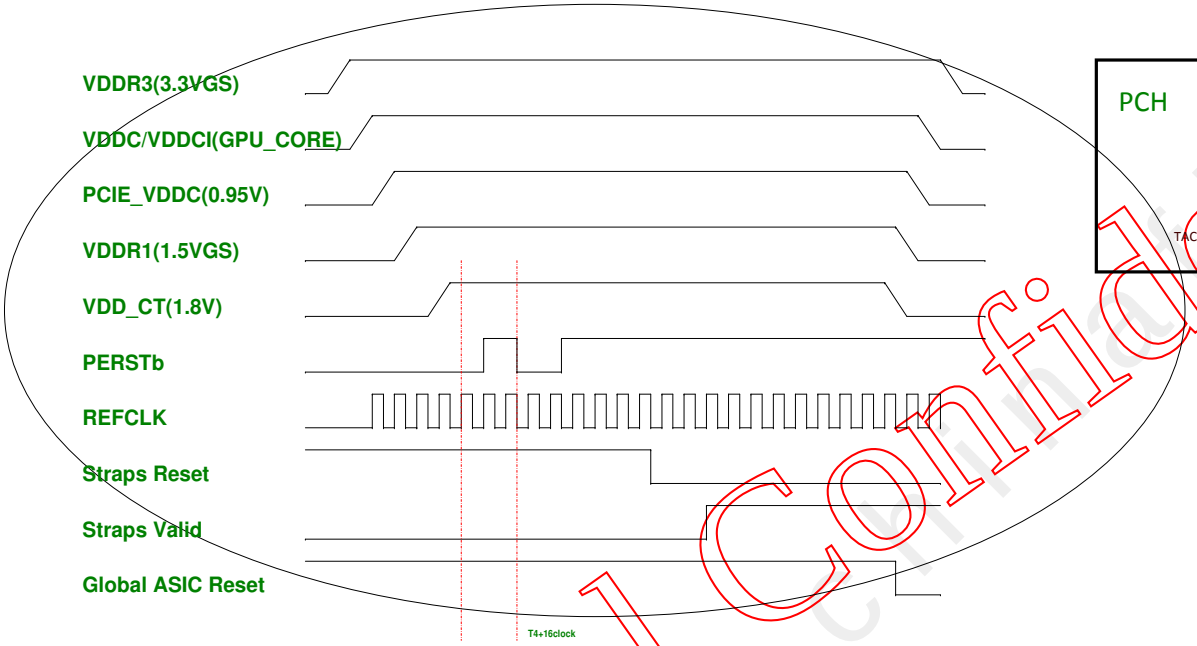
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

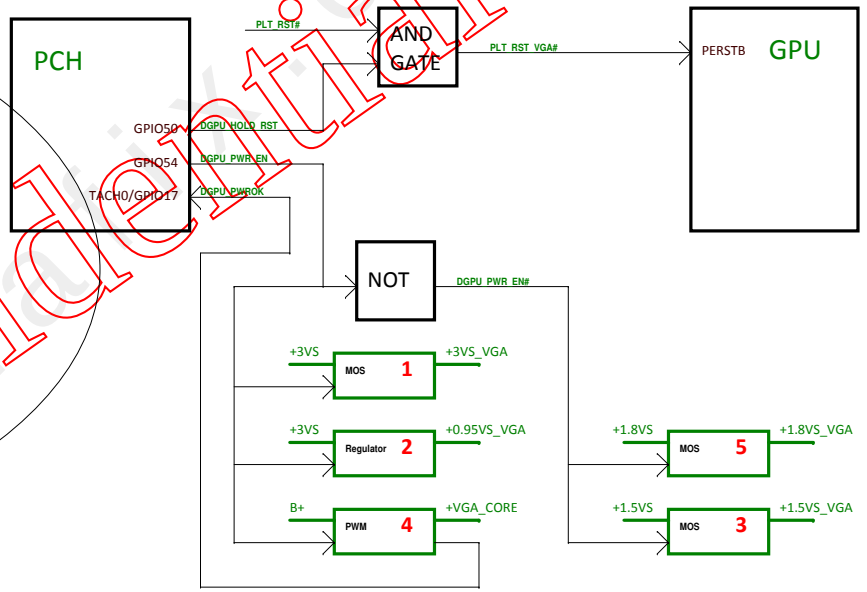
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



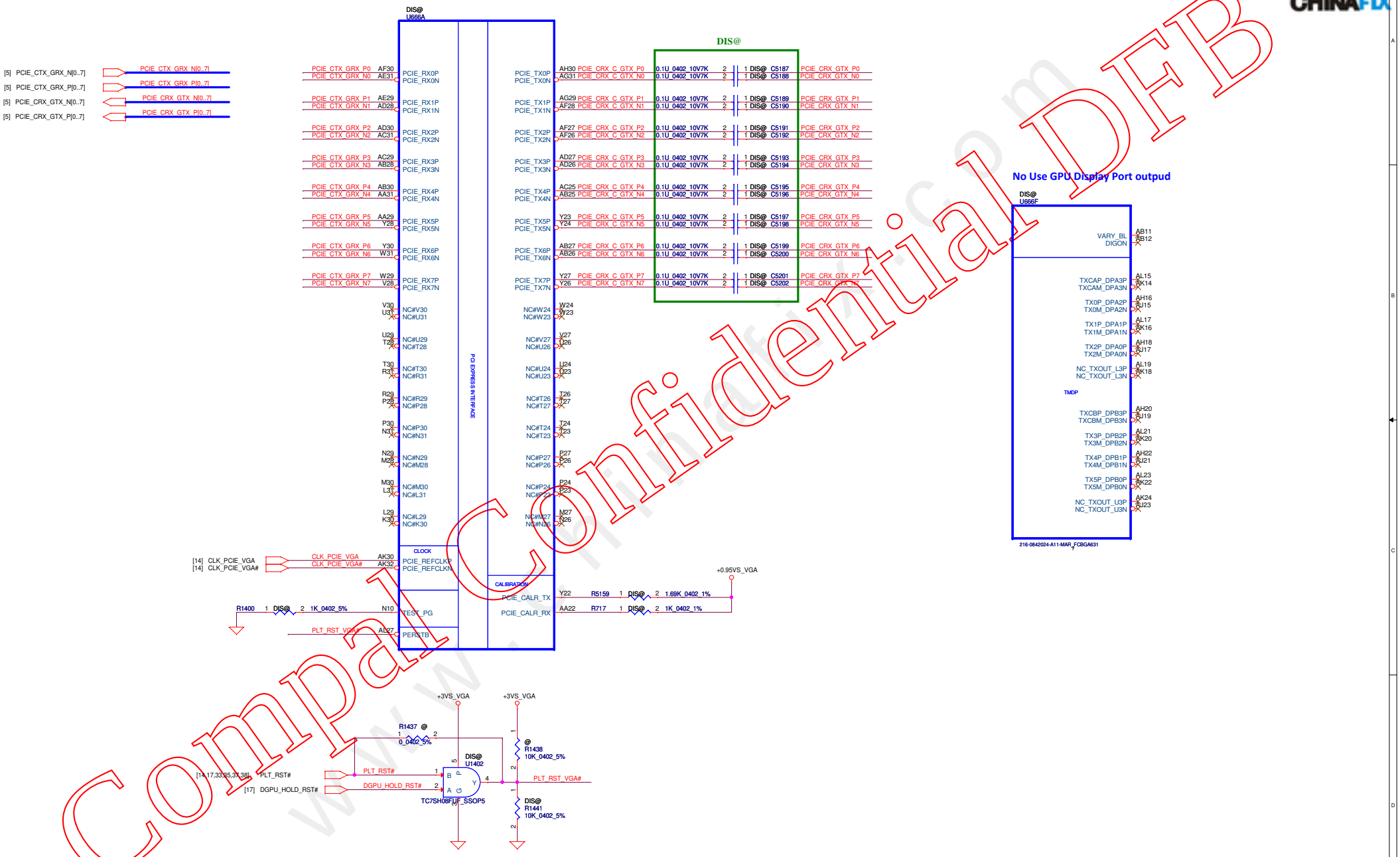
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: MARS_Note

Size: Custom | Document Number: LA-9611P | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 22 of 53



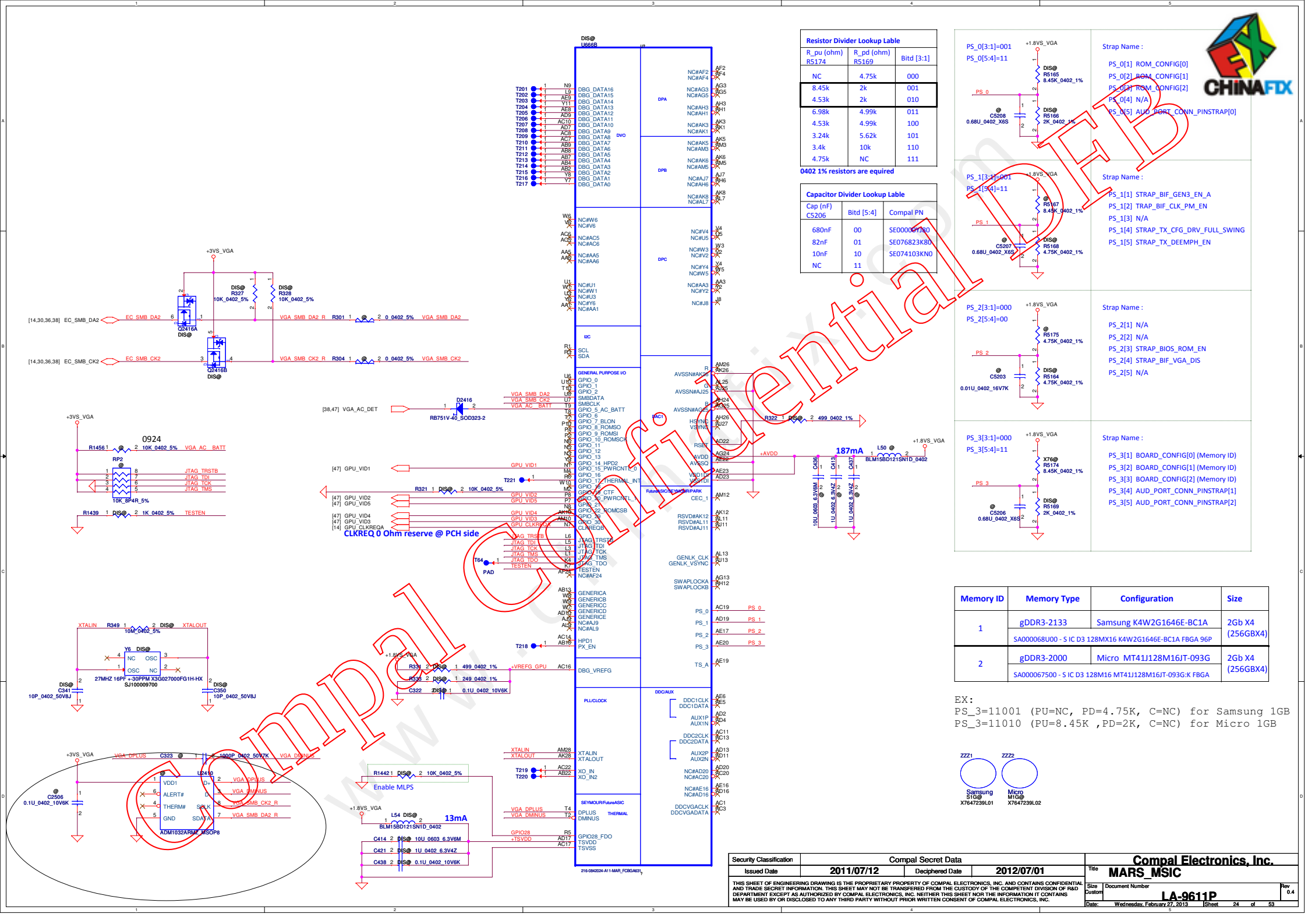
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: MARS_PCIE/DP

Size: Custom | Document Number: LA-9611P | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 23 of 53



Resistor Divider Lookup Lable

R_pu (ohm) R5174	R_pd (ohm) R5169	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF) C5206	Bitd [5:4]	Compal PN
680nF	00	SE000001J80
82nF	01	SE076823K80
10nF	10	SE074103KN0
NC	11	

Memory ID	Memory Type	Configuration	Size
1	gDDR3-2133	Samsung K4W2G1646E-BC1A	2Gb X4 (256GBX4)
	SA000068U00 - S IC D3 128MX16 K4W2G1646E-BC1A FBGA 96P		
2	gDDR3-2000	Micro MT41J128M16JT-093G	2Gb X4 (256GBX4)
	SA000067500 - S IC D3 128M16 MT41J128M16JT-093G:K FBGA		

EX:
PS_3=11001 (PU=NC, PD=4.75K, C=NC) for Samsung 1GB
PS_3=11010 (PU=8.45K ,PD=2K, C=NC) for Micro 1GB

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

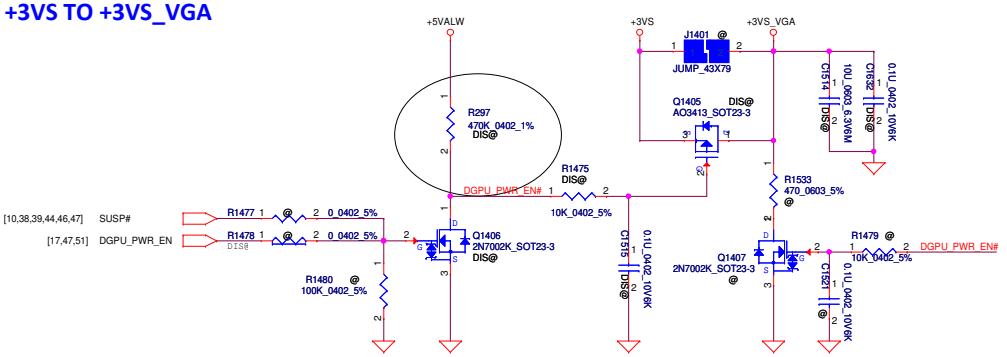
Compal Electronics, Inc.

Title: MARS_MSIC

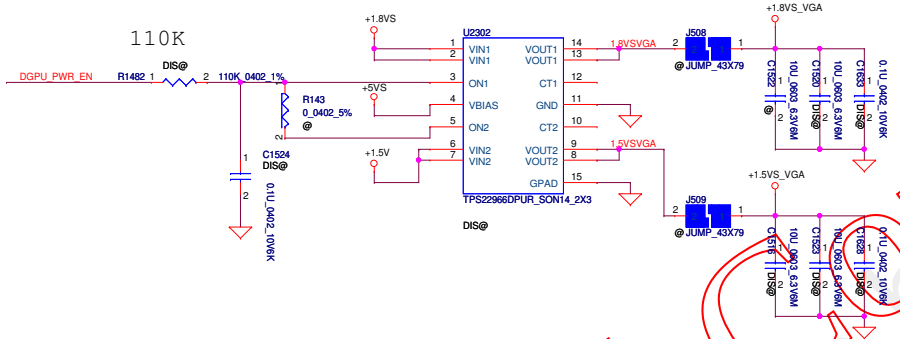
Size: Custom | Document Number: LA-9611P | Rev: 0.4

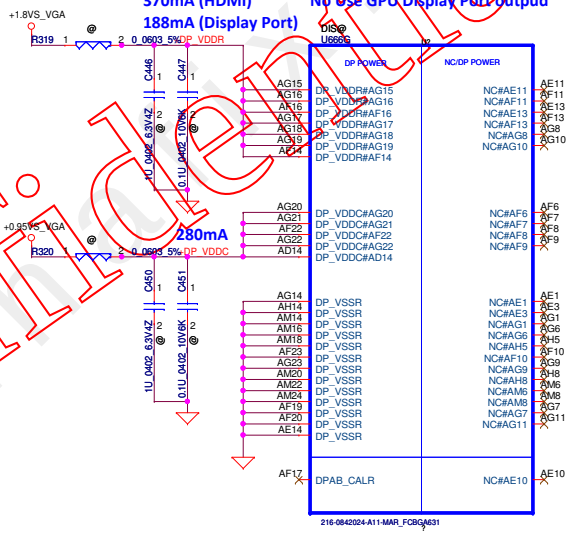
Date: Wednesday, February 27, 2013 | Sheet 24 of 53

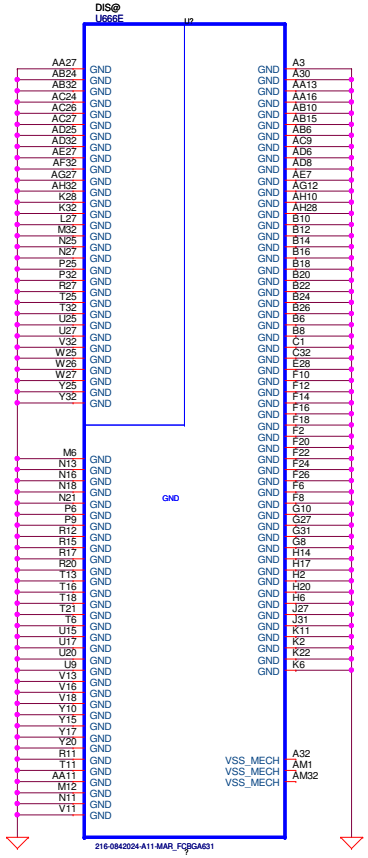
+3VS TO +3VS_VGA



+1.8VS TO +1.8VS_VGA
+1.5V TO +1.5VS_VGA







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.			
Title: MARS_Power/GND			
Size: Custom	Document Number: LA-9611P		Rev: 0.4
Date: Tuesday, February 26, 2013	Sheet 25 of 53		

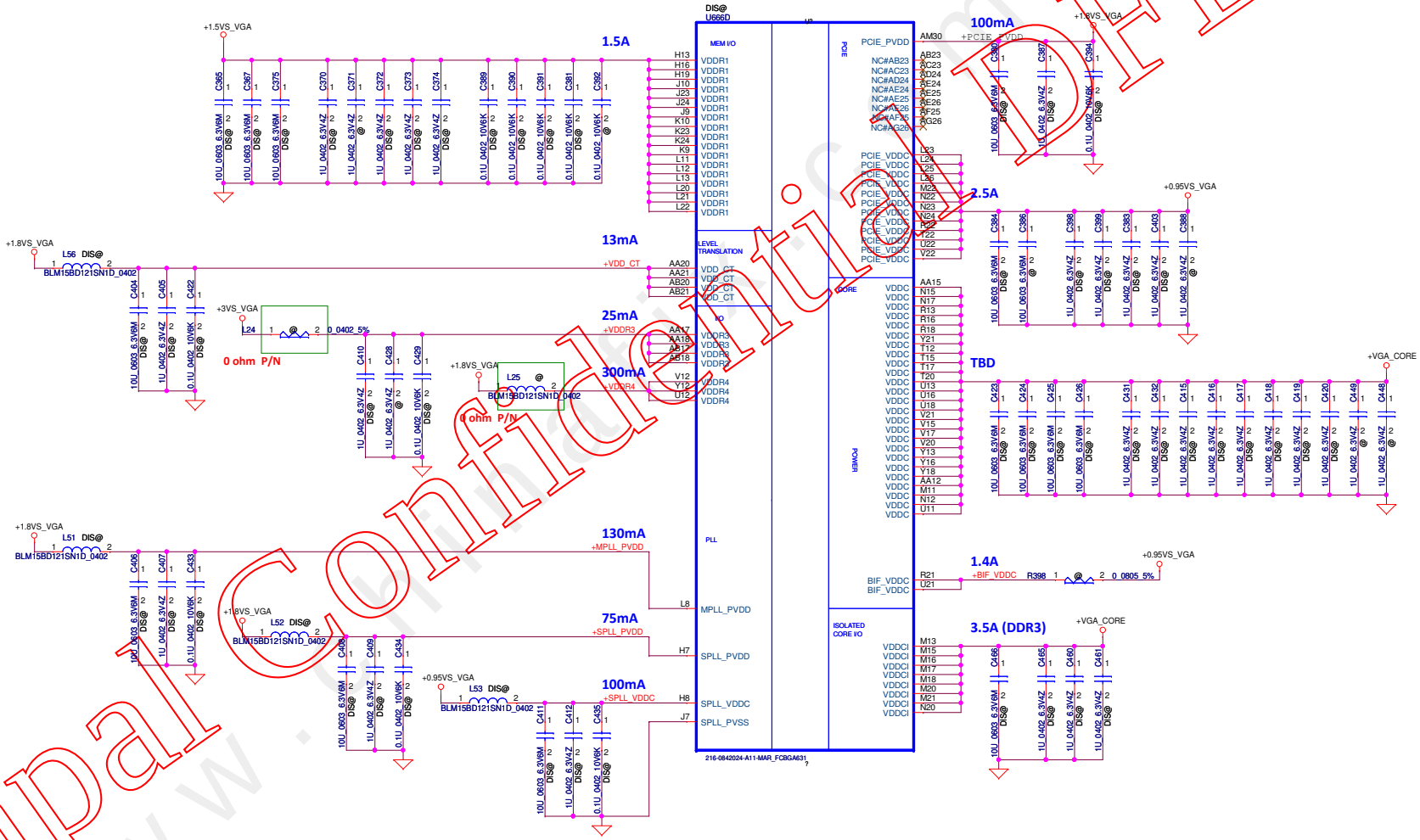
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: MARS_Power

Size: Custom | Document Number: LA-9611P | Rev: 0.4

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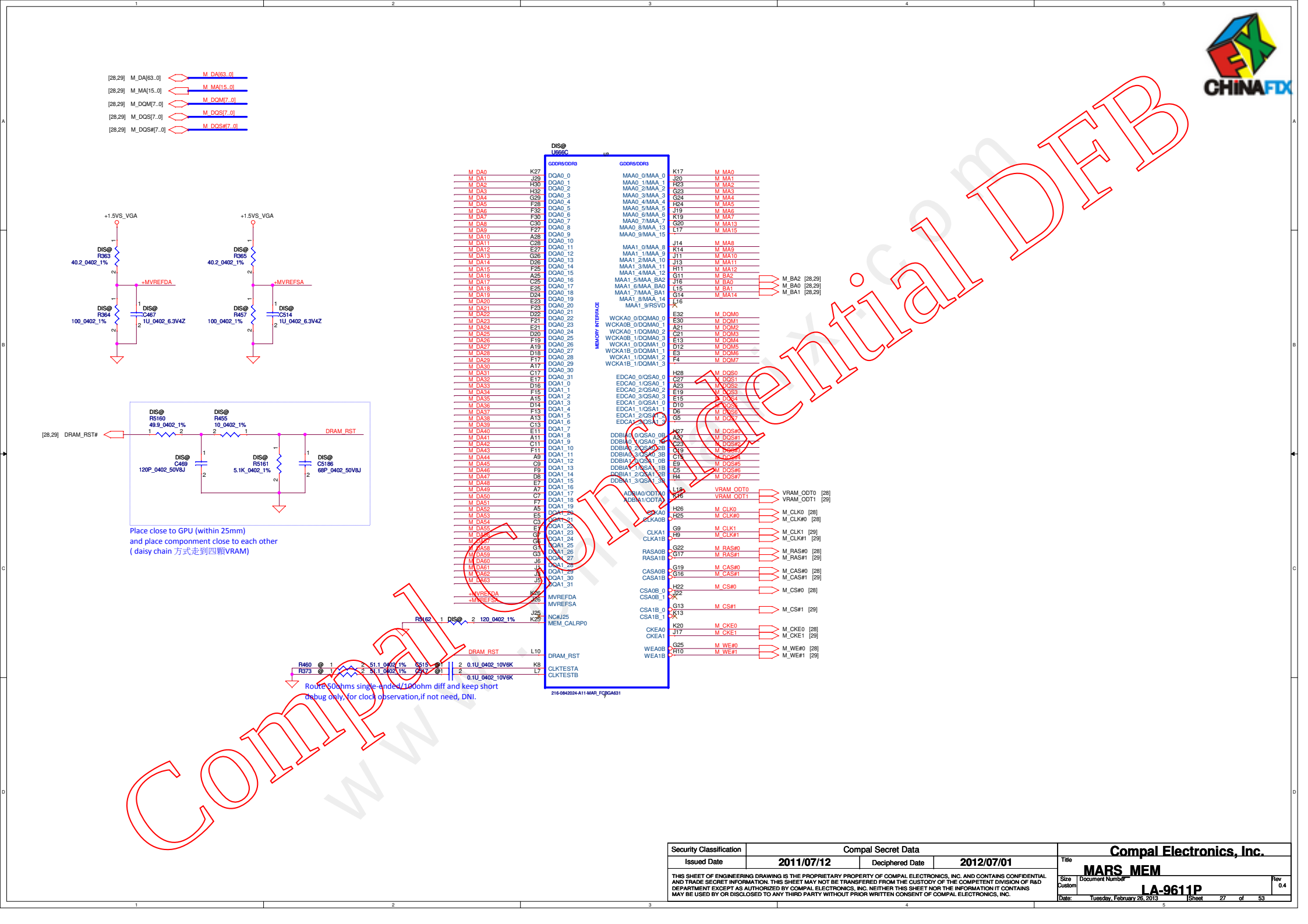
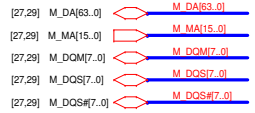
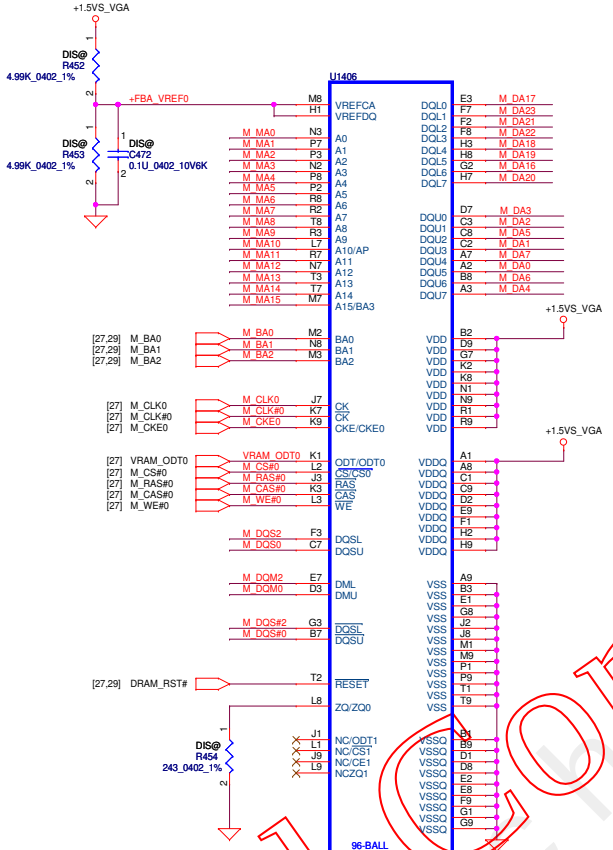


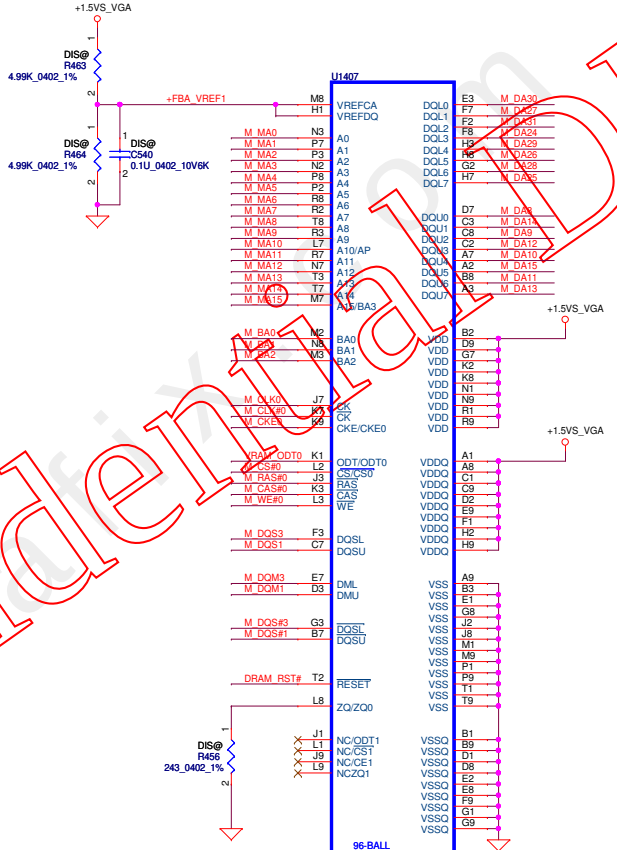
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

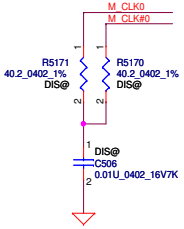
Compal Electronics, Inc.			
Title	MARS_MEM		
Size Custom	Document Number LA-9611P		Rev 0.4
Date: Tuesday, February 26, 2013	Sheet 27 of 53		

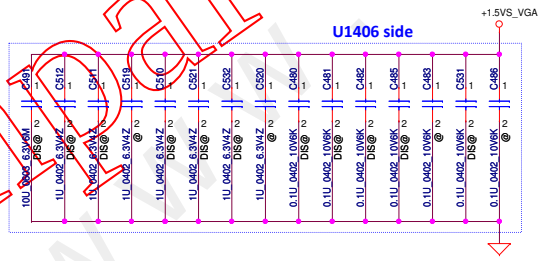
Memory Partition A - Lower 32 bits

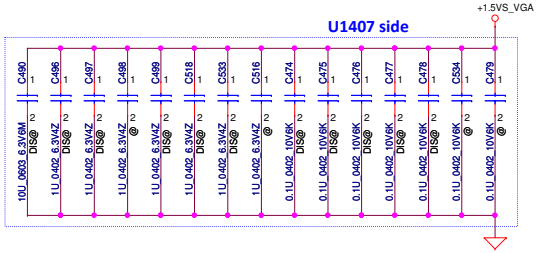












Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: MARS_VRAM A Lower

Size: Custom | Document Number: LA-9611P | Rev: 0.4

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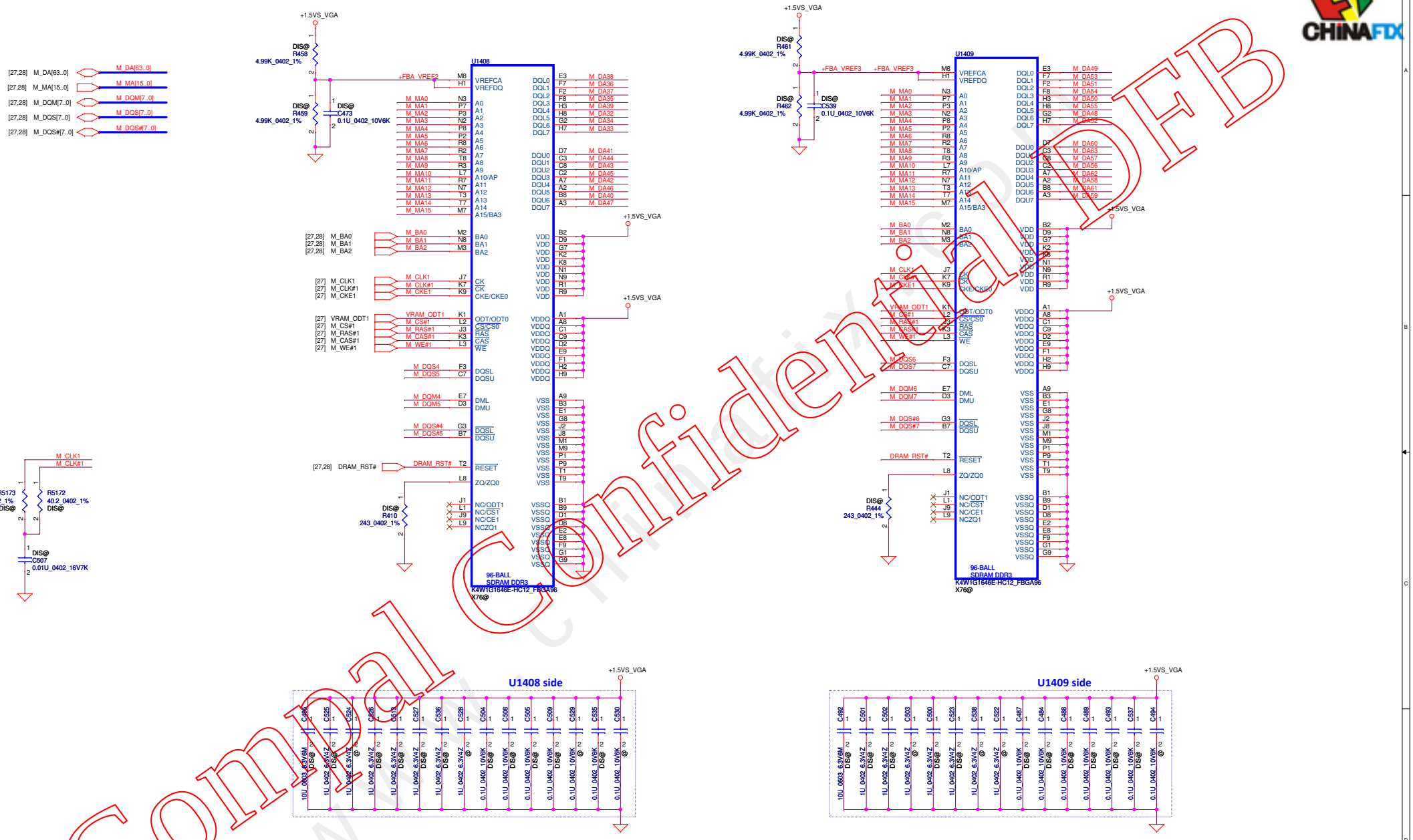
Memory Partition A – Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.			
Title: MARS_VRAM A Upper			
Size: Custom	Document Number: LA-9611P		Rev: 0.4
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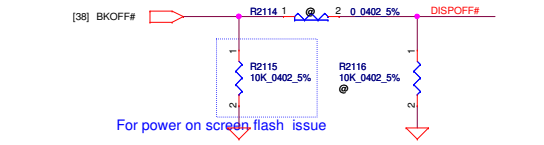

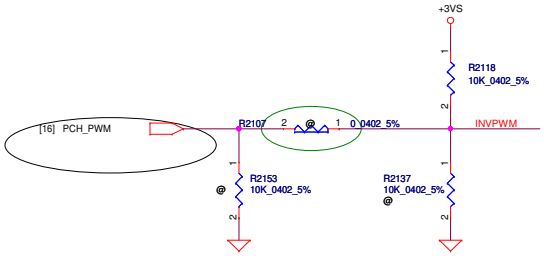

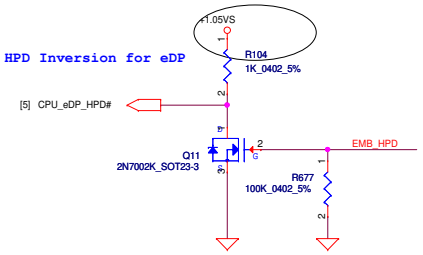

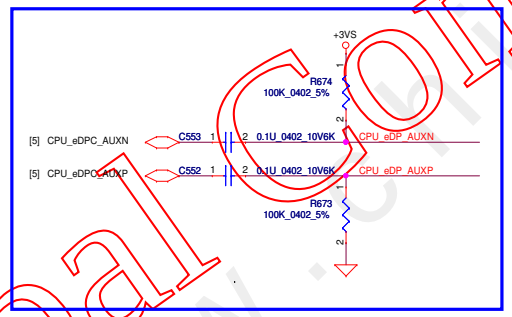

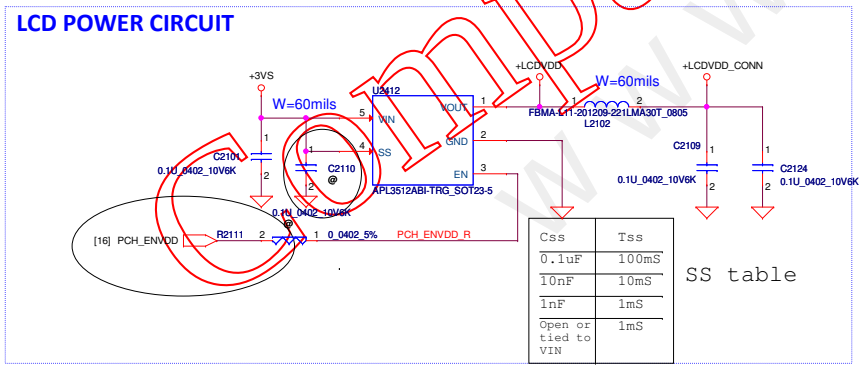

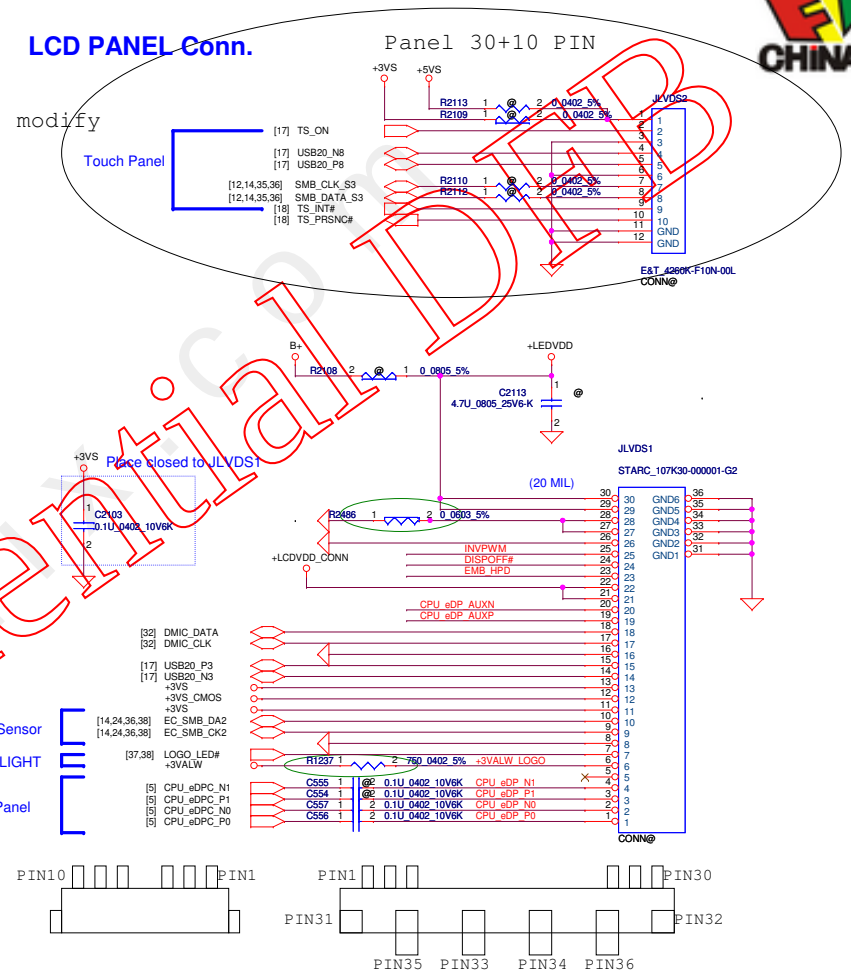

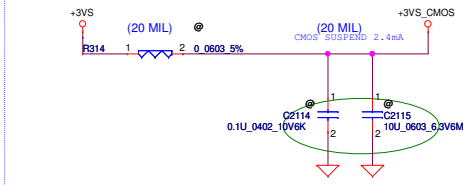

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: LVDS Connector

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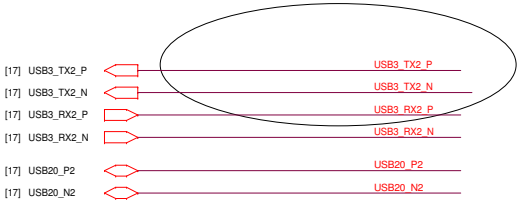
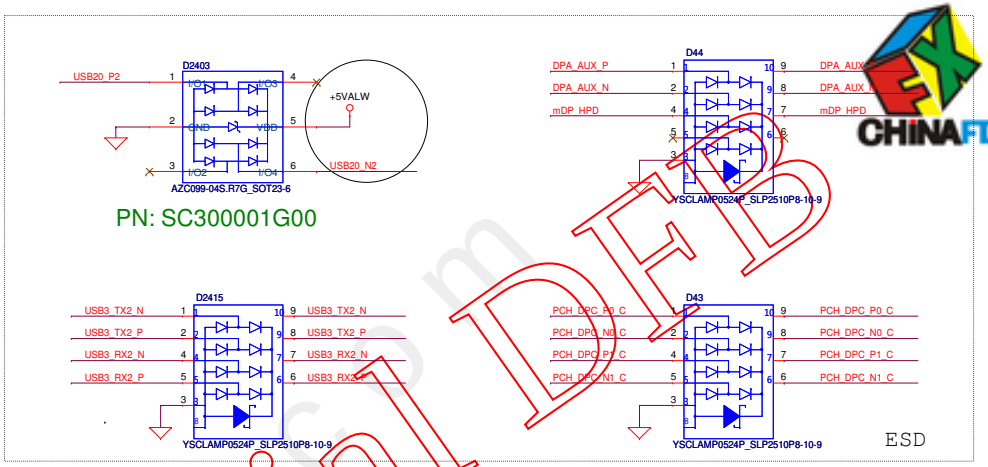
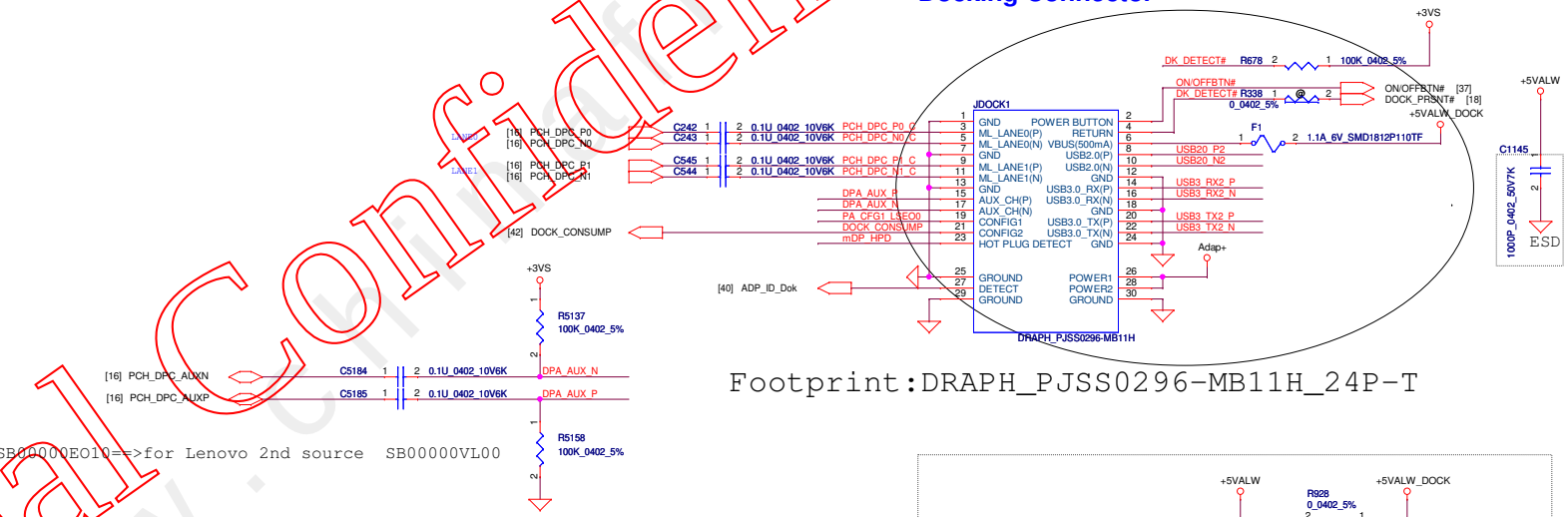
Docking (USB3.0)





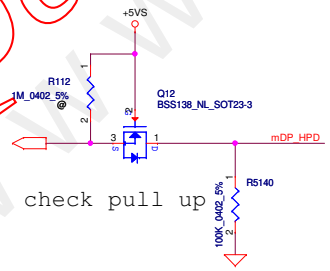
Docking (Display Port)

Docking Connector

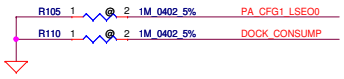


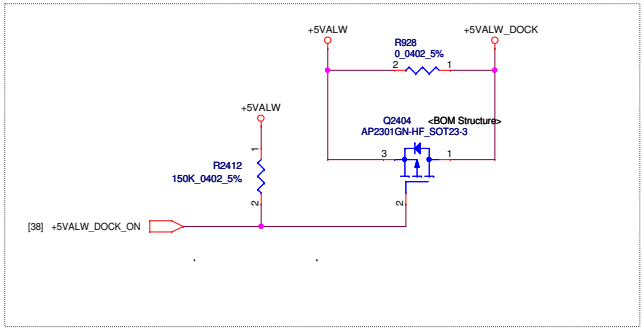
Footprint:DRAPH_PJSS0296-MB11H_24P-T

SB00000EO10==>for Lenovo 2nd source SB00000VL00



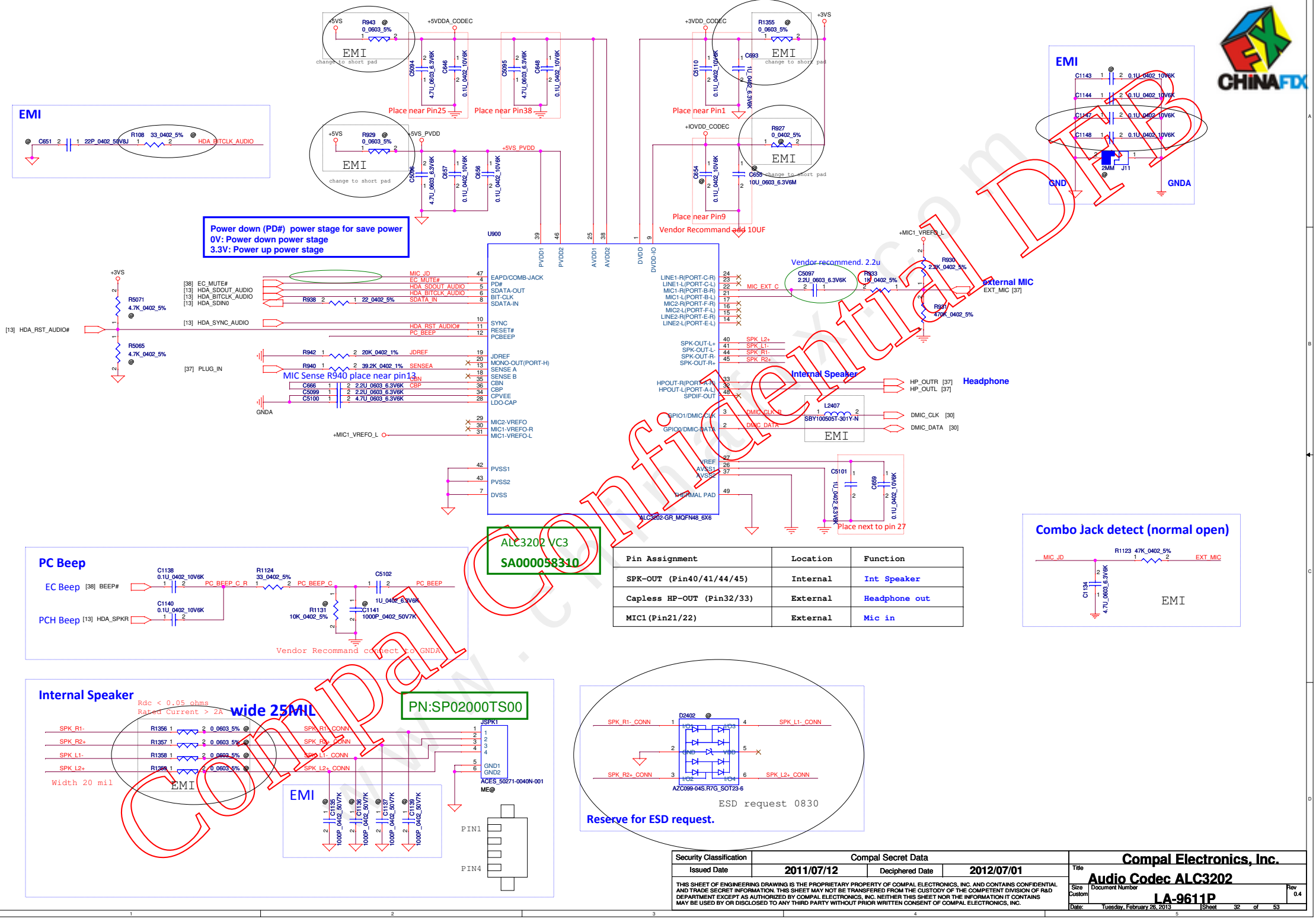
check pull up





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.			
Title: Docking			
Size: Custom	Document Number: LA-9611P		Rev: 0.4
Date: Tuesday, February 26, 2013	Sheet 31 of 53		



Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

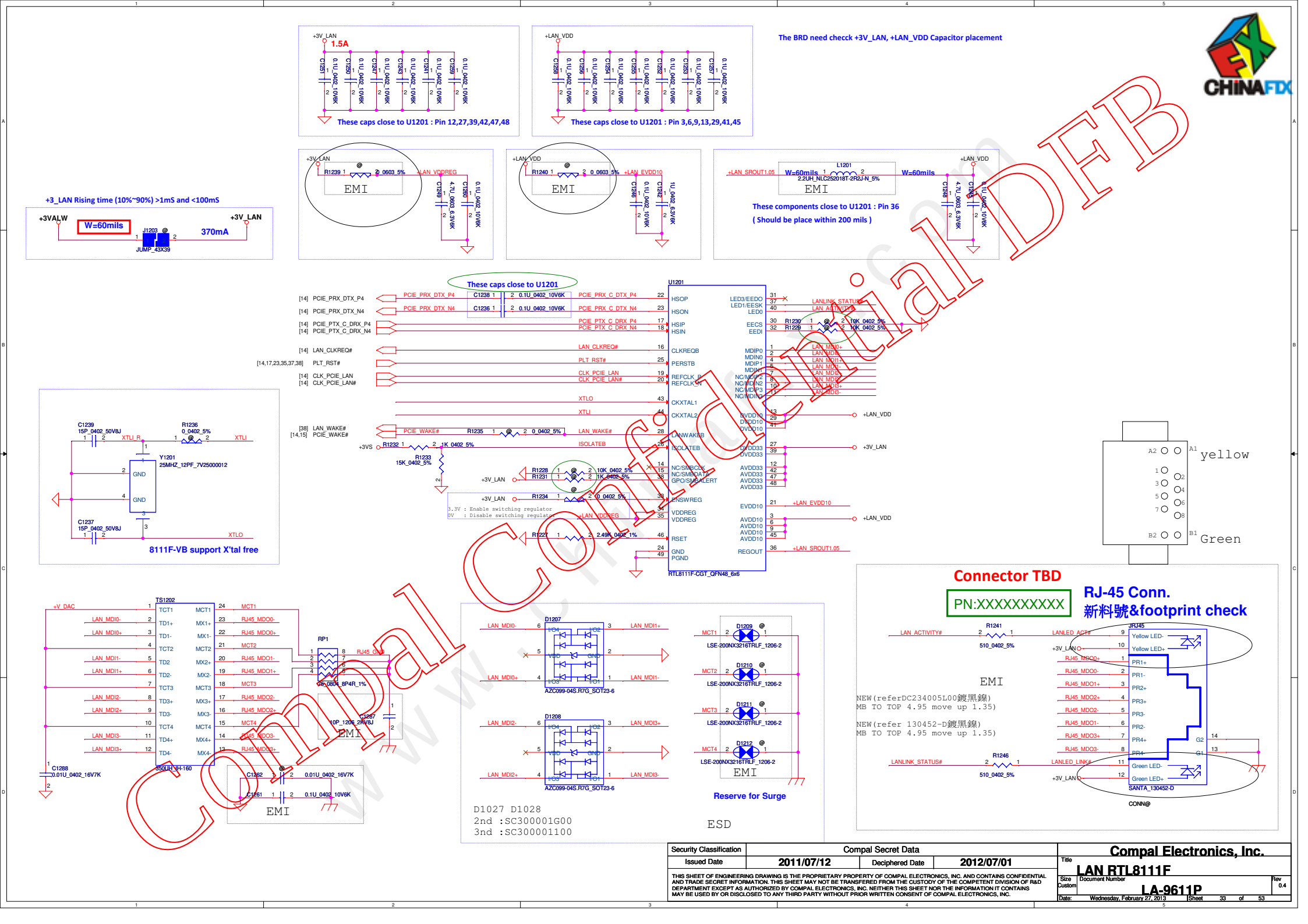
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: Audio Codec ALC3202

Size: Custom | Document Number: LA-9611P | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 32 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.			
Title	LAN RTL8111F		
Size	Document Number		Rev
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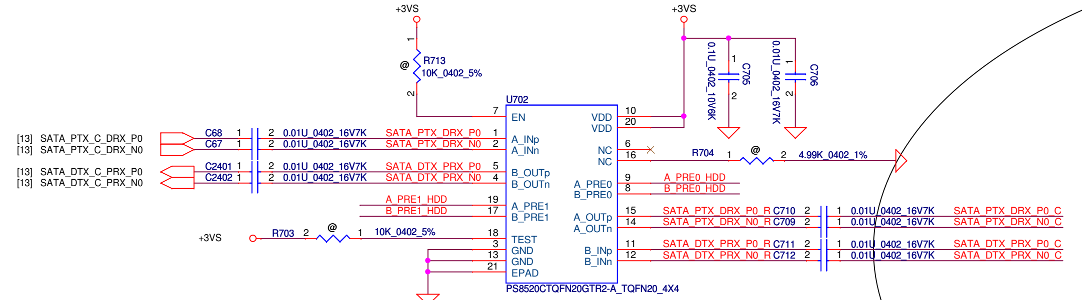
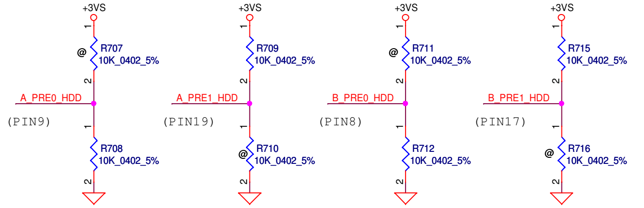
SATA HDD BTB CONN.





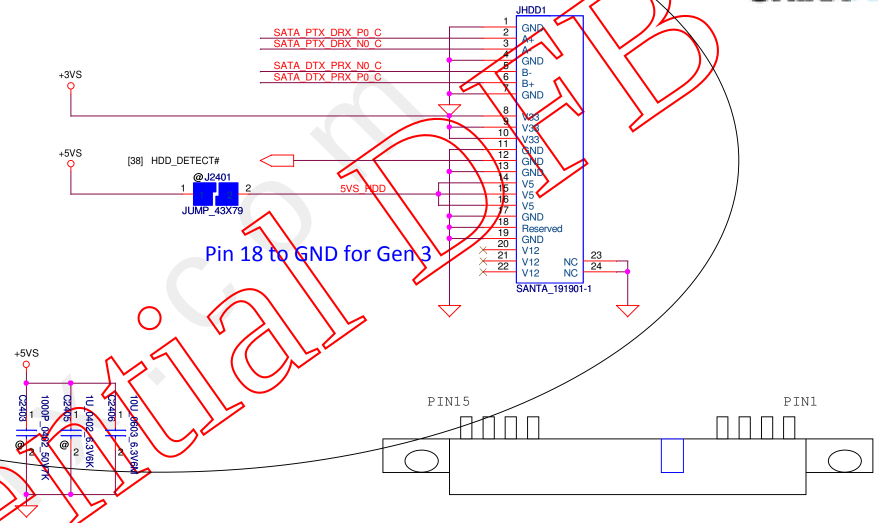
	TEST (Internal pull Low)
Normal operation (default)	Low
Compliance testing mode enable	High

	A_PRE1/B_PRE1 (Internal pull Low)	A_PRE0/B_PRE0 (Internal pull Low)
0dB, no pre-emphasis	Low	Low
1.5dB pre-emphasis is selected	Low	High
2.5dB pre-emphasis is selected	High	Low
3.5dB pre-emphasis is selected	High	High

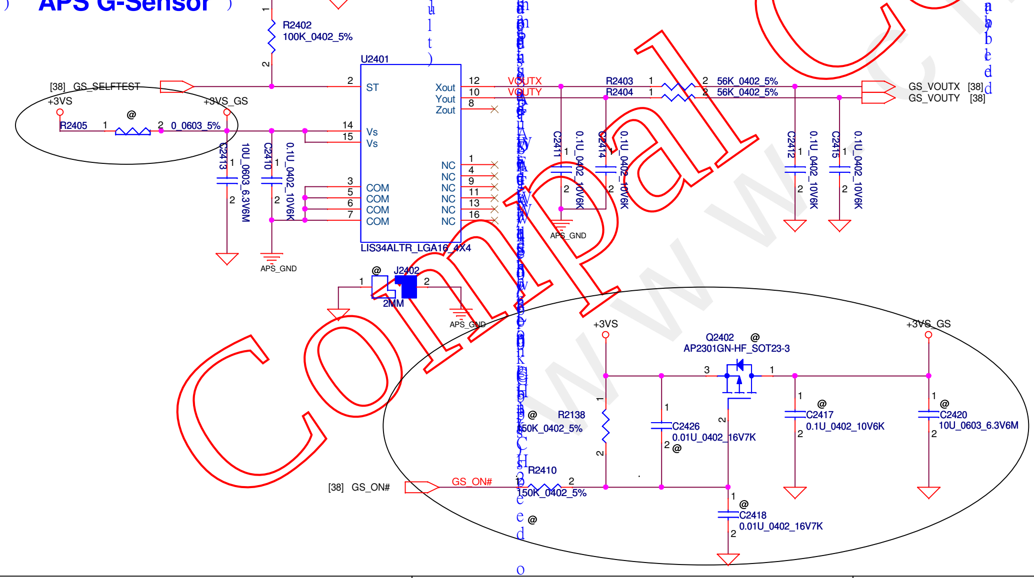
EN	Device Function StandBy Mode
0	D[illegible]
1	[illegible]

SATA HDD CONN.

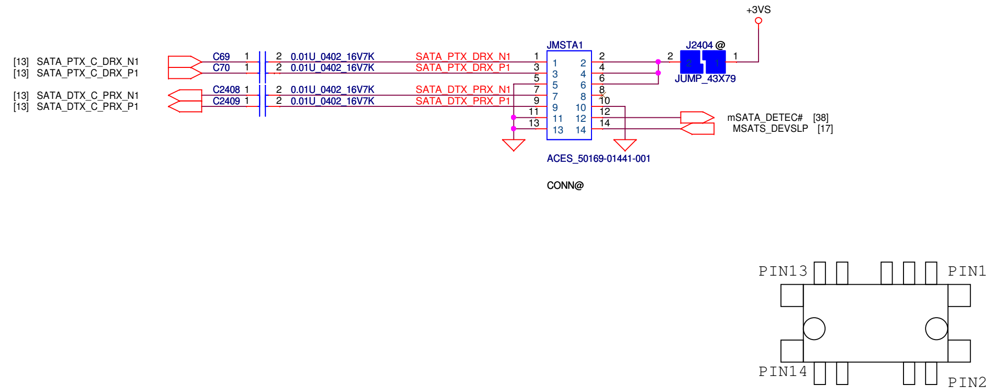
PN:XXXXXXXXXX



APS G-Sensor



mSATA CONN.



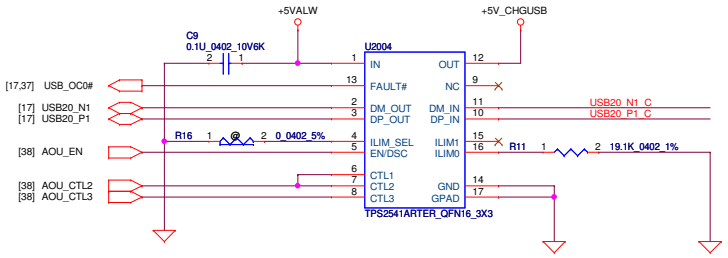
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

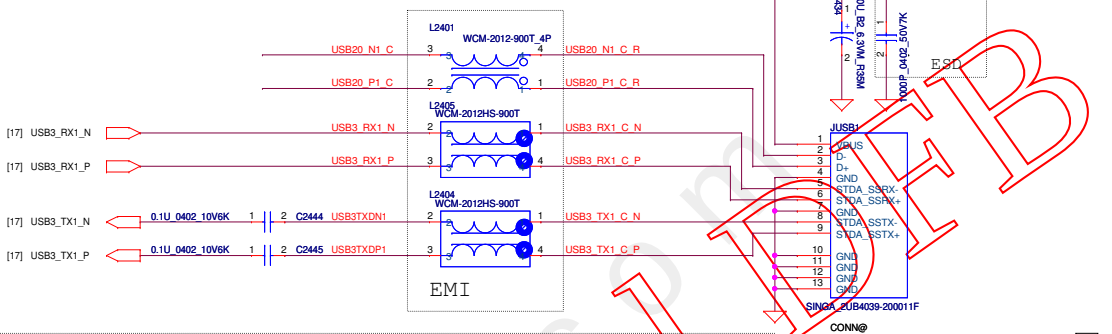
Title: HDD/mSATA/G-Sensor

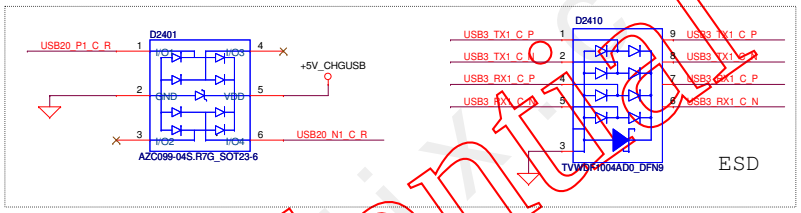
Size: Custom | Document Number: LA-9611P | Rev: 0.4

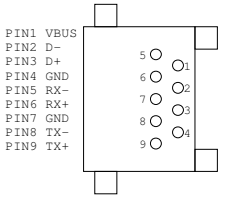
USB 3.0 Charger & Conn.



Superworld's common mode choke(SM070001V00) has quality issue for USB 3.0

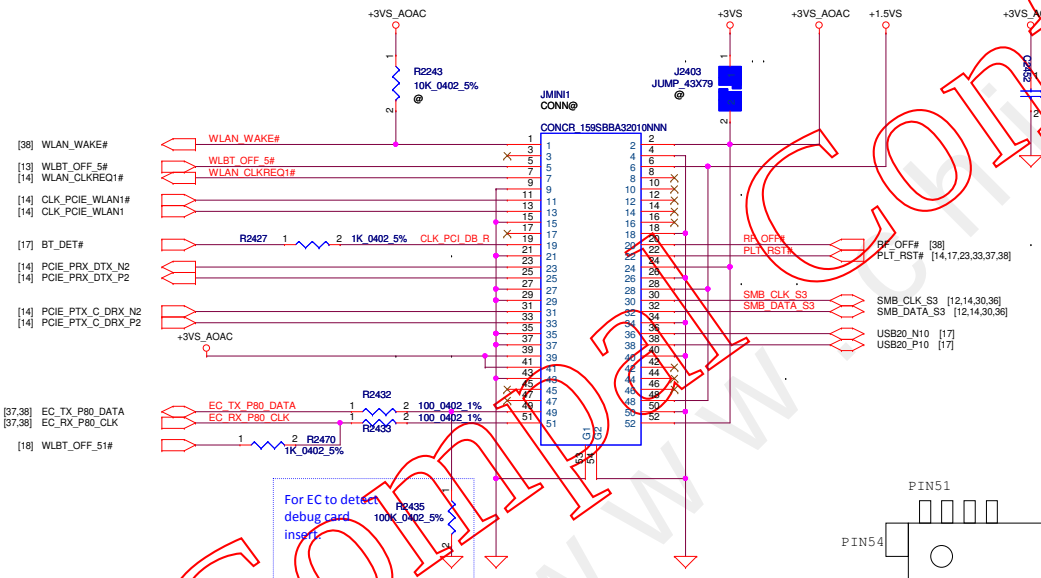




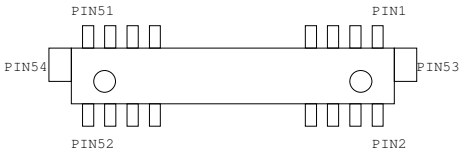


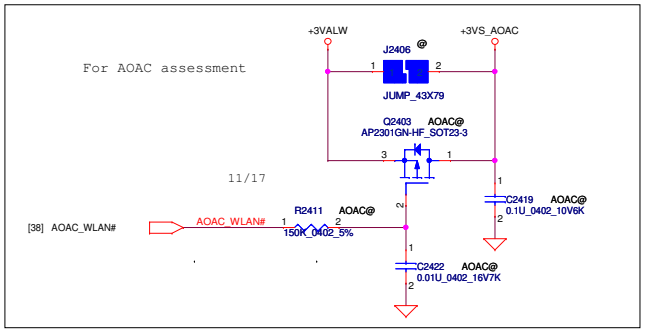
Mini-Express Card for WLAN/WiMAX(Half)

Mini-Express Card(WLAN/WiMAX)



NEW(apply compal PN)
159SBBA32010NNN





Need check WLAN/BT module OFF pin

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

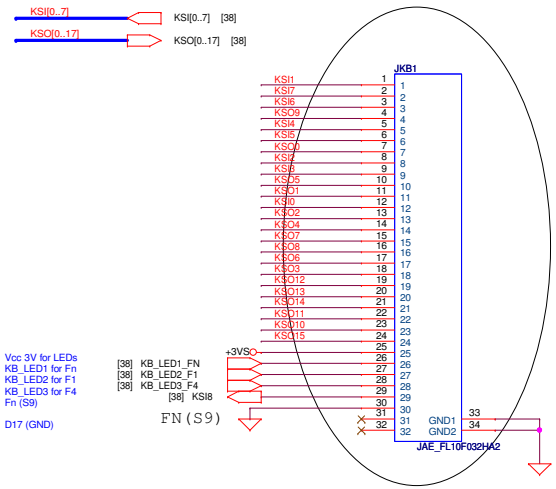
Compal Electronics, Inc.

Title: USB 3.0 Connector & WLAN

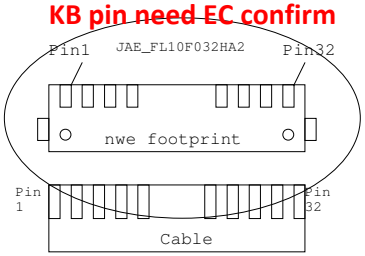
Size: Custom | Document Number: LA-9611P | Rev: 0.4

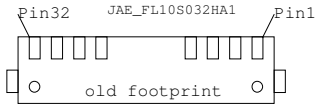
Date: Tuesday, February 26, 2013 | Sheet 35 of 53

INT_KBD Conn.



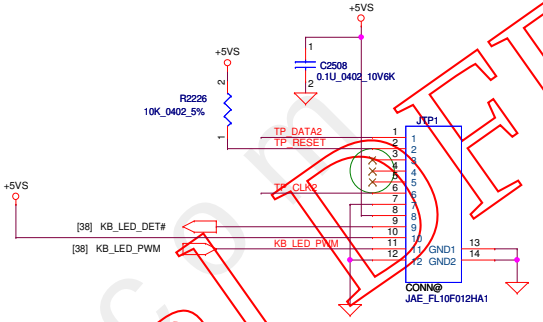
KB pin need EC confirm

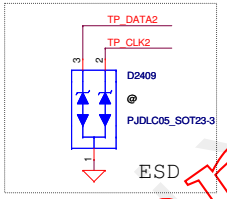




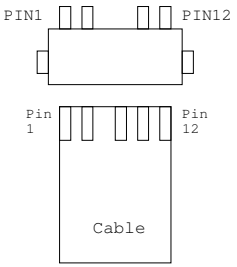
Track point

PN:SP01001CH00

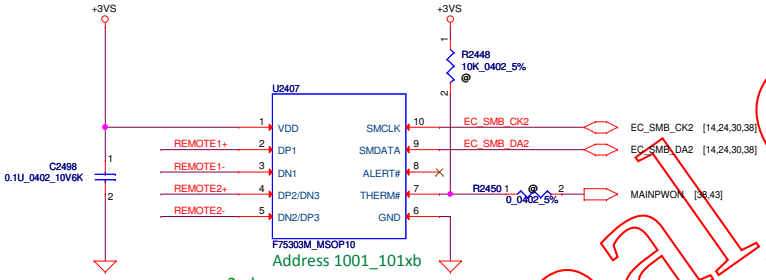




change footprint & PN check PIN1

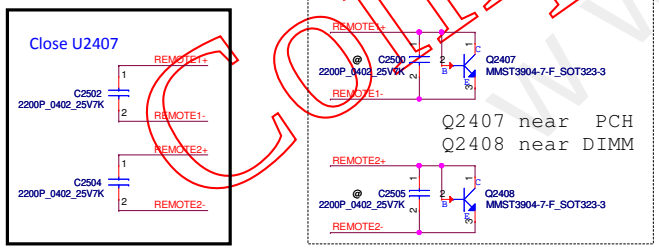


Fintek thermal sensor placed near CPU Core



Address 1001_101xb

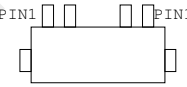
2nd source
SA000029210-->EMC1403-2-AIZL-TR

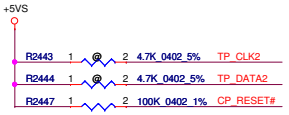


Q2407 near PCH
Q2408 near DIMM

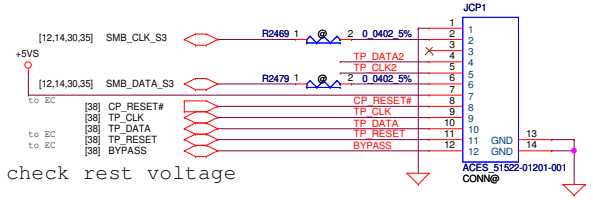
REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Click pad

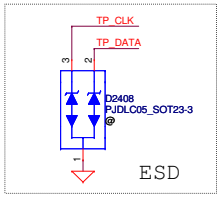




PN:XXXXXXXX



check rest voltage



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

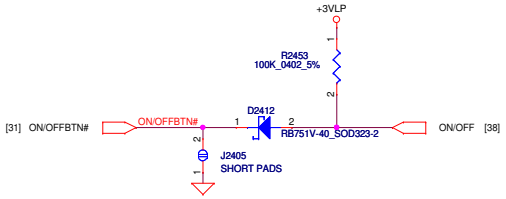
Compal Electronics, Inc.

Title: KB/CP/TP/FP/Thermal Sensor

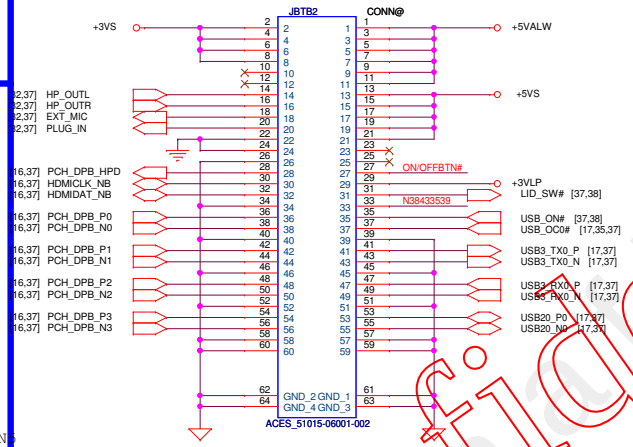
Size: Custom | Document Number: LA-9611P | Rev: 0.4

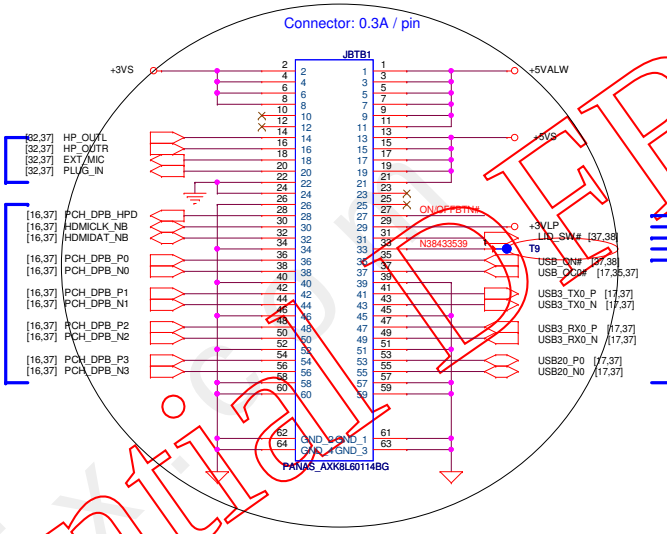
Date: Tuesday, February 26, 2013 | Sheet 36 of 53

Power Button



I/O Board CONN.





Audio combo Jack

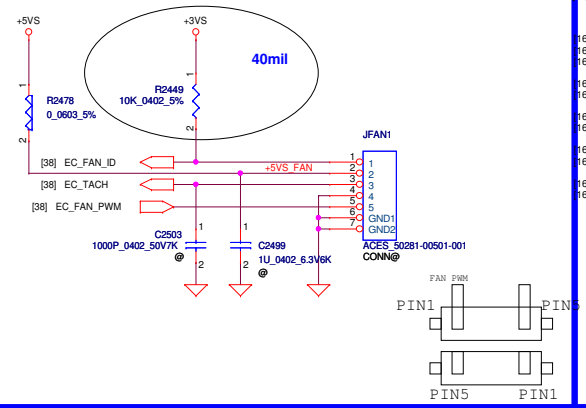
HDMI

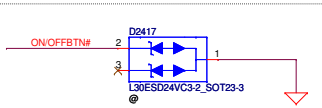
Power Button

Lid Switch & LED

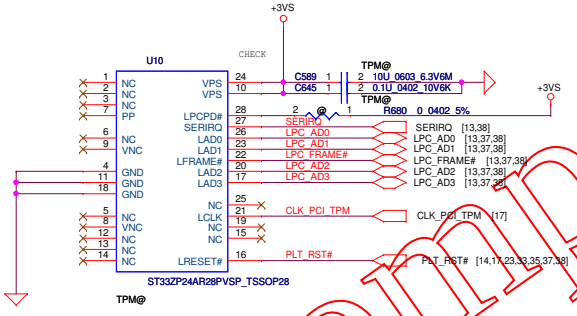
to EC

USB3.0

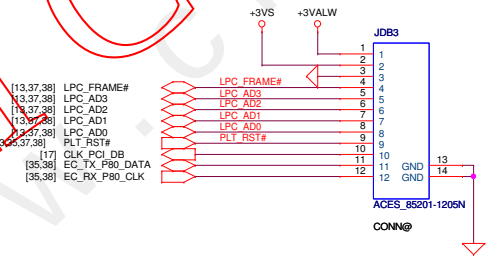




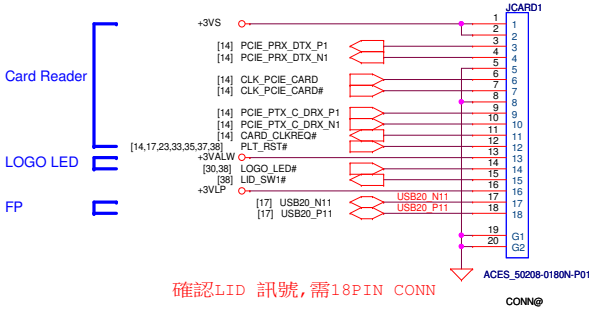
TPM



Debug Conn.



Card Reader CONN.



確認LID 訊號,需18PIN CONN

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

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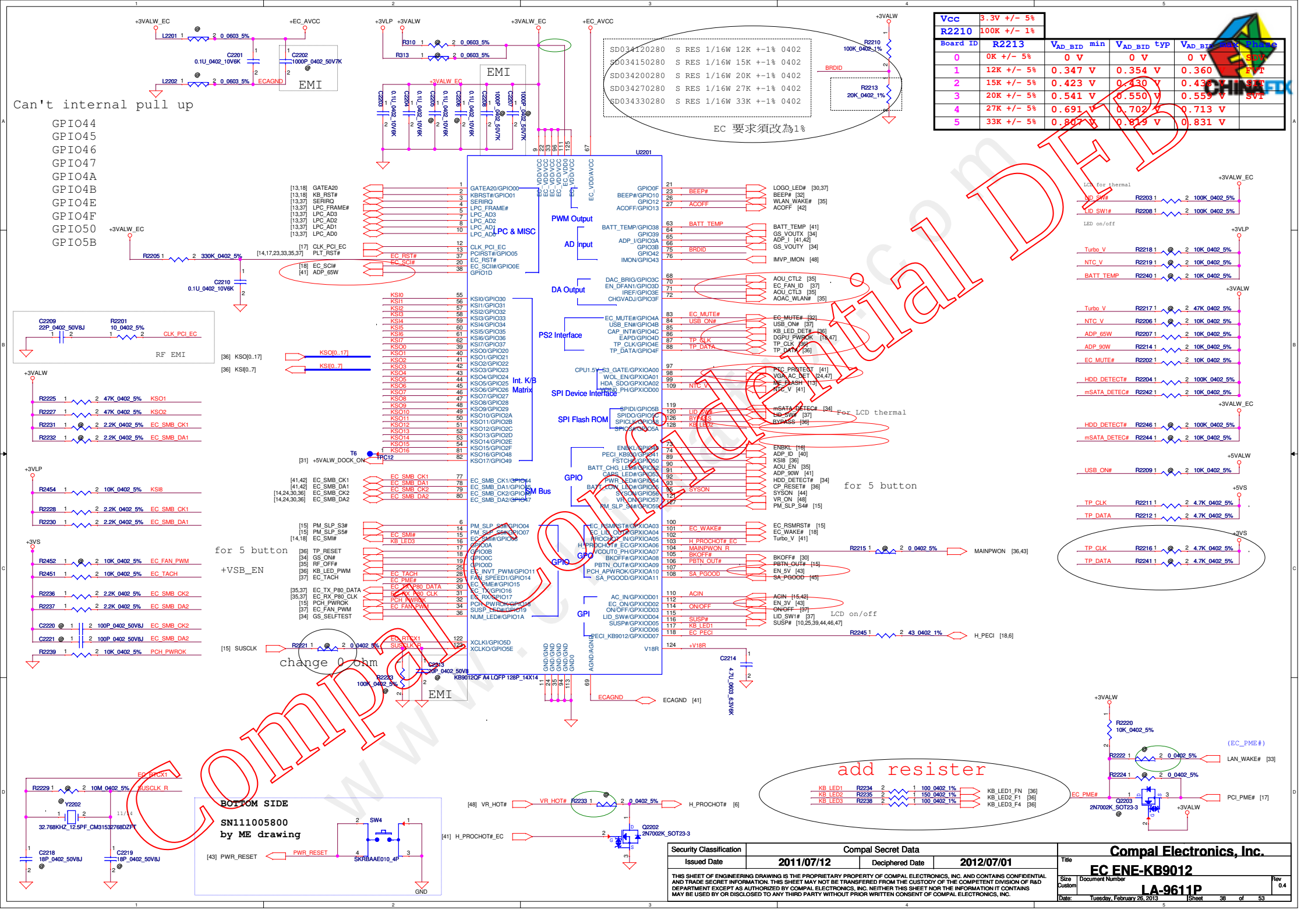
Compal Electronics, Inc.	
Title	PBTN/FAN/TPM/RTC/IO Board
Size: Custom	Document Number: LA-9611P
Rev	0.4
Date: Tuesday, February 26, 2013	Sheet 37 of 53



Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	12K +/- 5%	0.347 V	0.354 V	0.360	EVT
2	15K +/- 5%	0.423 V	0.430 V	0.436	SVT
3	20K +/- 5%	0.541 V	0.550 V	0.559 V	SVT
4	27K +/- 5%	0.691 V	0.702 V	0.713 V	
5	33K +/- 5%	0.807 V	0.819 V	0.831 V	

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

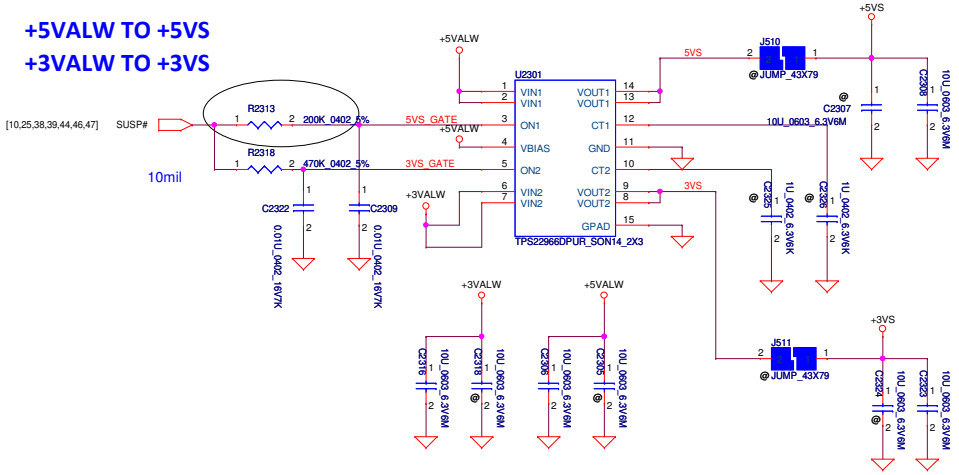
Compal Electronics, Inc.

Title: EC ENE-KB9012

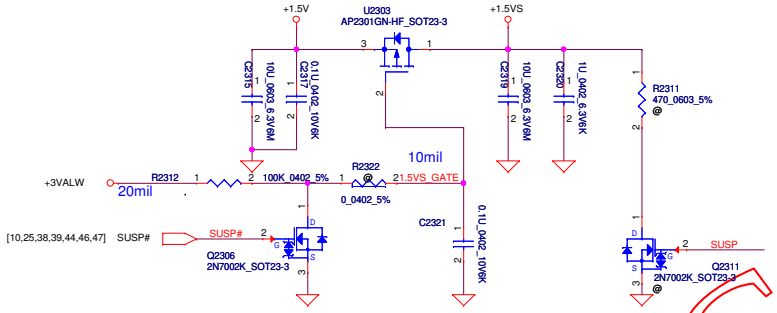
Size: Custom | Document Number: LA-9611P | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 38 of 53

+5VALW TO +5VS
+3VALW TO +3VS

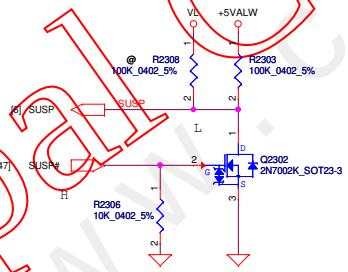


+1.5V to +1.5VS

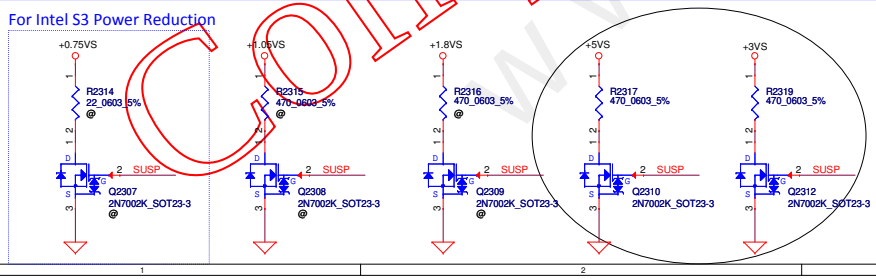


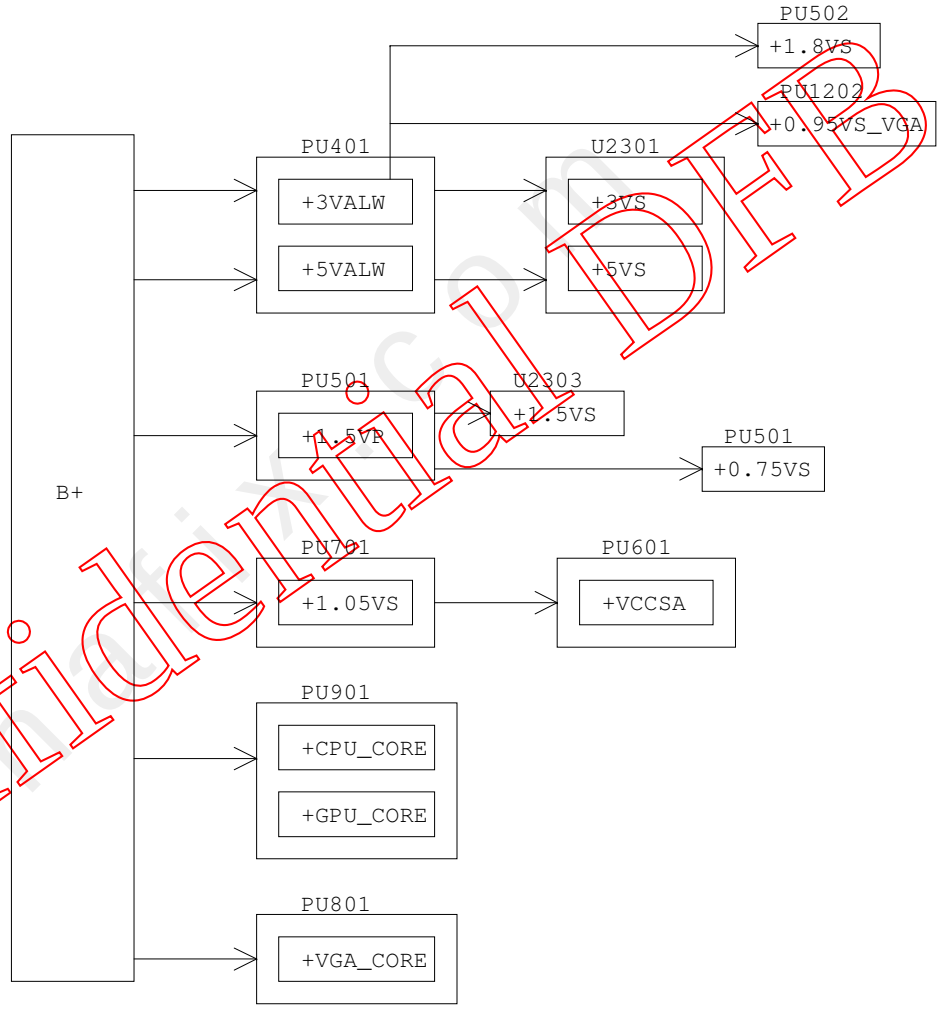
+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3



For Intel S3 Power Reduction





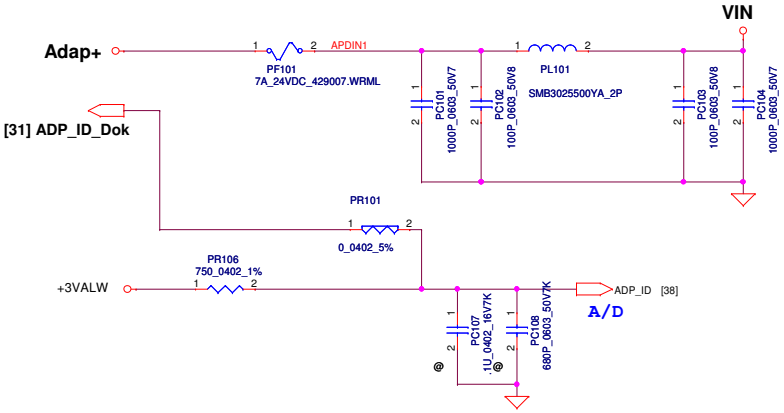
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **DC Interface**

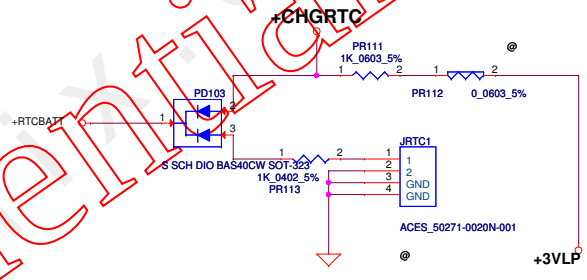
Size: Custom | Document Number: **LA-9611P** | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 39 of 53



ADP_ID

AC Adapter	45W	65W	90W	135W
R(ohm)	118	287	549	1000
ADP_ID(V)	0.449	0.913	1.395	1.886
Detection -Voltage(V)	<=0.663, >0.234	<=1.134, >0.693	<=1.618, >1.172	<=2.109, >1.663



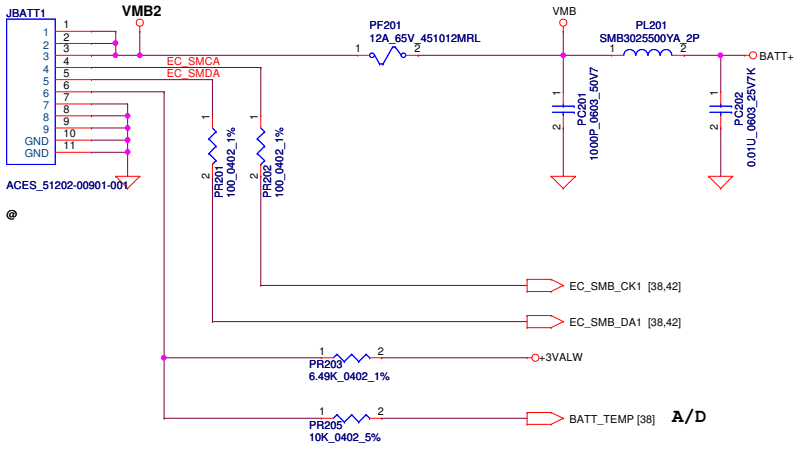
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: ***PWR DCIN***

Size	Document Number	Rev
Custom	VIUS1	0.4

Date: Tuesday, February 26, 2013 | Sheet 40 of 53



Rsistance between Turbo_V and ECAGND:

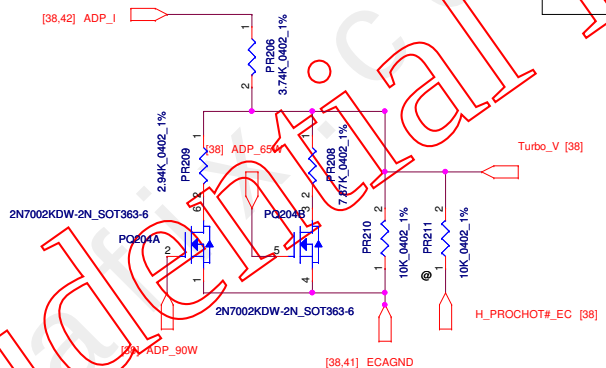
45 W: 10K (Default)
65 W: 4.4K (ADP_65W to High,ADP_90W to Low)
90 W: 2.27K (ADP_90W to High,ADP_65W to Low)

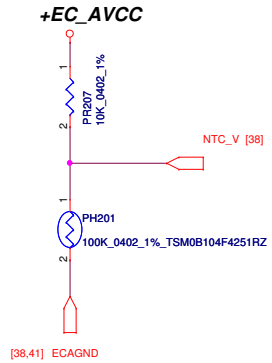
Trigger Power:

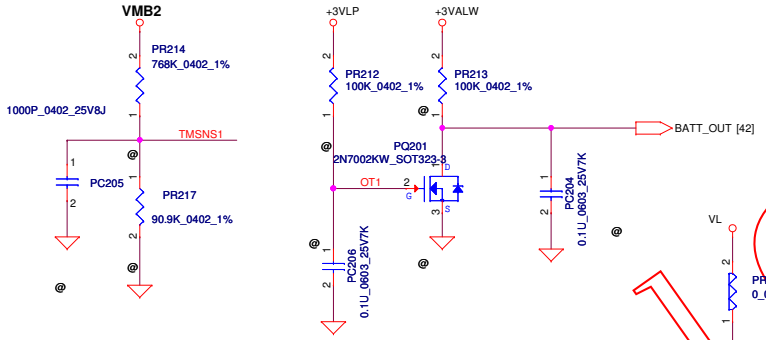
45 W → 55 W → ADP_I:1.65
65 W → 74 W → ADP_I:2.22
90 W → 106 W → ADP_I:3.18

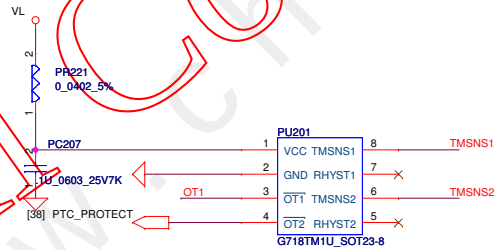
PH201 under CPU botten side :

CPU thermal protection at 100 degree C





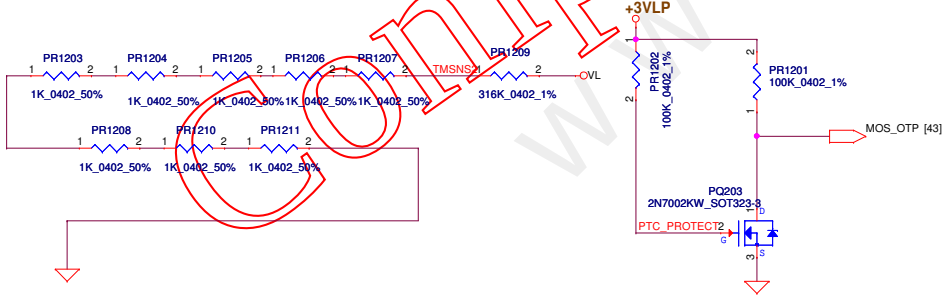




PH201:

Temp.	Rman.	Rnor.	Rmin. (Kohm)
93	7.3419	7.0792	6.8253

Posestor

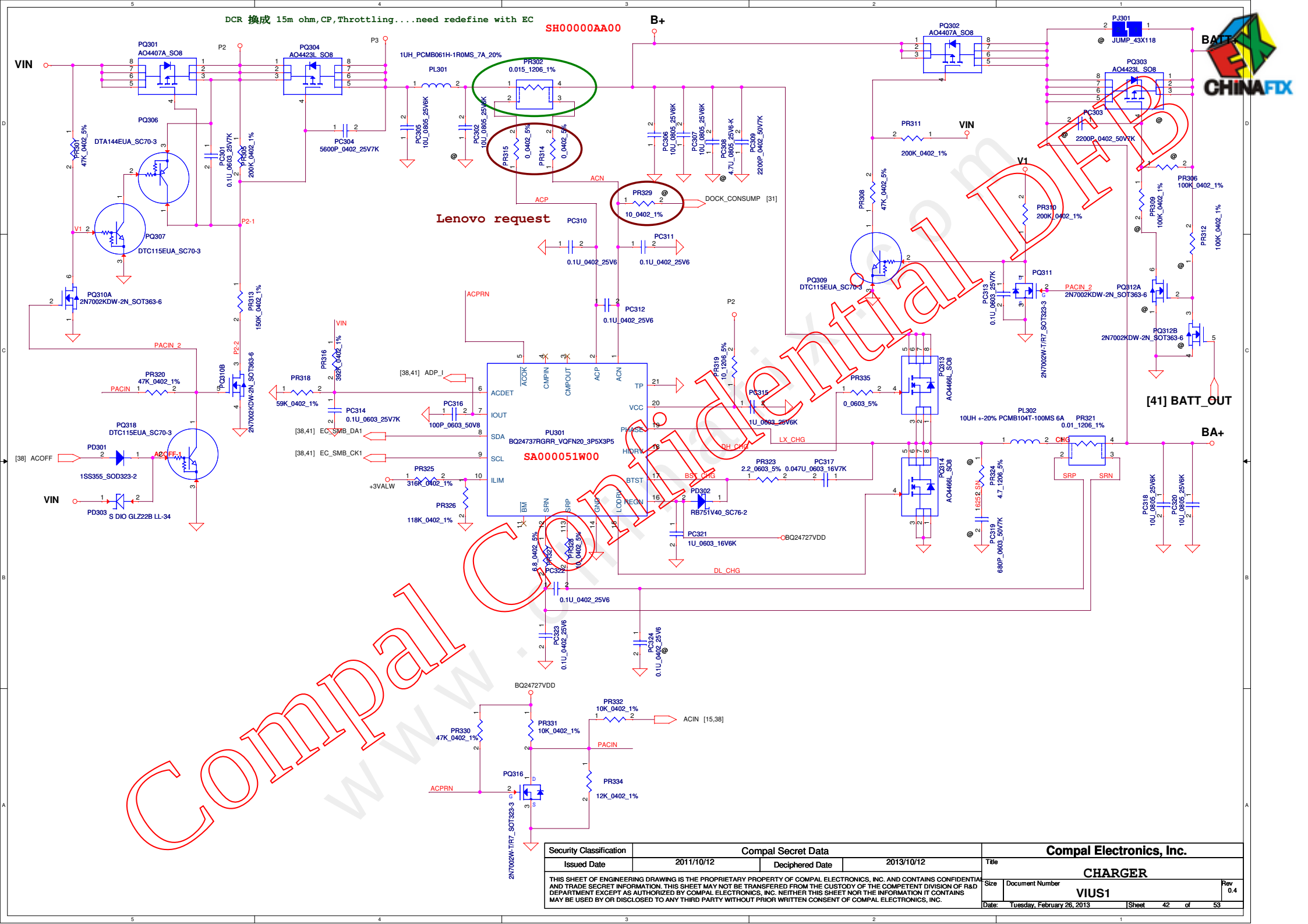


MOS_OTP:
Default:High
Active :Low

PTC_PROTECT:
Default:Low
Active :High

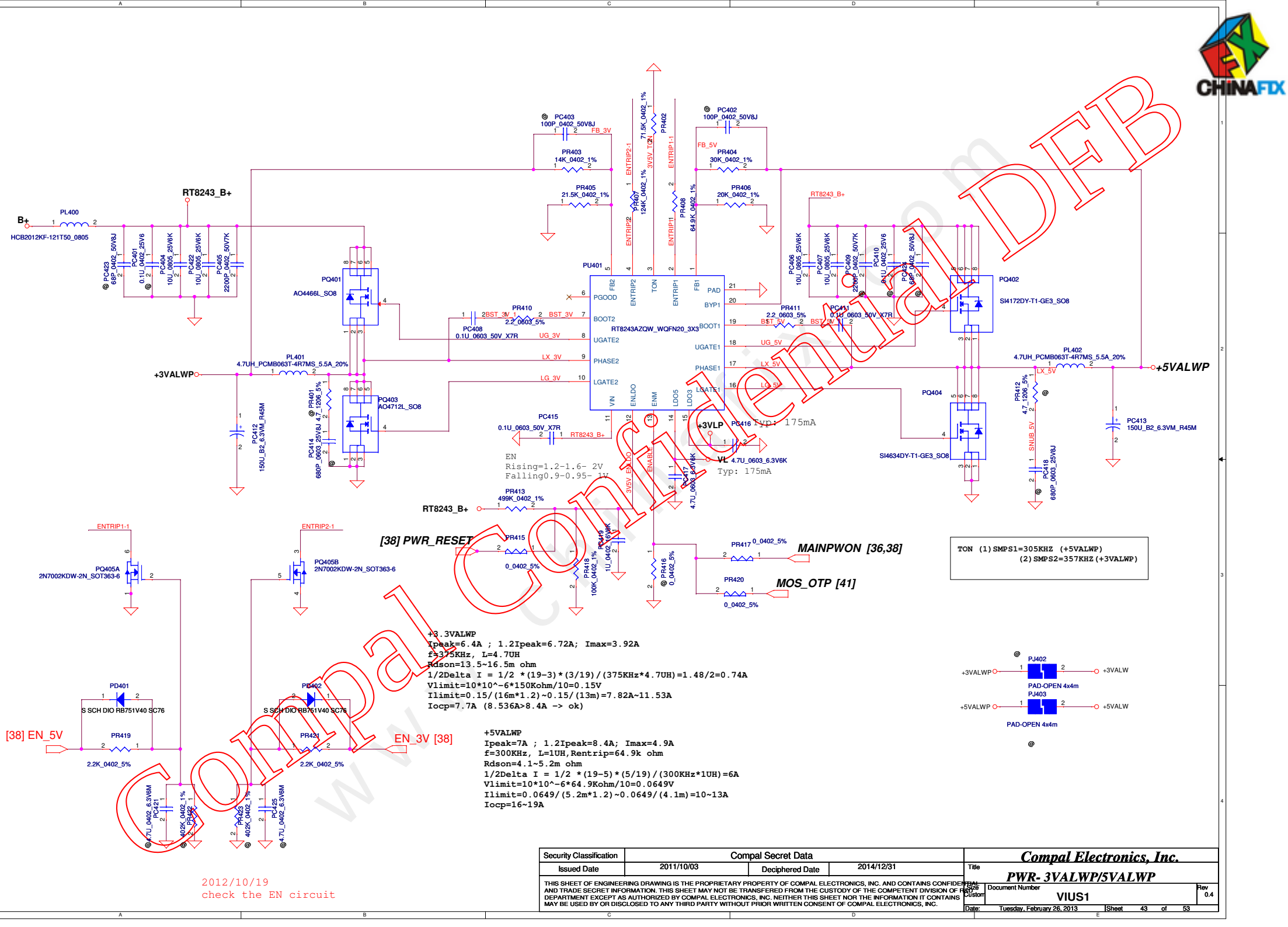
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Title	Compal Electronics, Inc.		
	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: VIUS1		Rev: 0.4
Date: Tuesday, February 26, 2013	Sheet 41 of 53		



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	CHARGER		
Size	Document Number	VIUS1	Rev 0.4
Date: Tuesday, February 26, 2013	Sheet 42 of 53		



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

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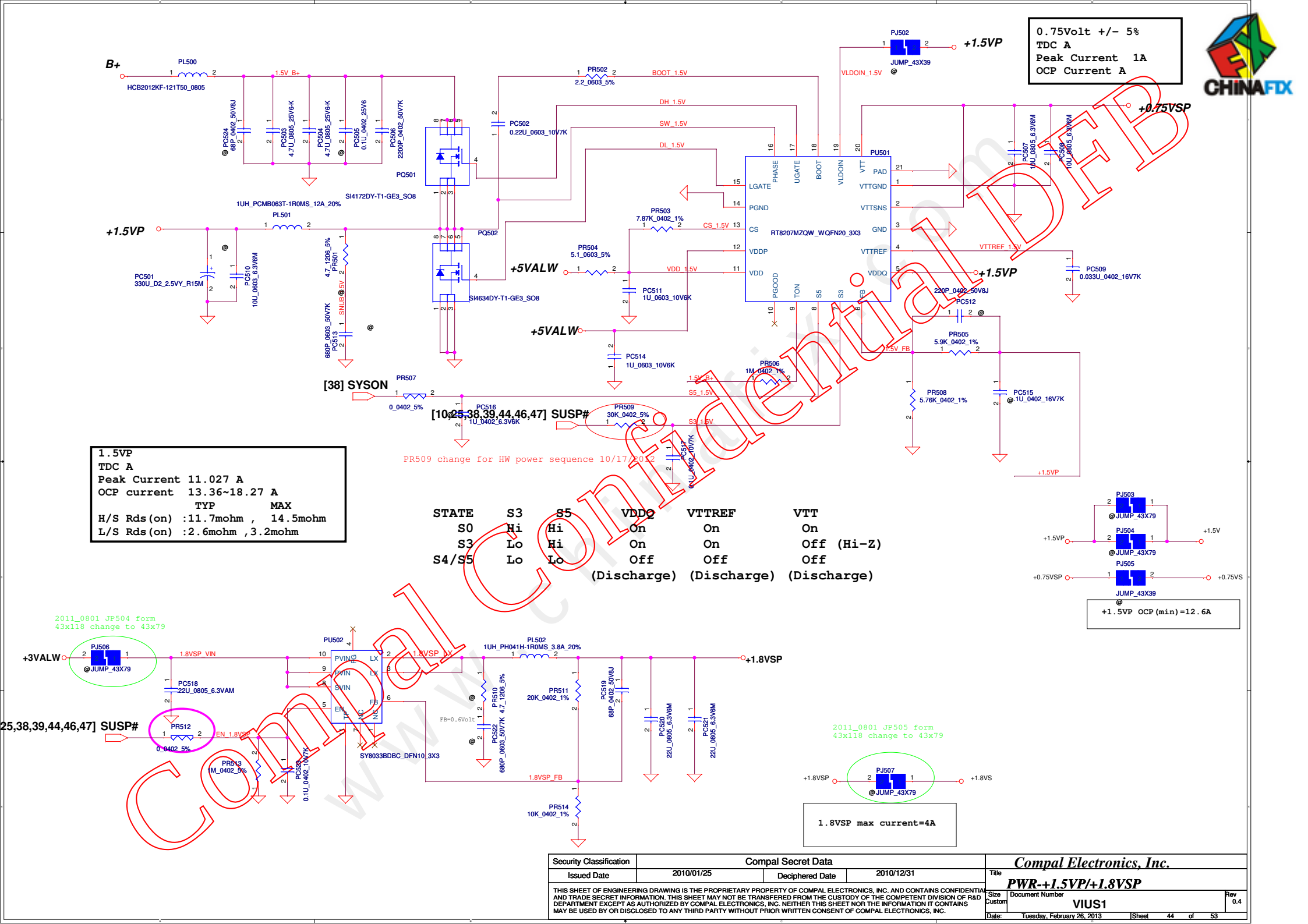
Compal Electronics, Inc.			
Title	PWR- 3VALWP/5VALWP		
Size	Document Number	VIUS1	Rev 0.4
Custom			
Date: Tuesday, February 26, 2013	Sheet 43 of 53		


0.75Volt +/- 5%
TDC A
Peak Current 1A
OCP Current A
B+
PL500
HCB2012KF-121T50_0805
1.5V_B+
PR502
2.2_0603_5%
BOOT_1.5V
DH_1.5V
SW_1.5V
DL_1.5V
PC502
0.22U_0603_10V7K
PQ501
SI4172DY-T1-GE3_SO8
PQ502
SI4634DY-T1-GE3_SO8
1UH_PCMB063T-1R0MS_12A_20%
PL501
+1.5VP
PC501
330U_D2_2.5VY_R15M
PC510
10U_0603_6.3V6M
4.7_1206_5%
PR501
SNUB@5V
680P_0603_50V7K
PC513
PJ502
JUMP_43X39
VLDOIN_1.5V
+0.75VSP
PU501
RT8207MZQW_WQFN20_3X3
LGATE
PHASE
UGATE
BOOT
VLDOIN
VTT
PAD
VTTGND
VTTSNS
PGND
CS
GND
VDDP
VTTREF
VDD
VDDQ
PGOOD
TON
S5
S3
FB
PR503
7.87K_0402_1%
CS_1.5V
PR504
5.1_0603_5%
VDD_1.5V
PC511
1U_0603_10V6K
+5VALW
PC514
1U_0603_10V6K
PC507
10U_0805_6.3V6M
PC508
10U_0805_6.3V6M
VTTREF_1.5V
PC509
0.033U_0402_16V7K
220P_0402_50V8J
PC512
PR505
5.9K_0402_1%
1.5V_FB
PR506
1M_0402_1%
PR508
5.76K_0402_1%
PC515
@.1U_0402_16V7K
[38] SYSON
PR507
0_0402_5%
PC516
1U_0402_6.3V6K
[10,25,38,39,44,46,47] SUSP#
PR509
30K_0402_5%
S5_1.5V
S3_1.5V
PR509 change for HW power sequence 10/17/2012
PC517
0.1U_0402_10V7K
1.5VP
TDC A
Peak Current 11.027 A
OCP current 13.36~18.27 A
TYP MAX
H/S Rds(on) :11.7mohm , 14.5mohm
L/S Rds(on) :2.6mohm ,3.2mohm
STATE S3 S5 VDDQ VTTREF VTT
S0 Hi Hi On On On
S3 Lo Hi On On Off (Hi-Z)
S4/S5 Lo Lo Off Off Off
(Discharge) (Discharge) (Discharge)
PJ503
@JUMP_43X79
PJ504
@JUMP_43X79
PJ505
JUMP_43X39
+1.5VP OCP(min)=12.6A
2011_0801 JP504 form
43x118 change to 43x79
+3VALW
PJ506
@JUMP_43X79
1.8VSP_VIN
PU502
PVIN
SVIN
LX
FB
EN
NC
SY8033BDBC_DFN10_3X3
1.8VSP_LX
PL502
1UH_PH041H-1R0MS_3.8A_20%
+1.8VSP
PR510
4.7_1206_5%
FB=0.6Volt
PC522
680P_0603_50V7K
PR511
20K_0402_1%
PC519
68P_0402_50V8J
PC520
22U_0805_6.3V6M
PC521
22U_0805_6.3V6M
[25,38,39,44,46,47] SUSP#
PR512
0_0402_5%
EN_1.8VSP
PR513
1M_0402_5%
PC523
0.1U_0402_10V7K
1.8VSP_FB
PR514
10K_0402_1%
2011_0801 JP505 form
43x118 change to 43x79
PJ507
@JUMP_43X79
1.8VSP max current=4A
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www.chinafix.com
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2010/12/31
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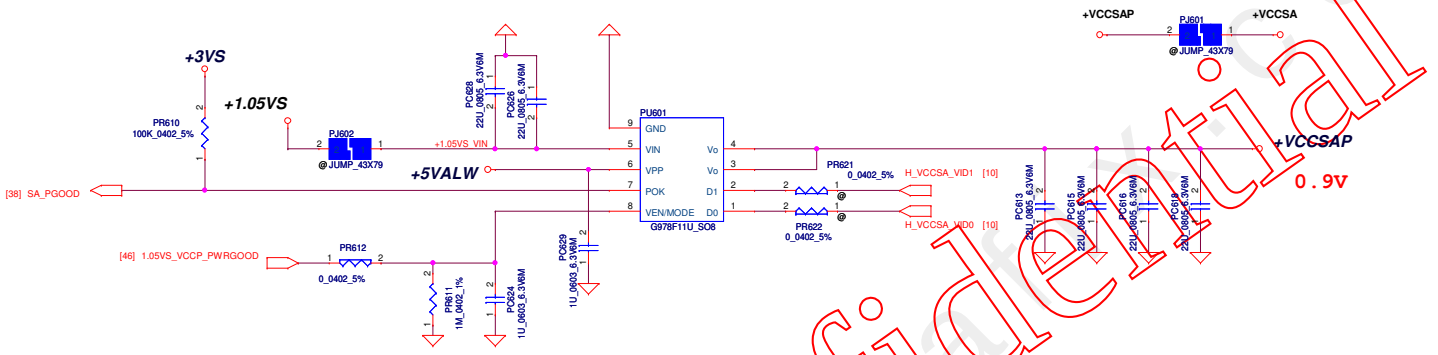
Compal Electronics, Inc.
Title
PWR-+1.5VP/+1.8VSP
Size
Custom
Document Number
VIUS1
Rev
0.4
Date:
Tuesday, February 26, 2013
Sheet
44
of
53

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 2.9A
Peak Current 4A
OCP current 5.4A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	VIUS1	0.4

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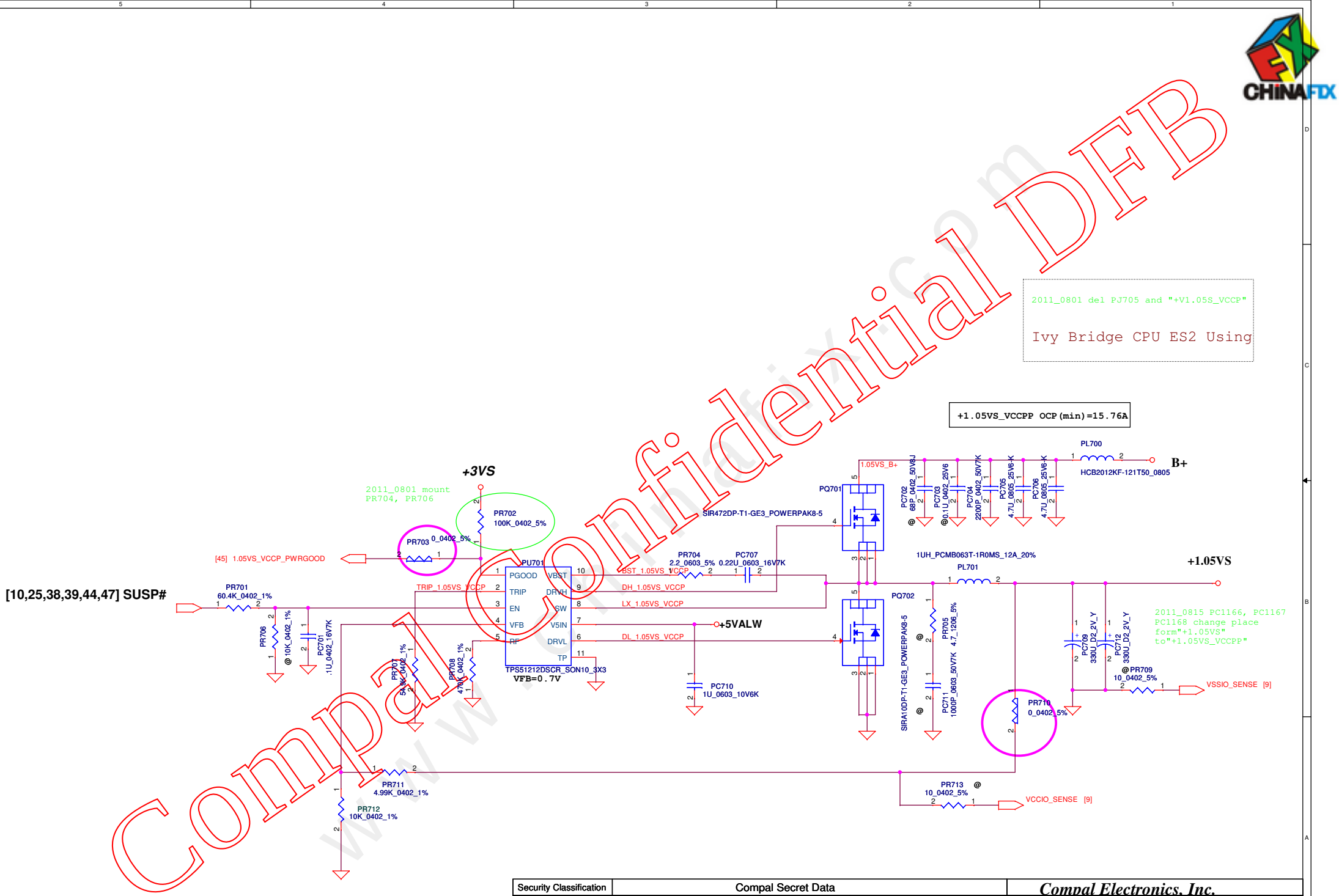

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR +1.05VS_VCCPP			
Size: Custom	Document Number: VIUS1		Rev: 0.4
Date: Tuesday, February 26, 2013		Sheet 46 of 53	

GPI021	GPI029	GPI030	GPI020	GPI015	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	0	0	1.200V
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V Default
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

+VGA_CORE Near VGA Core

ISEN1_VGA是否要加

ISEN2_VGA是否要加

Layout Note:
Place near Phase1 Choke

Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

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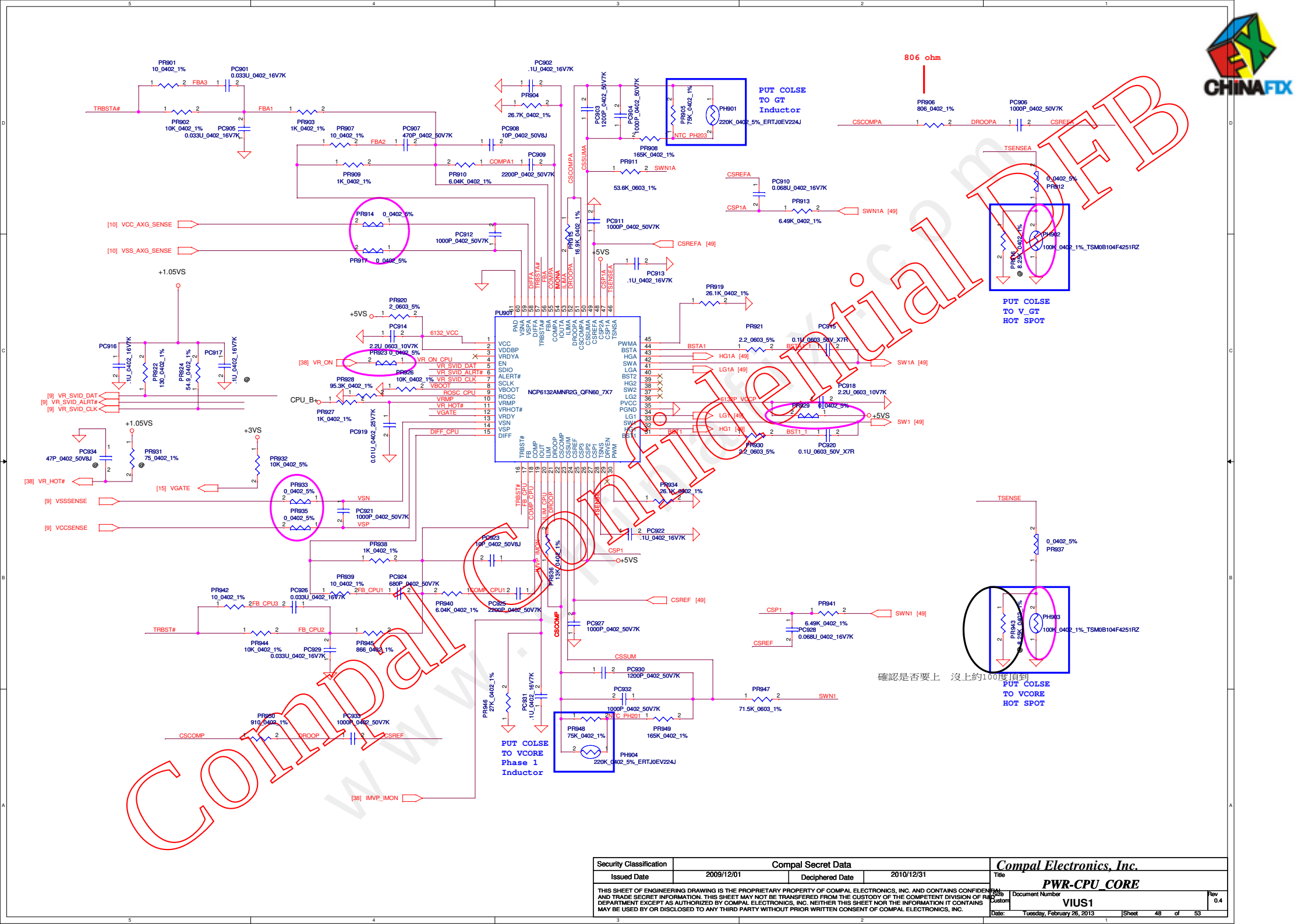
Compal Electronics, Inc.

Title: VGA_COREP

Size: | Document Number: VIUS1 | Rev: 0.4

Date: Tuesday, February 26, 2013 | Sheet 47 of 53



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: ***PWR-CPU_CORE***

Size	Document Number	Rev
Custom	VIUS1	0.4

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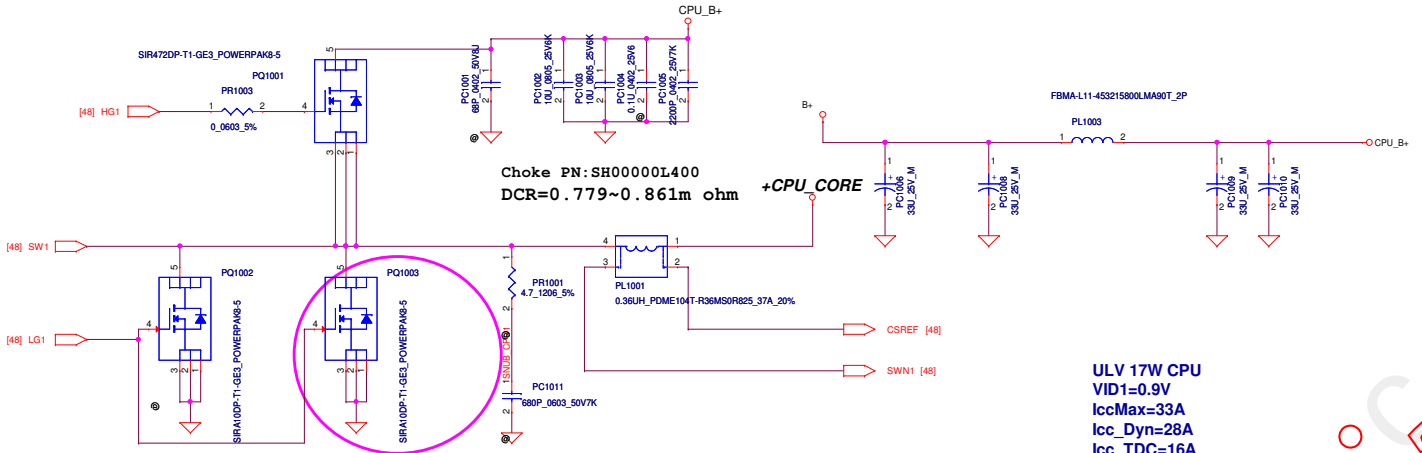
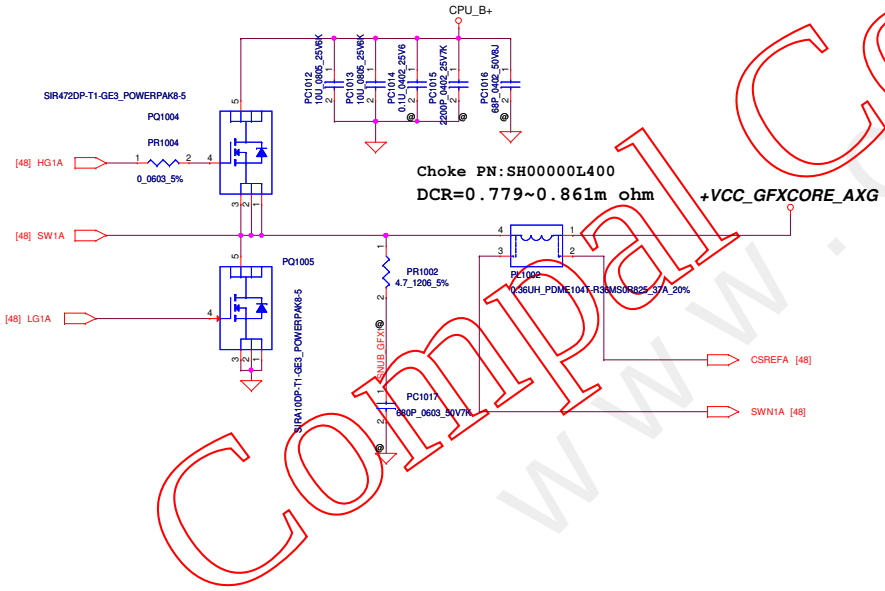


ULV 17W CPU
VID1=0.9V
IccMax=33A
Icc_Dyn=28A
Icc_TDC=16A
R_LL=2.9m ohm



ULV GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
Custom	VIUS1	0.4

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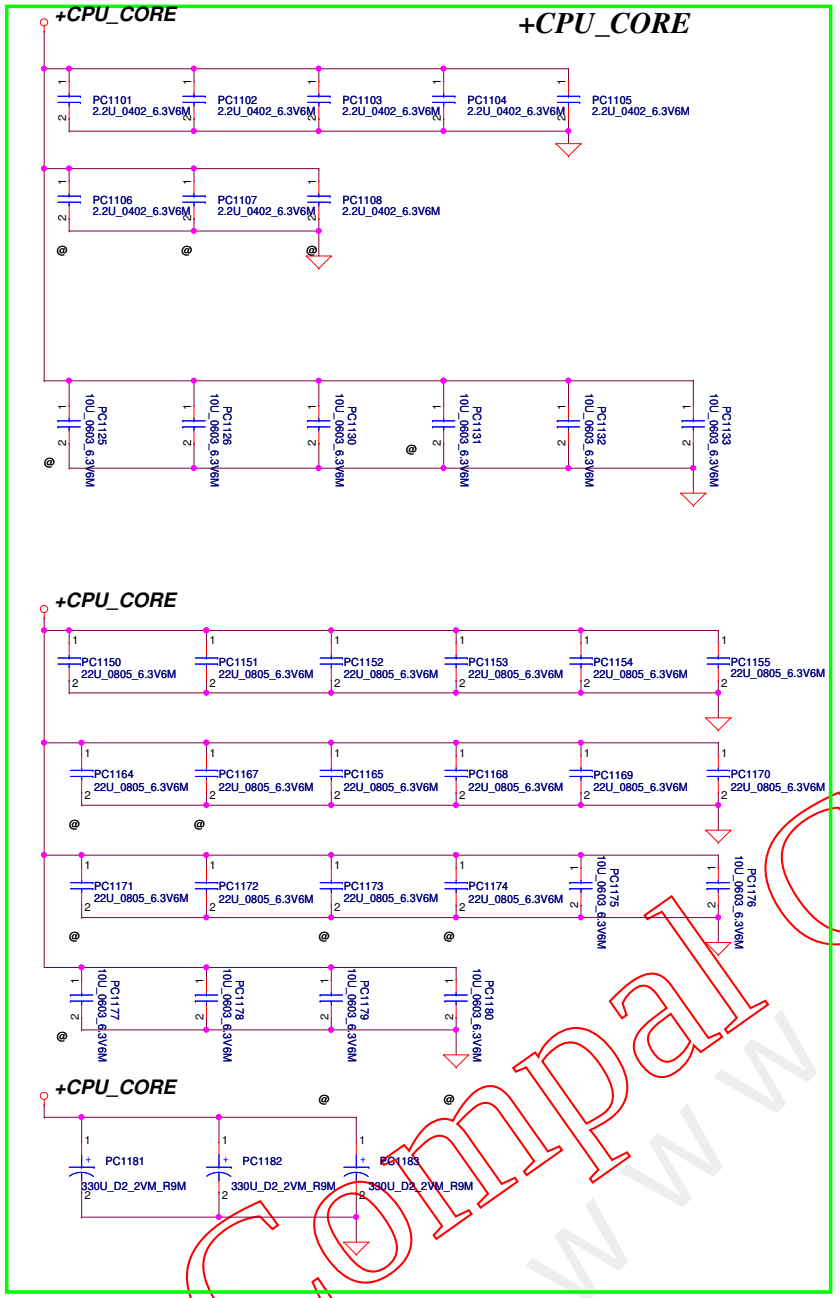
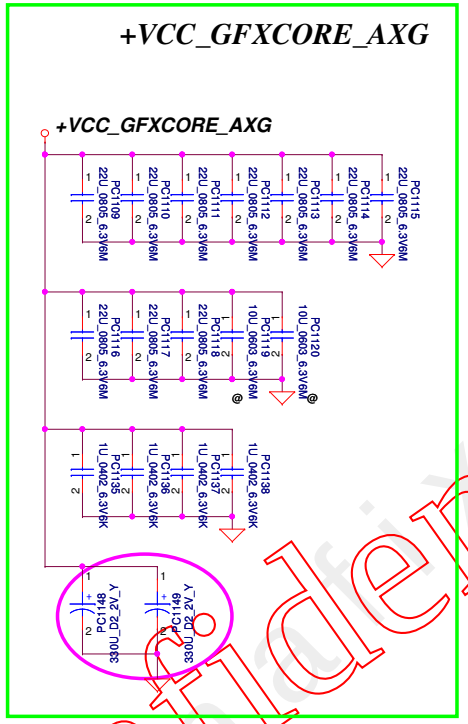
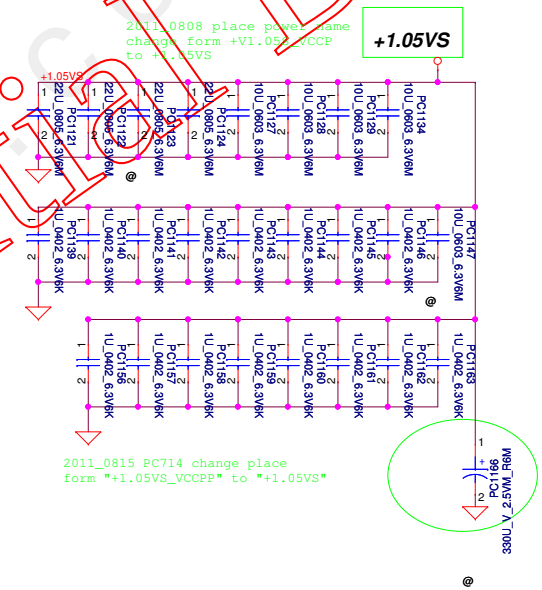






Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

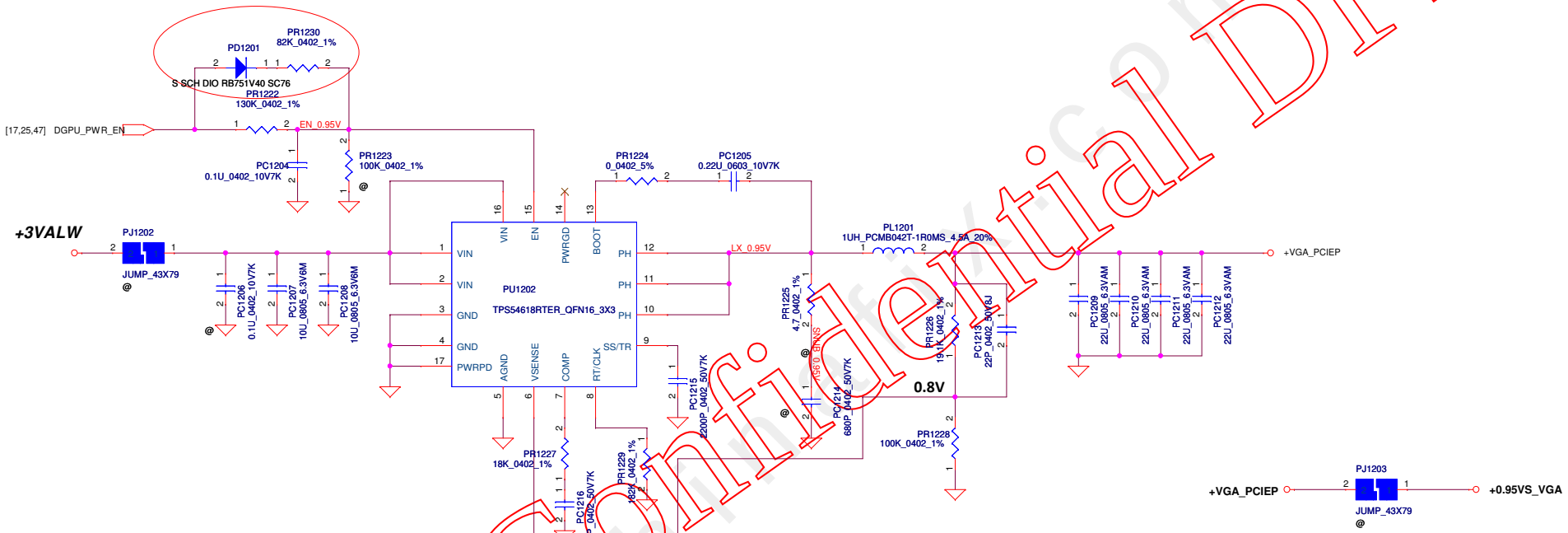
Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	VIUS1	0.4

Date: Tuesday, February 26, 2013 Sheet 50 of 53

PR1230,PD1201 add for HW power sequence required 10/31/2012



Security Classification	Compal Secret Data		
Issued Date	2011/07/01	Deciphered Date	2012/07/01

Compal Electronics, Inc.			
Title	PWR-PROSESTOR		
Size: Custom	Document Number: VIUS1		Rev: 0.4
Date: Tuesday, February 26, 2013	Sheet 51 of 53		

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1				2012/06/05	
2				2012/06/08	
3				2012/06/08	
4				2012/06/08	
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2009/01/06

Compal Electronics, Inc.

Title	PIR (PWR)	
Size: Custom	Document Number: VIUS1	Rev: 0.4
Date: Tuesday, February 26, 2013	Sheet 52 of 53	

Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Title	PIR (EE)		
Size: Custom	Document Number: LA-8133P		Rev: 0.4
Date: Tuesday, February 26, 2013	Sheet 53 of 53		