ZZZ8
DAZ@
DAZ04300100
PCB

ZZZ1
DA2@
MAIN BOARD
DA600007E10
PCB

ZZZ2
DA2@
E board
DA40000A910
PCB

ZZZ3
DA2@
FP board
DA600007D10
PCB

ZZZ4
DA2@
Function board
DA40000AA10
PCB

ZZZ5
DA2@
USB board
DA40000AB10
PCB

ZZZ6
DA2@
IO board
DA40000AC10
PCB

ZZZ7
DA2@
Power board
DA40000AD10
PCB

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JAT10 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-04-07

REV:1.0

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Custom	401556	B

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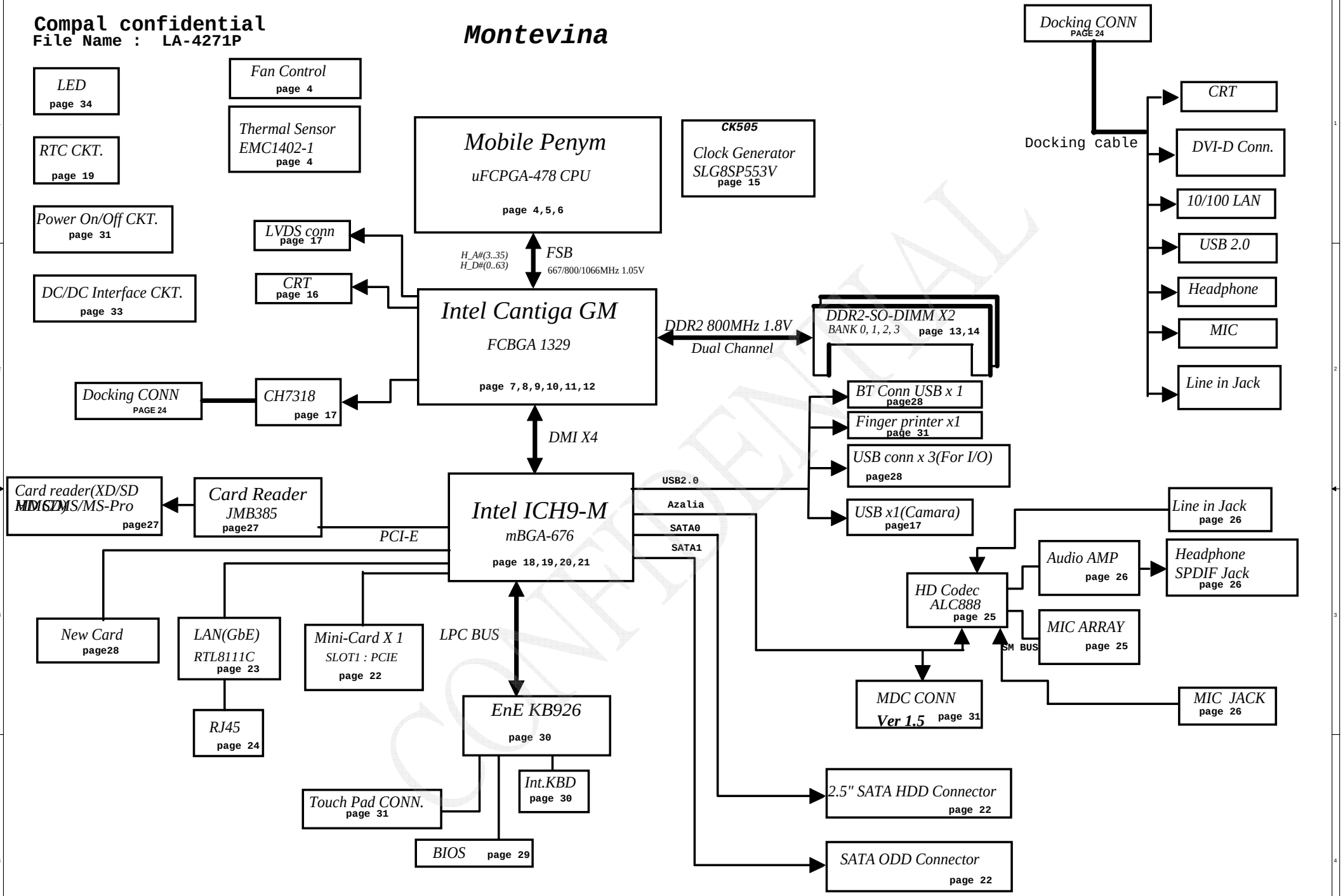
Compal confidential
File Name : LA-4271P

Montevina



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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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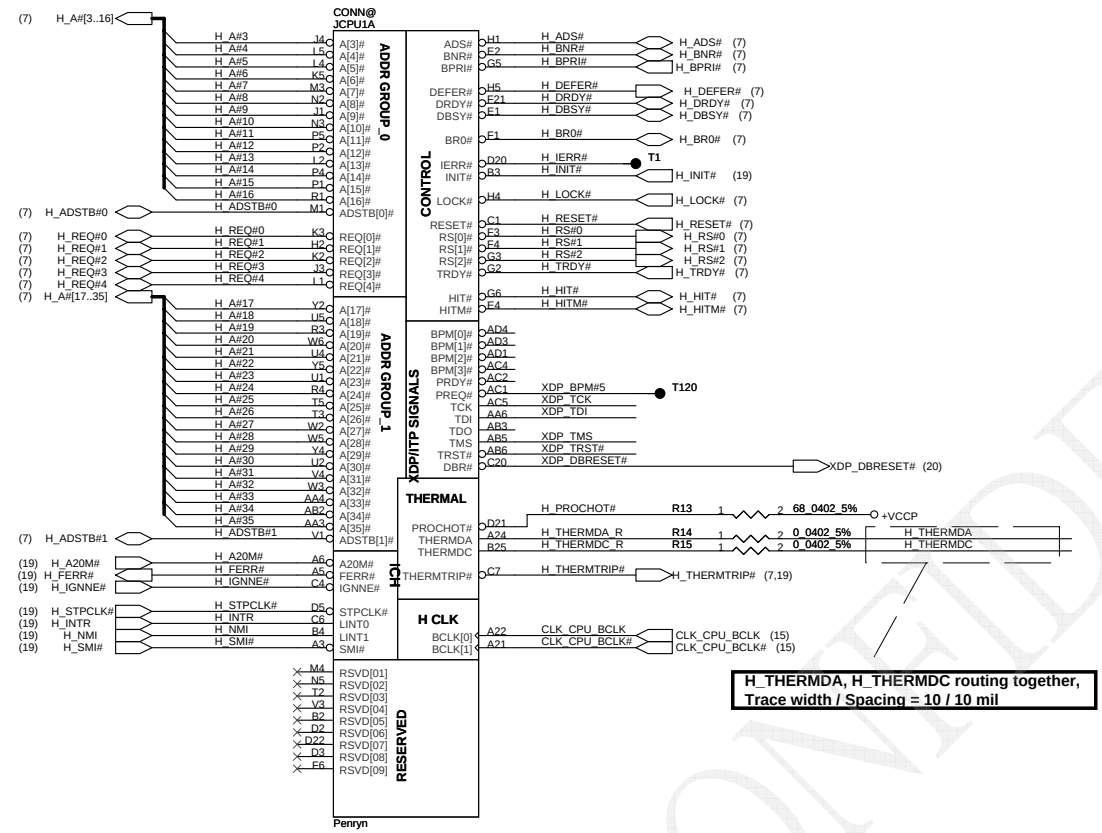
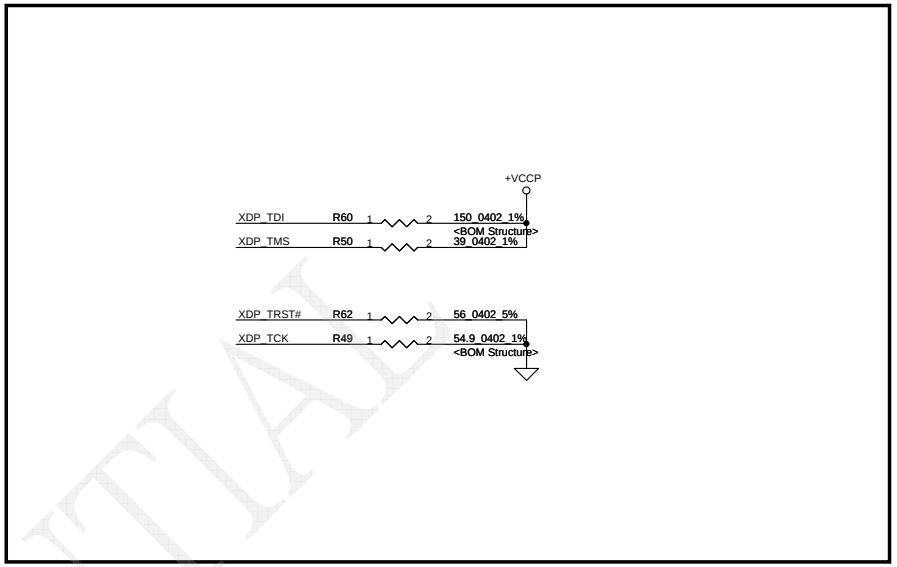
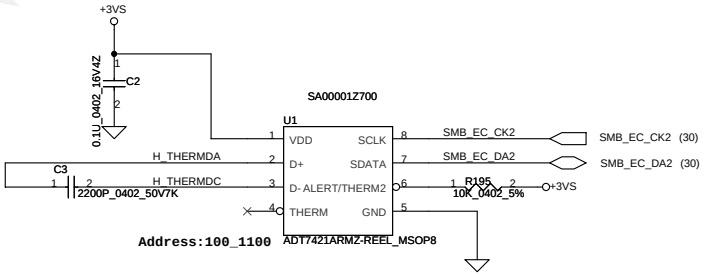
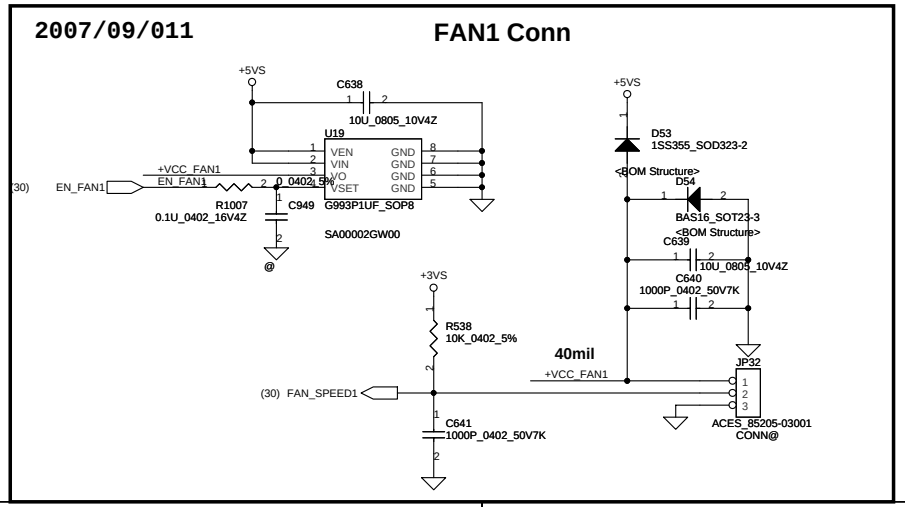
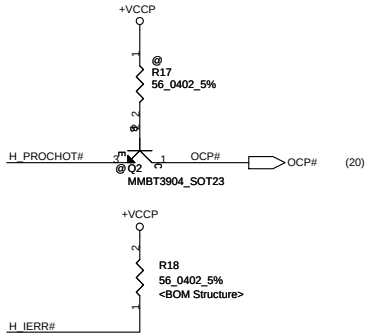


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil









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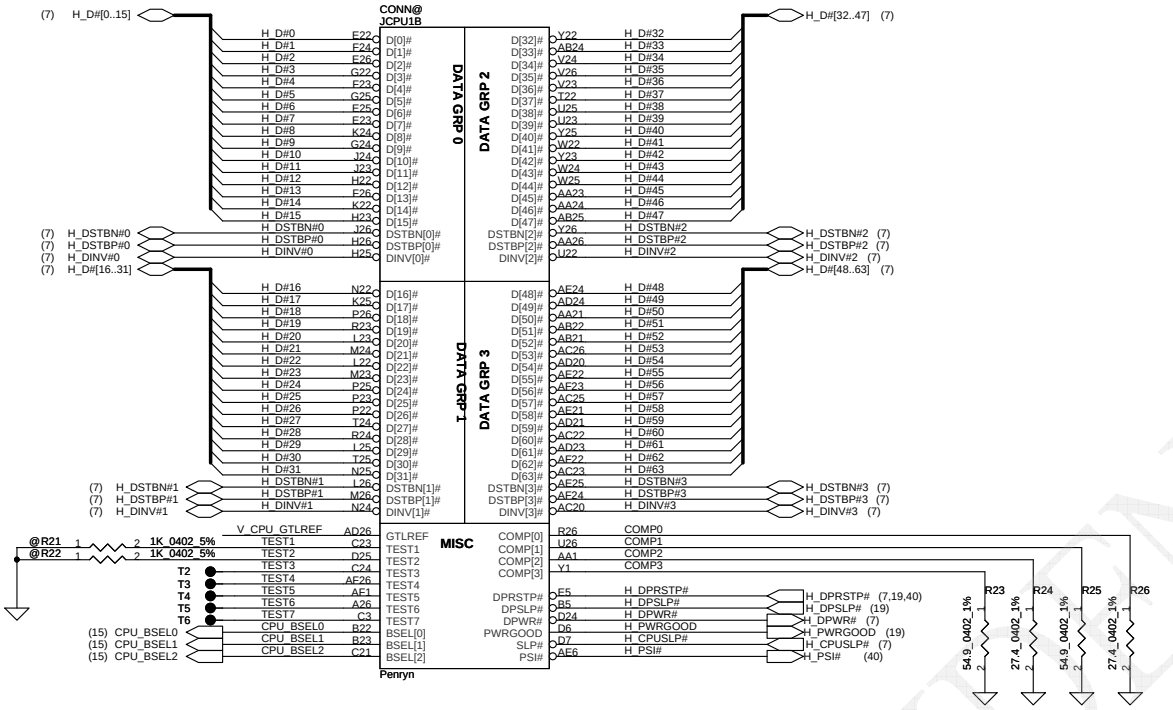
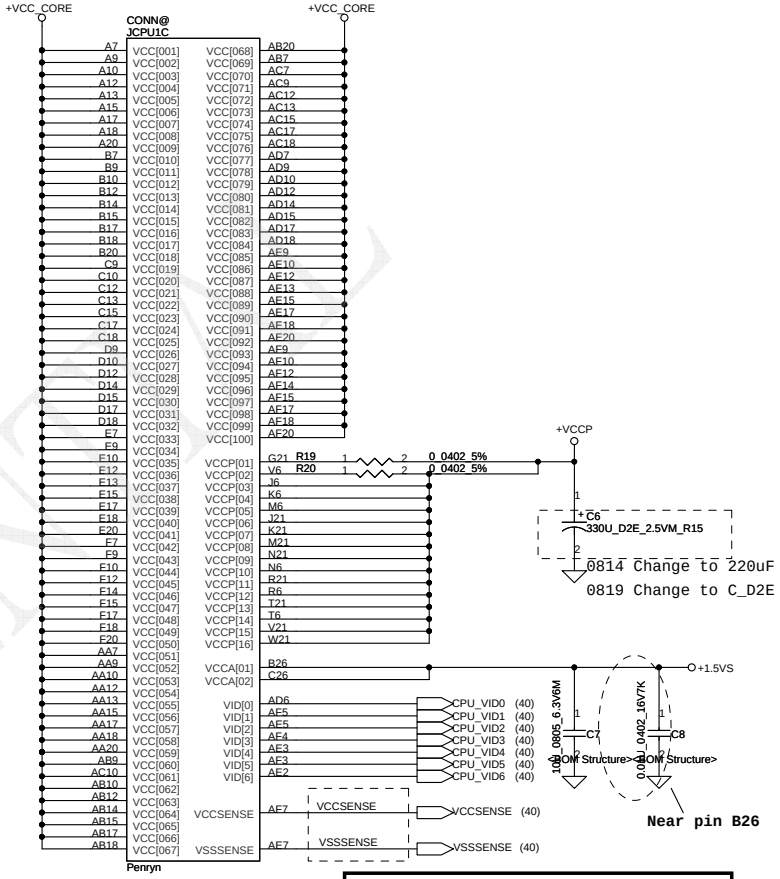


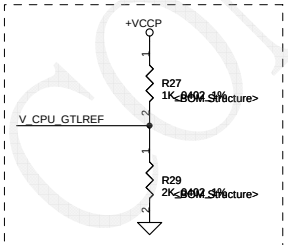
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

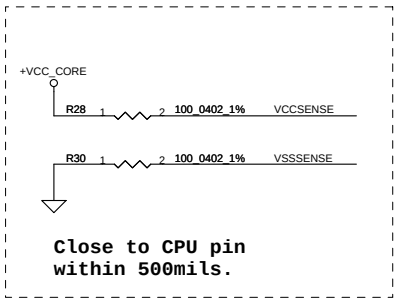
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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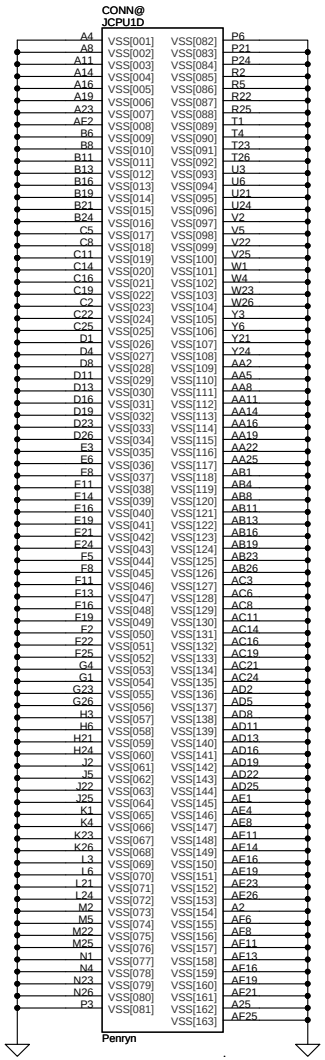
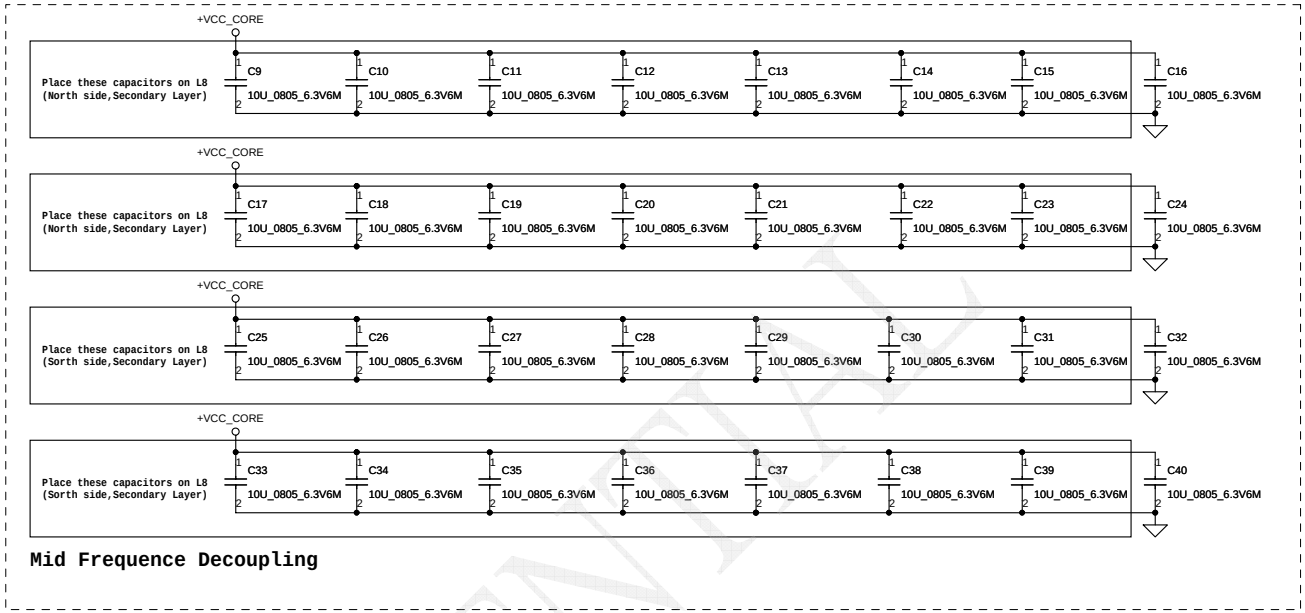
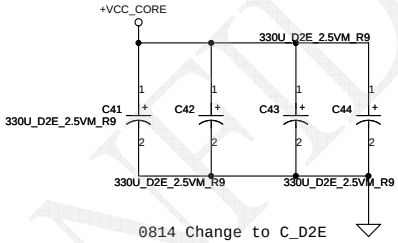


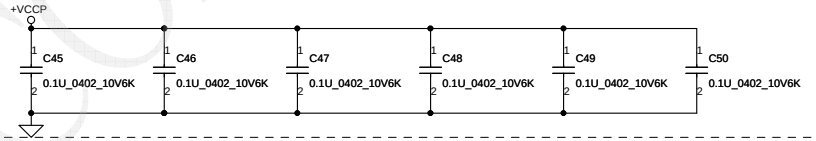


Mid Frequence Decoupling



0814 Change to C_D2E

Place these inside socket cavity on L8 (North side Secondary)



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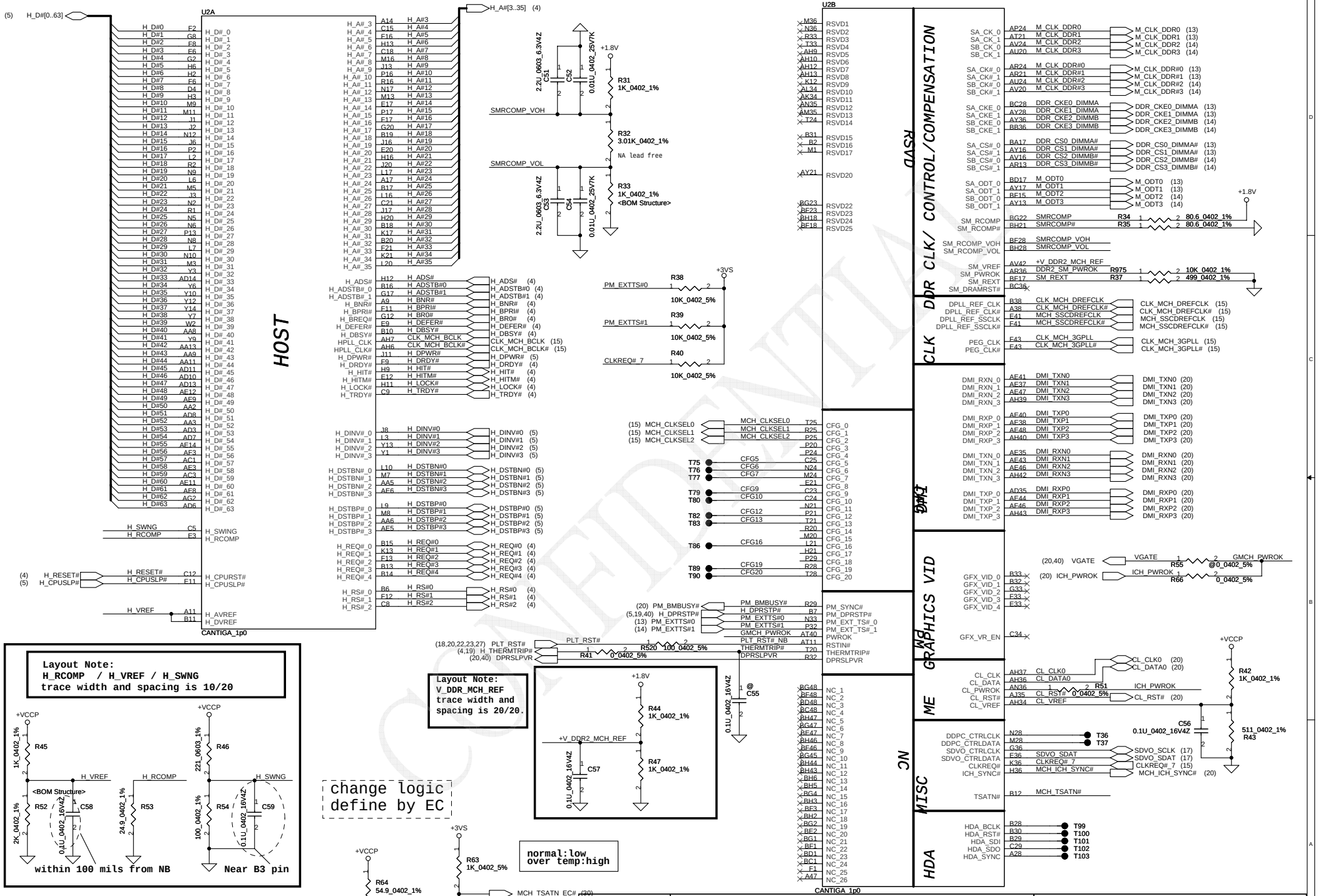

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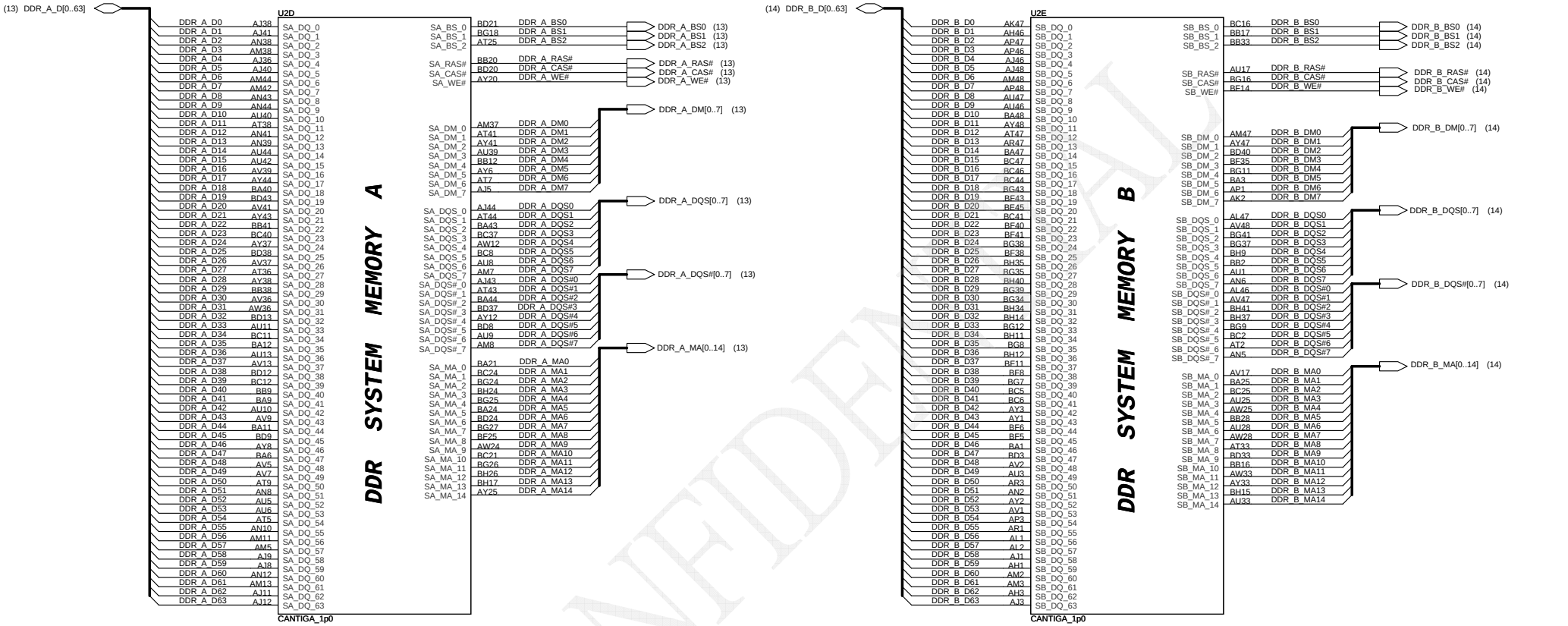

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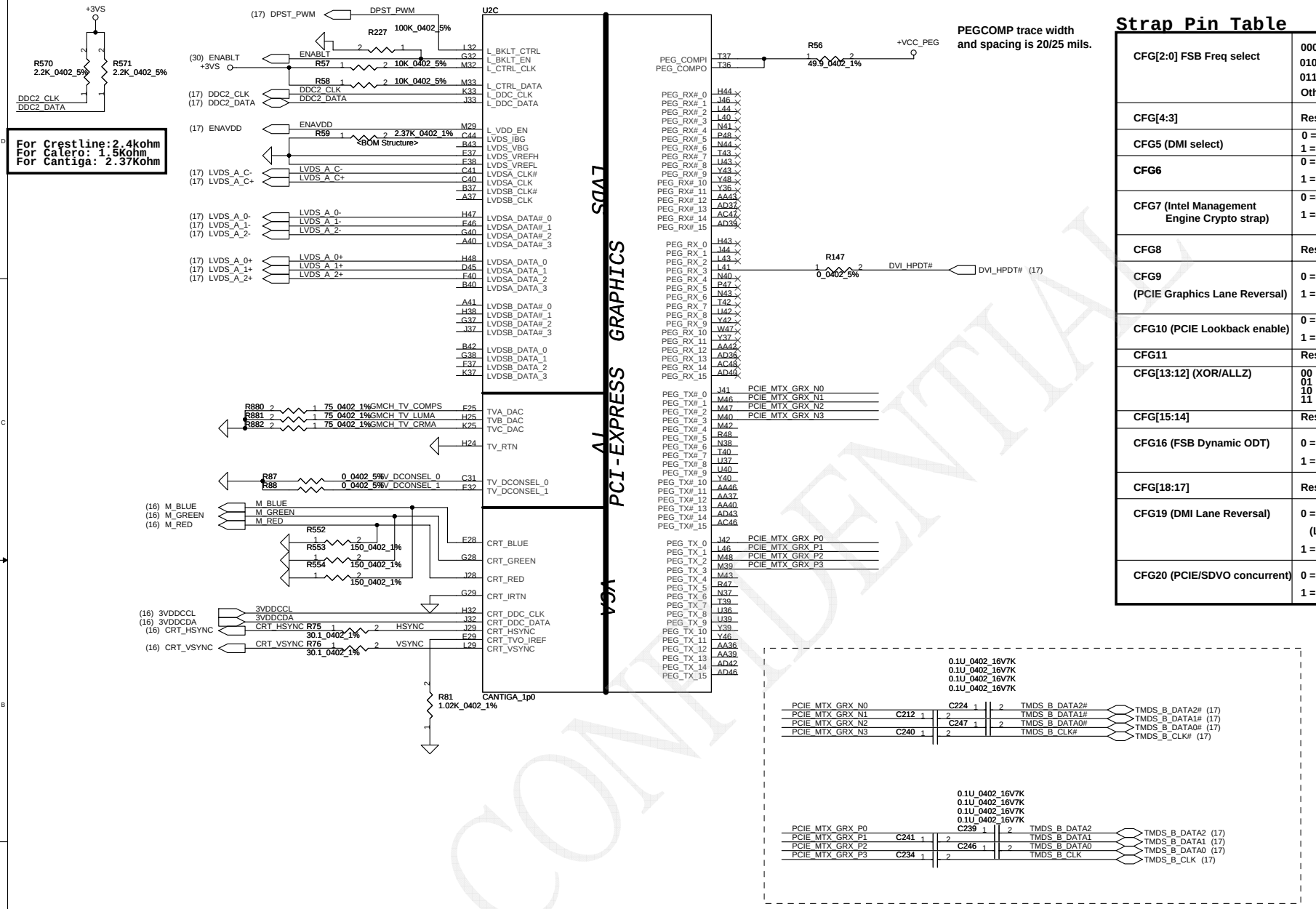

PEGCOMP trace width and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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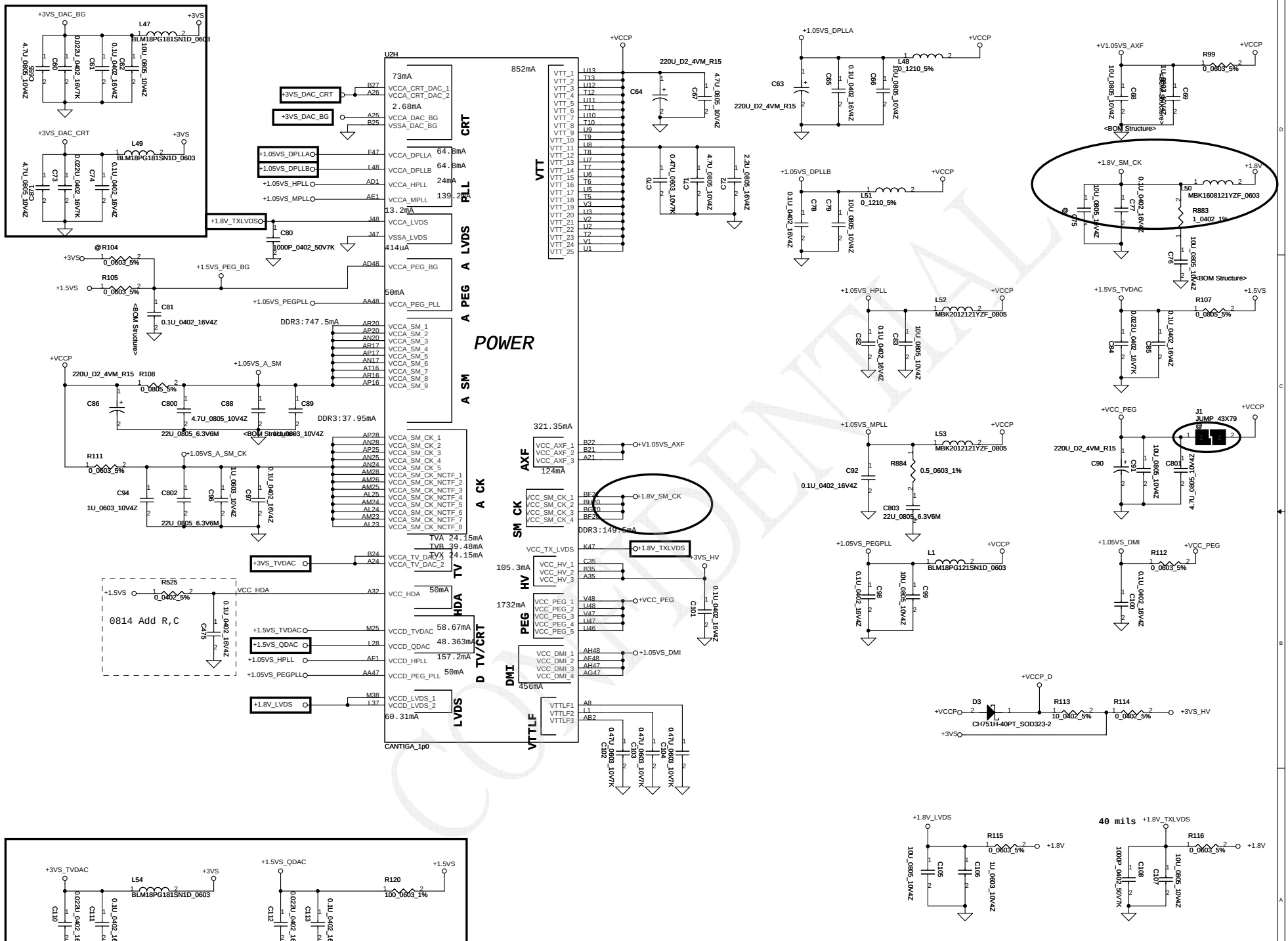

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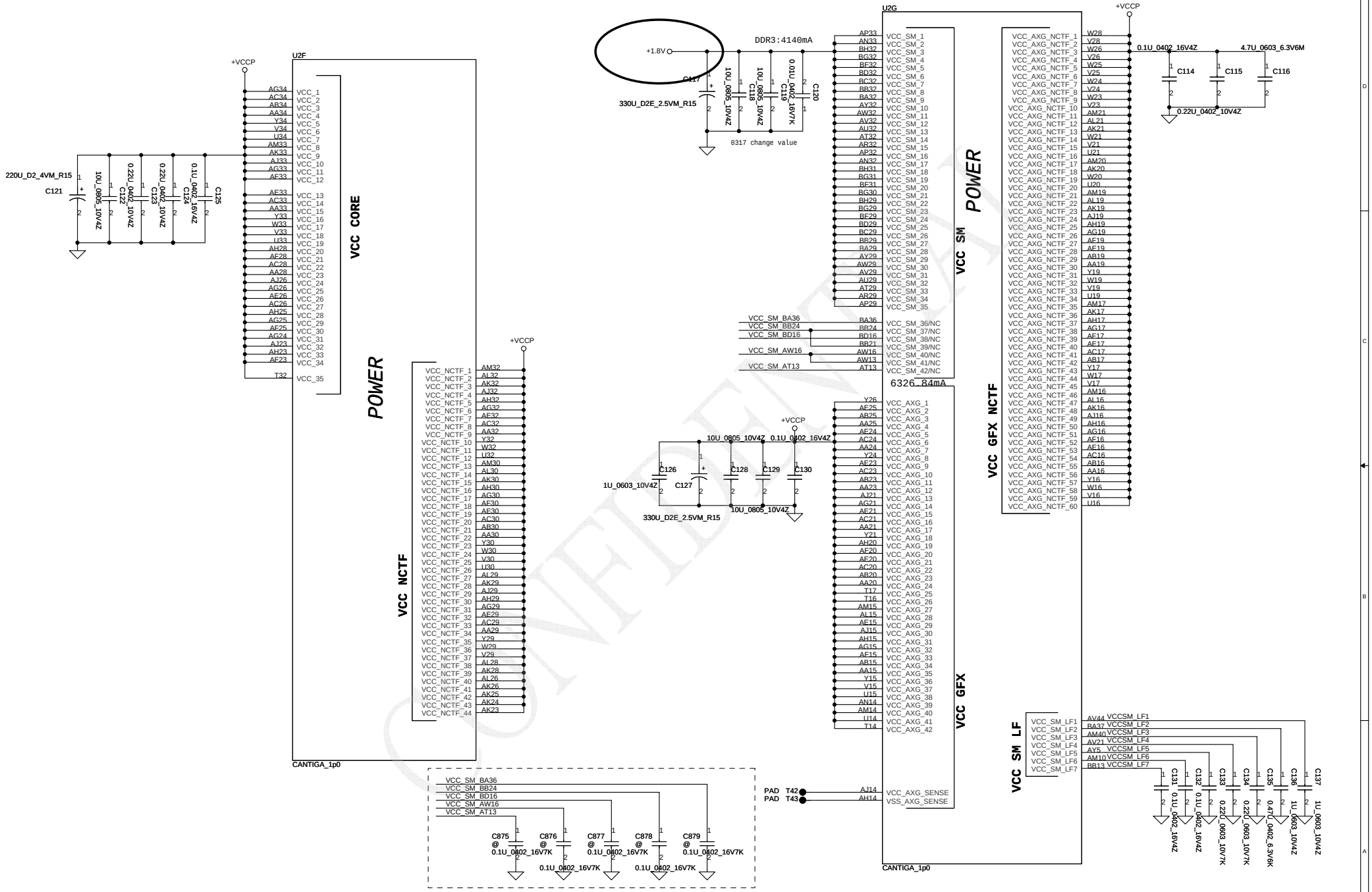

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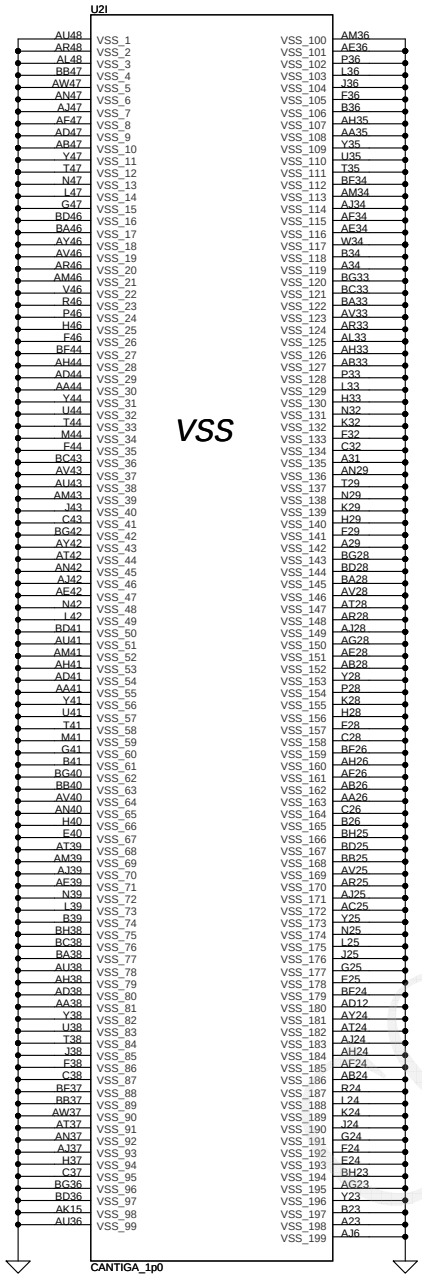

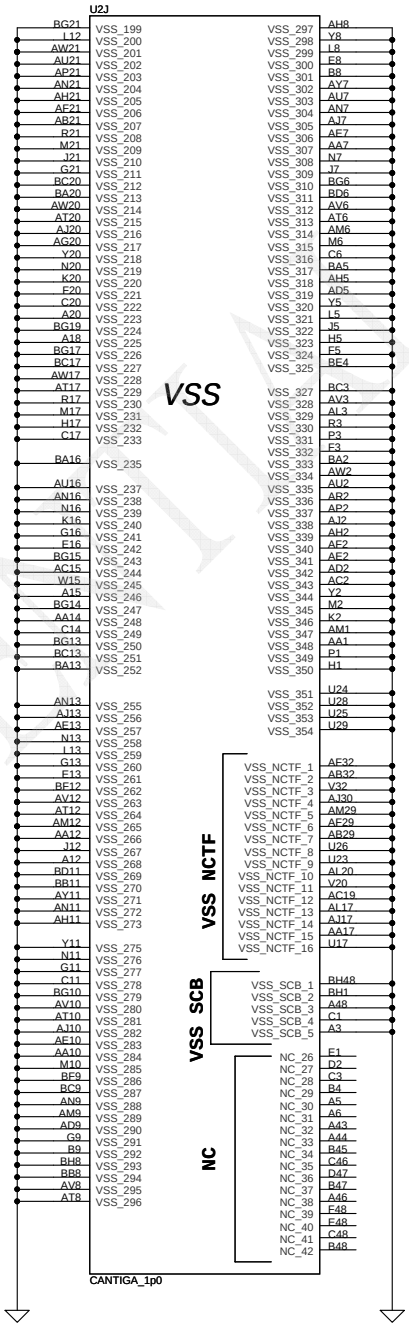

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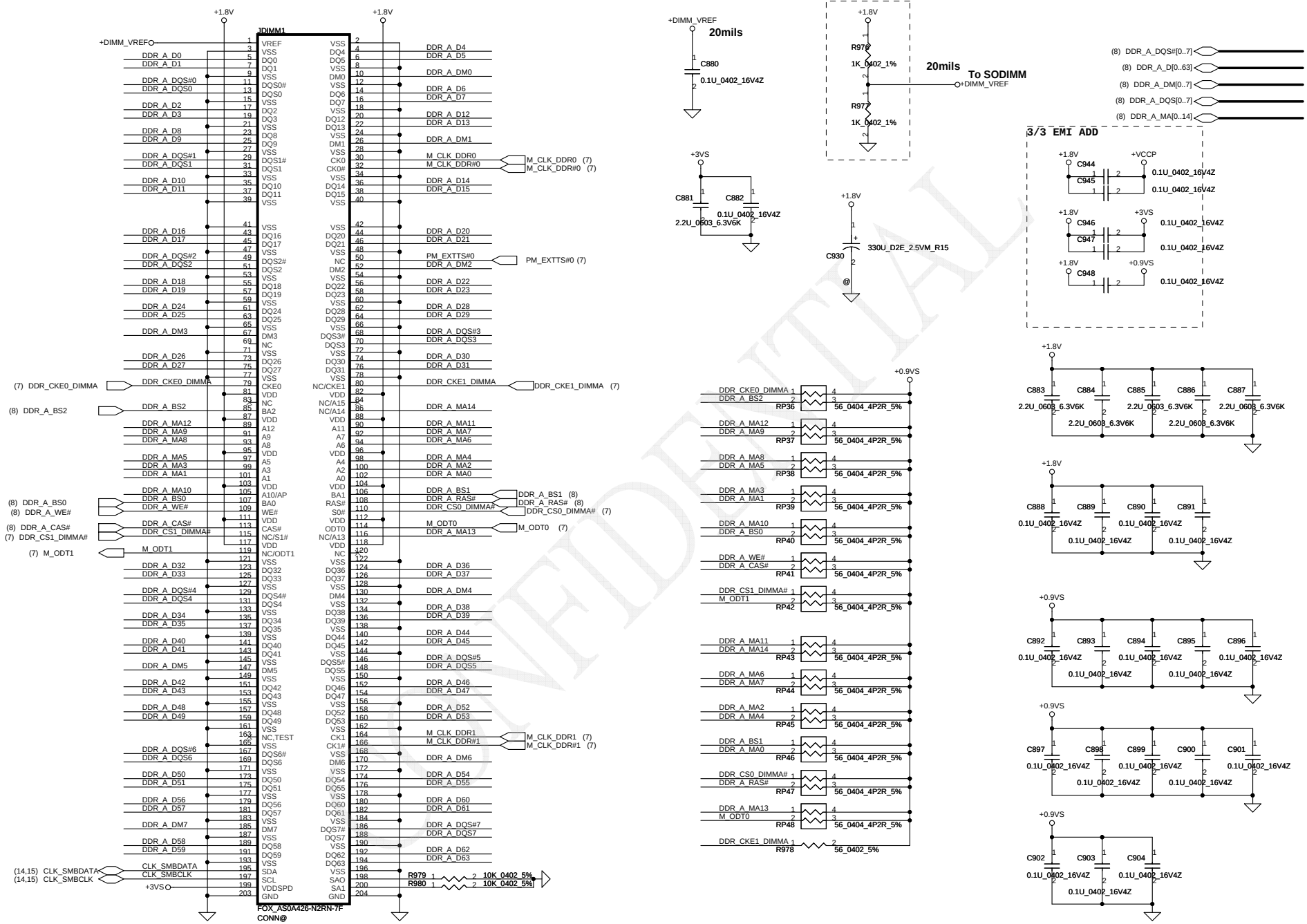

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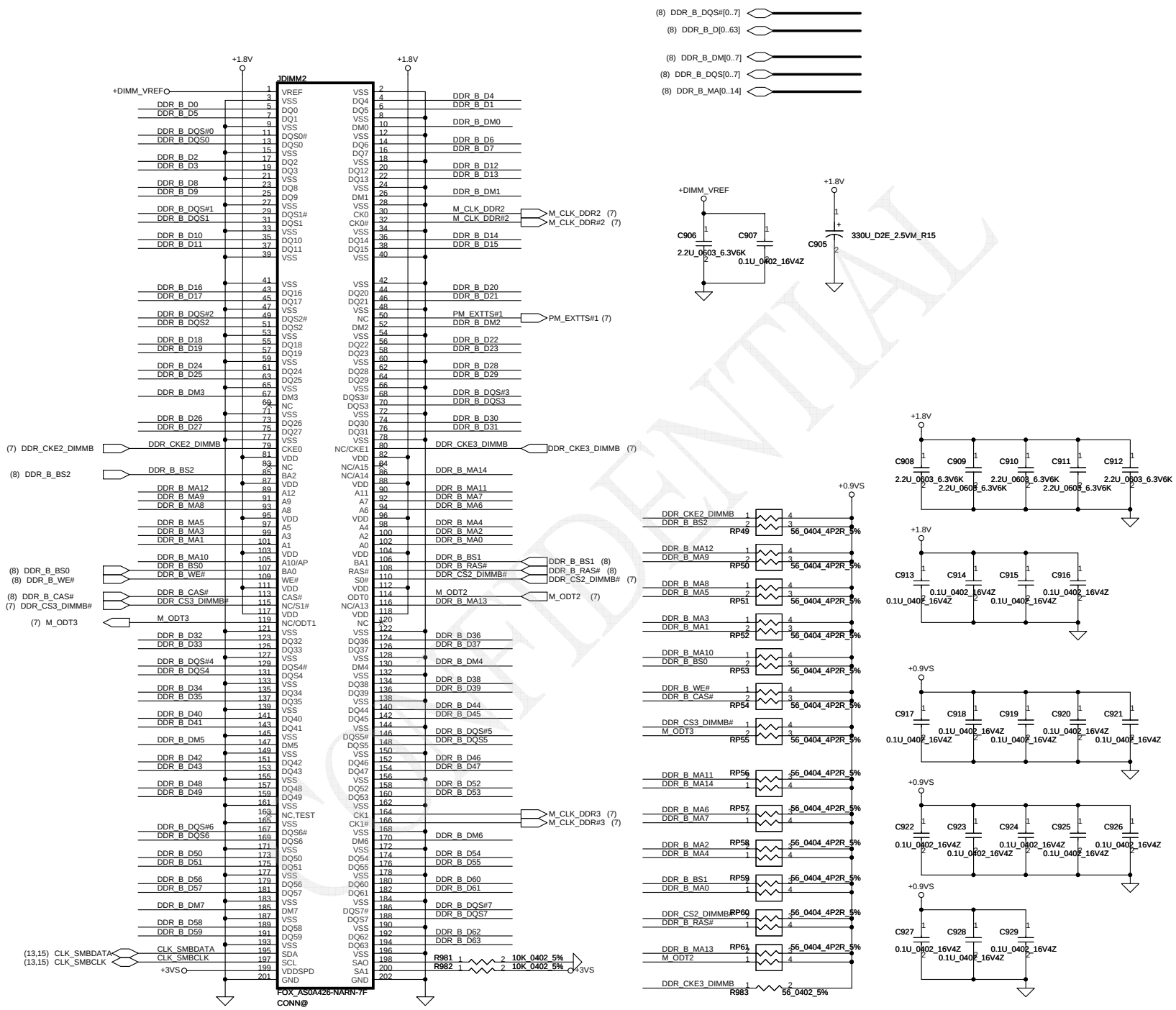

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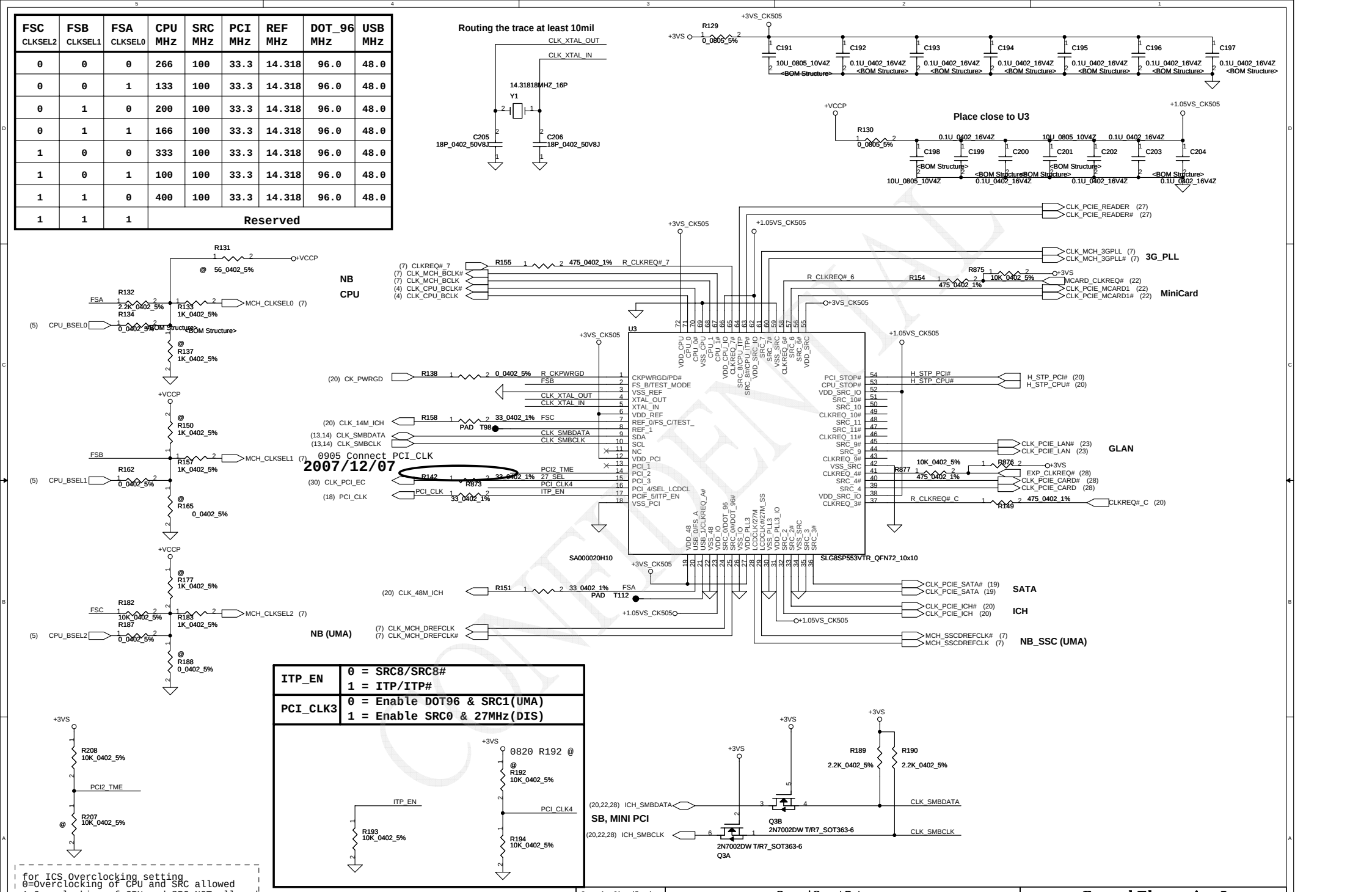
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



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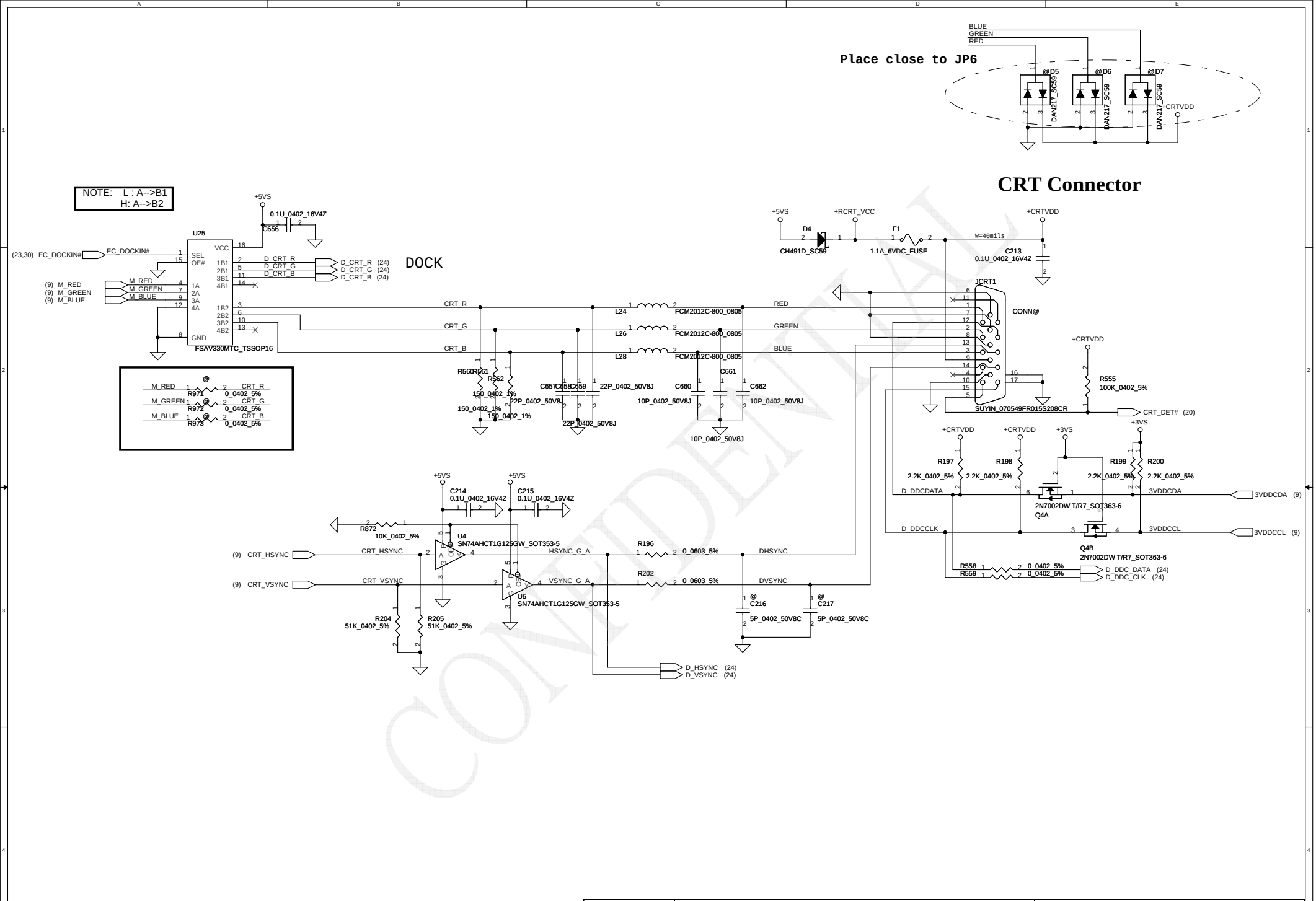

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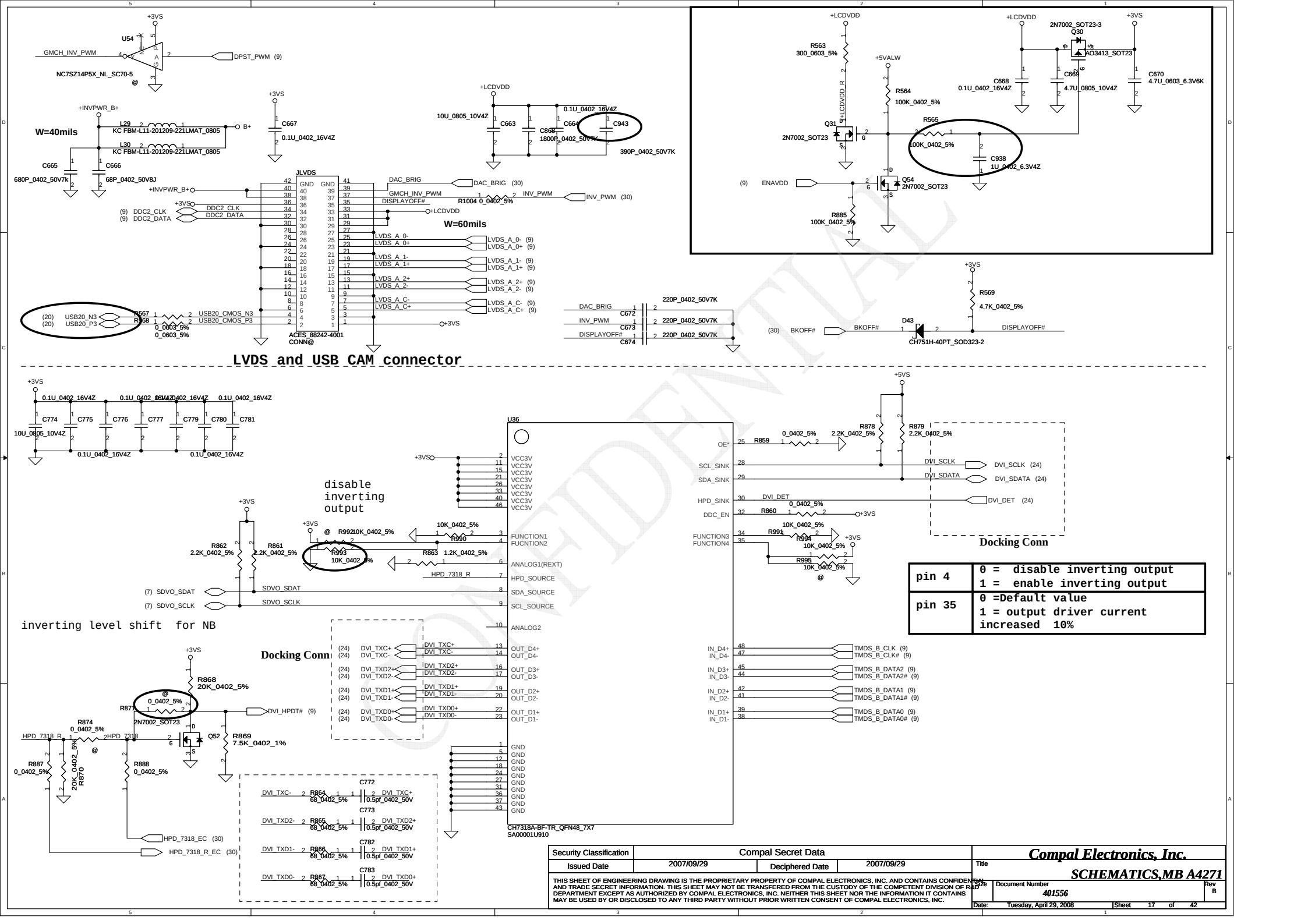

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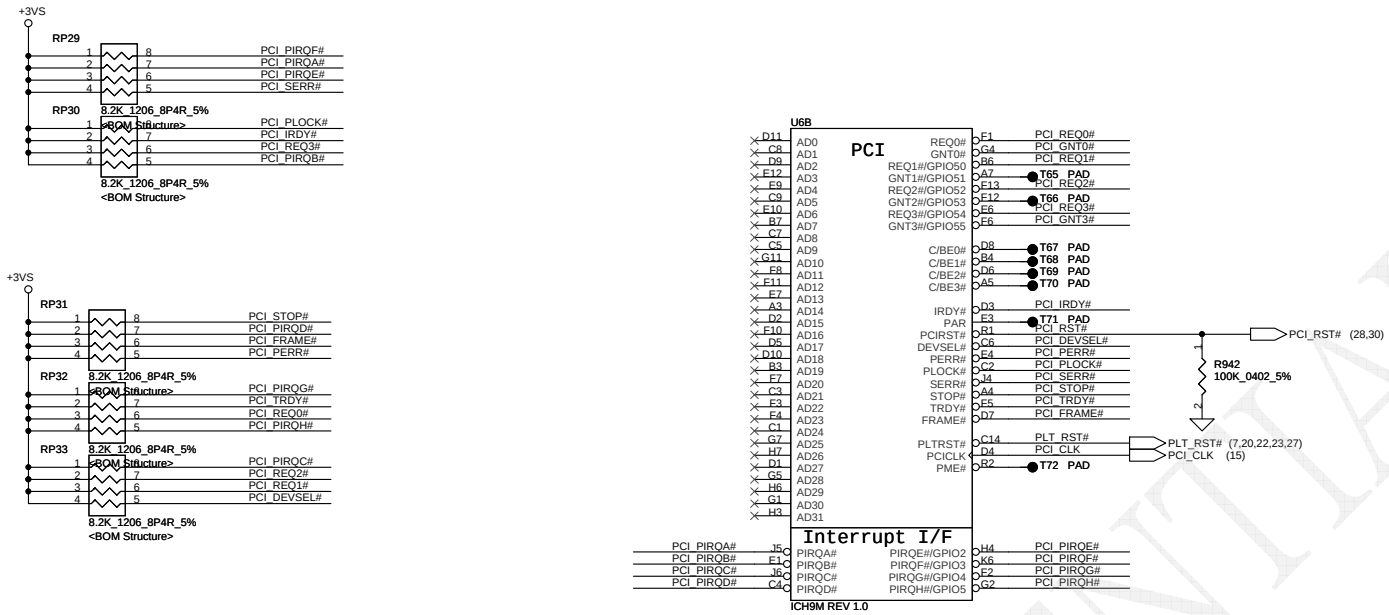
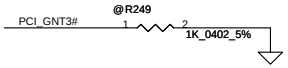
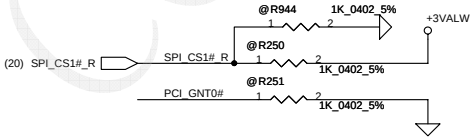


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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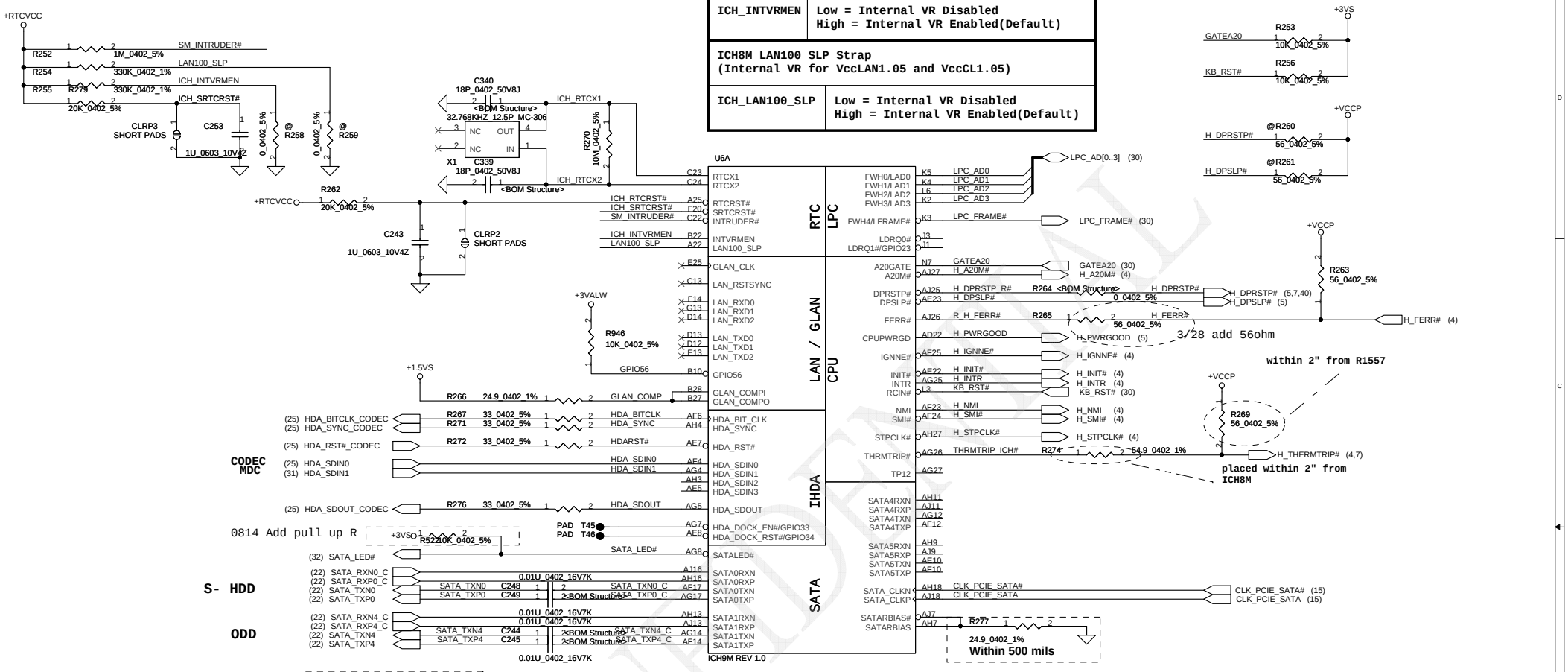
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

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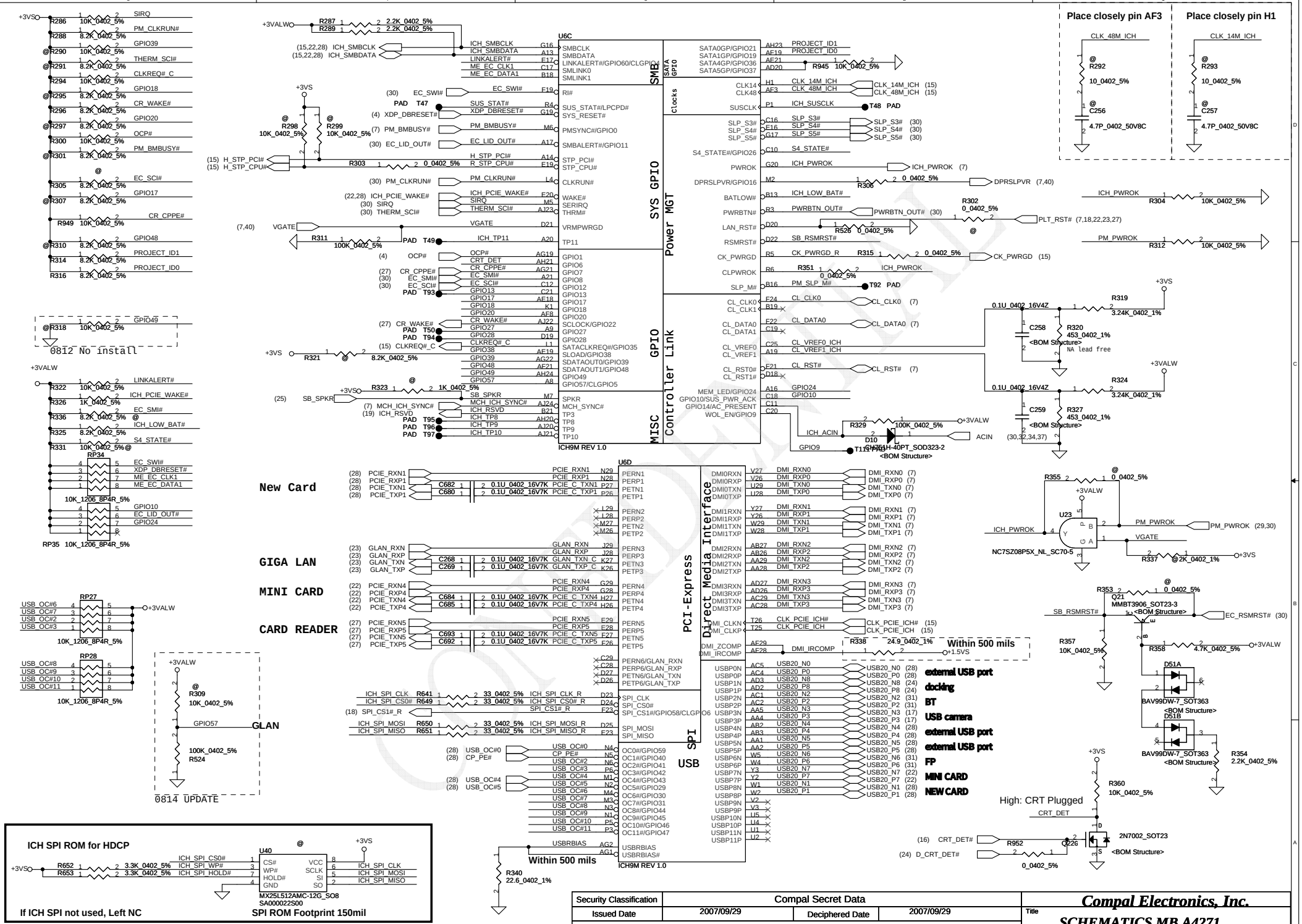
Place closely pin AF3
Place closely pin H1
U6C
ICH9M REV 1.0
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
U6D
PCI-Express
Direct Media Interface
SPI
USB
New Card
GIGA LAN
MINI CARD
CARD READER
GLAN
0812 No install
0814 UPDATE
Within 500 mils
external USB port
docking
BT
USB camera
external USB port
external USB port
FP
MINI CARD
NEW CARD
High: CRT Plugged
ICH SPI ROM for HDCP
If ICH SPI not used, Left NC
SPI ROM Footprint 150mil
MX25L512AMC-12G_SO8
SA000022S00
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2007/09/29
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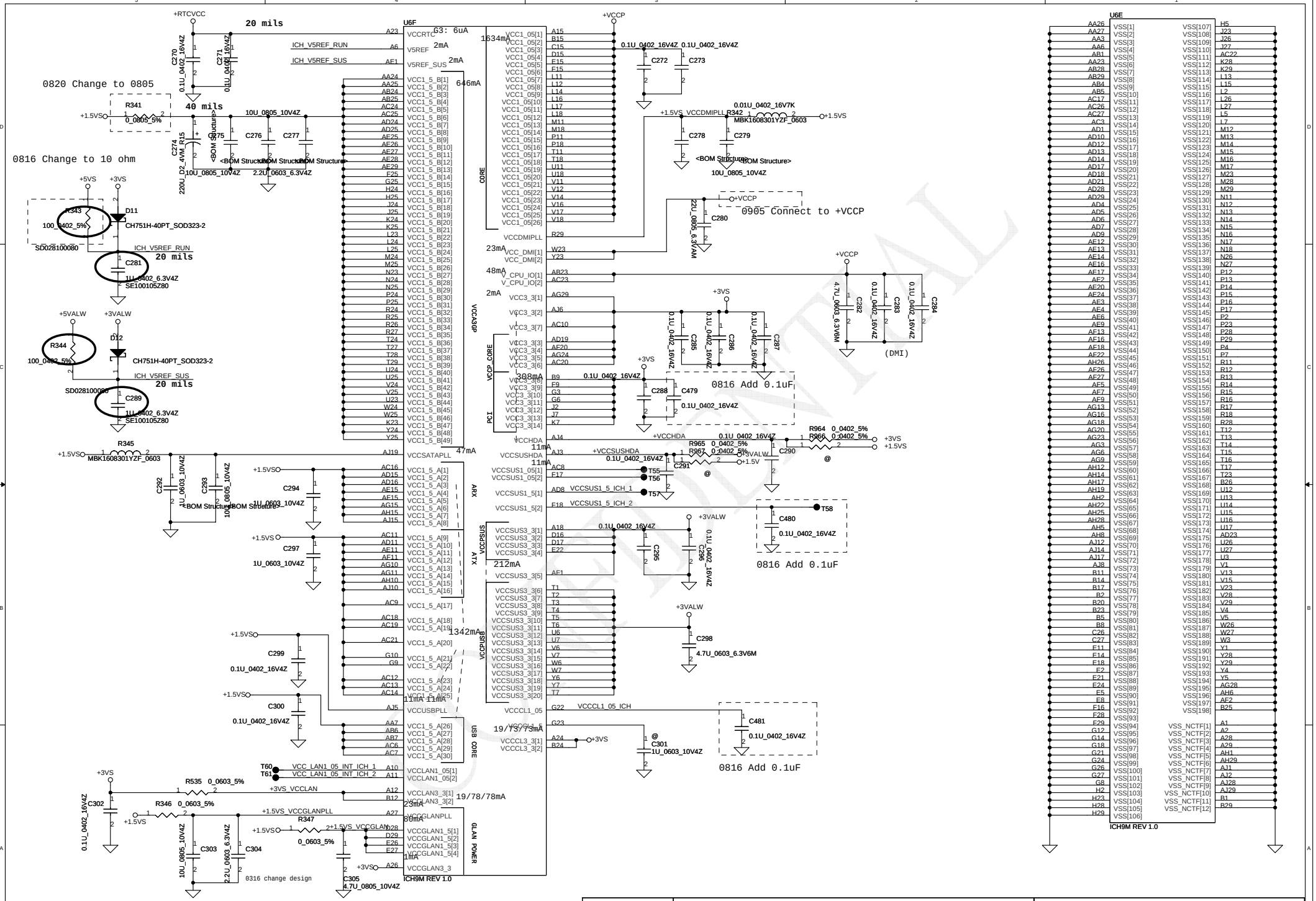

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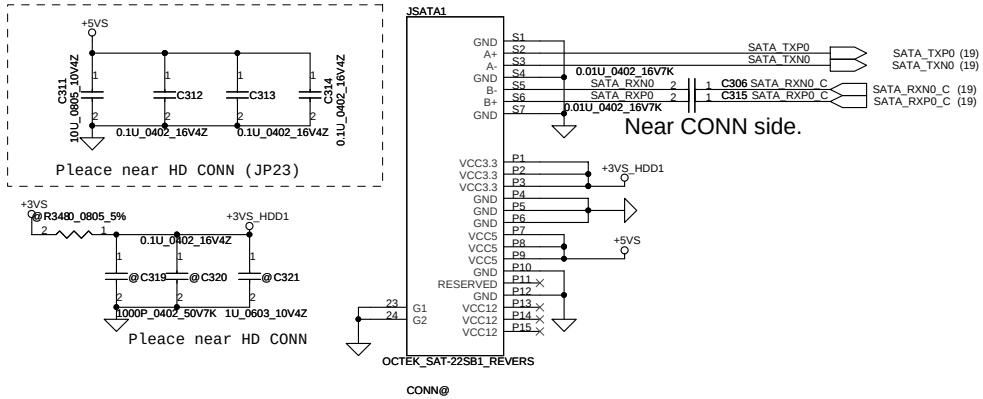
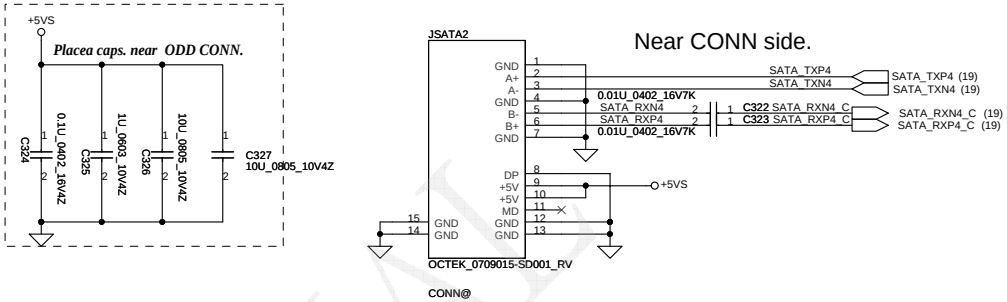
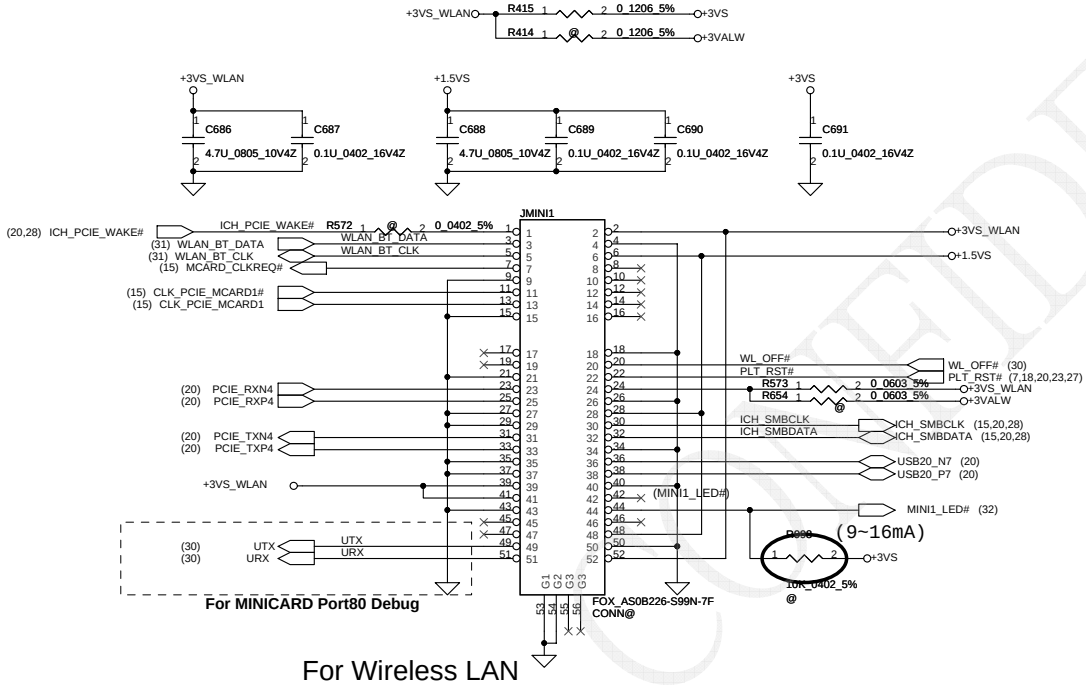
HDD Connector



CD-ROM Connector





For Wireless LAN

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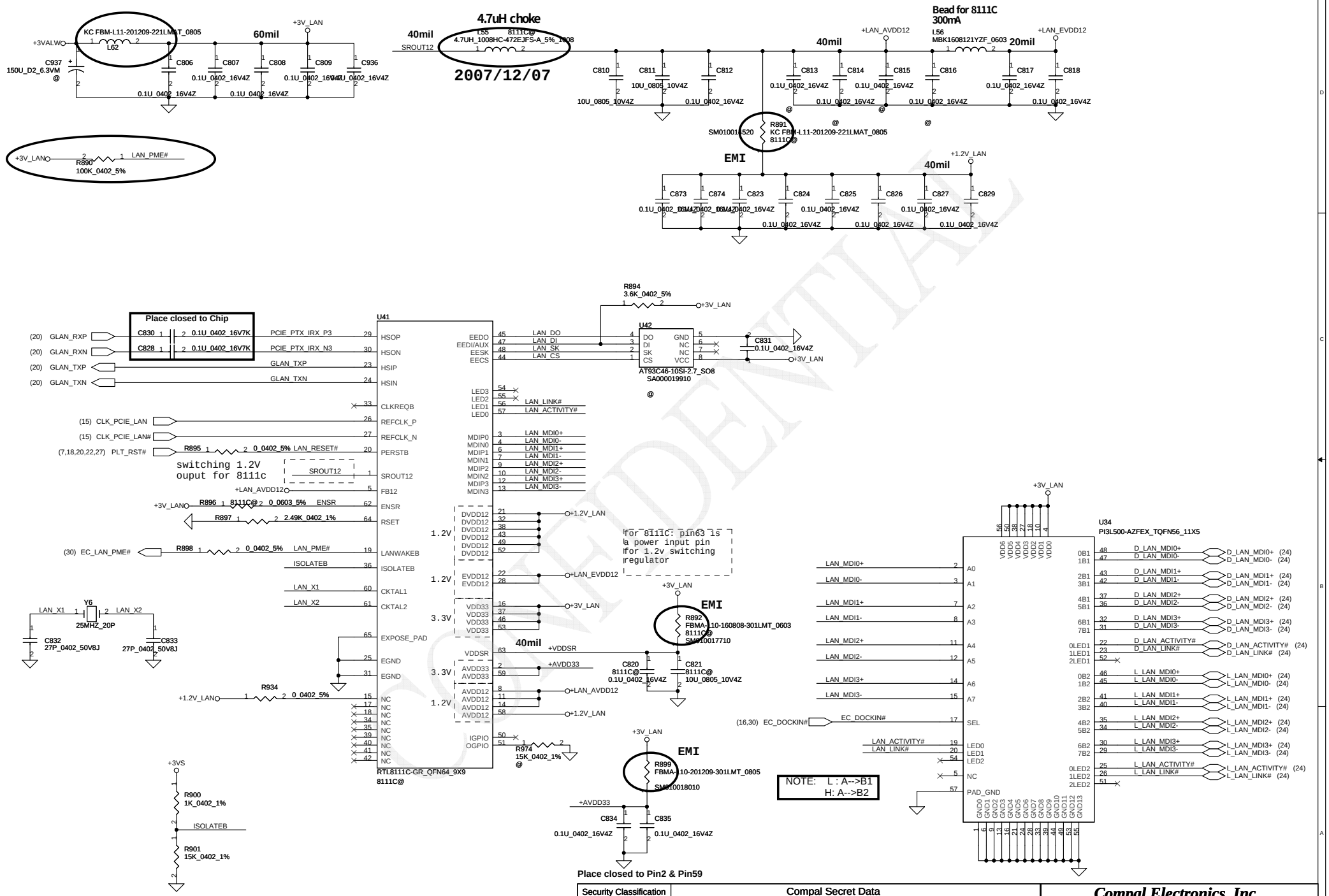
LAN RTL8111C/8102E



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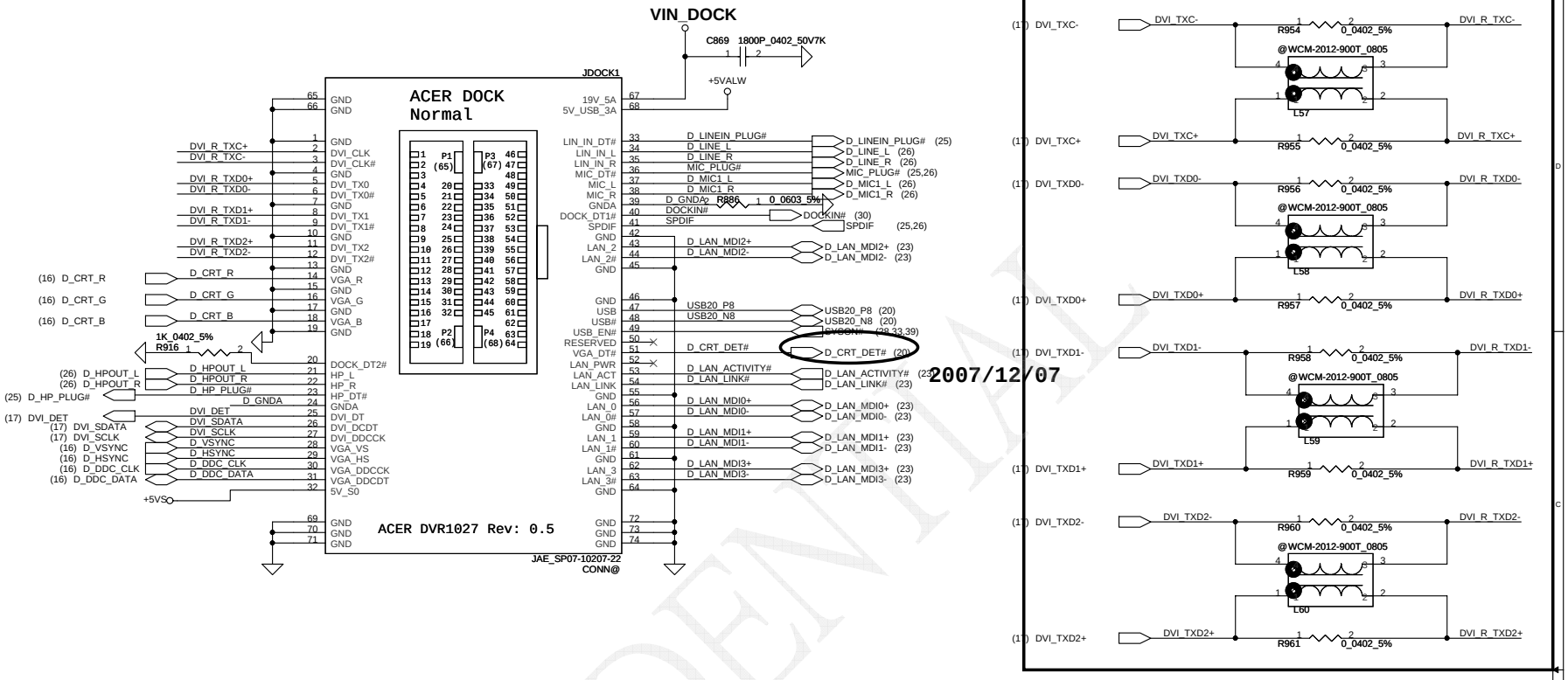

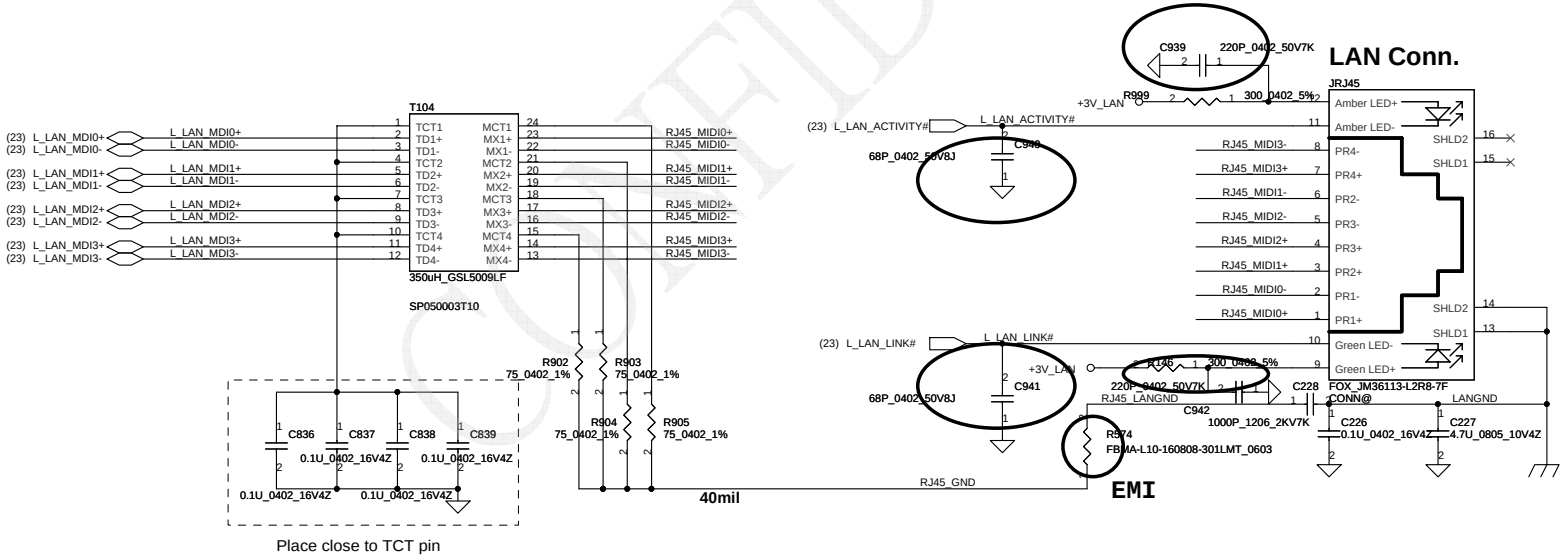

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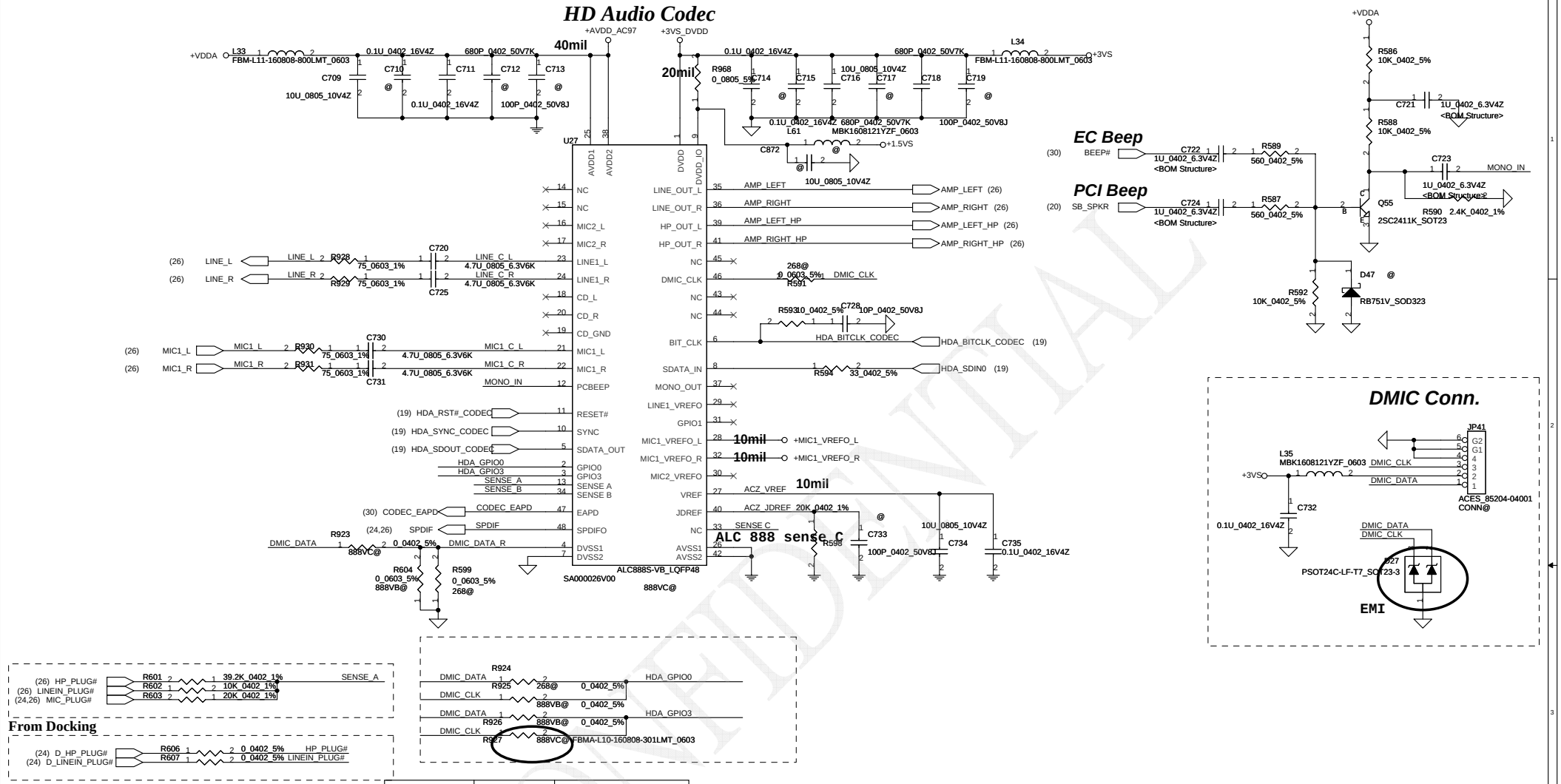
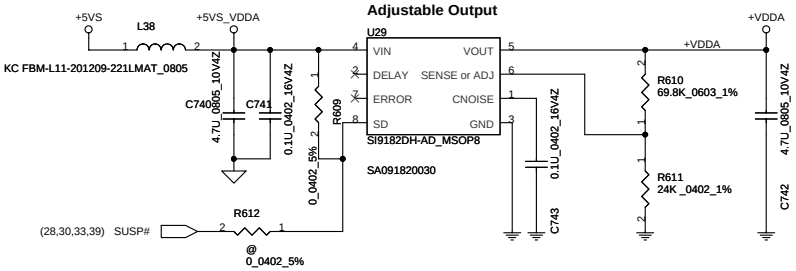
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)
SENSE C	39.2K	CD
	20K	1st S/PDIF Out
	10K	2nd S/PDIF Out
	5.1K	S/PDIF-IN

Regulator for CODEC



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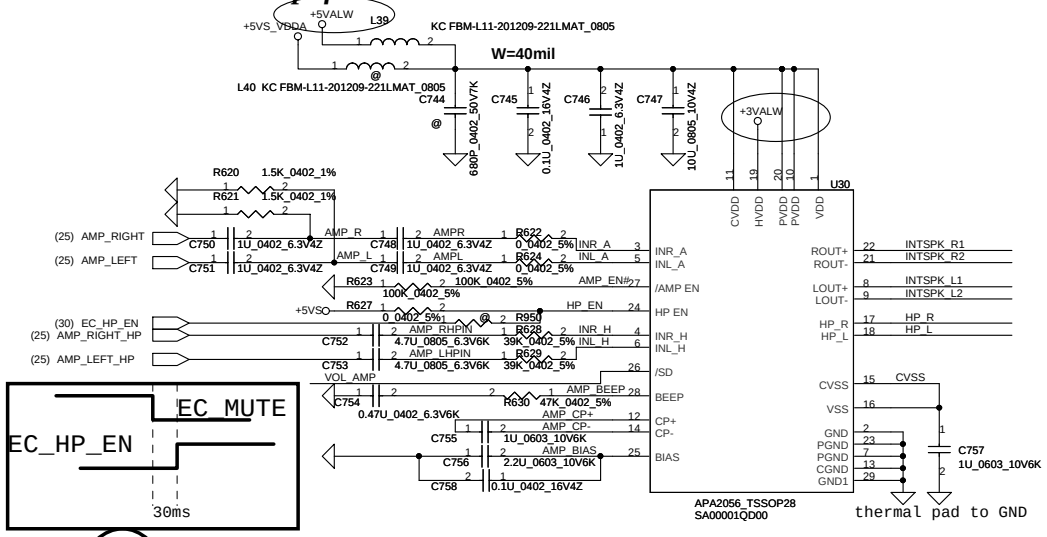
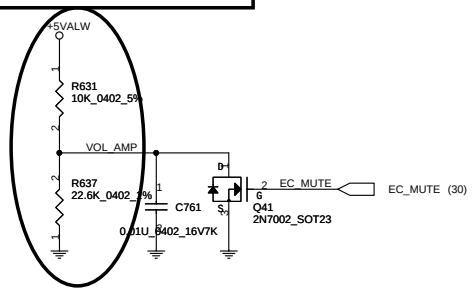
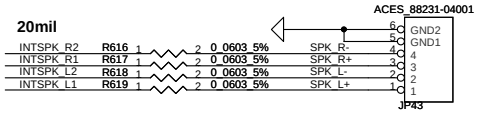
APA2057 SPK/HP Amplifier

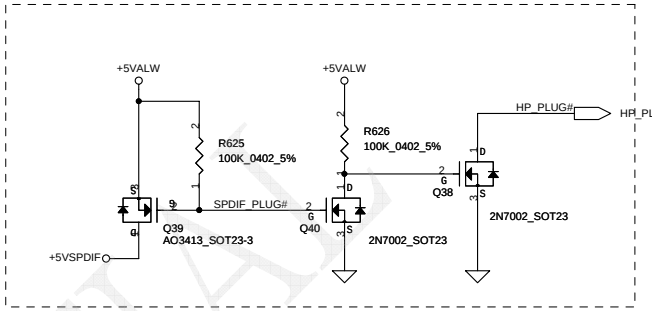


IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



Int. Speaker Conn.

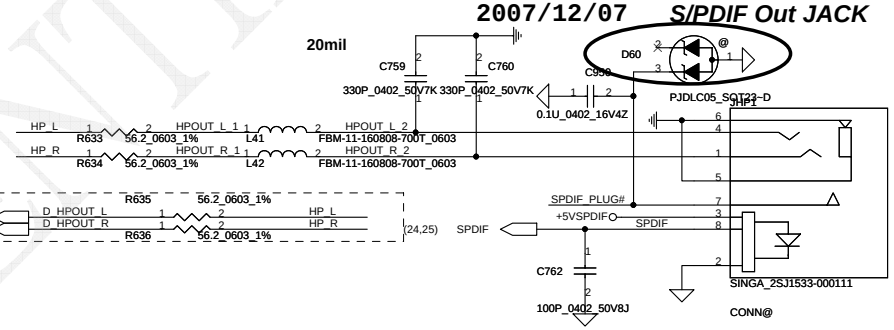




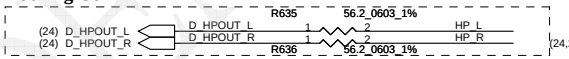
LINE Out/Headphone Out

2007/12/07

S/PDIF Out JACK

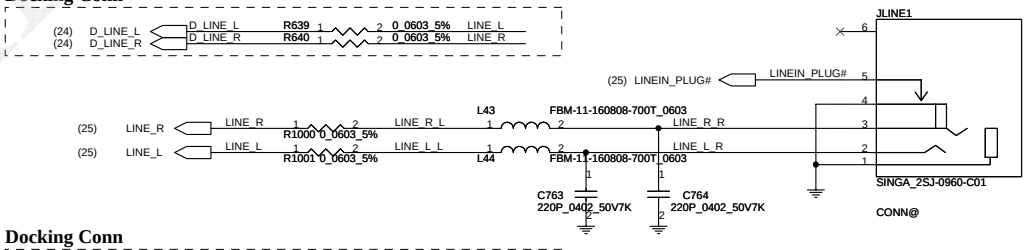


Docking Conn

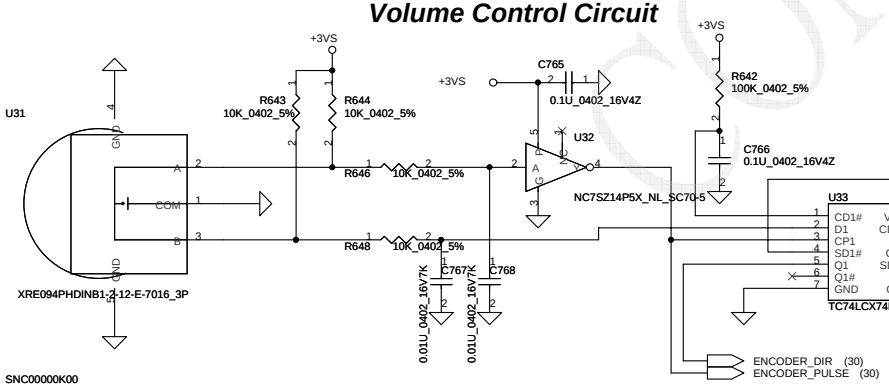


LINE-IN JACK

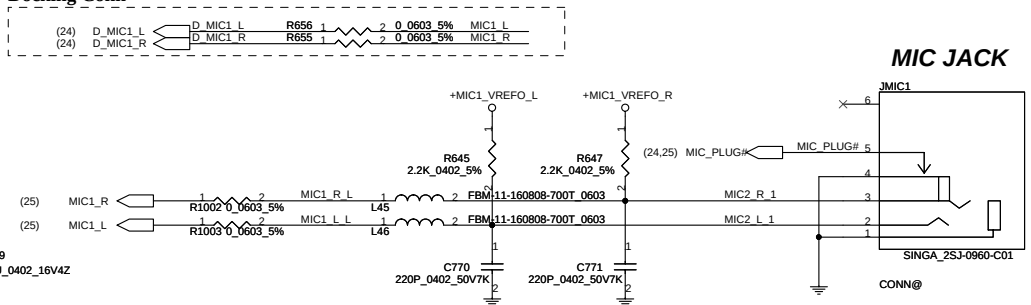
Docking Conn



Volume Control Circuit



Docking Conn



MIC JACK

SNC00000K00

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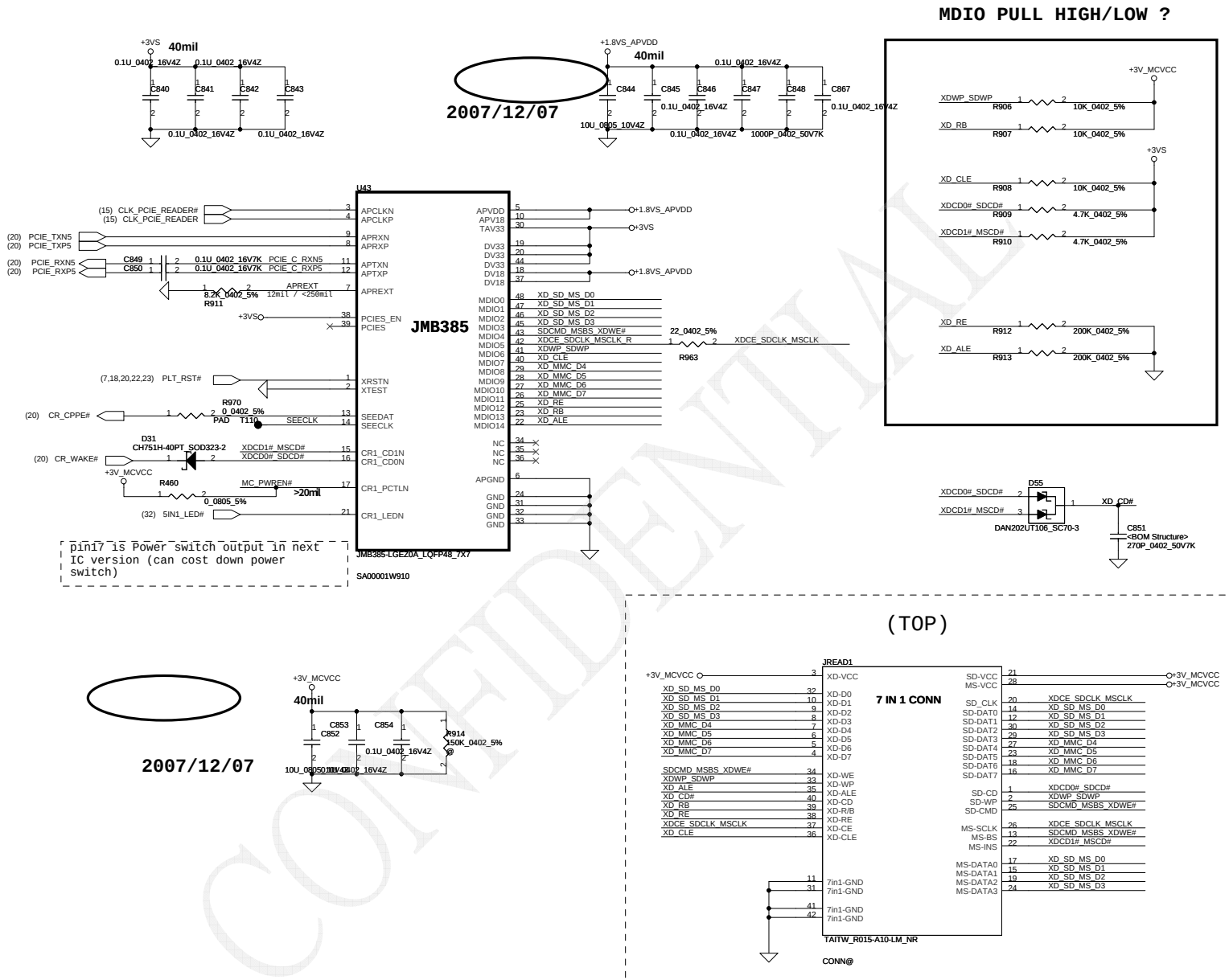

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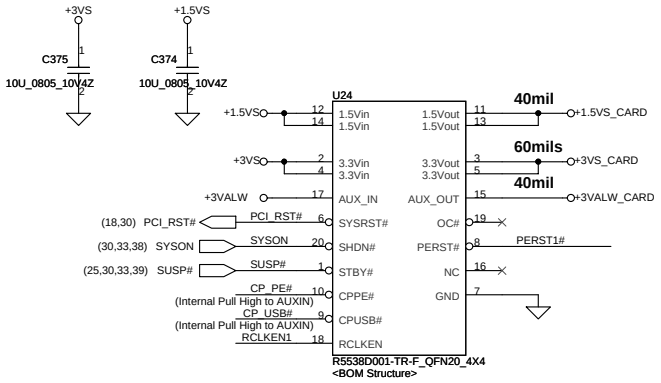
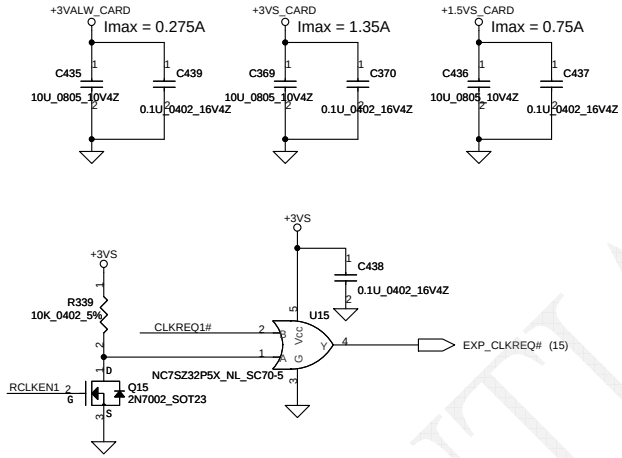
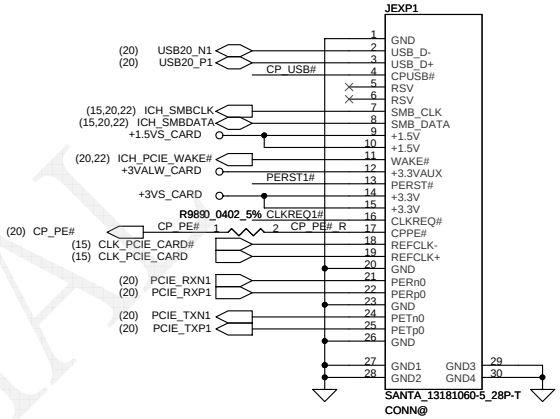
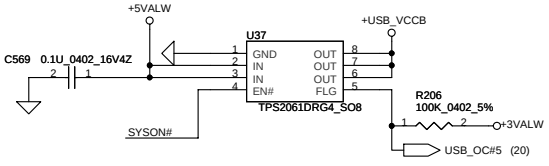
New Card Power Switch

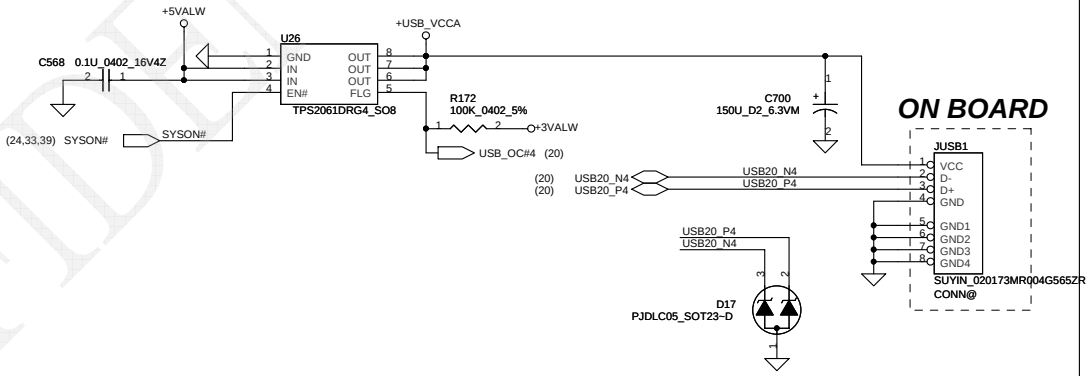


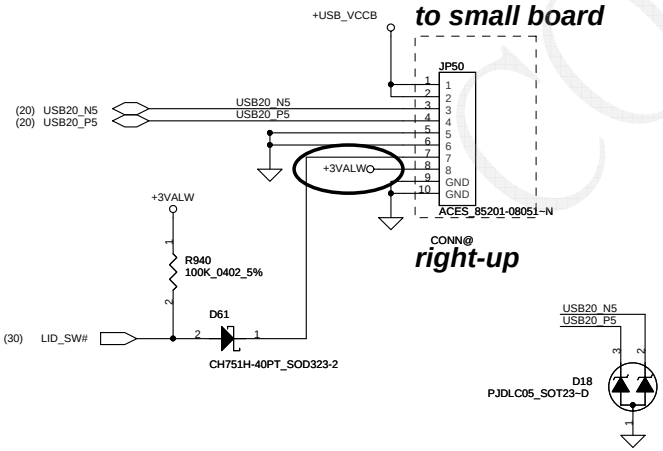


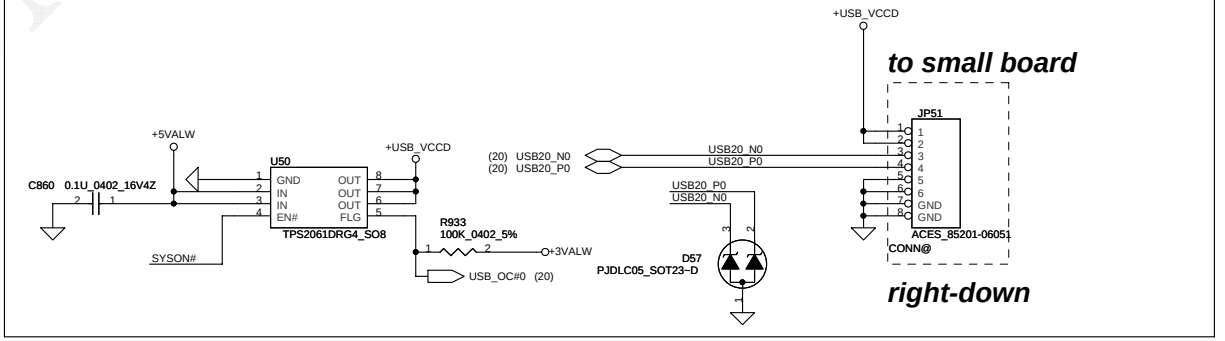
New Card Socket (Left/TOP)











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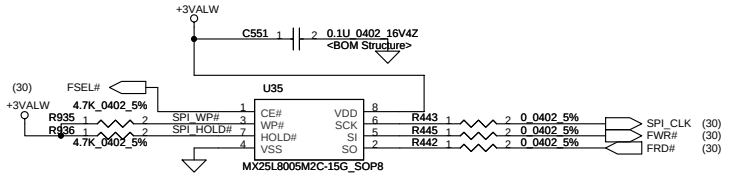
BIOS

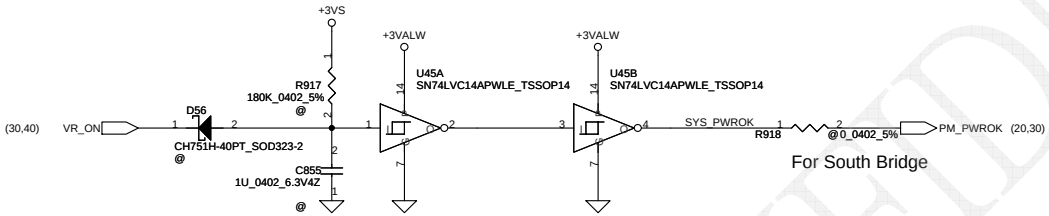


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

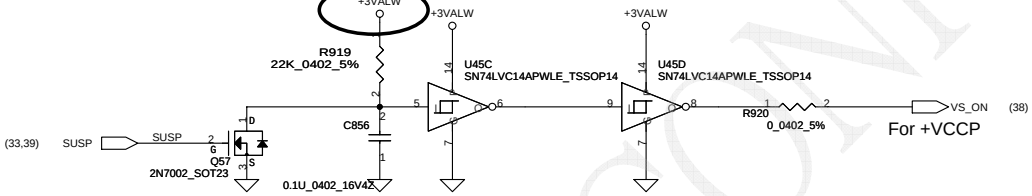
2007/12/07

reserve ***VS_ON will be drived by EC***

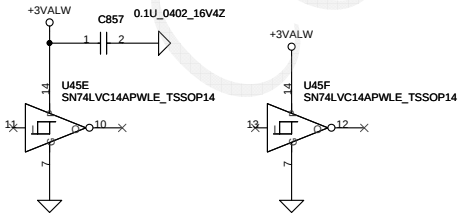
Power ON Circuit

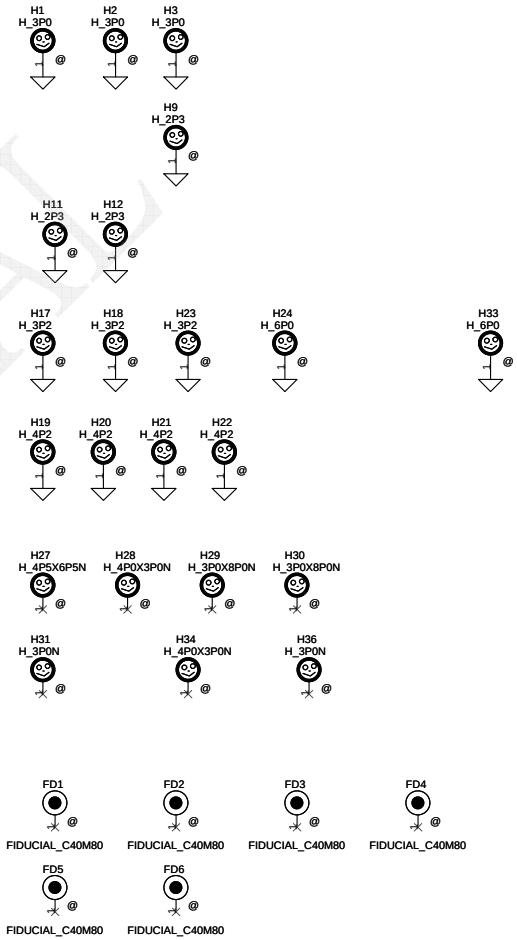


For South Bridge



For +VCCP





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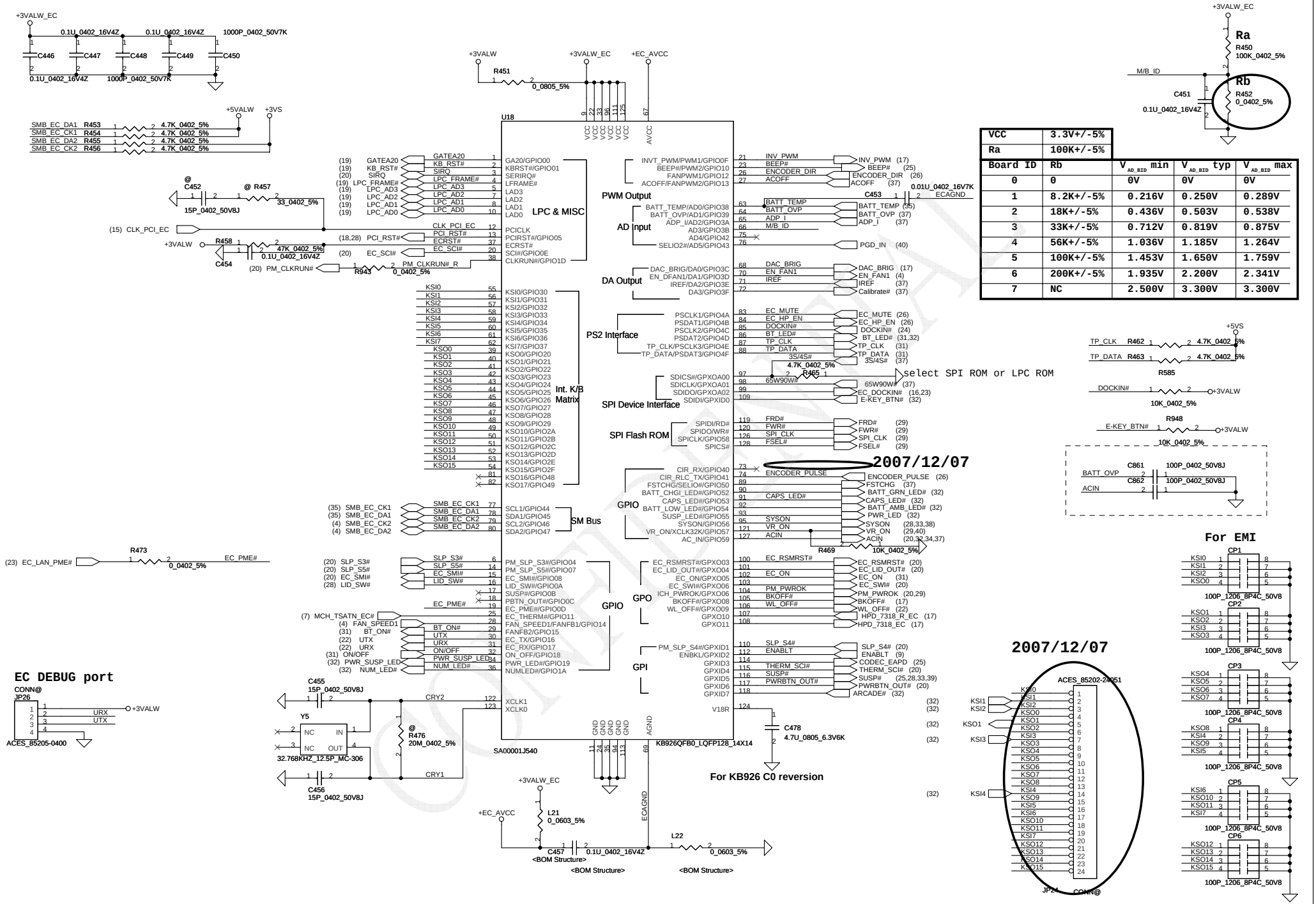

VCC	3.3V+/-5%
Ra	100K+/-5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

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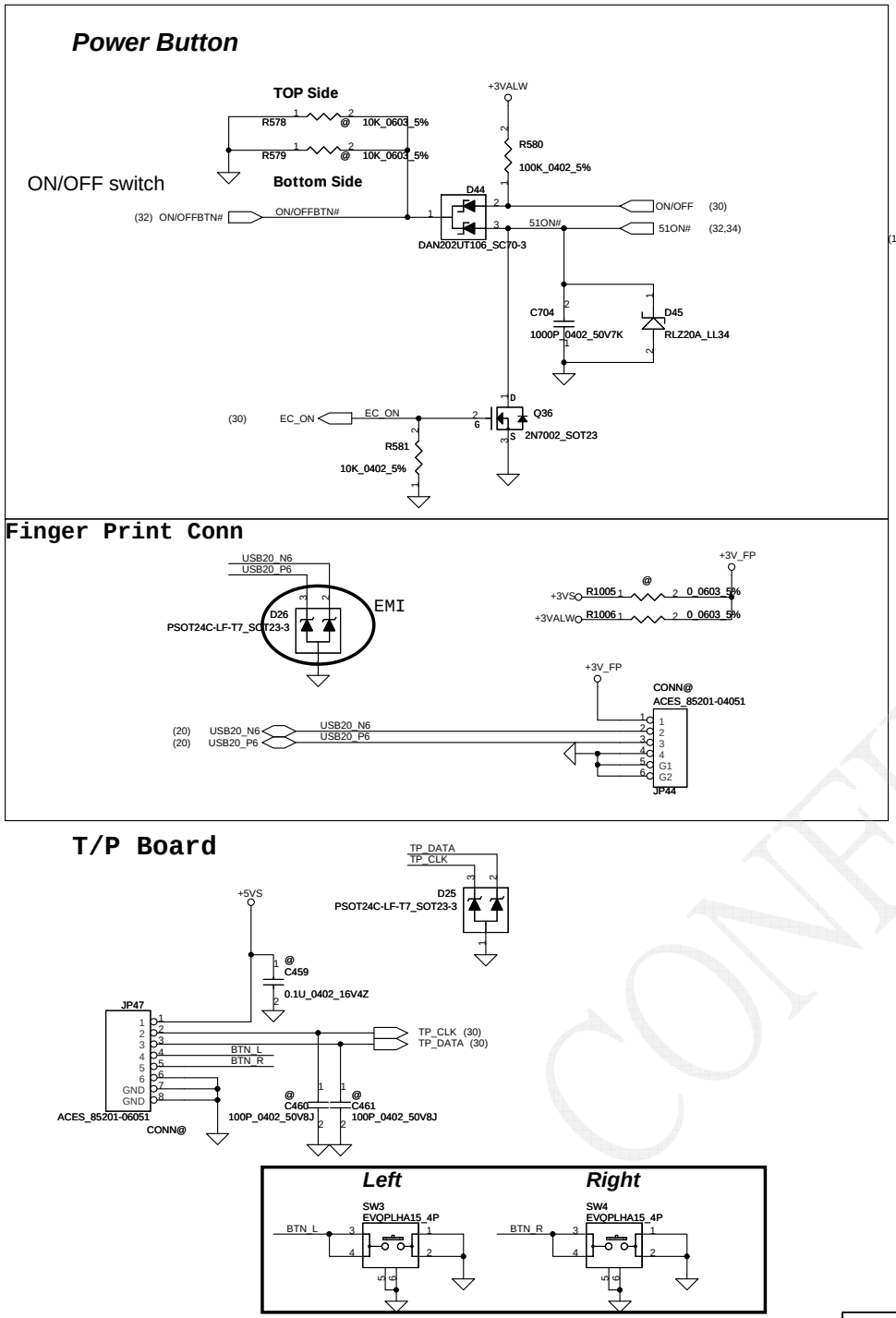

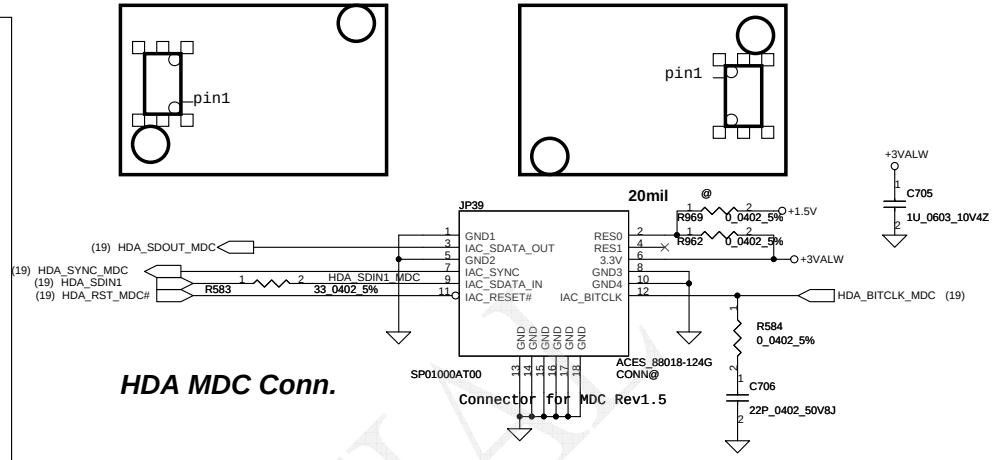

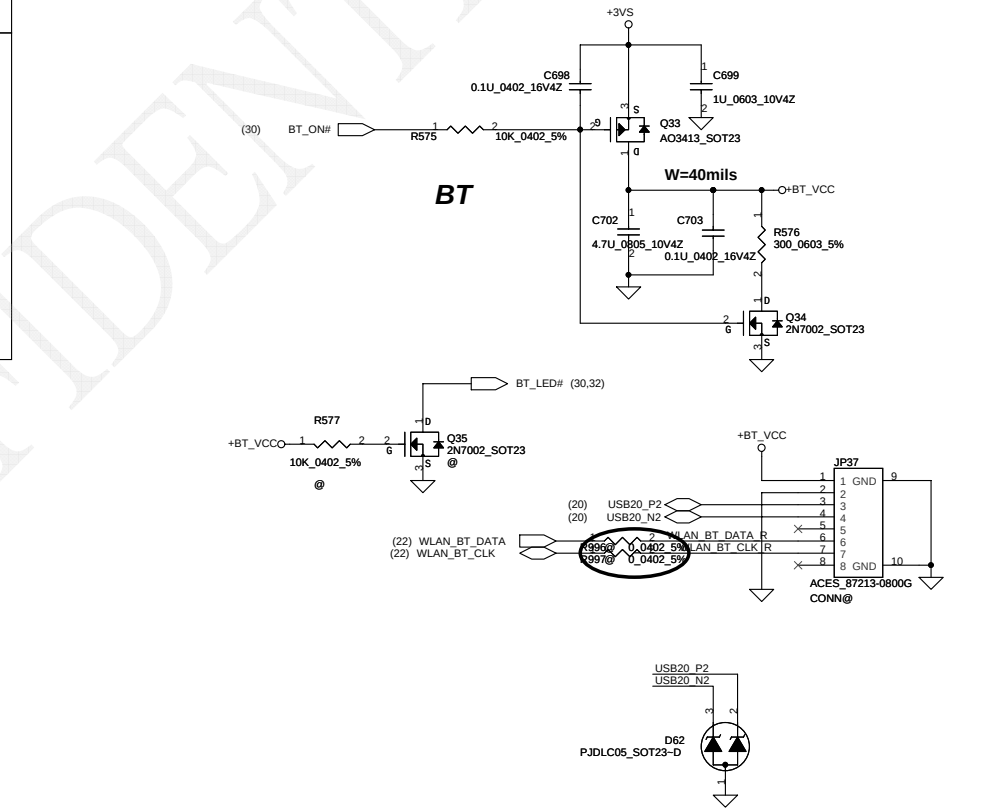

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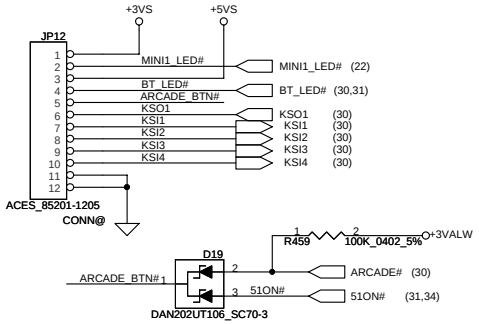
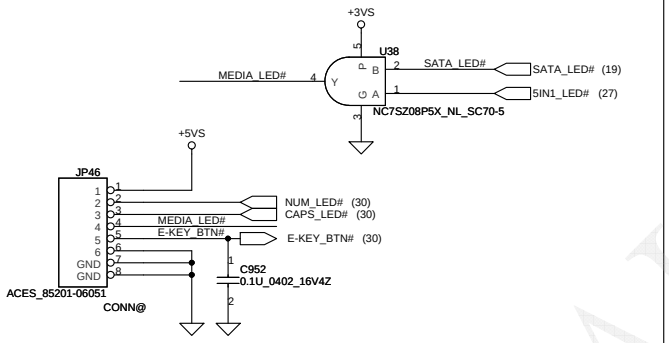
TO S/W B

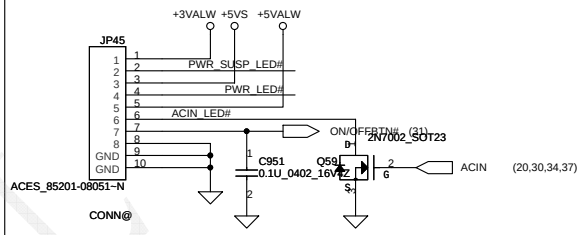


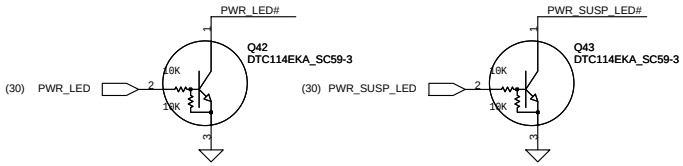
	KSO1
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#

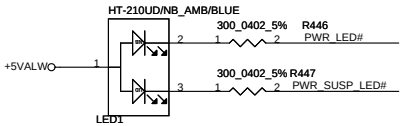
LED & E-BTN/B



TO POWER BTN/B







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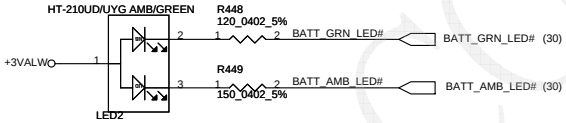

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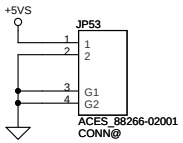

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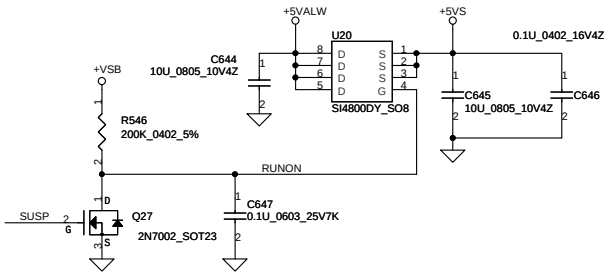
+5VALW to +5VS Transfer



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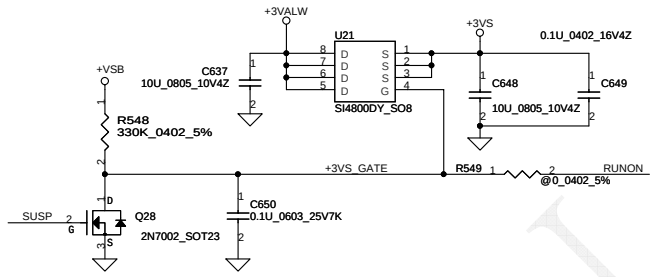
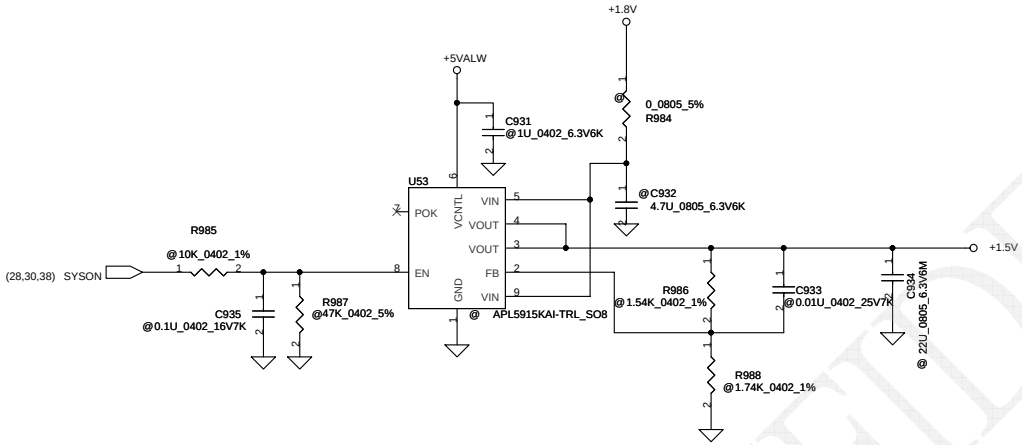
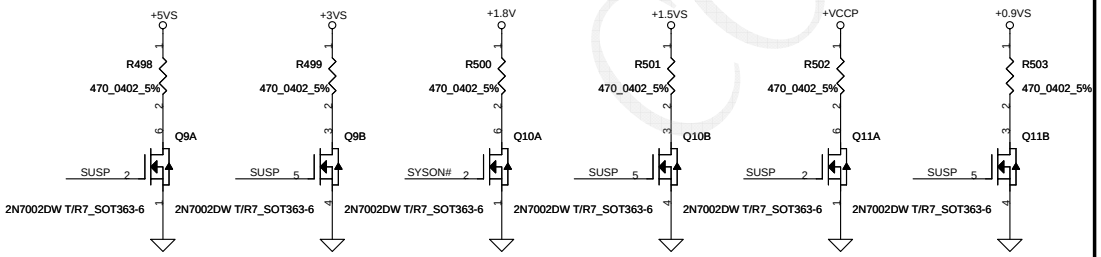
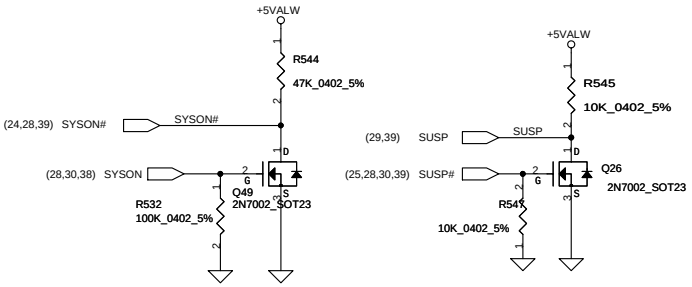




Discharge circuit





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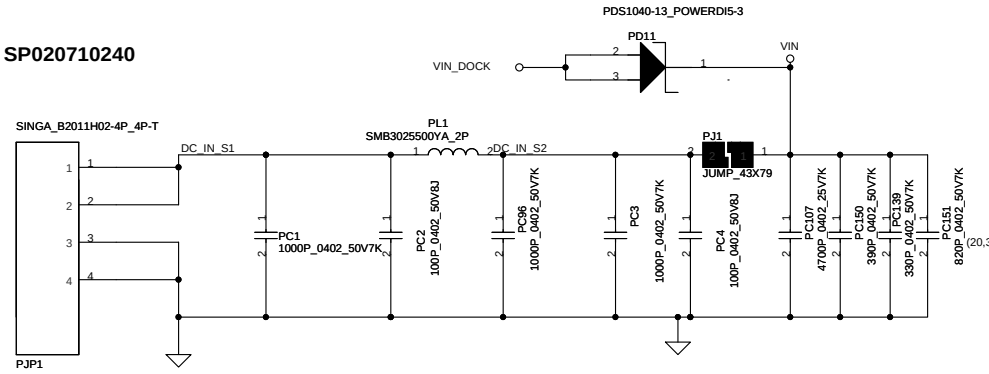
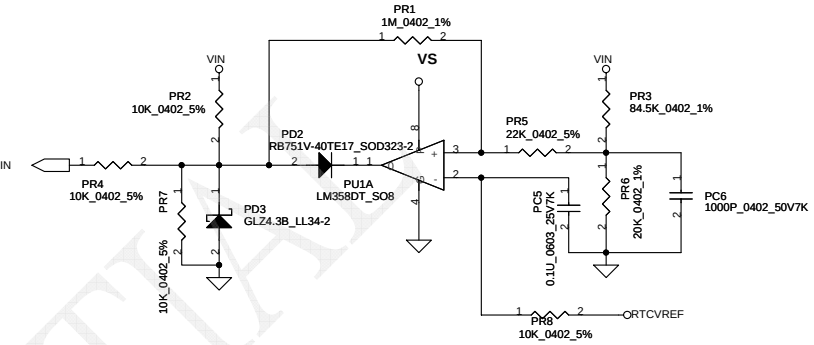
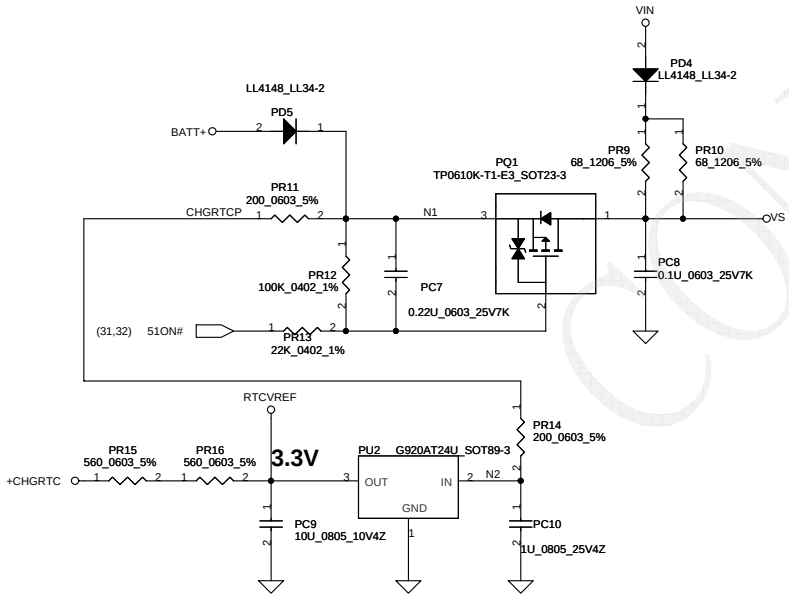
SP020710240

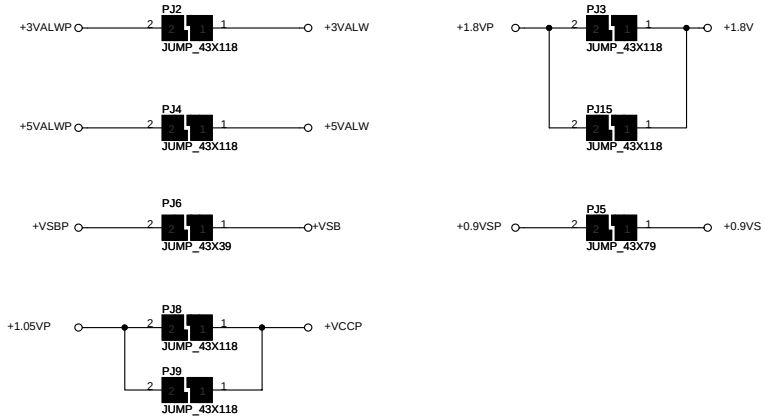




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





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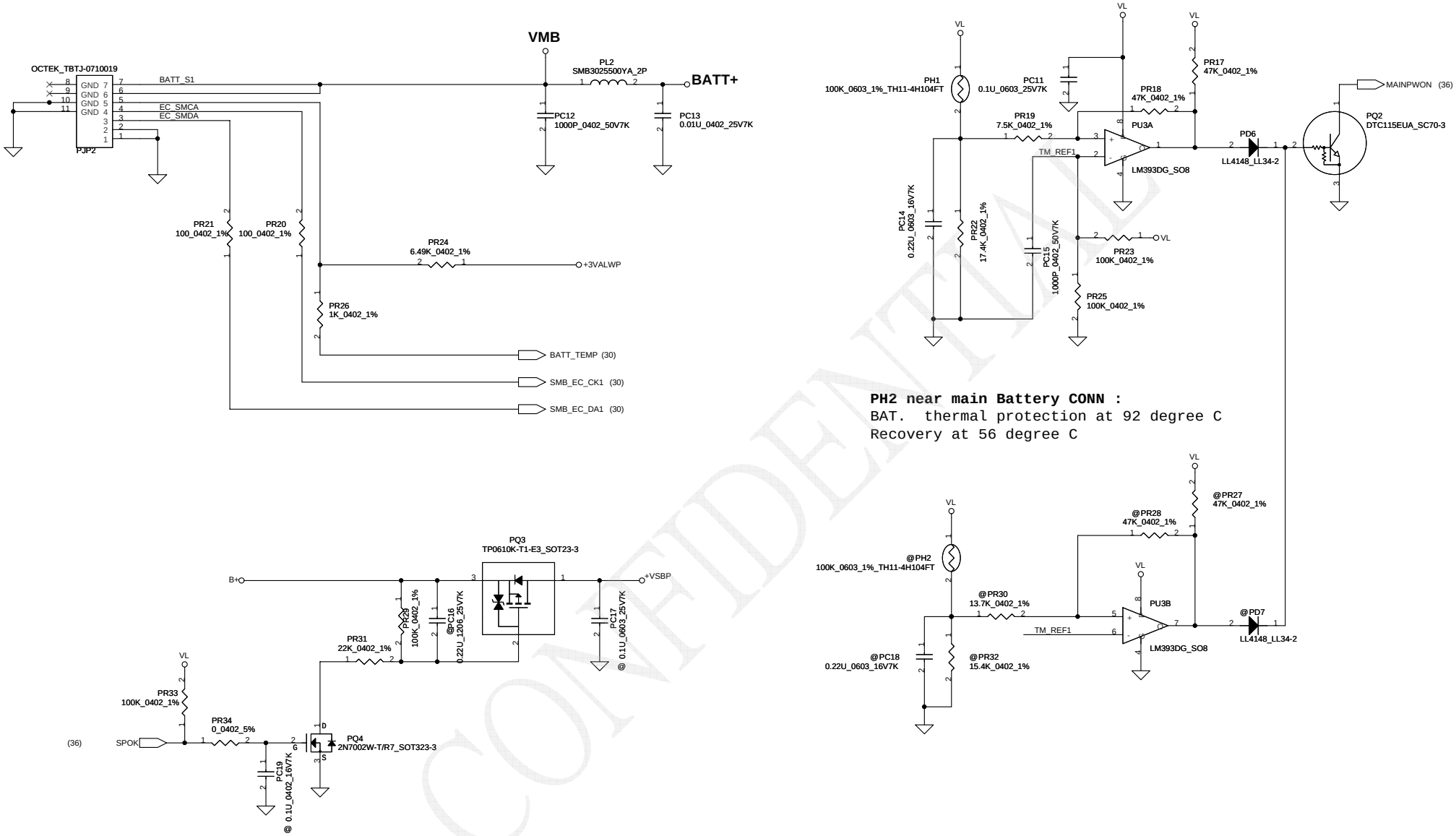
PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C

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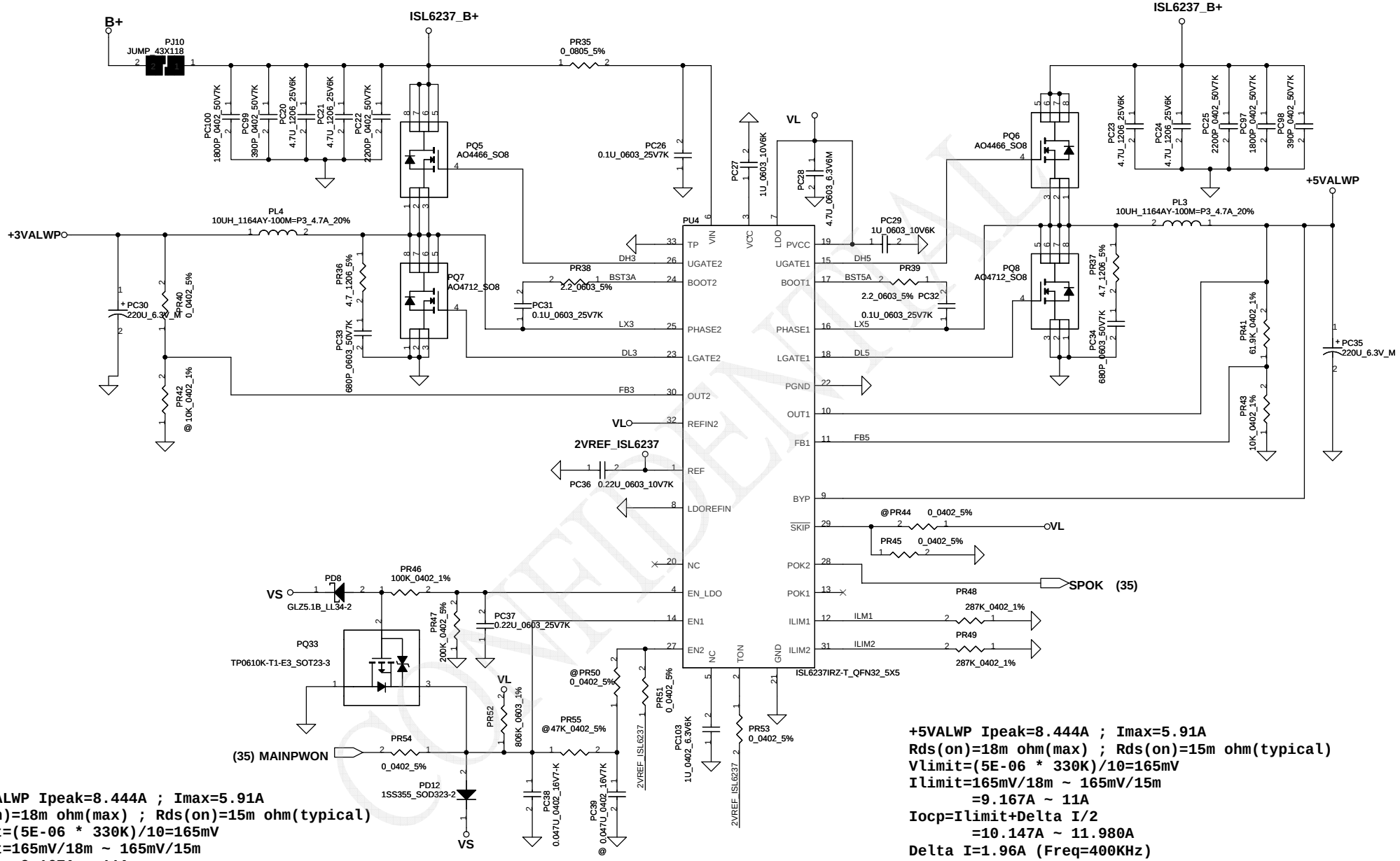

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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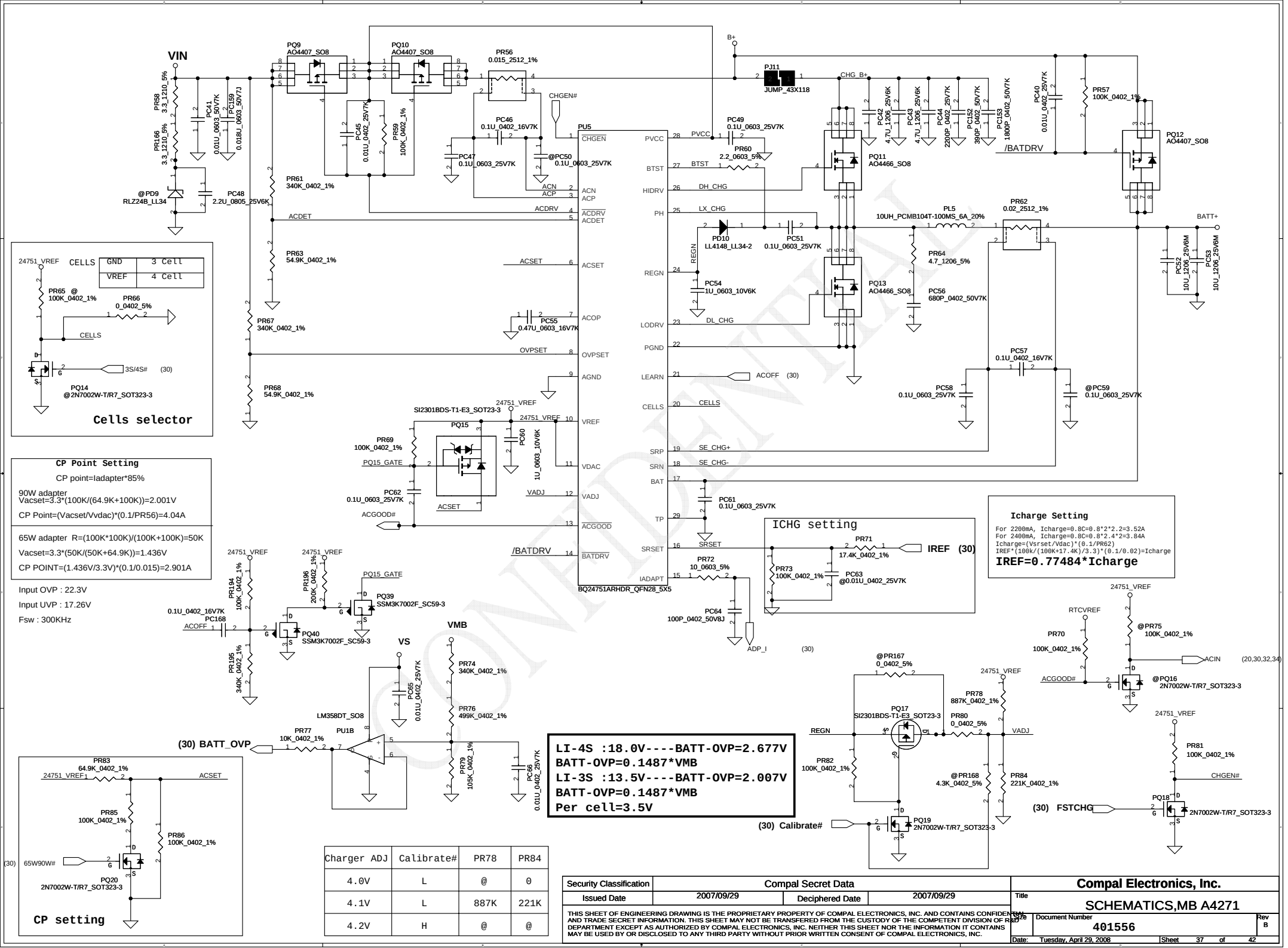

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	@	@

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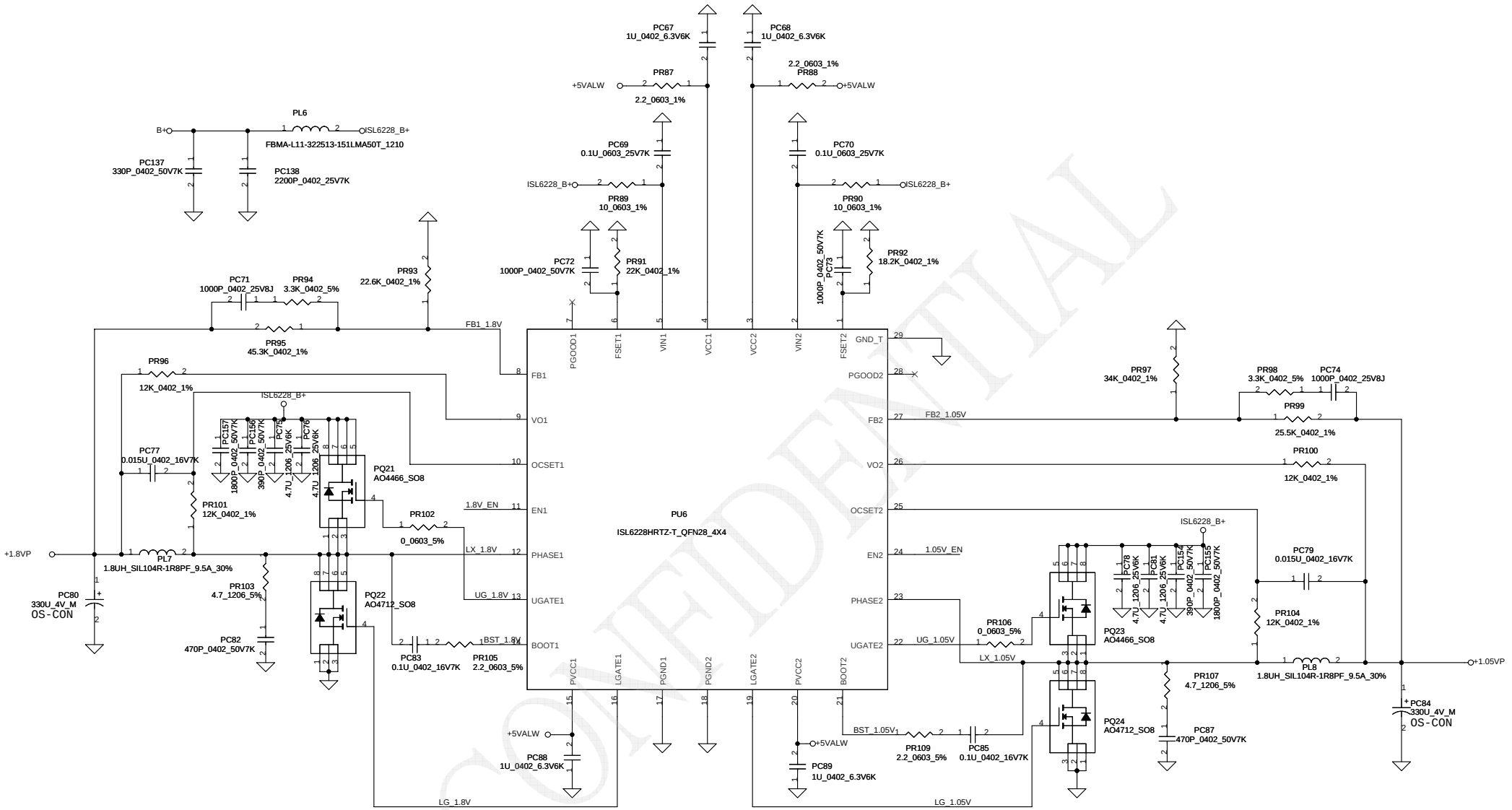

1.8VP Ipeak=9.45A ; Imax=6.615A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=12K ohm
Iocp=12A
Csen=L/(Rocset*DCR)=0.015uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.05VP Ipeak=8.8A ; Imax=6.16A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=12K ohm
Iocp=12A
Csen=L/(Rocset*DCR)=0.015uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

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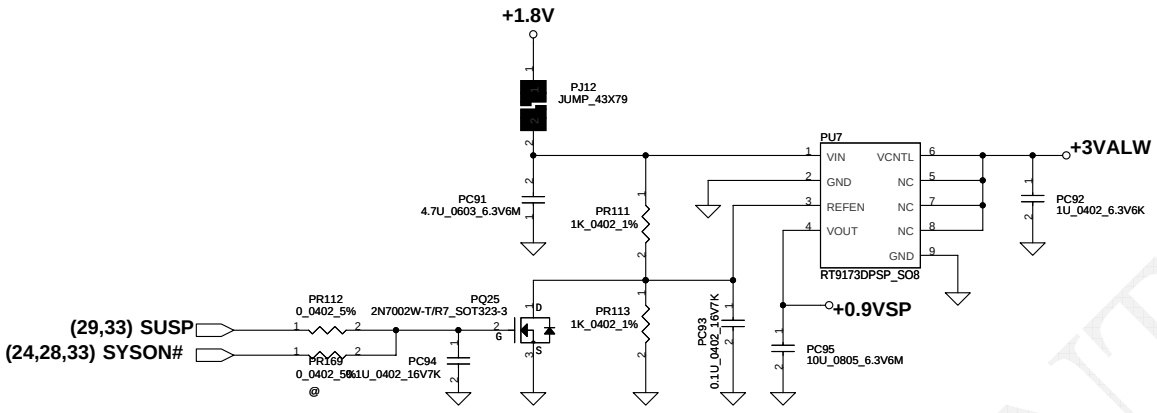

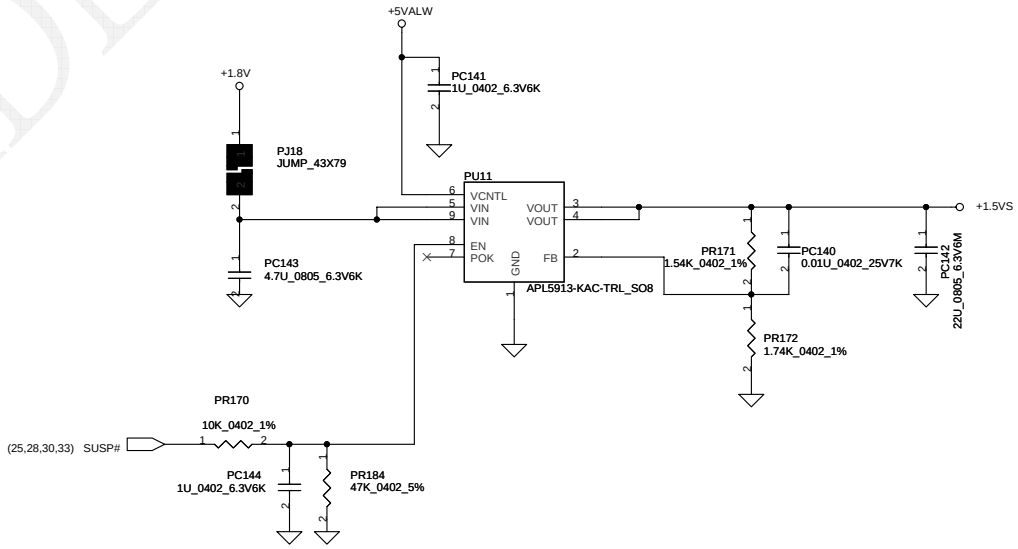

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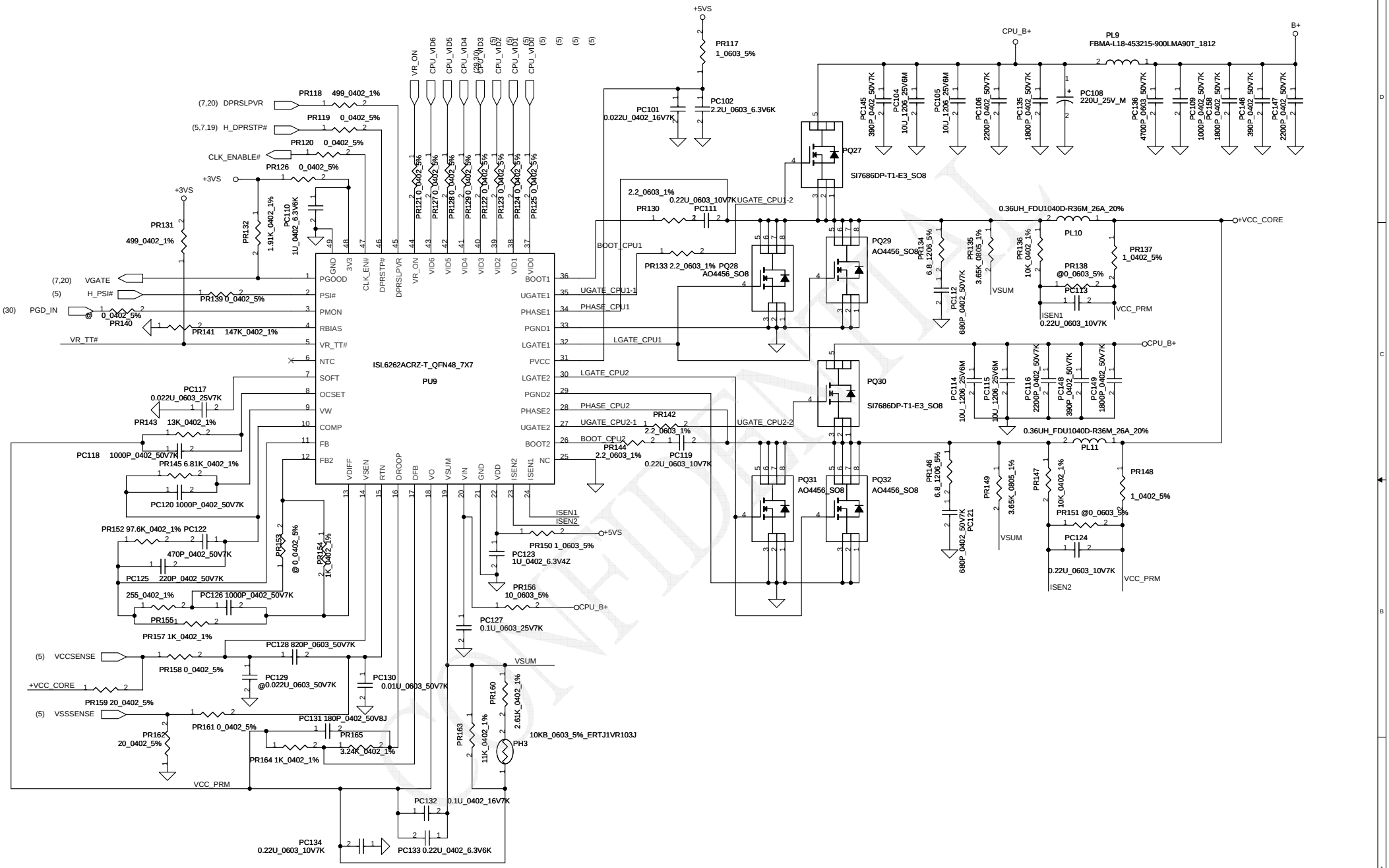

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Exchange battery connector pin	Use wrong model		35	Swap pin definition of PJP2	2007 12/12	EVT
2		For 2nd source of ISL6237		36	Add PC103 SE107105M80(S CER CAP 1U 6.3V M X5R 0603) on pin 5 of PU4	2007 12/12	EVT
3		Some risk in heavy load		37	Change PL5 to SH000005Z80(S COIL 10UH +-20% PCMB104T-100MS 6A)	2007 12/12	EVT
4		For EN function of PU4		36	Add PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K) on pin 3 of PQ33 to VS	2007 12/12	EVT
5		Down size		36	Change PC38 from 0603 to 0402(SE076473K80)	2007 12/12	EVT
6		Down size		34	Change PC7 from 1206 to 0603(SE000005Z80)	2007 12/12	EVT
7		Down size		37	Change PC49 from 0805 to 0603(SE042104K80)	2007 12/12	EVT
8		Down size		36	Change PC28 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
9		Down size		39	Change PC91 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
10		Down size		39	Change PC96 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
11		Down size		39	Change PC92 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
12		Down size		39	Change PC97 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
13		Down size		40	Change PC110 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
14		Down size		35	Change PC14 from 0805 to 0603(SE026224K80)	2007 12/12	EVT
15		Down size		35	Change PC18 from 0805 to 0603(SE026224K80)	2007 12/12	EVT
16		For EMI		34	Add PC107 SE075472K80(S CER CAP 4700P 25V K X7R 0402) from VIN to GND	2007 12/12	EVT
17		For EMI		34	Add PC139 SE074331K80(S CER CAP 330P 50V K X7R 0402) from VIN to GND	2007 12/12	EVT
18		For EMI		40	Add PC135 SE074182K80(S CER CAP 1800P 50V K X7R 0402) from CPU_B+ to GND	2007 12/12	EVT
19		For EMI		40	Add PC136 SE025472K80(S CER CAP 4700P 50V K X7R 0603) from B+ to GND	2007 12/12	EVT
20		For EMI		38	Add PR103 SD001470B80(S RES 1/4W 4.7 +-5% 1206) from pin 12 of PU6 to PC82	2007 12/12	EVT
21		For EMI		38	Add PC82 SE074471K80(S CER CAP 470P 50V K X7R 0402) from PR103 to GND	2007 12/12	EVT
22		For EMI		38	Add PR107 SD001470B80(S RES 1/4W 4.7 +-5% 1206) from pin 23 of PU6 to PC82	2007 12/12	EVT
23		For EMI		38	Add PC87 SE074471K80(S CER CAP 470P 50V K X7R 0402) from PR107 to GND	2007 12/12	EVT

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24		For more current		34	Change PD11 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/12	EVT
25		Space is not enough		34	Delete PD1	2007 12/18	EVT
26				37	Change PR70 Pin 1 to RTCVREF	2007 12/18	EVT
27		Down size		37	Change PC56 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
28		Down size		40	Change PC112 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
29		Down size		40	Change PC121 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
30		Down size		36	Change PC103 from 0603 to 0402(SE000000K80)	2007 12/18	EVT
31		Down size		40	Change PC128 from 0603 to 0402(SE000003W00)	2007 12/20	EVT
32	~~APL5913 EN pin impedance must keep under 20K~~	~~For APL5913 EN risk~~		~~39~~	~~Change PR184 from 47K to 20K(SD028200280)~~	~~2007 12/31~~	~~EVT~~
33		Improve 3V/5V OCP		36	Change PR48、PR49 from 330K to 287K(SD000005D80) Change PL3、PL4 from 4.7uH to 10uH(SH000008R80)	2008 02/25	DVT
34		Improve Load line		40	Change PR165 from 4.42K to 3.24K(SD034324180)	2008 02/25	DVT
35		For EMI		34	Add PC96 1000pF(SE074102K80)	2008 02/25	DVT
36		For EMI			Add PC97、PC98、PC99、PC100、PC145、PC146、PC147、PC148、PC149、PC150、PC151、PC152、PC153、PC154、PC155、PC156、PC157 ~~Delete PR64、PC56 "@" mark~~	2008 02/27	DVT
37					Change PR38、PR39、PR60、PR105、PR109、PR130、PR144 from 0 to 2.2		
38		Prevent ACOP issue		37	Add PC168、PQ39、PQ40、PR194、PR195、PR196	2008 02/27	DVT
39		HW request		39	Change PC144 to 1uF , delete PR184 "@" mark	2008 02/27	DVT
40		For EMI			Add PC158、PC159	2008 03/03	DVT
41		Thermal request		35	Change PR19 from 13.7K to 7.5K (SD034750180) Change PR22 from 15.4K to 17.4K (SD034174280)	2008 03/14	PVT1
42							
43							
44							
45							
46							

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