Compal confidential

Liverpool 10AR/10ARG

KSWAE LA-4971P Schematics Document

Mobile AMD S1G2 S1G3/
RS780MN & RS780MC & RX781 & RS880 /
SB700 & SB710

2009-04-22 Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Title: *Cover Sheet*

Size: Custom | Document Number: *LA-4971P* | Rev: 1.0

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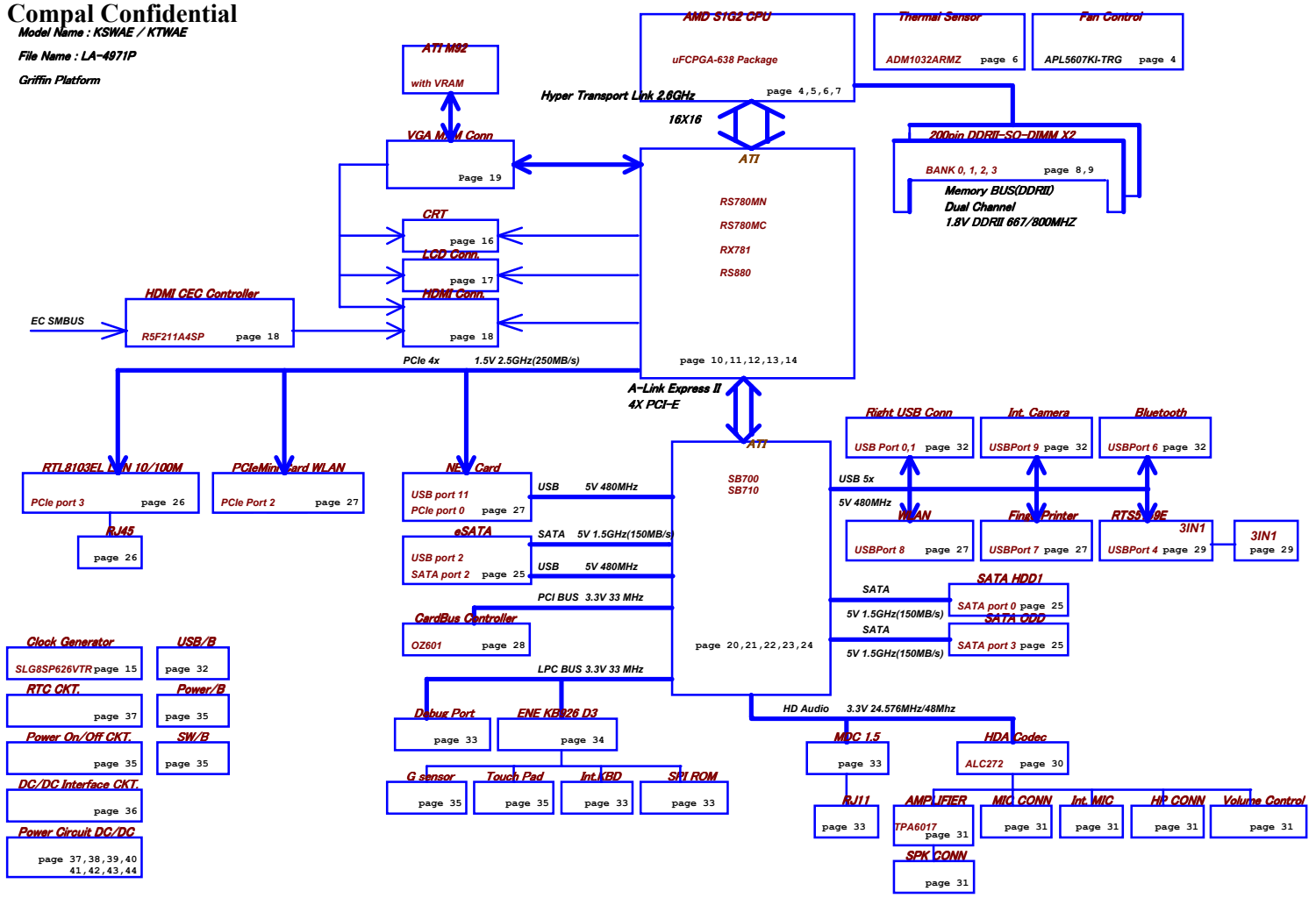
Model Name : KSWAE / KTWAE

File Name : LA-4971P

Griffin Platform



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Title: **Block Diagram**

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Voltage Rails

O : ON
X : OFF

State \ power plane	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D2		

EC SM Bus2 address

Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D2		
Ext. VGA/B		
CS/B		

Symbol Note :

: Digital Ground

: Analog Ground

@ : just reserve , no build

DEBUG@ : reserve for debug.

Layout Notes

UMA@: means for RS780M.

Platform	Item	CPU	NB	VGA	SB	Comment
PUMA@	GM@	S1G2	RS780MC	NA	SB700	
	GM@	S1G2	RS780MN	NA	SB700	
	PM@+GPM@	S1G2	RS780MN	MXM	SB700	
	PM@+PM1@	S1G2	RX781	MXM	SB700	

Platform	Item	CPU	NB	VGA	SB	Comment
TIGRIS@	GM@	S1G3	RS880MC	NA	SB710	
	GM@	S1G3	RS880M	NA	SB710	
	PM@+GPM@	S1G3	RS880M	MXM	SB710	
	PM@+PM1@	S1G3	RX881	MXM	SB710	

BTO (Build-To-Order) Option Table

Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD		WiFi		G- sensor		3 in 1 card reader
Description	(E / A)	(B)	(R)	(S)			(H)				
Explain					16"	17"	Half - size		First	Second	RTS5159
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@	WIMAX@	G@ + G_1st@	G@ + G_2nd@	CARD@

Function	FingerPrinter	CAMERA & MIC		HDMI			LVDS wireset	DC-IN		CHIPSET		
Description	(F)	(X)		(Y)								
Explain		CAMERA	MIC	AMD(UMA)	ATI VGA/B	COMMON	Cost down					
BTO	FP@	CAM@	MIC@	IHDMI@	HDMI@	H@	LVDSSET@	16inch_45@	17inch_45@	PUMA@	TIGRIS@	

SMBUS Control Table

	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD	MXM Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	KB926		V	V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V							V
I2C_CLK I2C_DATA	RS780M								V			
DDC_CLK0 DDC_DATA0	RS780M									V		
DDC_CLK1 DDC_DATA1	RS780M											
SCL0 SDA0	SB700					V	V				V	
SCL1 SDA1	SB700							V				
SCL2 SDA2	SB700											
SCL3 SDA3	SB700											

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Title: Notes List

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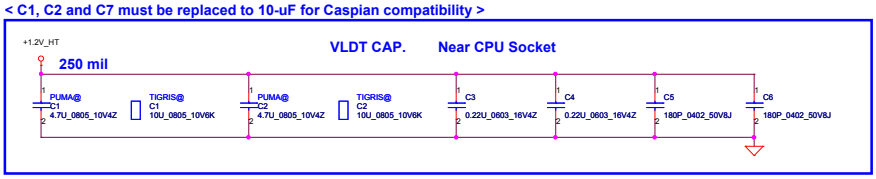
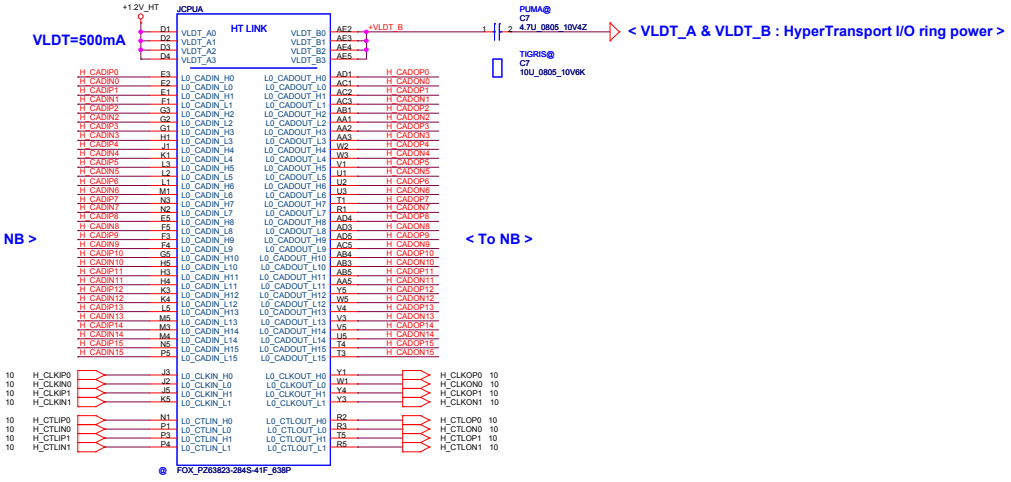
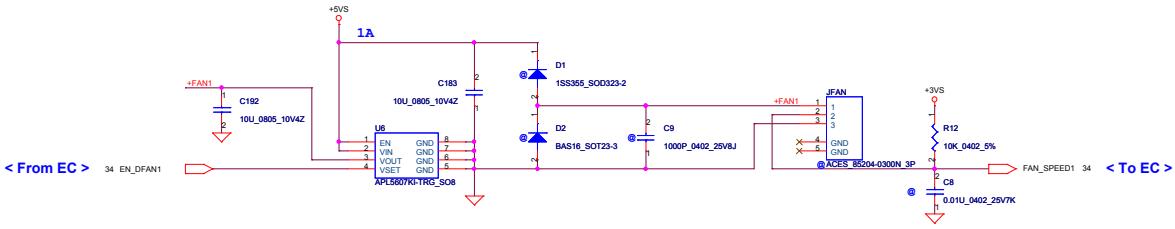
< C1, C2 and C7 must be replaced to 10-uF for Caspian compatibility >





< FAN Control Circuit : Vout = 1.6 x Vset >



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Title: **AMD CPU S1G2 HT I/F**

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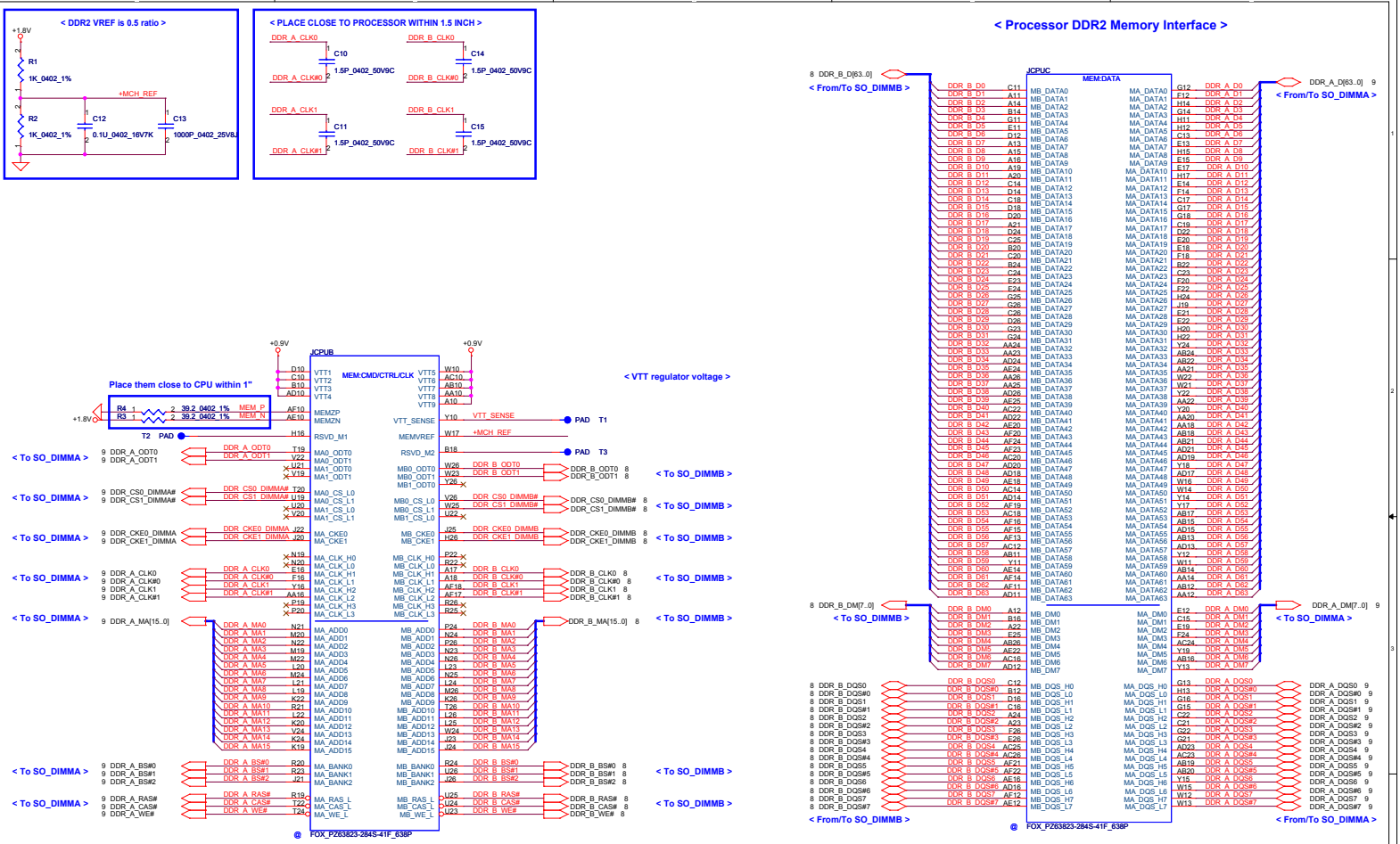
< Processor DDR2 Memory Interface >



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Compal Electronics, Inc.

Title: **AMD CPU S1G2 DDRII I/F**

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< Close to CPU >

+CPU_CORE_0
R487 10_0402_5% CPU_VDD0_RUN_FB_H
R486 10_0402_5% CPU_VDD0_RUN_FB_L

+CPU_CORE_1
Un-Mount R489 For Caspian
R489 PUMA@ 10_0402_5% CPU_VDD1_RUN_FB_H
R488 PUMA@ 10_0402_5% CPU_VDD1_RUN_FB_L

Change R488 to 10K For Caspian

< Differential feedback for VDDNB >
Close to CPU
+VDDNB
R484 10_0402_5% CPU_VDDNB_RUN_FB_H
R485 10_0402_5% CPU_VDDNB_RUN_FB_L

< Sideband-Temperature Sensor Interface Clock & Data>
< Sideband-Temperature Sensor Interface Interrupt >
< Compensation Resistor to VSS >
< Compensation Resistor to VLDT >
R13 44.2 0402 1% CPU_HTREF0
R14 44.2 0402 1% CPU_HTREF1
+1.2V_HT

JCPUD

Pin	Signal	Pin	Signal
F8	+2.5VDDA	M11	KEY1
F9	VDDA1 / VDDA2	W18	KEY2
A9	CPU_CLKIN_SC_P	A6	SVC / CPU_SVC 43
A8	CPU_CLKIN_SC_N / CLKIN_H / CLKIN_L	A4	SVD / CPU_SVD 43
B7	LDT_RST# / RESET_L	AF8	THERMTRIP_L / CPU_THERMTRIP# R
A7	H_PWRGD / PWROK	AC7	PROCHOT_L / CPU_PROCHOT# 1,8
F10	LDT_STOP# / LDTSTOP_L	AA8	MEMHOT_L / R42 300_0402_5% +1.8V
C6	CPU_LDT_REQ_R# / LDTREQ_L	W7	THERMDC / CPU_THERMDC
AF4	SIC	W8	THERMDA / CPU_THERMDA
AF5	SID	W9	+1.8V sense no support
AE6	ALERT_L	Y9	
R6	CPU_HTREF0 / HT_REF0	H6	VDDNB_FB_H / CPU_VDDNB_RUN_FB_H 43
P8	CPU_HTREF1 / HT_REF1	G6	VDDNB_FB_L / CPU_VDDNB_RUN_FB_L 43
F6	CPU_VDD0_RUN_FB_H / VDD0_FB_H	E10	DBREQ_L / CPU_DBREQ#
E6	CPU_VDD0_RUN_FB_L / VDD0_FB_L	AE9	TDO
Y6	CPU_VDD1_RUN_FB_H / VDD1_FB_H	J7	TEST28_H / CPU_TEST28_H_PLLCHRZ_P
AB6	CPU_VDD1_RUN_FB_L / VDD1_FB_L	H8	TEST28_L / CPU_TEST28_L_PLLCHRZ_N
G10	DBRDY	D7	TEST17 / CPU_TEST17_BP3
A9	TMS	E7	TEST16 / CPU_TEST16_BP2
AC9	TCK	E7	TEST15
AD9	TRST_L	C7	TEST14
AF9	TDI	C3	TEST7
AD7	TEST23 / CPU_TEST23_TSTUPD	K8	TEST10 / CPU_TEST10_ANALOGOUT
H10	TEST18	C4	TEST8
G9	TEST19	C9	TEST29_H / CPU_TEST29_H_FBCLKOUT_P
E9	TEST25_H / CPU_TEST25_H_BYPASSCLK_H	C8	TEST29_L / CPU_TEST29_L_FBCLKOUT_N
E8	TEST25_L / CPU_TEST25_L_BYPASSCLK_L	H18	RSVD10
AB8	TEST21 / CPU_TEST21_SCANEN	H19	RSVD9
AF7	TEST20 / CPU_TEST20_SCANCLK2	AA7	RSVD8
AE7	TEST24 / CPU_TEST24_SCANCLK1	D5	RSVD7
AE8	TEST22	C5	RSVD6
AC8	TEST12	A3	RSVD1
AF8	TEST27	A5	RSVD2
C2	TEST9 / R25 0_0402_5%	B3	RSVD3
AA6	TEST6	B5	RSVD4
		C1	RSVD5

@ FOX_PZ63823-284S-41F_638P

< Debug ready >
< JTAG debug port >
T9 PAD
T10 PAD
T11 PAD
T12 PAD
T19 PAD

< Serial VID Interface clock & data >
< Thermal Sensor Trip output >
< HTC-active state indication or command >
< Thermal diode cathode & anode >
< Differential feedback for VDDIO >
< VDDIO : DDR SDRAM I/O ring power supply>
< Differential feedback for VDDNB >
< Northbridge power supply >
< Debug request >
PAD T22
PAD T21
PAD T20
PAD T5
PAD T6
PAD T7
PAD T8
PAD T13
PAD T14
route as differential as short as possible testpoint under package
@R32 300_0402_5% +1.2V_HT
Add R32 at PVT

< 200-MHz PLL Reference Clock >
15 CLK_CPU_BCLK
C20 3900P_0402_50V7K CPU_CLKIN_SC_P
R8 169_0402_1%
15 CLK_CPU_BCLK#
C21 3900P_0402_50V7K CPU_CLKIN_SC_N
Address:100_1100 Place close to CPU wihtin 1.5"

< Filtered PLL Supply Voltage >
+2.5VS
L1 FBM_L11_201209_300L_0805
VDDA=300mA
+2.5VDDA
@ C16 100U_D2_6.3VM
C17 4.7U_0805_10V4Z
C18 3300P_0402_50V7K
C19 0.22U_0603_16V4Z

< Serial VID Interface clock & data >
+1.8VS
0718 AMD --> 1K ohm
R22 1K_0402_5% CPU_SVC
R23 1K_0402_5% CPU_SVD

Add R497 and R498 at PVT
+1.8V
TIGRIS@ R497 510_0402_5% CPU_TEST25_H_BYPASSCLK_H @ R498 510_0402_5%
@ R499 510_0402_5% CPU_TEST25_L_BYPASSCLK TIGRIS@ R500 510_0402_5%

+1.8VS
R15 300_0402_5%
20 LDT_RST# LDT_RST#
@ C22 0.01U_0402_25V7K

+1.8VS
R21 300_0402_5%
20,43 H_PWRGD H_PWRGD
C23 0.1U_0402_16V7K

+1.8VS
R36 300_0402_5%
11,20 LDT_STOP# LDT_STOP#
@ C25 0.01U_0402_25V7K

+1.8VS
R30 300_0402_5%
11,20 CPU_LDT_REQ# CPU_LDT_REQ#
PUMA@ R27 0_0402_5% CPU_LDT_REQ_R#
C24 0.01U_0402_25V7K @
Un-Mount R27 For Caspian

+1.8V
R10 10K_0402_5%
R5 300_0402_5%
CPU_THERMTRIP# R
Q3 MMBT3904_NL_SOT23-3
@D12 CH751H-40PT_SOD323-2 < To power circuitry> ENTRIP2 38,40
@D20 CH751H-40PT_SOD323-2 < To power circuitry> EN0 37,40
D16 CH751H-40PT_SOD323-2 < To SB700 ACPI block> H_THERMTRIP# 21

+1.8V
R9 300_0402_5%
CPU_PROCHOT# 1,8
@ R11 0_0402_5%
< To SB700 CPU block> H_PROCHOT# 20

Add R29 and R31 at PVT
TIGRIS@ R31 300_0402_5% CPU_TEST20_SCANCLK2
TIGRIS@ R29 300_0402_5% CPU_TEST23_TSTUPD
R26 300_0402_5% CPU_TEST21_SCANEN
R28 300_0402_5% CPU_TEST24_SCANCLK1

< HDT Connector >
< R41 Close to CPU > < R494 Close to CPU >
CPU_DBREQ#
+1.8V T23 PAD R41 300_0402_5% @ R494 0_0402_5%
@ R40 220_0402_5%
@ R39 220_0402_5%
@ R38 220_0402_5%
@ R37 220_0402_5%
+1.8V T24 PAD
+1.8V LDT_RST#
JP3 @ SAMTEC_ASP-68200-07
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

< Thermal Sensor >
+3VS
C26 0.1U_0402_16V7K
U2 ADM1032ARM-1 2REEL_MSOP8
VDD, D+, D-, THERM#, SCLK, SDATA, ALERT#, GND
THERMDA_CPU
C27 2200P_0402_50V7K THERMDC_CPU
< noise filter cap >
< From EC >
EC_SMB_CK2 EC_SMB_CK2 19,34,35
EC_SMB_DA2 EC_SMB_DA2 19,34,35

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Title: AMD CPU S1G2 CTRL
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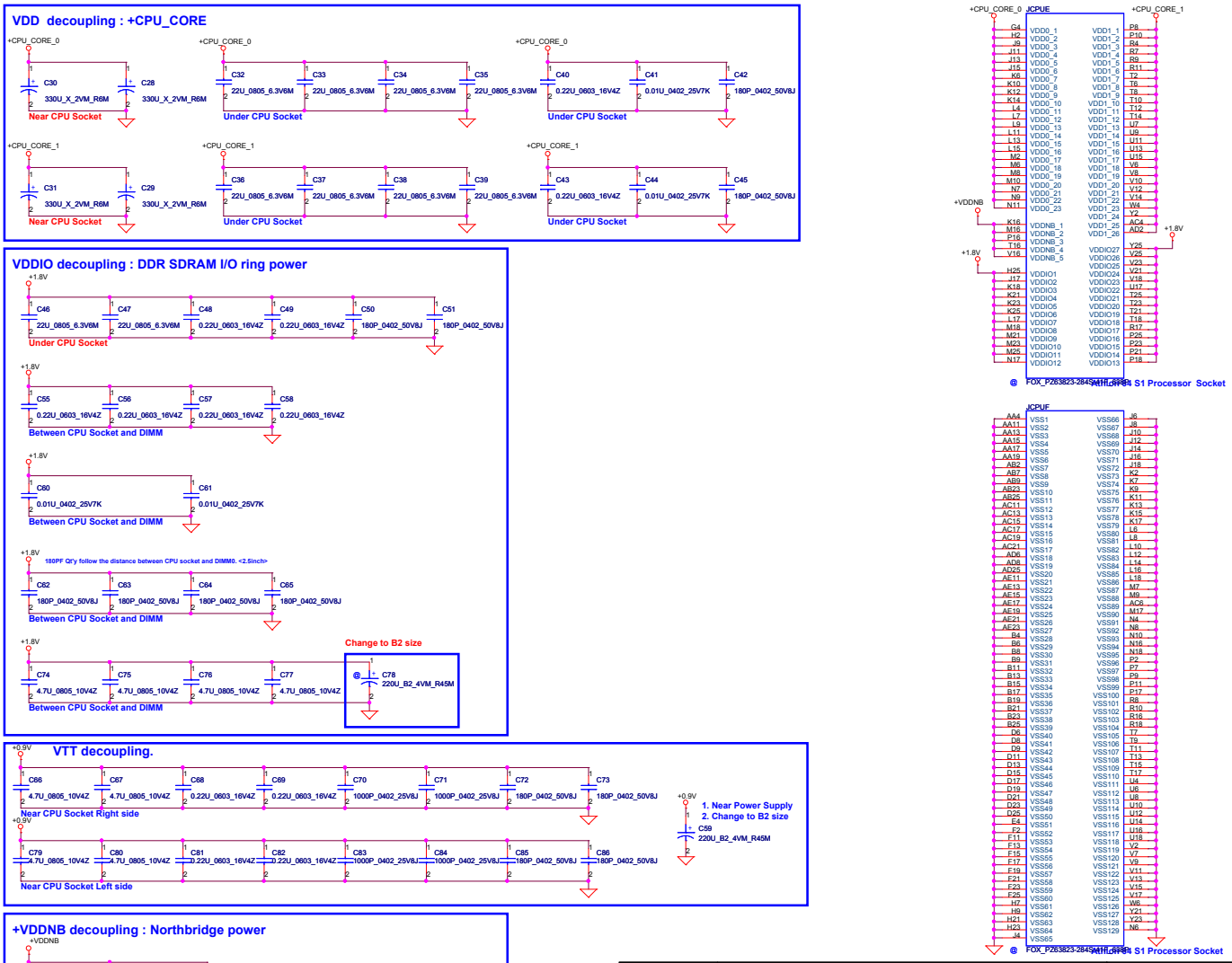

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Title: AMD CPU S1G2 PWR & GND

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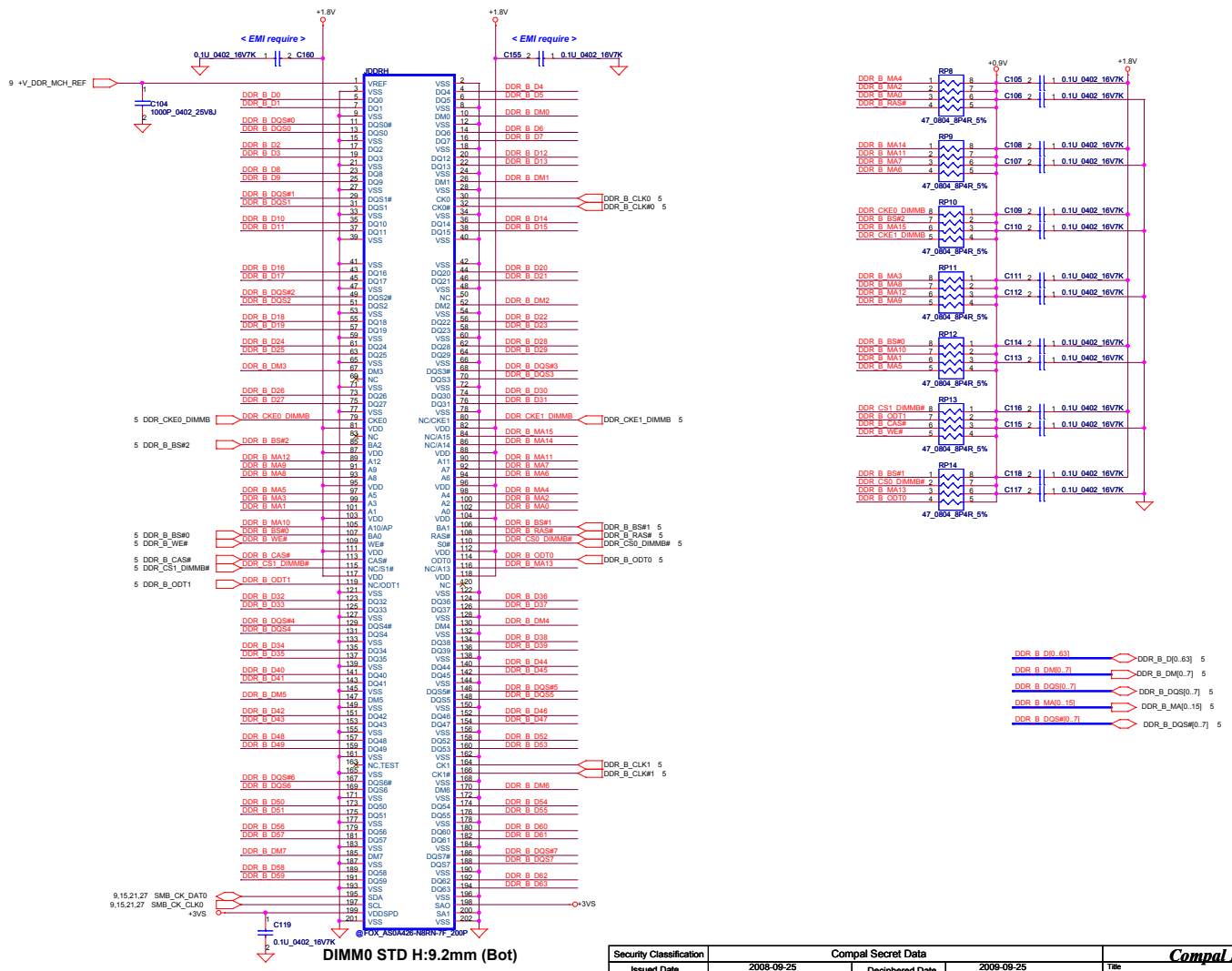

DIMM0 STD H:9.2mm (Bot)

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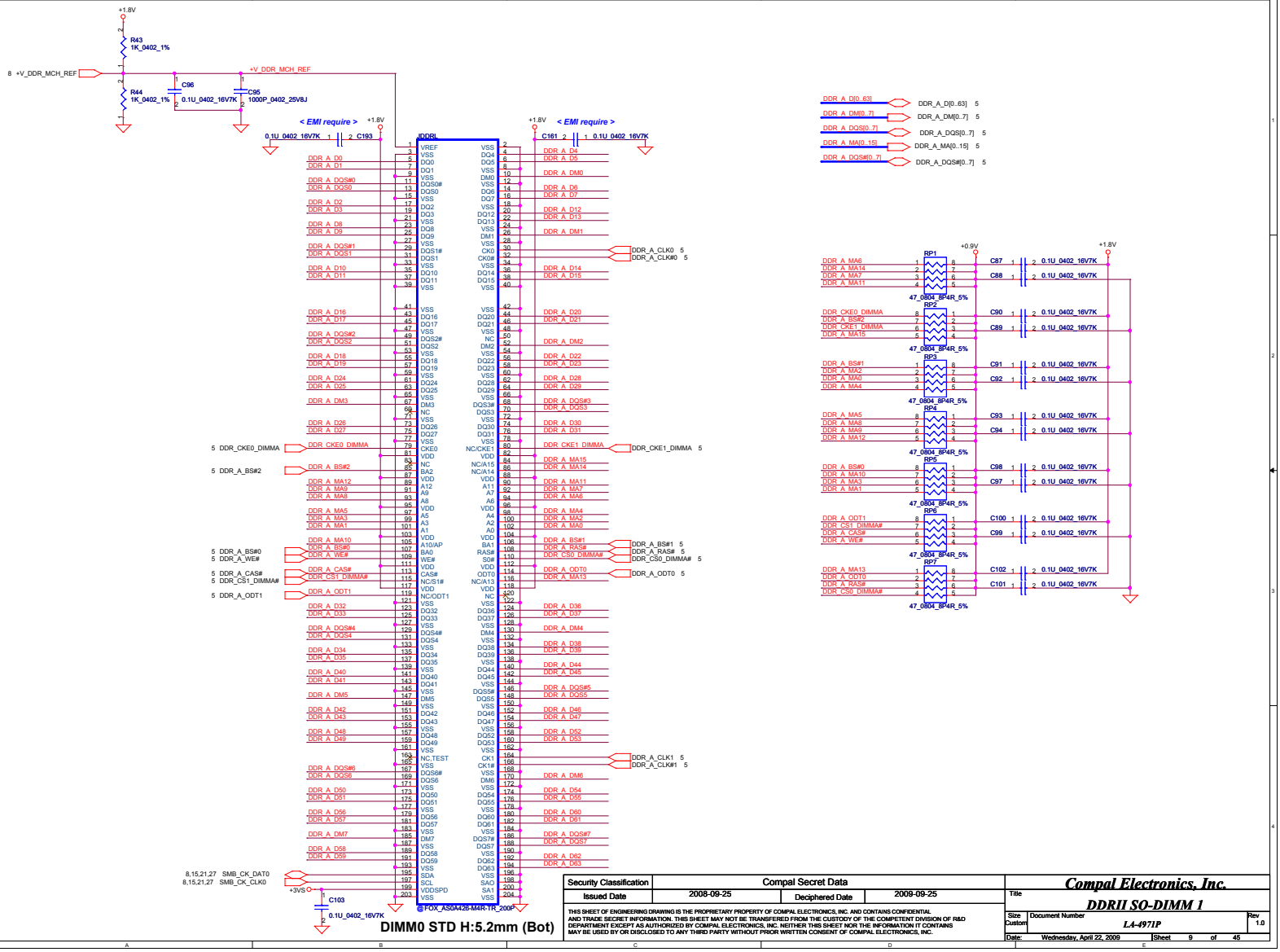

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Title: **DDRII SO-DIMM 1**

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U3B GM : RS780MN & RS780MC, PM : RX781

PCIE I/F GFX (PART 2 OF 6)

< From MXM VGA board >

Signal	Pin	Polarity inversion
PCIE_GTX_C_MRX_P[0..15] / PCIE_GTX_C_MRX_N[0..15]	PCIE_GTX_C_MRX_P[0..15] 19 / PCIE_GTX_C_MRX_N[0..15] 19	
PCIE_GTX_C_MRX_N0	D4	Polarity inversion
PCIE_GTX_C_MRX_P0	C4	
PCIE_GTX_C_MRX_P1	A3	
PCIE_GTX_C_MRX_N1	B3	
PCIE_GTX_C_MRX_N2	C2	Polarity inversion
PCIE_GTX_C_MRX_P2	C1	
PCIE_GTX_C_MRX_N3	E5	Polarity inversion
PCIE_GTX_C_MRX_P3	F5	
PCIE_GTX_C_MRX_N4	G5	Polarity inversion
PCIE_GTX_C_MRX_P4	G6	
PCIE_GTX_C_MRX_N5	H5	Polarity inversion
PCIE_GTX_C_MRX_P5	H6	
PCIE_GTX_C_MRX_N6	J6	
PCIE_GTX_C_MRX_P6	J5	
PCIE_GTX_C_MRX_N7	J7	Polarity inversion
PCIE_GTX_C_MRX_P7	J8	
PCIE_GTX_C_MRX_N8	L5	Polarity inversion
PCIE_GTX_C_MRX_P8	L6	
PCIE_GTX_C_MRX_N9	M6	Polarity inversion
PCIE_GTX_C_MRX_P9	L8	
PCIE_GTX_C_MRX_N10	P7	Polarity inversion
PCIE_GTX_C_MRX_P10	M7	
PCIE_GTX_C_MRX_N11	P5	Polarity inversion
PCIE_GTX_C_MRX_P11	M5	
PCIE_GTX_C_MRX_N12	R8	Polarity inversion
PCIE_GTX_C_MRX_P12	P8	
PCIE_GTX_C_MRX_N13	R6	Polarity inversion
PCIE_GTX_C_MRX_P13	R5	
PCIE_GTX_C_MRX_N14	P4	Polarity inversion
PCIE_GTX_C_MRX_P14	P3	
PCIE_GTX_C_MRX_N15	T4	Polarity inversion
PCIE_GTX_C_MRX_P15	T3	

GFX_RX0P, GFX_RX0N, GFX_RX1P, GFX_RX1N, GFX_RX2P, GFX_RX2N, GFX_RX3P, GFX_RX3N, GFX_RX4P, GFX_RX4N, GFX_RX5P, GFX_RX5N, GFX_RX6P, GFX_RX6N, GFX_RX7P, GFX_RX7N, GFX_RX8P, GFX_RX8N, GFX_RX9P, GFX_RX9N, GFX_TX10P, GFX_TX10N, GFX_RX11P, GFX_RX11N, GFX_RX12P, GFX_RX12N, GFX_RX13P, GFX_RX13N, GFX_RX14P, GFX_RX14N, GFX_RX15P, GFX_RX15N

GFX_TX0P, GFX_TX0N, GFX_TX1P, GFX_TX1N, GFX_TX2P, GFX_TX2N, GFX_TX3P, GFX_TX3N, GFX_TX4P, GFX_TX4N, GFX_TX5P, GFX_TX5N, GFX_TX6P, GFX_TX6N, GFX_TX7P, GFX_TX7N, GFX_TX8P, GFX_TX8N, GFX_TX9P, GFX_TX9N, GFX_TX10P, GFX_TX10N, GFX_TX11P, GFX_TX11N, GFX_TX12P, GFX_TX12N, GFX_TX13P, GFX_TX13N, GFX_TX14P, GFX_TX14N, GFX_TX15P, GFX_TX15N

Signal	Pin	Capacitor	Value
PCIE_MTX_C_GRX_P0	A5	PM@ C120	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N0	B5	PM@ C121	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P1	A4	PM@ C122	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N1	B4	PM@ C123	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P2	C3	PM@ C124	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N2	B2	PM@ C125	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P3	D1	PM@ C126	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N3	D2	PM@ C127	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P4	E2	PM@ C128	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N4	E1	PM@ C129	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P5	F4	PM@ C130	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N5	F3	PM@ C131	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P6	F1	PM@ C132	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N6	F2	PM@ C133	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P7	H4	PM@ C134	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N7	H3	PM@ C135	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P8	H1	PM@ C136	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N8	H2	PM@ C137	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P9	J2	PM@ C138	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N9	J1	PM@ C139	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P10	K4	PM@ C140	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N10	K3	PM@ C141	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P11	K1	PM@ C142	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N11	K2	PM@ C143	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P12	M4	PM@ C144	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N12	M3	PM@ C145	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P13	M1	PM@ C146	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N13	M2	PM@ C147	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P14	N2	PM@ C148	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N14	N1	PM@ C149	0.1U 0402 16V7K
PCIE_MTX_C_GRX_P15	P1	PM@ C150	0.1U 0402 16V7K
PCIE_MTX_C_GRX_N15	P2	PM@ C151	0.1U 0402 16V7K

< To MXM VGA board >

Signal	Pin	Polarity inversion
PCIE_MTX_C_GRX_P[0..15] / PCIE_MTX_C_GRX_N[0..15]	PCIE_MTX_C_GRX_P[0..15] 19 / PCIE_MTX_C_GRX_N[0..15] 19	
PCIE_MTX_C_GRX_N0		Polarity inversion
PCIE_MTX_C_GRX_P0		
PCIE_MTX_C_GRX_N1		Polarity inversion
PCIE_MTX_C_GRX_P1		
PCIE_MTX_C_GRX_N2		
PCIE_MTX_C_GRX_P2		
PCIE_MTX_C_GRX_N3		Polarity inversion
PCIE_MTX_C_GRX_P3		
PCIE_MTX_C_GRX_N4		
PCIE_MTX_C_GRX_P4		
PCIE_MTX_C_GRX_N5		
PCIE_MTX_C_GRX_P5		
PCIE_MTX_C_GRX_N6		
PCIE_MTX_C_GRX_P6		
PCIE_MTX_C_GRX_N7		
PCIE_MTX_C_GRX_P7		
PCIE_MTX_C_GRX_N8		
PCIE_MTX_C_GRX_P8		
PCIE_MTX_C_GRX_N9		
PCIE_MTX_C_GRX_P9		
PCIE_MTX_C_GRX_N10		
PCIE_MTX_C_GRX_P10		
PCIE_MTX_C_GRX_N11		
PCIE_MTX_C_GRX_P11		
PCIE_MTX_C_GRX_N12		Polarity inversion
PCIE_MTX_C_GRX_P12		
PCIE_MTX_C_GRX_N13		
PCIE_MTX_C_GRX_P13		
PCIE_MTX_C_GRX_N14		Polarity inversion
PCIE_MTX_C_GRX_P14		
PCIE_MTX_C_GRX_N15		
PCIE_MTX_C_GRX_P15		

PCIE I/F GPP

< To New Card >

Signal	Pin	Capacitor	Value
27 PCIE_PTX_C_IRX_P0	AE3	C152	0.1U 0402 16V7K
27 PCIE_PTX_C_IRX_N0	AD4	C153	0.1U 0402 16V7K
	AE2		
	AD3		
	AD1		
27 PCIE_PTX_C_IRX_P2	AD2		
27 PCIE_PTX_C_IRX_N2	Y5		
26 PCIE_PTX_C_IRX_P3	W6		
26 PCIE_PTX_C_IRX_N3	U5		
	U6		
	U8		
	U7		

GPP_RX0P, GPP_RX0N, GPP_RX1P, GPP_RX1N, GPP_RX2P, GPP_RX2N, GPP_RX3P, GPP_RX3N, GPP_RX4P, GPP_RX4N, GPP_RX5P, GPP_RX5N

GPP_TX0P, GPP_TX0N, GPP_TX1P, GPP_TX1N, GPP_TX2P, GPP_TX2N, GPP_TX3P, GPP_TX3N, GPP_TX4P, GPP_TX4N, GPP_TX5P, GPP_TX5N

Signal	Pin	Capacitor	Value
PCIE_ITX_C_PRX_P0	AC1	C152	0.1U 0402 16V7K
PCIE_ITX_C_PRX_N0	AC2	C153	0.1U 0402 16V7K
	AB4		
	AB3		
PCIE_ITX_C_PRX_P2	AA2	WLAN@ C156	0.1U 0402 16V7K
PCIE_ITX_C_PRX_N2	AA1	WLAN@ C157	0.1U 0402 16V7K
PCIE_ITX_C_PRX_P3	Y1	C158	0.1U 0402 16V7K
PCIE_ITX_C_PRX_N3	Y2	C159	0.1U 0402 16V7K
	Y4		
	Y3		
	V1		
	V2		

< To New Card >

< To WLAN >

< To LAN >

Signal	Pin
PCIE_ITX_C_PRX_P0	27
PCIE_ITX_C_PRX_N0	27
PCIE_ITX_C_PRX_P2	27
PCIE_ITX_C_PRX_N2	27
PCIE_ITX_C_PRX_P3	26
PCIE_ITX_C_PRX_N3	26

PCIE I/F SB

< From SB700 : x4 PCIE A-link >

Signal	Pin
20 SB_RX0P	AA8
20 SB_RX0N	Y8
20 SB_RX1P	AA7
20 SB_RX1N	Y7
20 SB_RX2P	AA5
20 SB_RX2N	AA6
20 SB_RX3P	W5
20 SB_RX3N	Y5

SB_RX0P, SB_RX0N, SB_RX1P, SB_RX1N, SB_RX2P, SB_RX2N, SB_RX3P, SB_RX3N

SB_TX0P, SB_TX0N, SB_TX1P, SB_TX1N, SB_TX2P, SB_TX2N, SB_TX3P, SB_TX3N

Signal	Pin	Capacitor	Value
SB_TX0P_C	AD7	C162	0.1U 0402 16V7K
SB_TX0N_C	AE7	C163	0.1U 0402 16V7K
SB_TX1P_C	AE6	C164	0.1U 0402 16V7K
SB_TX1N_C	AD6	C165	0.1U 0402 16V7K
SB_TX2P_C	AB6	C166	0.1U 0402 16V7K
SB_TX2N_C	AC6	C168	0.1U 0402 16V7K
SB_TX3P_C	AD5	C169	0.1U 0402 16V7K
SB_TX3N_C	AE5	C167	0.1U 0402 16V7K

< To SB700 : x4 PCEI A-link>

Signal	Pin	Resistor	Value
PCE_CALRP(PCE_BCALRP)	AC8	R55	1.27K 0402 1%
PCE_CALRN(PCE_BCALRN)	AB8	R56	2K 0402 1%

+1.1VS

< TX Impedance Calibration. Connect to GND >
< RX Impedance Calibration. Connect to VDDPCIE >

RS780MCR3@ RS780M_FCBGA528

U3A

HYPER TRANSPORT CPU I/F (PART 1 OF 6)

< From S1G2 CPU : x16 HT>

Signal	Pin
H_CADOP[0..15] / H_CADON[0..15]	H_CADOP[0..15] 4 / H_CADON[0..15] 4
H_CADOP0	Y25
H_CADON0	Y24
H_CADOP1	V22
H_CADON1	V23
H_CADOP2	V25
H_CADON2	V24
H_CADOP3	U24
H_CADON3	U25
H_CADOP4	T25
H_CADON4	T24
H_CADOP5	P22
H_CADON5	P23
H_CADOP6	P25
H_CADON6	P24
H_CADOP7	N24
H_CADON7	N25
H_CADOP8	AC24
H_CADON8	AC25
H_CADOP9	AB25
H_CADON9	AB24
H_CADOP10	AA24
H_CADON10	AA25
H_CADOP11	Y22
H_CADON11	Y23
H_CADOP12	W21
H_CADON12	W20
H_CADOP13	V21
H_CADON13	V20
H_CADOP14	U20
H_CADON14	U21
H_CADOP15	U19
H_CADON15	U18

HT_RXCAD0P, HT_RXCAD0N, HT_RXCAD1P, HT_RXCAD1N, HT_RXCAD2P, HT_RXCAD2N, HT_RXCAD3P, HT_RXCAD3N, HT_RXCAD4P, HT_RXCAD4N, HT_RXCAD5P, HT_RXCAD5N, HT_RXCAD6P, HT_RXCAD6N, HT_RXCAD7P, HT_RXCAD7N, HT_RXCAD8P, HT_RXCAD8N, HT_RXCAD9P, HT_RXCAD9N, HT_RXCAD10P, HT_RXCAD10N, HT_RXCAD11P, HT_RXCAD11N, HT_RXCAD12P, HT_RXCAD12N, HT_RXCAD13P, HT_RXCAD13N, HT_RXCAD14P, HT_RXCAD14N, HT_RXCAD15P, HT_RXCAD15N

HT_TXCAD0P, HT_TXCAD0N, HT_TXCAD1P, HT_TXCAD1N, HT_TXCAD2P, HT_TXCAD2N, HT_TXCAD3P, HT_TXCAD3N, HT_TXCAD4P, HT_TXCAD4N, HT_TXCAD5P, HT_TXCAD5N, HT_TXCAD6P, HT_TXCAD6N, HT_TXCAD7P, HT_TXCAD7N, HT_TXCAD8P, HT_TXCAD8N, HT_TXCAD9P, HT_TXCAD9N, HT_TXCAD10P, HT_TXCAD10N, HT_TXCAD11P, HT_TXCAD11N, HT_TXCAD12P, HT_TXCAD12N, HT_TXCAD13P, HT_TXCAD13N, HT_TXCAD14P, HT_TXCAD14N, HT_TXCAD15P, HT_TXCAD15N

Signal	Pin
H_CADIP[0..15] / H_CADIN[0..15]	H_CADIP[0..15] 4 / H_CADIN[0..15] 4
H_CADIP0	D24
H_CADIN0	D25
H_CADIP1	E24
H_CADIN1	E25
H_CADIP2	F24
H_CADIN2	F25
H_CADIP3	F23
H_CADIN3	F22
H_CADIP4	H23
H_CADIN4	H22
H_CADIP5	J25
H_CADIN5	J24
H_CADIP6	K24
H_CADIN6	K25
H_CADIP7	K23
H_CADIN7	K22
H_CADIP8	F21
H_CADIN8	G21
H_CADIP9	G20
H_CADIN9	H21
H_CADIP10	J20
H_CADIN10	J21
H_CADIP11	J18
H_CADIN11	K17
H_CADIP12	L19
H_CADIN12	J19
H_CADIP13	M19
H_CADIN13	L18
H_CADIP14	M21
H_CADIN14	P21
H_CADIP15	P18
H_CADIN15	M18

< To S1G2 CPU : x16 HT>

Signal	Pin
4 H_CLKOP0	T22
4 H_CLKON0	T23
4 H_CLKOP1	AB23
4 H_CLKON1	AA22
HT_RXCLK0P	H_CLKIP0 4
HT_RXCLK0N	H_CLKIN0 4
HT_RXCLK1P	H_CLKIP1 4
HT_RXCLK1N	H_CLKIN1 4
HT_TXCLK0P	H24
HT_TXCLK0N	H25
HT_TXCLK1P	L21
HT_TXCLK1N	L20
4 H_CTLOP0	M22
4 H_CTLON0	M23
4 H_CTLOP1	R21
4 H_CTLON1	R20
HT_RXCTL0P	H_CTLIP0 4
HT_RXCTL0N	H_CTLIN0 4
HT_RXCTL1P	H_CTLIP1 4
HT_RXCTL1N	H_CTLIN1 4
HT_TXCTL0P	M24
HT_TXCTL0N	M25
HT_TXCTL1P	P19
HT_TXCTL1N	R18

Signal	Pin
HT_RXCALP	C23
HT_RXCALN	A24
HT_TXCALP	B24
HT_TXCALN	B25

301 0402 1% R57 1 — 2 HT_RXCALP / HT_RXCALN

0718 Place within 1" layout 1:2

RS780MCR3@ RS780M_FCBGA528

NEED CHECK R57 & R58 WITH AMD

HT_TXCALP R58 1 — 2 301 0402 1% HT_TXCALN

< Transmitter Calibration Resistor to HT_TXCALN >

0718 Place within 1" layout 1:2

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3	AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7	AUX1 and HPD1

< If integrated GFX is used, some PCIE pairs are used as HDMI signal pairs >

Signal	Resistor	Value	Signal	Pin
PCIE_MTX_GRX_P0 IHDMI@	R74	0 0402 5%	HDMI_TXD2+	18,19
PCIE_MTX_GRX_N0 IHDMI@	R75	0 0402 5%	HDMI_TXD2-	18,19
PCIE_MTX_GRX_P1 IHDMI@	R76	0 0402 5%	HDMI_TXD1+	18,19
PCIE_MTX_GRX_N1 IHDMI@	R81	0 0402 5%	HDMI_TXD1-	18,19
PCIE_MTX_GRX_P2 IHDMI@	R82	0 0402 5%	HDMI_TXD0+	18,19
PCIE_MTX_GRX_N2 IHDMI@	R83	0 0402 5%	HDMI_TXD0-	18,19
PCIE_MTX_GRX_P3 IHDMI@	R84	0 0402 5%	HDMI_CLK0+	18,19
PCIE_MTX_GRX_N3 IHDMI@	R85	0 0402 5%	HDMI_CLK0-	18,19

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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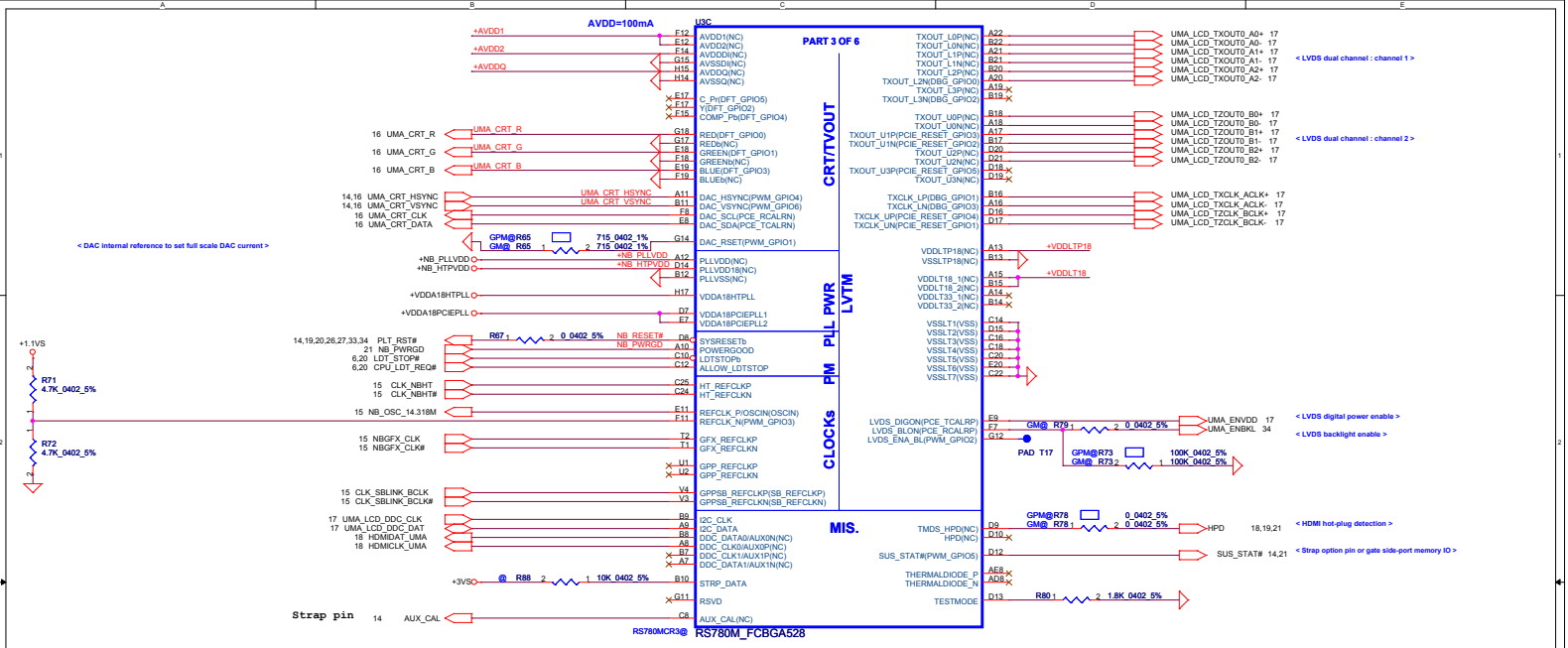
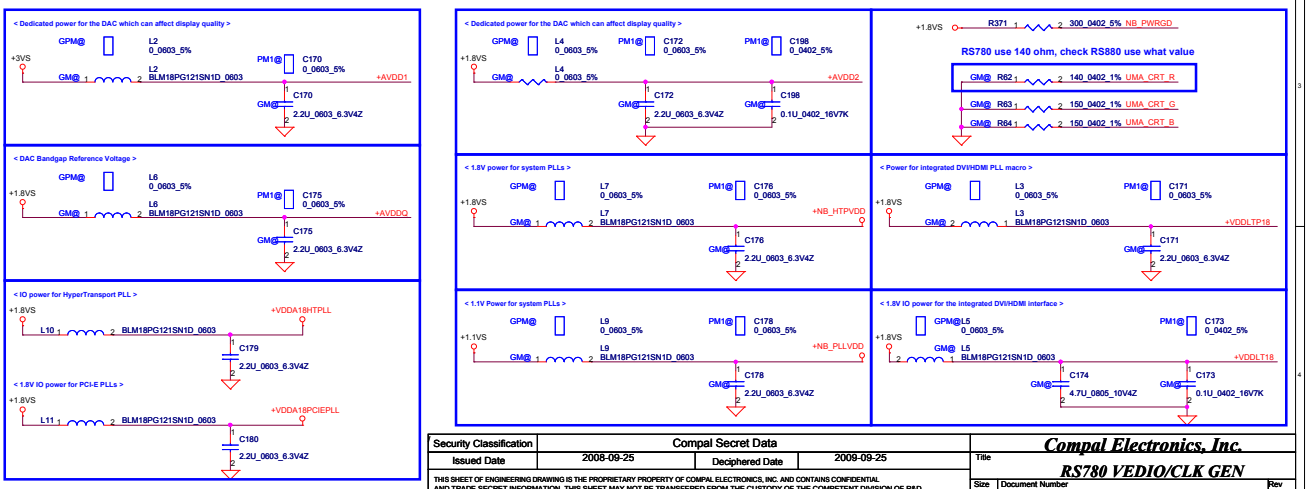
Compal Electronics, Inc.

Title: RS780M&RX781-HT/PCIE

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 10 of 45





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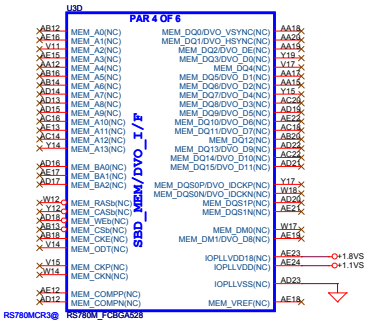
Title: RS780 VEDIO/CLK GEN

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 11 of 45



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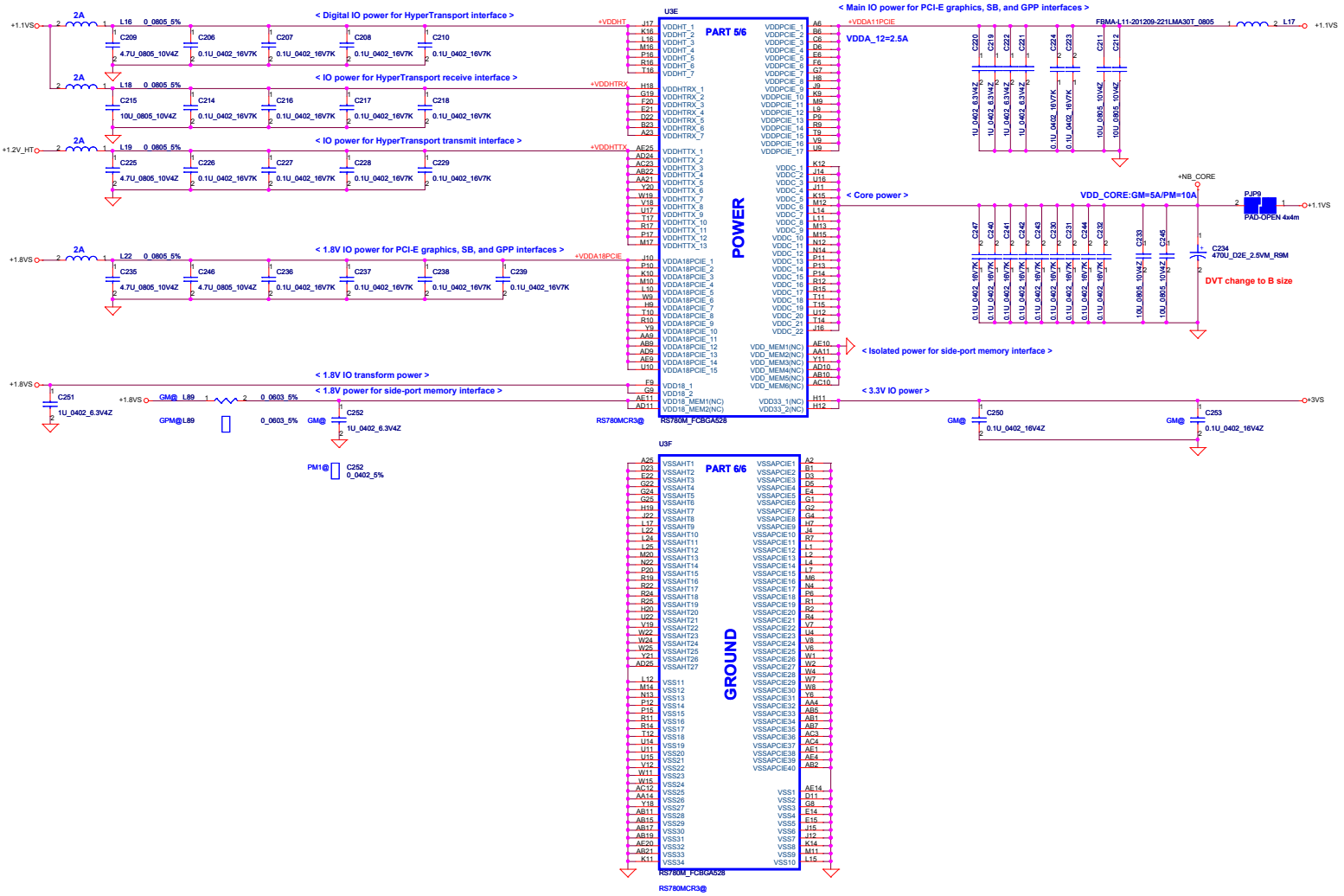
Compal Electronics, Inc.

Title: **RS780M&RX781 SIDE PORT**

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 12 of 45



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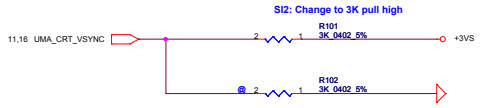
Compal Electronics, Inc.

Title: RS780M&RX781 PWR/GND

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 13 of 45

< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K >



< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)

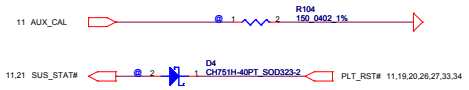
PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

< RS780 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS780 DFT_GPIO1 >



< DFT_GPIO1 : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

< RS780 use HSYNC to enable SIDE PORT (internal pull high) >

< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb >

RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)
0 : Enable (RS780)

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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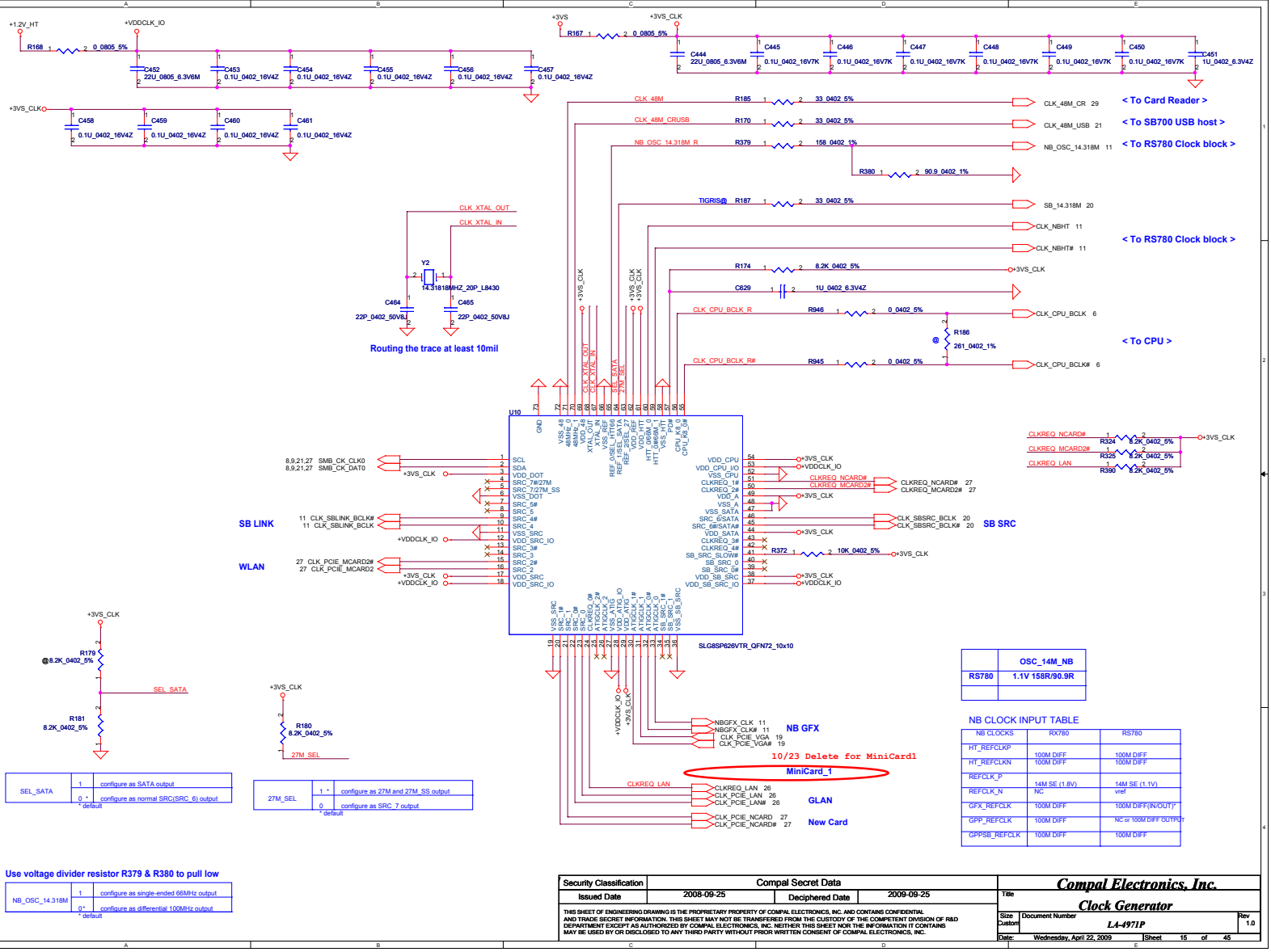
Title: RS780M&RX781 STRAPS

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 14 of 45



	OSC_14M_NB
RS780	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

SEL_SATA		
	1	configure as SATA output
	0 *	configure as normal SRC(SRC_6) output

* default

27M_SEL		
	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

* default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M		
	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output

* default

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

Title: **Clock Generator**

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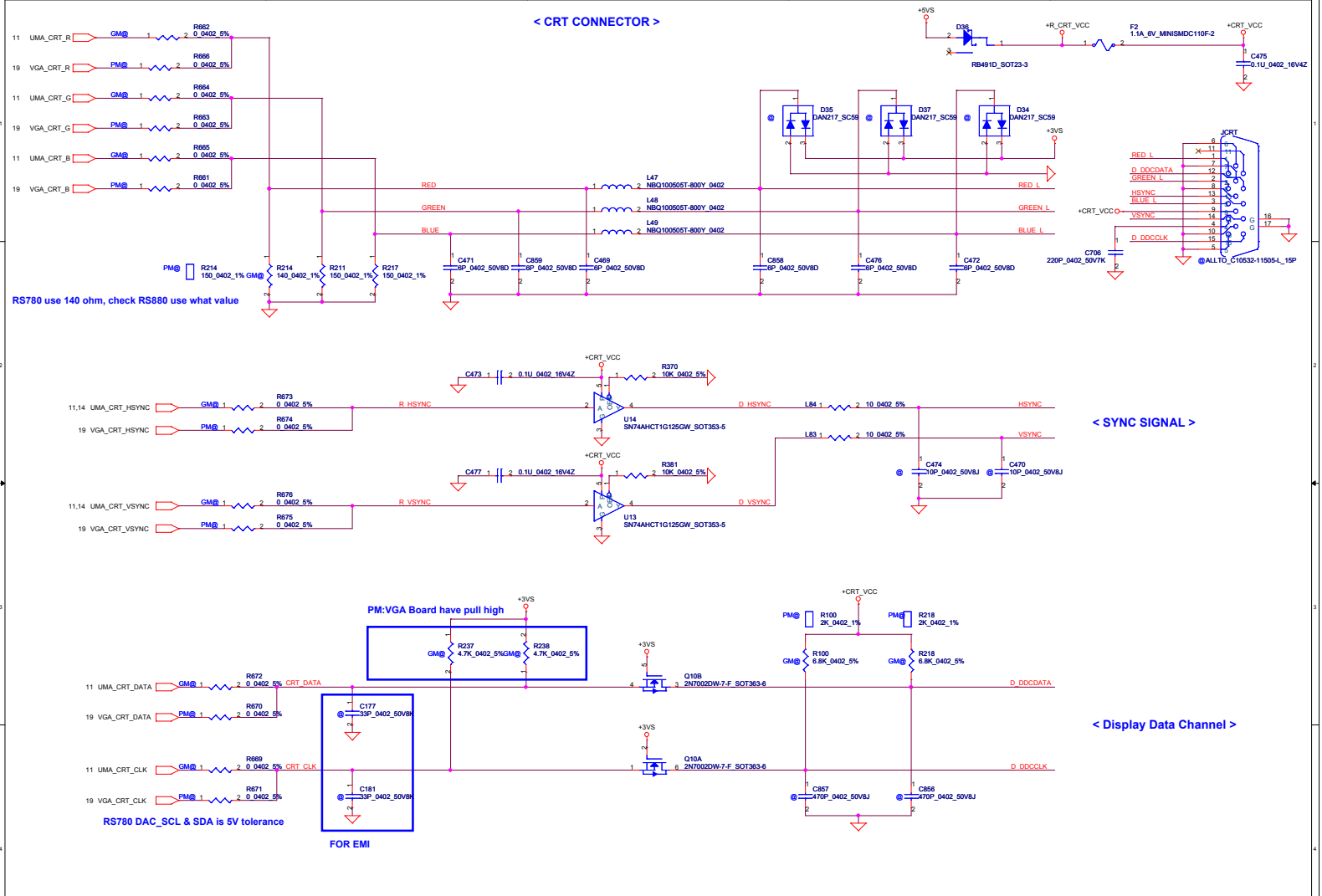
Date: Wednesday, April 22, 2009 | Sheet 15 of 45

< CRT CONNECTOR >



RS780 use 140 ohm, check RS880 use what value

< SYNC SIGNAL >

< Display Data Channel >

RS780 DAC_SCL & SDA is 5V tolerance

FOR EMI

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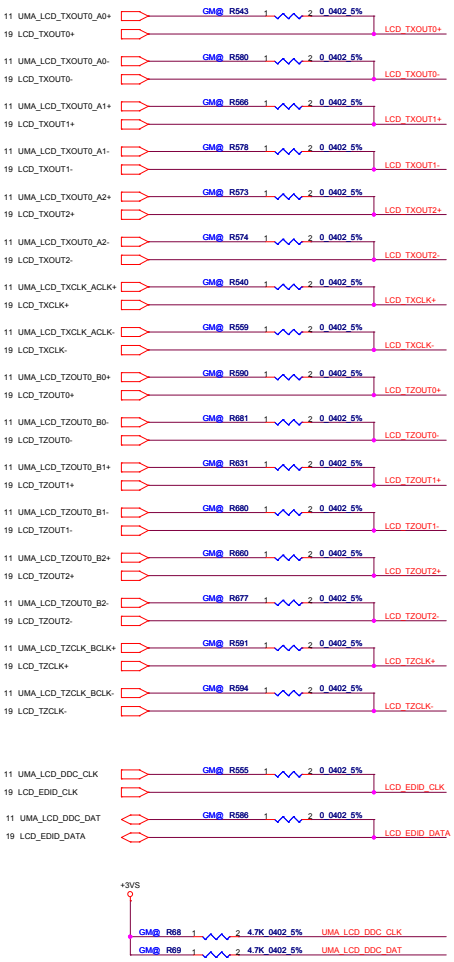
Compal Electronics, Inc.

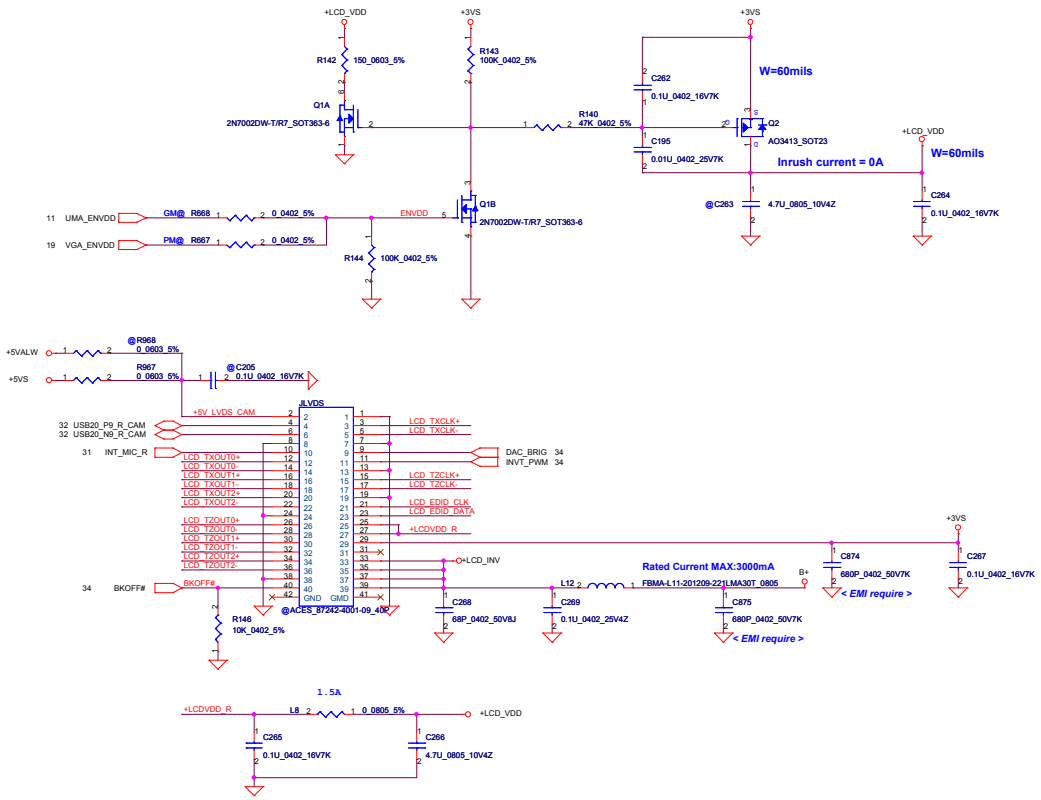
Title: **CRT/TV-OUT Connector**

Size	Document Number	Rev
Custom	LA-4971P	1.0

Date: Wednesday, April 22, 2009 | Sheet 16 of 45

LCD/PANEL BD. Conn.





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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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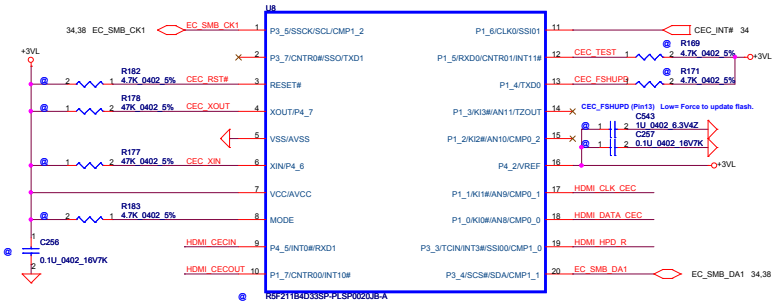
Compal Electronics, Inc.

Title: LCD CONN.

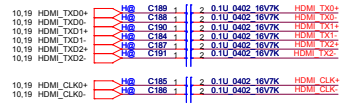
Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 17 of 45

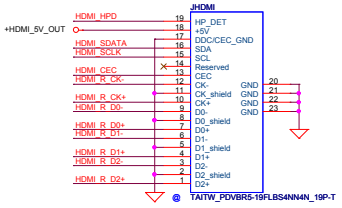
< HDMI CEC Controller >



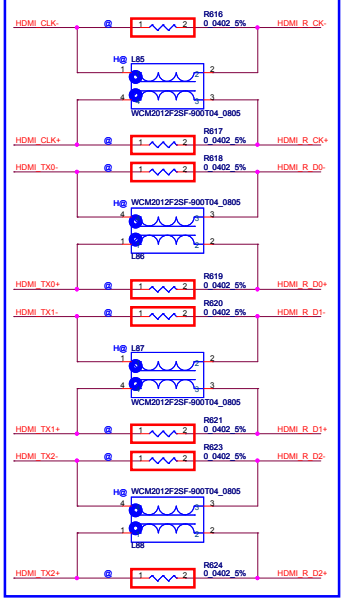
SI:Add R616~R624 for EMI requset



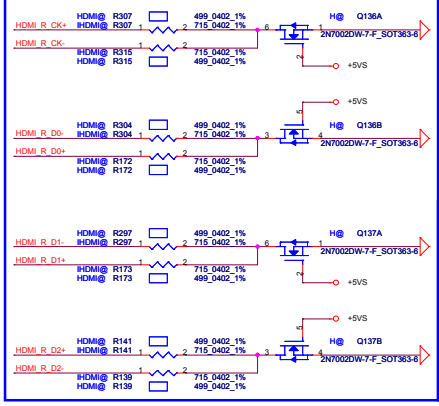
< HDMI Connector >



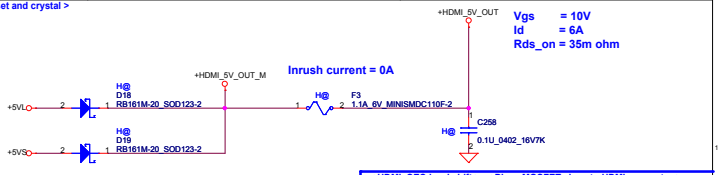
< EMI solution >



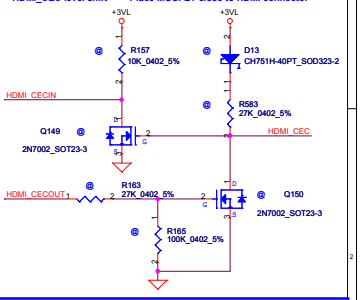
< Termination resistor >



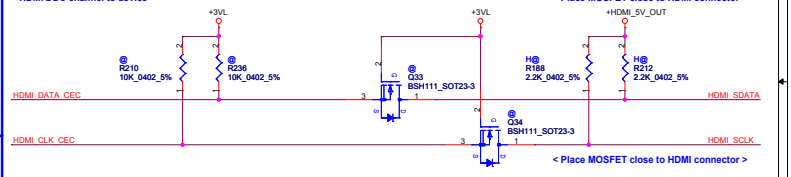
< Power, reset and crystal >



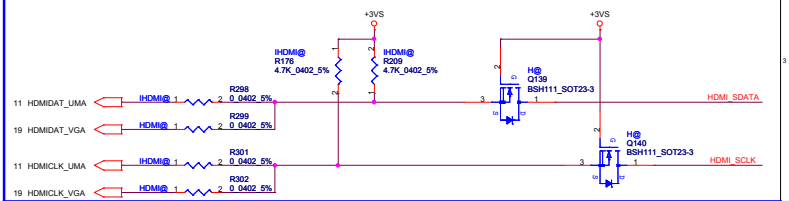
< HDMI_CEC level shift > < Place MOSFET close to HDMI connector >



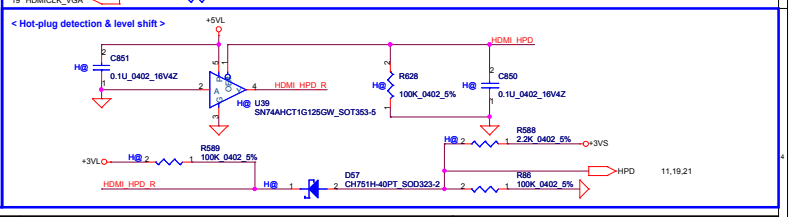
< HDMI DDC channel to device > < Place MOSFET close to HDMI connector >



< Place MOSFET close to HDMI connector >



< Hot-plug detection & level shift >



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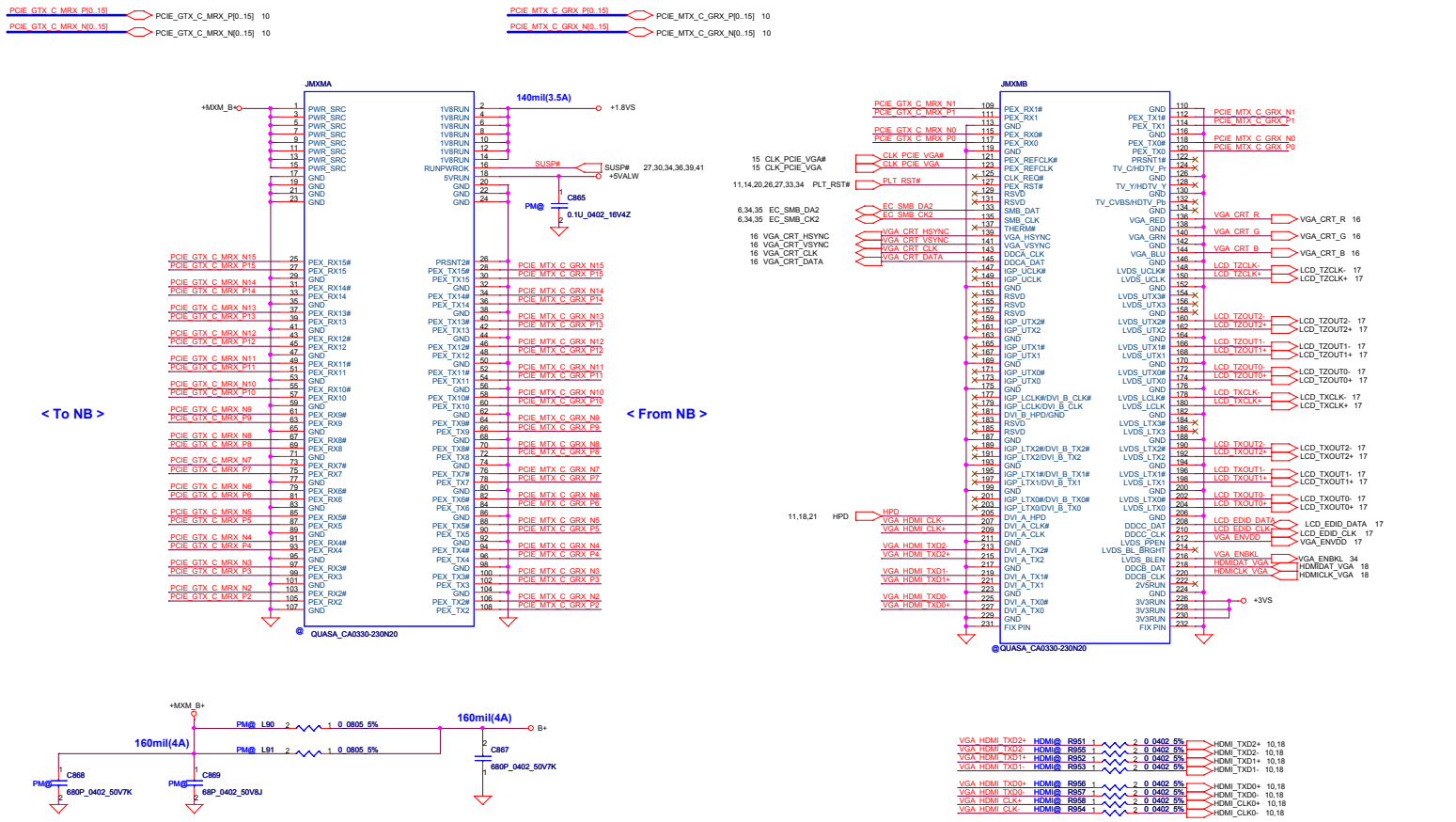
Compal Electronics, Inc.

Title	HDMI/CEC	
Size: Custom	Document Number: LA-4971P	Rev: 1.0
Date: Wednesday, April 22, 2009	Sheet 18 of 45	



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title: MXM Connector
				Size: Custom; Document Number: LA-4971P; Rev: 1.0
				Date: Wednesday, April 22, 2009; Sheet 19 of 45

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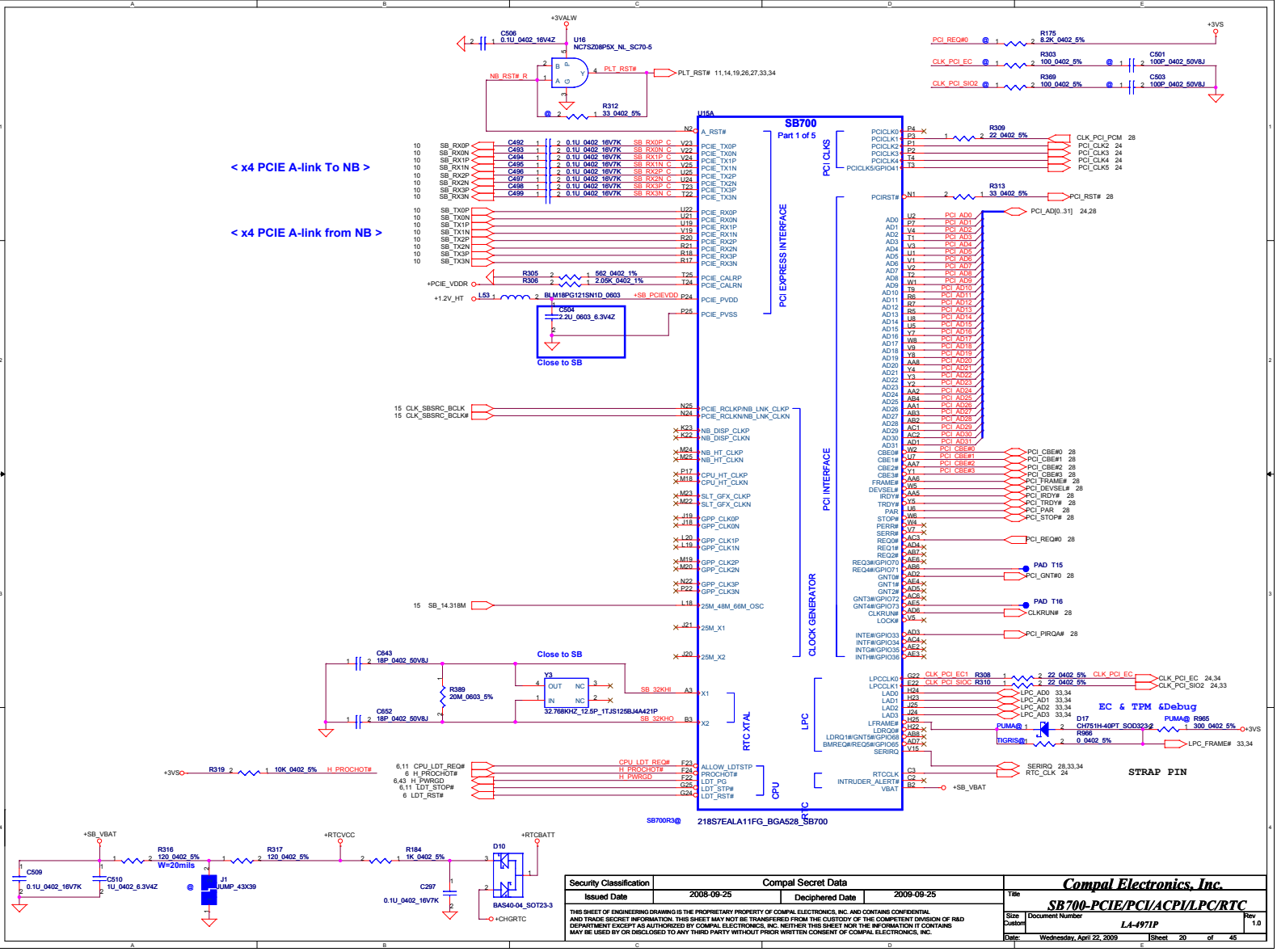

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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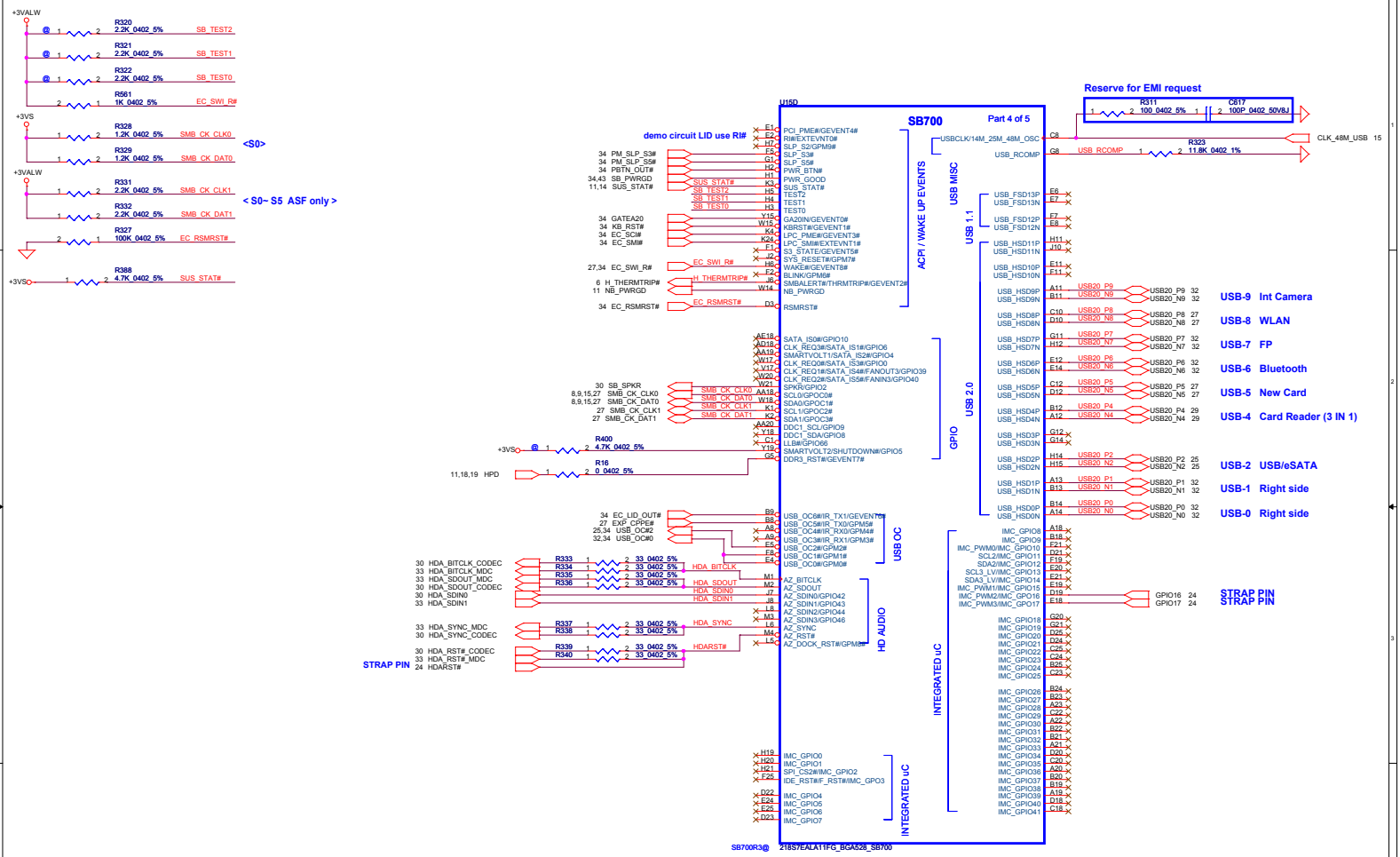
Title	Compal Electronics, Inc.
	SB700-PCIE/PCI/ACPI/LPC/RTC
Size: Custom	Document Number: LA-4971P
	Rev: 1.0
Date: Wednesday, April 22, 2009	Sheet 20 of 45



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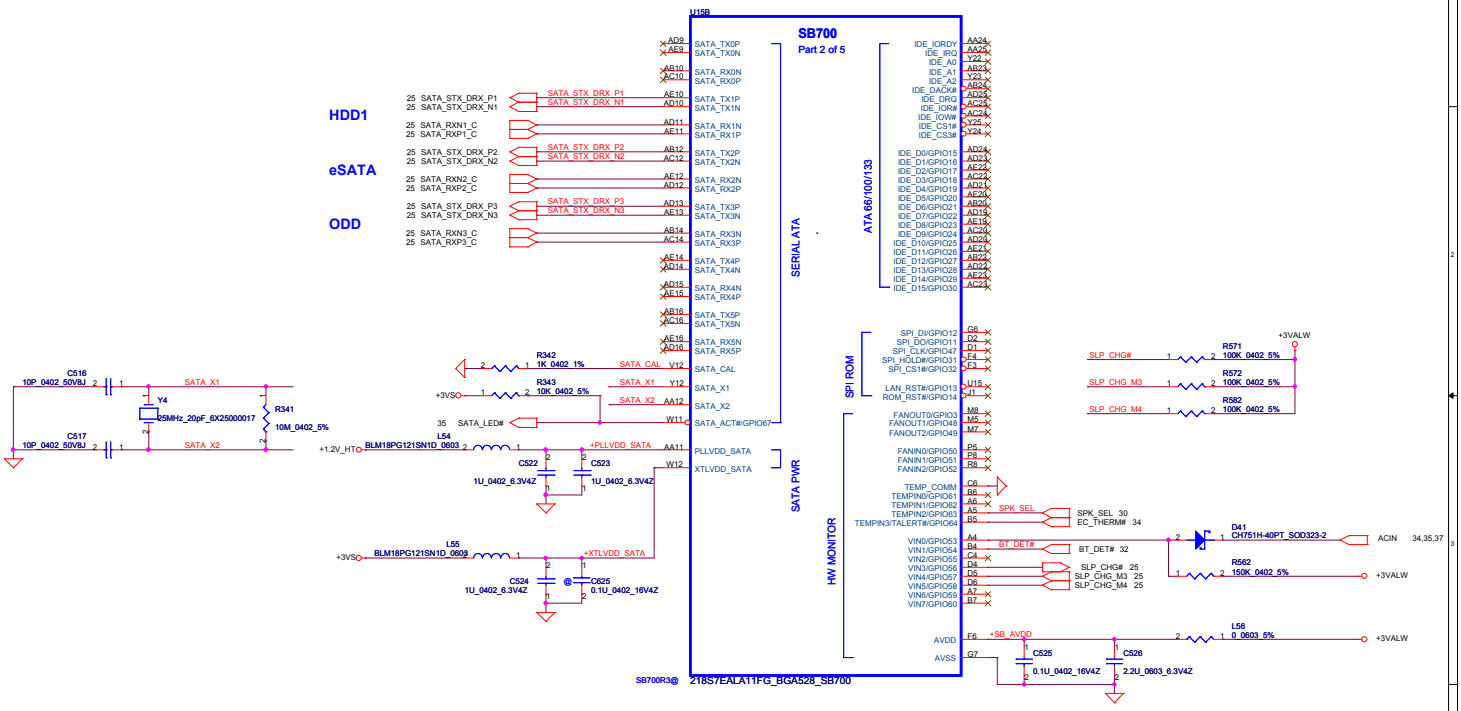
Compal Electronics, Inc.

Title: **SB700 USB/AC97**

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 21 of 45



Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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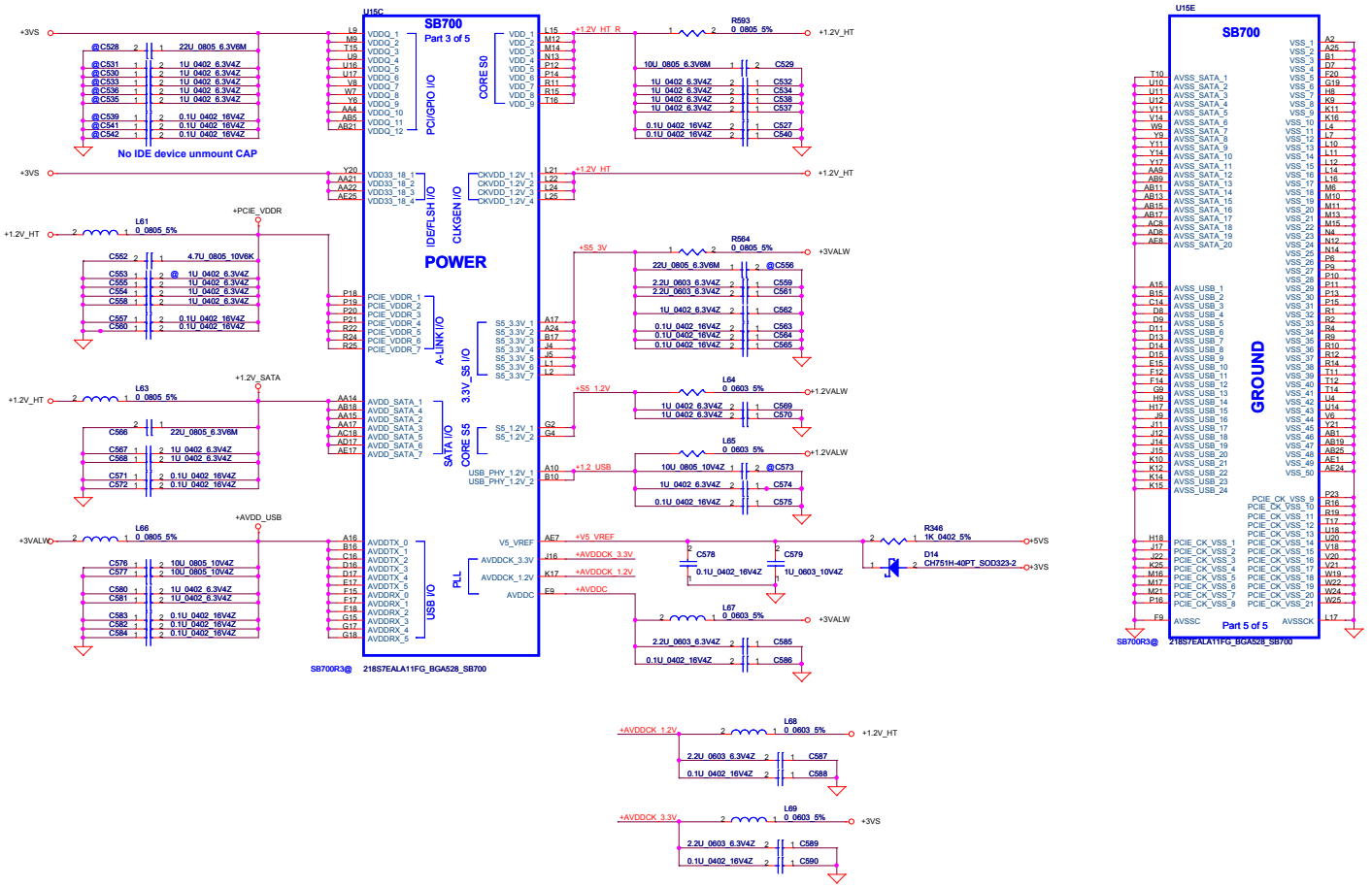
Compal Electronics, Inc.

Title: **SB700 SATA/IDE/SPI**

Size	Document Number	Rev
Custom	LA-4971P	1.0

Date: Wednesday, April 22, 2009 | Sheet 22 of 45



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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

Title: **SB700 Power/GND**

Size	Document Number	Rev
Custom	LA-4971P	1.0

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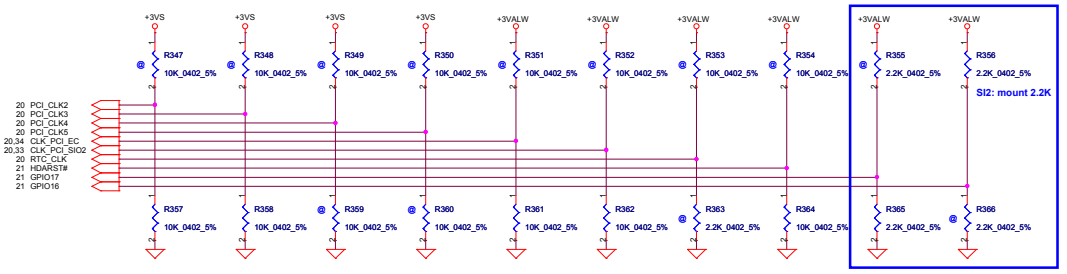
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

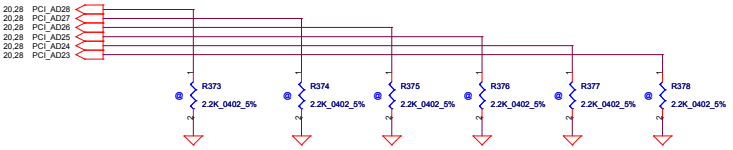


Need to confirm if SB SPI ROM will mount

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



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Compal Electronics, Inc.

Title: SB700 STRAPS

Size: Custom | Document Number: LA-4971P | Rev: 1.0

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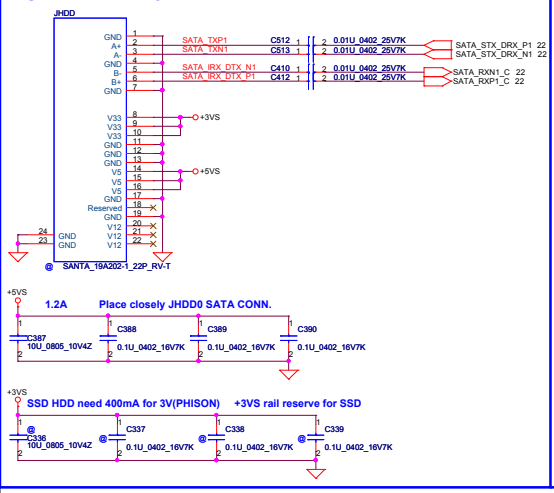
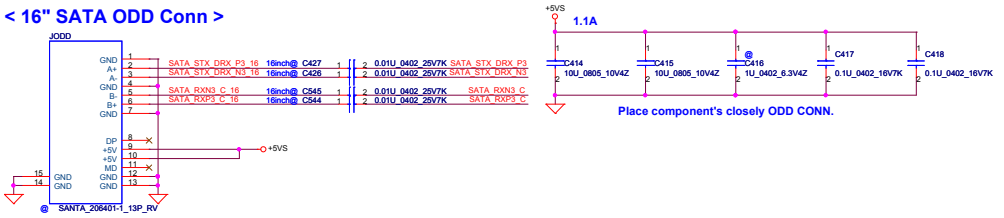
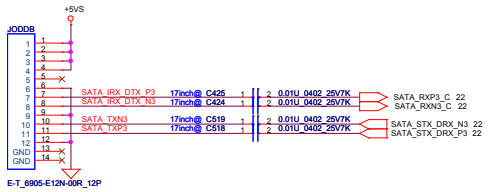
< SATA HDD1 Conn >



< 16" SATA ODD Conn >

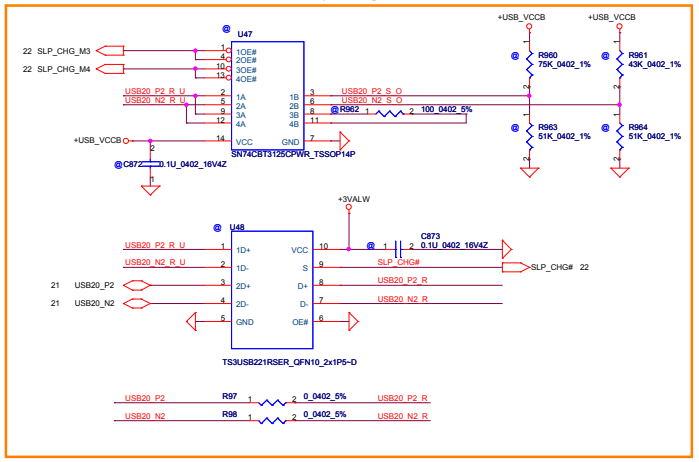


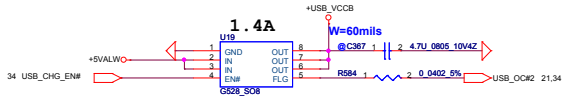
< 17" SATA ODD Conn >

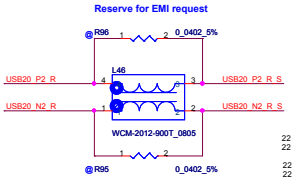


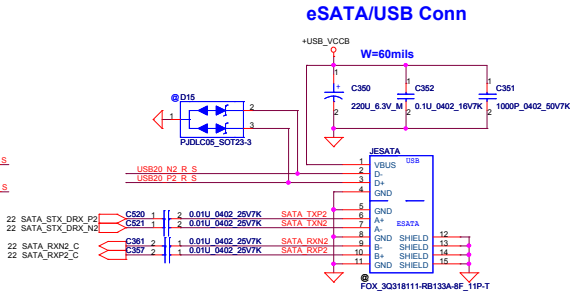
< eSATA/USB >

10/22 Add for USB Sleep & Charge M3/M4









	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG#	FUNCTION
LOW	D=1D
HIGH	D=2D

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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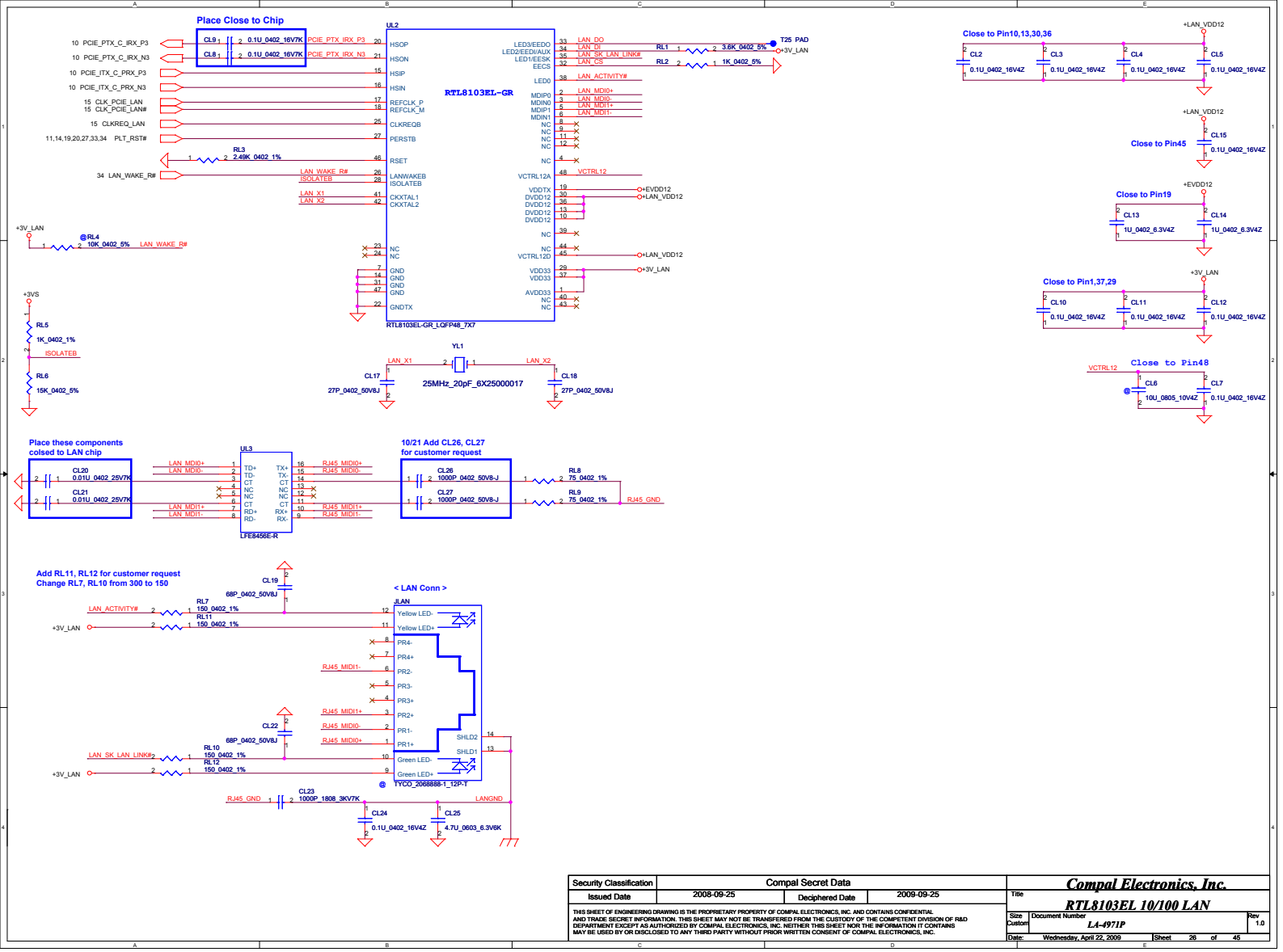
Compal Electronics, Inc.

Title: SATA HDD/ODD/ESATA_USB

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 25 of 45



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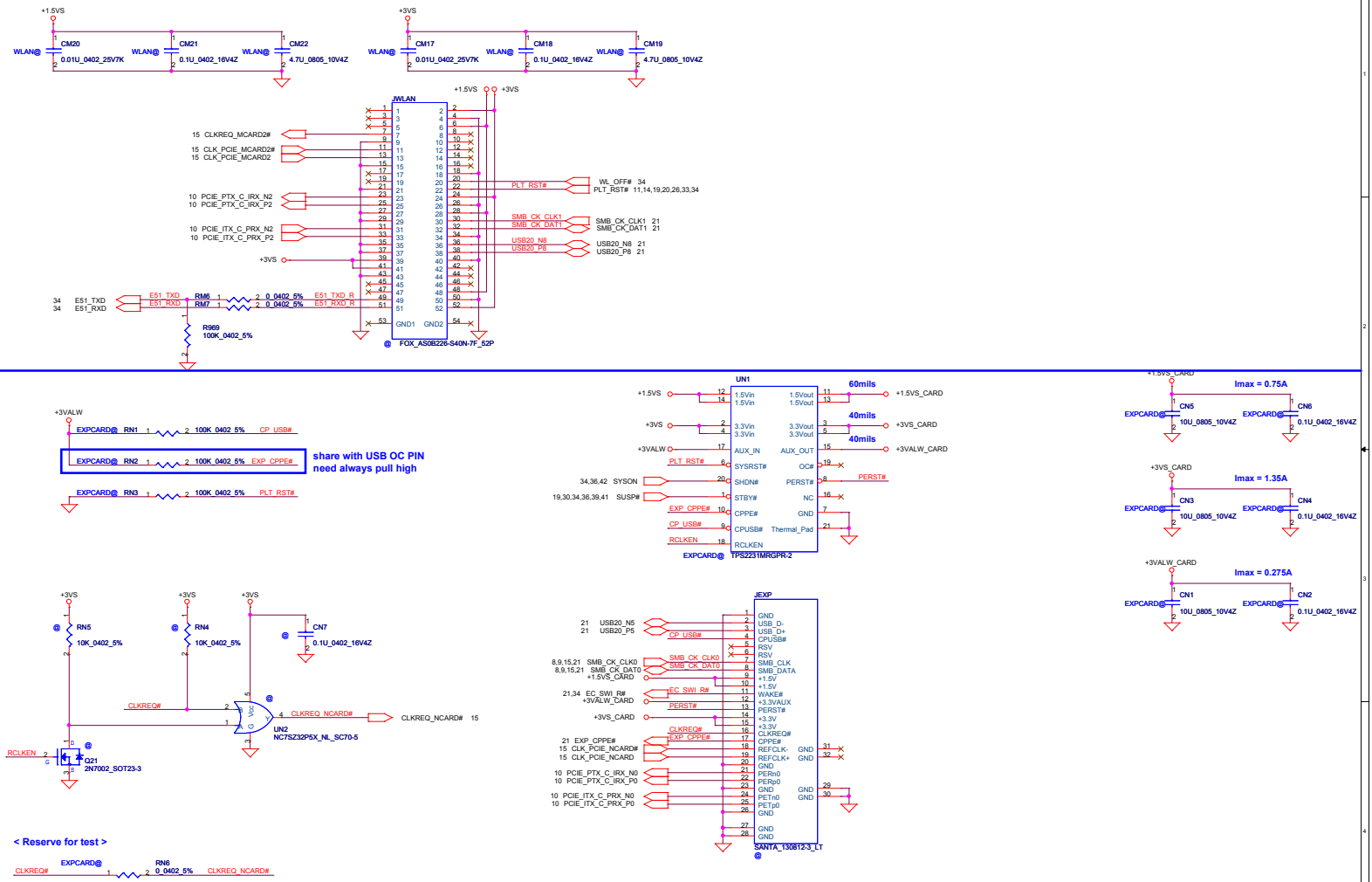
Compal Electronics, Inc.

Title: **RTL8103EL 10/100 LAN**

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 26 of 45

< PCIe Mini Card for WLAN >



Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

Title: **NEW CARD/WLAN/KS**

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 27 of 45

22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

+3VS
RB22 33K_0402_5% CLKRUN#
RB23 33K_0402_5% SERIRQ
RB24 33K_0402_5% PCI_PIRQA#

For EMI

CLK_PCI_PCM
@ RB21 10_0402_5%
@ CB14 10P_0402_50V8J

20,24 PCI_AD[0..31] — PCI_AD[0..31]
20 PCI_CBE#[0..3] — PCI_CBE#[0..3]

+S1_VCC
CB11 0.1U_0402_16V4Z PCMCIA@
CB12 4.7U_0805_10V4Z PCMCIA@
CB1 0.1U_0402_16V4Z PCMCIA@
CB2 4.7U_0805_10V4Z PCMCIA@
+3VS +5VS
CB3 4.7U_0805_10V4Z PCMCIA@
CB4 0.1U_0402_16V4Z PCMCIA@

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

+S1_VCC
UB2 OZ2210GN-B1_SO8 PCMCIA@
VCC/VPP +3.3V
VCC/VPP +3.3V
VCC5# +5V
VCC3# GND

+3VS
CB5 10U_0805_10V4Z PCMCIA@
CB6 0.1U_0402_16V4Z PCMCIA@
CB7 0.1U_0402_16V4Z PCMCIA@
CB8 0.1U_0402_16V4Z PCMCIA@
PCMCIA@ RB16 33K_0402_5%
PCMCIA@ RB17 33K_0402_5%

+3VS
CB9 10U_0805_10V4Z PCMCIA@
CB10 0.1U_0402_16V4Z PCMCIA@
CB13 0.1U_0402_16V4Z PCMCIA@

UB1 PCMCIA@ OZ601TN_TQFP128-D

Pin	Signal
64, 77, 97, 115	CORE_VCC, CORE_VCC, CORE_VCC, CORE_VCC
1, 20, 33	PCI_VCC, PCI_VCC, PCI_VCC
124, 125, 123	VCC5#/VCCD0#/SDATA, VCC3#/VCCD1#/SCLK, VPP_PGM/VPPD0/SLATCH
4, 5, 6, 7, 8, 9, 10, 13, 14, 15, 16, 17, 18, 19, 21, 22, 28, 29, 30, 31, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 46	PCI_AD31, PCI_AD30, PCI_AD29, PCI_AD28, PCI_AD27, PCI_AD26, PCI_AD25, PCI_AD24, PCI_AD23, PCI_AD22, PCI_AD21, PCI_AD20, PCI_AD19, PCI_AD18, PCI_AD17, PCI_AD16, PCI_AD15, PCI_AD14, PCI_AD13, PCI_AD12, PCI_AD11, PCI_AD10, PCI_AD9, PCI_AD8, PCI_AD7, PCI_AD6, PCI_AD5, PCI_AD4, PCI_AD3, PCI_AD2, PCI_AD1, PCI_AD0
127	IDSEL
11, 12, 49, 50	PCI_CBE#3, PCI_CBE#2, PCI_CBE#1, PCI_CBE#0
26, 27, 23, 24, 25, 47, 48	PCI_CLK, DEVSEL#, FRAME#, IRDY#, TRDY#, STOP#, PAR
51	PERR#/SPKR_OUT
2, 3	REQ#, GNT#
126, 120	RST#, PME#/RI_OUT#
55, 54, 53, 52	MF6, MF4, MF3, MF0
32, 45, 65, 96, 128	GND
103, 102, 101, 100, 99, 110, 109, 108, 106, 105, 104, 118, 95, 94, 93, 75, 74, 73, 71, 72, 70, 69, 68, 85, 84, 82, 83, 80, 81, 78, 79, 76	S1_D10, S1_D9, S1_D1, S1_D8, S1_D0, S1_A0, S1_A1, S1_A2, S1_A3, S1_A4, S1_A5, S1_A6, S1_A25, S1_A7, S1_A24, S1_A17, S1_IOWR#, S1_A9, S1_IORD#, S1_A11, S1_OE#, S1_CE2#, S1_A10, S1_D15, S1_D7, S1_D13, S1_D6, S1_D12, S1_D5, S1_D11, S1_D4, S1_D3
107, 114, 117, 116, 113, 61, 58, 60, 91, 89, 62, 88, 59, 87, 119, 98, 86, 63, 57, 121, 56, 122, 92, 90	S1_A16, S1_A23, S1_A15, S1_A22, S1_A21, S1_A20, S1_A13, S1_A14, S1_WAIT#, S1_INPACK#, S1_WE#, S1_RDY#, S1_A19, S1_WP, S1_RST, S1_D2, S1_D14, S1_A18, S1_VS1, S1_VS2, S1_CD1#, S1_CD2#, S1_BVD2, S1_BVD1
111, 112, 66, 67	S1_REG#, S1_A12, S1_A8, S1_CE1#

PCI_AD20 PCMCIA@ 1 — 2 RB19 100_0402_5% IDSEL

20 CLK_PCI_PCM
20 PCI_DEVSEL#
20 PCI_FRAME#
20 PCI_IRDY#
20 PCI_TRDY#
20 PCI_STOP#
20 PCI_PAR
30 PCM_SPK# — PCM_SPK#
20 PCI_REQ#0
20 PCI_GNT#0
20 PCI_RST#
20 CLKRUN# — CLKRUN# @ 2 — 1 RB20 0_0402_5%
20,33,34 SERIRQ
20 PCI_PIRQA#

PCMCIA@ 1 — 2 RB18 33_0402_5%

PCMCIA Socket
JPCM @SANTA_130625-3_LT

Pin	Signal
1, 35, 2, 36, 3, 37, 4, 38, 5, 39, 6, 40, 7, 41, 8, 42, 9, 43, 10, 44, 11, 45, 12, 46, 13, 47, 14, 48, 15, 49, 16, 50, 17, 51, 18, 52, 19, 53, 54, 20, 55, 21, 56, 22, 57, 23, 24, 58, 25, 59, 26, 60, 27, 61, 28, 62, 29, 63, 30, 64, 31, 65, 32, 66, 33, 67, 34, 68	GND, GND, DATA3, CD1#, DATA4, DATA11, DATA5, DATA12, DATA6, DATA13, DATA7, DATA14, CE1#, DATA15, ADD10, CE2#, OE#, VS1#, ADD11, IORD#, ADD9, IOWR#, ADD8, ADD17, ADD13, ADD18, ADD14, ADD19, WE#, ADD20, READY, ADD21, VCC, VCC, VPP, VPP, ADD16, ADD22, ADD15, ADD23, ADD12, ADD24, ADD7, ADD25, ADD6, VS2#, ADD5, RESET, ADD4, WAIT#, ADD3, INPACK#, ADD2, REG#, ADD1, BVD2, ADD0, BVD1, DATA0, DATA8, DATA1, DATA9, DATA2, DATA10, WP, CD2#, GND, GND, GND
69, 70, 71, 72	GND, GND, GND, GND
S1_D3, S1_CD1#, S1_D4, S1_D11, S1_D5, S1_D12, S1_D6, S1_D13, S1_D7, S1_D14, S1_CE1#, S1_D15, S1_A10, S1_CE2#, S1_OE#, S1_VS1, S1_A11, S1_IORD#, S1_A9, S1_IOWR#, S1_A8, S1_A17, S1_A13, S1_A18, S1_A14, S1_A19, S1_WE#, S1_A20, S1_RDY#, S1_A21, S1_A16_R, S1_A22, S1_A15, S1_A23, S1_A12, S1_A24, S1_A7, S1_A25, S1_A6, S1_VS2, S1_A5, S1_RST, S1_A4, S1_WAIT#, S1_A3, S1_INPACK#, S1_A2, S1_REG#, S1_A1, S1_BVD2, S1_A0, S1_BVD1, S1_D0, S1_D8, S1_D1, S1_D9, S1_D2, S1_D10, S1_WP, S1_CD2#	
+S1_VCC	17, 51, 18, 52

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

Title: CardBus O2 OZ601

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Date: Wednesday, April 22, 2009 | Sheet 28 of 45

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.

IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

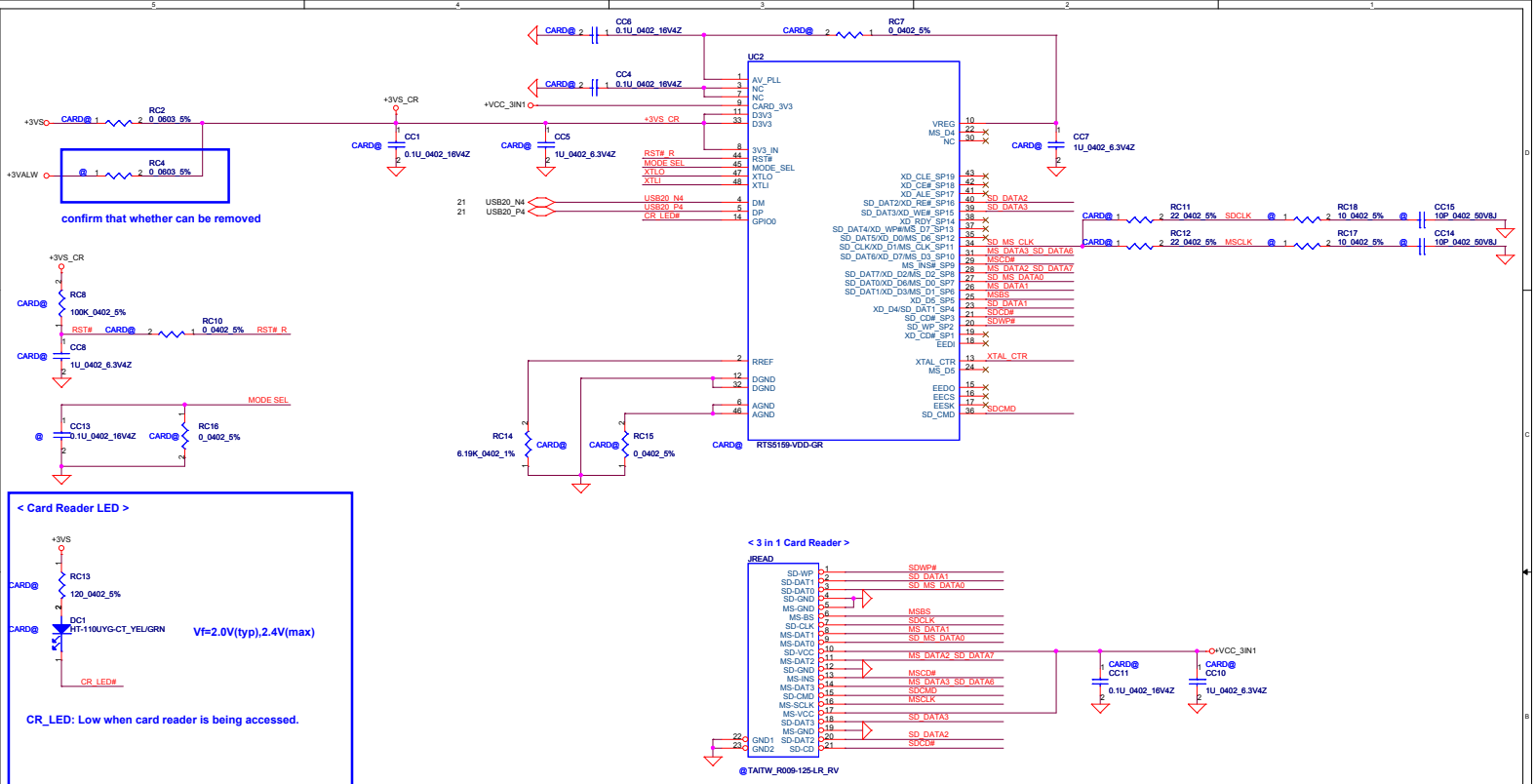
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.

THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127 ball F4

must check IDSEL, PCI_PIRQ#,



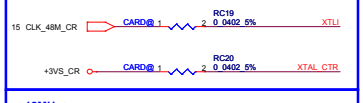
< Card Reader LED >

Vf=2.0V(typ),2.4V(max)

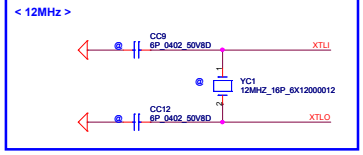
CR_LED: Low when card reader is being accessed.

< 3 in 1 Card Reader >

< 48MHz > Cost-down option



< 12MHz >



R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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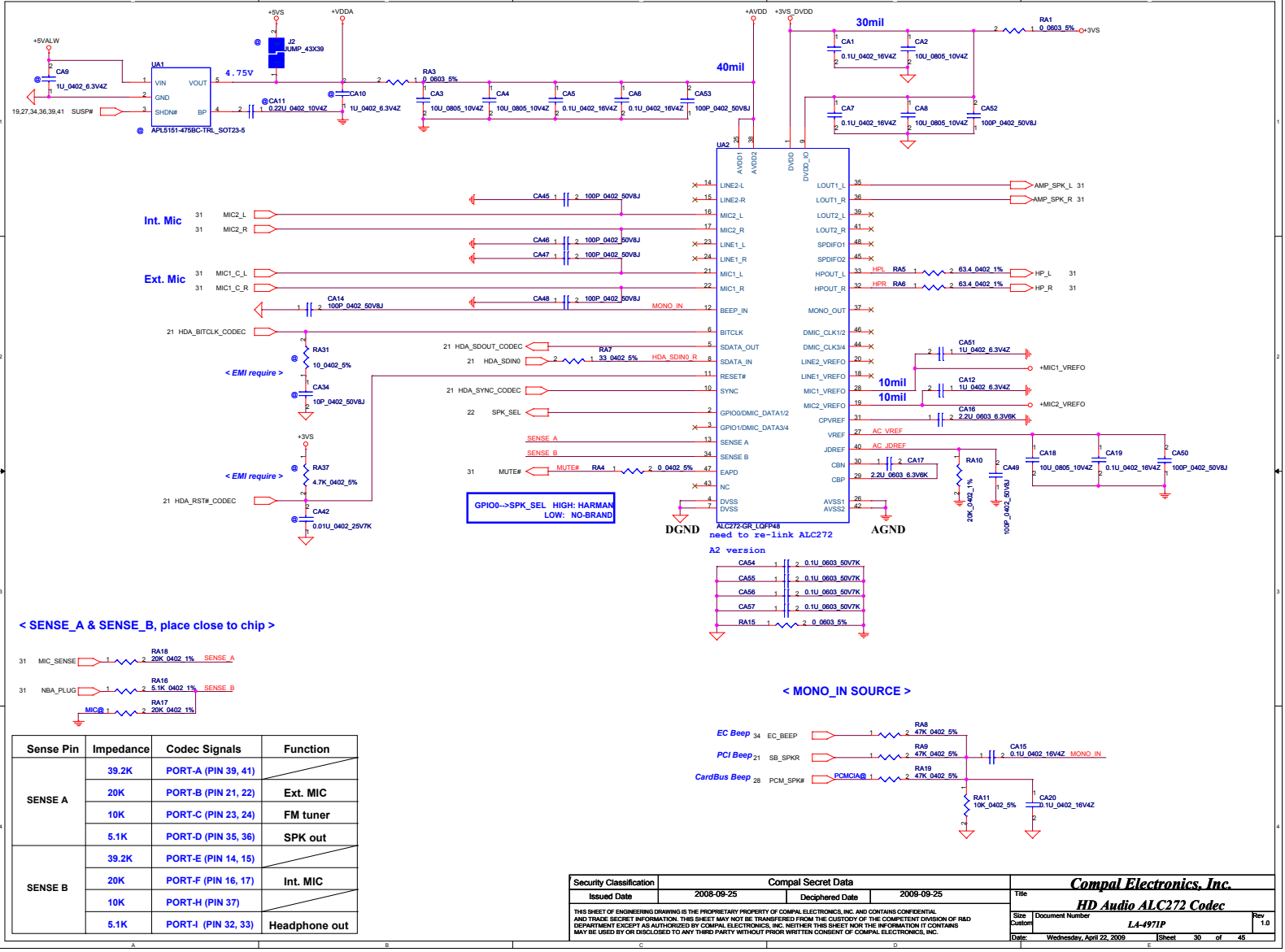
Compal Electronics, Inc.

Title: RTS5159 Card Reader

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 29 of 45



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

Title: HD Audio ALC272 Codec

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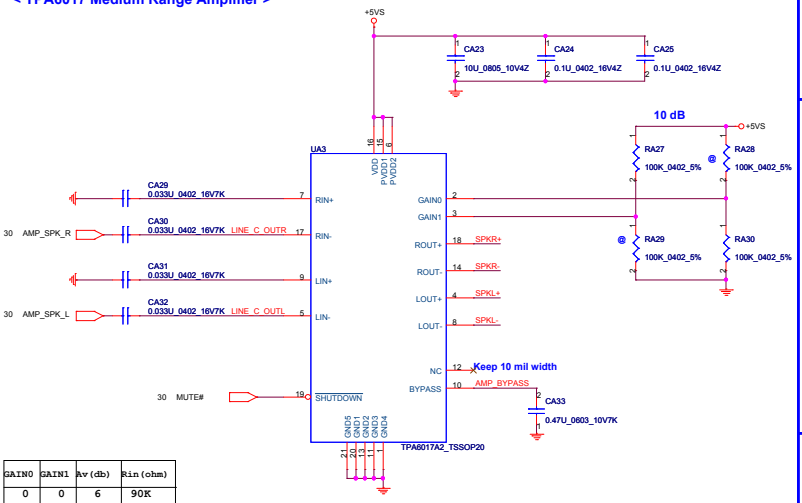
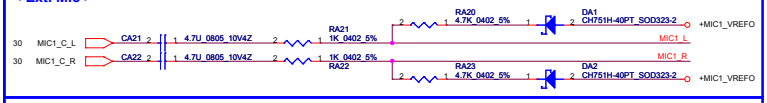
< TPA6017 Medium Range Amplifier >

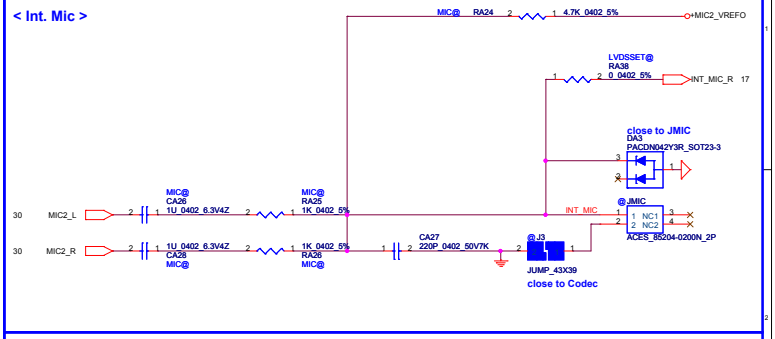


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

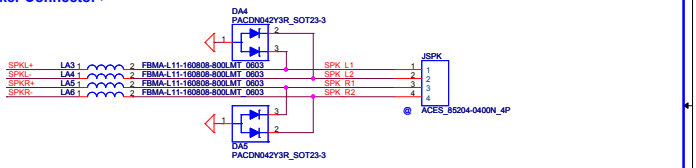
< Ext. Mic >



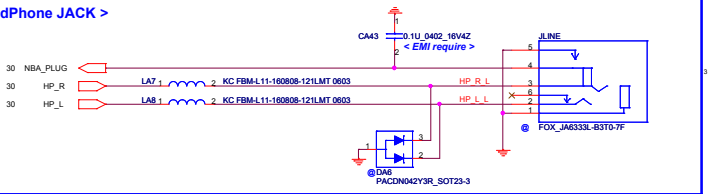
< Int. Mic >



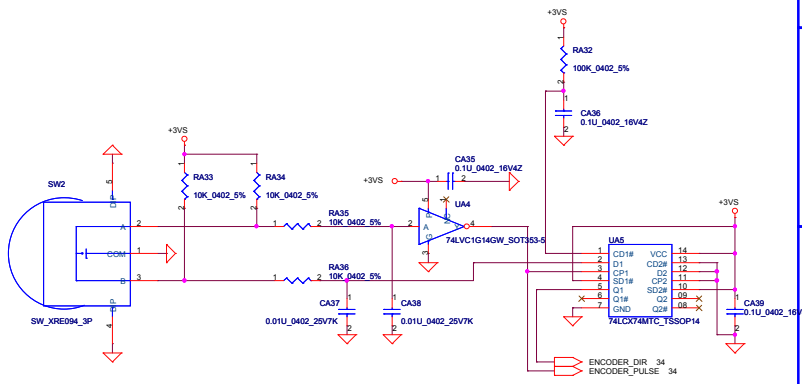
< Speaker Connector >



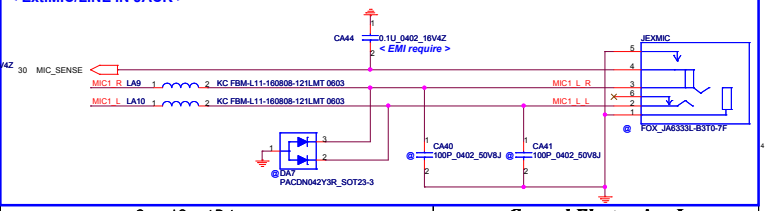
< HeadPhone JACK >



< Volume Control >



< Ext.MIC/LINE IN JACK >



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Compal Electronics, Inc.

Title: AMP/Audio Jack/HP/SPEAKER/VR

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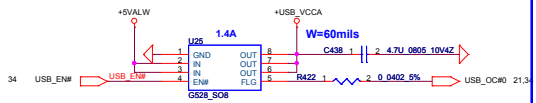
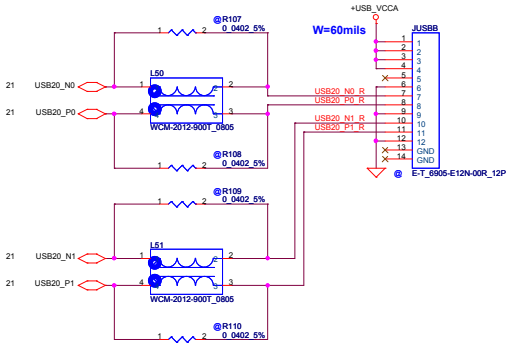
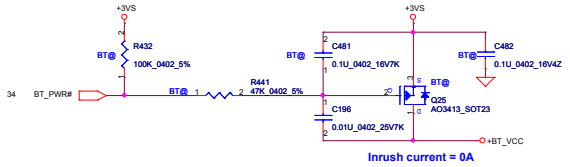
< USB Right-side Board, USB port 0,1 >



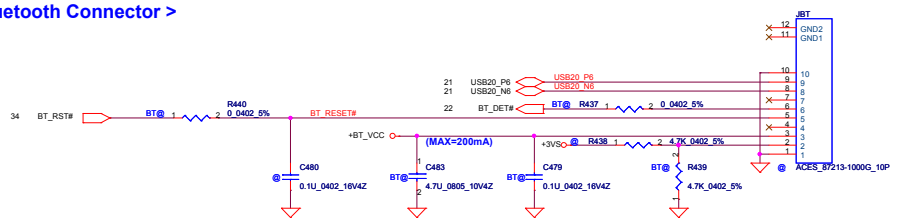
< Reserve for EMI request >



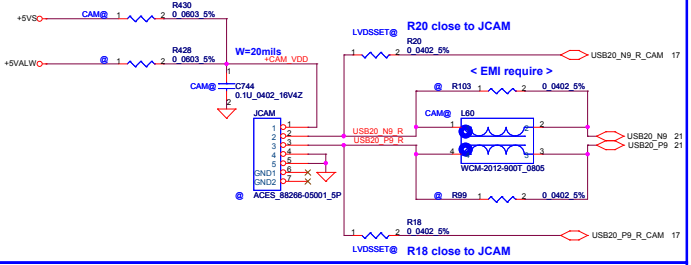
< BlueTooth Interface, USB port6 >



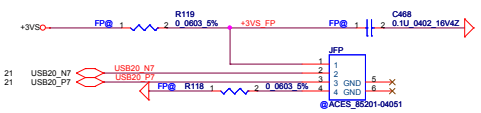
< Bluetooth Connector >



< Int. Camera, USB port 9 >



< Finger Printer, USB port 7 >



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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

Title: USB/BT/FingerPrint

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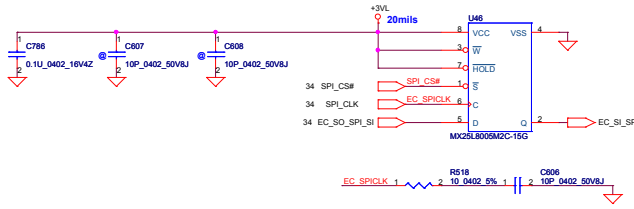
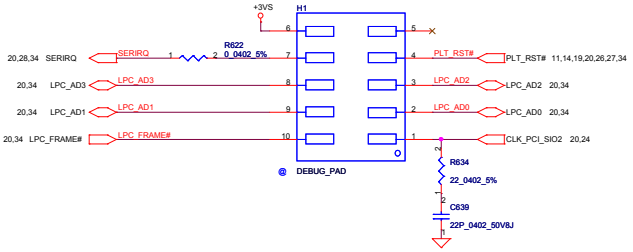
< SPI Flash 8MB*1 >

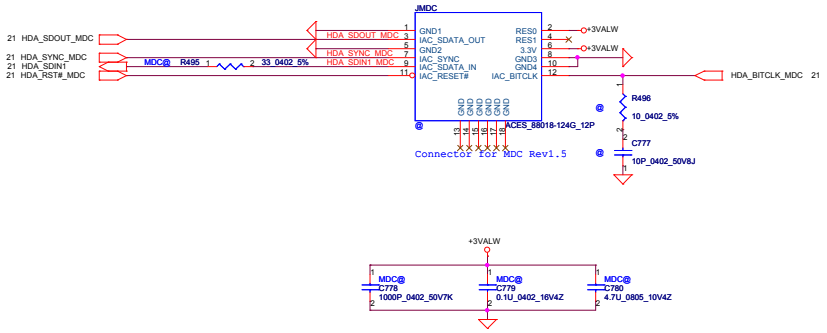


< LPC Debug Port >

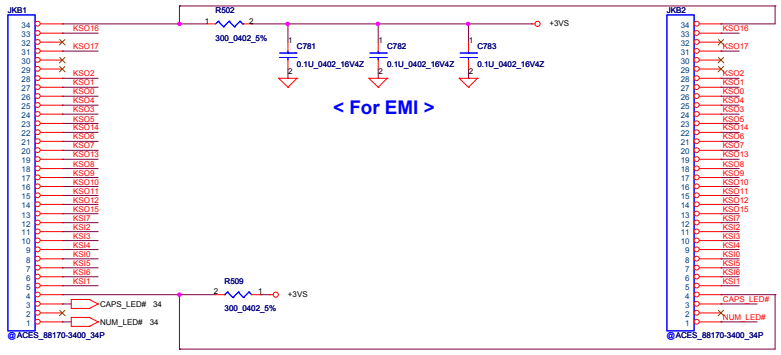
Please place the PAD under DDR DIMM.



< MDC 1.5 Conn >



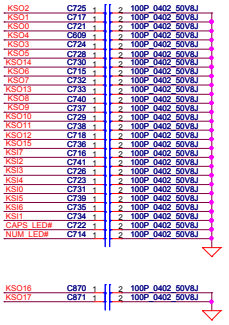
< KEYBOARD CONN 16" >



< KEYBOARD CONN 17" >

< For EMI >

< For EMI >



KSI[0..7] KSI[0..7] 34,35

KSO[0..17] KSO[0..17] 34,35

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Compal Electronics, Inc.

Title: SPI/LPC/PS2/MDC/FM/CIR

Size: Custom | Document Number: LA-4971P | Rev: 1.0

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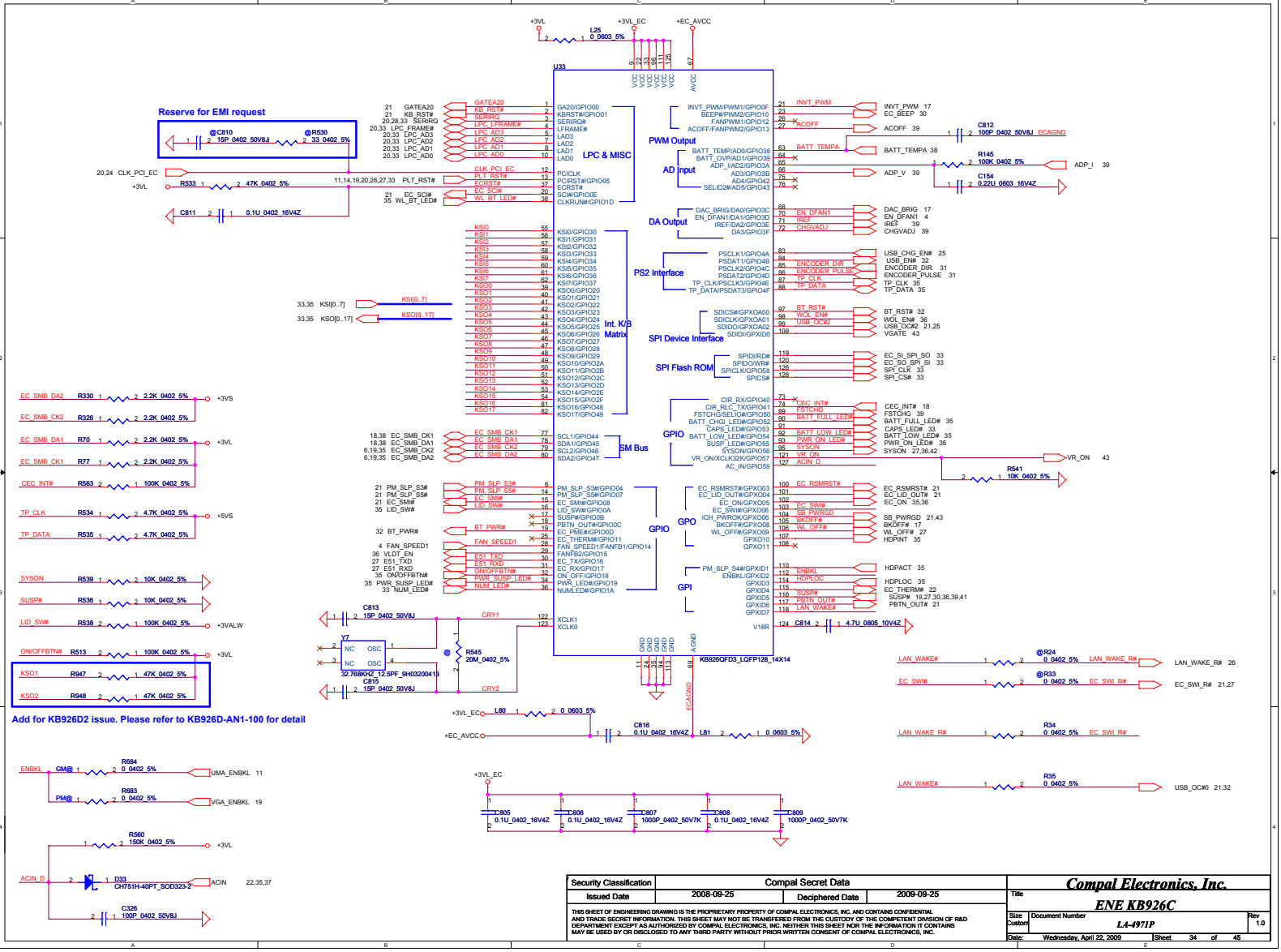
U33
KB926QFD3_LQFP128_14X14
LPC & MISC
PWM Output
AD input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Reserve for EMI request
Add for KB926D2 issue. Please refer to KB926D-AN1-100 for detail
Security Classification
Compal Secret Data
Issued Date
2008-09-25
Deciphered Date
2009-09-25
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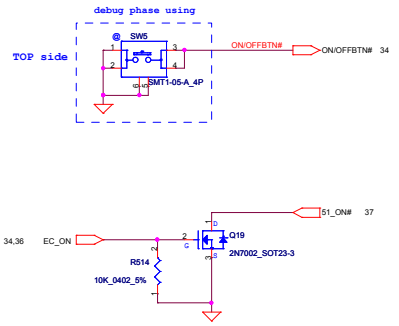
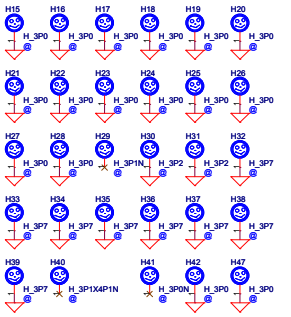
Compal Electronics, Inc.
Title
ENE KB926C
Size
Custom
Document Number
LA-4971P
Rev
1.0
Date:
Wednesday, April 22, 2009
Sheet
34
of
45

< Power Button for Debug >



< Screw Hole >

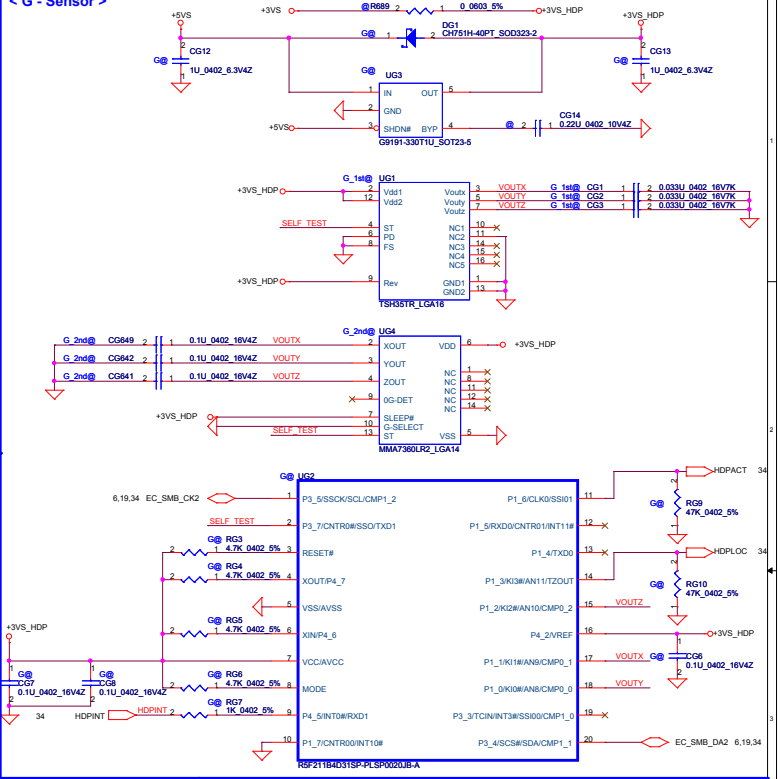


PCB Fedical Mark PAD

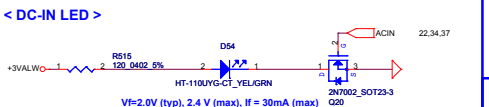
FD1 FD2 FD3 FD4

MDC: H30, H31
VGA: H38, H39
CPU: H32, H33, H34, H35
Mini Card : H36, H37
Others: H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H25, H26, H27, H28, H29, H40, H47

< G - Sensor >



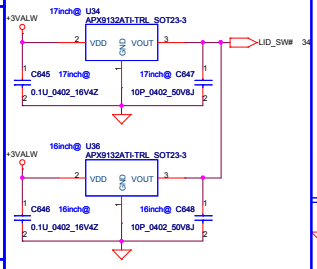
< DC-IN LED >



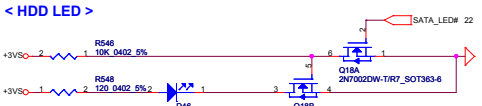
Vf=2.0V (typ), 2.4 V (max), If = 30mA (max)

Remove WiMAX LED control circuit

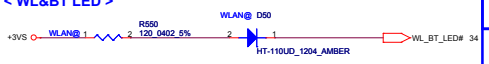
< LID Switch >



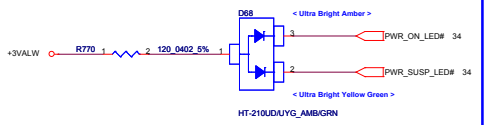
< HDD LED >



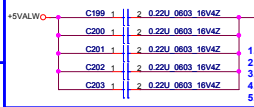
< WL&BT LED >



< POWER-ON & SUSPEND LED >



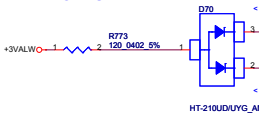
< EMI reserve >



1.C199 : U19
2.C200 : PU5
3.Top side of PU12 for noise bounce.
4.C202 : U25
5.C203 : PU9

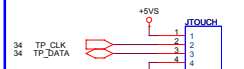
1.U25
2.Botton side of JWLAN for keep noise return path.
3.Top side of PU12 for noise bounce.
4.Top side of PU5 for noise bounce.
5.U19

< BATT CHARGE/FULL LED >

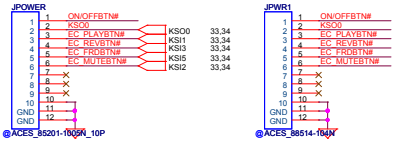


Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

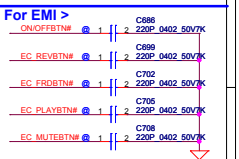
< Touch/B Connector >



< SW/B Connector >



< For EMI >



Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

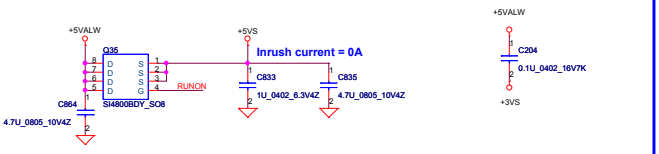
Title: LED/LID/PB/FB/SCREW HOLE

Size: Custom | Document Number: LA-4971P | Rev: 1.0

Date: Wednesday, April 22, 2009 | Sheet 35 of 45

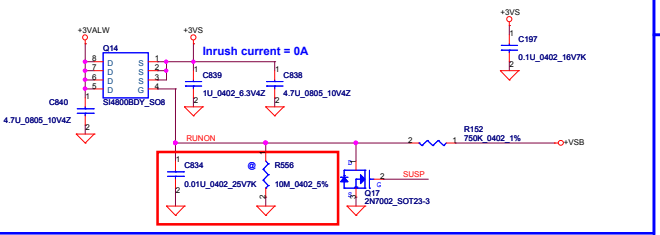
< +5VALW TO +5VS >

< close to PQ20, must EMI confirm >

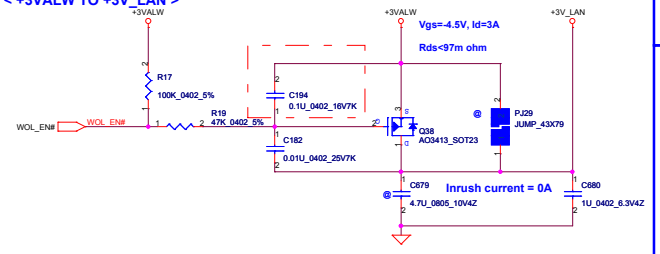


< +3VALW TO +3VS >

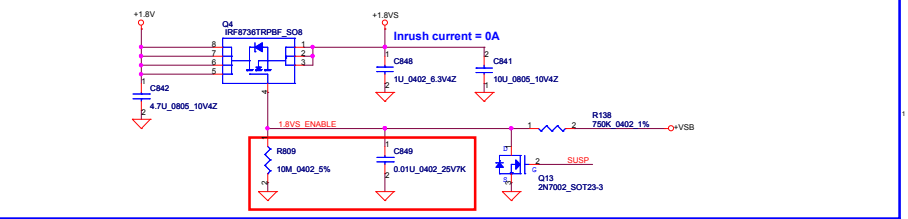
< close to PQ20, must EMI confirm >



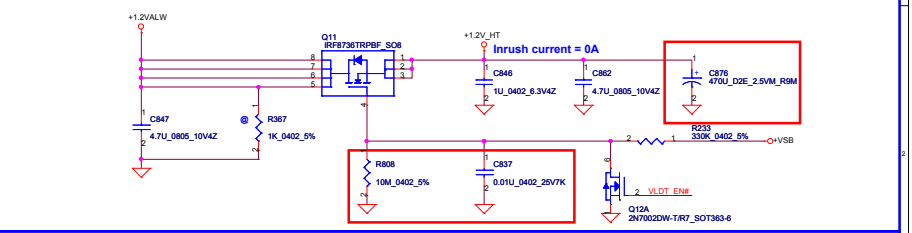
< +3VALW TO +3V_LAN >



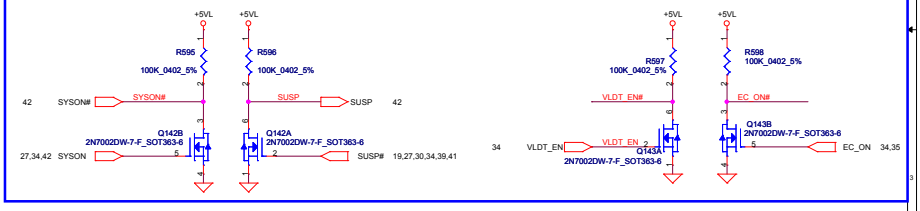
< +1.8V TO +1.8VS >



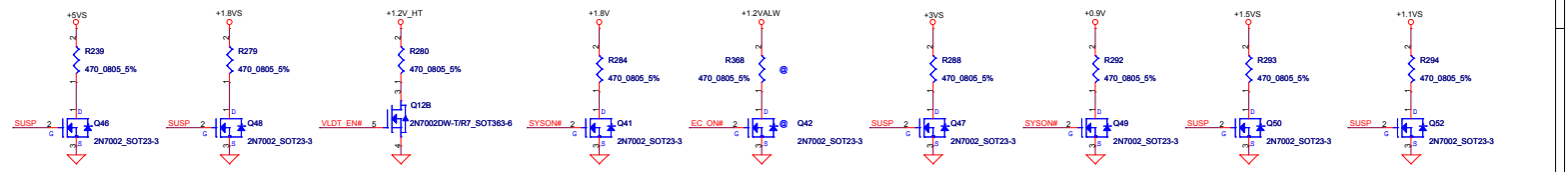
< +1.2VALW TO +1.2V_HT >



< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



< Discharge circuit >



Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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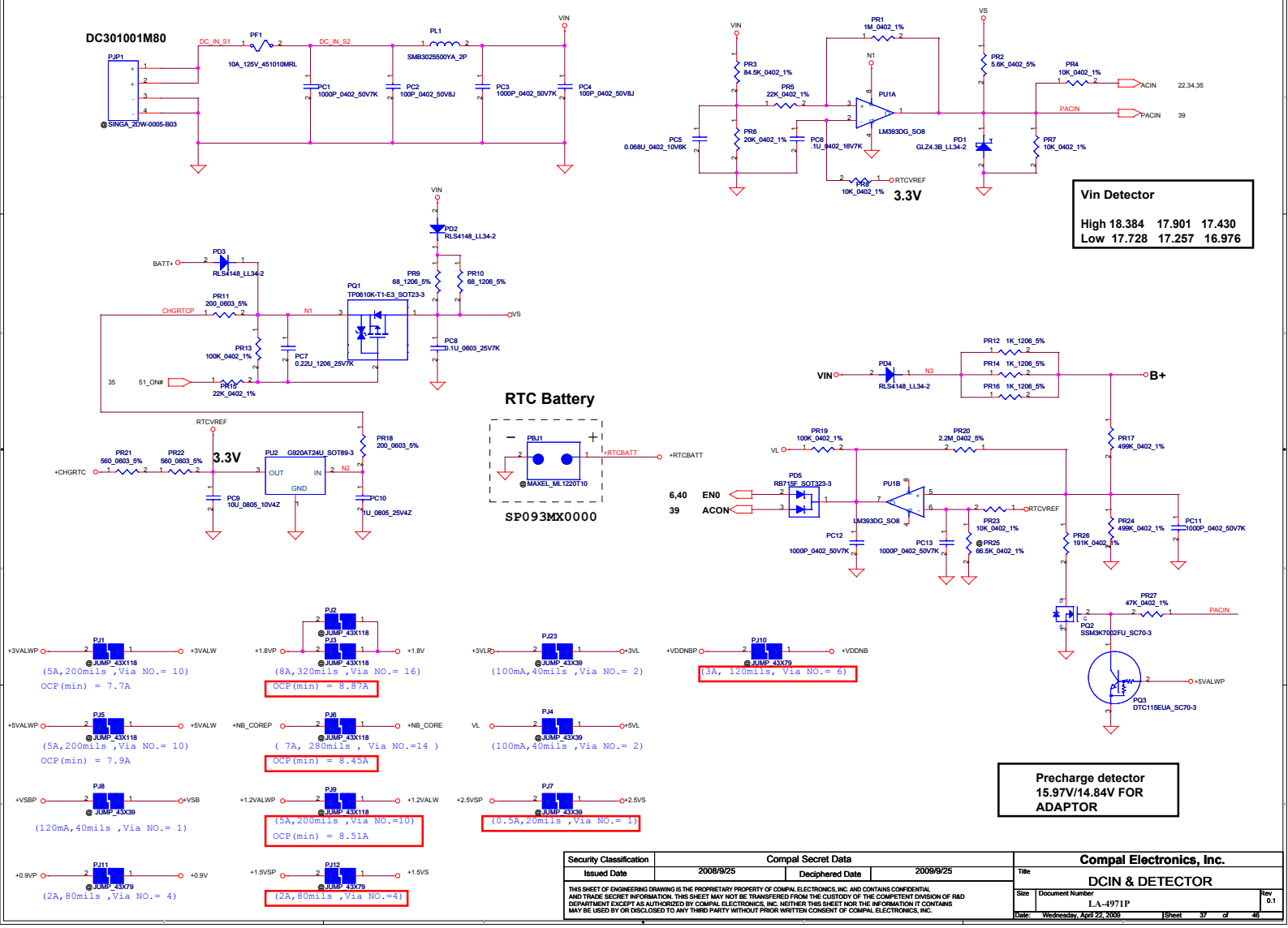
Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size	Document Number	Rev
Custom	LA-4971P	1.0

Date: Wednesday, April 22, 2009 | Sheet 36 of 45



Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

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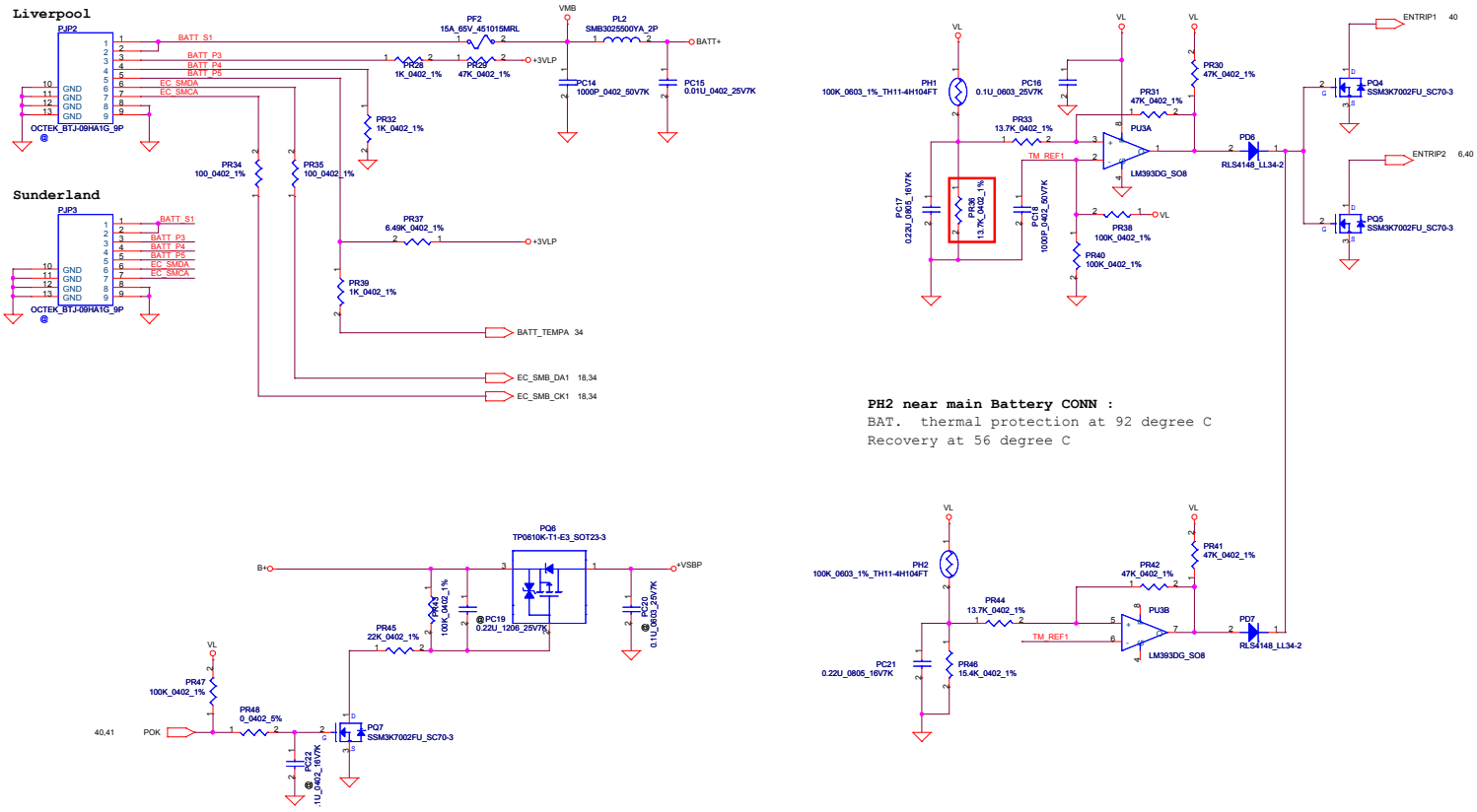
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size | Document Number: LA-4971P | Rev: 0.1

Date: Wednesday, April 22, 2009 | Sheet 37 of 46



Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

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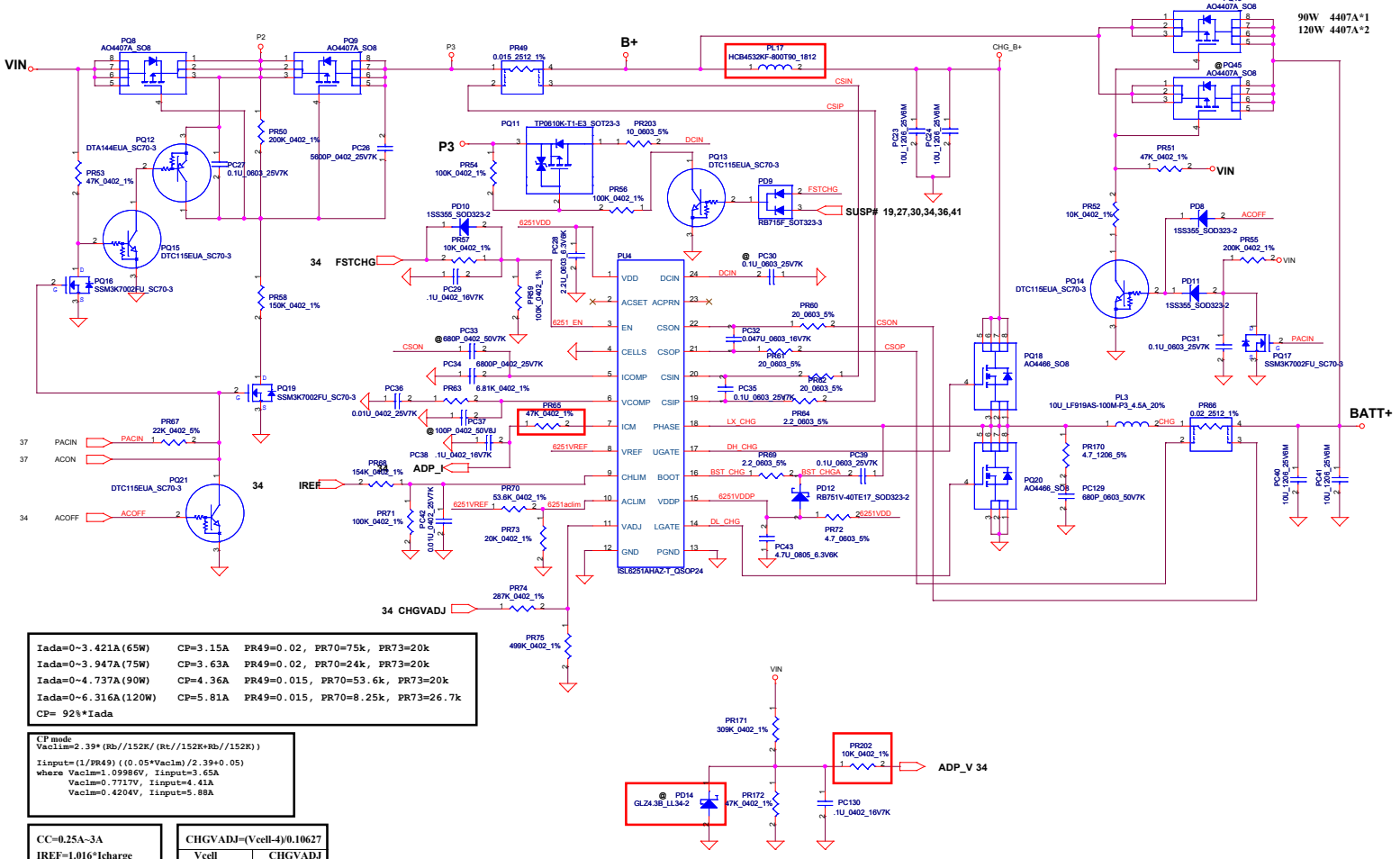
Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number: LA-4971P | Rev: 0.1

Date: Wednesday, April 22, 2009 | Sheet 38 of 46




```
Iada=0~3.421A(65W)    CP=3.15A   PR49=0.02, PR70=75k, PR73=20k
Iada=0~3.947A(75W)    CP=3.63A   PR49=0.02, PR70=24k, PR73=20k
Iada=0~4.737A(90W)    CP=4.36A   PR49=0.015, PR70=53.6k, PR73=20k
Iada=0~6.316A(120W)   CP=5.81A   PR49=0.015, PR70=8.25k, PR73=26.7k
CP= 92%*Iada
```

```
CP mode
Vaclim=2.39*(Rb//152K/(Rt//152K+Rb//152K))

Iinput=(1/PR49)((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.09986V, Iinput=3.65A
      Vaclm=0.7717V, Iinput=4.41A
      Vaclm=0.4204V, Iinput=5.88A
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: LA-4971P | Rev: 0.1

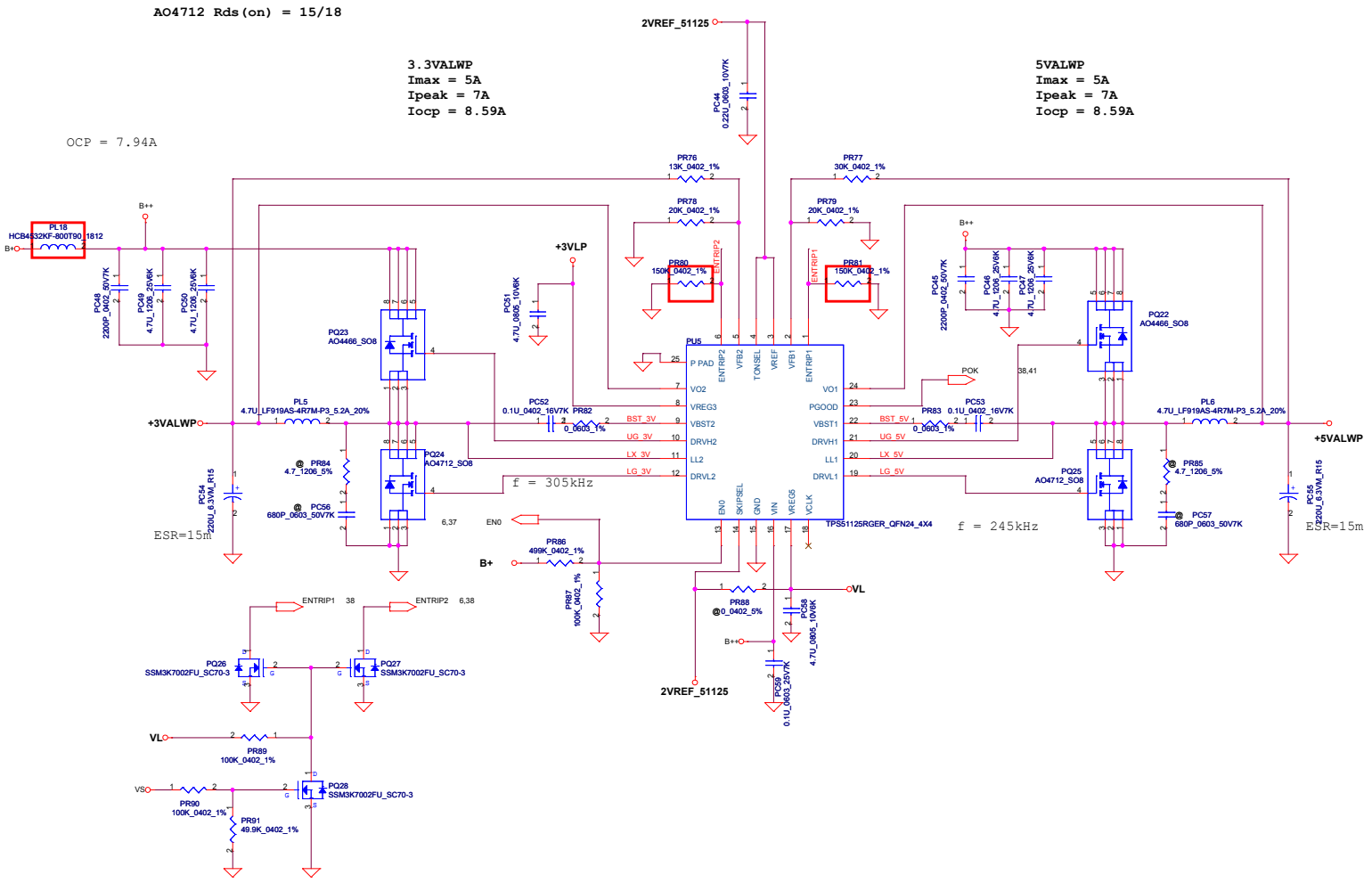
Date: Wednesday, April 22, 2009 | Sheet 39 of 46

AO4712 Rds(on) = 15/18

3.3VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

5VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

OCP = 7.94A



Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

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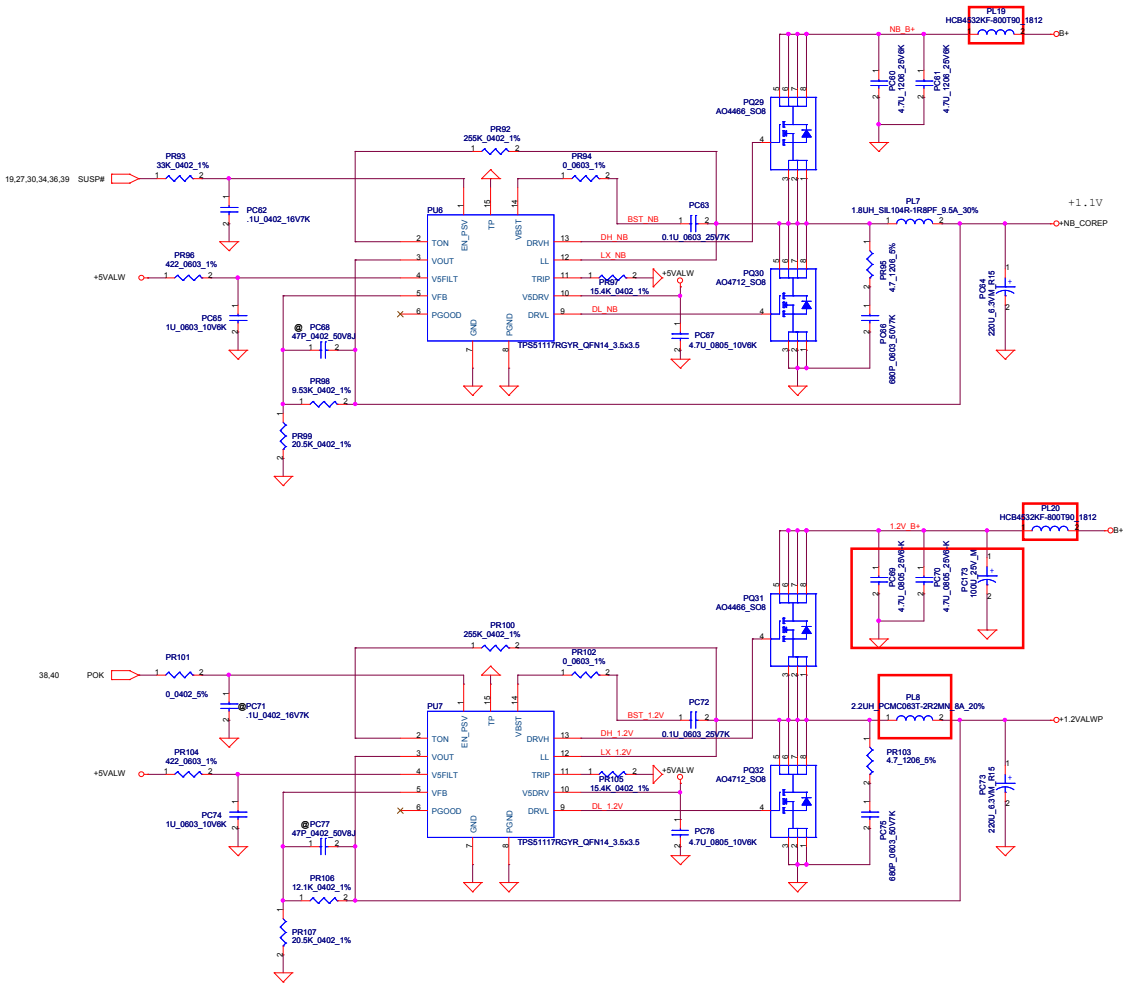
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: LA-4971P | Rev: 0.1

Date: Wednesday, April 22, 2009 | Sheet 40 of 46



Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

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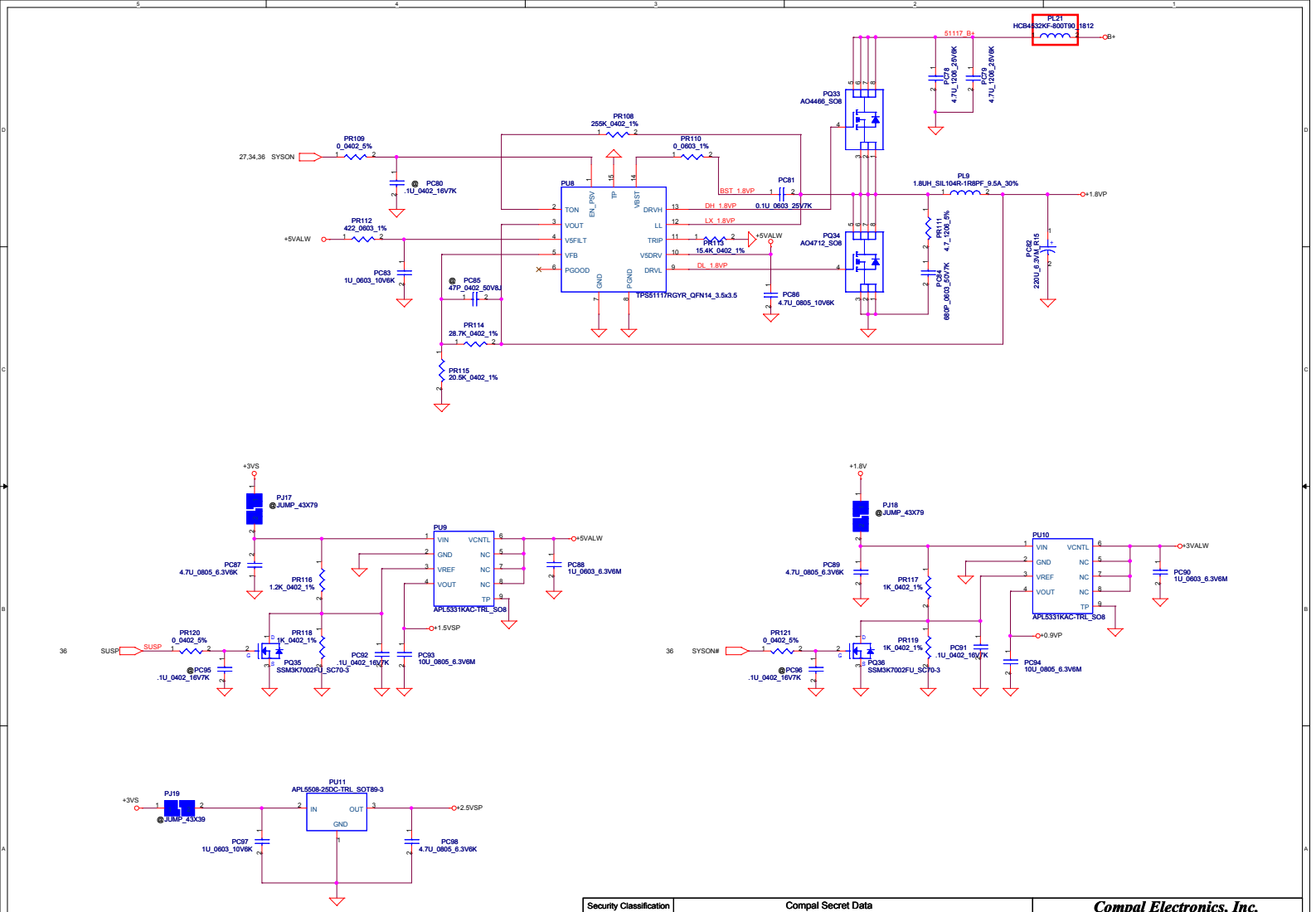
Compal Electronics, Inc.

Title: **NB_COREP/1.2VALWP**

Size | Document Number: LA-4971P | Rev: 0.1

Date: Wednesday, April 22, 2009 | Sheet 41 of 46



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Issued Date	2008/9/25	Deciphered Date	2009/9/25

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Compal Electronics, Inc.

Title: **1.8VP/0.9VP/1.5VSP2.5VSP**

Size | Document Number: LA-4971P | Rev: 0.1

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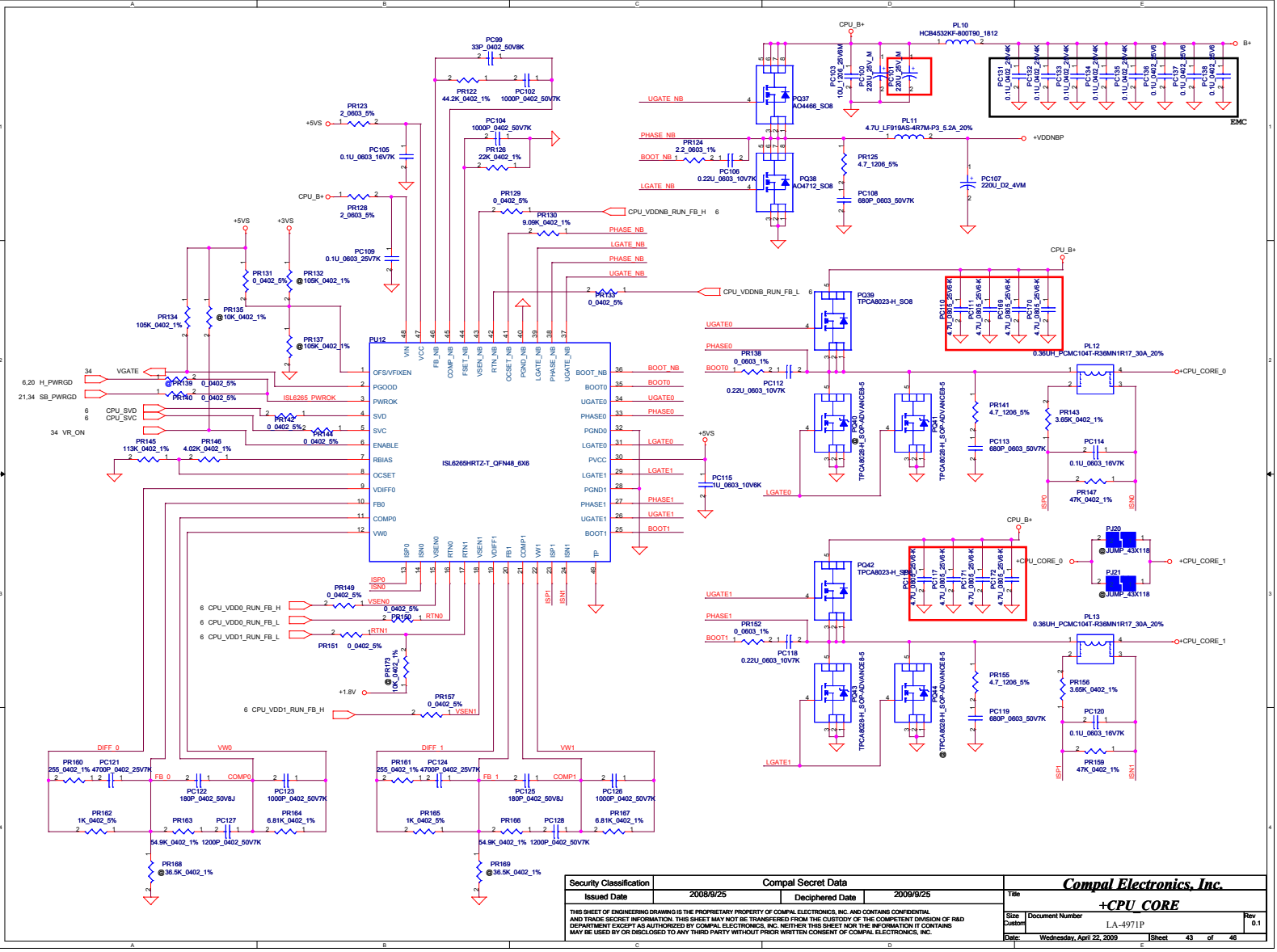

Security Classification	Compal Secret Data		
Issued Date	2008/9/25	Deciphered Date	2009/9/25

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Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
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Version Change List (P. I. R. List) for Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

1. 2009/02/23 --> change R70, R77 from 4.7K to 2.2K
2. 2009/02/23 --> change R178 from 4.7K to 47K
3. 2009/02/26 --> change SPI ROM from SST to MXIC
4. 2009/02/26 --> change D36 from ROHM to PANJI
5. 2009/02/27 --> change the footprint of T9, T10, T11, T12, T19, T20 from TPC12 to TPC24
6. 2009/02/27 --> change 5V power of LCD connector
7. 2009/03/02 --> unmount R556
8. 2009/03/04 --> change RA16 from 5% to 1%
9. 2009/03/10 --> change R146 from 100k ohm to 10k ohm
10. 2009/03/10 --> change Y2 from SJ114P3M730 to SJ114P3MG00
11. 2009/03/11 --> change C686, C699, C702, C705, C706, C708, CA27 from SE074221K00SE to SE074221K80 for Green part
12. 2009/03/11 --> change LAN_WAKE# & EC_SWI#
13. 2009/03/11 --> unmount USB sleep & charge, add R97 & R98
14. 2009/03/11 --> unmount HDMI CEC controller and related components.
15. 2009/03/11 --> connect USB_OC#0 to LAN_WAKE# through 0 ohm
16. 2009/03/12 --> change H42 from NPH to PH
17. 2009/03/12 --> add PR203 10Ohm
18. 2009/03/24 --> change F2 footprint to F_MINISMDC110F-2
19. 2009/03/24 --> Add R370 & R381
20. 2009/03/24 --> change R557's BOM structure from H@ to @
21. 2009/03/24 --> change R440 from 0 ohm to 100k ohm
22. 2009/03/31 --> Replace PJ13, PJ30, PJ14, PJ15, PJ16 by PL17, PL18, PL19, PL20, PL21
23. 2009/04/02 --> Add R969 on E51_TXD
24. 2009/04/02 --> Modify +HDMI_5V_OUT Circuit Remove Q159, R160, Q26, R557, C876 and add D19
25. 2009/04/02 --> Change R440 from 100k to 0 for Askey BT Reset
26. 2009/04/02 --> Change C480's BOM Stuucture from BT@ to @
27. 2009/04/06 --> Change SW5's BOM Stuucture to @ for MP
28. 2009/04/06 --> Add C876 for Power noise issue
29. 2009/04/06 --> Add D20 for Power issue
30. 2009/04/17 --> Change D12's BOM Stuucture to @
31. 2009/04/22 --> Change C876 & C234 from 330u to 470u (SGA00001U00) for Power noise issue

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Issued Date	2008/9/25	Deciphered Date	2009/9/25

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12 52 VGA_CORE 1/2 Compal for EMI requset Add PR7

HW4 Product Improvement Record (P.I.R.)

< Liverpool & Sunderland >

< R1 for customer BOM STRUCTURE >			< R3 for mass production BOM STRUCTURE >		
RS780MN	U3	RS780MNR1@ RS780MN R1	RS780MN	U3	RS780MNR3@ RS780MN R3
RS780MC	U3	RS780MCR1@ RS780MC R1			
RX781	U3	RX781R1@ RX781 R1	RX781	U3	RX781R3@ RX781 R3
SB700	U15	SB700R1@ SB700R1			

< Tigris >

< R1 for customer BOM STRUCTURE >			< R3 for mass production BOM STRUCTURE >
RS880MN	U3	RS880MNR1@ RS880MN R1	RS880MN
RS880MC	U3	RS880MCR1@ RS880MC R1	RS880MC
RX881	U3	RX881R1@ RX881 R1	RX881
SB710	U15	SB710R1@ SB710 R1	SB710

< DC Jack >

DC-IN	PJP1	16inch_45@ PJP1
DC-IN	PJP1	17inch_45@ PJP1

Use MEMO : change UG1 R5F211B4D31SP (SA000037Y60) to R5F211B4D34SP (SA00003A600)

< PCB >

PCB	ZZZ	PCB 075 LA-4971P LS-4971P/4972P/4973P REV1.0 M/B

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Issued Date	2008-09-25	Deciphered Date 2009-09-25	Title PIR
			Size Document Number Rev 1.0
			Date: Wednesday, April 22, 2009 Sheet 45 of 45

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