

Compal Confidential

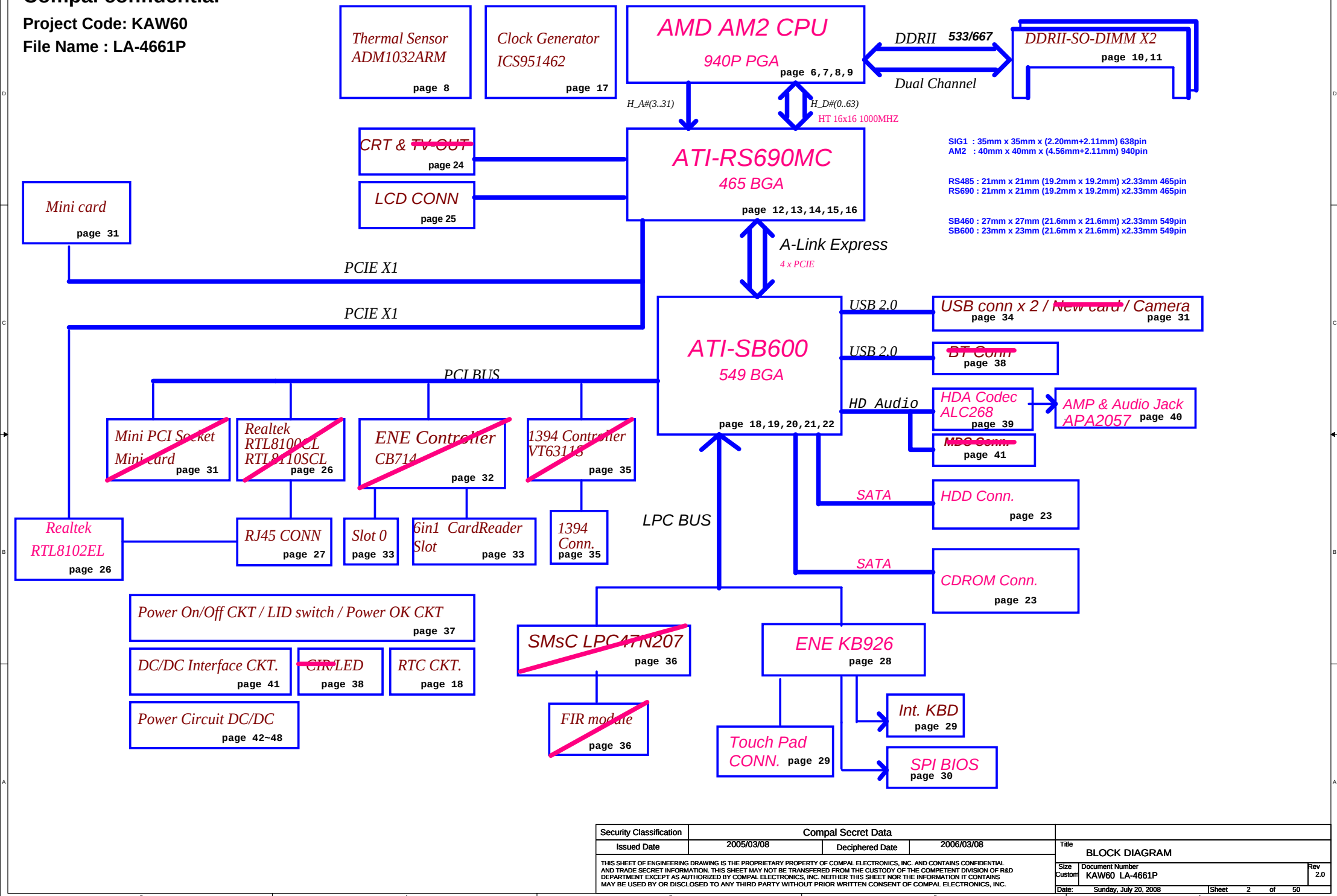
KAW60 Schematics Document

AMD AM2 / RS690MC / SB600

2008 / 08 / 08 Rev:1.0 FOR Pre-MP

Security Classification		Compal Secret Data			
Issued Date		2005/05/09	Deciphered Date		2006/03/08
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File Name : LA-4661P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000X b		

SB600 SM Bus address

Device	Address
Clock Generator (ICS951462)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

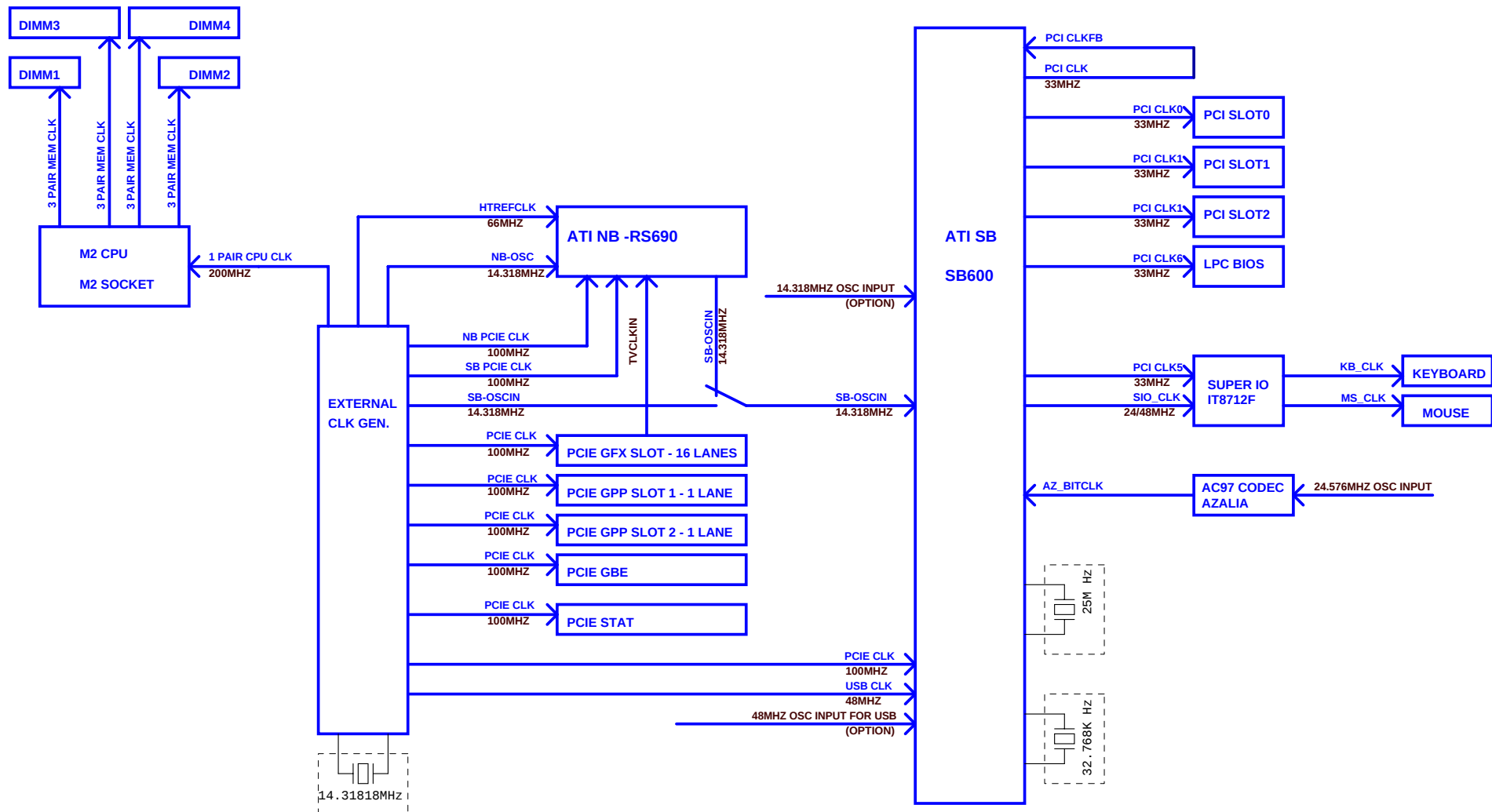
SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

[illegible]

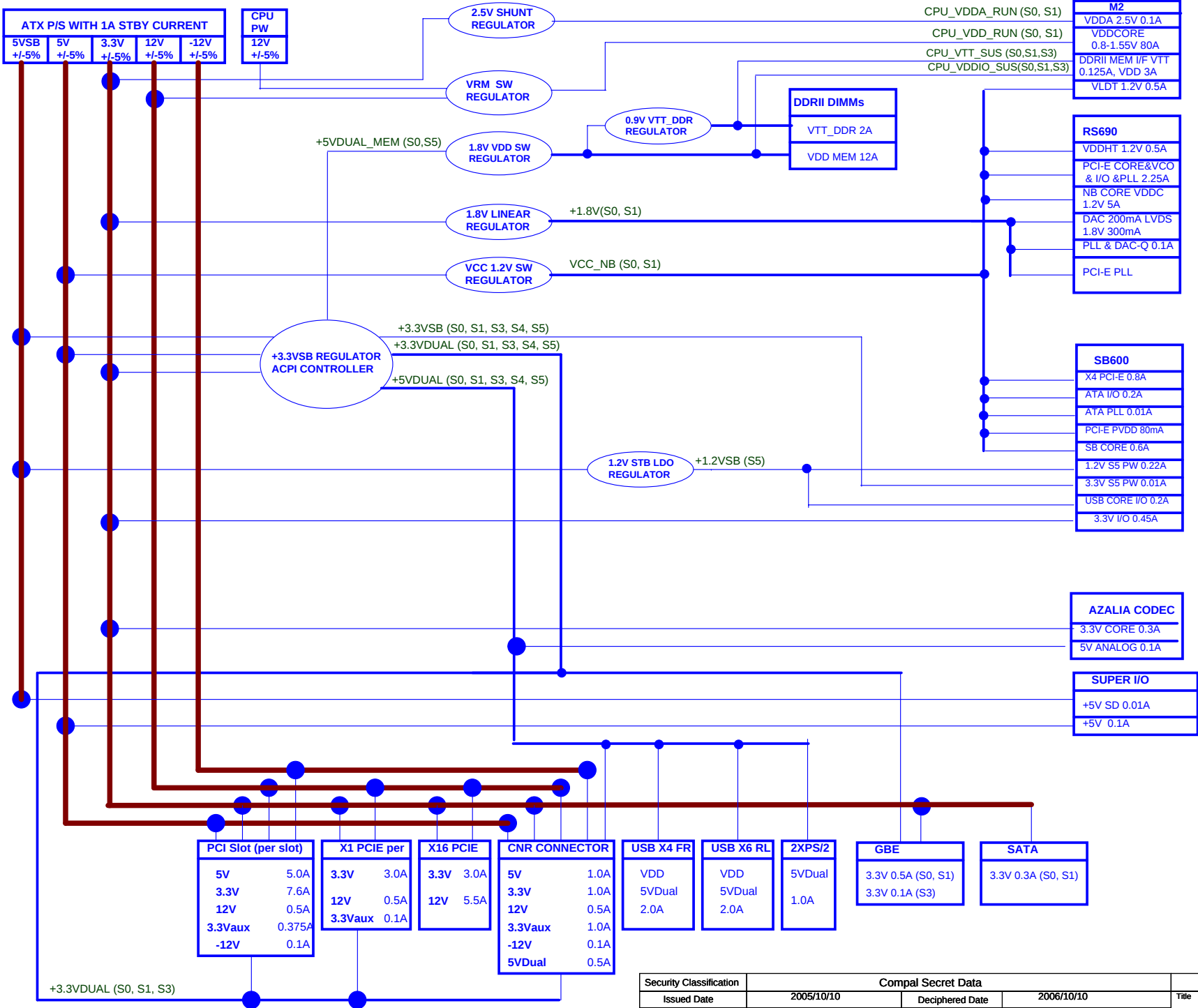
Security Classification		Compal Secret Data		Title TABLE OF CONTENTS		
Issued Date	2005/03/08	Deciphered Date	2006/03/08			
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				Custn	HCW51 LA-3121P	2.0
				Date:		Thursday, July 24, 2008



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				Sheet 4 of 50

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%



Security Classification		Compal Secret Data		Title	
Issued Date	2005/10/10	Deciphered Date	2006/10/10	POWER DELIVERY CHART	
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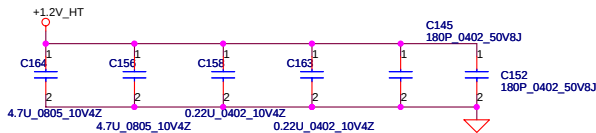
PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Trace length limit (Don't care)

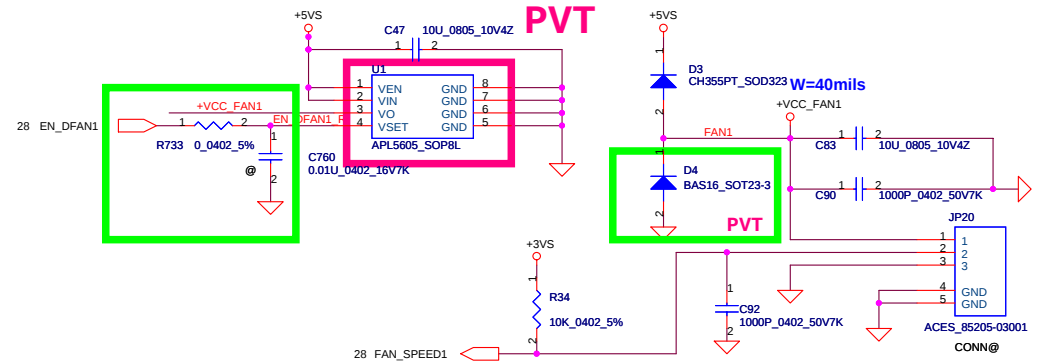
CONN@
SOC127MM48X51-948! 6090022000; JCPU1
TEMP SYMBOL



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDLT0 POWER PINS

FAN Conn



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KEEP THEM CLOSE TO
WITHIN 1"

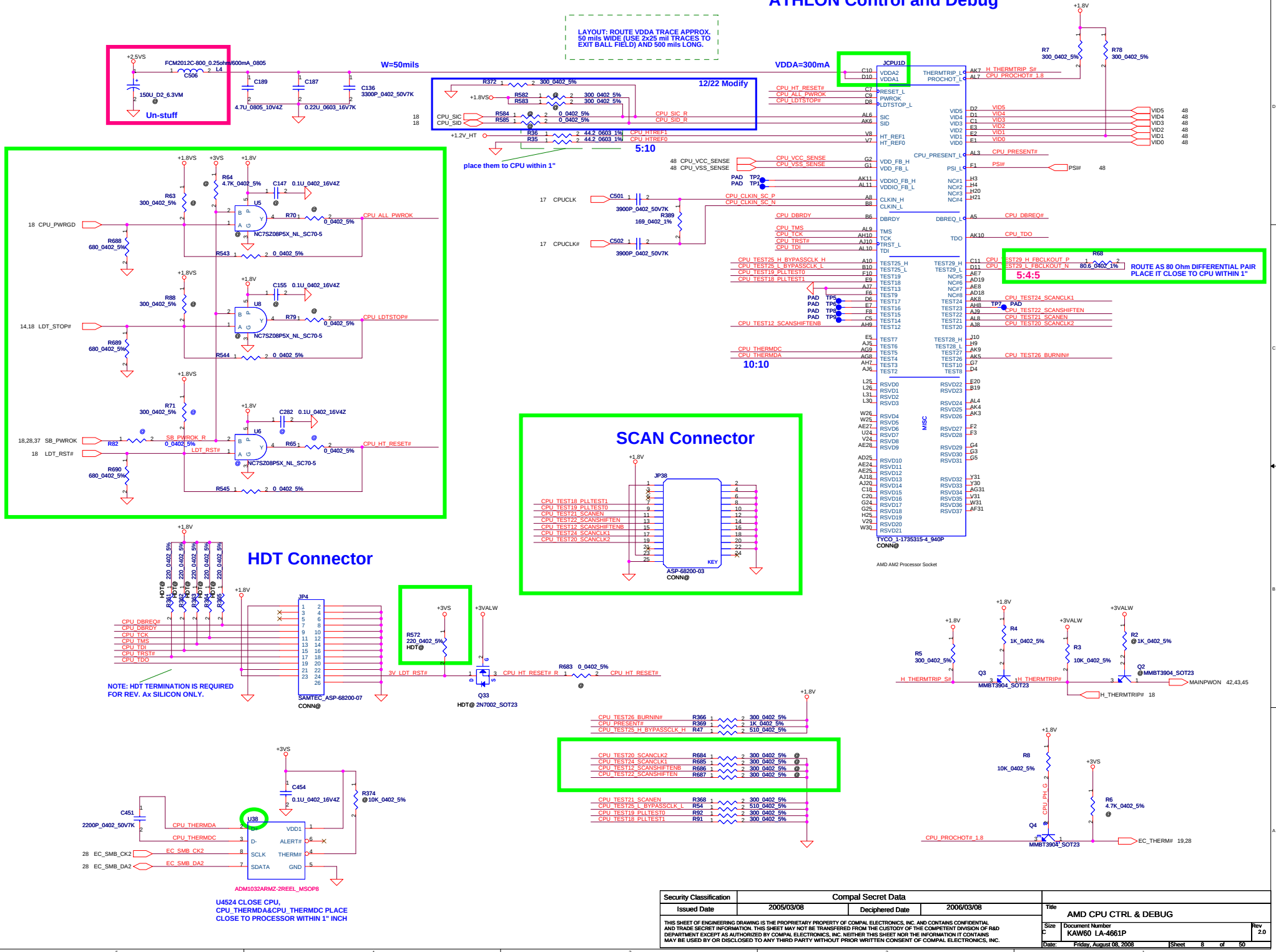


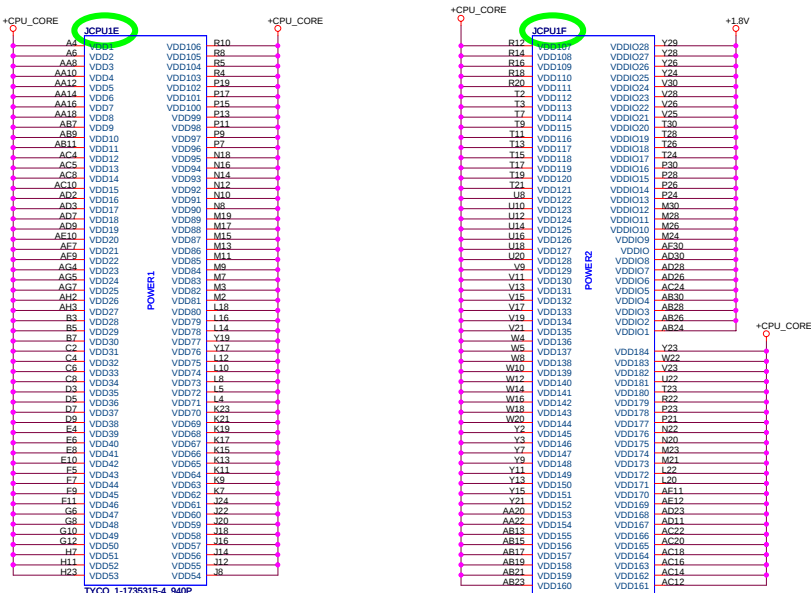
To reverse SODIMM socket



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ATHLON Control and Debug

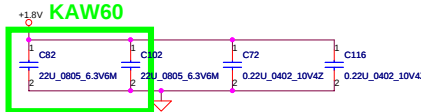




AMD Processor Socket

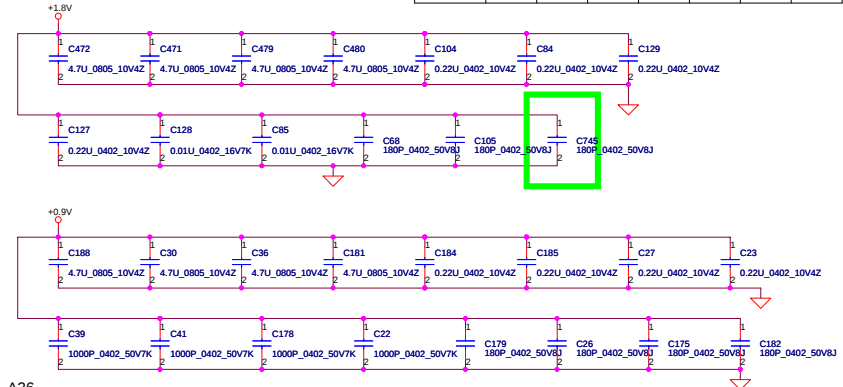


AMD Processor Socket



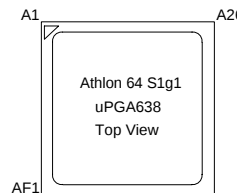
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE

	+1.8V	22u	10u	4.7u	.22u	.01u	180p	.0047u
HCW51		2	4	6	2	2		
Moray	2		2	5	1	3	2	
KAW60	2		4	6	2	3		

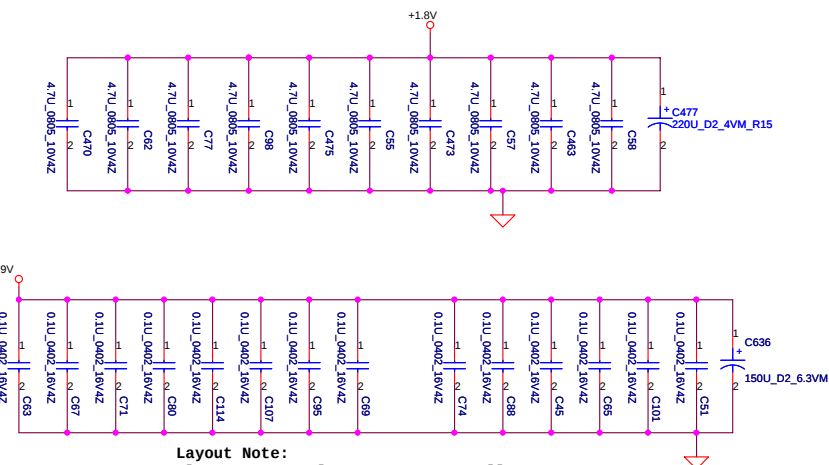
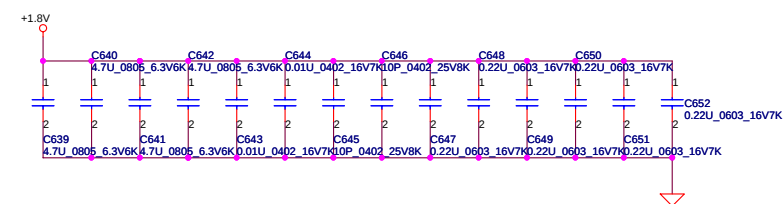
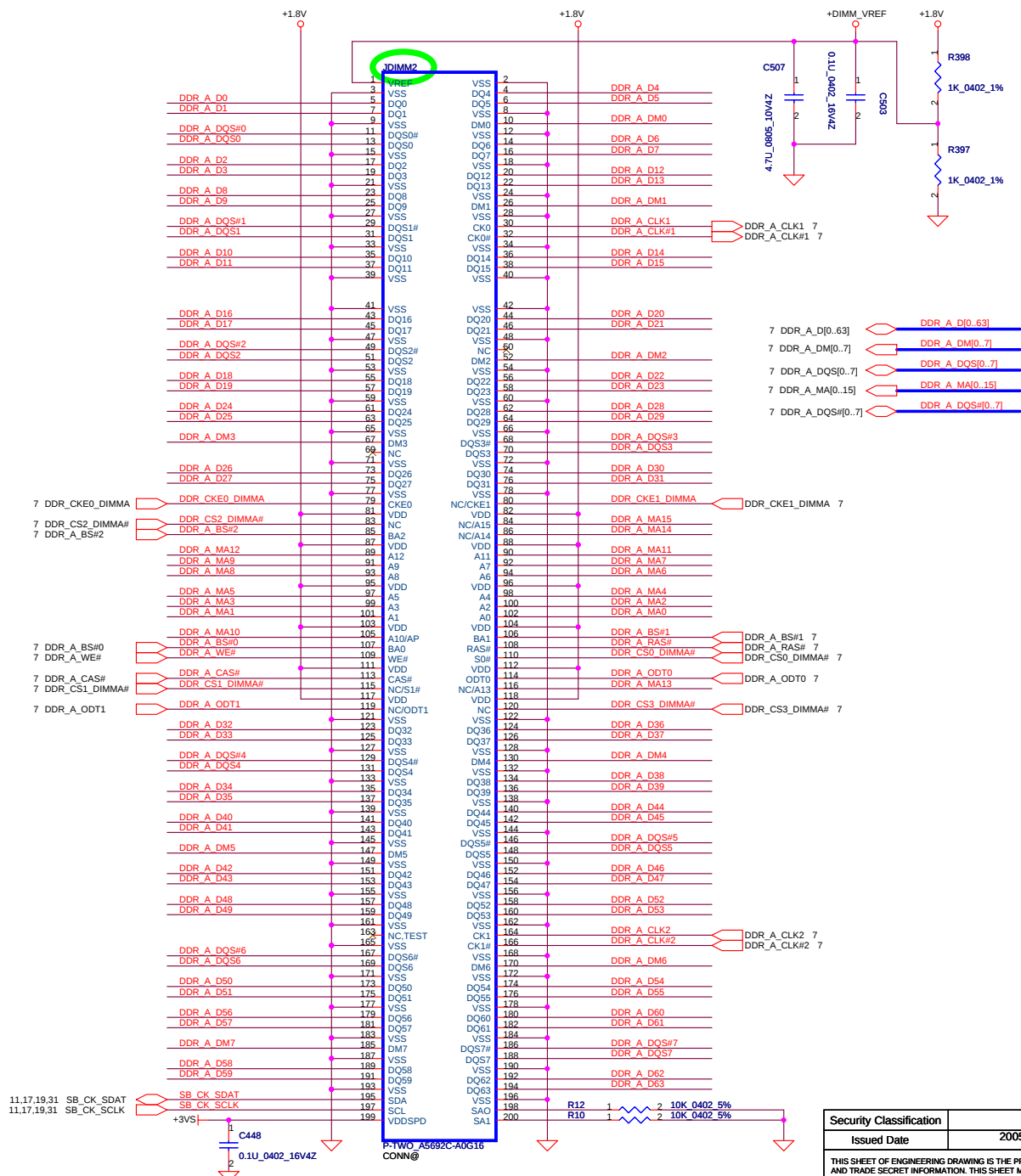


	+0.9V	4.7u	.22u	.0047u	1000p	180p
HCW51		4	4		4	4
Moray	2	4	4		4	4
KAW60	4	4			4	4

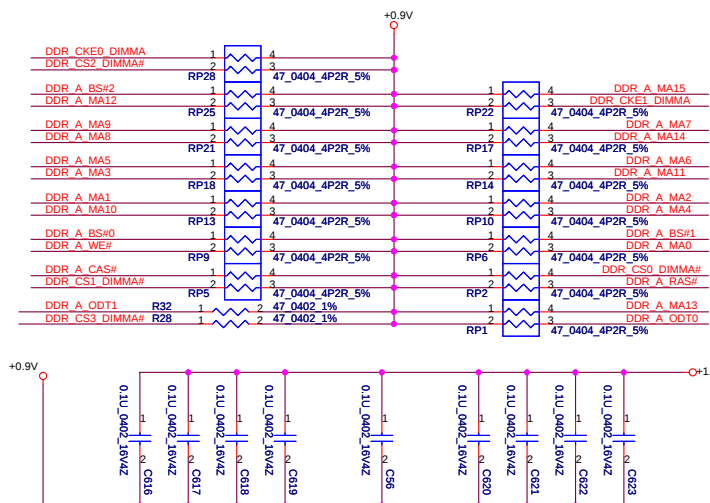
PROCESSOR POWER AND GROUND



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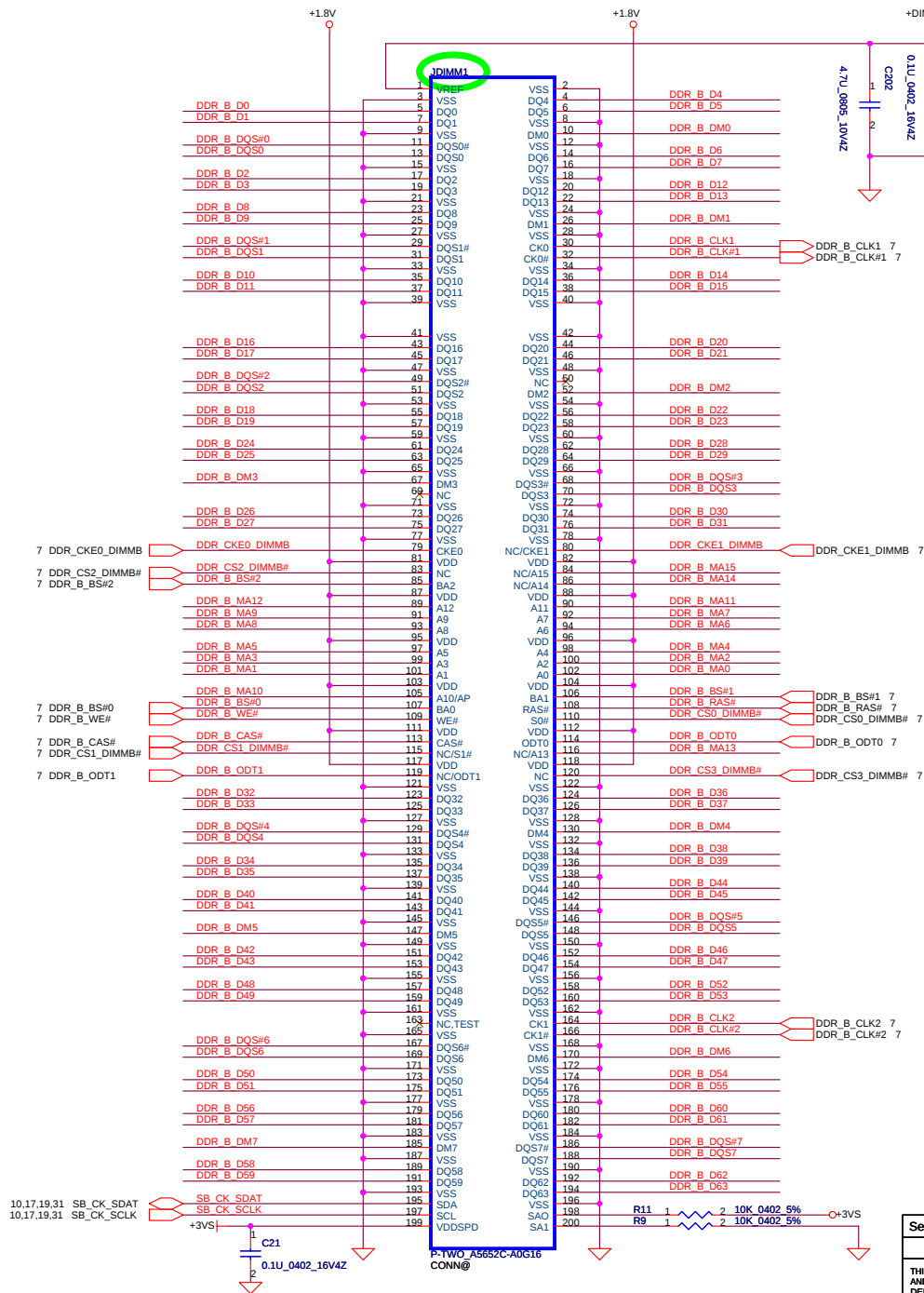


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

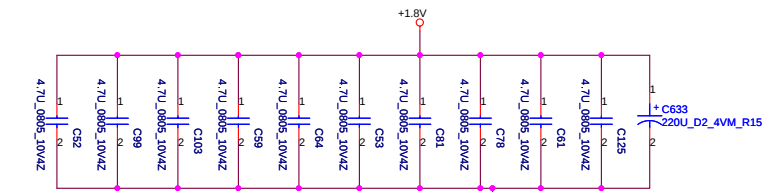


Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V

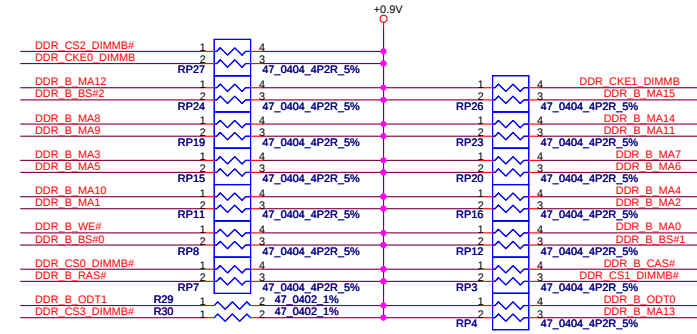
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- 7 DDR_B_D[0..63]
- 7 DDR_B_DM[0..7]
- 7 DDR_B_DQS[0..7]
- 7 DDR_B_MA[0..15]
- 7 DDR_B_DQS#0..7]



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V



Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V

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								DDR2 SO-DIMM II	
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								50	



Power Signal	S0	S1	S3	S4/S5	S6
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

[illegible]

GROUND

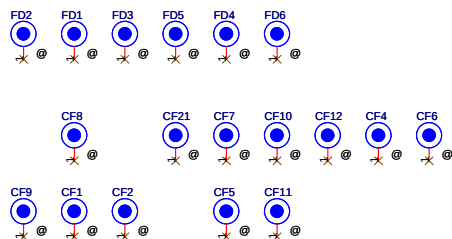
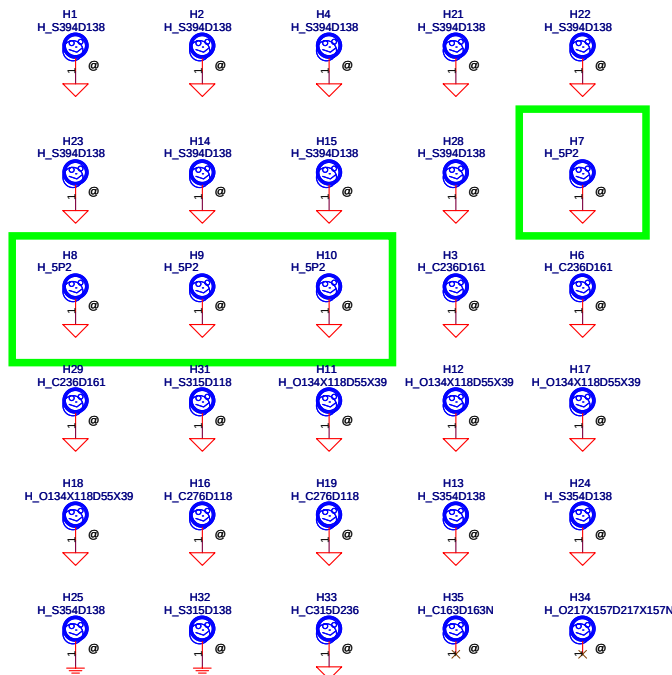
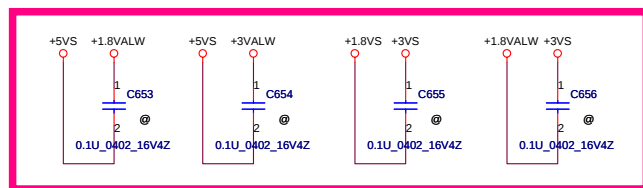
Component	Component	Component
A25	VSS1	VSSA2
F11	VSS2	VSSA3
D21	VSS3	VSSA4
E3	VSS4	VSSA5
G11	VSS5	VSSA6
Y23	VSS6	VSSA7
P11	VSS7	VSSA8
R24	VSS8	VSSA9
AE18	VSS9	VSSA10
M15	VSS10	VSSA11
J22	VSS11	VSSA13
G23	VSS12	VSSA15
J12	VSS13	VSSA16
L12	VSS14	VSSA17
L14	VSS15	VSSA18
L20	VSS16	VSSA19
L23	VSS17	VSSA20
M11	VSS18	VSSA21
M20	VSS19	VSSA22
M23	VSS20	VSSA24
M25	VSS21	VSSA25
N12	VSS22	VSSA26
N14	VSS23	VSSA27
L24	VSS25	VSSA28
P13	VSS26	VSSA30
P20	VSS27	VSSA32
P15	VSS28	VSSA33
R14	VSS29	VSSA34
R20	VSS30	VSSA35
W23	VSS31	VSSA36
Y25	VSS32	VSSA37
AD25	VSS33	VSSA38
U20	VSS34	VSSA39
H25	VSS35	VSSA40
W24	VSS36	VSSA41
Y22	VSS37	VSSA42
AC23	VSS38	VSSA44
D25	VSS39	VSSA45
G24	VSS40	VSSA46
AC14	VSS41	VSSA47
AC22	VSS42	VSSA48
R23	VSS44	VSSA49
C4	VSS45	VSSA50
AE22	VSS46	VSSA51
T23	VSS47	
T25	VSS48	
R17	VSS49	
H23	VSS50	
M17	VSS51	
AC15	VSS52	
F17	VSS53	
D4	VSS54	
M13	VSS55	
AC16	VSS56	
H12	VSS57	
B7	VSS59	
	VSS60	
	VSS61	
	VSS62	

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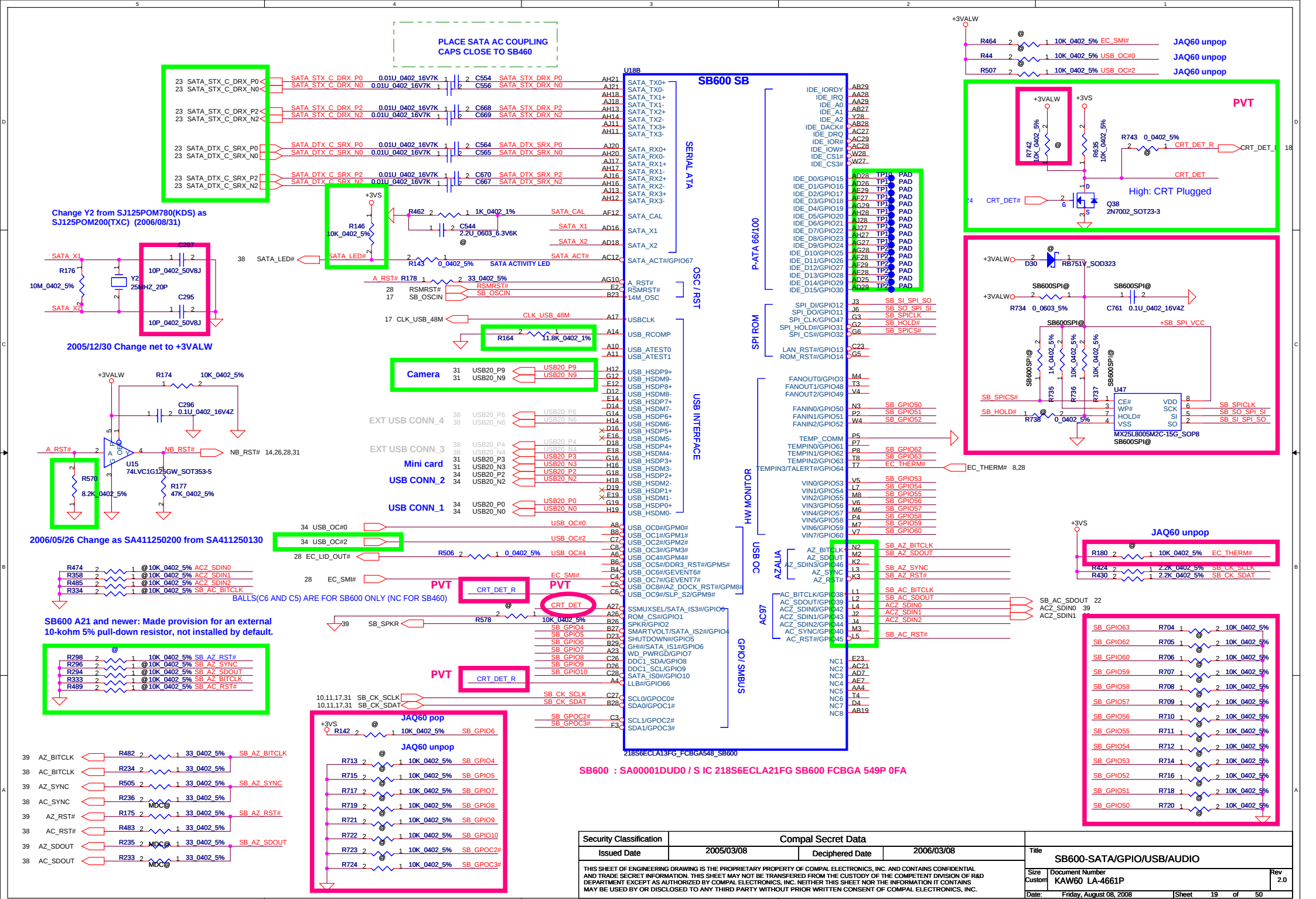


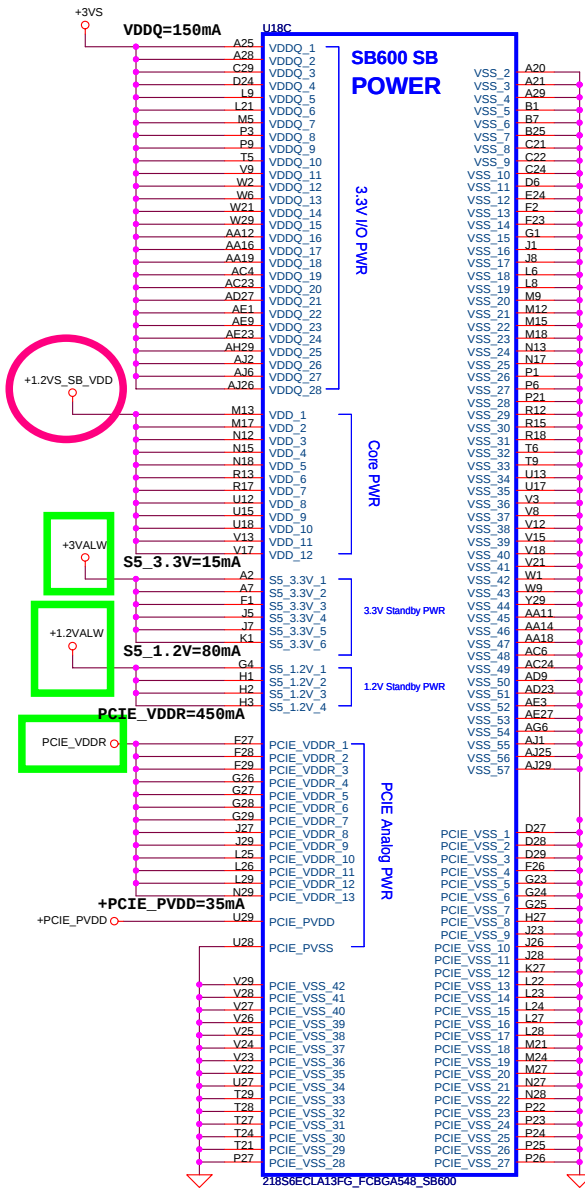
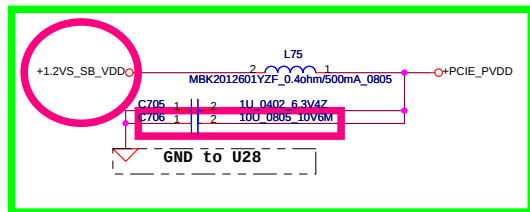
LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



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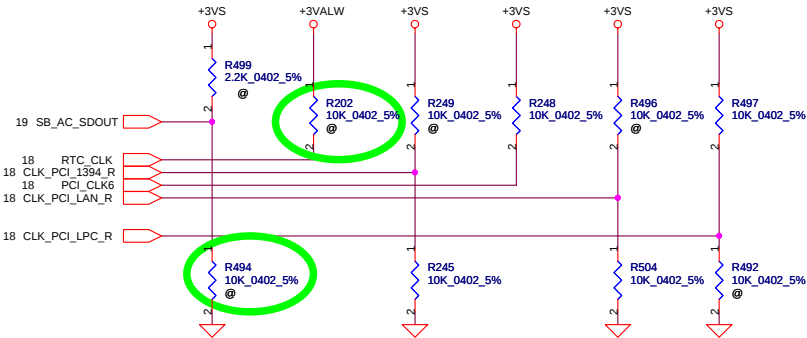


SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

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REQUIRED STRAPS

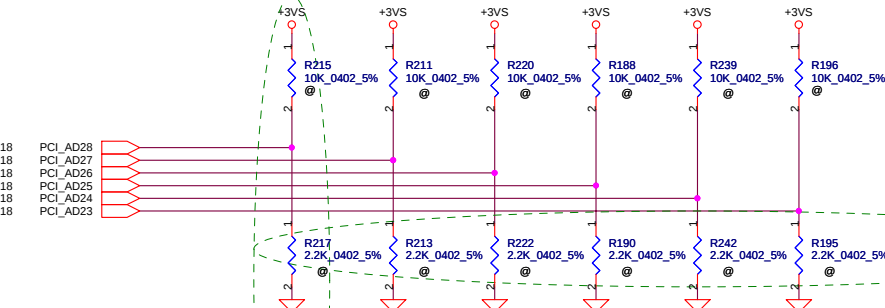
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



					SB600		SB460	
	AC_SDOOUT	RTC_CLK	PCI_1394_R	PCI_CLK6	PCI_LAN_R	PCI_LPC_R	PCI_LAN_R	PCI_LPC_R
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]			

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

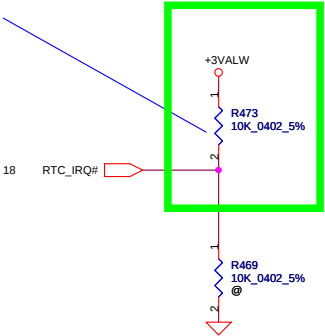


	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

NOTE: R473 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.

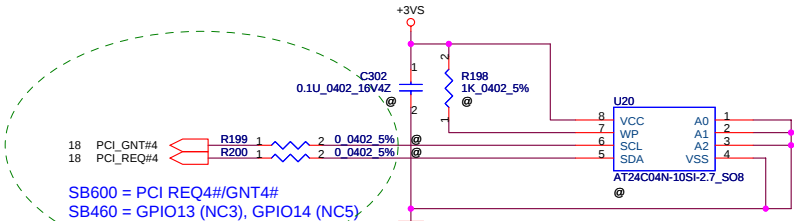


SB460 ONLY

	ACPWRON	SPDIF_OUT	PCI_MINI_R	PCI_PCM_R	PCI_SIO_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

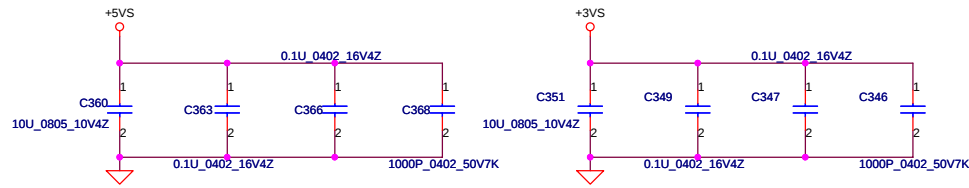


SB PCIE EEPROM STRAPS

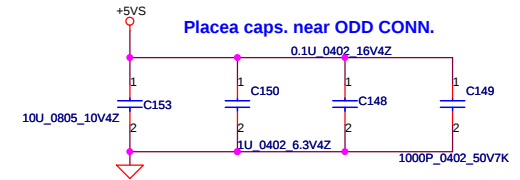
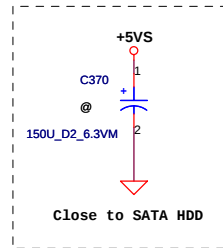
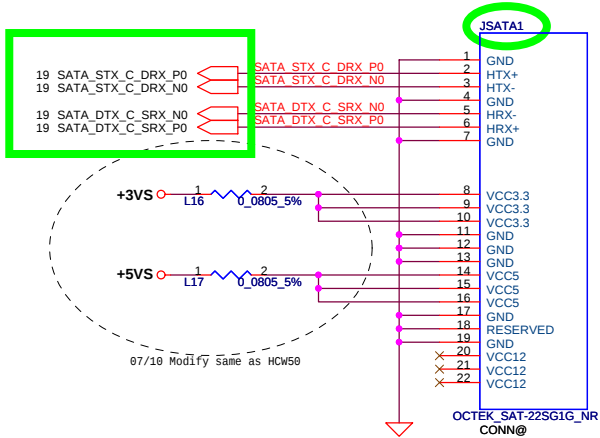
SB460 ONLY

SB600 ONLY

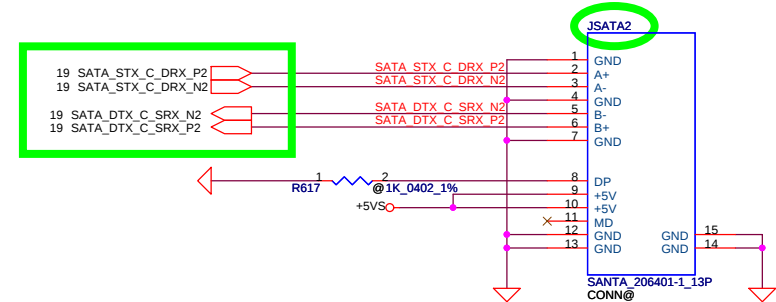
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Issued Date		2005/03/08		Deciphered Date		2006/03/08		Title							
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								Size	Document Number						Rev
									KAW60 LA-4661P						2.0
								Date:	Friday, August 08, 2008				Sheet	22	of



SATA HDD CONN

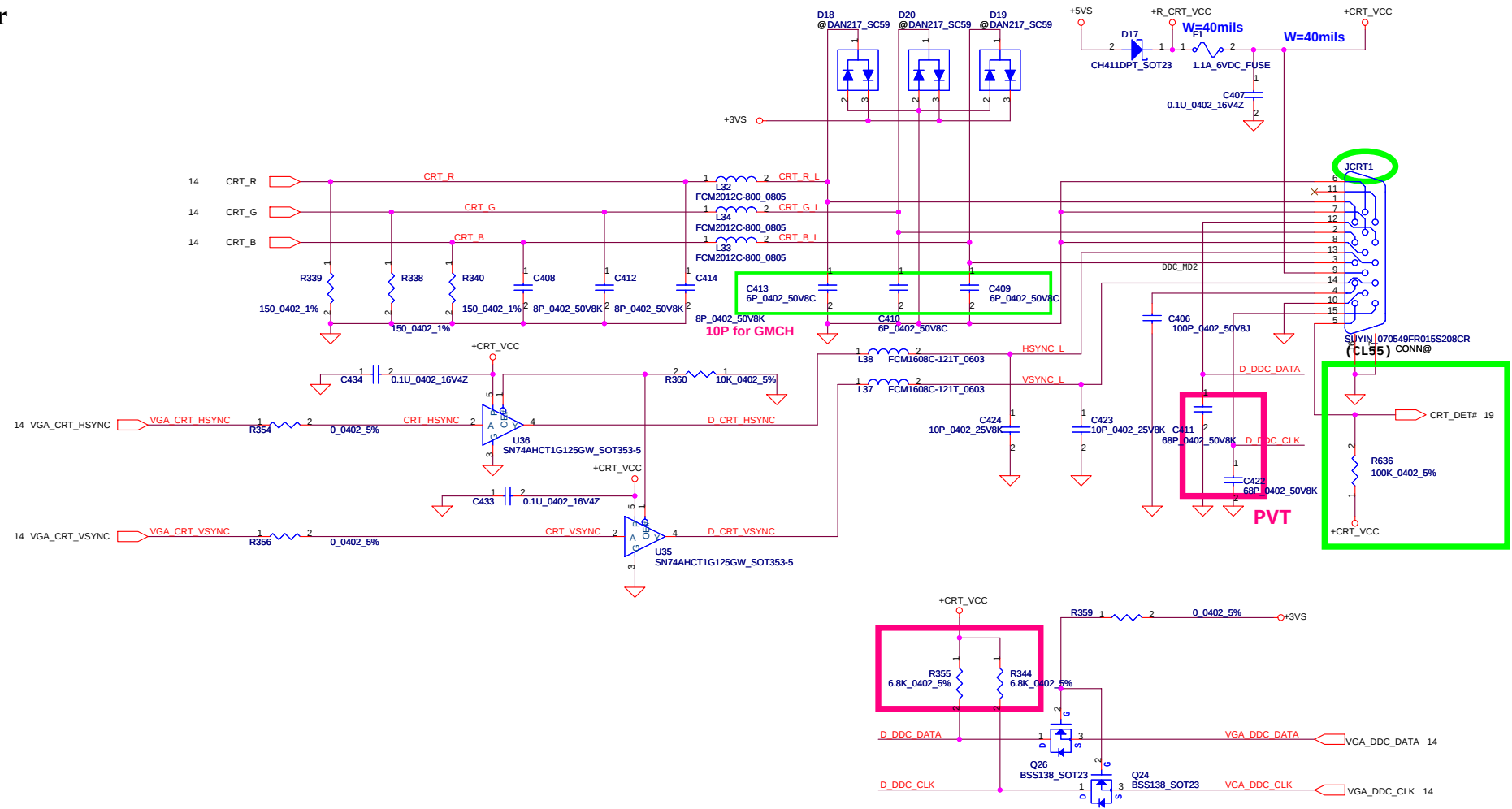


SATA ODD CONN



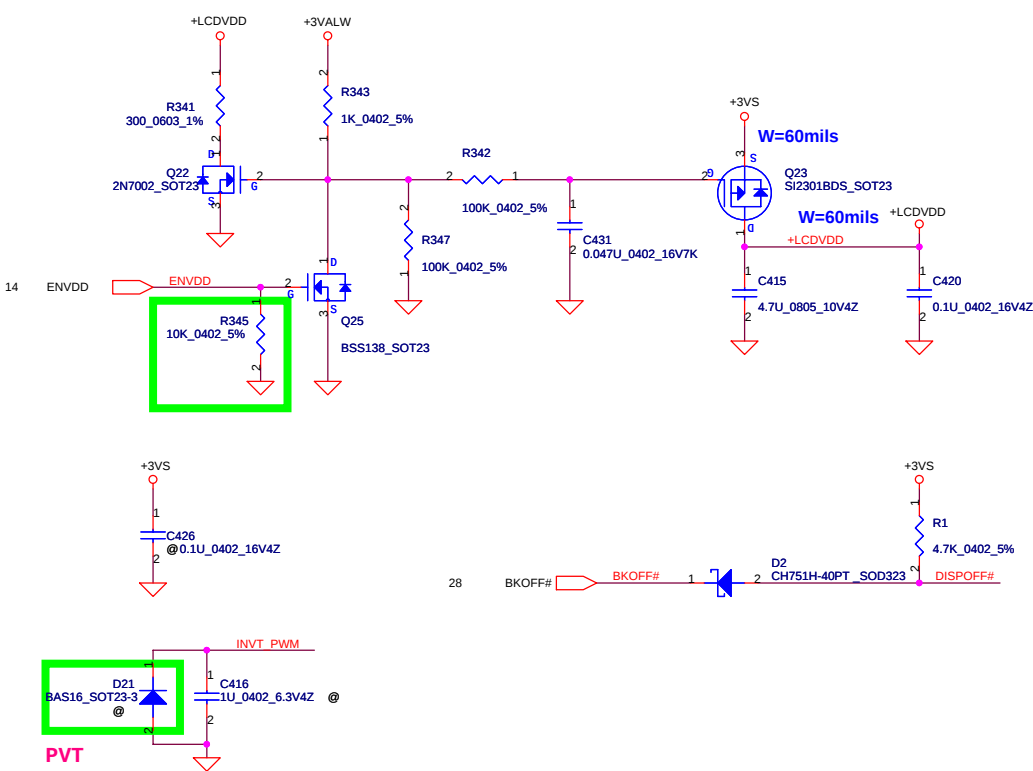
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				Date: Friday, August 08, 2008	Rev 2.0
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CRT Connector

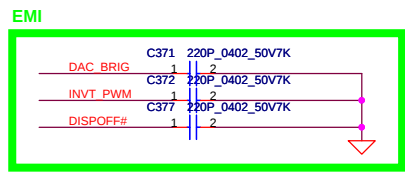
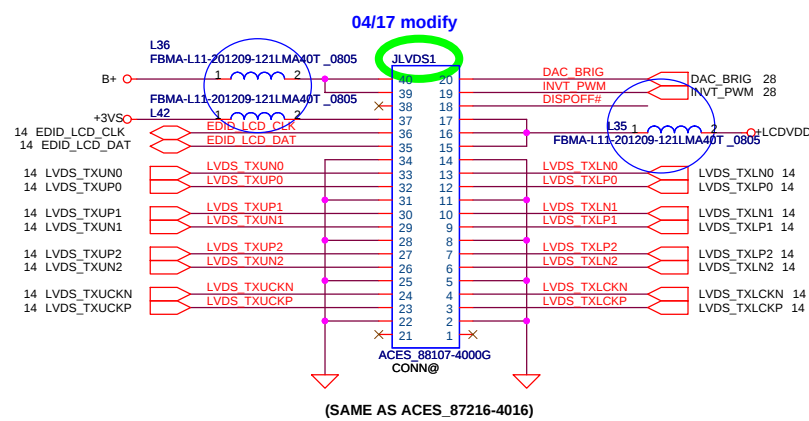


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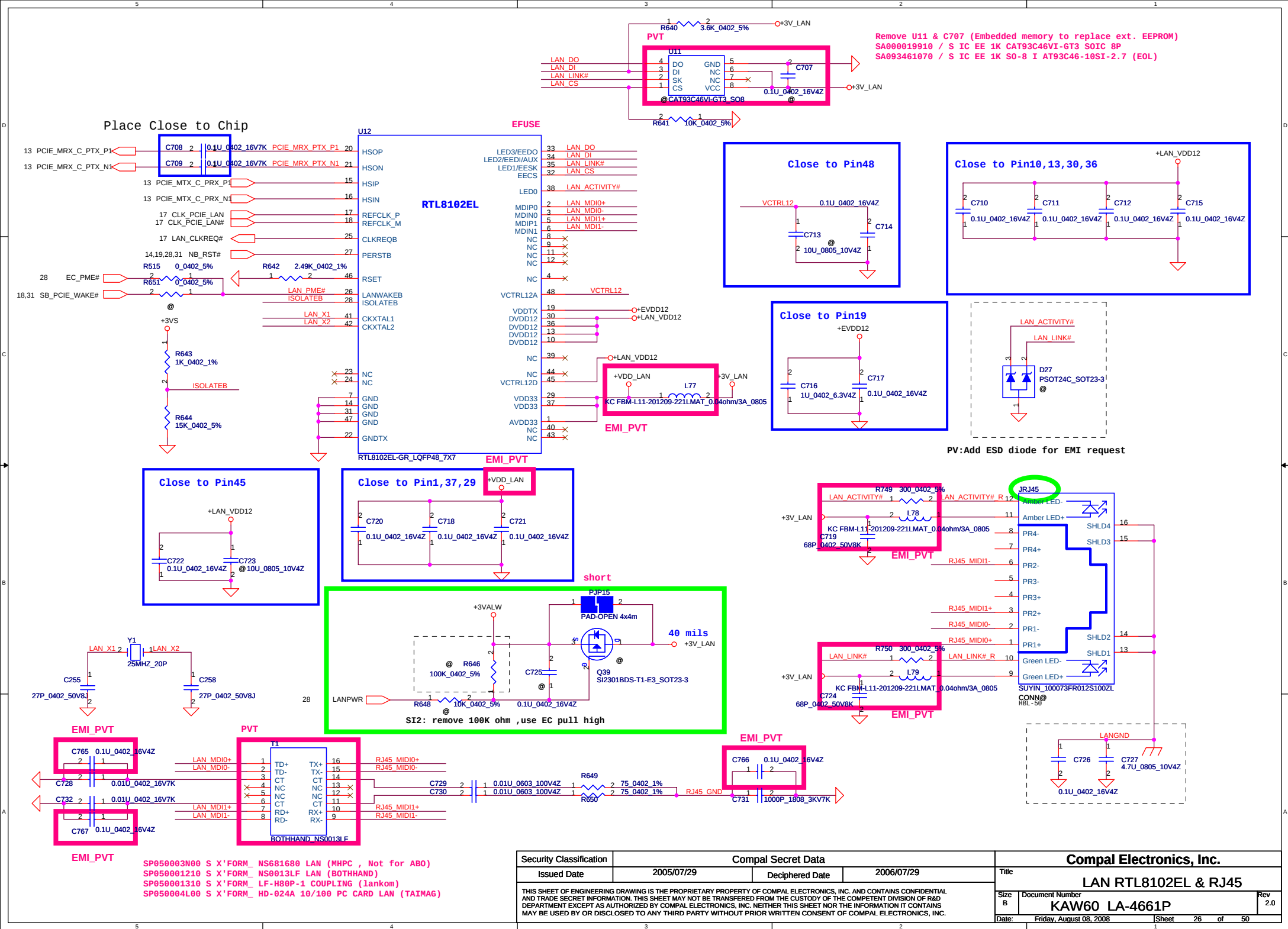
LCD POWER CIRCUIT



LCD/PANEL CONN.

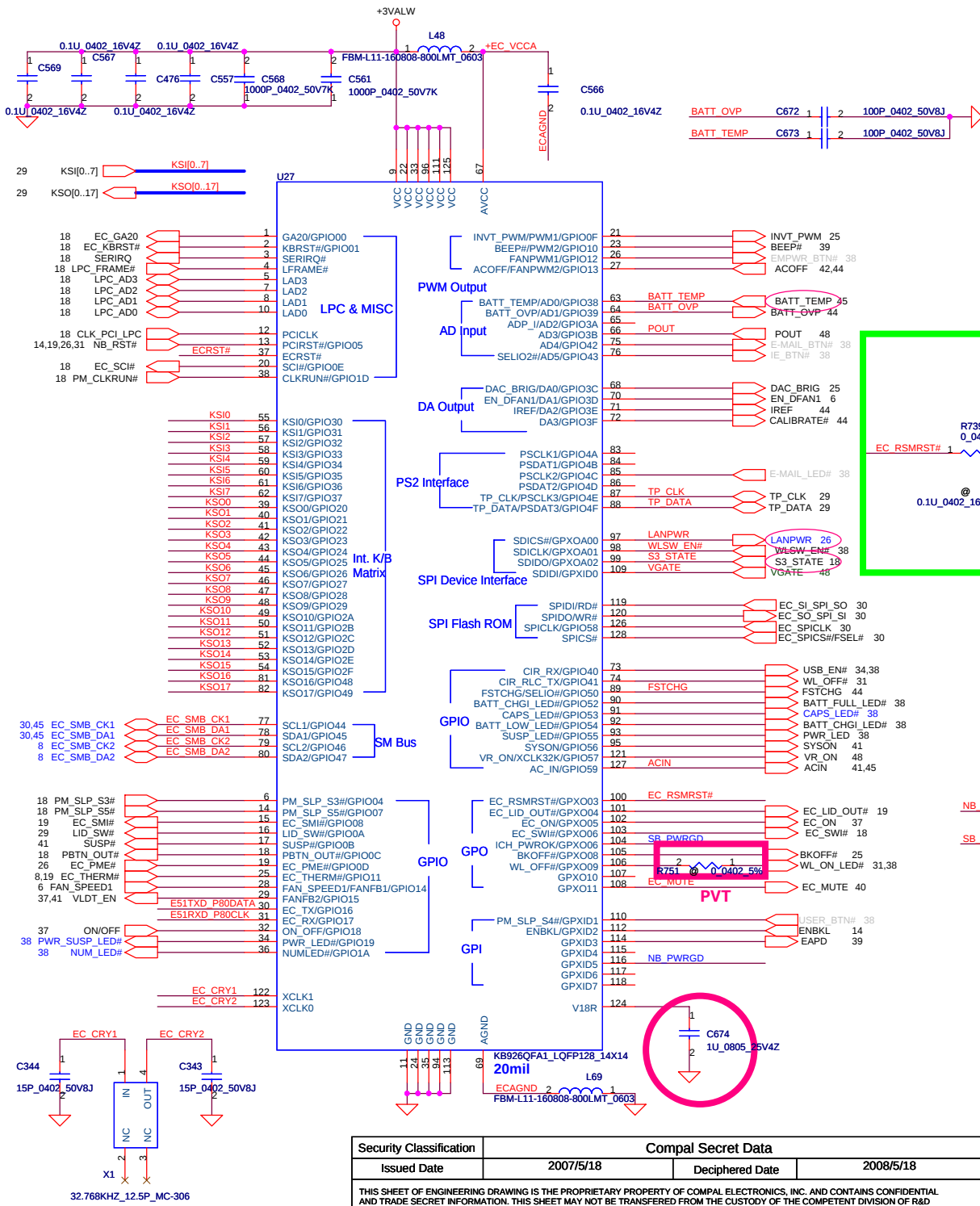
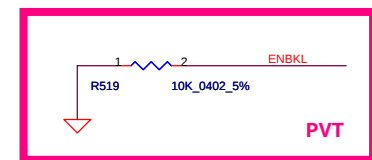
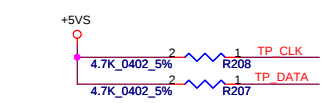
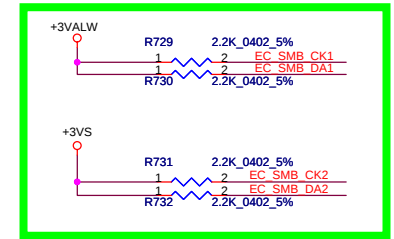
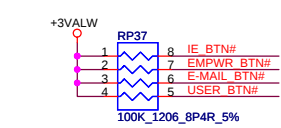
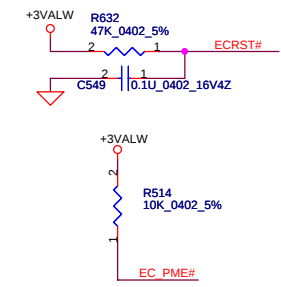
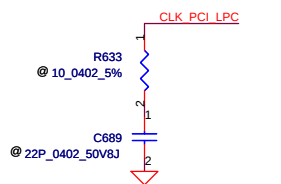


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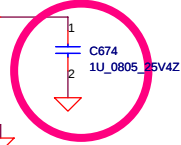
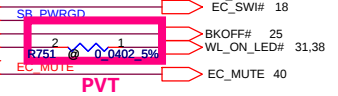
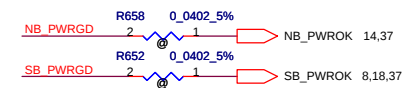
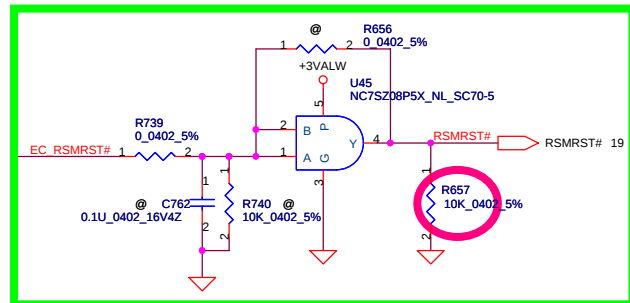
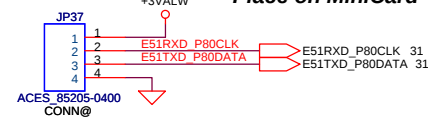


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					Date:	Tuesday, June 17, 2008			Sheet



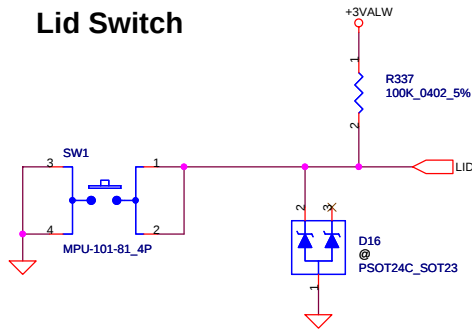
For EC Tools

Place on MiniCard

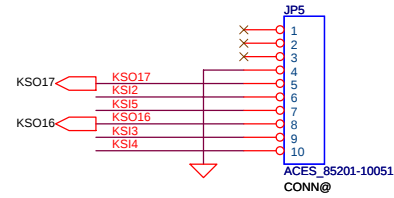


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				Date:	Friday, August 08, 2008
				Sheet	28 of 50

Lid Switch

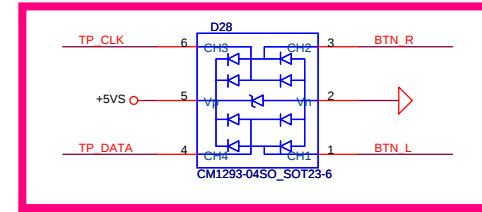


W/O media board (LS2921P)

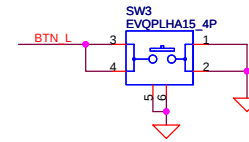


	KSO16	KSO17
KSI2	PLAY	VOL_UP
KSI3	STOP	VOL_DOWN
KSI4	NEXT	ARCADE_TV
KSI5	REV	

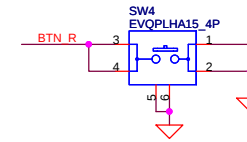
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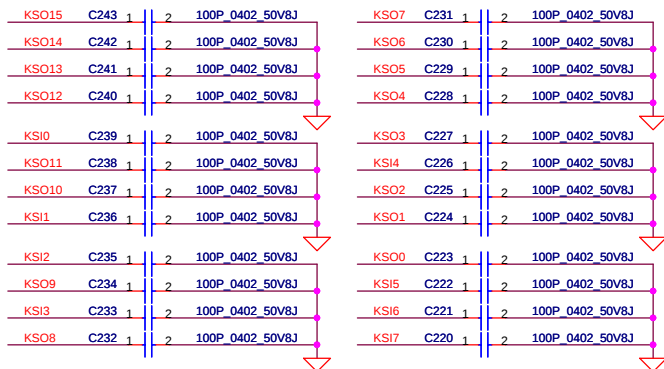
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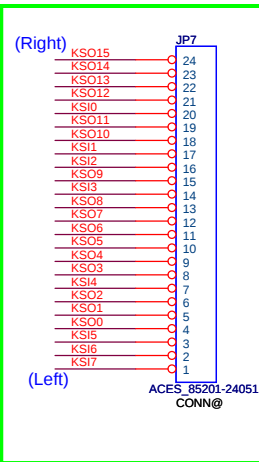
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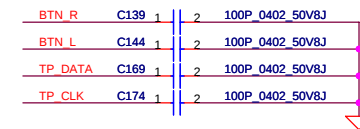
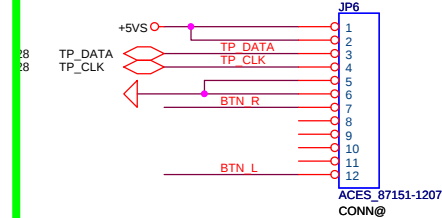
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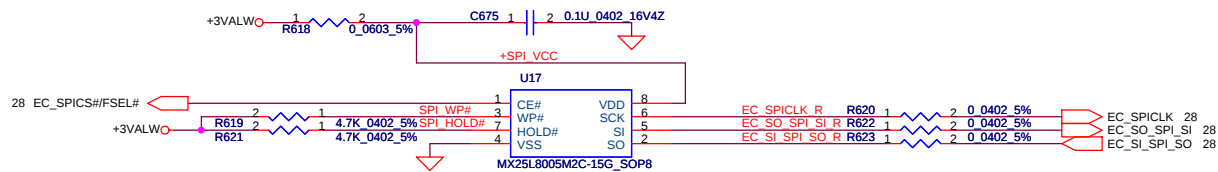
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KSO[0..15] KSO[0..15] 28



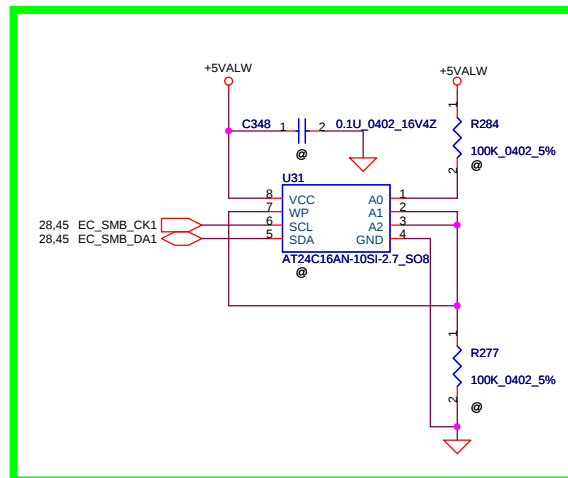
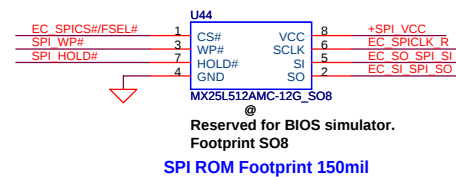
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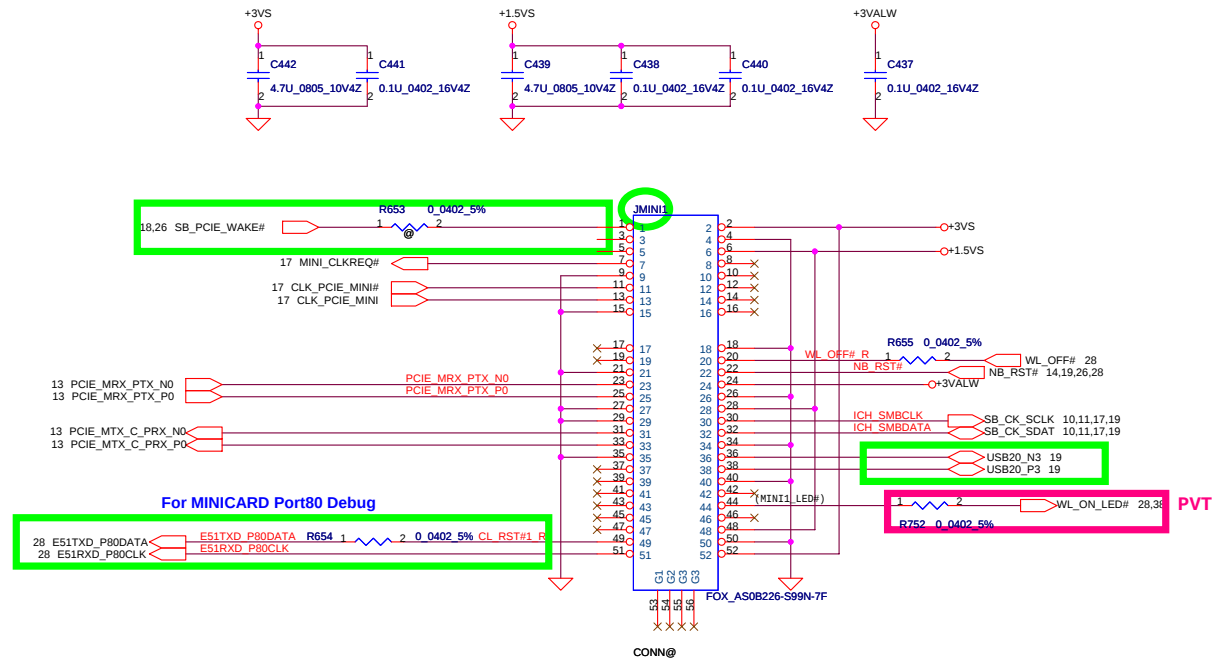
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SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

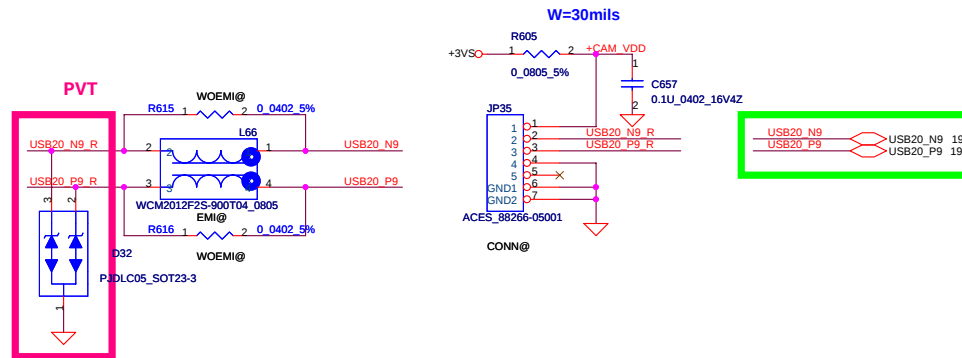


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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

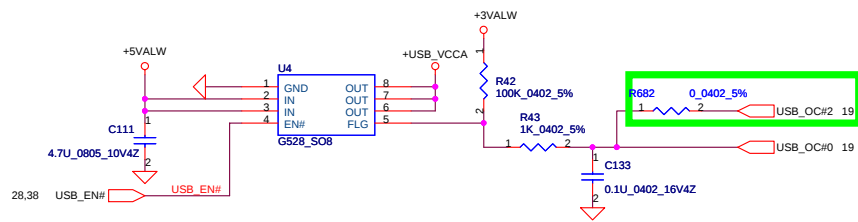
Camera



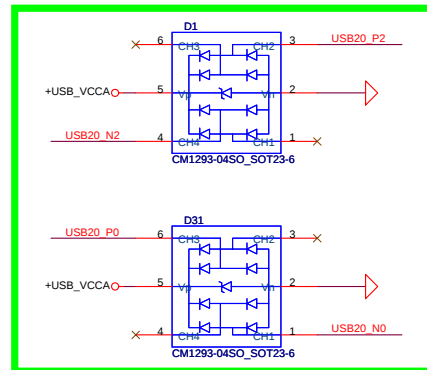
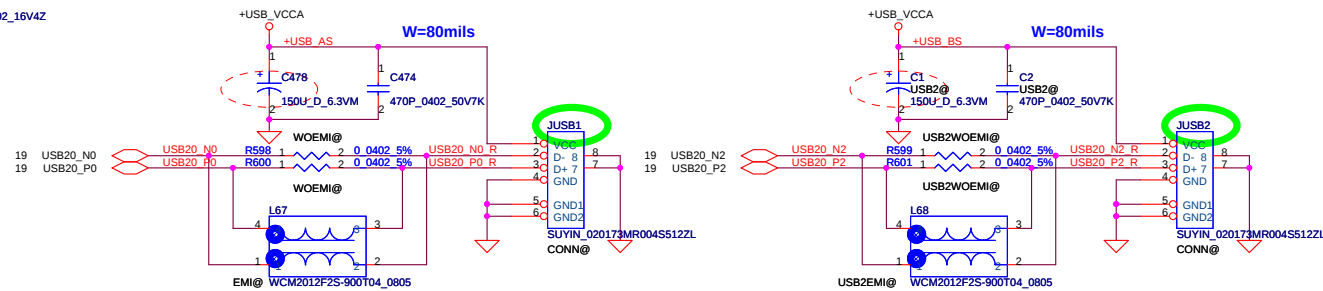
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				Size B Document Number KAW60 LA-4661P Rev 2.0
Date: Friday, August 06, 2008				Sheet 31 of 50

A		B		C		D		E	
1									
2									
3									
4									

A		B		C		D		E	
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2									
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4									



USB CONN. 1 & 2

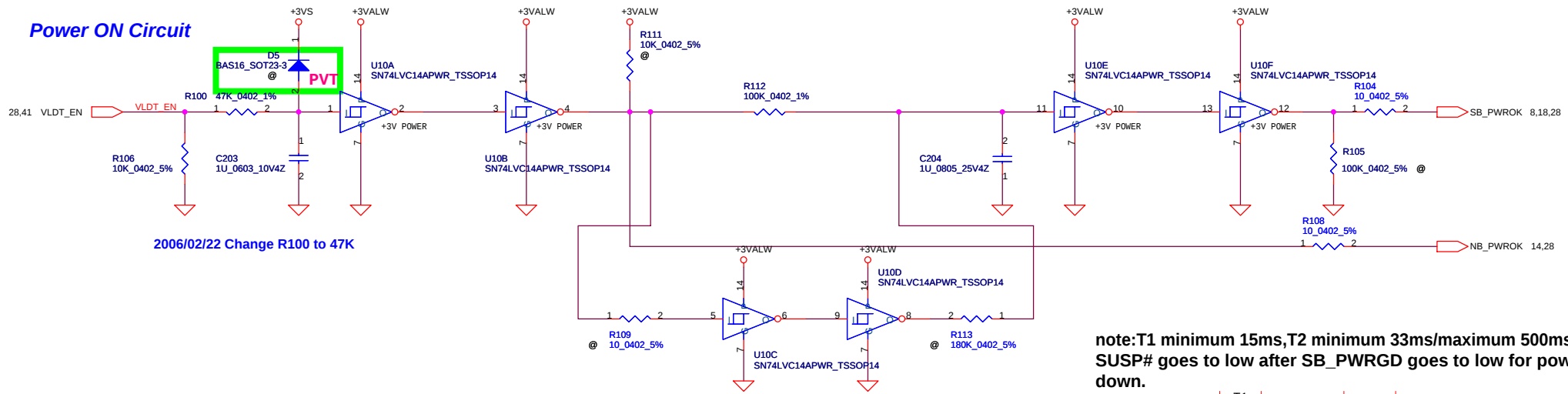


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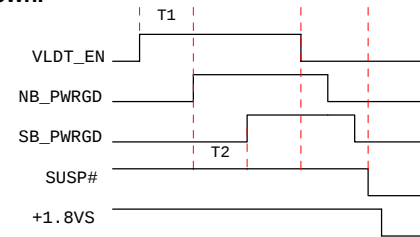
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				Date:	Tuesday, June 17, 2008	Sheet 36 of 50

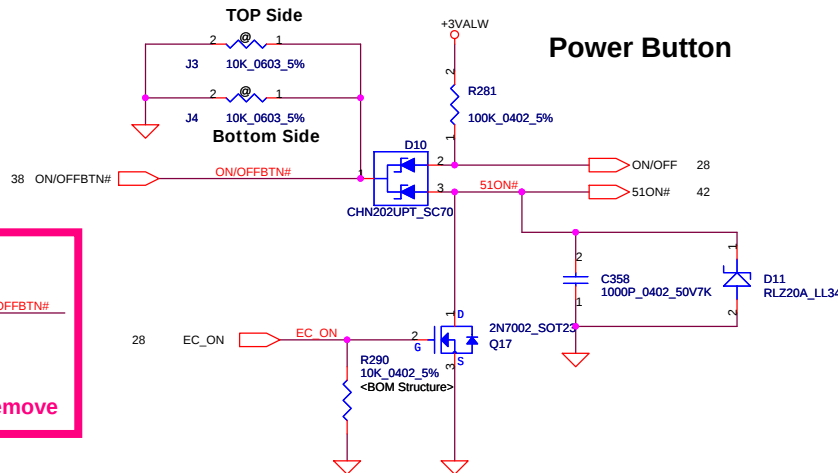
Power ON Circuit



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power down.

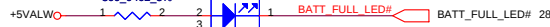
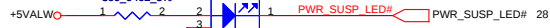
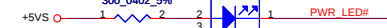


Power Button

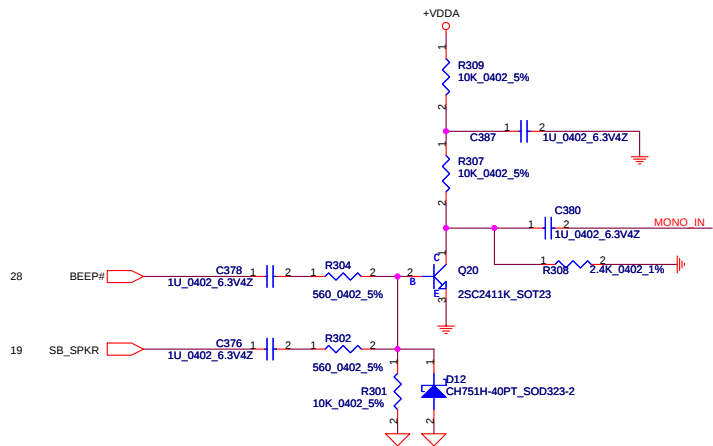


MP remove

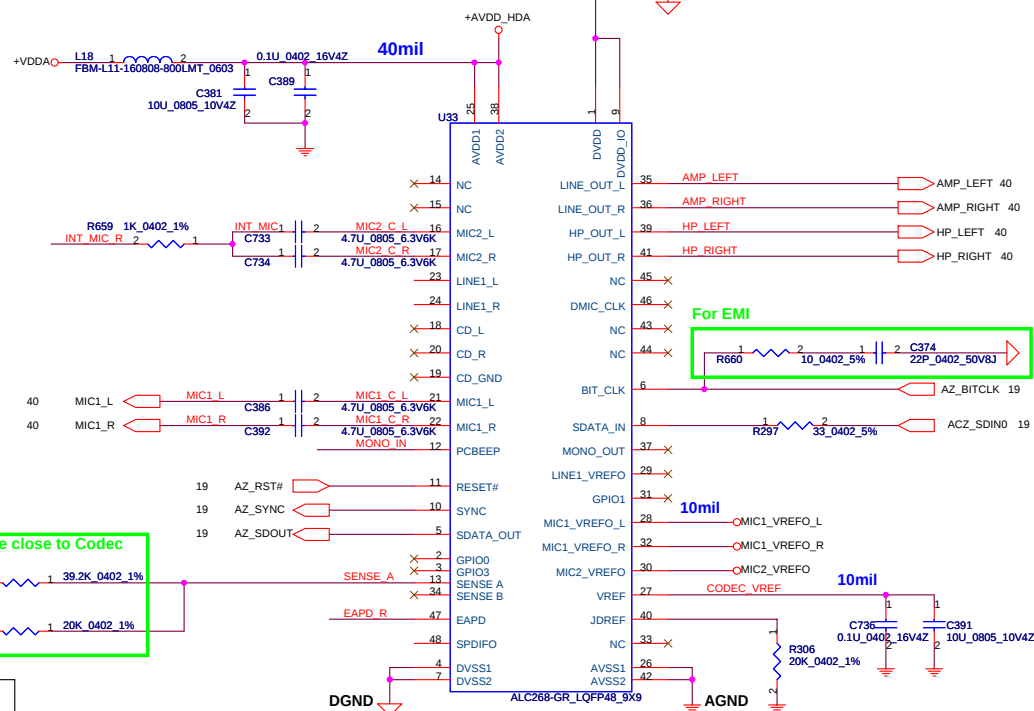
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				Size	Rev
				Document Number KAW60 LA-4661P	
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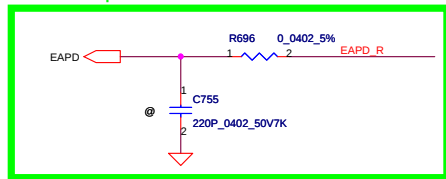


HD Audio Codec



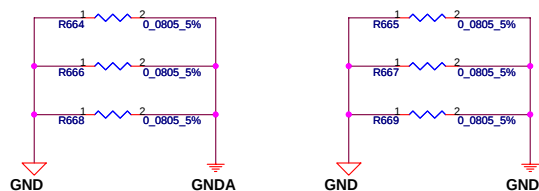
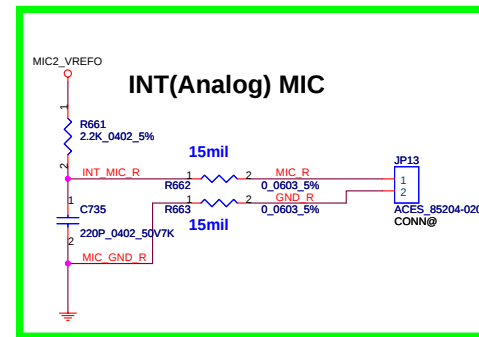
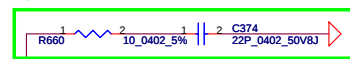
Place close to Codec

For EMI request

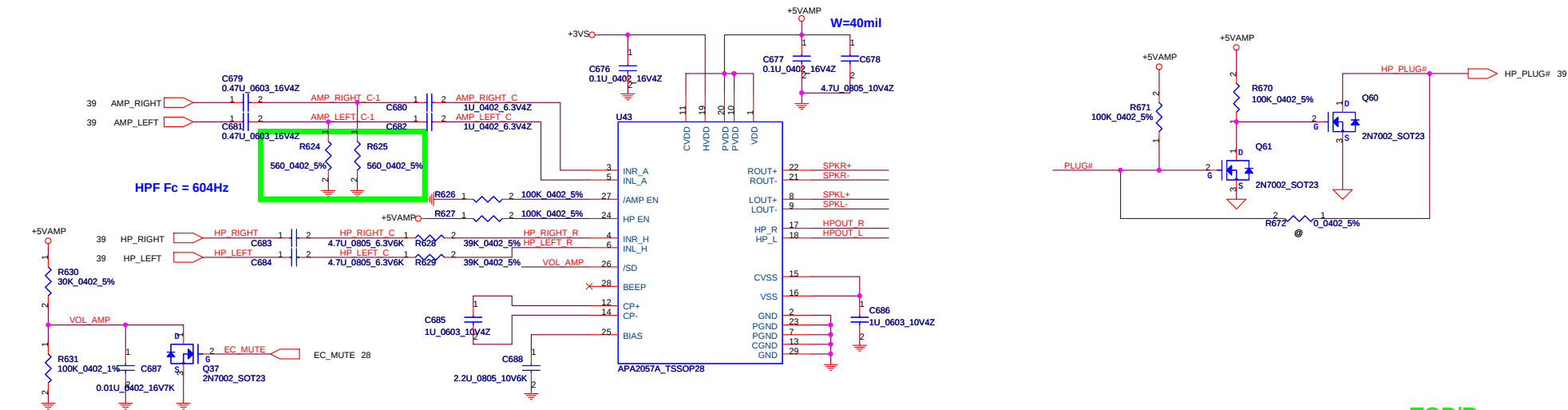


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

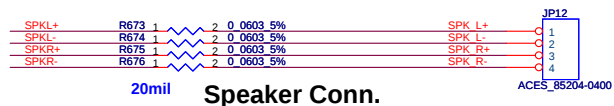
For EMI



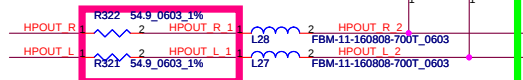
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	HDA Codec ALC268	
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				8	KAW60 LA-4661P
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Gain= 14dB

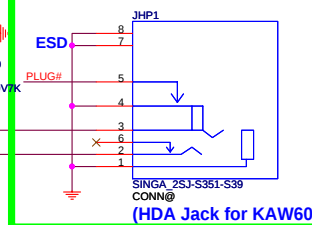


FSOV_Change 75 to 54.9 ohm



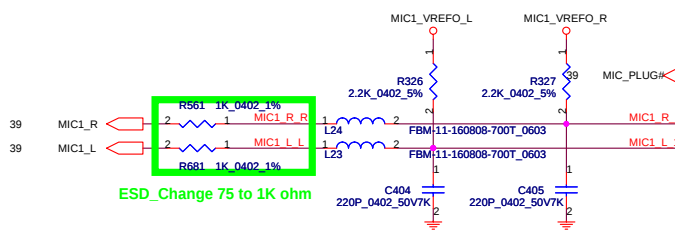
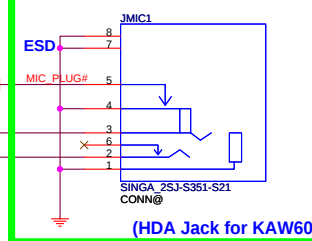
TOP/R

LINE Out / HP Out JACK



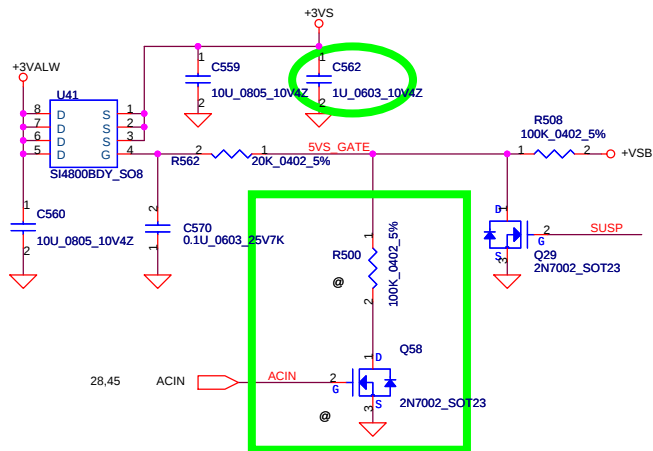
TOP/L

MIC JACK

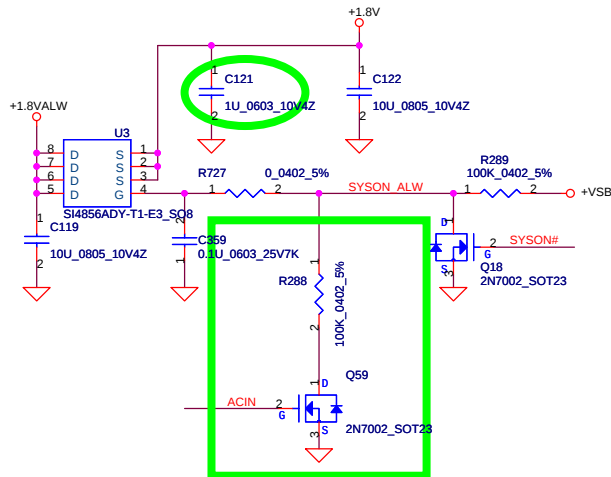


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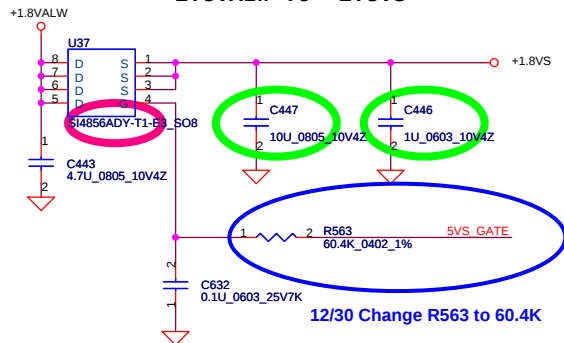
+3VALW TO +3VS



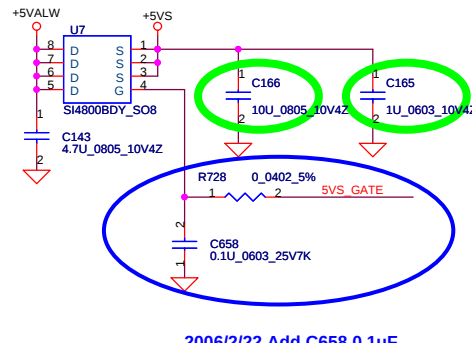
+1.8VALW TO +1.8V



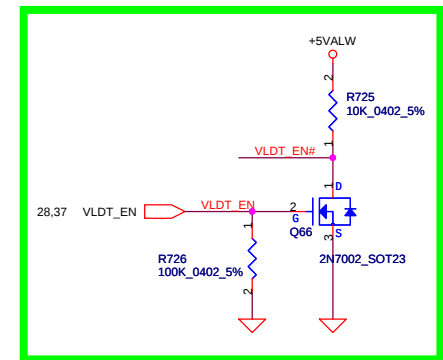
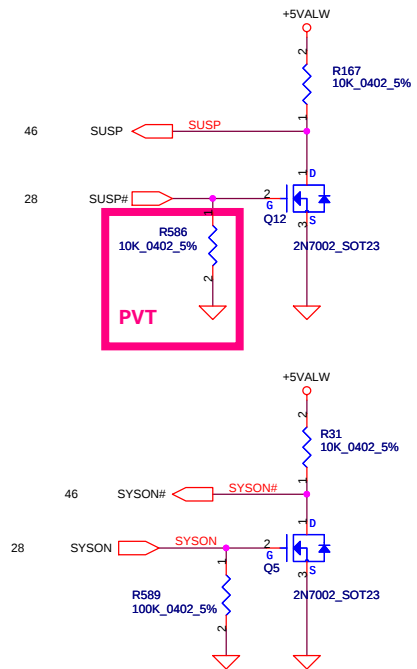
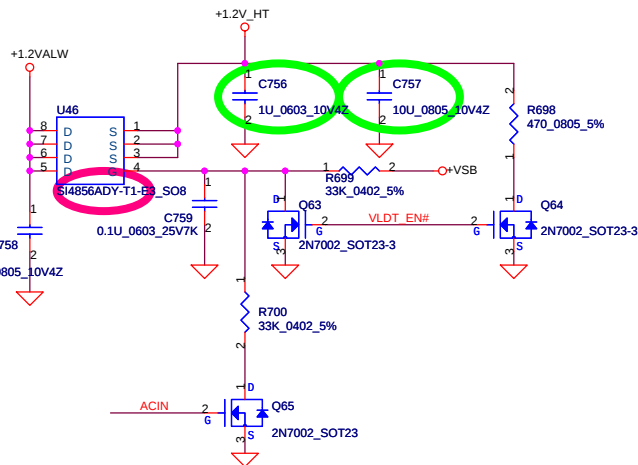
+1.8VALW TO +1.8VS



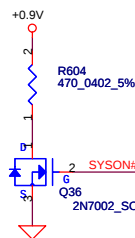
+5VALW TO +5VS



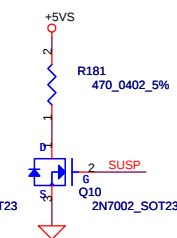
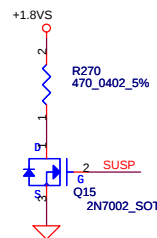
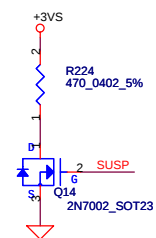
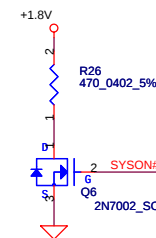
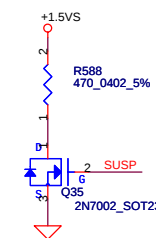
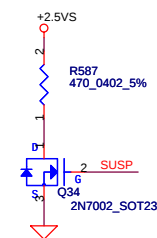
+1.2VALW TO +1.2V_HT



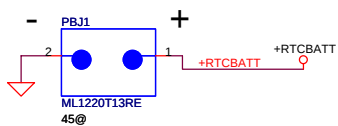
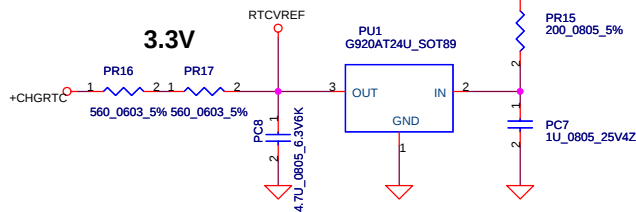
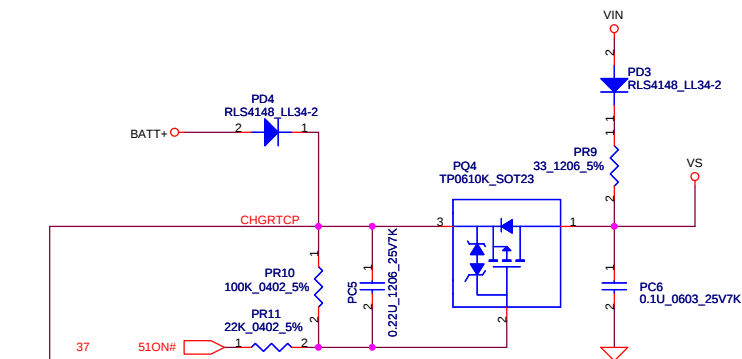
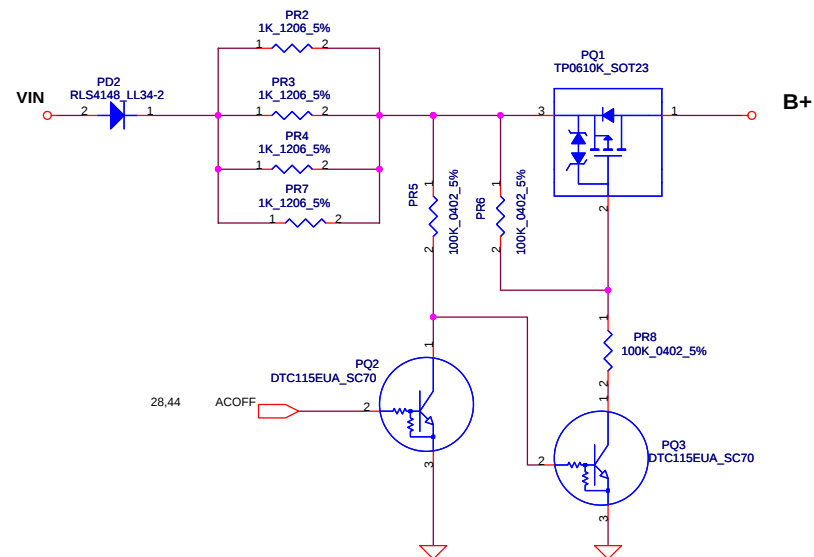
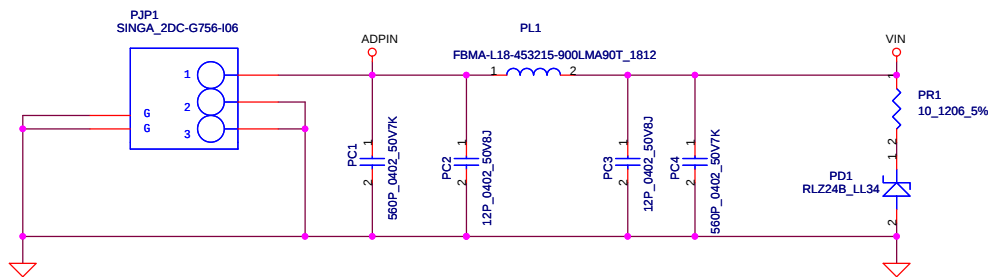
Near PU8



Near PU12



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Issued Date	2005/03/08	Deciphered Date	2006/03/08	Size	DC INTERFACE
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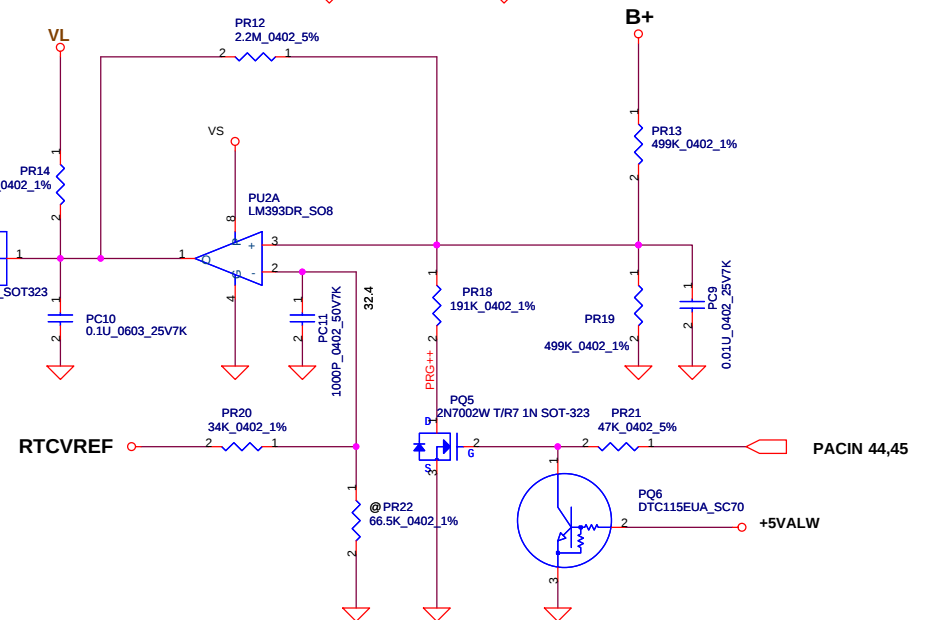


ACIN

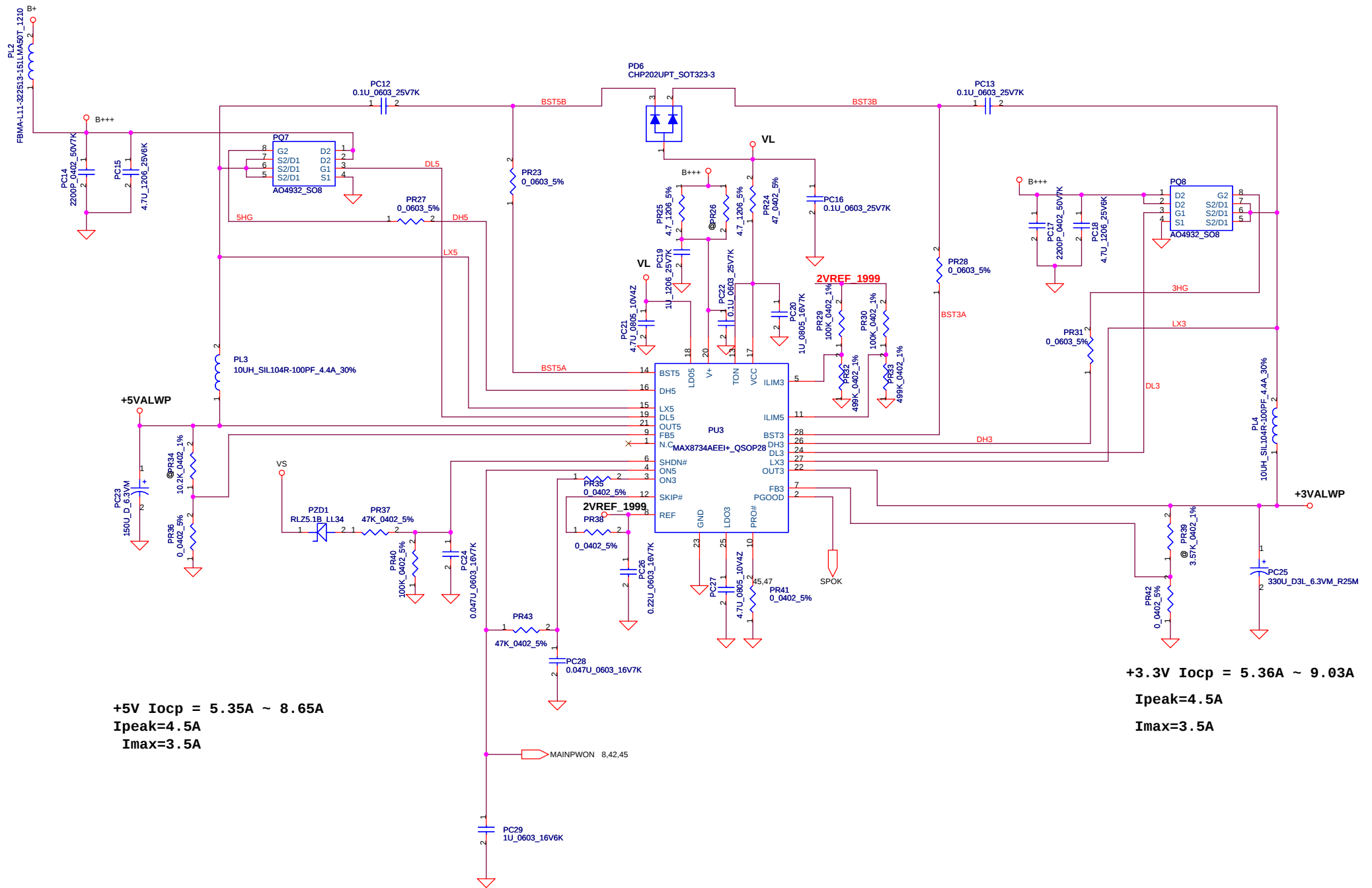
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



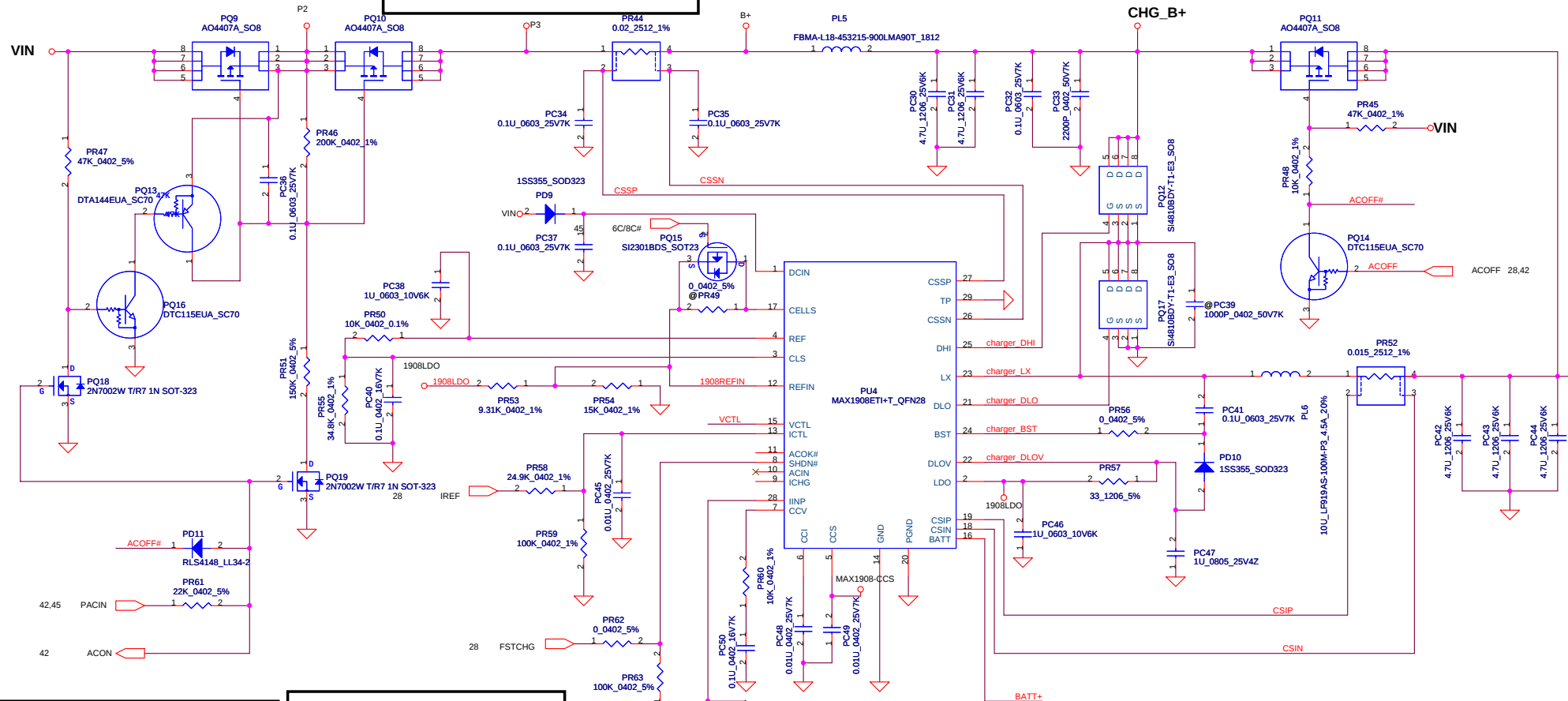
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Issued Date	2008/06/11	Deciphered Date	2009/06/11	Title	DCIN/DECTOR
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										+5VALWP/+3VALWP	
										KAW60	
										Rev 0.1	
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										Sheet 43 of 50	

I_{adp}=0~2.912A(65W)

CP Point:
85% CP Point, $3.42A \times 0.85 = 2.907A \sim 2.912A$
Iinput = $(34.8K / 44.8K) \times (75 / 20) = 2.912A$



Charger ADJ	Calibrate#	PR170	PR173
4.0V	L	@	@
4.1V	L	665K	221K
4.2V	H	@	@

$$\begin{aligned} V_{refin} &= V_{1908LD0} * (15K / (9.31K + 15K)) \\ &= 5.4V * (15K / (9.31K + 15K)) = 3.331V \\ V_{vctl} &= 3.331 * (221K / (221K + 665K)) = 0.83087V \\ V_{batt} &= CELLS * (4 + (0.4 * (V_{vctl} / V_{refin}))) \\ &= 3 * (4 + (0.4 * (0.83087 / 3.331))) = 12.29v \end{aligned}$$

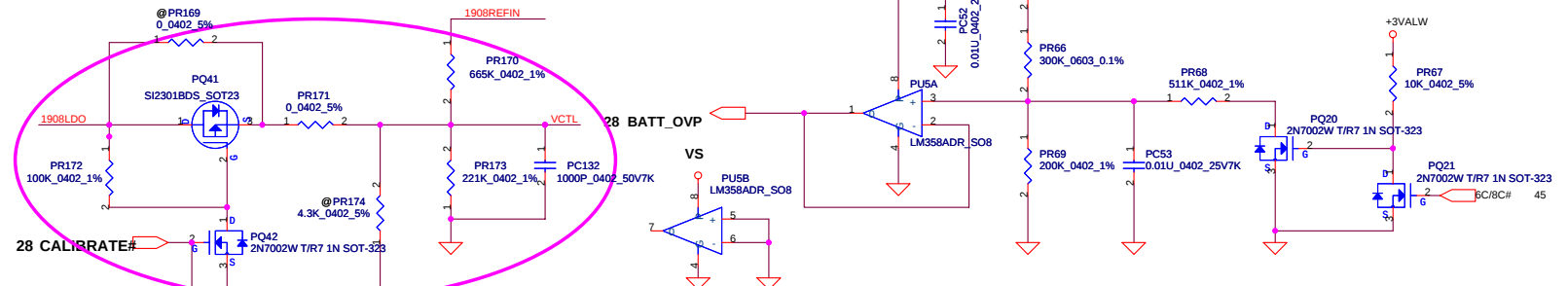
IREF=0.832*Icharge
IREF=0.73~3.3V

2P3S:4400mAH
0.8C=3.52A

```
OVP-Voltage:
LI-3SBattery Pack=13.5V---BATT-OVP=2.0061V
Battery-OVP=0.1486*BATT+
```

$$V_{batt} = CELLS * (4V + (0.4 * (V_{vctl} / V_{refin})))$$

Charge voltage
3S CC-CV MODE : 12.6V



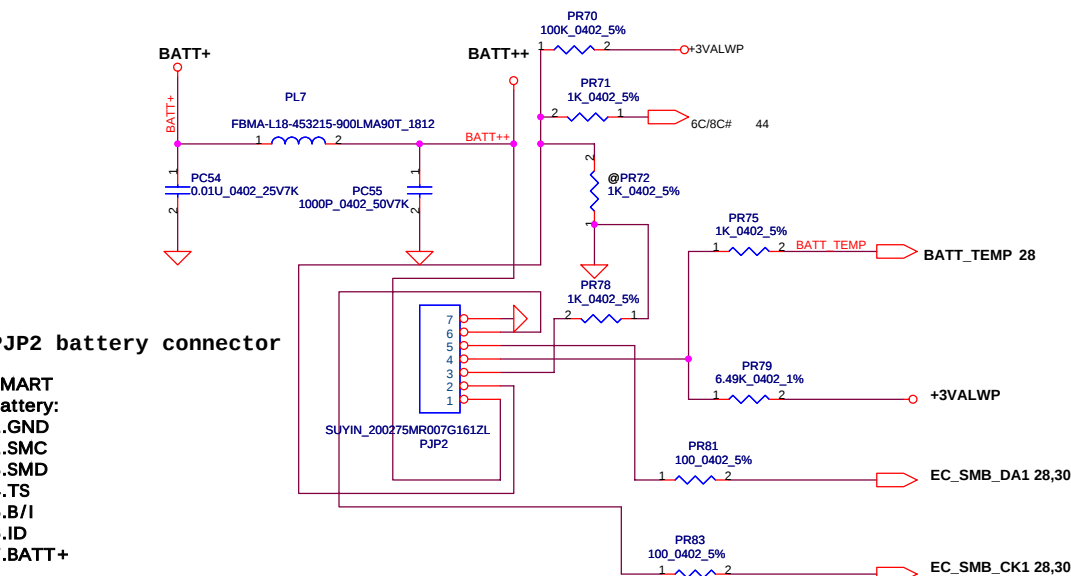
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Issued Date	2008/06/11	Deciphered Date	2009/06/11	Charger			
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				Size	Document Number	Rev	
				Date:	Friday, August 08, 2008	Sheet	44 of 50

PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C

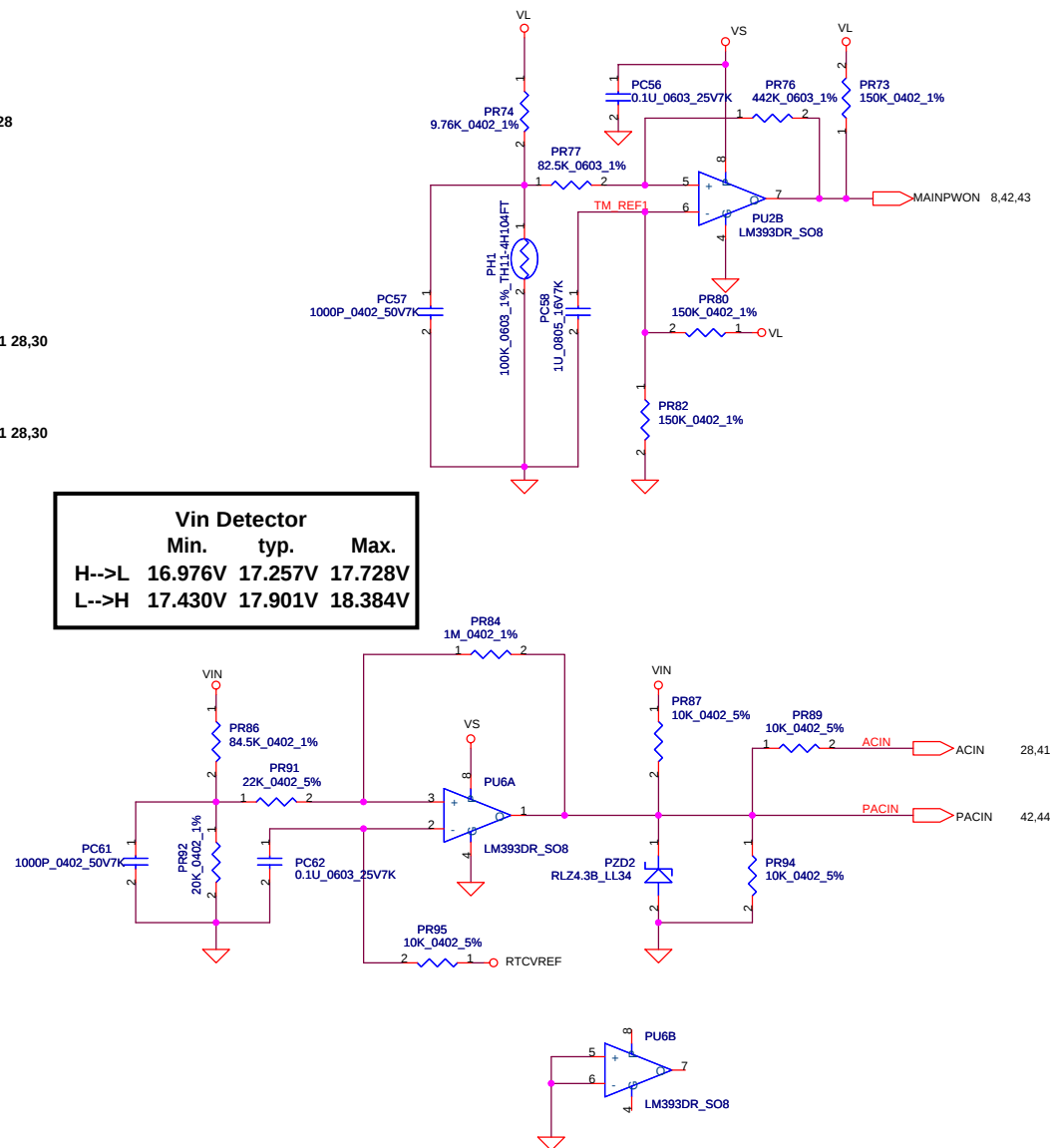
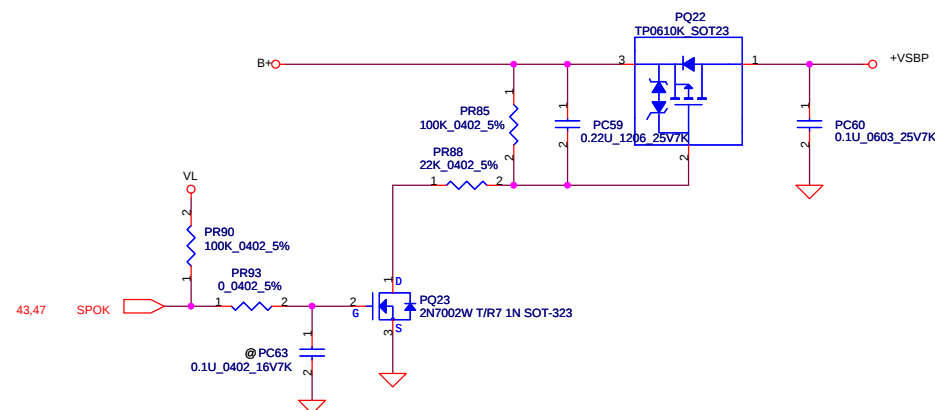
PJP2 battery connector

SMART
Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+

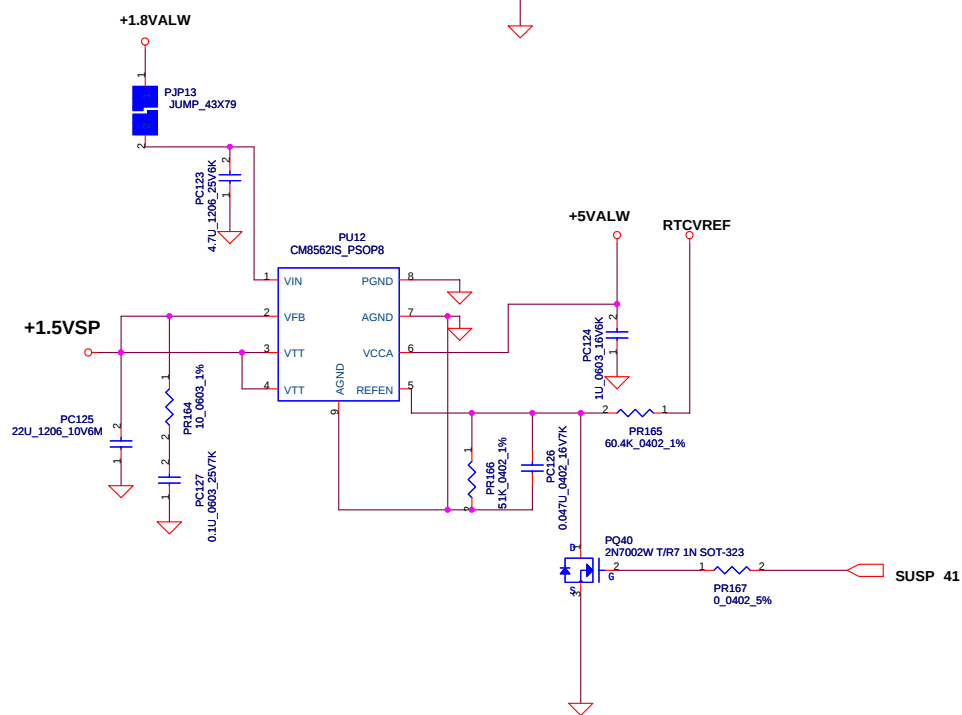
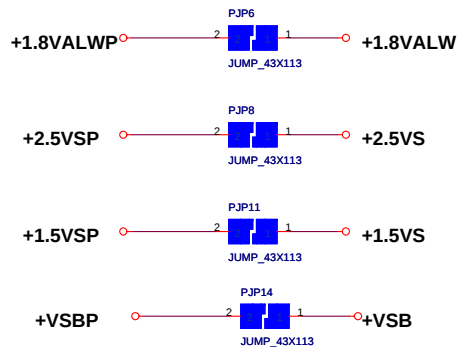
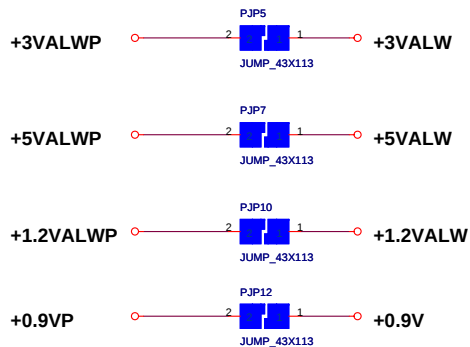
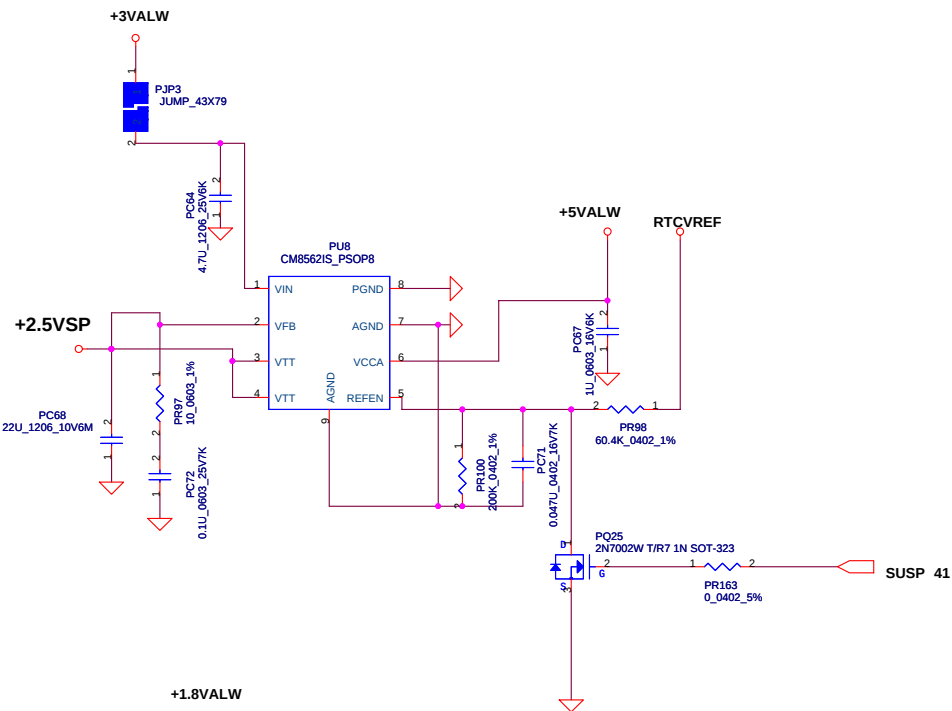
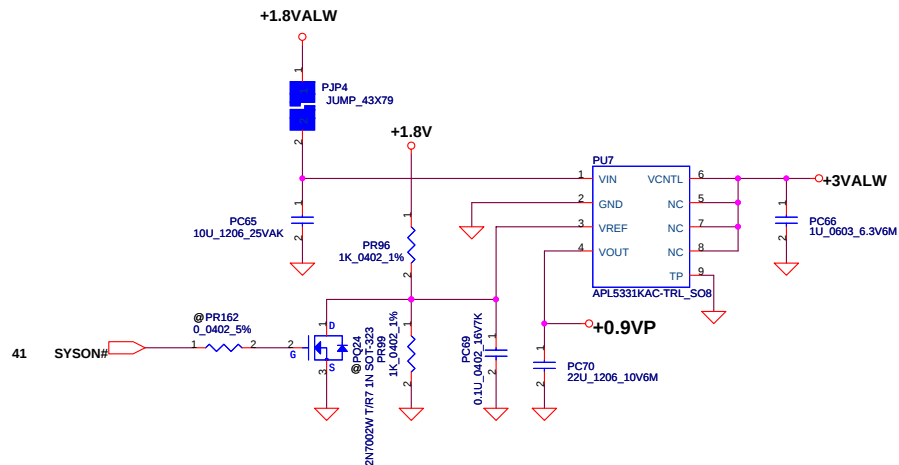
KAW60 is used JAL90 battery connector footprint, but pin definition is reverse compare with KAW60 original battery connector, so schematic must be change to satisfy with JAL90 connector.



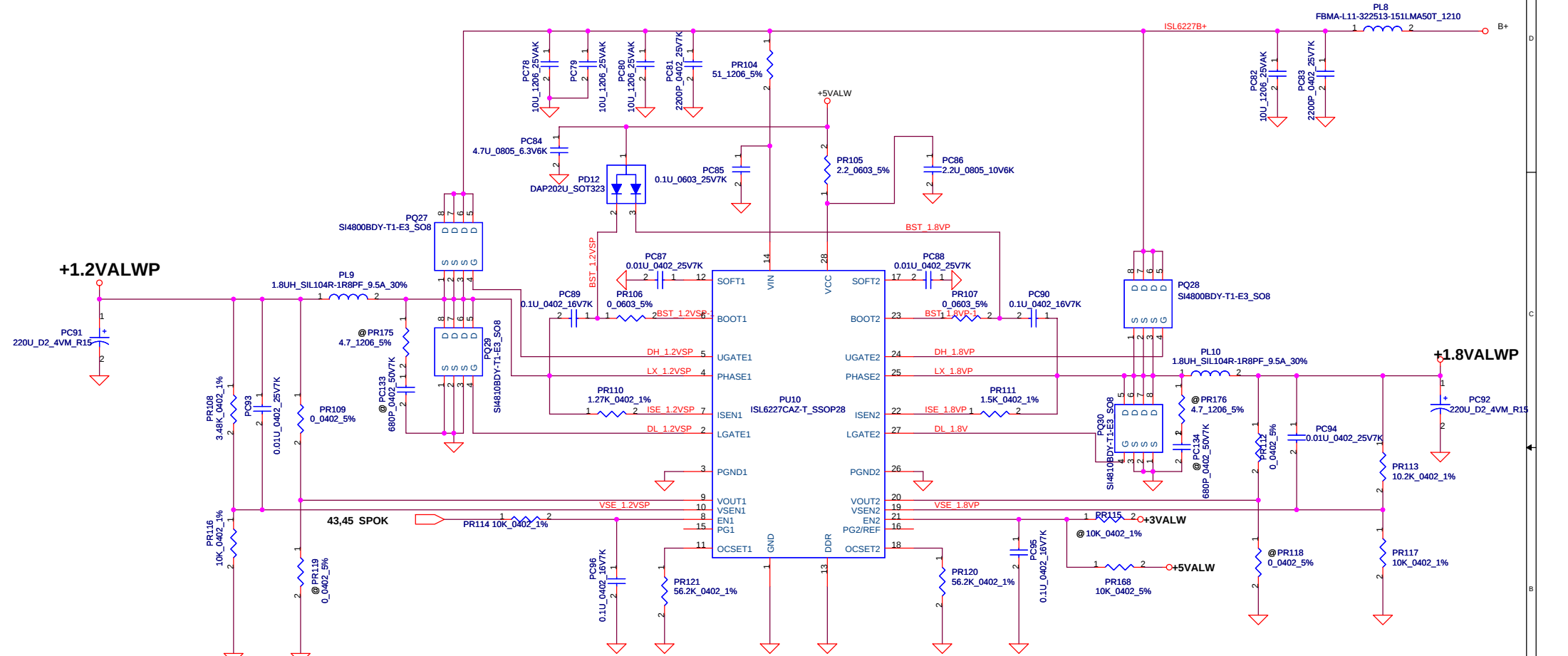
Vin Detector
Min. typ. Max.
H-->L 16.976V 17.257V 17.728V
L-->H 17.430V 17.901V 18.384V



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										BATTERY CONN. / OTP	
										KAW60	
										Rev 0.1	
										Date: Friday, August 08, 2008	
										Sheet 45 of 50	



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				Custom	KAW60
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				Sheet	46 of 50
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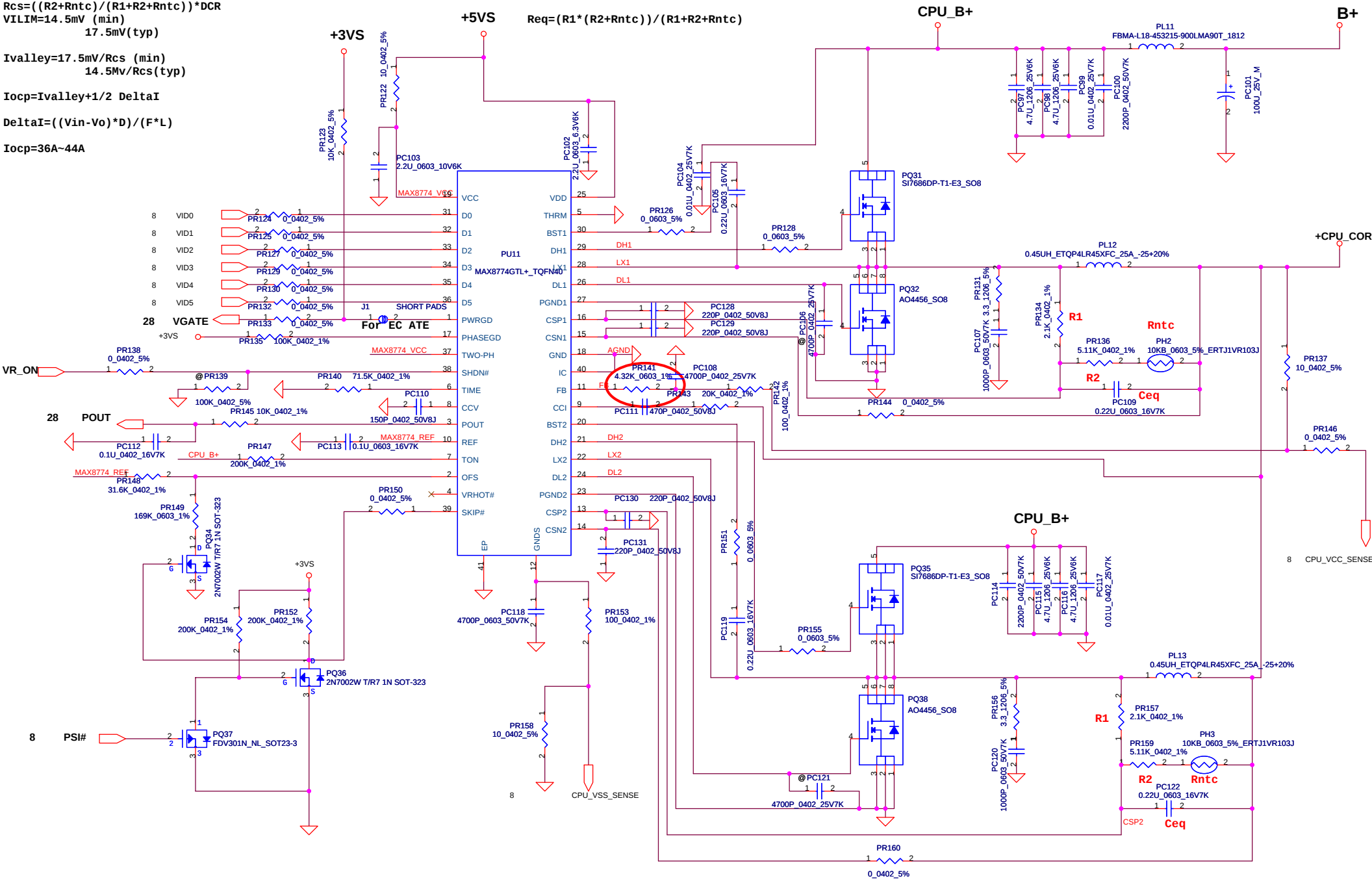
Ipeak=6.47A, Imax=6.47*0.7=4.53A
Iocpmin=7.79A
Iocpmax=11.83A

Ipeak=8.5A, Imax=6A
Iocpmin=8.76A
Iocpmax=13.46A

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OCP Setting:
 $Rcs=((R2+Rntc)/(R1+R2+Rntc))*DCR$
 $VILIM=14.5mV \text{ (min)}$
 $17.5mV \text{ (typ)}$
 $Ivalley=17.5mV/Rcs \text{ (min)}$
 $14.5mV/Rcs \text{ (typ)}$
 $Iocp=Ivalley+1/2 \Delta I$
 $\Delta I=((Vin-Vo)*D)/(F*L)$
 $Iocp=36A-44A$

$Rcs*Ce q=L/Req \text{ must be satisfy!}$
 $Req=(R1*(R2+Rntc))/(R1+R2+Rntc)$



<BOM Structure>

Security Classification		Compal Secret Data			
Issued Date		2008/06/11	Deciphered Date	2009/06/11	Title
					+CPU_CORE
					Size
					Custom
					Document Number
					KAW60
					Rev
					0.1
					Date
					Friday, August 08, 2008
					Sheet
					48 of 50

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	material issue.	Change to currently design	0.1	44	Change PQ9, PQ10, PQ11 from SB944070000(S TR A04407 1P S08 W/D) to SB00000DL00(S TR S TR A04407A 1P S08)	08,07/22	to PVT
2	material issue.	Change to currently design	0.1	48	Change PQ31 and PQ35 from SB578400080(S TR SI7840-T1 -E3 1N S08) to SB000008L80(S TR SI7686DP-T1-E3 1N POWERPAK S08)	08,07/22	to PVT
3	material issue.	A04916 will be EOL, change to A04932	0.1	43	Change PQ7 and PQ8 from SB000002W80(S TR A04916 2N S08) to SB00000BG00(S TR A04932 2N S08)	08,07/22	to PVT
4	BOM error	BOM error	0.1	48	Change PR141 from SD014200180(S RES 1/10W 2K 0603 1%) to SD014432180(S RES 1/10W 4.32K 0603 1%)	08,07/22	to PVT
5	material issue.	SI4810 will be EOL, change to SI4894.	0.1	47	Change PQ12, PQ17, PQ29, PQ30 from SB548100020(S TR SI4810BDY-T1-E3 1N S08) to SB00000D300(S TR SI4894BDY-T1-E3 1N S08)	08,07/22	to PVT
6	Add VGATE pull high resistor.	Add VGATE pull high resistor.	0.1	48	Add PR123 SD028100280(S RES 1/16W 10K 0402 5%)	08,07/22	to PVT
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

PHASE	PAGE	MODIFICATION LIST	PURPOSE
PVT/MP	P.19 & 24	Update CRT_DET & CRT_DET# net name	NA
	P.18 & 19	Change CRT_DET from GPIO61 to GPIO00 & reserved R741 , R742 , R743	For ACER AP test CRT detect feature
	P.20	Remove L71 , C694 & C697	For +3Vs (1.5V) , +5Vs (0.388V) , +1.8Vs (0.154V) on S5 leakage issue
	P.28	Change R519 from 100K to 10K	For RS690MC ENBKL had unexpected 3.3V pulse before normal display & white screen flash symptom appear
	P.14	Reserved U48 , U49 , R744 , R745 , R746 , R747 , C763	For RS690MC ENBKL , ENVDD if had unexpected 3.3V pulse before normal display
	P.28 & 31	Modify WL_ON_LED# from KB926 to JMINI1 control	WL LED activity behavior controlled by wireless mini card itself
	P.38	Update SW9 Footprint & P/N	NA
	P.41	Change R586 from 100K to 10K	For Susp# had 3V level glitch when G3 to S5 (Plug AC in) & caused +5Vs /+3Vs had leakage immediately
	P.6	Change D4 as SC1BAS16000(S DIO BAS16PT S0T-23)	Sourcer recommend
	P.26	Change U11 as SA000019910(S IC EE 1K CAT93C46VI-GT3 S0IC 8P)	SA093461070 (S IC EE 1K S0-8 I AT93C46-10SI-2.7) EOL
	P.50	Change T1 as SP050001210 / S X'FORM_ NS0013LF LAN (BOTHHAND)	MHPC X'form part not for ABO , Sourcer recommend
	P.18	Delete R695,R179,R484 for SB_TEST pin	AMD reference schematic
	P.20	Reserved C764 (1u_0402)	AMD reference schematic & design guide
	P.38	Modify WL_LED power rail as +3Vs	NA
	P.28 & 38	Modify LED control of SATA drive from EC to SB (Add Q67)	EC(media_led#/pin86 , reference sata_led# from SB) control behavior abnormal
	P.17	Change C510 , C511 of 14.318MHz as 27P from 22P	NA
	P.37 & 25	Change D5 , D21 as SC1BAS16000	NA
	P.26	Add L77 , C765 , C766 , C767 & change R645 / R647 as L78 / L79 , reserved C719 , C724	EMI request
	P.31 & 34	Stuff L66 , L67 , L68 & remove R615 , R616 , R598 , R599 , R600 , R601	EMI request
	P.29	Stuff D28	ESD request
	P.6	Update net EN_DFAN1_R	NA
	P.6	Update JCPU1 PCB footprint as SOC127MM48X51-948	NA
	P.26	Add R749 , R750 (300ohm_0402)	For LAN external EEPROM program issue
	P.31	Add D32 (SCA00000A00)	ESD request
	P.28 & 31	Reserved R751 & R752	Reserved WL_LED controlled by EC (Navarrow project)
	P.24	Change C411 & C412 PN from SE081680k80 to SE071680J80	AP Code
	P.6	Change U1 as SA00001Z900 (S IC APL5605KI-TRL S0P 8P)	(SA009930010) S IC G993P1UF S0P 8P FAN LDO EOL
	P.15	Change C330 as 0402 package	NA

ZZZ



PCB 06B LA-4661P REV1 M/B

LA4661MB Rev0 : DA600009Z00
LA4661MB with Sub/B Rev1 : DAZ06B00100

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/08	Deciphered Date	2006/03/08	PIR-HW & Option Component	
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