

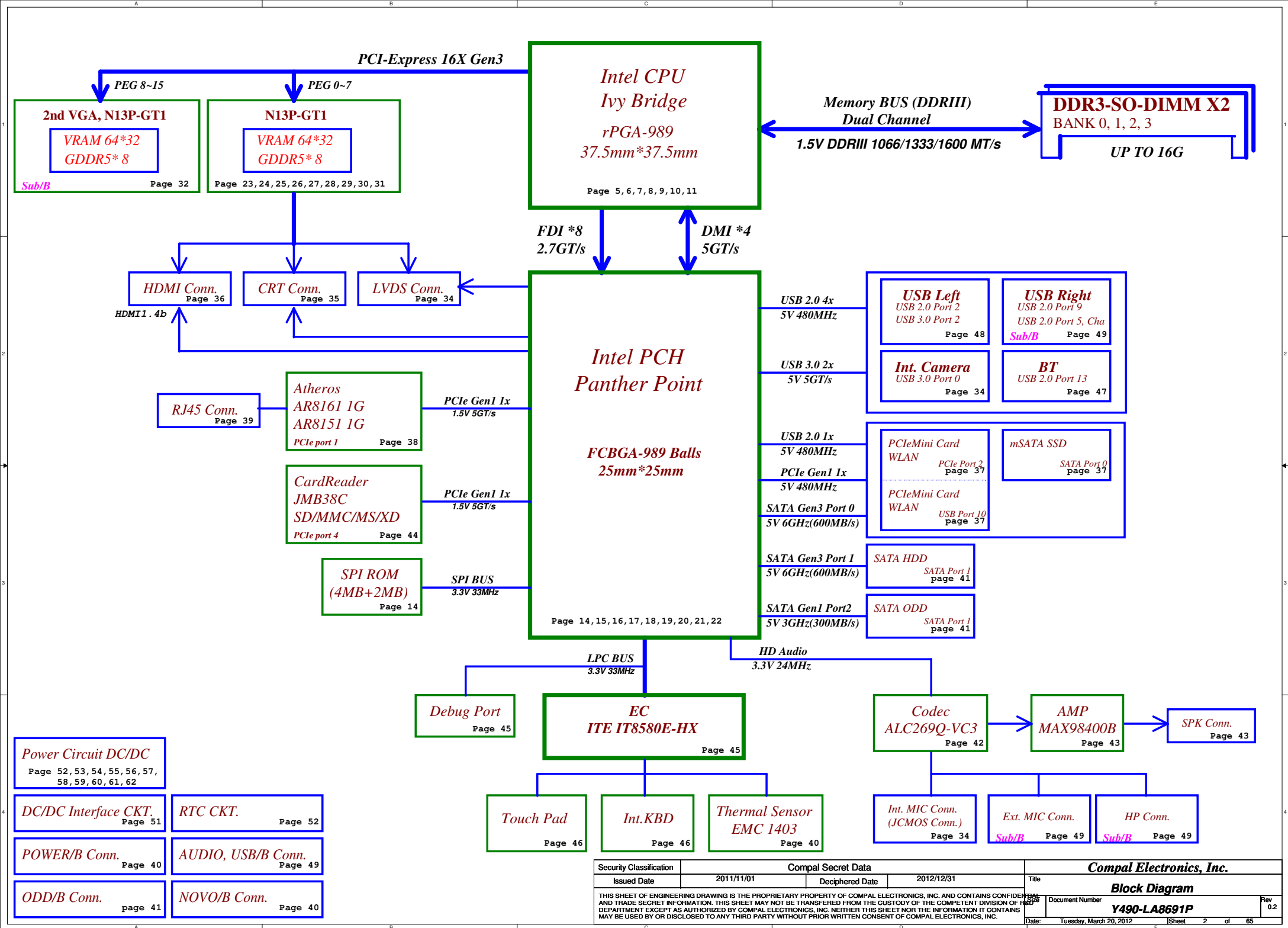
QIQY5

Whisky3.0 (Y490)

LA-8691P Rev0.2 Schematic

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13P GT1-A2 + 2nd VGA N13P GT1-A2
2012-02-05 Rev0.2

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
	XHCI 1	0	Camera
		1	
		2	USB Port (Left Side)
		3	
		4	
		5	USB Port (Right Side)
		6	
		7	
		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



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Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

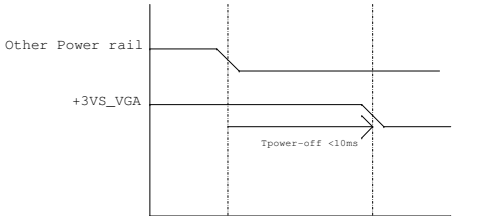
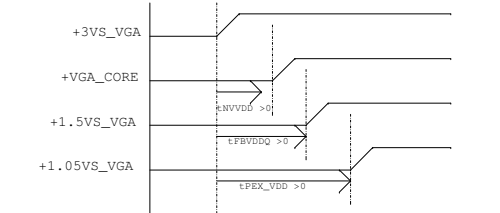
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Device ID		setting		I2C Slave addresses ID	
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E	
			1	0x9C	

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

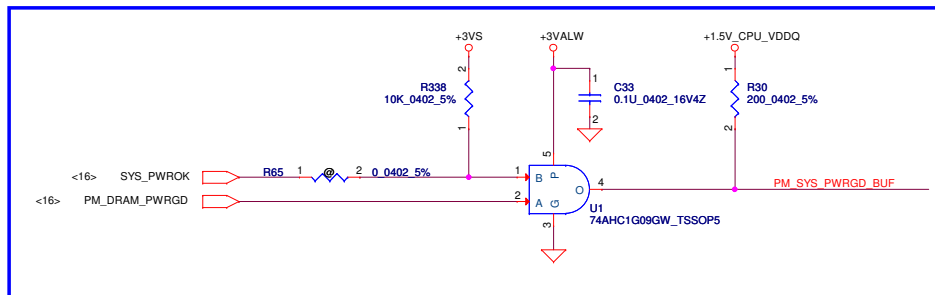
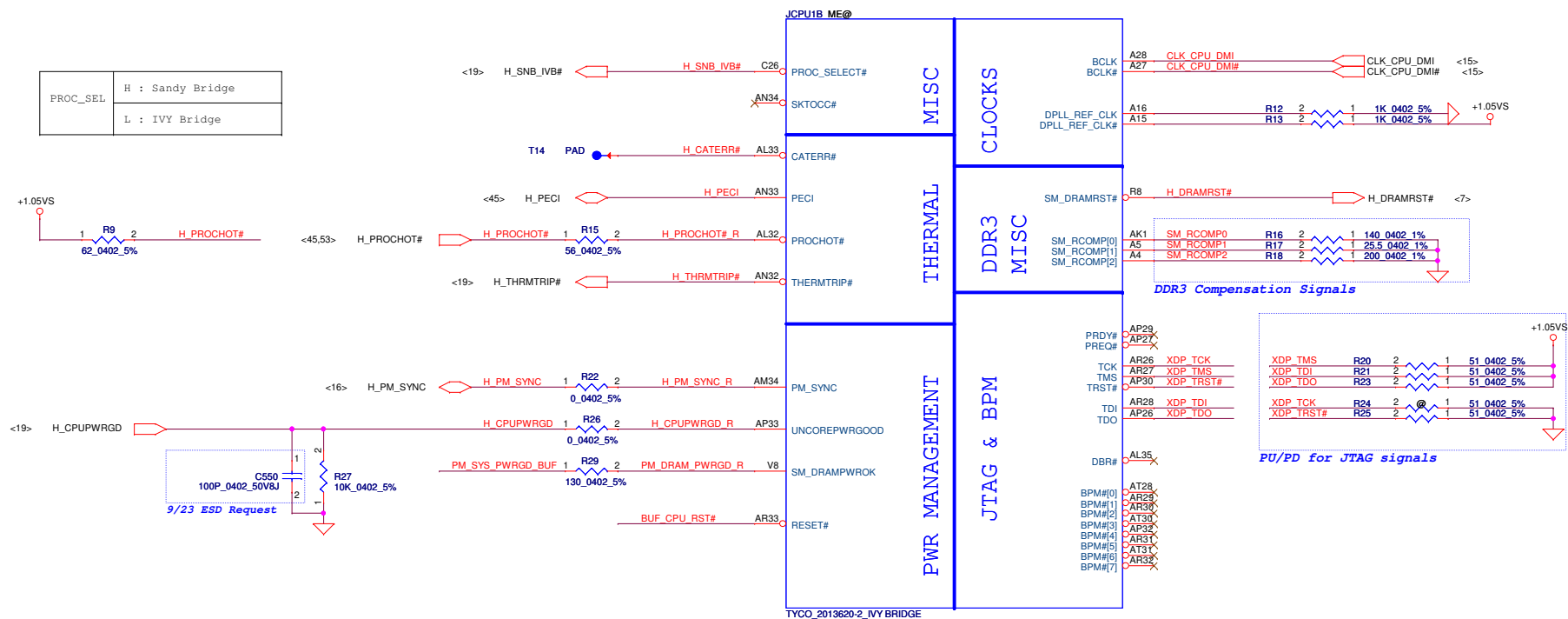
GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		



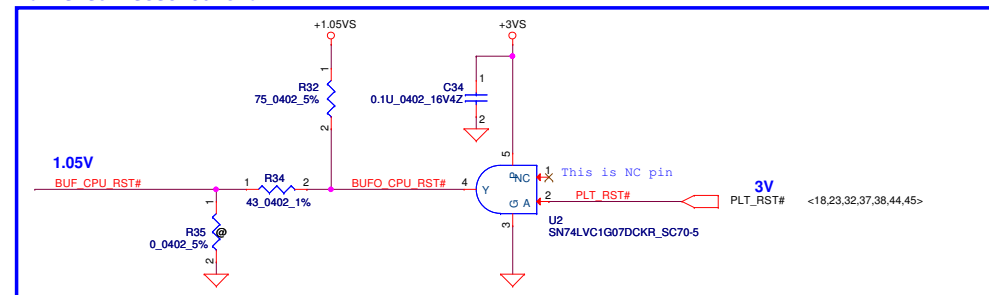
- 1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

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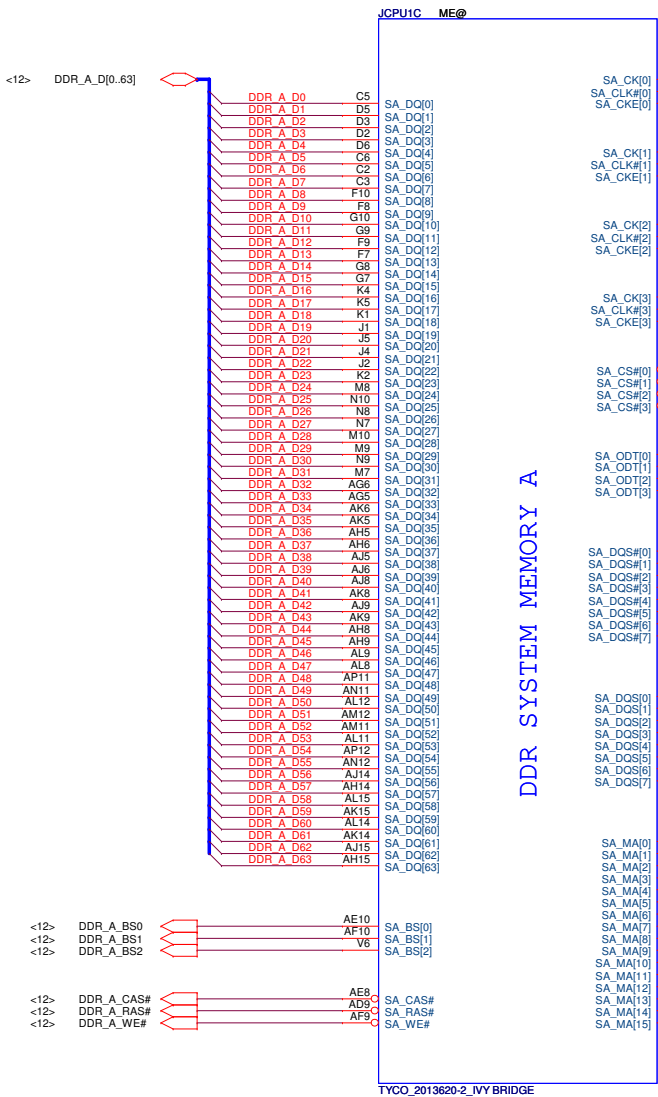
PROC_SEL	H : Sandy Bridge
	L : IVY Bridge



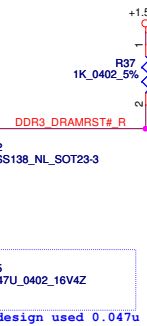
Buffered Reset to CPU



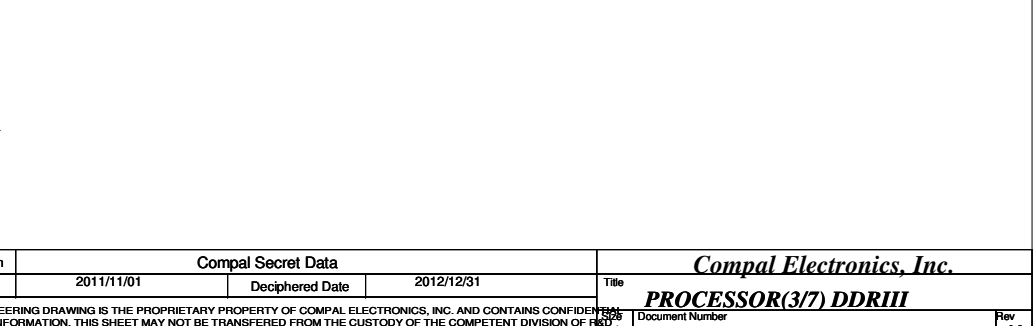
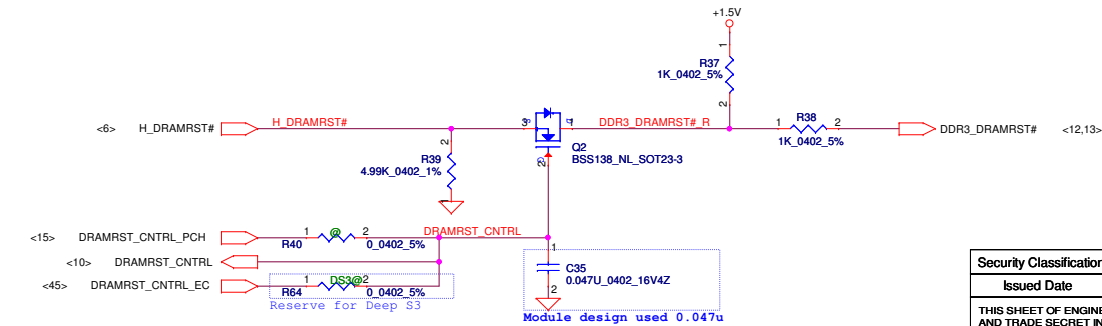
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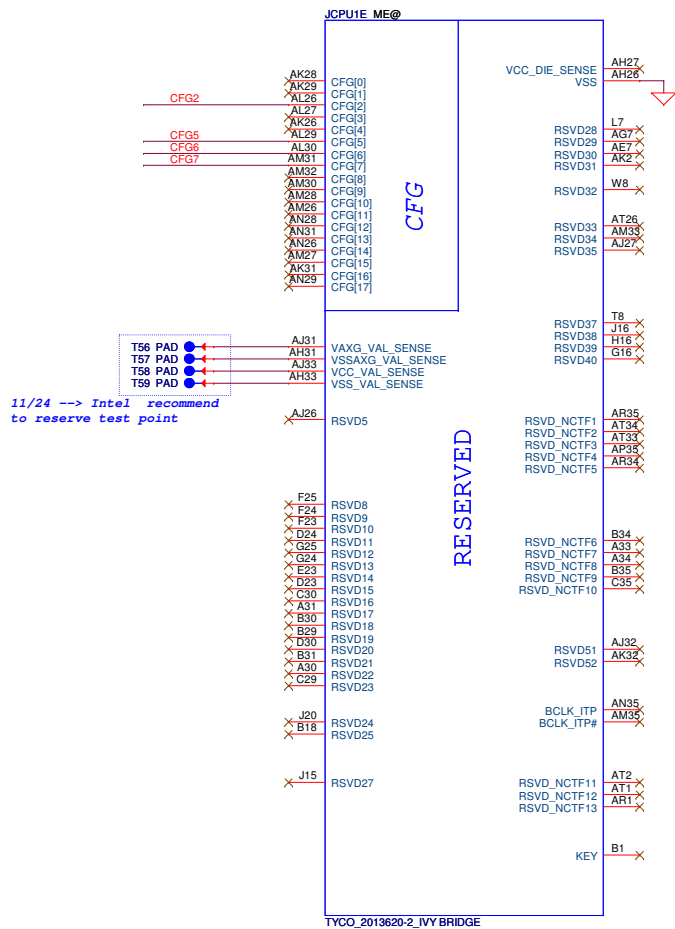
DDR SYSTEM MEMORY A



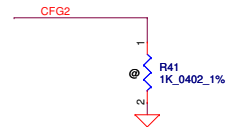
DDR SYSTEM MEMORY B



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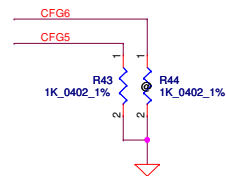


CFG Straps for Processor

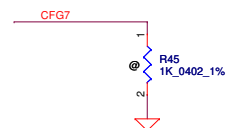


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

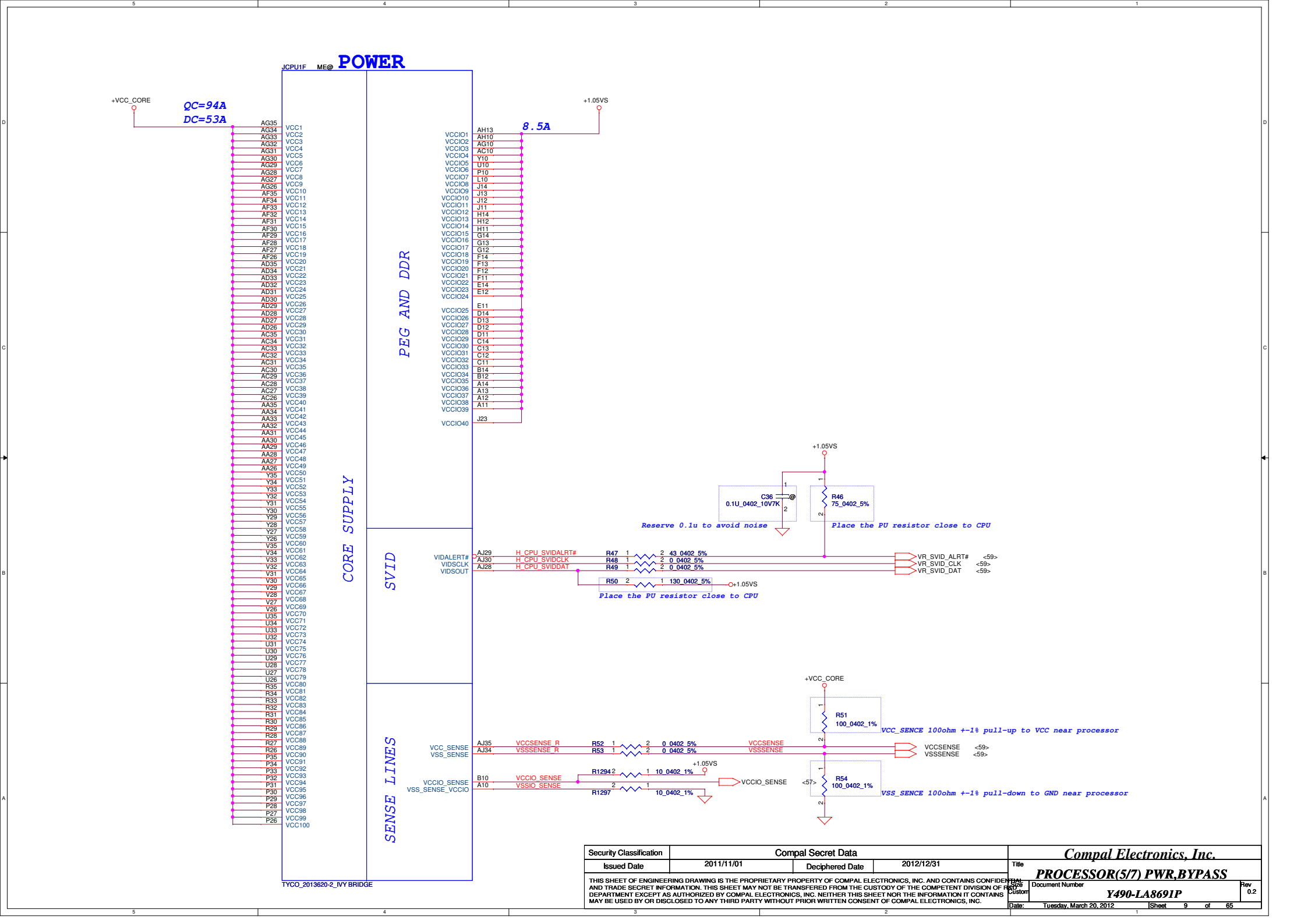
Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled ★10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

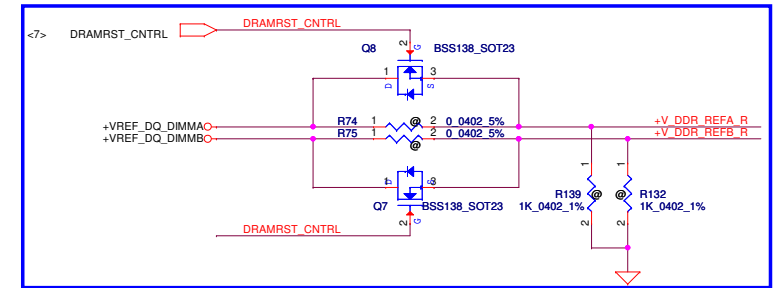
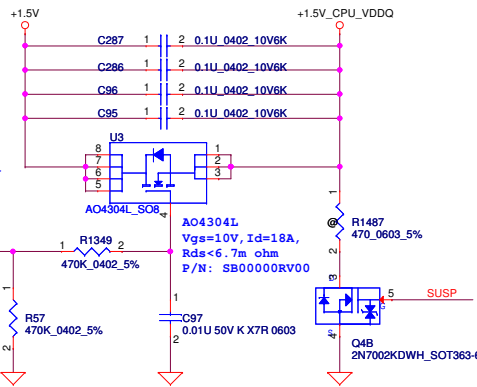
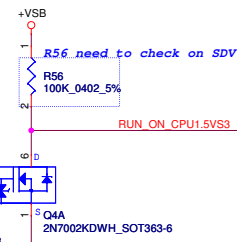
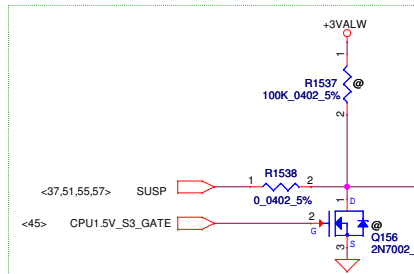


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



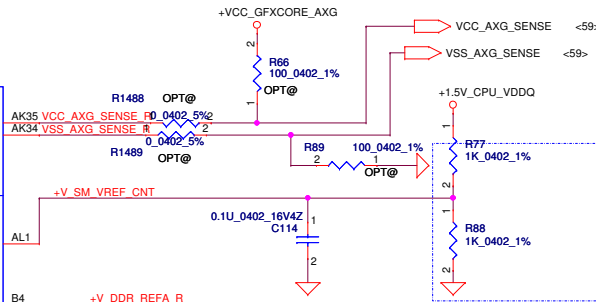
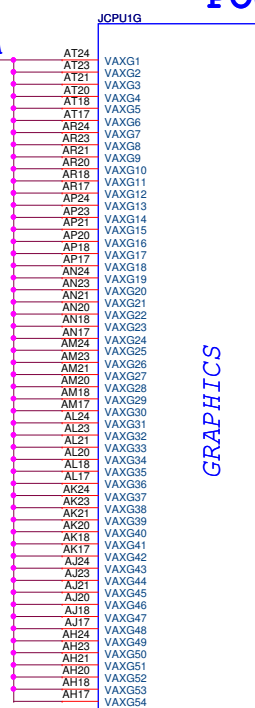
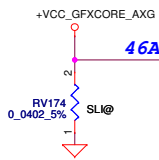
+1.5V_CPU_VDDQ

For Deep S3

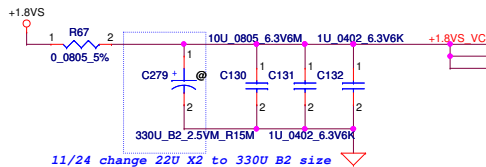
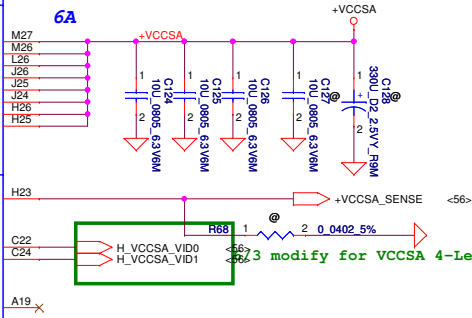
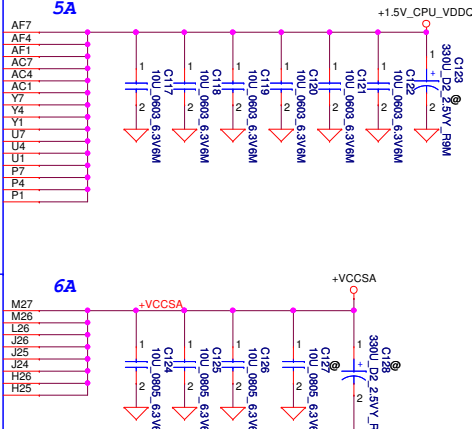


6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

POWER



Place the PU/PD resistor close to CPU within 2 inch (Reserve power side)

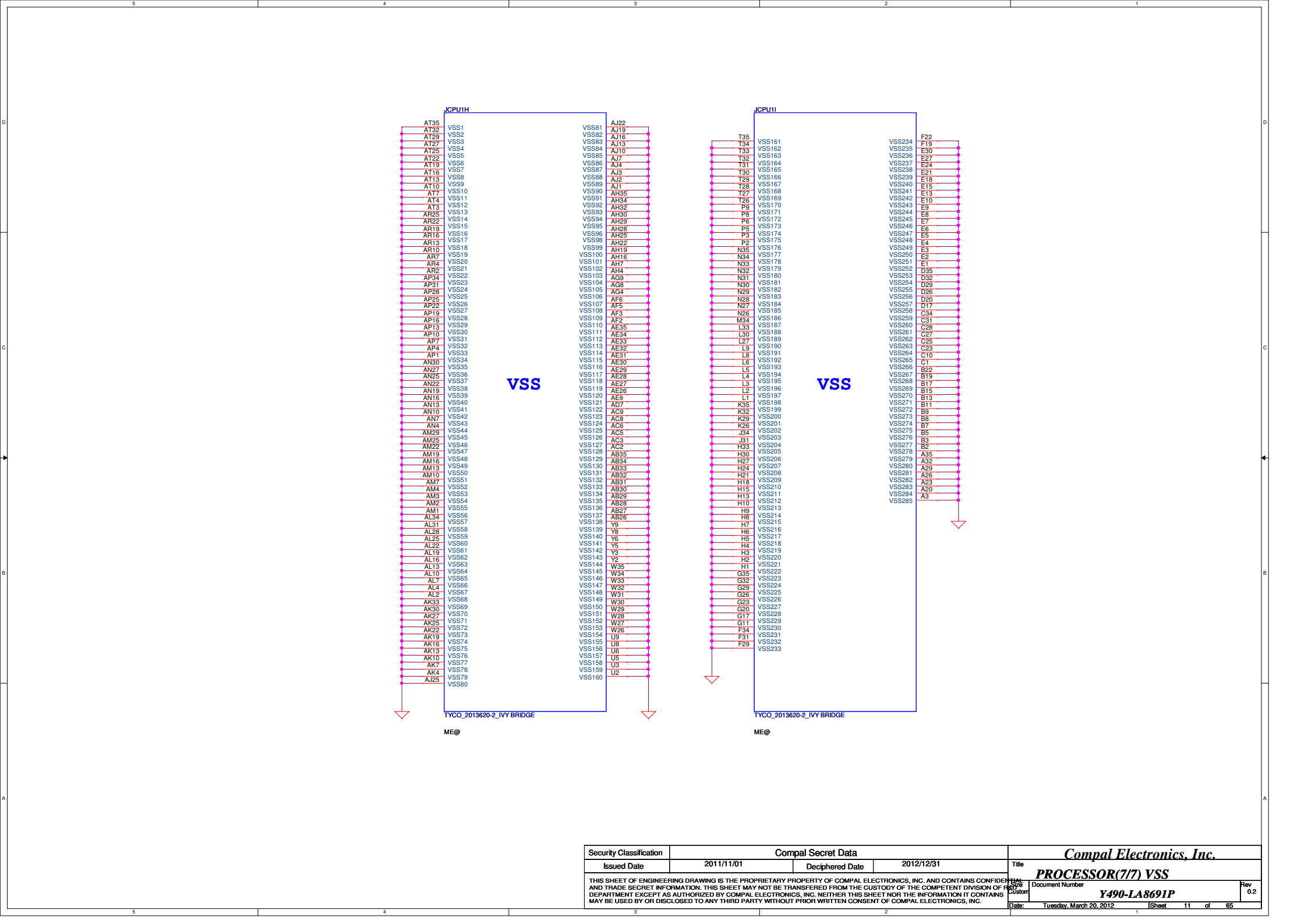


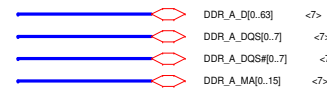
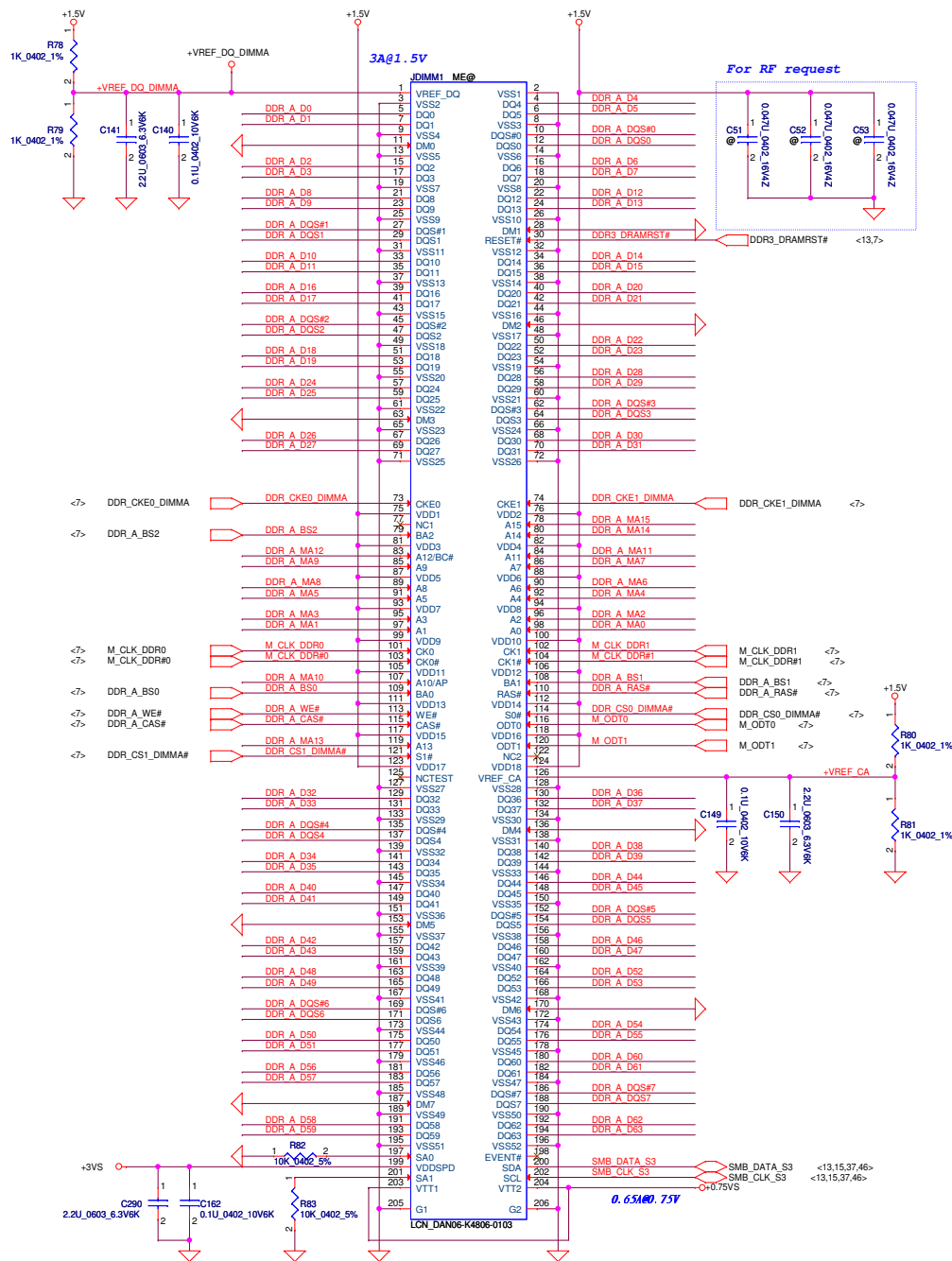
11/24 change 22U X2 to 330U B2 size

TYCO 2013620-2_VYBRIDGE

ME@

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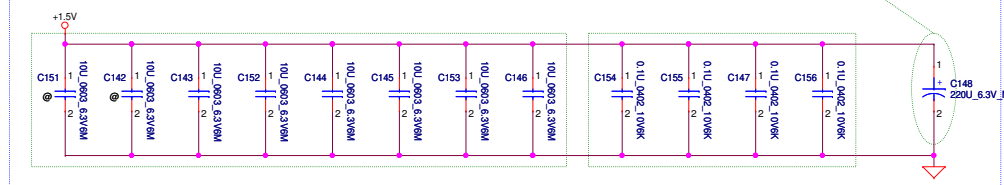


DDR3 SO-DIMM A

```
> DDR_A_D[0..63]      <7>
> DDR_A_DQS[0..7]     <7>
> DDR_A_DQS#[0..7]    <7>
> DDR_A_MA[0..15]     <7>
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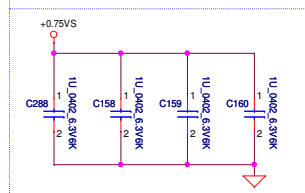
Layout Note:
Place near DIMM

```
OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4
```



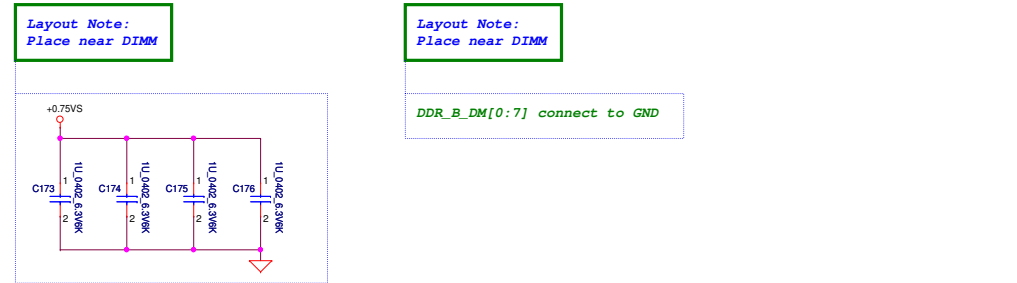
Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

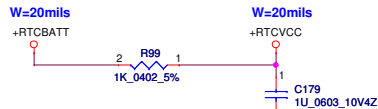


DDR_A_DM[0:7] connect to GND

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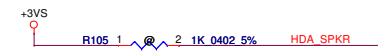


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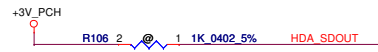


INTVRMEN

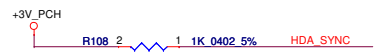
★ H : Integrated VRM enable (Default)
L : Integrated VRM disable
(INTVRMEN should always be pull high.)



HIGH= Enable (No Reboot)
★ LOW= Disable (Default)



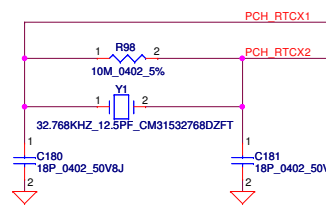
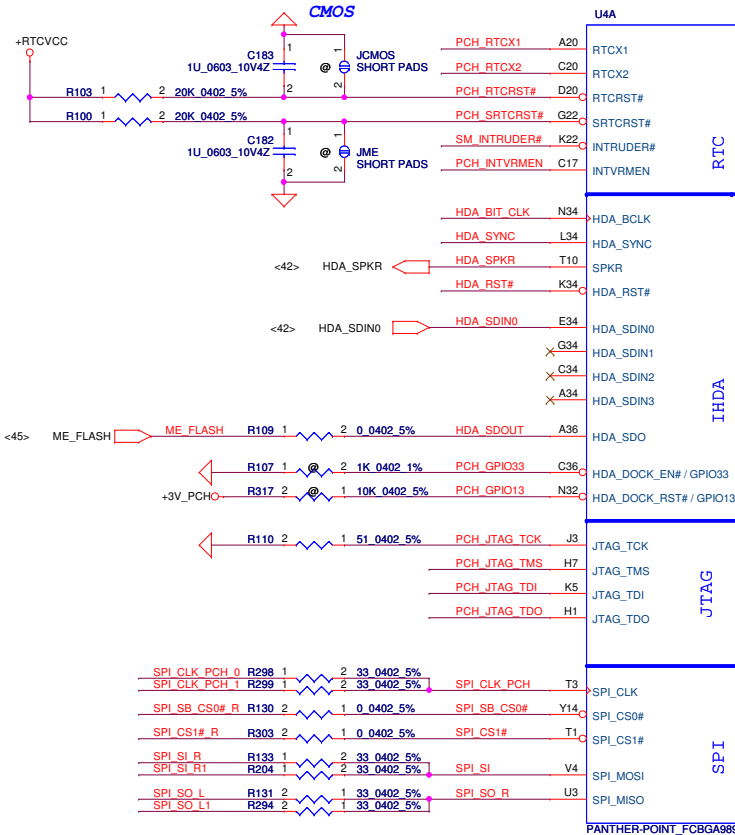
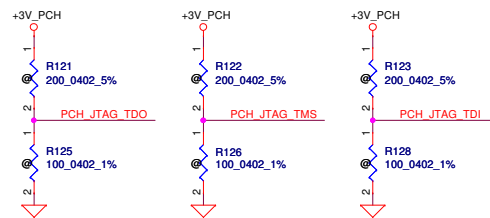
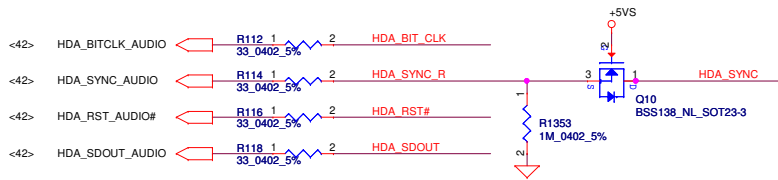
★ Low = Disabled (Default)
High = Enabled
[Flash Descriptor Security Override]



This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
1.5V when sampled high (Default)
★ 1.8V when sampled low
Needs to be pulled High for Chief River platform

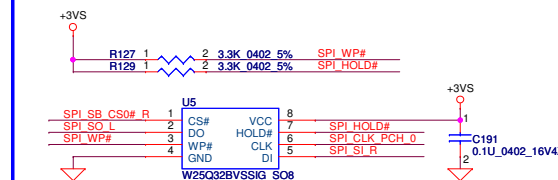
HDA AUDIO



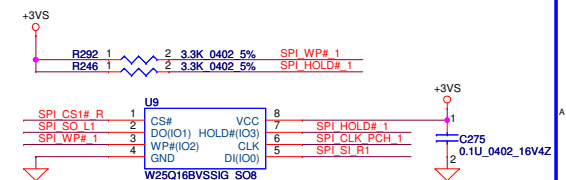
For EMI



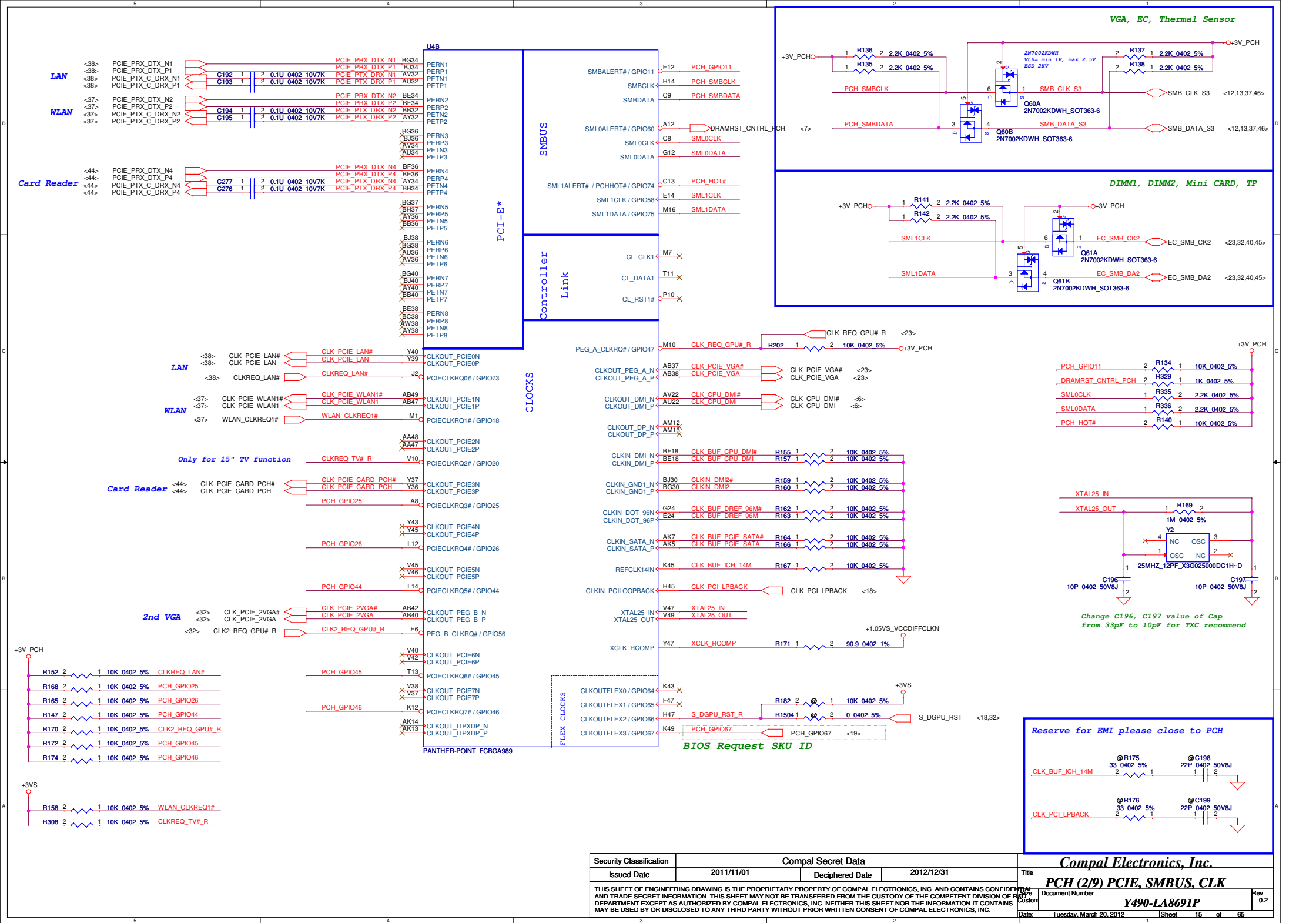
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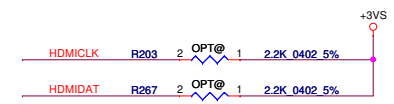
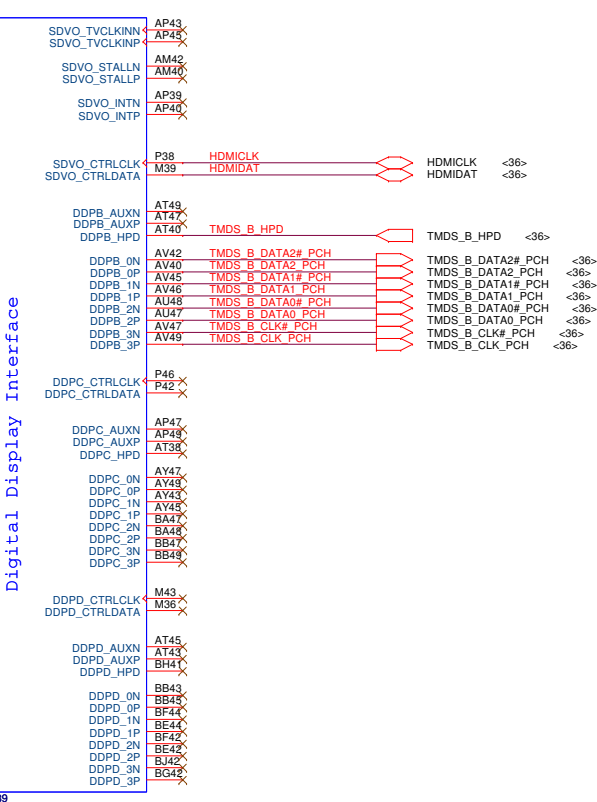
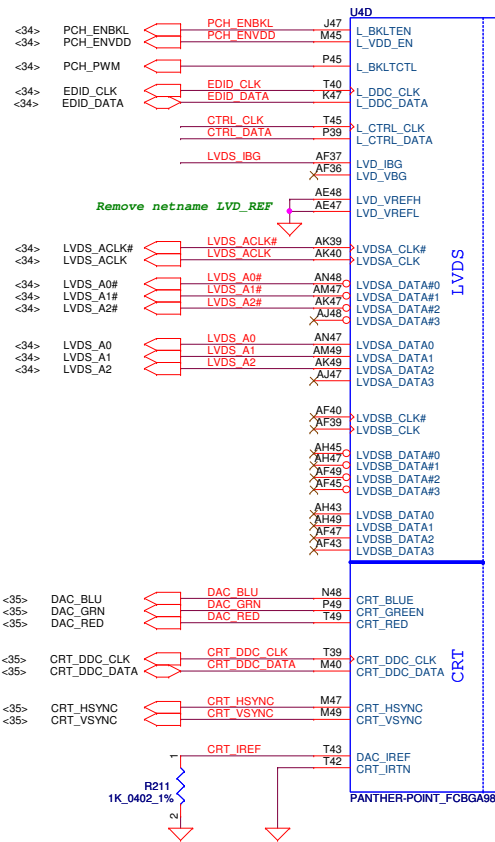
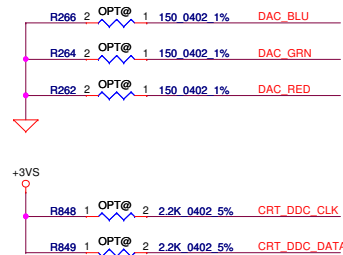
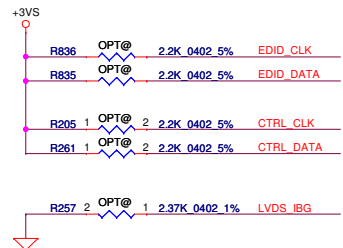


2MB P/N : SA00003FO10

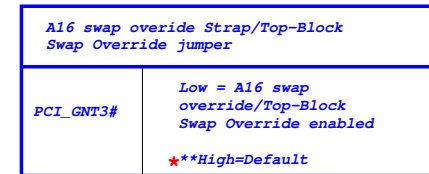
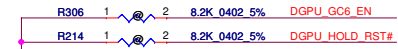
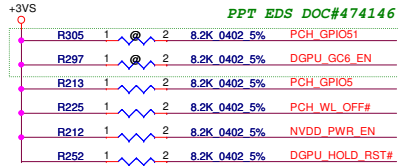
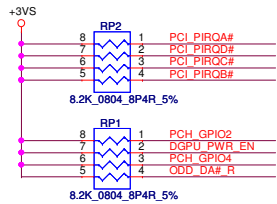


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Date: Tuesday, March 20, 2012				Rev 0.2





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Date: Tuesday, March 20, 2012				Sheet 17 of 65				Rev 0.2			



GPI053 => This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.

<15,32> S_DGPU_RST

<58> NVDD_PWR_EN

<23,51> DGPU_PWR_EN

<27> DGPU_GC6_EN

<37> PCH_WL_OFF#

<41> ODD_DA#_R

<23,32,37,38,44,45,6> PLT_RST#

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<45> CLK_PCI_EC

<37> CLK_PCI_DB

<15> CLK_PCI_LPBACK

<45> CLK_PCI_EC

<37> CLK_PCI_DB

<15> CLK_PCI_LPBACK

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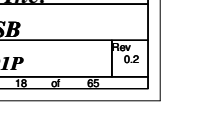
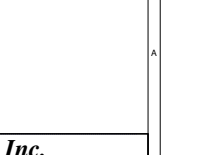
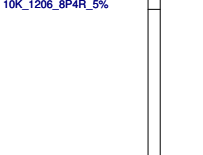
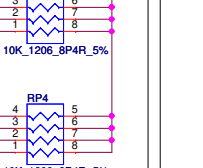
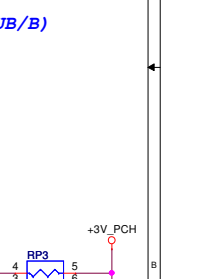
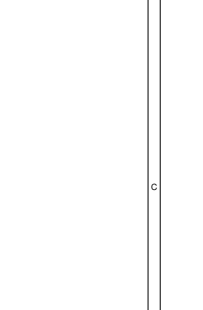
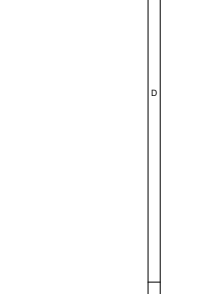
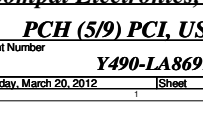
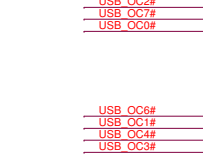
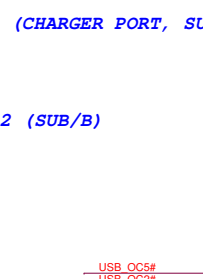
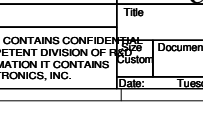
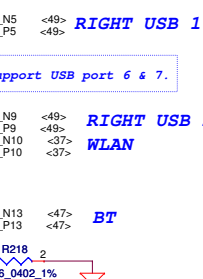
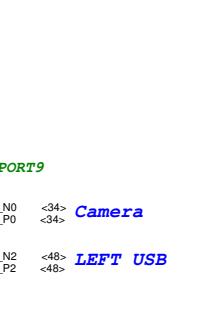
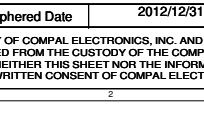
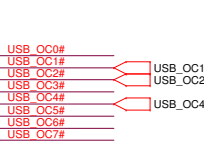
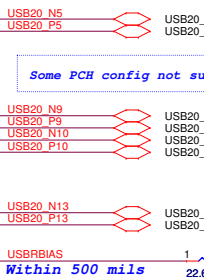
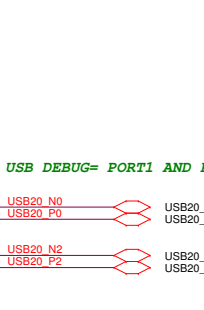
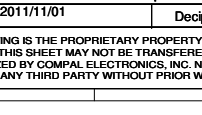
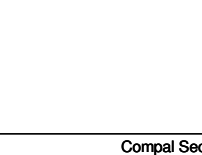
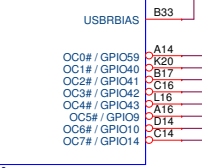
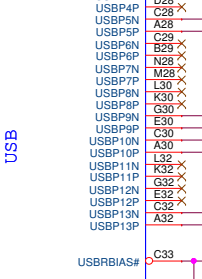
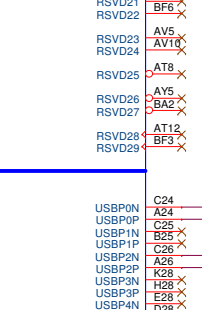
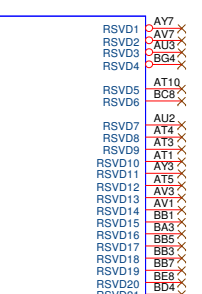
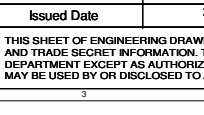
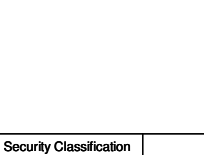
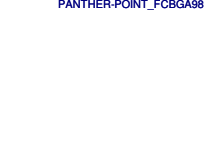
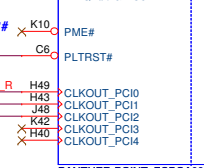
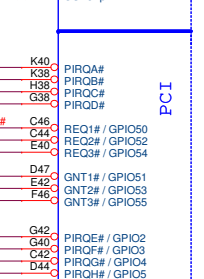
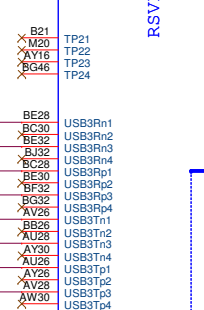
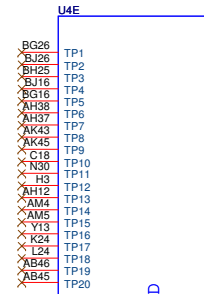
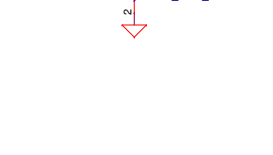
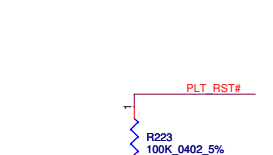
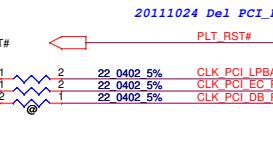
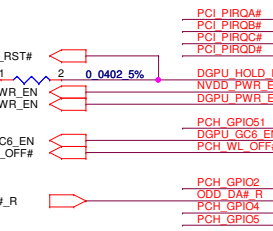
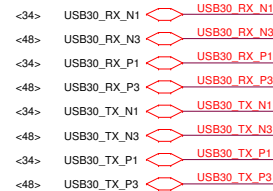
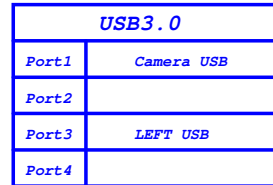
<45> CLK_PCI_EC

<37> CLK_PCI_DB

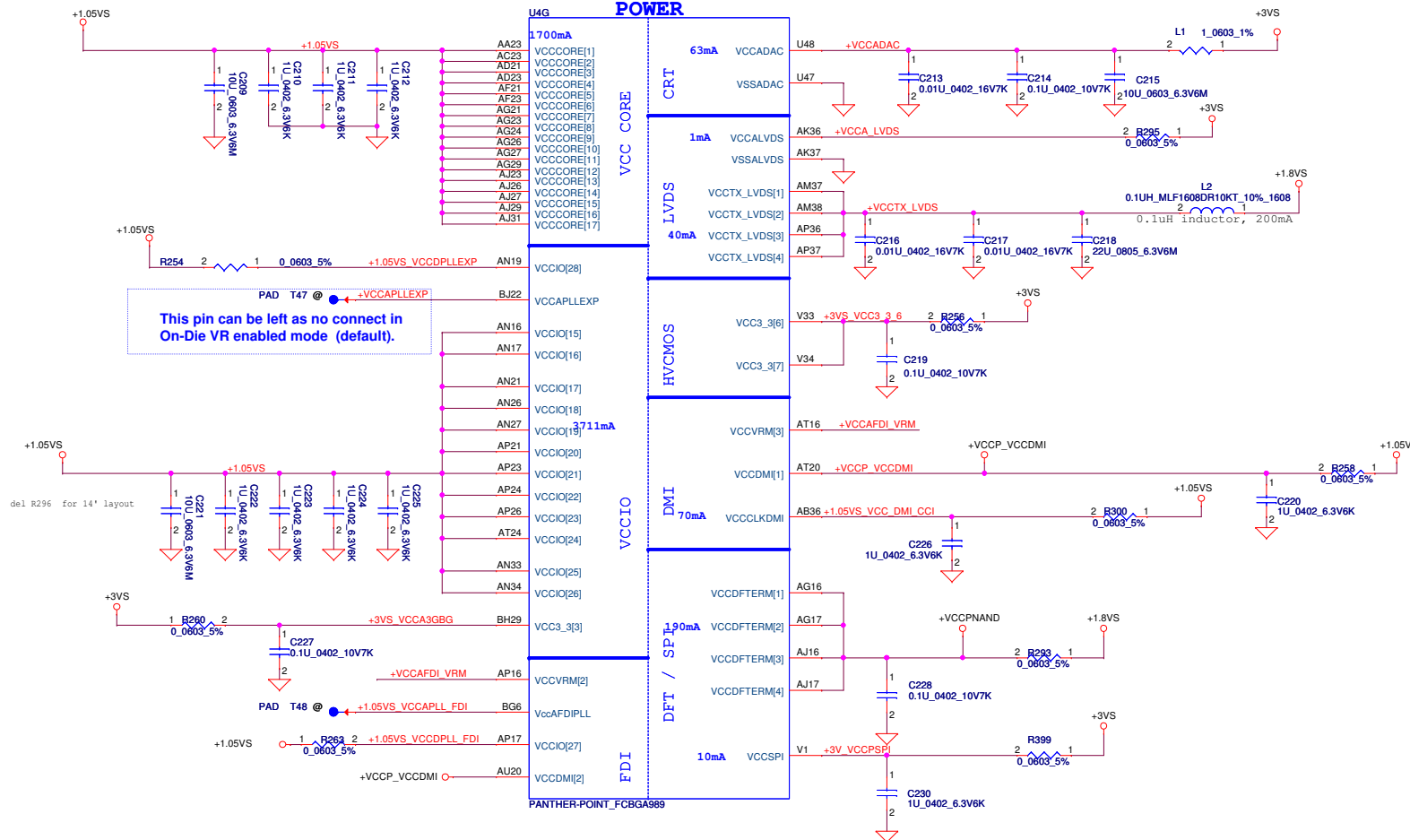
<15> CLK_PCI_LPBACK

<45> CLK_PCI_EC

<37> CLK_PCI_DB



L1 change to 1 ohm P/N
S RES 1/10W 1 +-1% 0603

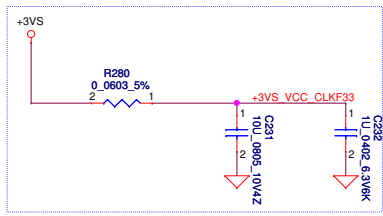


This pin can be left as no connect in On-Die VR enabled mode (default).

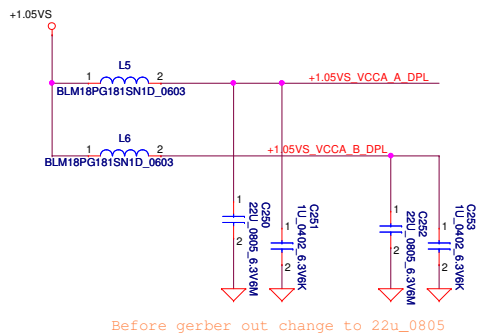
Intel recommend VCCVRM==>1.5V FOR MOBILE
stuff R265 and unstuff R266 VCCVRM==>1.8V FOR DESKTOP
VCCVRM = 160mA detail waiting for newest spec

PCH Power Rail Table
Refer to CPU EDS R1.5

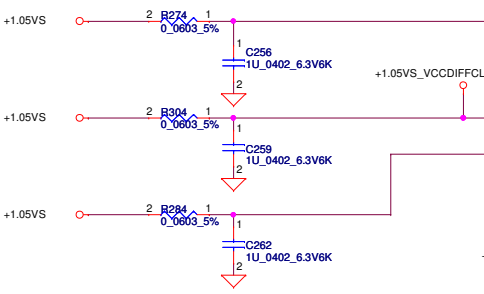
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



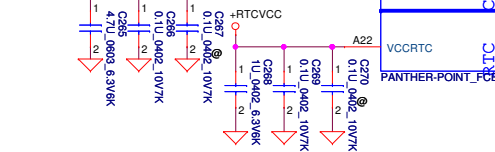
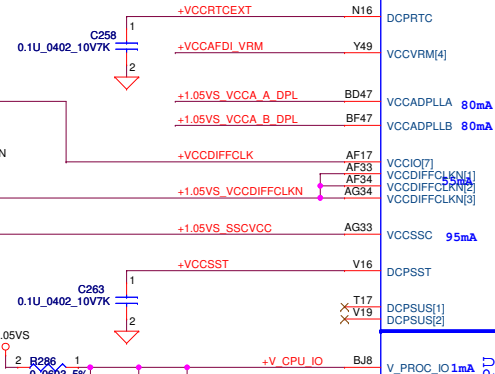
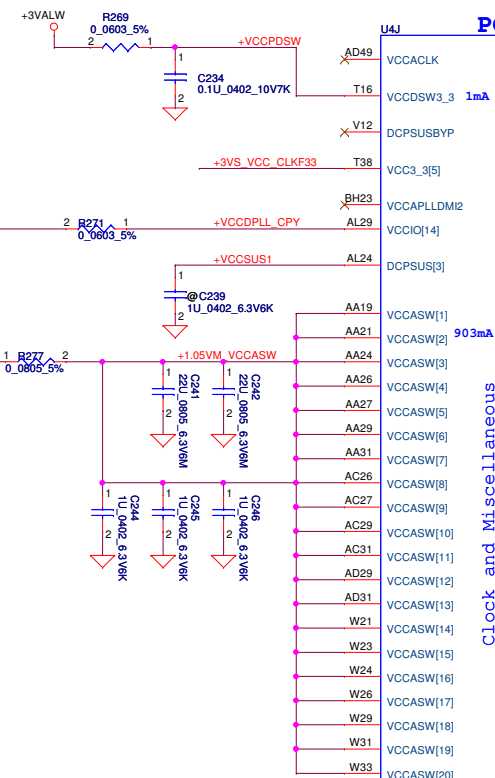
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA



Before gerber out change to 22u_0805



Have internal VRM



POWER

USB

PCI/GPIO/LPC

SATA

MISC

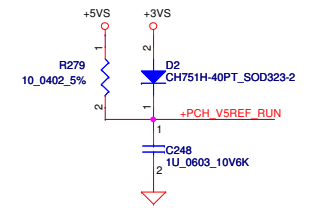
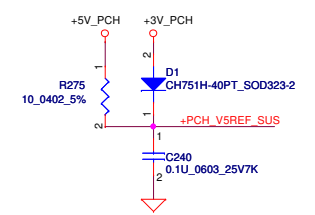
CPU

Clock and Miscellaneous

RTC

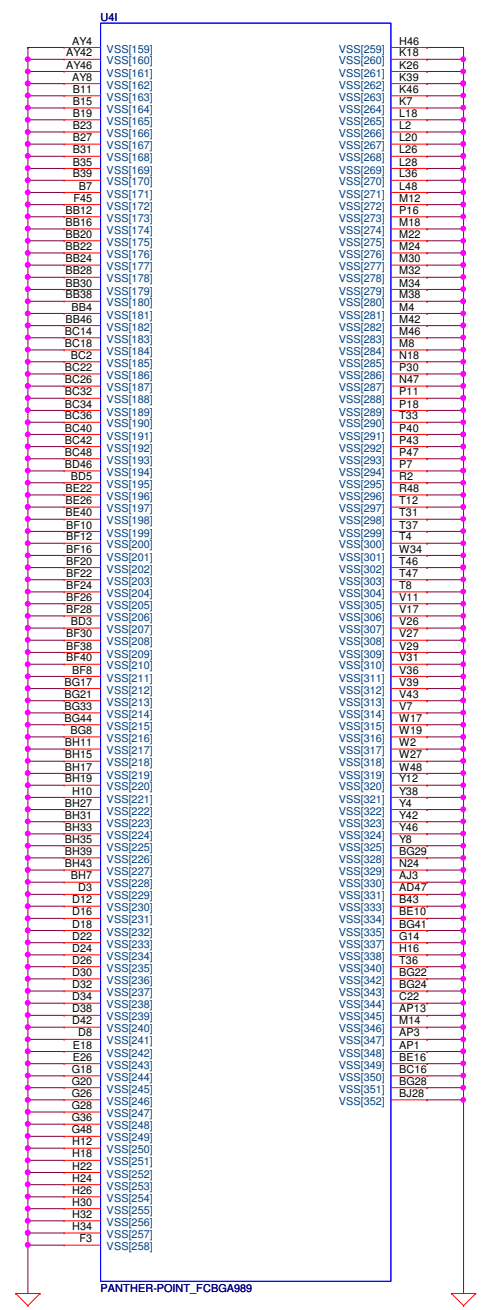
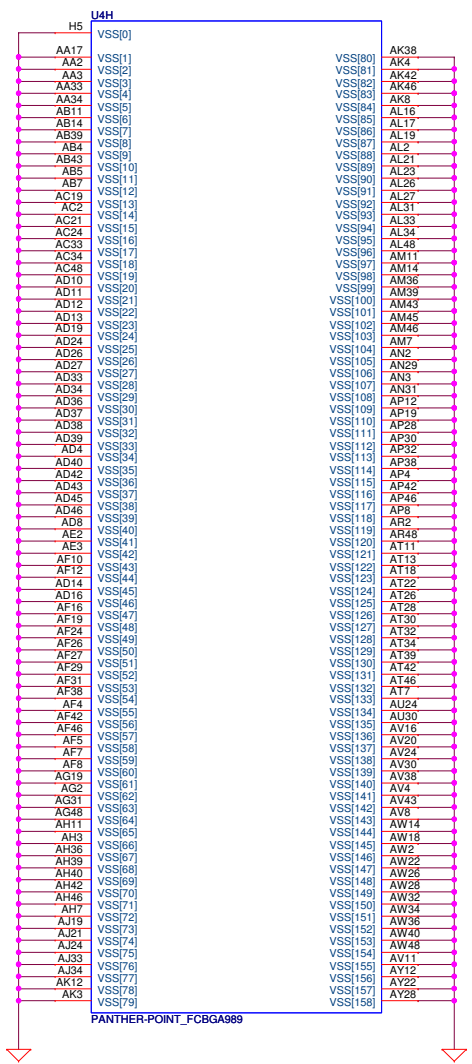
RTC

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

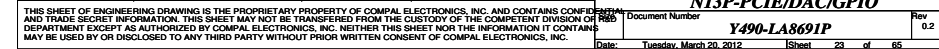


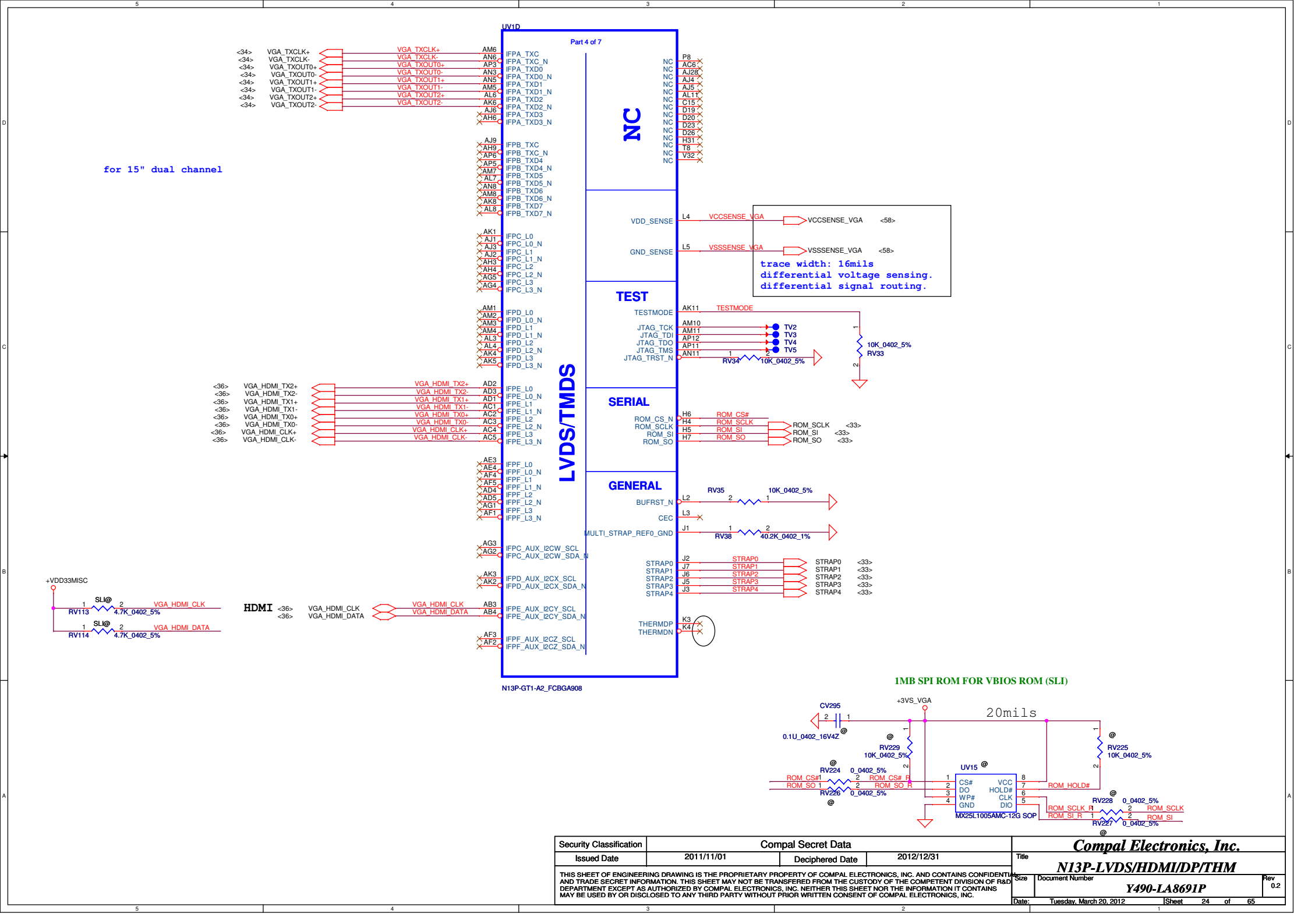
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

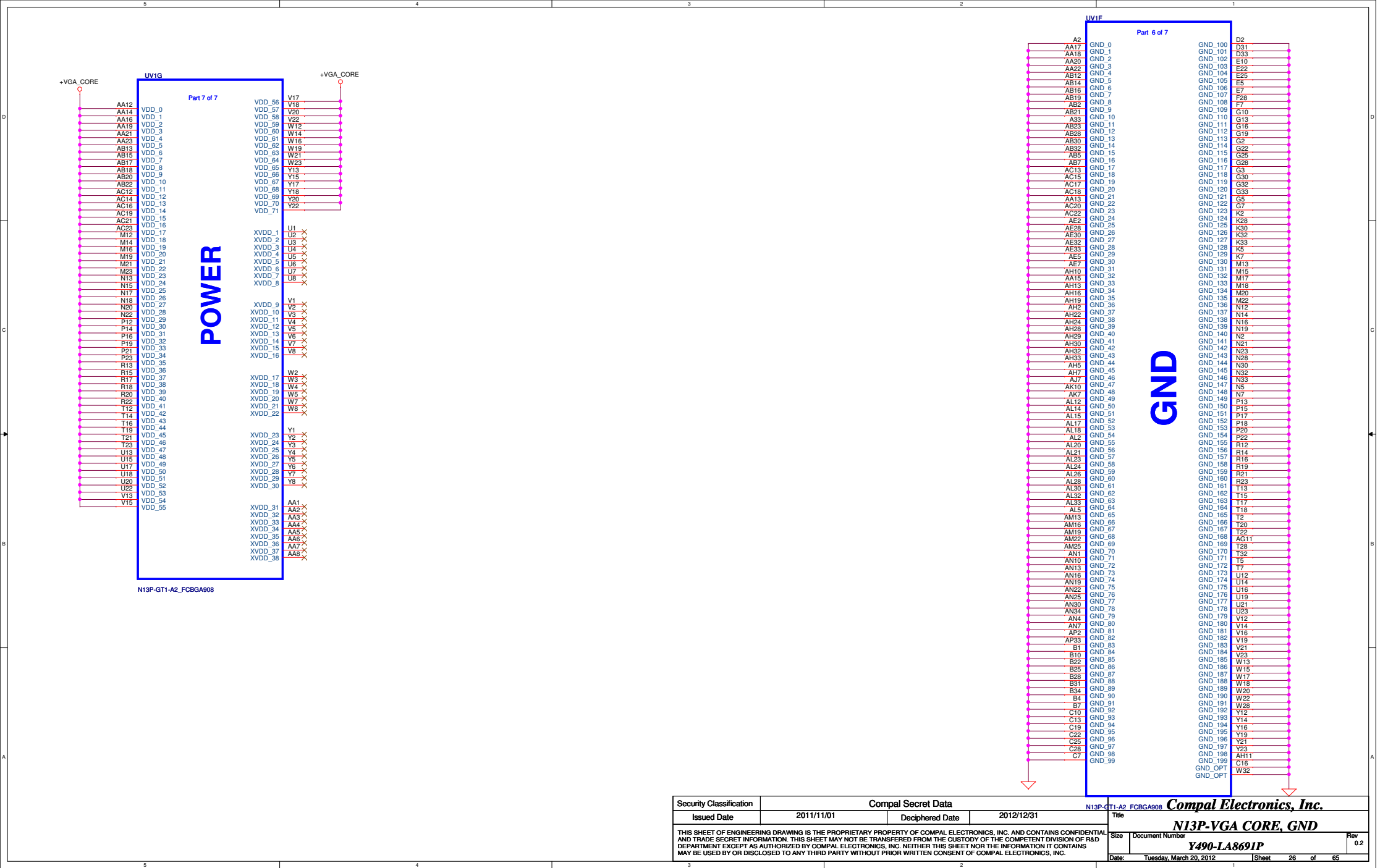
Security Classification		Compal Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	Compal Electronics, Inc. PCH (8/9) PWR	
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				Date: Tuesday, March 20, 2012	Sheet 21 of 65

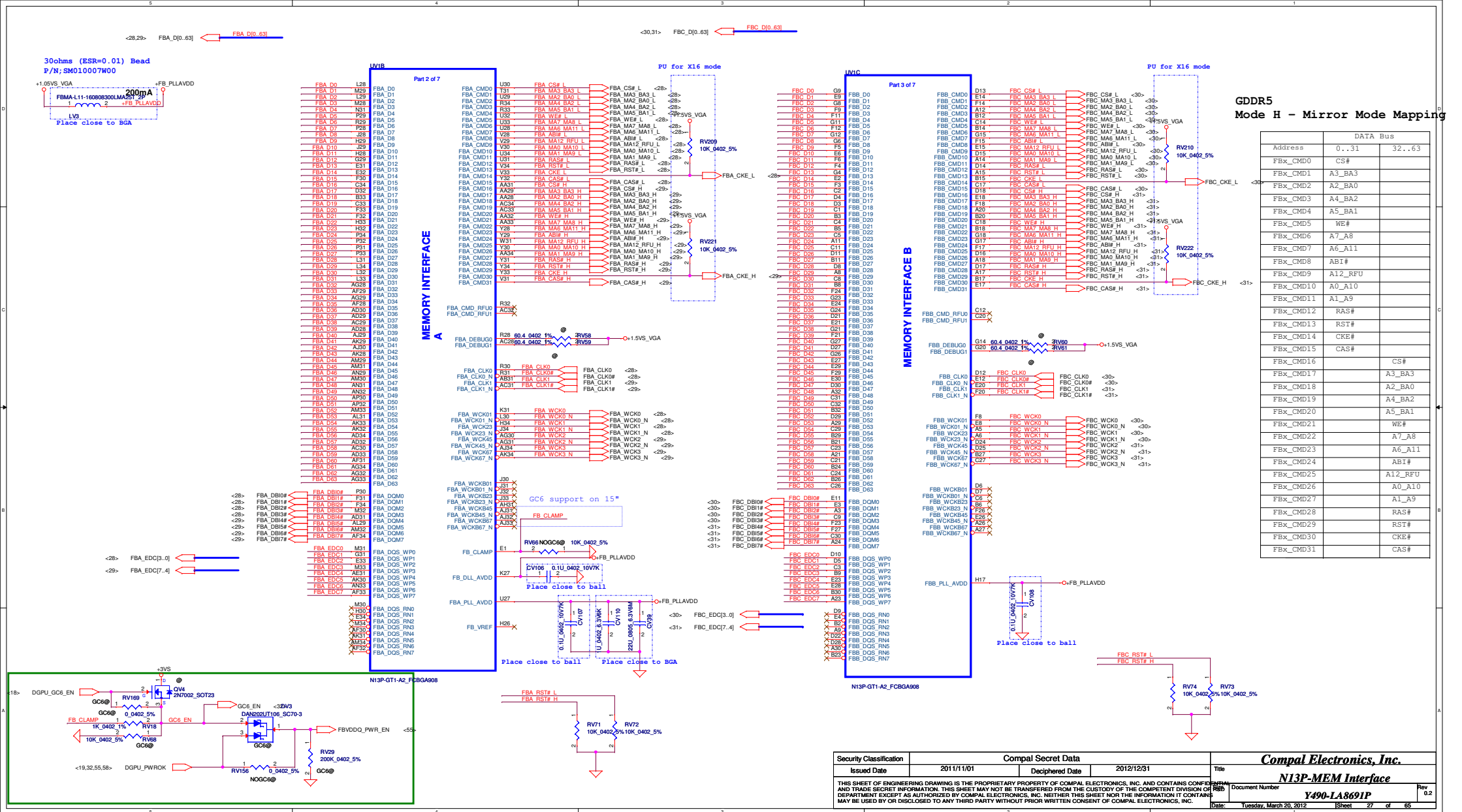


Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2011/11/01		Deciphered Date		2012/12/31		Title					
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								Document Number		Y490-LA8691P		Rev	
								Customer		0.2			
								Date:		Tuesday, March 20, 2012		Sheet 22 of 65	







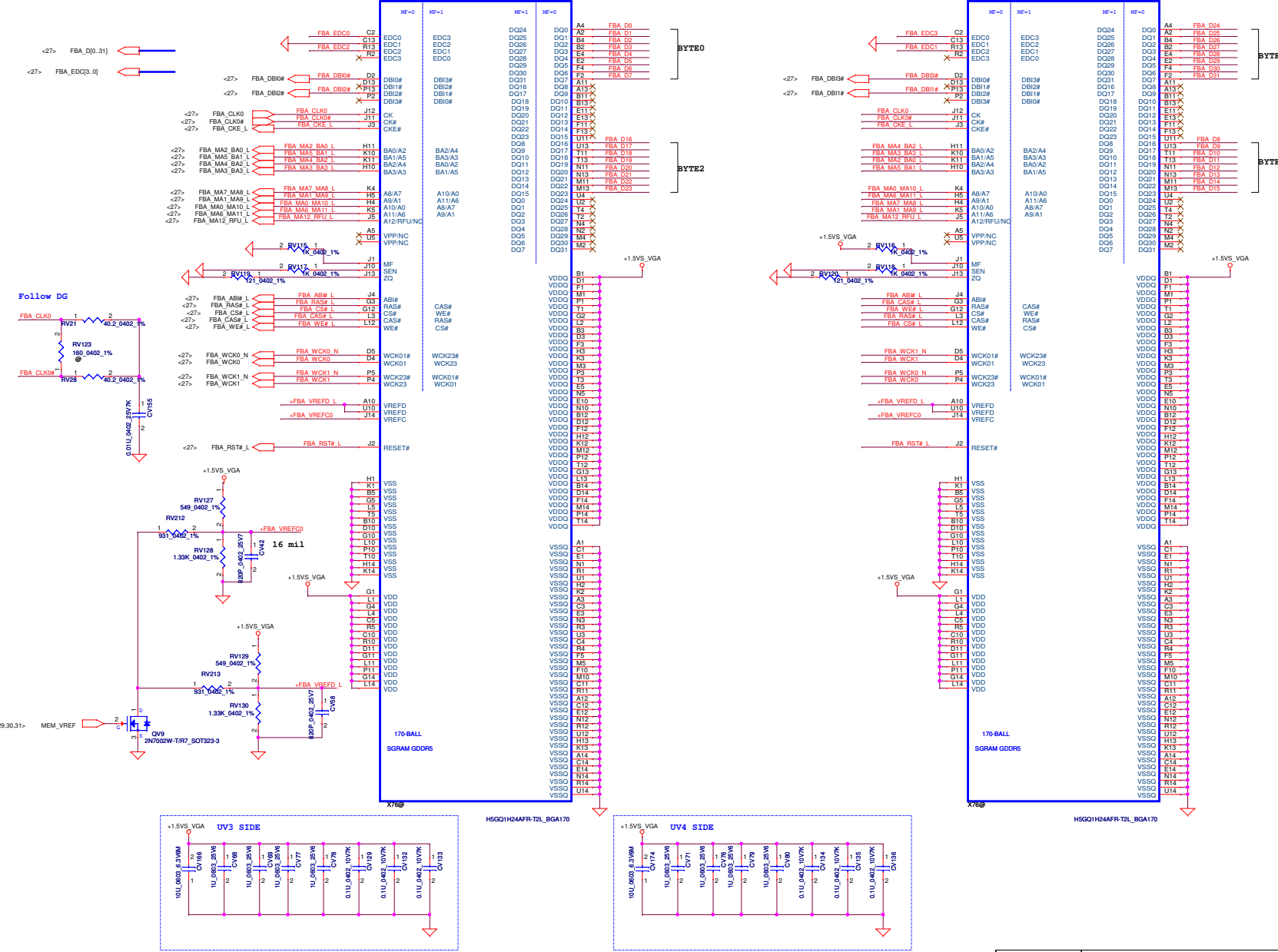


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	AB1#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		AB1#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

Security Classification	Compal Secret Data			Compal Electronics, Inc. N13P-MEM Interface		
Issued Date	2011/1/01	Deciphered Date	2012/12/31	Title	N13P-MEM Interface Y490-LA8691P	
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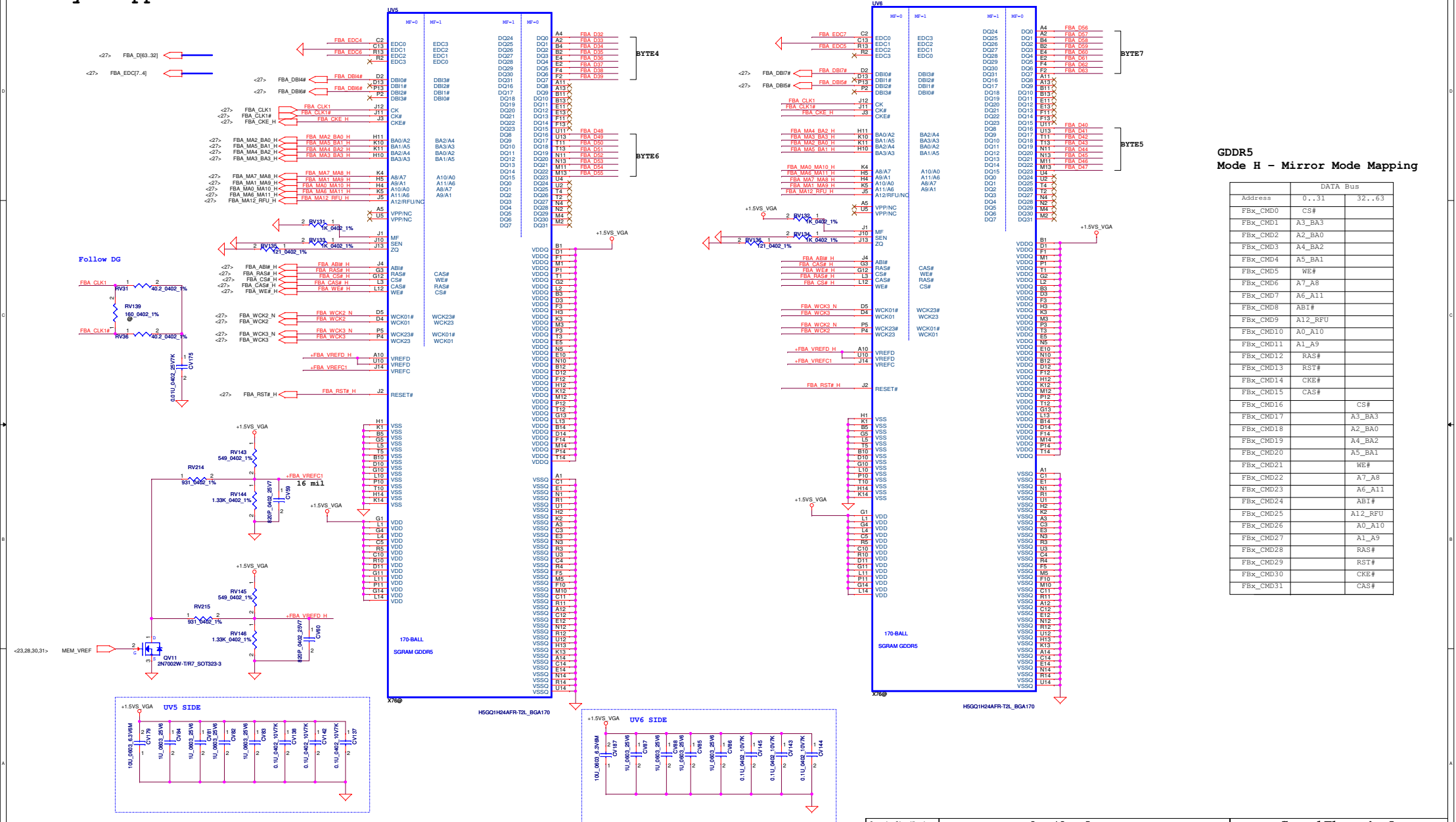
Memory - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

Address	DATA Bus
FBx_CMD0	CS#
FBx_CMD1	A3_BA3
FBx_CMD2	A2_BA0
FBx_CMD3	A4_BA2
FBx_CMD4	A5_BA1
FBx_CMD5	WE#
FBx_CMD6	A7_A8
FBx_CMD7	A6_A11
FBx_CMD8	AB1#
FBx_CMD9	A12_RFU
FBx_CMD10	A0_A10
FBx_CMD11	A1_A9
FBx_CMD12	RAS#
FBx_CMD13	RST#
FBx_CMD14	CKE#
FBx_CMD15	CAS#
FBx_CMD16	CS#
FBx_CMD17	A3_BA3
FBx_CMD18	A2_BA0
FBx_CMD19	A4_BA2
FBx_CMD20	A5_BA1
FBx_CMD21	WE#
FBx_CMD22	A7_A8
FBx_CMD23	A6_A11
FBx_CMD24	AB1#
FBx_CMD25	A12_RFU
FBx_CMD26	A0_A10
FBx_CMD27	A1_A9
FBx_CMD28	RAS#
FBx_CMD29	RST#
FBx_CMD30	CKE#
FBx_CMD31	CAS#

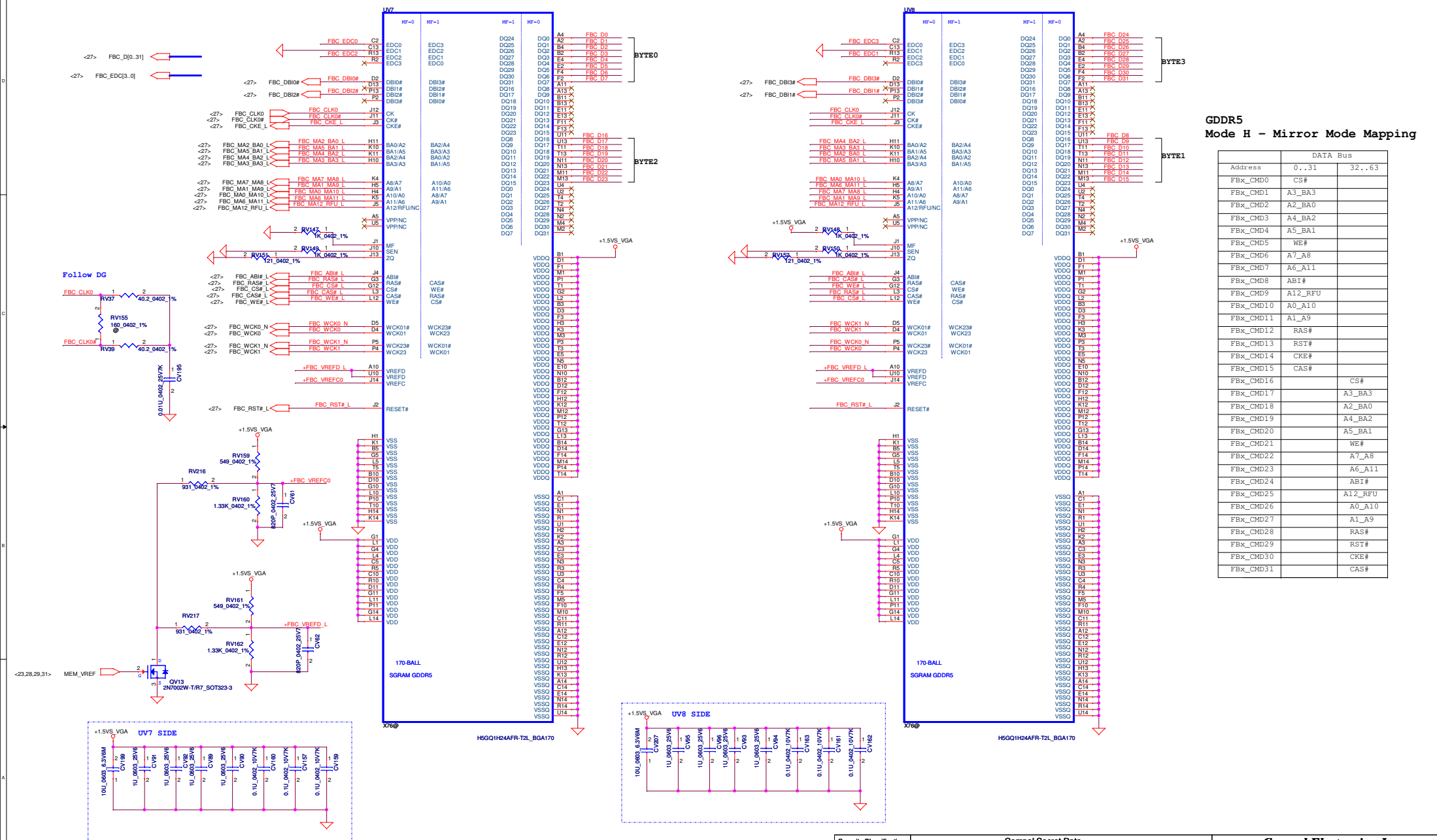
Memory – Upper 32 bits



	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	AB1#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RA5#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17	A3_BA3	
FbX_CMD18	A2_BA0	
FbX_CMD19	A4_BA2	
FbX_CMD20	A5_BA1	
FbX_CMD21	WE#	
FbX_CMD22	A7_A8	
FbX_CMD23	A6_A11	
FbX_CMD24	AB1#	
FbX_CMD25		A12_RFU
FbX_CMD26	A0_A10	
FbX_CMD27	A1_A9	
FbX_CMD28	RA5#	
FbX_CMD29	RST#	
FbX_CMD30	CKE#	
FbX_CMD31	CAS#	

Security Classification	Compul Secret Data		Title		Rev 0.2
Issued Date	2011/1/01	Deciphered Date	2012/12/31	N13P.VRAM A Upper Y490 L8691P	
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			Date:	Tuesday, March 20, 2012	Sheet 29 of 65

Memory Partition C - Lower 32 bits

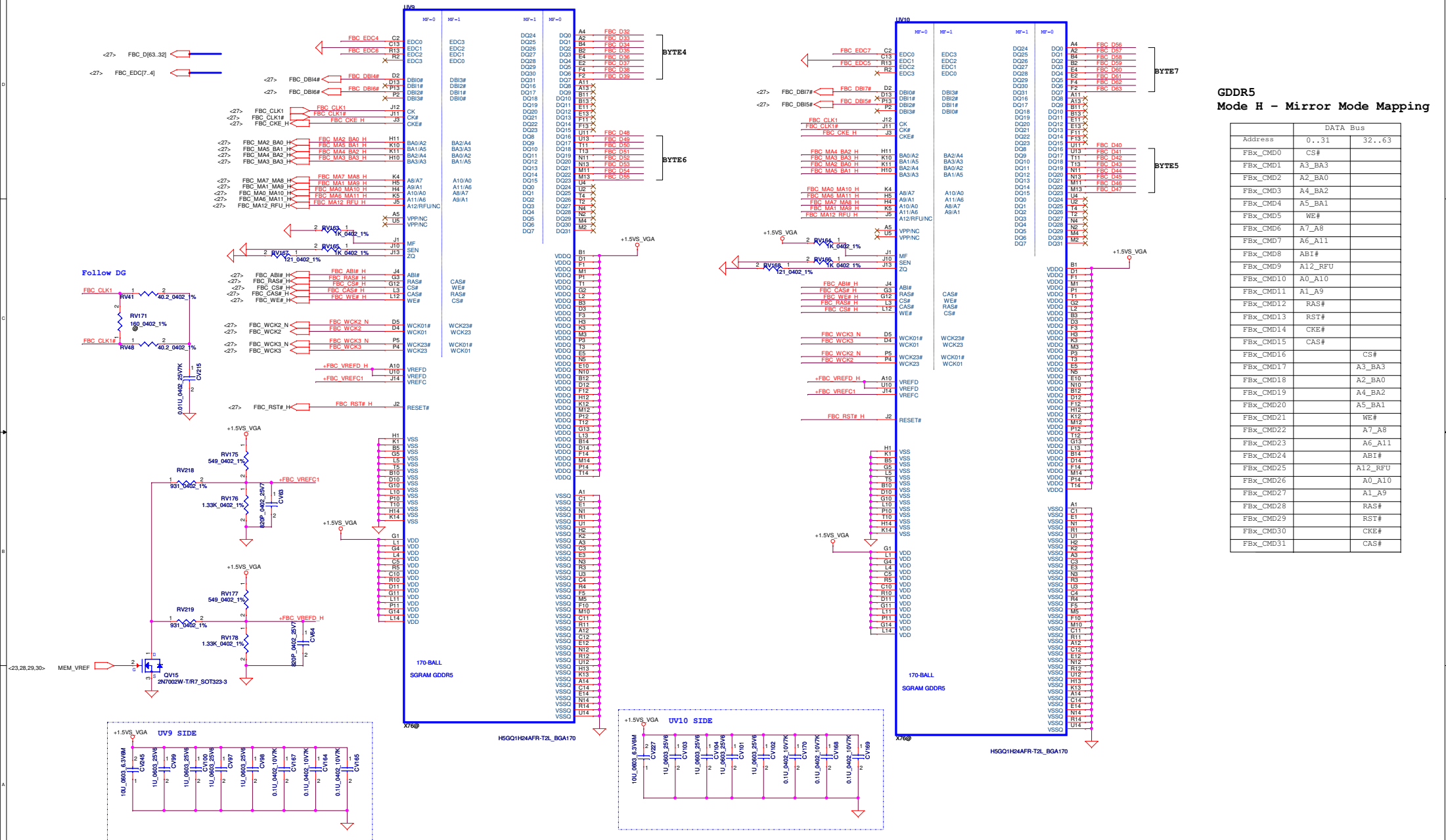


Mode H – Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	AB1#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		AB1#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

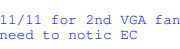
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Issued Date	2011/1/01	Deciphered Date	2011/12		
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Date: Tuesday, March 20, 2012 Sheet 30 of 65					

Memory Partition C - Upper 32 bits

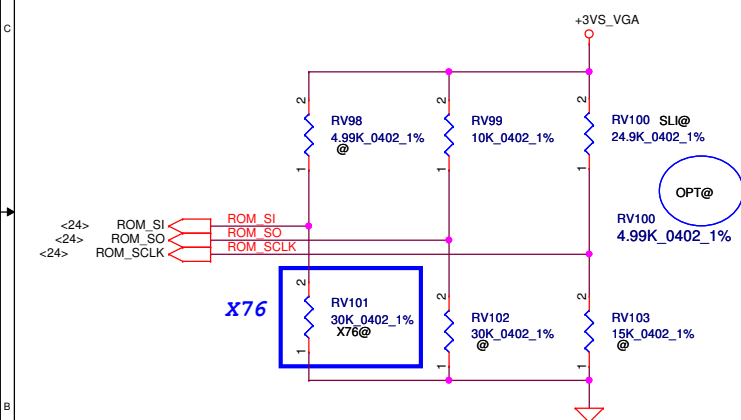
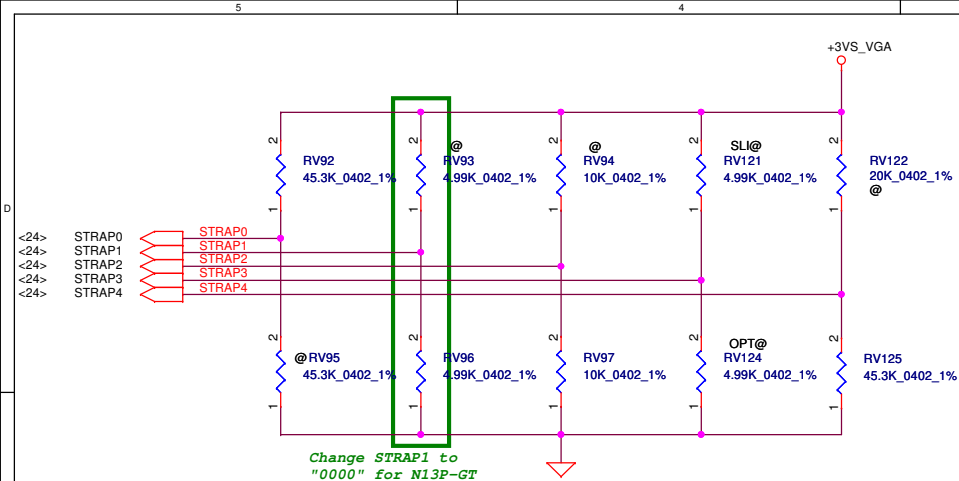


GDDR5 Mode H - Mirror Mode Mapping

Address	0..31	32..63
FBK_CMD0	CS#	
FBK_CMD1	A3_BA3	
FBK_CMD2	A2_BA0	
FBK_CMD3	A4_BA2	
FBK_CMD4	A5_BA1	
FBK_CMD5	WE#	
FBK_CMD6	A7_A8	
FBK_CMD7	A6_A11	
FBK_CMD8	ABI#	
FBK_CMD9	A12_RFU	
FBK_CMD10	A0_A10	
FBK_CMD11	A1_A9	
FBK_CMD12	RAS#	
FBK_CMD13	RST#	
FBK_CMD14	CKE#	
FBK_CMD15	CAS#	
FBK_CMD16		CS#
FBK_CMD17		A3_BA3
FBK_CMD18		A2_BA0
FBK_CMD19		A4_BA2
FBK_CMD20		A5_BA1
FBK_CMD21		WE#
FBK_CMD22		A7_A8
FBK_CMD23		A6_A11
FBK_CMD24		ABI#
FBK_CMD25		A12_RFU
FBK_CMD26		A0_A10
FBK_CMD27		A1_A9
FBK_CMD28		RAS#
FBK_CMD29		RST#
FBK_CMD30		CKE#
FBK_CMD31		CAS#



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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

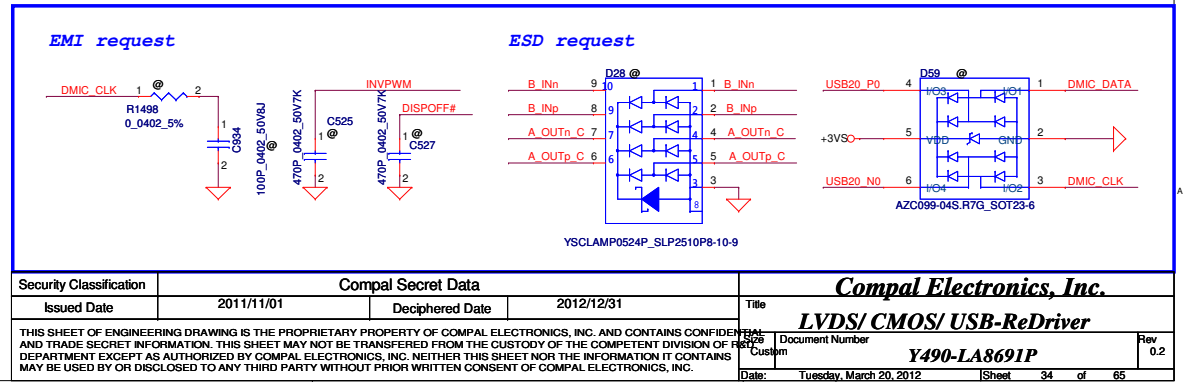
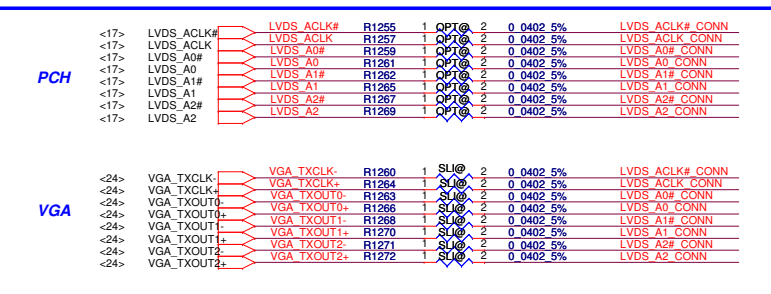
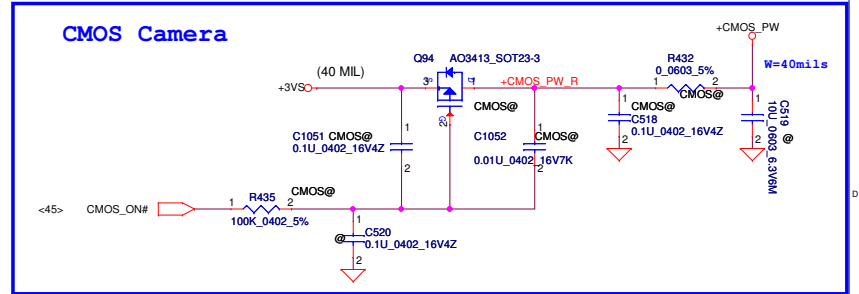
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

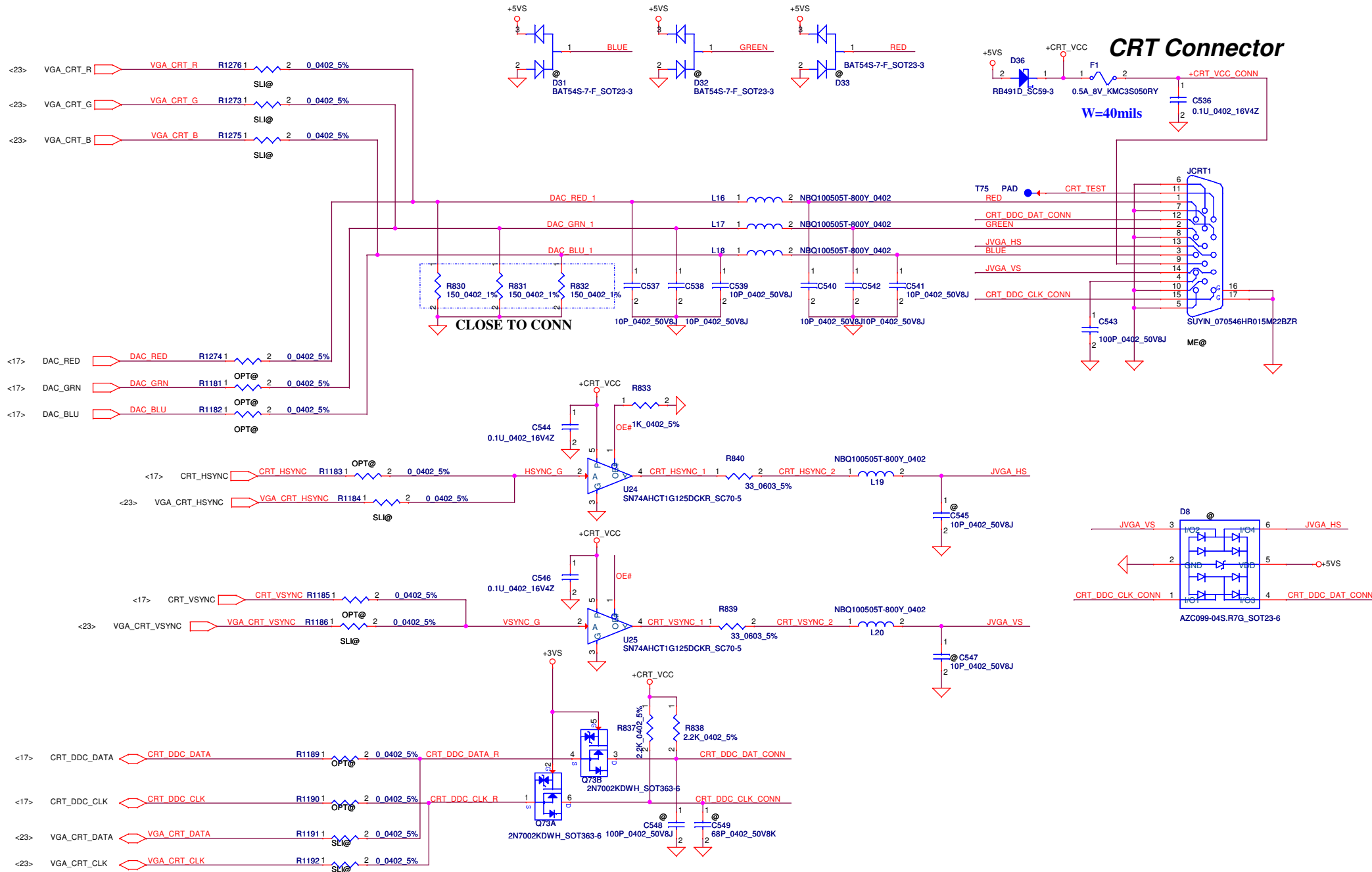
X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PU 25K (SLI)	PU 45K	PD 5K	PD 10K	PU 5K	PD 10K
		K4G10325FG-HC04 1G 32Mx32	PD 45K							
	Hynix	H5GQ2H24MFR-T2C 2G 64Mx32	PD 25K							
		H5GQ1H24BFR-T2C 1G 32Mx32	PD 35K							

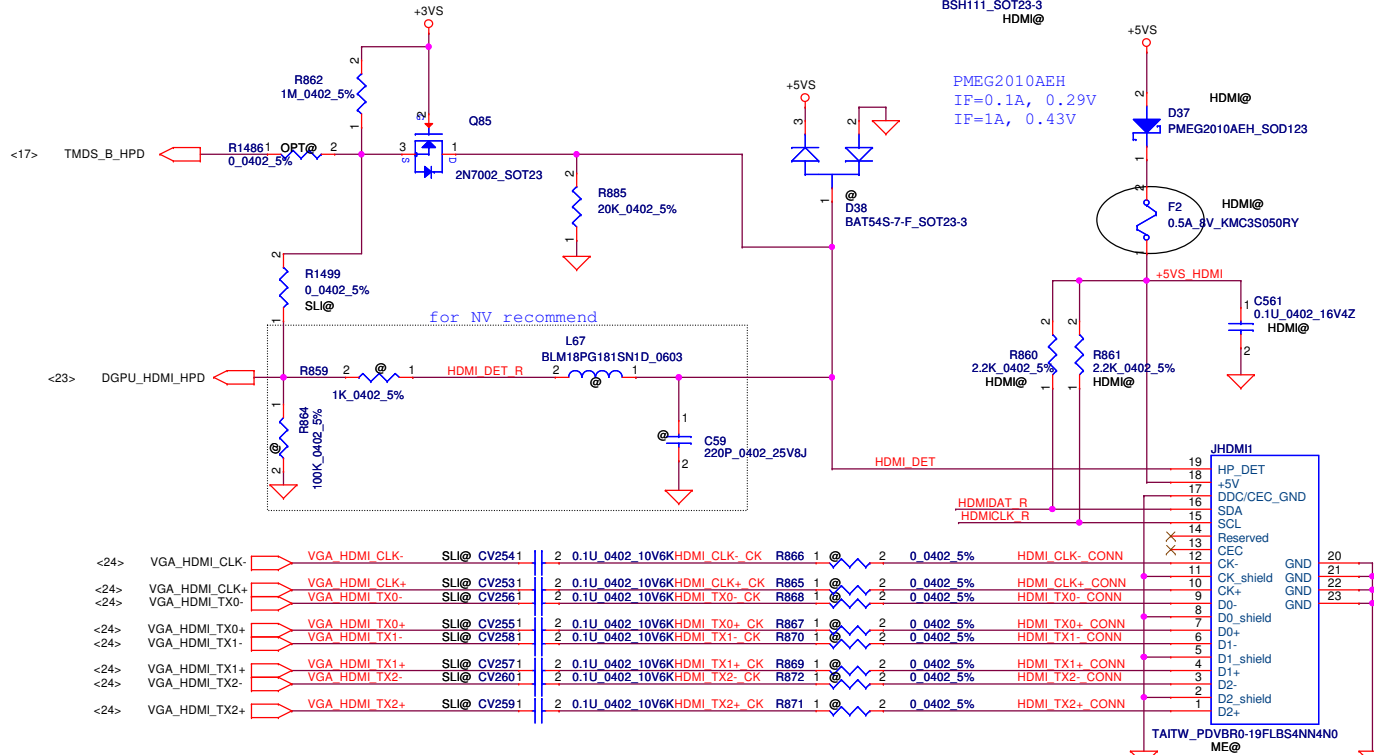
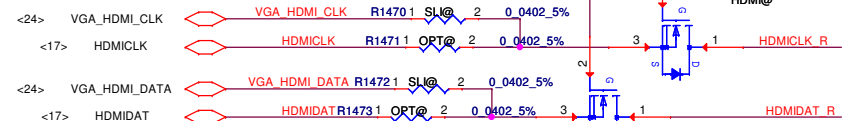
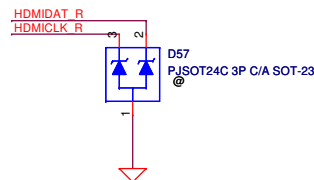
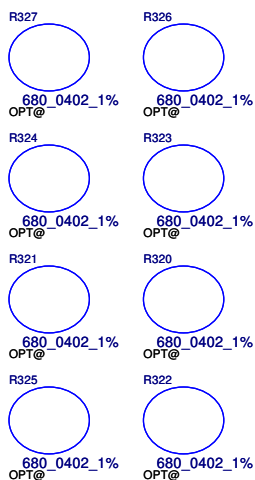
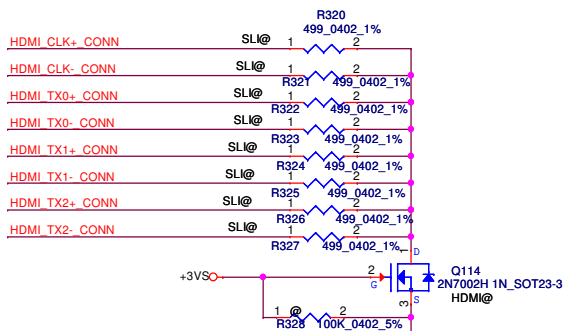
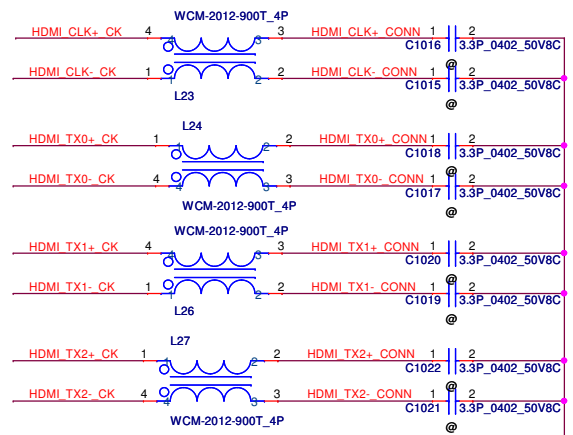
VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J

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Size	Custom	Document Number	Y490-LA8691P	Rev	0.2
Date:	Tuesday, March 20, 2012	Sheet	35	of	65

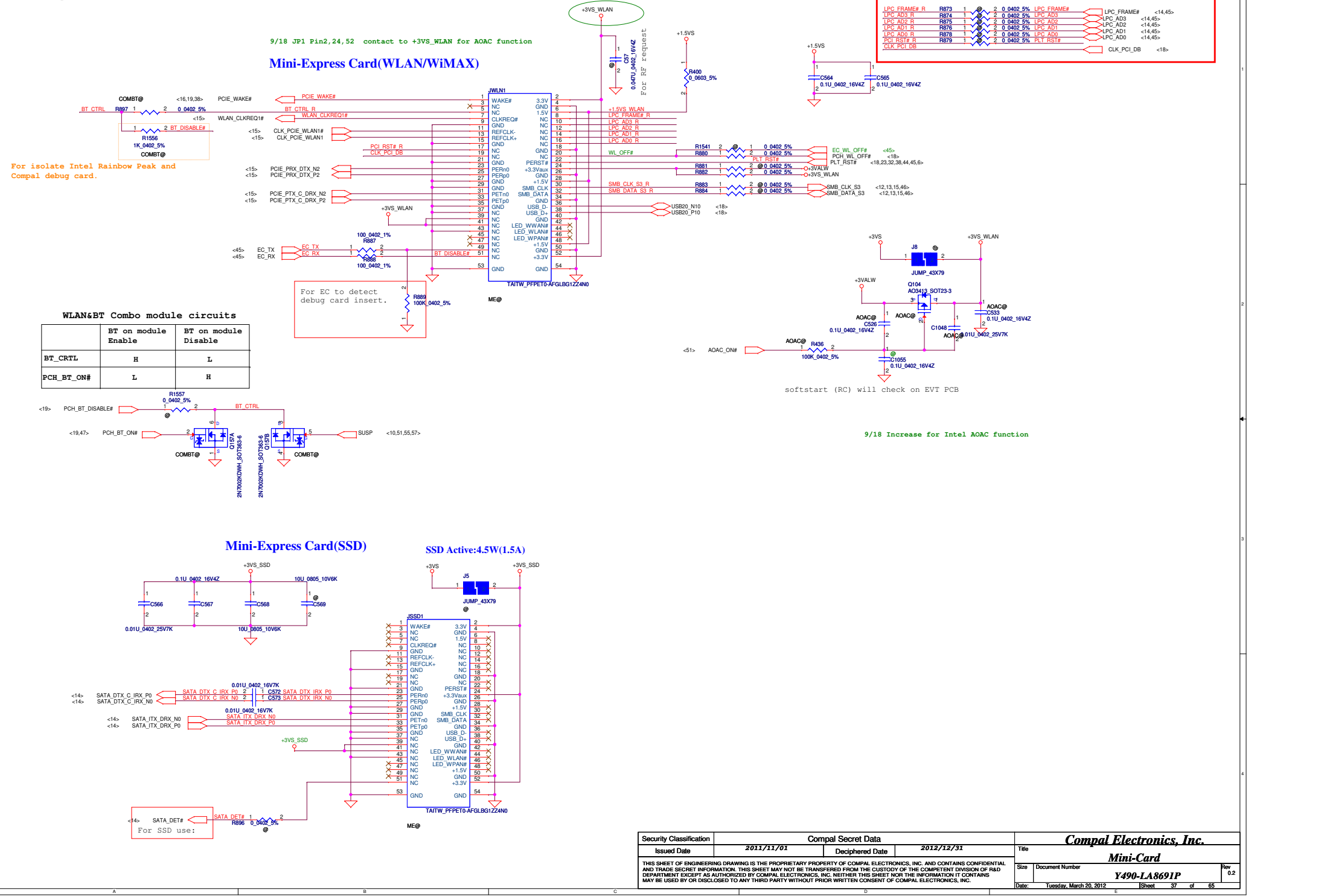


<17>	TMDS_B_DATA2#_PCH	TMDS_B_DATA2#_PCH	OPT@	C200	1	2	0.1U	0402	10V6K	HDMI TX2- CK
<17>	TMDS_B_DATA2#_PCH	TMDS_B_DATA2#_PCH	OPT@	C201	1	2	0.1U	0402	10V6K	HDMI TX2+ CK
<17>	TMDS_B_DATA1#_PCH	TMDS_B_DATA1#_PCH	OPT@	C203	1	2	0.1U	0402	10V6K	HDMI TX1- CK
<17>	TMDS_B_DATA1#_PCH	TMDS_B_DATA1#_PCH	OPT@	C206	1	2	0.1U	0402	10V6K	HDMI TX1+ CK
<17>	TMDS_B_DATA0#_PCH	TMDS_B_DATA0#_PCH	OPT@	C204	1	2	0.1U	0402	10V6K	HDMI TX0- CK
<17>	TMDS_B_DATA0#_PCH	TMDS_B_DATA0#_PCH	OPT@	C205	1	2	0.1U	0402	10V6K	HDMI TX0+ CK
<17>	TMDS_B_CLK#_PCH	TMDS_B_CLK#_PCH	OPT@	C208	1	2	0.1U	0402	10V6K	HDMI CLK- CK
<17>	TMDS_B_CLK#_PCH	TMDS_B_CLK#_PCH	OPT@	C207	1	2	0.1U	0402	10V6K	HDMI CLK+ CK



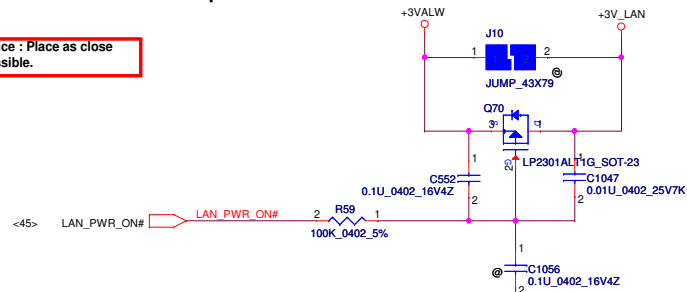
Security Classification				Compal Secret Data				Compal Electronics, Ltd.			
Issued Date				2011/11/01				Deciphered Date			
2012/12/31				Title				HDMI CONN			
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Date: Tuesday, March 20, 2012				Document Number				Rev 0.2			
Sheet 36 of 65				Date: Tuesday, March 20, 2012				Sheet 36 of 65			

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

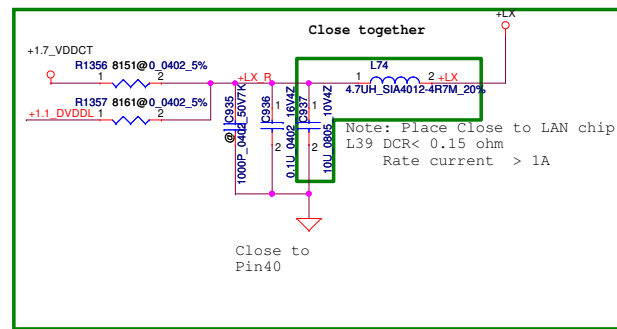
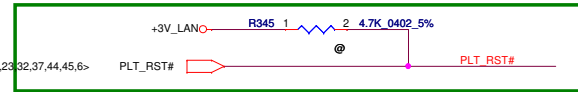


Atheros request can't disable LAN power

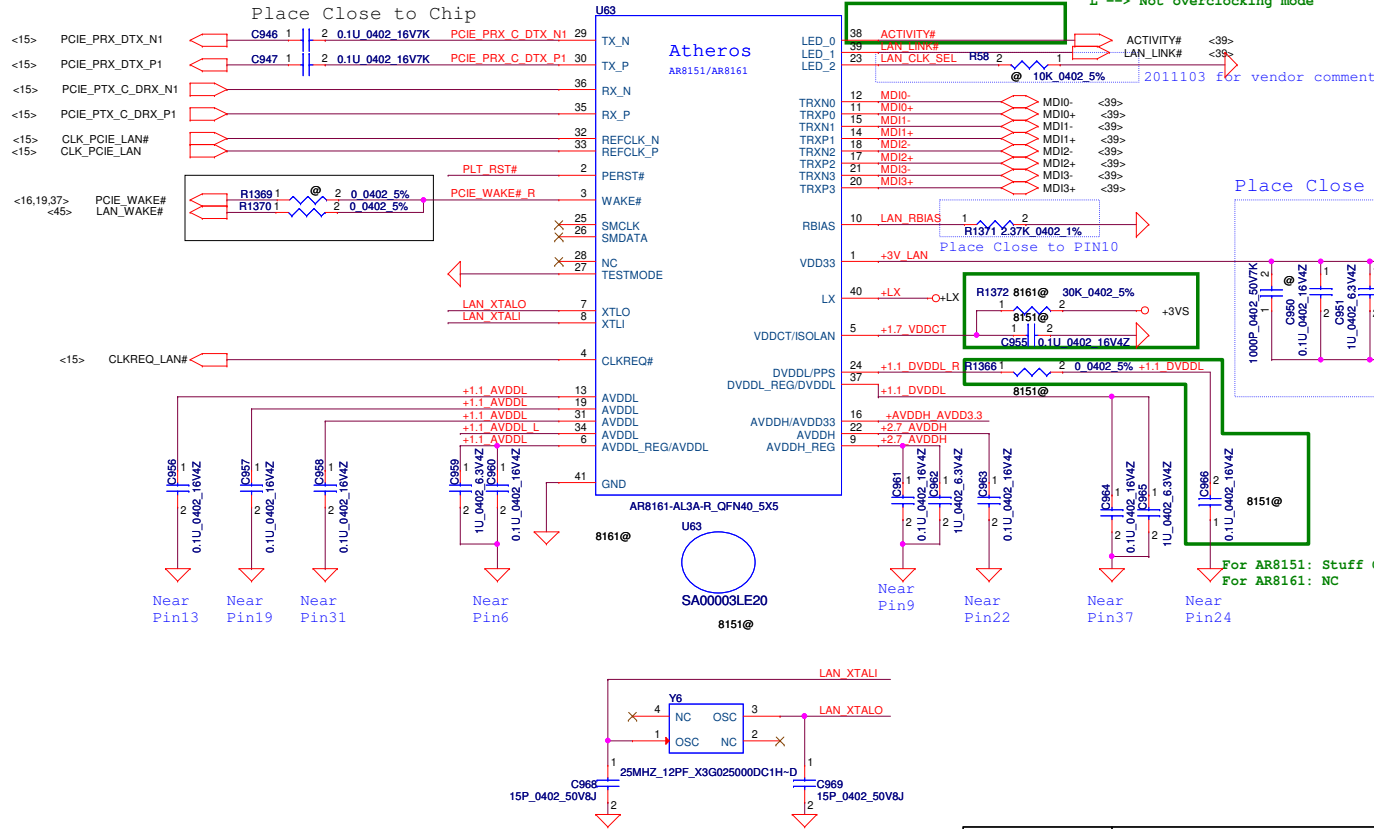
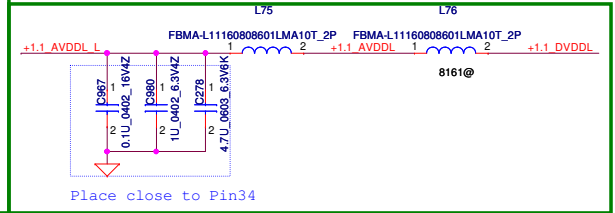
Layout Notice : Place as close chip as possible.



Vendor recommend reseve the
PU resistor close LAN chip

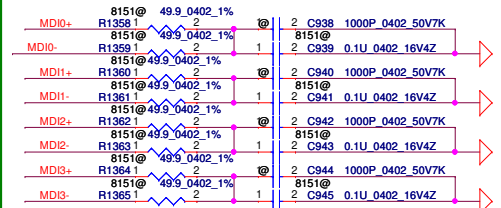


	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76



```
H --> Overclocking mode
L --> Not overclocking mode
```

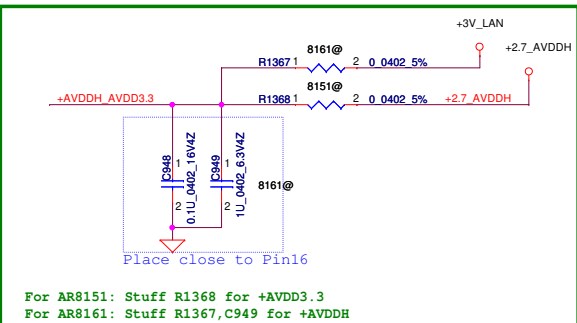
Place Close to PIN1



Note : C938, C940, C942, 944, reserved for EMI.

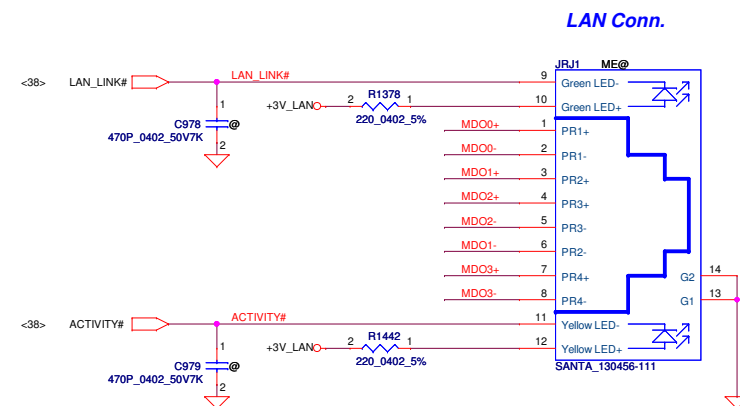
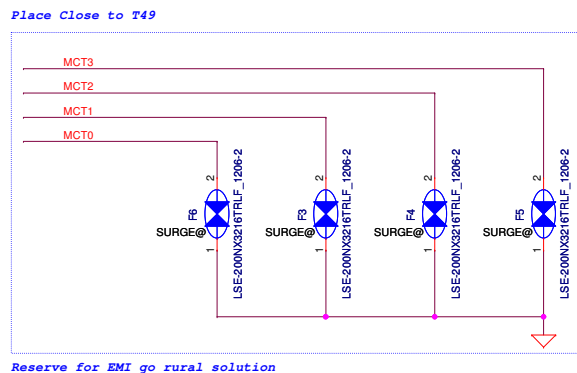
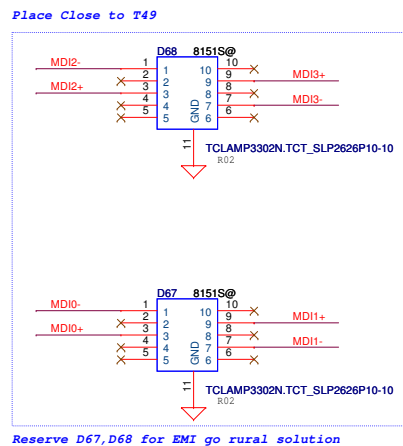
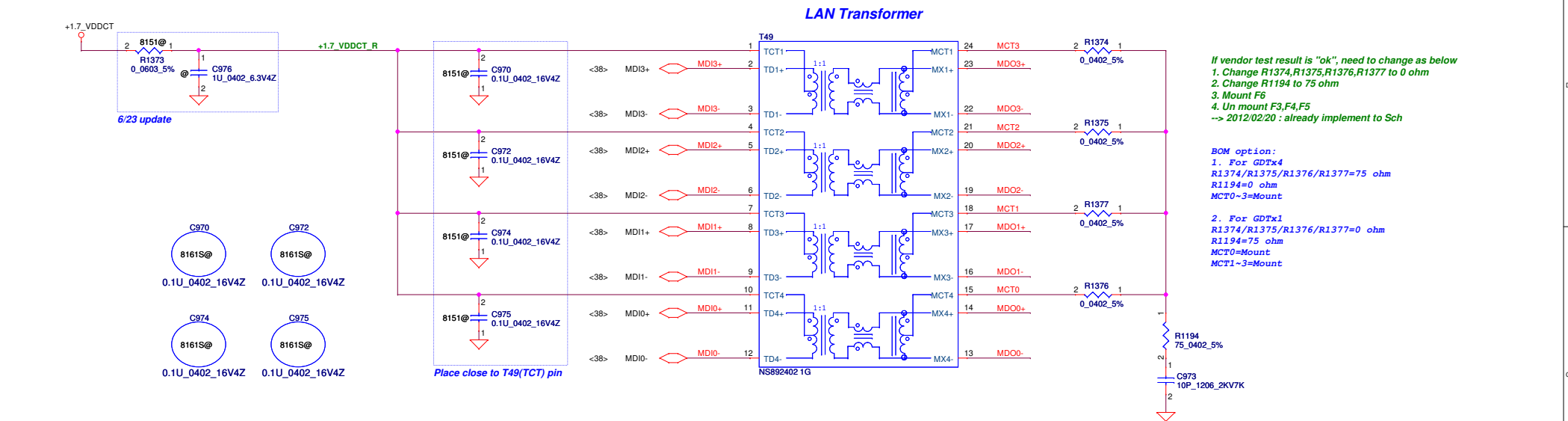
For AR8151: Stuff 49.9K and 0.1u

For AR8161: NC

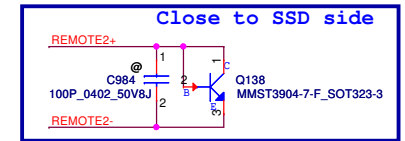
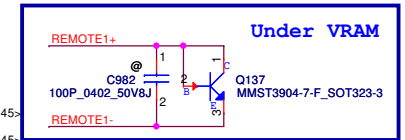
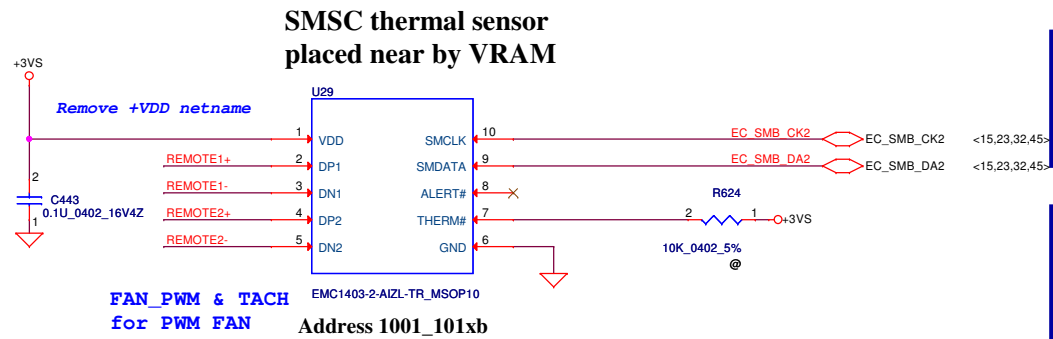
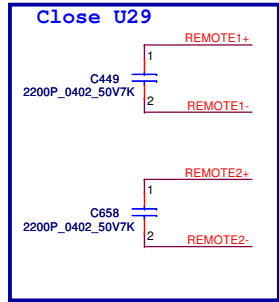


```
For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367,C949 for +AVD
```

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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title LAN-AR8151/8161			
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				Date:	Tuesday, March 20, 2012	Sheet	38 of 65



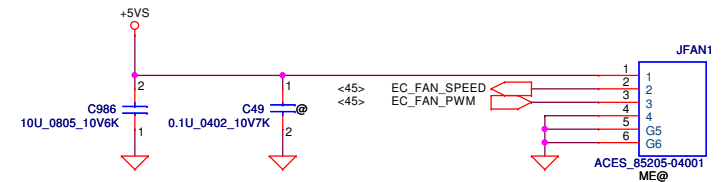
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/11/01				Title			
Deciphered Date				2012/12/31				LAN Transformer			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number				Y490-LA8691P			
Date				Tuesday, March 20, 2012				Rev			
Sheet				39				0.2			



internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

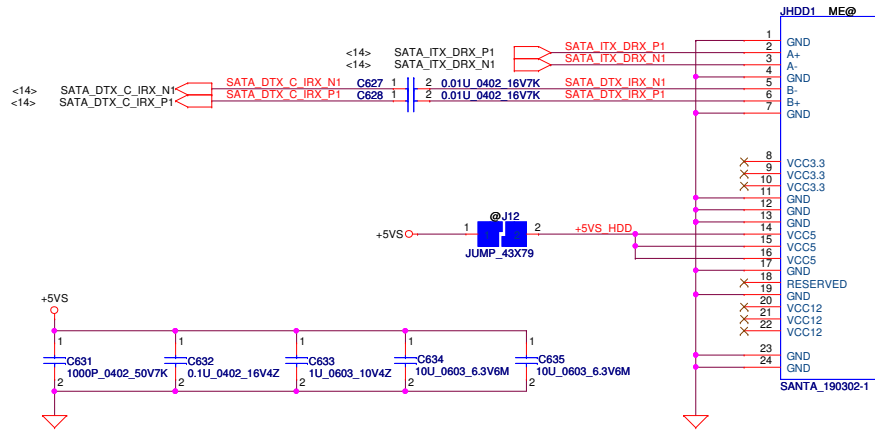
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

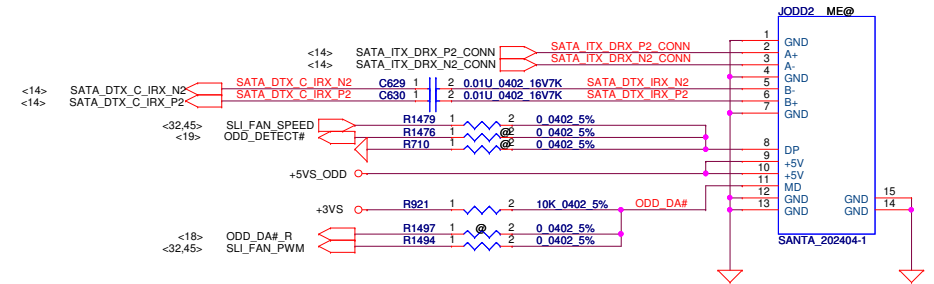


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Size	Custom	Document Number	Y490-LA8691P		Rev
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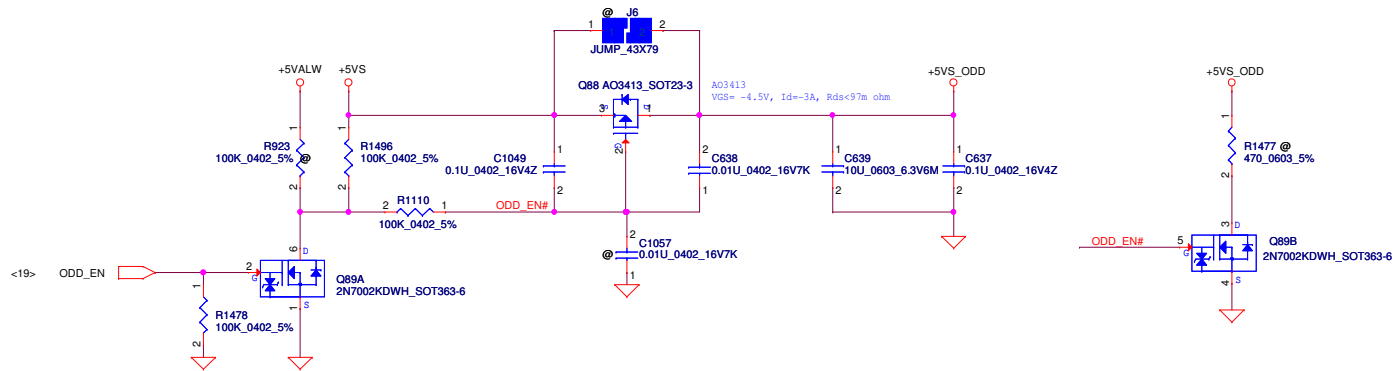
SATA HDD Conn.



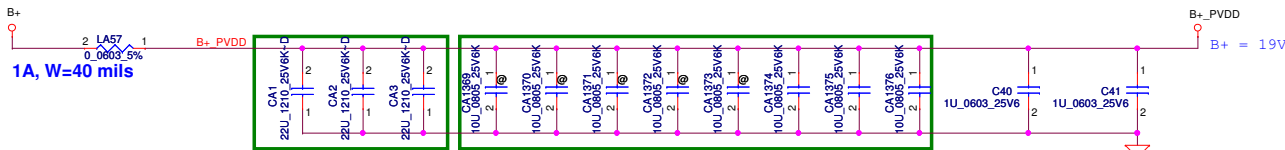
SATA ODD Conn.



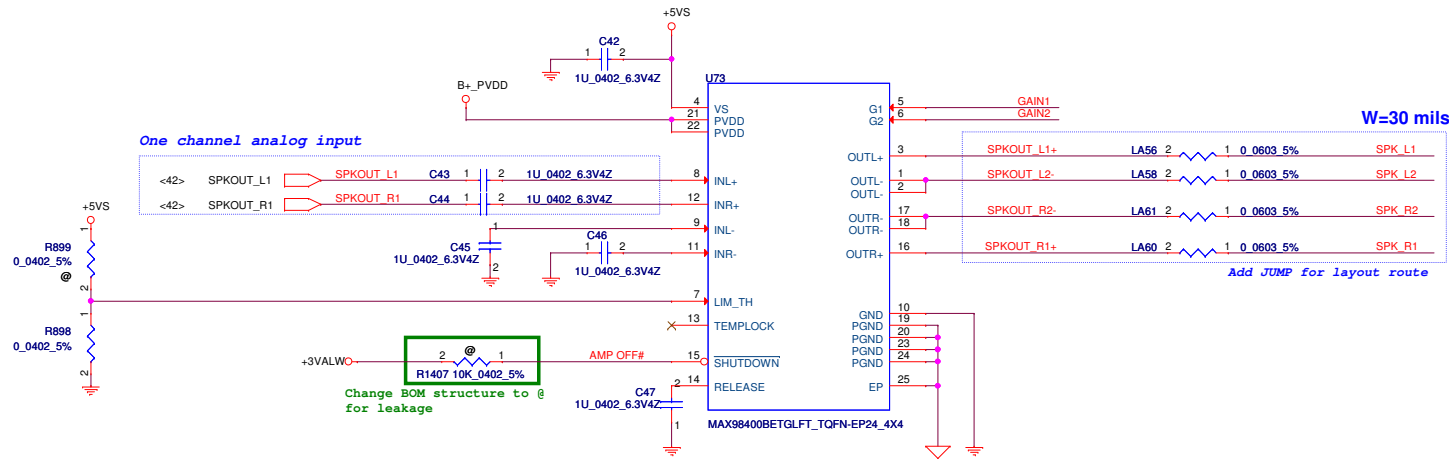
ODD Power Control



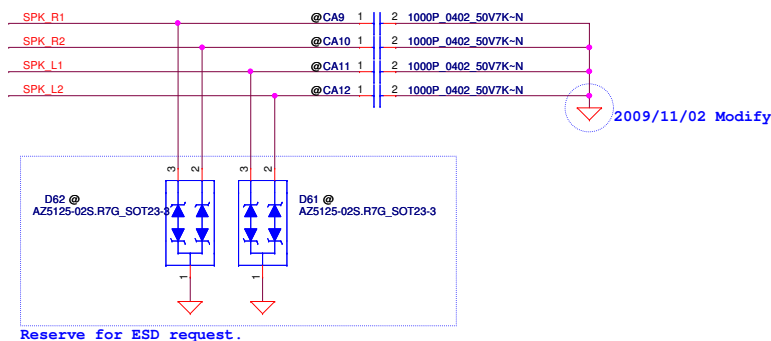
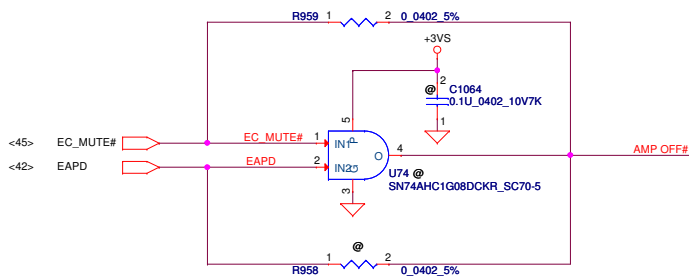
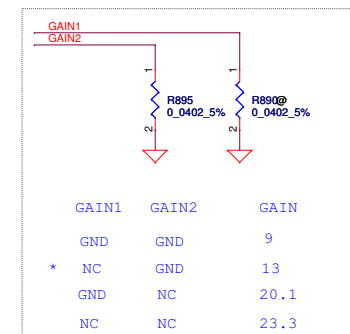
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title
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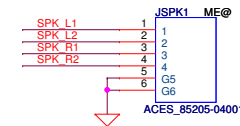
One channel analog input

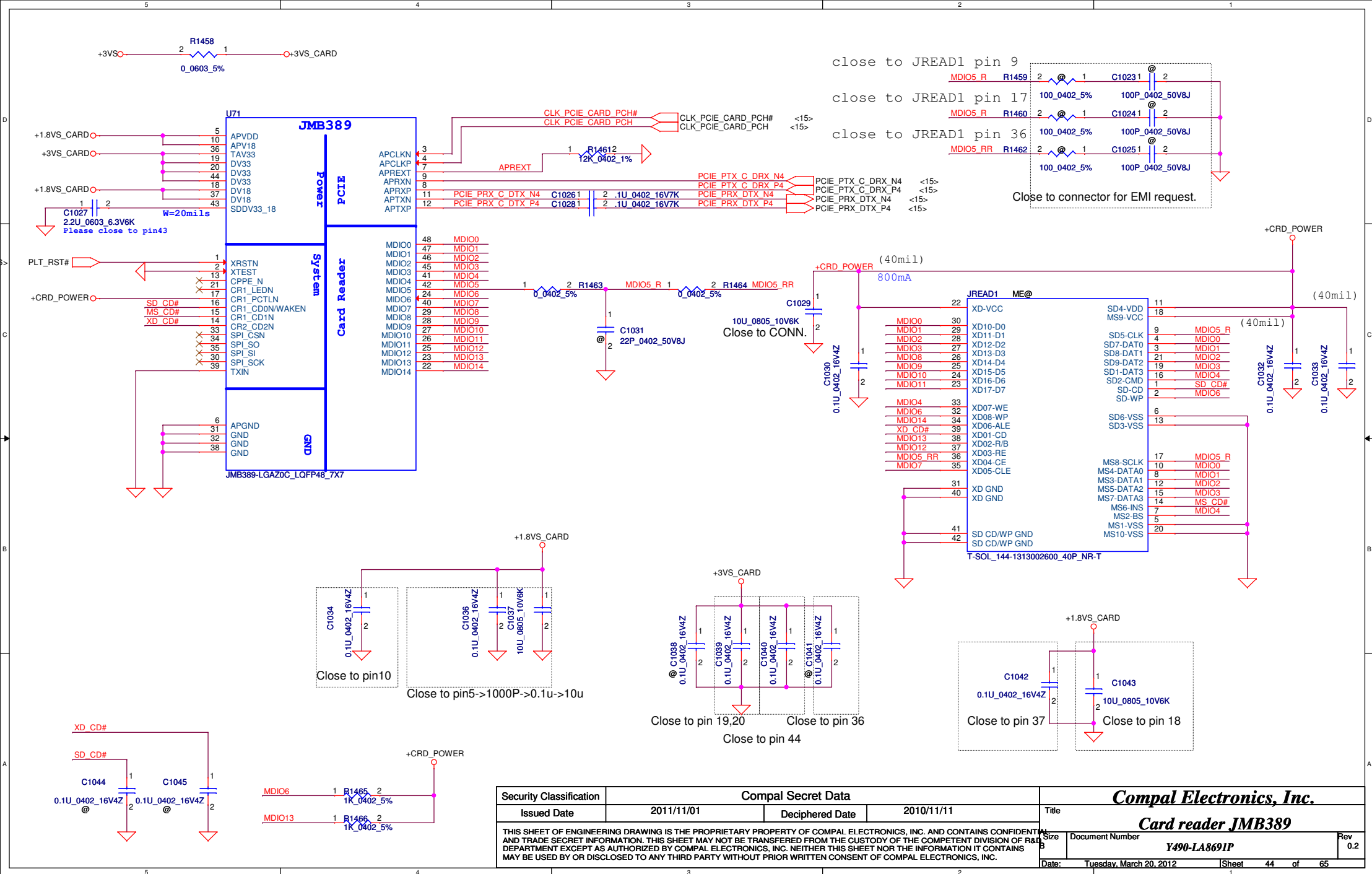


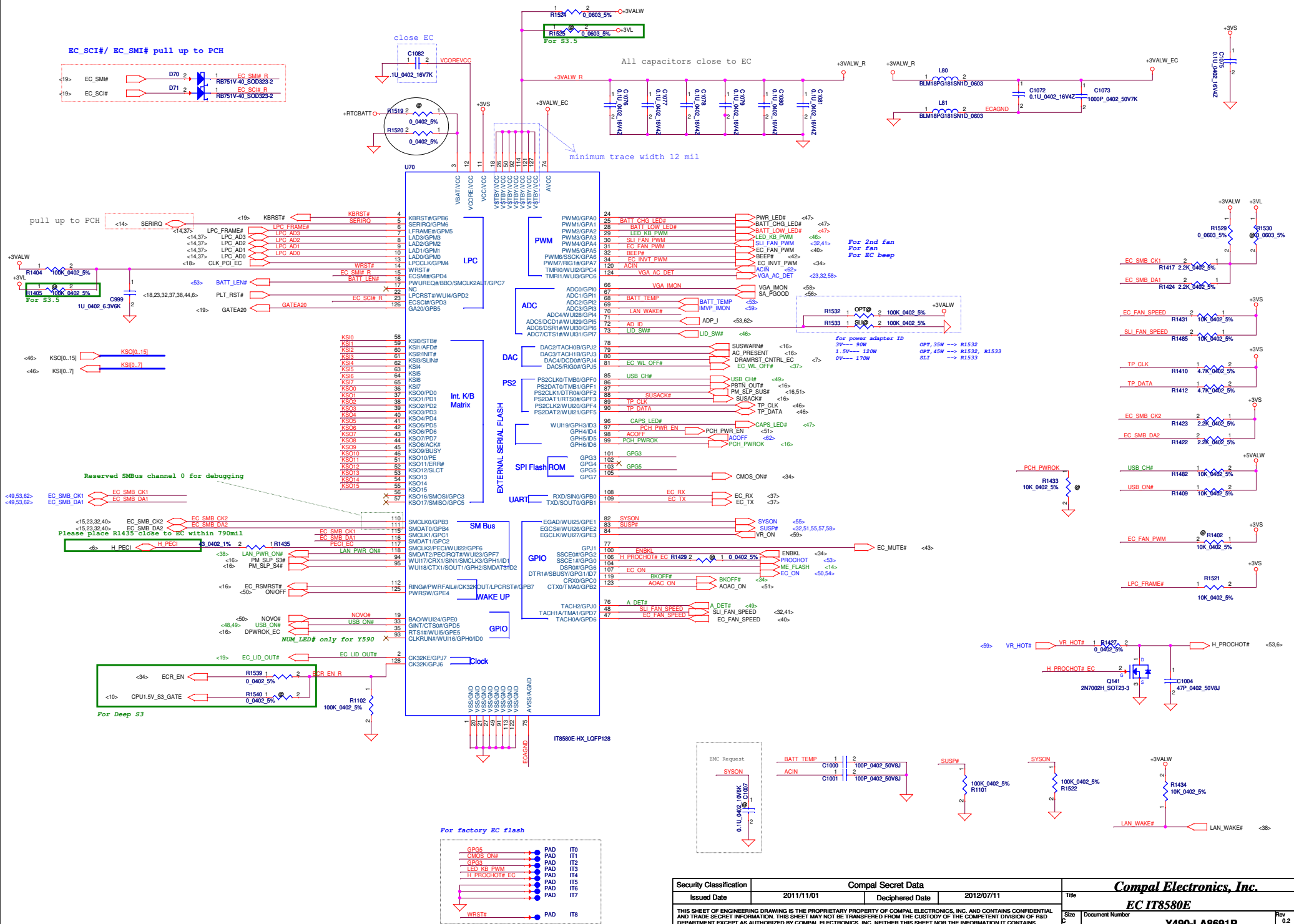
GAIN SETTING



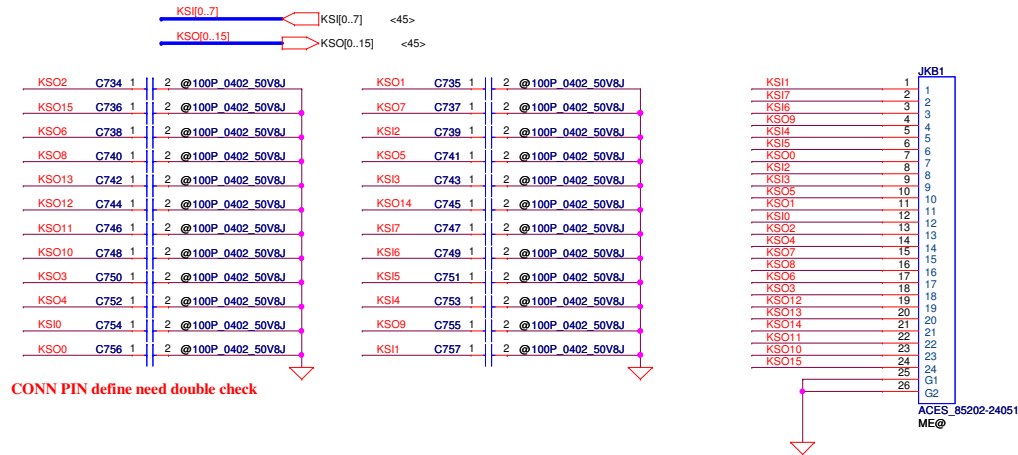
Speaker Conn.



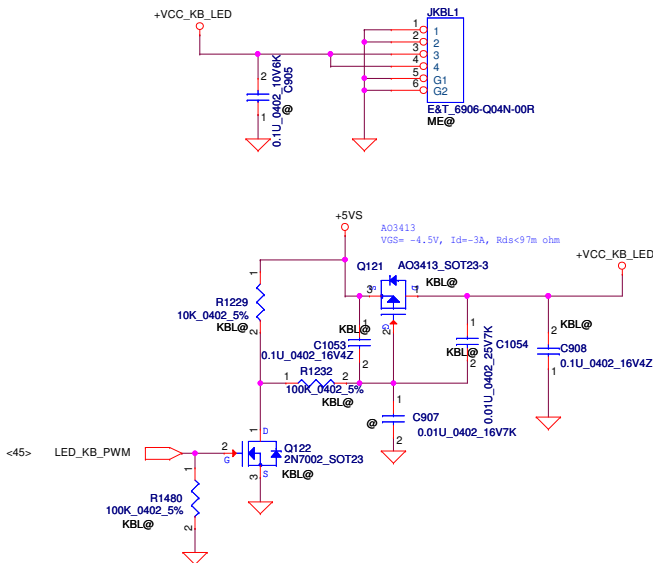




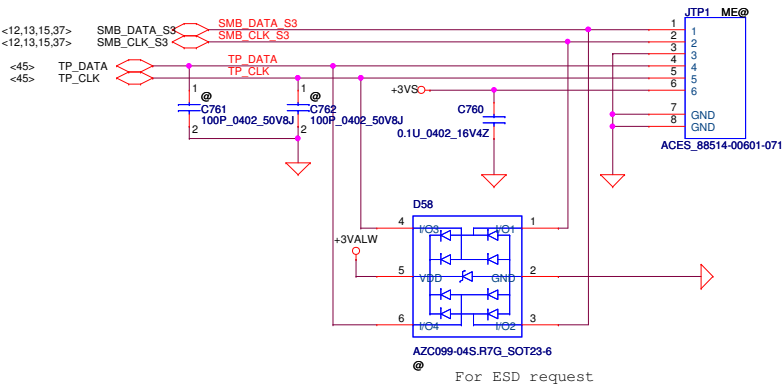
14" INT_KBD Conn.



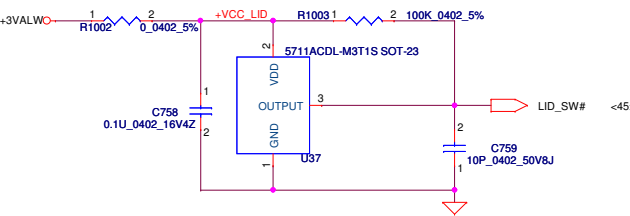
KB Lighting CONN.4pin

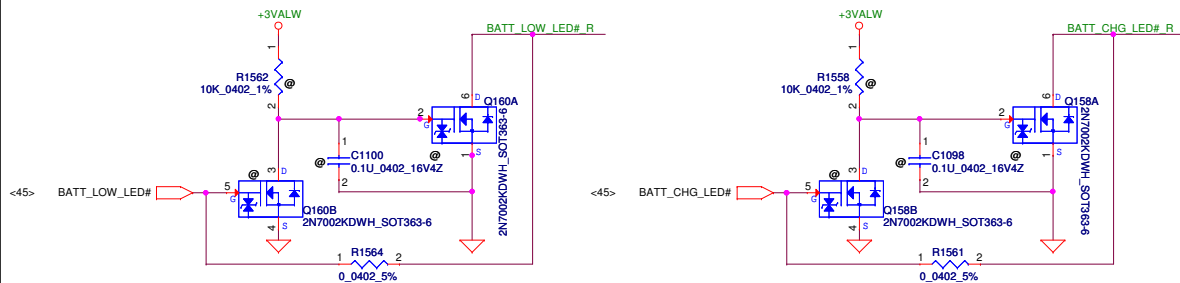


To TP/B Conn.

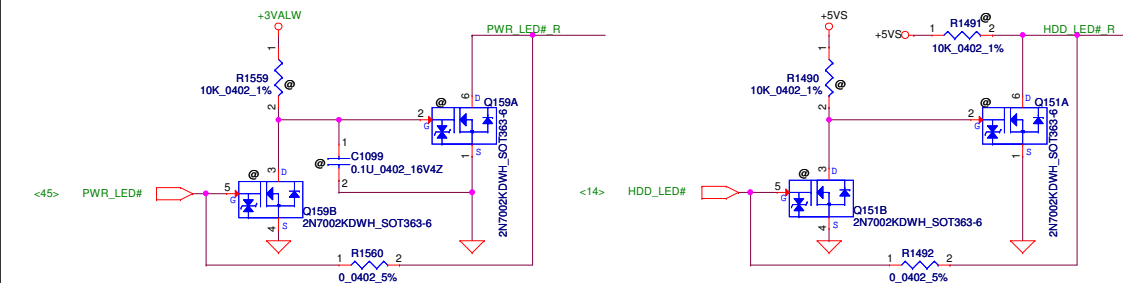
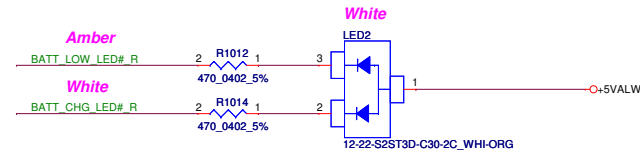


Lid Switch

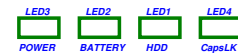
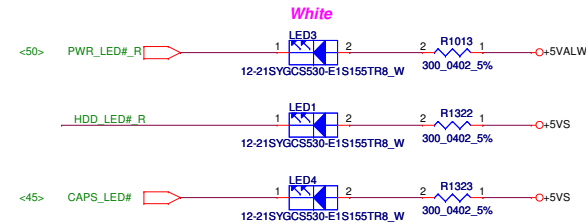




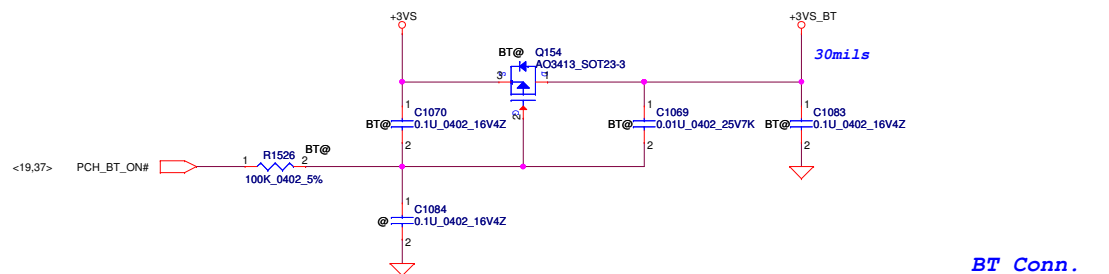
BATT CHARGE/LOW LED



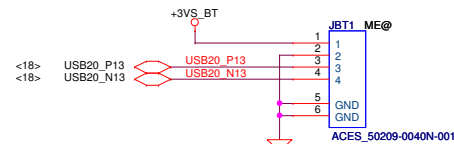
PWR LED HDD LED CapsLK LED



BlueTooth DC



BT Conn.



PCB Fedcal Mark PAD



Screw Hole

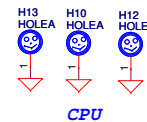
CPU and GPU: H_3P8X 6

C: H_3P8X 3

B: H_3P8X 3

MIN PCIE: H_3P3 X 1

E: H_3P3X 1

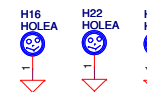


CPU

GPU

ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

A: H_2P8X 8



E: H_3P3X 1

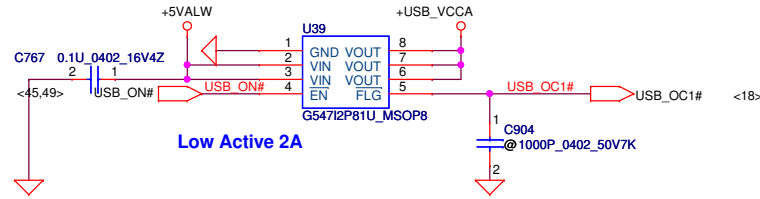
H_4P0X3P0NX 3

H_2P0X 2



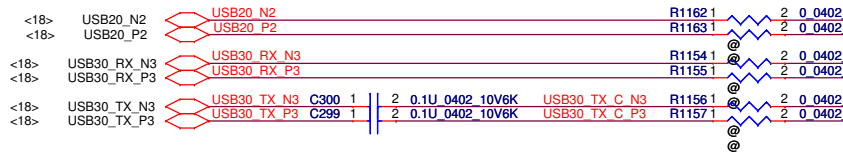
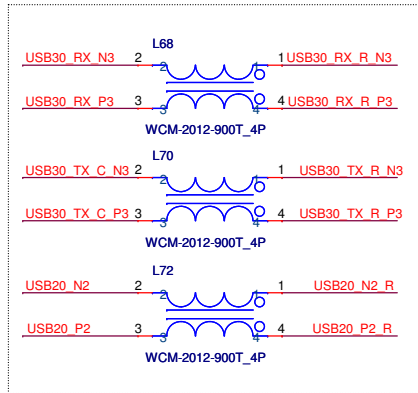
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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	
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LEFT SIDE USB3.0 PORT X1

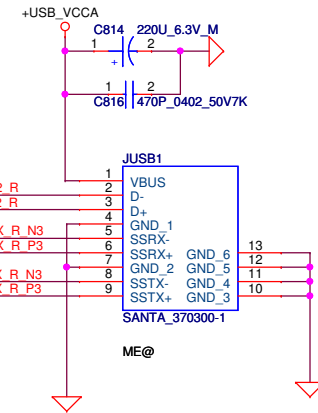
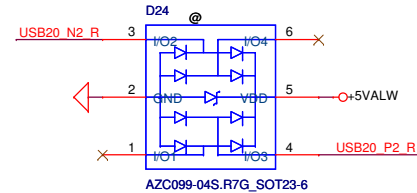
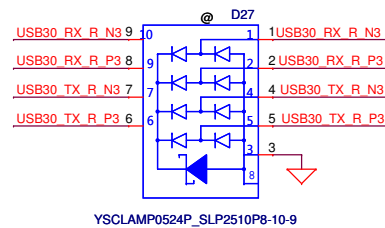


Low Active 2A

For EMI request
USB2.0 choke --> SM070000I00
USB3.0 Choke --> SM070001U00



For ESD request



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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	USB3.0 ports
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Right side USB Charger Port (USB_Port5, near JM1C1)



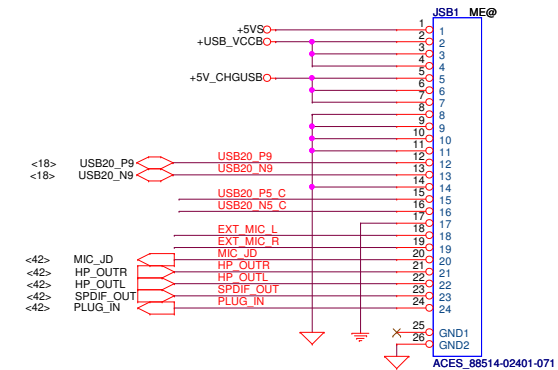
ILIM SETTING

SEL Pin Decode

```

Pull LOW
0R -1010_000
★ 10K-1010_000
12K-1010_000
15K-1010_000
18K-0110_000
22K-0110_000
27K-0110_000
33K-0110_000

```

AUDIO/B Conn.

need change to 無錫 material
COMPAL : SP010015W1J
Footprint : 88514-0240N-071

EXT. MIC

+MIC1_VREFO_L

Remove Diode (DA1, DA2)

RA1622 2.2K_0402_5%

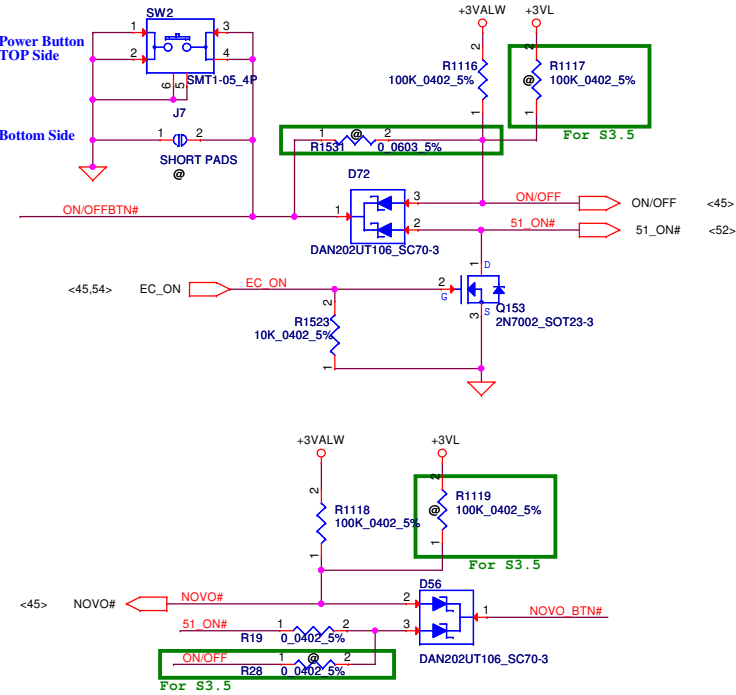
RA1623 2.2K_0402_5%

<42> MIC2_R RA1634 2 1 1K_0402_5% EXT_MIC_R

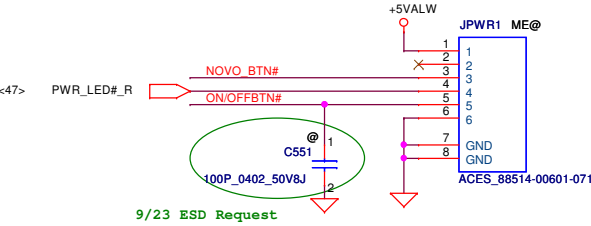
<42> MIC1_R RA1633 2 1 1K_0402_5% EXT_MIC_L

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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	Audio B Conn/USB charger
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ON/OFF switch



Power Button/B link
to Function/B Conn. 10pin

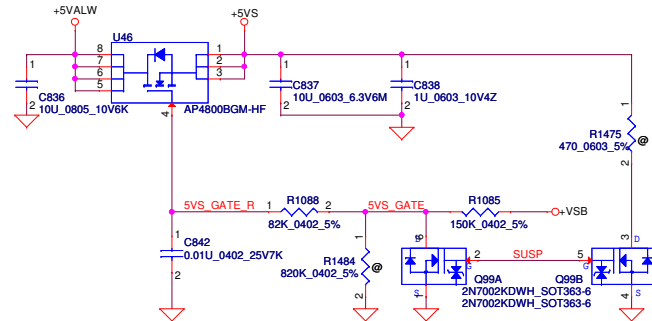


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

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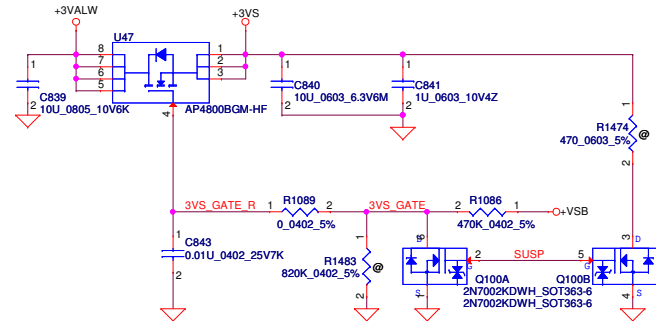
+5VALW to +5VS

AP4800BGM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V

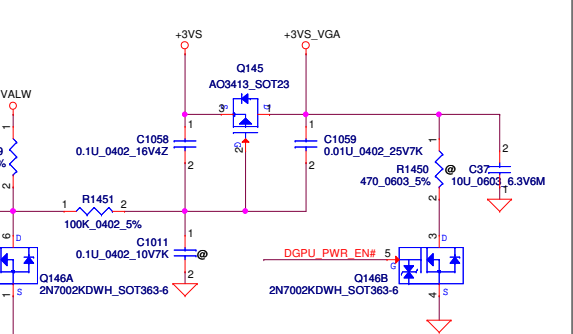
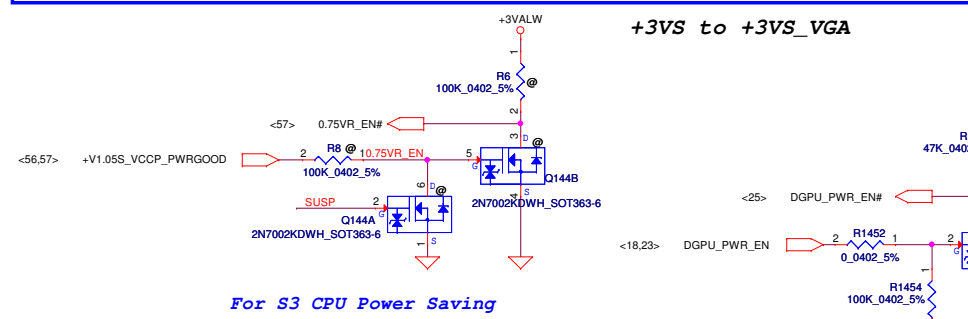
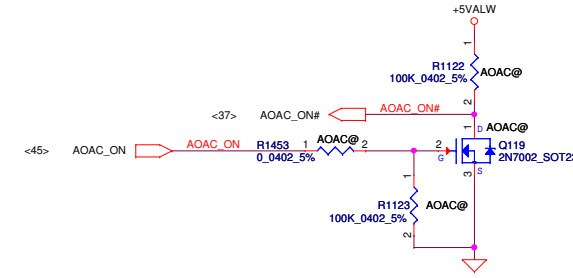
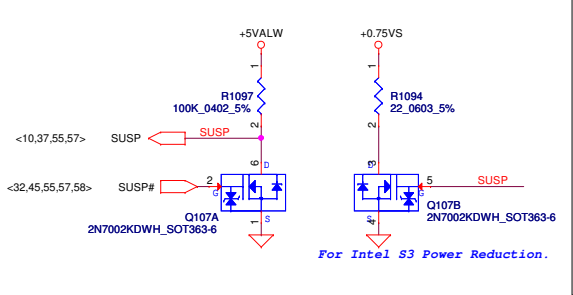
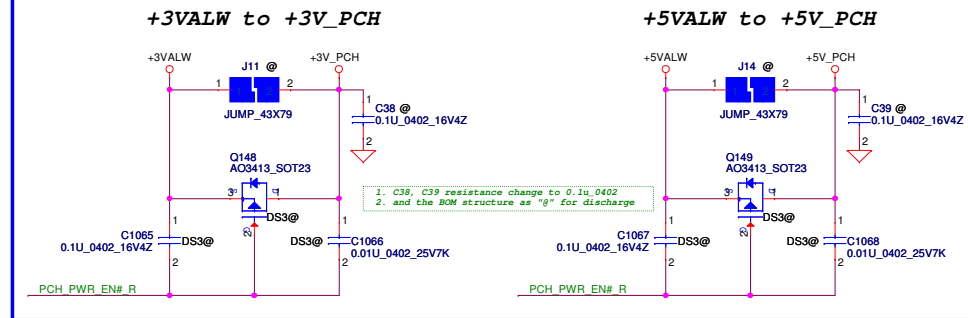
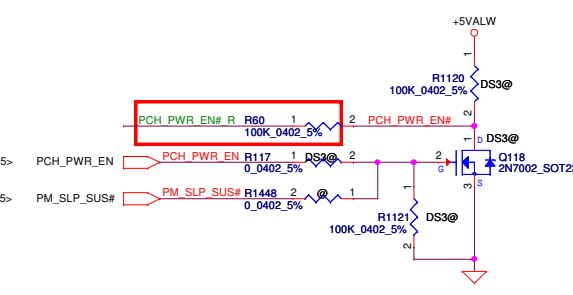
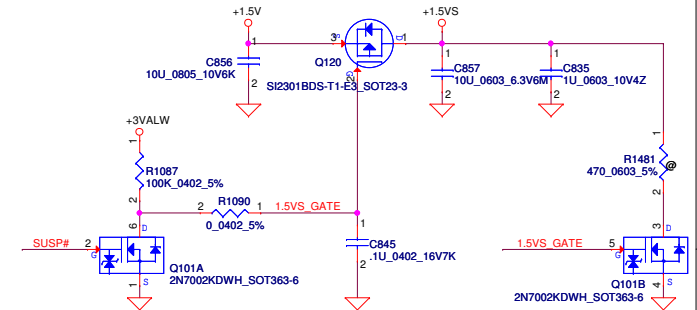


+3VALW to +3VS

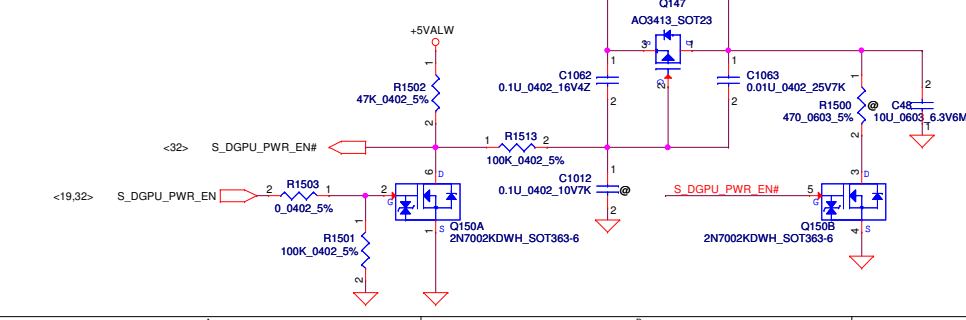
AP4800BGM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V



+1.5V to +1.5VS

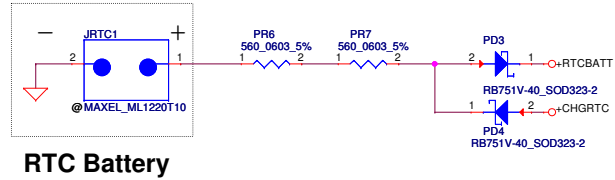
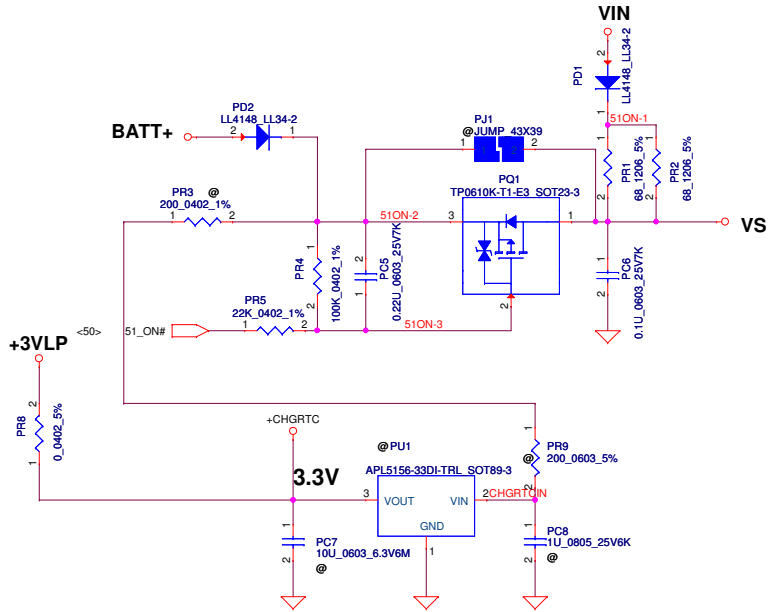
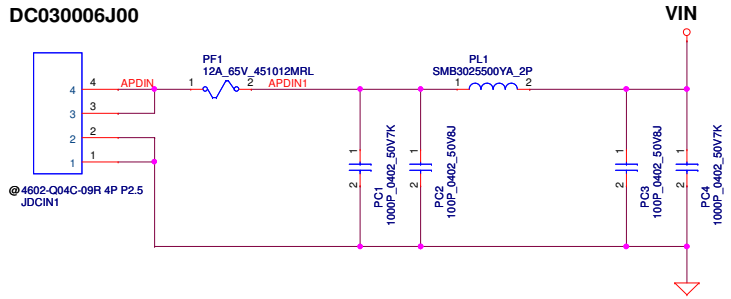


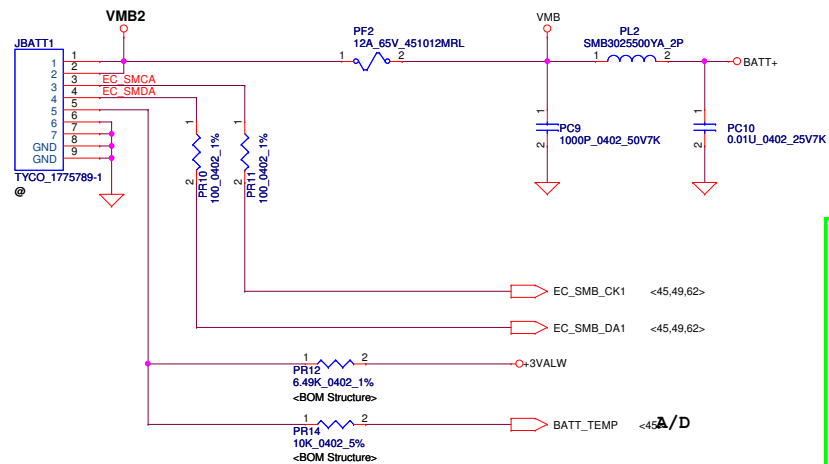
+3VS to +3VS_SLI



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DC030006J00

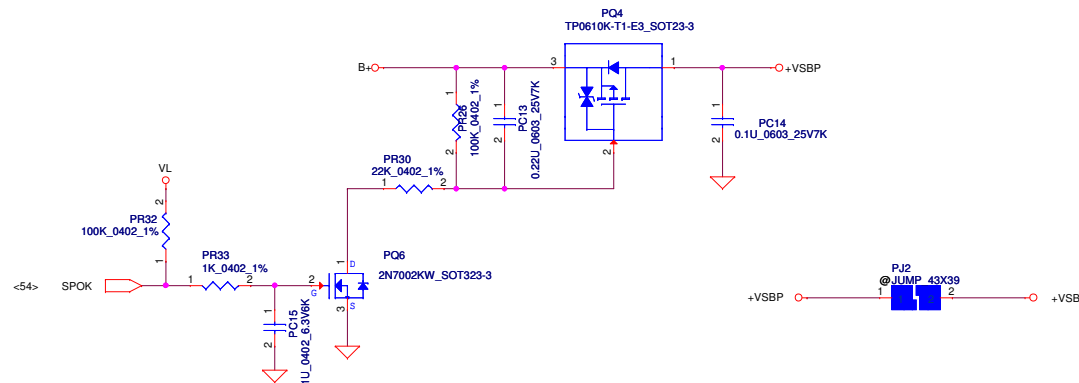
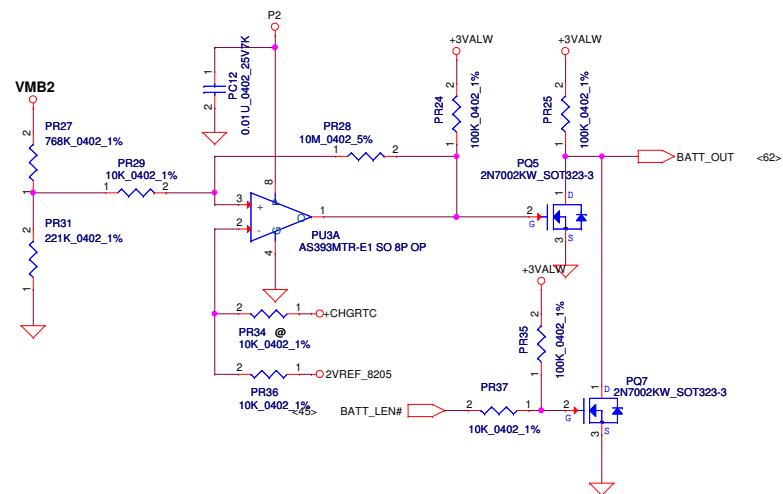
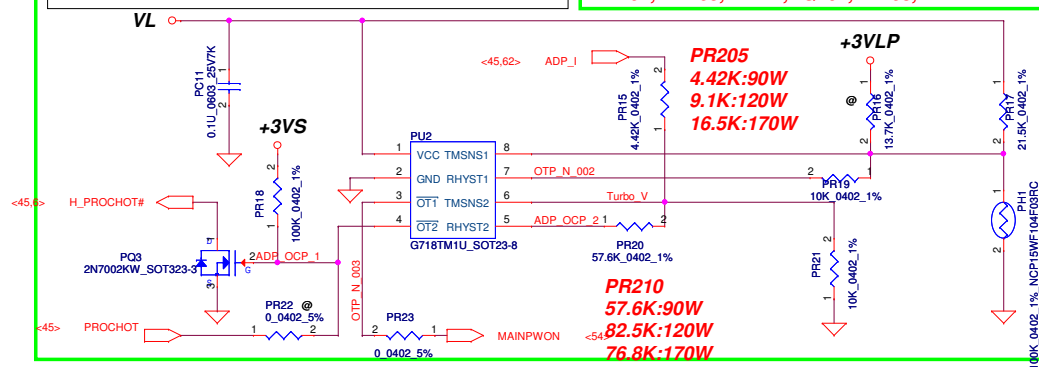




PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +/-3 degree C

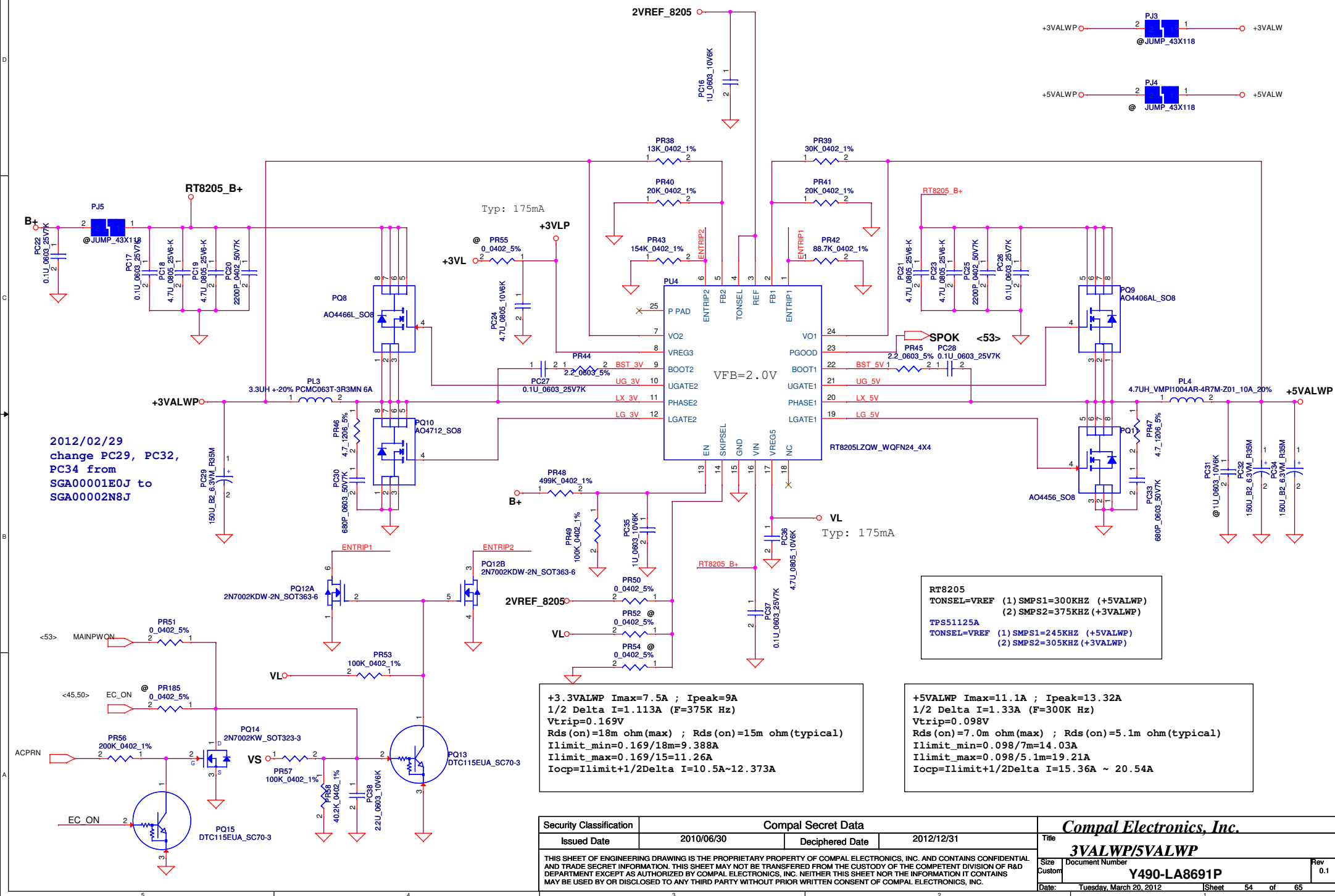
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 (Red square) --> Remove PU1 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



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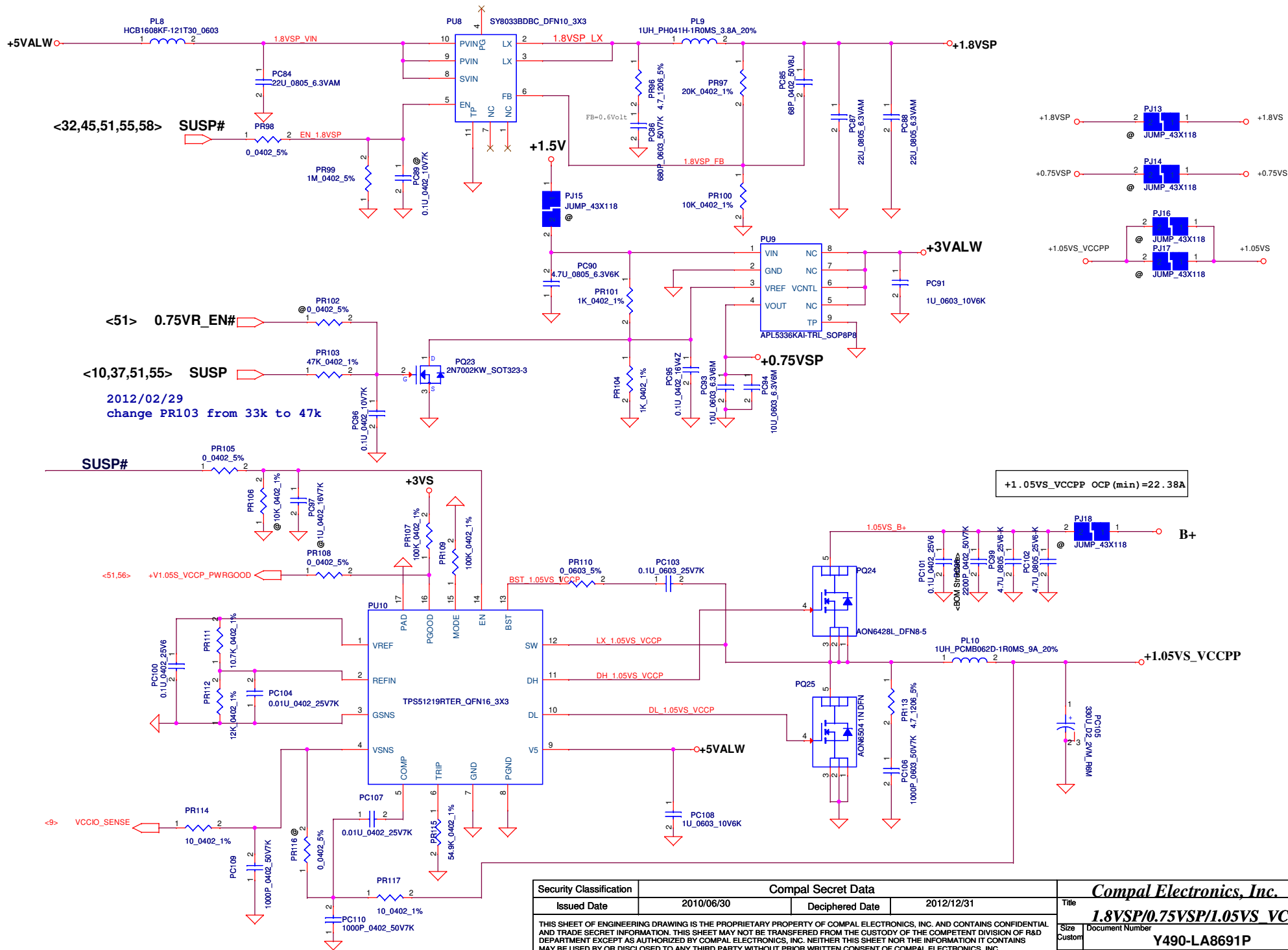
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



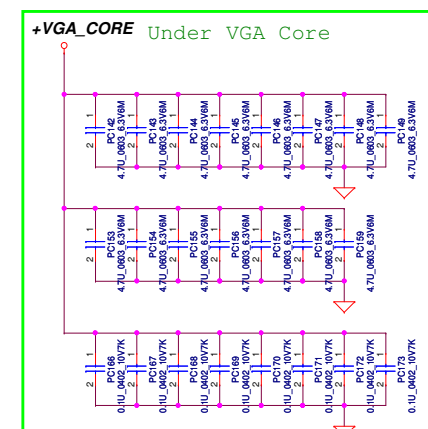
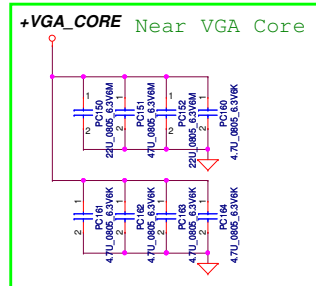
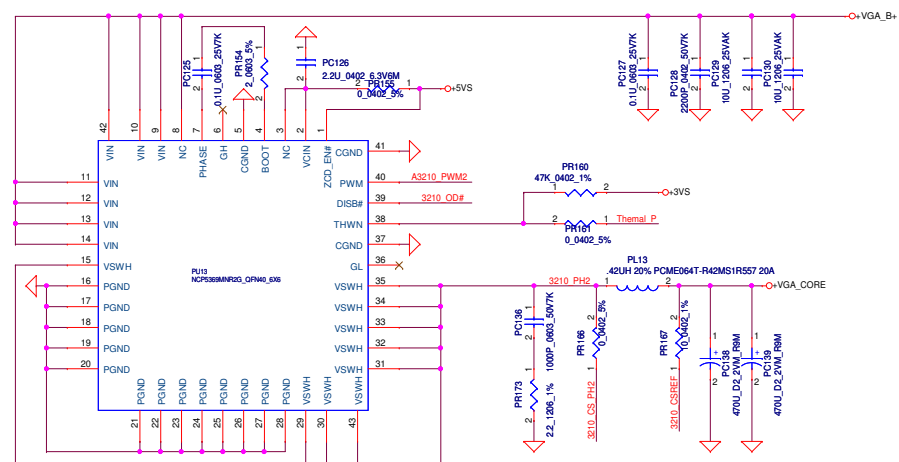
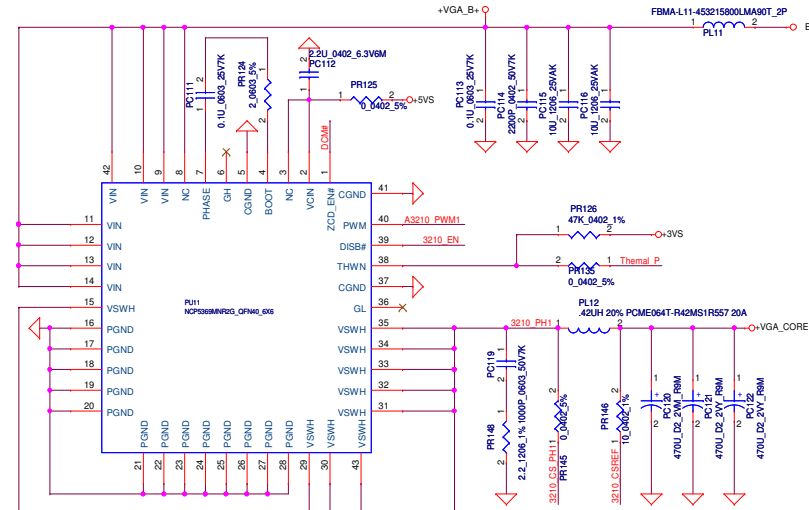
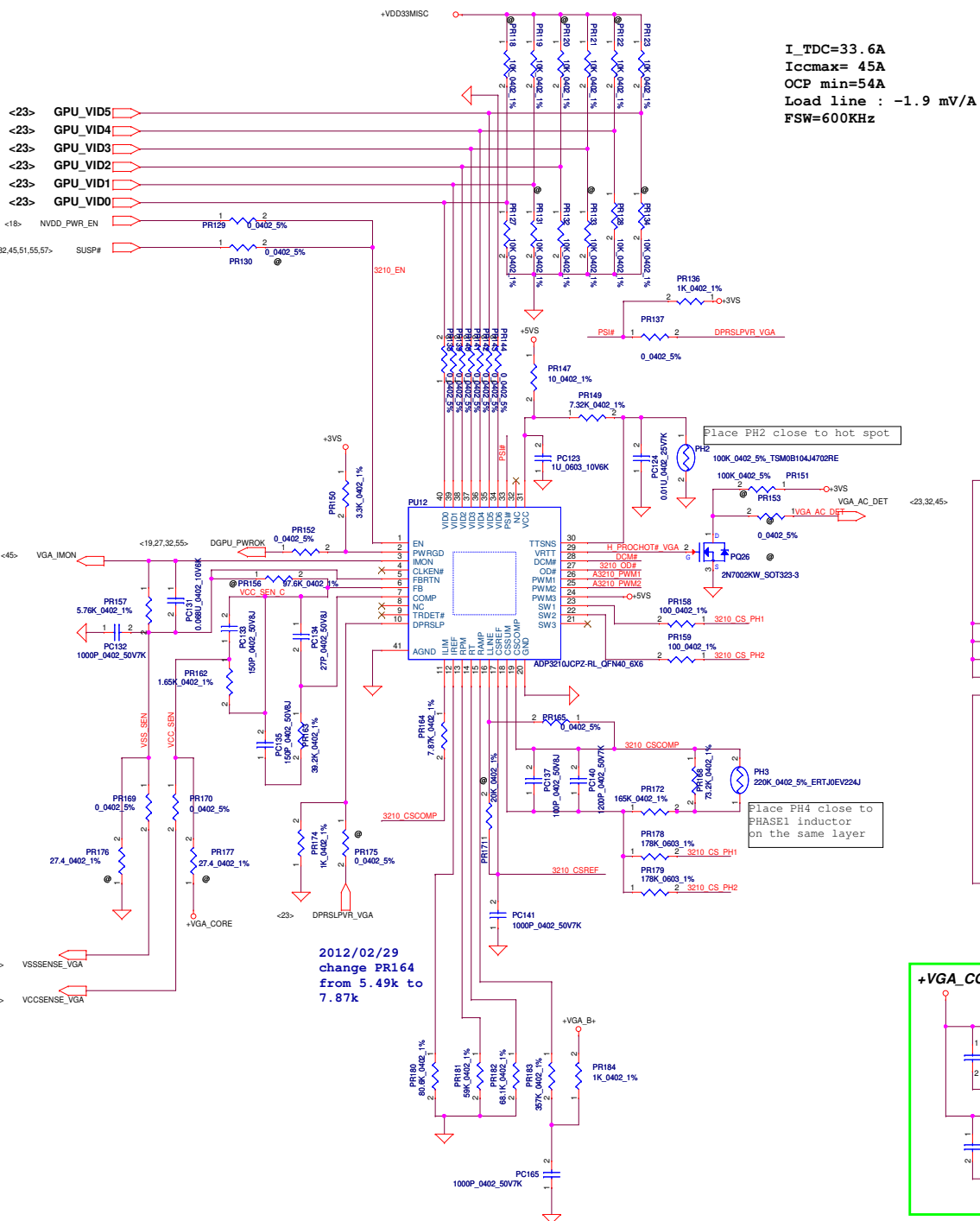
$I_{ocp}=13.58A\sim 23.10A$



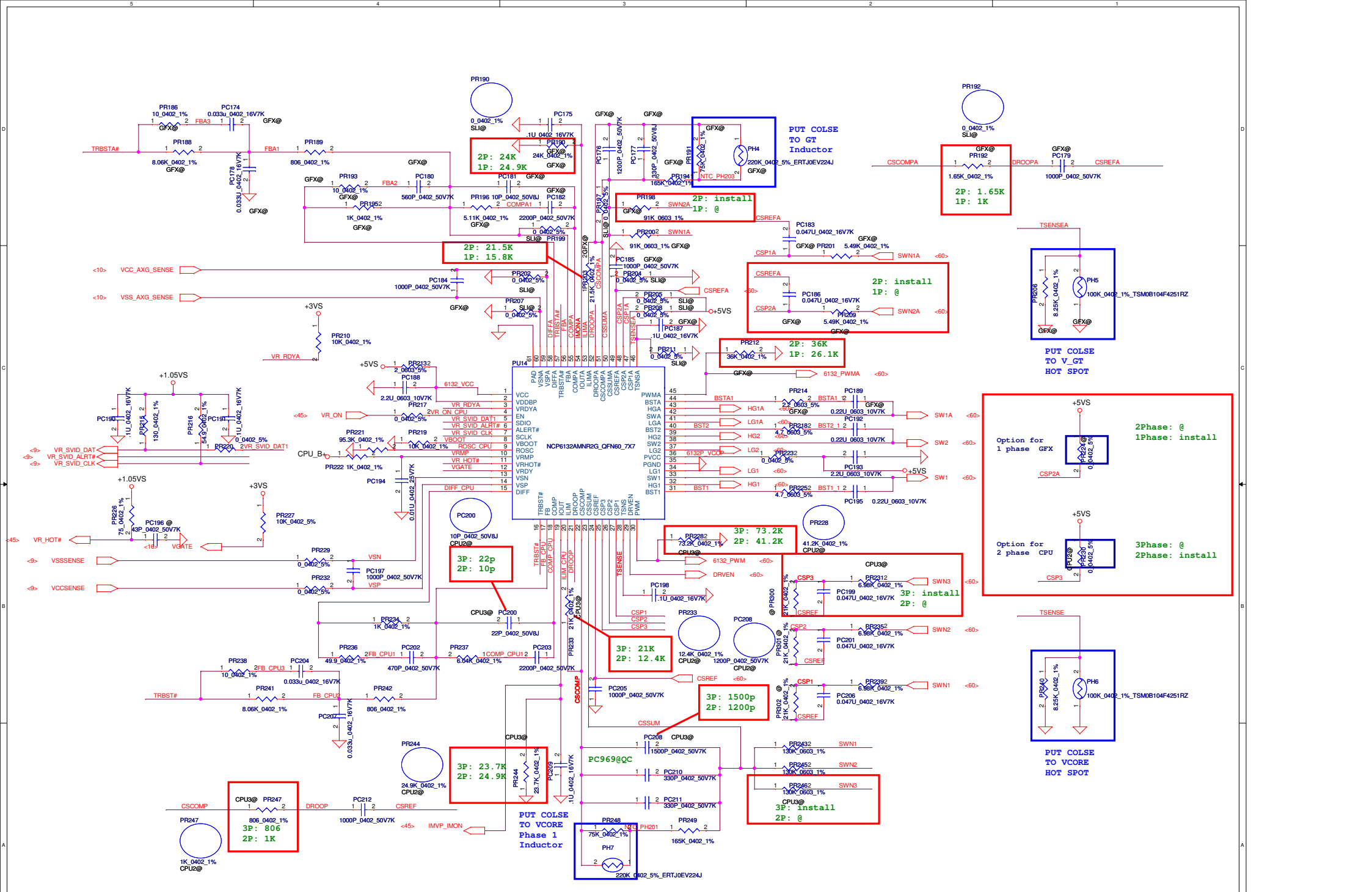
Date: Tuesday, March 20, 2012		Sheet 55 of 65	
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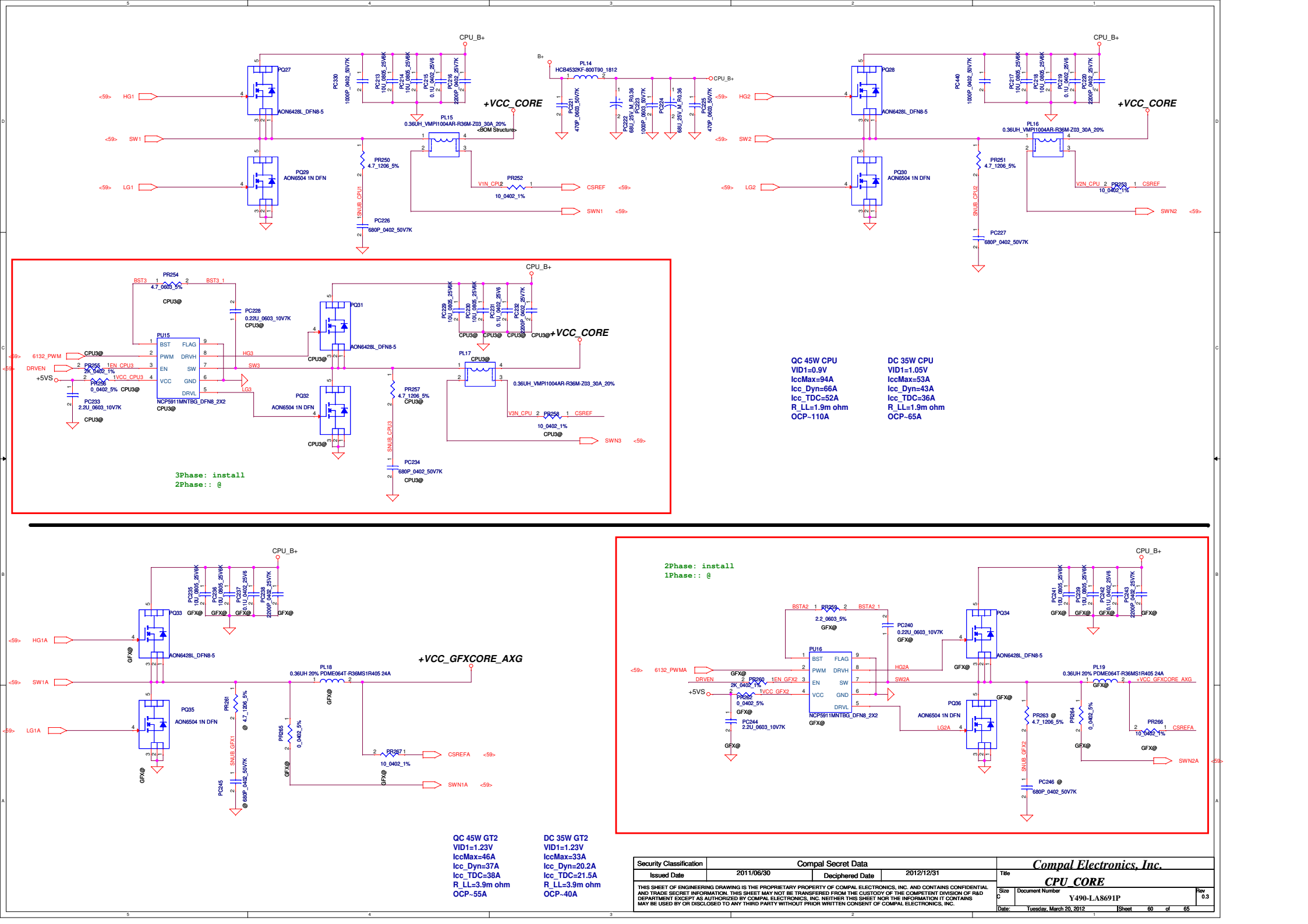


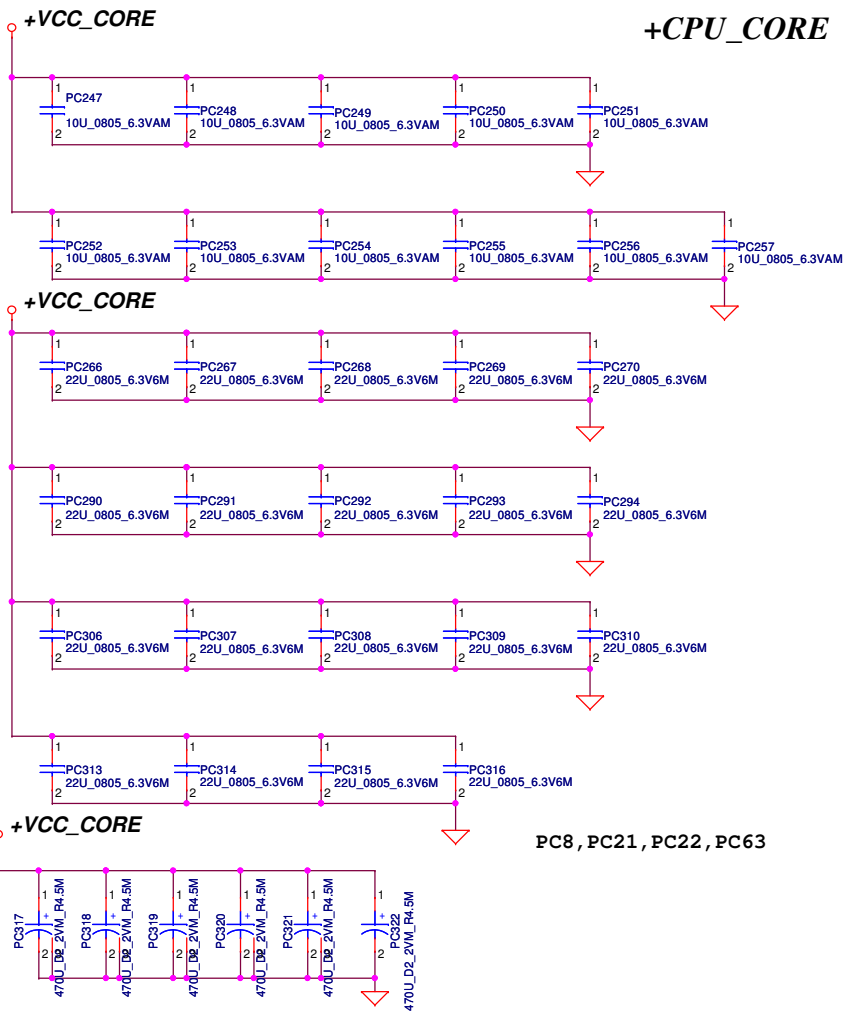
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title	1.8VSP/0.75VSP/1.05VS_VCCPP
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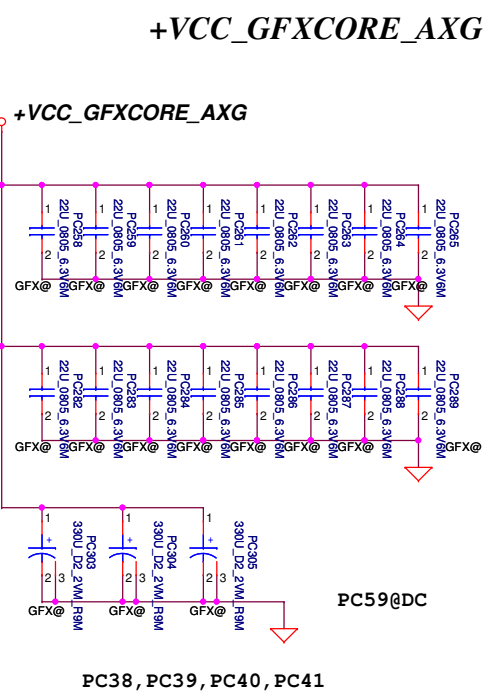






DC: PC73, PC74, PC75, PC76, PC77, PC78 (330uF/9m)
 QC: PC76, PC78 (470uF/4.5m), PC73, PC74, PC75 (330uF/9m)

PC8, PC21, PC22, PC63



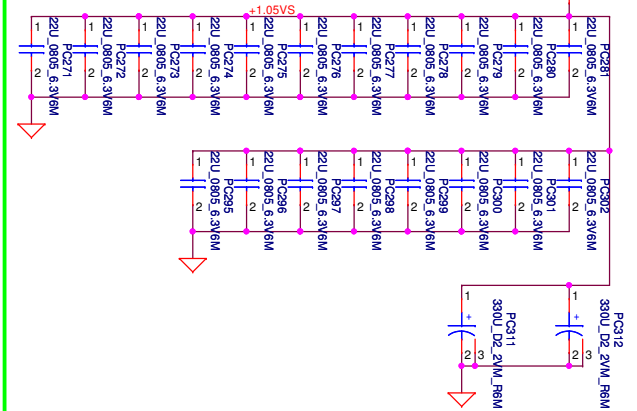
PC38, PC39, PC40, PC41

PC38, PC39, PC40, PC41

Below is 458544_CRV_PDDG_0.5 Table 5-8.

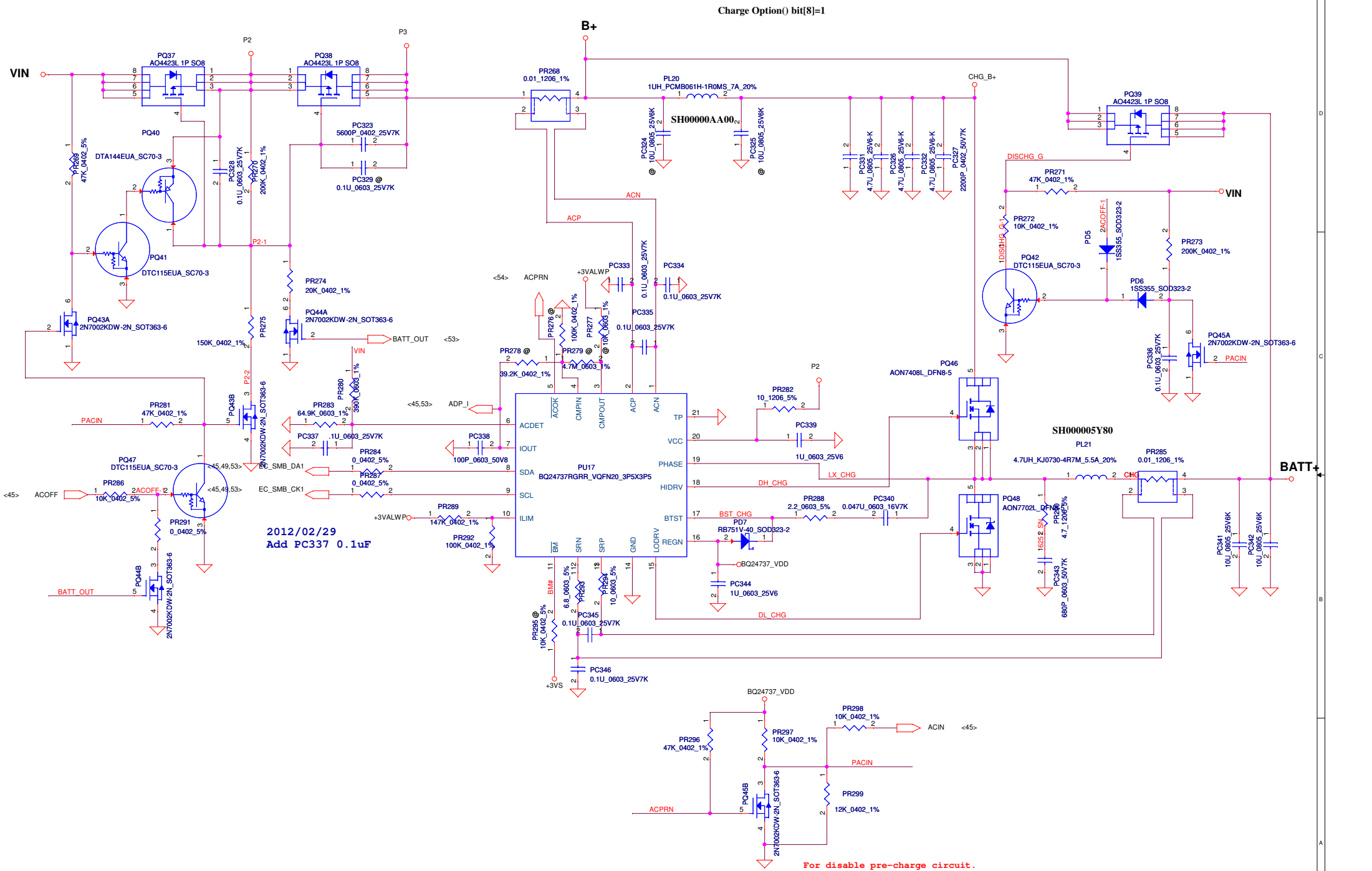
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05VS



PC32, PC49, PC54, PC55, PC56

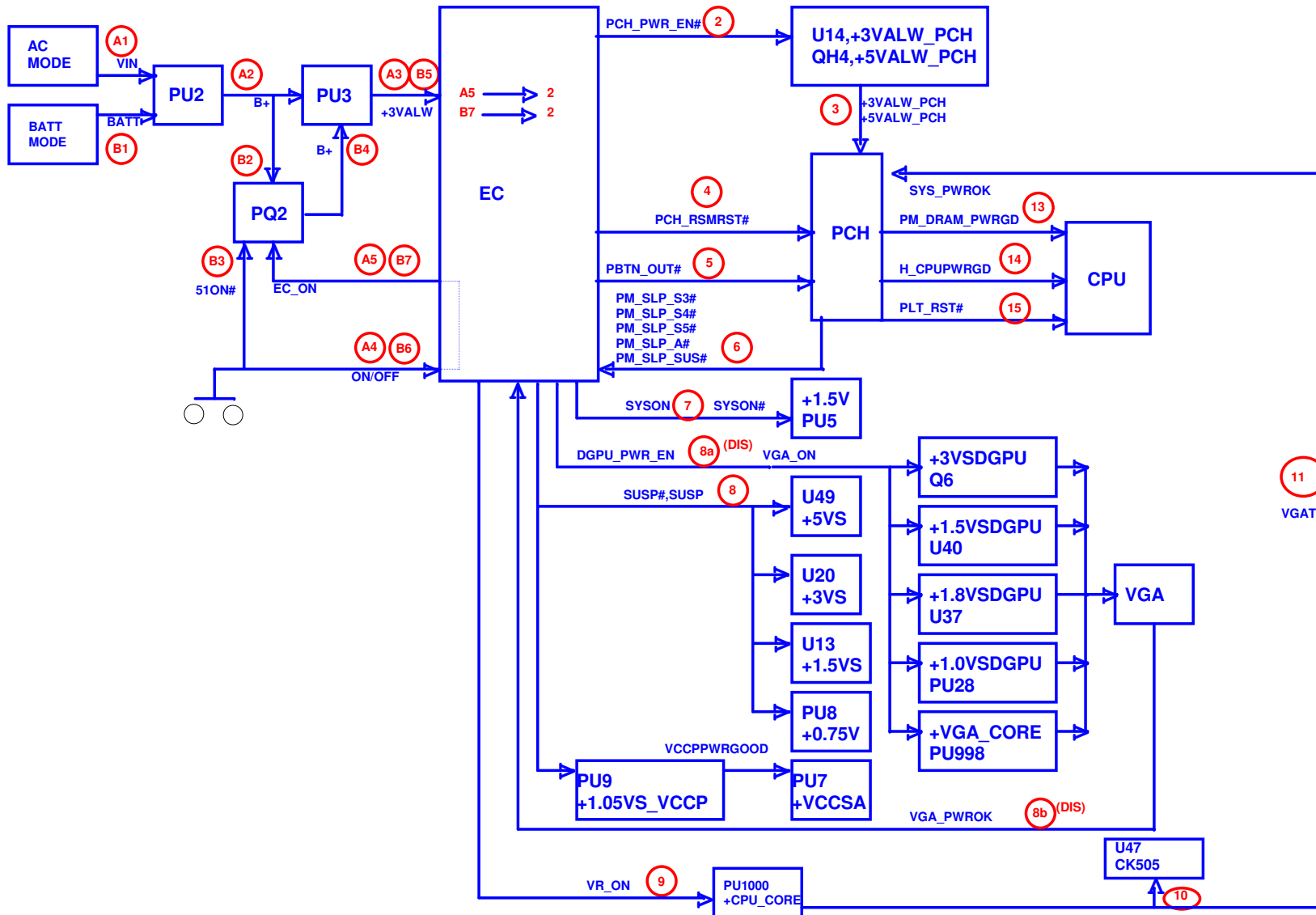
Security Classification		Compal Secret Data		Title	
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2012/02/29
Add PC337 0.1uF

For disable pre-charge circuit.

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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10					
11					
12					
13					
14					
15					
16					
17					

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HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "a" to "DS3a"
				For Deep S3 Function

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				Document Number Rev 0.1	
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