Compal confidential

Schematics Document

Mobile AMD S1G3 CPU with ATI RS880M(NB) & SB710(SB) core logic

2009-08-27

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/03/23	Deciphered Date	2010/03/23

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Title: Cover Sheet			
Size: Custom	Document Number: LA-4961P		Rev: 1.0
Date: Thursday, August 27, 2009	Sheet 1 of 54		

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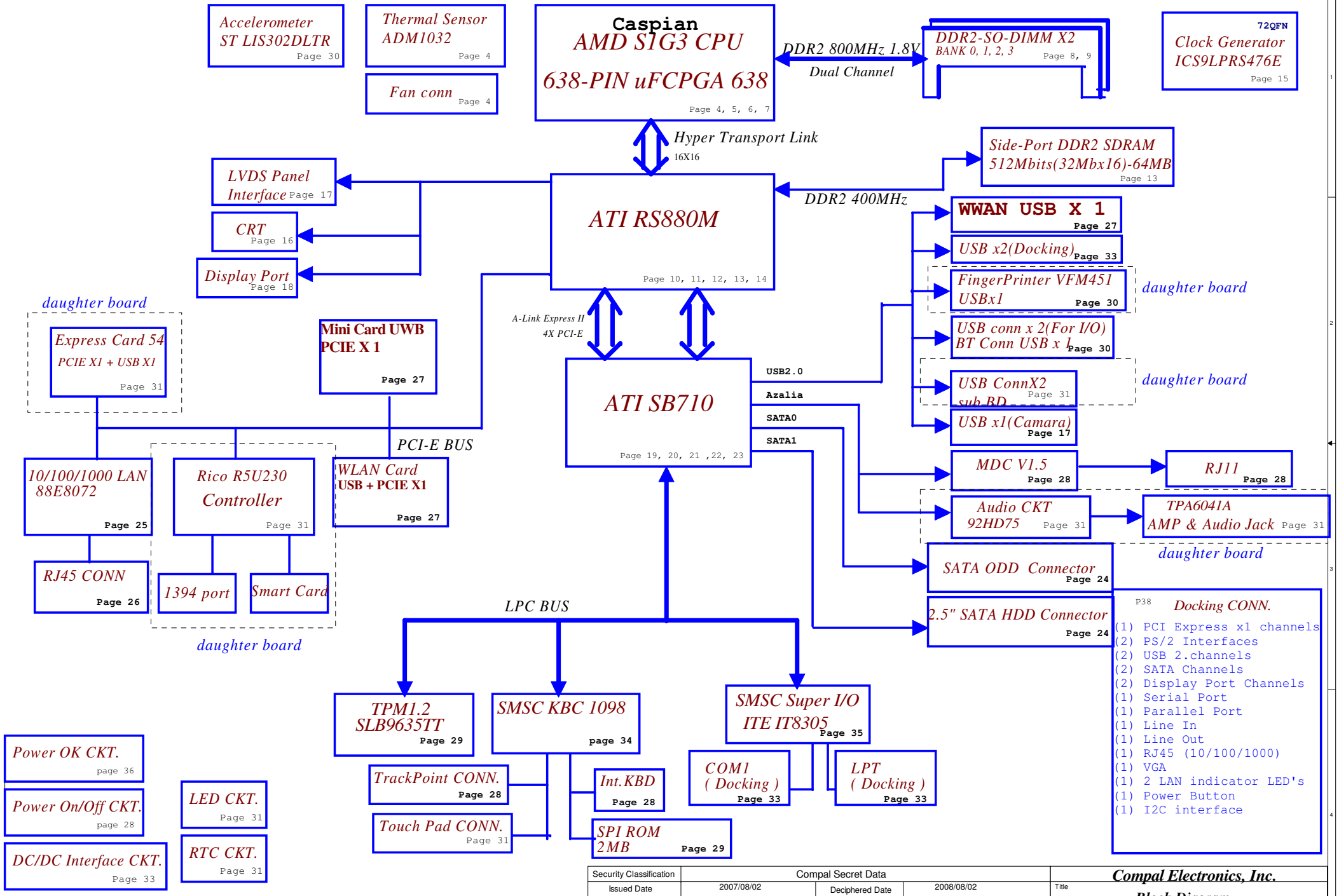
TAG UMA



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Title: Block Diagram

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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B VL +3VL	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +CPU_CORE_0 +2.5VS +1.8VS +NB_VDDC +VDDA11PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

Layout Notes

: Question Area Mark.(Wait check)

"*" as default BOM setting
@ : means just reserve , no build
45@ : Install when 45 level Assy.
CONN@:means ME part

SMBUS Control Table

	SOURCE	INVERTER	BATT	EEPROM SERIAL	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_CK_CLK0 SMB_CK_DAT0	SB710	X	X	X	V	V	X	X	X	X	V
SMB_CK_CLK1 SMB_CK_DAT1	SB710	X	X	X	X	X	X	X	X	X	X

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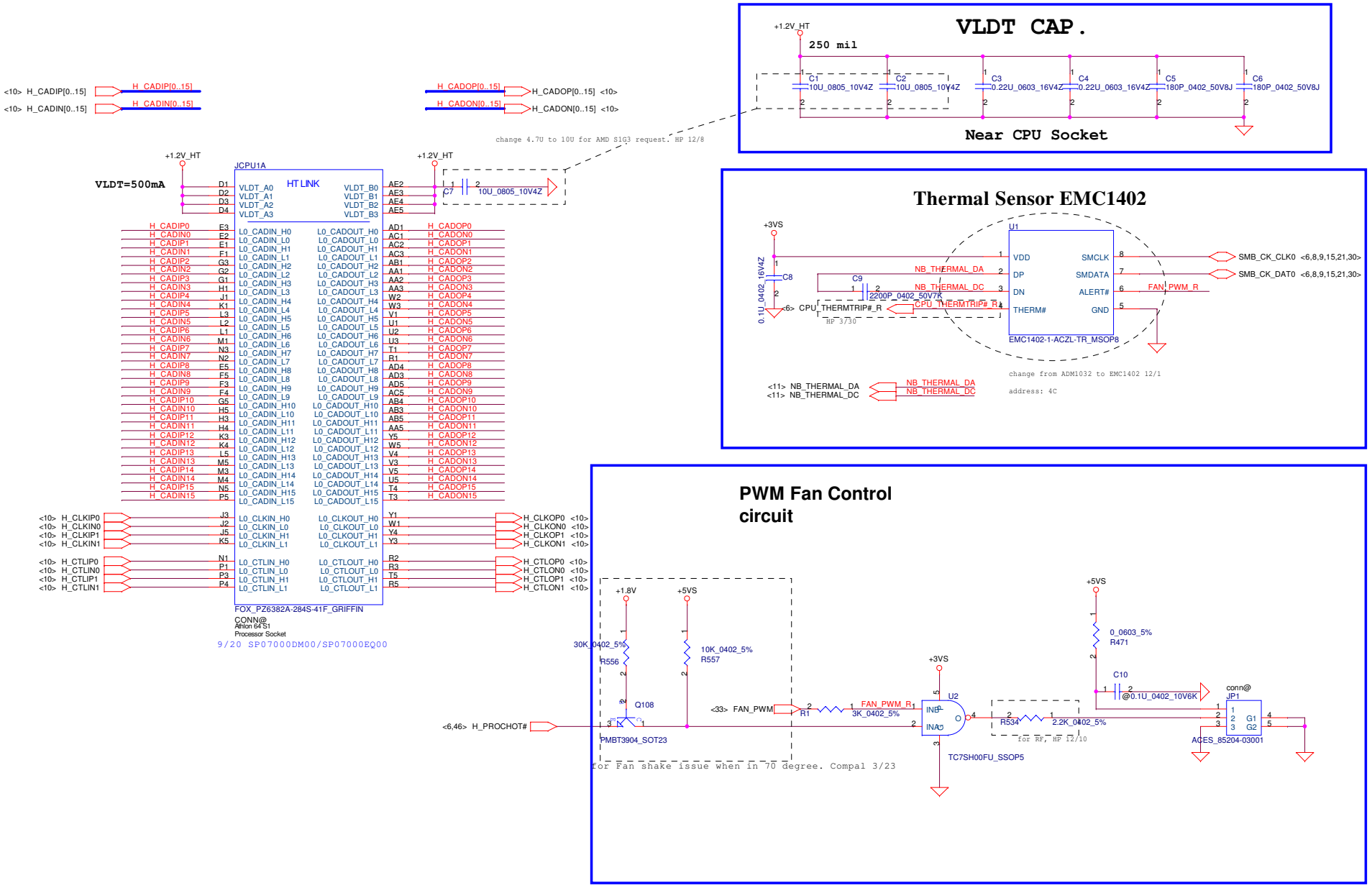

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Compal Electronics, Inc.

Title: **AMD CPU S1G2 HT I/F**

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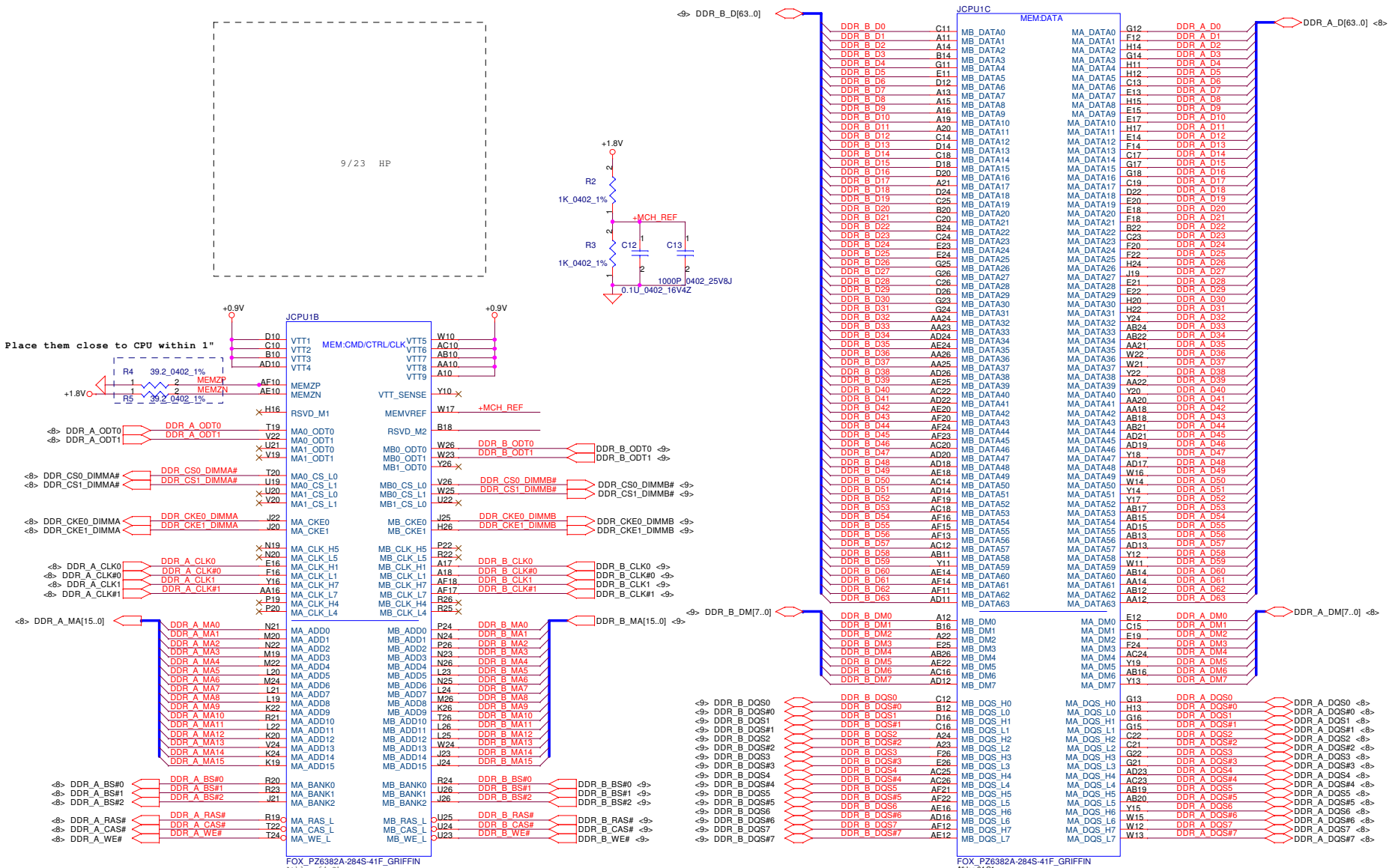
Processor DDR2 Memory Interface



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Compal Electronics, Inc.

Title: **AMD CPU S1G2 DDRII I/F**

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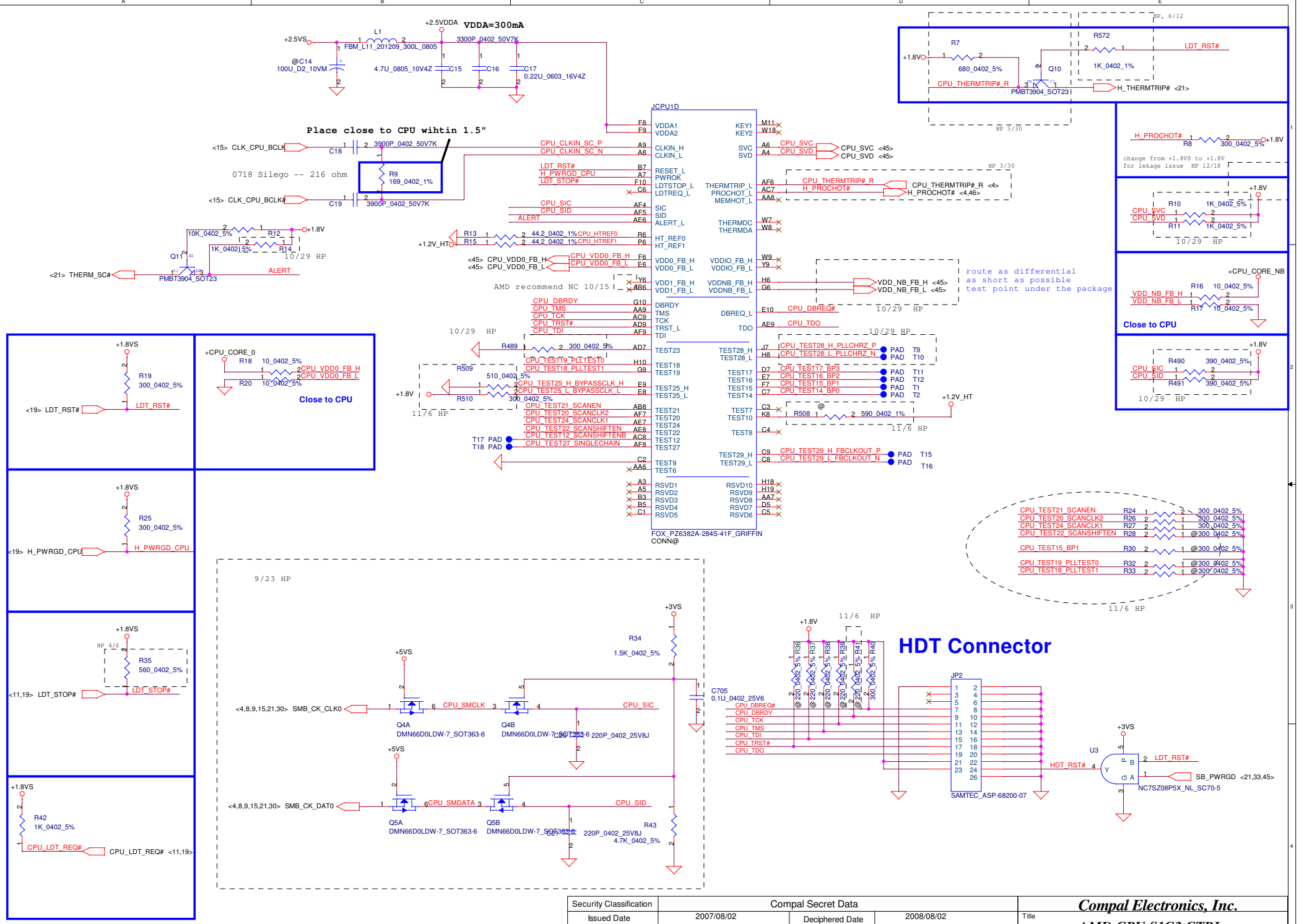

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Compal Electronics, Inc.

Title: **AMD CPU S1G2 CTRL**

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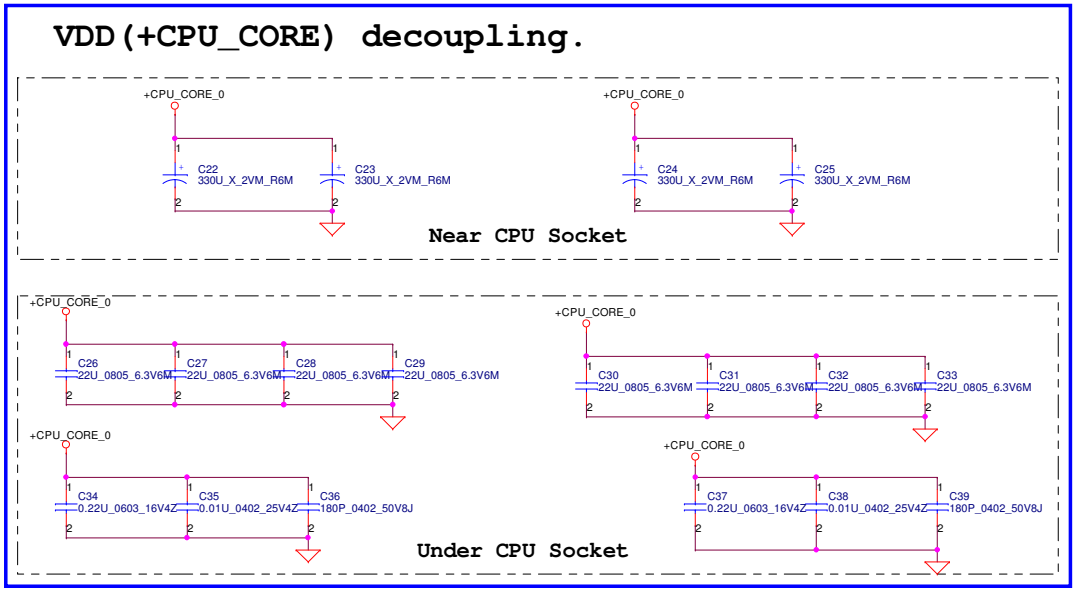
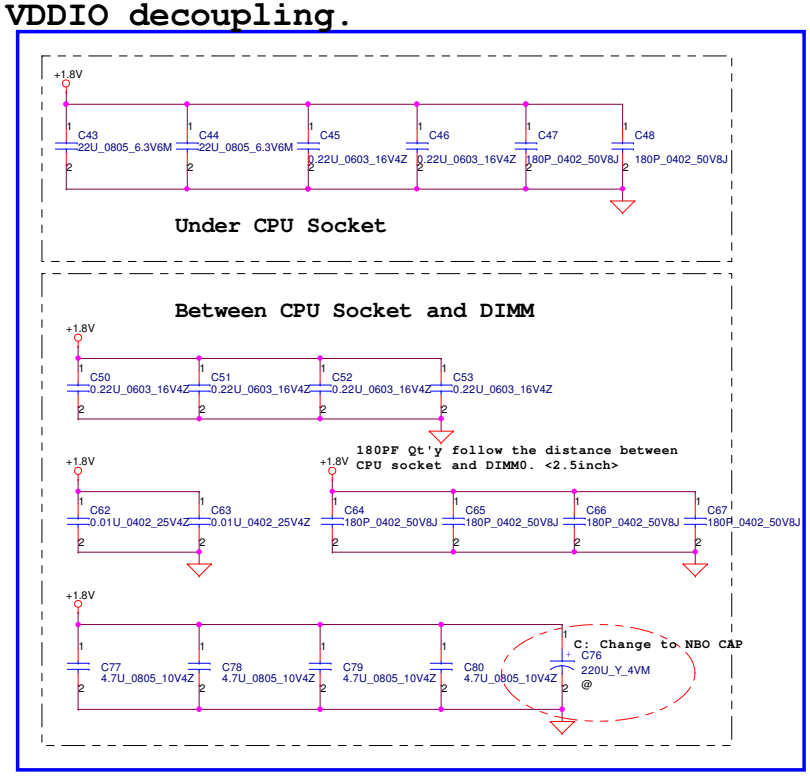
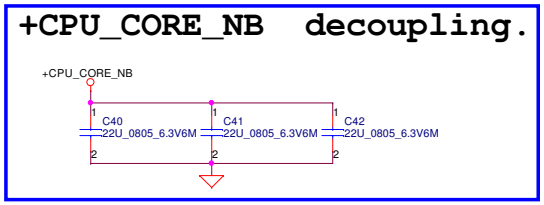
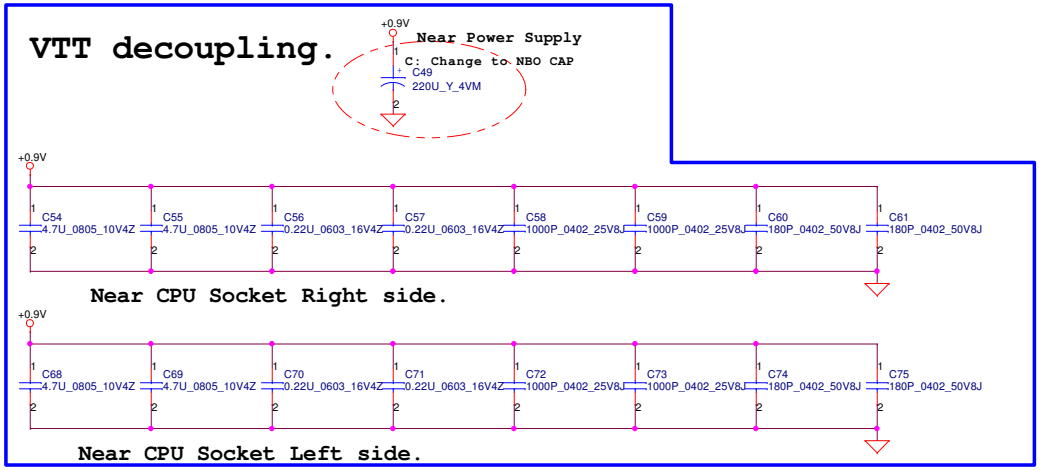
Date: Thursday, August 27, 2009 | Sheet 6 of 54









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Title: AMD CPU S1G2 PWR & GND

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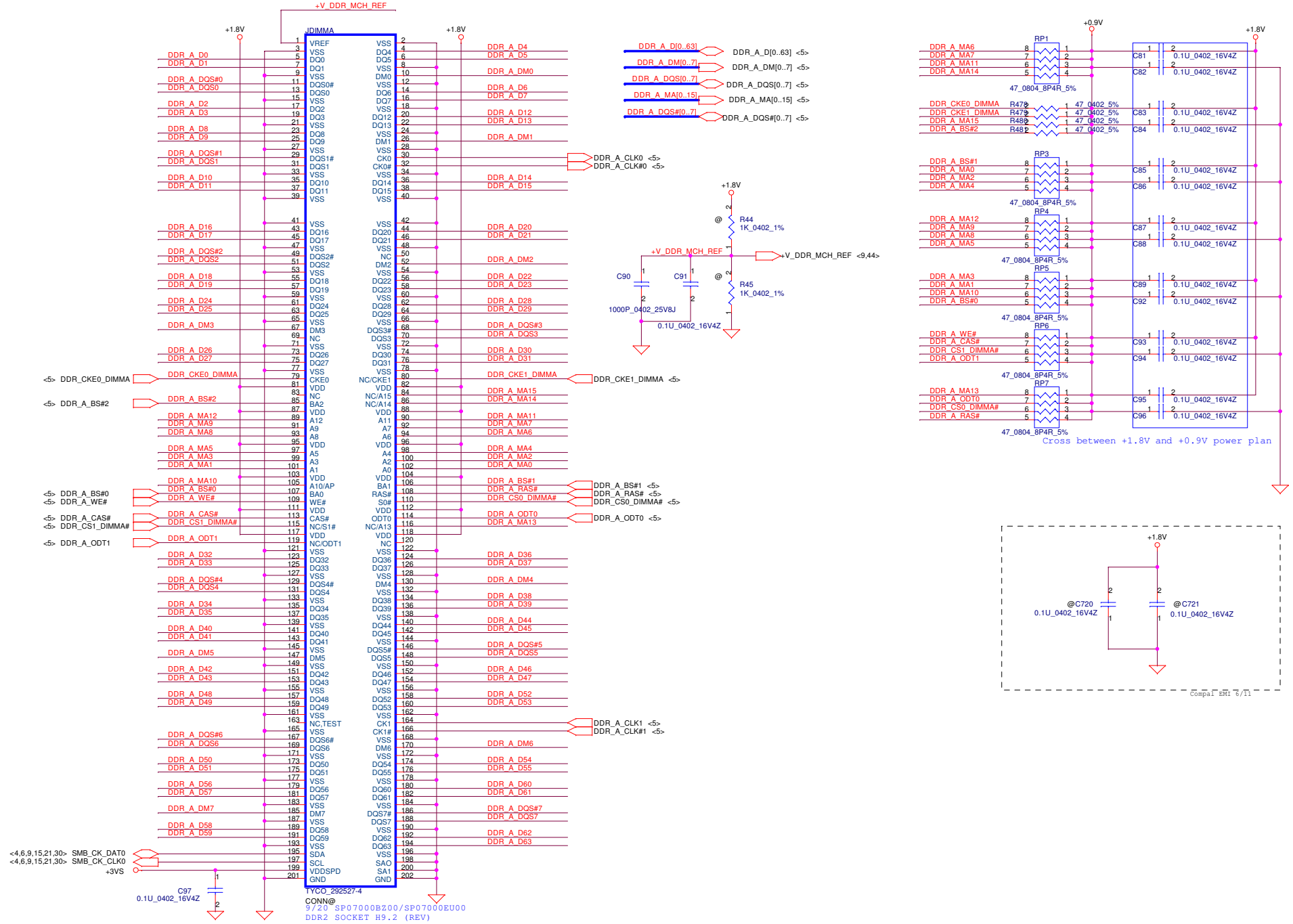

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Compal Electronics, Inc.

Title: **DDRII SO-DIMM 1**

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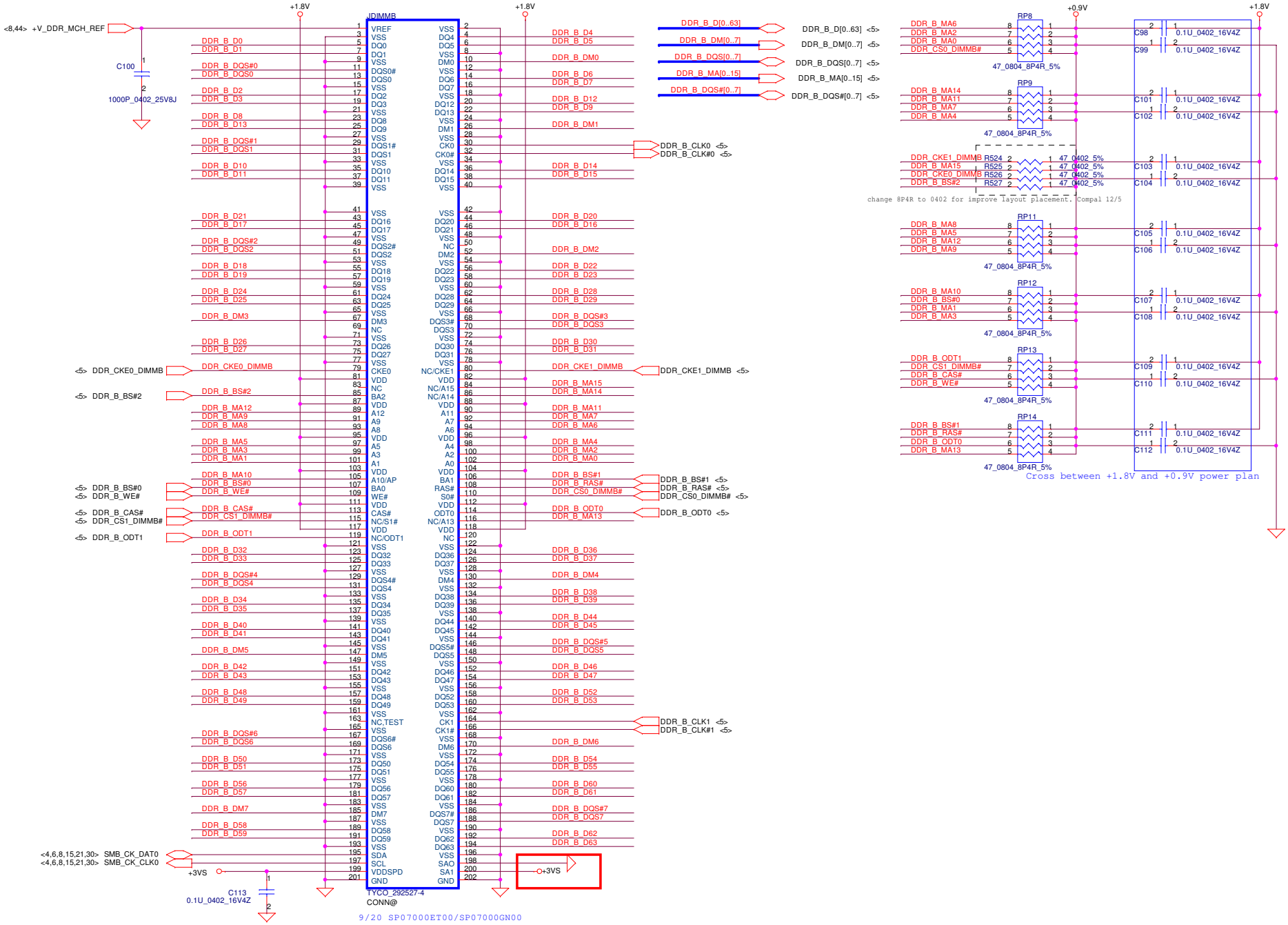

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Compal Electronics, Inc.

Title: **DDRII SO-DIMM 2**

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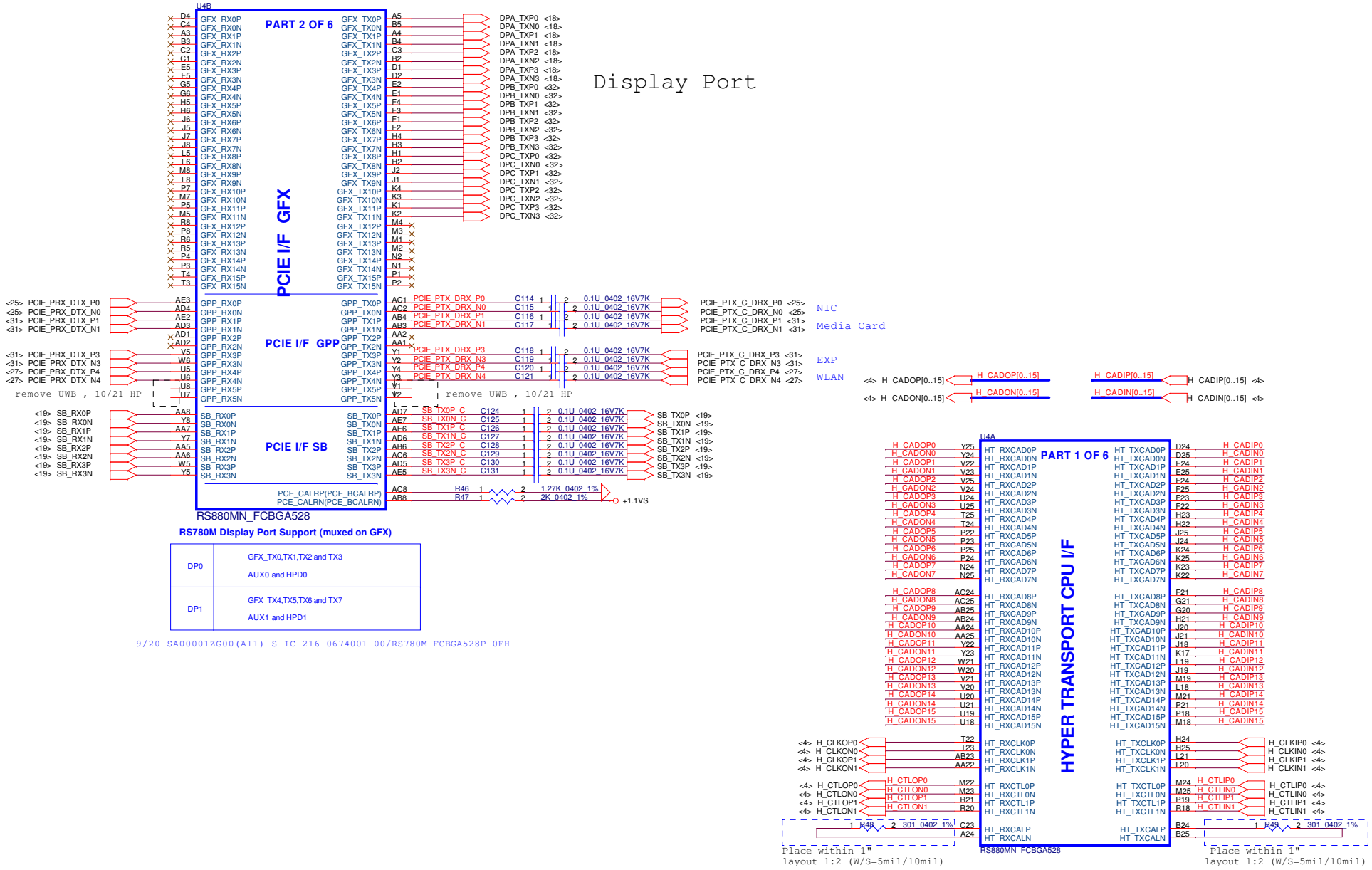

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

9/20 SA000012G00(A11) S IC 216-0674001-00/RS780M FCBGA528P 0FH

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Compal Electronics, Inc.

Title: **RS880-HT/PCIE**

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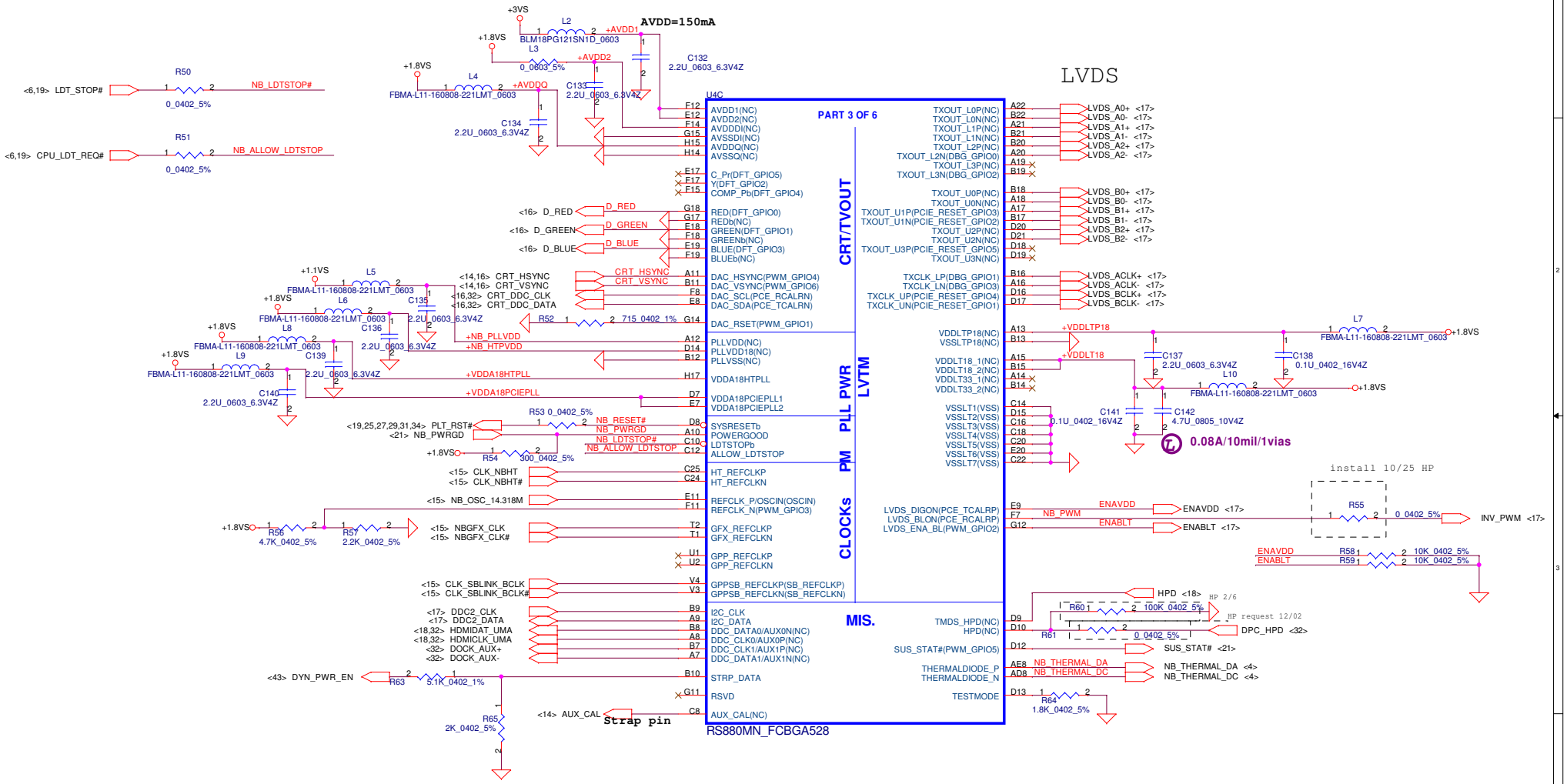
Date: Thursday, August 27, 2009 | Sheet 10 of 54



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Compal Electronics, Inc.

Title: **RS880 VEDIO/CLK GEN**

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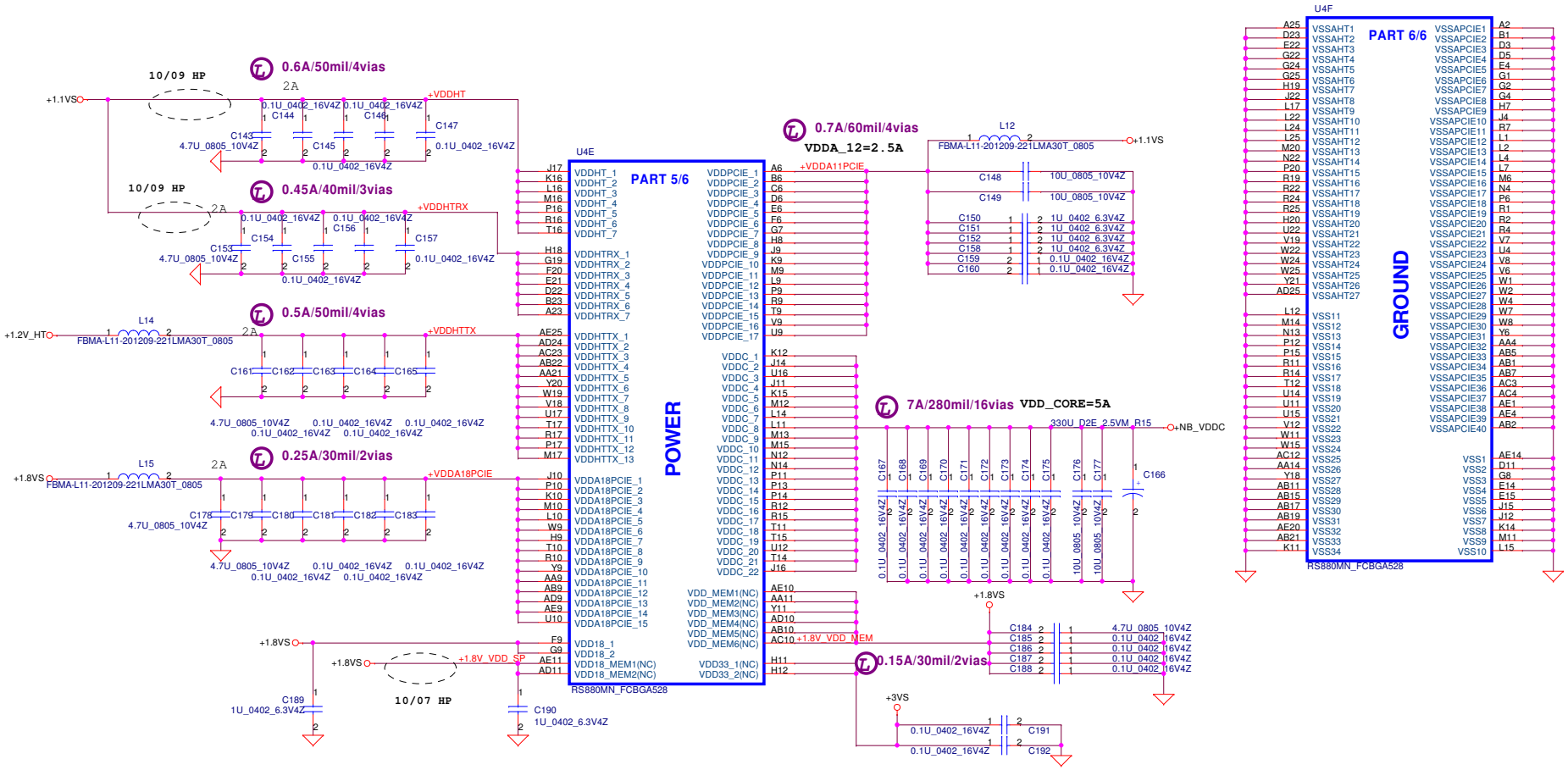
Date: Thursday, August 27, 2009 | Sheet 11 of 54



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Compal Electronics, Inc.

Title: **RS880 PWR/GND**

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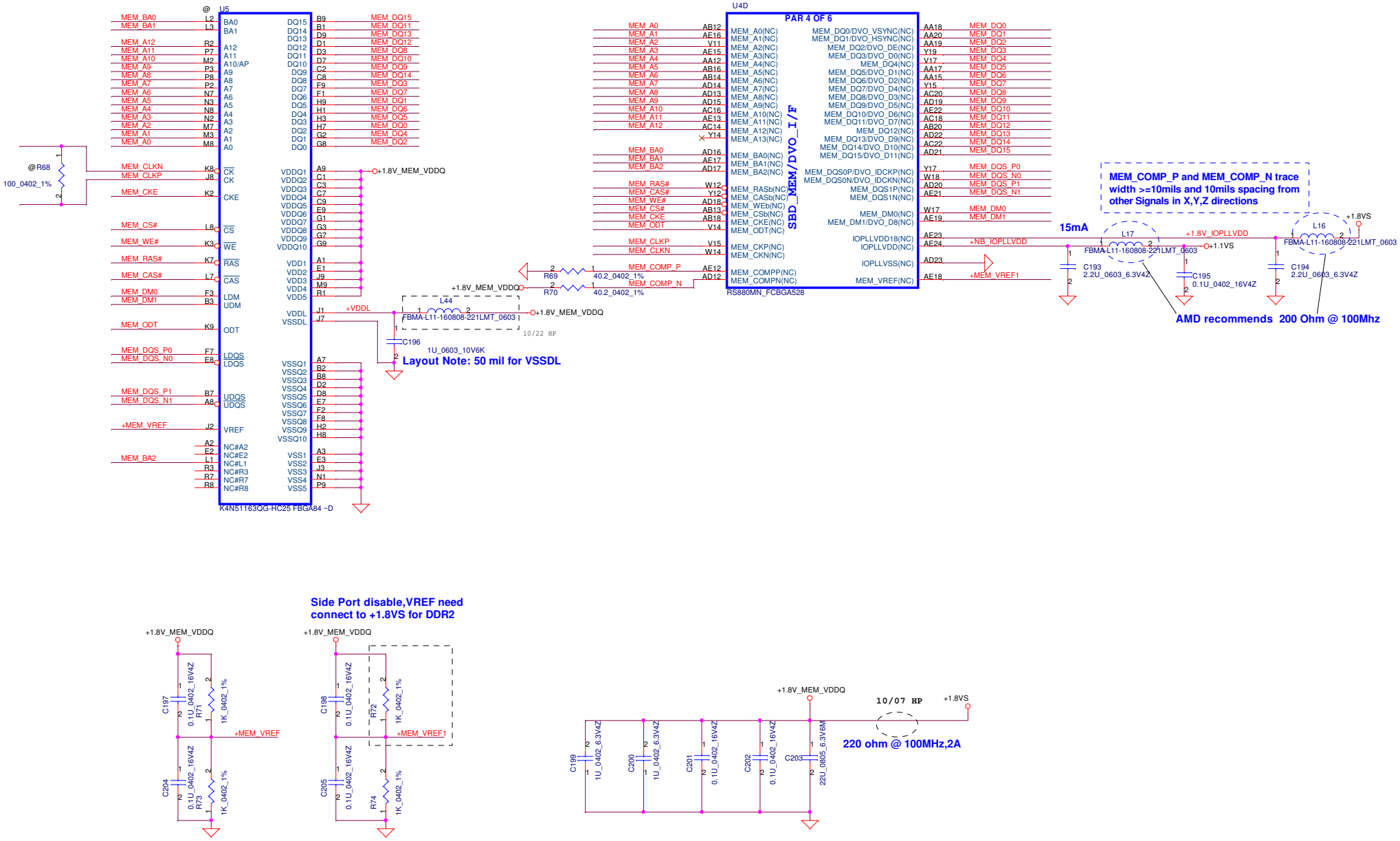
Date: Thursday, August 27, 2009 | Sheet 12 of 54



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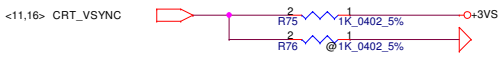
Title: **RS880 Side-Port DDR2 SDRAM**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 13 of 54

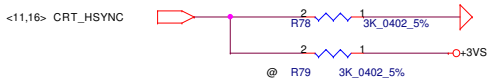
RS780 DFT_GPIO5 mux at CRT_VSYNC pull low to 3K



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Disable (RS780)  Enable (RX780)
0 : Enable (RS780)   Disable (RX780)
PIN: RX780:NB_TV_C; RS740: RS740_DFT_GPIO5; RS780: VSYNC#
```

RS780 use HSYNC to enable SIDE PORT (internal pull high)



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
```

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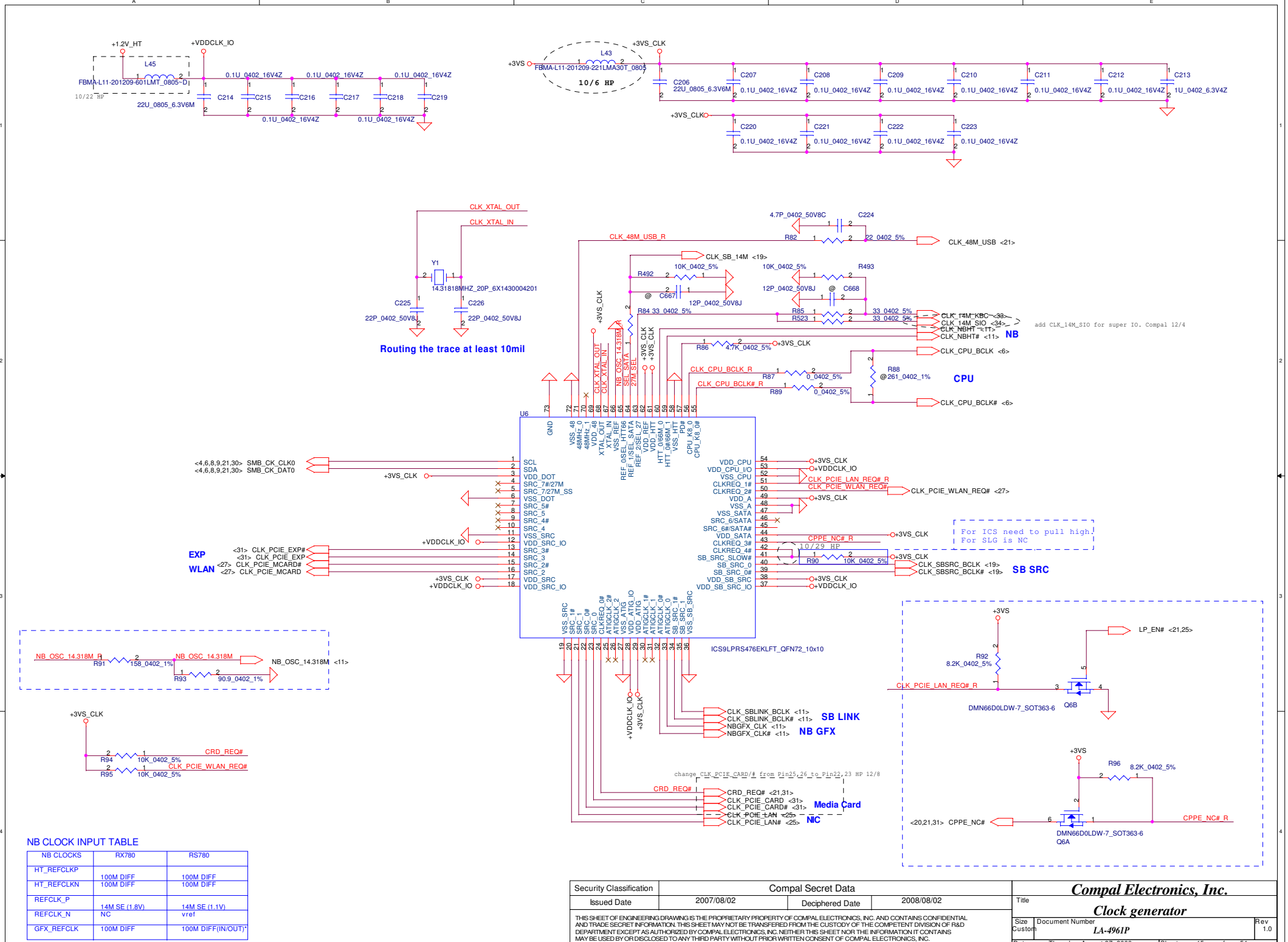
Title: **RS880 STRAPS**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 14 of 54



NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*

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Compal Electronics, Inc.

Title: **Clock generator**

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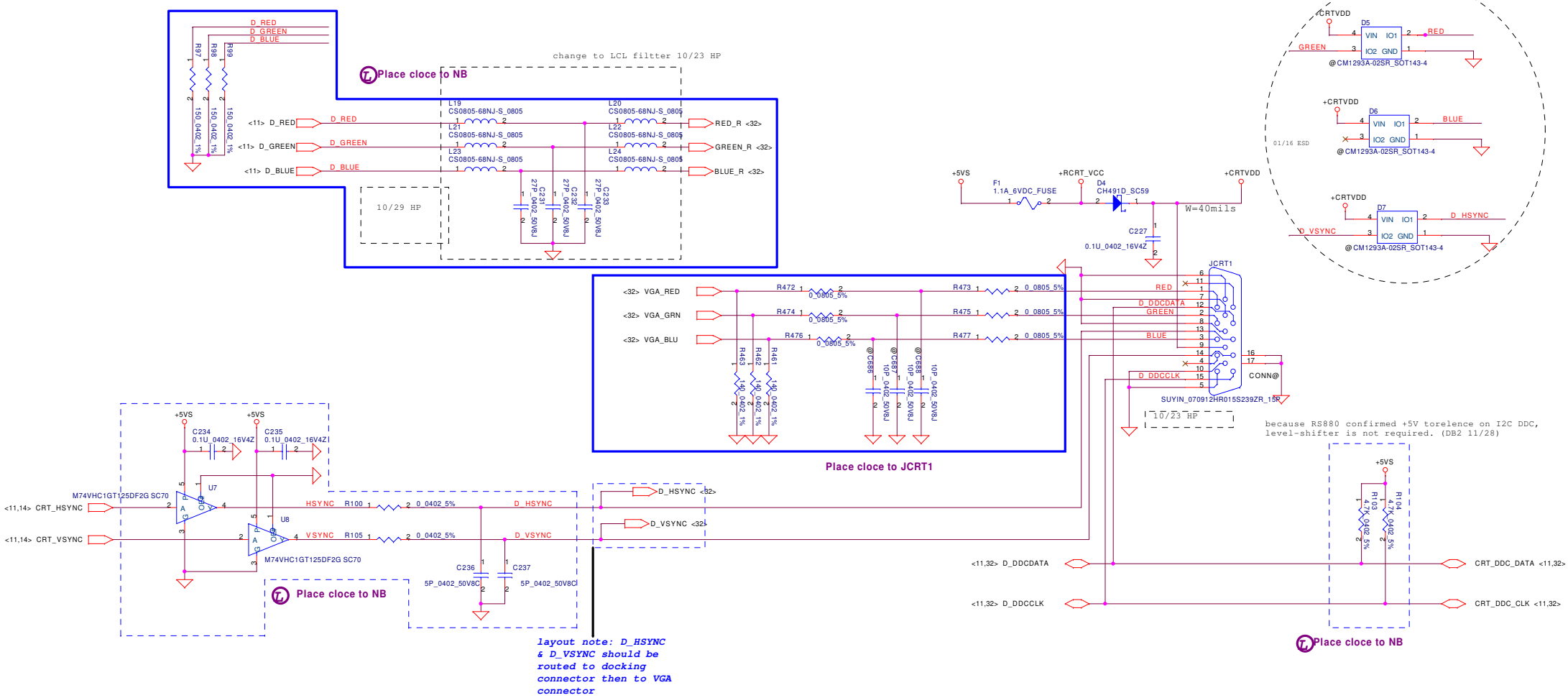
Date: Thursday, August 27, 2009 | Sheet 15 of 54



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Compal Electronics, Inc.

Title: **CRT Connector**

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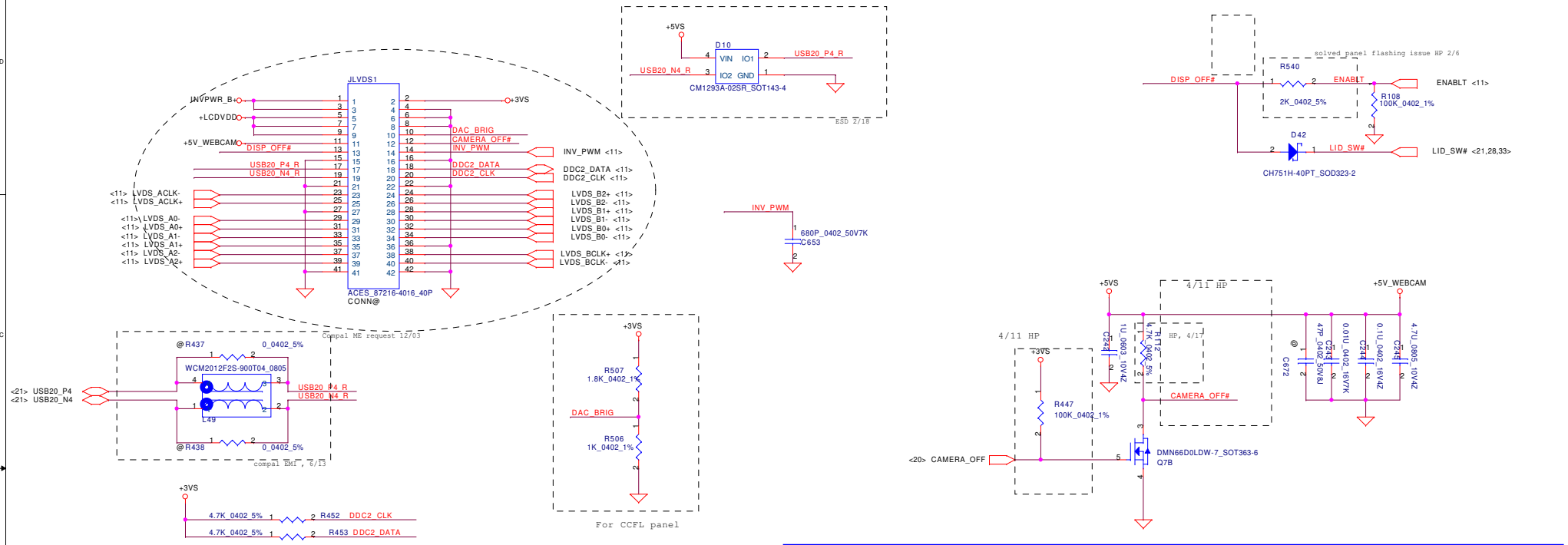
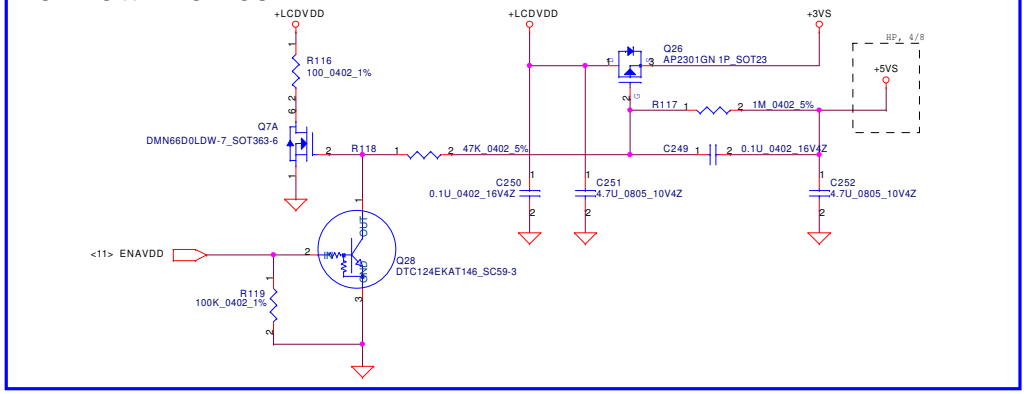
LCD/PANEL BD. CONN.



LCD POWER CIRCUIT



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Title: **LCD CONN & Q-Switch & GPIO Ext.**

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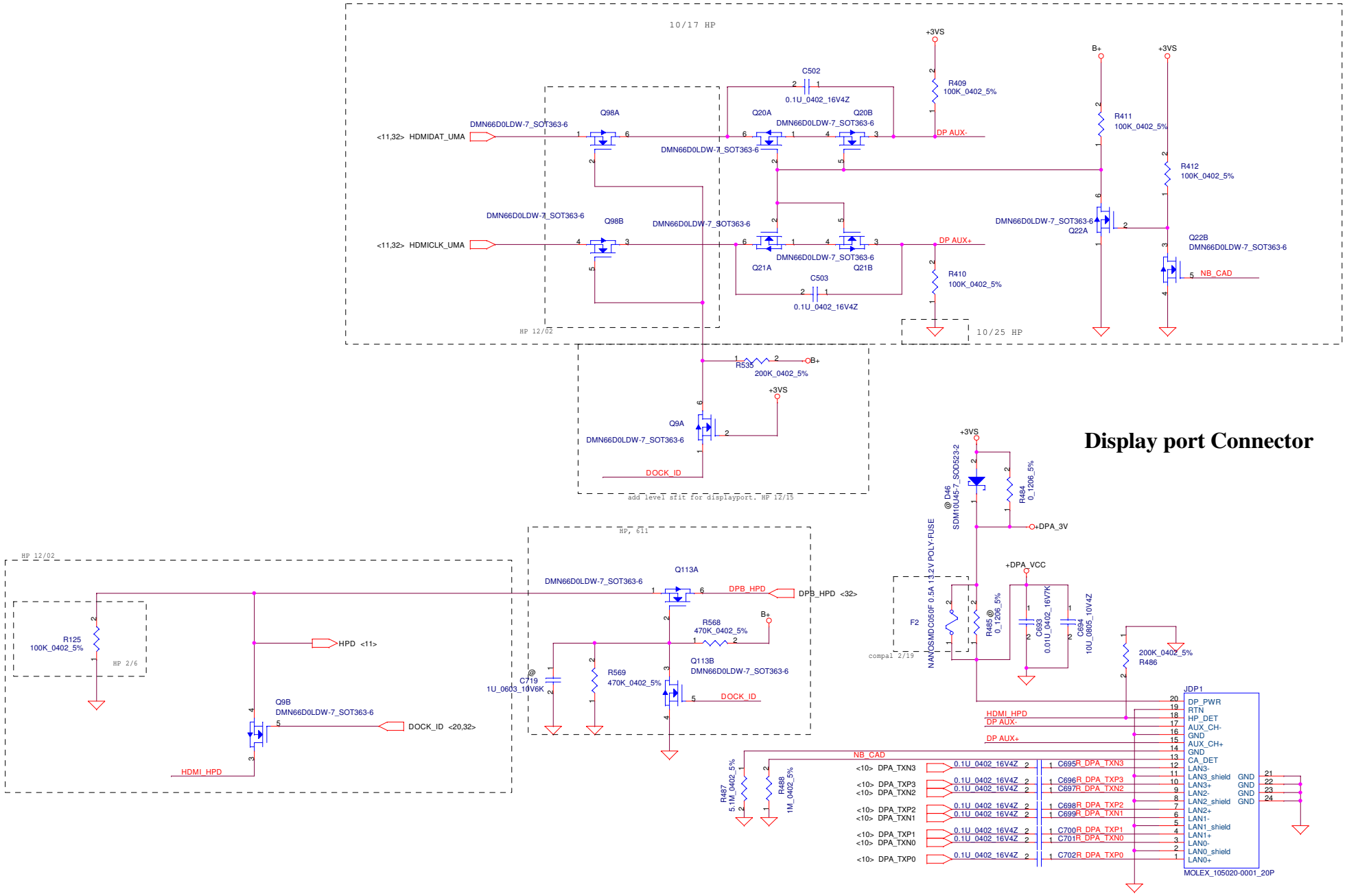
Display port Connector



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Compal Electronics, Inc.

Title: **Display port**

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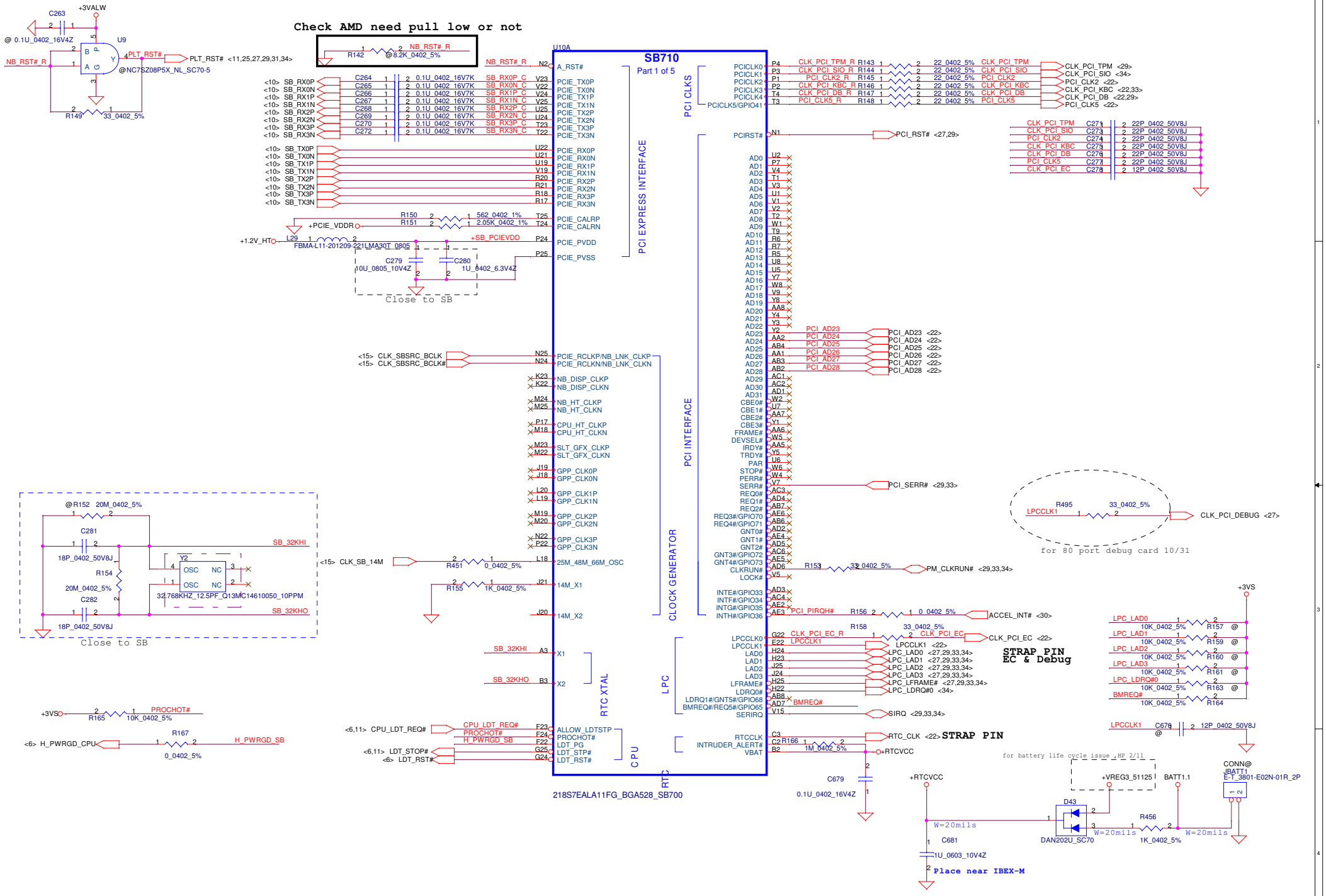

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Issued Date	2007/08/02	Deciphered Date	2008/08/02

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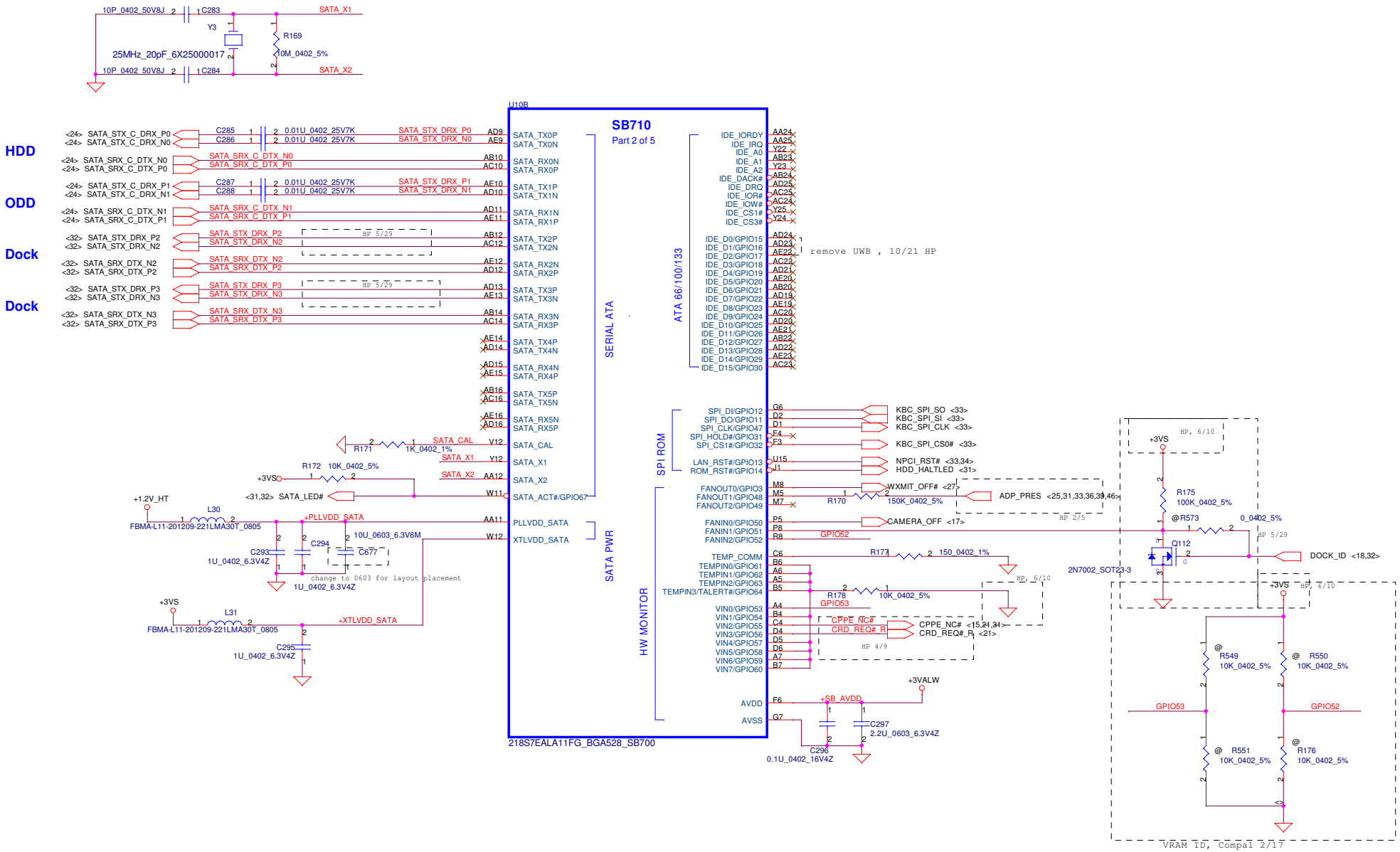
Compal Electronics, Inc.

Title: **SB710-PCIE/PCI/ACPI/LPC/RTC**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 19 of 54



VRAM ID	GPIO52	GPIO53
Hynix 64MB (main source)	0	0
Samsung 128MB(2nd source)	0	1
Hynix 128MB (2nd source)	1	0
Samsung 128MB (2nd source)	1	1

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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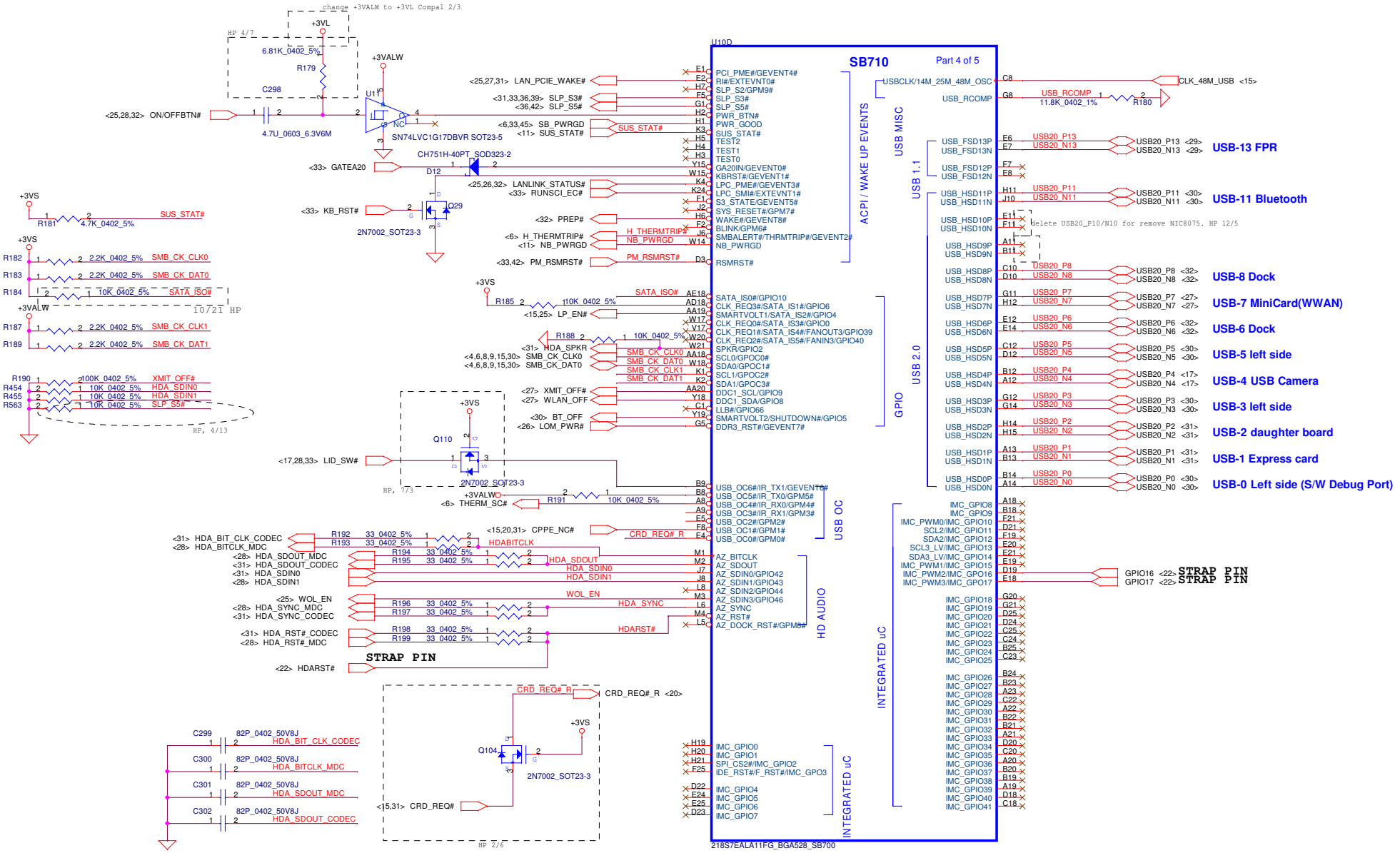
Compal Electronics, Inc.

Title: **SB710 SATA/IDE/SPI**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 20 of 54



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Issued Date	2007/08/02	Deciphered Date	2008/08/02

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Compal Electronics, Inc.

Title: **SB710 USB/AC97**

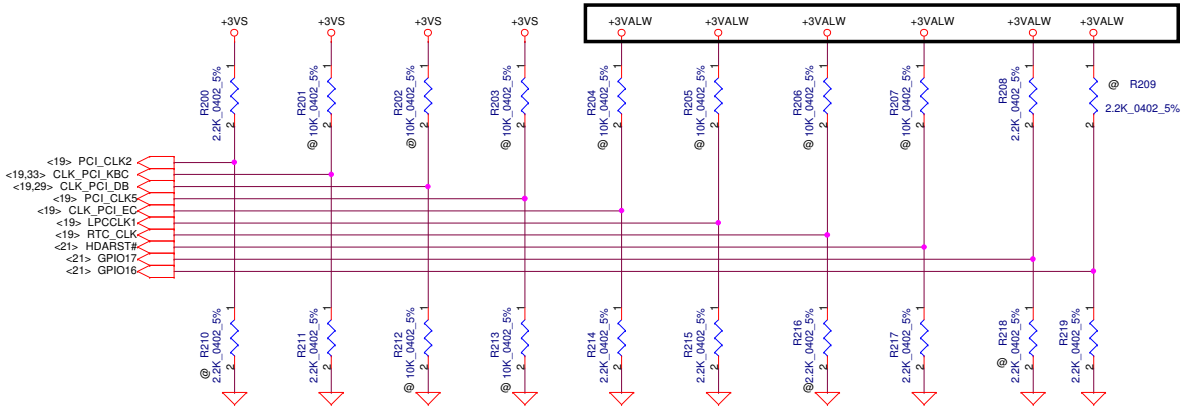
Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 21 of 54

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

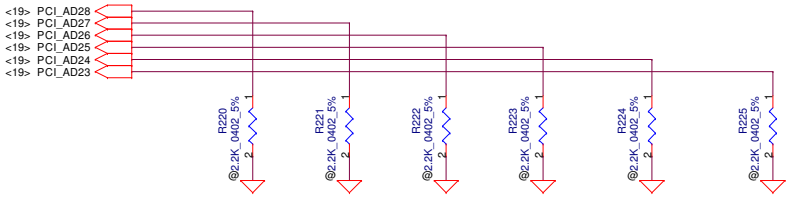
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



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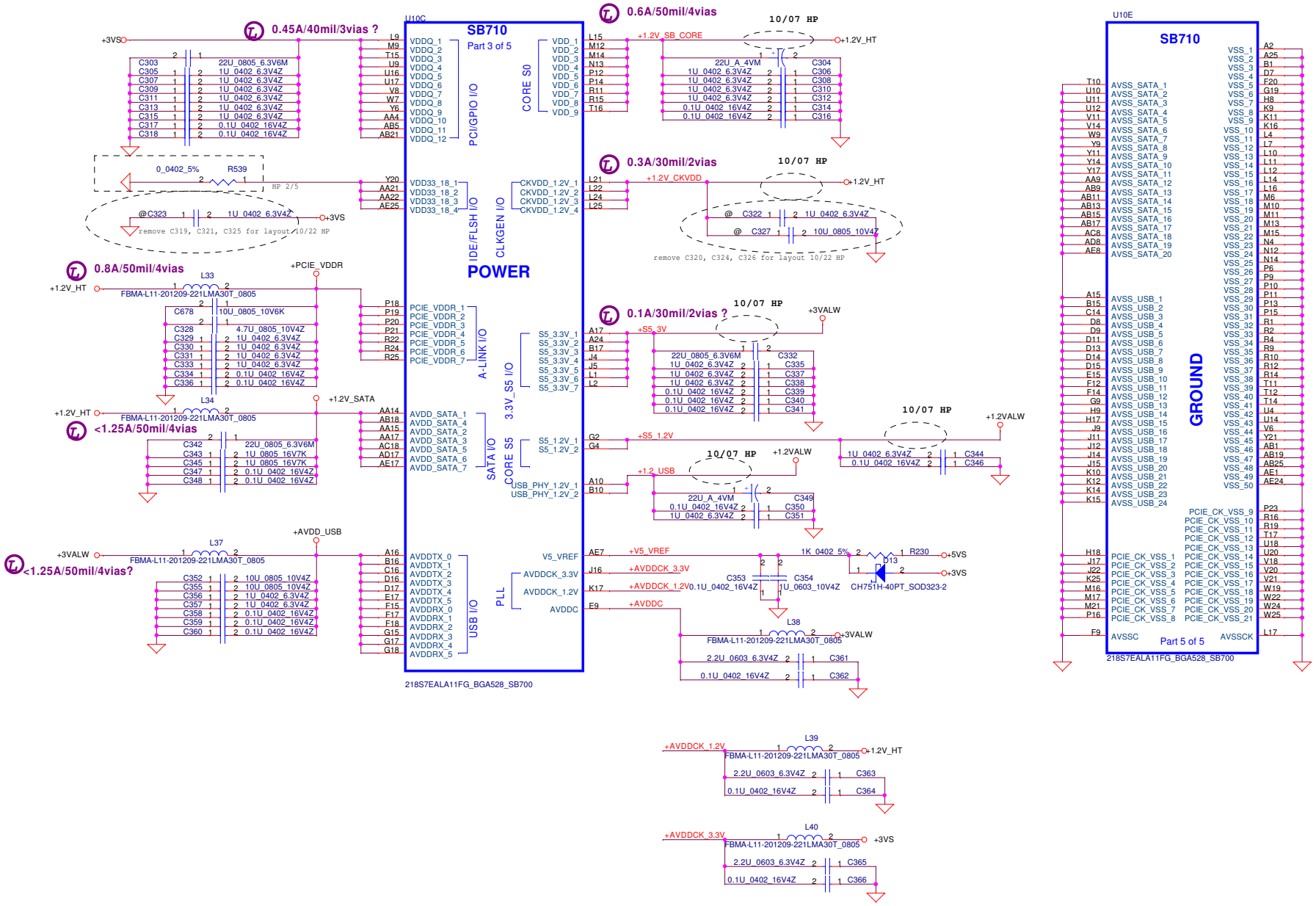
Compal Electronics, Inc.

Title: SB710 STRAPS

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 22 of 54



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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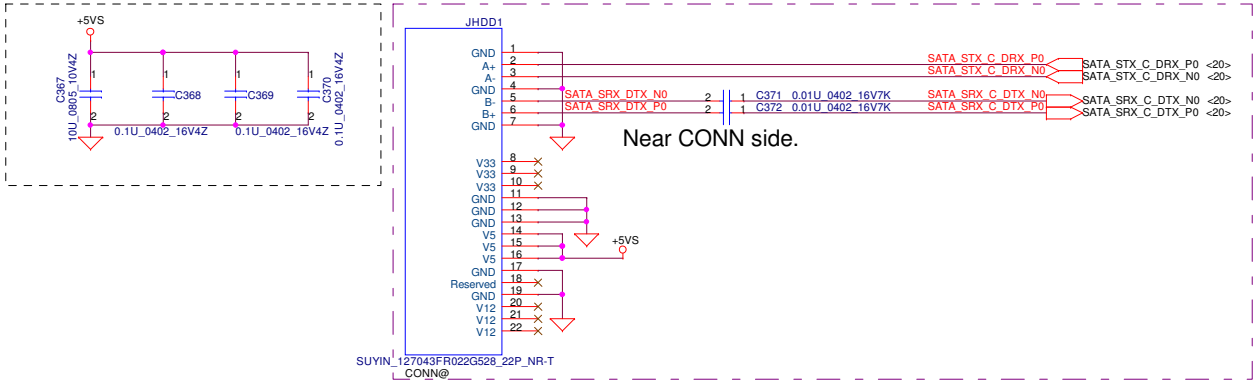
Compal Electronics, Inc.

Title: **SB710 PWR/GND**

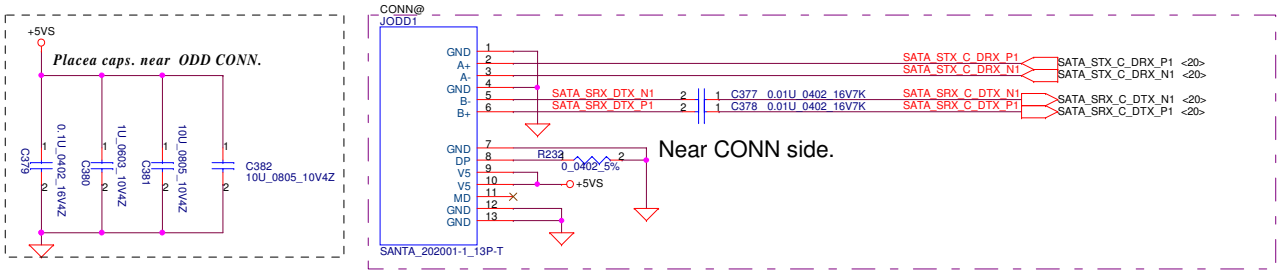
Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 23 of 54

HDD Connector



CD-ROM Connector



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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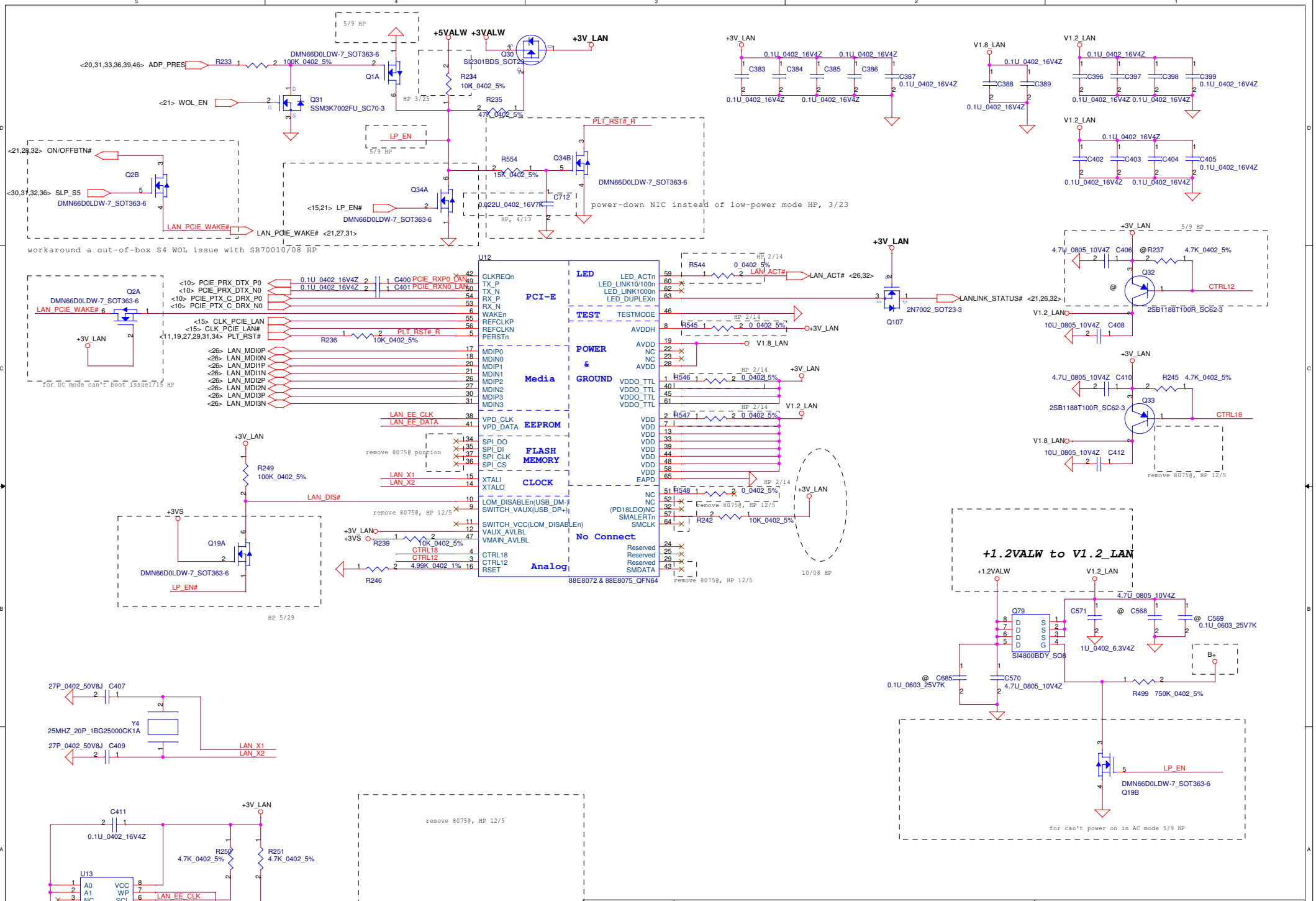
Compal Electronics, Inc.

Title: **HDD/CDROM**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 24 of 54



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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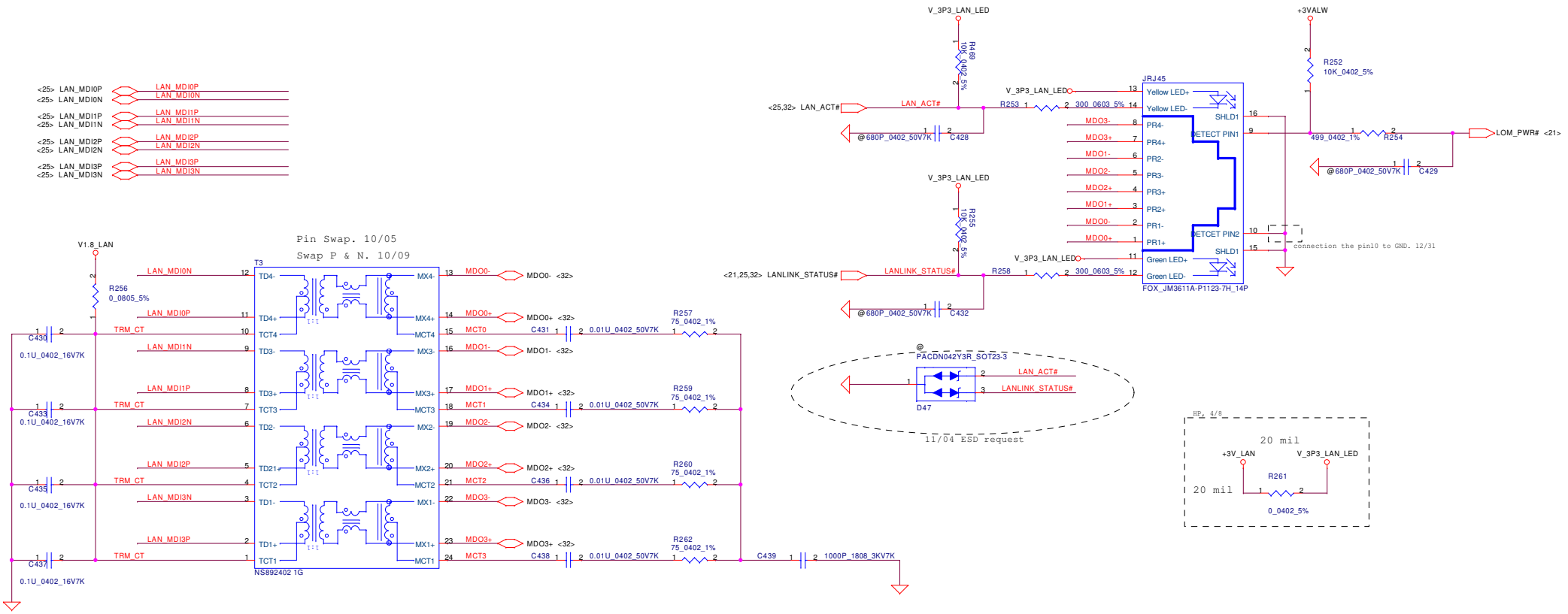
Compal Electronics, Inc.

Title: Giga LAN 88E8072

Size | Document Number | Rev 1.0

Date: Thursday, August 27, 2009 | Sheet 25 of 54



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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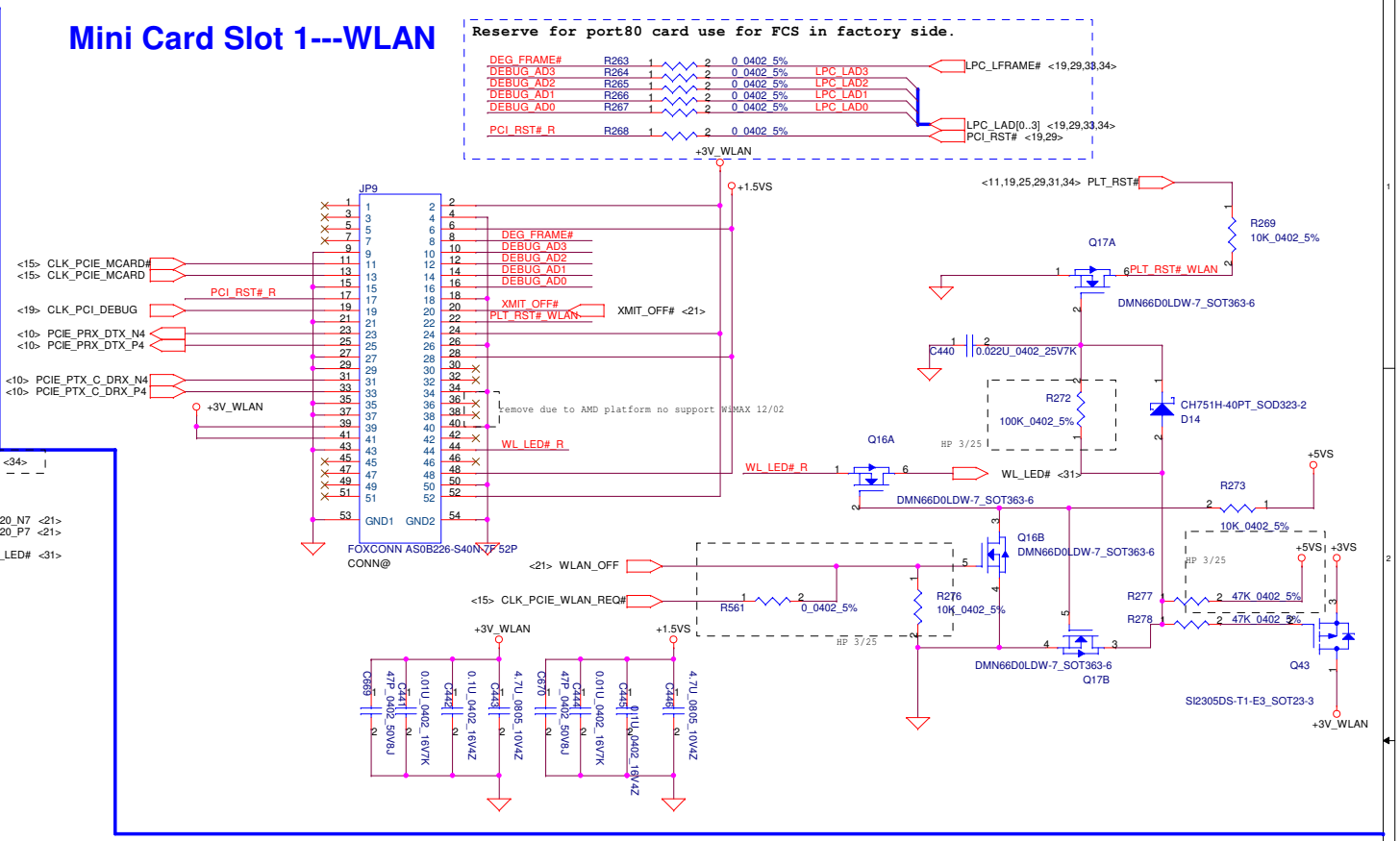
Compal Electronics, Inc.

Title: **Magnetic & RJ45**

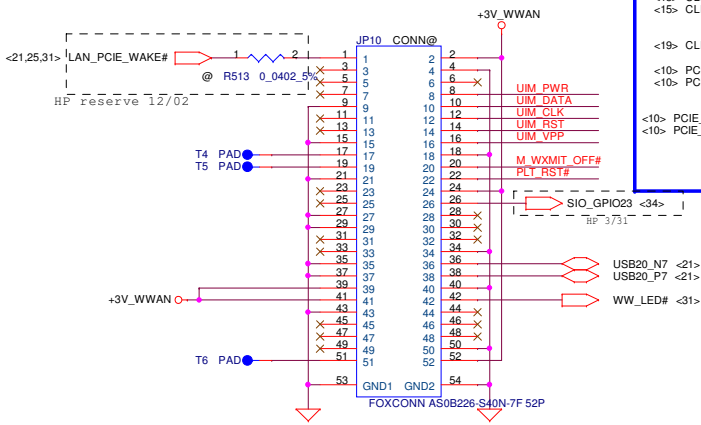
Size | Document Number: **LA-4961P** | Rev: 1.0

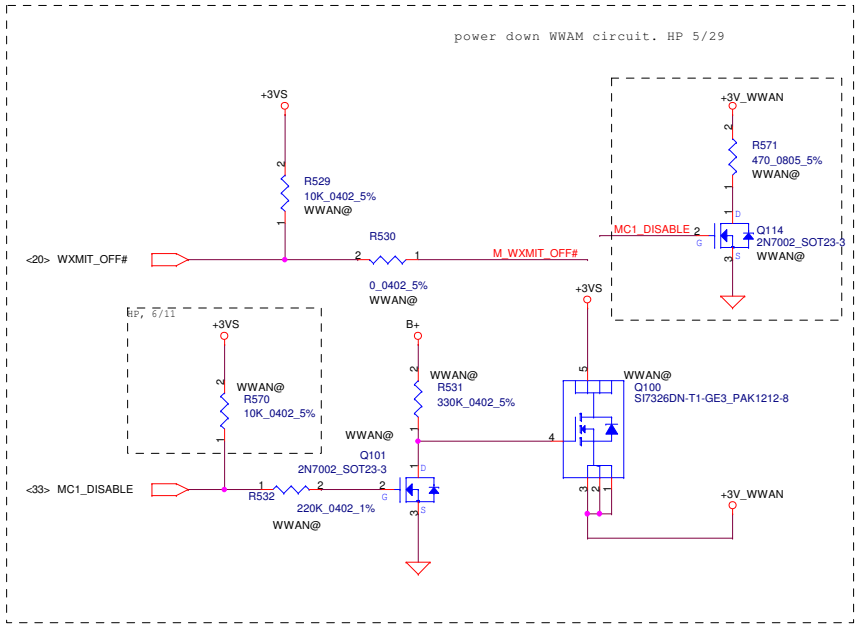
Date: Thursday, August 27, 2009 | Sheet 26 of 54

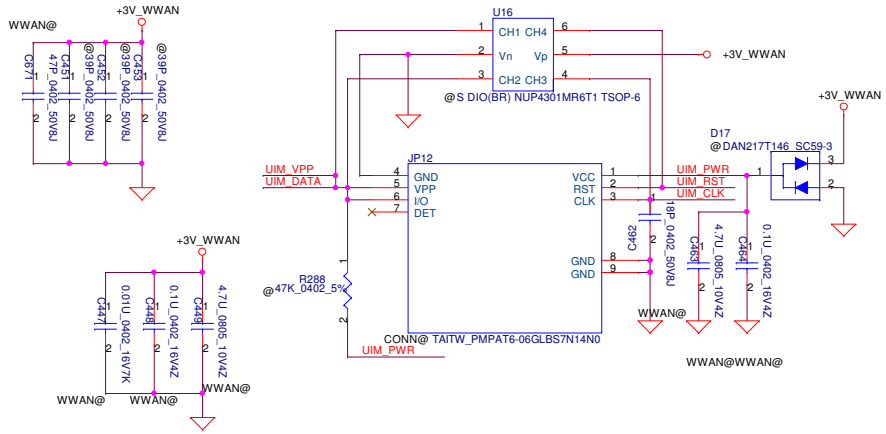
Mini Card Slot 1---WLAN



Mini Card Slot3--WWAN







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Issued Date	2008/03/13	Deciphered Date	2009/05/11

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Compal Electronics, Inc.

Title: **WLAN&WWAN Mini-Card**

Size | Document Number: *LA-4961P* | Rev 1.0

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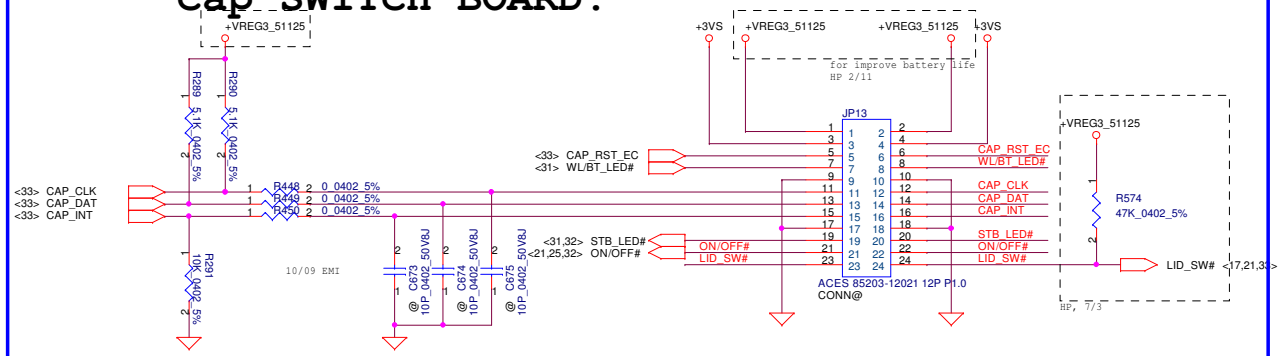
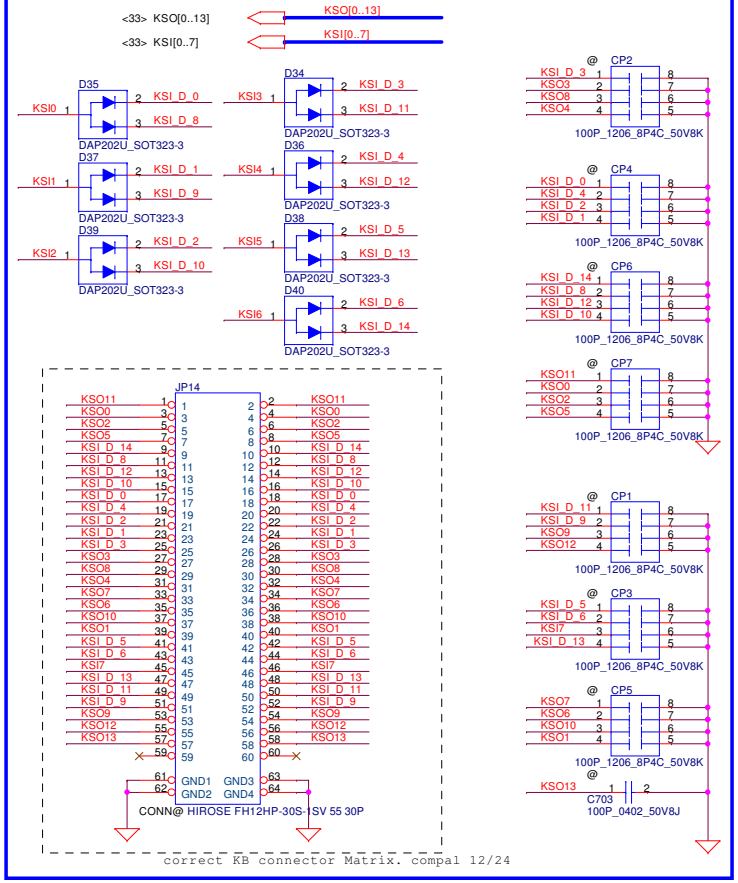
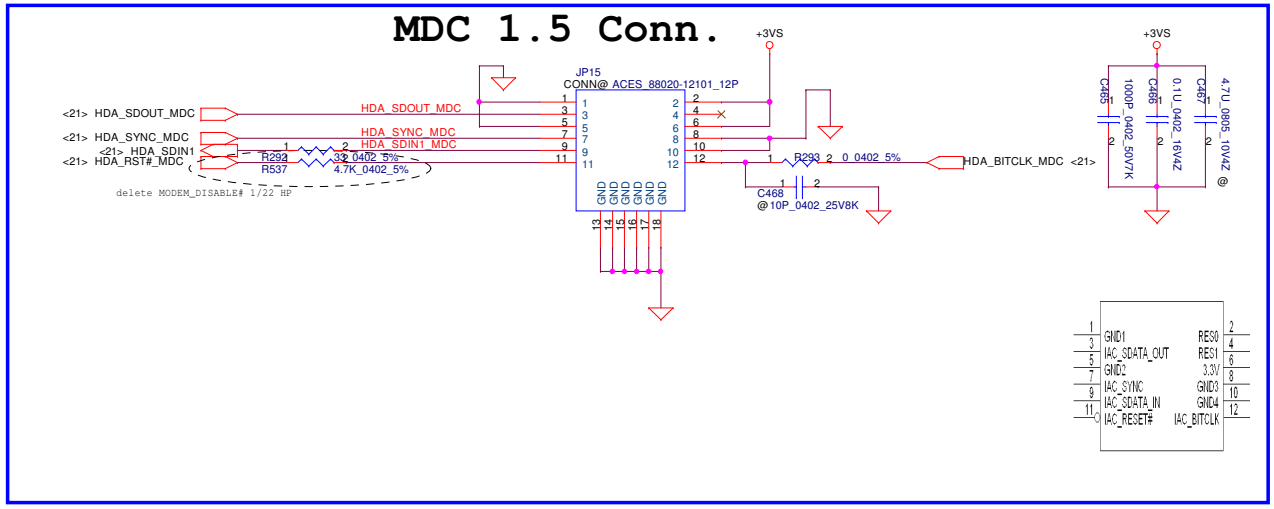
Cap SWITCH BOARD.



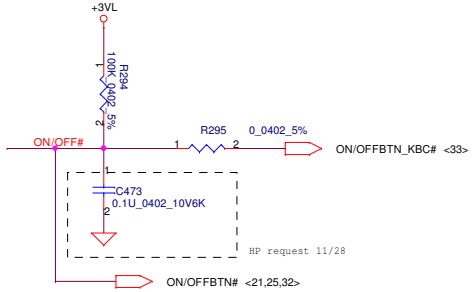
INT_KBD CONN.



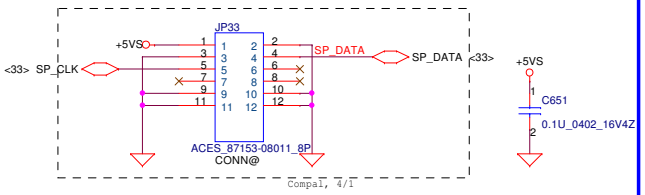
MDC 1.5 Conn.



Power button



TrackPoint CONN.



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Issued Date	2008/03/13	Deciphered Date	2009/05/11

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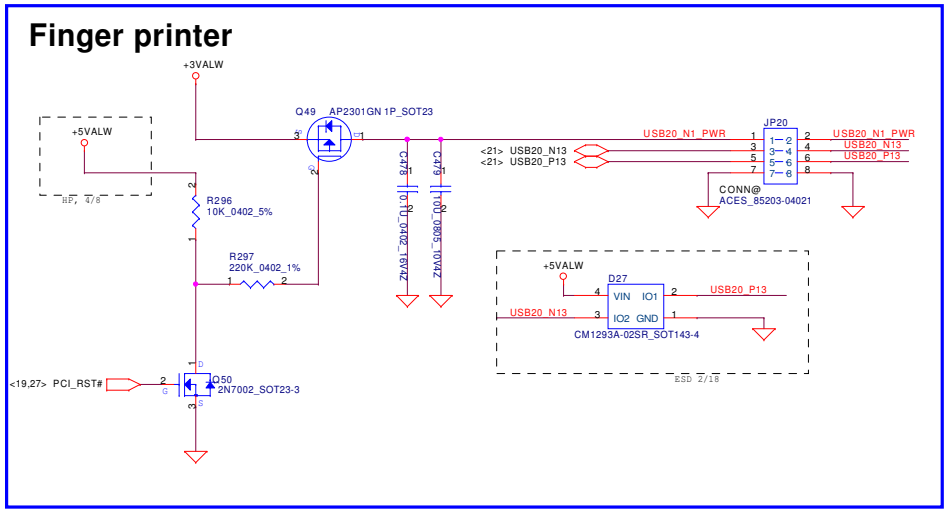
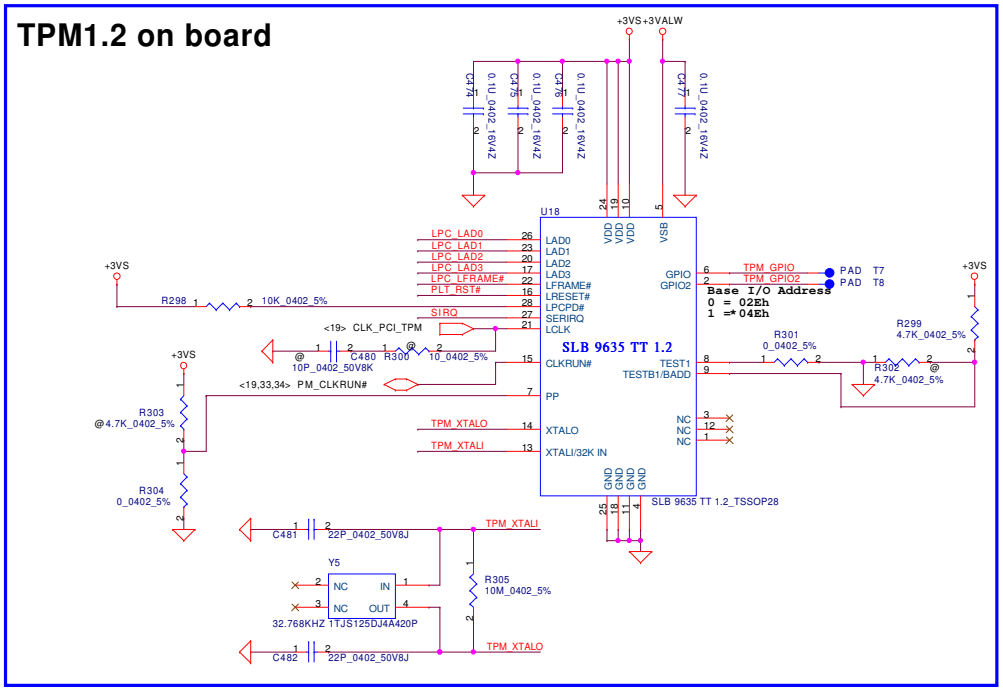
Compal Electronics, Inc.

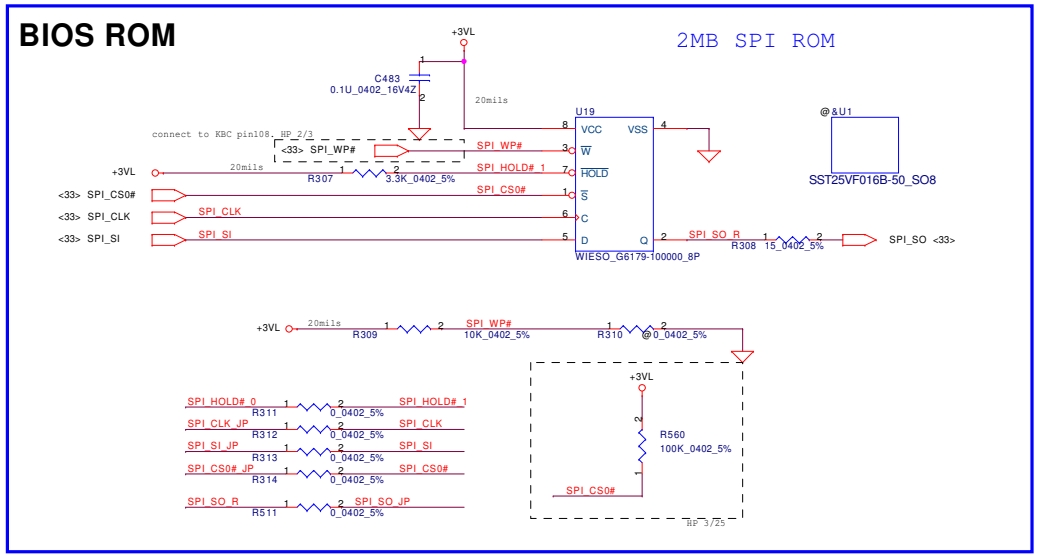
Title: *MDC/KBD/ON_OFF/LID*

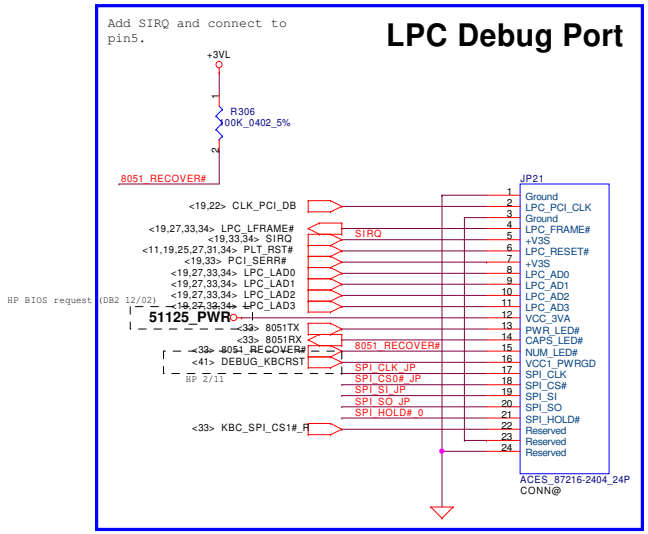
Size | Document Number: *LA-4961P* | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 28 of 54









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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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Compal Electronics, Inc.

Title: **TCG/BIOS ROM/PS2/SW LPC DEBUG**

Size	Document Number	Rev
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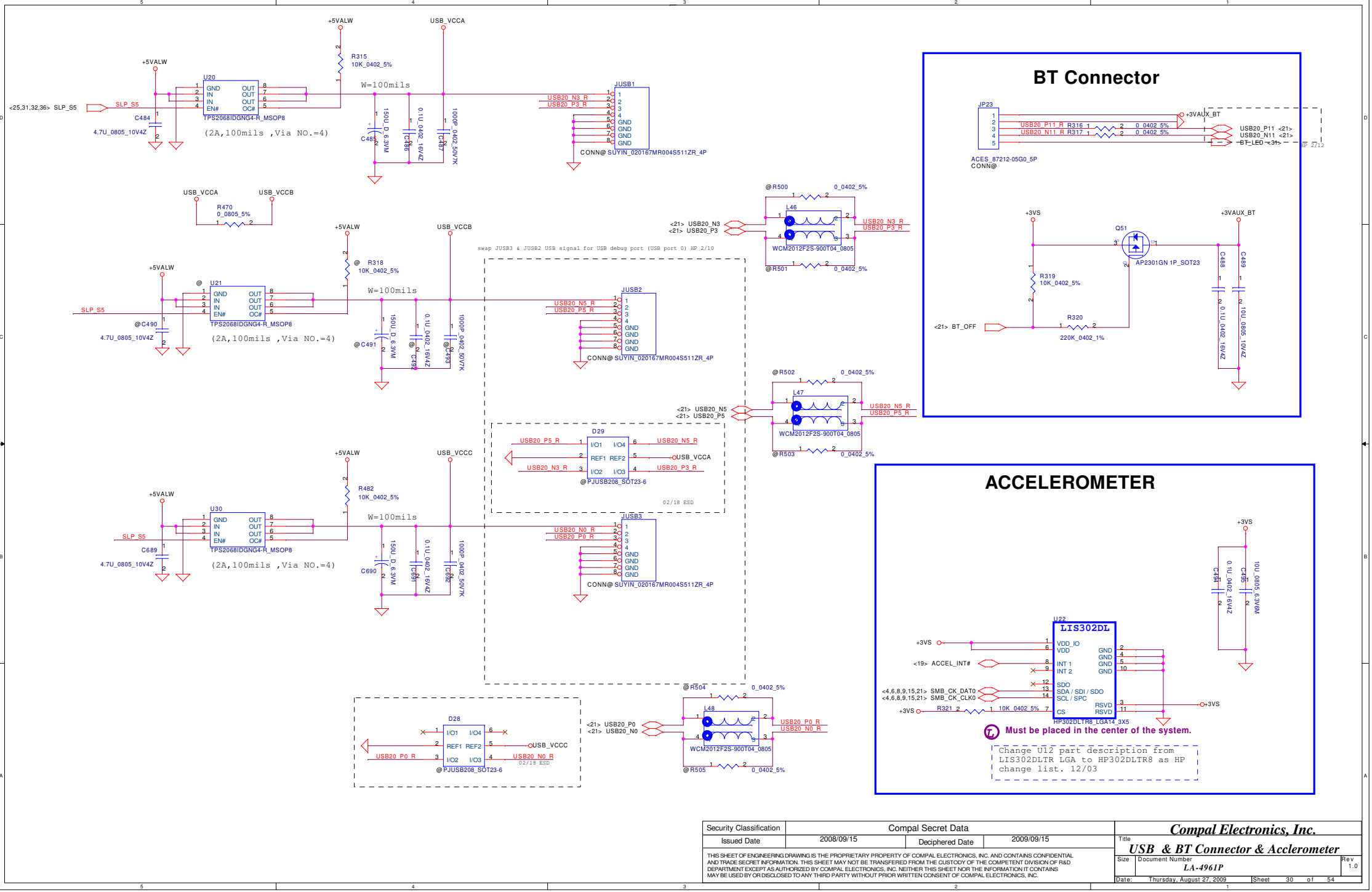

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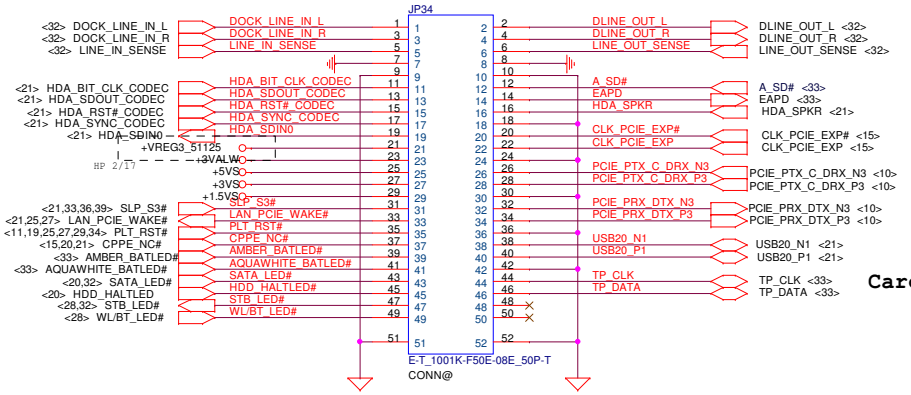
Compal Electronics, Inc.

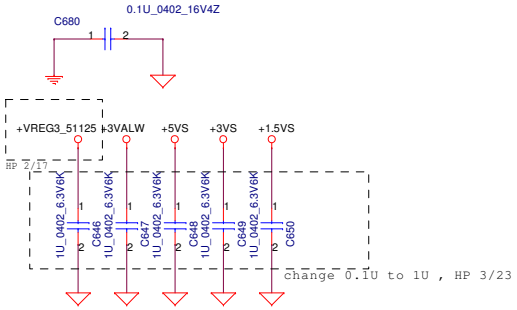
Title: **USB & BT Connector & Acclerometer**

Size	Document Number	Rev
	LA-4961P	1.0

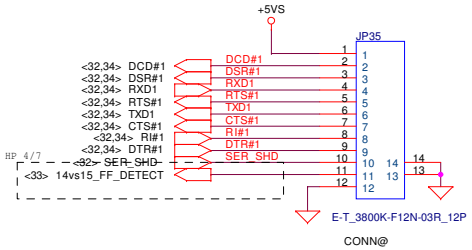
Date: Thursday, August 27, 2009 | Sheet 30 of 54

Audio/Express Card/TP/LEDs Connector

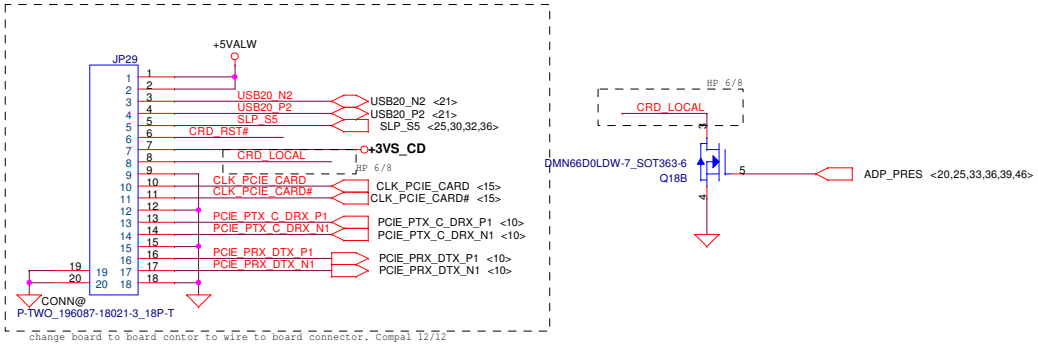


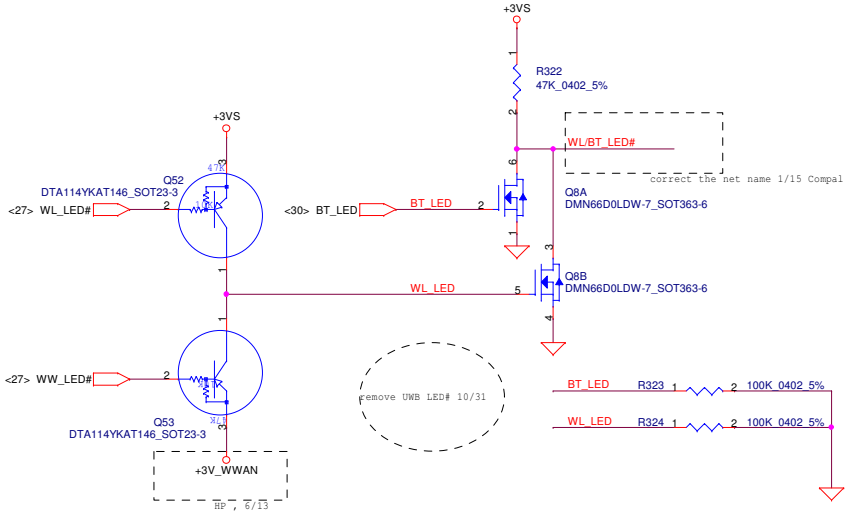


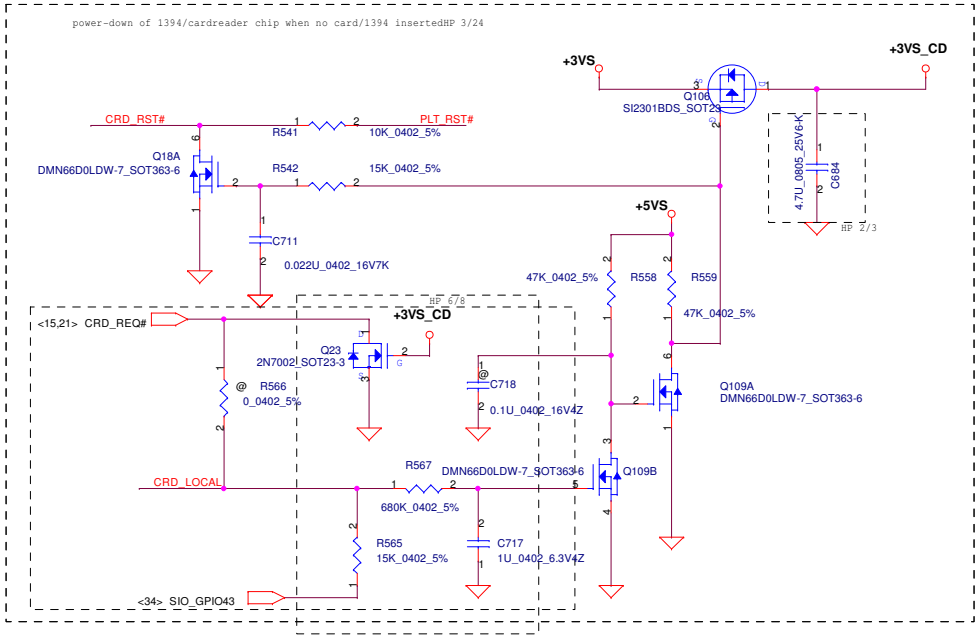
Serial Port CONN



Card Reader 7 in 1 + 1 Port USB Connector







10/21 move 1394A to card reader USB board

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Issued Date	2008/09/01	Deciphered Date	2010/09/01

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Compal Electronics, Inc.

Title: **CR&LEDS&PW&Audio&Exp Conn**

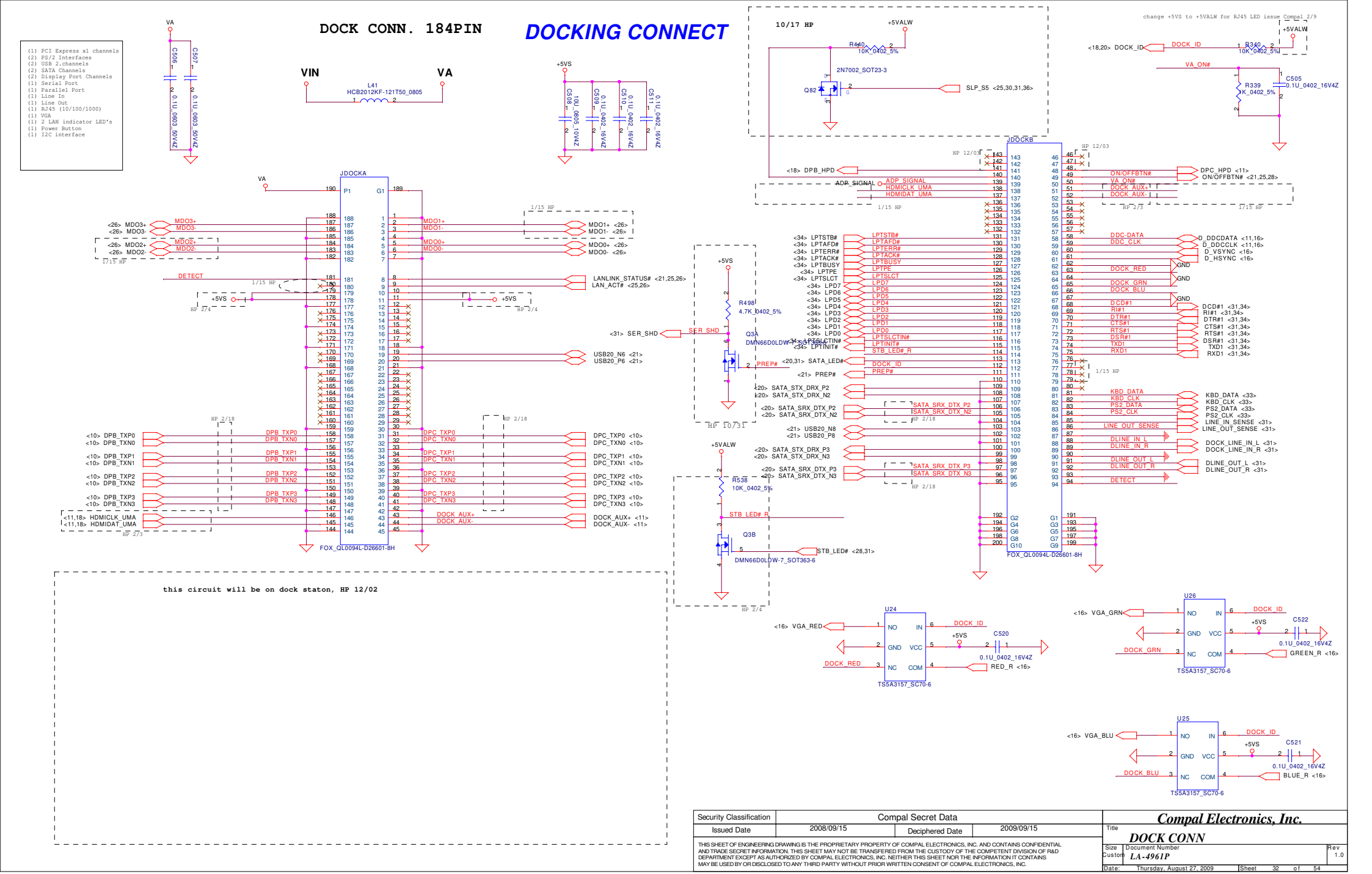
Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 31 of 54

DOCK CONN. 184PIN

DOCKING CONNECT

(1) PCI Express x1 channels
(2) PS/2 Interfaces
(2) USB 2.channels
(2) SATA Channels
(2) Display Port Channels
(1) Serial Port
(1) Parallel Port
(1) Line In
(1) Line Out
(1) RJ45 (10/100/1000)
(1) VGA
(1) 2 LAN indicator LED's
(1) Power Button
(1) I2C interface



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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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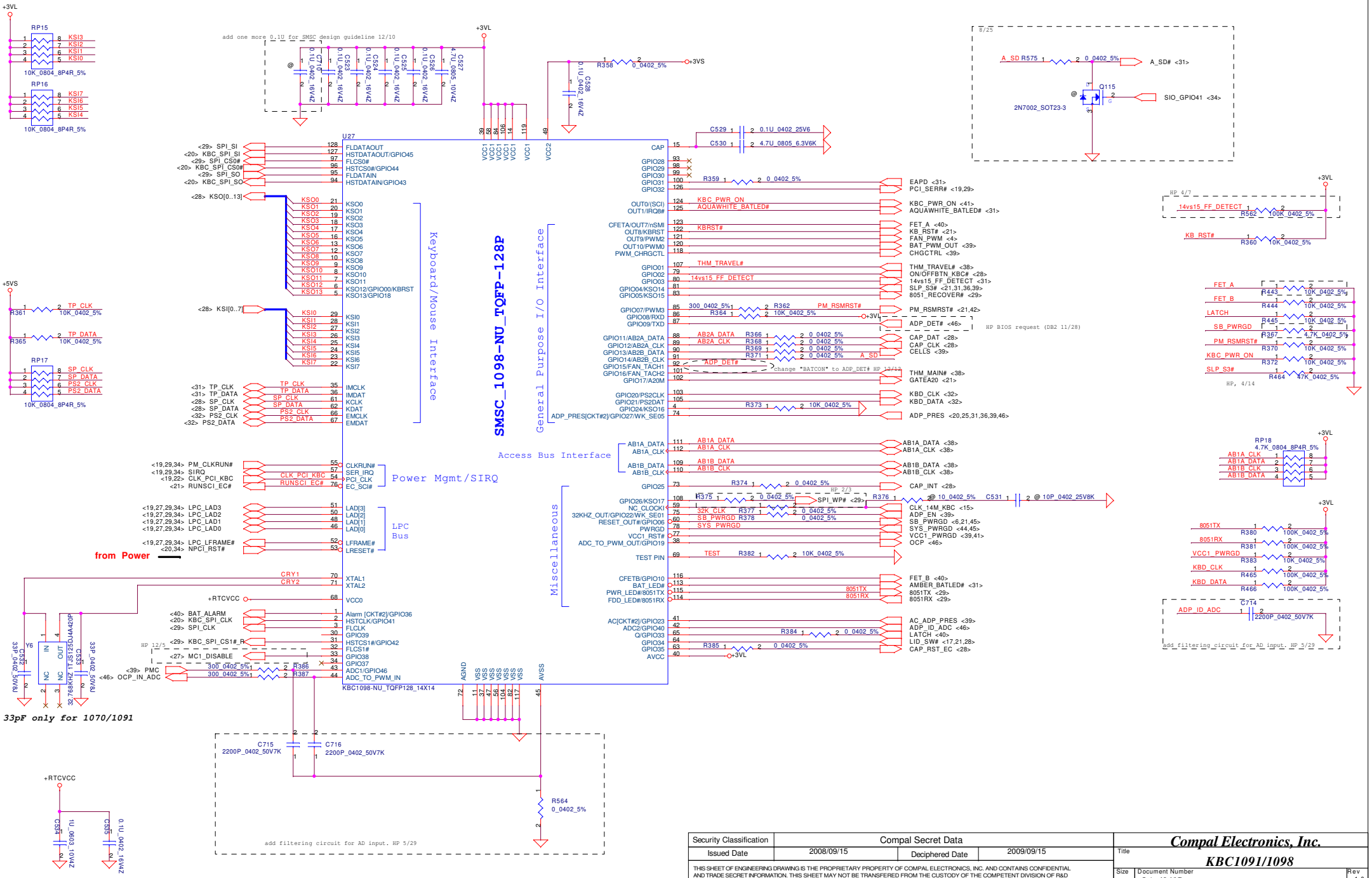
Compal Electronics, Inc.

Title: **DOCK CONN**

Size	Document Number	Rev
Custom	LA-4961P	1.0

Date: Thursday, August 27, 2009 | Sheet 32 of 54



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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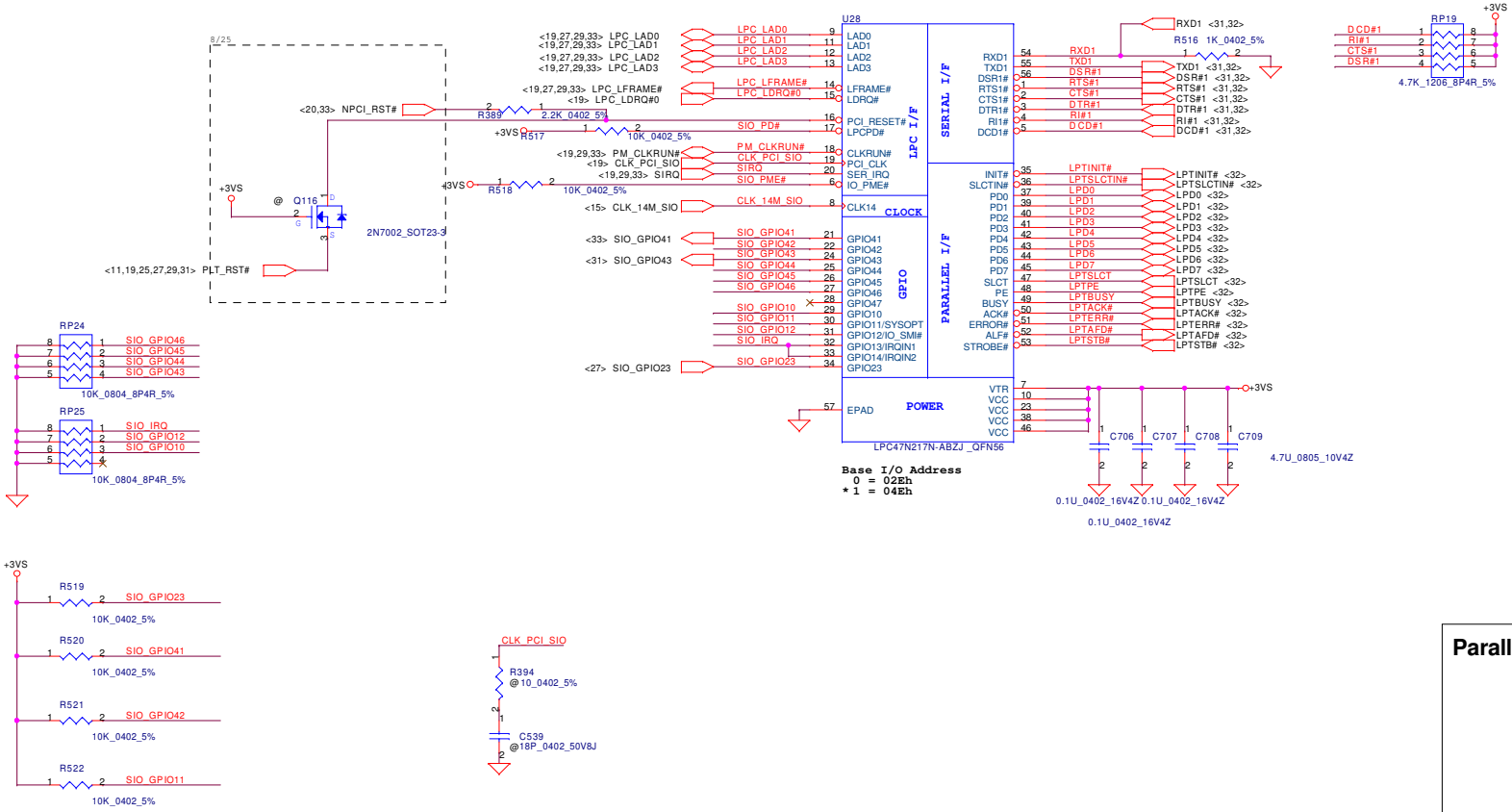
Compal Electronics, Inc.

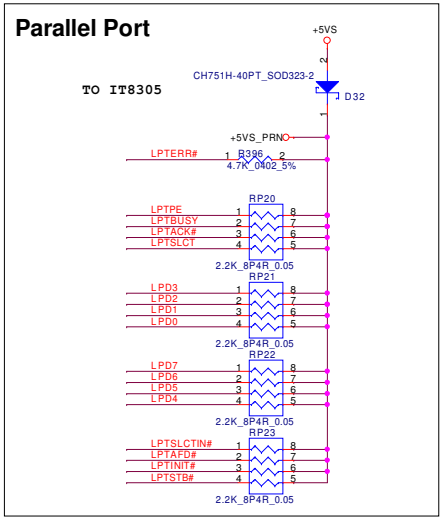
Title: **KBC1091/1098**

Size | Document Number: *LA-4961P* | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 33 of 54



Parallel Port



Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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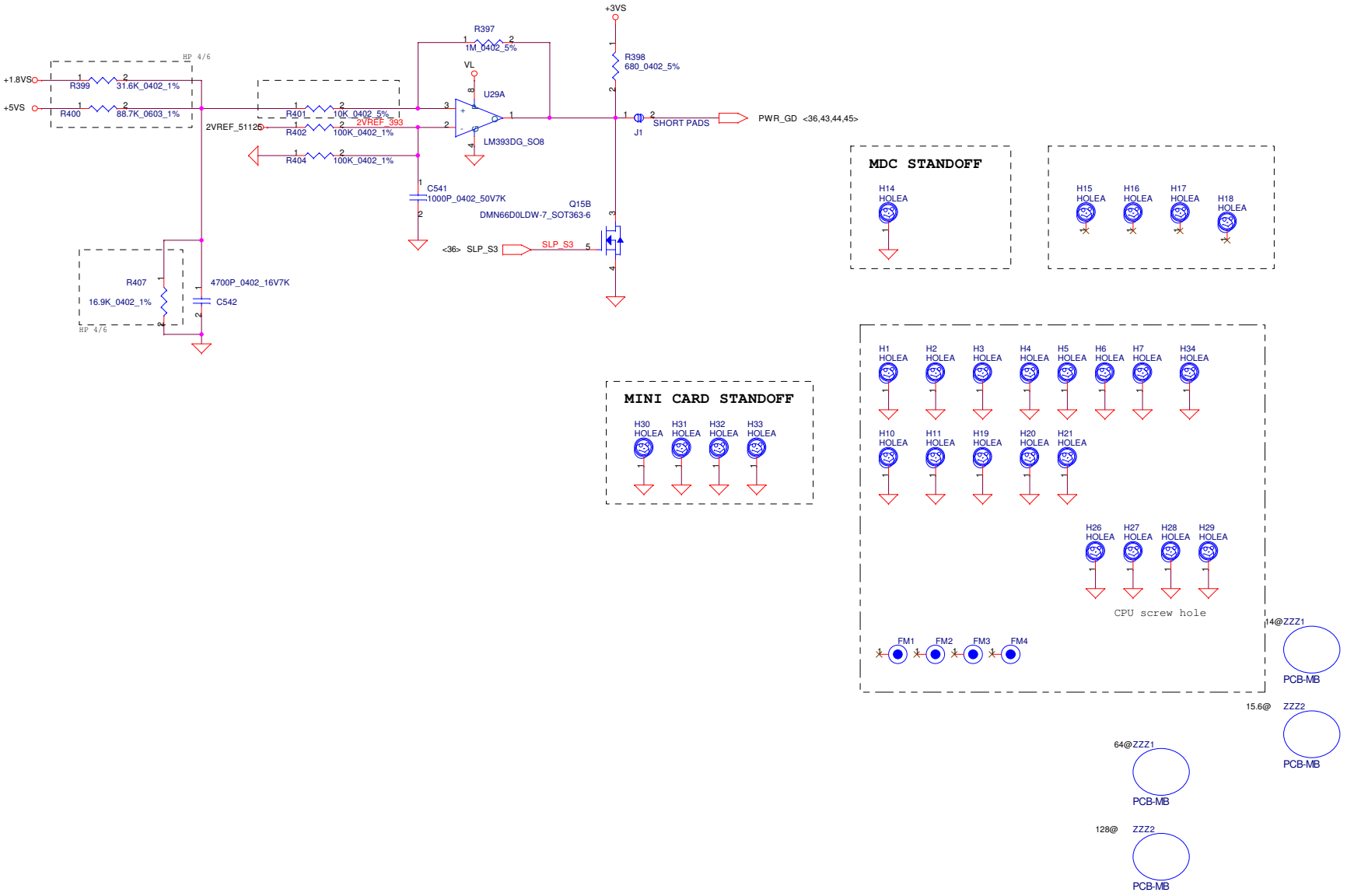
Compal Electronics, Inc.

Title: **Super I/O LPC47N217**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 34 of 54



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

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Compal Electronics, Inc.

Title: **POK CKT**

Size | Document Number: *LA-4961P* | Rev: 1.0

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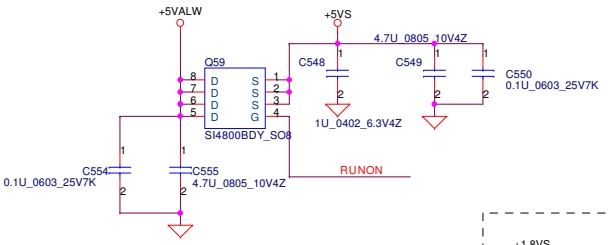
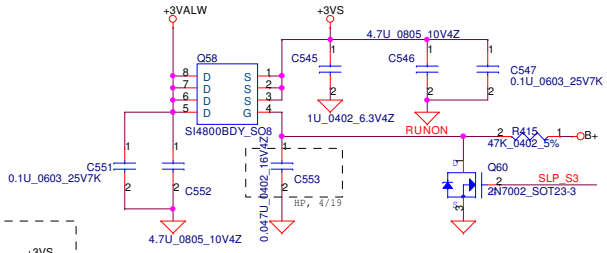
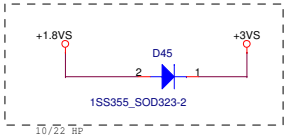
+5VALW TO +5VS

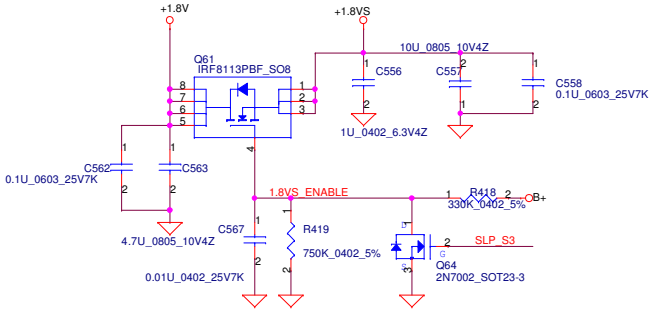


+3VALW TO +3VS

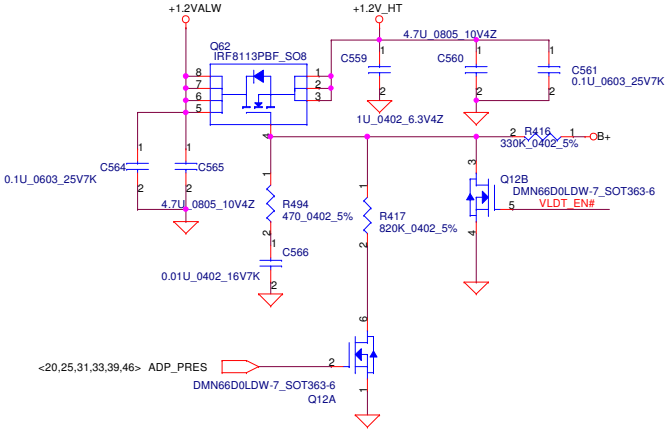




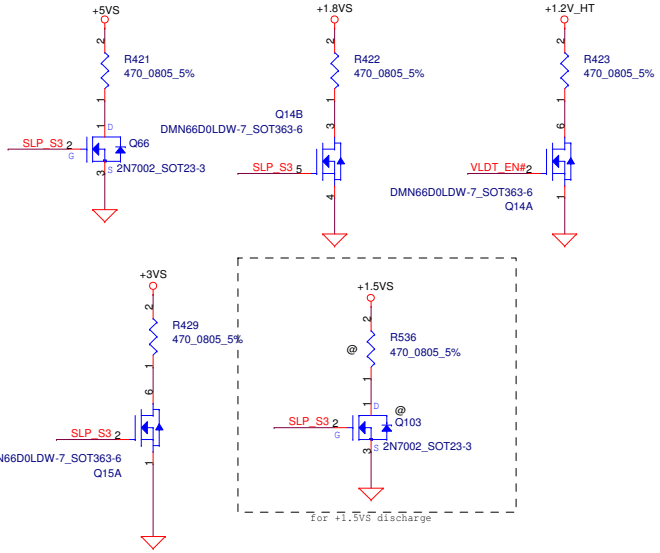
+1.8V TO +1.8VS

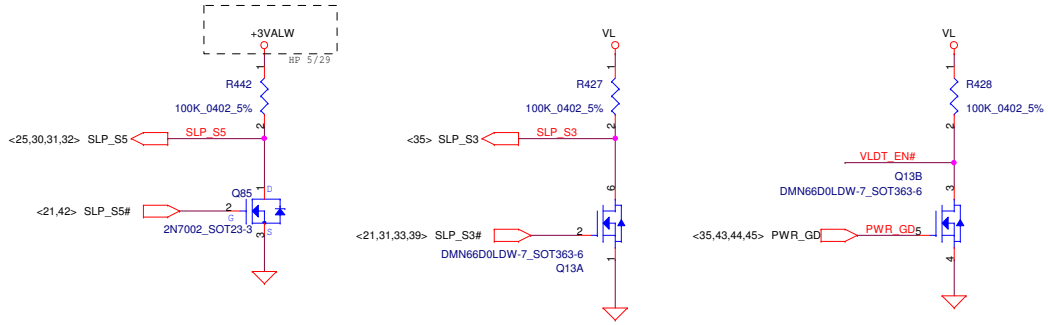


+1.2VALW TO +1.2V_HT



Discharge circuit





Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

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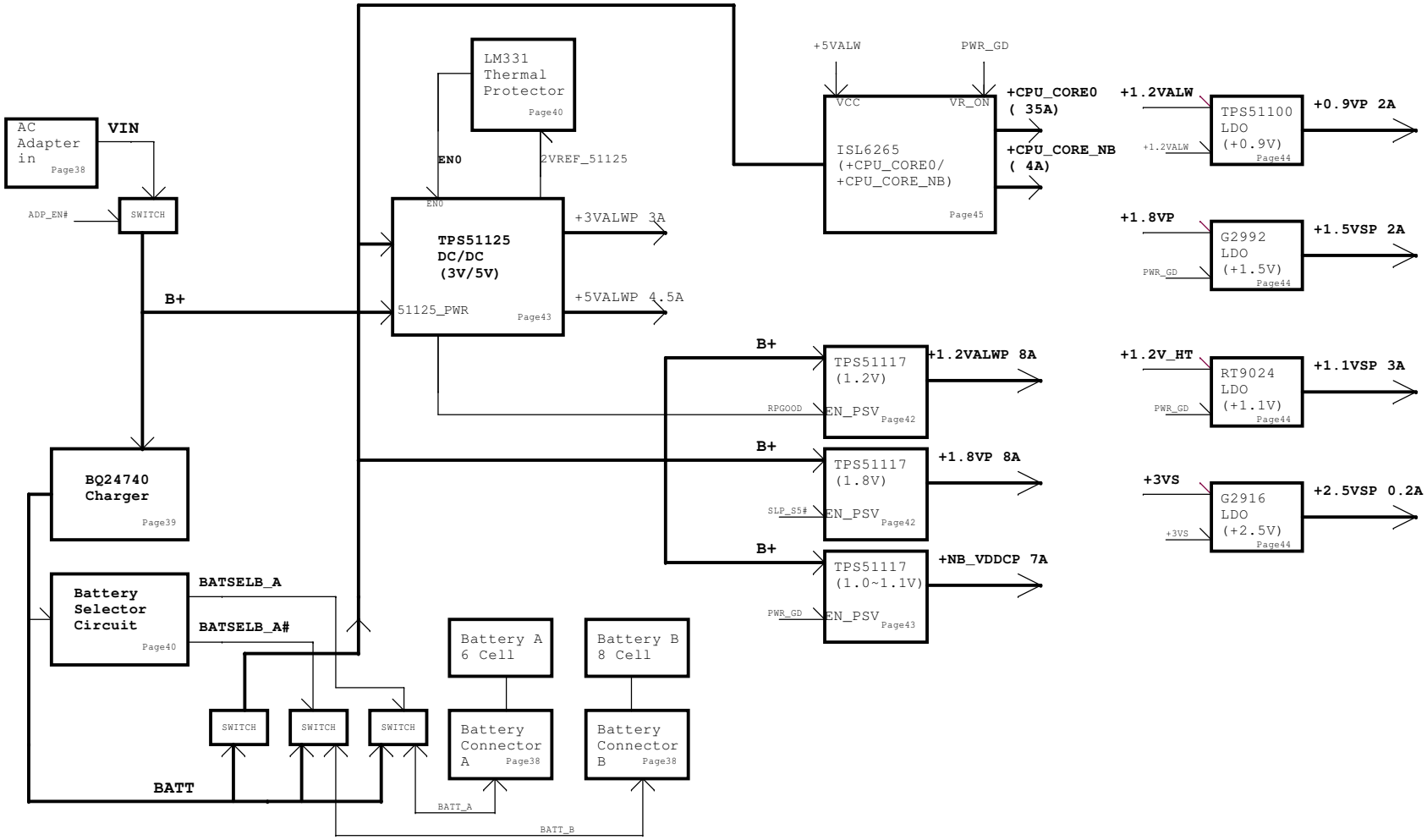

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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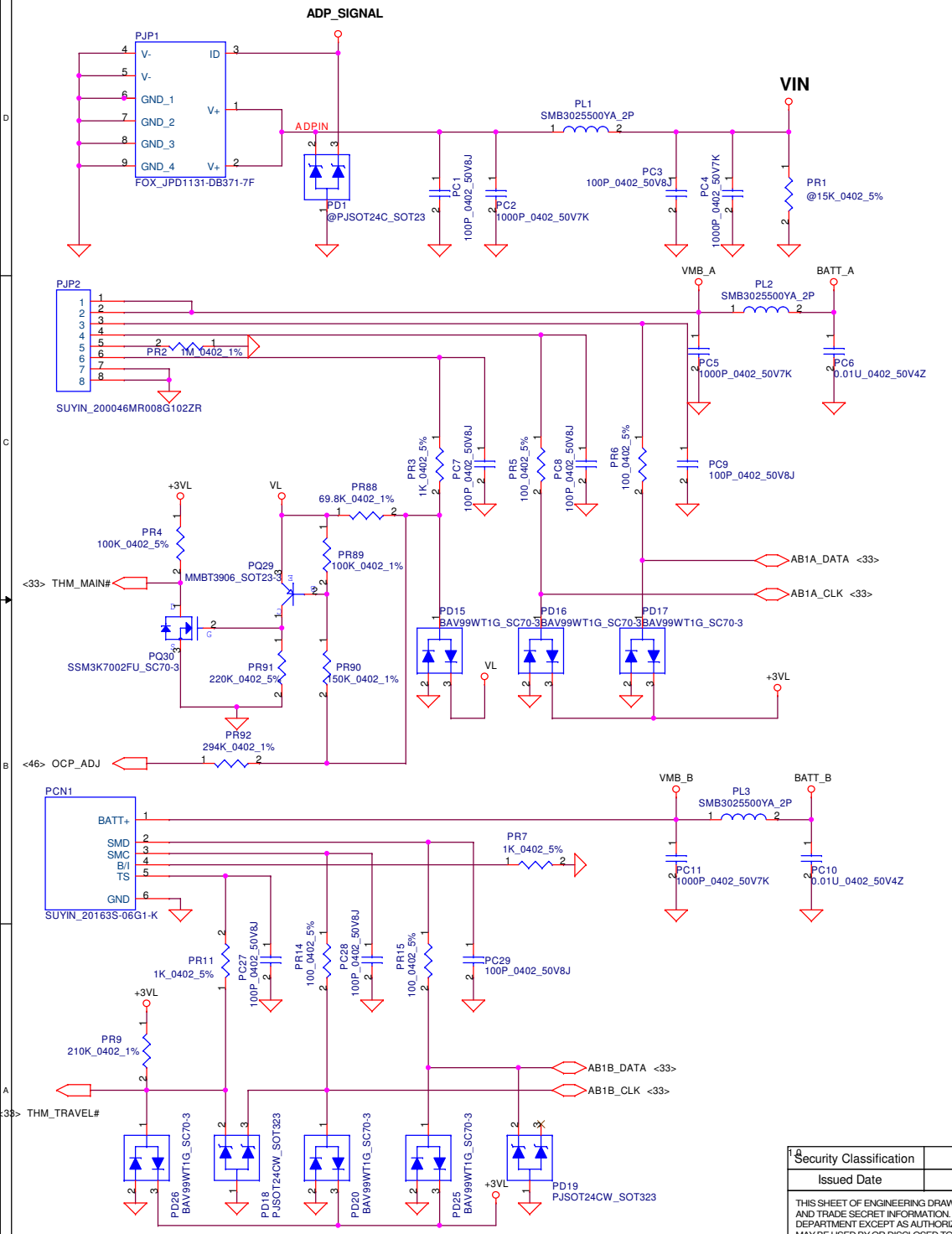
Compal Electronics, Inc.

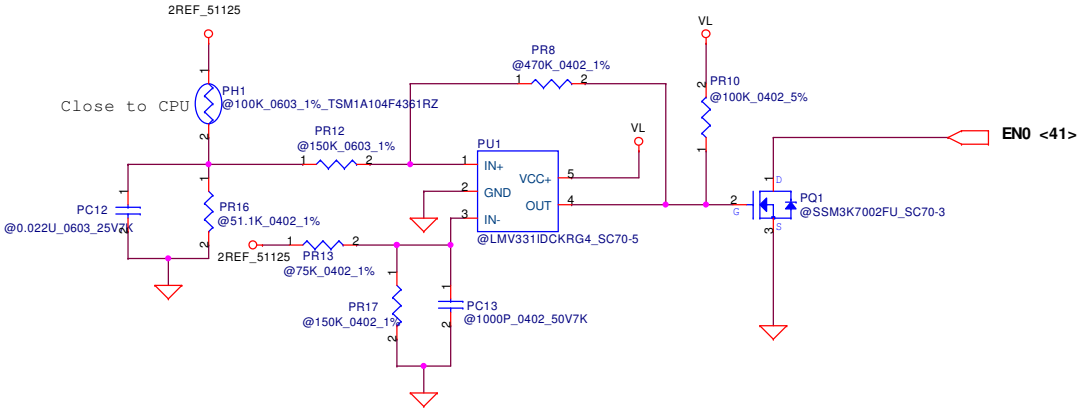
Title: **POWER BLOCK DIAGRAM**

Size: Custom | Document Number: LA-4961P | Rev

Date: Thursday, August 27, 2009 | Sheet 37 of 54



PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
(Need to be checked)



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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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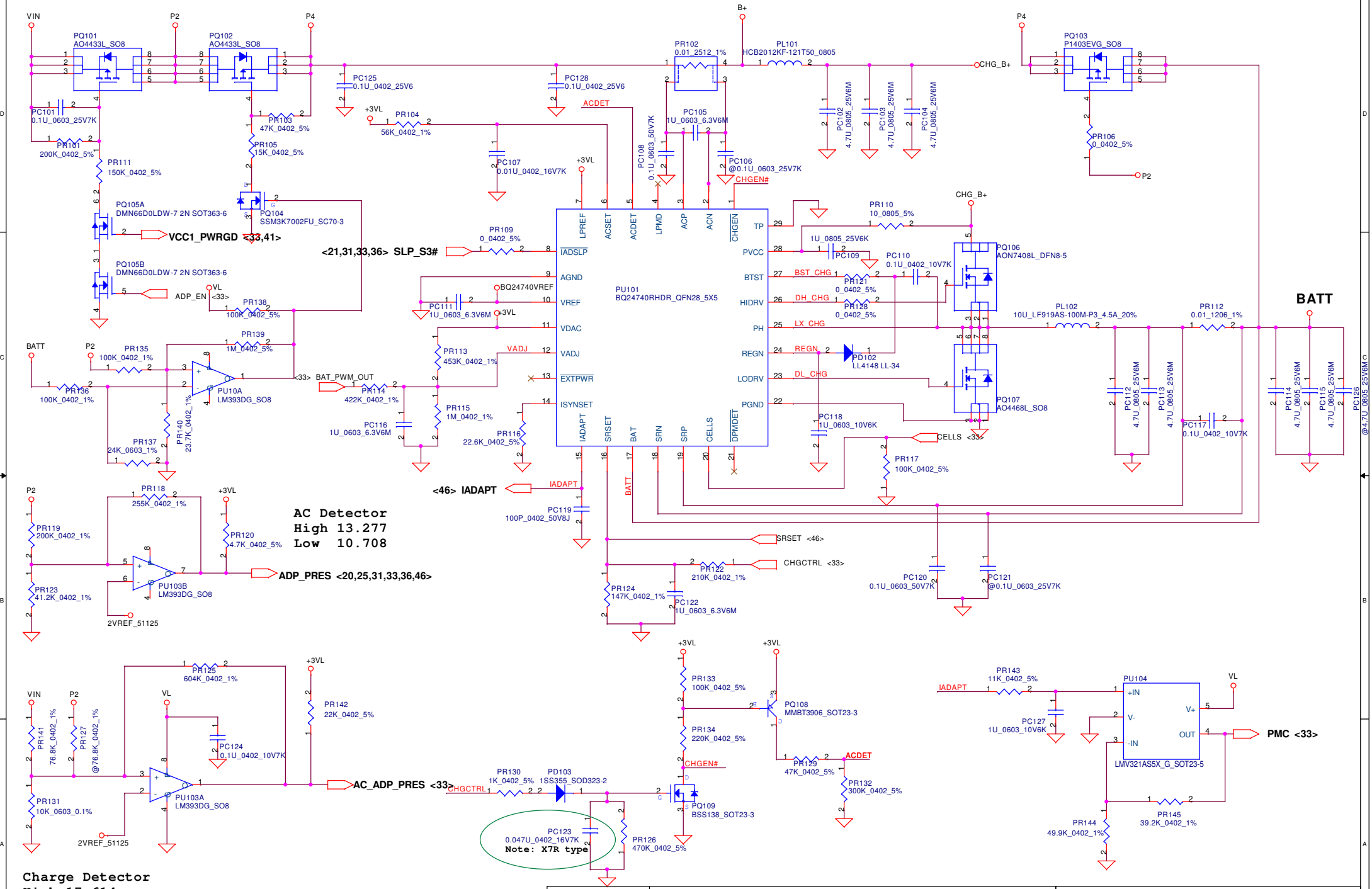
Compal Electronics, Inc.

Title: **DC-IN/ BATTERY CONN**

Size: Custom | Document Number: LA-4961P | Rev

Date: Thursday, August 27, 2009 | Sheet 38 of 54



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Compal Electronics, Inc.

Title: **Charger**

Size: | Document Number: *LA-4961P* | Rev: 1.0

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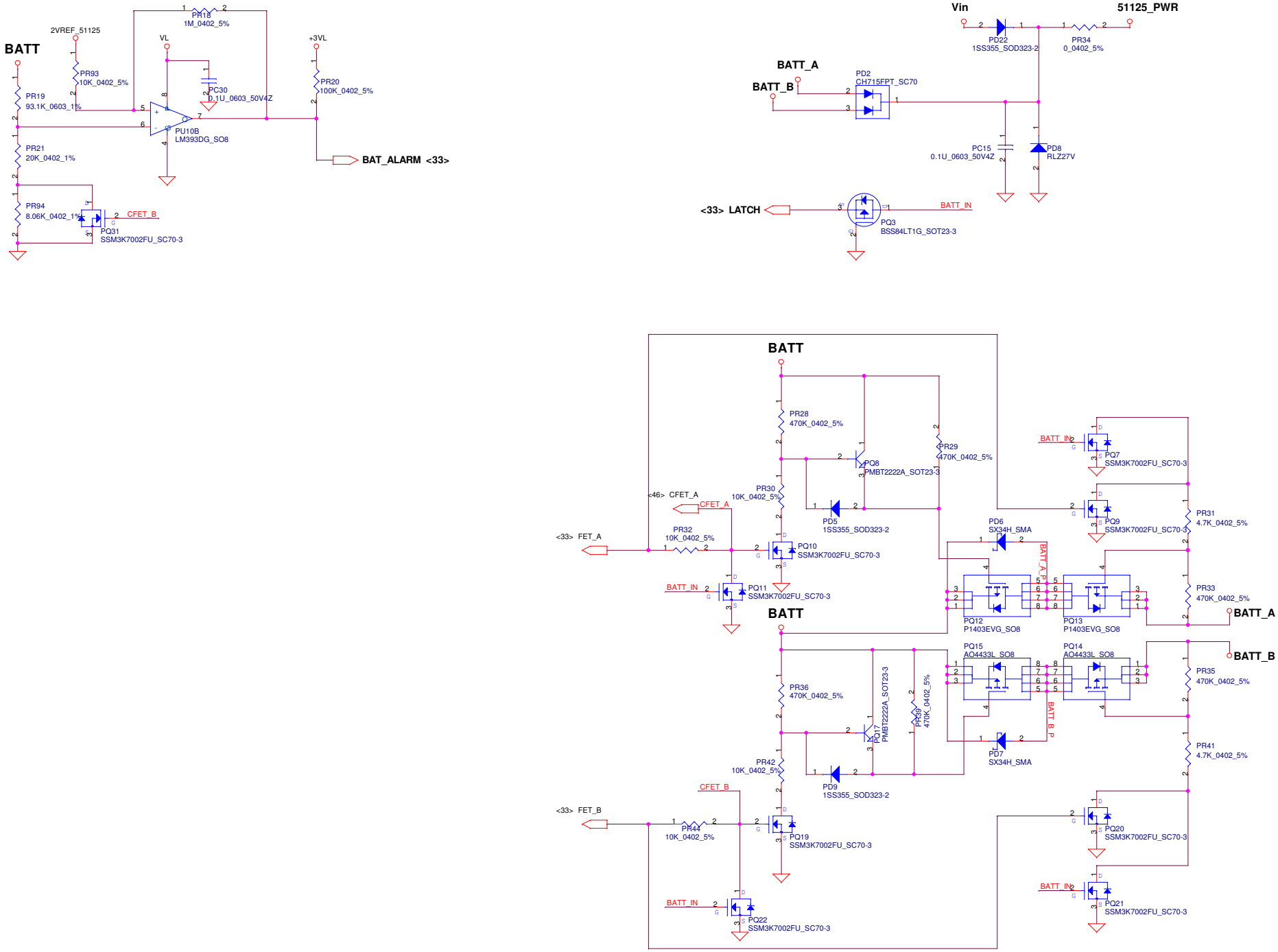

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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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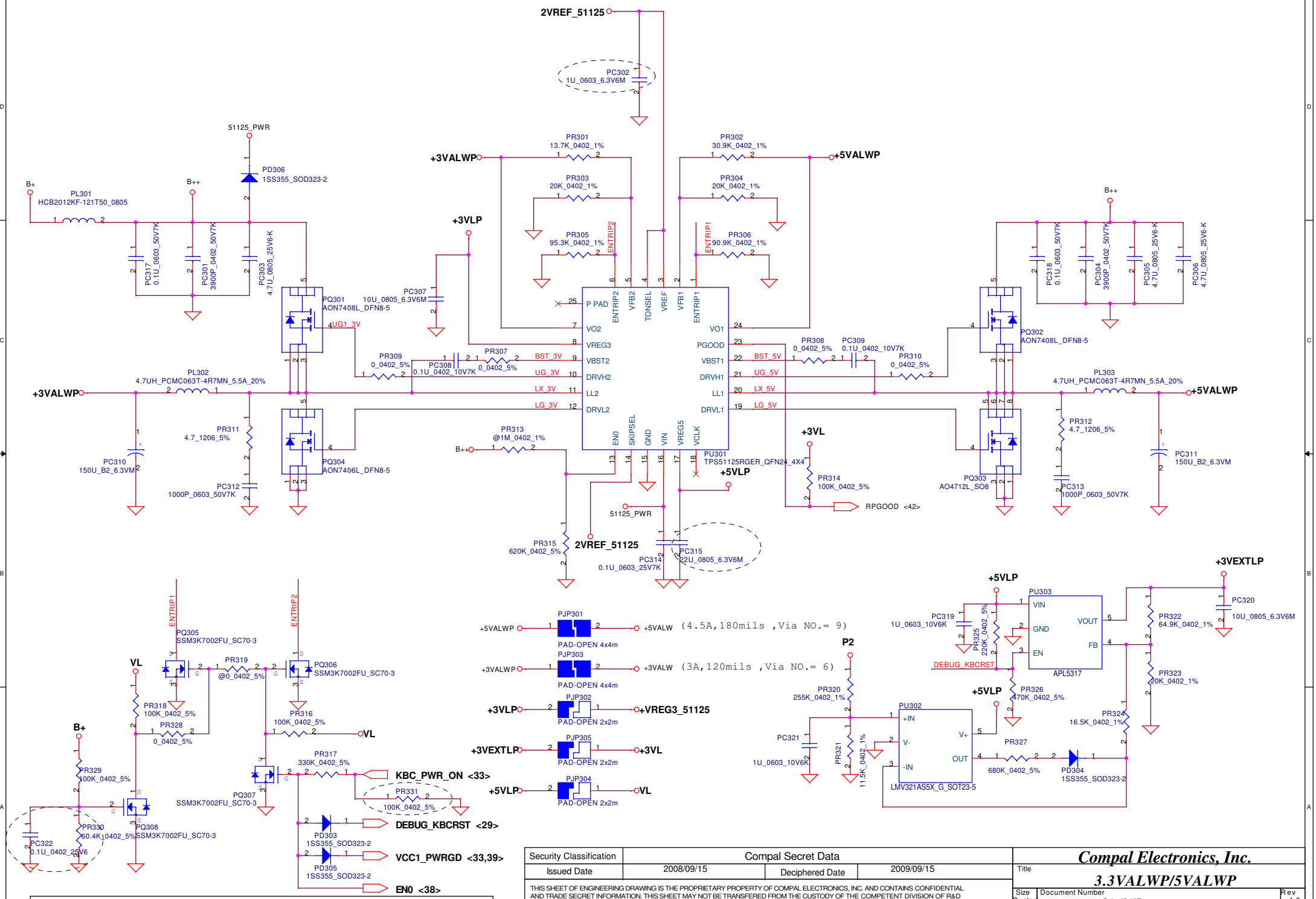
Compal Electronics, Inc.

Title: **Battery selector**

Size: Custom | Document Number: **LA-4961P** | Rev

Date: Thursday, August 27, 2009 | Sheet 40 of 54



Enable +5VALWP when DC mode for S5 power consumption

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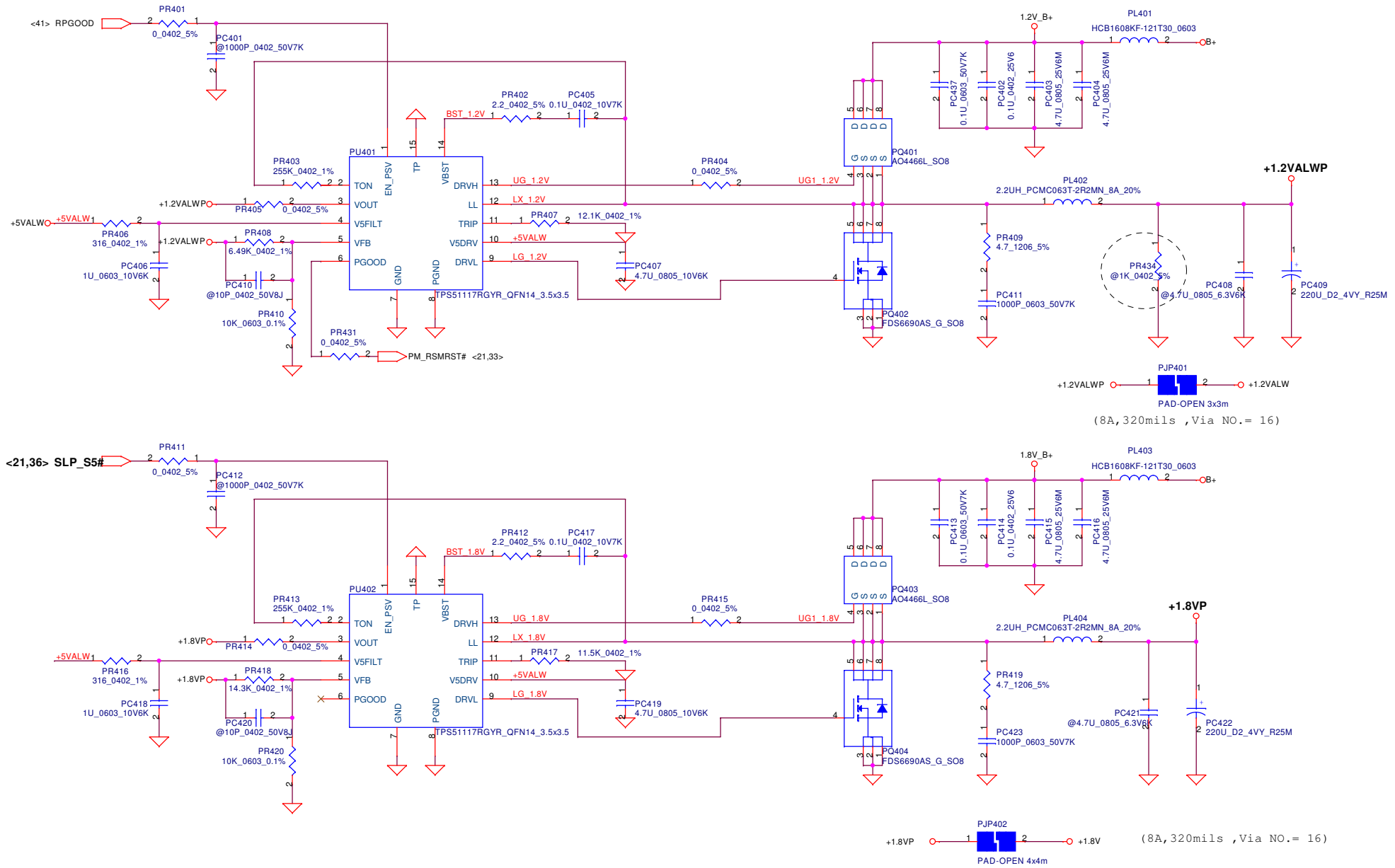
Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 41 of 54



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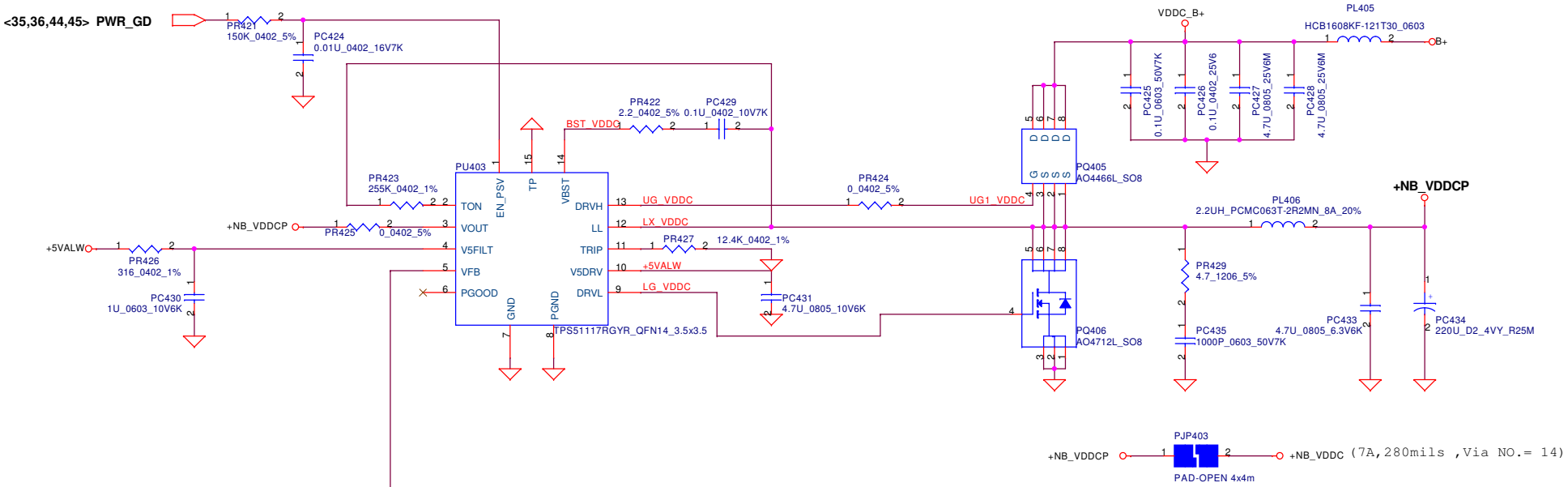
Compal Electronics, Inc.

Title: **1.2VALWP/1.8VP**

Size | Document Number: *LA-4961P* | Rev 1.0

Date: Thursday, August 27, 2009 | Sheet 42 of 54



DYN_PWR_EN	NB_VDDC
0	1.1
1	1.0

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

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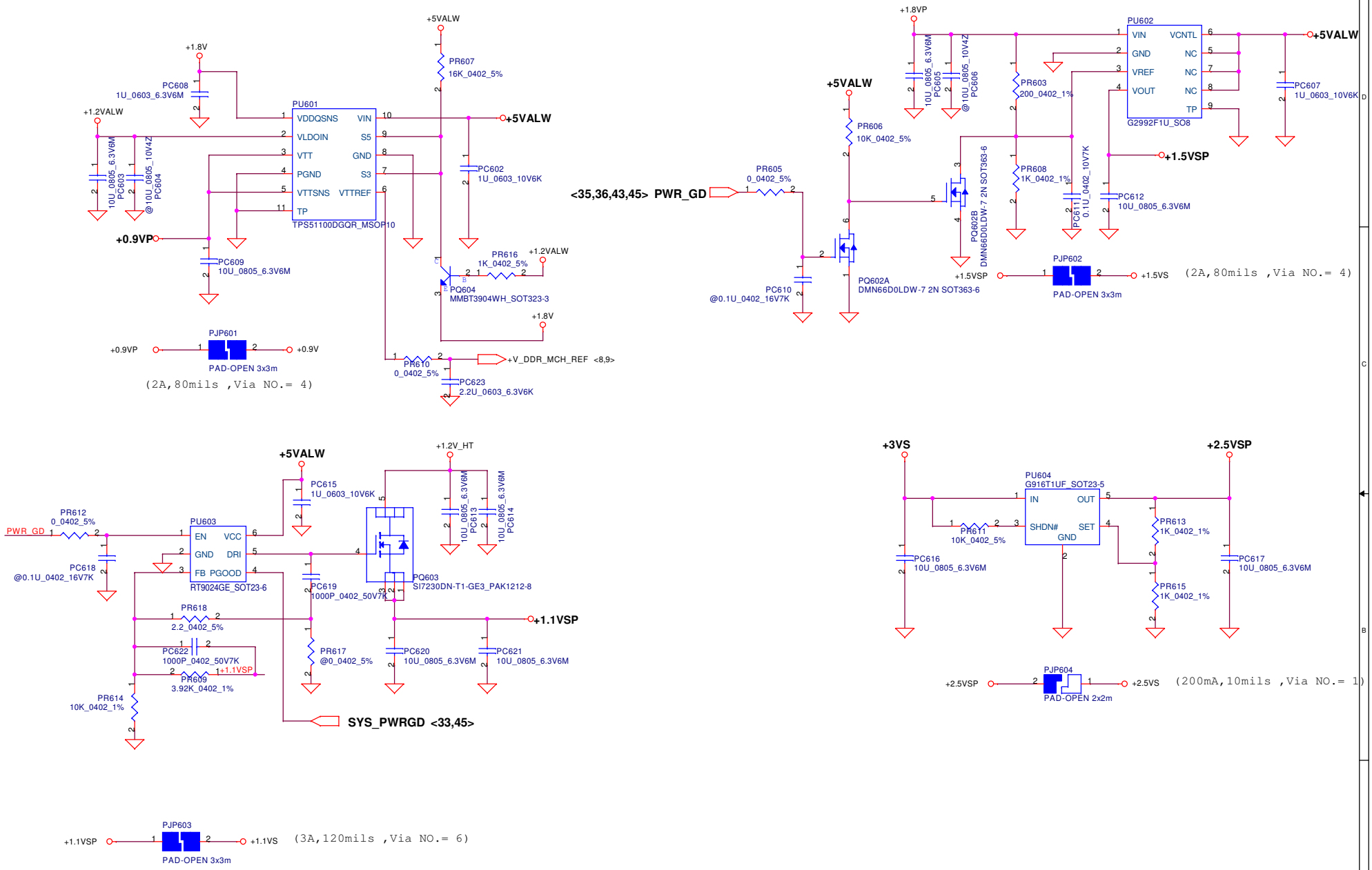
Compal Electronics, Inc.

Title: **NB_VDDC**

Size: Document Number: *LA-4961P* Rev: 1.0

Date: Thursday, August 27, 2009 Sheet 43 of 54



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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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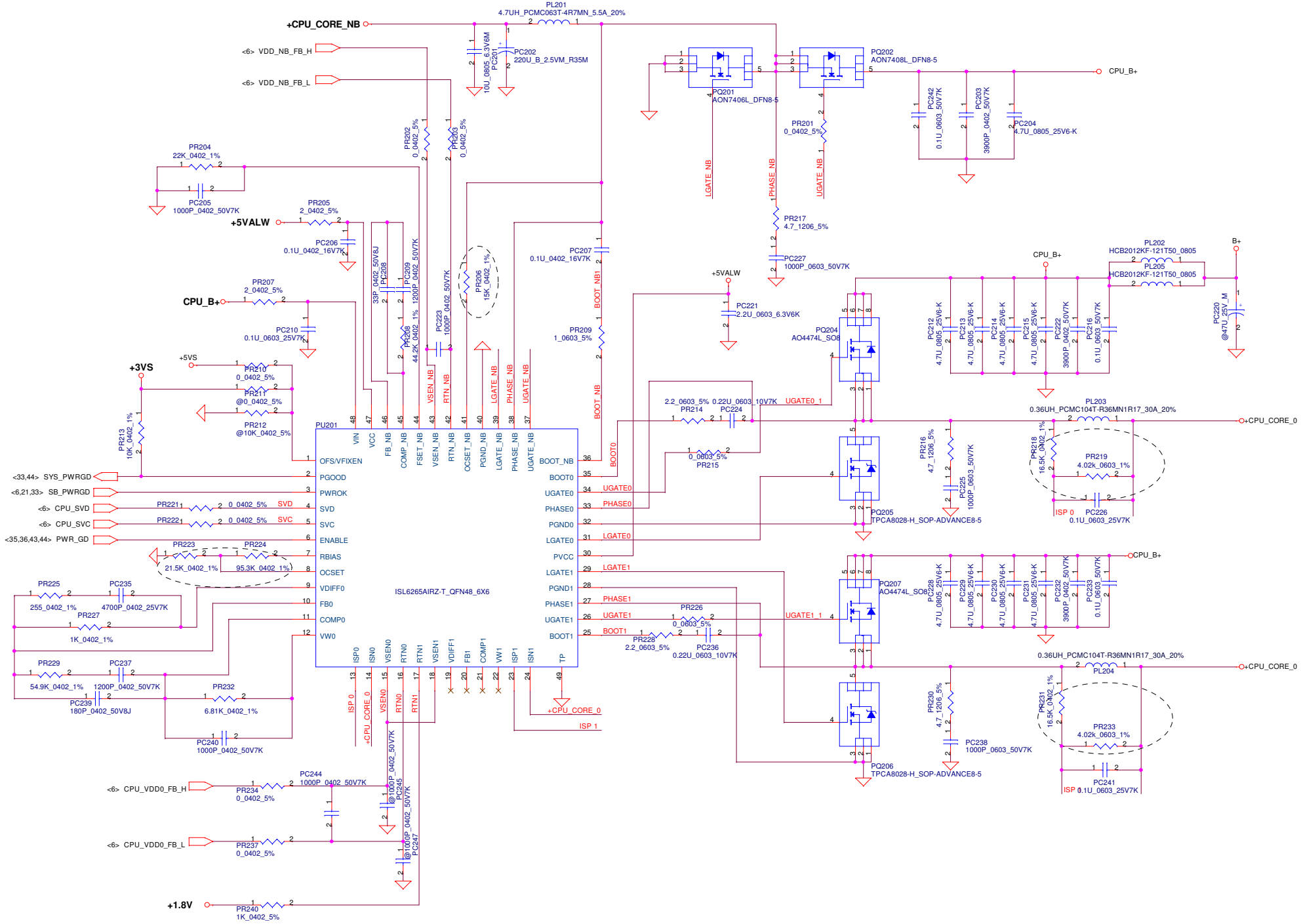
Compal Electronics, Inc.

Title: **0.9V/1.5VS/1.1VS/2.5VS**

Size | Document Number: *LA-4961P* | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 44 of 54



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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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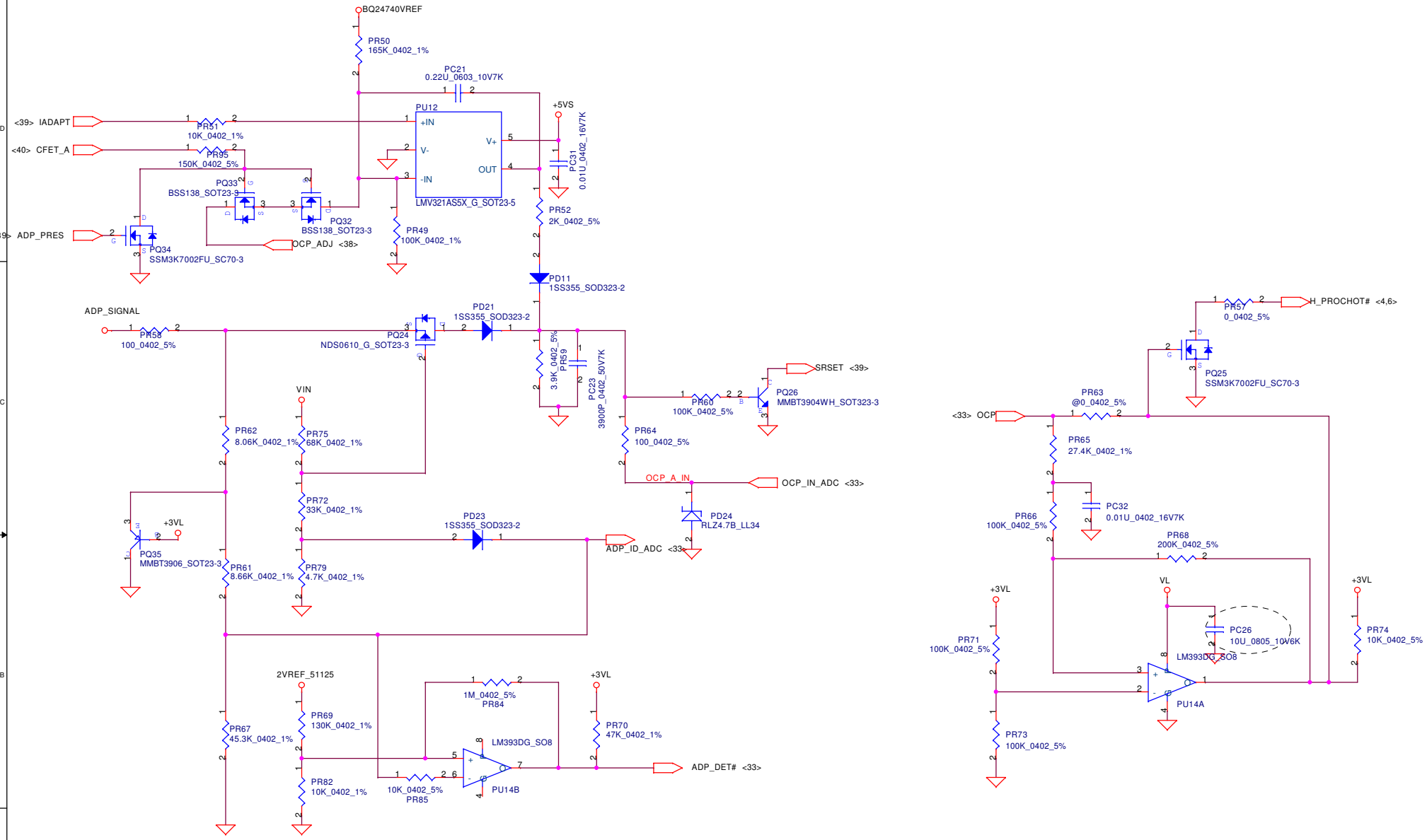
Compal Electronics, Inc.

Title: **CPU_CORE**

Size: Custom | Document Number: LA-4961P | Rev: 1.0

Date: Thursday, August 27, 2009 | Sheet 45 of 54



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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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Compal Electronics, Inc.

Title: **ADP_OCP**

Size: Custom | Document Number: **LA-4961P** | Rev

Date: Thursday, August 27, 2009 | Sheet 46 of 54

Item	Date	Phase	Reason for change	PG#	Modify List
1	2008/12/11	DB1-->DB2	BATCON circuit is removed due to SM5c 1098 design.	40	Delete PD10, PR45 and PU9
2	2009/01/16	DB2-->SI1	Modify circuit for Debug board	40	Change PR34 from 100 ohm to 0 ohm
3	2009/01/16	DB2-->SI1	Improve DDR termination power rail efficiency	44	Change DDR termination solution from G2992 to TPS51100
4	2009/01/22	DB2-->SI1	Modify the charger funtion	39	Modify the watch-dog circuit
5	2009/02/03	DB2-->SI1	Modify the Vin/Charge detector	39	Fine tune the trigger point
6	2009/02/03	DB2-->SI1	Modify the watch-dog sequence	39	Change PR133.1 and PQ108.3 to +3VL
7	2009/02/03	DB2-->SI1	Fine tune Power monitor setting	39	Change PR143 from 100 to 11K Change PR145 from 33K to 39.2K
8	2009/02/10	DB2-->SI1	Additional +3VL for KBC ADC accuracy	41	Add external +3VL LDO
9	2009/02/18	DB2-->SI1	Add +V_DDR_MCH_REF net	44	Add +V_DDR_MCH_REF net
10	2009/02/19	DB2-->SI1	For EMI request	39	Add PC125 and PC128 as 0.1u
11	2009/02/19	DB2-->SI1	Adjust NB_VDDC between 0.95V and 1.1V (instead of 1.0V and 1.1V).	43	Change PR430 to 23.7K_0402_1% and PR433 to 191K_0402_1%
12	2009/02/20	DB2-->SI1	For EMI request	41 45	3V/5V PR311/PC312:4.7ohm/ 1000pF PC317/PC301:0.1uF/ 3900pF PR312/PC313:4.7ohm/ 1000pF PC318/PC304:0.1uF/ 3900pF CPU CORE PR217/PC227:4.7ohm/ 1000pF PC242/PC203:0.1uF/ 3900pF PR216/PC225:4.7ohm/ 1000pF PC216/PC222:0.1uF/ 3900pF PR230/PC238:4.7ohm/ 1000pF PC233/PC232:0.1uF/ 3900pF
14	2009/04/07	SI1-->SI2	For HP's request, add a diode which connects the B++ and 51125_PWR	41	Add PD306 as 1SS355
15	2009/04/09	SI1-->SI2	To improve the power efficiency when S5 under DC mode, Re-connect the EN signal (ENTRIP1/2) to 2 singal N-MOSFET	41	Change PQ305 from 2N7002KDW-2N_SOT363 to SSM3K7002FU_SC70 Add PQ306 as SSM3K7002FU_SC70-3
16	2009/04/14	SI1-->SI2	Enable +5VALWP when DC mode	41	Add PR318 as 100K which is the pull high of PQ305.3 to VL Connect PQ305.3 to DEBUG_KBCRST
17	2009/04/16	SI1-->SI2	For EMI request	41	Change PD18 and PD19 from BAV99 to PJSOT24CW Delete PD20
18	2009/04/24	SI1-->SI2	Fine tune NB_VDDC power on sequence	43	Change PR421 from 10K to 150K Change PC424 from 1000P to 0.01u
19	2009/04/24	SI1-->SI2	Travel battery can not be detected issue	38	Change PR9 from 100K to 210K
20	2009/04/24	SI1-->SI2	For RF request	42 43	Add PC413,PC425 and PC437 as 0.1u Add PR409,PR419 and PR429 as 4.7 ohm Add PC411,PC423 and PC435 as 1000pF
21	2009/05/25	SI2-->PV	For S5 power consumption, reserve additional circuit to enable +5VALWP at battery mode	41	Add PR319 as 0 PQ308 as SSM3K7220FU PR329 as 100K PR330 as 15K PC322 as 0.01u Resserve PR328
22	2009/05/25	SI2-->PV	For AirLine adapter detection issue	39	Un-install PR127 Add PR141 as 78.6K between Vin and PU103.3 Change net name AC_AND_CHG to AC_ADP_PRES
23	2009/05/29	SI2-->PV	For HP request	42	Add a serial resistor (0ohm install) between pin 6 of PU401 and signal PM_RSMRST#.
24	2009/05/29	SI2-->PV	Because table of AC adapters has been expanded.	46	Change PR62 to 8.06K_1% PR61 to 8.66K_1% PR67 to 45.3K_1%
25	2009/05/30	SI2-->PV	Fine tune OCP setting	46	Change PR49 to 100K
26	2009/06/05	SI2-->PV	Enable +5VALW at S5 when battery mode	41	Uninstall PR319 Add PR328 as 0
27	2009/06/06	SI2-->PV	For EMI request (had been implemented at SI2)	42 43	Change PR402,PR412 from 0 to 2.2 Add PR409,PR419 as 4.7 PC411,PC423 as 1000p PC413,PC437 as 0.1u_0603 PC402,PC414 as 0.1u_0402 Change PR422 from 0 to 2.2 Add PR429 as 4.7 PC435 as 1000p PC425 as 0.1u_0603 PC426 as 0.1u_0402
28	2009/06/06	SI2-->PV	Fine tune power sequence for NB_VDDC (had been impelemented at SI2)	43	Change PR421 from 10K to 150K PC424 from 1000p to 0.01u
29	2009/06/06	SI2-->PV	Ensure the THM_MAIN# level lower enough when main battery be inserted (had been impelemented at SI2)	38	Change PR9 from 100K to 210K
30	2009/06/09	SI2-->PV	For HP request	44	Change PQ604 from 2N7002 to MMBT3904 Add PR616 as 10K
31	2009/06/09	SI2-->PV	For ESD request	38	Add PQ20, PQ25 and PQ26 as BAV99
32	2009/06/26	SI2-->PV (MEMO)	For HP's request	41	Change PR330 from 15K to 20K
33	2009/06/26	SI2-->PV (MEMO)	For HP's request	44	Change PR616 from 10K to 1K
34	2009/06/26	SI2-->PV (MEMO)	Fine tune Vsense feedback to prevnet feedback saturation issue	45	Change PR218 and PR231 from 3.65K to 16.5K PR223 from 100K to 21.5K PR224 from 17.4K to 95.3K PR206 from 14K to 15K Add PR219 and PR233 as 4.02K
35	2009/07/04	SI2-->PV (MEMO)	Fine tune enable signal level to make sure the switch can work normally	41	Change PR330 from 20K to 60.4K PC322 from 0.01u to 0.1u
36	2009/07/07	PV-->PV-R	Reserve a dummy load to prevent the leakage issue in the future. That issue has happened on PUMA platform	42	Reserve PR434 as 1K
37	2009/07/07	PV-->PV-R	Add a pull down resistor to prevent the floating of PQ307	41	Add PR331 as 1K
38	2009/07/07	PV-->PV-R	TI request to prevent LDO issue	41	Change PC302 from 0.22u to 1u
39	2009/07/15	PV-->PV-R	TI request to prevent LDO issue (Capacitance on VREG5 should be 33u at least)	41	Change PC315 from 10u to 22u PC26 from 1u to 10u

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	33	KBC 1098	11/28	HP BIOS	HP BIOS team design change	remove ADP_DET# signal connection from pin 80 of KBC to pin 87 (GPIO9)	0.2
~~2~~	~~29~~	~~LPC Debug port~~	~~11/28~~	~~HP BIOS~~	~~LPC debug card can't work~~	~~change JP21.16 conection from DEBUG_KBCRST to "51125_PWR"~~	~~0.2~~
3	29	VGA	11/28	HP	Design change for RS880M VGA I2C DDC	delete R101, R102, Q18,Q19	0.2
4	30,31	USB	12/1	Compal	all USB board can't work	change USB PWR switch enable signal from SLP_S5# to SLP_S5	0.2
5	4	Thermal senseor	12/1	Compal	System can't power on	thermal sensor change from ADM1032 to EMC1402	0.2
6	29	LPC Debug port	12/2	HP BIOS	LPC debug card can't work	change JP21.12 conection from "B+" to "51125_PWR" & change JP21.16 conection from "DEBUG_KBCRST" to "VCC1_PWRGD"	0.2
7	27	USB (WLAN conn)	12/2	HP	AMD platform is not support WiMAX	remove USB20_N9\P9 from WLAN connector (JP9)	0.2
8	27	WWAN	12/2	HP	HP Comm team design change	reserve R513 for LAN_PCIE_WAKE# of JP10 pin1	0.2
9	32	VGA	12/2	HP	VGA can't work issue	change DOCK_ID signal pullup power rail to +5VS	0.2
10	11	NB	12/2	HP	HP design change	change R61 from 10Kohm to 0 ohm	0.2
11	32	DOCK	12/2	HP	HP design change	remove Q23, Q5, Q6, R457~R460,R483,C682,C683	0.2
12	18	DP	12/2	HP	HP design change	remove C253, R467. add R514, Q98	0.2
13	17	LCD	12/3	Compal	Compal ME design change	change the LCD connector type	0.2
14	32	DOCK	12/3	HP	HP design change	remove SER_SHD signal & pin76 pullup 10k ohm to +5VS	0.2
~~15~~	~~25~~	~~NIC~~	~~12/3~~	~~HP~~	~~V1.2_LAN leakage issue~~	~~change power rail friom +1.2V_HT to +1.2VALW~~	~~0.2~~
16	32	DOCK	12/3	HP	all the FETs cicuit will be located inside docking station	All the CEC and CAD pins (143,46,142 and 47) will left as NC	0.2
17	34	Super IO	12/4	Compal	Compal design change	Change Super IO IT8305E to LPC47N217	0.2
18	15	CLK gen	12/4	Compal	Compal design change	add CLK_14M_SIO for Super IO & delete CLK_48M_SIO	0.2
19	9	DDRII	12/5	Compal	layout placement issue	cgange rsistor size from 8P4R to 0402	0.2
20	30	USB	12/5	HP	re-define the USB debug port (USB port 0)	Swap JUSB1 & JUSB2's USB signal	0.2
21	25	NIC	12/5	HP	V1.2_LAN leakage issue & improve layout	Swap power rail +1.2V_HT & V1.2_LAN	0.2
22	25	NIC	12/5	HP	HP recommand that 8075 is not needed	remove R246,R240,R241,R247,R244,R238,C421,U14 & USB signal	0.2
23	27	WWAM	12/5	HP	HP design change	add WWAM wakeup circuit	0.2
24	15	CLK gen	12/8	HP	Adding clk request signal for media/1394 daughter board for power saving benefit	change CLK_PCIE_CARD#/CLK_PCIE_CARD from pin25,26 to pin 22,23 & rename pin24 to CRD_REQ# & connect to JP29 pin20	0.2
26	4	CPU	12/8	HP	AMD S1G3 request for +1.2V_HT power rail	C1,C2,C7 change from 4.7U to 10U	0.2
27	26	WWAM	12/9	HP	HP design change	change R279 pin1 power rail from +3VALW to +3VS	0.2
28	4	FAN	12/10	HP	HP design change for RF	add R534	0.2
29	33	KBC	12/10	Compal	design change to meet SMSC guideline	add C710	0.2
30	31	KBC	12/12	HP	HP design change	change BATCON to ADP_DET# and connection Pin87 & pin92	0.2
31	18	Display Port	12/15	HP	add level shit control for DP	add Q102, R535	0.2
32	6	Leakage	12/18	HP	leakage fro +1.8VS	change power rail from +1.8VS to +1.8V	0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	KB connector	12/24	Compal	Key Board matrix error	Correct the right Key Board Matrix	0.3
2	26	LAN	12/31	Compal	LAN cable can't dectect	connection JRJ45 pin10 to GND	0.3
3	32	Docking	1/15	HP	Docking connector pin out error	delete pin 180 (PLT_RST#) & let it NC	0.3
4	32	Docking	1/15	HP	Docking connector pin out error	Swap pin assignment of pin2,3 & pin183,184	0.3
5	32	Docking	1/15	HP	Docking connector pin out error	Add connection for pin 51 to signal DOCK_AUX- pin 52 to signal DOCK_AUX+, pin 138 (HDMICLK_UMA) ,pin 137 (HDMIDAT_UMA)	0.3
6	32	Docking	1/15	HP	Docking connector pin out error	let pin77 & pin 78 NC pin because of the dock side is GND	0.3
7	32	Docking	1/15	HP	can't programing serial port by BIOS	SER_SHD signal (after Q96) connect to pin 10 of JP35 & let pin76 NC	0.3
8	25	NIC	1/15	HP	can't boot in DC mode	add Q2 to isolated when DC mode	0.3
9	31	WLAN_LED	1/15	Compal	WLAN_LED issue	correct the net name to WL/BT_LED#	0.3
10	28	MDC	1/22	HP	Modem disable GPIO is no needed	delete U17 RR173, connect HAD_RST#_MDC to pin 11 of MDC via a serial resistor (4.7K)	0.3
11	21	PWR on CKT	2/3	Compal	system auto power on after un-plug AC	change R179 power rail from +3VALW to +3VL	0.3
12	29,33	KBC	2/3	HP	for SPI lock feature & only apply to AMD platform	change R375 to 0ohm & connect to U19 pin3	0.3
13	32	Docking	2/3	HP	Display port working not right	Swap pin 146 and pin 145 connection	0.3
14	32	Docking	2/3	HP	Display port working not right	swap pin 52 and pin 51 connection	0.3
15	31	card reader	2/3	HP	to beefup with enough decoupling cap on MB	change C684 from 0.1U to 4.7U	0.3
16	32	Docking	2/4	HP	docking station design change	change pin11, pin178, oin179 from NC to +5VS	0.3
17	32	Docking	2/4	HP	docking station power LED abnormal	add Q3 for invert STB_LED# signal behavior	0.3
18	20 23	SB710	2/5	HP	for improve battery life	remove IDE PATA controller and flash controller power rail +3VS) & connect pin 1 of R170 to pin M5 of SB710	0.3
19	17	LCD Panel	2/6	HP	LCD Panel flashing issue	remove R106, D41 & add R540	0.3
20	17	card reader	2/6	HP	for power-down of 1394/cardreader chip when no card/1394 inserted	add Q104~Q107, R541~R543	0.3
21	11 18	DP	2/6	HP	design change	change R60 & R125 from 20k to 100K ohm	0.3
22	32	Docking	2/9	Compal	RJ45 green LED doesn't light with cable while system power off with AC in	change the R340 power rail from +5VS to +5VALW	0.3
23	30	USB	2/10	HP	correct the USB debug port 0 location	swap JUSB2 & JUSB3 signal	0.3
24	19	RTC	2/11	HP	for RTC battery life issue	change D43 pin2 power rail from +3VL to +VREG3_51125	0.3
~~26~~	~~19~~	~~SB710~~	~~2/12~~	~~HP~~	~~port 9,10,11 are un-used and BIOS can disable the one OHCI controller~~	~~change the USB port from port 11 to port 12~~	~~0.3~~

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27	25	NIC	2/14	HP	design change for 8059 (co-lay)	add R544~R548	0.3
28	31	Audio Express	2/17	HP	to improve battery life	change both pin 21 of JP34 and pin 1 of C646 connection to +VREG3_51125 (from +3VL	0.3
29	20	VRAM ID	2/17	Compal	add VRAM ID for side poert memory 2nd source	add R549, R550,R551,R176	0.3
30	32	Docking	2/18	HP	DP's 16 AC coupling remove to docking station	deletet C659~C666, C512~C519	0.3
31	32	Docking	2/18	HP	SATA's 4 AC coupling remove to docking station	deletet R342~R345	0.3
32	32	Docking	2/19	Compal	due to DP current is 500mA	change F2 from 3A to 0.5A	0.3

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1	25	NIC	3/23	HP	power-down NIC instead of low-power mode	add Q34, R554, C712, R555, Q107 & delete R186, R239	0.4
2	4	Fan	3/23	Compal	Fan shake when temperature in 70 degree	add Q108, C556 & C557	0.4
3	31	card reader	3/24	HP	1394 detection circuit design change	delete R533, R552,R543 & add R559, R558, Q108	0.4
4	29	SPI	3/25	HP	SMsC recommand to add 100k ohm fro select pin	add R560	0.4
5	27,25	WLAN, NIC	3/25	HP	power MOSFET can not be fully shutoff with +3V/+5V level	change R277 power rail from +3VS to +5VS & change R277 from 680 to 47k & R272 from 220K to 100K, R234 change power rail to +5VALW & change to 10K	0.4
6	27	WLAN	3/25	HP	HP design change	delete CLK_PCIE_WLAN_REQ# from JP9 pin 7 & connect CLK_PCIE_WLAN_REQ# to WLAN_OFF	0.4
7	27	SB710	3/25	HP	HP design change for GPIO56	connection CRD_REQ#_R to GPIO56	0.4
8	4, 6	CPU	3/30	HP	HP design change for CPU Thermal	change Q10 pin2 power rail from +1.8VS to +1.2V_HT & connection thermal sensor pin4 (thermal#) to CPU dirtertly.	0.4
9	27	WWAN	3/31	HP	HP design change for WWAN dection pin	contion JP10 pin26 to Super IO GPIO23	0.4
10	28	Point stick	4/1	Compal	Point Stick pin out error	Swap from pin1 to pin8	0.4
11	33	KBC	4/6	HP	BOM change	change pull down resistor on FET_A R443 from 1.2K to 10K; Change pulldown resistor on SB_PWRGD R367 from 1.2K to 4.7K	0.4
12	35	PWR OK	4/6	HP	BOM change	change PWR_GD resistor values - change R399 to 31.6K_1%, change R400 to 88.7K_1%, change R407 to 16.9K_1%, change R401 to 10K_5%	0.4
13	6	CPU	4/6	HP	BOM change	change R35 value to 560 ohm (instead of 300 ohm)	0.4
14	28	LID SWITCH	4/6	HP	LID_SW# is triggering very intermittently and cause lockup in POST B173	add Q110 & C713	0.4
15	21	power button	4/7	HP	Press twice power to power on in DC mode	change R179 to 4.7K	0.4
16	31, 33	KBC	4/7	HP	design change for detect 14" & 15.6" panel	add GPIO03 (14vs15_FF_DETECT) on KBC	0.4
17	26	NIC	4/8	HP	HP design change for LED, NIC is locate on the rear, not side of system. So, after docking, even NIC leds on NB side is blinking, users will not see it,	delete Q37 & Q38	0.4
18	17, 29	LCD & FP	4/8	HP	to make sure can turn off the power MOS	change the G gate of MOS to +5VS & +5VALW	0.4
19	26	NIC	4/9	HP	HP design change to simplified circuit	delete Q1B, R553	0.4
20	20	SB710	4/9	HP	HP design CPPE_NC# connection	CPPE_NC# connect to U10.C4 (GPIO55)	0.4
21	17	WebCan	4/11	HP	in order to support new Webcan	delete Q24, C248, R113 & R446, R174.then connect CARMERA_OFF to MOS G gate.	0.4

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22	21	SB710	4/13	HP	add a 10K pull-down resistor to signal "SLP_S5#"	add R563	0.4
23	20	NIC	4/13	HP	BOM change	change C712 to 0.022uF (from 0.1uF)	0.4
24	33	KBC	4/14	HP	add pull-down resistor to signal "SLP_S5#"	change R464 connection from +3VLto GND	0.4
25	32	docking	4/17	HP	design change	connect pin 2 of Q3A to signal PREP#, dock pin 111	0.4
26	36	DC-DC	4/19	HP	to fine turn power on sequence	change C553 from 0.01U to 0.047U	0.4

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1	25	NIC	5/9	HP	can't power on in AC mode due to PWR_GD be drive to low	delete R555, R512. change R499 pin2 from runon to B+. change Q79 power source from V1.2_LAN to +1.2VALW	0.5
2	27	WWAN	5/29	HP	Change WWAN circuit to follow what HP comm team, & power down WWAN card	delete R279, R528, Q99 & change Q100 pin5 power rail from +3VALW to +3VS	0.5
3	25	NIC	5/29	HP	to support LAN/WLAN switch	add FET Q111	0.5
4	33	KBC	5/29	HP	add filtering circuit for AD input	add C714, C715, C716,R564	0.5
5	20	SB710	5/29	HP	delete the SATA decoupling cap, Because the caps are located in docking station side already	delete C289~C292	0.5
6	36	DC-DC	5/29	HP	DC mode can't power on issue	connect R442.1 pin to +3VALW (instead of VL)	0.5
7	20	SB710	5/29	HP	for AMD vidoe driver reques	connect R175.2 to signal DOCK_ID (instead of GND) , and make R175 to 100K	0.5
8	31	card reader	6/4	HP	reserve 0 ohm for CRD)REQ#	add R565	0.5
9	13	sideport memory	6/5	AMD	AMD SCL suggection:Connected a 100-? 1% resistor between MEM_CKP and MEM_CKN (not installed by default).	un-install R68	0.5
10	31	card reader	6/8	HP	some 1394 not detected	add Q23, R566	0.5
11	25	NIC	6/8	Compal	in order to improve the placement	combine Q111 & Q97 as dual FET Q19	0.5
12	31	card reader	6/9	HP	the power down feature for BIOS (The idea is to have BIOS SIO GPIO control, if that GPIO is high, the circuit is enabled. If the GPIO is GPI or low, the power-down circuit then disabled.)	add R565, R567, C717,C718	0.5
13	18	DP	6/11	AMD	AMD require a blank time on HPD signal when docking station and NB both have DP. The change basically will block DPB HPD for a 100ms becuase pass through	delete R124, R514 add Q113,R568,R569,C719	0.5
14	27	WWAN	6/11	Compal	MC1_DISABL is open drain seeting need pull high, and +3V_WWAN need discharge circuit	addR570, R571, Q114	0.5
15	8	DDR	6/11	Compal	EMI request 0.1UF cap for +1.8V	add C720, C721	0.5
16	6	CPU	6/12	HP	HP request add 1k resistor between Q10.2 and LDT_RST#.	add R572	0.5
17	17	webcam	6/13	Compal	EMI request add com-choke for webcam	add L49	0.5
18	31	WWAN	6/13	HP	WWAN LED abnormal when power down	chajnge Q53 pin2 power rail from +3VS to +3V_WWAN	0.5

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1	30	USB	6/20	Compal	change C485, C491,C690 footprint for 2nd source	change footprint from C_D to C_D2E	0.6
2	21, 28	SMSC CBB	7/4	HP	for SMsC CBB utilized the Lid#.	move Q110 close to SB710 and pull high LID_SW#	0.6
1	31	card reader	8/13	HP	card reader can't detect & reduce power consumption	remove C718 and change R558 to 47K ohm	1.0
2	33	Audio	8/24	HP	there is the po-po sound when warm boot	add Q115, R575,Q116	1.0

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