

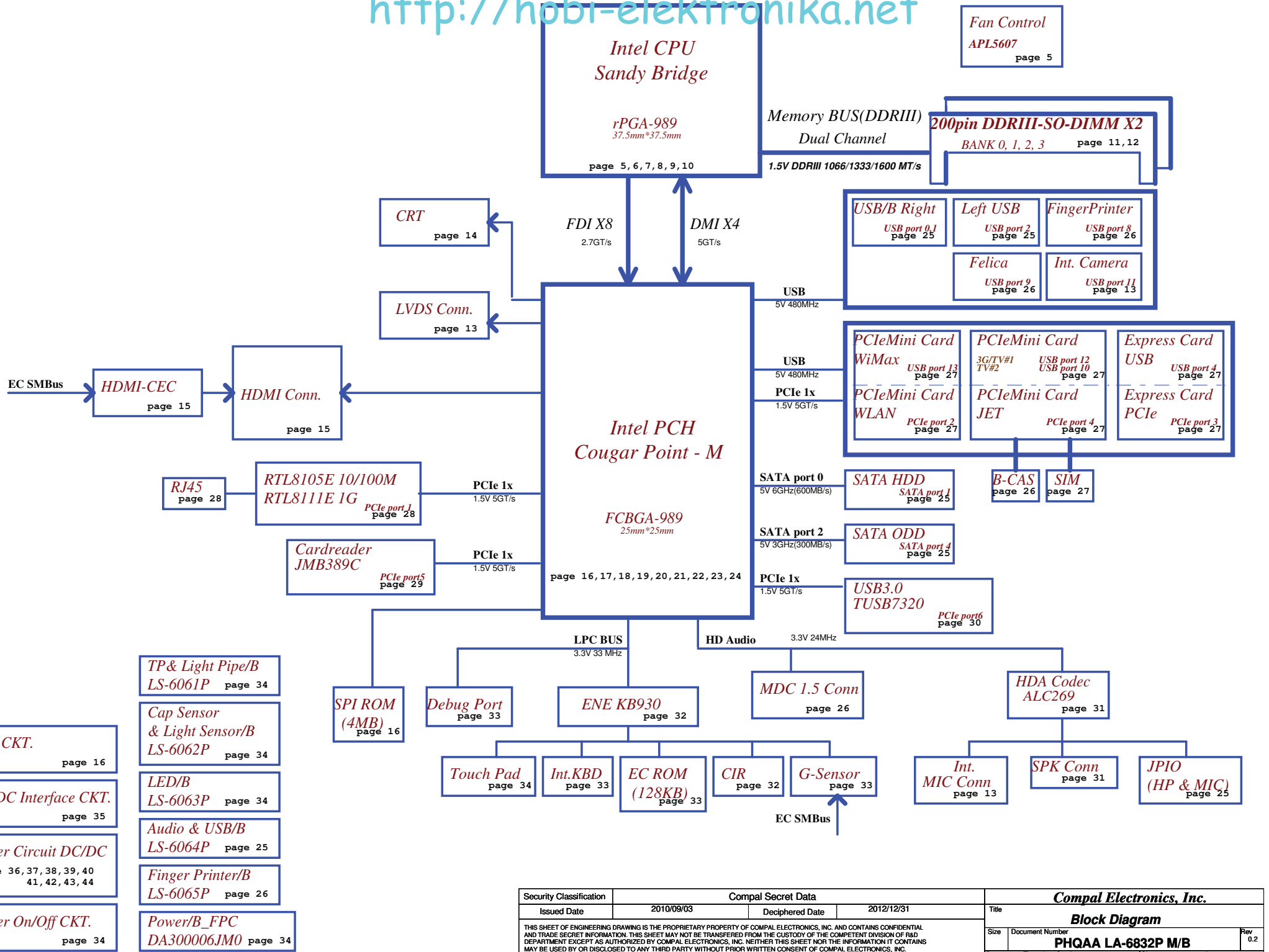
PHQAA

Marseille 10R/10RG

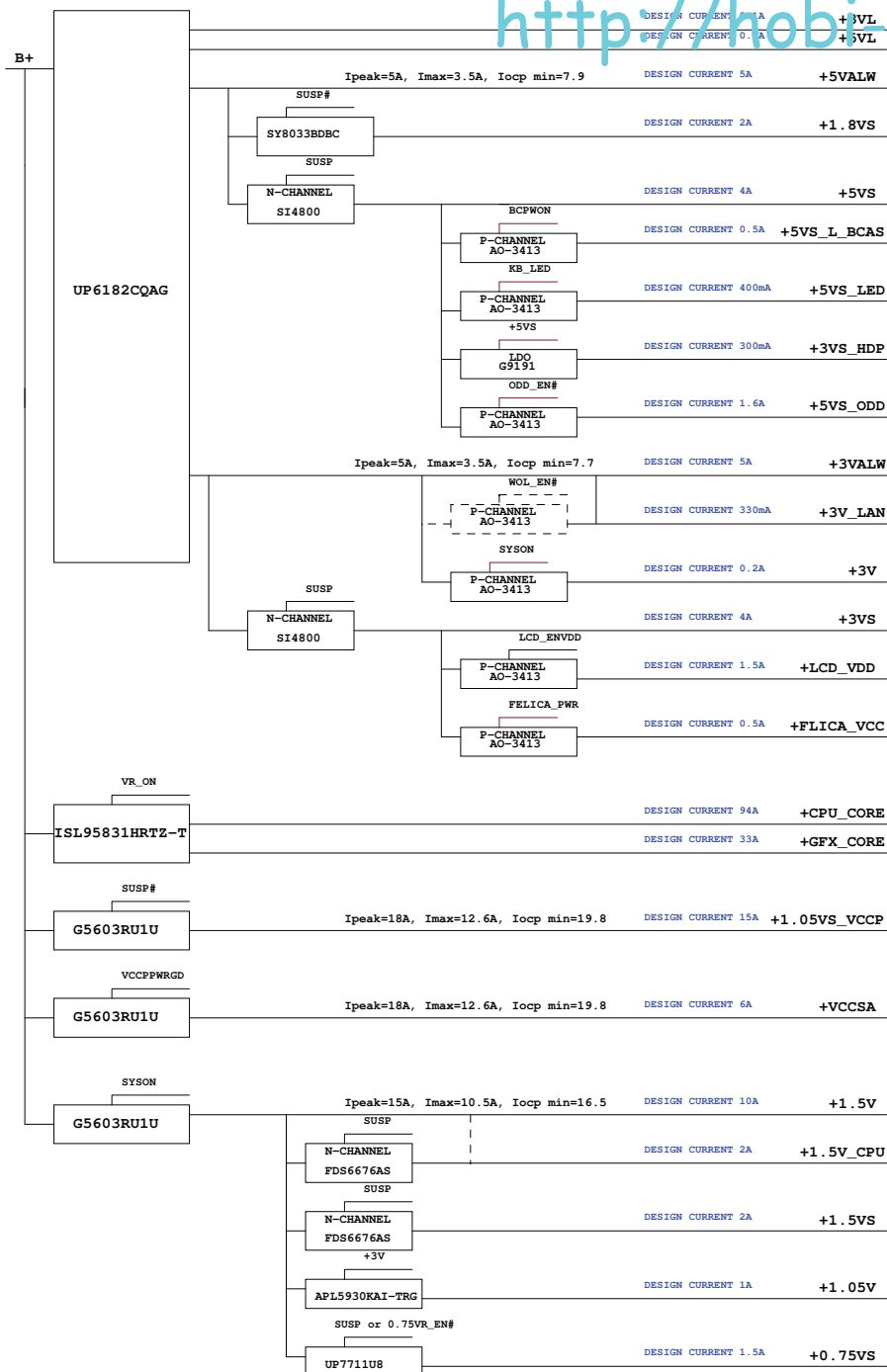
LA-6832P REV 0.2 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-09-03 Rev 0.1

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				Cover Page	
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				Block Diagram	
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

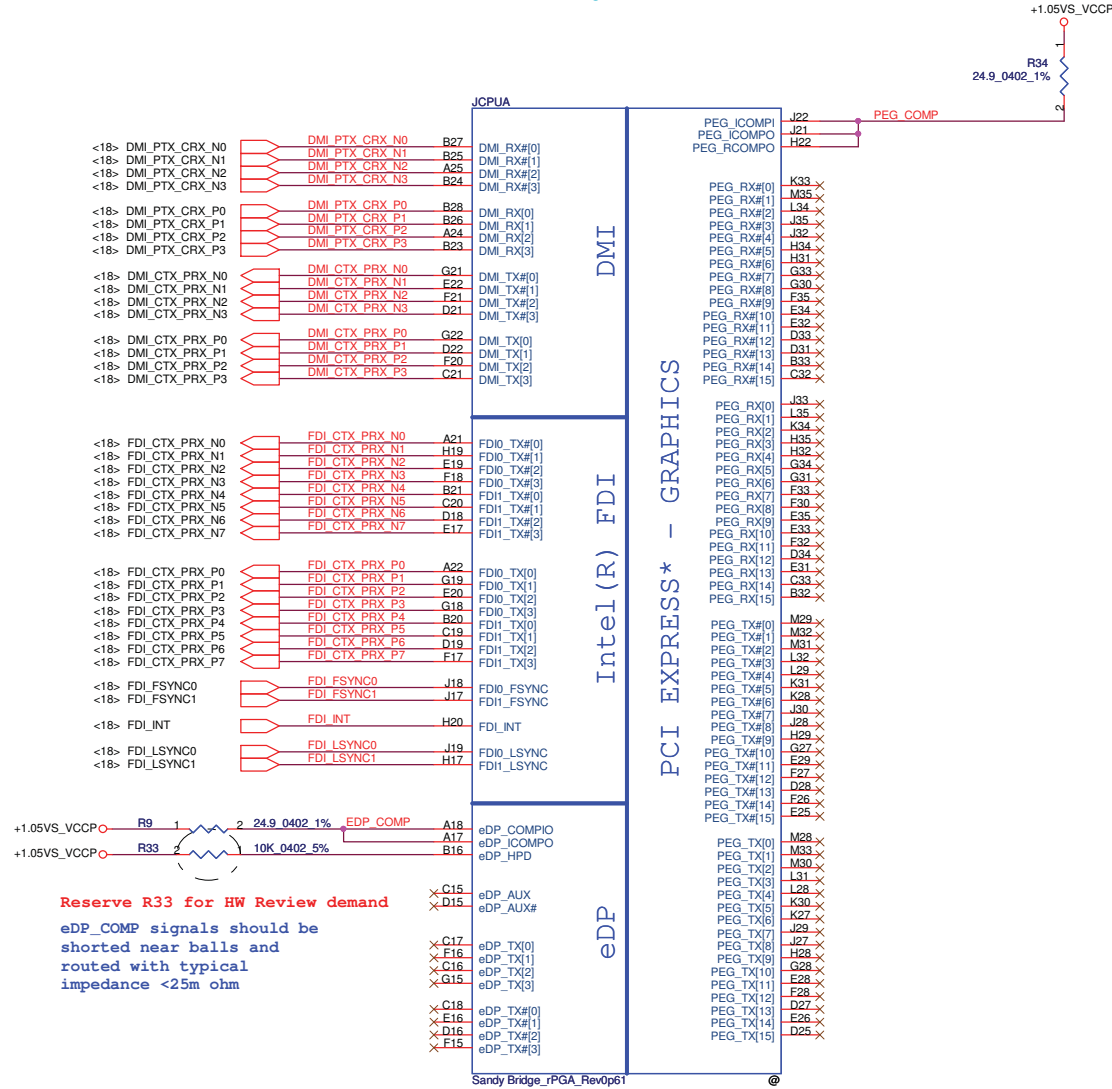
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving			GPU					
description	S3 Power Saving			N11P & N11E			N11M		
explain	No Power Saving	Power Saving		VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@		8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

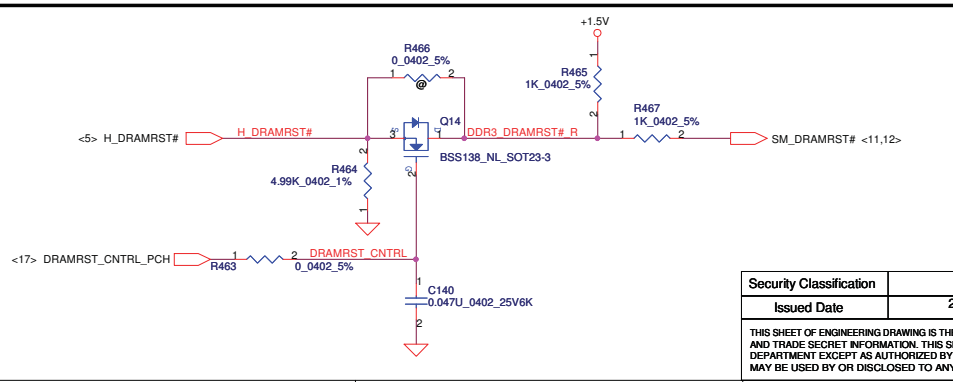
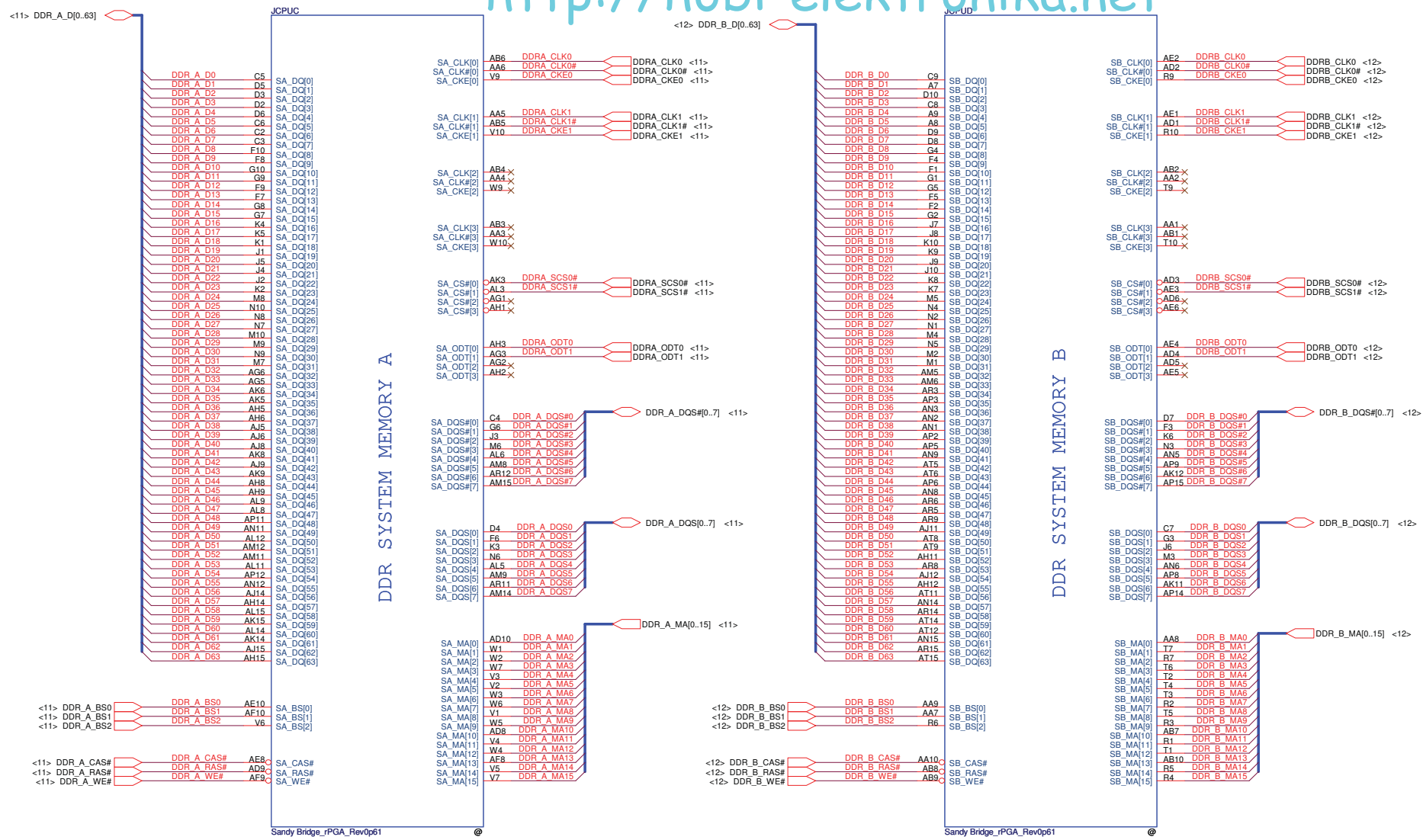
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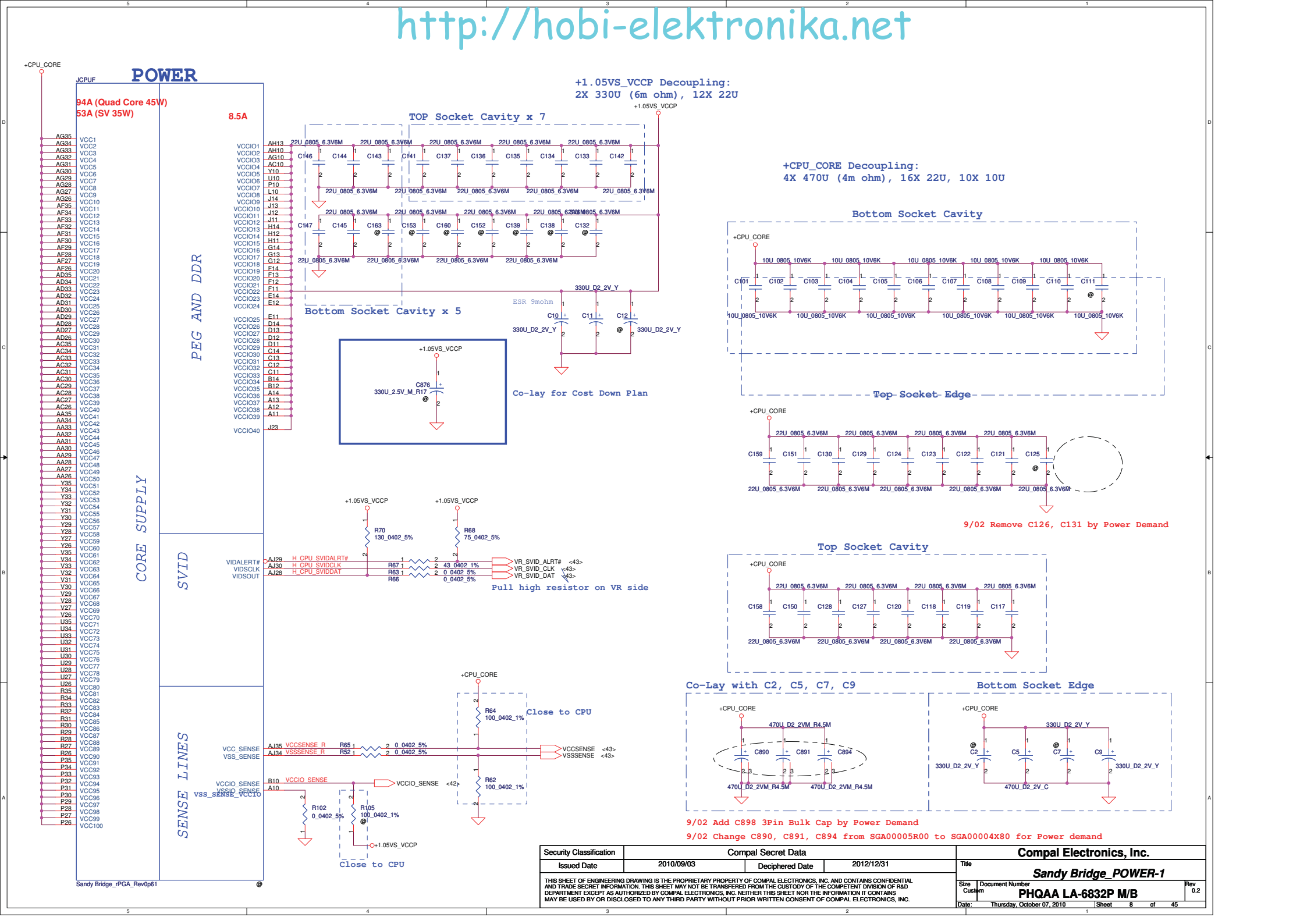
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)

PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

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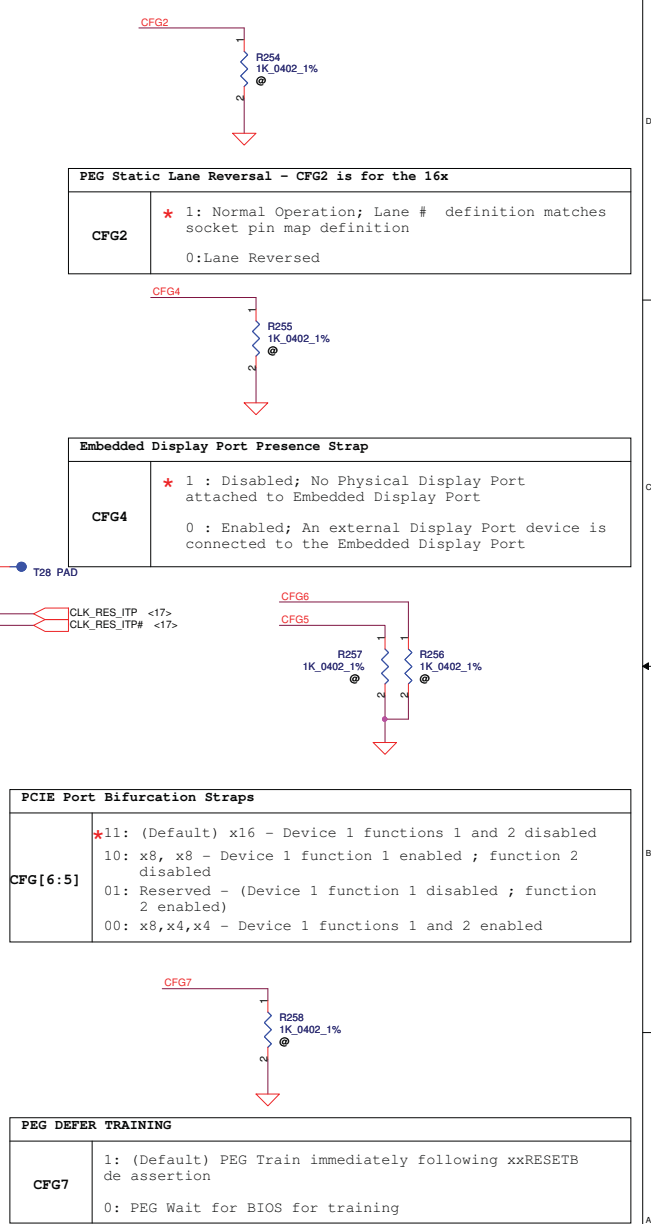
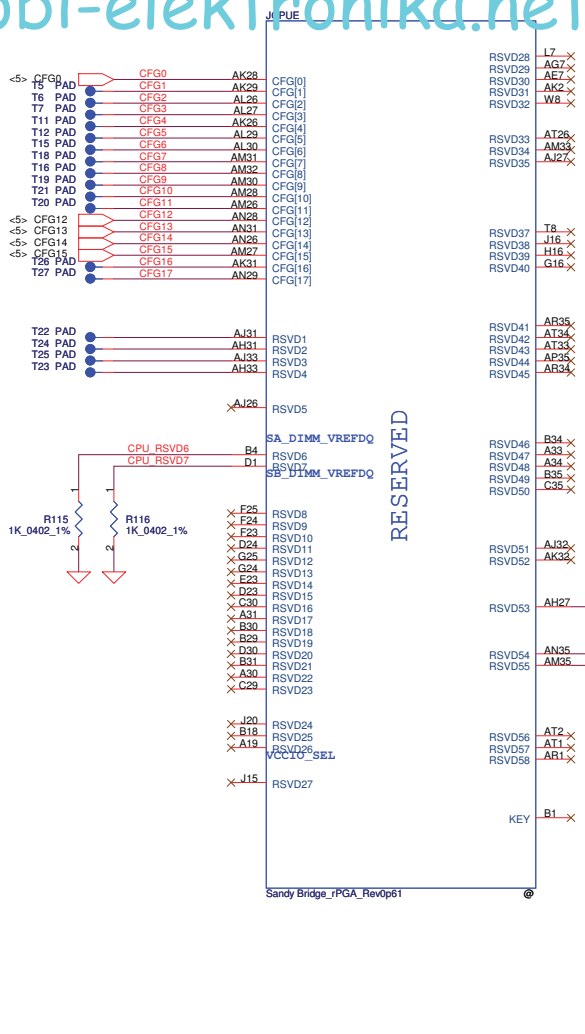
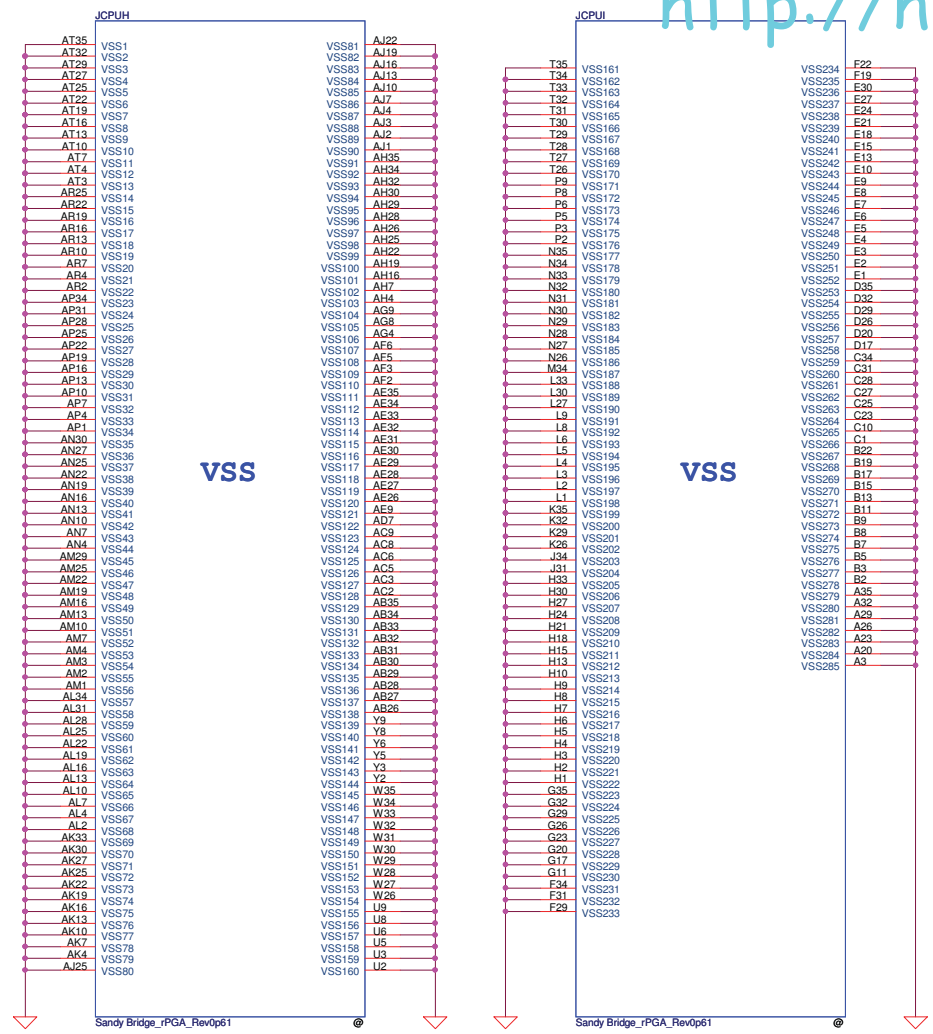


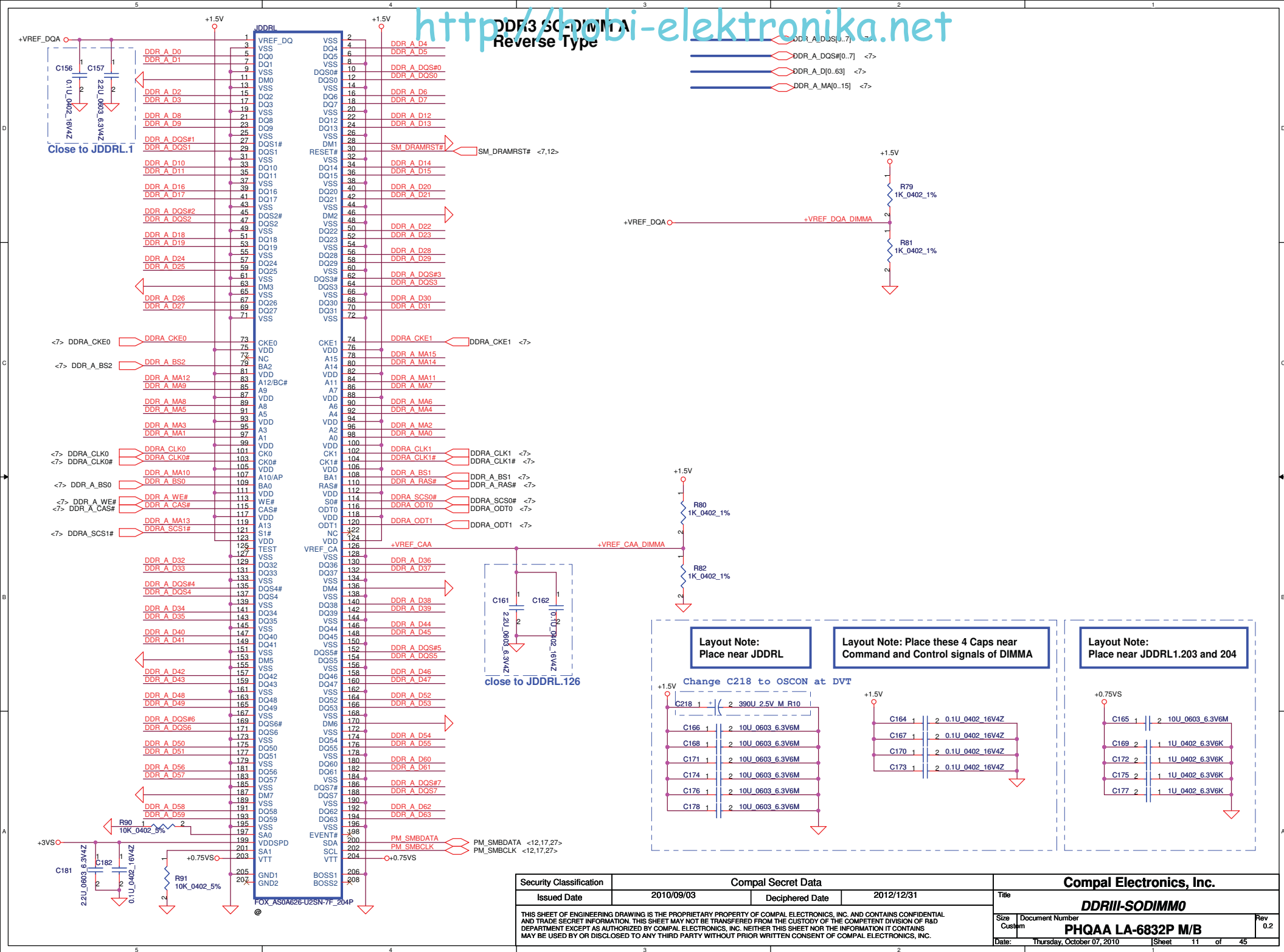
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[illegible]

CFG Straps for Processor

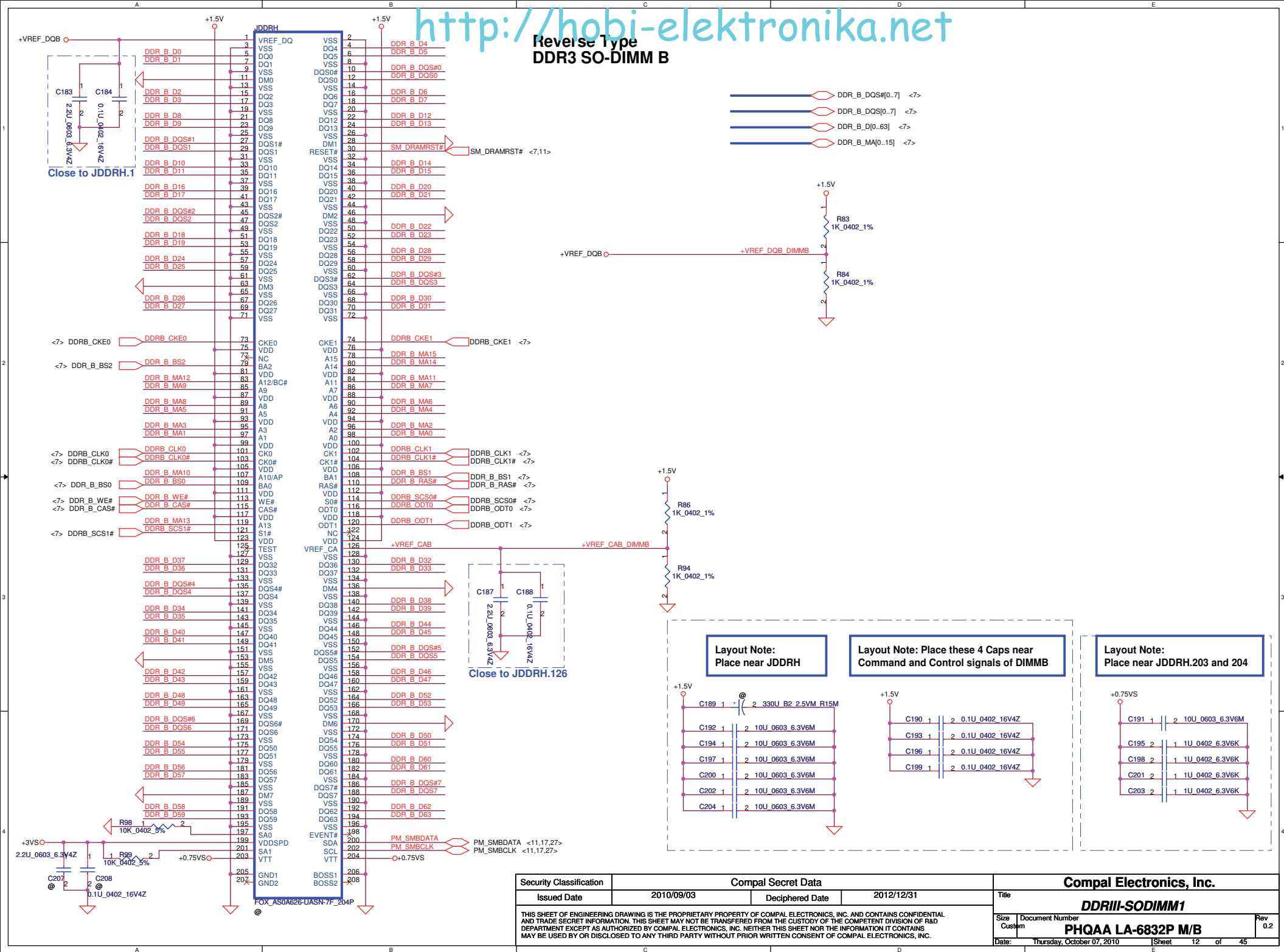
(CFG[17:0] internal pull high to VCCIO)

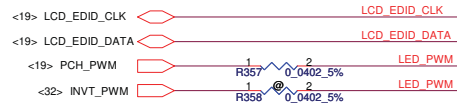




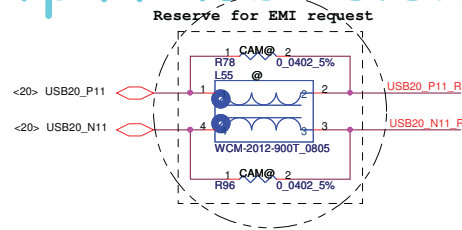
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				DDR/III-SODIMMO					
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Reverse Type
DDR3 SO-DIMM B

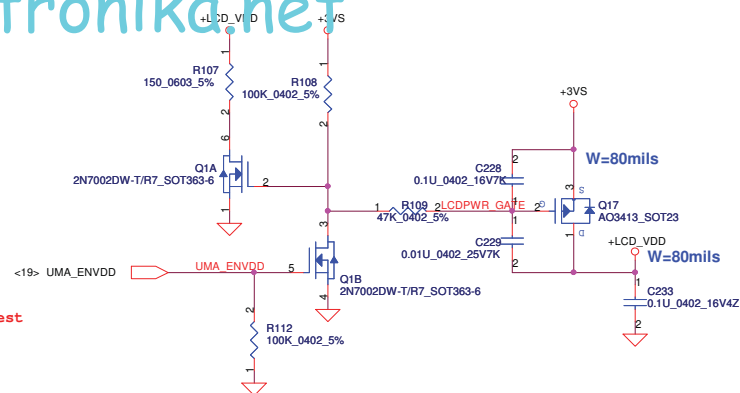




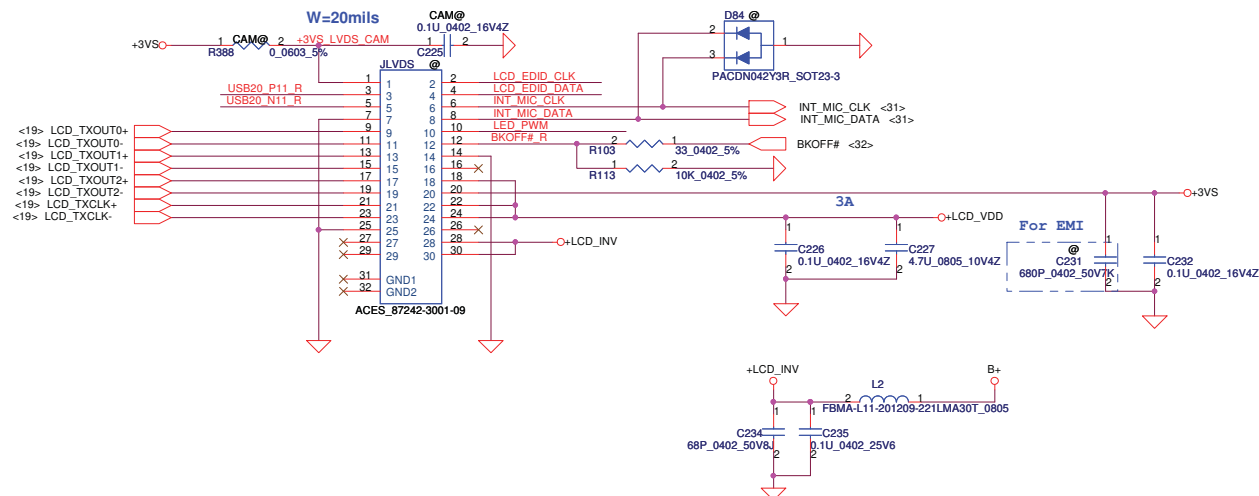
Close to LVDS Connector



8/20 Swap USB20_P11 and USB20_N11 for layout request

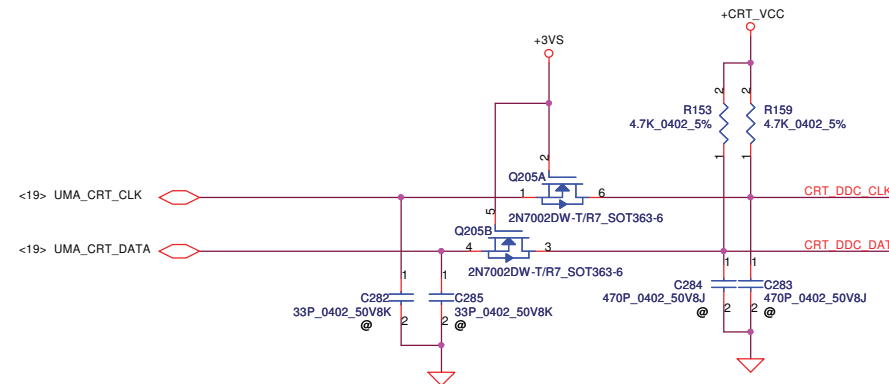
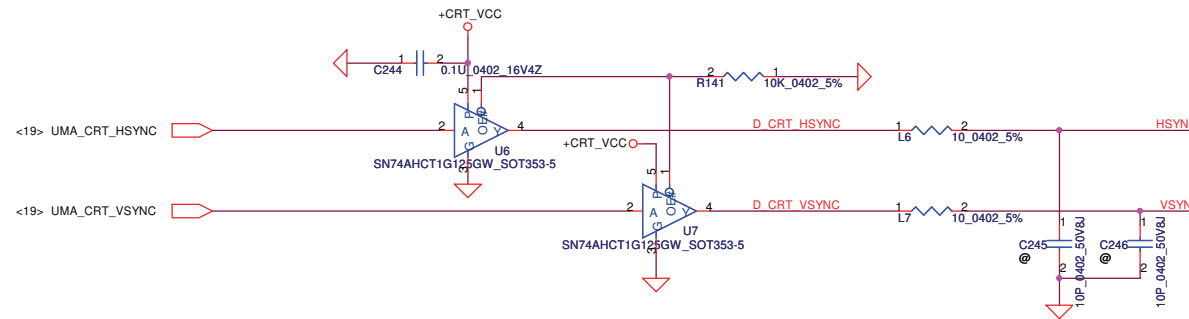
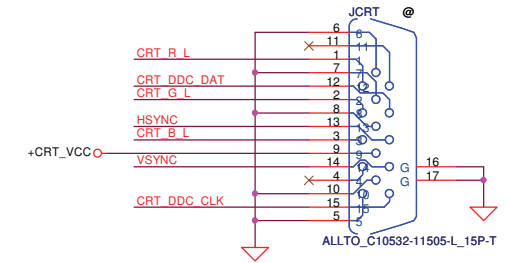
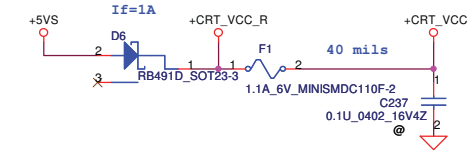
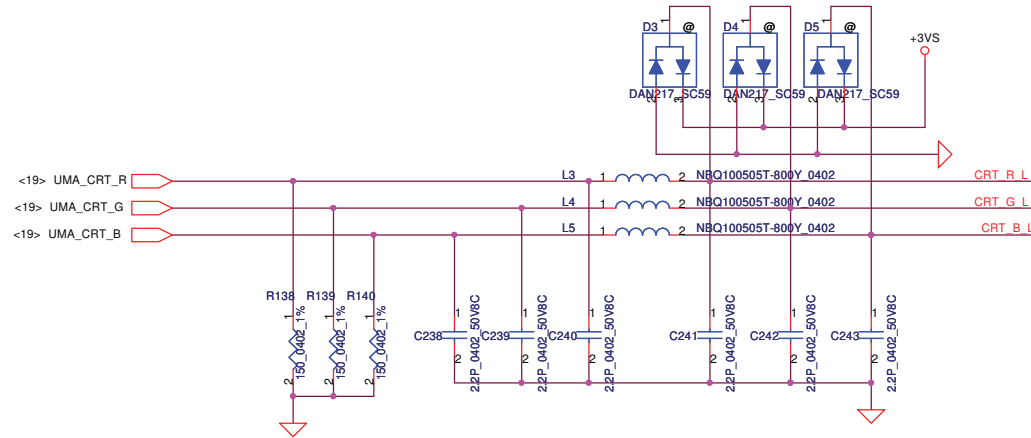


LCD/PANEL BD. Conn.

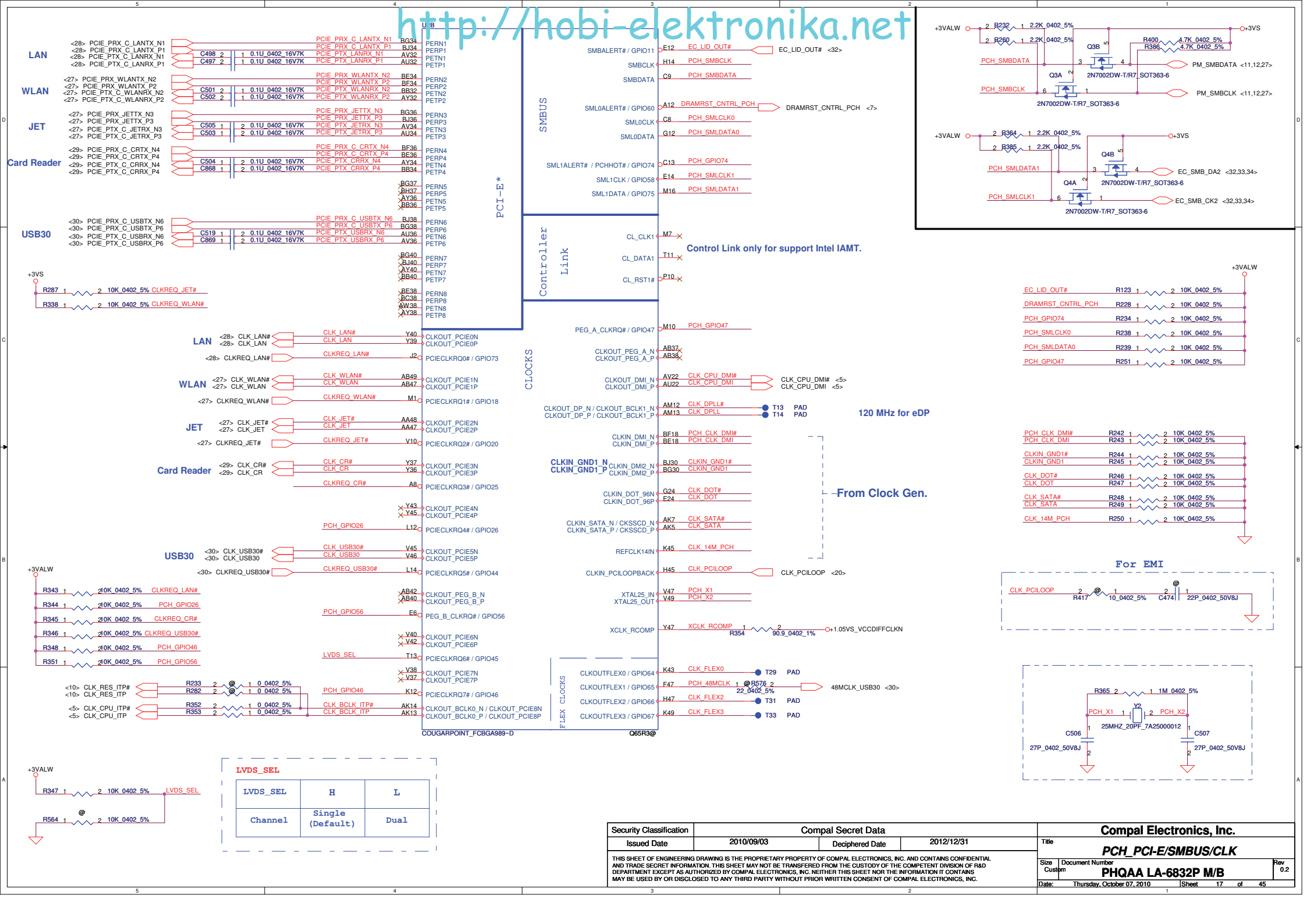
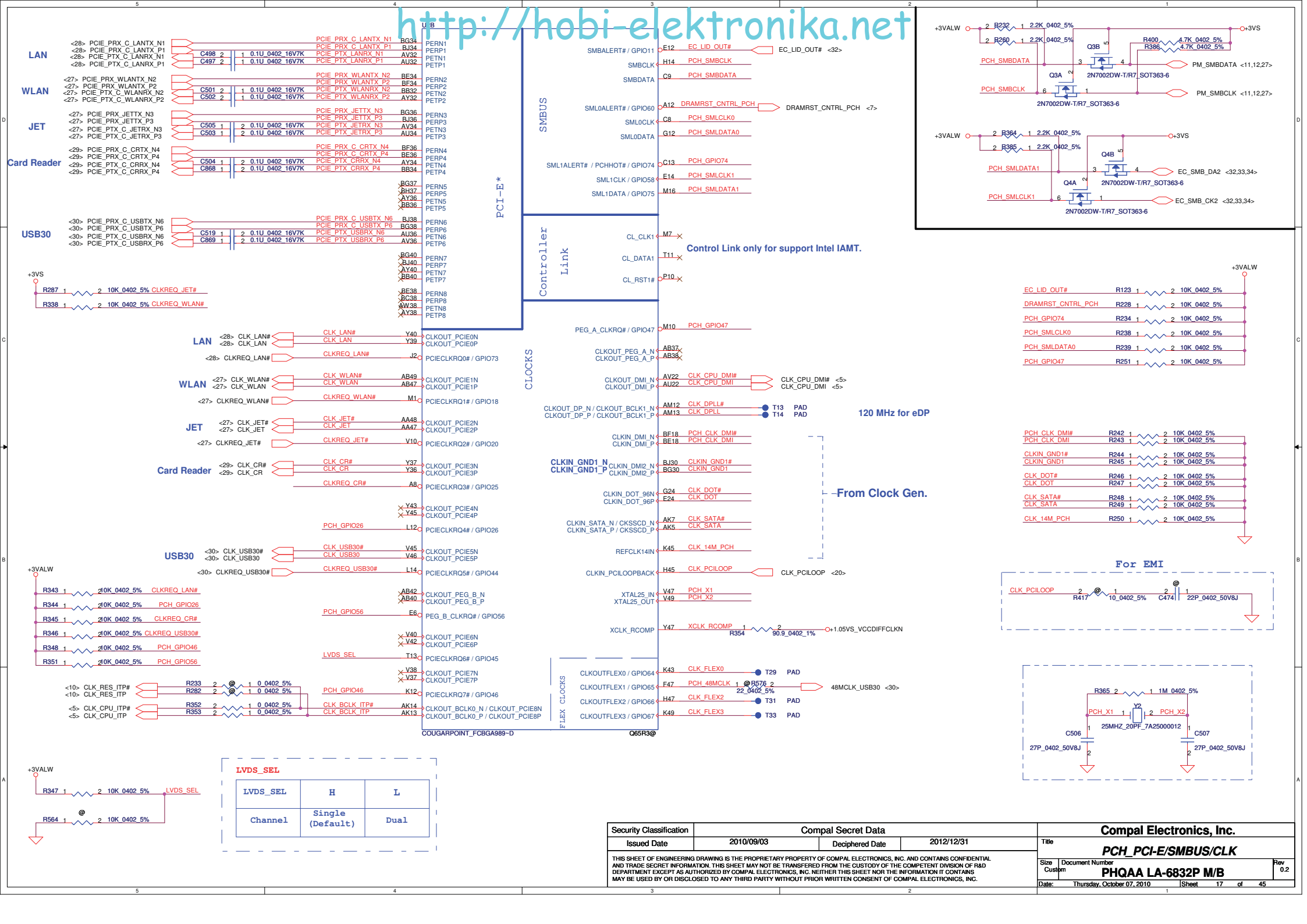
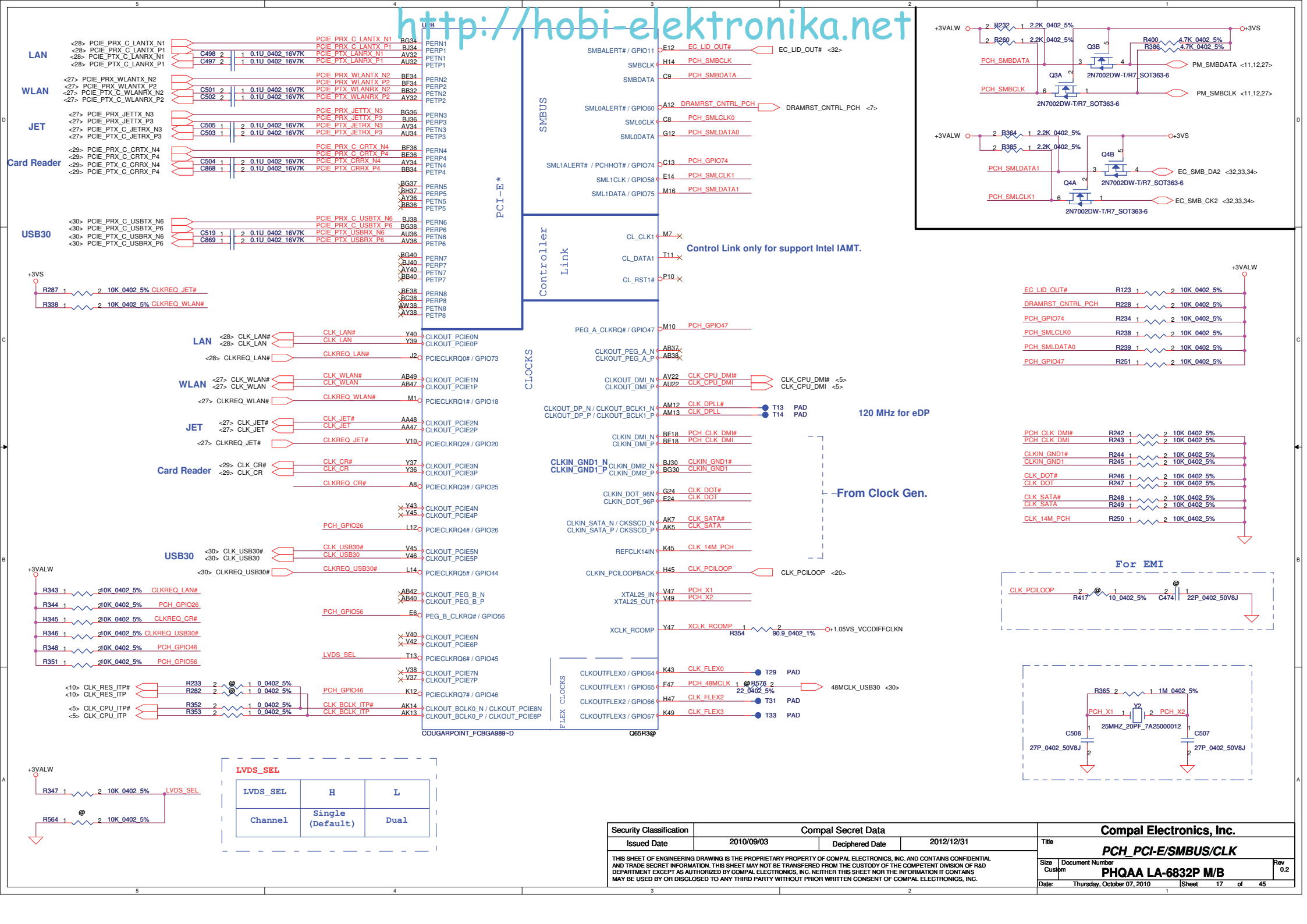


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CRT CONNECTOR



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LAN

- <28> PCIE_PRX_C_LANTX_N1
- <28> PCIE_PRX_C_LANTX_P1
- <28> PCIE_PTX_C_LANRX_N1
- <28> PCIE_PTX_C_LANRX_P1

WLAN

- <27> PCIE_PRX_WLANTX_N2
- <27> PCIE_PRX_WLANTX_P2
- <27> PCIE_PTX_C_WLANRX_N2
- <27> PCIE_PTX_C_WLANRX_P2

JET

- <27> PCIE_PRX_JETTX_N3
- <27> PCIE_PRX_JETTX_P3
- <27> PCIE_PTX_C_JETRX_N3
- <27> PCIE_PTX_C_JETRX_P3

Card Reader

- <29> PCIE_PRX_C_CRTX_N4
- <29> PCIE_PRX_C_CRTX_P4
- <29> PCIE_PTX_C_CRRX_N4
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USB30

- <30> PCIE_PRX_C_USBTX_N6
- <30> PCIE_PRX_C_USBTX_P6
- <30> PCIE_PTX_C_USBRX_N6
- <30> PCIE_PTX_C_USBRX_P6

SMBUS

- SMBALERT# / GPIO11
- SMBCLK
- SMBDATA
- SML0ALERT# / GPIO60
- SML0CLK
- SML0DATA
- SML1ALERT# / PCHHOT# / GPIO74
- SML1CLK / GPIO58
- SML1DATA / GPIO75

Controller Link

- CL_CLK1
- CL_DATA1
- CL_RST1#

CLOCKS

- CLKOUT_PCIE0N
- CLKOUT_PCIE0P
- CLKOUT_PCIE1N
- CLKOUT_PCIE1P
- CLKOUT_PCIE2N
- CLKOUT_PCIE2P
- CLKOUT_PCIE3N
- CLKOUT_PCIE3P
- CLKOUT_PCIE4N
- CLKOUT_PCIE4P
- CLKOUT_PCIE5N
- CLKOUT_PCIE5P
- CLKOUT_PCIE6N
- CLKOUT_PCIE6P
- CLKOUT_PCIE7N
- CLKOUT_PCIE7P
- CLKOUT_BCLK0_N
- CLKOUT_BCLK0_P
- CLKOUT_BCLK1_N
- CLKOUT_BCLK1_P
- CLKOUT_BCLK2_N
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- CLKOUT_BCLK77_N
- CLKOUT_BCLK77_P
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- CLKOUT_BCLK78_P
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- CLKOUT_BCLK79_P
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- CLKOUT_BCLK82_P
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- CLKOUT_BCLK84_P
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- CLKOUT_BCLK97_N
- CLKOUT_BCLK97_P
- CLKOUT_BCLK98_N
- CLKOUT_BCLK98_P
- CLKOUT_BCLK99_N
- CLKOUT_BCLK99_P

FLEX CLOCKS

- CLK_FLEX0
- CLK_FLEX1
- CLK_FLEX2
- CLK_FLEX3

LVDS_SEL

LVDS_SEL	H	L
Channel	Single (Default)	Dual

Security Classification

Security Classification	Compal Secret Data
Issued Date	2010/09/03
Deciphered Date	2012/12/31

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Compal Electronics, Inc.

PCH_PCI-E/SMBUS/CLK

PHQAA LA-6832P M/B

Date: Thursday, October 07, 2010 **Sheet:** 17 of 45

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LAN

- <28> PCIE_PRX_C_LANTX_N1
- <28> PCIE_PRX_C_LANTX_P1
- <28> PCIE_PTX_C_LANRX_N1
- <28> PCIE_PTX_C_LANRX_P1

WLAN

- <27> PCIE_PRX_WLANTX_N2
- <27> PCIE_PRX_WLANTX_P2
- <27> PCIE_PTX_C_WLANRX_N2
- <27> PCIE_PTX_C_WLANRX_P2

JET

- <27> PCIE_PRX_JETTX_N3
- <27> PCIE_PRX_JETTX_P3
- <27> PCIE_PTX_C_JETRX_N3
- <27> PCIE_PTX_C_JETRX_P3

Card Reader

- <29> PCIE_PRX_C_CRTX_N4
- <29> PCIE_PRX_C_CRTX_P4
- <29> PCIE_PTX_C_CRRX_N4
- <29> PCIE_PTX_C_CRRX_P4

USB30

- <30> PCIE_PRX_C_USBTX_N6
- <30> PCIE_PRX_C_USBTX_P6
- <30> PCIE_PTX_C_USBRX_N6
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SMBUS

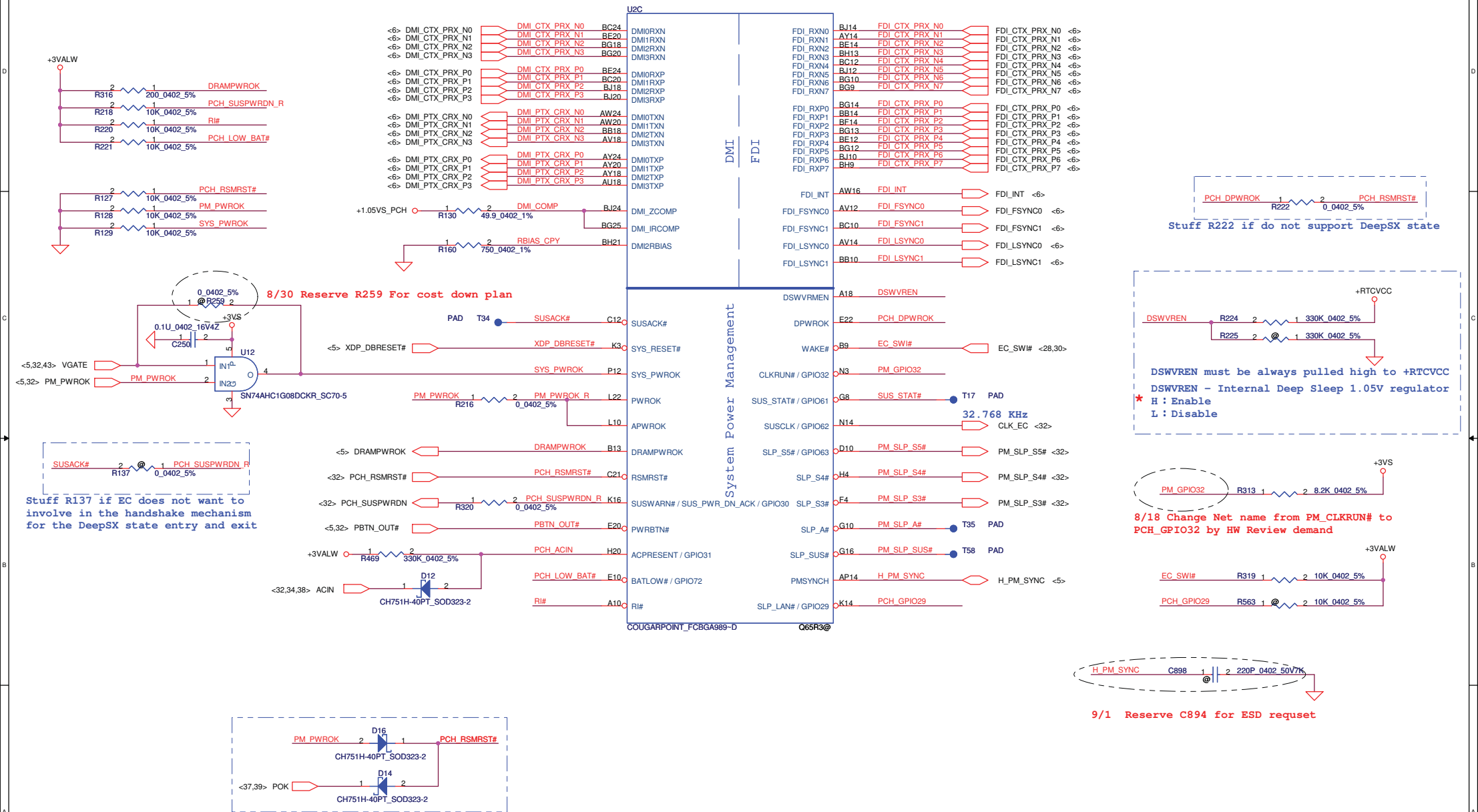
- SMBALERT# / GPIO11
- SMBCLK
- SMBDATA
- SML0ALERT# / GPIO60
- SML0CLK
- SML0DATA
- SML1ALERT# / PCHHOT# / GPIO74
- SML1CLK / GPIO58
- SML1DATA / GPIO75

Controller Link

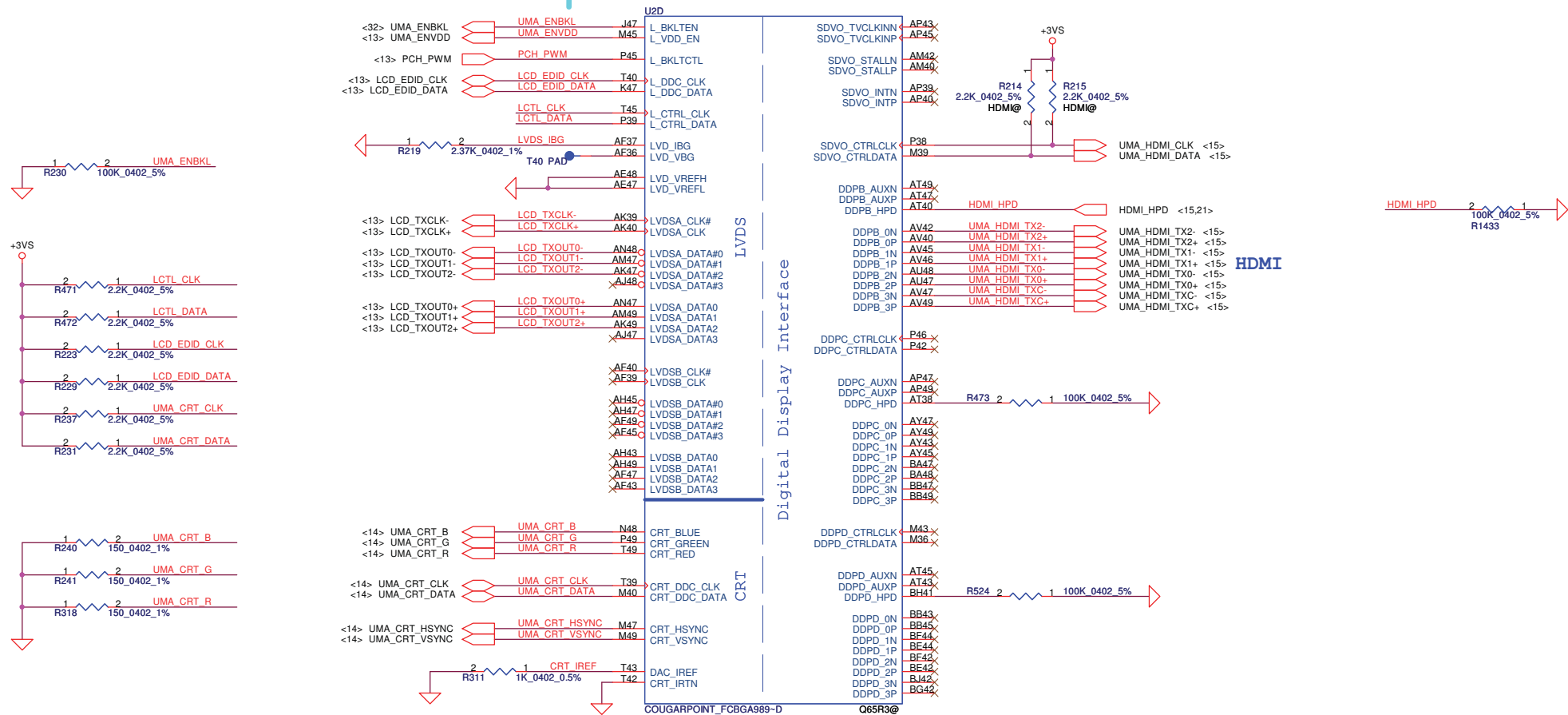
- CL_CLK1
- CL_DATA1
- CL_RST1#

CLOCKS

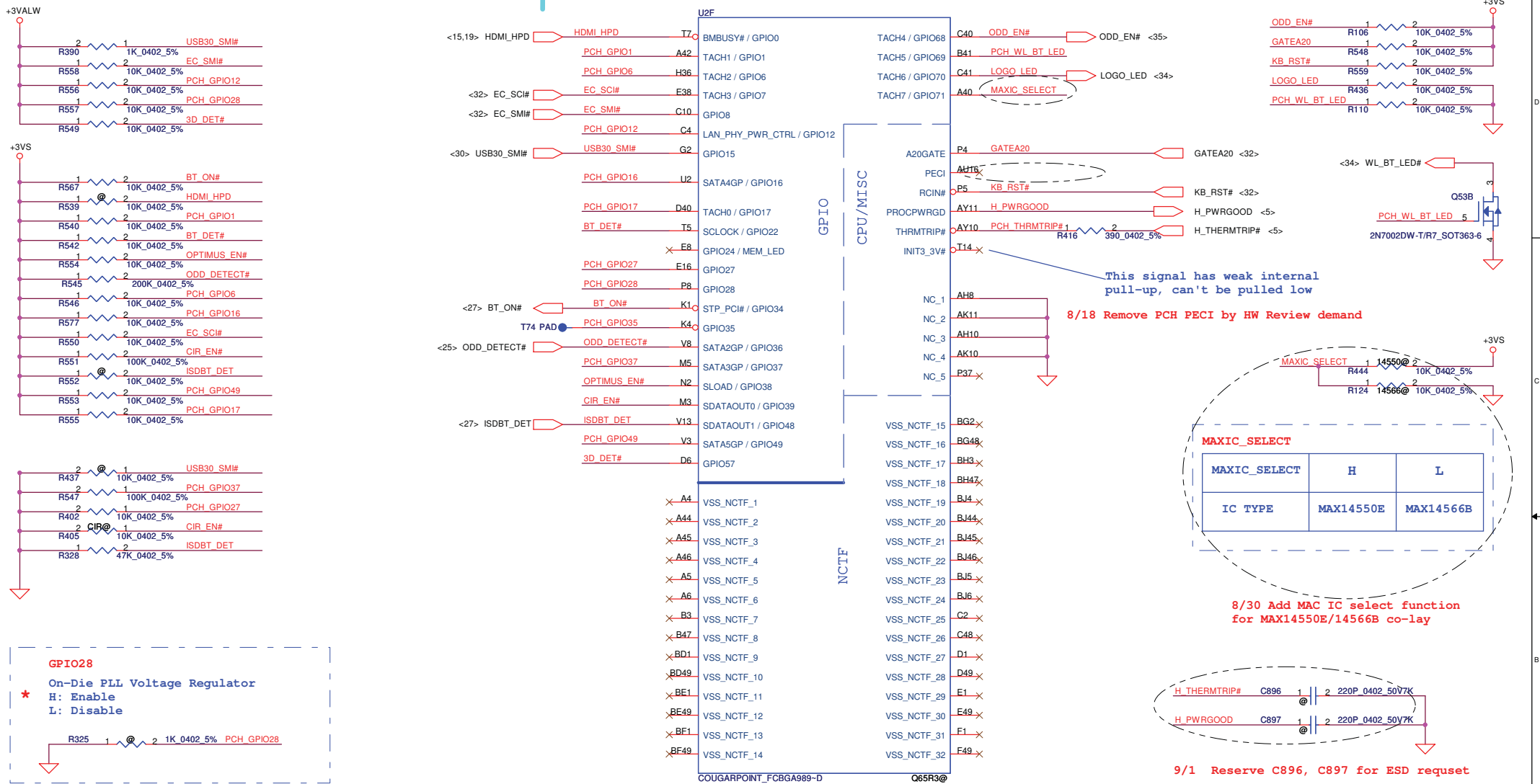
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- CLKOUT_PCIE0P
- CLKOUT_PCIE1N
- CLKOUT_PCIE1P
- CLKOUT_PCIE2N
- CLKOUT_PCIE2P
- CLKOUT_PCIE3N
- CLKOUT_PCIE3P
- CLKOUT_PCIE4N
- CLKOUT_PCIE4P
- CLKOUT_PCIE5N
- CLKOUT_PCIE5P
- CLKOUT_PCIE6N
- CLKOUT_PCIE6P
- CLKOUT_PCIE7N
- CLKOUT_PCIE7P
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- CLKOUT_BCLK120_N
- CLKOUT_BCLK120_P



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Size	Document Number	Rev		Date	
Custom	PHQAA LA-6832P M/B	0.2		Thursday, October 07, 2010	
Sheet		18		of 45	

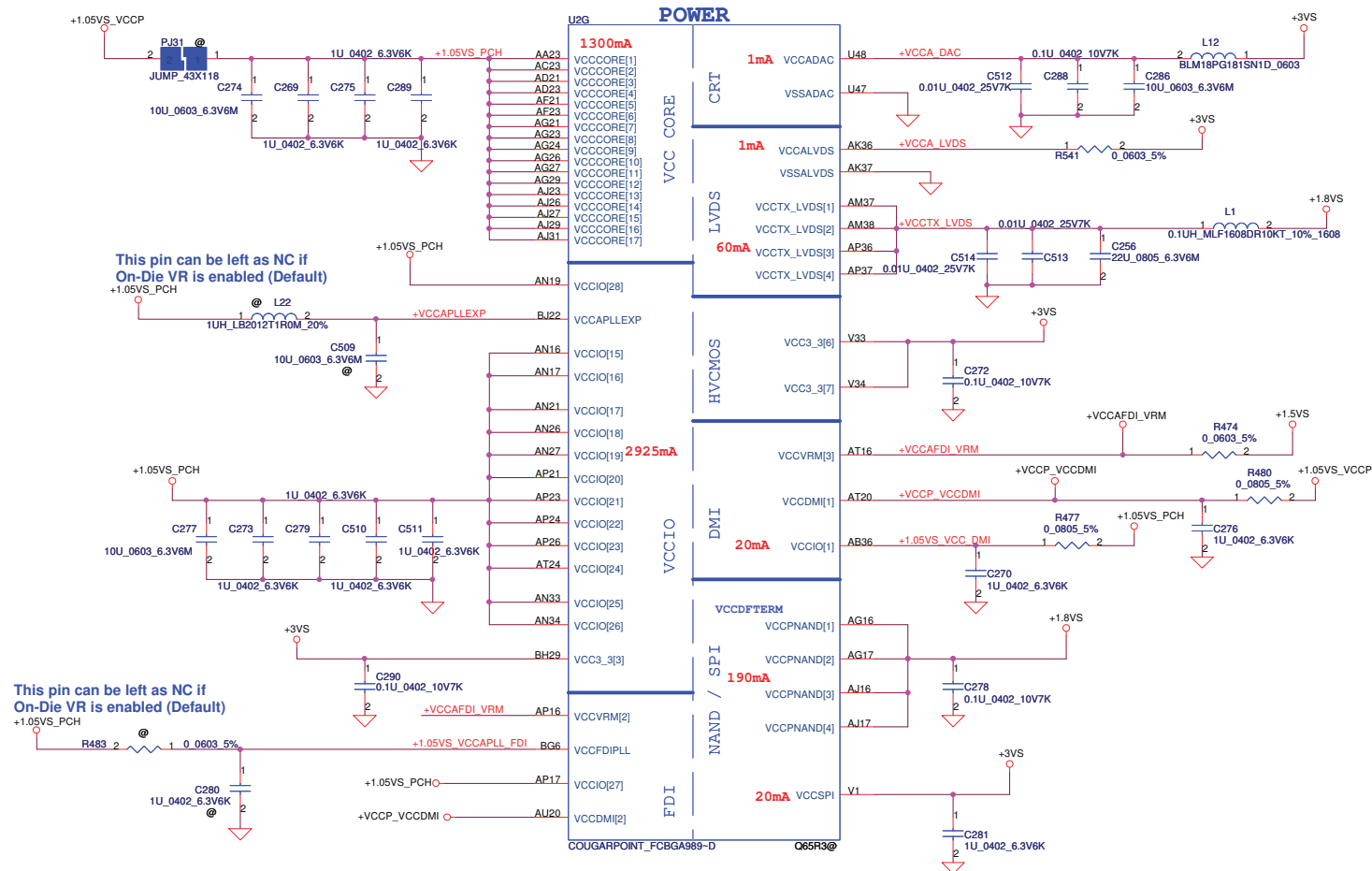


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Size	Custom	Document Number	PHQAA LA-6832P M/B	Rev	0.2
Date:	Thursday, October 07, 2010	Sheet	19	of	45

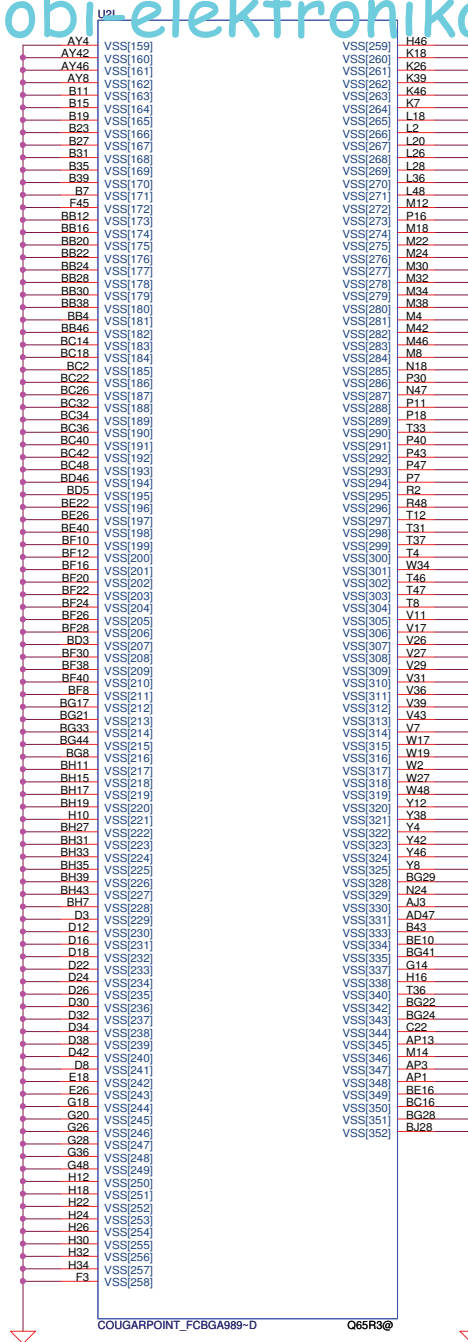
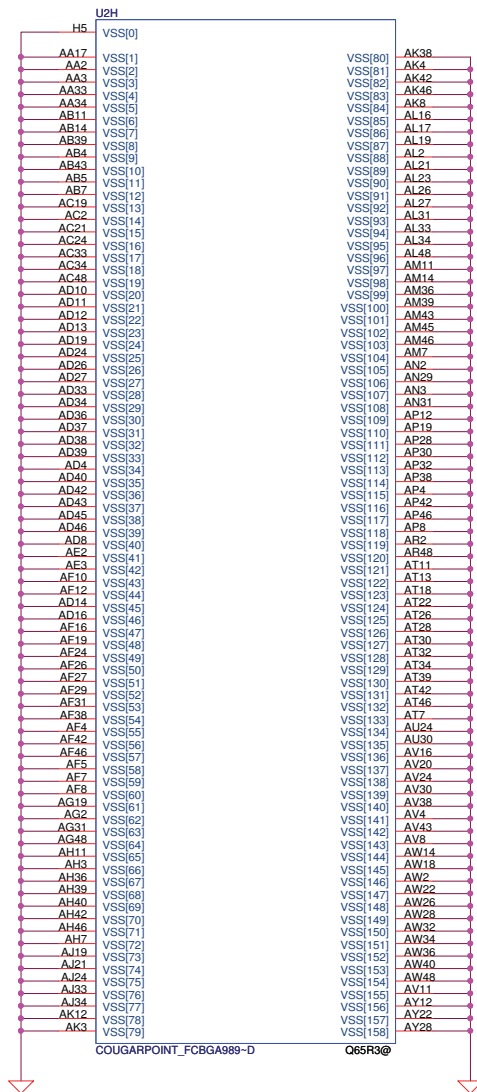


OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title PCH_CPU/GPIO		
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				Date: Thursday, October 07, 2010		Sheet 21 of 45

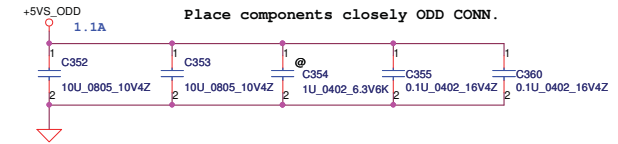
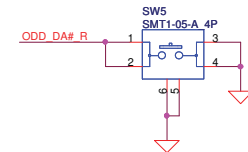


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



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Size	Custom	Document Number	PHQAA LA-6832P M/B	Rev	0.2
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WCM-2012-900T_0805

10/04 Swap USB20_P0, USB20_N0, USB20_P1, USB20_N1 for layout request

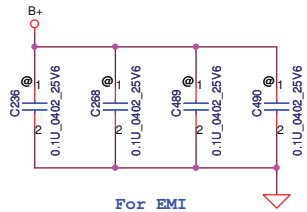
Signal	Pin
USB_VCCA	22
USB20_N1_R	21
USB20_P1_R	20
USB20_N0_R	19
USB20_P0_R	18
HP_R	17
HP_L	16
MIC1_L	15
MIC1_R	14
BACK_SENSE	13
NBA_PLUG	12
	11
	10
	9
	8
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	4
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	1

ACES_85201-2005N

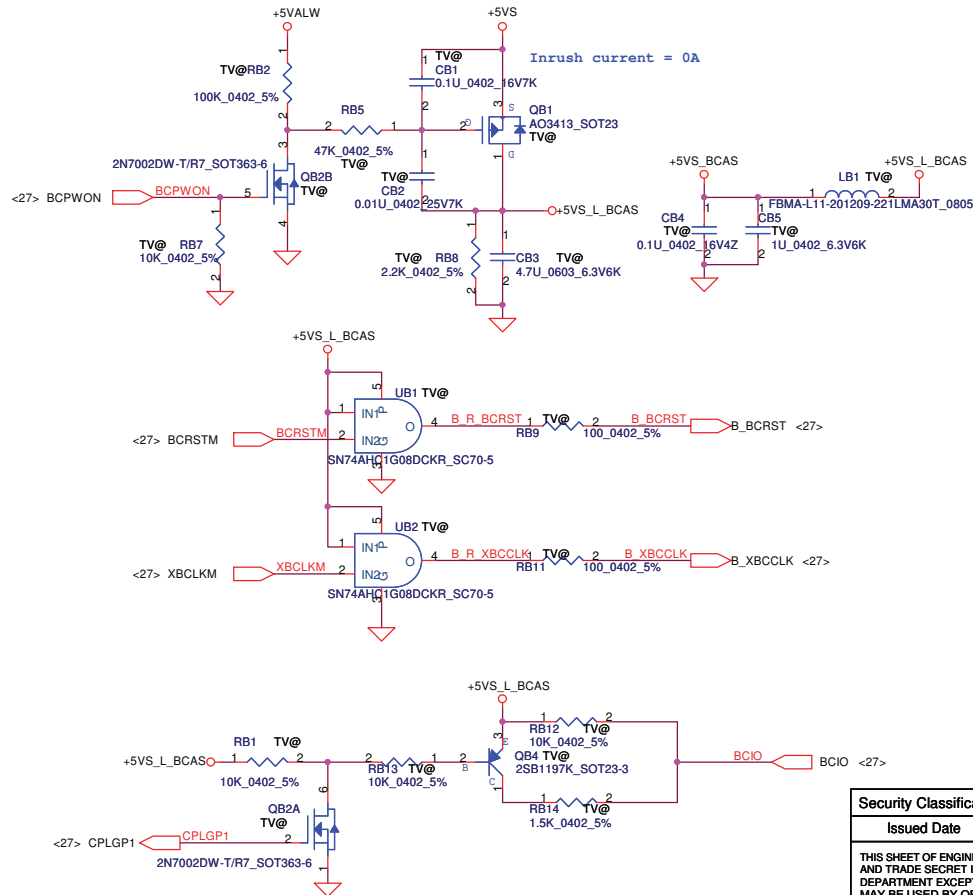
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Security Classification		Compal Secret Data		Compal Electronics, Inc. SATA-HDD/ODD/USB	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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Screw cap for ESD request

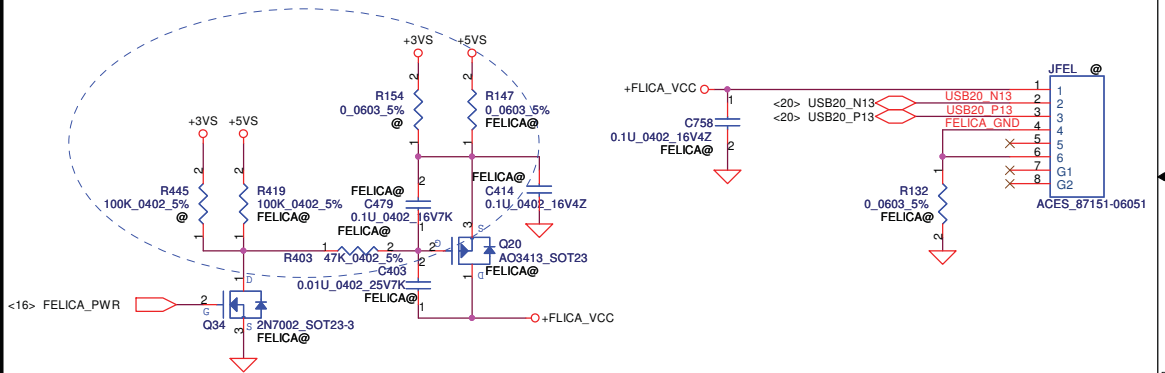


B-CAS Circuit

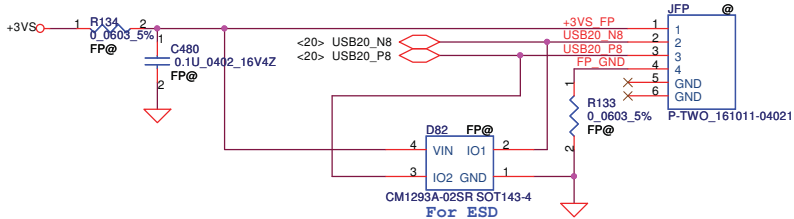


Felica

Reserve +3VS Felica by Customer demand.
2010/09/27

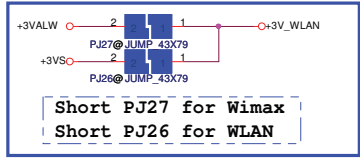


Finger printer



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		Size		Document Number					Rev
				PHQAA LA-6832P M/B					0.2
		Date:		Thursday, October 07, 2010			Sheet		26 of 45

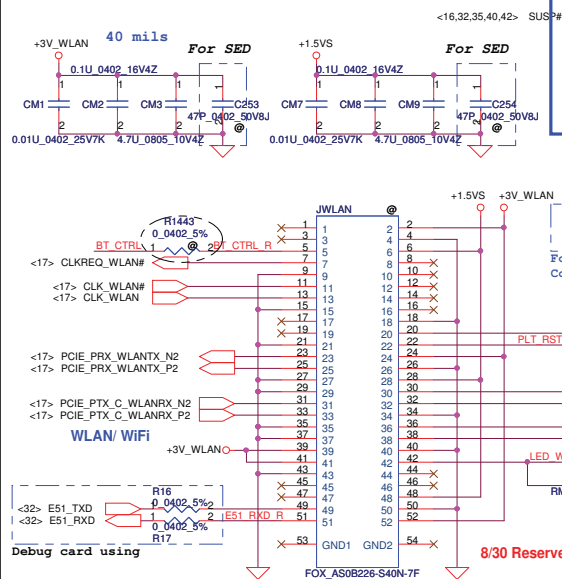
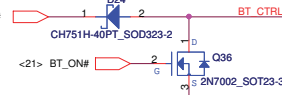
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



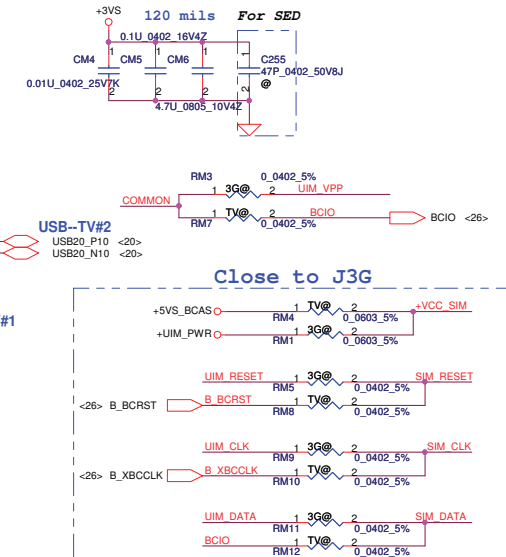
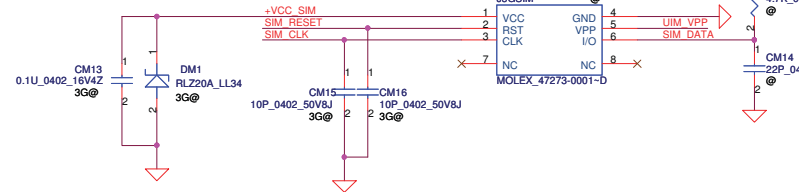
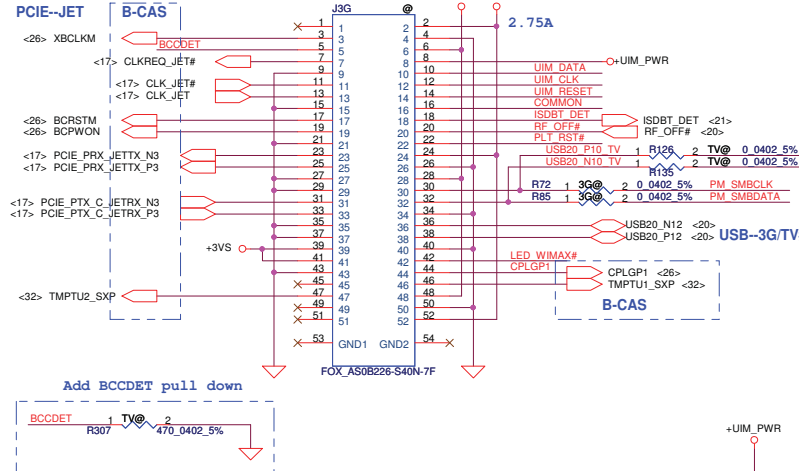
WLAN&BT Combo Circuits

	BT on module	BT on module
	Enable	Disable
BT_CTRL	H	L
BT_ON#	L	H

**If +3V_WLAN is +3VS, please remove D24



Slot 2 Full PCIe Mini Card-3G/TV Tuner



USB Sleep & Charge Auto-Mode Mode3/Mode4

MAX14566B

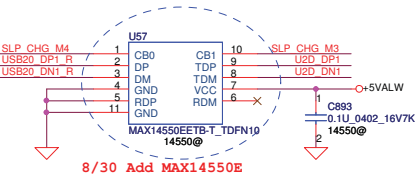
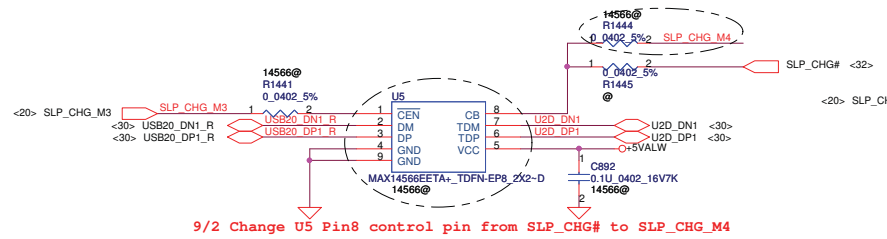
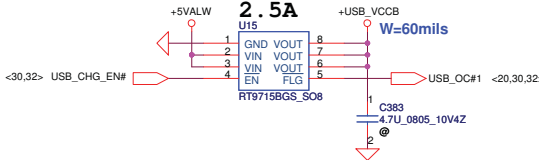
CB0 SLP_CHG#	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E

CB: SLP_CHG#	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14550E

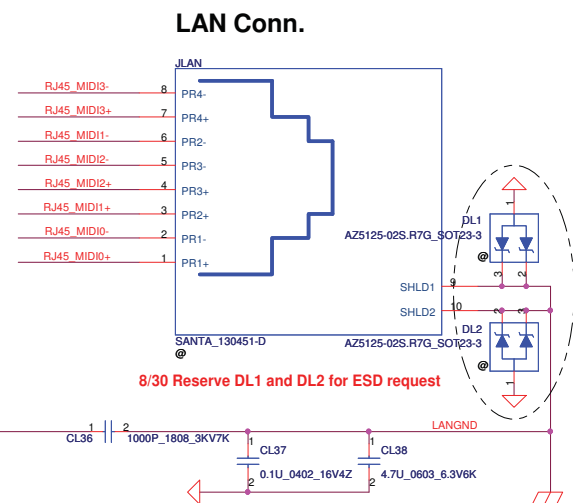
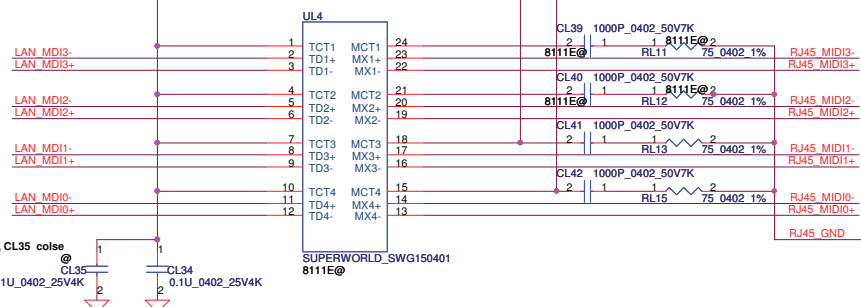
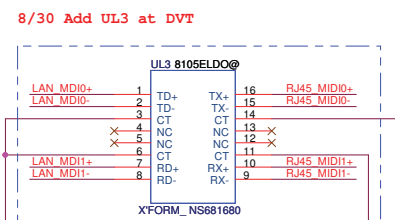
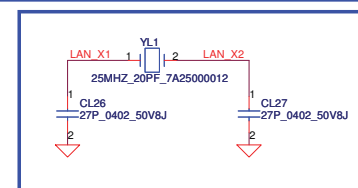
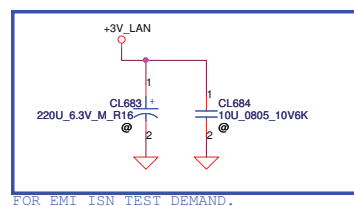
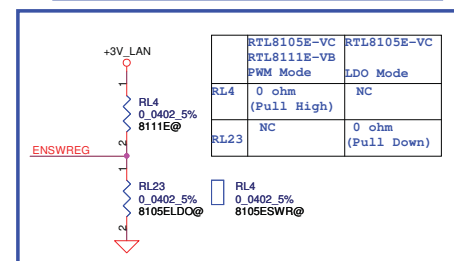
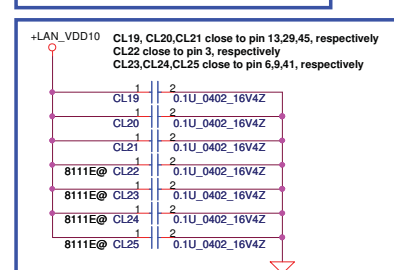
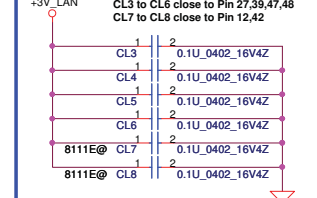
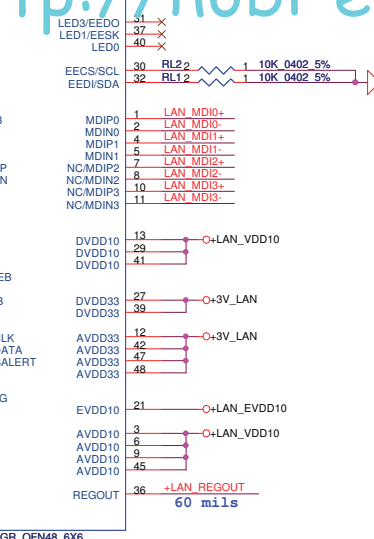
CB0 SLP_CHG_M4	CB1 SLP_CHG_M4	STATUS
0	0	AUTO MODE
0	1	MODE3
1	0	MODE4
1	1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM



9/2 Change U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4
9/2 Add 14566 & 14550

8/30 Add MAX14550E

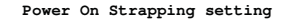
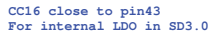
Security Classification	Compal Secret Data		Title	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Compal Electronics, Inc.
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Size	Document Number	Rev	PHQAA LA-6832P M/B	
Date	Thursday, October 07, 2010	Sheet	27	of 45



For P/N and footprint
Please place them to ISPD page

UL1	UL1
	
8105E-VC 10/100M 8105ELDO@	8105E-VC 10/100M 8105ESWR@
UL3	
	
10/100M transformer 8105ESWR@	

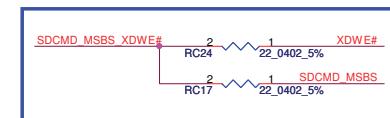
Security Classification		Compal Secret Data		Compal Electronics, Inc. PCle-LAN-RTL8105E/8111E	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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				Date: Thursday, October 07, 2010	Sheet 28 of 45



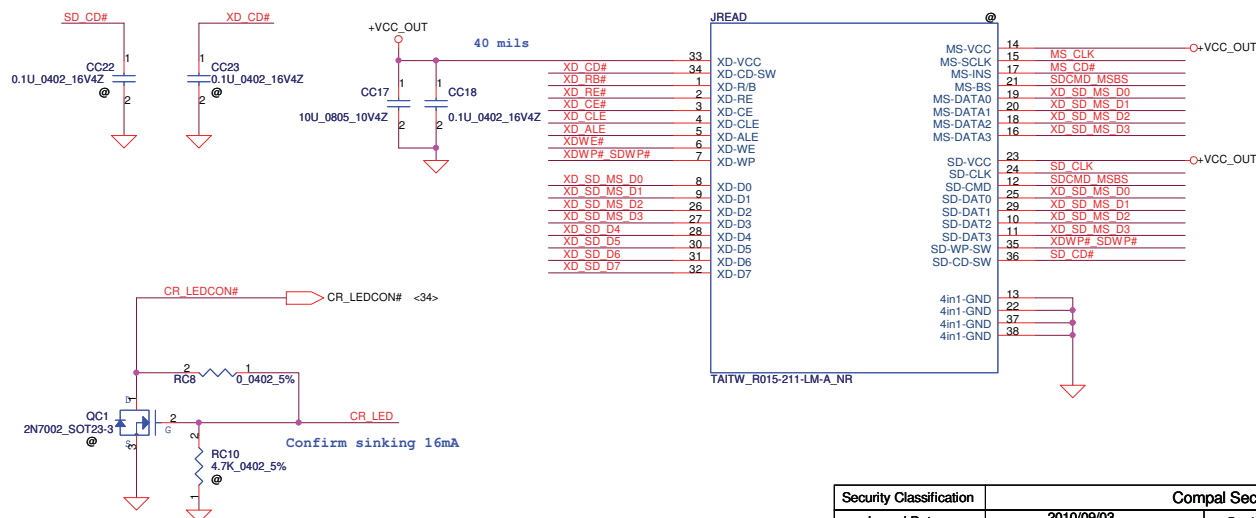
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★



Add RC24 and RC17 close to UC1 for xD issue

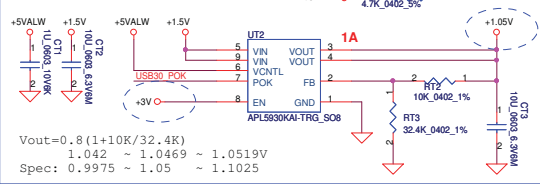


5 in 1 Card Reader

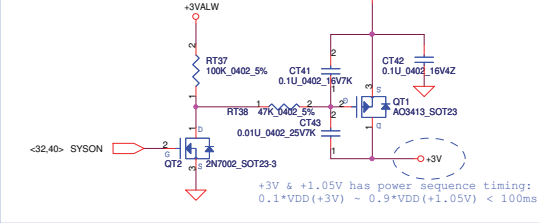


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/09/03	Deciphered Date	2012/12/31	PCle-CardReader JMB389		
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				Size	Document Number	Rev
				Custom	PHQA LA-6832P M/B	0.2
Date:				Thursday, October 07, 2010	Sheet	29 of 45

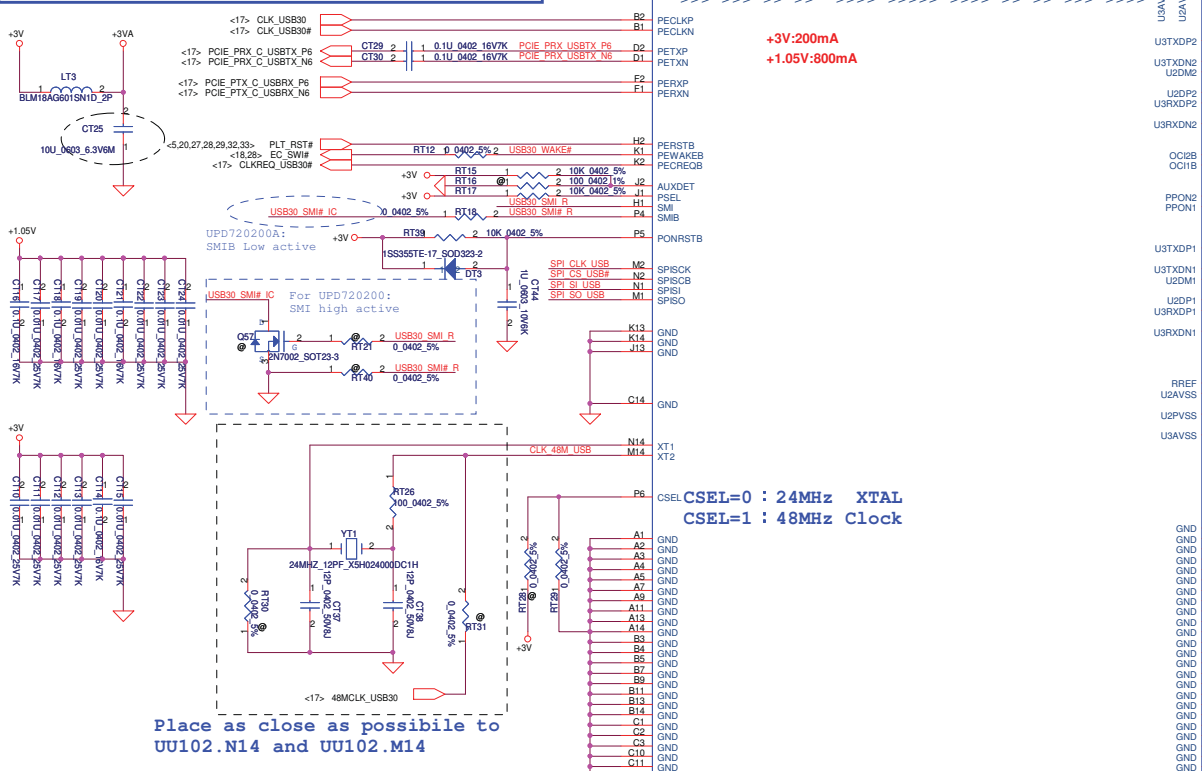
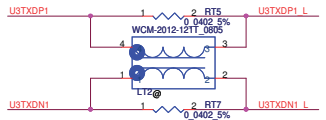
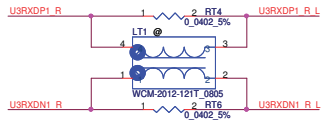
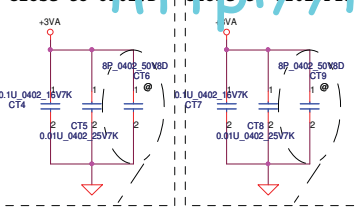
+1.5V to +1.05V Transfer



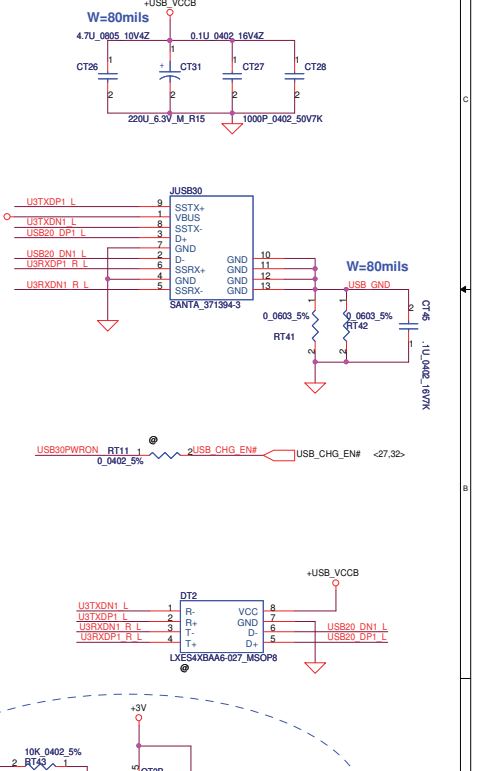
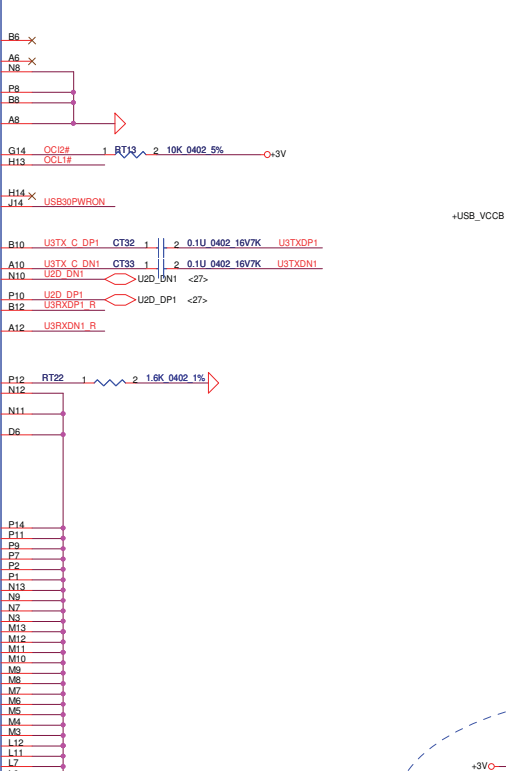
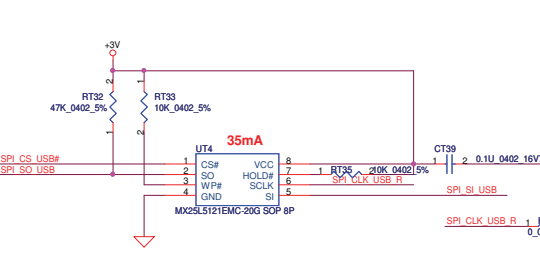
+3VALW to +3V Transfer



Close to U102.D Close to U102.P1

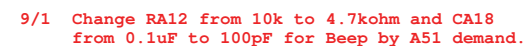
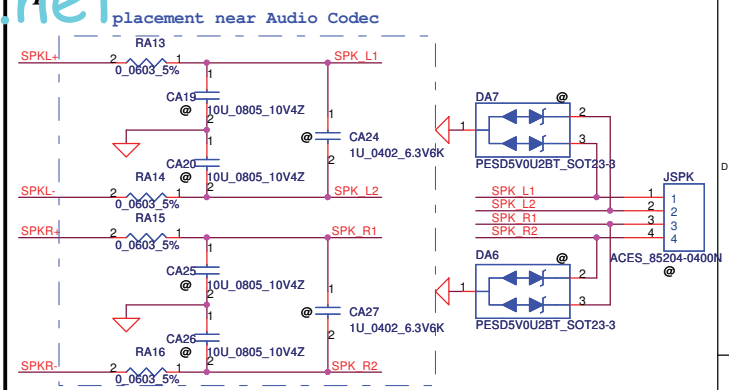


9/2 Change CT25 from SE093106K80 (10uF_0805) to SE000005T80 (10uF_0603) by sourcer demand



2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

Security Classification		Compal Secret Data		Title	
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2009/10/9		2010/01/23		PHQAA LA-6832P M/B	
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Sheet		30		of	
Rev		0.2			



The schematic diagram illustrates the MIC1_VREF0_L and MIC1_VREF0_R circuit. It features two operational amplifiers, OA1A and OA1B, both 2N7002DW-T/R_7_SOT363-6. OA1A is configured as a voltage follower with its non-inverting input connected to MIC1_VREF0_L and its output connected to MIC1_VREF0_R. OA1B is configured as a voltage follower with its non-inverting input connected to MIC1_VREF0_R and its output connected to MIC1_VREF0_L. The circuit also includes resistors RA33 (1K_0402_5%), RA32 (1K_0402_5%), RA29 (2.2K_0402_5%), RA28 (100K_0402_5%), RA43 (100K_0402_5%), and RA34 (100K_0402_5%). The input signals are MIC1_LINE1_R_R, MIC1_LINE1_R_L, and SM_SENSE#. The output signals are MIC1_VREF0_R, MIC1_VREF0_L, and BACK_SENSE.

place close to chip

MIC_SENSE

20K_0402_1%

RA10

1

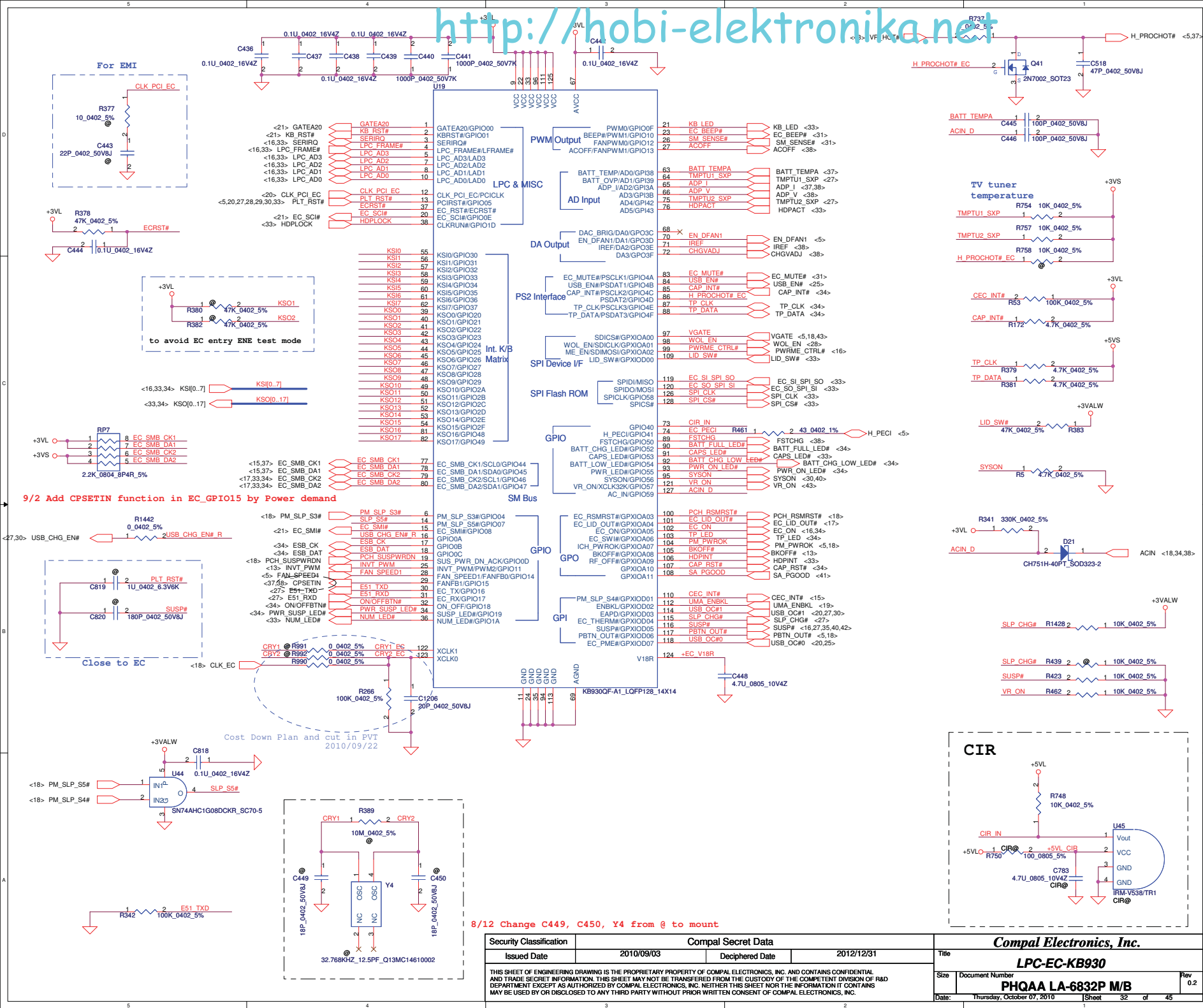
SENSE_A

<25> NBA_PLUG

39.2K_0402_1%

RA21

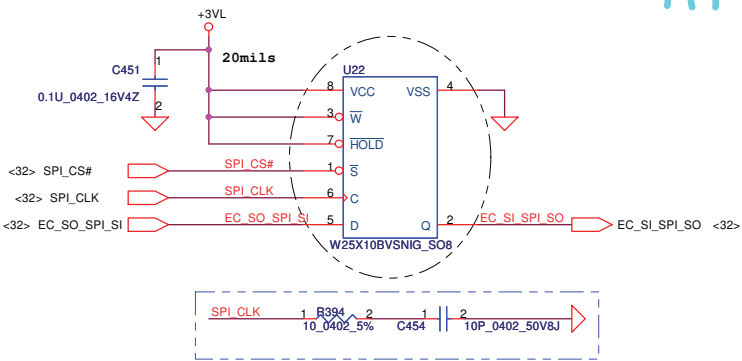
Compal Electronics, Inc.			
Title HDA-ALC269/HP/MIC			
Size	Document Number PHQAA LA-6832P M/B		Rev 0.2
Date:	Thursday, October 07, 2010	ISheet	31 of 45



8/12 Change C449, C450, Y4 from @ to mount

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2010/09/03		2012/12/31		LPC-EC-KB930	
PHQAA LA-6832P M/B		Rev		0.2	
Date:		Thursday, October 07, 2010		Sheet	
32		of		45	

SPI Flash (256KB)

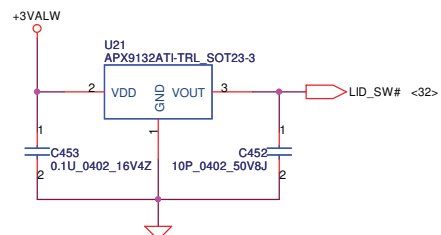


8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00

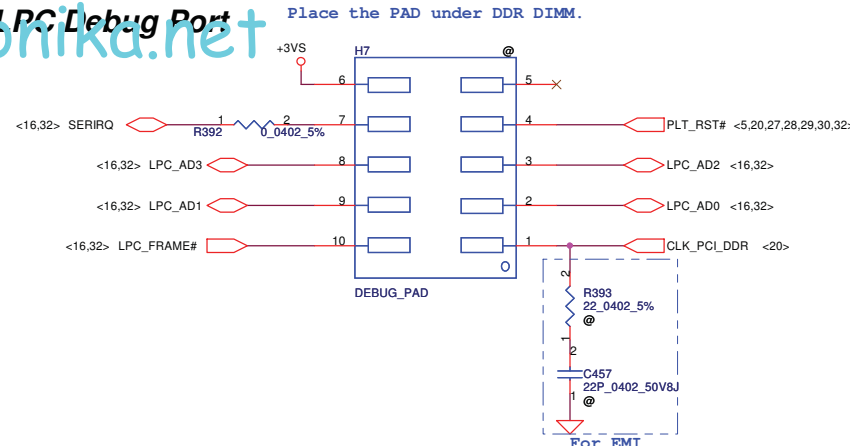
9/03 Change U22 change to SA00003FL10

<http://hobi-elektronika.net>

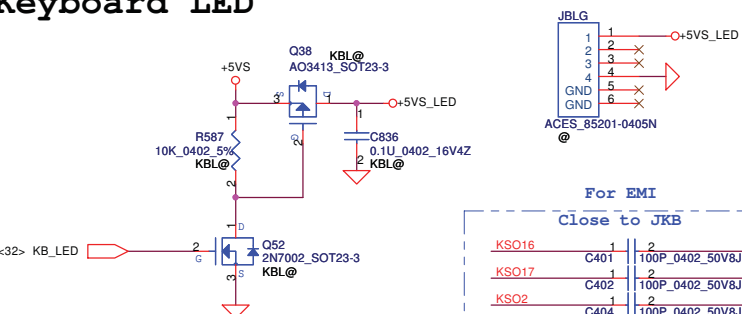
Lid SW



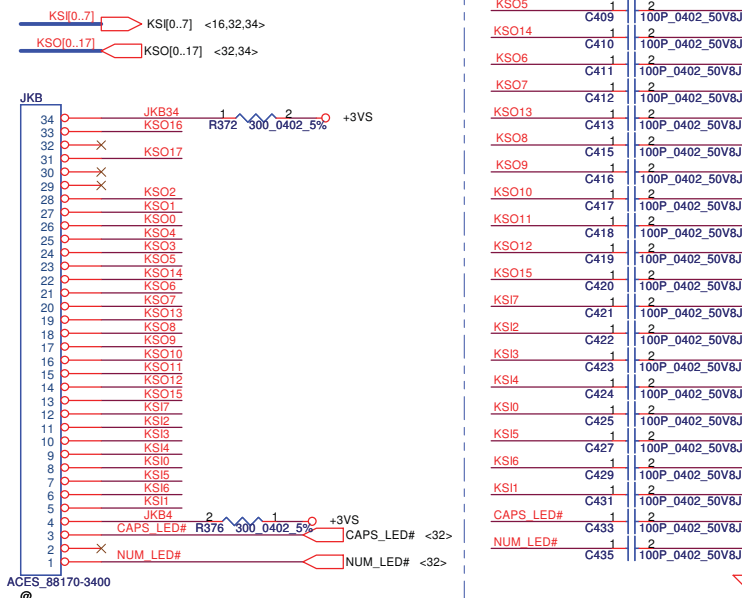
LPC Debug Port



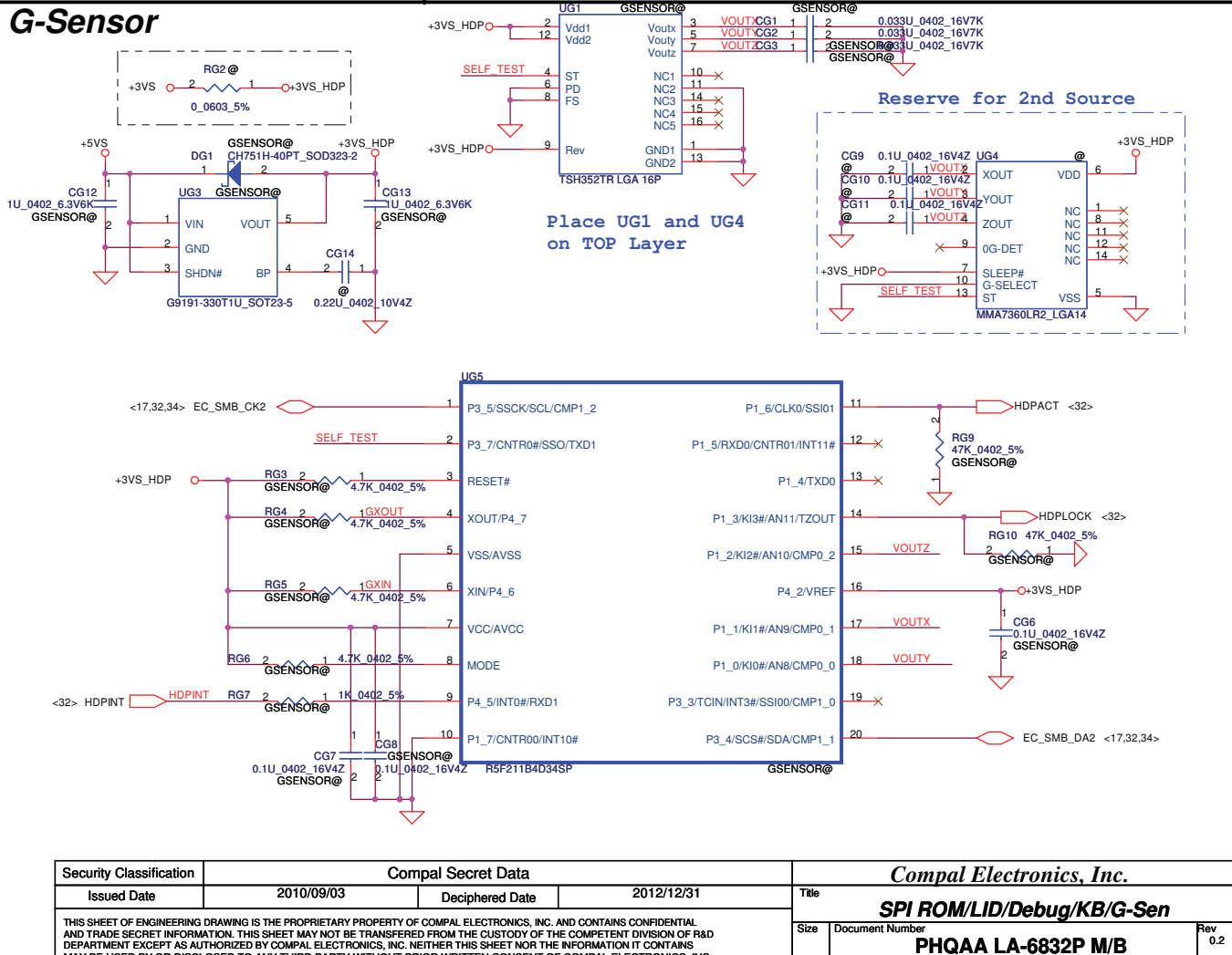
Keyboard LED



KEYBOARD CONN.

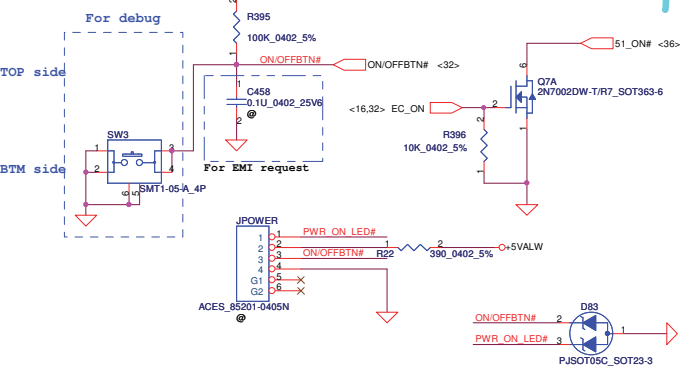


G-Sensor

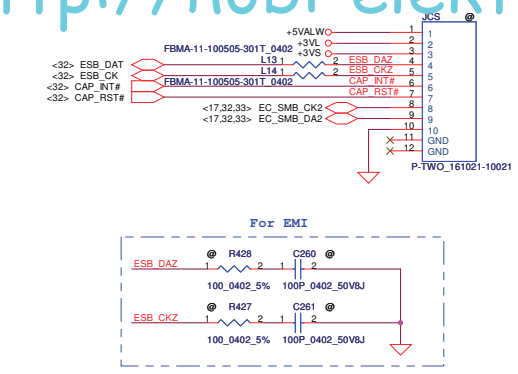


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Size	Document Number	PHQAA LA-6832P M/B		Rev 0.2
Date:	Thursday, October 07, 2010	Sheet	33	of 45

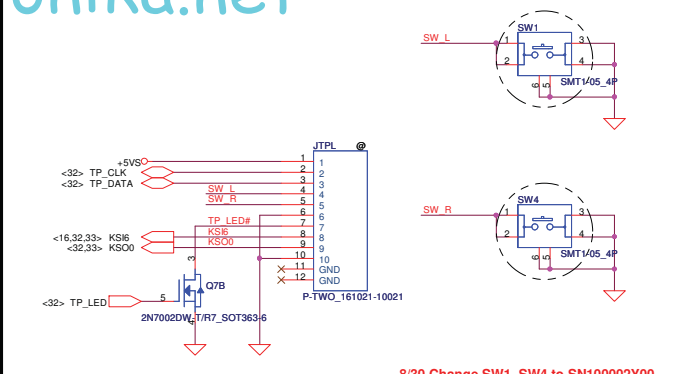
Power Button



Capacitor Sensor / Light Sensor Conn.



Touchpad & Light Pipe Connector

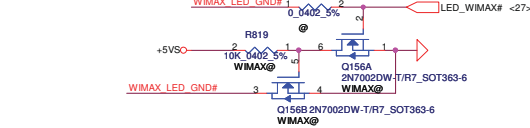


8/30 Change SW1, SW4 to SN10002Y00

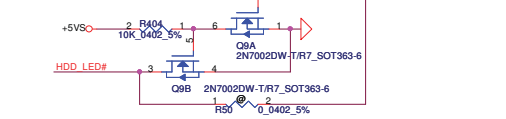
DC-IN LED



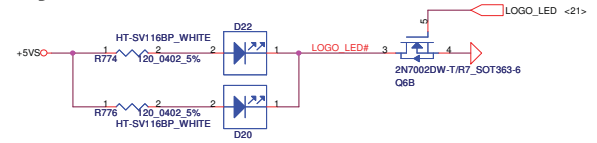
WiMAX LED



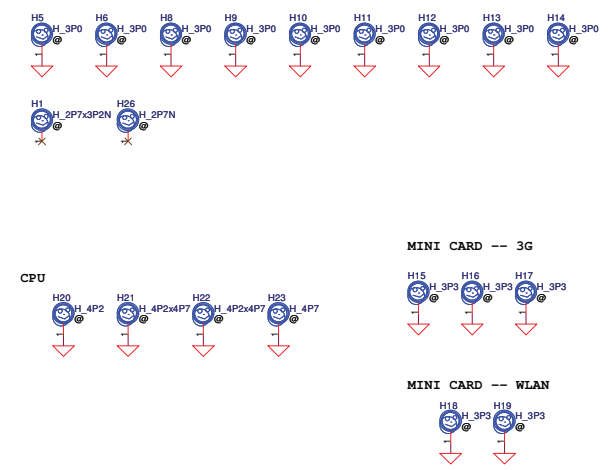
HDD LED



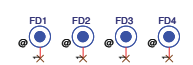
Logo LED



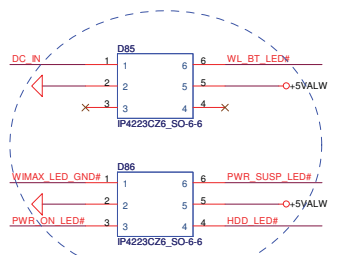
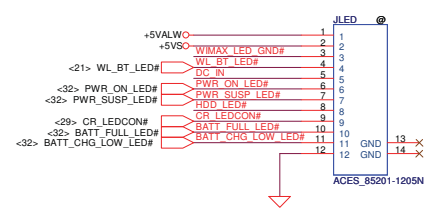
Screw Hole



PCB Federal Mark PAD

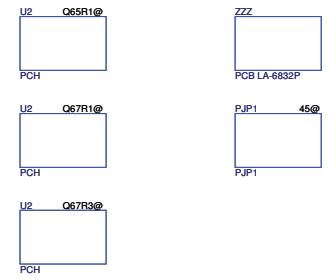


LED/B Connector

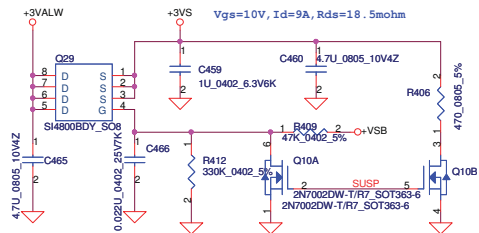


For ESD Demand 2010/10/01

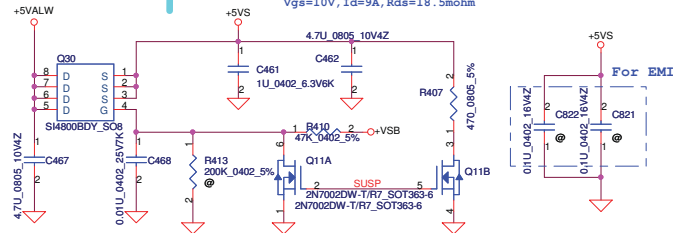
ISPD



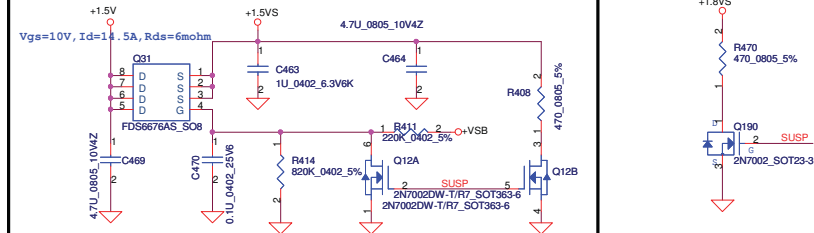
+3VALW TO +3VS



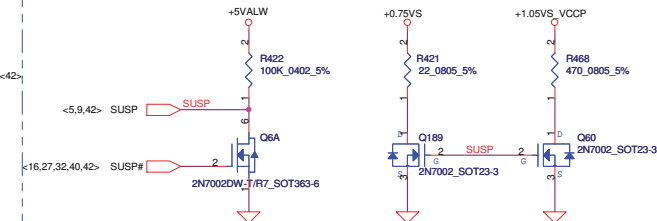
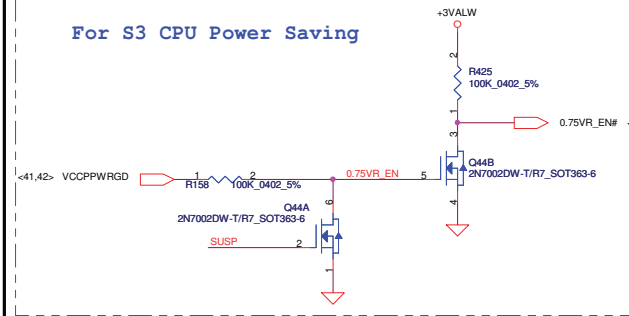
+5VALW TO +5VS



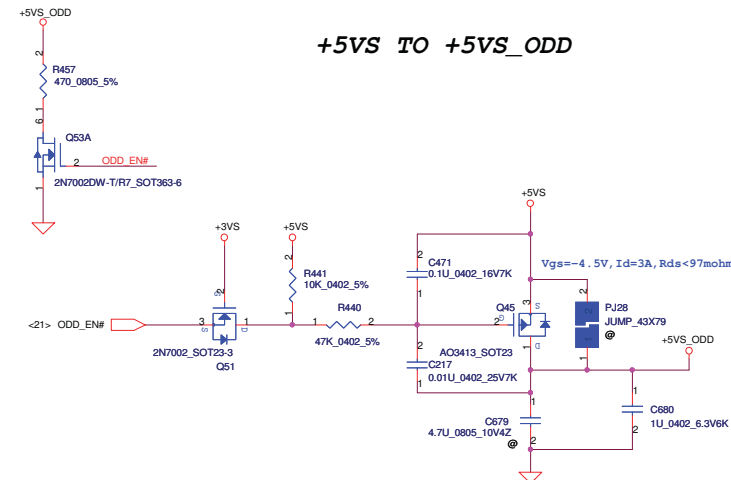
+1.5V to +1.5VS



For S3 CPU Power Saving

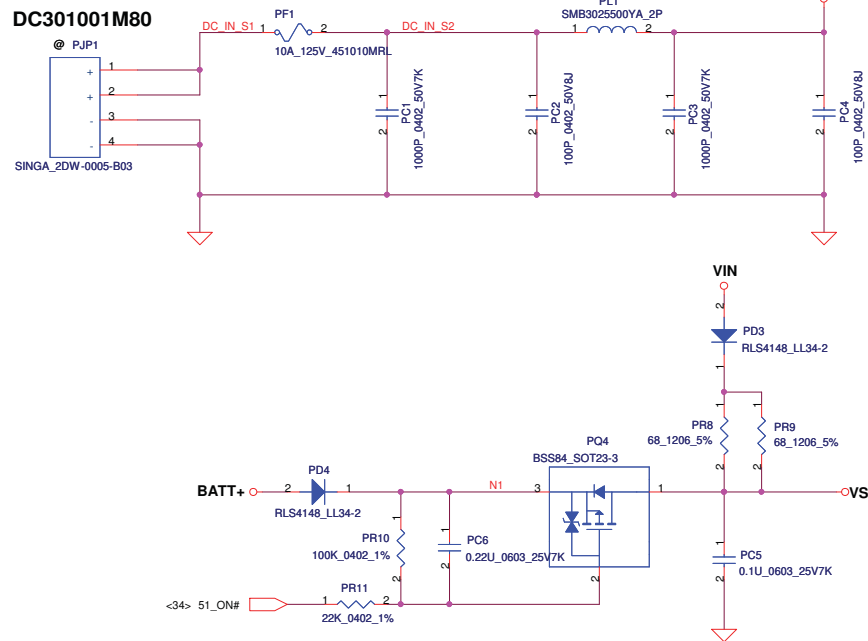


+5VS TO +5VS_ODD



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				PHQAA LA-6832P M/B	
				Date:	Thursday, October 07, 2010
				Sheet	35 of 45

DC301001M80



+3VALWP (5A, 200mils, Via NO.= 10)
OCP=8.6A

+0.75VSP (1A, 40mils, Via NO.= 2)

+5VALWP (5A, 200mils, Via NO.= 10)
OCP=7.9A

+VCCSAP (6A, 240mils, Via NO.= 12)

+1.8VSP (1.65A, 70mils, Via NO.= 4)
OCP=4.2A

+3VLP (100mA, 40mils, Via NO.= 2)

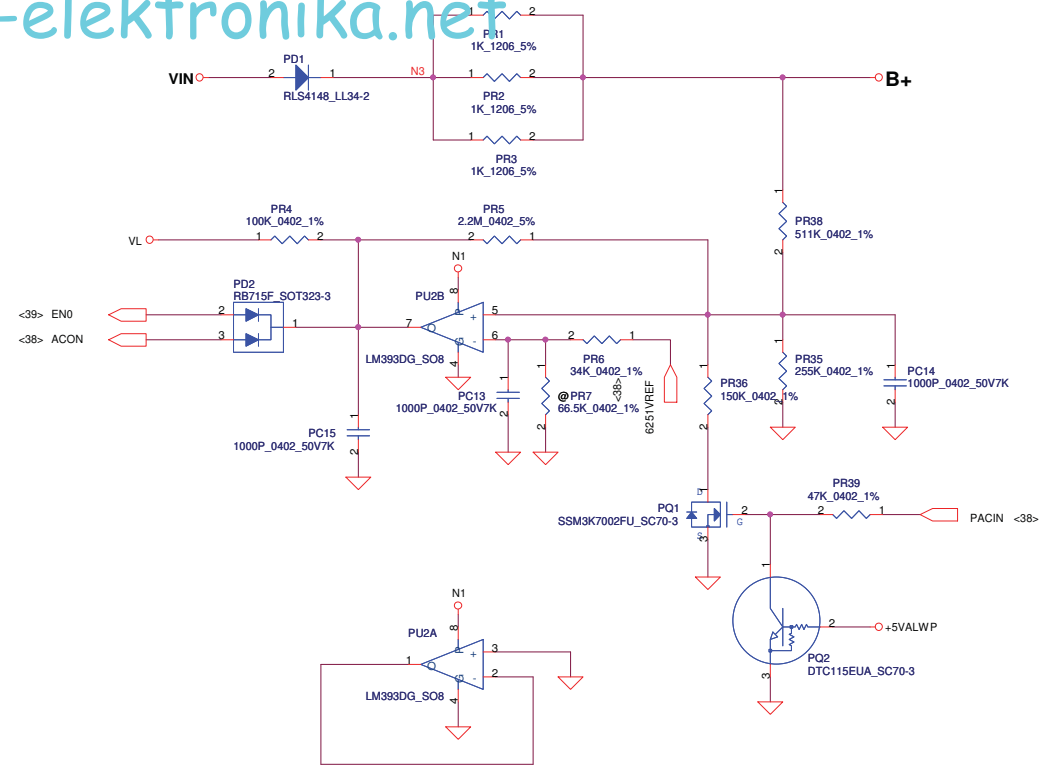
+VSBP (120mA, 40mils, Via NO.= 1)

VL (100mA, 40mils, Via NO.= 2)

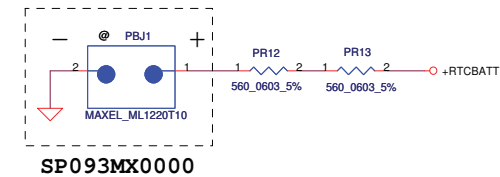
+1.5VP (16A, 640mils, Via NO.= 32)

+1.05VS_VCCPP (17A, 680mils, Via NO.=34)

+GFX_COREP (33A, 1320mils, Via NO.=66)
OCP=40A



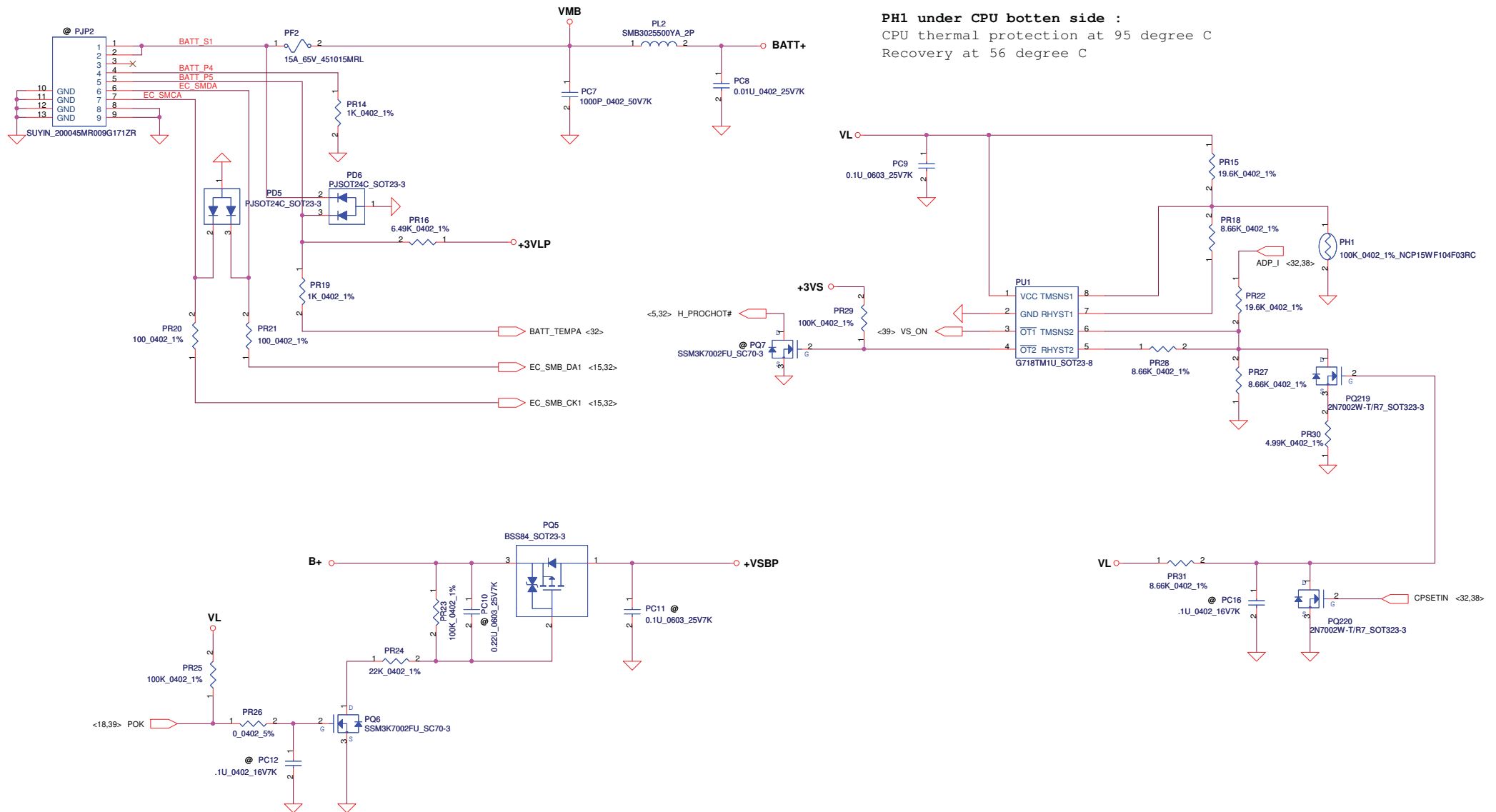
RTC Battery

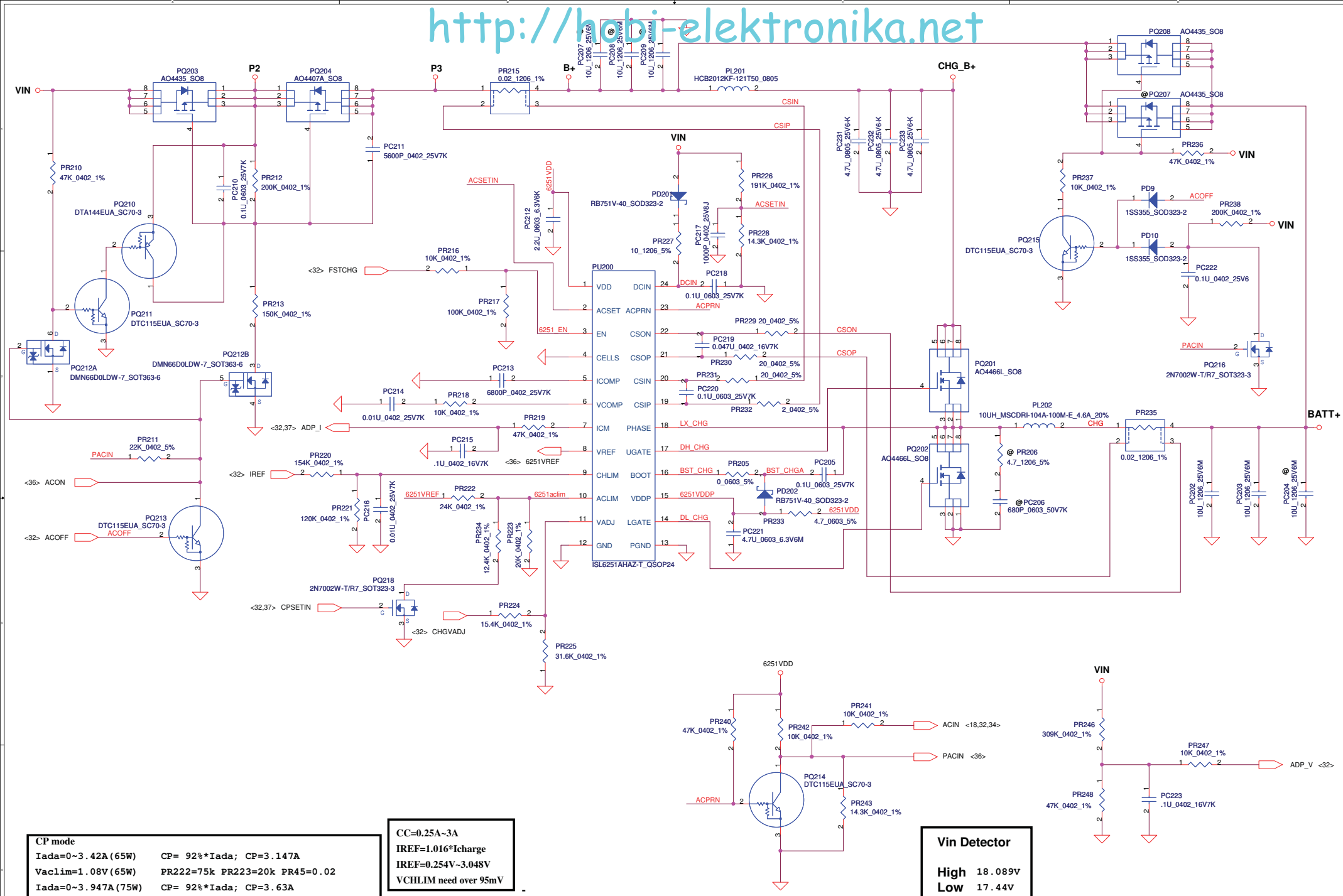


ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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					NHQA LA-6831P M/B	0.1
				Date:	Thursday, October 07, 2010	Sheet 36 of 58





CP mode

$I_{ada}=0\sim 3.42A$ (65W) $CP=92\%I_{ada}$; $CP=3.147A$
 $V_{acim}=1.08V$ (65W) $PR222=75k$ $PR223=20k$ $PR45=0.02$
 $I_{ada}=0\sim 3.947A$ (75W) $CP=92\%I_{ada}$; $CP=3.63A$
 $V_{acim}=0.736V$ (75W) $PR222=24k$ $PR223=20k$ $PR45=0.02$
 $I_{ada}=0\sim 4.737A$ (90W) $CP=92\%I_{ada}$; $CP=4.36A$
 $V_{acim}=0.736V$ (90W) $PR222=53.6k$ $PR223=20k$ $PR45=0.015$
 $I_{ada}=0\sim 6.316A$ (120W) $CP=92\%I_{ada}$; $CP=5.81A$
 $V_{acim}=0.736V$ (120W) $PR222=8.25k$ $PR223=26.7k$ $PR45=0.015$

CC=0.25A-3A

IREF=1.016*Icharge

IREF=0.254V-3.048V

VCHLM need over 95mV

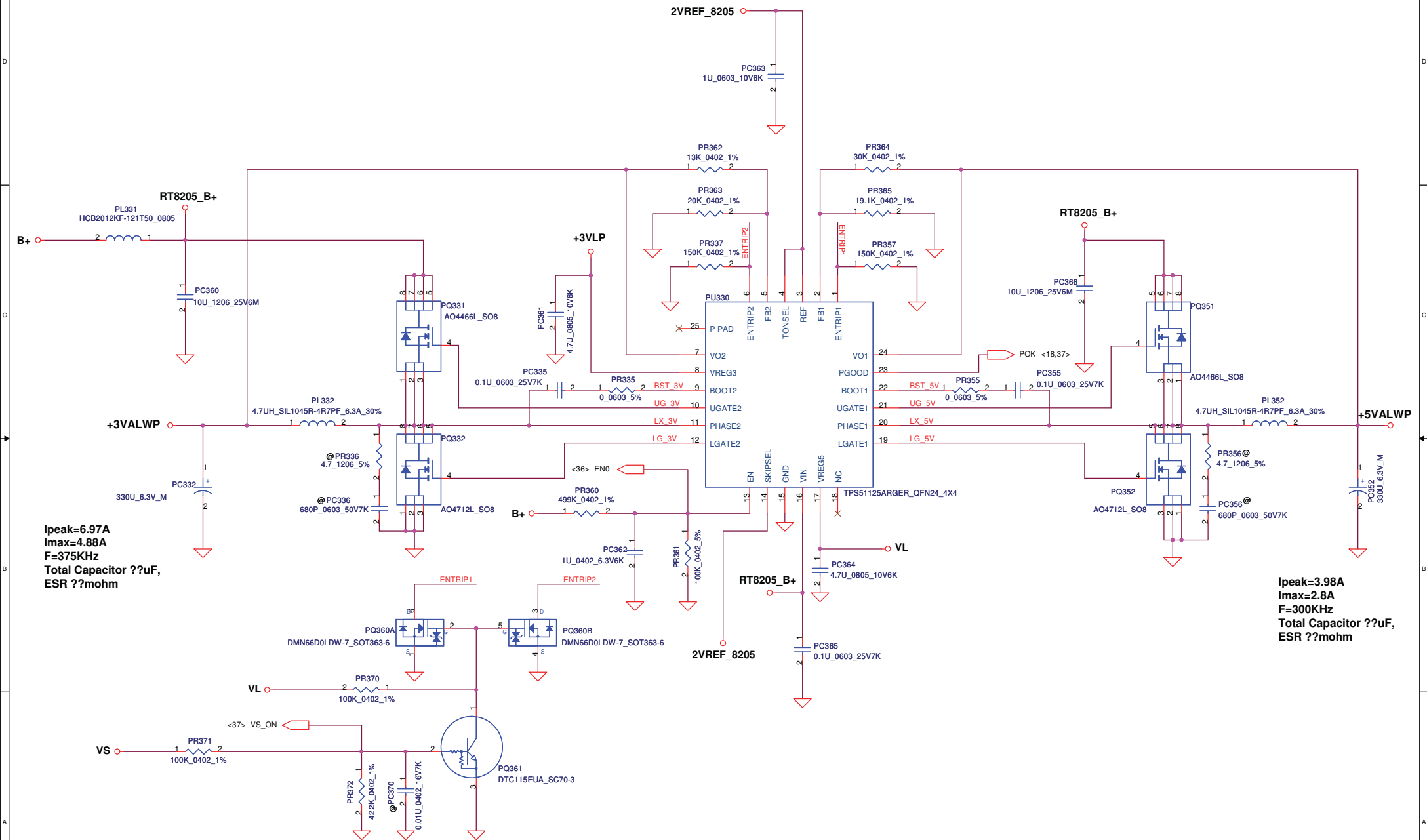
CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

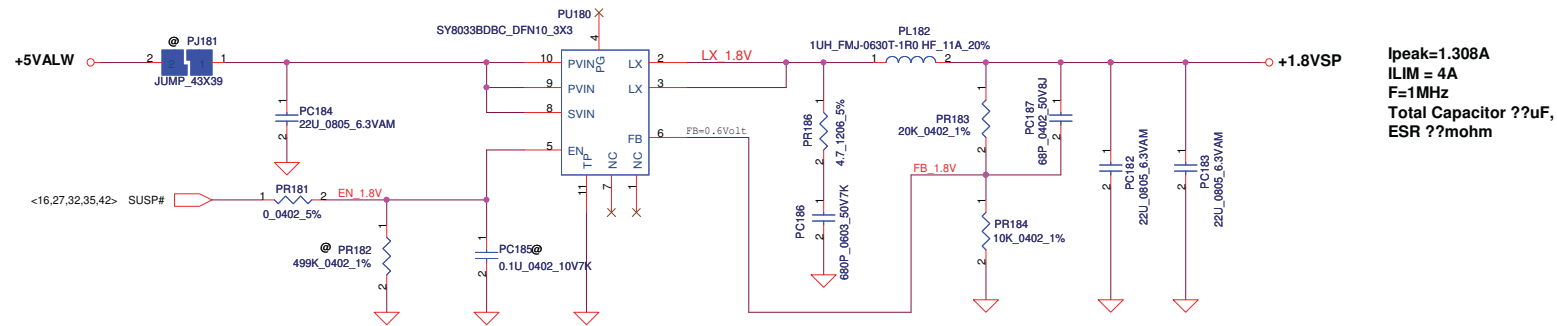
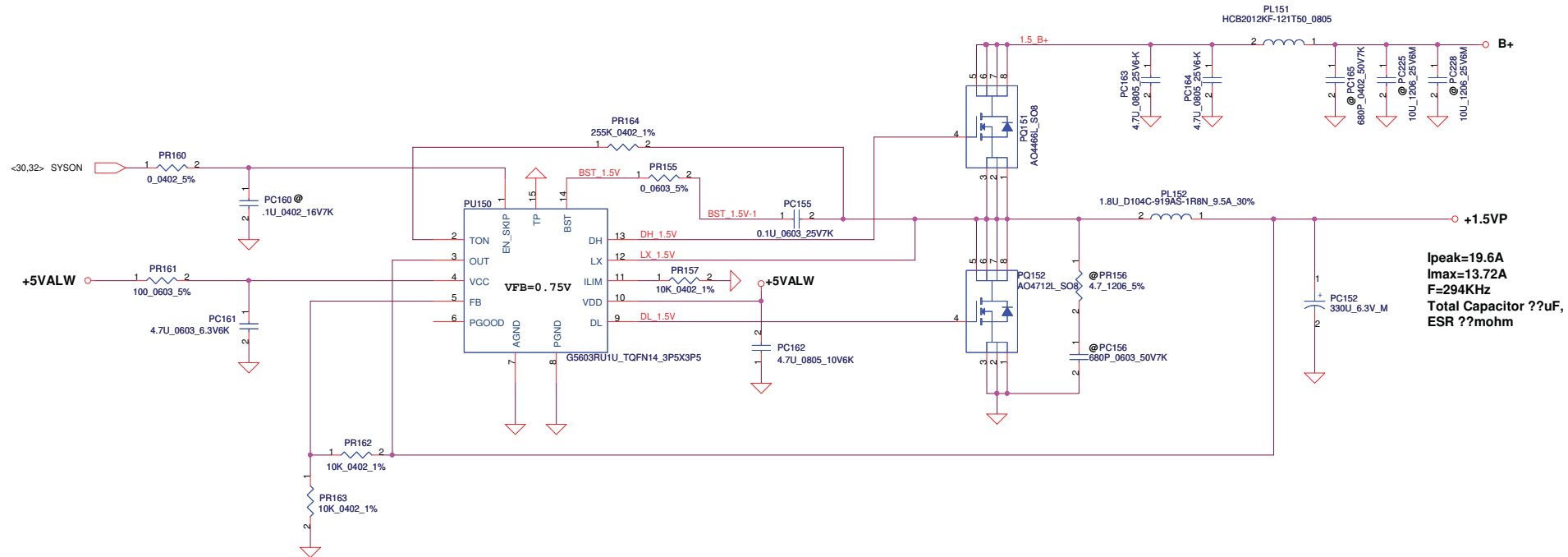
Vin Detector

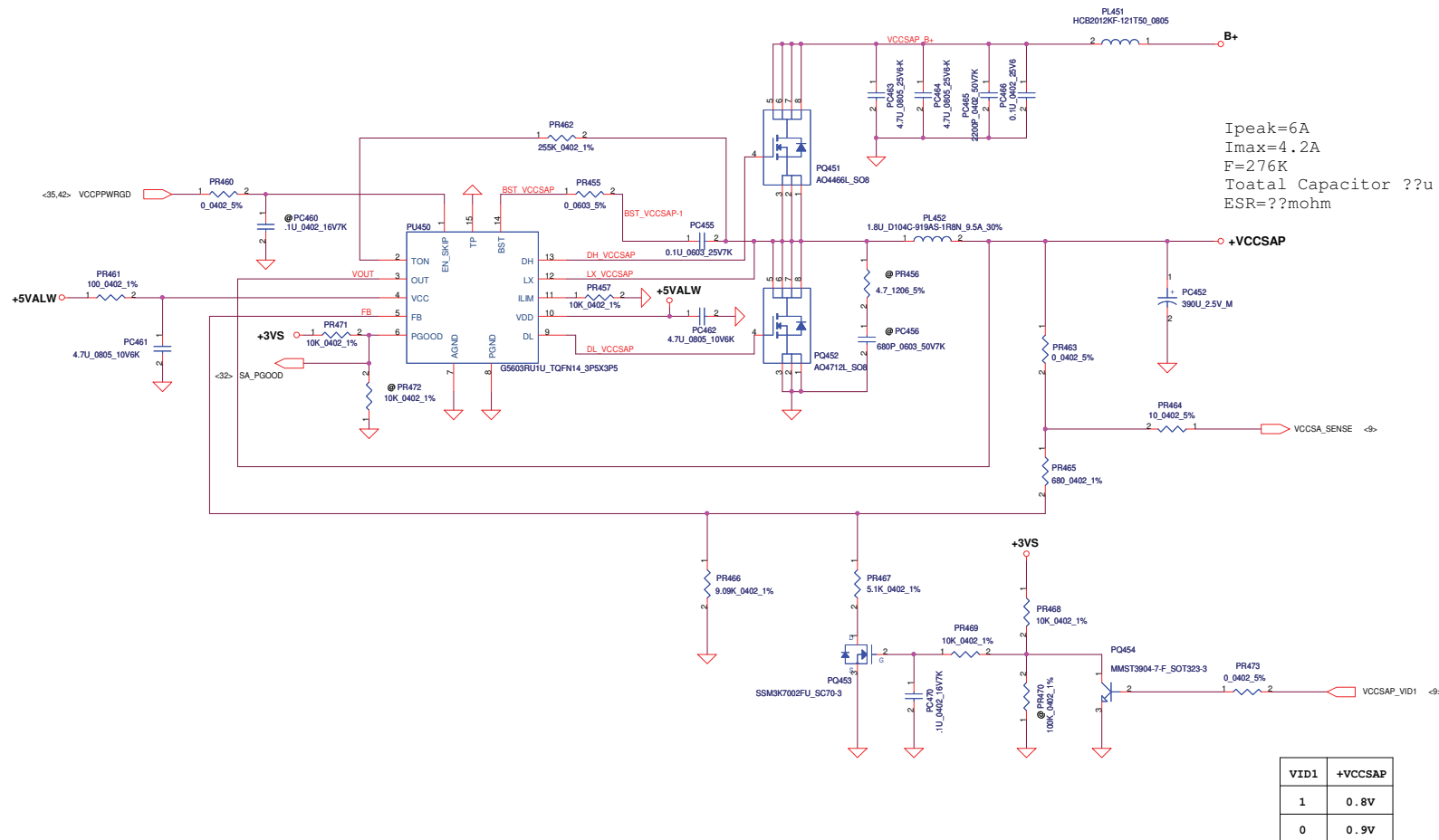
High 18.089V
 Low 17.44V

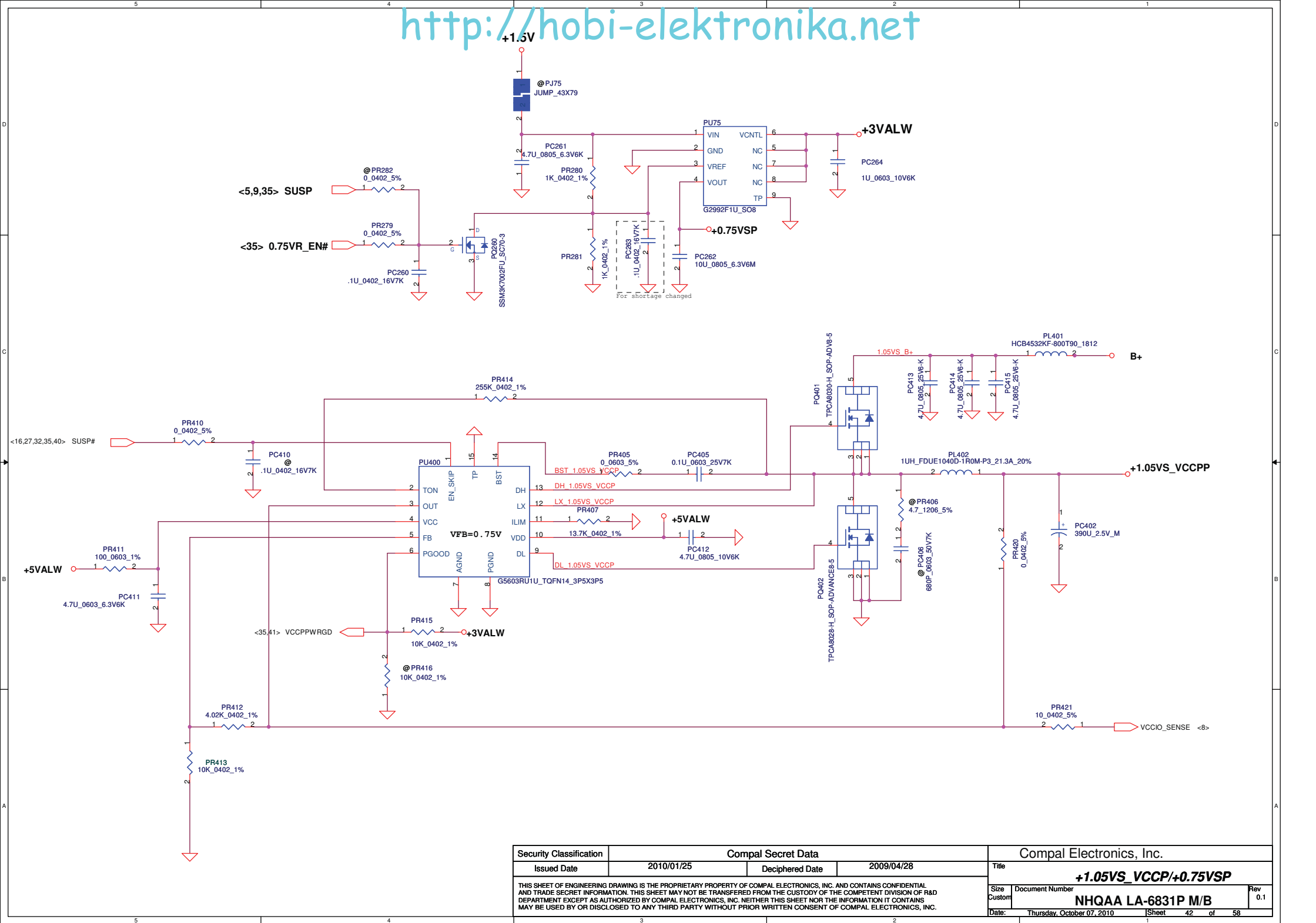
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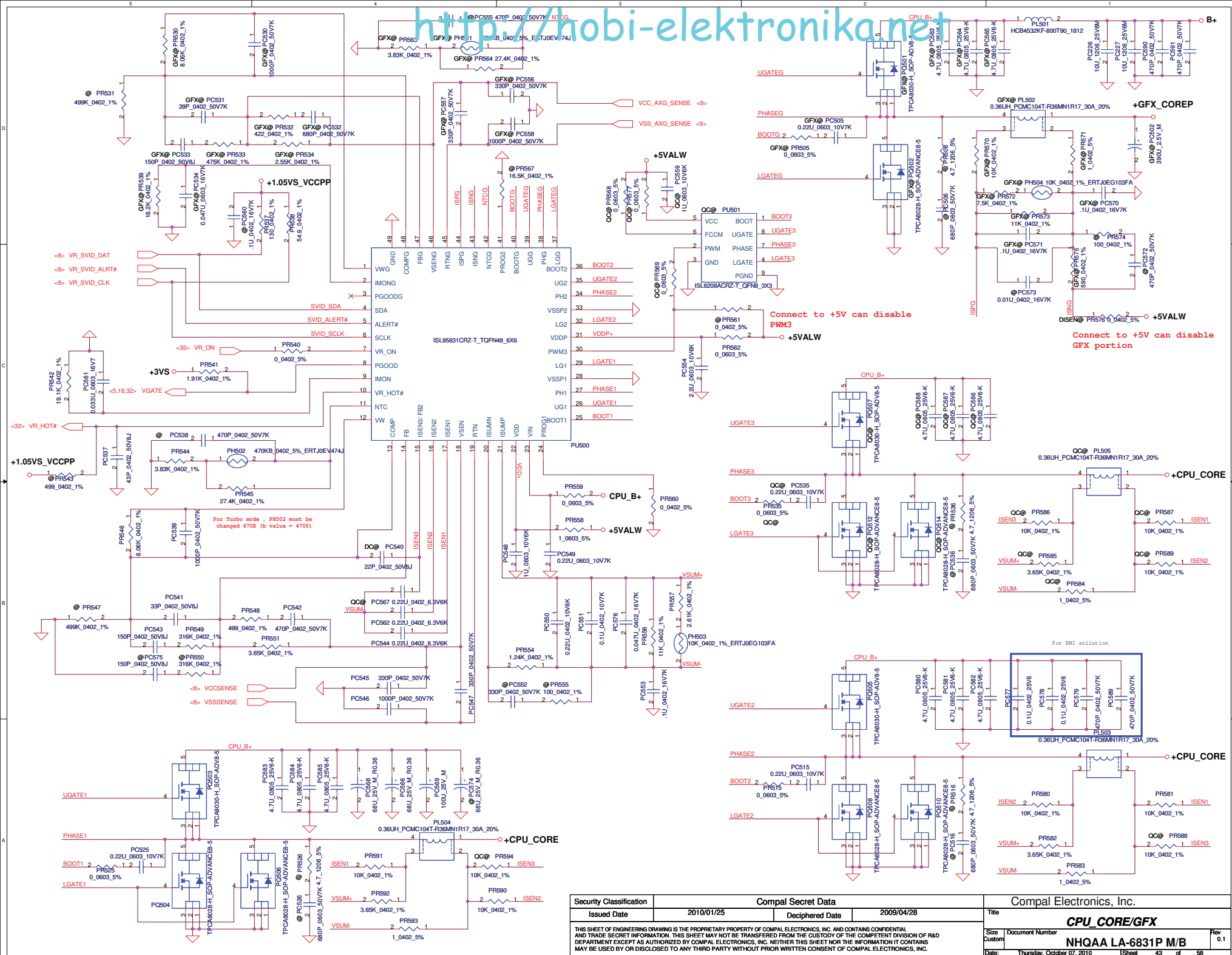






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Title			
CPU_CORE/GFX			
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2010/09/07	P37-PWR_BATTERY CONN / OTP	Remove PQ7 SSM317002FU	Adapter protect circuit not ready
2.	2010/09/07	P40-PWR+1.5VP/+1.8VSP	Change PQ152 to AO4712L	Use same part number
3.	2010/09/07	P41-PWR+VCCSAP	Change PQ452 to AO4712L	Use same part number
4.	2010/09/07	P40-PWR+1.5VP/+1.8VSP	Change PQ151 to AO446L	Use same part number
5.	2010/09/07	P53-PWR+VCCSAP	Change PQ451 to AO446L	Use same part number
6.	2010/09/07	P50-PWR-CHARGER	Change PQ201,PQ202 to AO4466L	Use same part number
7.	2010/09/07	P50-PWR-CHARGER	Change PQ203 to AO4435L and remove PQ207	For UMA SKU
8.	2010/09/07	P50-PWR-CHARGER	Add PR234 12.4k	For DC and QC CP setting
9.	2010/09/07	P55-PWR-CPU_CORE/GFX	Add PR560 0 Ohm	Set CPU VBOOT to 0V
10.	2010/09/07	P50-PWR-CHARGER	Add PR222 24k and PR223 20k	For CP setting
11.	2010/09/07	P55-PWR-CPU_CORE/GFX	Add PR544 3.83k,PR545 27.4k,PH502 470k	Add CPU NTC NET
12.	2010/09/07	P55-PWR-CPU_CORE/GFX	Change PR551 from 3.83k to 3.65k	For CPU_CORE load line
12.	2010/09/07	P55-PWR-CPU_CORE/GFX	Change PC550 0.33u to 0.22u and add PC551 0.1u	For shortage issue

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				Power PIR	
				Size	Rev
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HW PIR (Product Improve Record)

NWQAA LA-6832P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2010/09/03

NO DATE PAGE MODIFICATION LIST

PURPOSE

Item	Date	Page	Component	Solution	Request
1)	07/21		Delete	30g,DHDMIg,DI5g,EDPg,NO3Dg,OPTg,UMAg	For low cost Huron River
2)	08/11		Update room		
3)	08/11	09	Change	R119 change to g	
4)	08/12	16	Add	R442, R443	For SPI debug circuit
5)	08/12	16	Change	R572, R573, R574, R575, R569 from g to mount	For SPI debug circuit
6)	08/12	20	Remove	USB20_P3/N3 from PCH	Don't need USB20/30 BTO
7)	08/12	30	Remove	DT1, USB20, RT14, RT20, RT23, RT24	Don't need USB20/30 BTO
8)	08/12	32	Change	C449, C450, Y4 from g to mount	
9)	08/13	15	Change	L8, L9 L10, L11 from SM070001600 to SM070001310	For EMI demand
10)	08/13	30	Change	RT11 to g	
11)	08/13	30	Change	RT19 to USB30g	
12)	08/13	30	Change	CT3 from SE0000005TN0 to SE0000005T80	
13)	08/13	30	Remove	RT25, RT27	Don't need USB20/30 BTO
14)	08/17	5	Remove	R14	For HW Review demand
15)	08/18	6	Reserve	R33	For HW Review demand
16)	08/18	9	Reserve	R119	To follow CRB 1.0
17)	08/18	11	Remove	R32, R89	For HW Review demand
18)	08/18	12	Remove	R35, R97	For HW Review demand
19)	08/18	26	Reserve	C236, C268, C490	For HW Review demand
20)	08/18	15	Remove	R435, R438, R453(0 ohm)	
21)	08/18	15	Change	R195, R197, R198, R202, R201, R203, R205, R206 to SD028680080	
22)	08/18	15	Remove	R207	For HW Review demand
23)	08/18	18	Change	Net name from PM_CLKRUN# to PCH_GPI032	For HW Review demand
24)	08/18	20	Change	R324 From 1K to 2.2K	For Intel check list demand
25)	08/18	21	Remove	PCH PECL signal	By HW Review demand
26)	08/18	25	Remove	C363, C364, C365, C366	By HW Review demand
27)	08/18	30	Change	U74 to SA00004600	For CIC demand
28)	08/18	30	Change	USB30g to always mount	Due to no BTO USB20/30.
29)	08/18	27	Remove	all new card function	
30)	08/20	9	Add	PJ32	For Cost down +1.5V to +1.5V_CPU
31)	08/20	13	Swap	USB20_P11 and USB20_N11	For layout request
32)	08/20	25	Swap	USB20_P0, USB20_N0, USB20_P1, USB20_N1	For layout request
33)	08/23		Update Power schematic		
34)	08/23	20	Swap	PCI_PIRQC#, PCH_GPI04, PCH_GPI02, PCI_PIRQA#	For layout request
35)	08/23	20	Swap	SLP_CHG_M3, SLP_CHG_M4, USB_OC#0	For layout request
36)	08/30	18	Reserve	R259	For cost down plan
37)	08/30		Change	USB3.0 Connector	For ME demand
38)	08/30	21	Add	USB Sleep & Charge MAXIC_Select pin in GPIO71(Remove T73)	For MAX14550E/14566B co-lay
39)	08/30	25	Change	C426 to Aluminum Solid Cap 220u	For cost down
40)	08/30	27	Add	USB Sleep & Charge IC: MAX14550E	
41)	08/30	28	Add	16pin X'form for cost down, and P/N is SP050006E00	For cost down
42)	08/30	28	Change	PWRME_CTRL# from PCH_GPI033 to HDA_SDO	By Intel spec
43)	08/30	16	Change	U53 PIN 9 from KS14 to KS13	
44)	08/30	16	Change	R442, R443 from 10k to 100k	
45)	08/30	16	Change	U56 Pin3 from K506 to +5VALW	
46)	08/30	16	Add	R227 100k ohm	
47)	08/30	28	Reserve	D85 and D86	For ESD request
48)	08/30	30	Swap	U3RXDN1_R, U3RXDN1_R_L, U3RXDP1_R, U3RXDP1_R_L	For layout request
49)	08/30	16	Change	U13 from SA000021A00 to SA000031N00	Due to EOL of SA000021A00
50)	08/30	27	Reserve	R1443 for WLAN Mini PCIE Card Pin5	
51)	08/30	33	Change	U22 From SA00003GK00 to SA00003GM10	Due to EOL of SA00003GK00
52)	08/30	34	Change	SW1, SW4 to SN100002Y00	
53)	09/01	28	Add	LL5 for ISN Test	For EMI demand
54)	09/01	31	Change	RA12 from 10k to 4.7kohm and CA18 from 0.1uF to 100pF	For Beep by A51 demand.
55)	09/01	32	Add	CPSETIN to power	For 65W/75W select
56)	09/01	18,20,21	Reserve	C894, C895, C896, C897	For ESD request
57)	09/02	08	Remove, add	C126, C131 and add C898 3Pin Bulk Cap	By Power Demand
58)	09/02	27	Add	14566g & 14550g	
59)	09/02	27	Change	U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4	
60)	09/02	33	Change	EC ROM size from 256KB(SA00003GM10) to 128KB(SA00003FL10)	
61)	09/02	11	Change	C165,C166,C168,C171,C174,C176,C178 from SE093106M80 to SE0000005T80	For sourcer demand
62)	09/02	12	Change	C191,C192,C194,C197,C200,C202,C204 from SE093106M80 to SE0000005T80	For sourcer demand
63)	09/02		Change	CT25 from SE093106K80 (10uF_0805) to SE0000005T80 (10uF_0603)	For sourcer demand
64)	09/03	08	Change	C890, C891, C894 from SGA000005R00 to SGA00004X80	For Power demand
65)	09/06	33	Change	U22 change to SA00003FL10	
66)	09/06	28	Delete	U14 8105ELDOg and 8105ESWRg	

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