

COMPAL CONFIDENTIAL

MODEL NAME : QAL80
PCB NO : LA-7781P (DA600000OP10)
BOM P/N : 4319EK31L01
GPIO MAP: E4_VC_GPIO_map_rev_1.1

Dalmore 14 UMA

Ivy Bridge + Panther POINT
2012-02-24
REV : 1.0 (A00)
@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
ATG TPM	L51	1@ 5@
ATG Non-TPM	L52	2@ 5@
TPM	L01	1@
Non-TPM	L02	2@

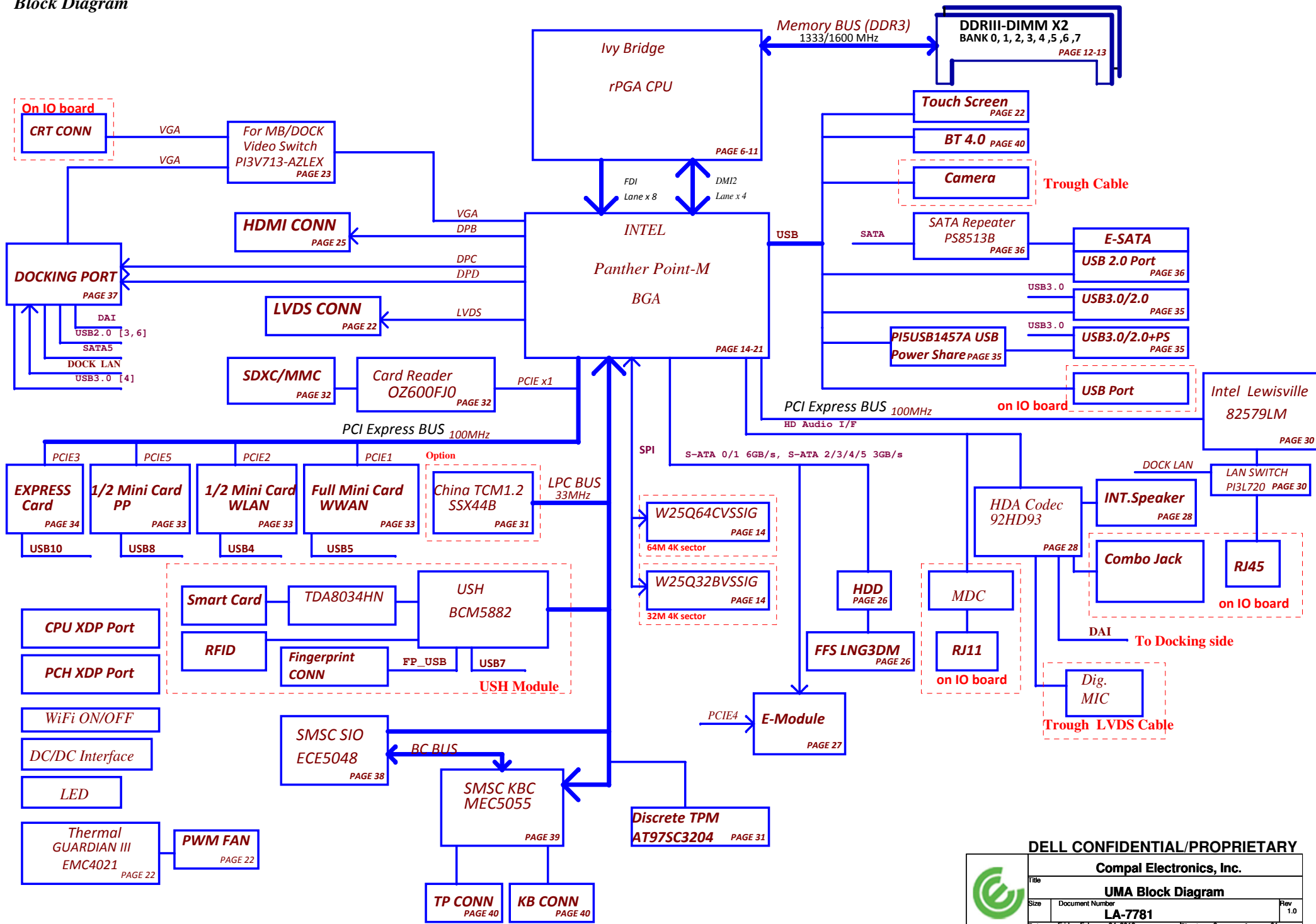
Part Number	Description
DA600000OP10	PCB OLD LA-7781P REV1 M/B UMA

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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+PWR_SRC_S +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask		0.50
			Add Plating		1.45
1	Top		Copper foil	0.5oz	0.65
			Prepreg	1080	2.60
2	VCC		Copper foil	1oz	1.35
			Core	3mil	3.00
3	Sig 1		Copper foil	1oz	1.35
			Prepreg	7628 HRC*2.2116+7628 HRC*2	33.50
4	Sig 2		Copper foil	1oz	1.35
			Core	3mil	3.00
5	GND		Copper foil	1oz	1.35
			Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.45
			SolderMask		0.50
Overall Thickness (1.4mm ± 10%)				55.1	55.30000

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side Top)
	1	JUSB2 (Right side Bottom)
	2	JESA1 (Right side ESATA)
	3	DOCKING
	4	WLAN
	5	WWAN
	6	DOCKING
	7	USH->BIO
	8	JMINI3(Flash)
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

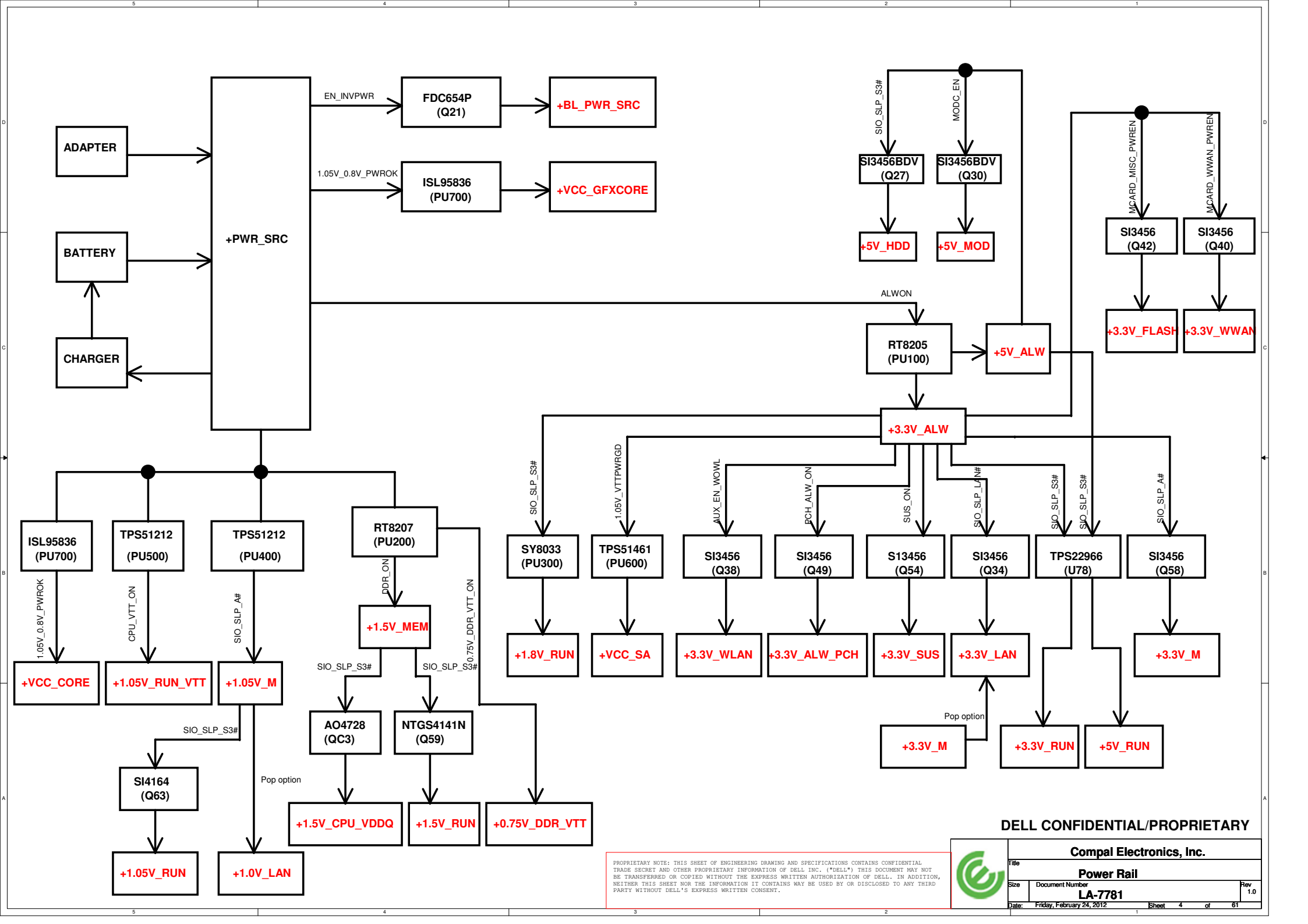
USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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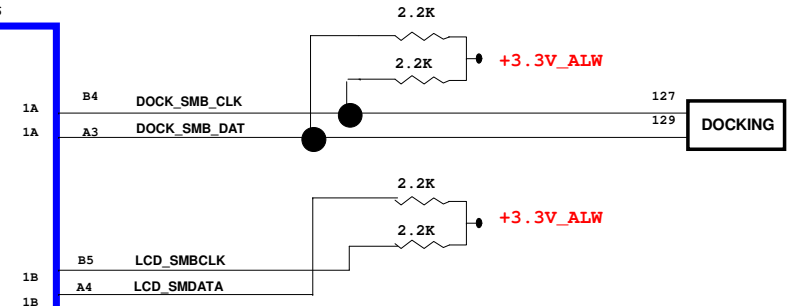
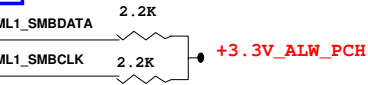
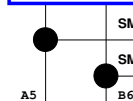
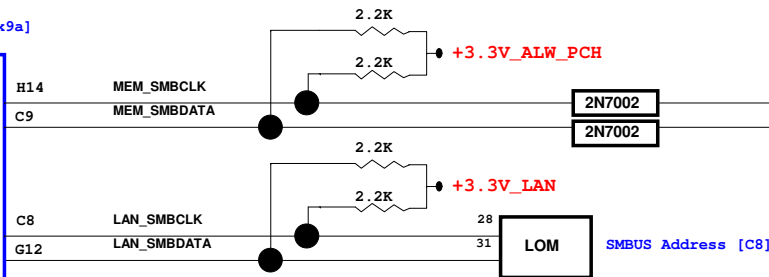
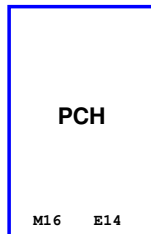
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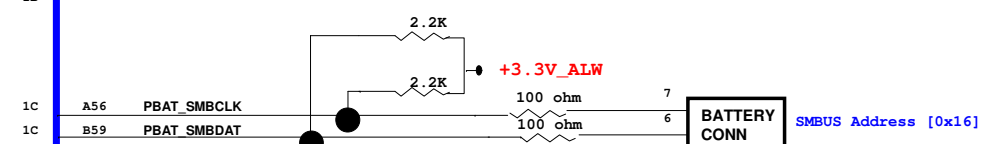
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SMBUS Address [0x9a]

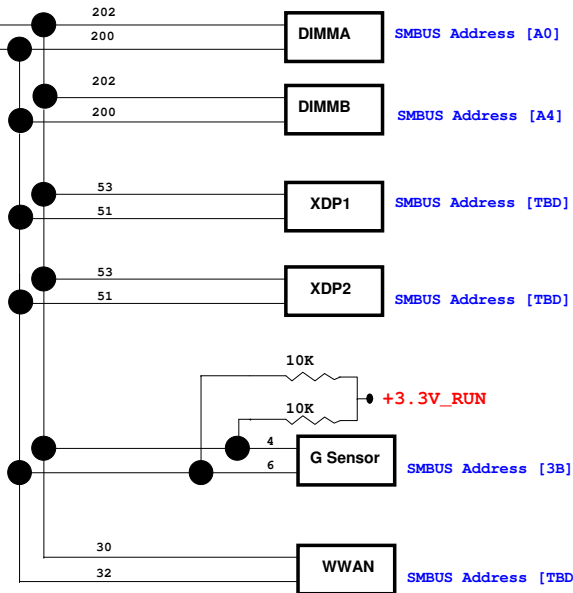
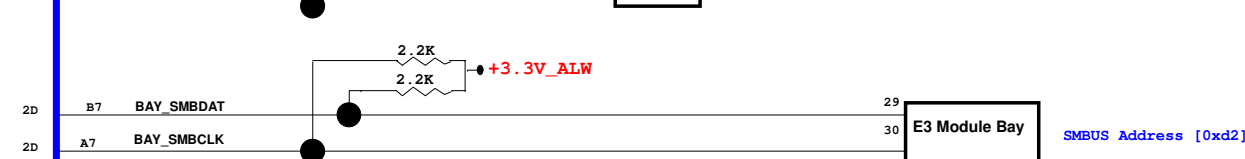
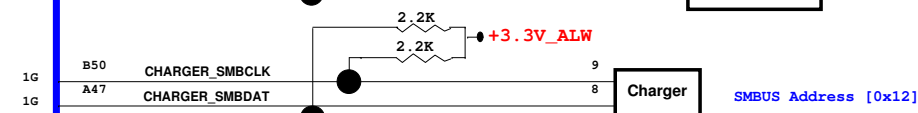
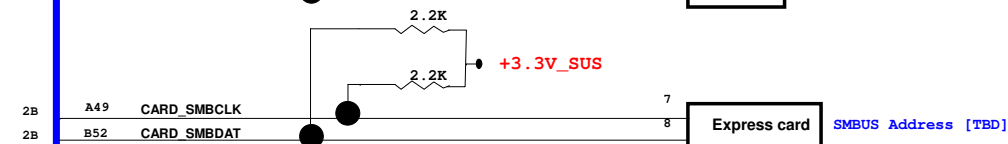
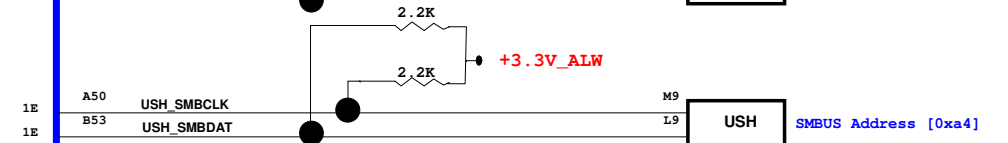


SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

KBC



MEC 5065

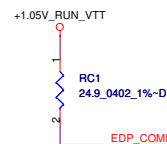


+1.05V_RUN_VTT

RC2

24.9_0402_1%~D

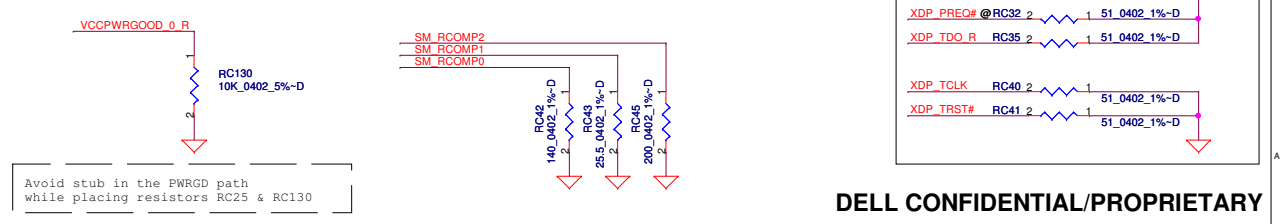
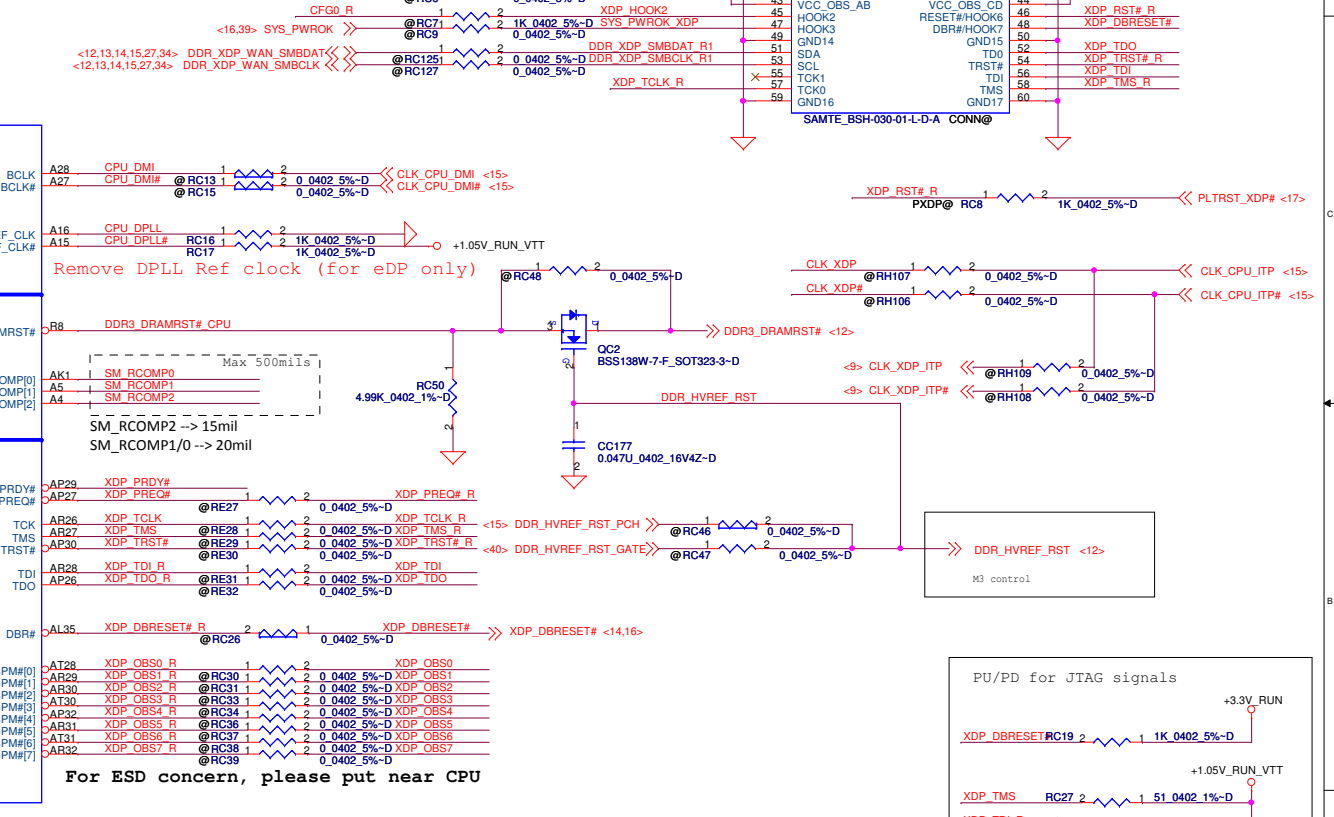
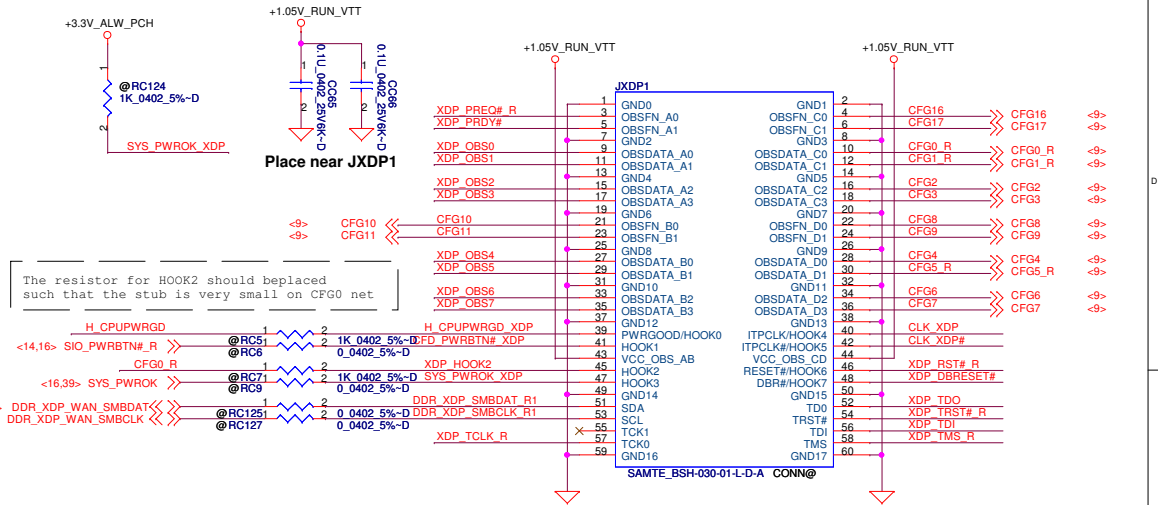
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

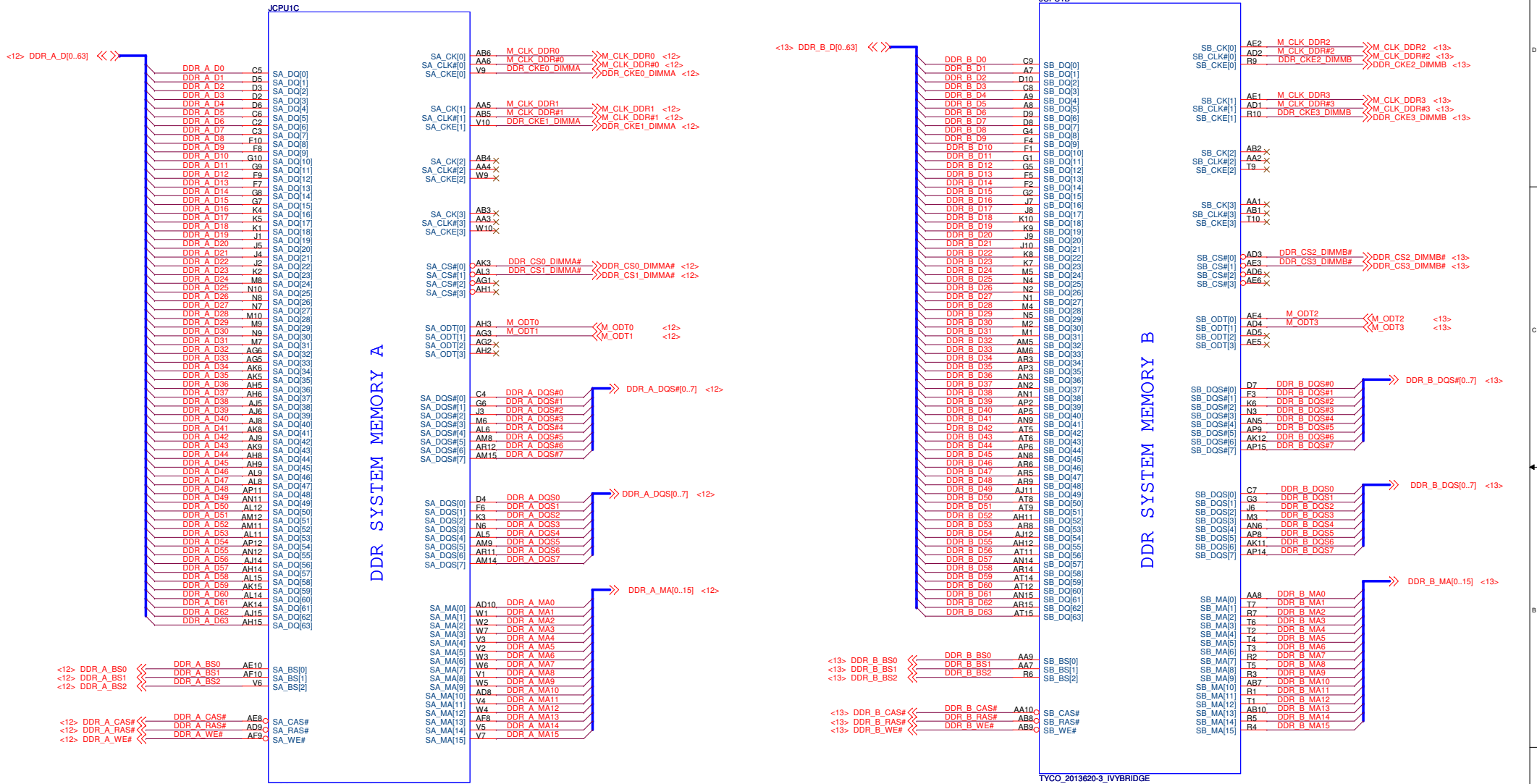


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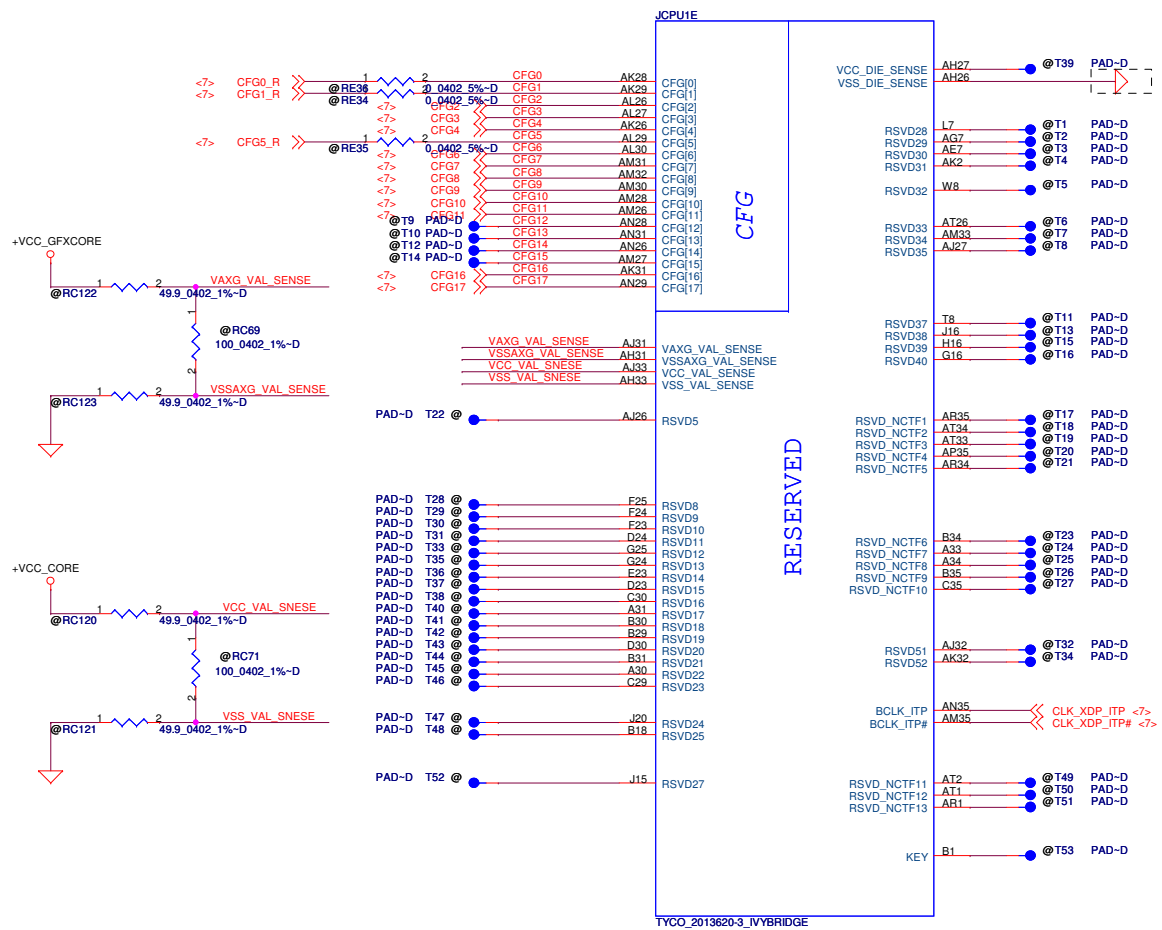
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Title			
Ivy Bridge (1/6)			
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CFG Straps for Processor



CFG2

@RC51
1K_0402_5%-D

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

CFG4

@RC52
1K_0402_5%-D

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6

CFG5

@RC54
1K_0402_5%-D

@RC53
1K_0402_5%-D

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7

@RC56
1K_0402_5%-D

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

JCPU1F

+VCC CORE
53A

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- V35 VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- V25 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+1.05V_RUN_VTT

8.5A

- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AG10
- VCCIO4 AC10
- VCCIO5 Y10
- VCCIO6 U10
- VCCIO7 P10
- VCCIO8 L10
- VCCIO9 J14
- VCCIO10 J13
- VCCIO11 J12
- VCCIO12 J11
- VCCIO13 H14
- VCCIO14 H12
- VCCIO15 H11
- VCCIO16 G14
- VCCIO17 G13
- VCCIO18 G12
- VCCIO19 F14
- VCCIO20 F13
- VCCIO21 F12
- VCCIO22 F11
- VCCIO23 E14
- VCCIO24 E12
- VCCIO25 D14
- VCCIO26 D13
- VCCIO27 D12
- VCCIO28 D11
- VCCIO29 C14
- VCCIO30 C13
- VCCIO31 C12
- VCCIO32 C11
- VCCIO33 B14
- VCCIO34 B12
- VCCIO35 A14
- VCCIO36 A13
- VCCIO37 A12
- VCCIO38 A11
- VCCIO39 J23
- VCCIO40 J23

Note: Place the PU resistors close to CPU
RC61 close to CPU 300 - 1500mils

H_CPU_SVIDALRT# 1 RC61 2 43_0402_5%-D <<VIDALERT_N <51>

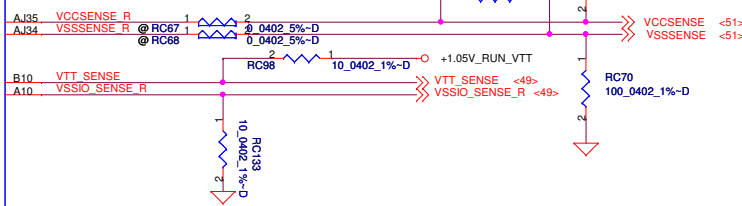
+1.05V_RUN_VTT

CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

RC63 130_0402_1%-D

H_CPU_SVIDALRT# must be routed between the VIDSOUT and VIDSCLK lines to reduce cross talk. 18 mils spacing to others.

Place RC66, RC70, RC75 near CPU



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *
* Description 5A to Mem controller(+1.5V_CPU_VDDQ) 5-6A to 2 DIMMs/channel 2-5A to +1.5V_RUN & +0.75V_DDR_VTT		

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Ivy Bridge (1/6)

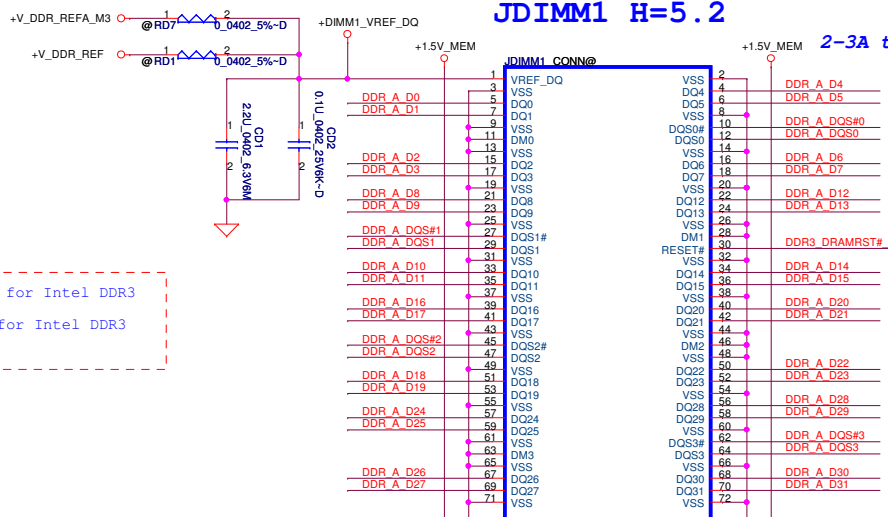
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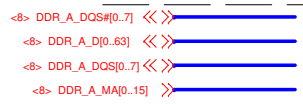
JDIMM1 H=5.2

2-3A to 1 DIMMs/channel

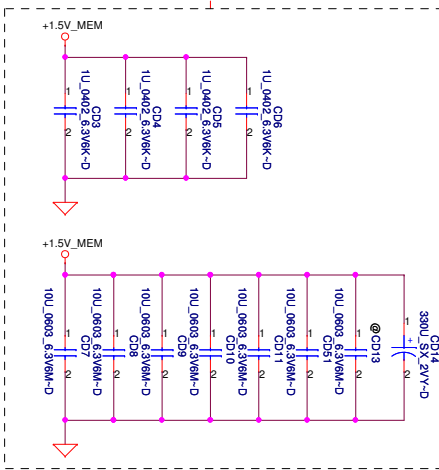


```
Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3
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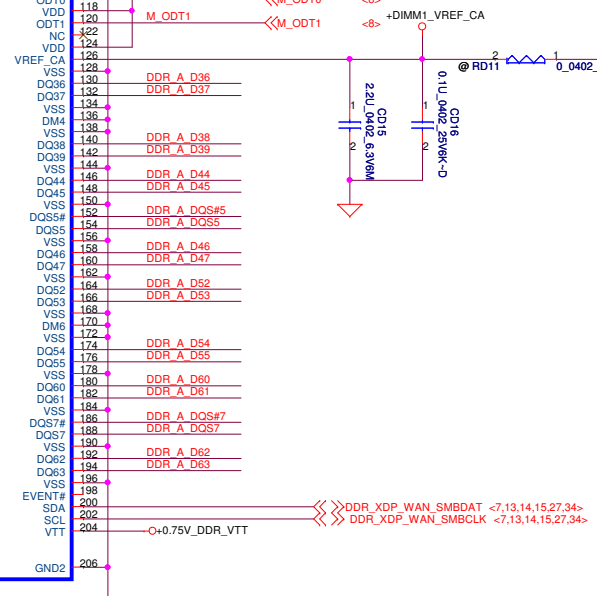
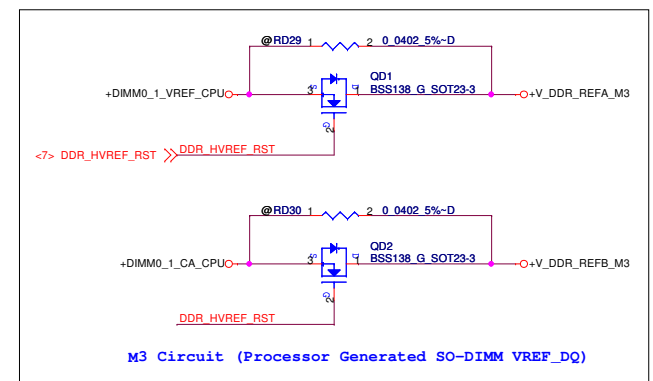
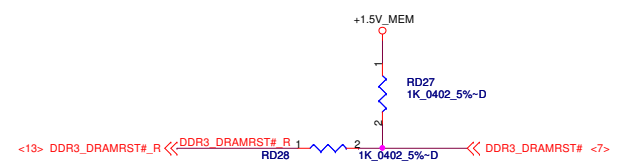
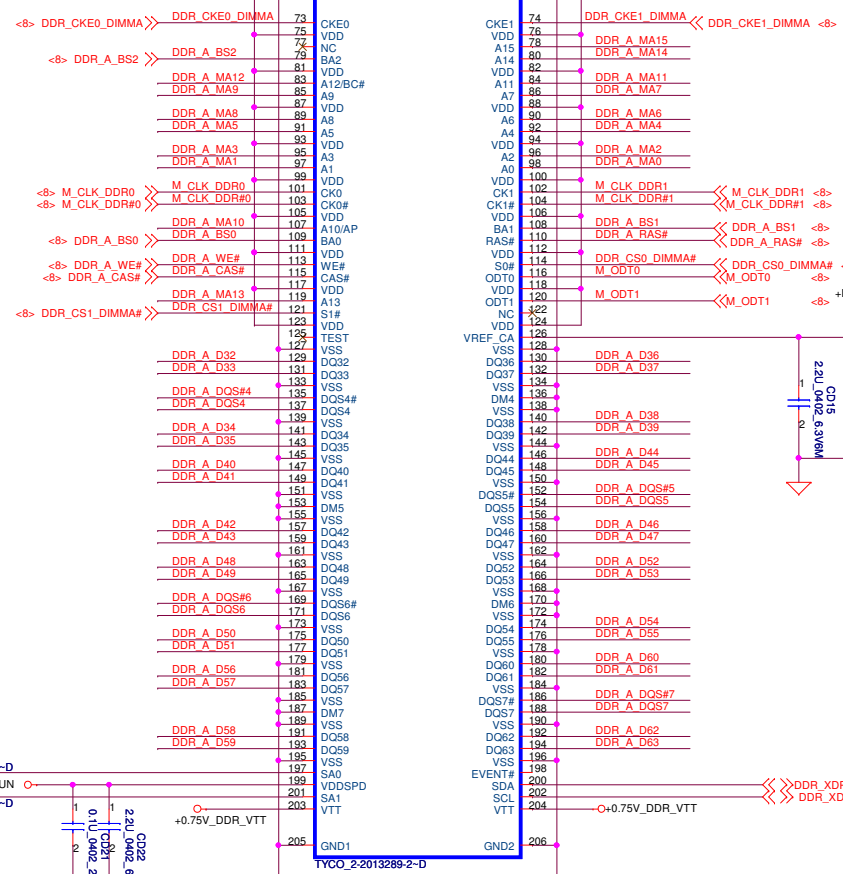
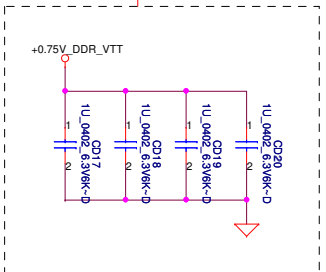
All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



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DDRIII-SODIMM SLOT1

Number
LA-7781

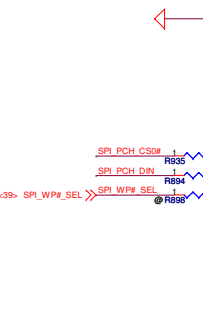
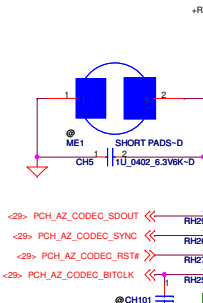
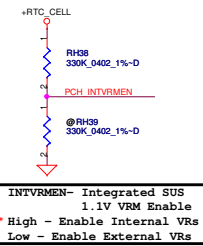
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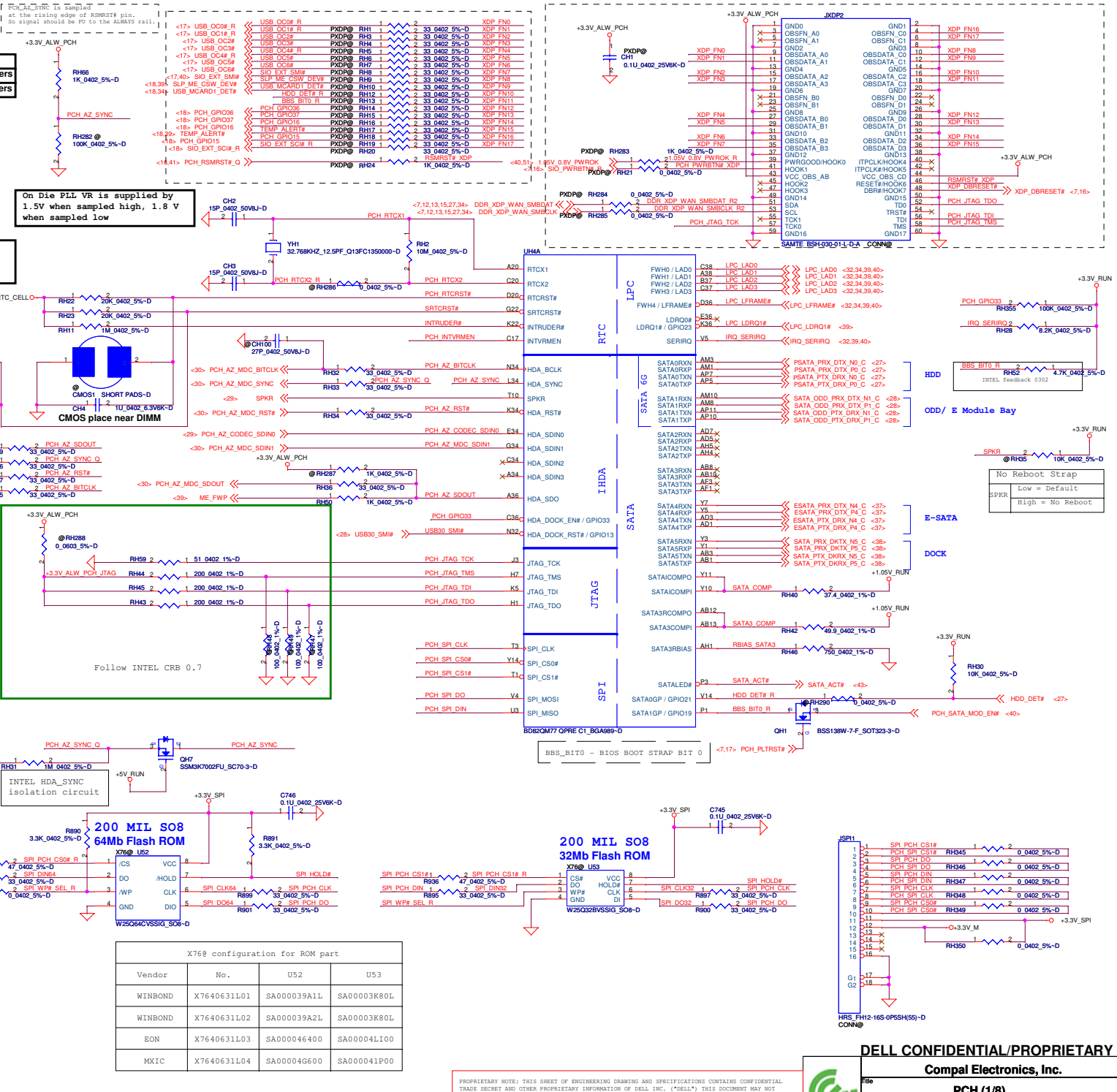
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CMOS CLR1		CMOS setting	
Shunt	Clear CMOS	Shunt	Clear ME RTC Registers
Open	Keep CMOS	Open	Keep ME RTC Registers



X76@ configuration for ROM part			
Vendor	No.	U52	U53
WINBOND	X7640631L01	SA000039A1L	SA00003K80L
WINBOND	X7640631L02	SA000039A2L	SA00003K80L
EON	X7640631L03	SA000046400	SA00004L100
MXIC	X7640631L04	SA000046G00	SA00004L100



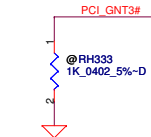
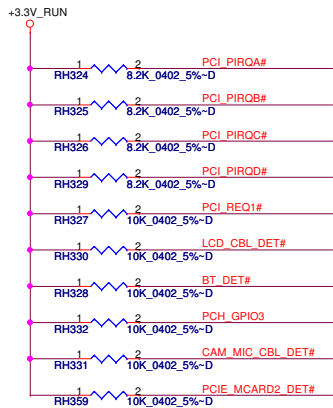
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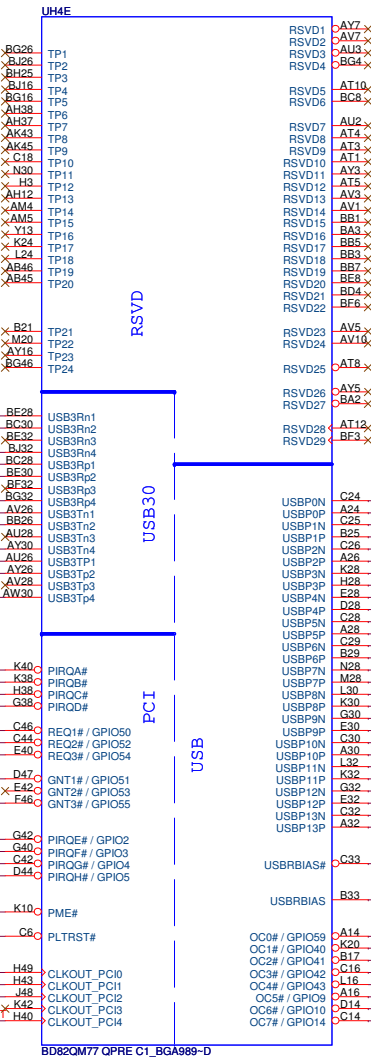
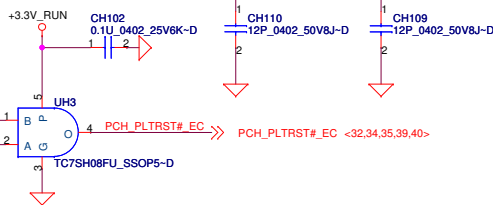
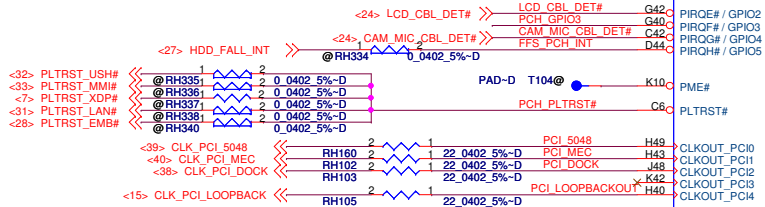
File PCH (1/8)

Size Document Number LA-7781

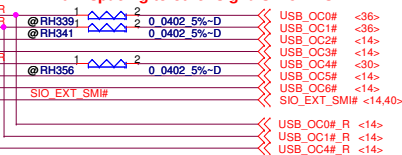
Date: Friday, February 24, 2012 Sheet 14 of 61



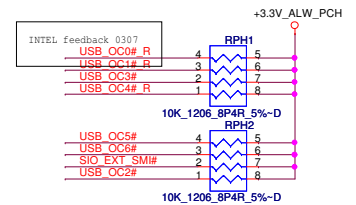
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



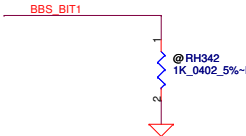
Route single-end 50-ohms and max 500-mils length.
Minimum spacing to other signals: 15 mils



- >Right Side Top
- >Right Side Bottom
- >Right side E-SATA
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >DOCK
- >USH
- >Flash
- >Left side
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch

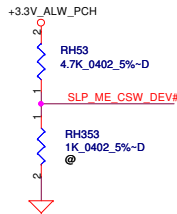


Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

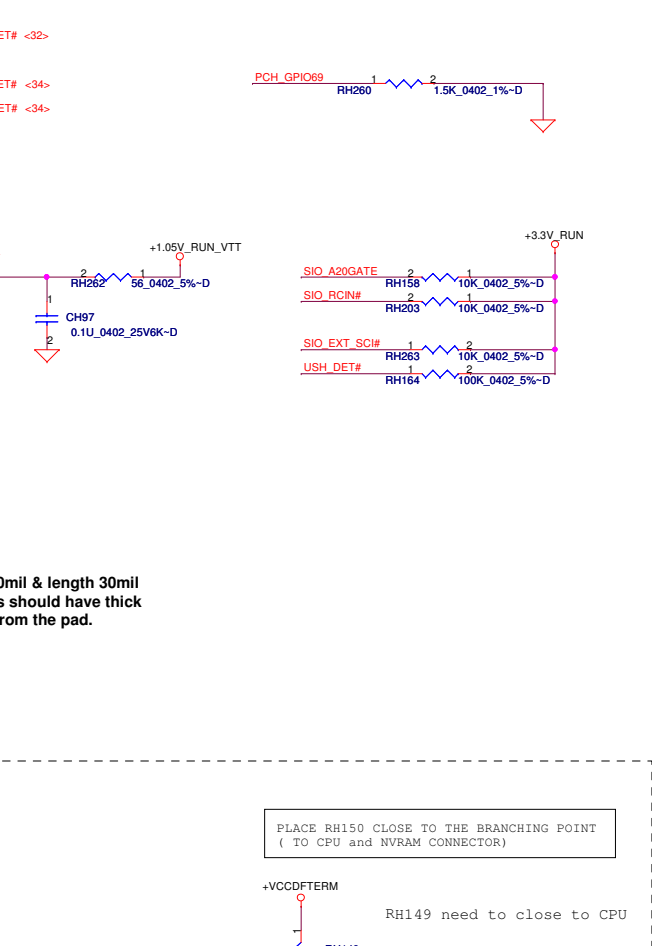
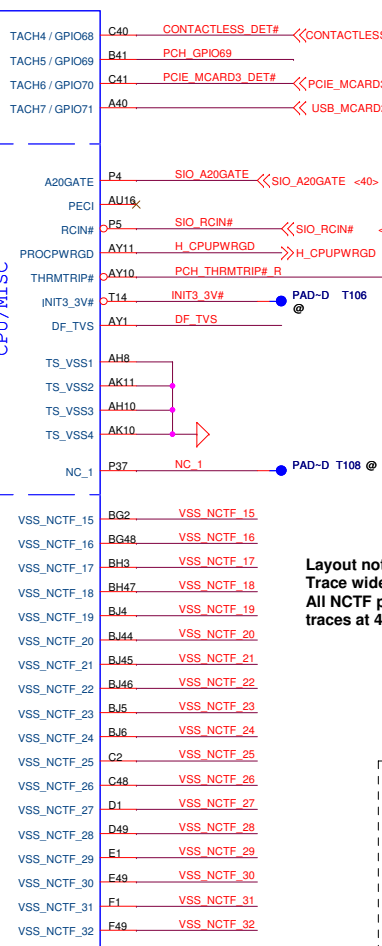
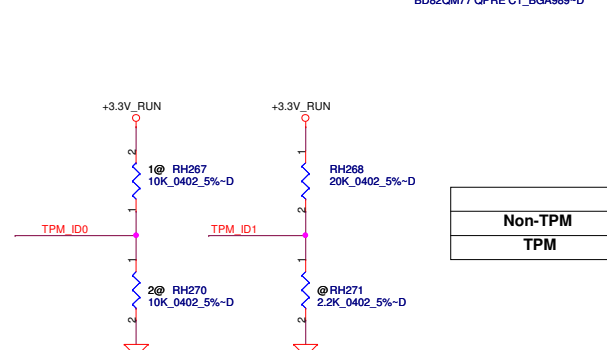
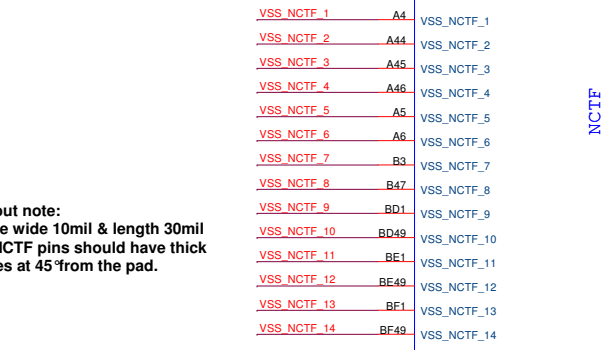
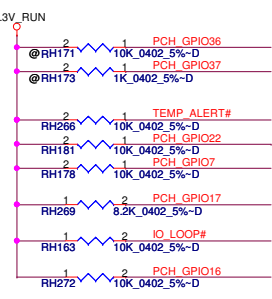
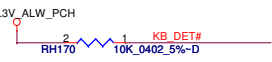
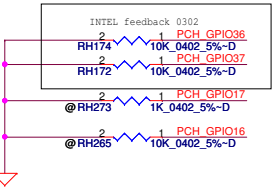
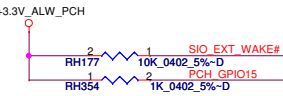
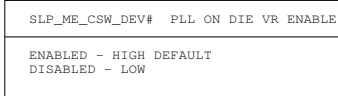


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Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

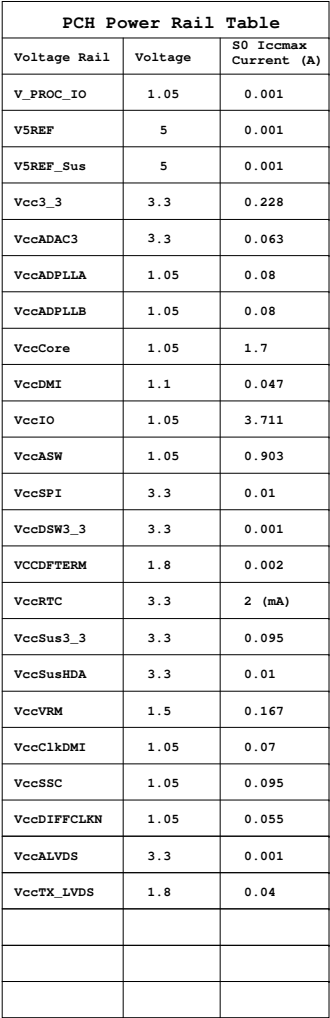
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

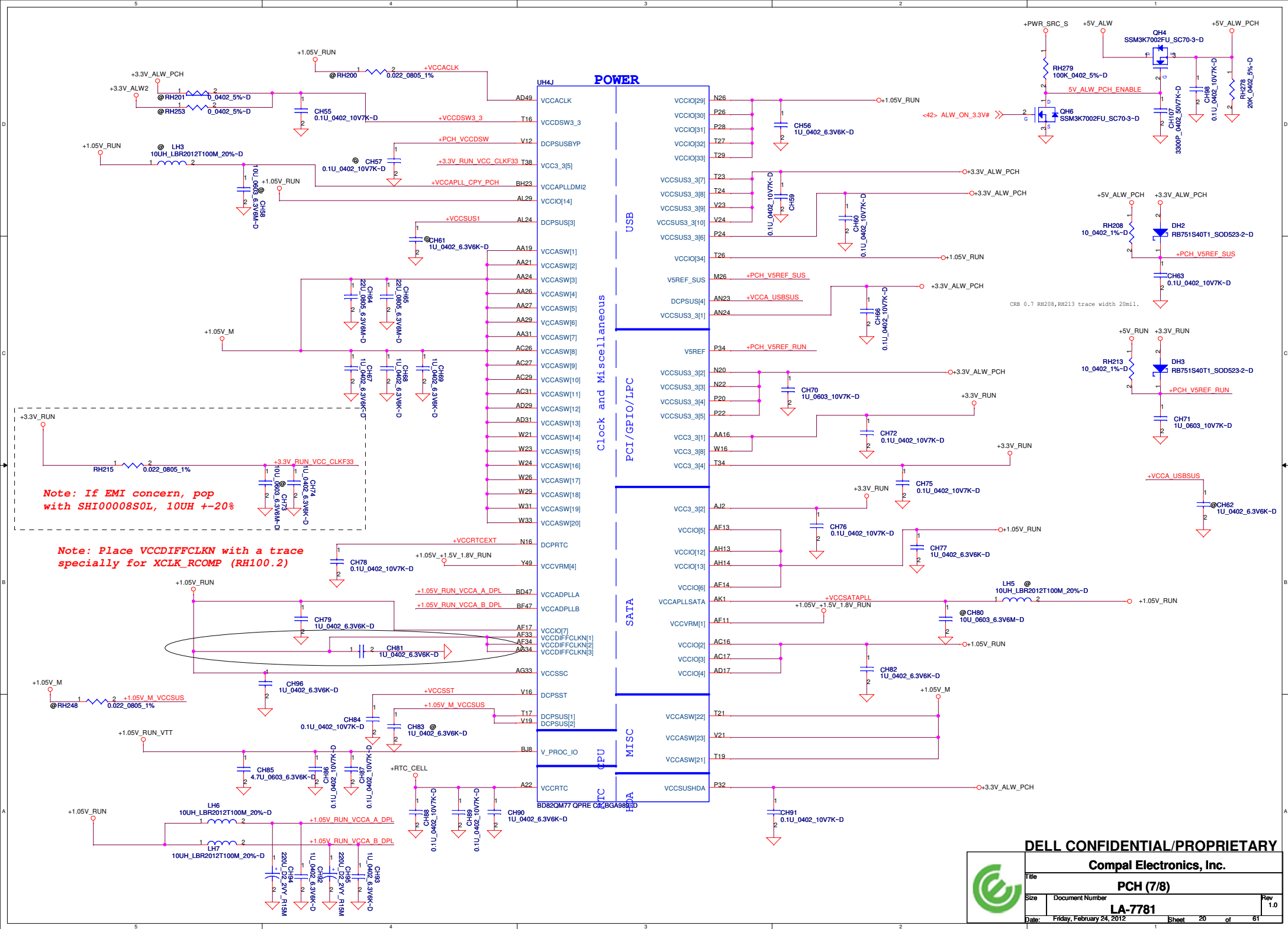
	TPM_ID0	TPM_ID1
Non-TPM	0	1
TPM	1	1

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PCH (5/8)
LA-7781
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UH4H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK46
AA33	VSS[4]	VSS[83] AK8
AA34	VSS[5]	VSS[84] AL16
AB11	VSS[6]	VSS[85] AL17
AB14	VSS[7]	VSS[86] AL19
AB39	VSS[8]	VSS[87] AL2
AB4	VSS[9]	VSS[88] AL21
AB43	VSS[10]	VSS[89] AL23
AB5	VSS[11]	VSS[90] AL26
AB7	VSS[12]	VSS[91] AL27
AC19	VSS[13]	VSS[92] AL31
AC2	VSS[14]	VSS[93] AL33
AC21	VSS[15]	VSS[94] AL34
AC24	VSS[16]	VSS[95] AL48
AC33	VSS[17]	VSS[96] AM11
AC34	VSS[18]	VSS[97] AM14
AC48	VSS[19]	VSS[98] AM39
AD10	VSS[20]	VSS[99] AM43
AD11	VSS[21]	VSS[100] AM45
AD12	VSS[22]	VSS[101] AM46
AD13	VSS[23]	VSS[102] AM7
AD19	VSS[24]	VSS[103] AN2
AD24	VSS[25]	VSS[104] AN29
AD26	VSS[26]	VSS[105] AN3
AD27	VSS[27]	VSS[106] AN31
AD33	VSS[28]	VSS[107] AP12
AD36	VSS[29]	VSS[108] AP19
AD37	VSS[30]	VSS[109] AP28
AD38	VSS[31]	VSS[110] AP29
AD39	VSS[32]	VSS[111] AP32
AD4	VSS[33]	VSS[112] AP38
AD40	VSS[34]	VSS[113] AP4
AD42	VSS[35]	VSS[114] AP42
AD43	VSS[36]	VSS[115] AP46
AD45	VSS[37]	VSS[116] AP8
AD46	VSS[38]	VSS[117] AR2
AD46	VSS[39]	VSS[118] AR48
AD8	VSS[40]	VSS[119] AT11
AE2	VSS[41]	VSS[120] AT13
AE3	VSS[42]	VSS[121] AT22
AF10	VSS[43]	VSS[122] AT26
AF12	VSS[44]	VSS[123] AT28
AD14	VSS[45]	VSS[124] AT30
AD16	VSS[46]	VSS[125] AT32
AF16	VSS[47]	VSS[126] AT34
AF19	VSS[48]	VSS[127] AT39
AF24	VSS[49]	VSS[128] AT42
AF26	VSS[50]	VSS[129] AT46
AF27	VSS[51]	VSS[130] AU24
AF29	VSS[52]	VSS[131] AU30
AF31	VSS[53]	VSS[132] AV16
AF38	VSS[54]	VSS[133] AV20
AF4	VSS[55]	VSS[134] AV24
AF42	VSS[56]	VSS[135] AV30
AF5	VSS[57]	VSS[136] AV38
AF7	VSS[58]	VSS[137] AV43
AF8	VSS[59]	VSS[138] AV8
AG19	VSS[60]	VSS[139] AW14
AG2	VSS[61]	VSS[140] AW2
AG32	VSS[62]	VSS[141] AW22
AG31	VSS[63]	VSS[142] AW26
AG48	VSS[64]	VSS[143] AW28
AH11	VSS[65]	VSS[144] AW32
AH3	VSS[66]	VSS[145] AW36
AH36	VSS[67]	VSS[146] AW40
AH39	VSS[68]	VSS[147] AW48
AH40	VSS[69]	VSS[148] AW11
AH42	VSS[70]	VSS[149] AW12
AH46	VSS[71]	VSS[150] AW14
AH7	VSS[72]	VSS[151] AW22
AJ19	VSS[73]	VSS[152] AW36
AJ21	VSS[74]	VSS[153] AW40
AJ24	VSS[75]	VSS[154] AW48
AJ33	VSS[76]	VSS[155] AY11
AJ34	VSS[77]	VSS[156] AY22
AK12	VSS[78]	VSS[157] AY28
AK3	VSS[79]	VSS[158]

BD82QM77 QPRE C1_BGA989-D

UH4I		
F3	VSS[159]	VSS[259] H46
AY4	VSS[160]	VSS[260] K18
AY42	VSS[161]	VSS[261] K26
AY46	VSS[162]	VSS[262] K39
AY8	VSS[163]	VSS[263] K46
B11	VSS[164]	VSS[264] K7
B15	VSS[165]	VSS[265] L18
B19	VSS[166]	VSS[266] L2
B23	VSS[167]	VSS[267] L20
B27	VSS[168]	VSS[268] L26
B31	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
B12	VSS[173]	VSS[273] M18
BB16	VSS[174]	VSS[274] M22
BB20	VSS[175]	VSS[275] M24
BB22	VSS[176]	VSS[276] M30
BB24	VSS[177]	VSS[277] M32
BB28	VSS[178]	VSS[278] M34
BB30	VSS[179]	VSS[279] M38
BB38	VSS[180]	VSS[280] M4
BB4	VSS[181]	VSS[281] M42
BB46	VSS[182]	VSS[282] M46
BC14	VSS[183]	VSS[283] M8
BC18	VSS[184]	VSS[284] N18
BC2	VSS[185]	VSS[285] N30
BC22	VSS[186]	VSS[286] N47
BC26	VSS[187]	VSS[287] P11
BC32	VSS[188]	VSS[288] P18
BC34	VSS[189]	VSS[289] P33
BC46	VSS[190]	VSS[290] P40
BC40	VSS[191]	VSS[291] P43
BC42	VSS[192]	VSS[292] P7
BC48	VSS[193]	VSS[293] R2
BD46	VSS[194]	VSS[294] R48
BD5	VSS[195]	VSS[295] T12
BE22	VSS[196]	VSS[296] T31
BE26	VSS[197]	VSS[297] T4
BE40	VSS[198]	VSS[298] T4
BE10	VSS[199]	VSS[299] T734
BF12	VSS[200]	VSS[300] T46
BF16	VSS[201]	VSS[301] T8
BF20	VSS[202]	VSS[302] V11
BF22	VSS[203]	VSS[303] V17
BF24	VSS[204]	VSS[304] V26
BF26	VSS[205]	VSS[305] V27
BF28	VSS[206]	VSS[306] V29
BF30	VSS[207]	VSS[307] V31
BF38	VSS[208]	VSS[308] V36
BF40	VSS[209]	VSS[309] V38
BF8	VSS[210]	VSS[310] V7
BG17	VSS[211]	VSS[311] W17
BG21	VSS[212]	VSS[312] W19
BG24	VSS[213]	VSS[313] W2
BG33	VSS[214]	VSS[314] W27
BG44	VSS[215]	VSS[315] W48
BH11	VSS[216]	VSS[316] Y12
BH15	VSS[217]	VSS[317] Y38
BH17	VSS[218]	VSS[318] Y4
BH19	VSS[219]	VSS[319] Y42
H10	VSS[220]	VSS[320] Y46
BH27	VSS[221]	VSS[321] Y8
BH31	VSS[222]	VSS[322] Y8
BH33	VSS[223]	VSS[323] Y8
BH35	VSS[224]	VSS[324] Y8
BH39	VSS[225]	VSS[325] BG29
BH43	VSS[226]	VSS[326] N24
BH7	VSS[227]	VSS[327] N24
DA4	VSS[228]	VSS[328] AD47
D1	VSS[229]	VSS[329] B43
D12	VSS[230]	VSS[330] BE10
D16	VSS[231]	VSS[331] BG41
D18	VSS[232]	VSS[332] G14
D22	VSS[233]	VSS[333] H16
D24	VSS[234]	VSS[334] I36
D26	VSS[235]	VSS[335] BG22
D30	VSS[236]	VSS[336] BG24
D32	VSS[237]	VSS[337] C22
D34	VSS[238]	VSS[338] AP13
D38	VSS[239]	VSS[339] M14
D42	VSS[240]	VSS[340] AP3
D8	VSS[241]	VSS[341] AP1
E18	VSS[242]	VSS[342] BE16
E26	VSS[243]	VSS[343] BC16
G18	VSS[244]	VSS[344] BG28
G20	VSS[245]	VSS[345] B128
G26	VSS[246]	VSS[346]
G28	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G48	VSS[249]	VSS[349]
H12	VSS[250]	VSS[350]
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

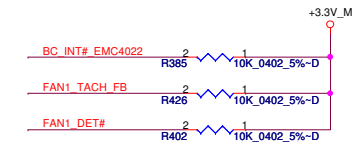
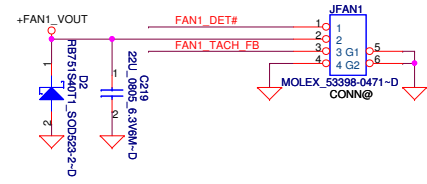
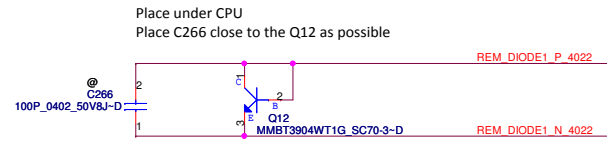
BD82QM77 QPRE C1_BGA989-D

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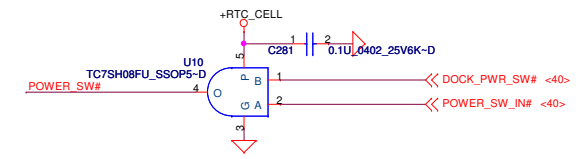
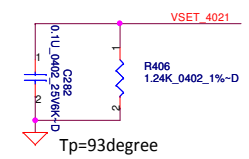
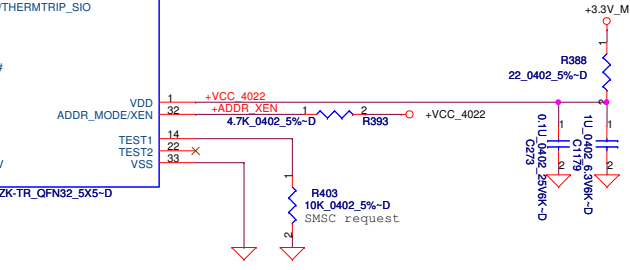
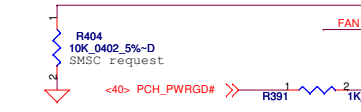
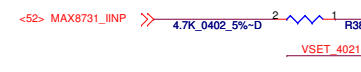
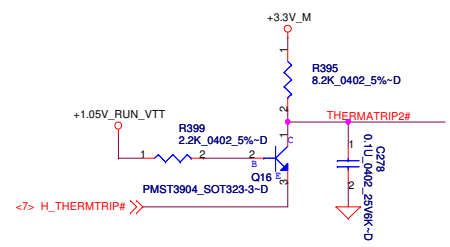
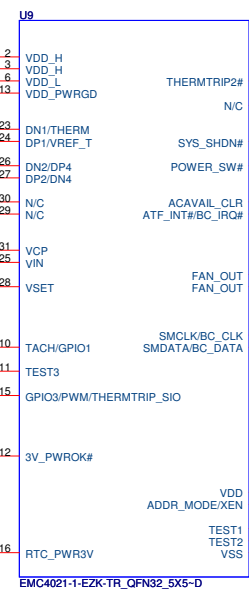
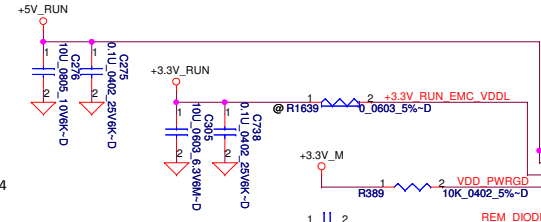
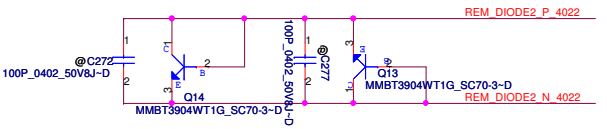


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Title			
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(1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.

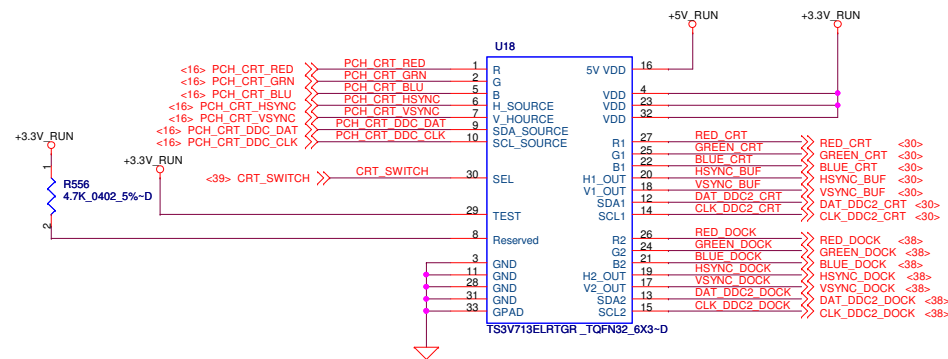


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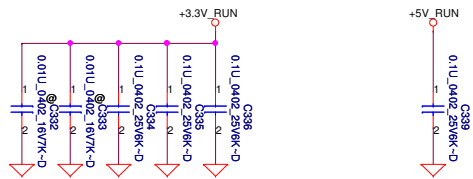
Compal Electronics, Inc.			
FAN & Thermal Sensor			
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SW for MB/DOCK

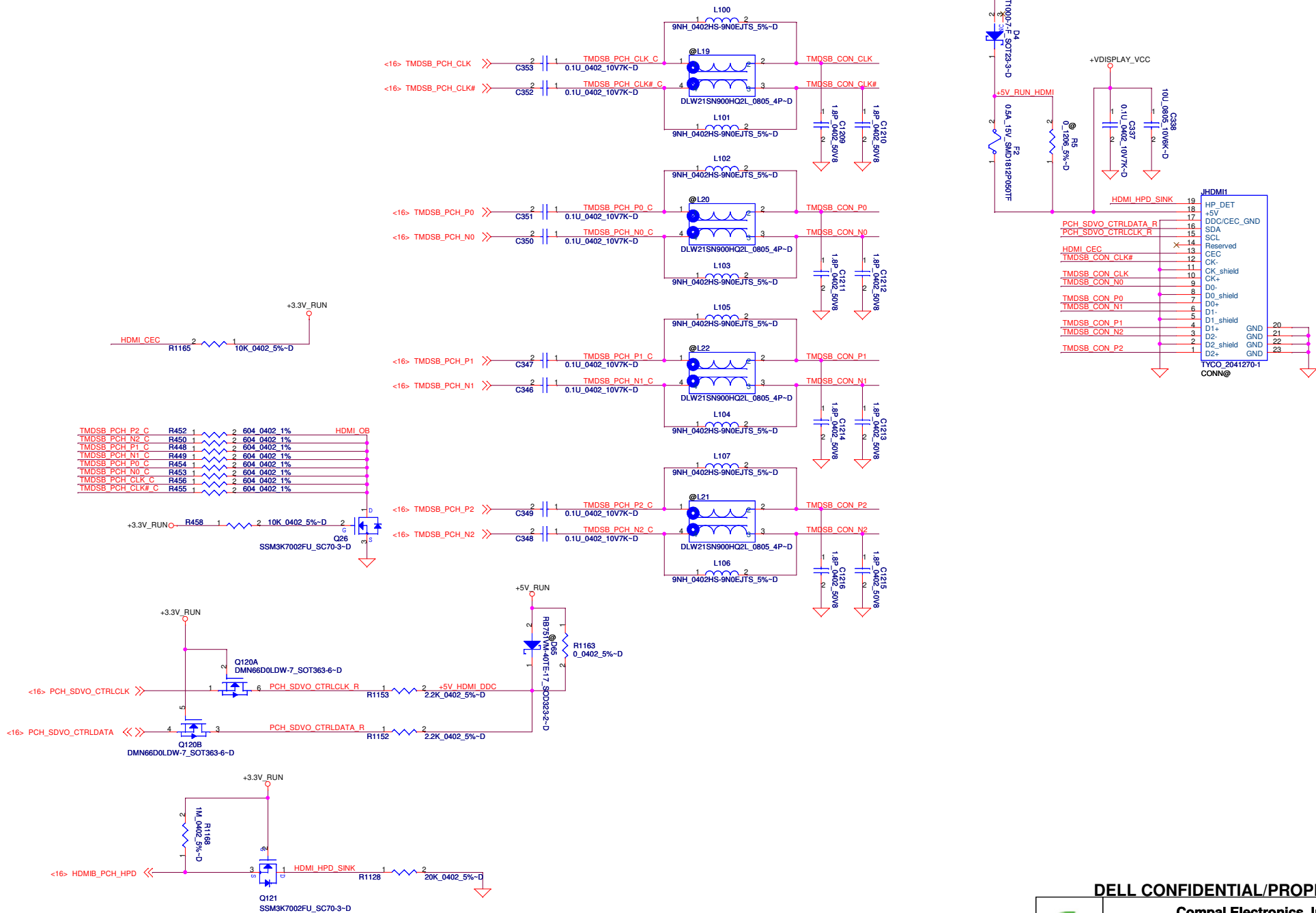


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



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	Compal Electronics, Inc.		
	Title		
	CRT/Video switch		
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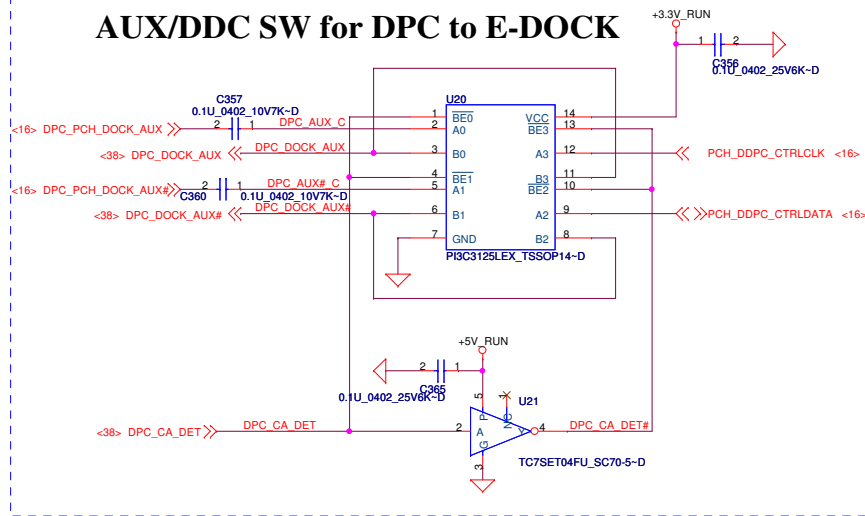


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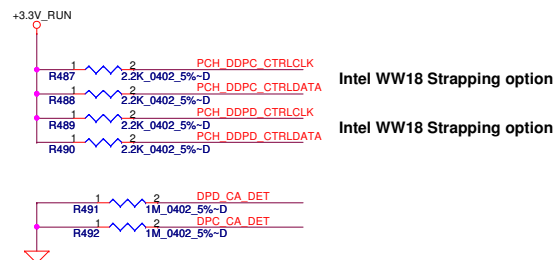
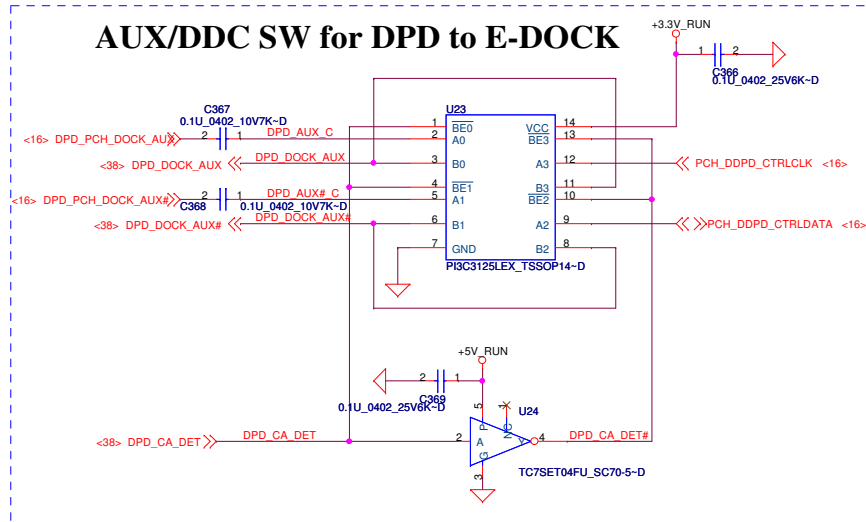
Title		
HDMI port		
Size	Document Number	Rev
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AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample available on May.

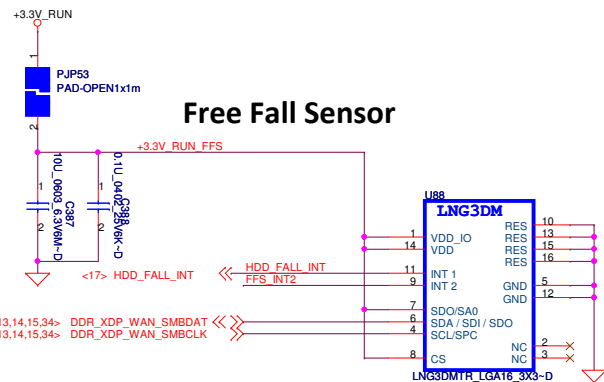
AUX/DDC SW for DPD to E-DOCK



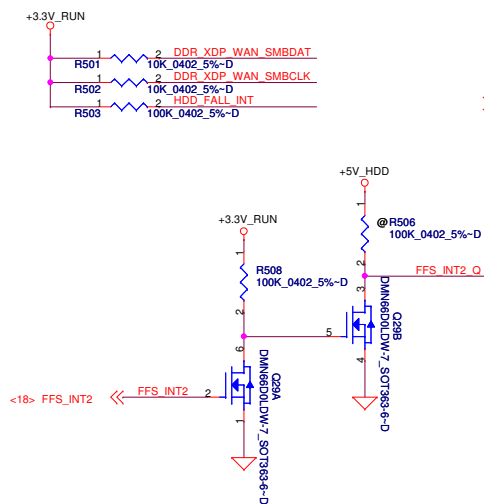
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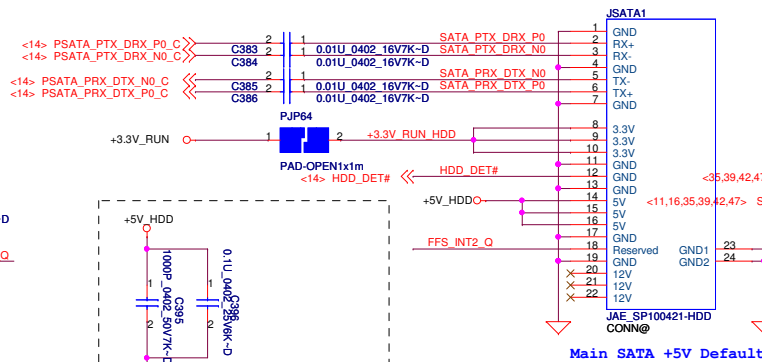
		Compal Electronics, Inc.	
		DP AUX SW	
Size	Document Number	Rev	
		1.0	
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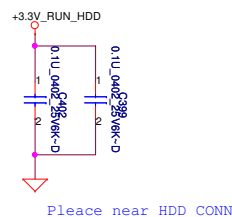
Free Fall Sensor



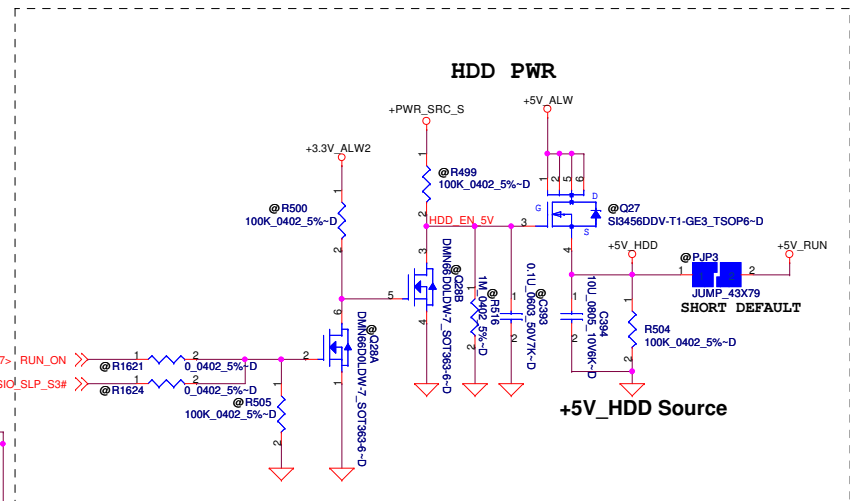
For HDD Temp.



Pleace near HDD CONN



Pleace near HDD CONN



HDD PWR

+5V_HDD Source

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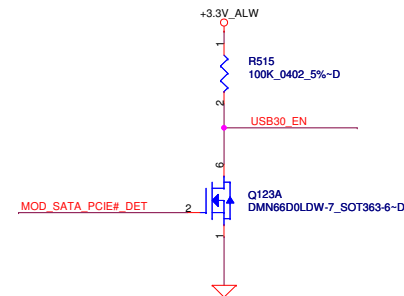
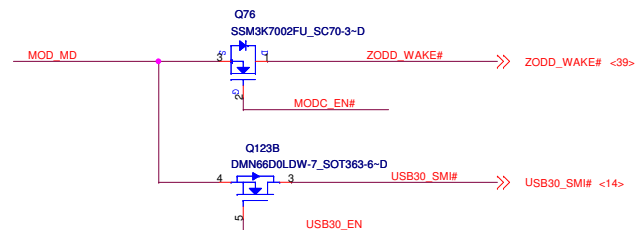
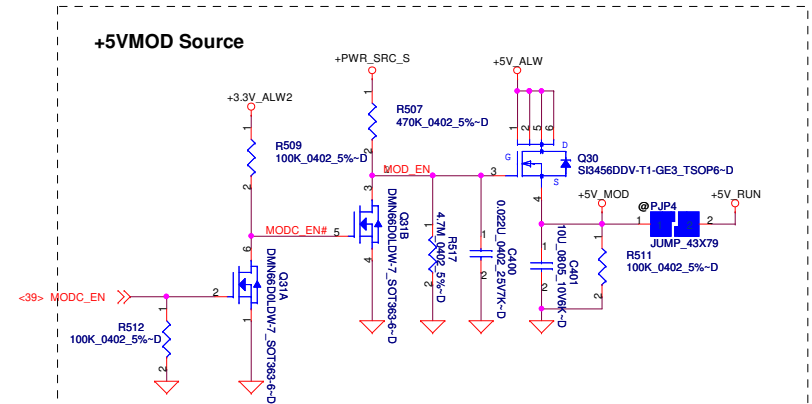
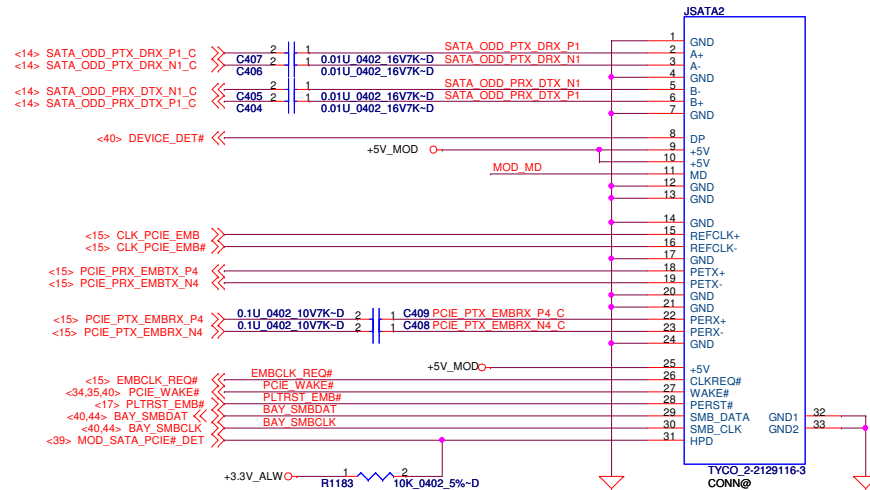
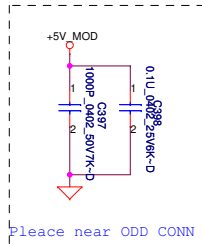
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HDD CONNECTOR			
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For ODD



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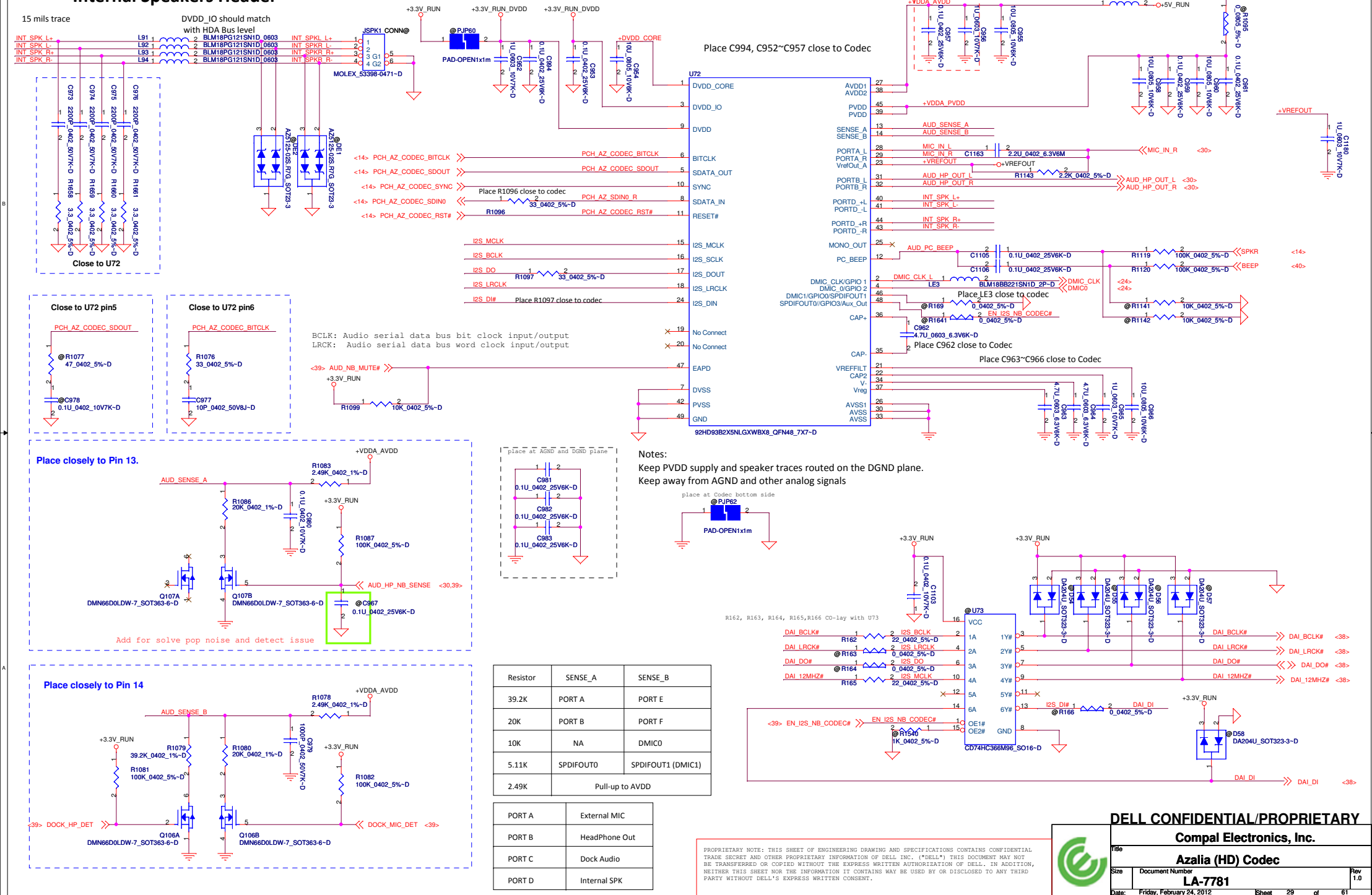


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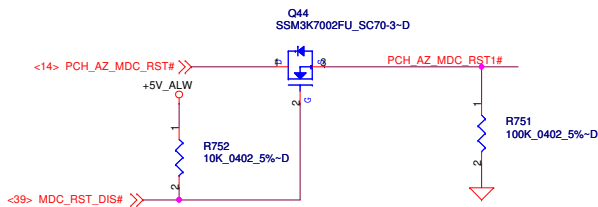
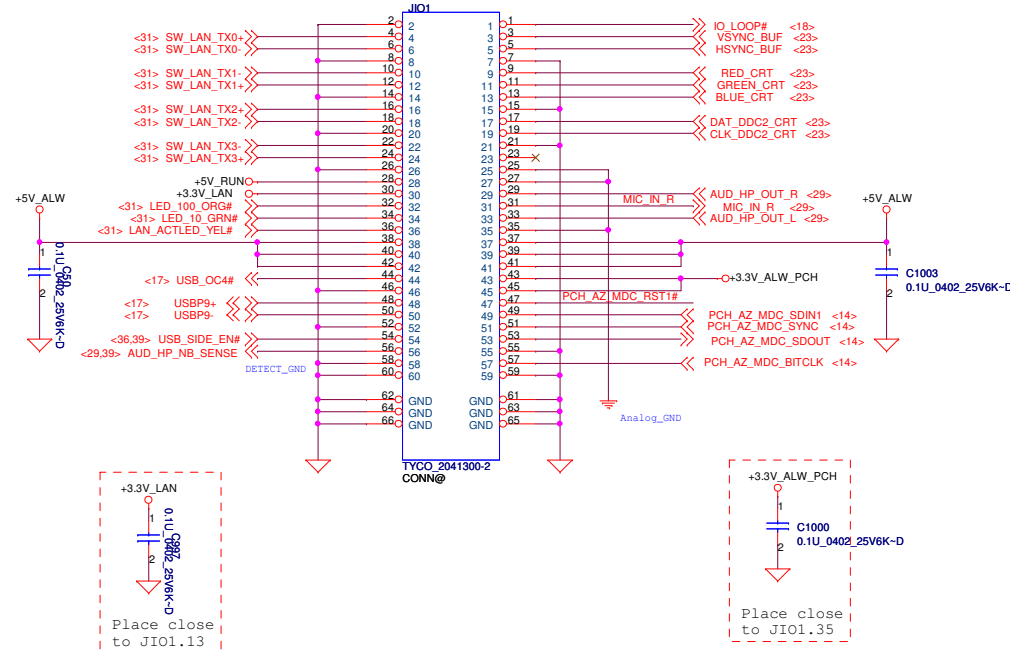
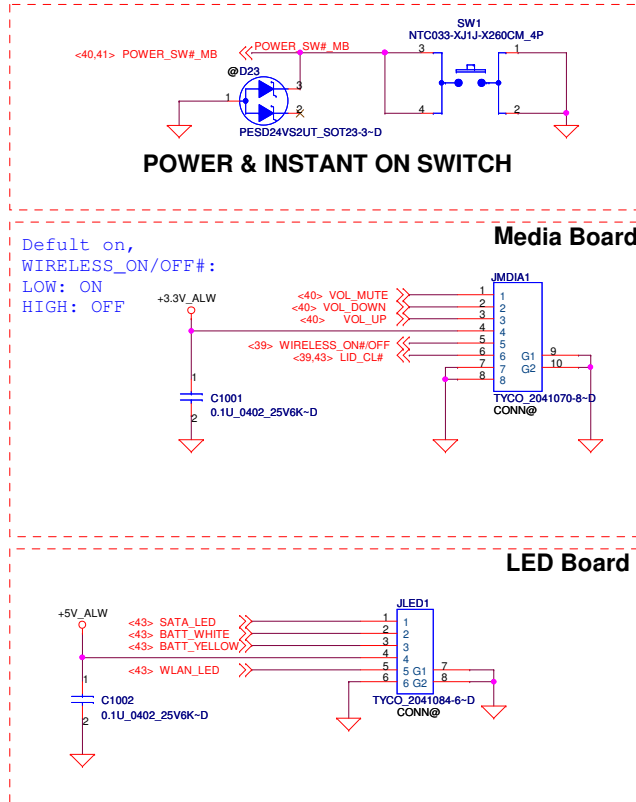
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ODD CONNECTOR			
Size	Document Number	Rev	
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Internal Speakers Header



I/O board CONN.

Change to TYCO_2041300-2_60P-T and Horizontal reverse to SSI



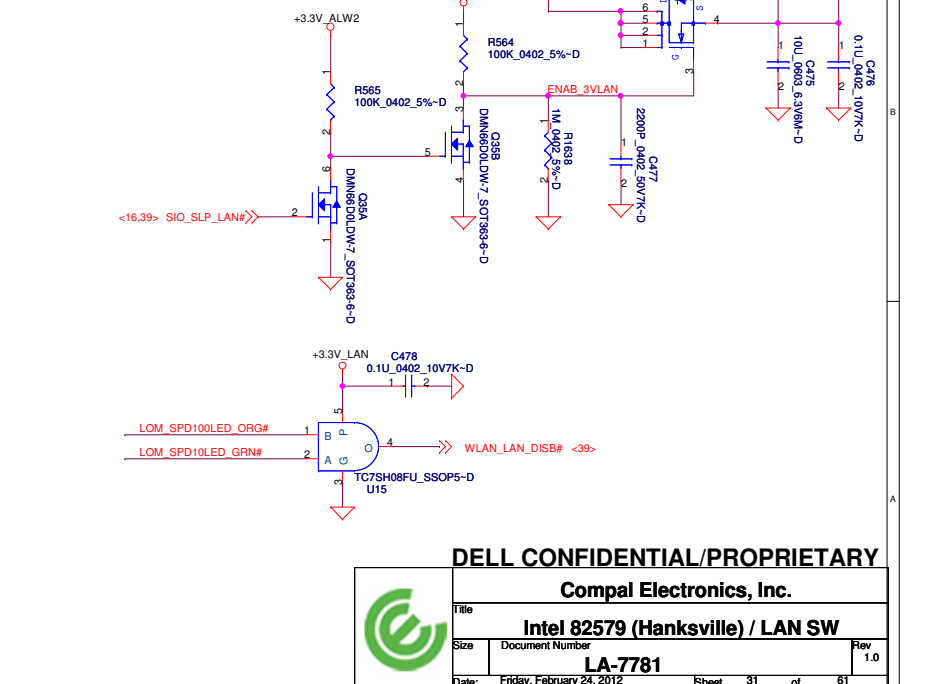
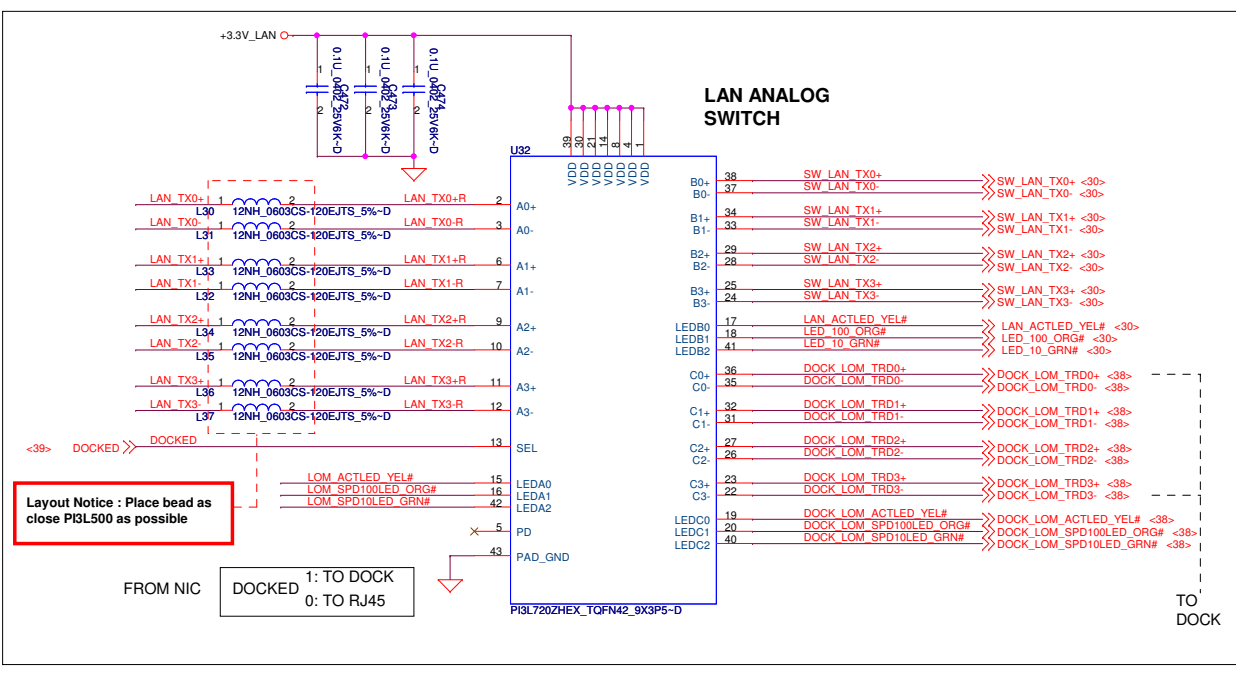
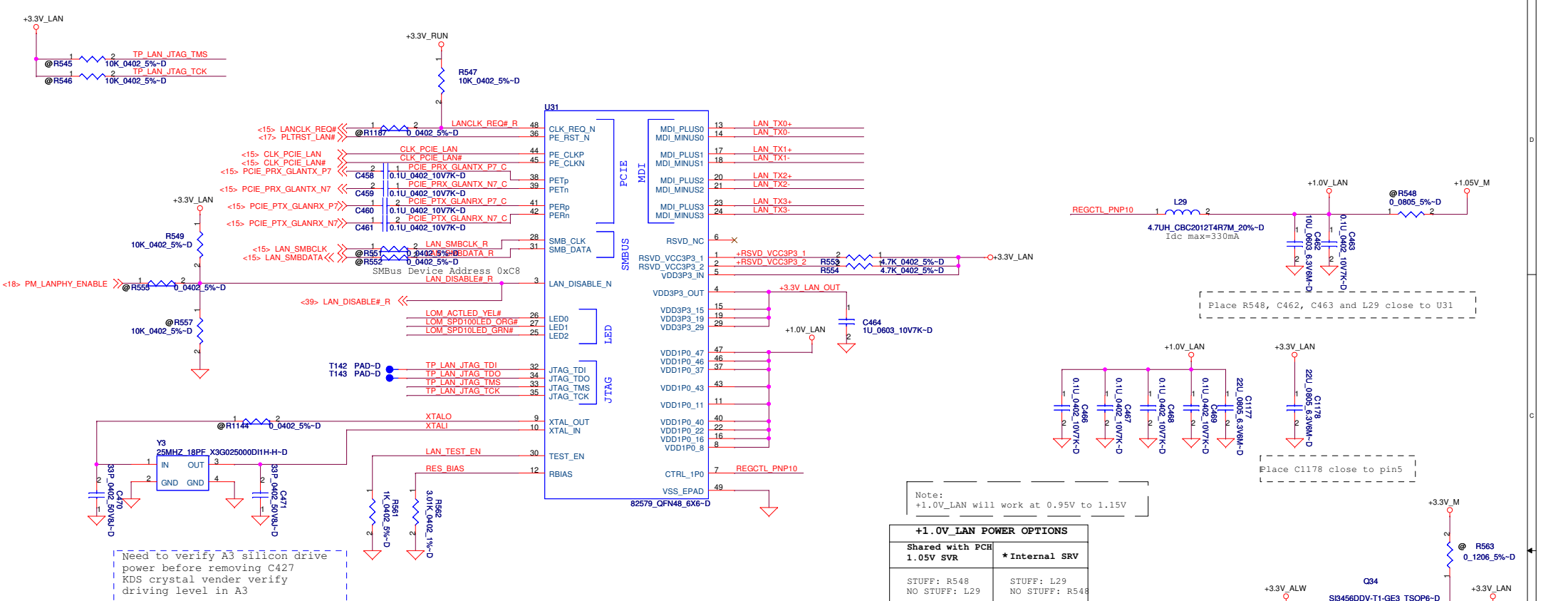
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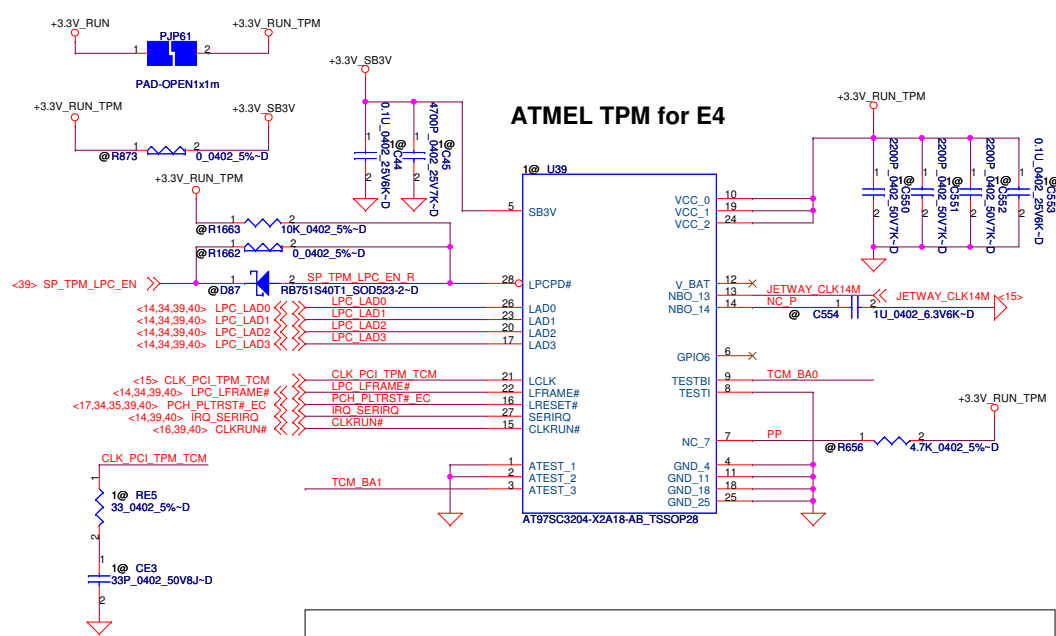
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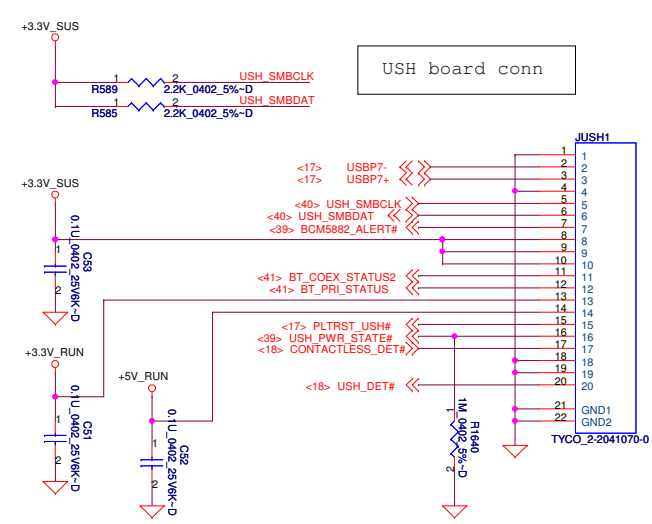
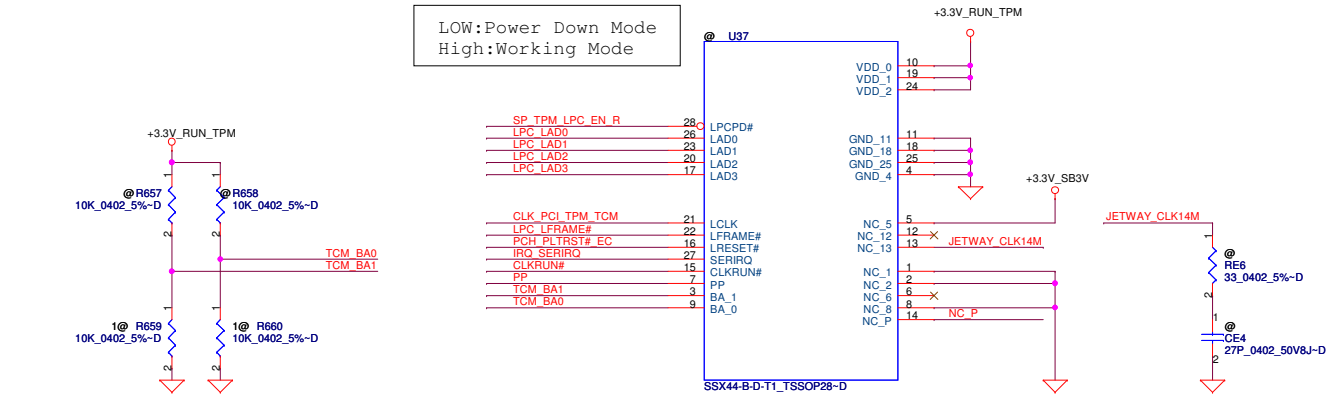
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PWR SW/Sub-board Connector		
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Co-lay U37 and U38
LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay



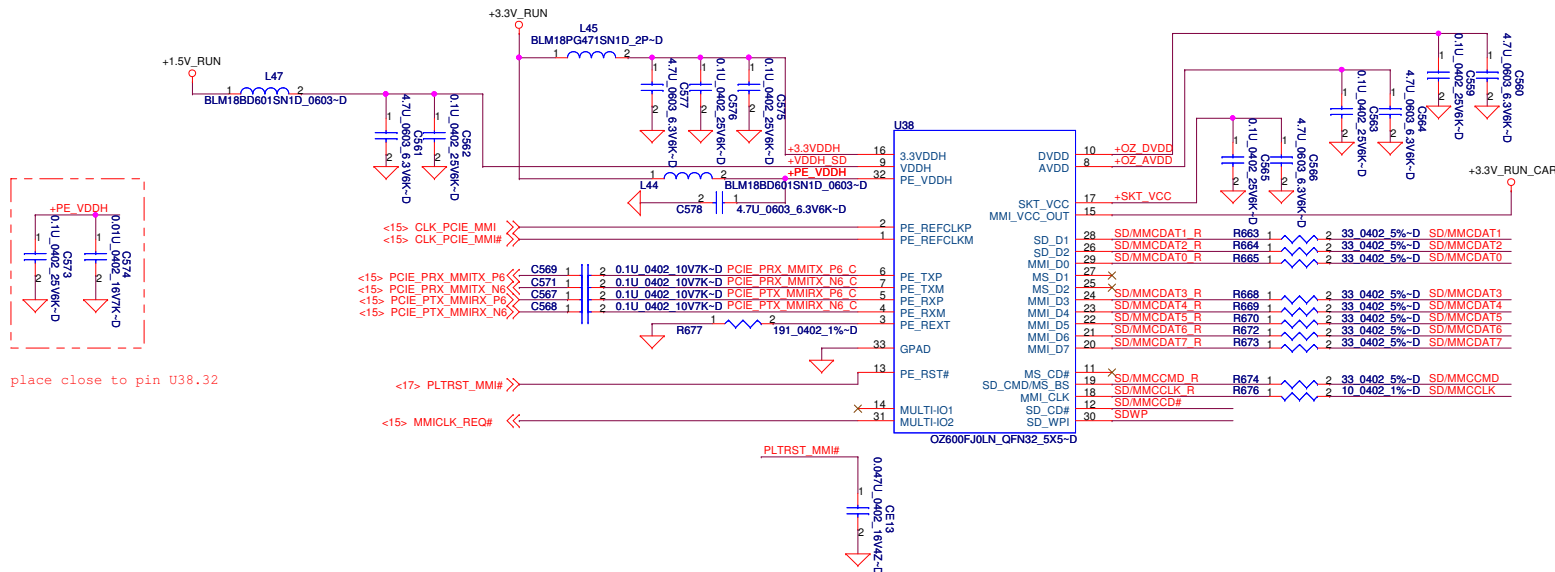
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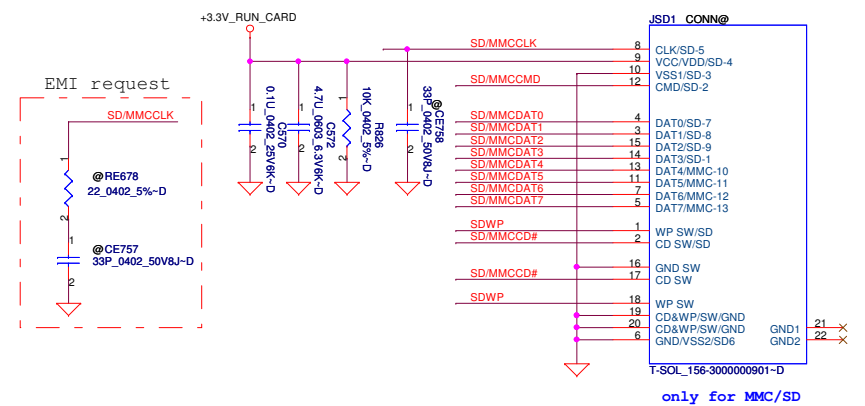


Title		
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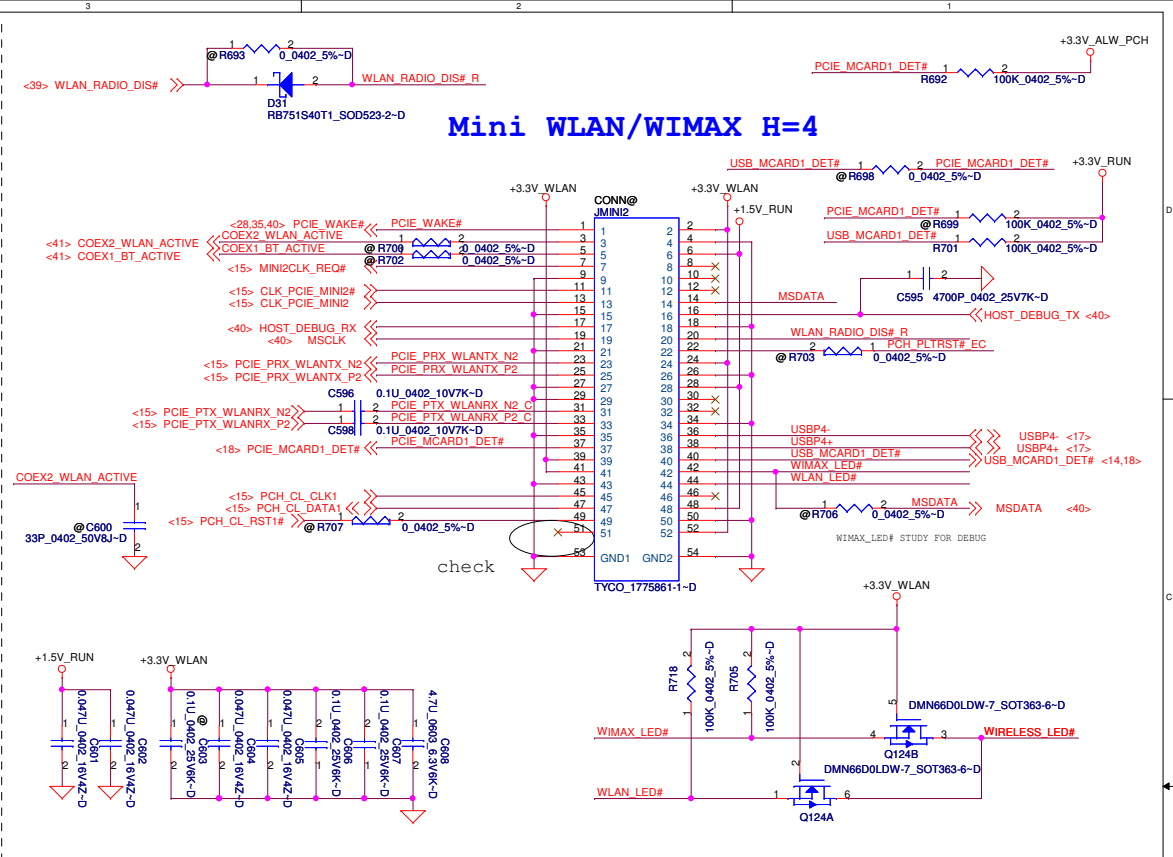
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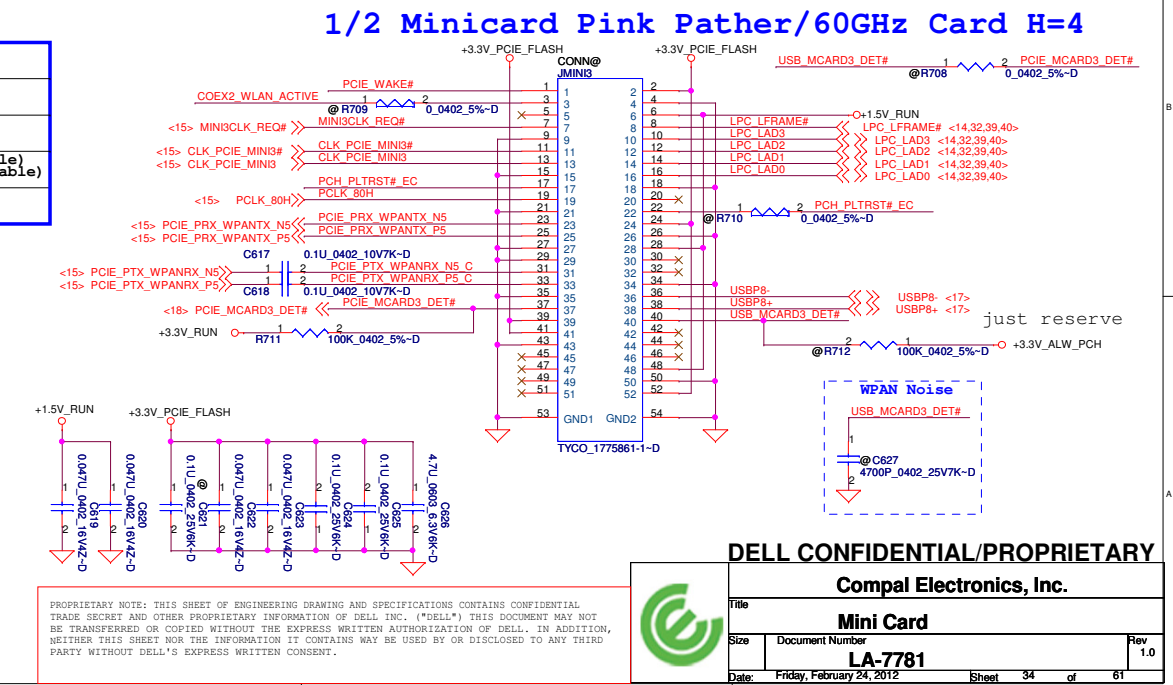
Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



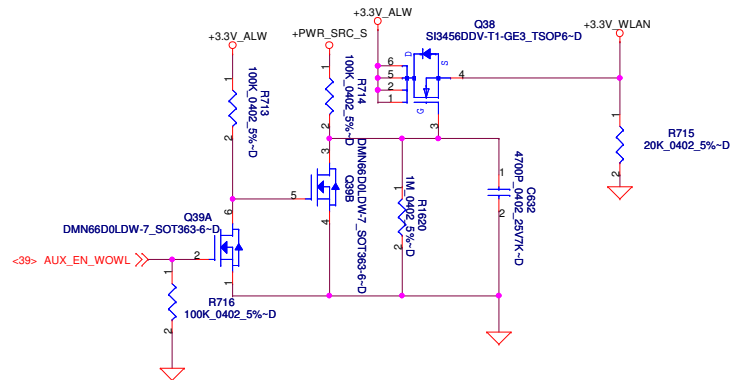
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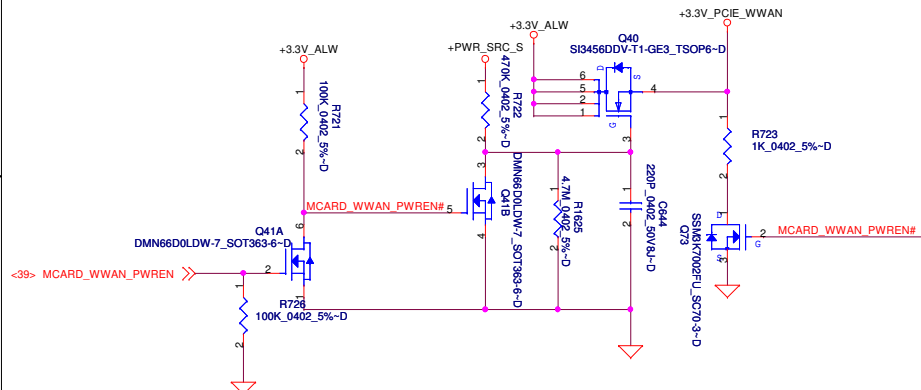
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA



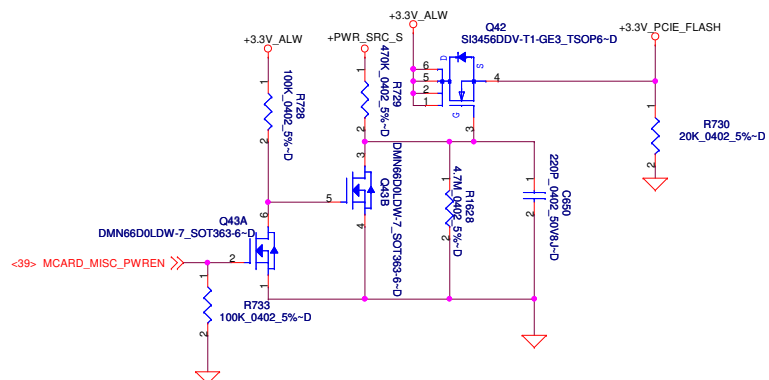
Power Control for Mini card2



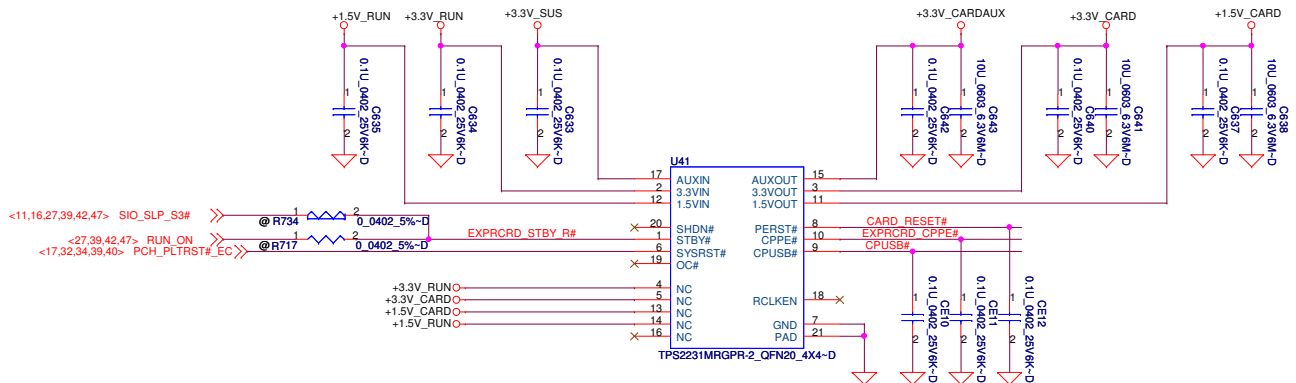
Power Control for Mini card1



Power Control for Mini card3

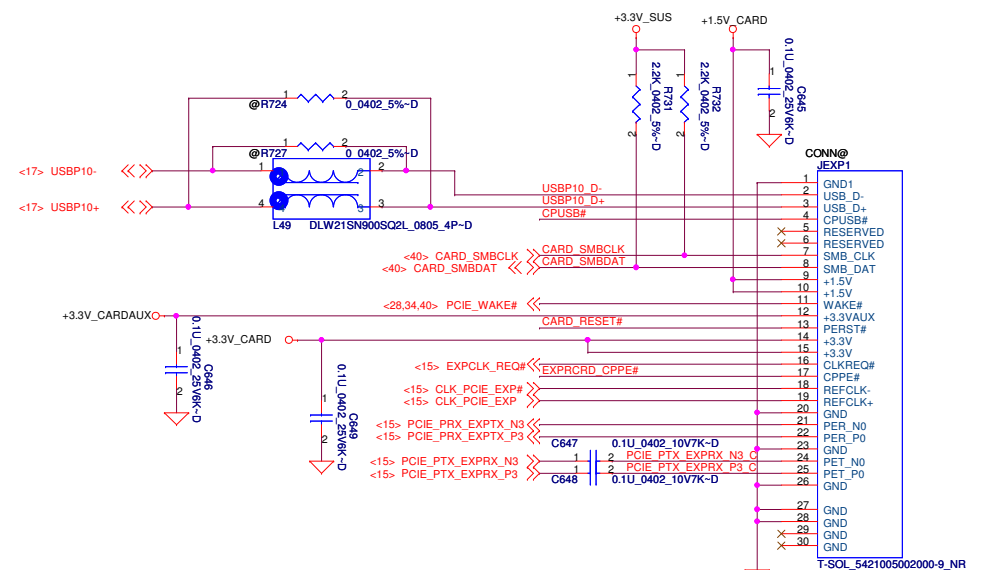


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin13 and pin14 to support GMT 2nd source part

Express Card Conn.



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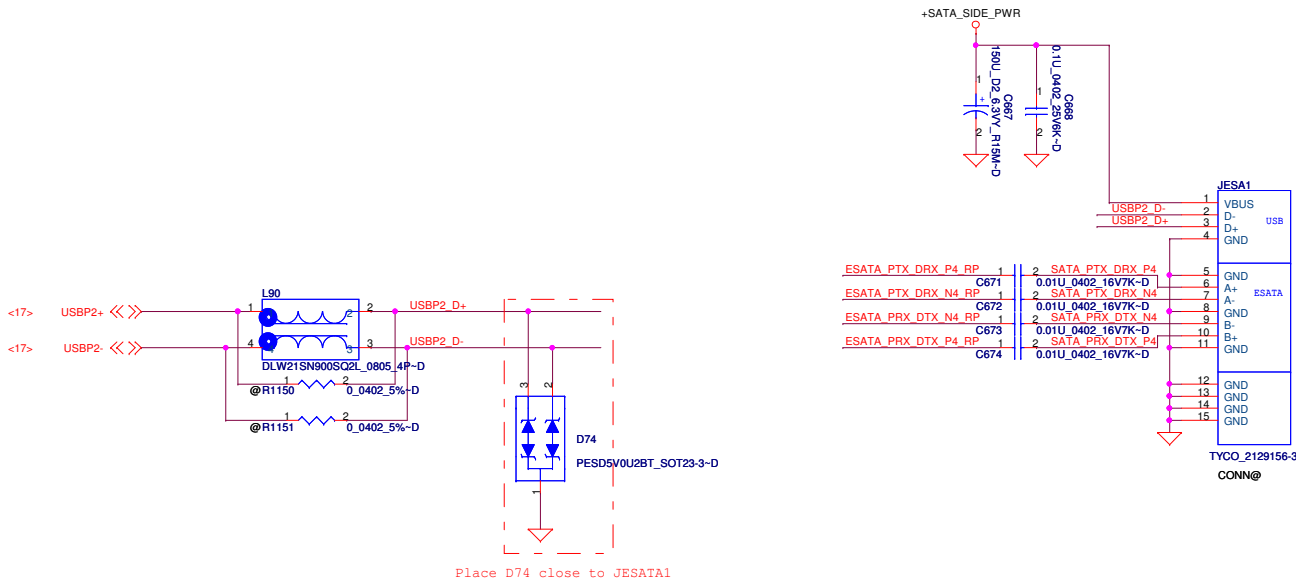
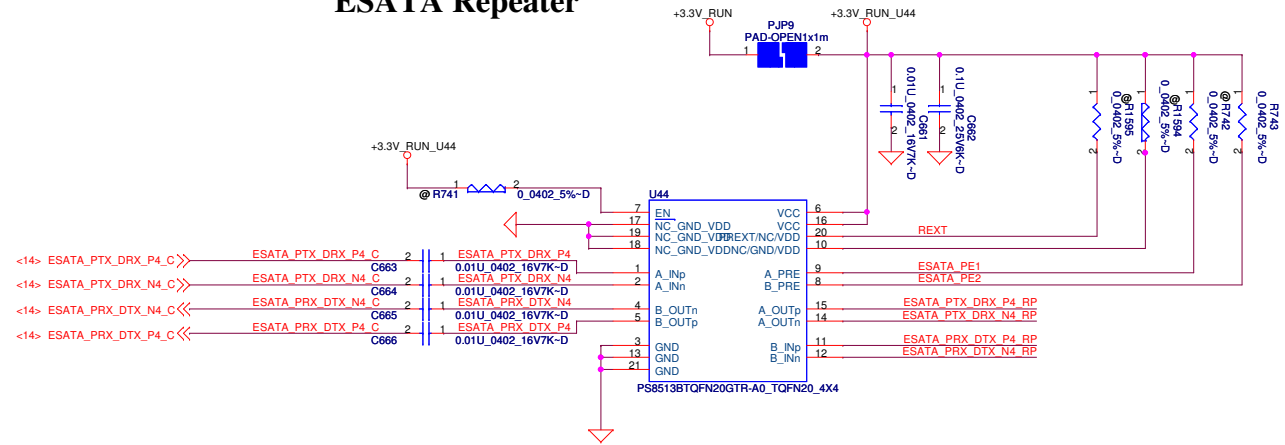
PCIE-SATA SW / PCIE PWR

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ESATA Repeater



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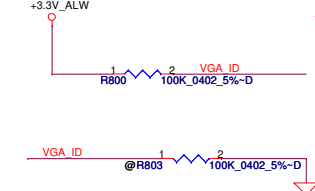
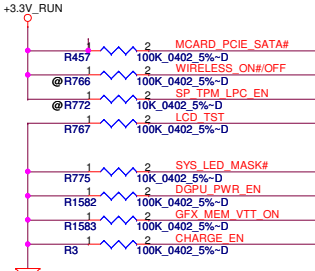
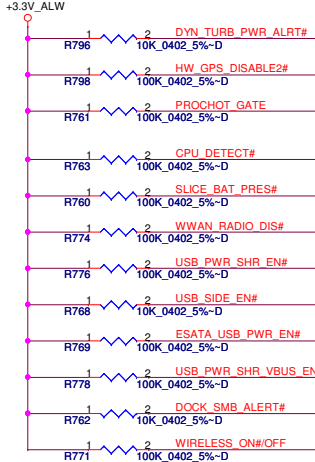
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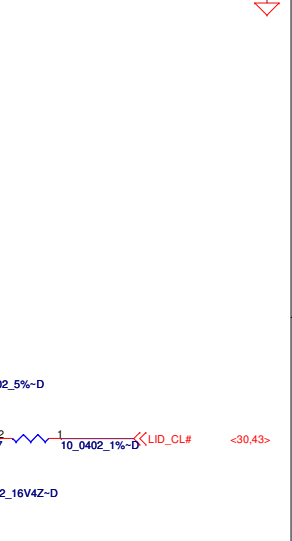
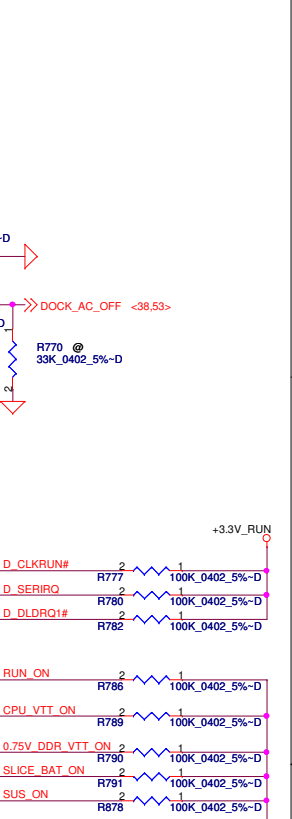
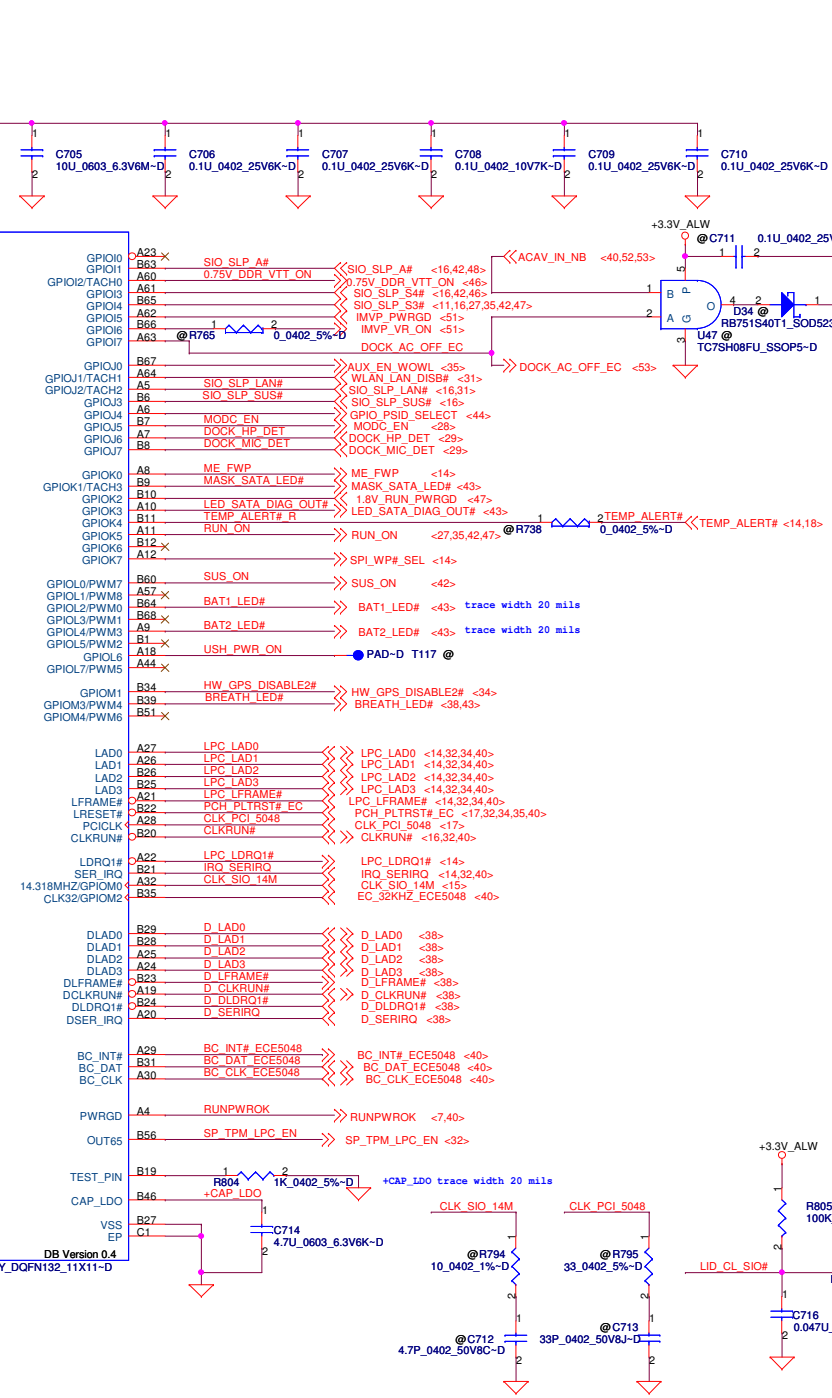
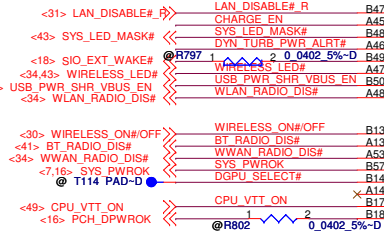
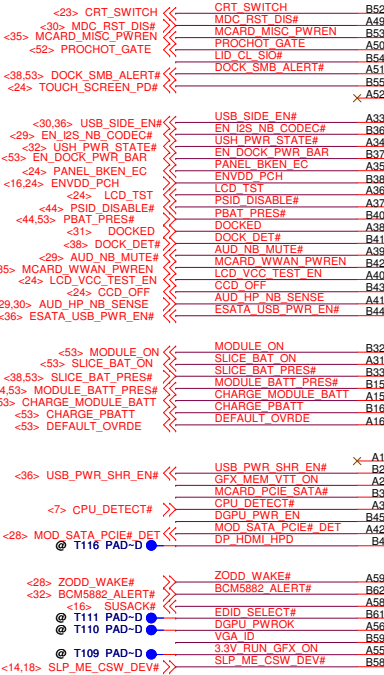
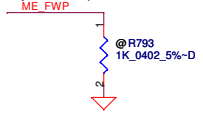
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1.0



	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)

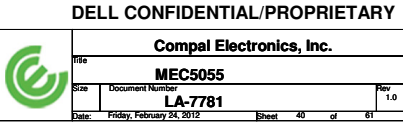


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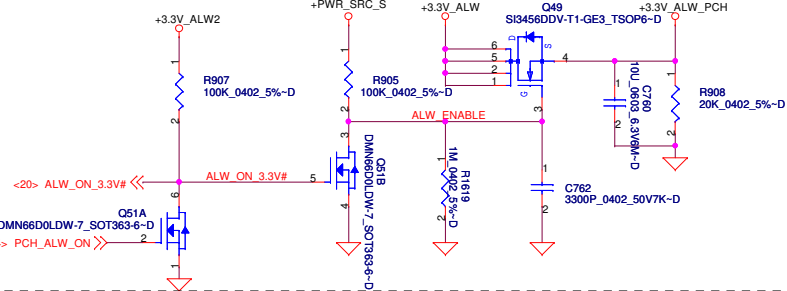


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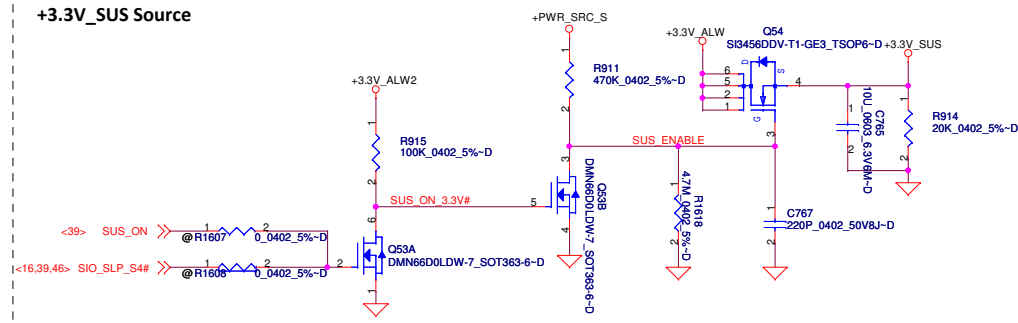
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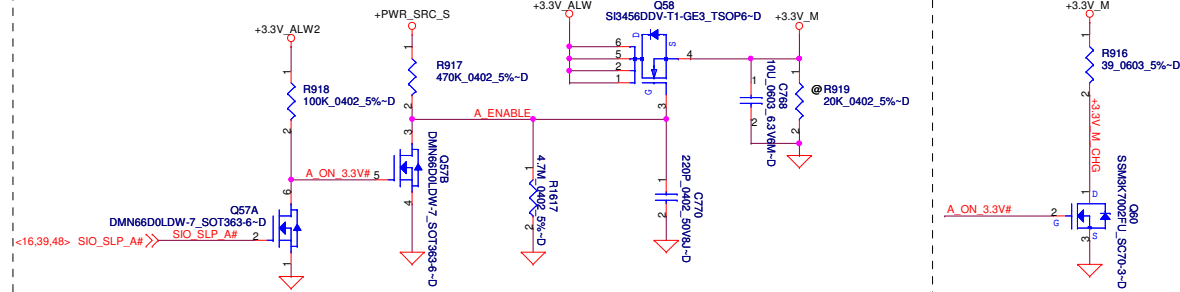
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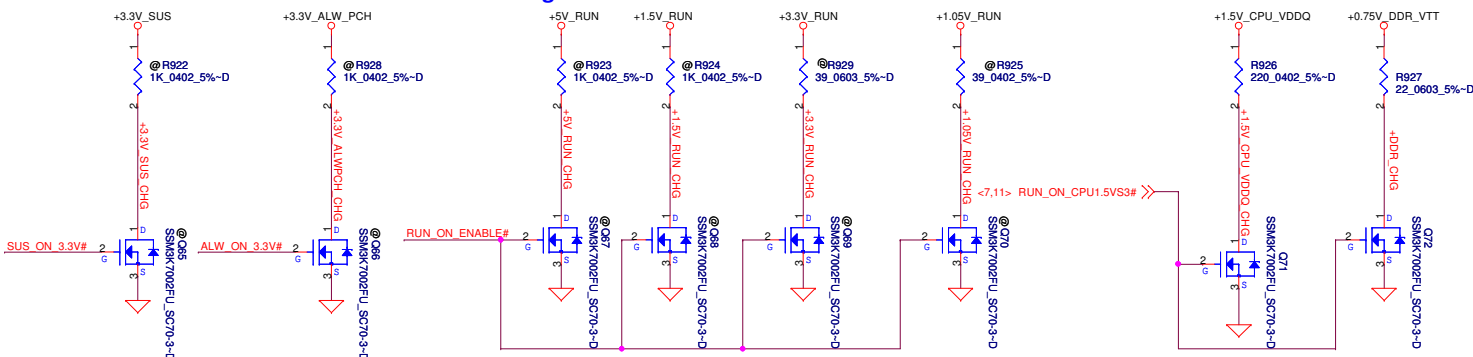
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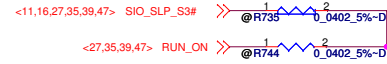
+3.3V_M Source



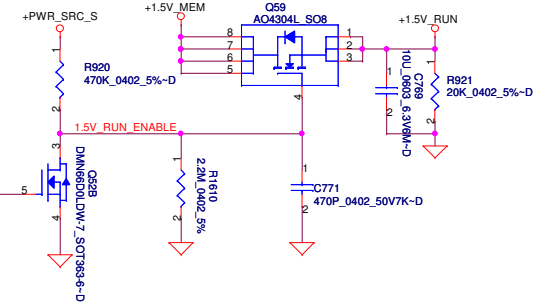
Discharg Circuit



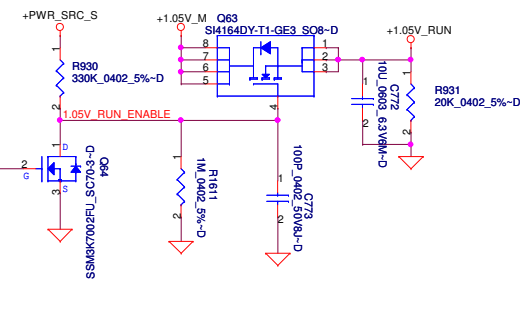
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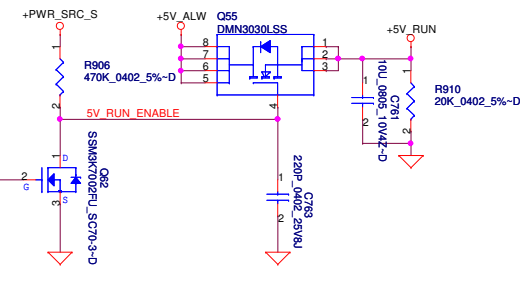
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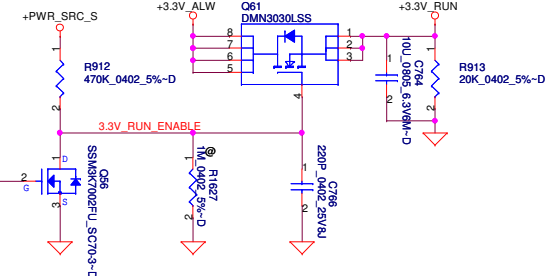
+1.05V_RUN Source



+5V_RUN Source



+3.3V_RUN Source



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POWER CONTROL

LA-7781



Size

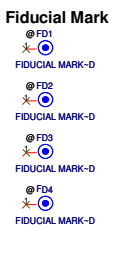
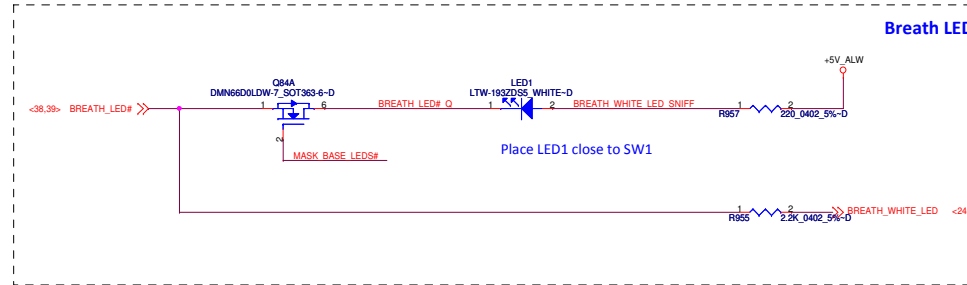
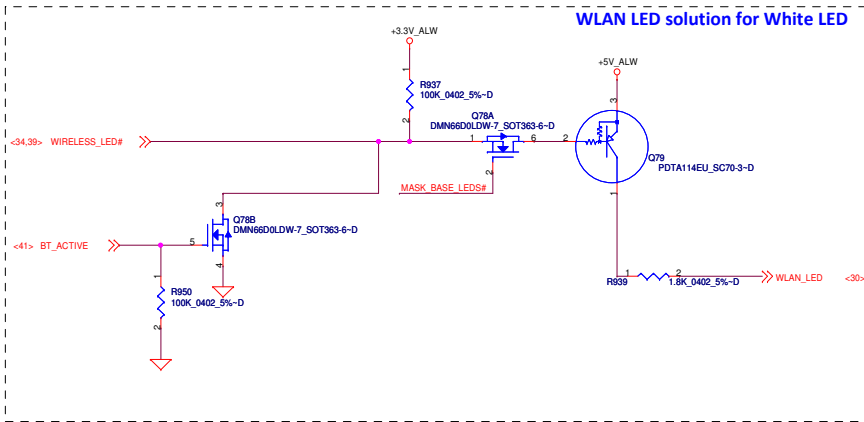
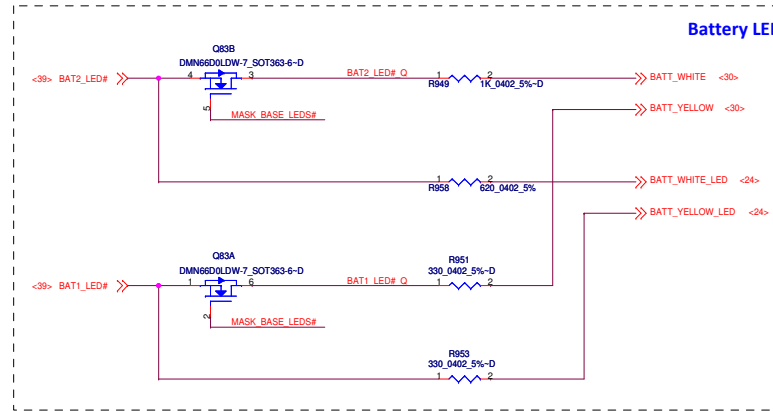
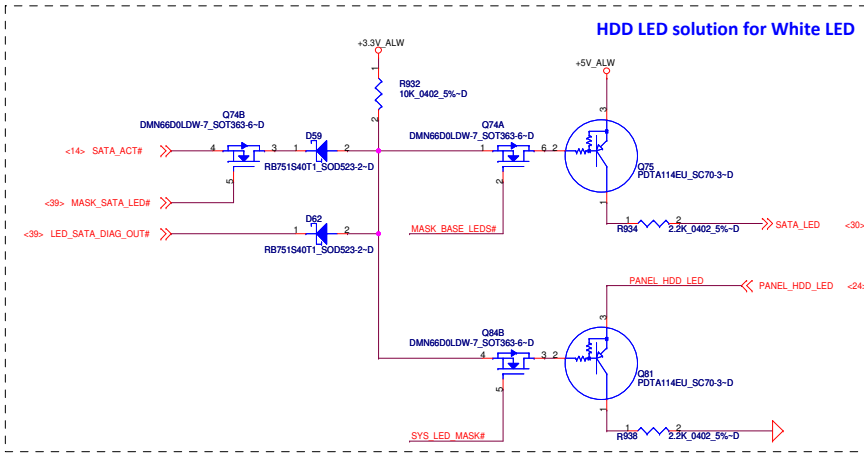
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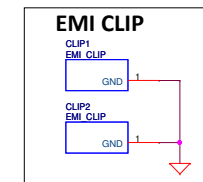
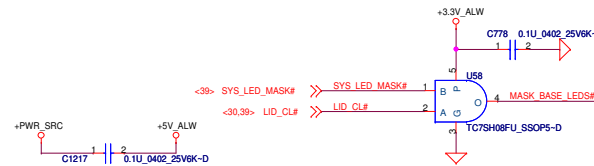
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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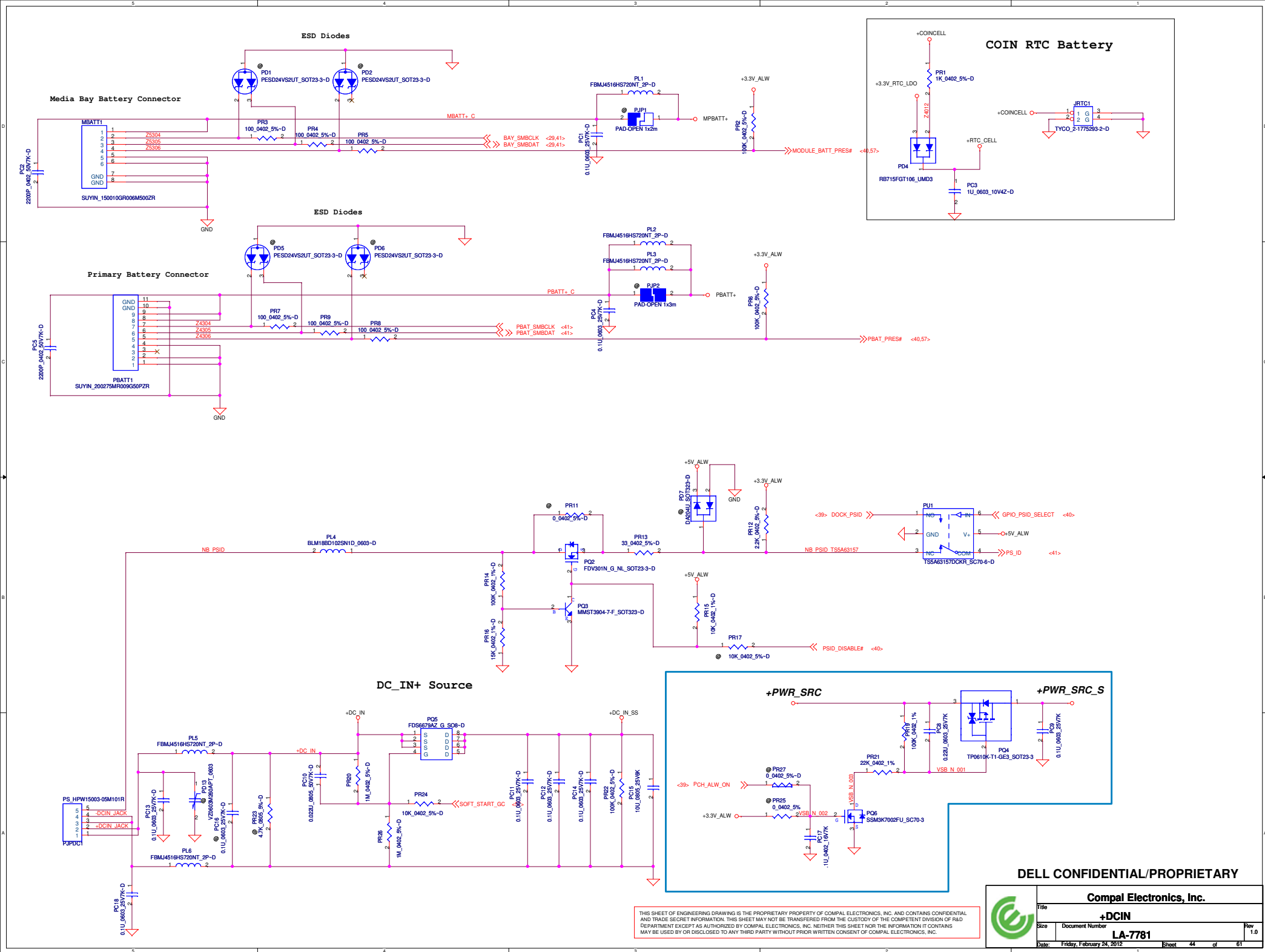
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PAD and Standoff

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Size

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Date

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Rev

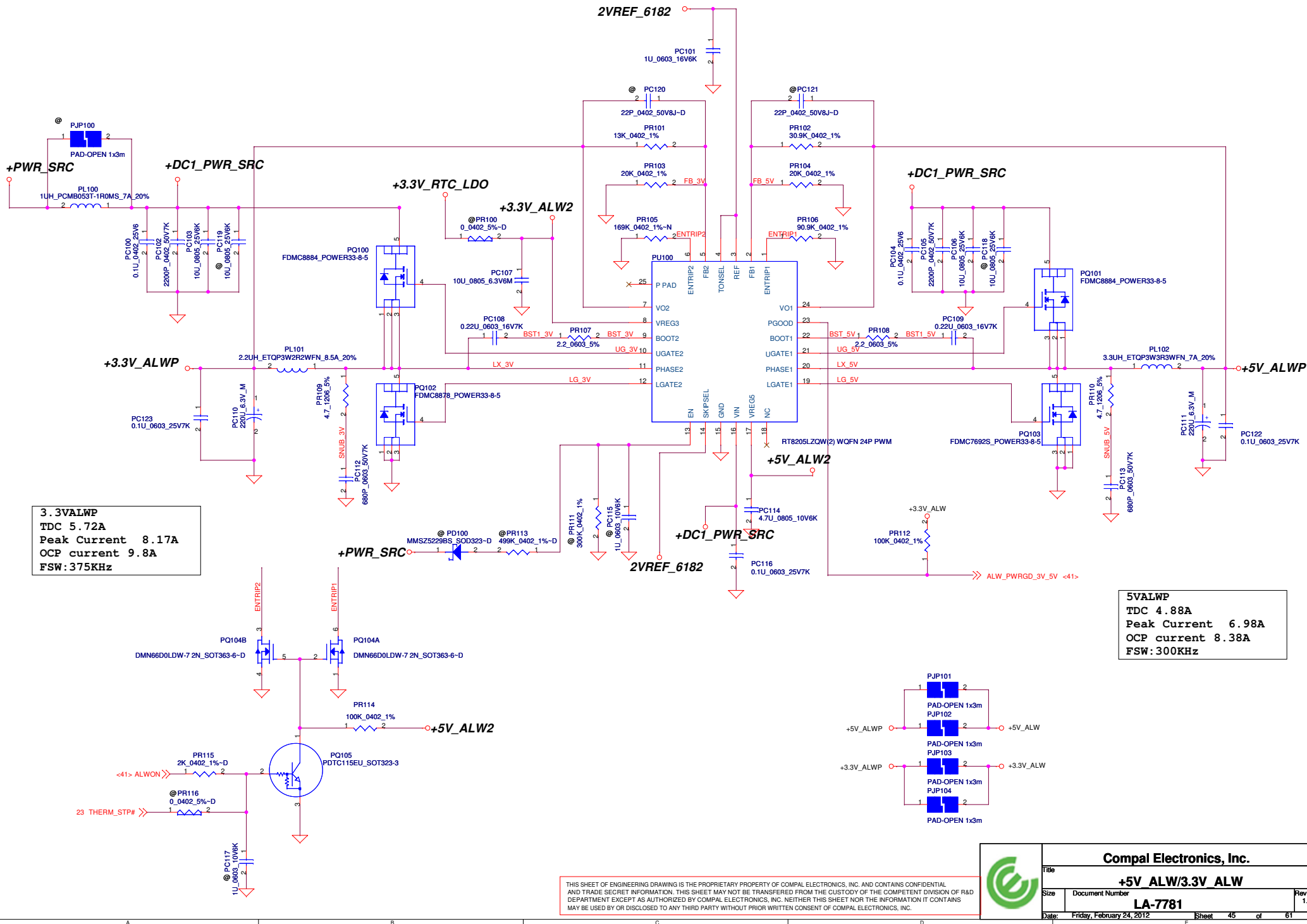
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of

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3.3VALWP
TDC 5.72A
Peak Current 8.17A
OCP current 9.8A
FSW: 375KHz

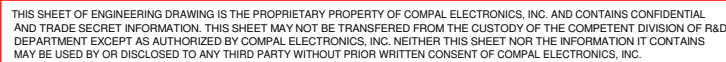
5VALWP
TDC 4.88A
Peak Current 6.98A
OCP current 8.38A
FSW: 300KHz

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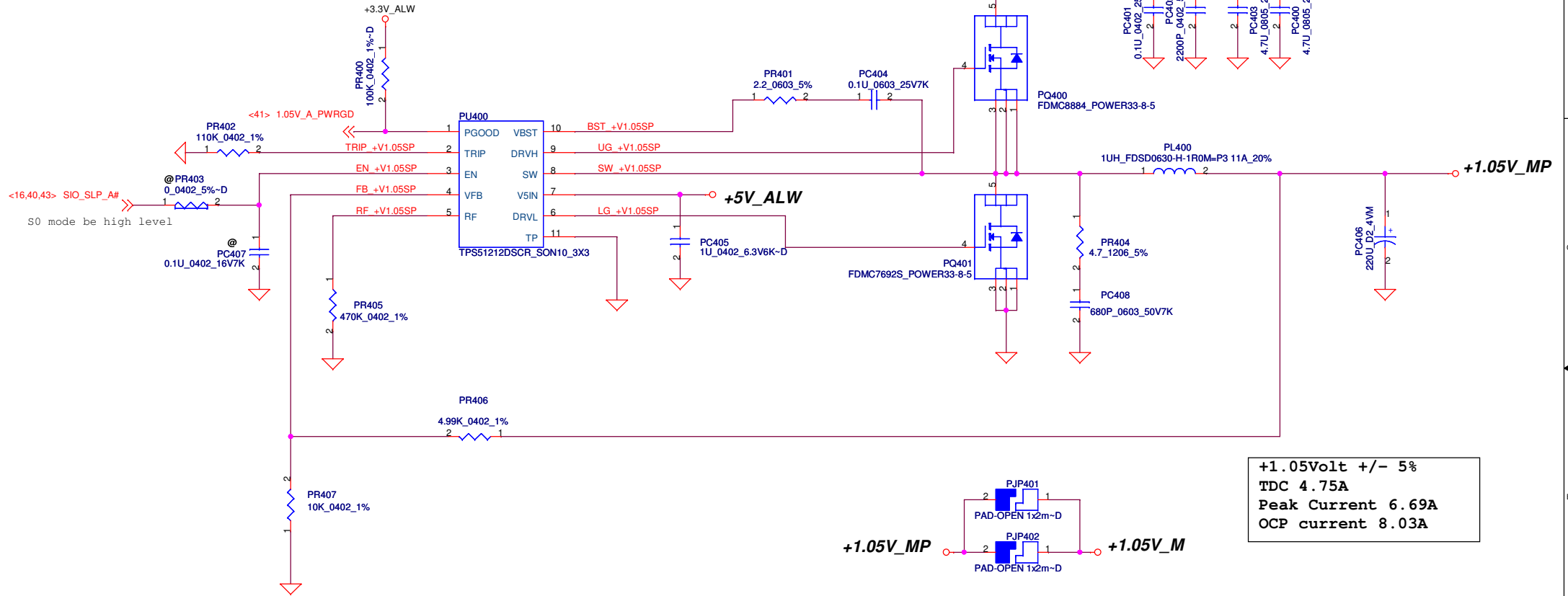


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Title		+5V_ALW/3.3V_ALW	
Size	Document Number	Rev	
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```
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A
```

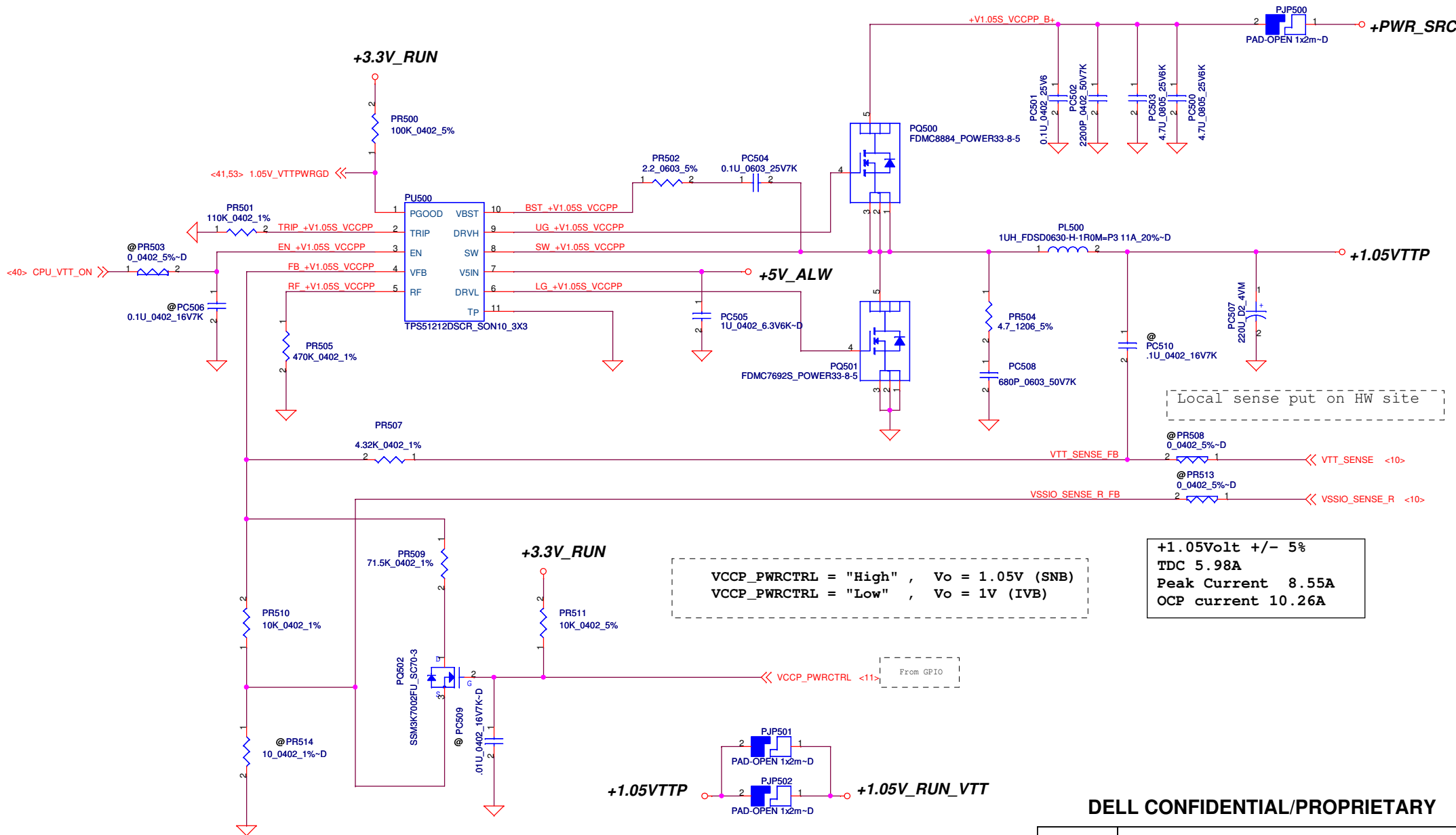


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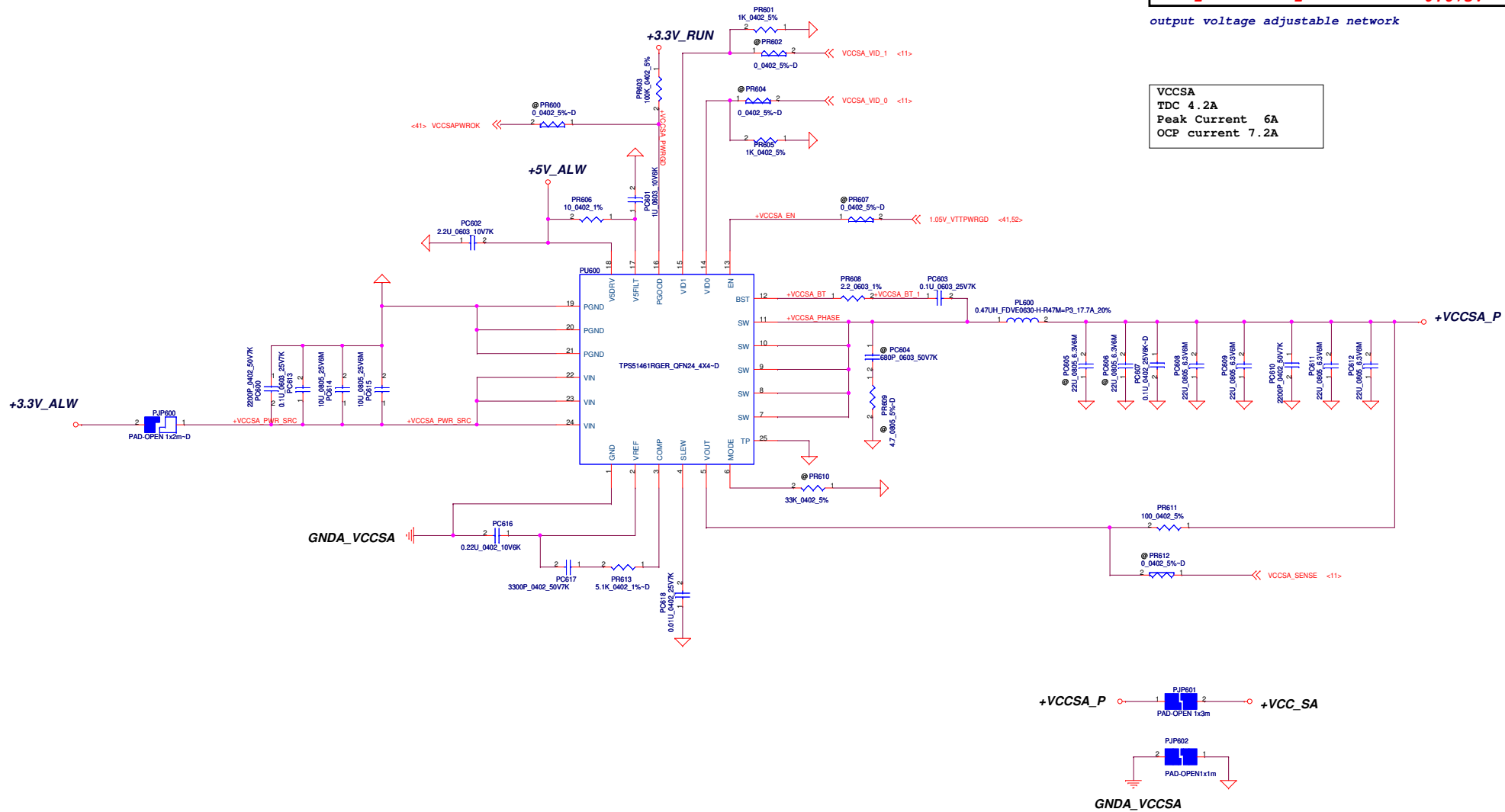
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+1.05V_M			
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Compal Electronics, Inc.			
Title			
+1.05V_RUN_VTT			
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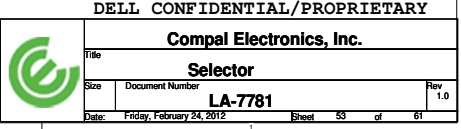
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		+VCC SA	
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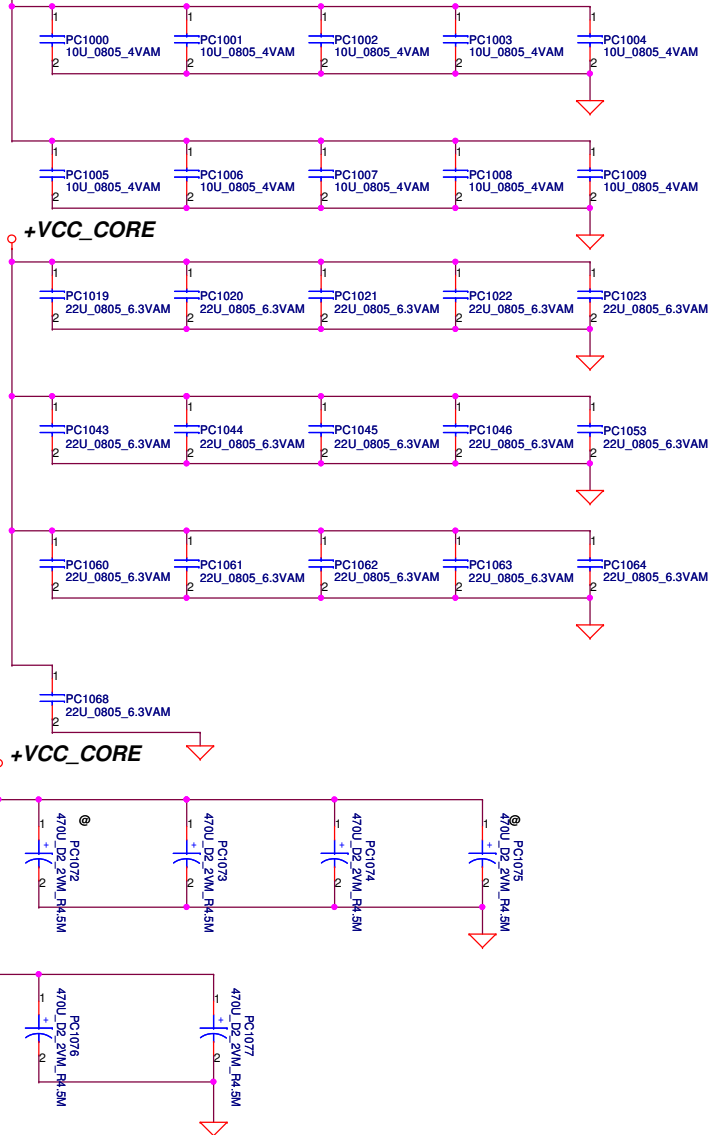


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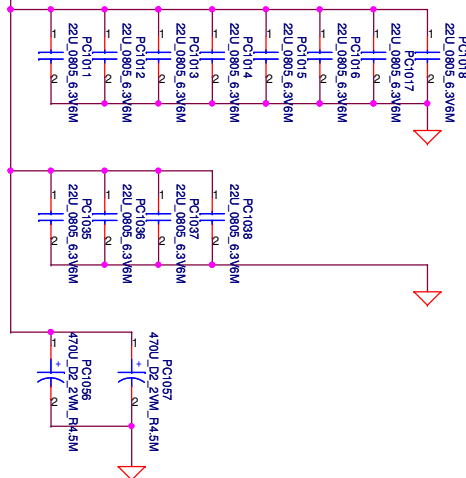
+VCC_CORE

+VCC_CORE



+VCC GFXCORE

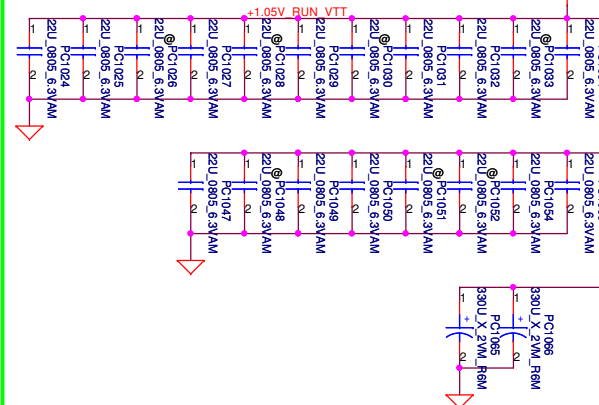
+VCC GFXCORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05V_RUN_VTT



For sandy bridge depop PC1267
For ivy bridge pop PC1267

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1	46	+1.5V_MEN	7/5	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	44	DCIN	8/4	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	45	+5V/3.3V	8/4	Compal	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	51	Vcore/GFX core	8/4	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Pop PC751,PR760,PC725,PR731, PC745,PR751(680pF 0603, 4.7 ohm 1206)	X01
5	45	+5V/3.3V	8/4	Compal	DFX concern, choke change from 10*10 to 7*7	PL101 change from 3.3u 10*10 to 2.2u 7*7 PL102 change from 3.3u 10*10 to 3.3u 7*7	X01
6	45 46	+5V/3.3V +1.5V_MEN	8/4	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC110,PC111 change from 220u polymer cap to 220u OScon cap PC208 change from 330u polymer cap to 390u OScon cap	X01
7	45 46	+5V/3.3V +1.5V_MEN	8/4	Compal	Prevent Jitter issue.	Add PC120,PC121,PC215 parallel with PR101,PR102,PR207	X01
8	51	Vcore/GFX core	8/4	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
9	51,52 45	Vcore, Charger +5V/3.3V	8/8	Compal Justin_Hsu	EMI solution.	Pop PL700.PL1300,PL100	X01
10	45 46	+5V/3.3V +1.5V_MEN	8/8	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Pop PR109,PC112,PR110,PC113,PC209,PR203 (680pF 0603, 4.7 ohm 1206)	X01
11	47,48 49	+1.8V/+1.05VM +1.05V_VTT	8/8	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Pop PR301(0805),PC305,PR404,PC408,PR504, PC508(680pF 0603, 4.7 ohm 1206)	X01
12	45	+5V/3.3V	8/10	Compal JimmyCC_Kuo	Suppress WWAN BB noise.	Add PC122,PC123 on +5V_ALWP and +3.3V_ALWP	X01
13	45-53		11/16	Compal	For cost saving, change the 0ohm resistors to layout short PAD.	Footprint change PR100,PR116,PR208,PR210, PR306,PR403,PR503,PR508,PR513,PR600,PR607, PR612,PR602,PR604,PR714,PR726,PR713,PR721, PR723,PR1300,PR1302,PR1312,PR1320,PR1339, PR1342,PR911,PR925,PR937,PR941,PR932,PR936, PR926,PR935,PR945,PR947,PR949,PR939,PR940, PR943,PR948,PR951,PR955,PR957,PR961,PR953, PR954,PR956,PR958,PR959,PR960,PR963	X02
14	44	DCIN	11/30	Compal	Reduce power consumption in S5.	Add PCH_ALW_ON for +PWR_SRC_S enable signal.	X02

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1	51	VCORE/GFXcore	12/09	Compal	Fine tune load line,OCP,transient response.	PR740 change from 2K to 2.1K ohm. PC740 change from 0.033uF to 0.082uF. PR750 change from 348 to 365 ohm. PC707 change from 0.022uF to 0.1uF. PR711 change from 357 to 412 ohm. PR702 change from 2.55k to 3.32K ohm.	X02
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
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1	42	HW	07/11/2011	COMPAL	E4 uses SIO_SLP_S4# for power control	DDR_ON and SUS_ON are replaced by SIO_SLP_S4#	X01
2	14, 39	HW	07/11/2011	COMPAL	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
3	11	HW	07/11/2011	COMPAL	Follow INTEL DG	Change RC99, RC100 from SD034100A8L (S RES 1/16W 10 +-1% 0402) to SD03410008L (S RES 1/16W 100 +-1% 0402)	X01
4	24	HW	07/11/2011	COMPAL	ATG needs touch screen circuit	Add "5@" for touch screen circuit of Dalmore 14" ATG	X01
5	22	HW	07/11/2011	COMPAL	UMA uses EMC4021 for cost concern	Change thermal sensor to EMC4021 for UMA	X01
6	42	HW	07/14/2011	COMPAL	Load SW sources output rising time mismatch and COS. cost concern	Change back to E3 +3.3V/5V_RUN discrete solution	X01
7	20	HW	07/14/2011	COMPAL	CH94 and CH95 to D2 size for cost concern	Change CH94 and CH95 from SGA0000170L to SGA00004L0L	X01
8	29	HW	07/19/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
9	20, 42	HW	07/21/2011	COMPAL	Vgs less than cut-in voltage in battery mode	Add control circuit for +5V_ALW_PCH	X01
10	27, 28, 42	HW	07/25/2011	COMPAL	Vgs of 5V MOS maybe large than max rating	Add R516, R517. Change Q55 from SB00000KQ0L to SB00000GV00	X01
11	11	HW	07/25/2011	COMPAL	Follow INTEL PDDG 0.8	De-pop RC140	X01
12	32	HW	07/25/2011	COMPAL	RESET_OUT# power sequence issue	Add R1640, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
13	15	HW	07/25/2011	COMPAL	Follow crystal measurement report	Change CH18 and CH19 to 8.2pF	X01
14	40	HW	07/27/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
15	34	HW	07/27/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
16	23	HW	07/28/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
17	16	HW	07/28/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5 circuit for HW solution	X01
18	29	HW	08/01/2011	COMPAL	Co-lay 92HD93 with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642; Q107/R171 Reserve for ALC290 only: C1204, C1205, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963	X01
19	41	HW	08/02/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
20	29	HW	08/02/2011	COMPAL	EMI request to add solution for BITCLK	Pop R1076 (33ohms) and C977 (10pF) for PCH_AZ_CODEC_BITCLK	X01
21	26	HW	08/03/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
22	17	HW	08/03/2011	COMPAL	Request from INTEL review feedback	Pop RH332 for PCH_GPIO3	X01

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23	42, 43	HW	08/04/2011	COMPAL	For cost saving	Change Q61 to SB00000GV00; HDD and breath LED control share Q84; Power team request Q59 change to SB00000L80L	X01
24	24, 29, 33	HW	08/08/2011	COMPAL	EMI request to add solution	Pop RE678 (22ohms), CE757 (33pF) and C981~3 (0.1uF). Add CE758 (33pF). Reserve C1206 and C1207.	X01
25	41	HW	08/08/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
26	39	HW	08/08/2011	COMPAL	RF request to add solution	Pop R795 (33ohms), C713 (32pF), RE5 (33ohms), CE3 (32pF), R885 (10ohms) and C747 (8.2pF)	X01
27	43	HW	08/08/2011	COMPAL	White light LED brightness is abnormal	Change R934, R938, R939, R949, R958, R957 and R955 to 2.2 Kohms	X01
28	40	HW	08/09/2011	COMPAL	ESD request add 0.1uF on ALWON	Reserve C1208 for ESD backup plan	X01
29	17	HW	08/10/2011	COMPAL	RF request 10pF on MEC and 5048 PCI CLK	Reserve 10pF bypass cap. at CH109 and CH110	X01
30	18	HW	08/11/2011	COMPAL	Delete TCM and Non-TPM configuration	De-pop RH270 and RH271. Always pop RH267 and RH268	X01
31	11	HW	08/12/2011	COMPAL	S3 can't resume issue	Control 1.5V_VDDQ by EC. Pop RC79 and de-pop RC82	X01
32	40	HW	08/15/2011	COMPAL	Change board ID to X02	Change R875 to 62Kohms	X02
33	14~21	HW	08/15/2011	COMPAL	Change PCH to B0 version	Change UH4 to SA00004NQ2L	X02
34	42	HW	08/18/2011	COMPAL	Rated Vgs of Q61 is 25V	De-pop R1627	X02
35	36	HW	08/19/2011	COMPAL	Follow INTEL DG	Change C410~C413 from 0.01uF to 0.1uF	X02
36	19	HW	08/19/2011	COMPAL	CRT ripple garbage display issue	Change LH1 from 180ohms bead to 1uH inductor	X02
37	29	HW	08/29/2011	COMPAL	IDT request and codec version change	Change C1163 from 1uF to 2.2uF and codec from WA to WB version	X02
38	43	HW	08/29/2011	COMPAL	To meet current limit resistor of LED spec	Change R949, R958, R957, R955, R939, R938, R934 from 2.2K to 1.2Kohms	X02
39	42	HW	09/02/2011	COMPAL	DMN3030LSS-13 poor soldering issue	Change Q55 and Q61 to A04478L	X02
40	39	HW	09/02/2011	COMPAL	SMSC change 5048 pin A23 to GPIOIO	Re-link ECE 5048 symbol	X02
41	25	HW	09/14/2011	COMPAL	HDMI EMI low cost solution	De-pop L19~L22. Add L100~107 (9nH) and C1209~C1216 (3.3pF)	X02
42	40	HW	09/14/2011	COMPAL	SMSC review feedback	Add R1656 and R1657 100Kohms to GND for I2S disabled	X02
43	29	HW	09/16/2011	COMPAL	Remove ALC290 co-lay circuit	Remove R1648, R1647, R1646, R1645, C1165, C1164, R1643, R1644, R1642, R171, C1204, C1205	X02
44	29	HW	09/16/2011	COMPAL	15" UMA speaker no sound issue	Add snubber on speaker trace with C: 2200pF and R: 3.3ohms. Change bead rated current from 200mA to 2A.	X02
45	33	HW	09/26/2011	COMPAL	EMI request to change SD CLK series R	R676 is changed from 33ohms to 10ohms	X02
46	42	HW	09/26/2011	COMPAL	1V leakage on +3.3V_RUN during system boot	Pop Q69 and R929 discharge circuit	X02
47	40	HW	09/26/2011	COMPAL	EC has internal pull up for volume signals	De-pop R1169, R1197 and R1118	X02

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D-48	42	HW	09/28/2011	COMPAL	INTEL timing spec, V2 fail	Change C763 to 470pF as that of +3.3V_RUN	X02
49	41	HW	10/05/2011	COMPAL	Chane reset IC to RT9818A-44GU3	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.	X02
50	39	HW	10/05/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R771 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766	X02
51	19	HW	10/11/2011	COMPAL	CRT ripple garbage display issue	Change CH36 from 10uF to 22uF	X02
52	7~42	HW	10/11/2011	COMPAL	For cost saving	Change 0 ohm resistor to short pad	X02
53	29	HW	10/11/2011	COMPAL	Change C973~C976 P/N and R1658~R1661 size	Change C973~C976 P/N to SE074222K8L. Change R1658~R1661 size to 0402.	X02
-54	42	HW	10/18/2011	COMPAL	+3.3V_SUS sequence timing probelm	Change C767 to 470pF, the same as that of +3.3V_RUN	X02
55	22	HW	10/18/2011	COMPAL	Thermal requests to change OTP from 88 to 93	Change R406 from 953ohms to 1.24Kohms	X02
G-56	43	HW	10/20/2011	COMPAL	BREATH LED flash issue when AC plugin	Add Q126 to control BREATH LED	X02
57	32	HW	10/24/2011	COMPAL	TPM is changed to AT97SC3204-X2A18-AB	U39(TPM) is changed to SA00004WQ10(AT97SC3204-X2A18-AB) for WIN8 support	X02
58	42	HW	10/25/2011	COMPAL	+3.3/5V_RUN inrush curren issue with 470pF	Change C763 and C766 form 470pF to 2200pF	X02
59	33	HW	10/25/2011	COMPAL	EMI change to reserve solution for SD/MMCLK	De-pop RE678 and CE757	X02
H-60	34	HW	11/04/2011	COMPAL	PCH GPIO52 changed to be free	De-pop R725, remove R695 and add RH359	X02
61	17, 39, 40	HW	11/07/2011	COMPAL	RF final solution for PCI clock noise	De-pop R795, C713, R885 and C747. Pop CH109 and CH110 with 12pF	X02
62	43	HW	11/07/2011	COMPAL	Change current limit resistors of LED	R949 from 2.2K to 1K, R939 from 2.2K to 1.8K, R957 from 2.2K to 220, R951 from 475 to 330, R953 from 475 to 330 and R958 from 2.2K to 620	X02
-67	14~21	HW	11/07/2011	COMPAL	Change PCH to C0 version	Change UH4 to SA00005BU0L	X02
B-68	11, 42	HW	11/07/2011	COMPAL	AO4728L leakage issue	Change QC3 and Q59 to AO4304L (SB00000RV00)	X02
69	32	HW	11/07/2011	COMPAL	+3.3V_RUN Giltch when AC plugin	Add R1662 0ohm resistor. Reserve D87 and R1663 (pull high to +3.3V_RUN_TPM) for HW solution backup.	X02
70		HW	11/07/2011	COMPAL	Change 1Kohms tolerance for cost saving	Change 1Kohms +-1% to +-5% except RC78, RC80, RC81 and RC84	X02
71	38	HW	11/11/2011	COMPAL	EMI request to add 33ohms for DP port	Add RE7~RE24 for DP portD and portC	X02
A-72		HW	11/16/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	RC72 from 100K to 330K; RC143 from 330K to 1M; CC136 from 0.1u to 0.022u R412 from 100K to 470K; R1632 from 1M to 4.7M; C293 from 0.1u to 0.022u R507 from 100K to 470K; R517 from 1M to 4.7M; C400 from 0.1u to 0.022u R722 from 100K to 470K; R1625 from 1M to 4.7M; C644 from 4700p to 220p R729 from 100K to 470K; R1628 from 1M to 4.7M; C650 from 4700p to 220p R917 from 100K to 470K; R1617 from 1M to 4.7M; C770 from 4700p to 220p R920 from 100K to 470K; R1610 from 470K to 2.2M; C771 from 4700p to 470p R930 from 100K to 470K; R1611 from 470K to 2.2M; C773 from 2200p to 100p R906 from 100K to 470K; C763 from 2200p to 220p R912 from 100K to 470K; C766 from 470p to 220p	X02
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73	36	HW	11/21/2011	COMPAL	ESD team modify USB3.0 ESD diode package	Change D78 and D79 to NXP IP4292CZ10-TBR(SC300002F0L, Package: XSON10)	X02
74	42	HW	11/21/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	R930 from 470K to 330K; R1611 form 2.2M to 1M	X02
75	36	HW	11/23/2011	COMPAL	Add USB PWR SW circuit with G547 for JUSB2	Add single channel USB PWR SW U5, G547. Add decoupling cap. C677 and C678 for SW IC input. Add decoupling cap. C652 and C655 at conn. side.	X02
76	38	HW	11/29/2011	COMPAL	EMI solution for E-Docking USB (port8)	Add bypass resistors, R1672 and R1673; choke L99 for backup	X02
77	35	HW	11/30/2011	COMPAL	From ESD team request	Pop C1208 for UMA trace, ALWON Add CE10~CE12 for EXP PWR SW signals, CPUSB#, EXPRCRD_CPPE# and CARD_RESET# Add 0ohm resistors, RE27~RE32 and RE34~RE36 to block ESD from XDP	X02
78	17,34,38	HW	12/02/2011	COMPAL	EMI solution for E-Docking USB port	Swap USB Port6 and Port8; reserve a 90ohms choke at E-Docking conn.: Port6 from Mini3 Pink Panther card to E-docking Port8 from E-Docking to Mini3 Pink Panther card	X02
79	14~21	HW	12/05/2011	COMPAL	Change PCH to C1 version (QS)	Change UH4 to SA00005BU1L	X02
80	24	HW	12/06/2011	COMPAL	EMI solution for USB port12 of camera	Pop 90ohms choke, L10; De-pop R427 and R428	X02
81	42	HW	12/07/2011	COMPAL	+3.3V_SUS sequence timing	R911 from 100K to 470K; R1618 from 1M to 4.7M; C767 from 470p to 220p	X02
82	43	HW	12/07/2011	COMPAL	Add EMI solution	Add C1217 with 0.1uF	X02
83	25	HW	12/08/2011	COMPAL	EMI final solution for HDMI port	Pop L100~L107 with 9nH. Change C1209~C1216 from 3.3pF to 1.8pF. Change R450, R452~R456 and R458~R459 from 680ohms to 604ohms.	X02
84	41	HW	12/08/2011	COMPAL	To prevent inrush current at reset IC input	Change R1629 from 0ohms to 33ohms resistor	X02
85	25	HW	12/28/2011	COMPAL	SMT request to change F2 footprint	For DFX conern of F2 2nd source, SP040003H0L, change F2 footprint to F_MF-MSMF050-2	X02
86	40	HW	01/13/2012	COMPAL	Change board ID to A00	Change R875 to 33Kohms	A00
87	14	HW	01/13/2012	COMPAL	Add X76@ for ROM part	Add X76@ for U52 and U53	A00
88	40	HW	01/13/2012	COMPAL	Change MEC5055 P/N for MP	Change U51 P/N to SA00003TZ2L	A00
89	38	HW	01/13/2012	COMPAL	System hangs after hot dock (DF531758)	Change R755 from 100Kohms to 10Kohms	A00
90	14~21,32	HW	02/01/2012	COMPAL	Chnage PCH, LAN chip P/N for X-build	UH4 is changed to SA00005BU3L U31 is changed to SA00003SI5L	A00
91	31	HW	02/01/2012	COMPAL	Change PWR button, SW1 back to E3 solution	change SW1 back to E3 solution, ALPS SKRBAE010	A00
92	15,18,32	HW	02/03/2012	COMPAL	Add BOM config for Non-TPM	Add 1@ for TPM and 2@ for Non-TPM config	A00
93	14	HW	02/16/2012	COMPAL	De-pop resistor on PCH JTAG for power saving	De-pop RH288, RH47, RH48 and RH49	A00
94	33	HW	02/20/2012	COMPAL	For SD card reader and KB ESD issue	Add 47nF CE13 close to reset input of SD card reader IC Add 100pF CE14 close to U4.3	A00
95	36	HW	02/24/2012	COMPAL	Samsung cell phone can't support CDP	Change charging mode to SDP only in S0 Add Q126 and change R1614 to 100Kohms (reserve this solution and R1614 10kohms)	A00
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96	36	HW	02/24/2012	COMPAL	Samsung cell phone can't support CDP	Change U2 to Seligo SA00004VH00	A00
97	41	HW	02/24/2012	COMPAL	Pericom IC fail	Change U4 to Richtek SA00005A60L	A00

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