

Compal confidential

Schematics Document

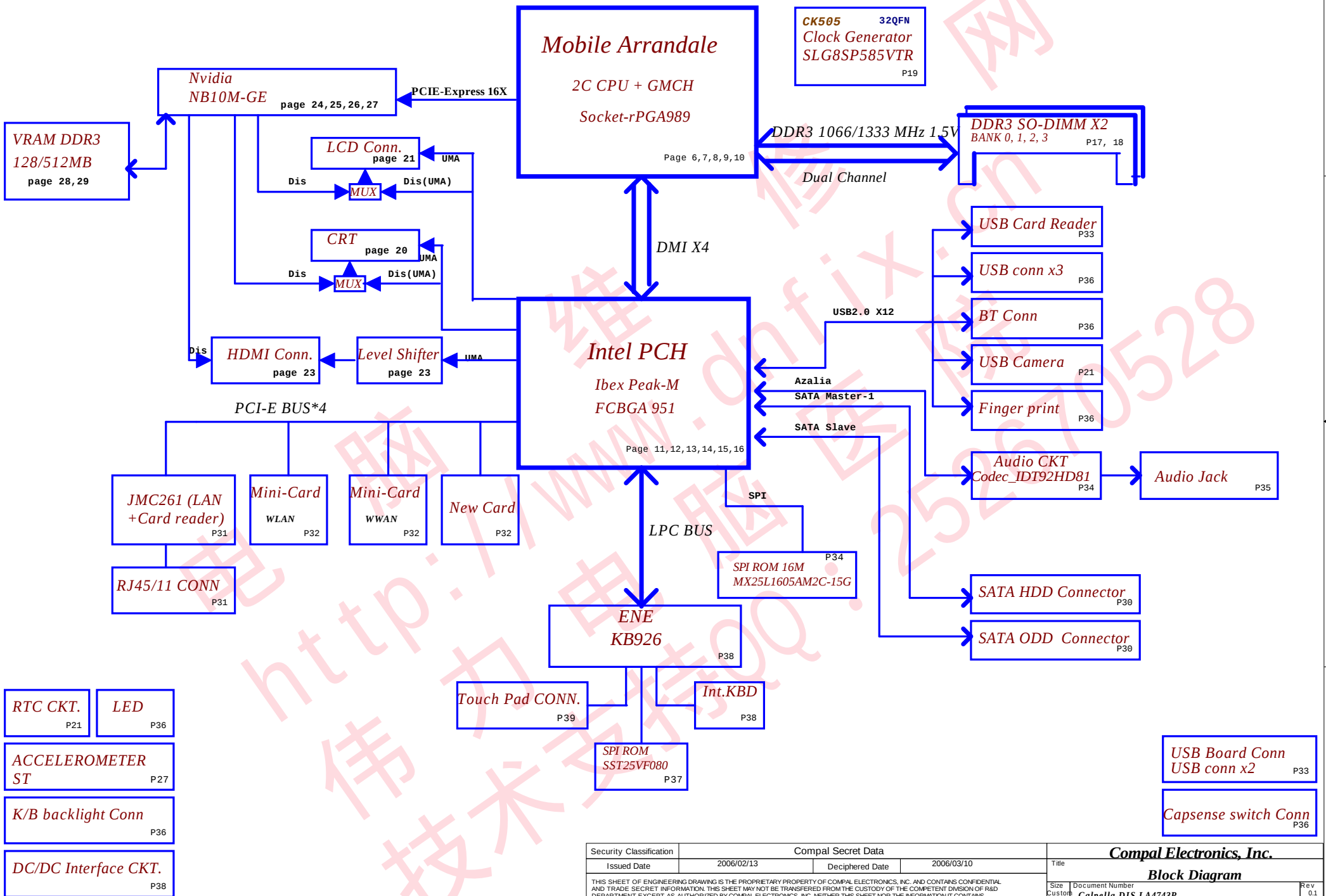
Mobile Auburndale rPGA989 with
Intel PCH(Ibex Peak-M) core logic

2009-04-13

機 等 密	硬體二部	
	產出人員	
	產出日期	
	解密日期	

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	Cover Sheet	
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				Custom	Calpella DIS LA4743P	0.1
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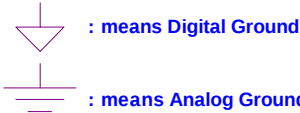
Calpella Consumer 13.3" UMA +Switchable



Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

Symbol Note :



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
SG@ :	means stuff when Switchable graphic
UMA@ :	means stuff when UMA skus
VRAM@ :	X76 level
8111DL@ :	Only for Giga LAN
DEBUG@ :	For debug
Cypress@ :	Only For Cypress Capacitor sensor board
ENE@ :	Only For ENE Capacitor sensor board
M3@ :	Only For Intel DDR3 VREF
PA@ :	Only For PA
PR@ :	Only For PR

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	X
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	WWAN
PCIe-2	WLAN
PCIe-3	LAN
PCIe-4	New card
PCIe-5	X
PCIe-6	X

SATA assignment:

SATA0	HDD
SATA1	ODD
SATA2	X
SATA3	X
SATA4	ESATA
SATA5	X

SMBUS Control Table

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK CHIP	WLAN WWAN	NB10M Thermal Sensor	NB10M-GE	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	PCH	V	X	X	V	V	V	X	X	X	V	V
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
		+3VS	+5VL		+3VS	+3VS	+3VALW		+5VL	+3VALW	+3VS	

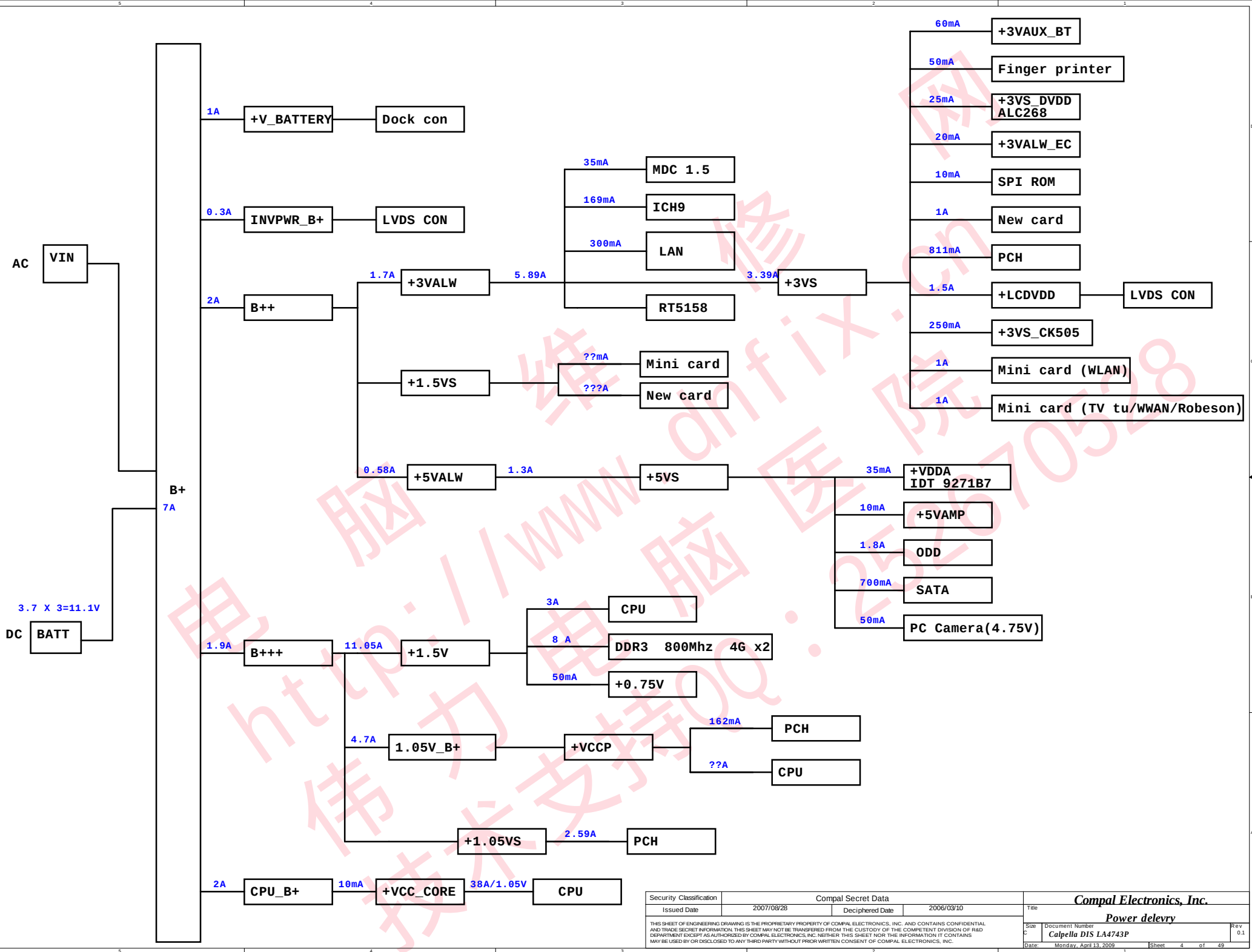
NB10M-GE SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
D_EDID_DATA D_EDID_CLK	NB10M	V	X	X
D_CRT_DDC_DATA D_CRT_DDC_DATA	NB10M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB10M	X	X	V

PCH I2C / SMBUS ADDRESSING

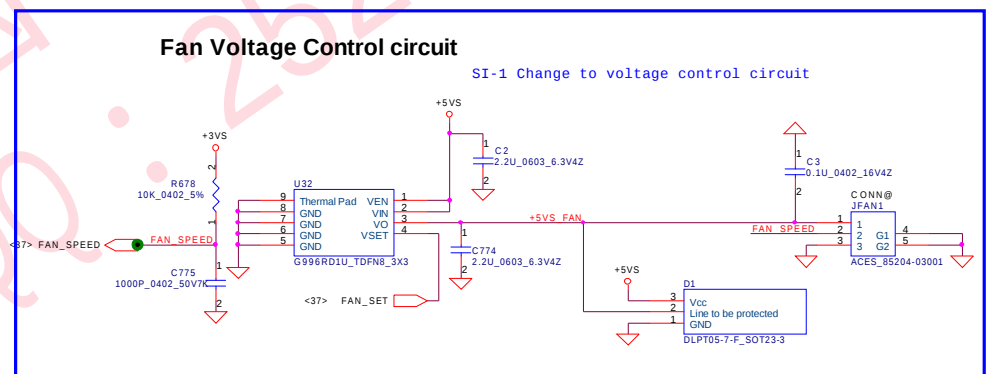
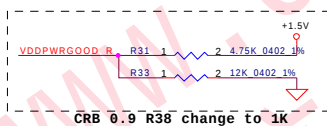
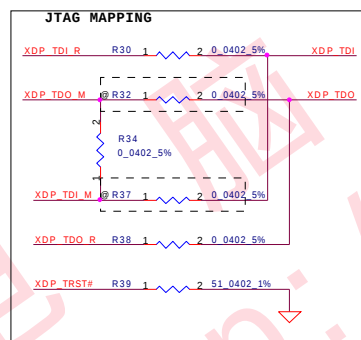
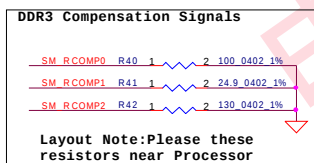
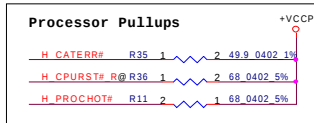
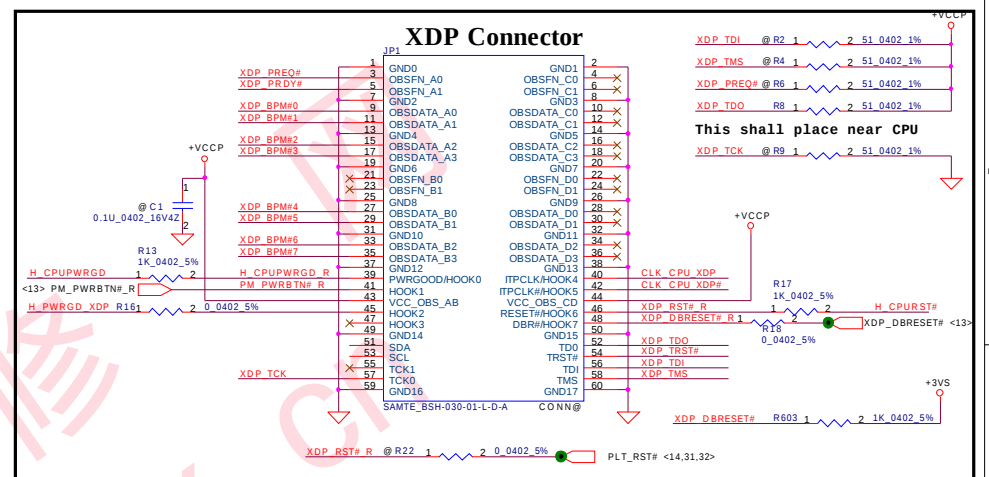
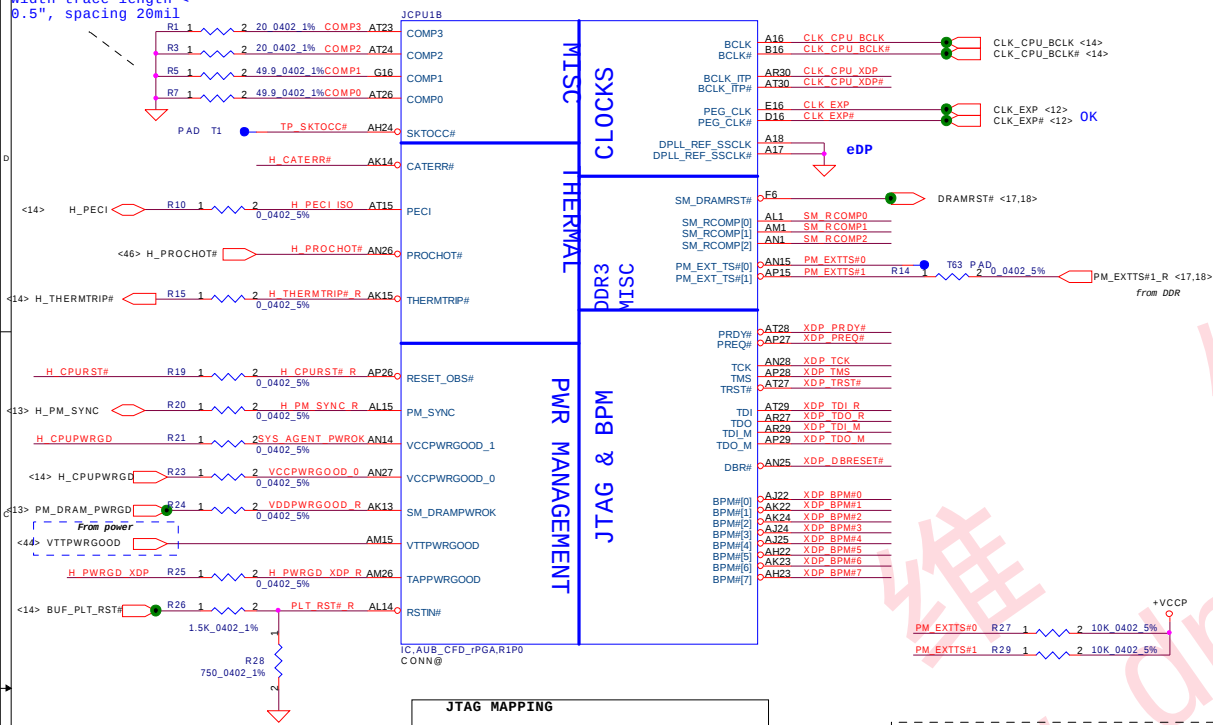
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

45172932L01 : Switchable graphic
45172932L02 : UMA only



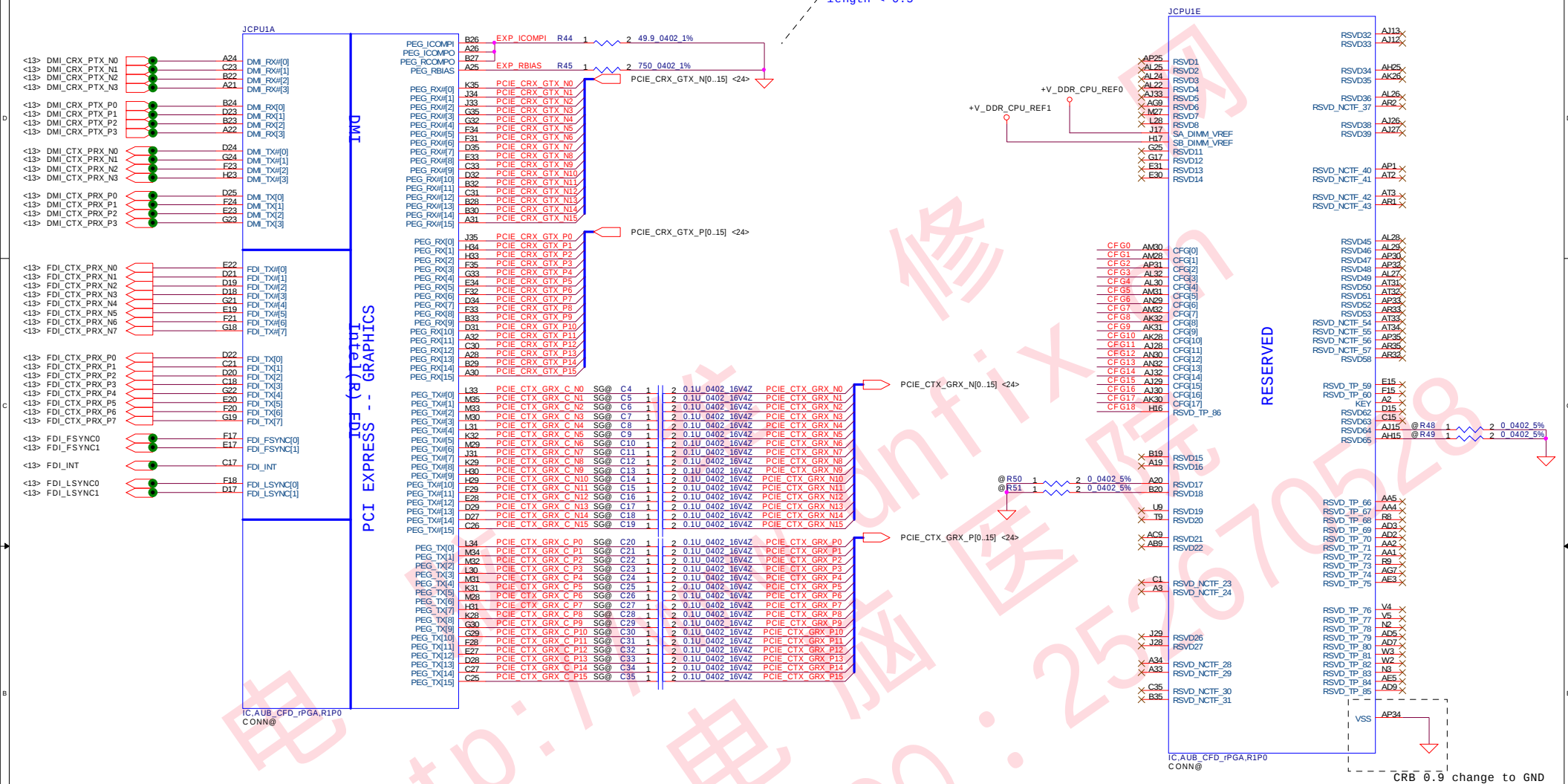
Calpella Discrete power on sequence				97.09.16.	Spec	define	min	Max
	Vin							
	B+							
	+3VL							
	+5VALW/+3VALW							
EC->PCH	RSMRST#	→ T1 ←			T1, >10ms, +3VALW to RSMRST#	T03	10 ms	-
	ON/OFF#	→ T2 ←			T2, User define			
EC->PCH	PWRBTN_OUT#	→ T3 ←			T3, 150ms, T4, 100ms			
PCH->EC	SLP_S5#	→ T5 ←			T5, >100ms, RSMRST# to SLP_S5#	T07	100 ms	-
PCH->EC	SLP_S4#	→ T6 ←			T6, >30us, SLP_S5# to SLP_S4#	T08	30 us	-
EC->PWR	SYSON	→ T7 ←			T7, 10ms, SLP_S3# to SYSON			
	+1.5V							
PCH->EC	SLP_S3#	→ T8 ←			T8, >30us, SLP_S4# to SLP_S3#	T09	30 us	-
EC->PWR	SUSP#	→ T9 ←			T9, 20ms, SLP_S3# to SUSP#			
	+5VS/+3VS/+1.8VS/+1.5VS/+1.05VS/+VCCP							
PWR->CPU	VTT_PWRGOOD	→ T10 ←			T10, VCCP stable to VTT_PWRGOOD assertion to the processor	T13	0.0001 ms	500 ms
EC->PWR	VR_ON	→ T11 ←			T11, >130ms, SLP_S3# to VR_ON	T16	99 ms	-
	+CPU_CORE	→ T12 ←			T12, Intel MVP soft start ramp-up time of +VOC_CORE	T17	-	3 ms
PWR->Clock	IMVP_CLK_EN#	→ T13 ←			T13, Duration Intel MVP V-boot, timing set by IMVP6.5	T18	10 us	100 us
	CLKIN_BCLK			Stable				
PWR->PCH or(EC->PCH)	VGATE or(PWROK)	→ T14 ←			T14, CLKIN_BCLK stable to VGATE assertion	T19	1 ms	-
PWR->PCH	PWROK	→ T15 ←			T15, IMVP_CLK_EN# to VGATE assert, Timing set by MVP6.5	T20	3 ms	20 ms
PWR->PCH	SYS_PWROK							
	MEPWROK				MEPWROK connect to PWROK (iAMT disable)			
	DRAMPWROK	→ T16 ←			T16, +1.5V stable to DRAMPWROK assertion, Timing set by PCH	T22	100 ns	-
	CLKOUT_BCLK	→ T17 ←			T17, VGATE assertion to DRAMPWROK assertion, Timing set by PCH	T23	1 ms	-
PCH->CPU	PROCPWRGD	→ T18 ←			T18, CLKOUT_BCLK stable to VCCPWRGOOD_0 + VCCPWRGOOD_1 assertion to Processor. Timing set by	T24	10 BCKS	-
	VCCPWRGOOD_0	→ T19 ←			T19, VTT_PWRGD to VCCPWRGOOD assertion, Timing set by PCH	T25	1 ms	-
	VCCPWRGOOD_1	→ T20 ←			T20, VGATE assertion to VCCPWRGOOD assertion, Timing by PCH	T26	1 ms	100 ms
		→ T21 ←			T21, VCORE stable to VCCPWRGOOD assertion	T27	0.05 ms	-
PCH->N.C.	SUS_STAT#	→ T22 ←			T22, VCCPWRGOOD to SUS_STAT#, timing default is 1ms	T28	0.03 ms	-
PCH->Device	PLT_RST#	→ T23 ←			T23, SUS_STAT# to PLTRST#, timing set by PCH	T29	60 us	-

Layout rule: 10mil
width trace length
0.5", spacing 20mil



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				Size	Document Number				Rev
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Layout rule : trace
length < 0.5"



CFG Straps for PROCESSOR

CFG0 @R52 1 2 3.01K 0402 1%

CFG4 @R53 1 2 3.01K 0402 1%

PCI-Express Configuration Select

CFG0
1: Single PEG★
0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG3 R54 1 2 3.01K 0402 1%

CFG3-PCI Express Static Lane Reversal

CFG3
1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 1,★

CFG4-Display Port Presence

CFG4
1: Disabled; No Physical★
Display Port

attached to Embedded Display Port
0: Enabled; An external
Display Port

device is connected to the
Embedded Display Port

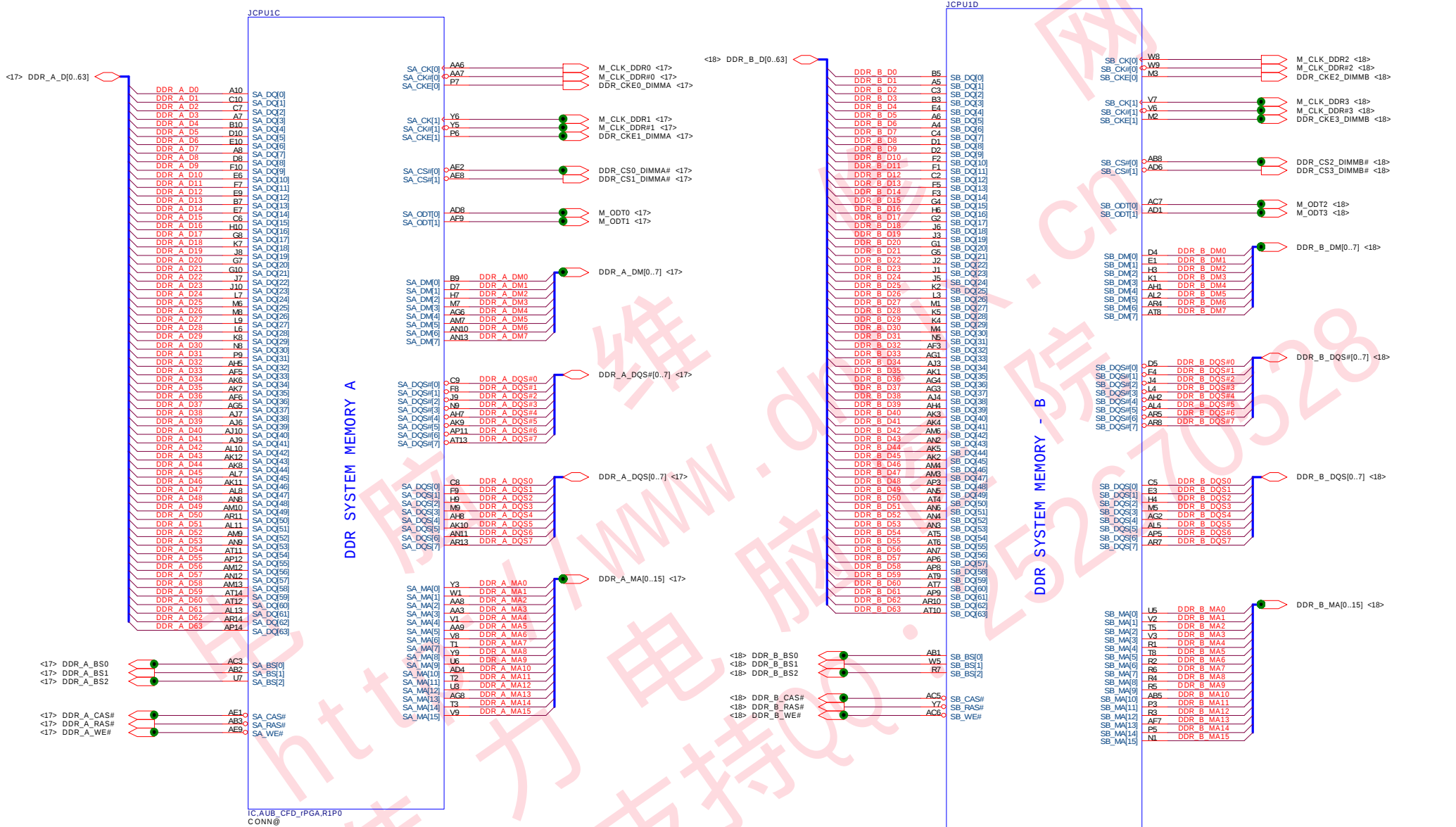
CFG7 @R55 1 2 3.01K 0402 1%

Only temporary for early
CFD samples (rPGA/BGA)

Only for pre E51 sample

CFG7
WW33 GPD 3.01K on CFG7 for PCIE Jitter
WW41: don't staff

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Title		Compal Electronics, Inc.	
Size		Auburndale(2/5)-DMI/PEG/FDI	
Custom		Calpella DIS LA4743P	
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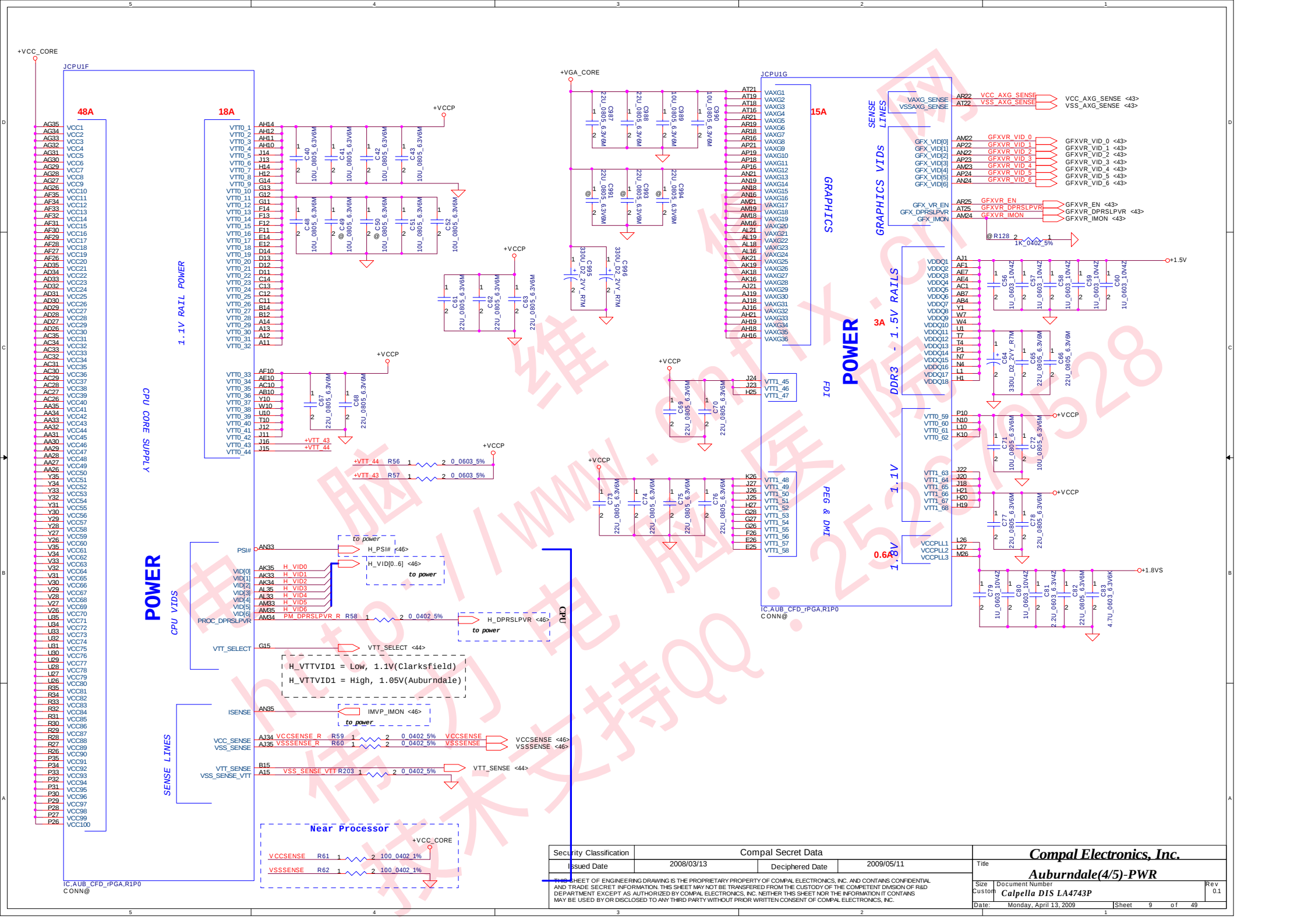


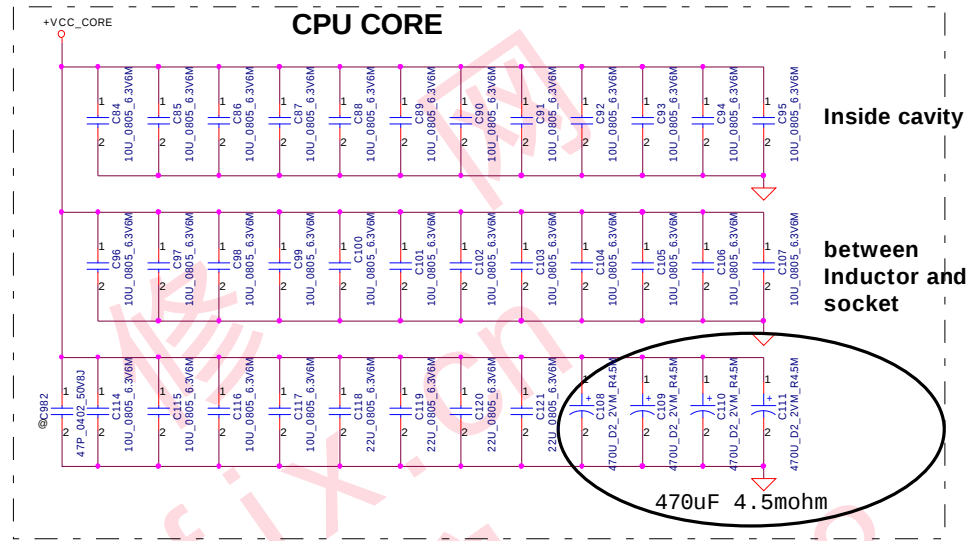
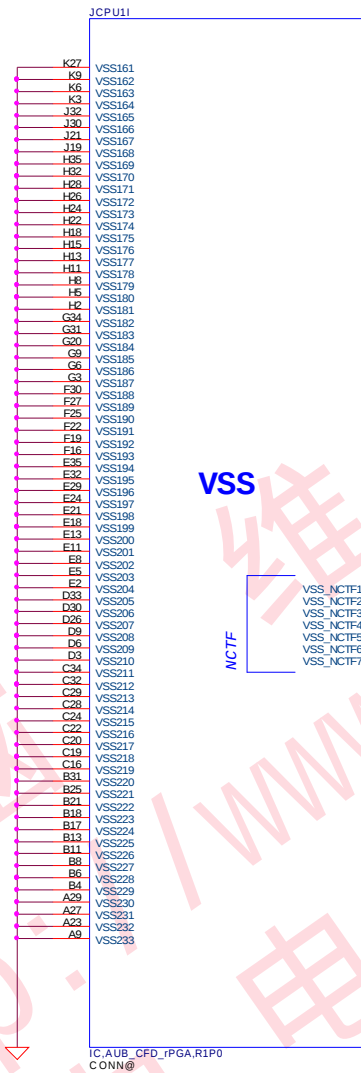
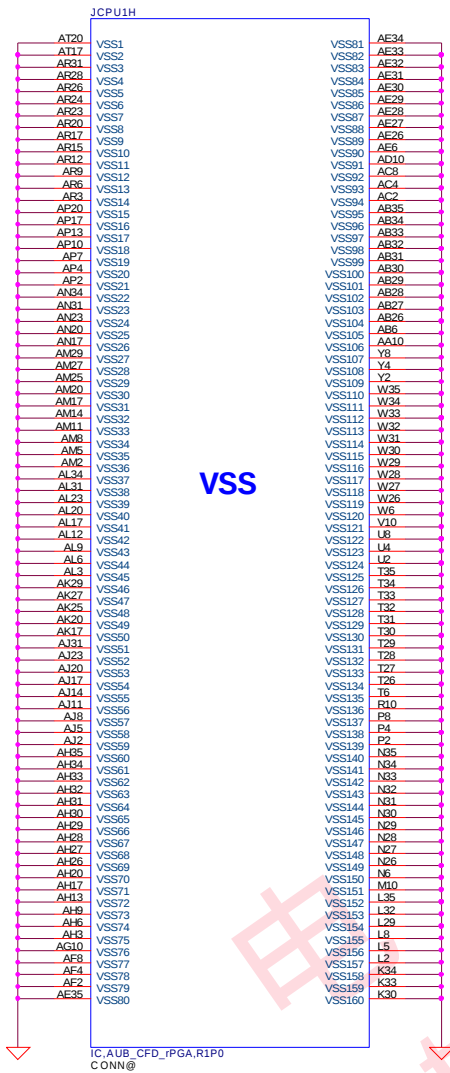
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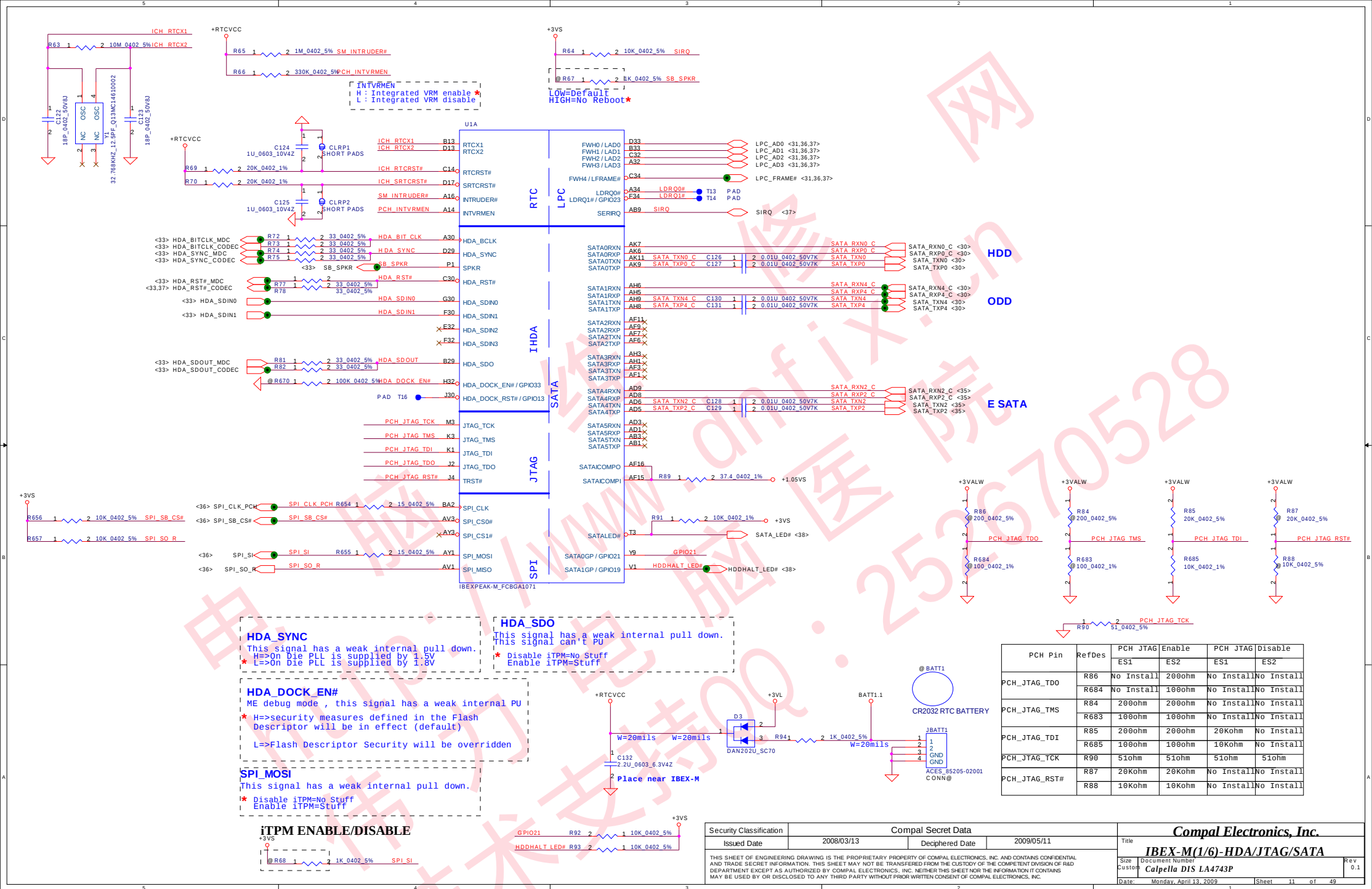
Cantiga(2/6)-DDR3 A/B CH

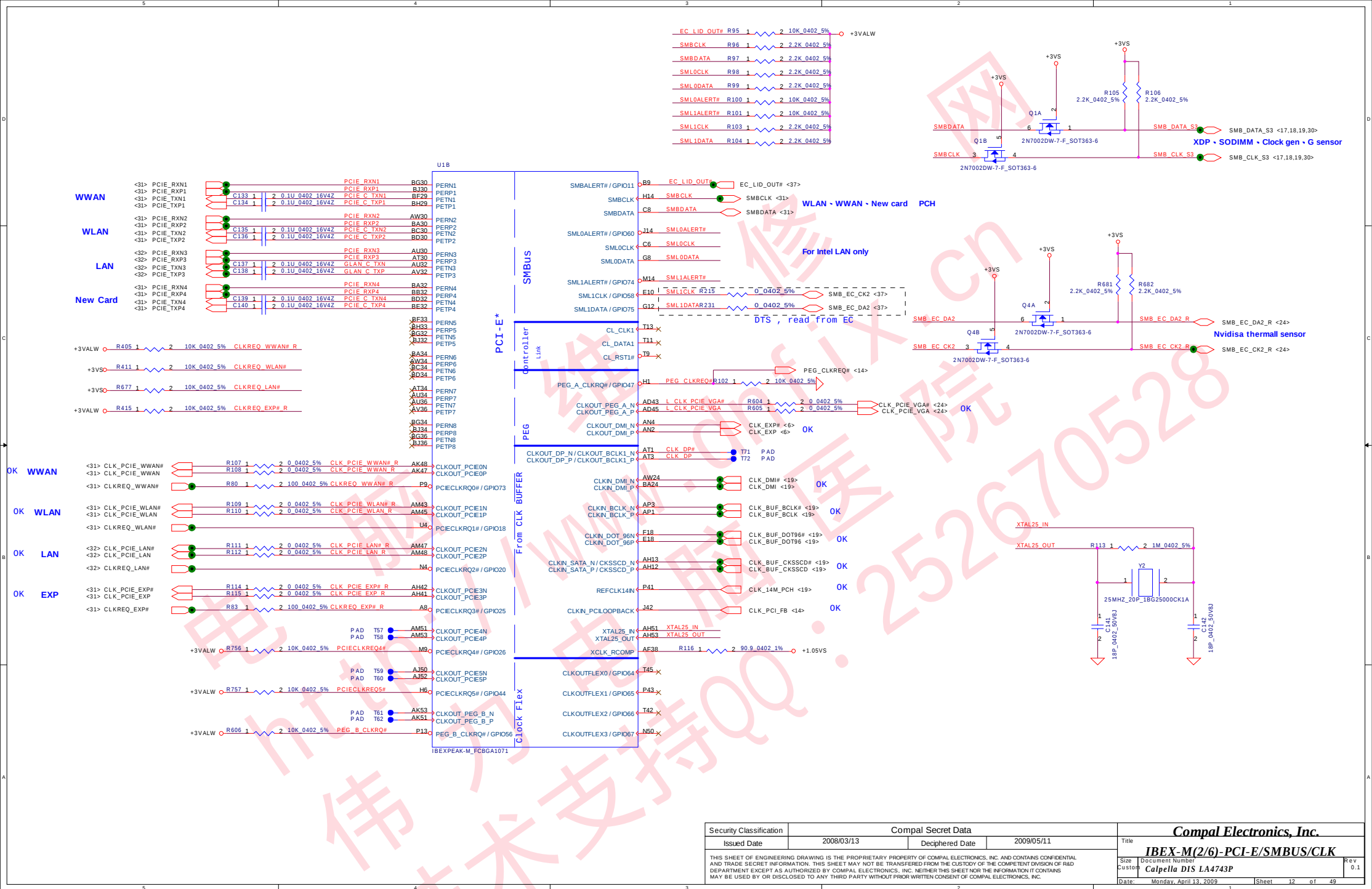
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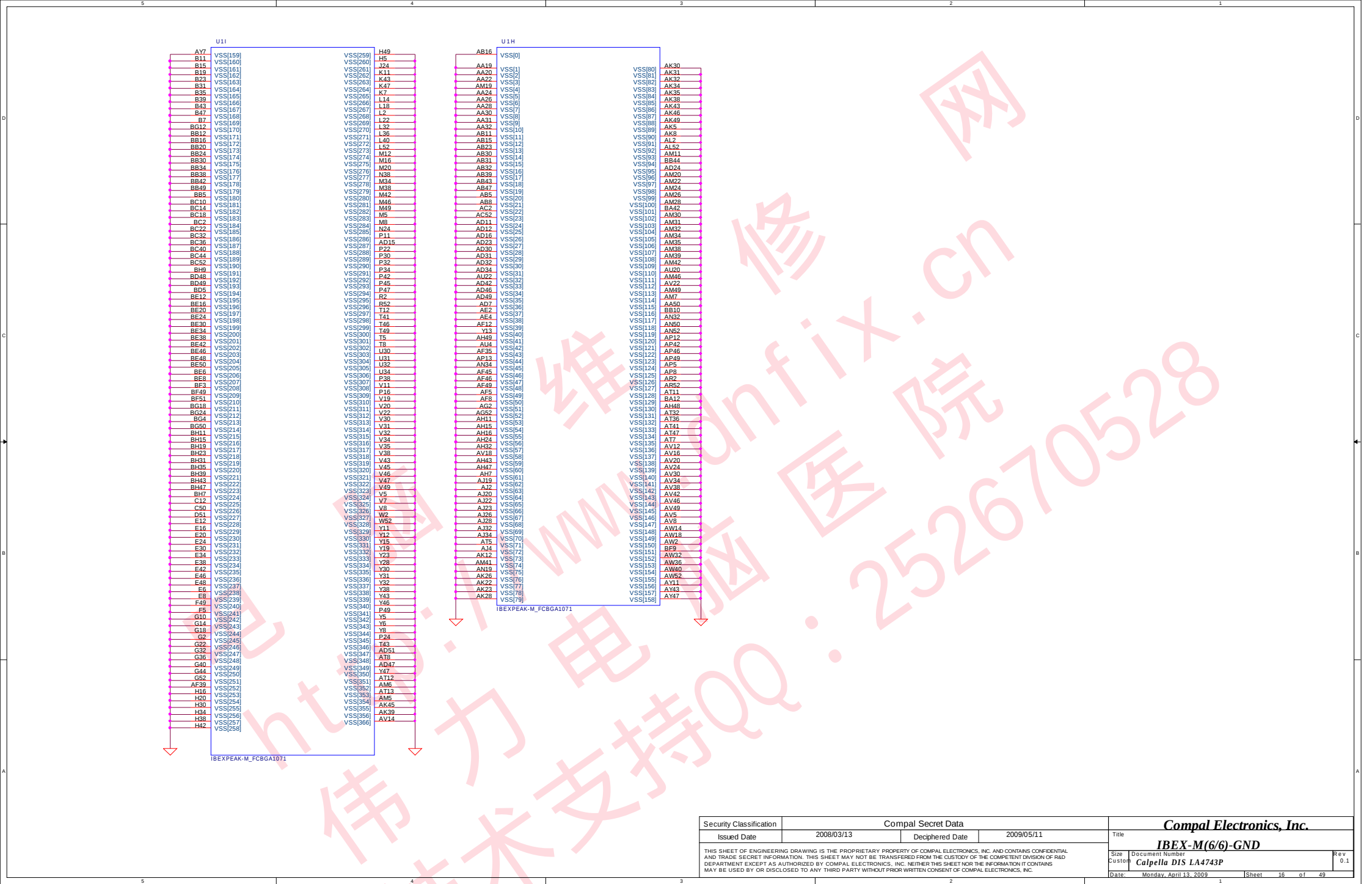




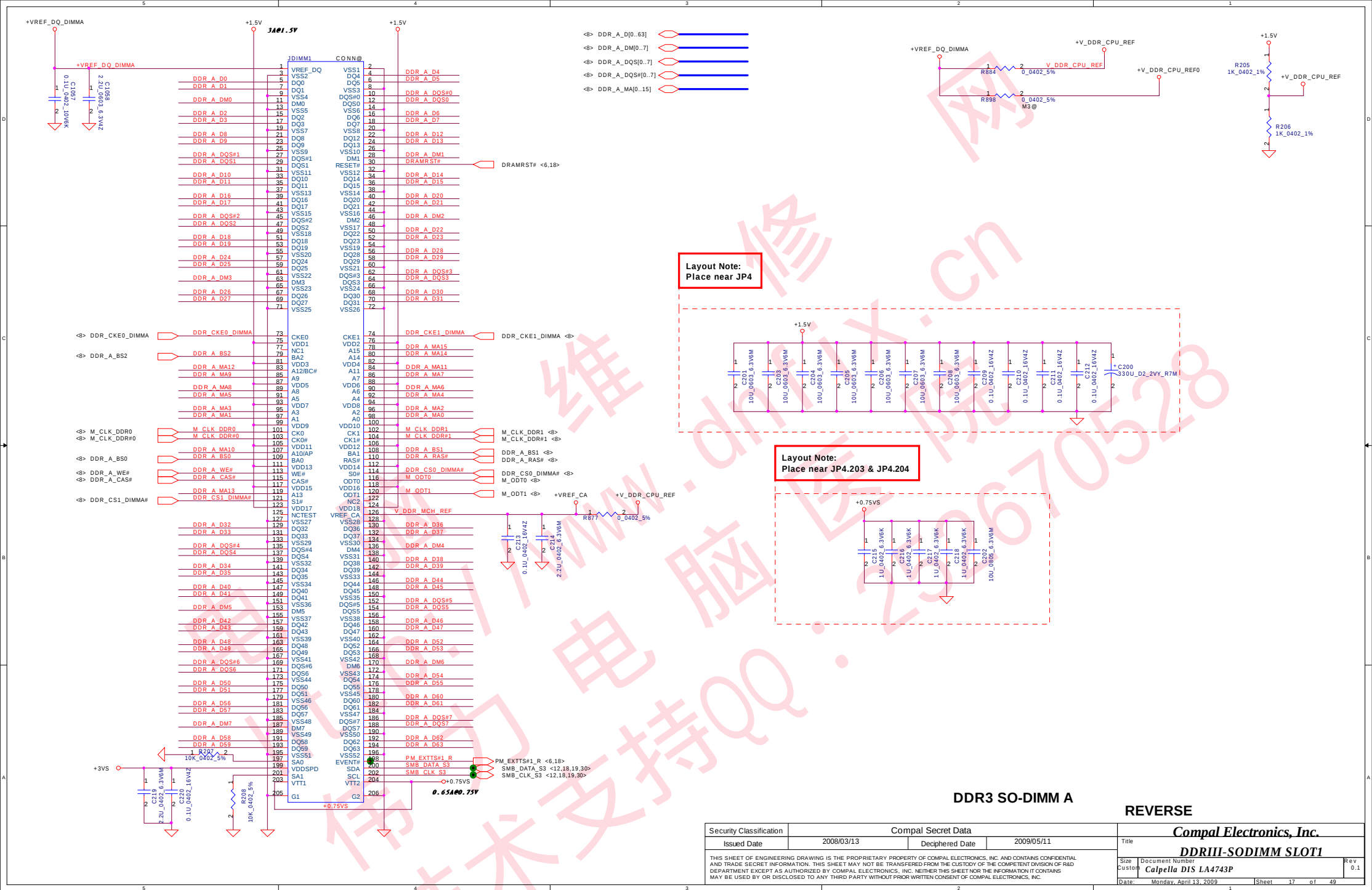
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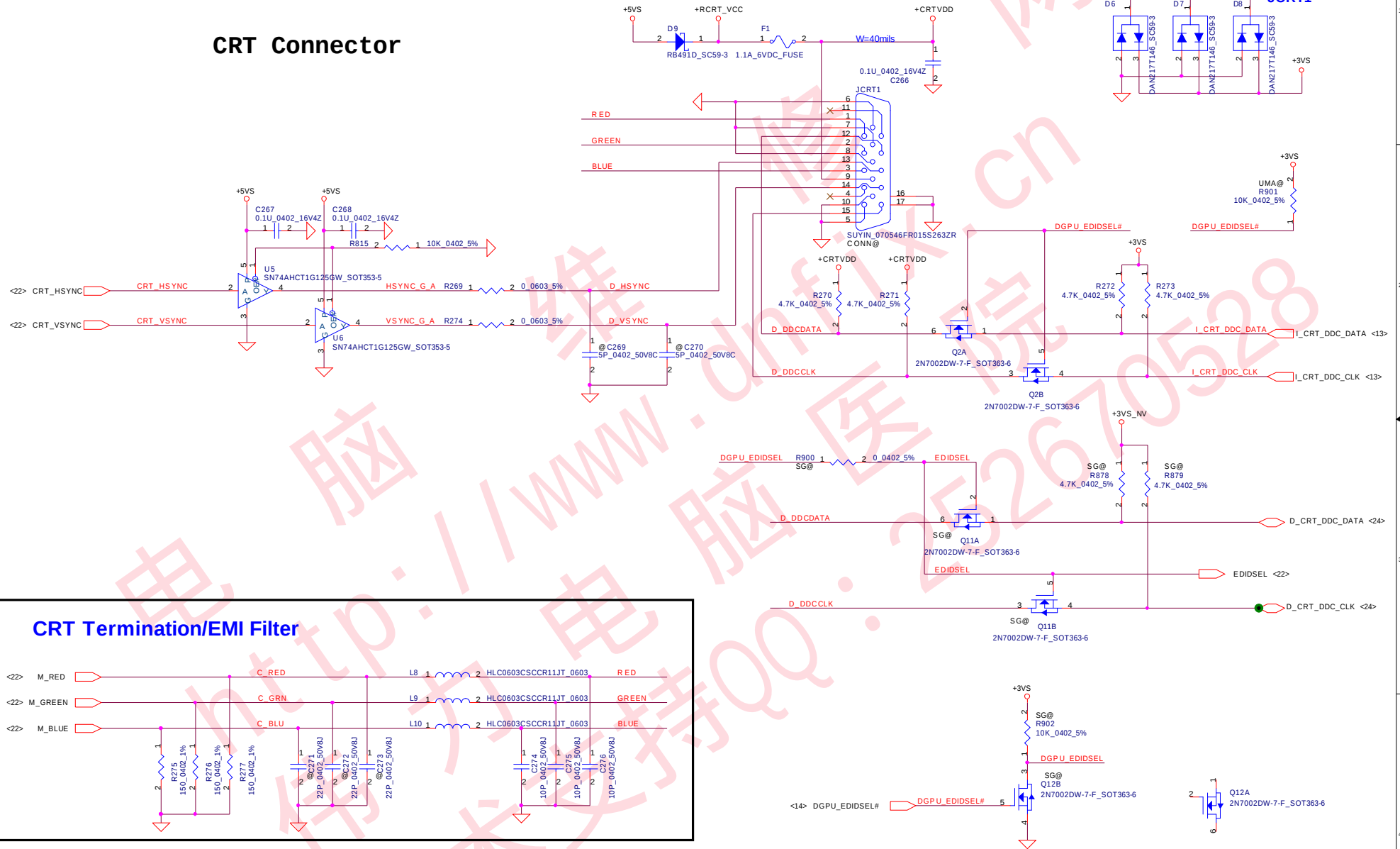




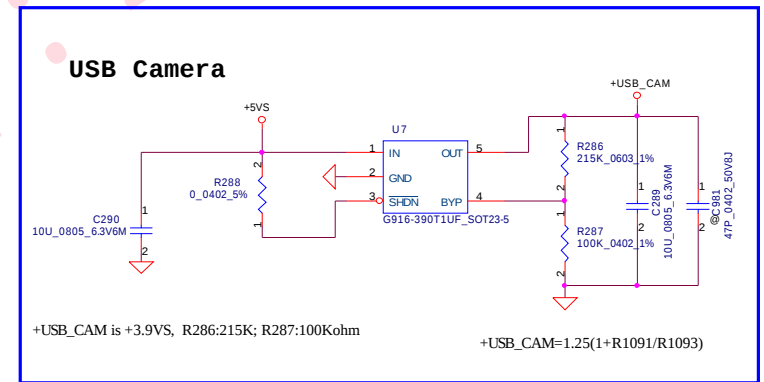
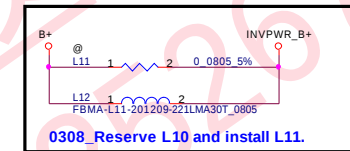
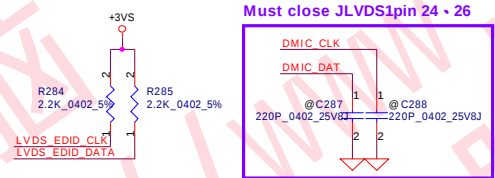
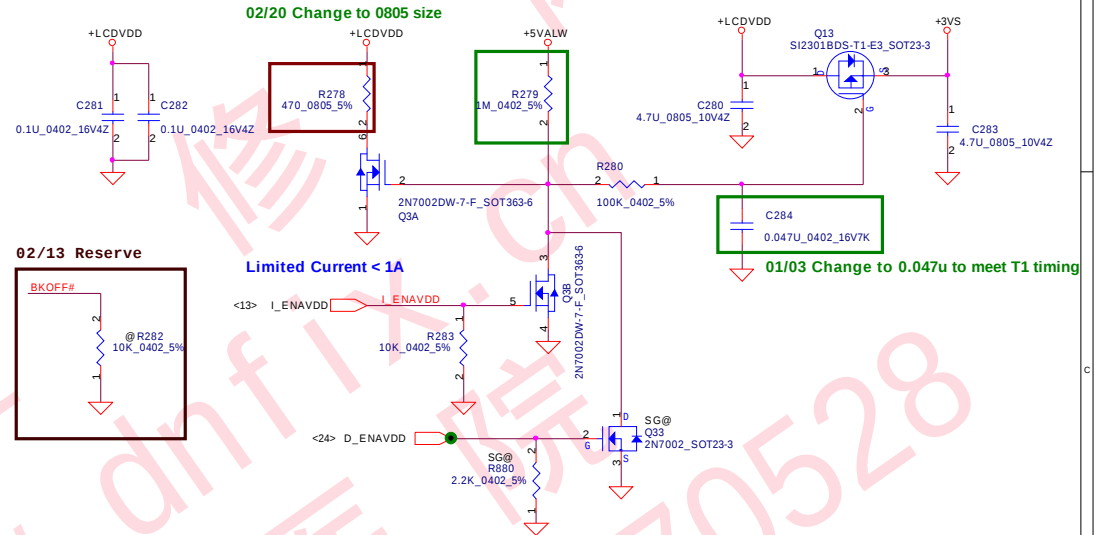
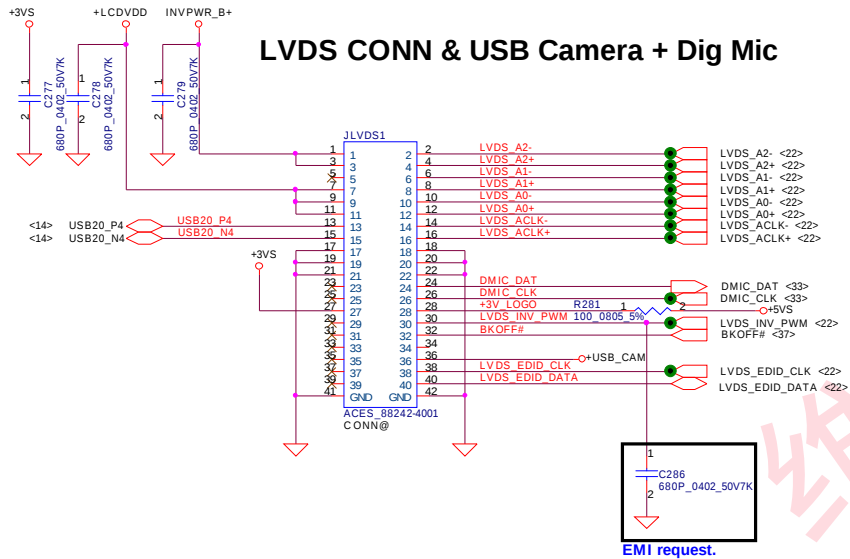
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CRT Connector

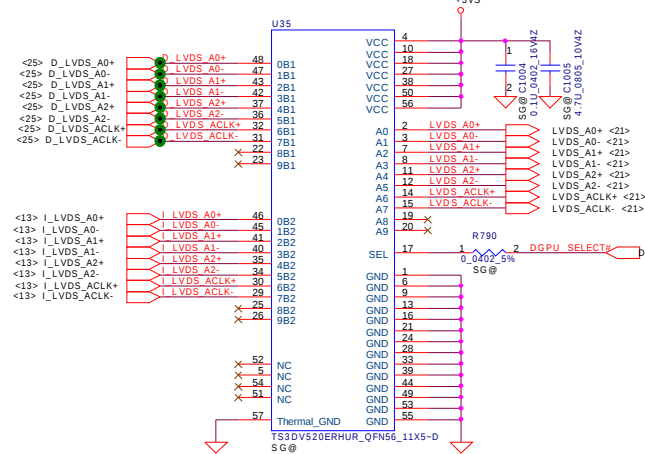


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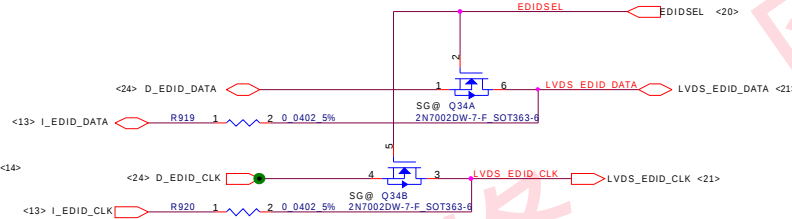


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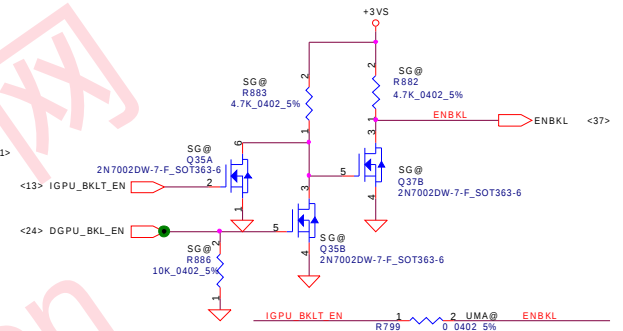
LVDS Switch



LVDS I2C switch



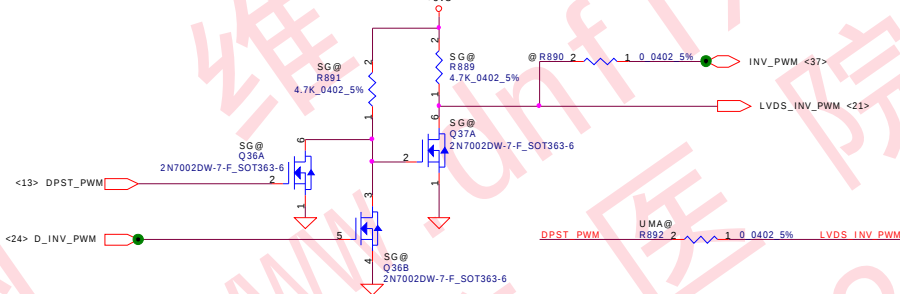
Backlight Enable



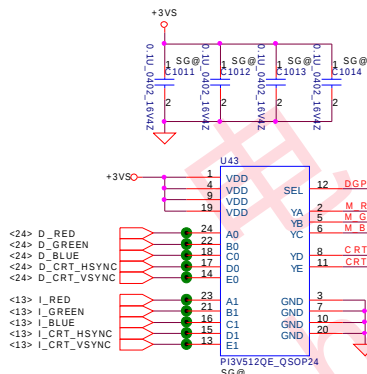
UMA ONLY (LVDS)

I LVDS A0-	RP36 4	1	LVDS A0-
I LVDS A0+	RP36 3	2	LVDS A0+
I LVDS A1-	RP37 4	1	LVDS A1-
I LVDS A1+	RP37 3	2	LVDS A1+
I LVDS A2-	RP38 4	1	LVDS A2-
I LVDS A2+	RP38 3	2	LVDS A2+
I LVDS ACLK-	RP39 4	1	LVDS ACLK-
I LVDS ACLK+	RP39 3	2	LVDS ACLK+

LVDS PWM switch



CRT Switch

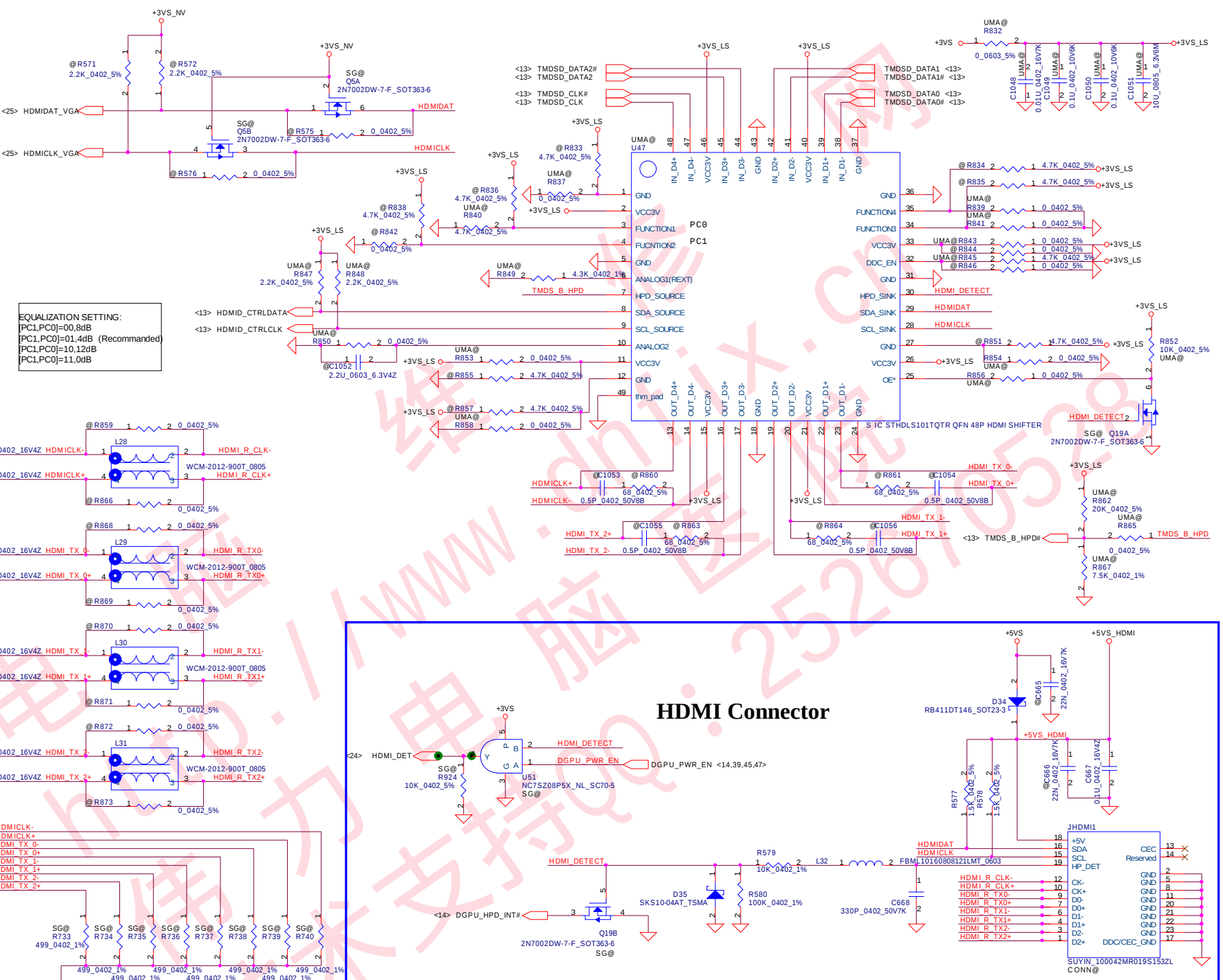


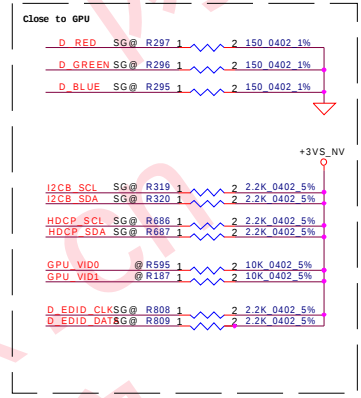
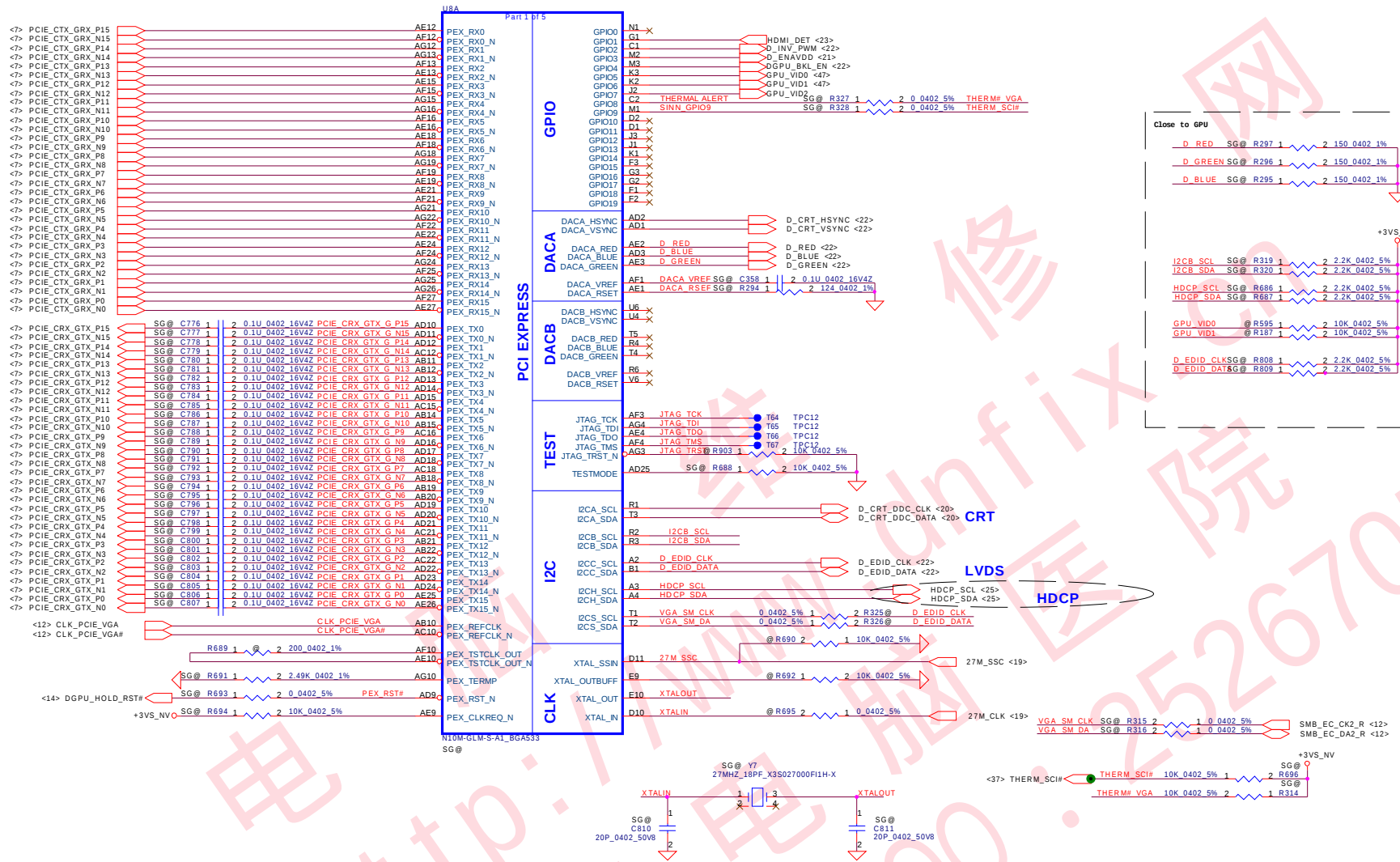
UMA ONLY (CRT)

I RED	R893 2	UMA@ 1 0.0402 5%	M RED
I GREEN	R894 2	UMA@ 1 0.0402 5%	M GREEN
I BLUE	R895 2	UMA@ 1 0.0402 5%	M BLUE
I CRT_HSYNC	R896 2	UMA@ 1 0.0402 5%	CRT_HSYNC
I CRT_VSYNC	R897 2	UMA@ 1 0.0402 5%	CRT_VSYNC

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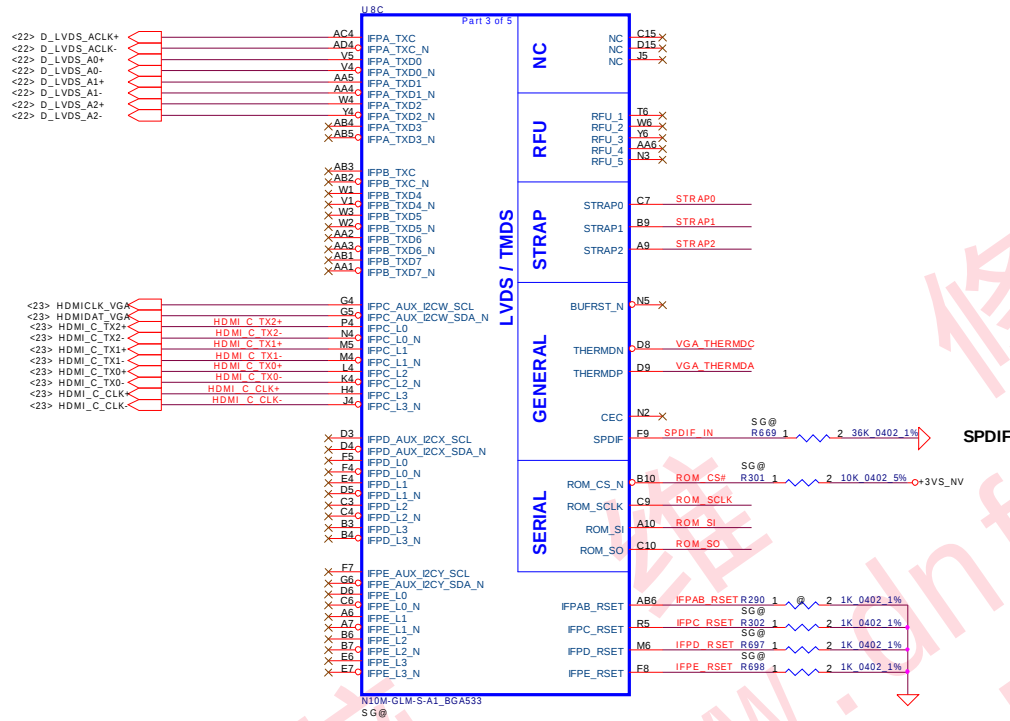
	ST	Parade 81011	Parade 8171
R833	X	X	X
R837	0 ohm	0 ohm	4.7K ohm
R836	X	4.7K ohm	X
R840	4.7K ohm	X	4.7K ohm
R838	X	X	4.7K ohm
R842	X	X	X
R849	3.9K ohm	499 ohm	499 ohm
R850	0 ohm	X	X
C1052	X	X	2.2uF
R853	0 ohm	0 ohm	X
R855	X	X	4.7K ohm
R857	X	X	4.7K ohm
R858	0 ohm	0 ohm	X
R851	X	X	4.7K ohm
R854	0 ohm	0 ohm	X
R843	0 ohm	0 ohm	X
R844	X	X	4.7K ohm
R839	0 ohm	X	4.7K ohm
R834	X	X	X
R841	0 ohm	X	X
R835	X	X	4.7K ohm
C667	0.1uF	1uF	1uF
R862	V	X	X
R867	V	X	X



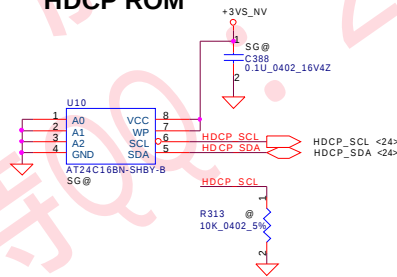


GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	HPD-C (used for IFPC)
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	NVDD VID2
GPIO8	IN	L	OVERT
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT	N/A	MEM_VREF
GPIO11	OUT	L	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	MEM_VID
GPIO14	OUT	H	PS Control
GPIO15	IN	N/A	HPD-E (used for IFPE)
GPIO16	OUT	N/A	FAN PWM Control
GPIO17		N/A	
GPIO18		N/A	
GPIO19	IN	N/A	HPD-D (used for IFPD)

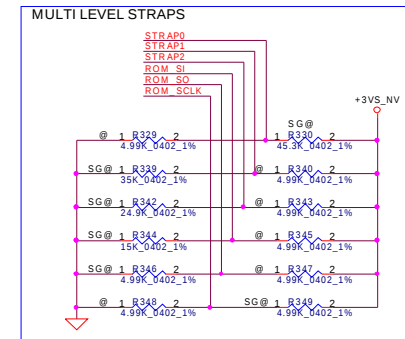
LVDS Interface



HDCP ROM

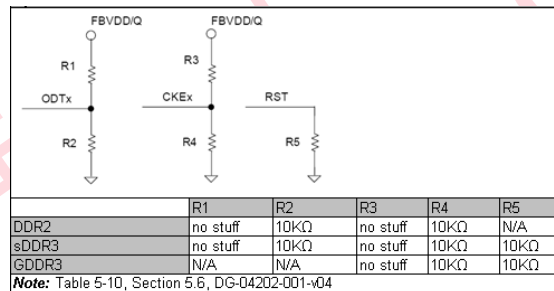
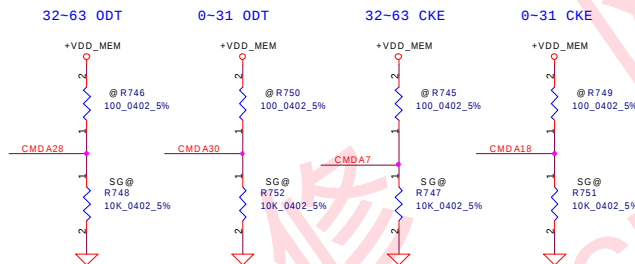
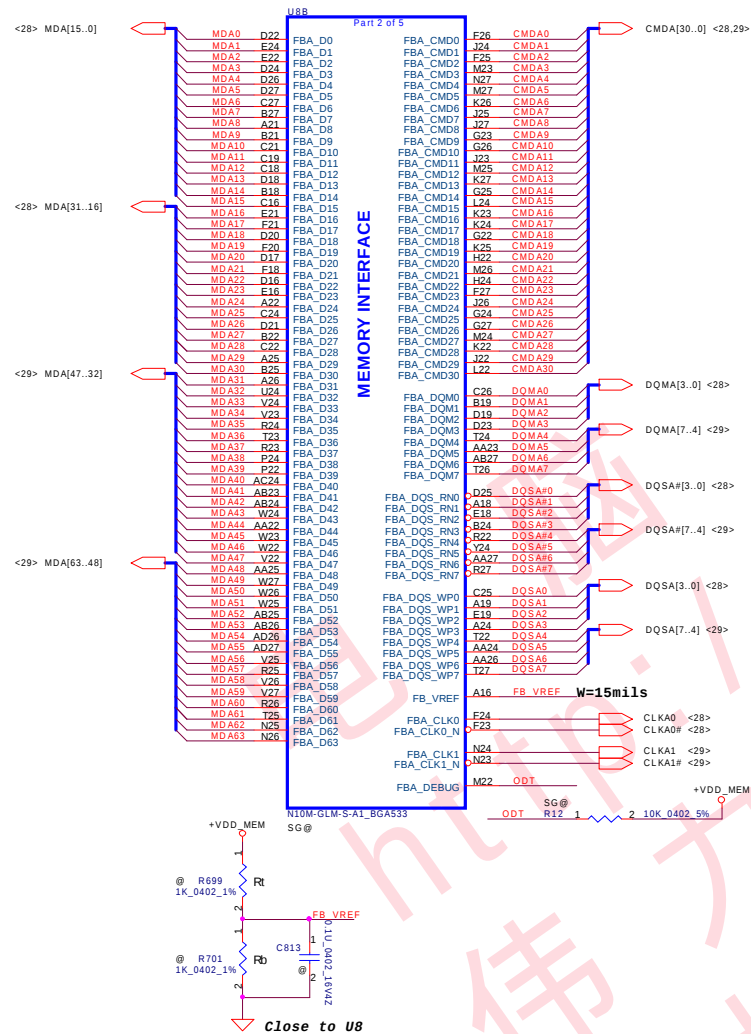


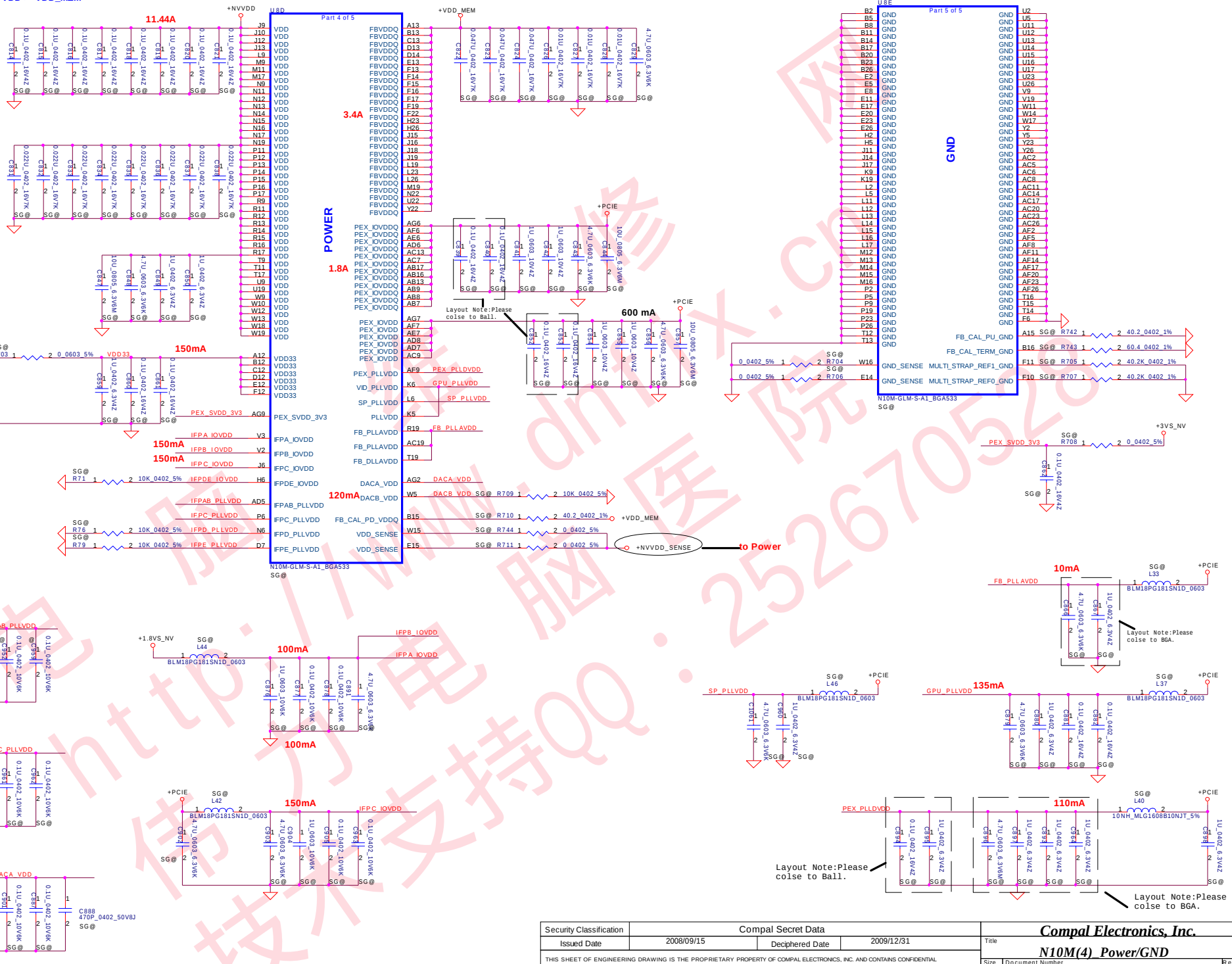
Straps



FB HW Strap for DDR3: (RAM_CFG @ROM_SI)
Hynix 64Mx16: 0000 (R344 pull-down 15K)
Samsung 64Mx16: 0001 (R344 pull-down 20K)

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2009/12/31	N10M(2) LVDS&DP&HDCP	
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				Custom	Calpella DIS LA4743P
				Date	Monday, April 13, 2009
				Sheet	25 of 49
				Rev	0.1





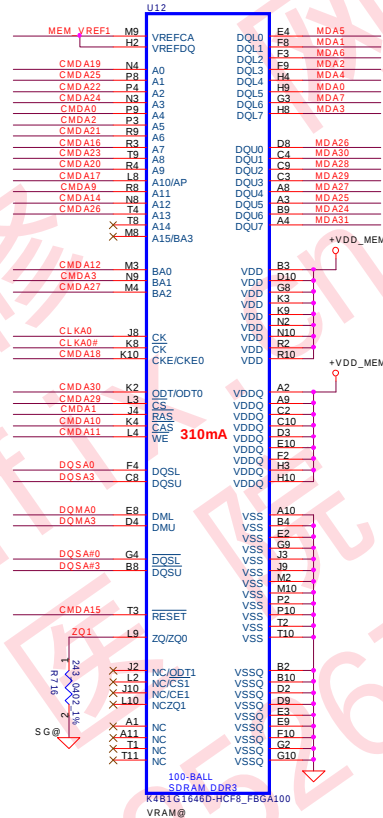
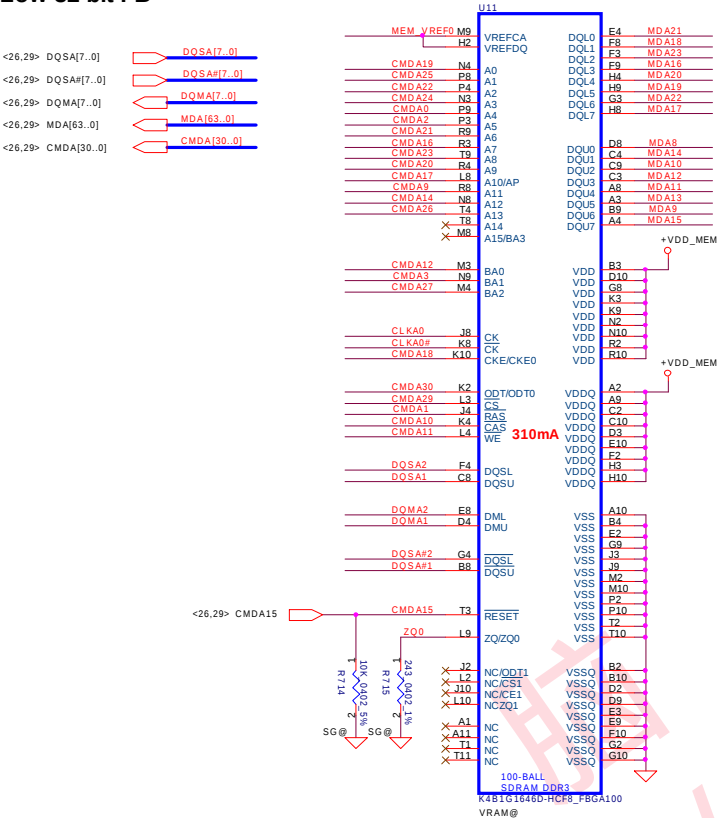
Security Classification		Compal Secret Data		Compal Electronics, Inc. N10M(4) Power/GND	
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	
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				Customer	0.1
				Document Number Capella D1S LA4743P	
Date:		Monday, April 13, 2009		Sheet	27 of 49

VRAM DDR3 chips (512MB)

64Mx16 DDR3 700MHz*4==>512MB

Low 32 bit FB

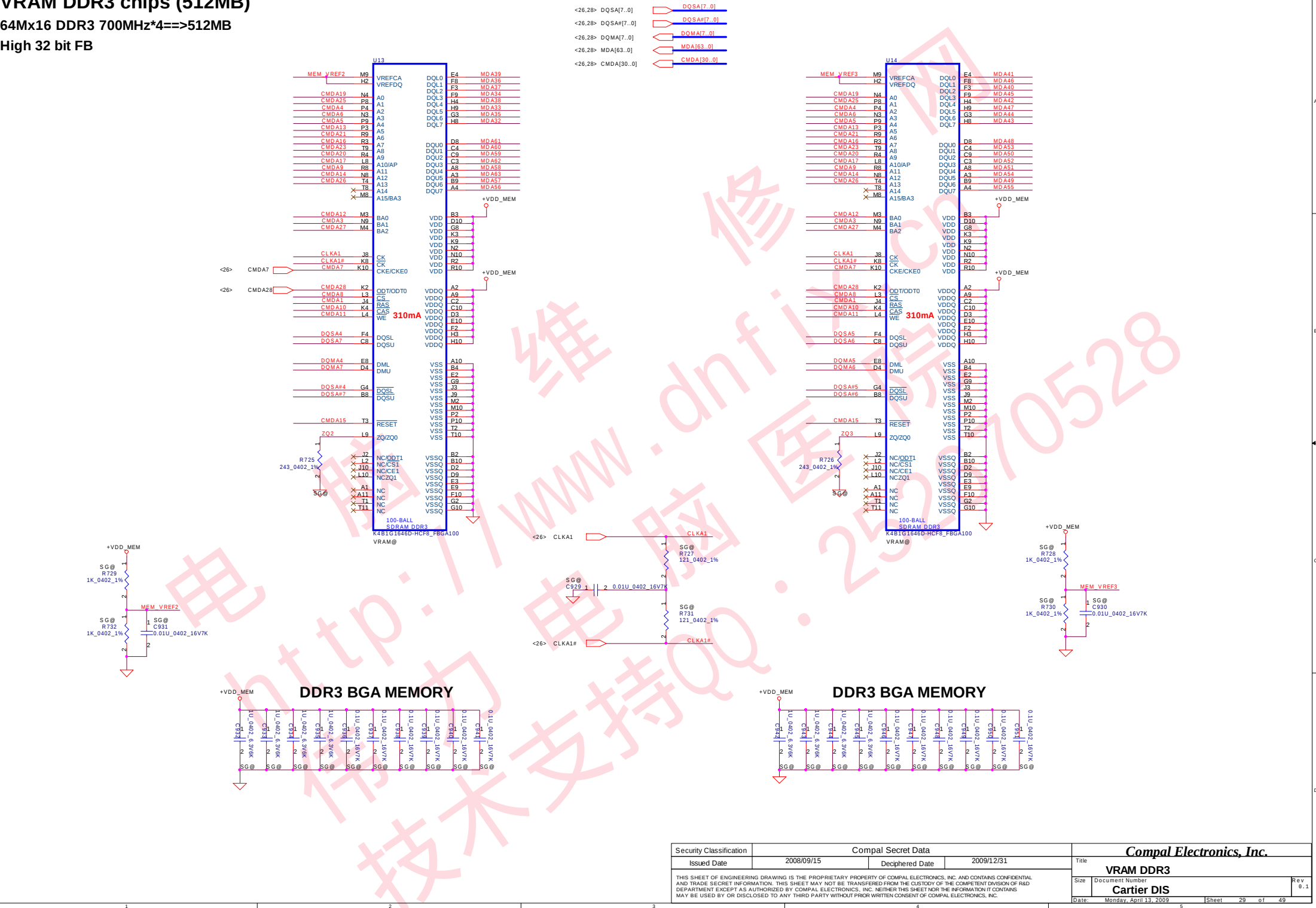
Hynix : H5TQ1G63BFR-12C-->SA000032400
Samsung : K4W1G1646E-HC12-->SA000035700



DATA Bus		
Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	ODT	
CMD29	CS#	
CMD30		
LOW HIGH		

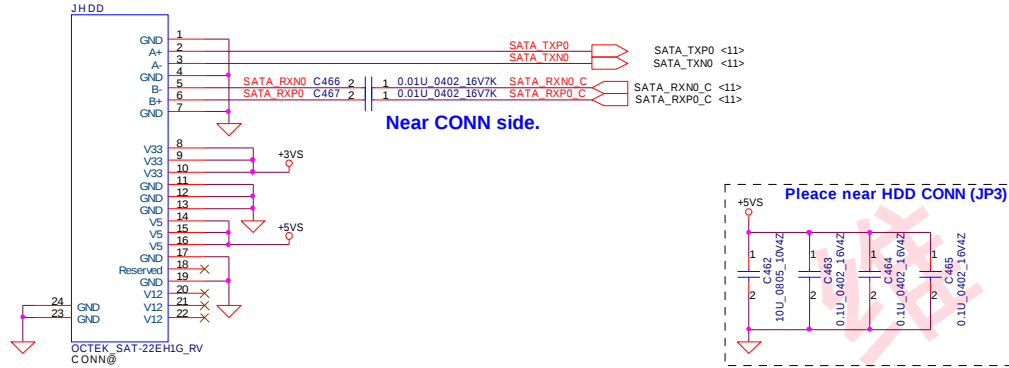


VRAM DDR3 chips (512MB)
64Mx16 DDR3 700MHz*4==>512MB
High 32 bit FB

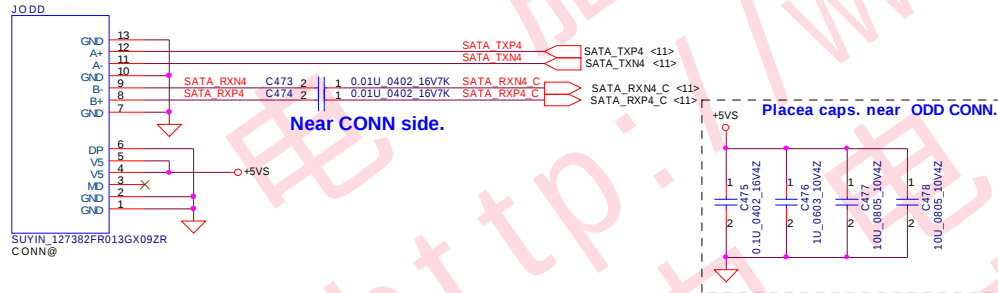


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Issued Date		2008/09/15	Deciphered Date	2009/12/31		Title			
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						Size	Document Number		Rev
						Cartier DIS			0.1
						Date	Monday, April 13, 2009		Sheet

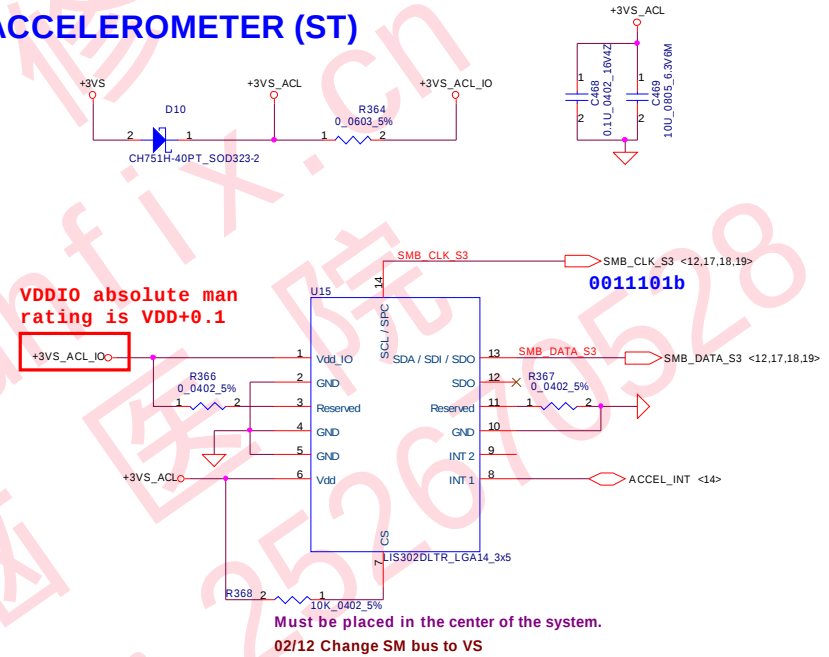
HDD Connector



CD-ROM Connector

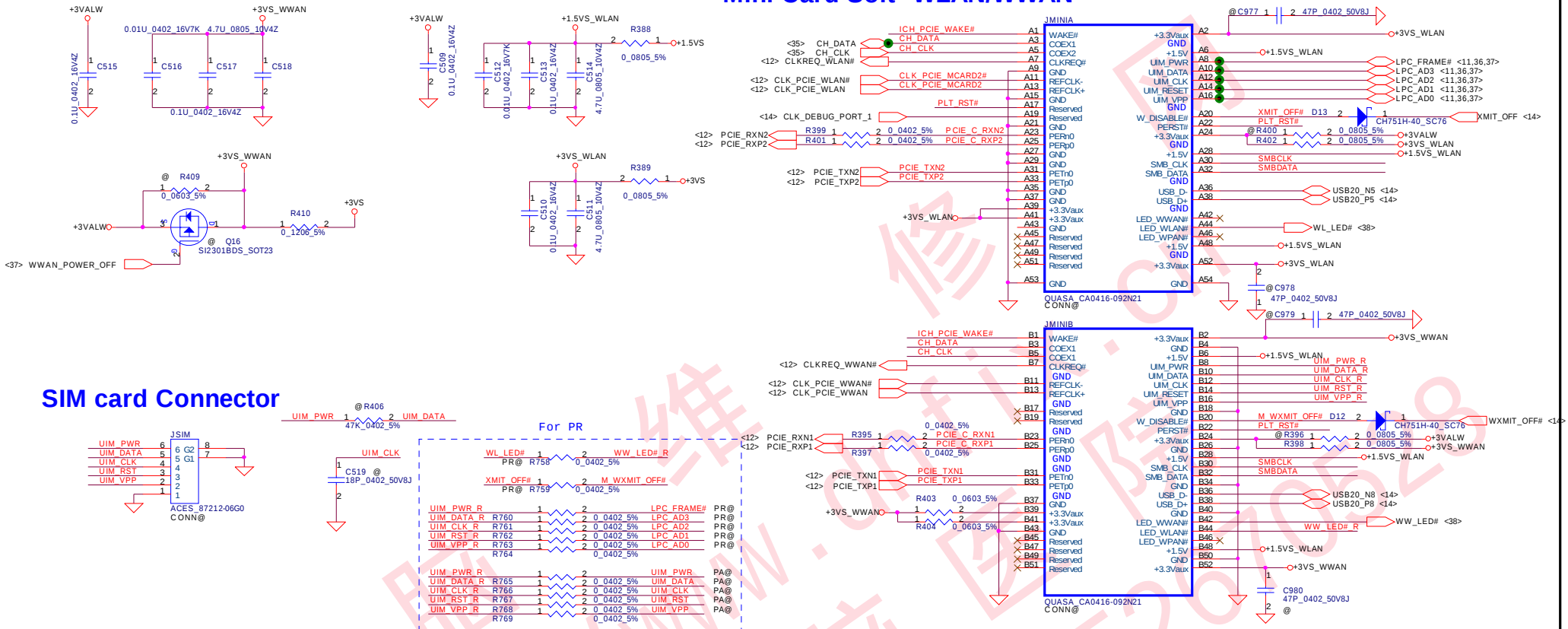


ACCELEROMETER (ST)

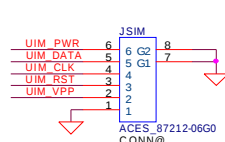


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	HDD & CDROM
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Date	Monday, April 13, 2009	Sheet	30	of	49

Mini Card Solt--WLAN/WWAN

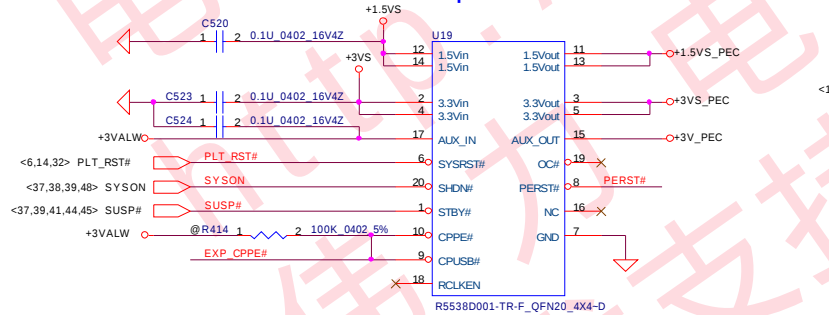


SIM card Connector



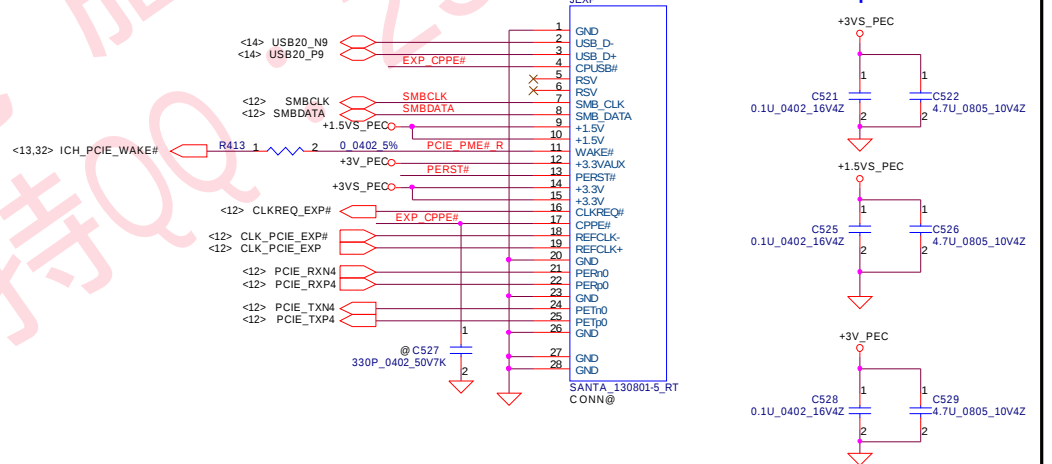
New Card

Express Card Power Switch

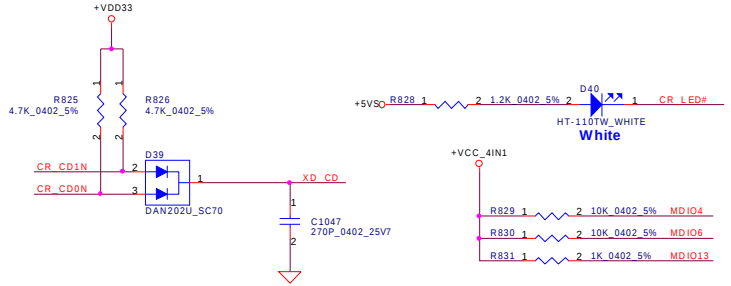
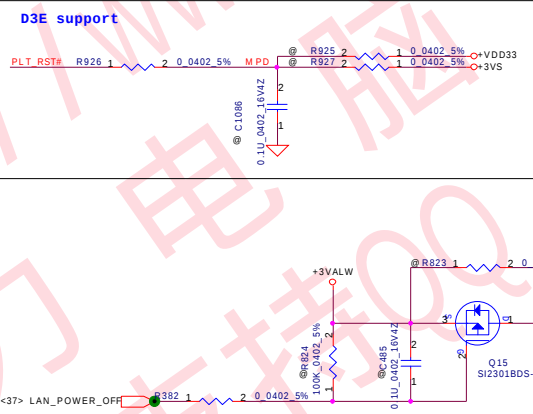
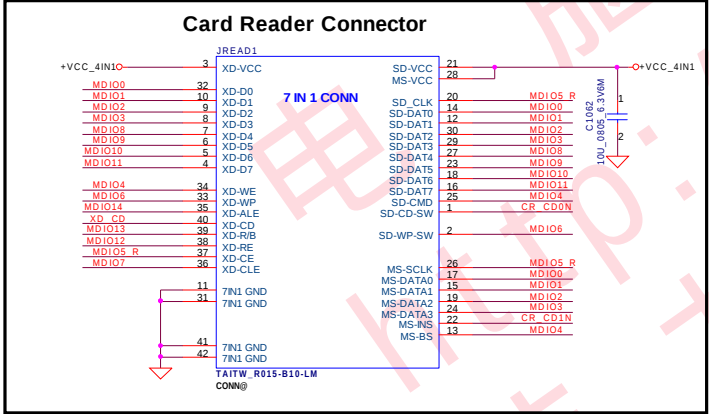
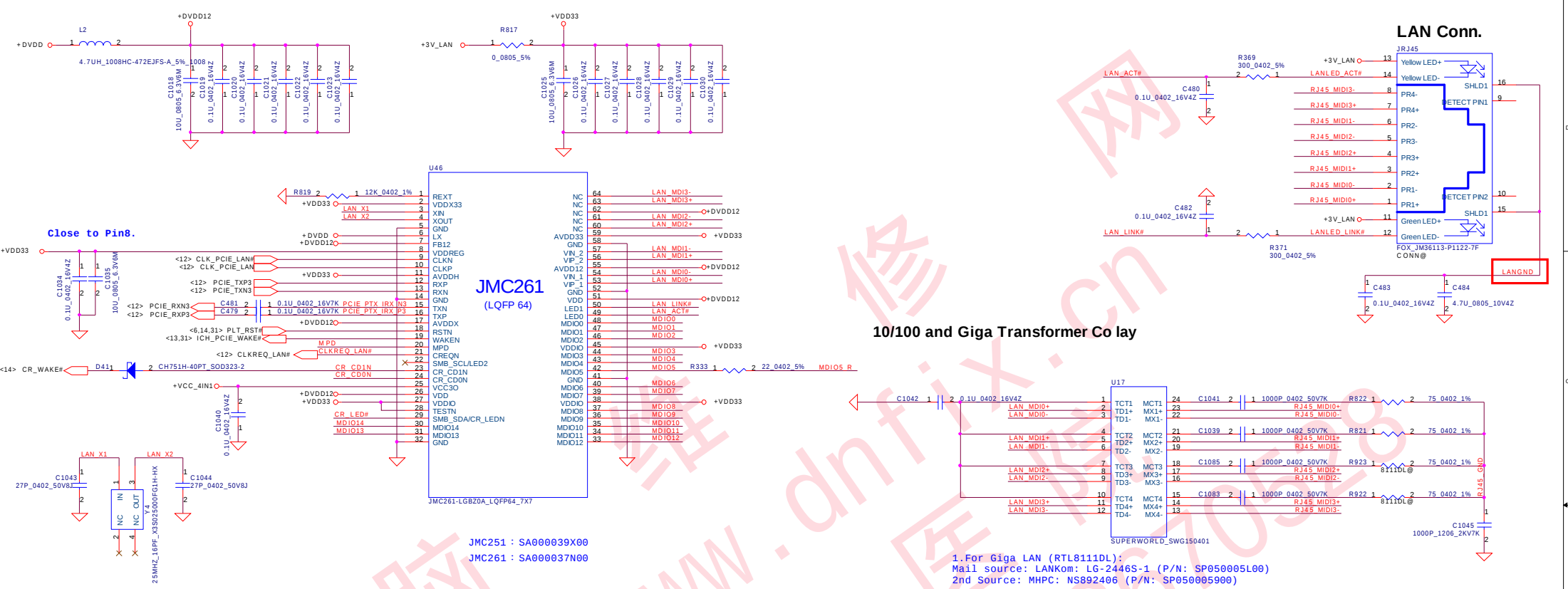


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

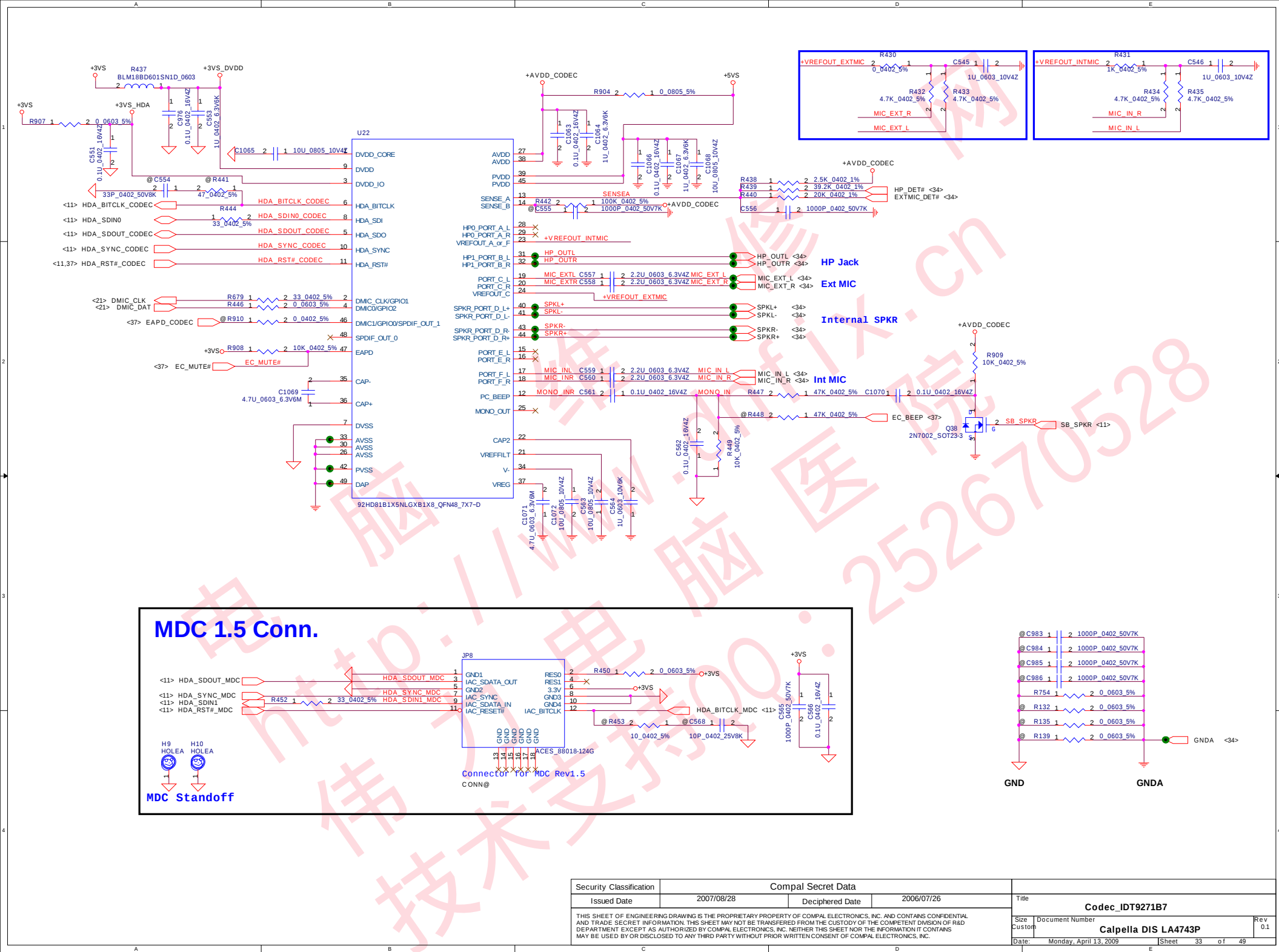
Near to Express Card slot.



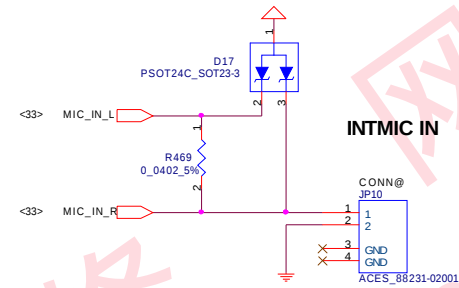
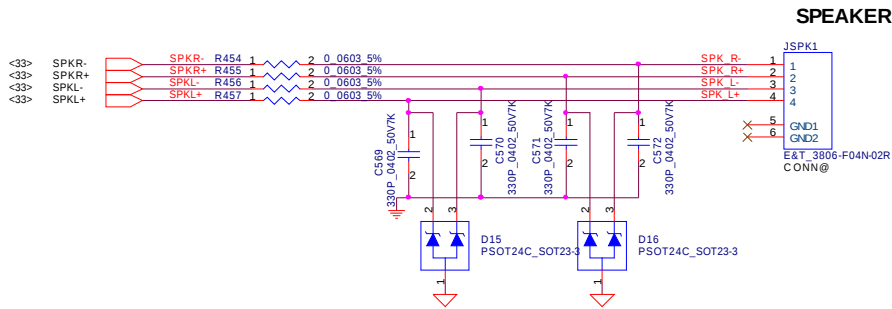
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	WLAN, WWAN, New Card	
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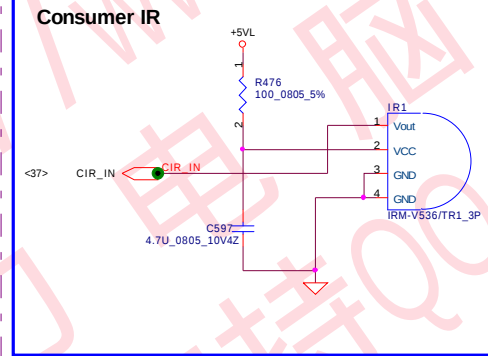
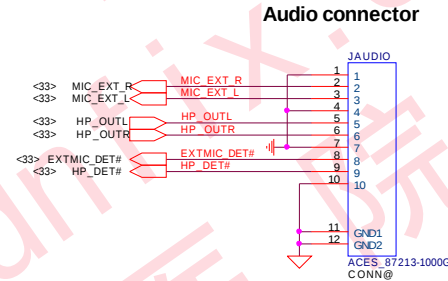
Security Classification	Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date		
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Date		Monday, April 13, 2009		Sheet	33 of 49

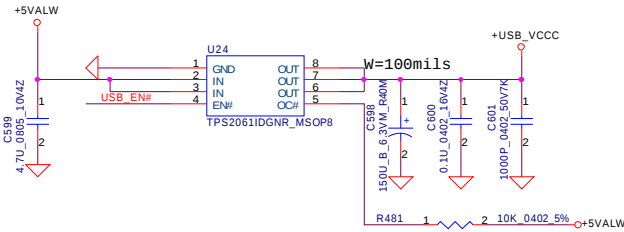


Add JSPK2 for PA

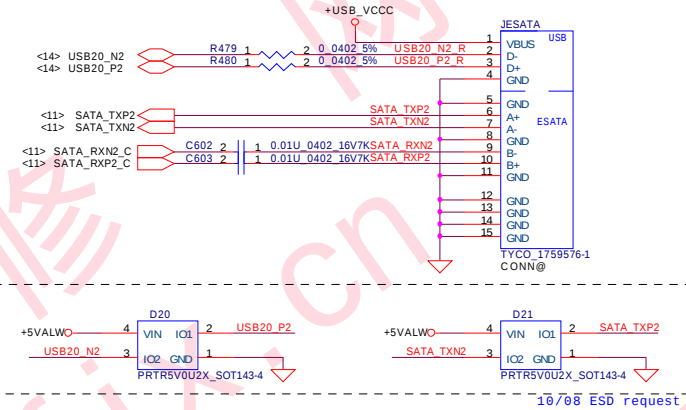


Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	AMP & Audio Jack	
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				Date Monday, April 13, 2009	Rev 0.1
				Sheet 34 of 49	

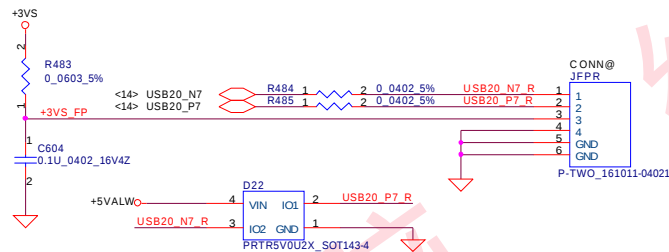
Right side USB Power Switch



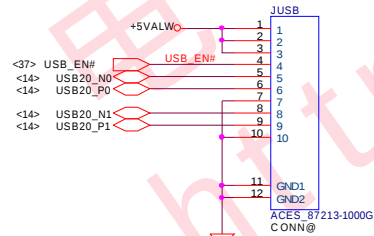
Right side ESATA/USB combination Connector



Finger printer

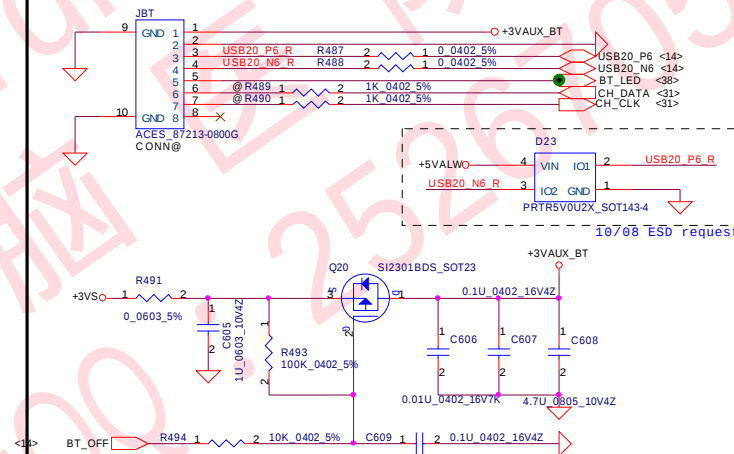


USB cable connector for Left side



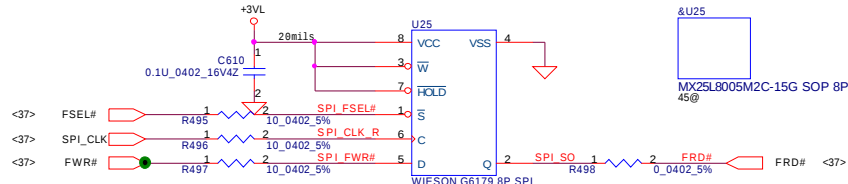
BT Connector

Need change to New version



Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	USB, BT, eSATA	
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SPI ROM => 1M (EC code)



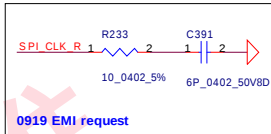
SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P

SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P (MXIC)

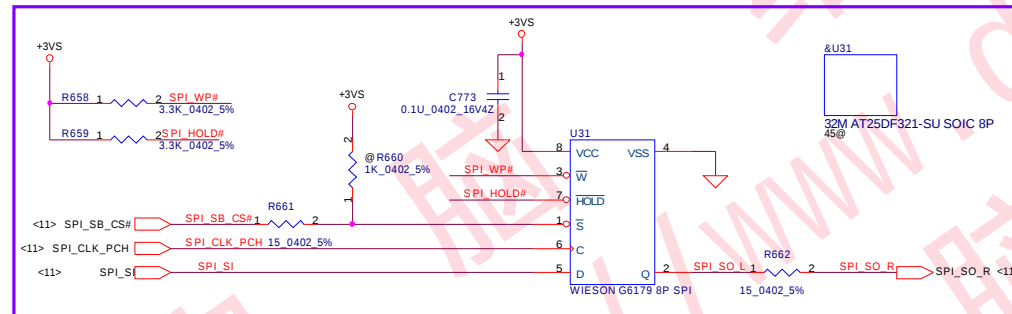
SA00001AW00 : S IC FL 16M MX25L1605AM2C-15G SOP 8P SPI (MXIC)

SA000021A00 : S IC FL 32M MX25L3205DM2I-12G SOP 8P (MXIC)

SA000031Q00 : S IC FL 32M AT25DF321-SU SOIC 8P (ATMEL)

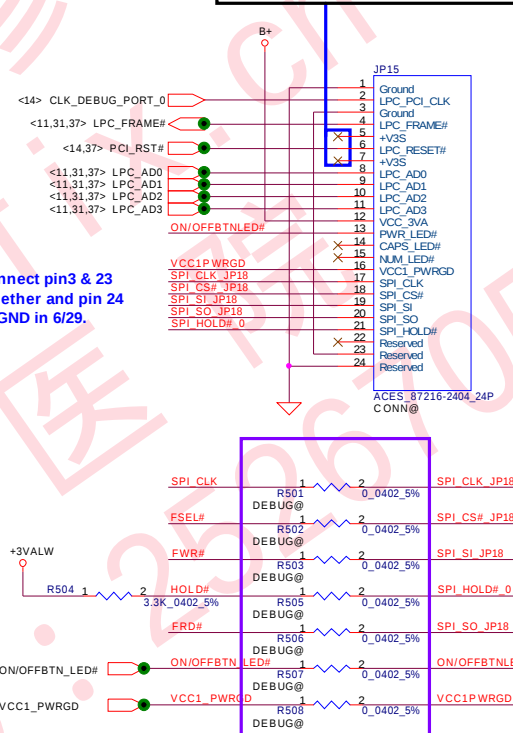


SPI ROM on PCH => 4M (ME code + System BIOS)



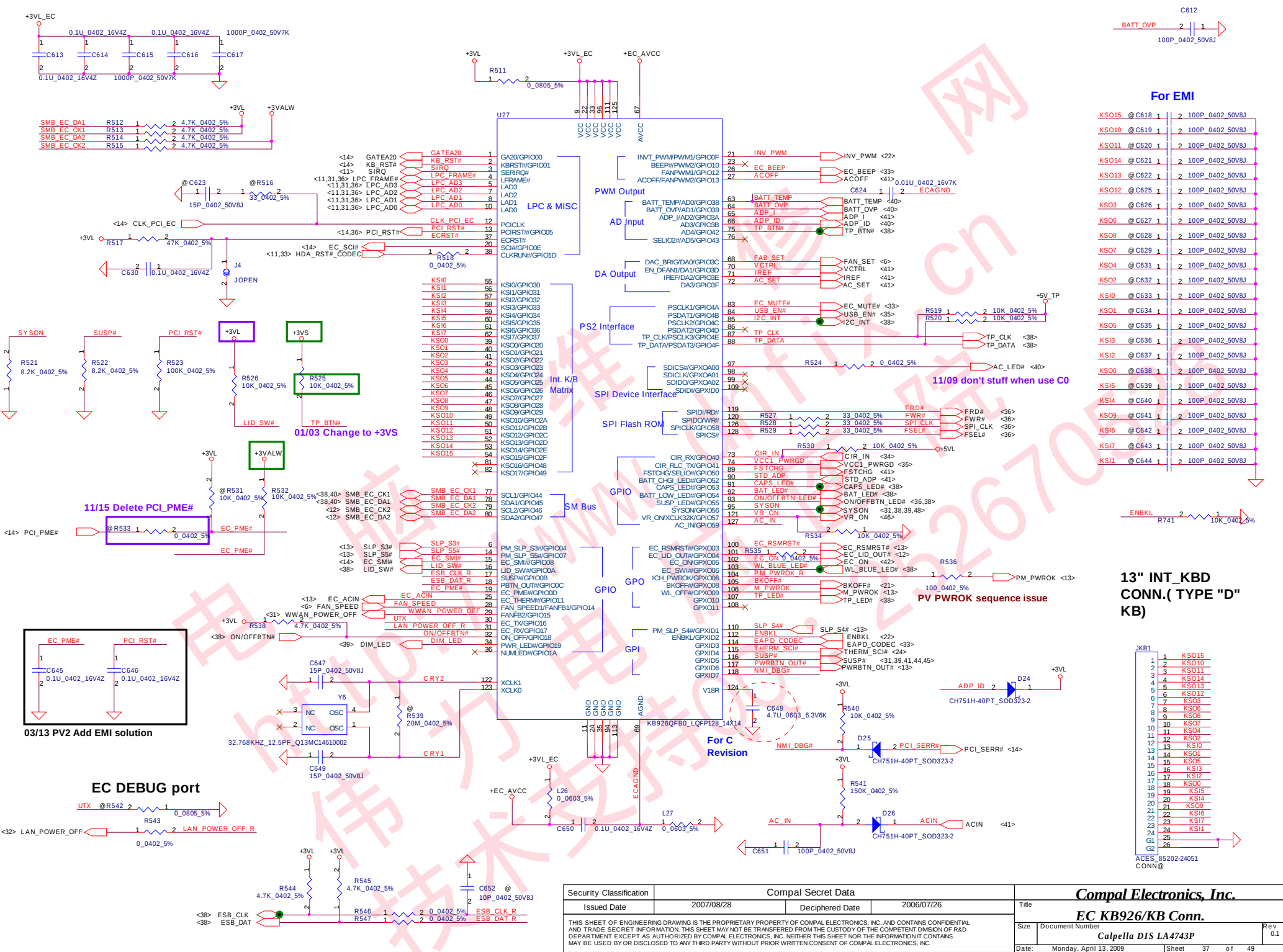
LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



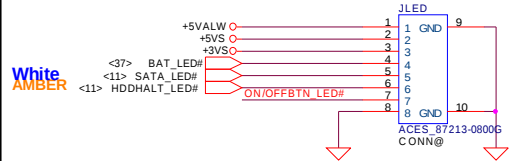
11/07 Add 0 Ohm for debug port

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				Date	Monday, April 13, 2009
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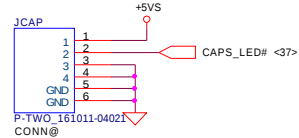


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Issued Date	2007/08/28	Deciphered Date	2006/07/26	EC KB926/KB Conn.	
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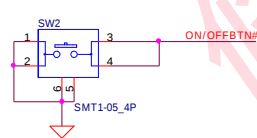
System LED Conn



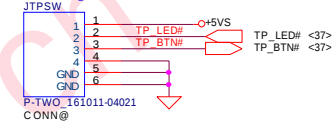
Caps-Lock Conn



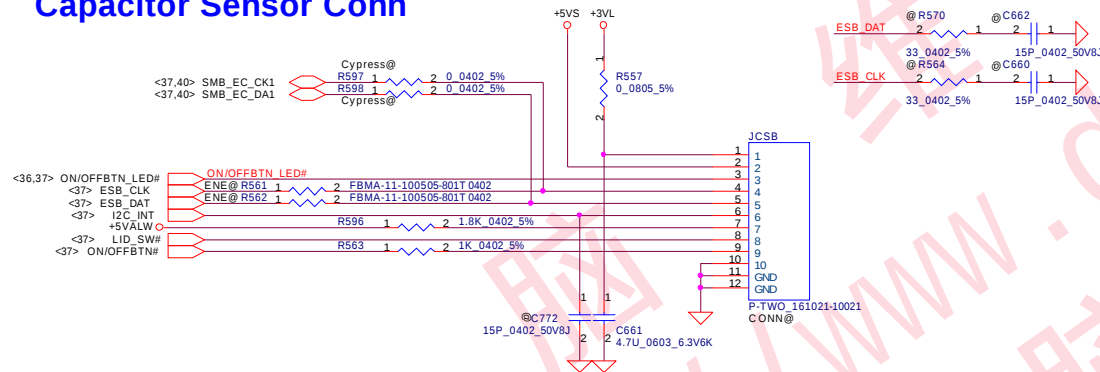
Power Button for debug only



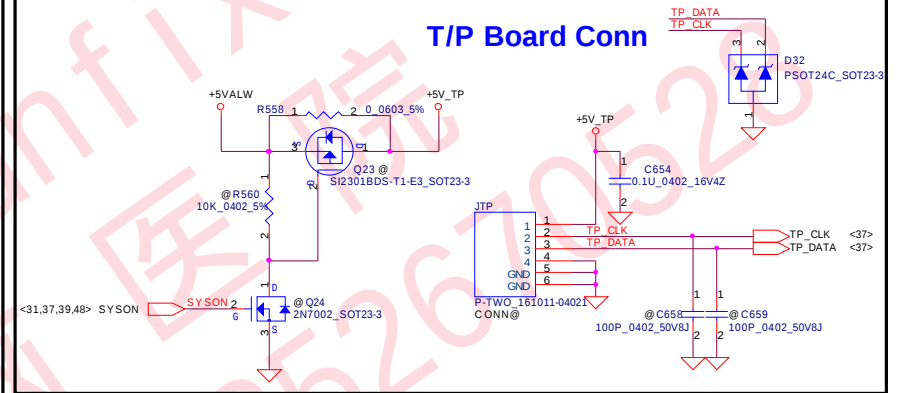
T/P Board (Inculde T/P_ON/OFF)



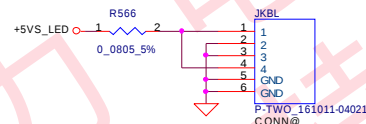
Capacitor Sensor Conn



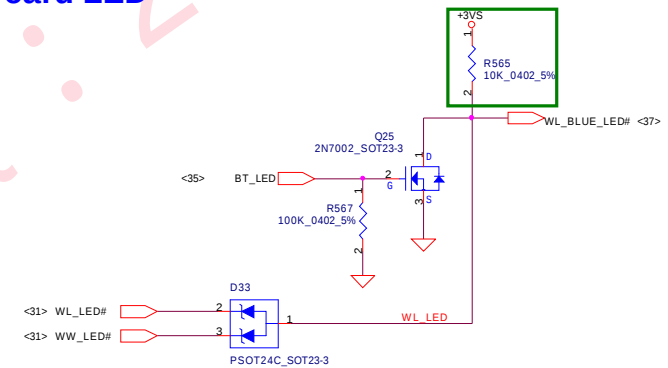
T/P Board Conn



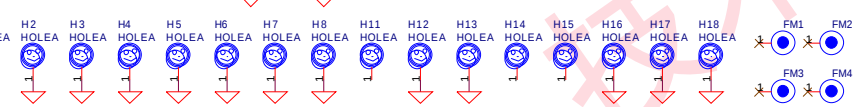
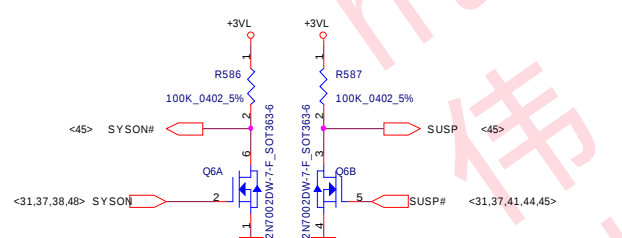
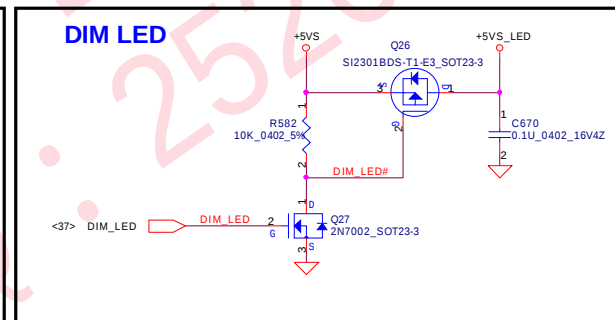
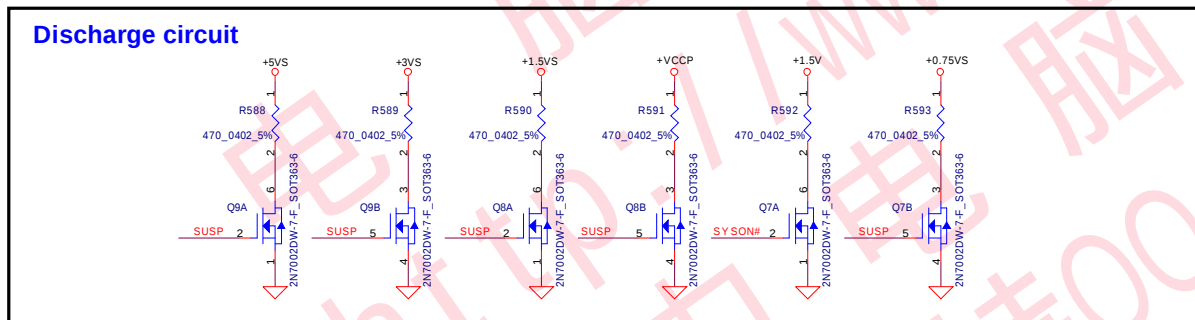
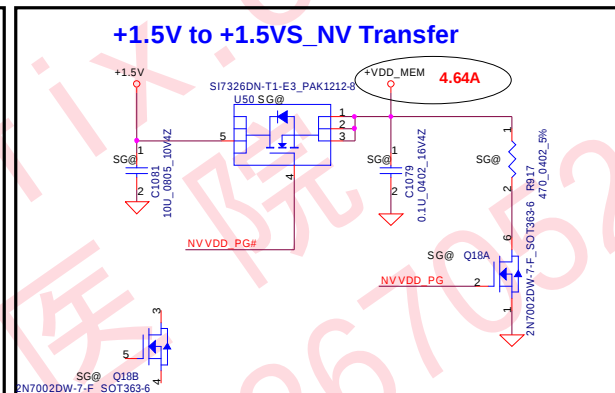
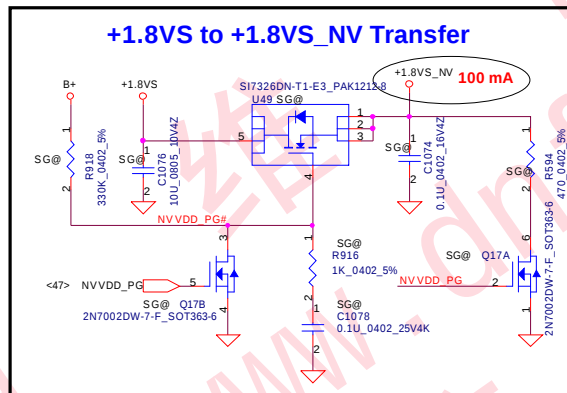
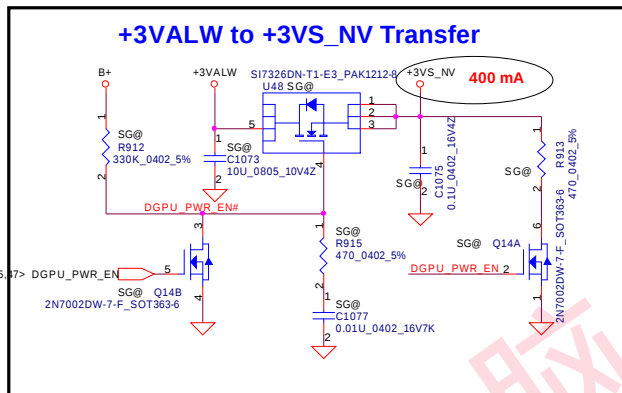
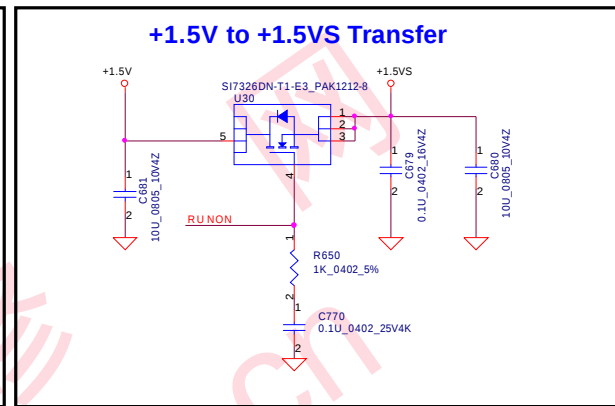
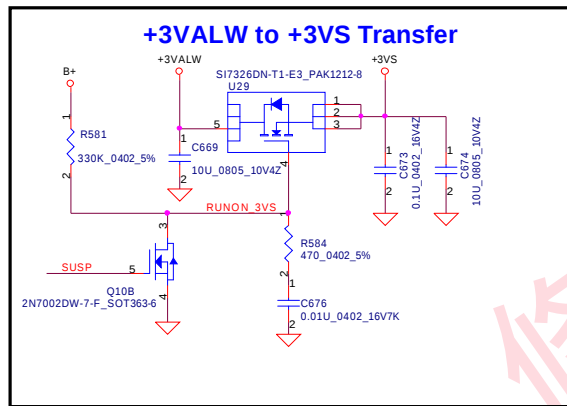
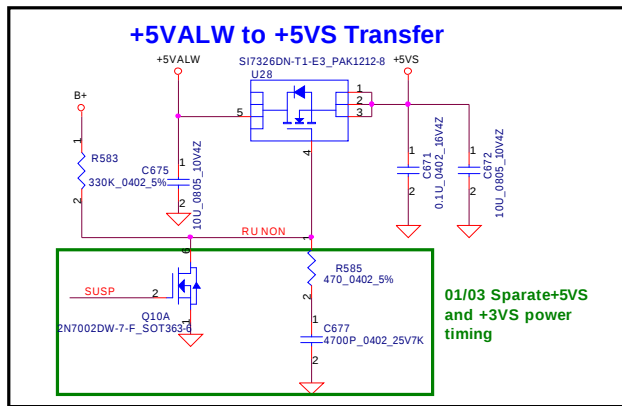
Keyboard backlight Conn



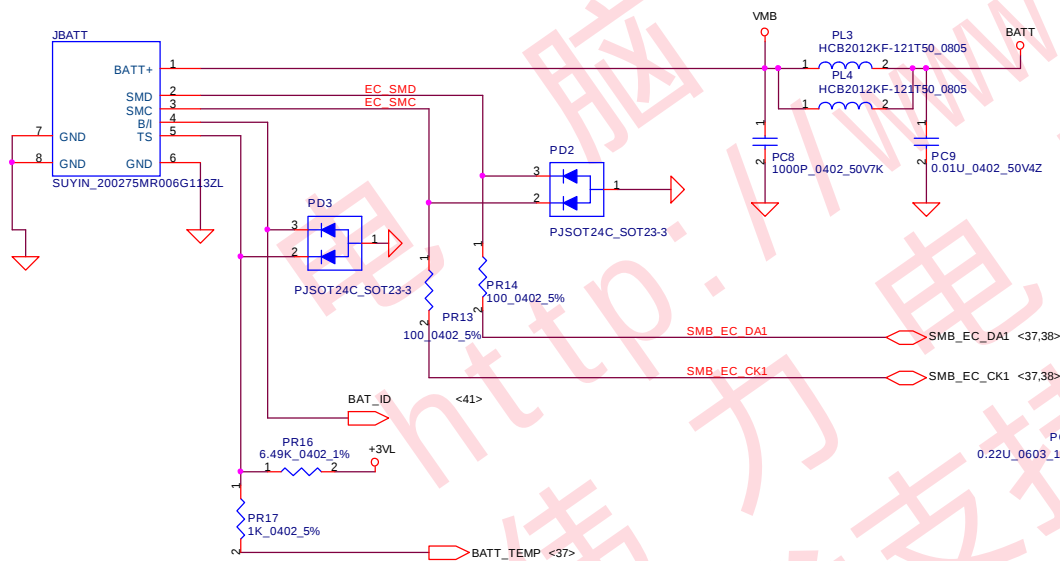
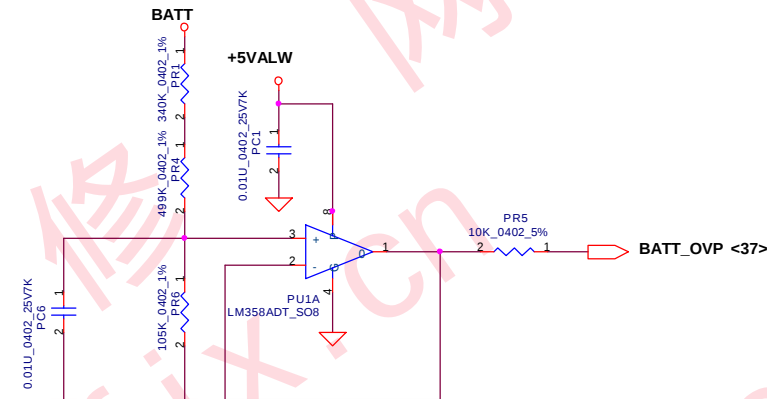
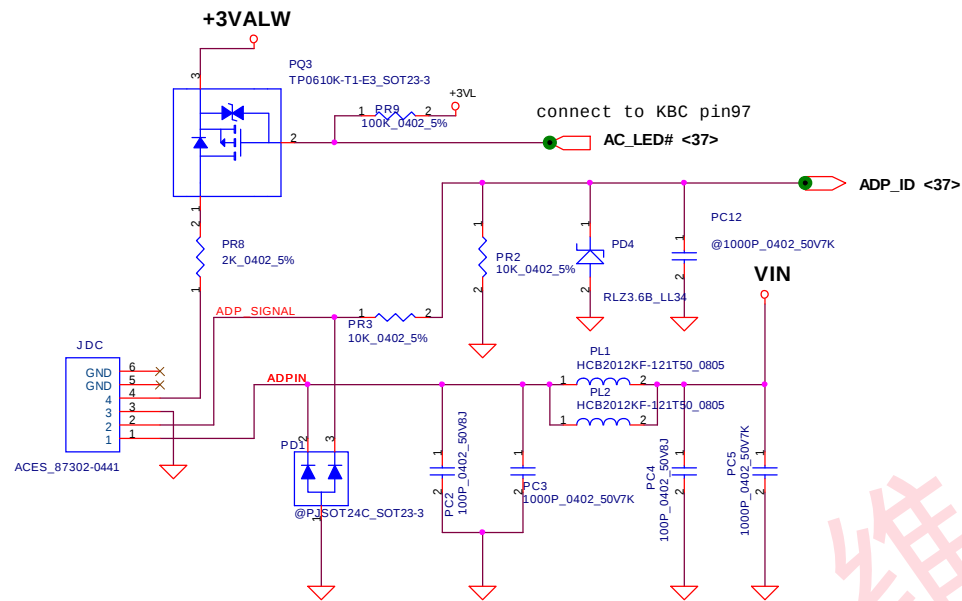
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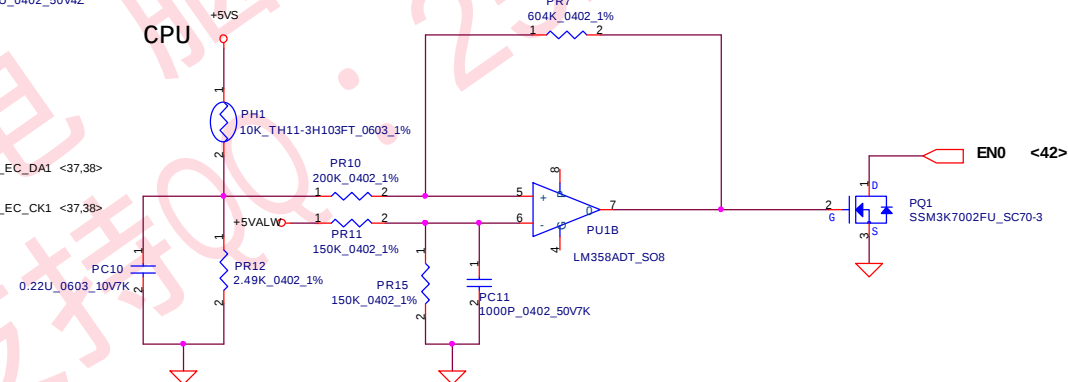
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Issued Date	2007/08/28	Deciphered Date	2006/07/26	Compal Electronics, Inc.	
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				Calpella DIS LA4743P	
Date	Monday, April 13, 2009	Sheet	38	of	49



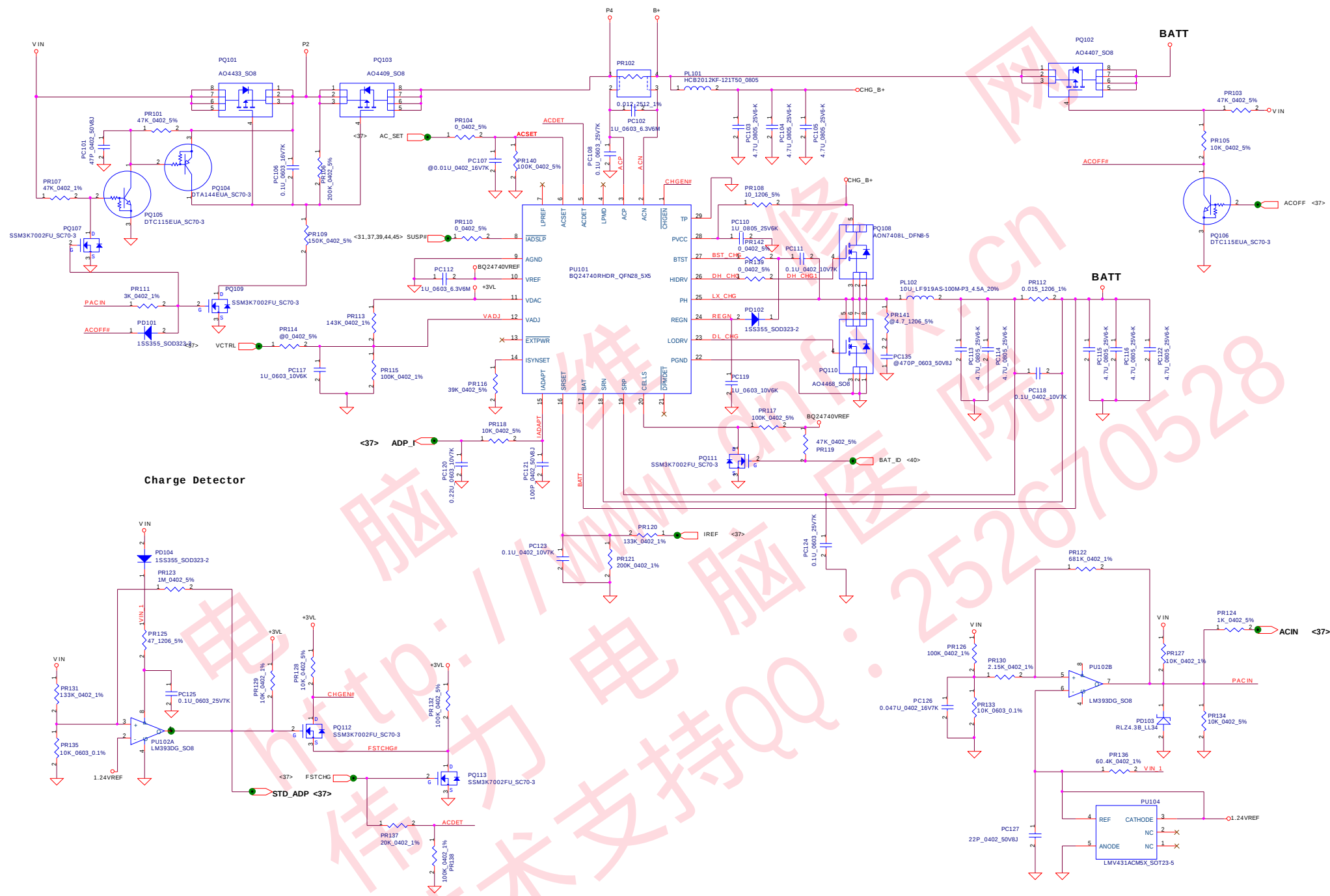
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				Calpella DIS LA4743P	
				Date	Monday, April 13, 2009
				Sheet	39 of 49



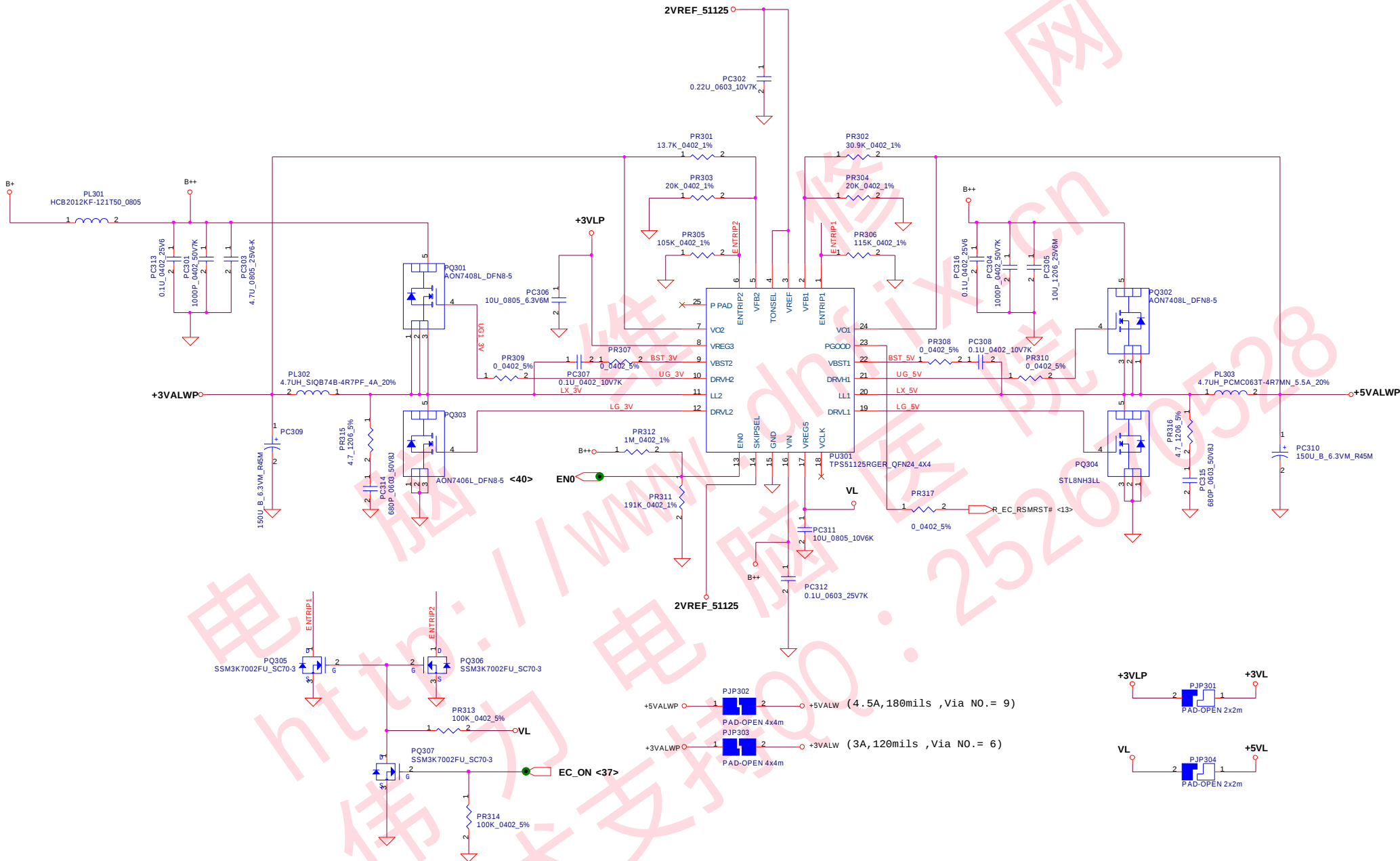
PH1 under CPU bottom side :
CPU thermal protection at 90 + -3 degree C



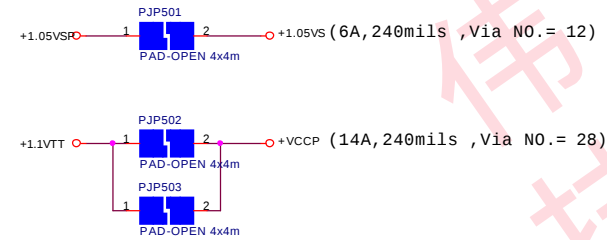
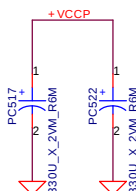
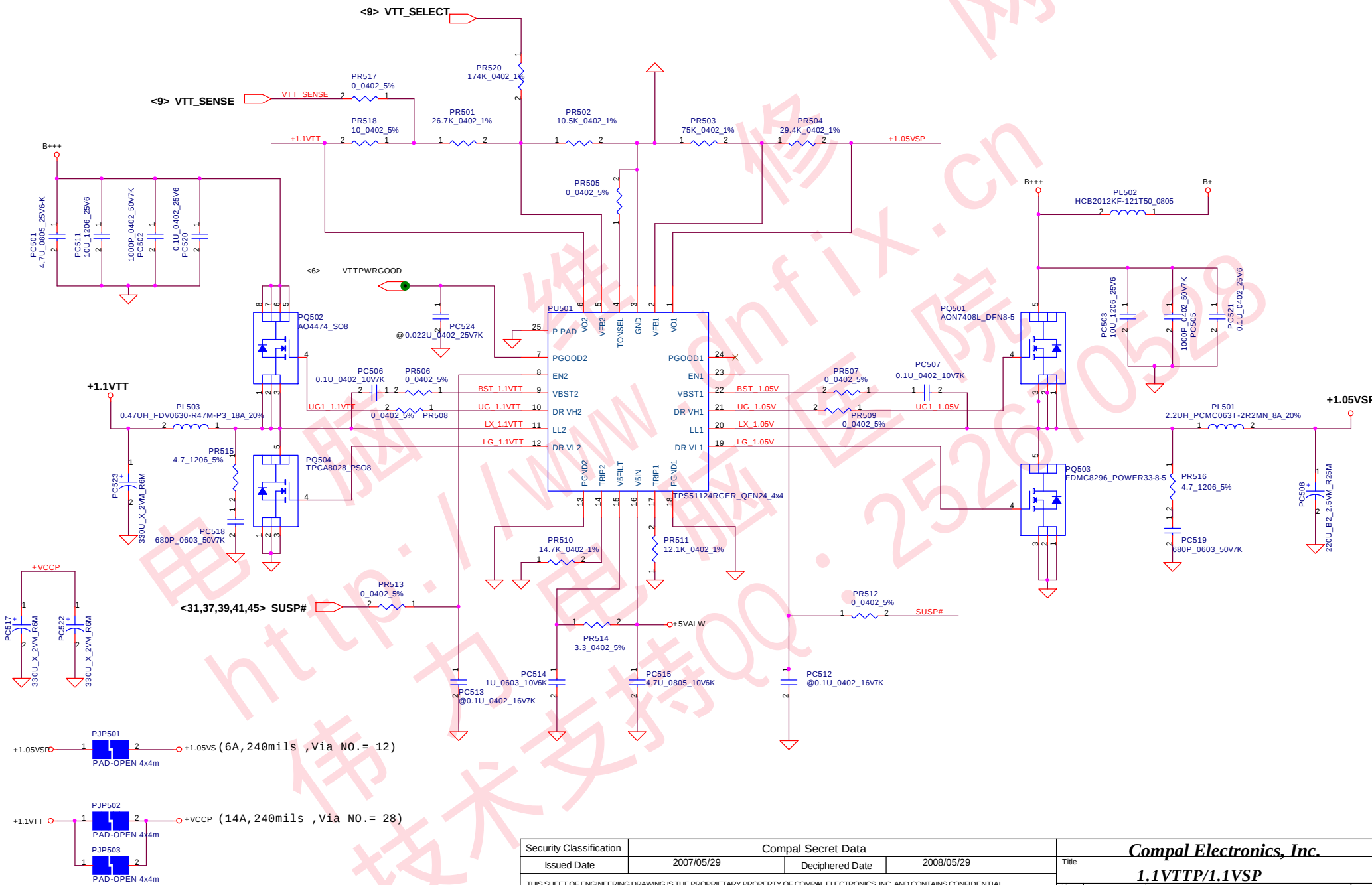
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Size	Document Number	Calpella DIS LA4743P		Rev	0.1
Date:	Monday, April 13, 2009	Sheet	40 of 49		



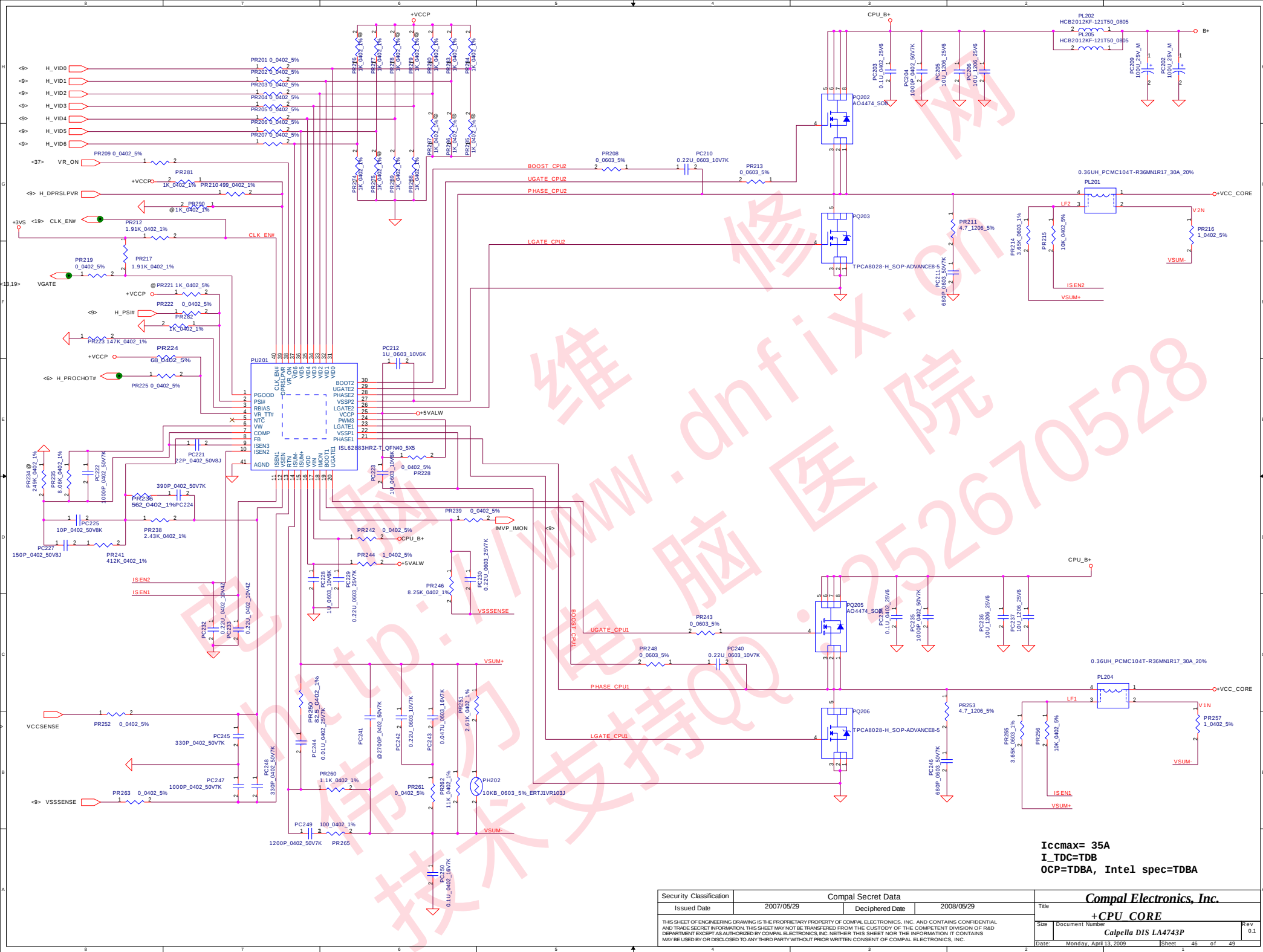
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				Date	Monday, April 13, 2009
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				Date:	Monday, April 13, 2009	Sheet 42 of 49

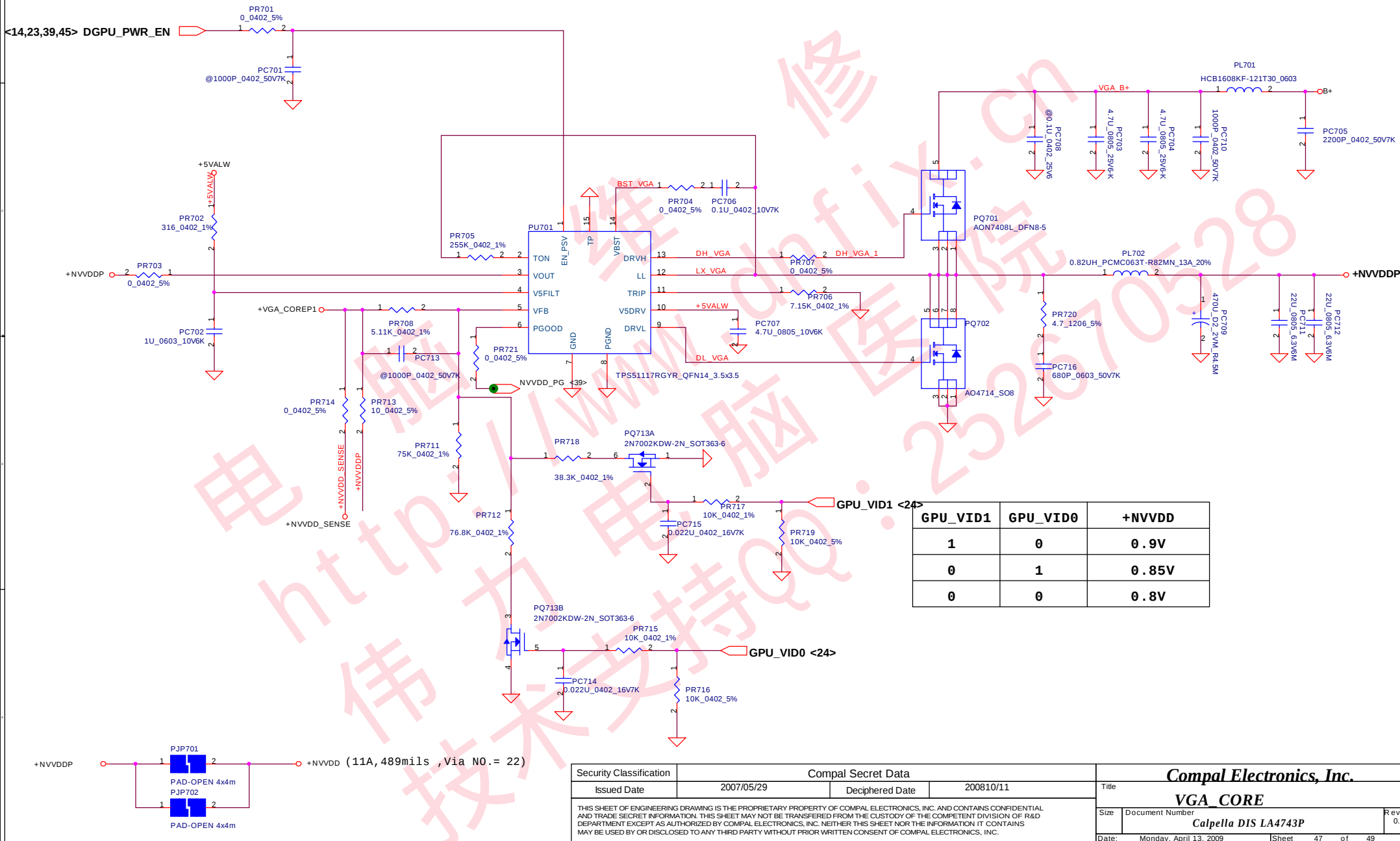


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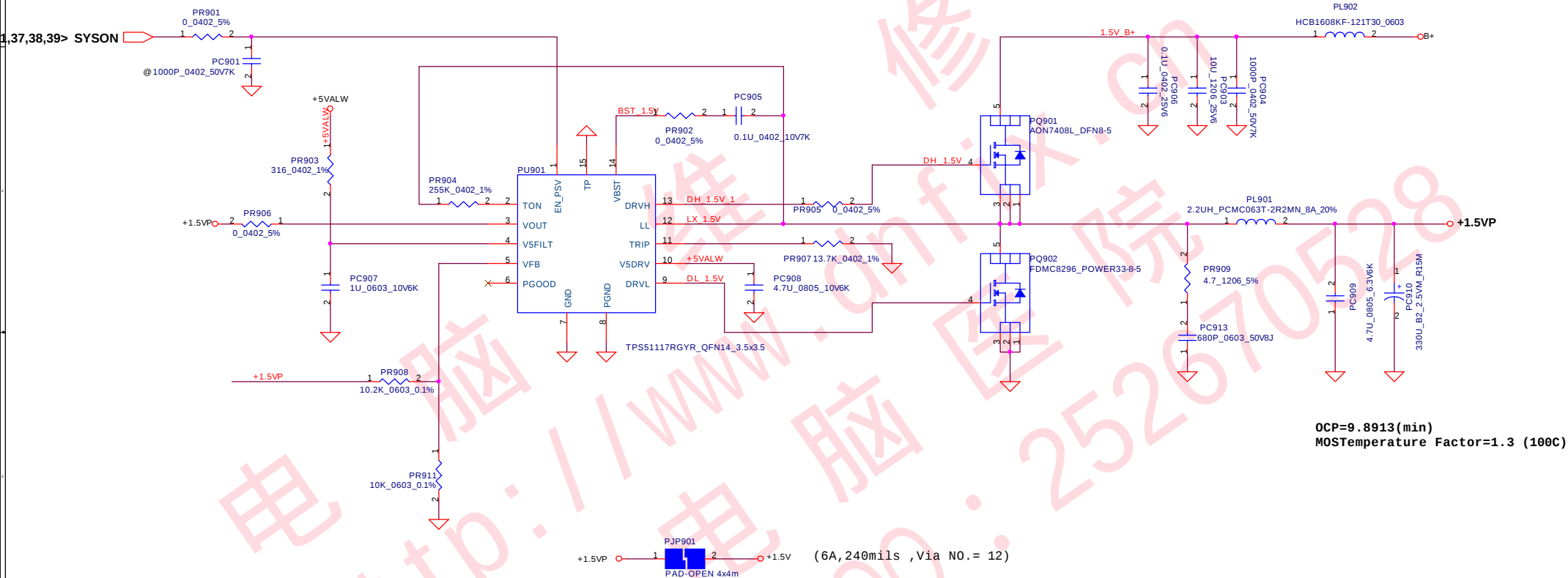
Iccmax= 35A
I_TDC=TDB
OCP=TDBA, Intel spec=TDBA

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GPU_VID1	GPU_VID0	+NVVDD
1	0	0.9V
0	1	0.85V
0	0	0.8V

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Issued Date		2007/05/29		Deciphered Date		200810/11		Title			
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								Calpella DIS LA4743P		0.1	
						Date:		Monday, April 13, 2009		Sheet 47 of 49	



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				Size	Document Number		Rev 0.	
				Calpella DIS LA4743P				
Date:		Monday, April 13, 2009		Sheet	48 of 49			

Version Change List (P. I. R. List) for Power Circuit

[illegible]