

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_PM+ICH9-M core logic

2008-02-25

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Voltage Rails

O MEANS ON

X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

USB assignment:

USB-0 Right side
USB-1 Right side
USB-2 Left side(with ESATA)
USB-3 Dock
USB-4 Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Finger Printer
USB-8 MiniCard(WWAN/TV)
USB-9 Express card
USB-10 X
USB-11 X

PCIe assignment:

PCIe-1 TV tuner/WWAN/Robeson
PCIe-2 X
PCIe-3 WLAN
PCIe-4 GLAN (Marvell)
PCIe-5 Card reader
PCIe-6 New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIF	MINI CARD	Sensor board	NB9M Thermal Sensor	NB9M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

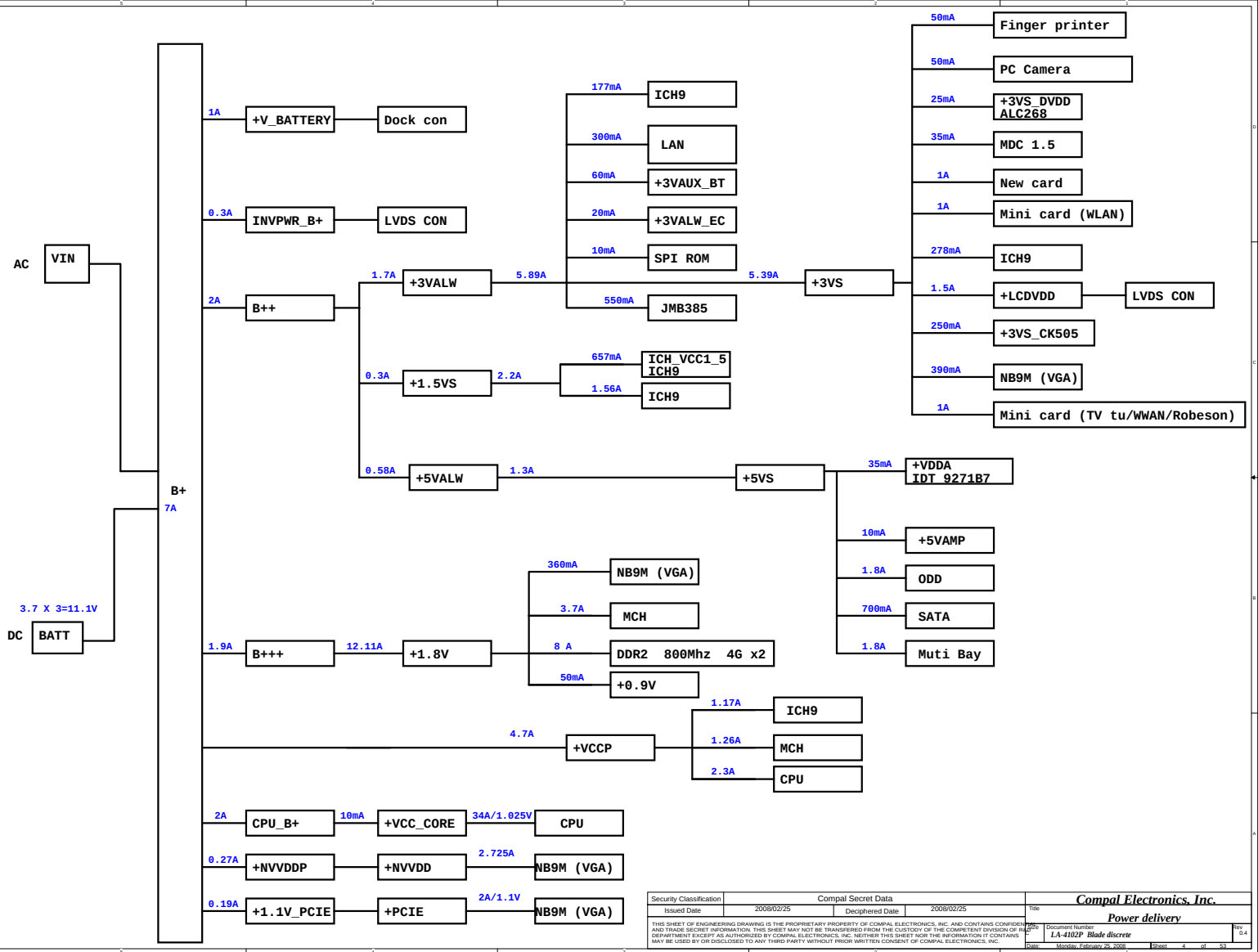
NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
DDC2_DATA DDC2_CLK	NB9M	V	X	X
3VDDCDA 3VDDCCL	NB9M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB9M	X	X	V

I2C / SMBUS ADDRESSING

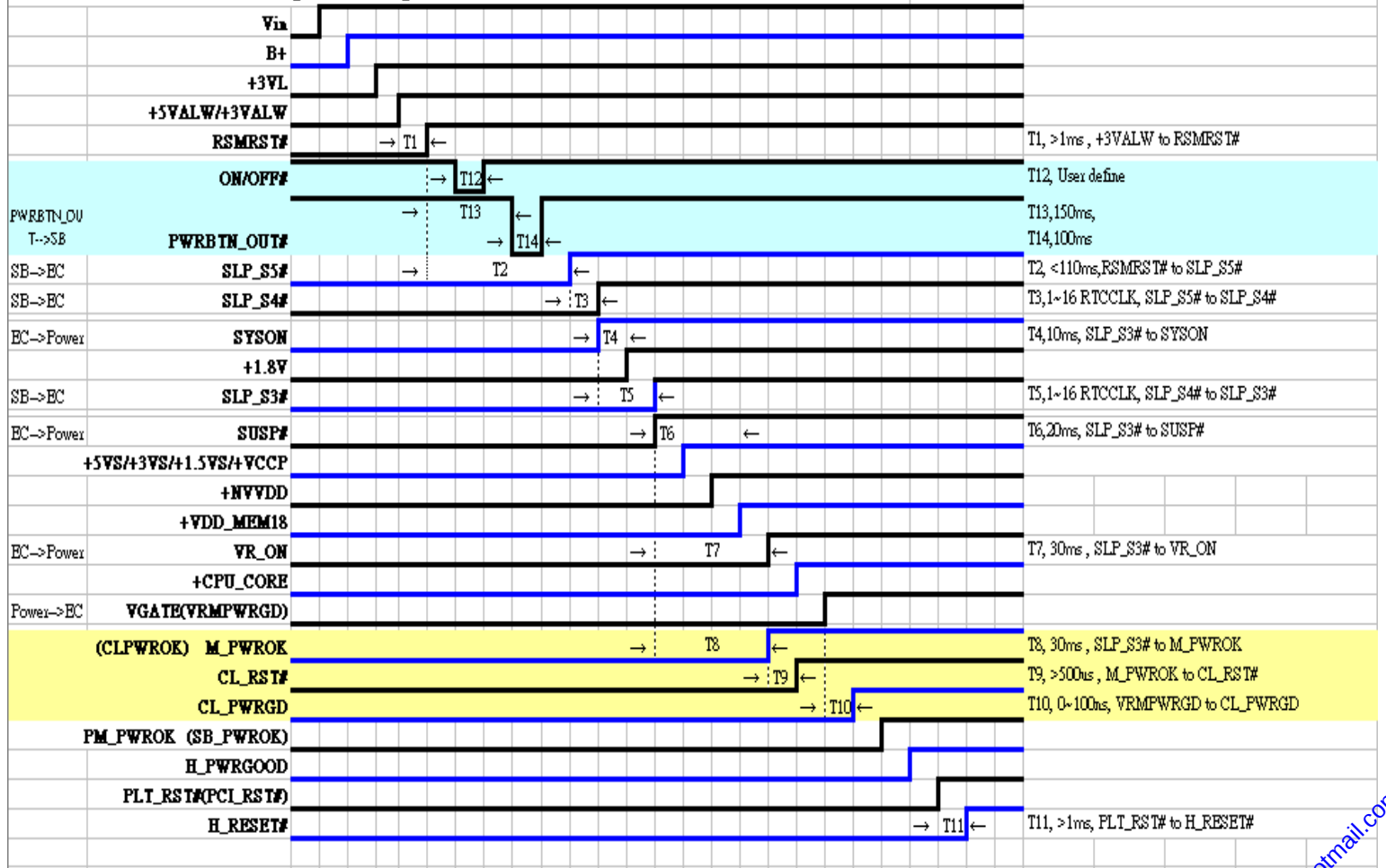
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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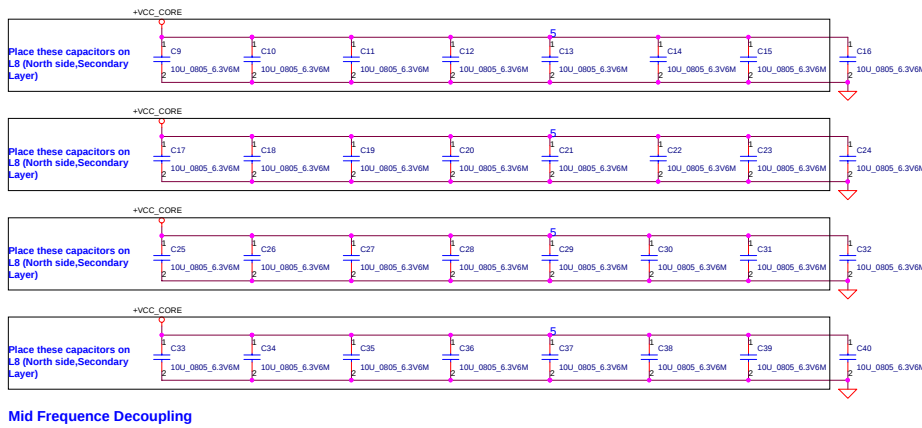
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				Power delivery
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JAL50 Discrete power sequence AC mode



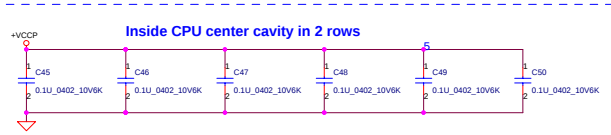
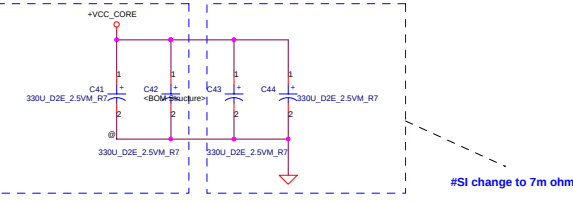
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				Power sequence	
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JCPUID		
AA	VSS[001]	P6
AA	VSS[002]	P21
A10	VSS[003]	P24
A14	VSS[004]	B2
A16	VSS[005]	B5
A18	VSS[006]	B22
A23	VSS[007]	B25
AF2	VSS[008]	T1
B6	VSS[009]	T26
B8	VSS[010]	T23
B11	VSS[011]	T2
B13	VSS[012]	T23
B16	VSS[013]	U6
B19	VSS[014]	U2
B21	VSS[015]	U24
B24	VSS[016]	V2
CA	VSS[017]	V5
CA	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W2
C18	VSS[022]	W2
C22	VSS[023]	Y3
CA5	VSS[024]	Y6
D1	VSS[025]	Y21
D4	VSS[026]	Y21
D6	VSS[027]	Y21
D11	VSS[028]	AA5
D13	VSS[029]	AA5
D16	VSS[030]	AA11
D18	VSS[031]	AA12
D23	VSS[032]	AA14
D23	VSS[033]	AA15
D26	VSS[034]	AA15
E3	VSS[035]	AA2
E6	VSS[036]	AA25
E6	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB12
E21	VSS[042]	AB13
E24	VSS[043]	AB15
F3	VSS[044]	AB3
F8	VSS[045]	AB5
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC11
F19	VSS[049]	AC14
F2	VSS[050]	AC15
F22	VSS[051]	AC15
F25	VSS[052]	AC19
G1	VSS[053]	AC24
G23	VSS[054]	AD2
G26	VSS[055]	AD5
H3	VSS[056]	AD8
H6	VSS[057]	AD11
H21	VSS[058]	AD13
H24	VSS[059]	AD15
J2	VSS[060]	AD16
J2	VSS[061]	AD19
J22	VSS[062]	AD25
K2	VSS[063]	AE1
K4	VSS[064]	AE1
K23	VSS[065]	AE14
K26	VSS[066]	AE14
L3	VSS[067]	AE15
L6	VSS[068]	AE15
L21	VSS[069]	AE23
L24	VSS[070]	AE23
M2	VSS[071]	AF5
M22	VSS[072]	AF5
M25	VSS[073]	AF13
M25	VSS[074]	AF13
N1	VSS[075]	AF13
N1	VSS[076]	AF13
N23	VSS[077]	AF13
N23	VSS[078]	AF13
N26	VSS[079]	AF13
P1	VSS[080]	AF25
P1	VSS[081]	AF25

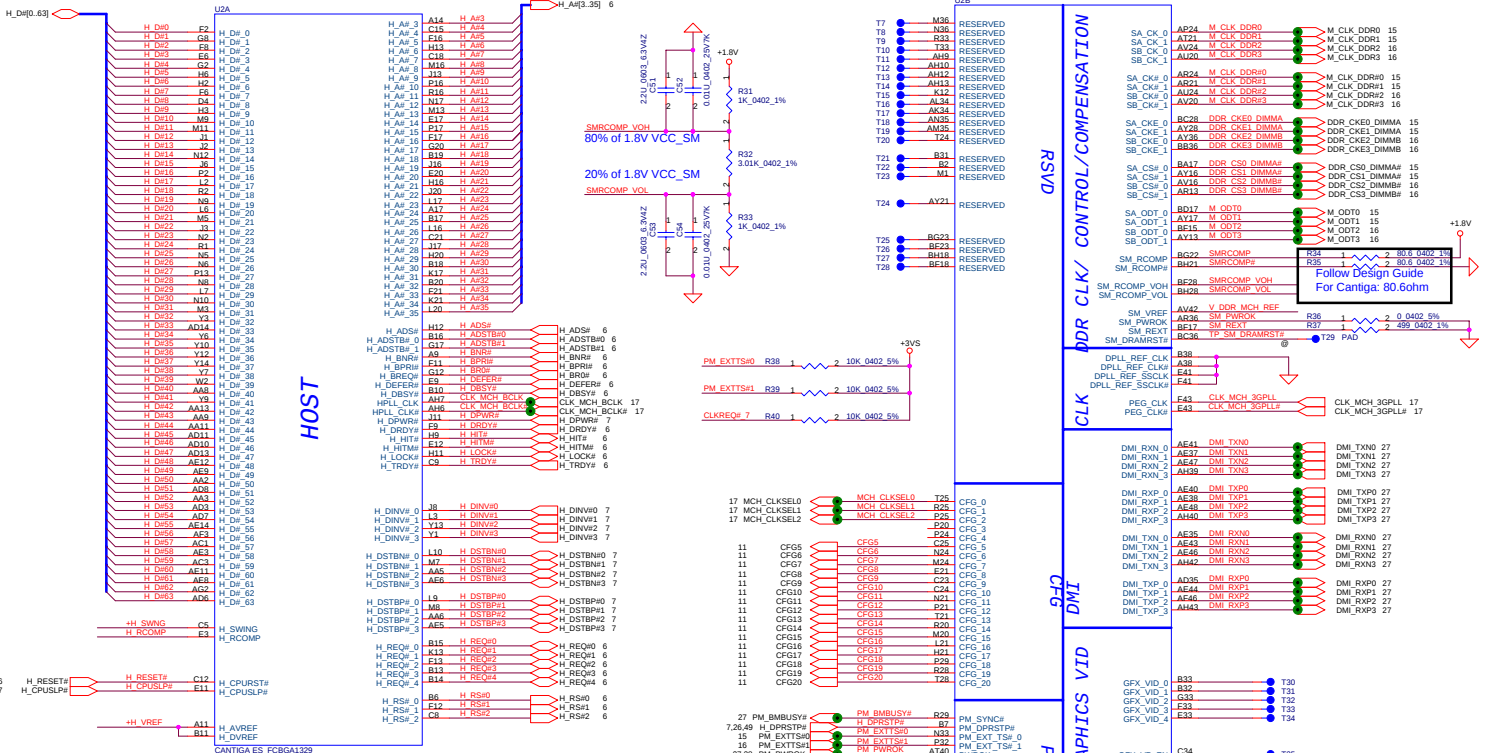


Near CPU CORE regulator

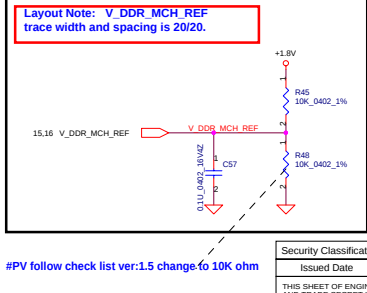
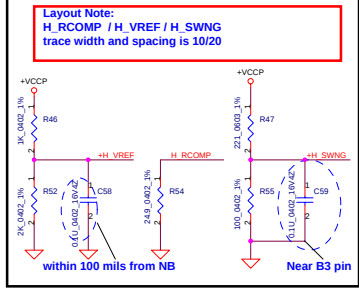
ESR <= 1.5m ohm
Capacitor > 1980uF



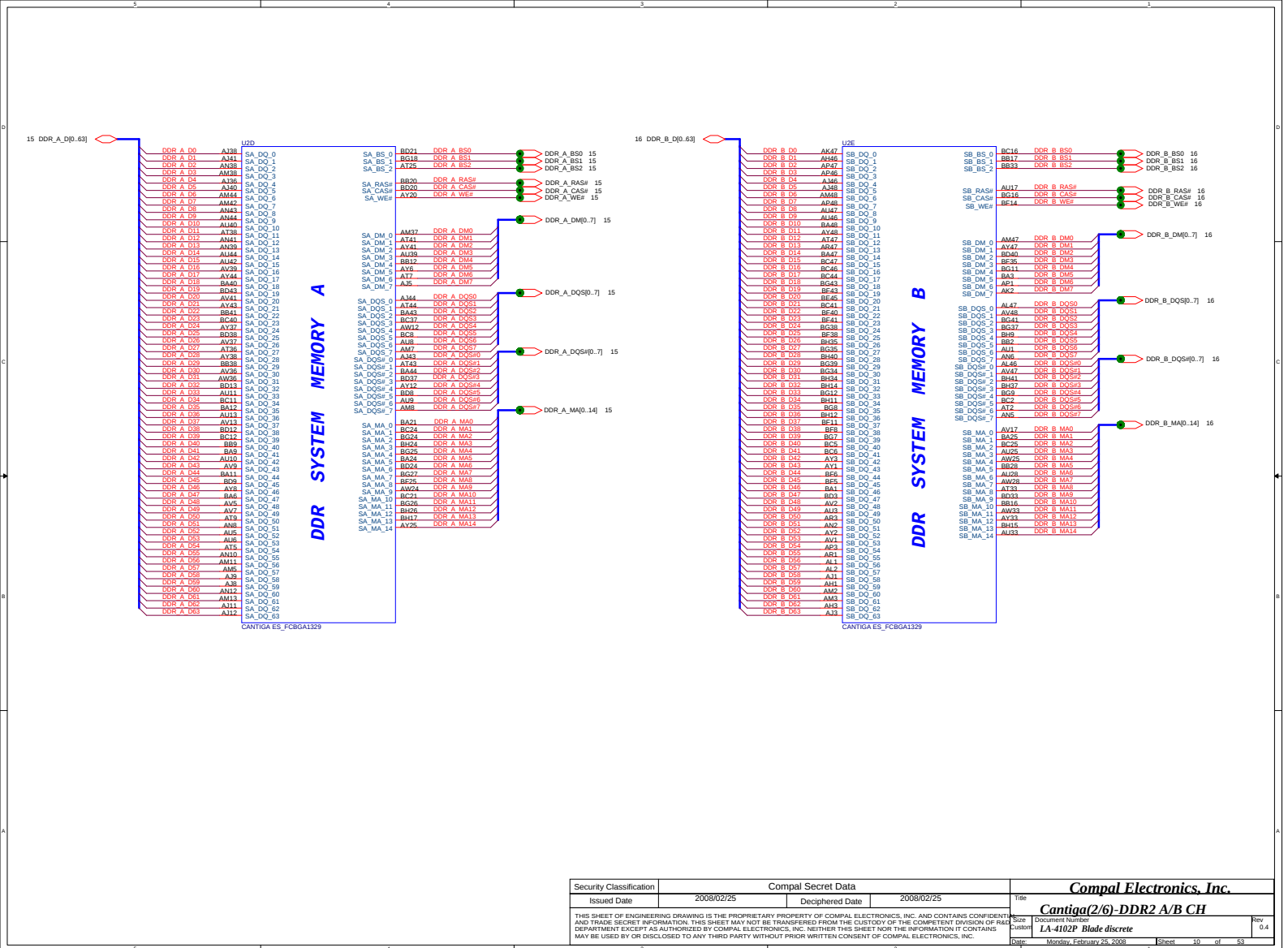
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Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

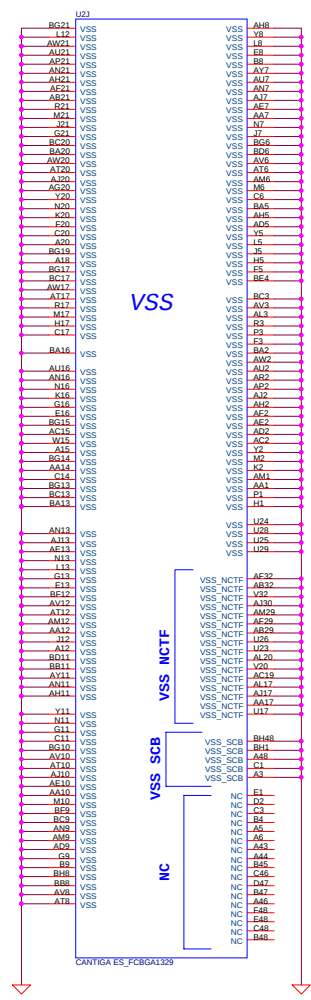
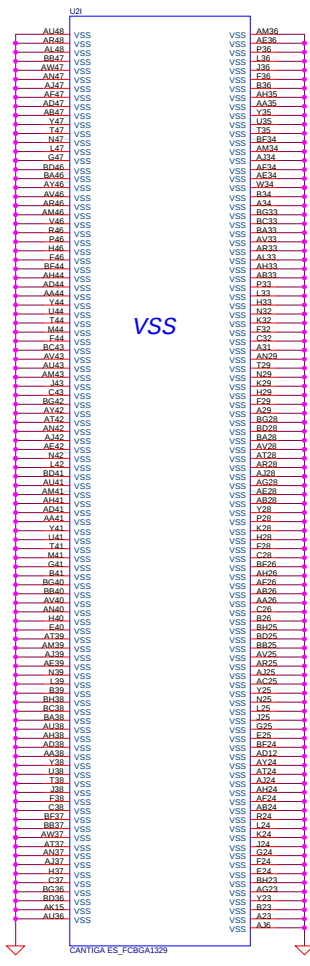


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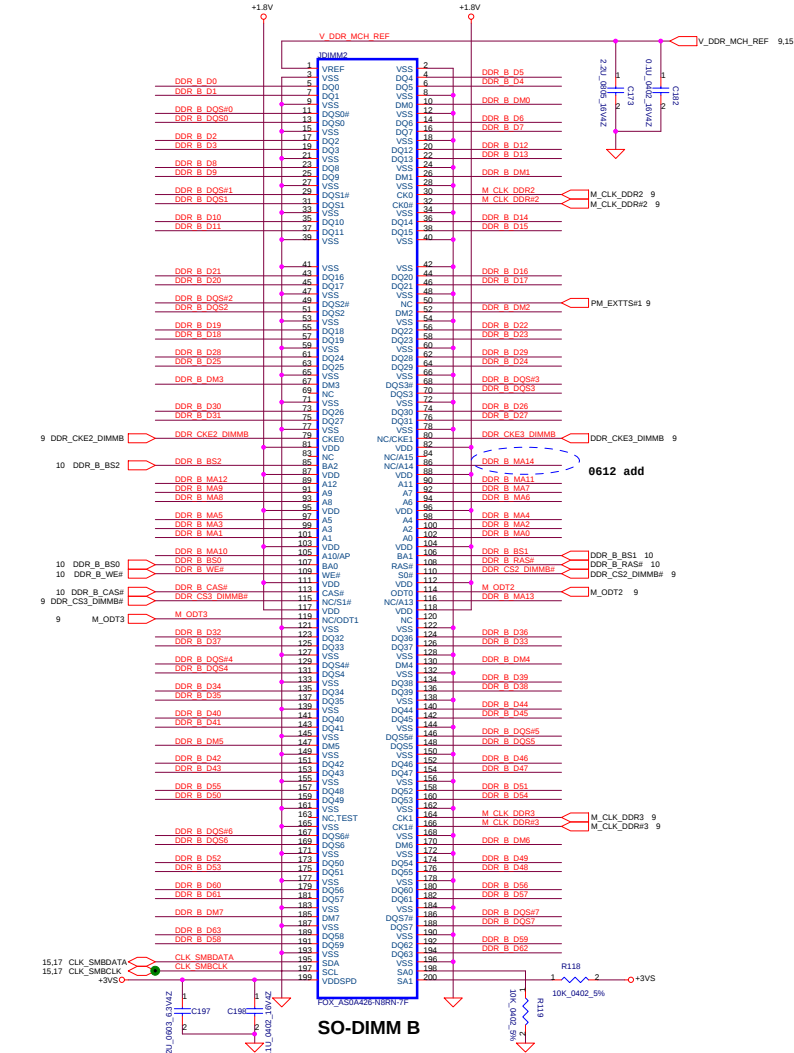
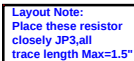
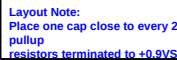


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Layout Note:
Place these resistor
closely JP3, all
trace length Max=1.5"



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ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#	V
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)	V

3V5

R180
10K_0402_5%

ITP_EN

R182
10K_0402_5%

⊕

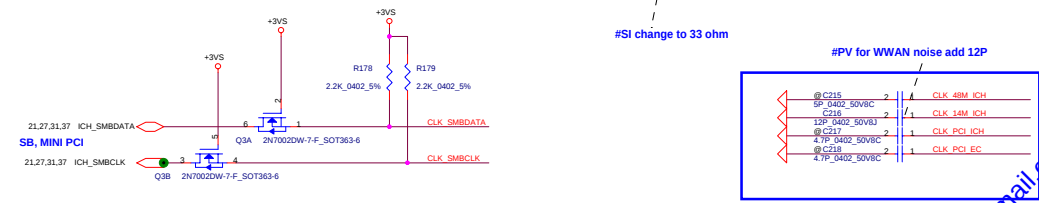
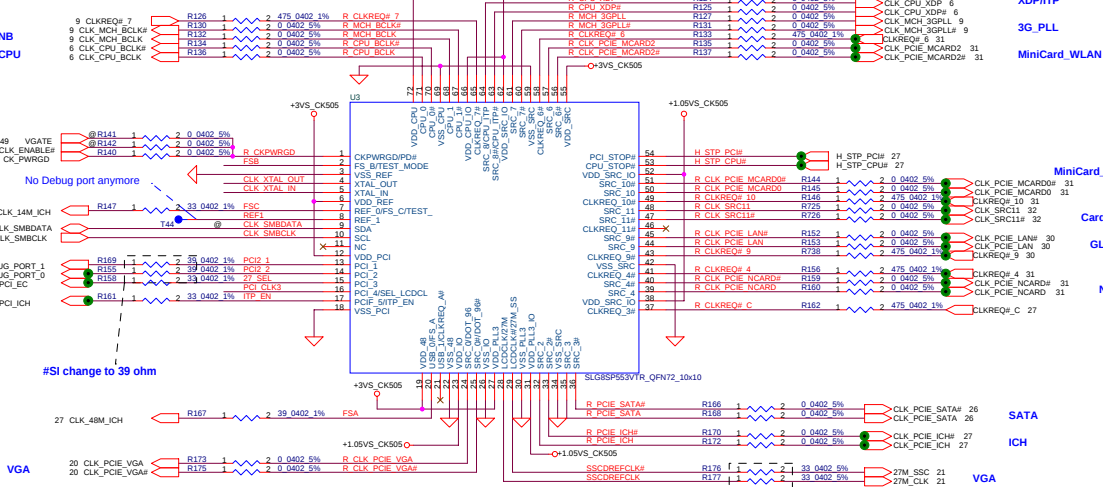
3V5

R181
10K_0402_5%

PCI_CLK3

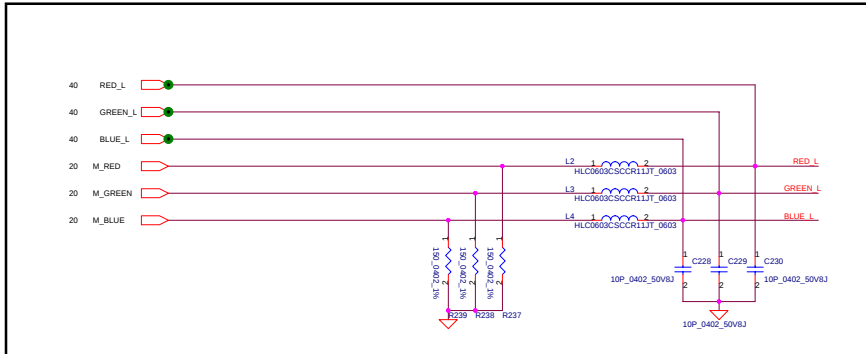
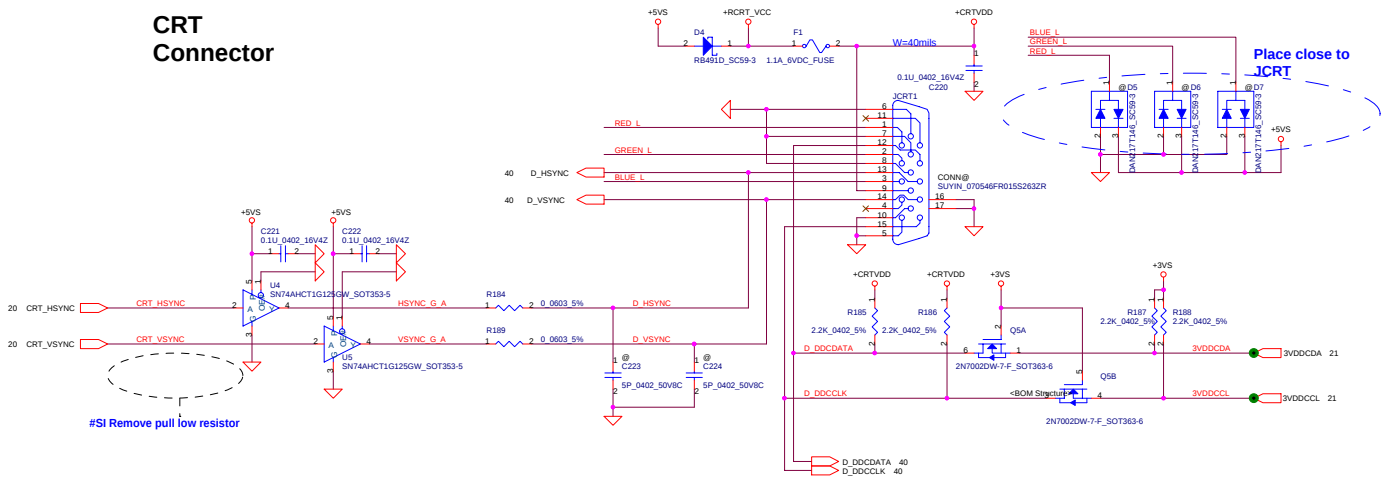
R183
10K_0402_5%

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CRT Connector

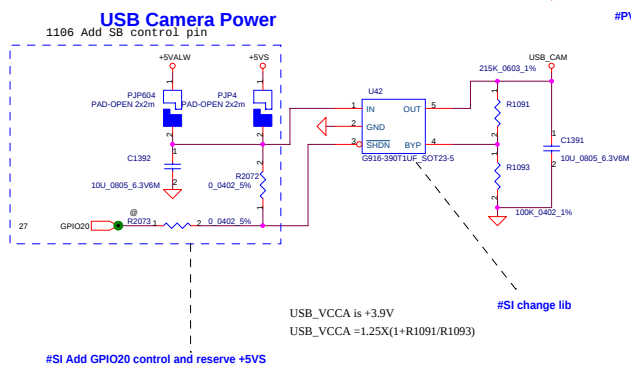
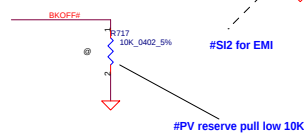


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CRT Connector

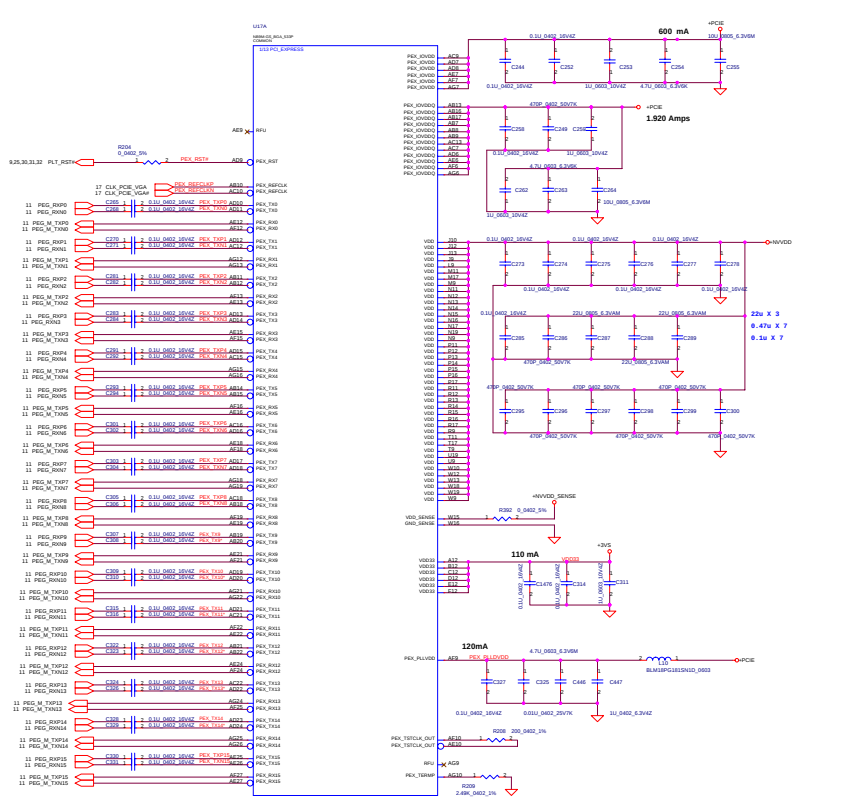
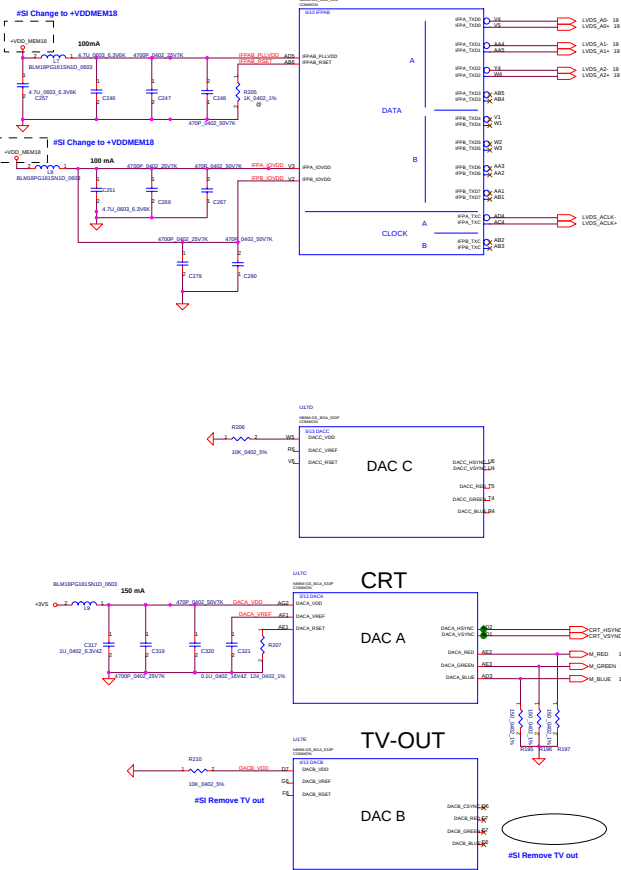
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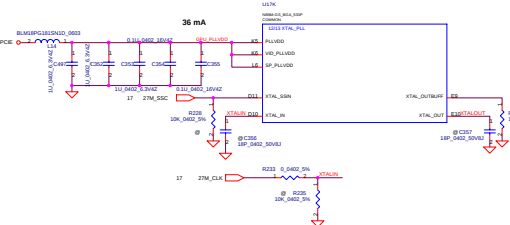
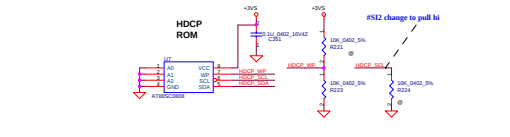
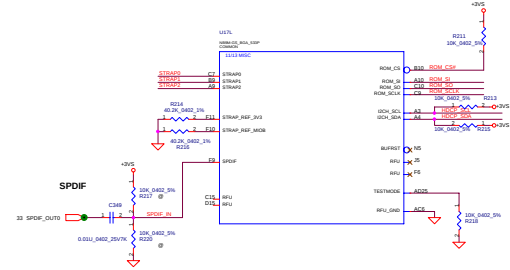
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LVDS & DAC Interface

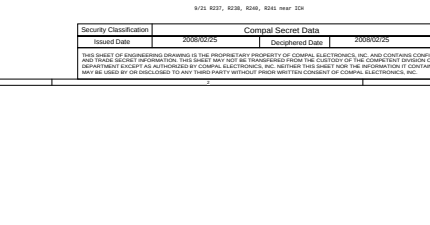
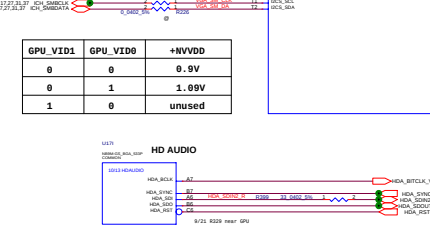
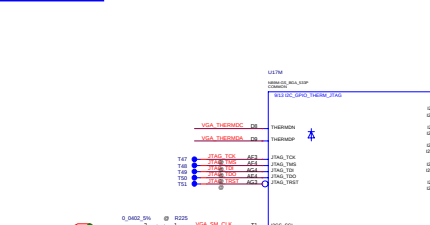
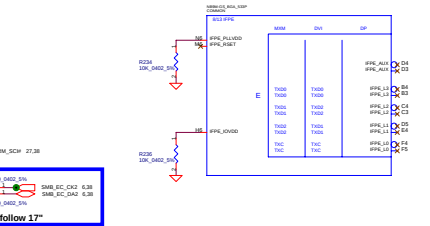
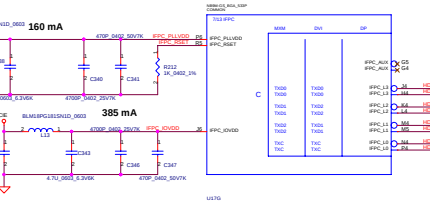
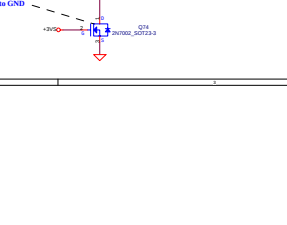
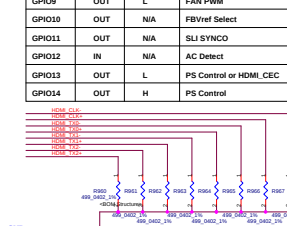
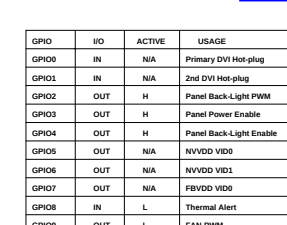
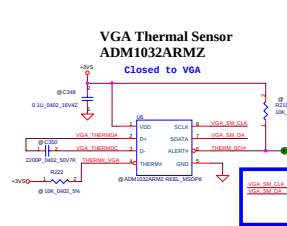
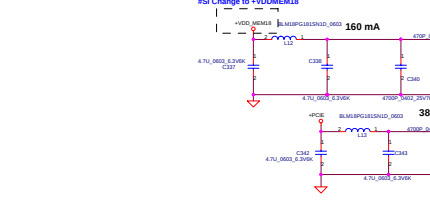
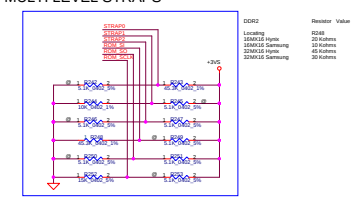
PEG Interface



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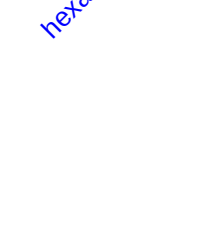
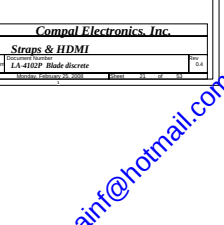
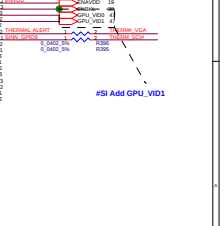
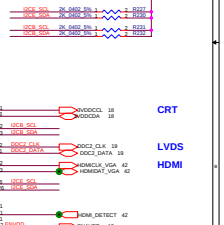
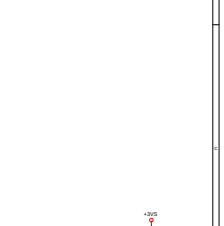
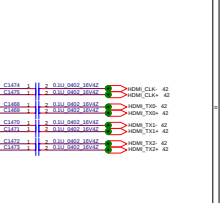


Straps MULTI LEVEL STRAPS



GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC0
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control

GPU_VID1	GPU_VID0	+NVVDD
0	0	0.9V
0	1	1.09V
1	0	unused

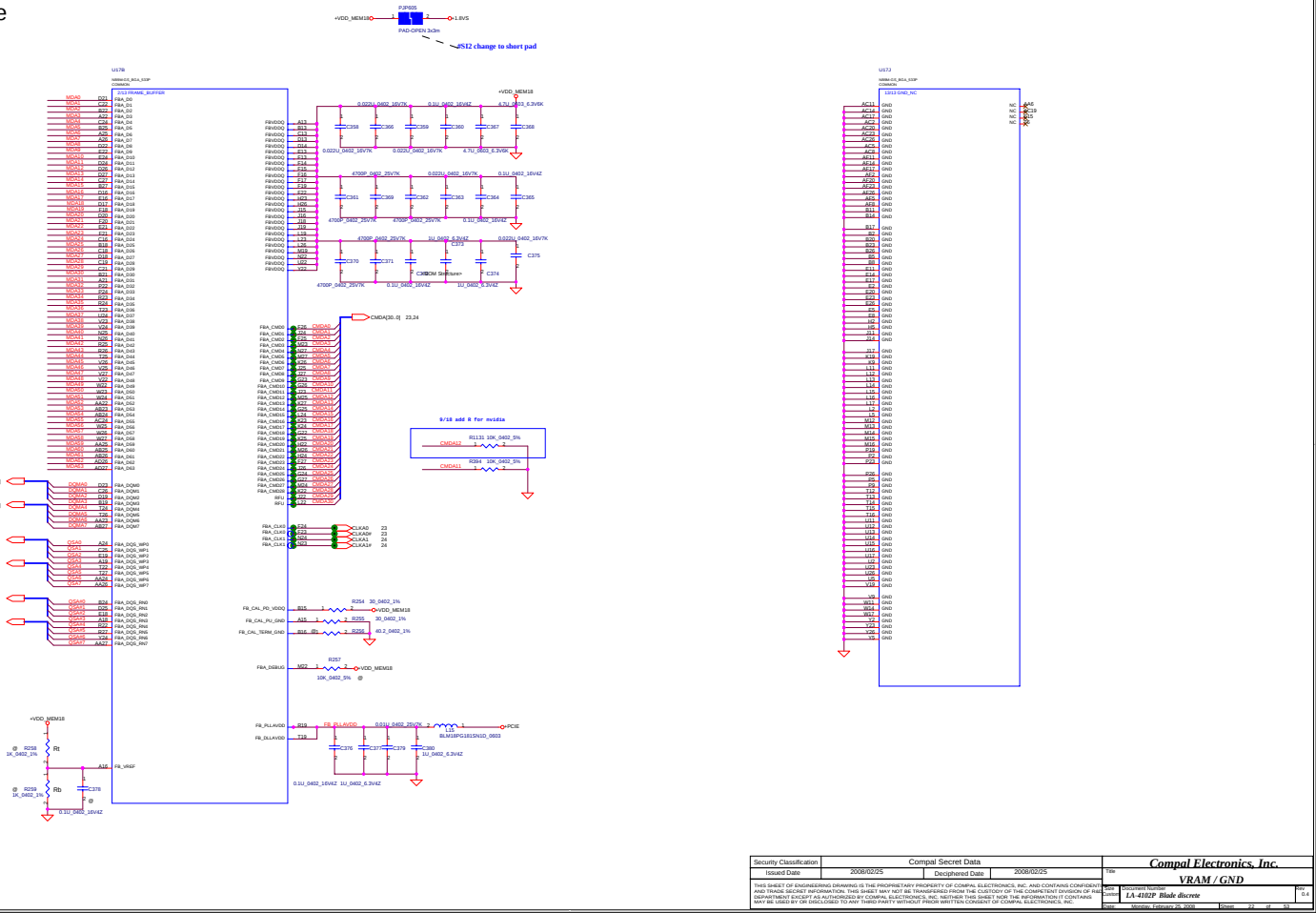


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Straps & HDMI		1A-010P

hexaint@hotmail.com

VRAM Interface

- 23 M04K15_01
- 23 M04K15_10
- 24 M04K17_01
- 24 M04K17_02
- 24 M04K17_03
- 24 M04K17_04

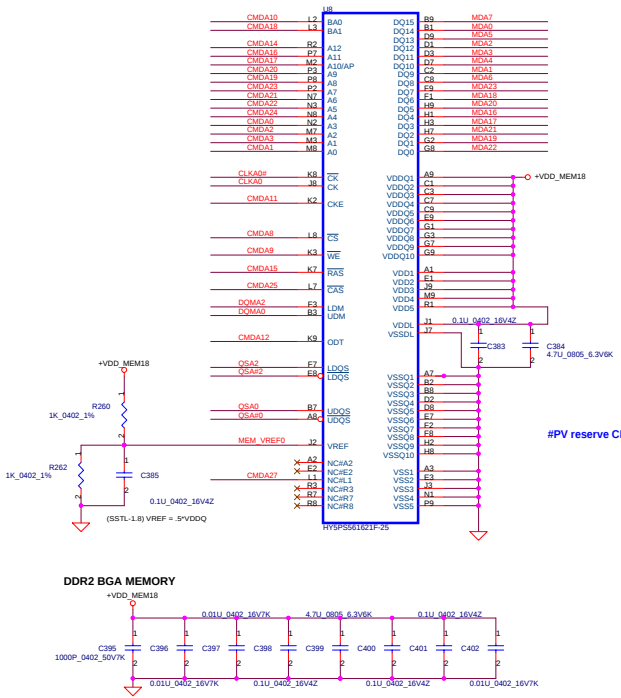


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Document Number		LA-4102P Blade driver							
Rev.		001		Date		02/25/08		Page 1 of 3	

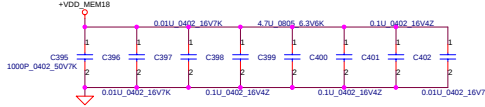
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB
64Mx16 DDR2 400MHz*4==>512MB

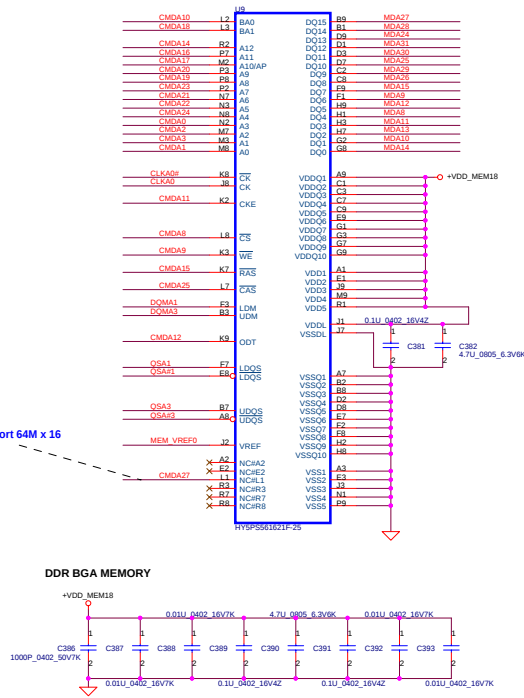
- 22.24 QSA[7..0] QSA[7..0]
- 22.24 QSA[7..0] QSA[7..0]
- 22.24 QMA[7..0] QMA[7..0]
- 22.24 MDA[93..0] MDA[93..0]
- 22.24 CMDA[93..0] CMDA[93..0]



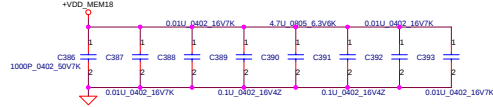
DDR2 BGA MEMORY



5

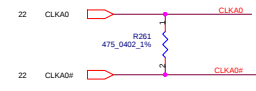


DDR2 BGA MEMORY



5

DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



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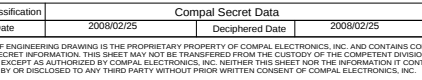
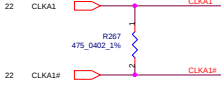
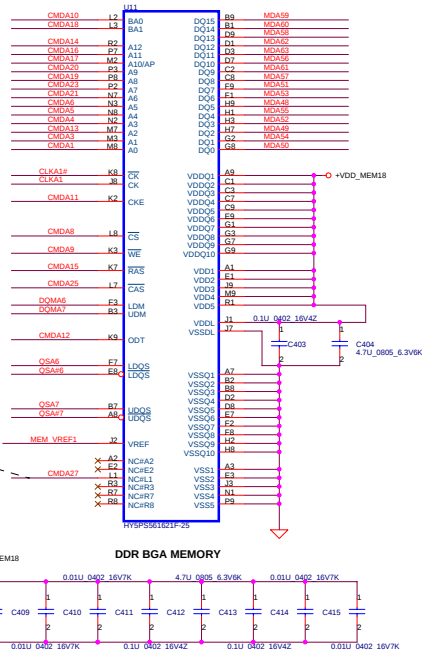
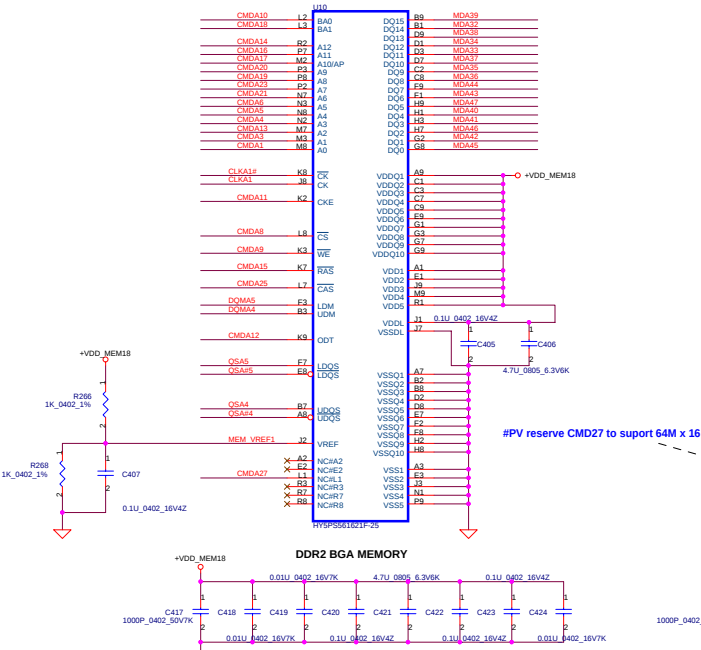
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

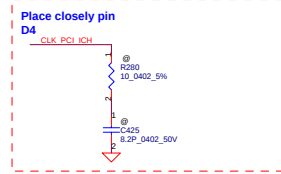
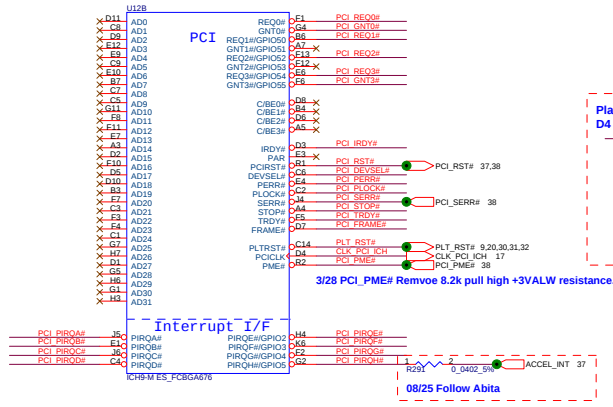
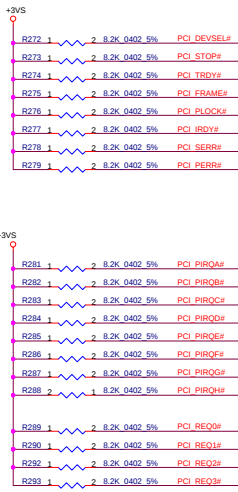
64Mx16 DDR2 400MHz*4==>512MB



Address	DATA Bus	
CMD0	A3	.63
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



Security Classification	Compal Secret Data		Title	
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Date	Monday, February 25, 2008	Sheet	8	of 16



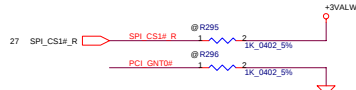
A16 swap override Strap

PCI_GNT3# Low= A16 swap override Enble
High= Default *



Boot BIOS Strap

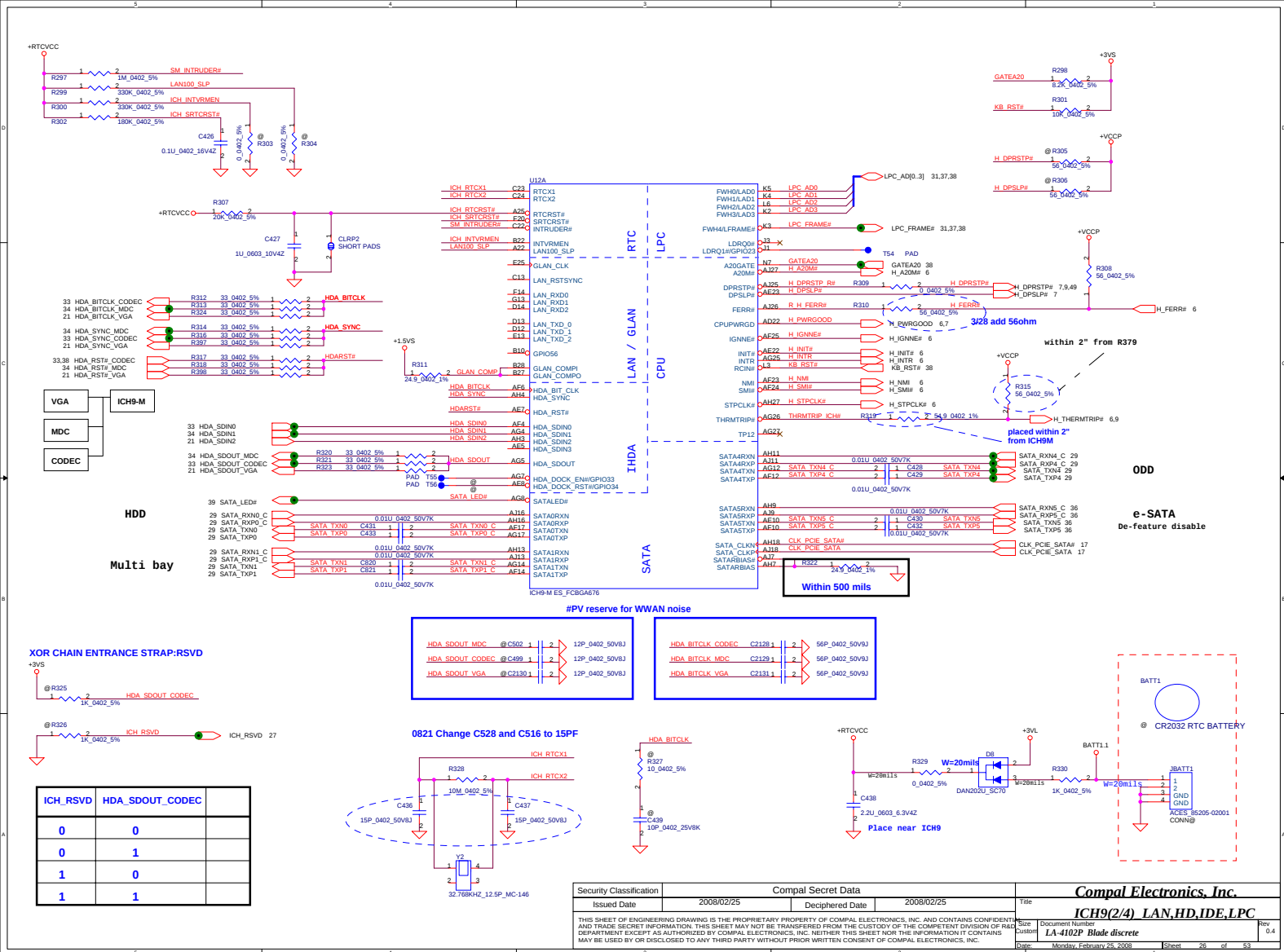
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



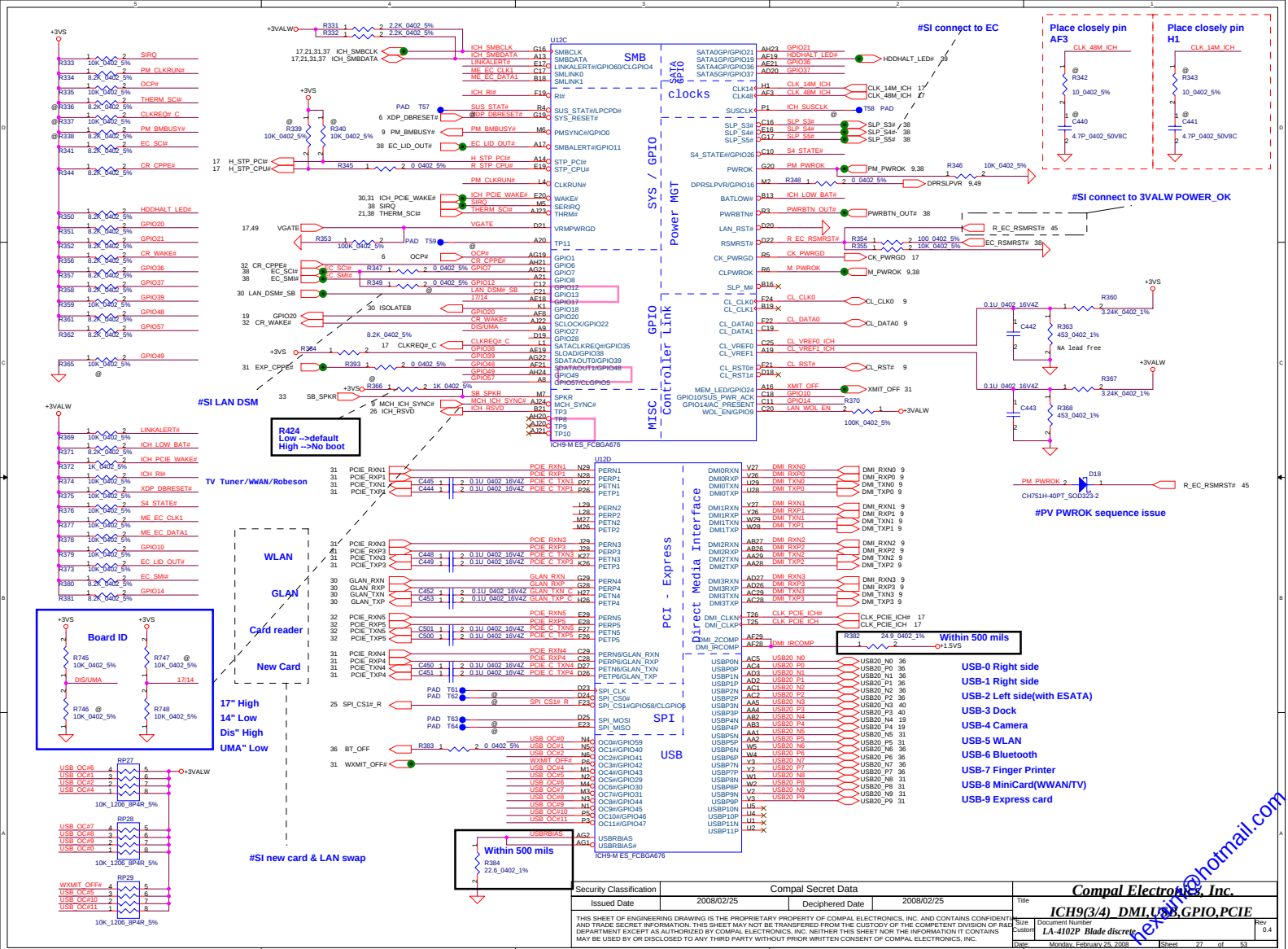
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				LA-1012 (P) secret discrete		
Size	Document Number			Rev	0.4	
Date	Monday, February 25, 2008	Sheet	26		of 53	

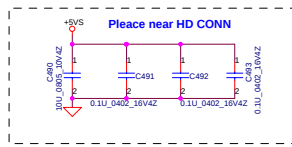
DELL CONF

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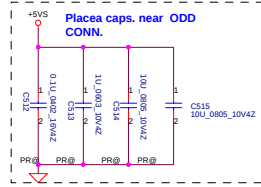
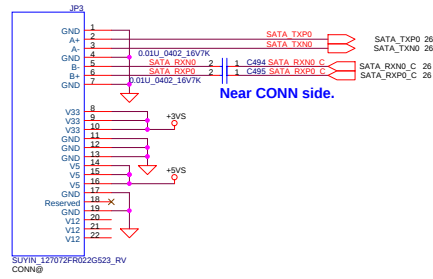


ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

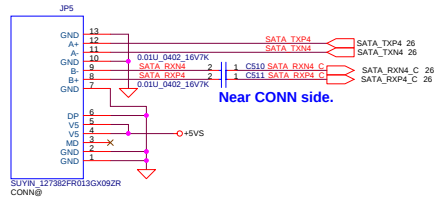




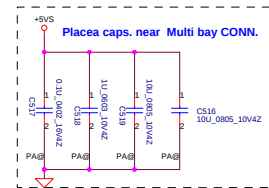
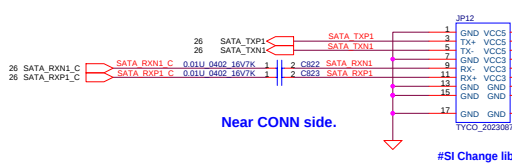
HDD Connector



CD-ROM Connector

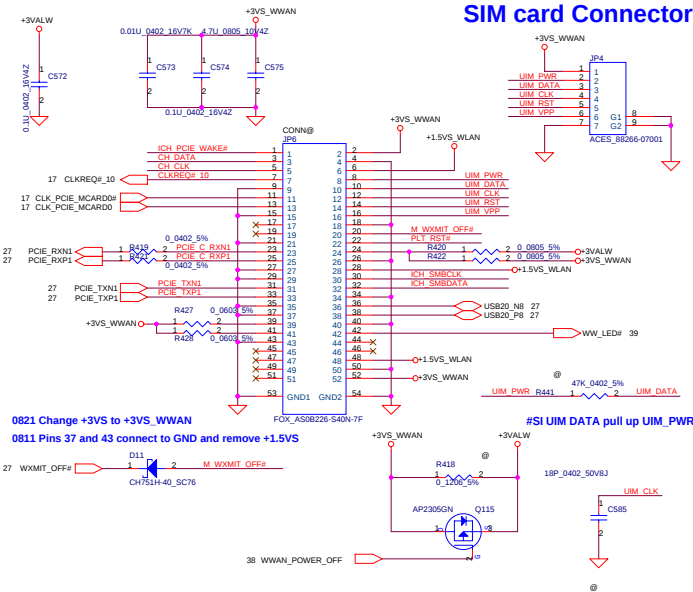


Multi Bay Connector

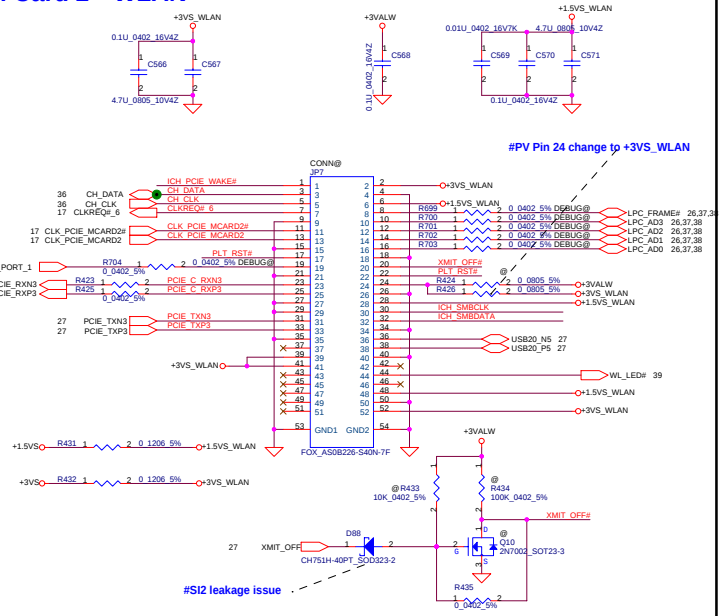


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				0.4
				Date
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Mini Card 0--TV tuner/WWAN/Robson

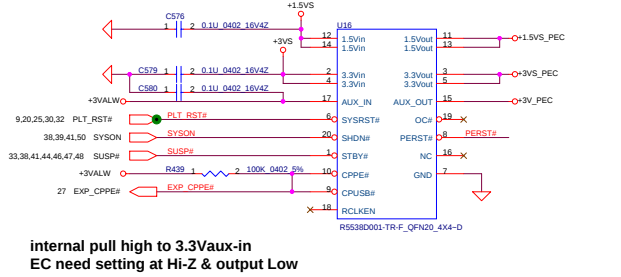


Mini Card 2---WLAN



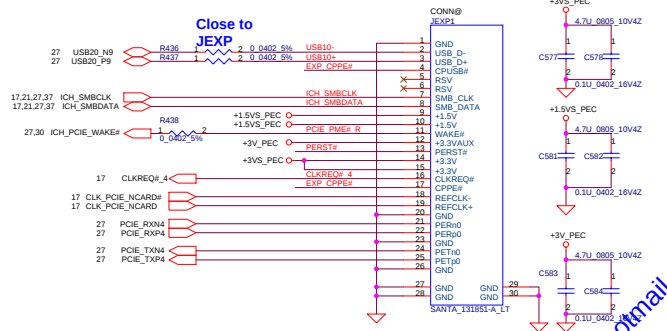
New Card

Express Card Power Switch

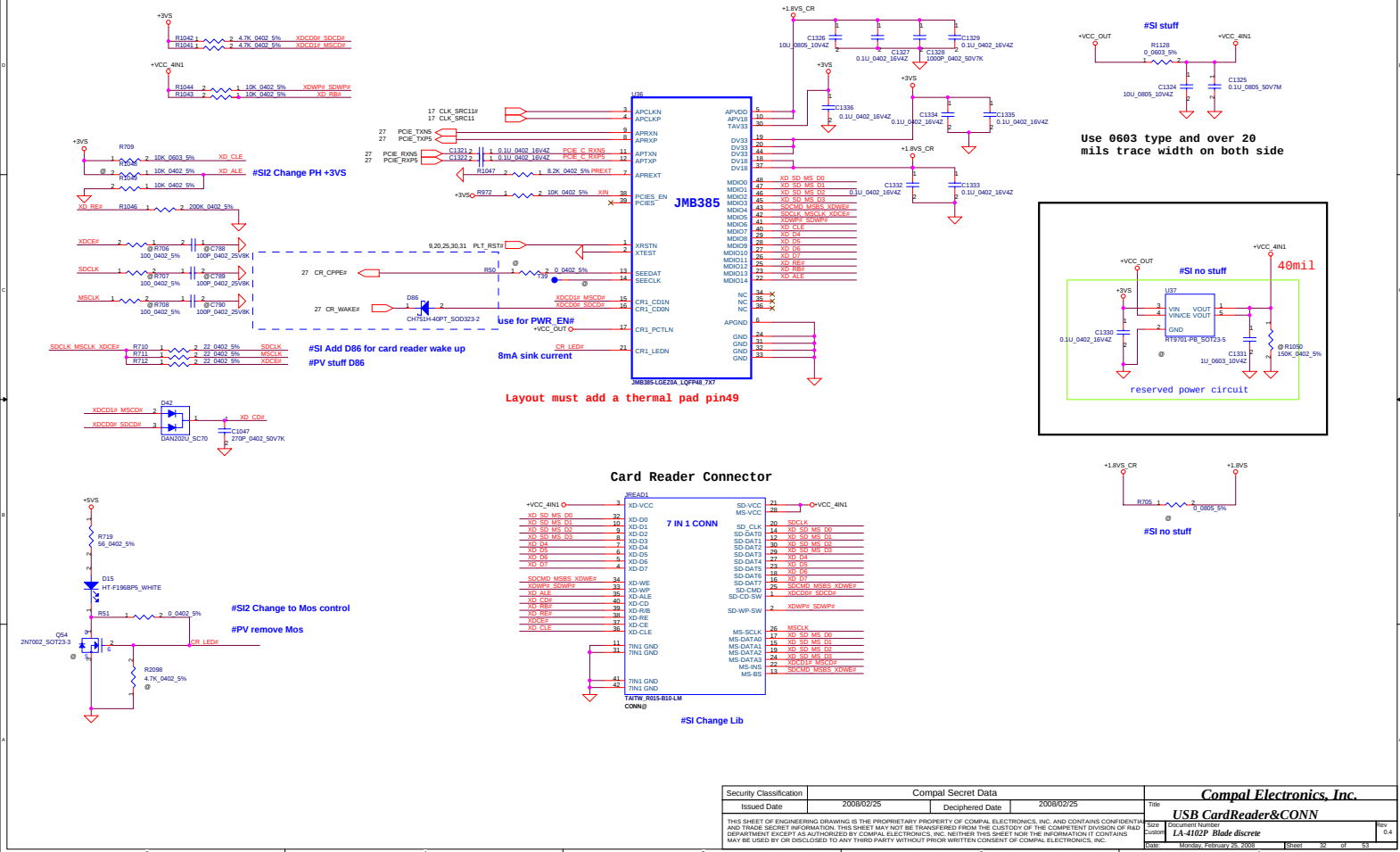


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Near to Express Card slot.

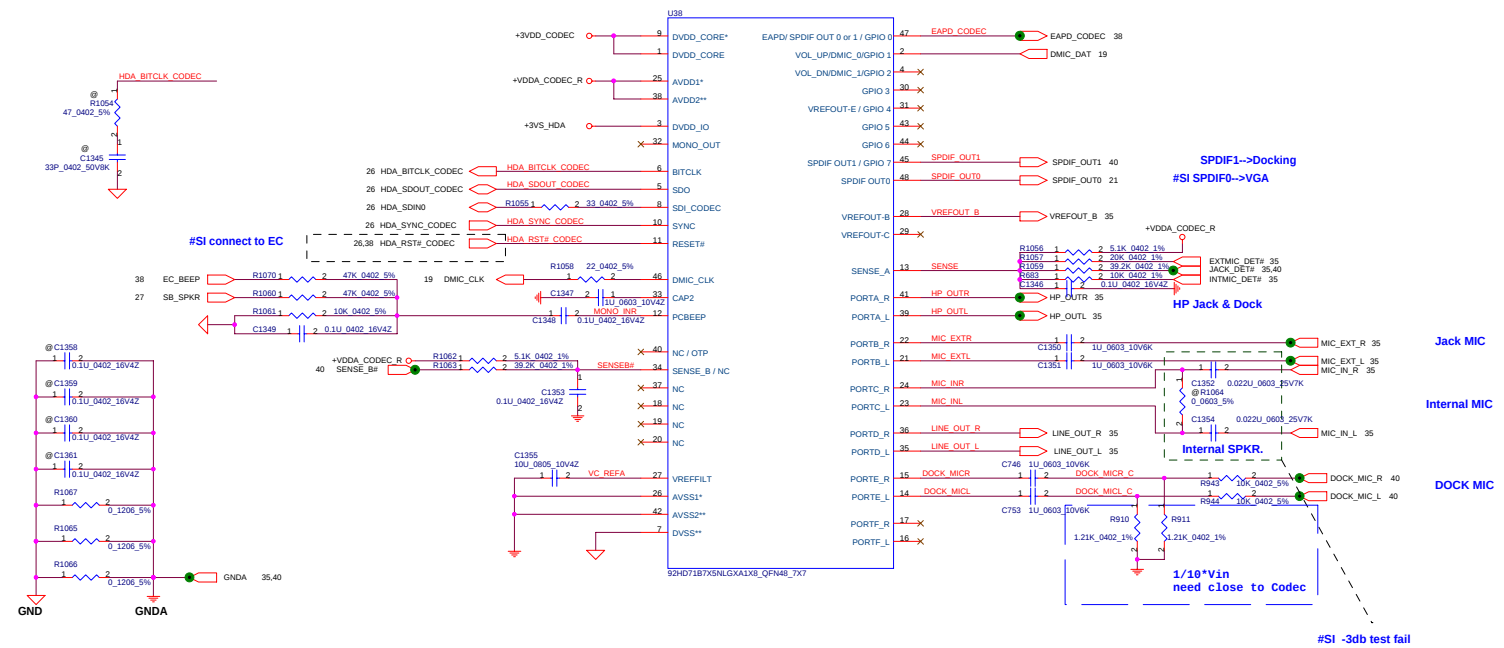
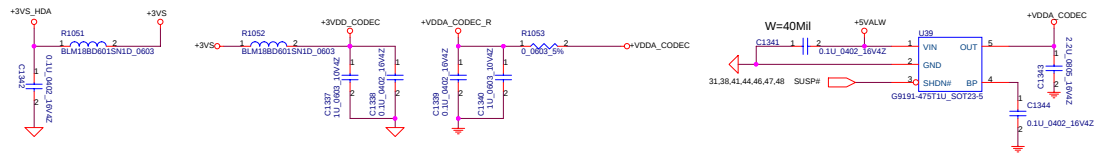


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			LA-10102 Not discrete	
Date	Monday, February 25, 2008		Sheet	31 of 53



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				Date 14-Mar-2012	File 10202_Fluid.docx	
				Sheet 32 of 53		

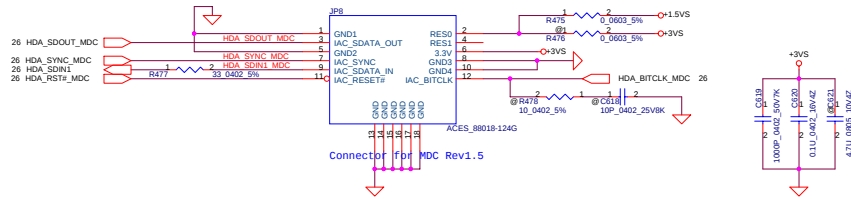
4.75V)
500mA



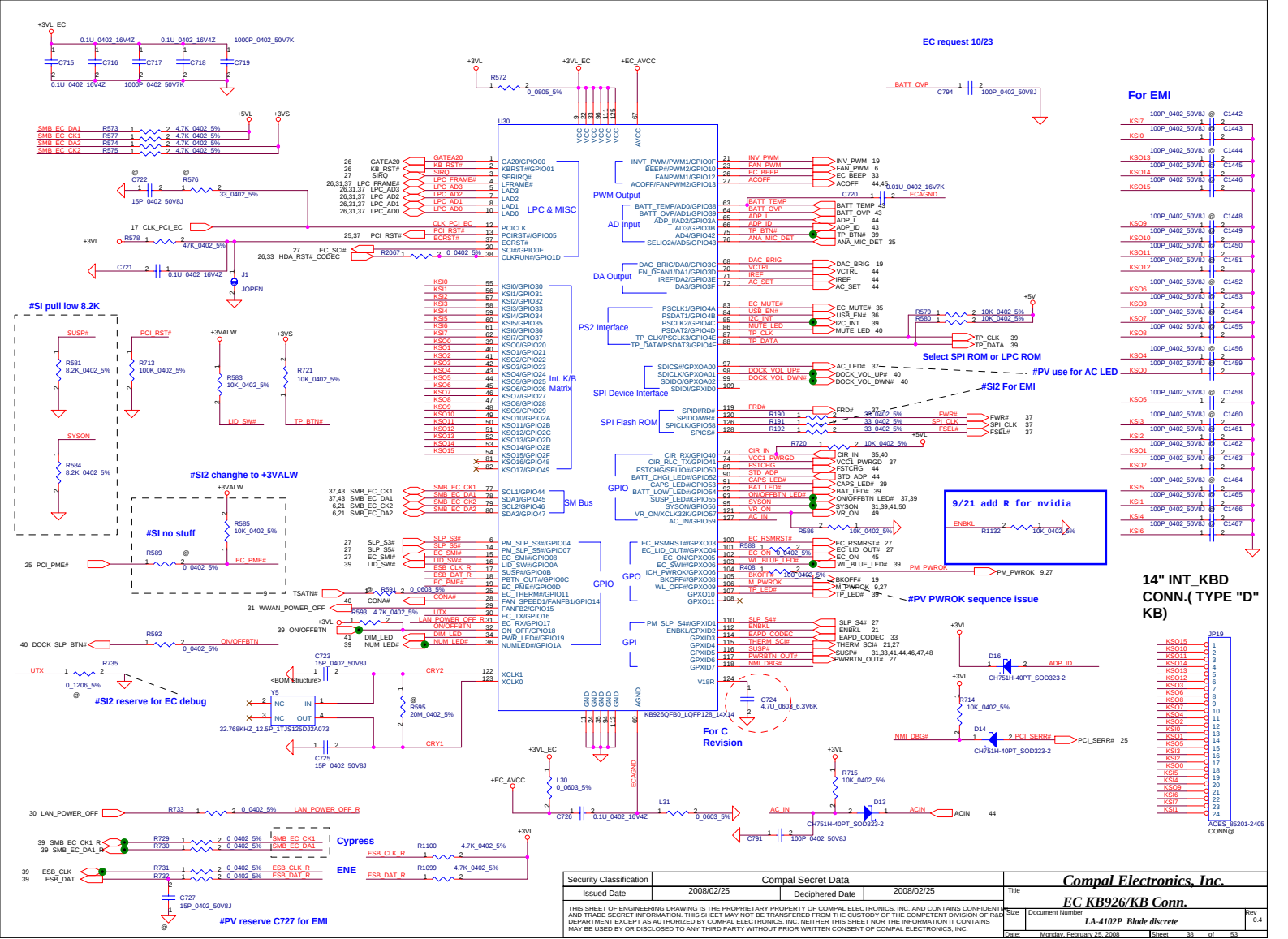
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

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MDC 1.5 Conn.



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System LED

Cap lock

Battery Charge LED

HDD LED

System Power LED

Keyboard backlight Conn

Mini card LED

BT_LED 36

2N7002_SOT23-3 Q112

100K_0402_5% R1126

10K_0402_5% R716

+3VS #S12 add PH +3VS

WL_BLUE_LEDw 38

0.0402_5% R193

WL_LEDw 31

0.0402_5% R194

WL_LED 31

0.0402_5% D19

CH7511-40PT_SOC323-2

#PV change to doilde

Capacitor Sensor Conn

The diagram illustrates the capacitor sensor connection for two different PCB layouts. The left layout shows the connection of the sensor chip to the ESB_CLK, ESB_DAT, and SMB_EC_CLK_L signals, with capacitors C2123, C2124, and C2134. The right layout shows the connection of the sensor chip to the +SVS_LED, +SVS_CAP, and +3V_L signals, with capacitors C261 and C60. Both layouts include labels for EMI and pass cap connections.

Left Layout:

- ESB_CLK (2) @ R2116 @ C2123 1SP_0402_50VBJ
- ESB_DAT (2) @ R2117 @ C2124 1SP_0402_50VBJ
- SMB_EC_CLK_L (38)
- ESB_CLK (38)
- EC_INT (38)
- NUM_LEDH (38)
- SMB_EC_DAT_L (38)
- C2134 1SP_0402_50VBJ
- #SI2 for EMI
- #SI2 add by pass cap

Right Layout:

- +SVS_LED (1)
- +SVS_CAP (1)
- +3V_L (1)
- C261 4.7U_0603_6.3V6K
- C60 22U_1_AVM
- #SI2 add by pass cap

ON/OFF Button Connector

38 ON/OFFBTN

37,38 ON/OFFBTN_LED

+5VSW_LED

0

1P10

1 2 3 4 5 6 7 8 9 10 11 12

ACES_B0201-04051 CONW#

38 LID_SWIF

10P_0402_50V6J

3VSWV

C219 0.1µ 0402_16V42

R2

JP11

1 2 3 4 5

G1 G2

XRES: 85051-04051

CONN@

Lid Switch Connector

The schematic diagram illustrates the T/P Board, which includes a TP LED driver and T/P Power section.

TP LED Driver: This section drives four TP LEDs (PA, PR, PA, PR) using a QSMF-C16E LED driver. The driver is configured with two channels, each driving two LEDs. The LEDs are connected to a +5V supply through a 10K_0402_5% resistor (R613, R610, R612, R611). The driver is controlled by TP_CLK and TP_DATA signals. The driver is labeled #PV TP LED separate between PA and PR.

T/P Power: This section provides power to the TP LEDs. It includes a 5V supply, a 10K_0402_5% resistor (R615), and a 0.0805_5% capacitor (C23). The power is delivered to the TP_LEDs through a 10K_0402_5% resistor (R612) and a 2N7002_SOT23-3 MOSFET (Q24). The MOSFET is controlled by a SYSON signal (31.38.41.50 SYSON) through a 10K_0402_5% resistor (R612). The MOSFET is labeled #PV for EMI stuff.

TP ON/OFF: This section controls the TP LEDs. It includes a 5V supply, a 10K_0402_5% resistor (R611), and a 0.0805_5% capacitor (C23). The power is delivered to the TP_LEDs through a 10K_0402_5% resistor (R612) and a 2N7002_SOT23-3 MOSFET (Q24). The MOSFET is controlled by a SYSON signal (31.38.41.50 SYSON) through a 10K_0402_5% resistor (R612). The MOSFET is labeled #PV for EMI stuff.

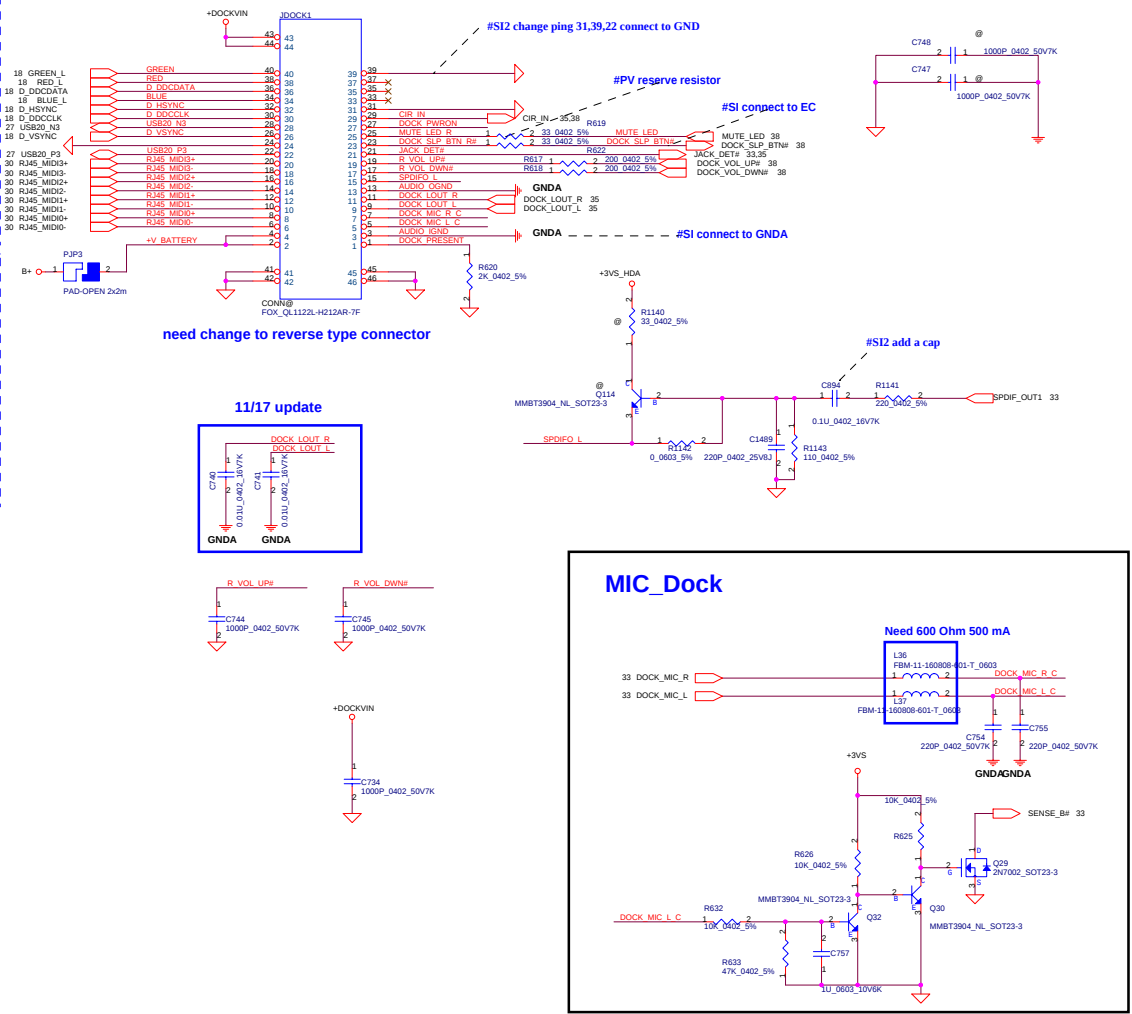
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2008/02/25	Deciphered Date	2008/02/25	LED, TP.KBL, Cub sensor board	
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#S12 Add pull up

+3V5

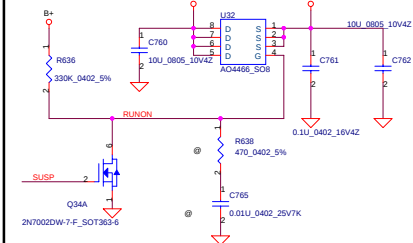
DOCK_V0L_UP# R594 2 1 10K_0402 5%

DOCK_V0L_DWN# R596 2 1 10K_0402 5%

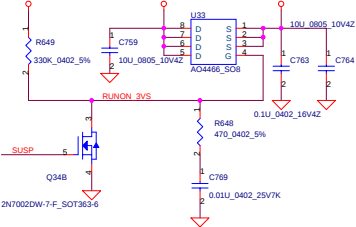


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Date	LA-4102P Blate, disc 8			Sheet	40 of 53

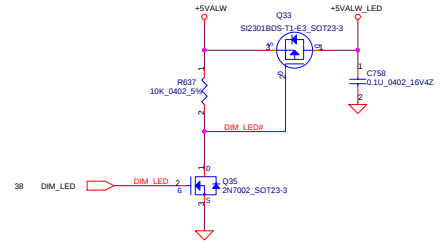
+5VALW to +5VS Transfer



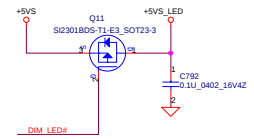
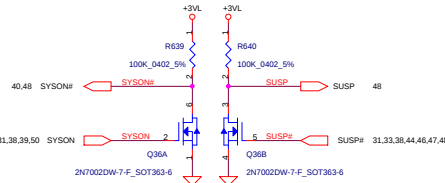
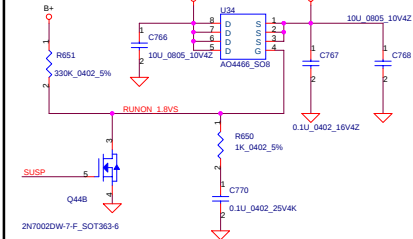
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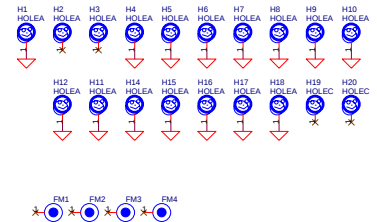
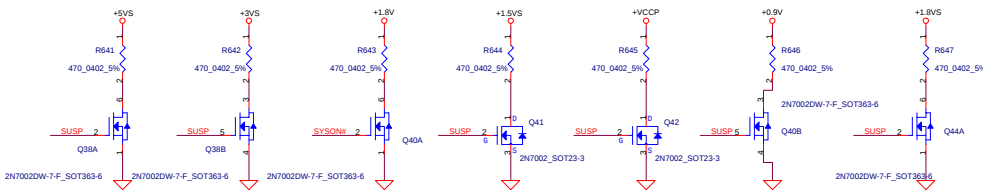
DIM LED



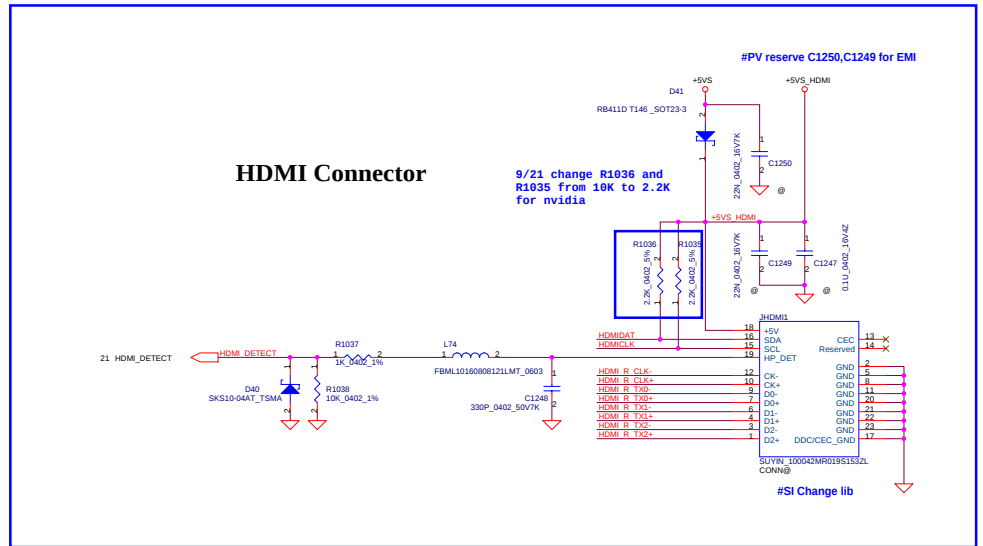
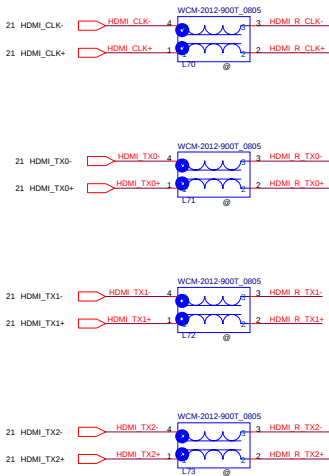
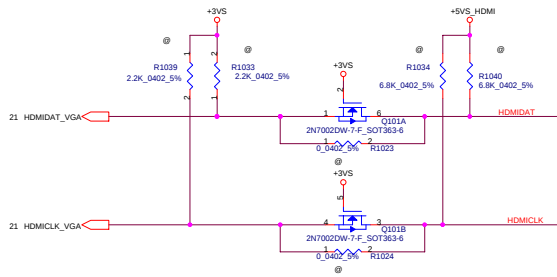
+1.8V to +1.8VS Transfer



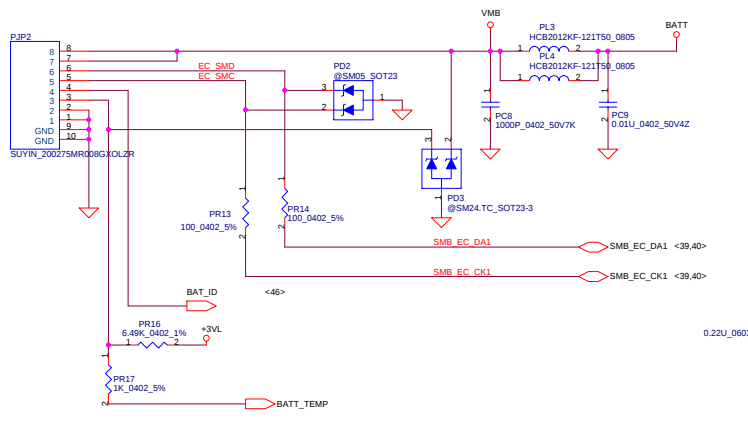
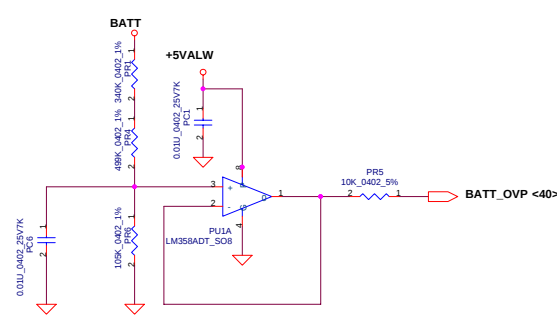
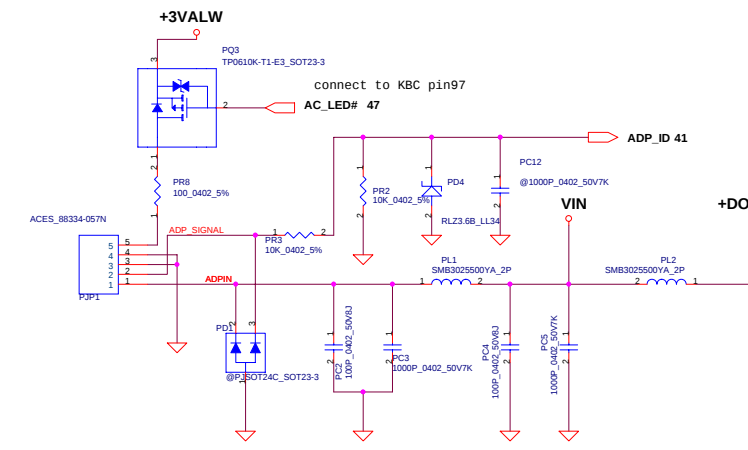
Discharge circuit



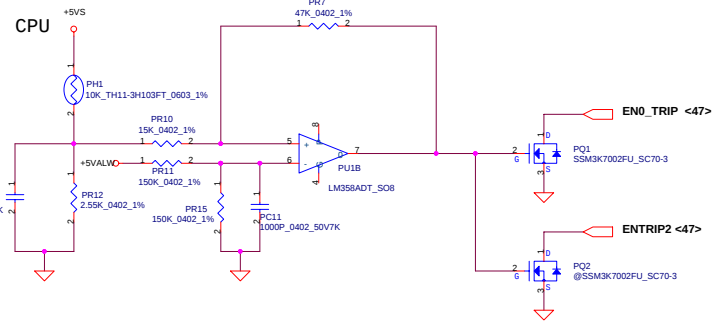
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	DC/DC Interface
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Date	Monday, February 25, 2008	Sheet	48	of 53



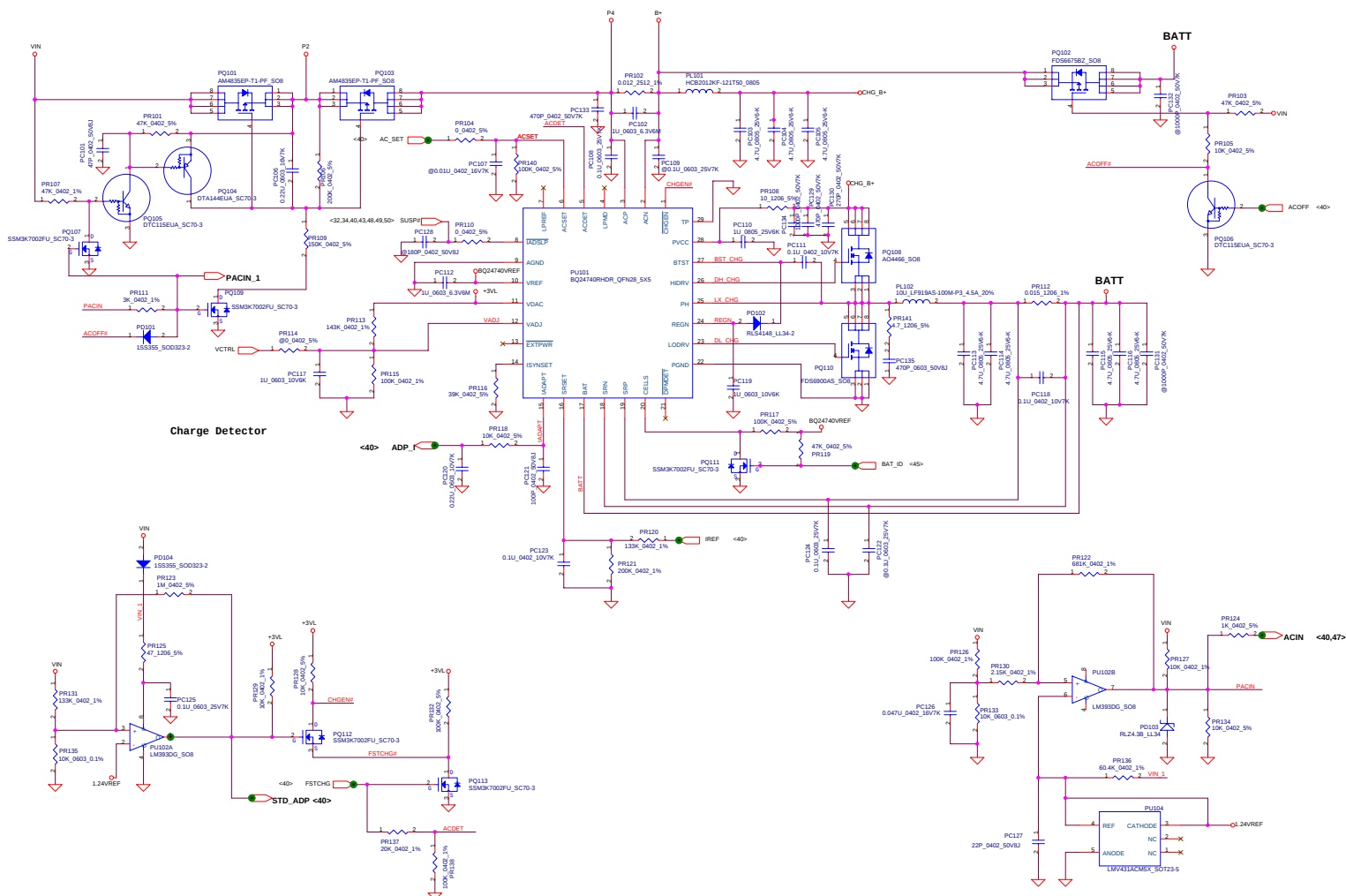
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				Document Number
				Custom
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
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				42 of 53



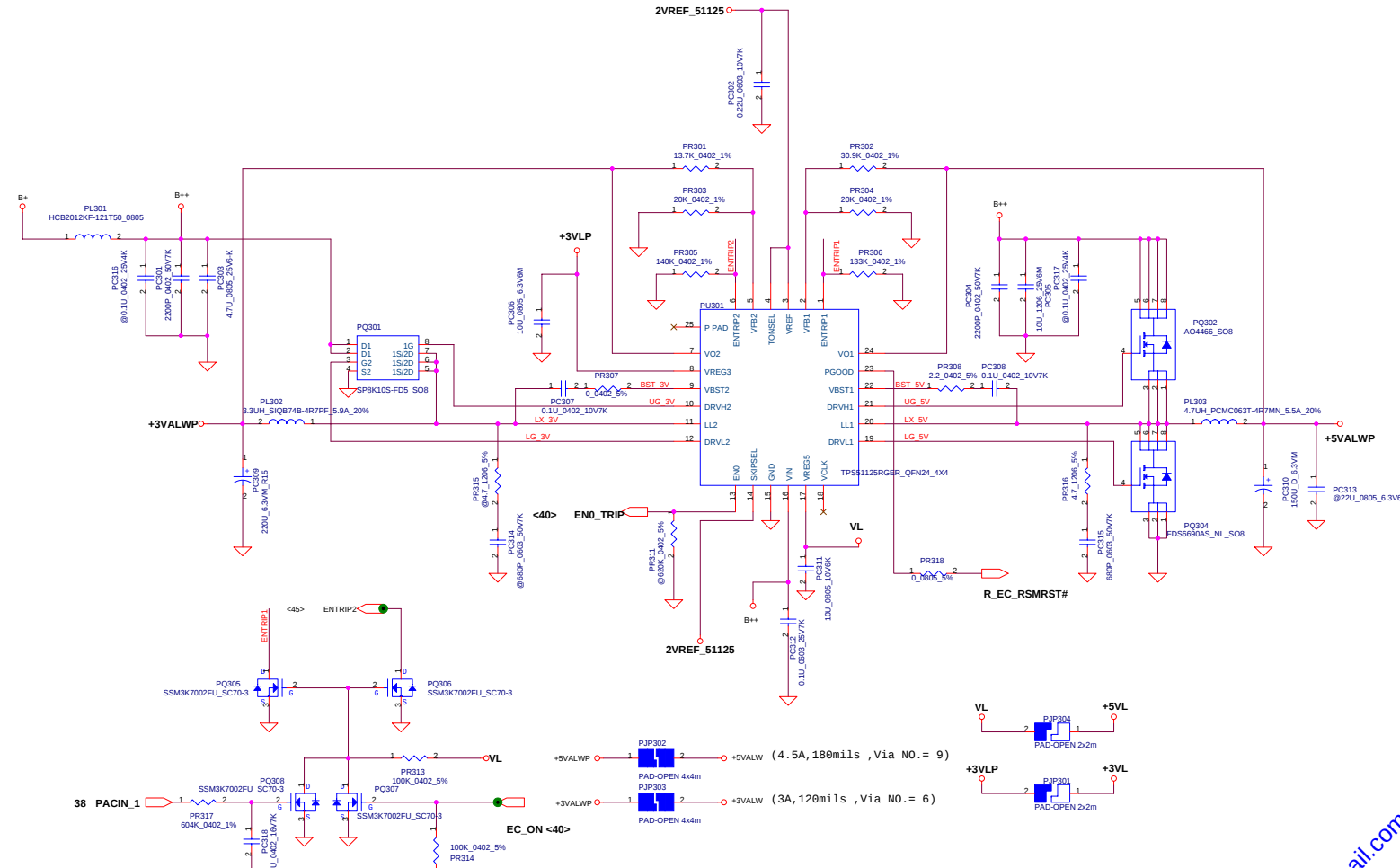
PH1 under CPU bottom side :
CPU thermal protection at 90 +3 degree C
Recovery at 47 +3 degree C



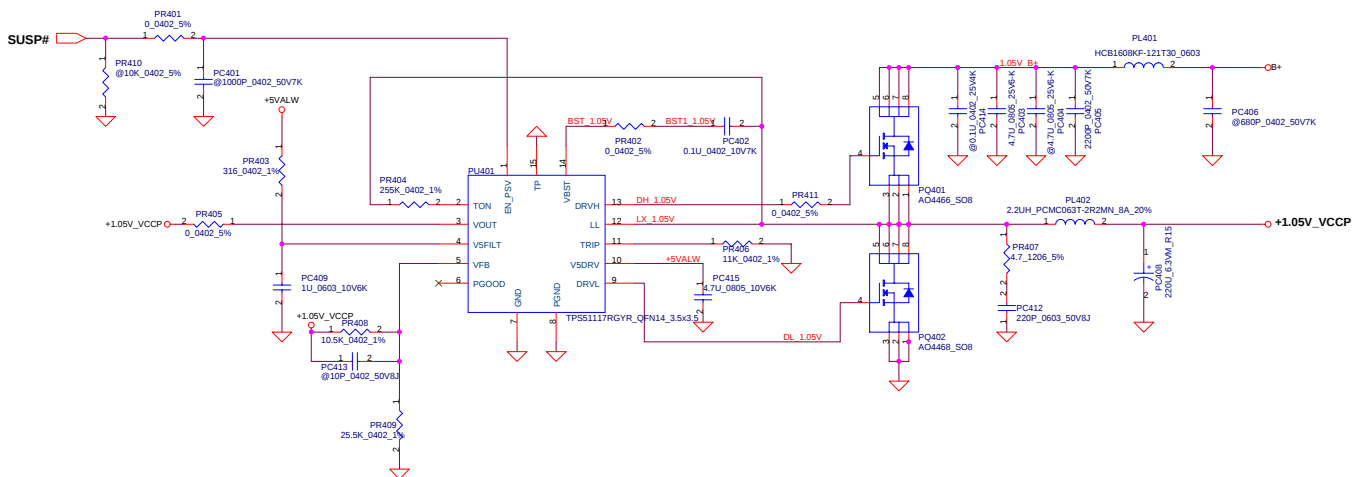
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	Title	DC Connector/CPU OTP
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Charger				LA-4102P Blade discrete	0.4
Date: Monday, February 25, 2008				Page	34

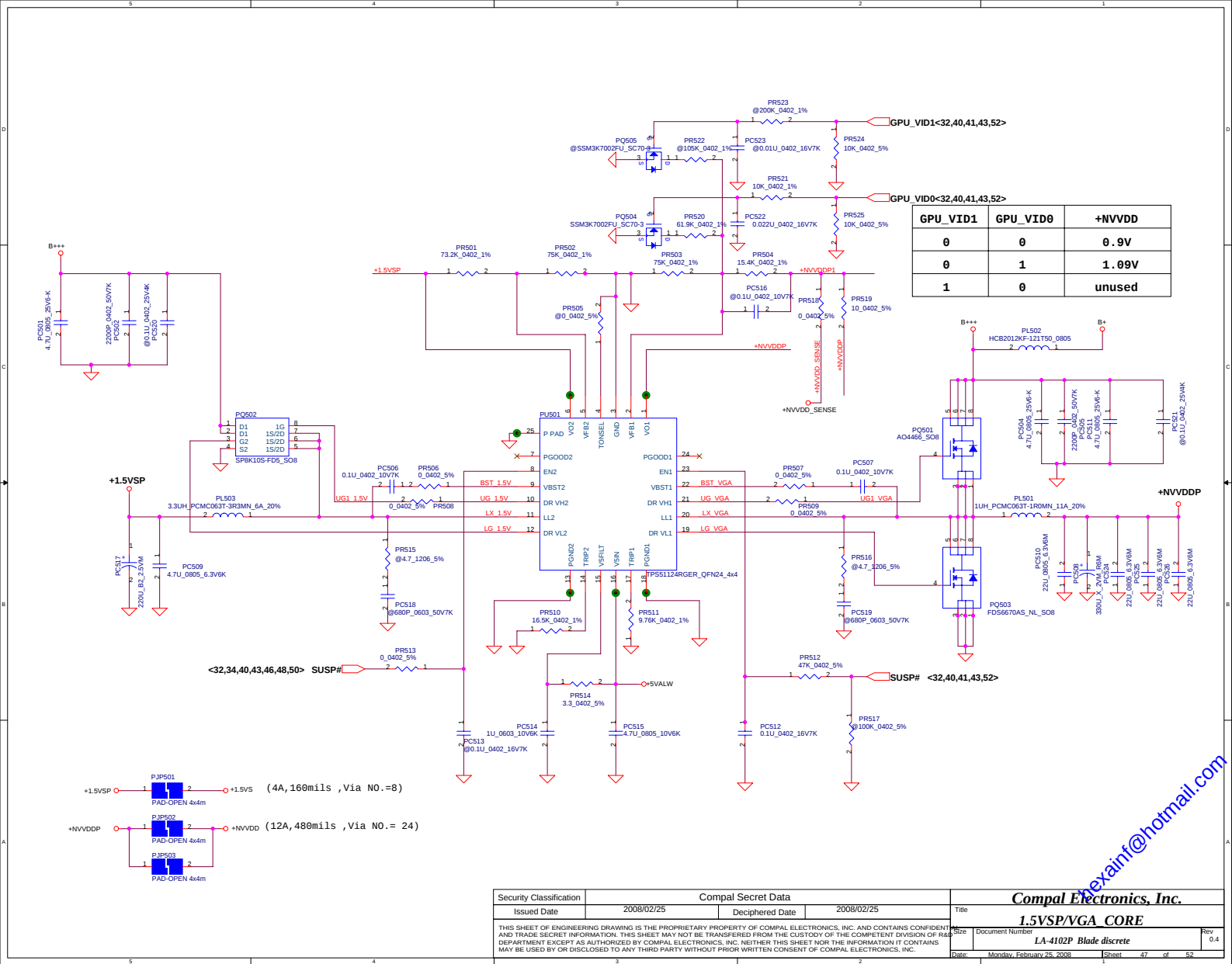


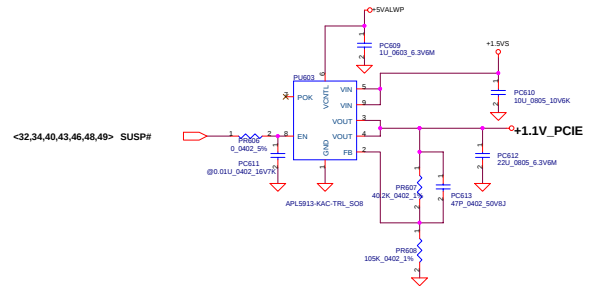
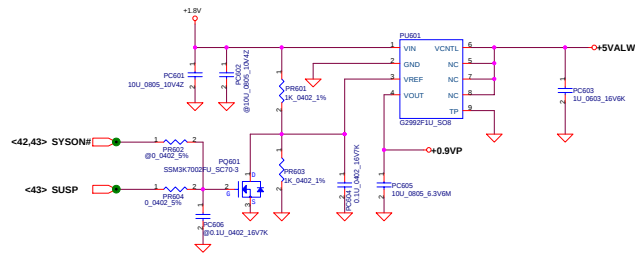
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		3.3VALWP/5VALWP	
2008/02/25		2008/02/25		3.3VALWP/5VALWP	
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				Document Number	
				LA-4102P Blade dispo	
				Date	
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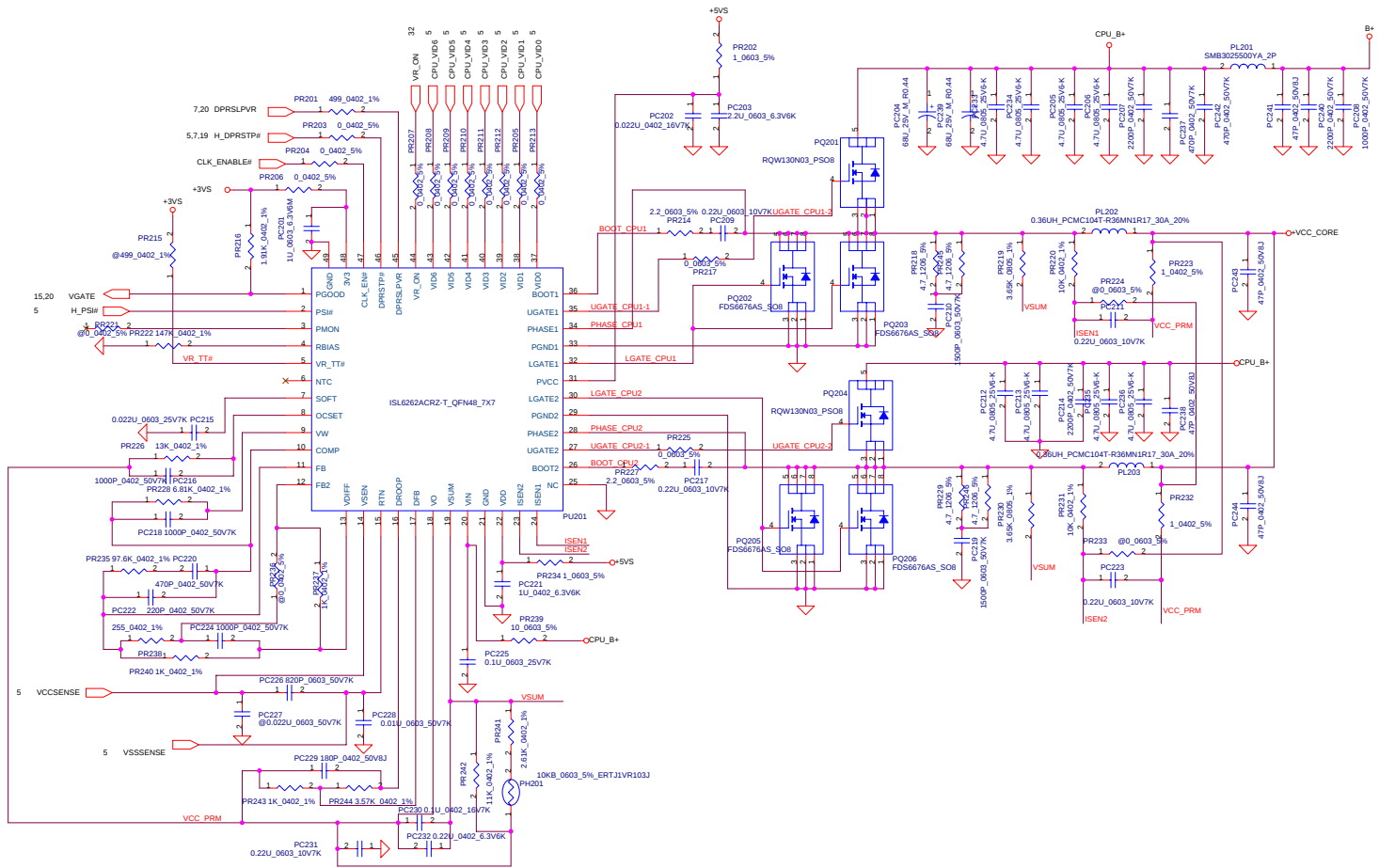
+1.05V_VCCP (6A, 240m11s , Via N0.=12)

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Issued Date	2008/02/25	Deciphered Date	2008/02/25	Title	1.05V VCCP
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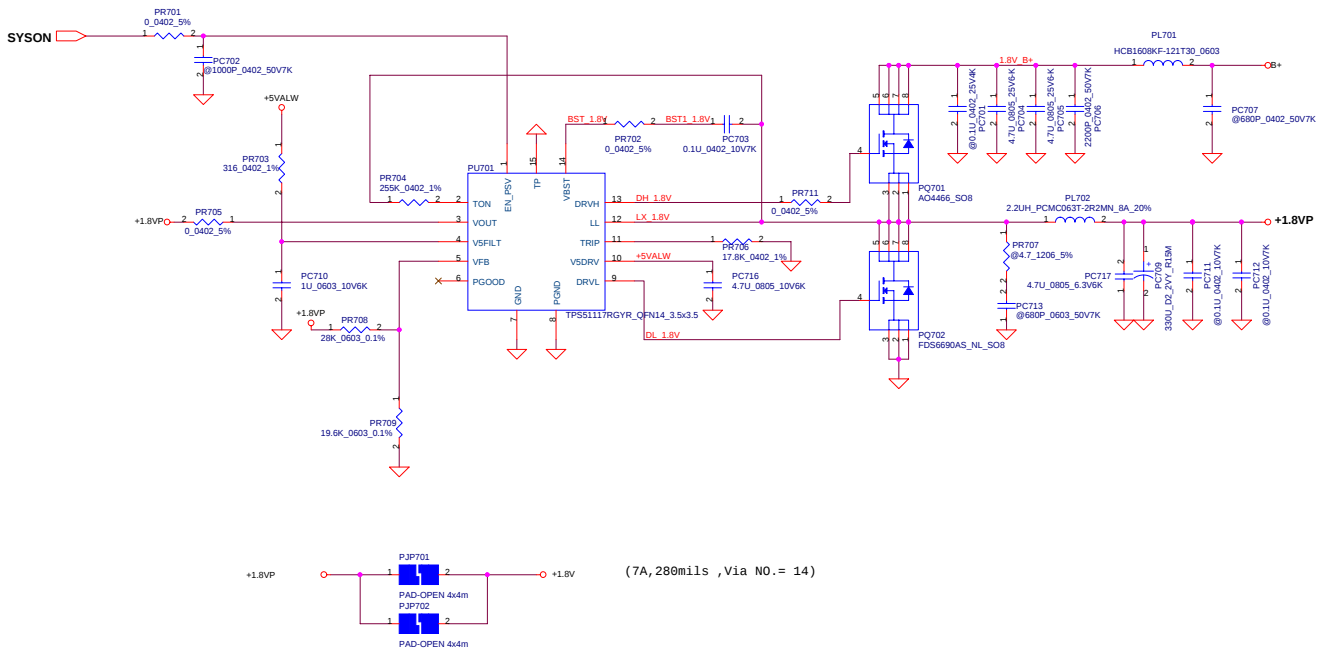


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Date: Monday, February 25, 2008				Rev: 04
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Compal Electronics, Inc.			
File	+CPU CORE		
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				Document Number	LA-4102P Blade discrete
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	43	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	45	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301, cancel PQ303.	
3	44	Charger	11/06	Compal	EMI solution	Add PC128	
4	49	CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	47	1.5VSP/VGA_CORE	11/06	Compal	for VGA voltage steps	Add PQ505, PR523, PR524, PR525	
6	45	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
7	44	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
8	49	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
9	47	+1.5VSP/VGA COREP	01/02	Compal	HW request	Change PR513 to 0_ohm	
10	44	Charger	01/02	Compal	EMI solution	Add PC135 and PR141	
11	49	+CPU_CORE	02/15	Compal	Change high-side MOS for WWAN	Change PQ201 and PQ204 to powerpak	
12	43	DC Connector /CPU_OTP	02/15	Compal	AC LED change to KBC control	ACLED# connect to EC pin 97	
13	43	DC Connector /CPU_OTP	02/19	Compal	WWAM issue	add PC241 47pF	
14	49	+CPU_CORE	02/19	Compal	WWAM issue	add PC243 PC244 47pF	

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Compal Electronics, Inc.
Power Changed List History-1
 LA-4102P *Rev. 0.4*
 Monday, February 25, 2008

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41, C42, C43, C44 Change ESR=7m ohm	11/21	DB
2	Disable TV out function from Docking	20	TV signal unconnected,DACB_VDD pull low 10K (R948).	11/07	DB
3	Update Connetor Library		CRT(JCRT1), HDMI(JHDMI1), ESATA(JP53), Finger print(JJP24), FAN(JP2), Speaker(JP60), Multi bay(JP12), Dual LED(D53, D54	11/17	DB
4	Delete LVDS B channel	19,20	Schematic Delete	11/17	DB
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K , R1093=100K,Add GPIO 20 to turn off power	11/07	DB
6	Reserve Card reader D3E function	27,32	GPIO6= CR_CPPE#, GPIO22=CR_WAKE#	11/17	DB
7	Swap PCIE LAN and New card	27	Swap PCIE4 and PICE6	11/17	DB
8	Change GPU 1.8VS power	20, 21	Change 1.8VS to +VDD_MEM18	11/17	DB
9	Change G sensor control from SB, LED drive by +5VS	27, 39	Change G sensor control from SB	11/17	DB
10	Avoid Battery mode can't boot issue	38, 45	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	DB
11	Add G sensor ST and Bosch	37	Add G sensor ST and Bosch	11/17	DB
12	Change LAN solution (Marvell to Realtek)	30	Change LAN solution (Marvell to Realtek)	11/17	DB
13	LAN transformer interfere	30	U19 Change to correct transformer type	11/17	DB
14	Cardreader schematic review,add D3E function	32	R709-->10K, R1047-->8.2K, R1128-->Stuff, R705-->@, U37-->@, Cardreader LED-->+5VS, add D3E function	11/17	DB
15	Jack can't detect normal	33	R1059 change from 39.2 to 39.2K	11/17	DB
16	Docking can not power on	40	Add power on circuit D57,Q13R751,R752,R753	11/17	DB
17	HP audio team recommend	33, 35	C1480-C1487, C1352, C1354 change to 0.022U, Amp output setup to 15.6 dB, Reserve C747, C748 for GNDA and GND	11/17	DB
18	Audio jack can't detect normal	35	Add Pull up resistor R750 to +3VALW	11/17	DB
19	Docking HP audio test fail	35	Add C795, C796 to avoid DC level, and add R968, R969 to reduce HP out level	11/17	DB
20	Leakage problem	38	Correct direction prectek leakage	11/07	DB
21	EC pin define update	38	Delete EC_PME#, SYSON PU, SUSP# PU, LID_SW# change to +3VALW, Delete CLKRUN#, R582->@ for C0 chip, C0R PU+5VL, add 100P to BATT_OVP(EC recommend)	11/07	DB
22	Can't Hibernation(SLP_S4#)	38	Connect SLP_S4# to SB	11/17	DB
23	EC can't receive docking present	40	CONA# change +3VL	11/12	DB
24	Reserve capacitor on digital MIC for EMI request	19	Add C496,C498	11/07	DB
25	Add 2N7002 to GND on HDMI to avoid leakage.	21	Add Q74	01/04	SI
26	+VDD_MEM18 to +1.8VS, change to jummpers	22	Delete R1124,R1125 add PJP605	01/04	SI
27	HDCP ROM fail. HDCP_SCL need pull high.	22	R224 no stuff. R213 stuff.	01/04	SI
28	Reserve capacitor on digital MIC for SED, WWAN noise	26	Add C499,C502	01/04	SI

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Change transformer vendor	30	change U19 library	01/04	SI
2	XMIT_OFF add a diode to avoid leakage.	31	Add D88	01/04	SI
3	Card reader recommend	32	XD_ALE need pull +3VS not pull low.	01/04	SI
4	change Q54 from transistor to MOS for cardreader LED.	32	Change Q54	01/04	SI
5	speaker pop issue	35	Change C1488 to 1U	01/04	SI
6	Reserve capacitor on SPI_FSEL#,CLK#,FER for EMI request	36	Add C2125,C2126,C2127	01/04	SI
7	Change EC_PME pull high from +3VL to +3VALW	38	R585 stuff	01/04	SI
8	Reserve damping resistor on SPI_CLK for EMI request	38	Add R191	01/04	SI
9	WLAN LED issue,WL_BLUE_LED# pull +3VS	39	Add R716	01/04	SI
10	Add bypass capacitance on sensor bottom	39	Add C261(4.7U)	01/04	SI
11	EC can't detect DOCK_PRESENT.	40	change R754 to 22 Ohm,R623 to 2K	01/04	SI
12	Add DOCK_VOL_UP#,DOCK_VOL_Down# pull +3VS	40	Add R594,R596	01/04	SI
13	SPDIF issue	40	follow Vader	01/04	SI
14	Docking CRT blurred	40	Change ping 31,39,22 connect to GND	01/04	SI
15	Change R650 and C770 to modify the power sequence	41	change R650 to 1K, C770 to 0.1u	01/04	SI
16	Add 12P on CLK_14M_ICh for WWAN noise	17	Add 12P on CLK_14M_ICh	02/15	PV
17	BKOFF# reserve pull low 10K	19	reserve R717	02/15	PV
18	Reserve CMD27 to support 64M X16	7,8	Reserve CMD27 to support 64M X16	02/15	PV
19	Reserve cap on HDA_BITCLK for WWAN noise issue	26	Reserve cap on HDA_BITCLK	02/15	PV
20	Reserve to prevent ESD issue	30	Reserve ESD diode on LAN LED pin	02/15	PV
21	Change WLAN and WWAN 0402 resistor to 0805	31	Change WLAN and WWAN 0402 resistor to 0805, and WLAN change to +3VS power plane	02/15	PV
22	Direct drive LED, and add D3E function diode	32	Direct drive LED and XD_ALE Pull L, and add D86 for D3E function	02/15	PV
23	Change R1092 value on BT power switch Gate	36	Change R1092 to 10K	02/15	PV
24	Correct AC_LED control by EC	38	AC_LED Change controll by EC	02/15	PV
25	Change all LED limit current resistor to 200 ohm	39	Change all LED limit current resistor to 200 ohm and add Touch pad LED for PR	02/15	PV
26	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	40	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	02/15	PV
27	follow check list ver:1.5	6	change R13 to 56 ohm;change R2~R8 to 51 ohm;change R11 to 0ohm	02/20	PV
28	Reserve Cap for EMI	42	add C1250,C1249	02/20	PV

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	follow check list Ver:1.5	17	reserve R148	02/15	PV
2	follow check list Ver:1.5	9	change R45,R48 to 10K	02/15	PV
3	boot code "88" power sequence fail	27	add Diode from PWROK to RSMRST	02/15	PV
4	Change BT,LAN,DOCK,Multibay connect for DFX			02/15	PV
5	Change WWAN and WLAN LED	39		02/15	PV
6	For EMI	37	SPI_CLK add R2118 , R2119 , R2120 => 33ohm add C2125 , C2126 , C2127 => 22pF;R553, 554, 556 =>10ohm	02/15	PV
7	For EMI	30	LAN add C656 and C657 => 0.1uF	02/15	PV
8	For EMI	39	T/P add D28 and C729	02/15	PV
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