Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_PM+ICH9-M core logic

LA-4082P Vader Discrete (NB9P-GS,NB9M-GE)

2007-12-26 Rev 0.4

機密 等級 研發二部 產品人員 產品日期 解密日期

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: *Cover Sheet*

Size: Custom | Document Number: *LA-4082P Vader Discrete* | Rev: 0.2

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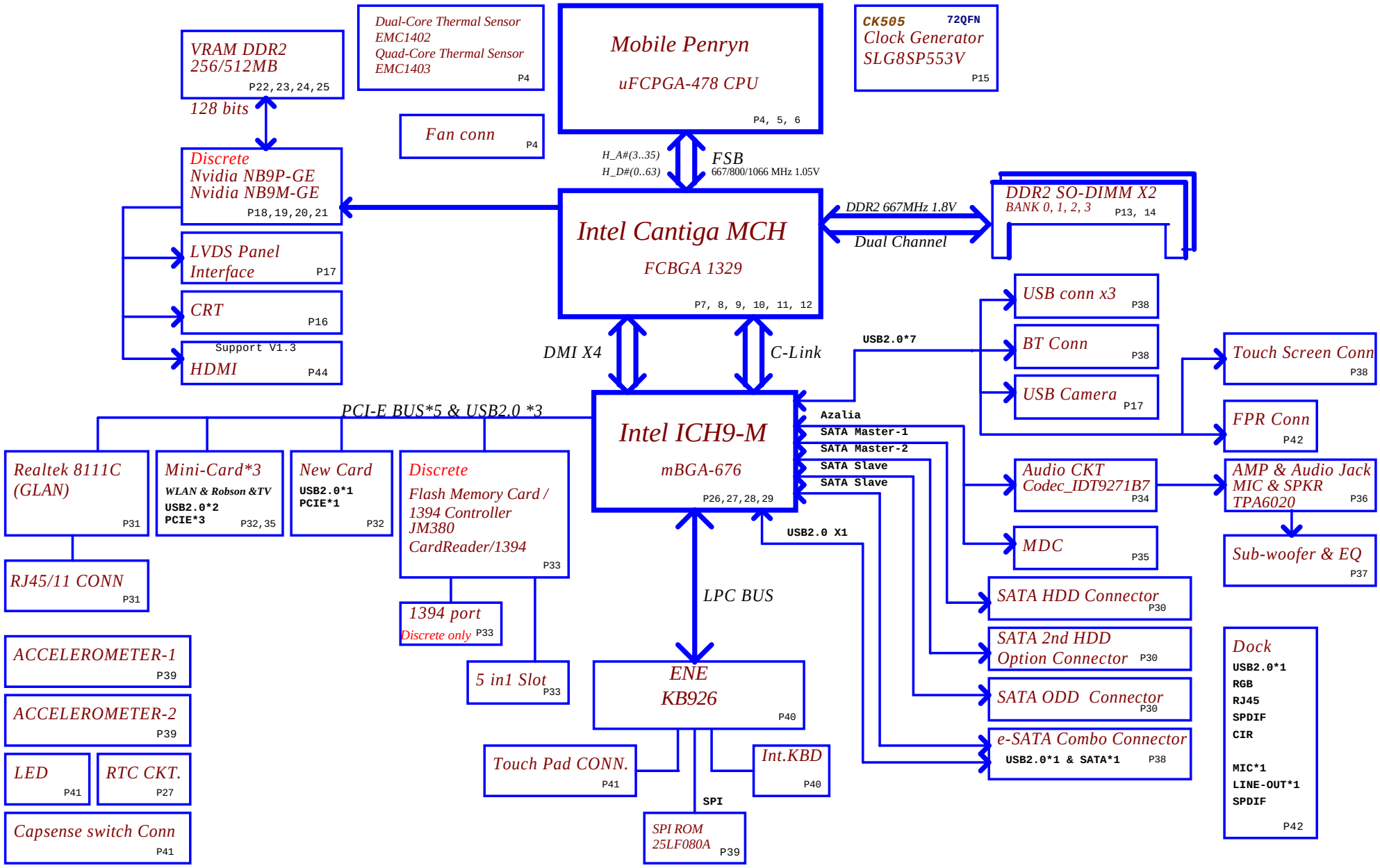
Montevina Consumer Discrete



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Block Diagram			
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
DDC2_CLK DDC2_DATA	NB9M	X	X	X	X	X	X	X	V	X

USB assignment:

USB-0 Right side
USB-1 Right side
USB-2 Left side(with ESATA)
USB-3 Dock
USB-4 Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Finger Printer
USB-8 MiniCard(WWAN/TV)
USB-9 Express card
USB-10 X
USB-11 X

PCIe assignment:

PCIe-1 TV tuner/WWAN/Robeson
PCIe-2 X
PCIe-3 WLAN
PCIe-4 New Card
PCIe-5 Card reader
PCIe-6 GLAN (Marvell)

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X
24C16	A0H	1010 000X
CAP BOARD -- Cypress	38H	
CAP BOARD -- ST	b0H	

EC SM Bus2 address

Device	HEX	Address
CPU EMC1402	4CH	1001 1000b
VGA	4DH	1001 1010b

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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Title: Notes List
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ITP-XDP Connector

1025 For Support Dual core and Quad core

Removed at 5/30.(Follow Chimay)

Change value in 5/02

This shall place near CPU

Place R191 within 200ps (~1") to CPU

Place TP with a GND 0.1" away

Delete H_PROCHOT# off-page due to VR doesn't have it's input pin @08/31

10708 follow Intel suggestion to change value

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mils

H_THERMDA2, H_THERMDC2 routing together, Trace width / Spacing = 10 / 10 mils

1025 For Support Dual core and Quad core

CPU	GTLREF_C	GTLREF2
Dual core (DC)	GND	0V
Quad core (QC)	Floating	2/3Vtt

PWM Fan Control circuit

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Compal Electronics, Inc.

Title: Penryn(1/3)-AGTL+/ITP-XDP

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

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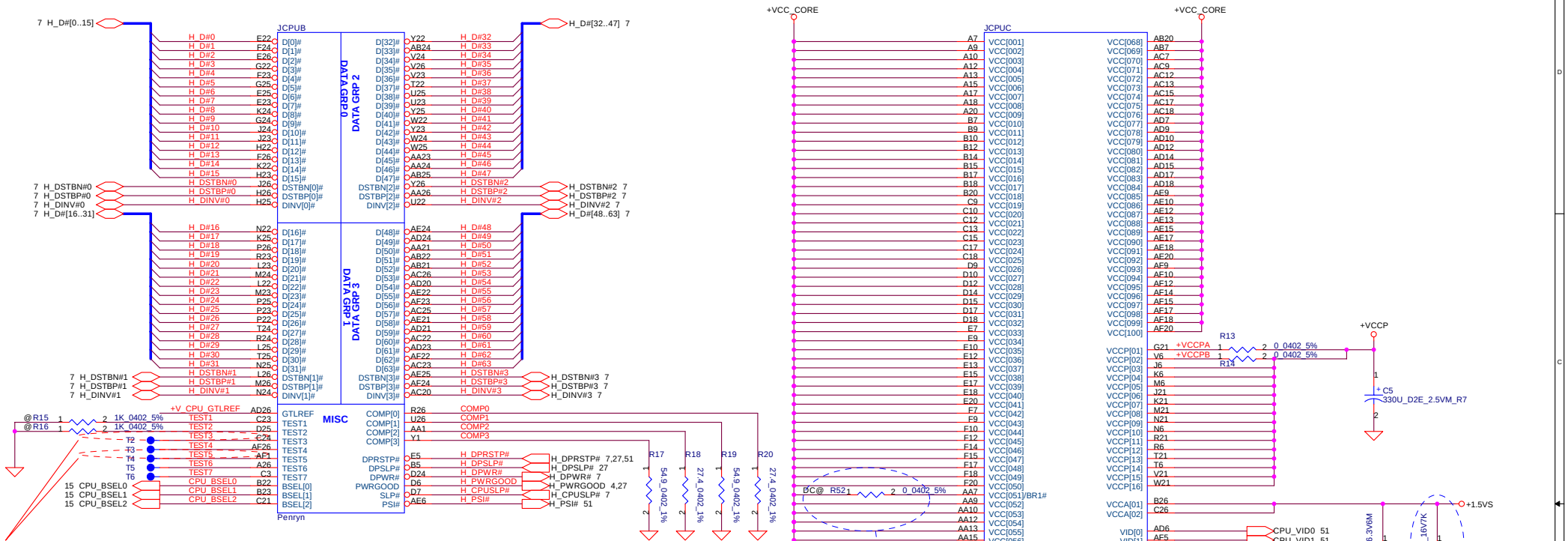
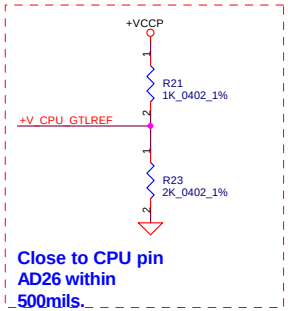


1025 For Support Dual core and Quad core

*** Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.**

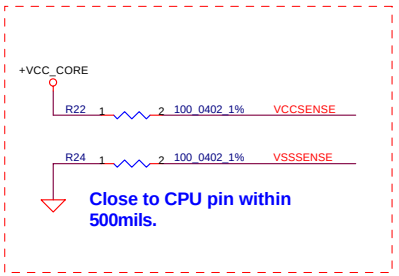
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Close to CPU pin AD26 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: **Penryn(2/3)-AGTL+/ITP-XDP**

Size	Document Number	Rev
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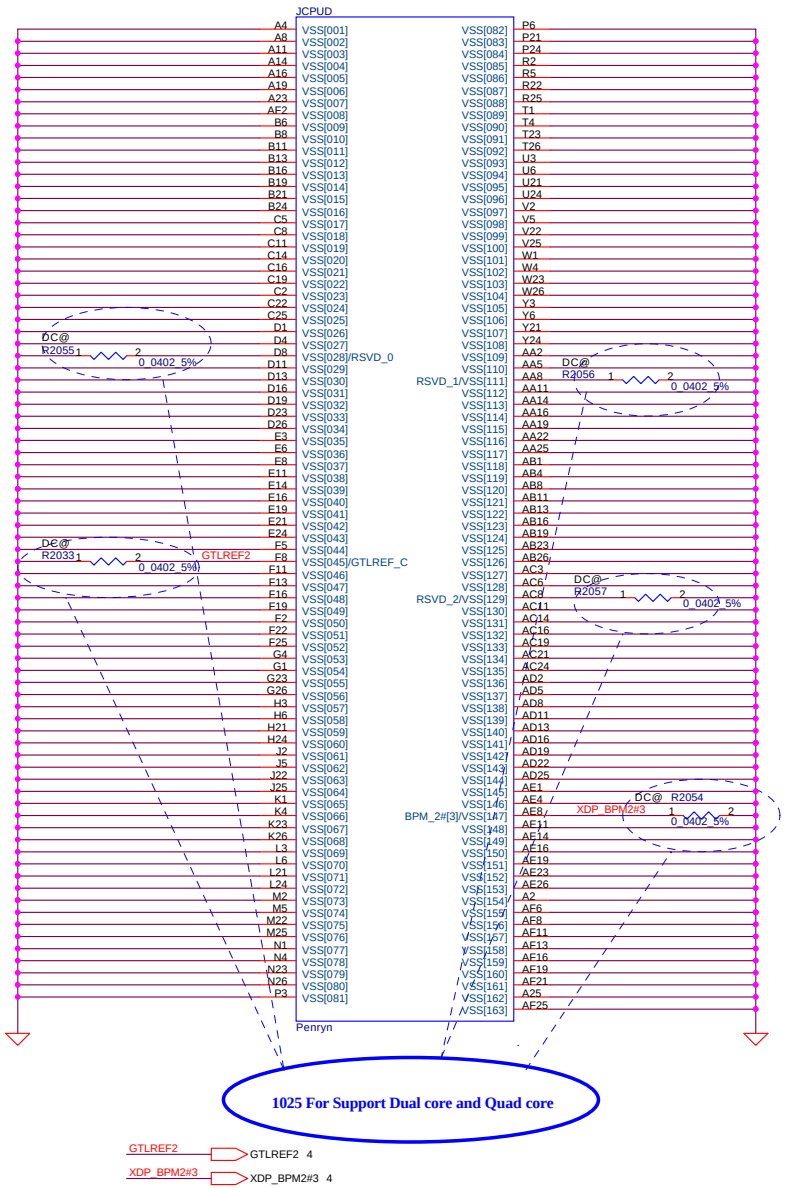
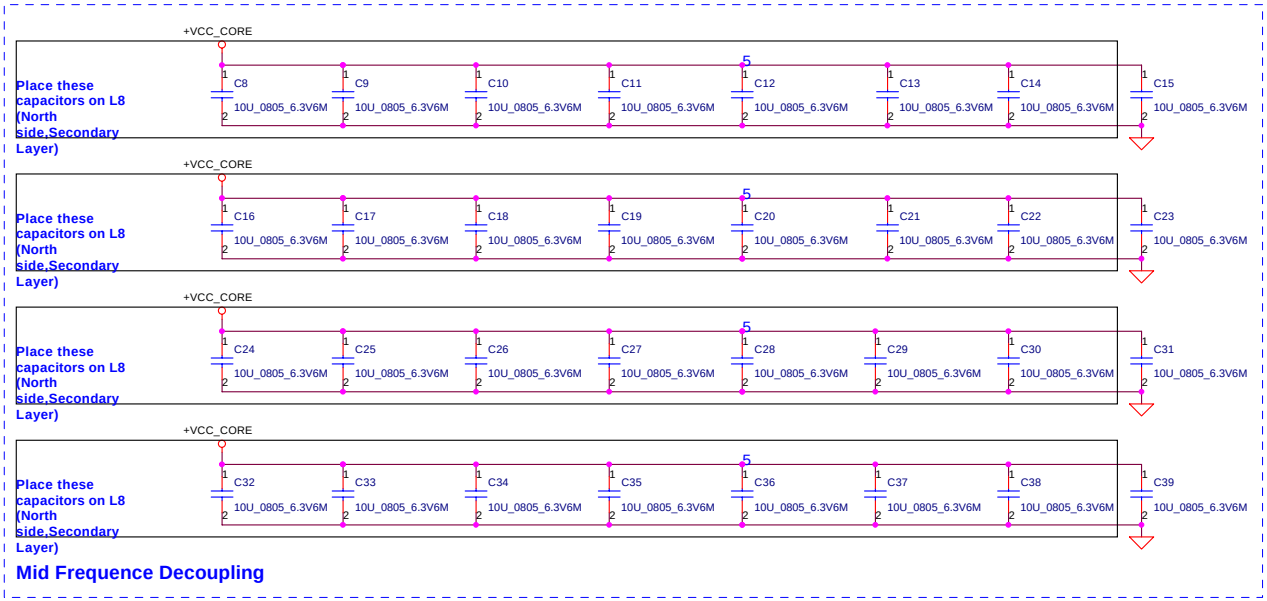
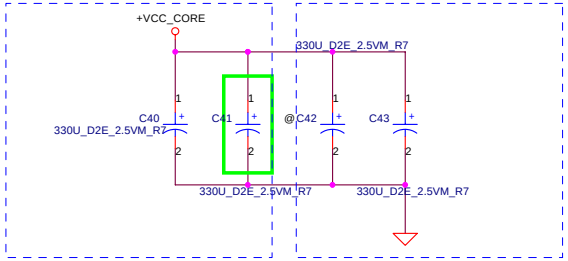
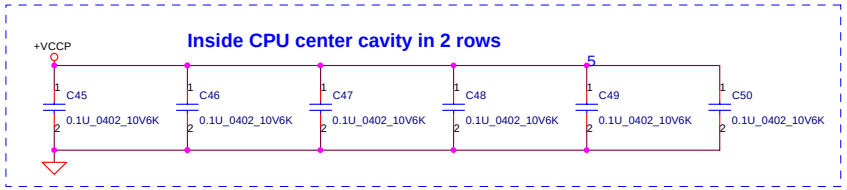




Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF





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Compal Electronics, Inc.

Title: **Penryn(3/3)-AGTL+/ITP-XDP**

Size	Document Number	Rev
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U57A

HOST

CANTIGA ES_FCBGA1329

U57B

RSVD

DDR CLK/ CONTROL/COMPENSATION

CLK

CFG

DMI

GRAPHICS VID

PM

ME

MISC

NC

HDA

CANTIGA ES_FCBGA1329

layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC

Follow Design Guide For Cantiga: 80.6ohm

1009 Follow Design Guide

1015 Follow Design Guide

0621 add CLK and DAT for DVI

0906 delete

0830 Add pull-up and pull-down resistor.

*R37*Follow Intel feedback

Delete Off-page @1028

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **Cantiga(1/6)-AGTL/DMI/DDR**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

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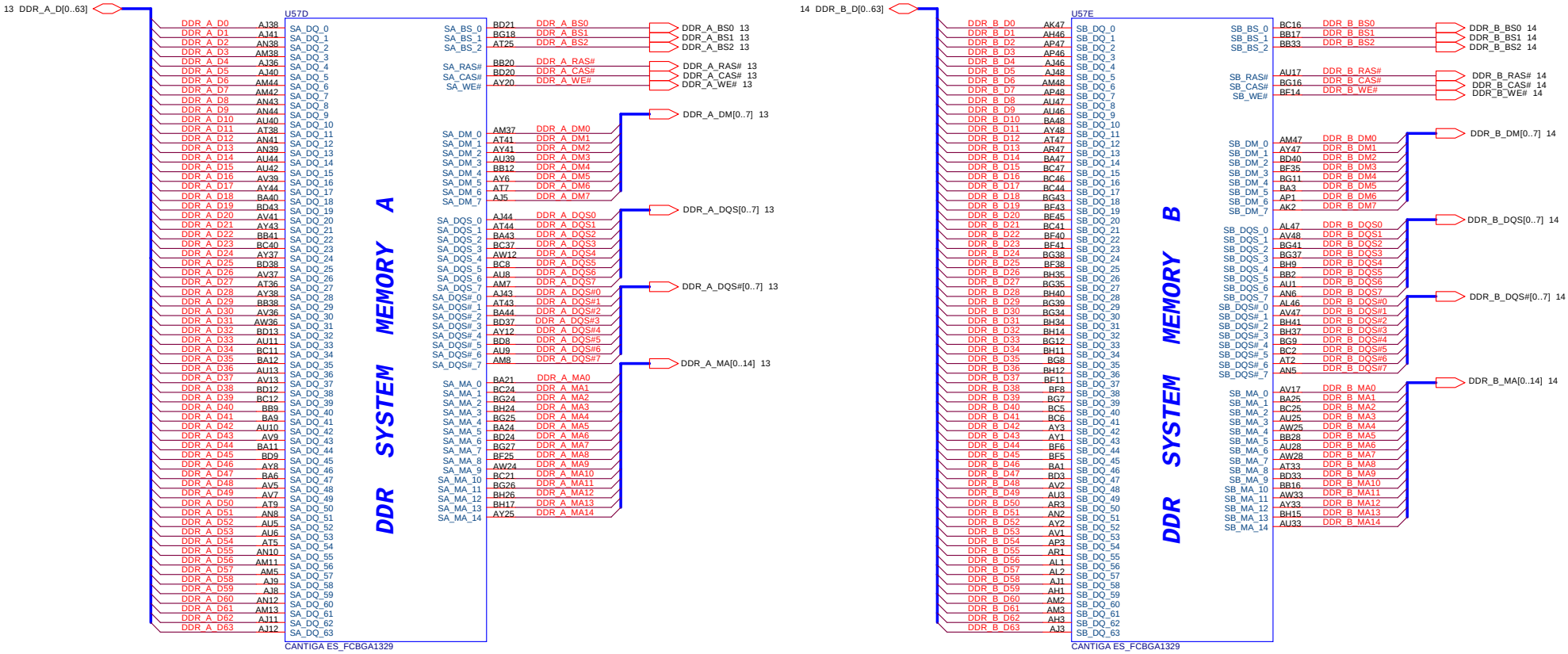

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

Size	Document Number	Rev
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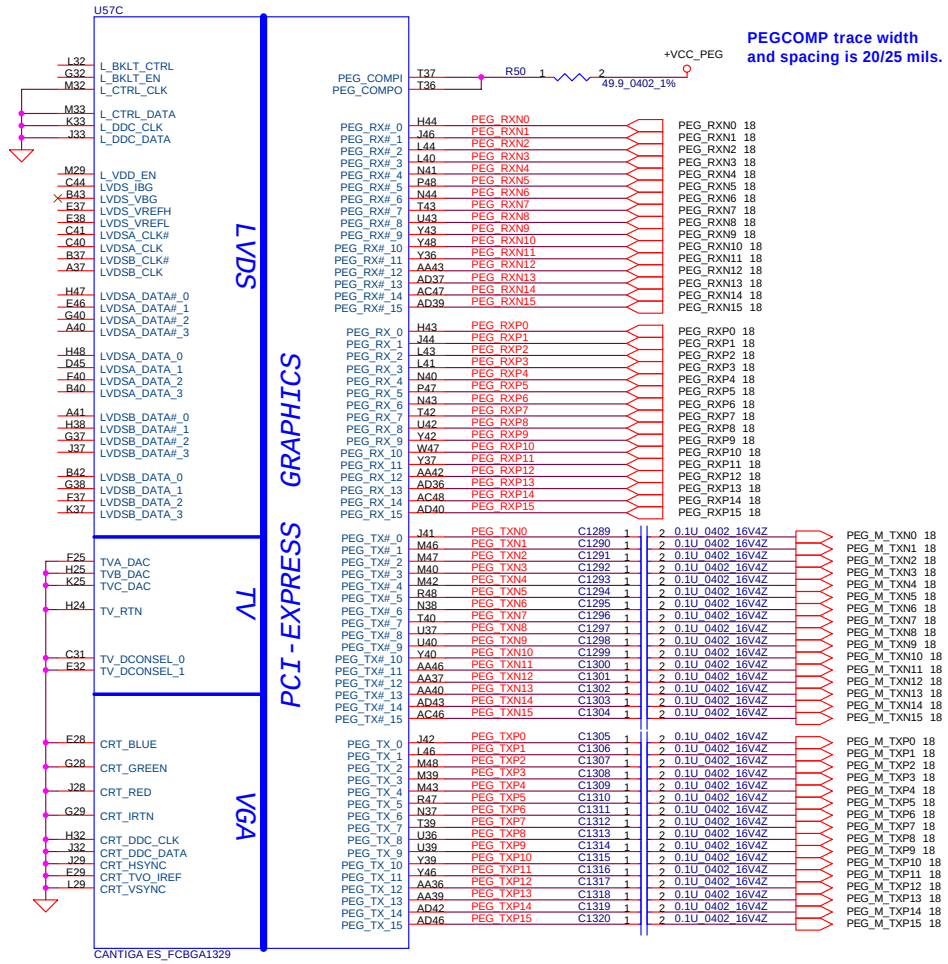
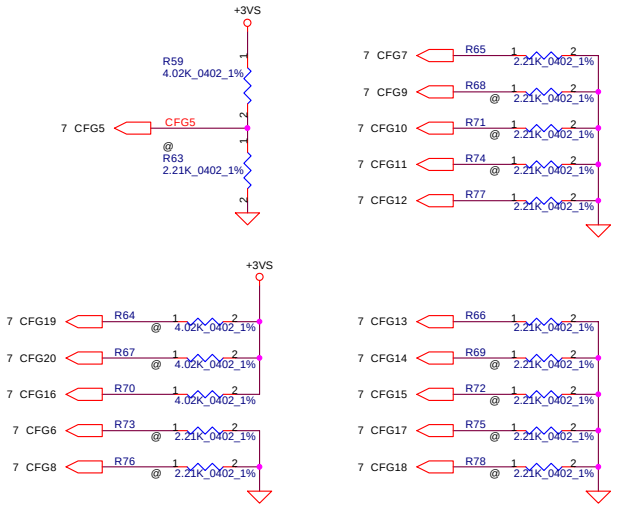


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz Selected By CPU 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
~~CFG6~~	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	Cantiga(3/6)-VGA/LVDS/TV
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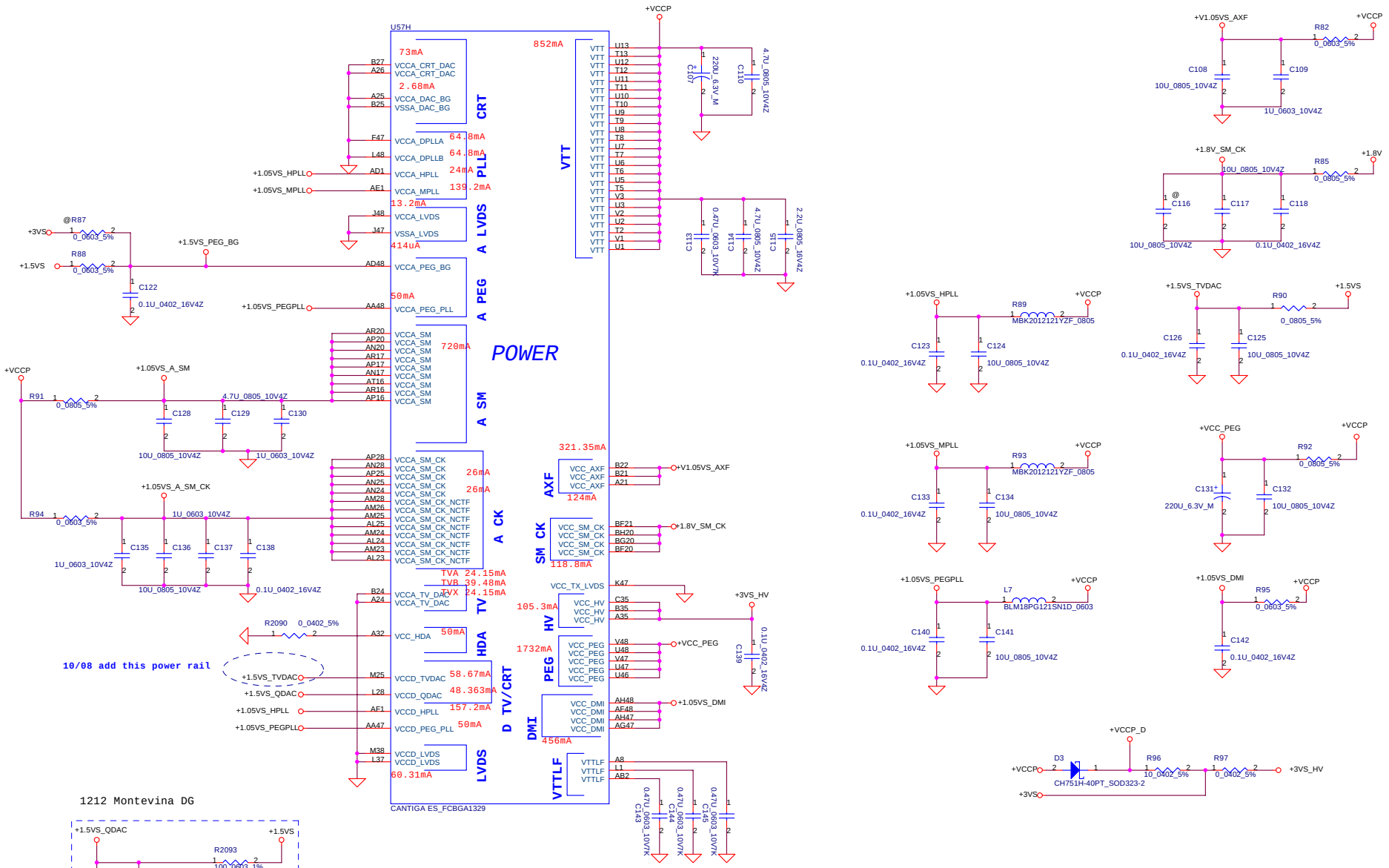

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(4/6)-PWR**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

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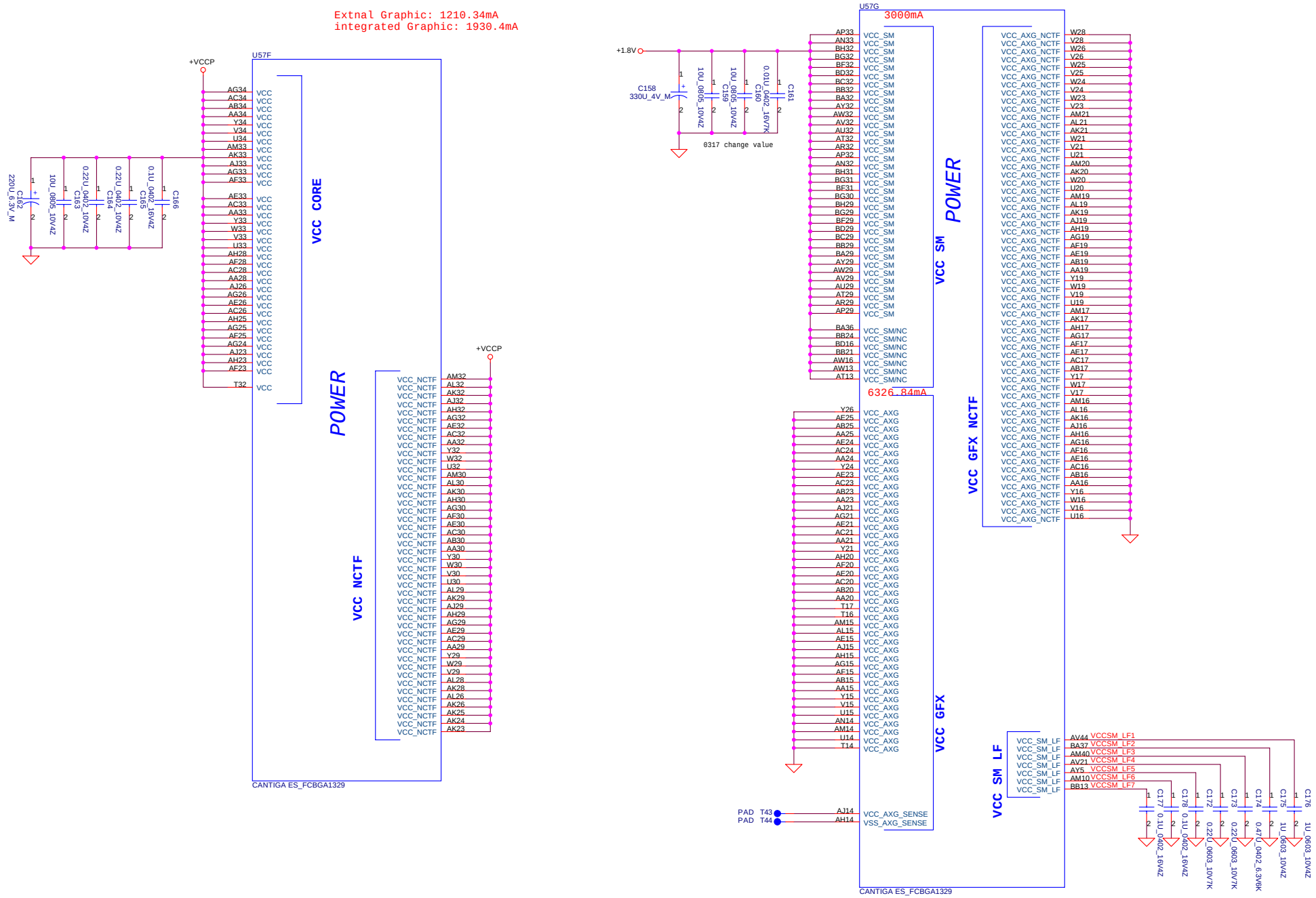

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(5/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

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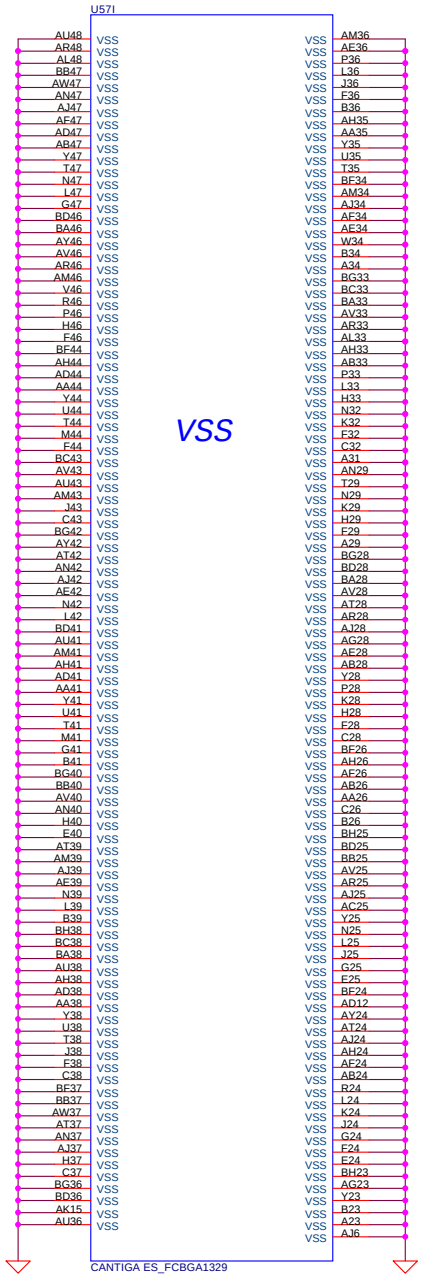

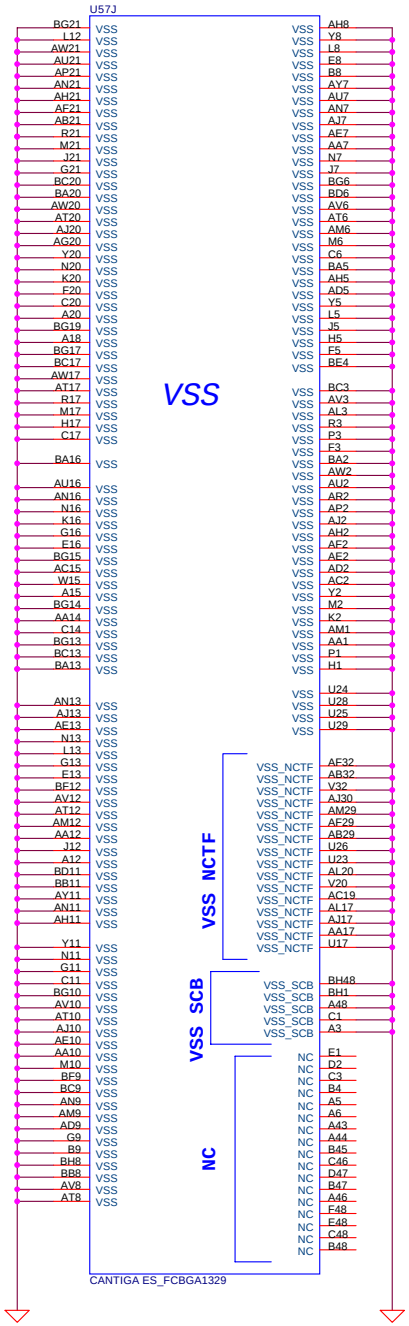

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(6/6)-PWR/GND**

Size	Document Number	Rev
Custom	*LA-4082P Vader Discrete*	0.2

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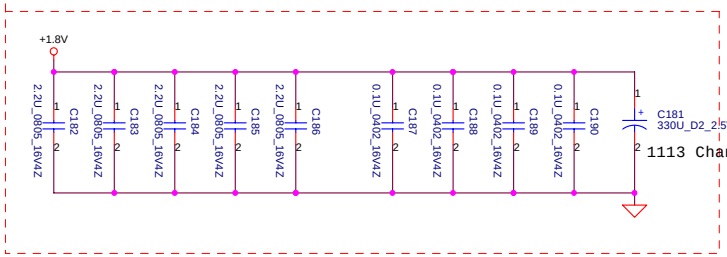
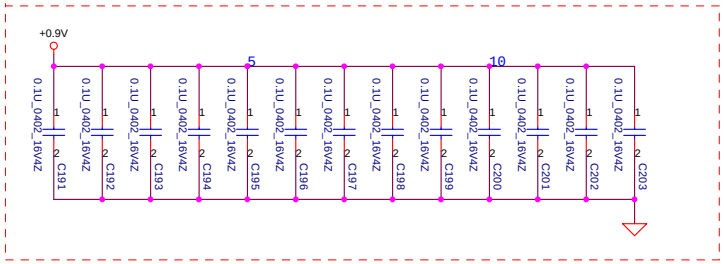
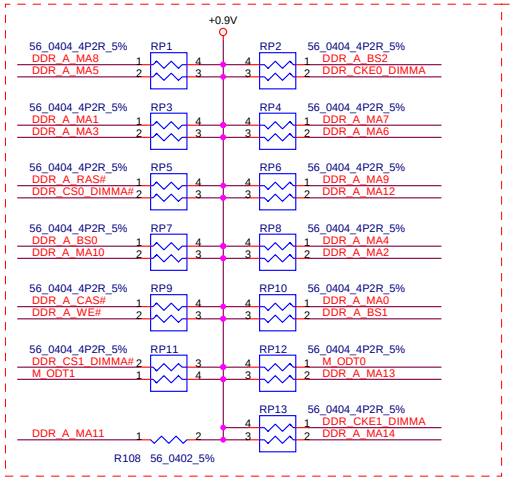
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..14]

Layout Note:
Place near JP3

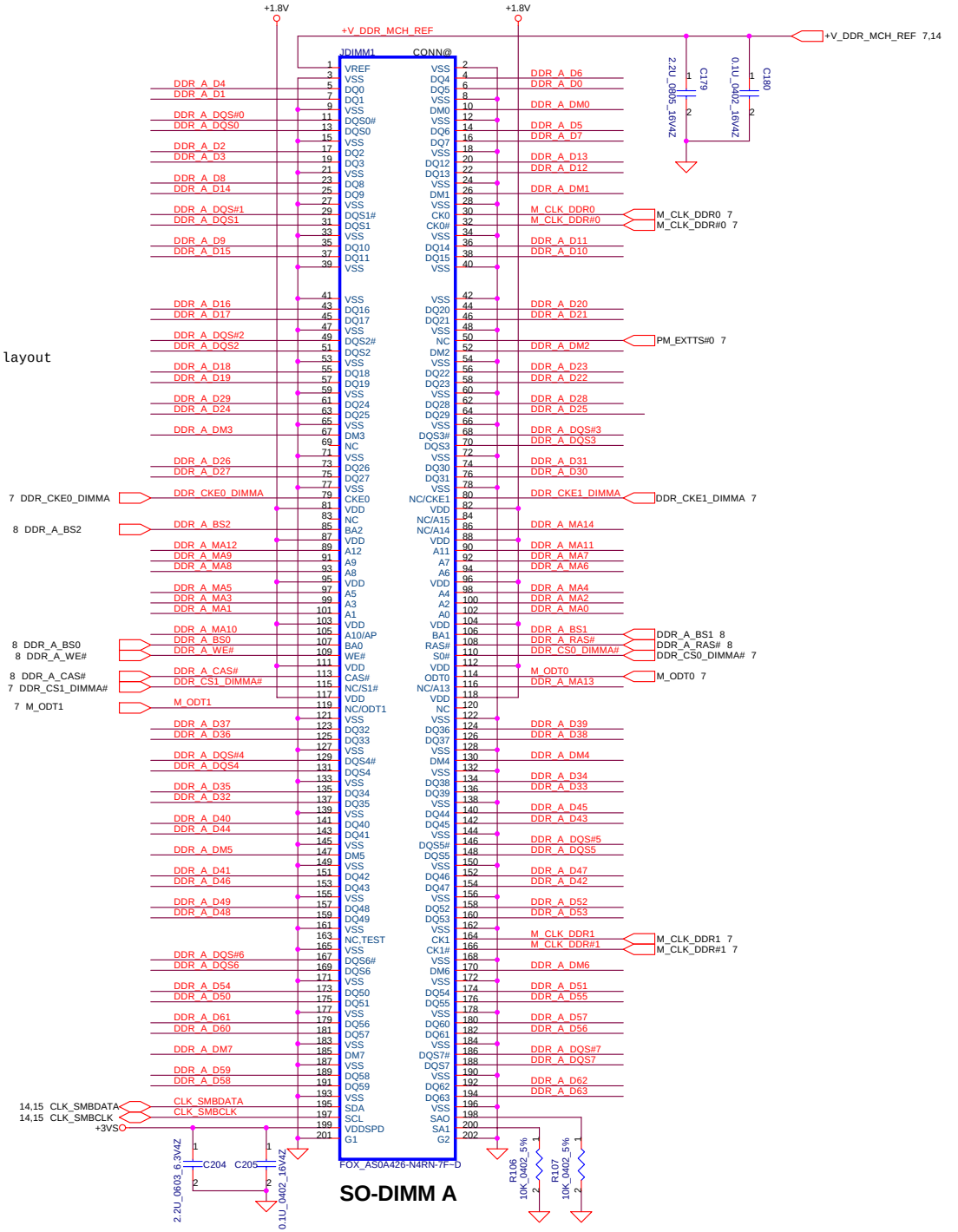


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS





Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

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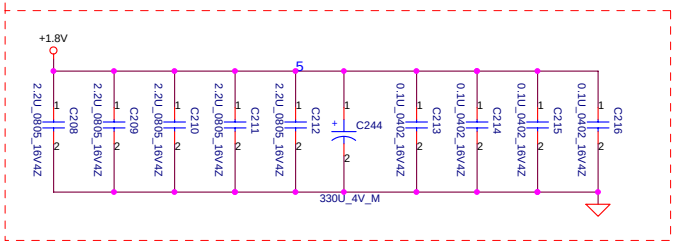
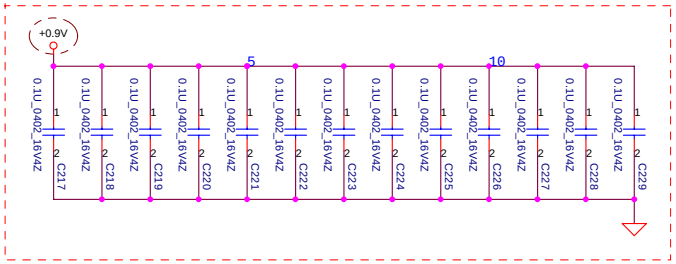
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..14]

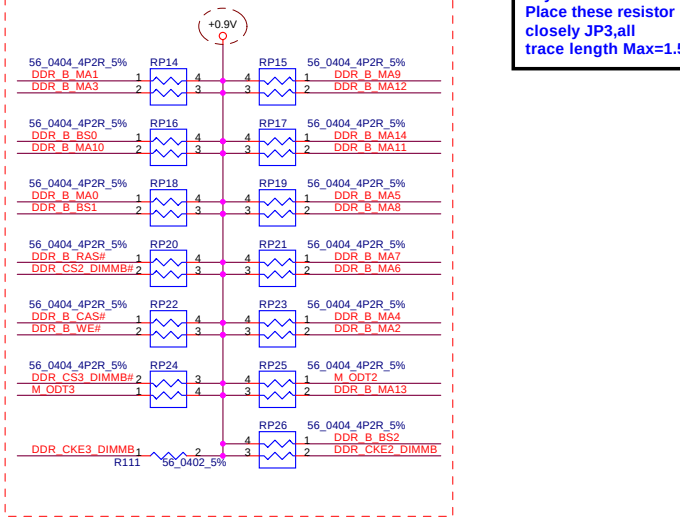
Layout Note:
Place near JP10

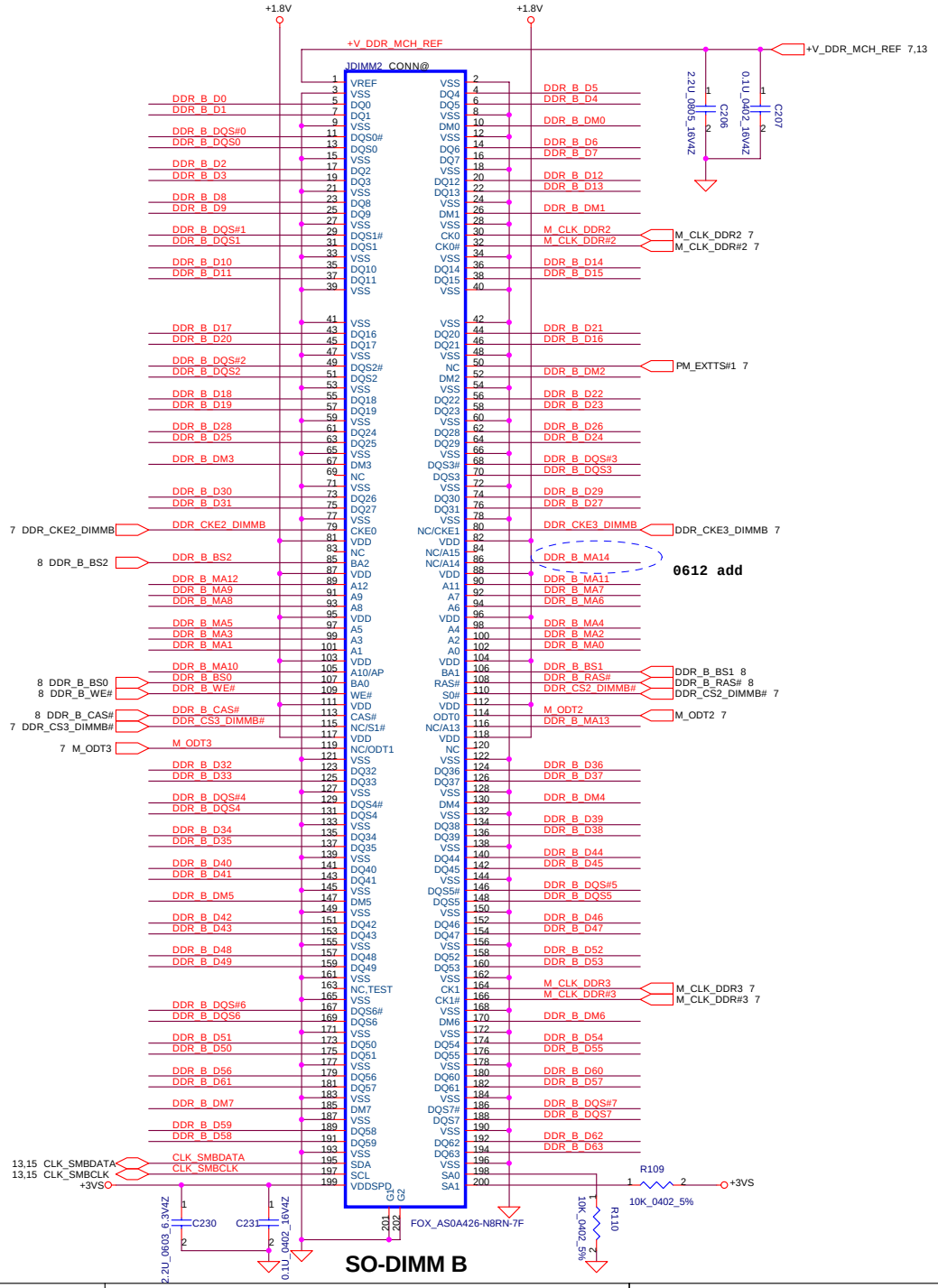


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

Size	Document Number	Rev
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

03/02 change

Routing the trace at least 10mil

Place close to U51

Vendor suggests 22pF

1025 Add R127 to meet Intel CLK design

1212 Add R and R

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

Security Classification	Compal Secret Data
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Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Clock Generator CK505

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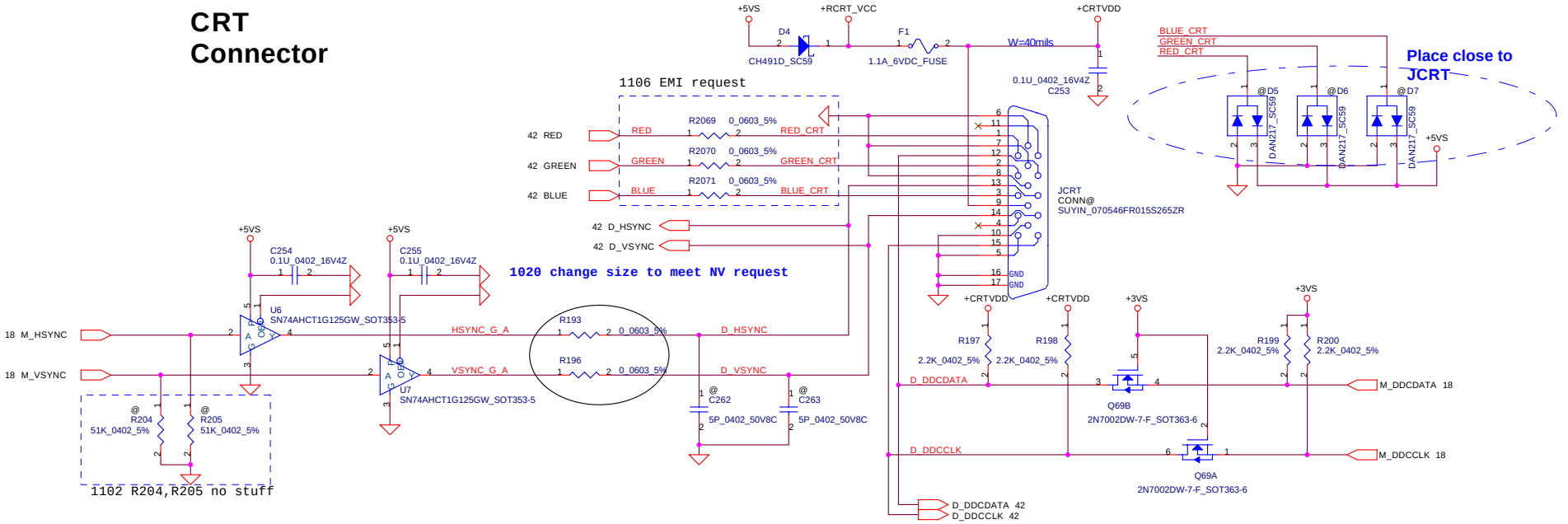
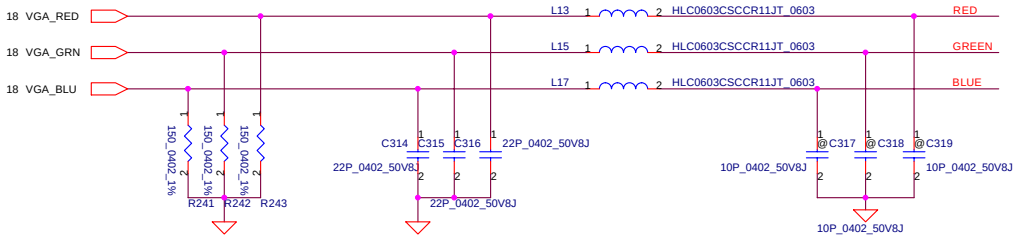
CRT Connector



CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: CRT Connector			
Size: Custom	Document Number: LA-4082P Vader Discrete		Rev: 0.2
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1108 EMI request

DMIC_CLK
DMIC_DAT
@C2110 220P_0402_25V8J
C2111 220P_0402_25V8J

+LCDVDD
C266 0.1U_0402_16V4Z
C267 0.1U_0402_16V4Z

+LCDVDD
change to 0805
R207 470_0805_5%
Q71A 2N7002DW-7-F_SOT363-6
+5VALW
R208 1M_0402_5%
R209 100K_0402_5%
+LCDVDD
Q7 SI2301BDS-T1-E3_SOT23-3
+3VS
C264 4.7U_0805_10V4Z
C265 4.7U_0805_10V4Z
C268 1000P_0402_25V

20 ENAVDD
2N7002DW-7-F_SOT363-6 Q71B
R210 2.2K_0402_5%

Limited Current < 1A

Avoid Panel display garbage after power on.

+LCDVDD
INVPWR_B+
C270 680P_0402_50V7K
C271 680P_0402_50V7K

LVDS CONN

JLVDS
ACES_88242-4001 CONN@

28 USB20_P4
28 USB20_N4
R565 0_0402_5% USB20_P4_R
R564 0_0402_5% USB20_N4_R

LVDS_A2- 18
LVDS_A2+ 18
LVDS_A1- 18
LVDS_A1+ 18
LVDS_A0- 18
LVDS_A0+ 18
LVDS_ACLK- 18
LVDS_ACLK+ 18

18 LVDS_BCLK+
18 LVDS_BCLK-
18 LVDS_B0+
18 LVDS_B0-
18 LVDS_B1+
18 LVDS_B1-
18 LVDS_B2+
18 LVDS_B2-

+3VS
C269 680P_0402_50V7K

DMIC_DAT 34
DMIC_CLK 34
+5VS
INV_PWM 40
BKOFF# 40
DAC_BRIG 40
+USB_CAM
DDC2_CLK 20
DDC2_DATA 20

+5V_LOGO R462 100_0805_5%

C272 470P_0402_50V8J
C2120 470P_0402_50V8J

Logo LED

1102 Change size to 0805

1212 EMI request

C273 470P_0402_50V8J

+3VS
R212 2.2K_0402_5%
R213 2.2K_0402_5%
DDC2_CLK
DDC2_DATA

B+
INVPWR_B+
@L8 0_0805_5%
L9 FBMA-L11-201209-221LMA30T_0805

0308_Reserve L8 and install L9.

+5VALW
@D17
USB20_N4_R
USB20_P4_R
VIN IO1
IO2 GND
PRTR5V0U2X_SOT143-4

USB Camera Power

1106 Add SB control pin

+5VALW
+5VS
@PJP5 PAD-OPEN 2x2m
PJP4 PAD-OPEN 2x2m
C1288 10U_0805_10V4Z
R2072 0_0402_5%
@R2073 0_0402_5%
28 GPIO20

U54
IN OUT
GND
SHDN BYP
G916-390T1UF_SOT23-5

R891 53.6_0402_1%
R892 24.9_0402_1%
C952 4.7U_0805_10V4Z

+USB_CAM

SA000025F00

S IC G916T1UF SOT23 5P ADJUSTABLE LDO

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

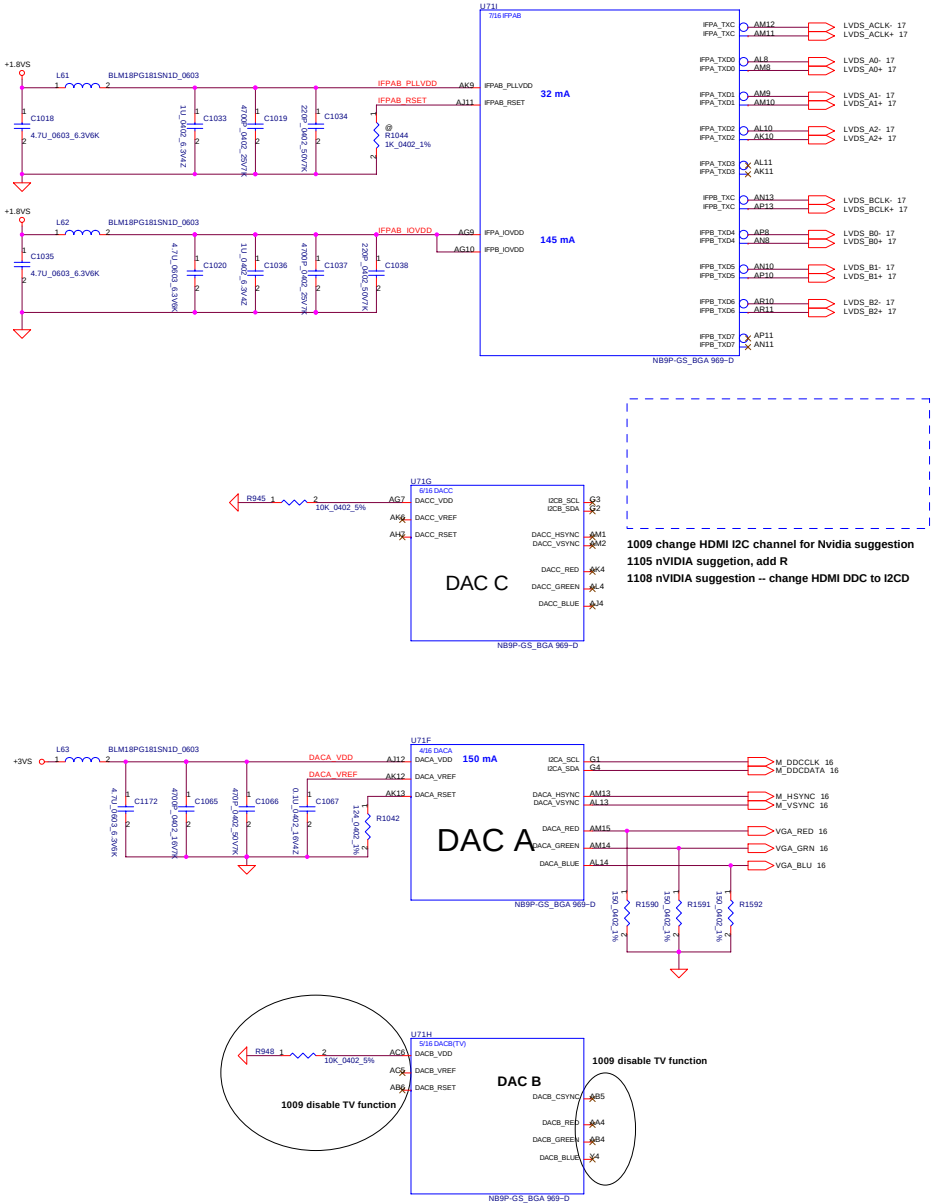
Compal Electronics, Inc.

Title: LCD CONN.

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

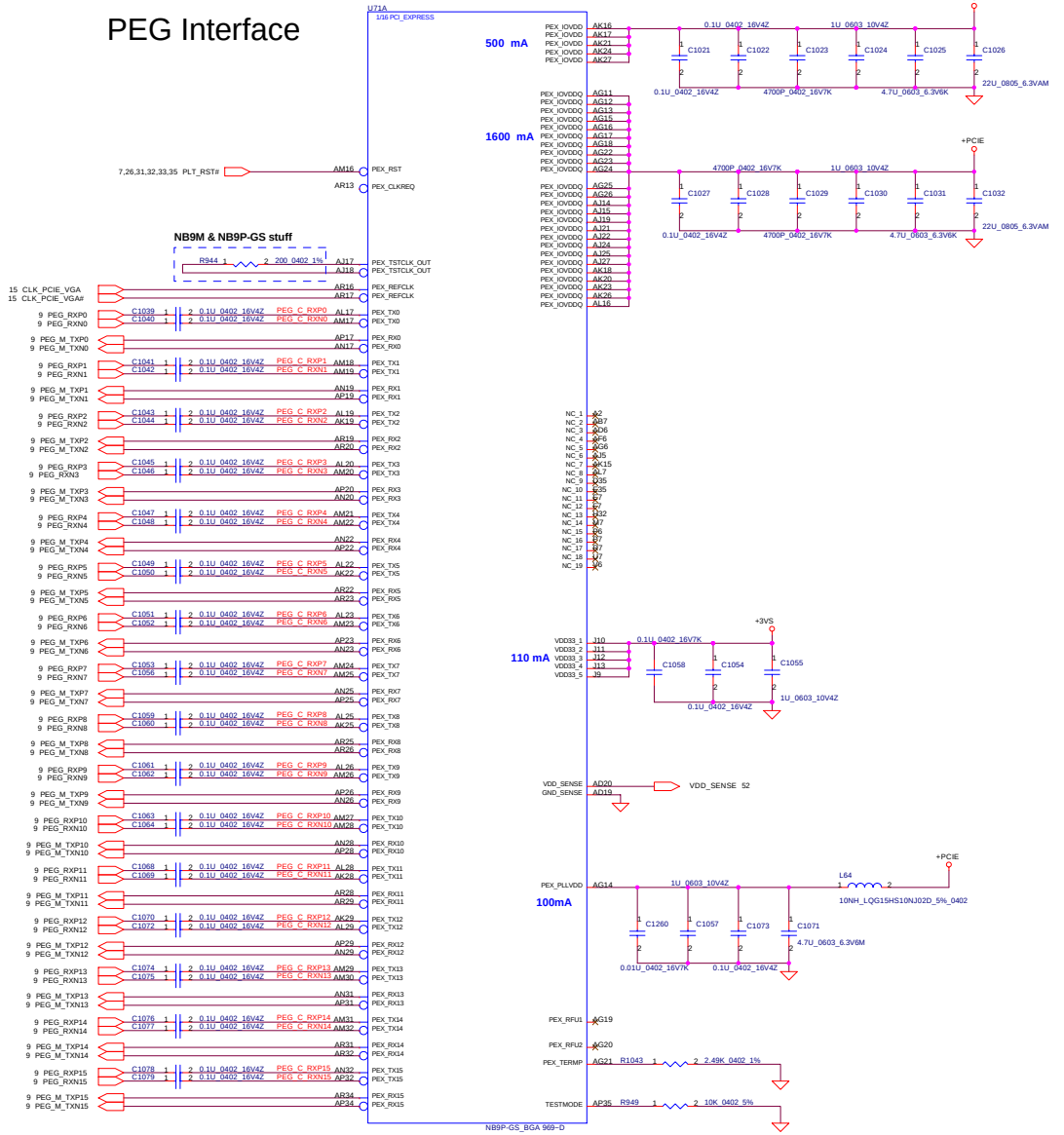
Date: Wednesday, December 26, 2007 | Sheet 17 of 58

LVDS & DAC Interface



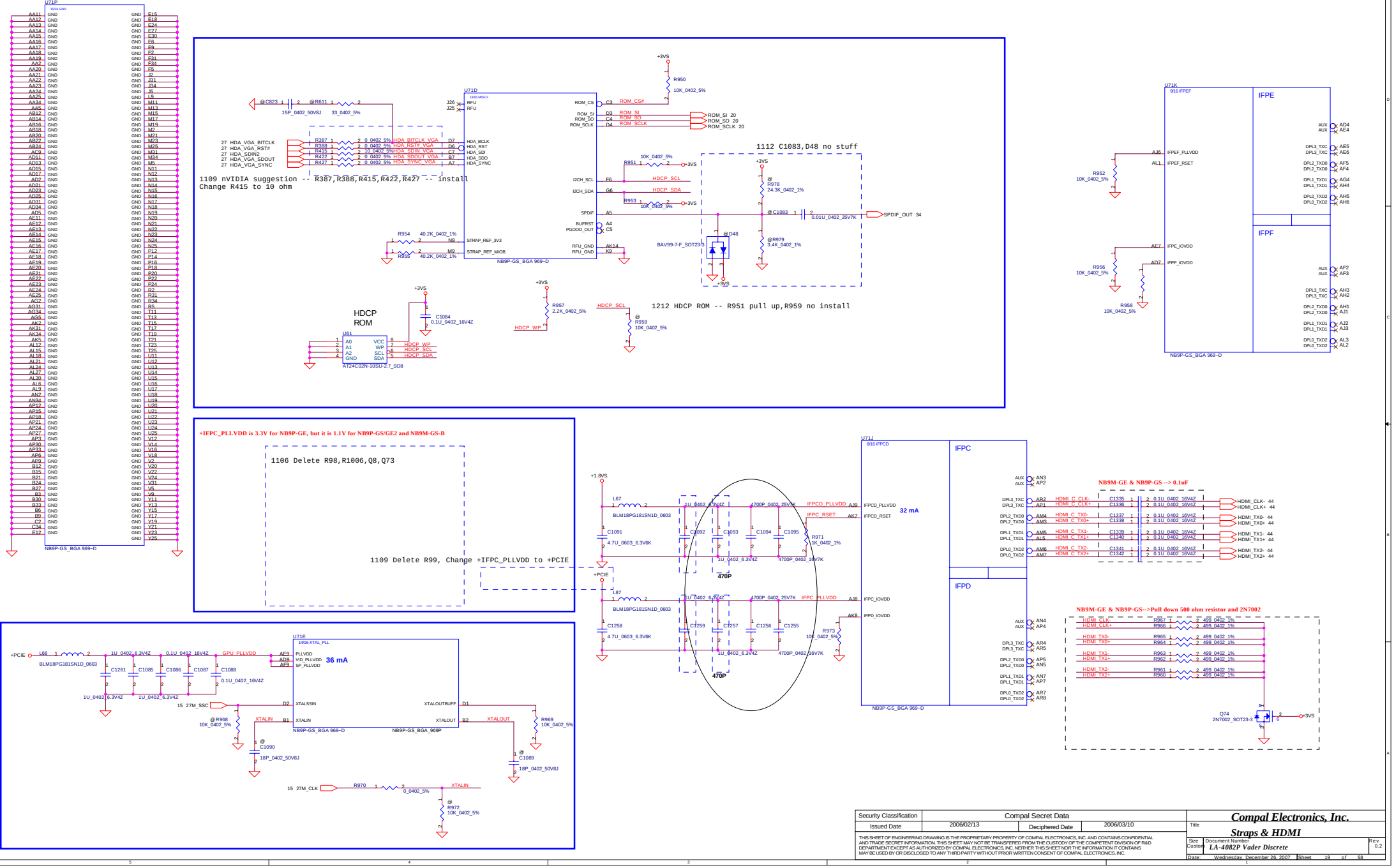
1009 change HDMI I2C channel for Nvidia suggestion
1105 nVIDIA suggetion, add R
1108 nVIDIA suggestion -- change HDMI DDC to I2CD

PEG Interface

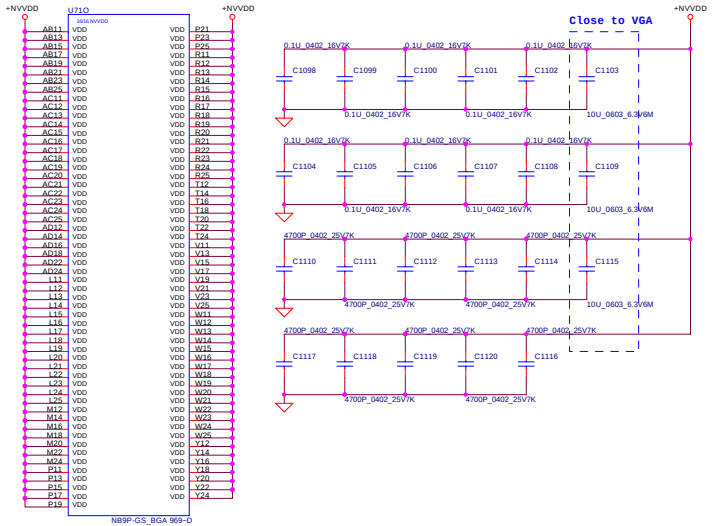


Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

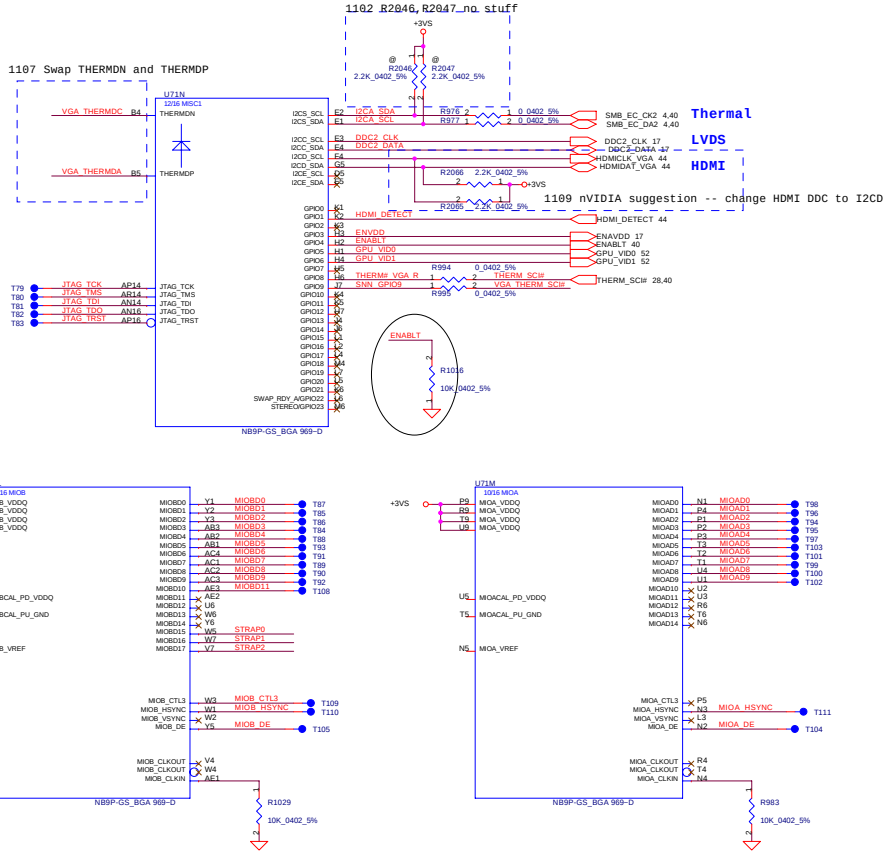
Title	Compal Electronics, Inc.		
	PEG & LVDS & DAC		
Size: Custom	Document Number: LA-4082P Vader Discrete		Rev: 0.2
Date: Wednesday, December 26, 2007	Sheet 18 of 58		


1109 nVIDIA suggestion -- R387,R388,R415,R422,R427 -- install
Change R415 to 10 ohm
1112 C1083,D48 no stuff
1212 HDCP ROM -- R951 pull up,R959 no install
HDCP ROM
+IFPC_PLLVDD is 3.3V for NB9P-GE, but it is 1.1V for NB9P-GS/GE2 and NB9M-GS-B
1106 Delete R98,R1006,Q8,Q73
1109 Delete R99, Change +IFPC_PLLVDD to +PCIE
NB9M-GE & NB9P-GS --> 0.1uF
NB9M-GE & NB9P-GS-->Pull down 500 ohm resistor and 2N7002
32 mA
36 mA
470P
470P
NB9P-GS_BGA 969-D
NB9P-GS_BGA 969P
Compal Electronics, Inc.
Straps & HDMI
LA-4082P Vader Discrete
Wednesday, December 26, 2007
Sheet 19 of 58

VGA Core power

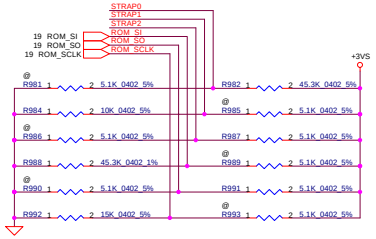


GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



MULTI LEVEL STRAPS For NB9M-Gx (64bit)

NB9P-GS and NB9P-GE2 is as same as NB9M-GE-B



	NB9P-GS	NB9M-GE/NB9P-GE2
STRAP0	pull up 45K	pull up 45K
STRAP1	pull down 10K	pull down 10K
STRAP2	pull up 10K	pull up 5K
ROM_SO	pull up 5K	pull up 5K
ROM_CLK	pull down 15K	pull down 15K

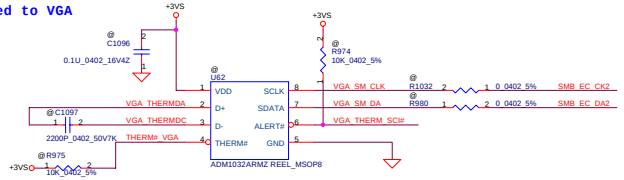
STRAP2 -- R987

	ROM_SI
Samsung 16Mx16	pull down 10K
Hynix 16Mx16	pull down 20K
Samsung 32Mx16	pull down 30K
Hynix 32Mx16	pull down 45K
Qimonda 32Mx16	pull down 35K

R988

VGA Thermal Sensor ADM1032ARMZ

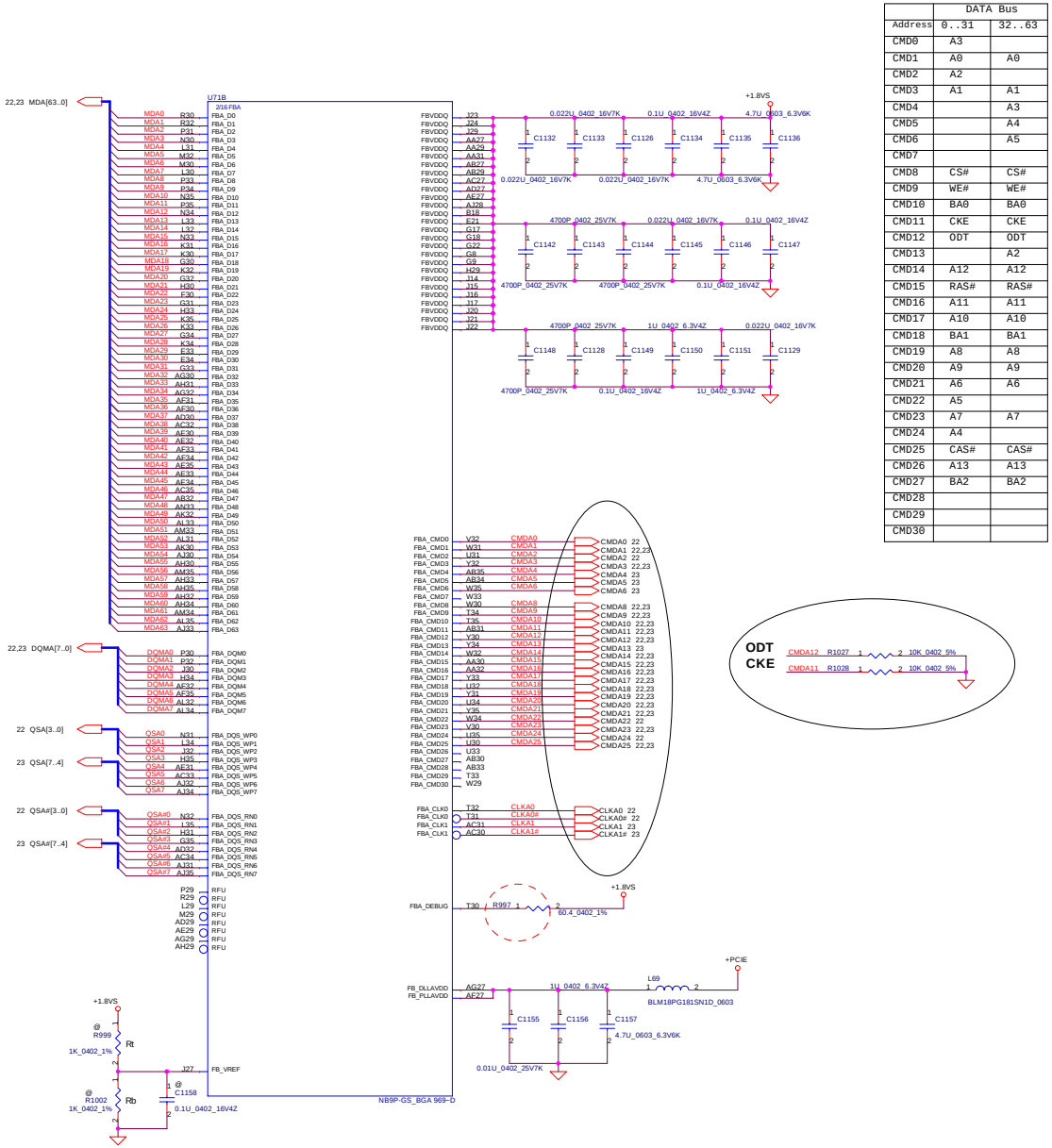
Closed to VGA



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

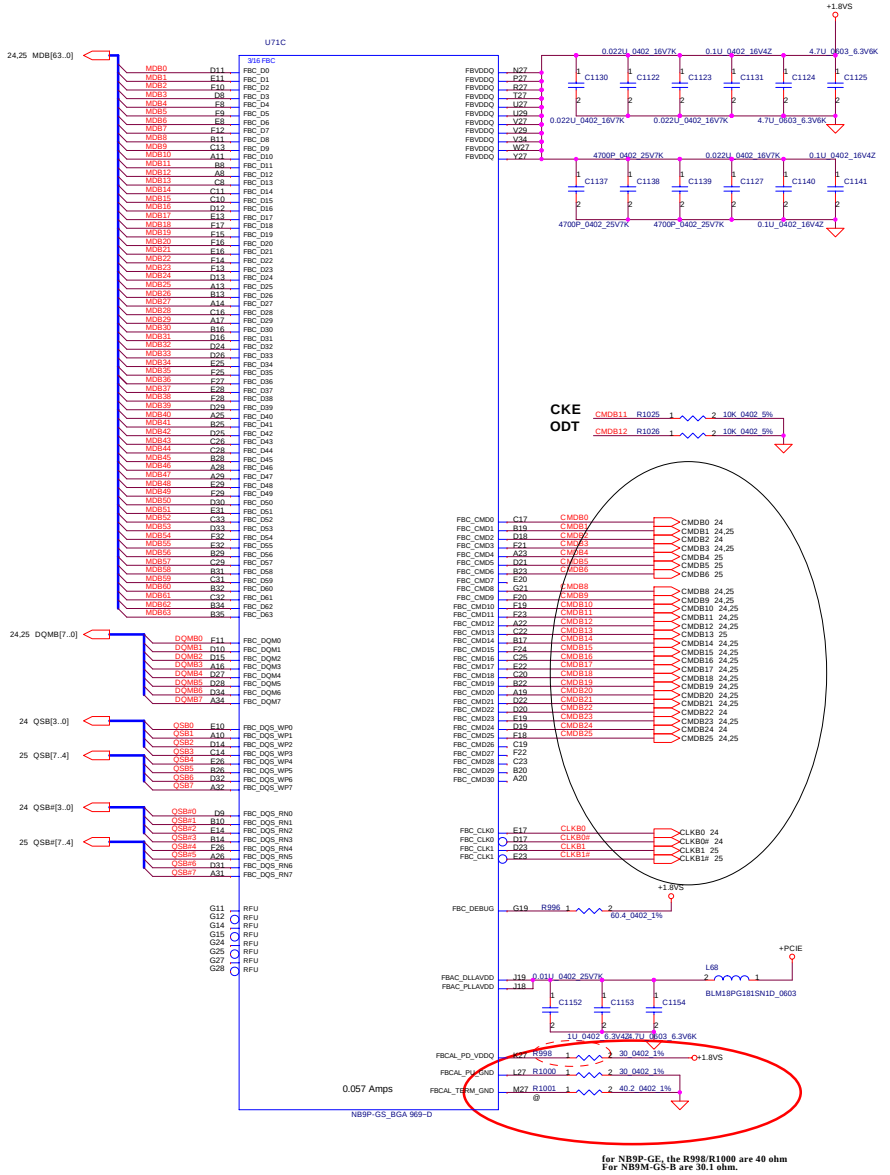
Compal Electronics, Inc.	
Title	GPIO & GND
Size / Document Number	LA-4082P Vader Discrete
Rev	0.2
Date: Wednesday, December 26, 2007	Sheet 20 of 58

VRAM Interface



	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

VREF = 0.5 * FBVDDQ
DDR2: 1.0V = 2.0V * 1K/(1K + 1K)
FBVREF = FBVDDQ * Rb/(Rt + Rb)



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

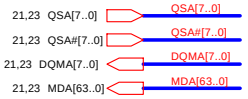
Title	Compal Electronics, Inc.		
	VRAM Interface		
Size	Document Number		Rev
Custom	LA-4082P Vader Discrete		0.2
Date:	Wednesday, December 26, 2007	Sheet	21 of 58

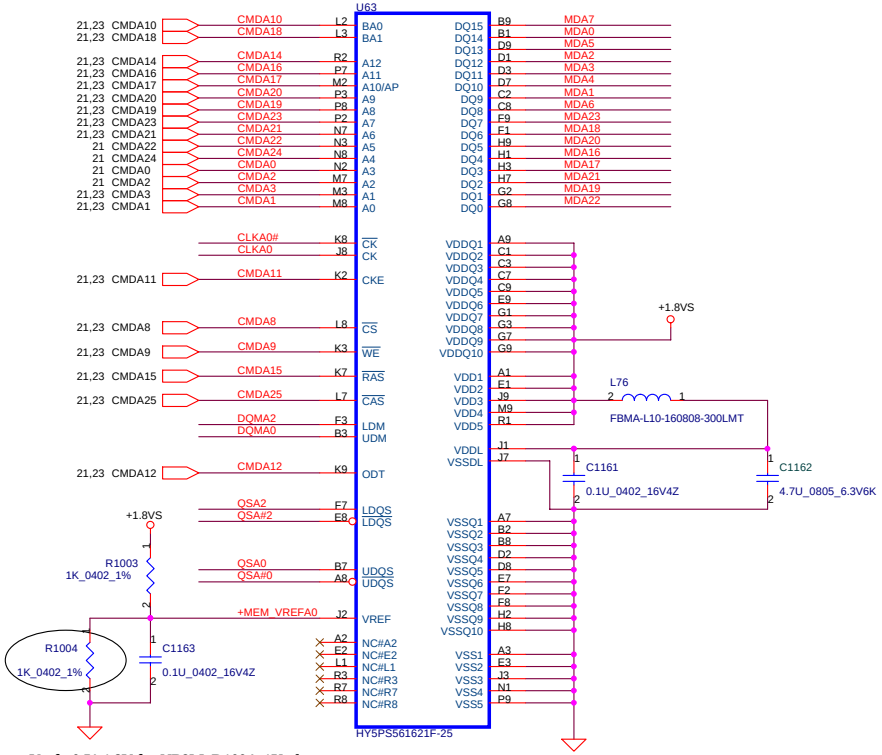
VRAM DDR2 chips (256MB & 512MB)

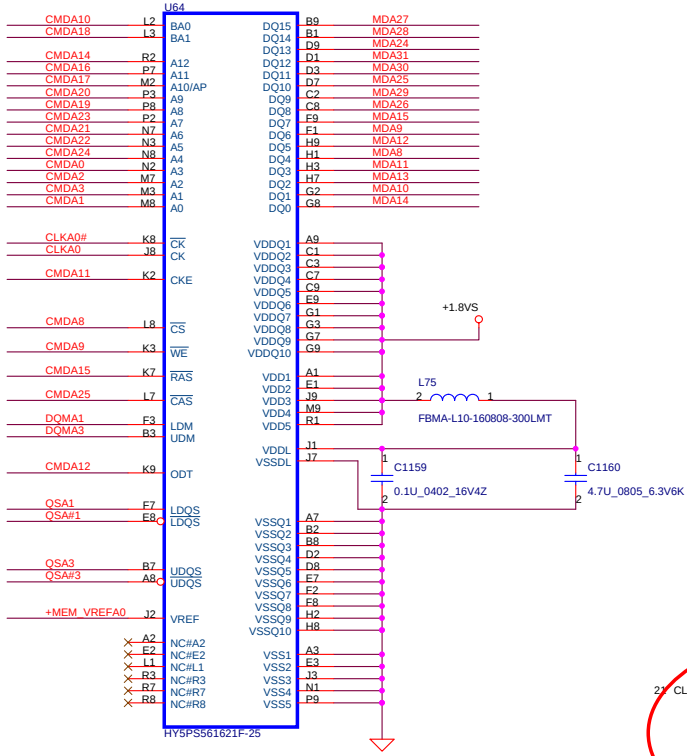
32Mx16 DDR2 400MHz *8==>512MB

32Mx16 DDR2 400MHz *4==>256MB

	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

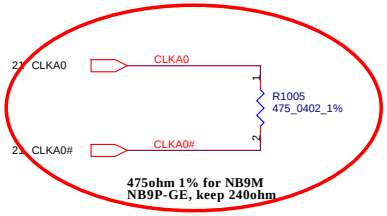






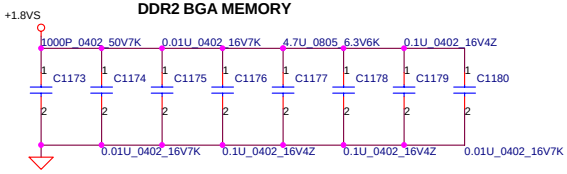
Vref= 0.5* 1.8V for NB9M, R1004=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1004=1K ohm

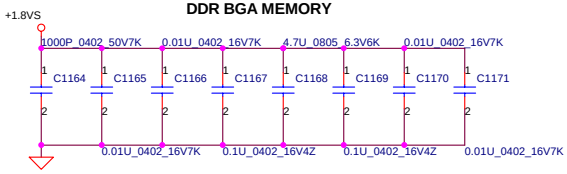


475ohm 1% for NB9M
NB9P-GE, keep 240ohm

DDR2 BGA MEMORY



DDR BGA MEMORY



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

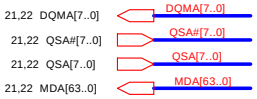
Compal Electronics, Inc.	
Title	CHANNEL A EXT. 256M_1
Size: Custom	Document Number: LA-4082P Vader Discrete
Rev	0.2
Date: Wednesday, December 26, 2007	Sheet 22 of 58

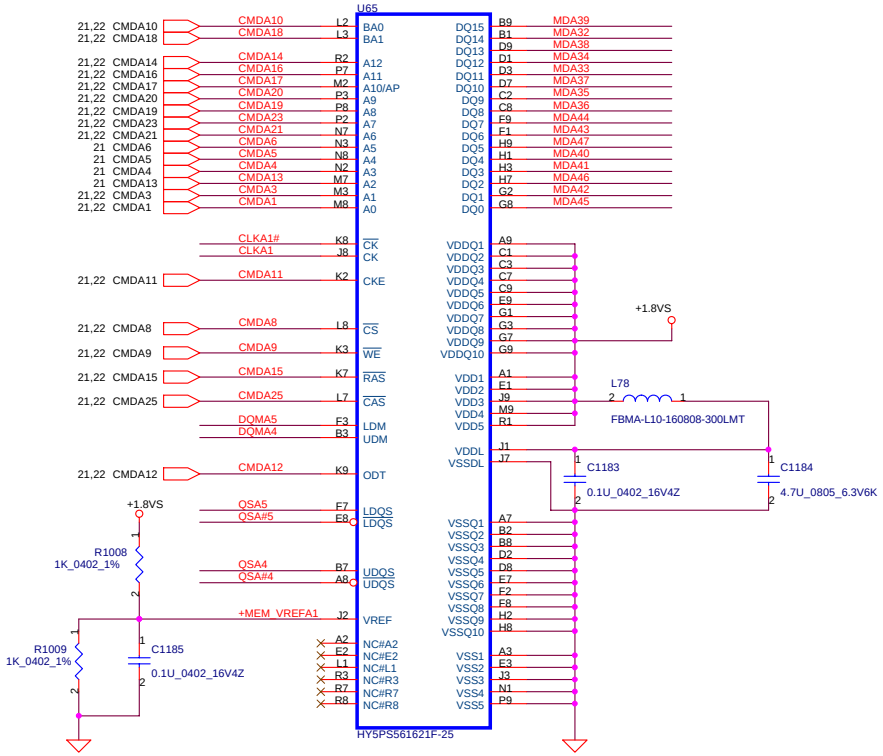
VRAM DDR2 chips (256MB & 512MB)

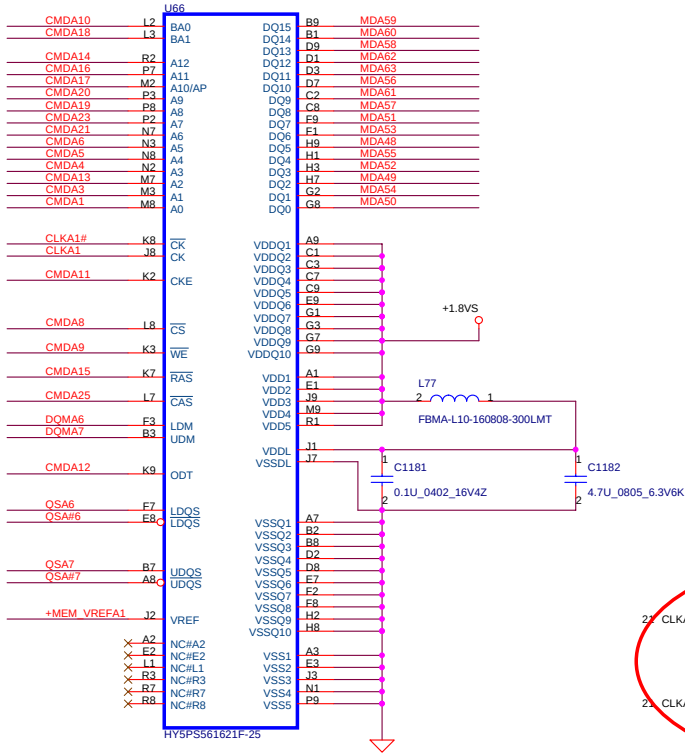
32Mx16 DDR2 400MHz *8==>512MB

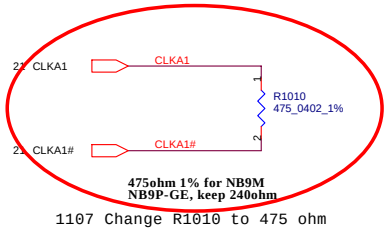
32Mx16 DDR2 400MHz *4==>256MB

	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		







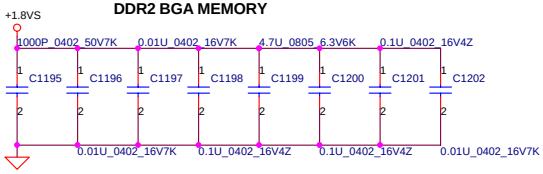


1107 Change R1010 to 475 ohm

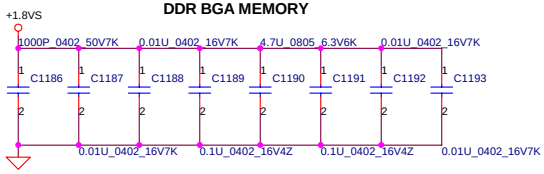
Vref= 0.5* 1.8V for NB9M, R1009=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1009=1K ohm

DDR2 BGA MEMORY



DDR BGA MEMORY



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CHANNEL A EXT. 256M_2**

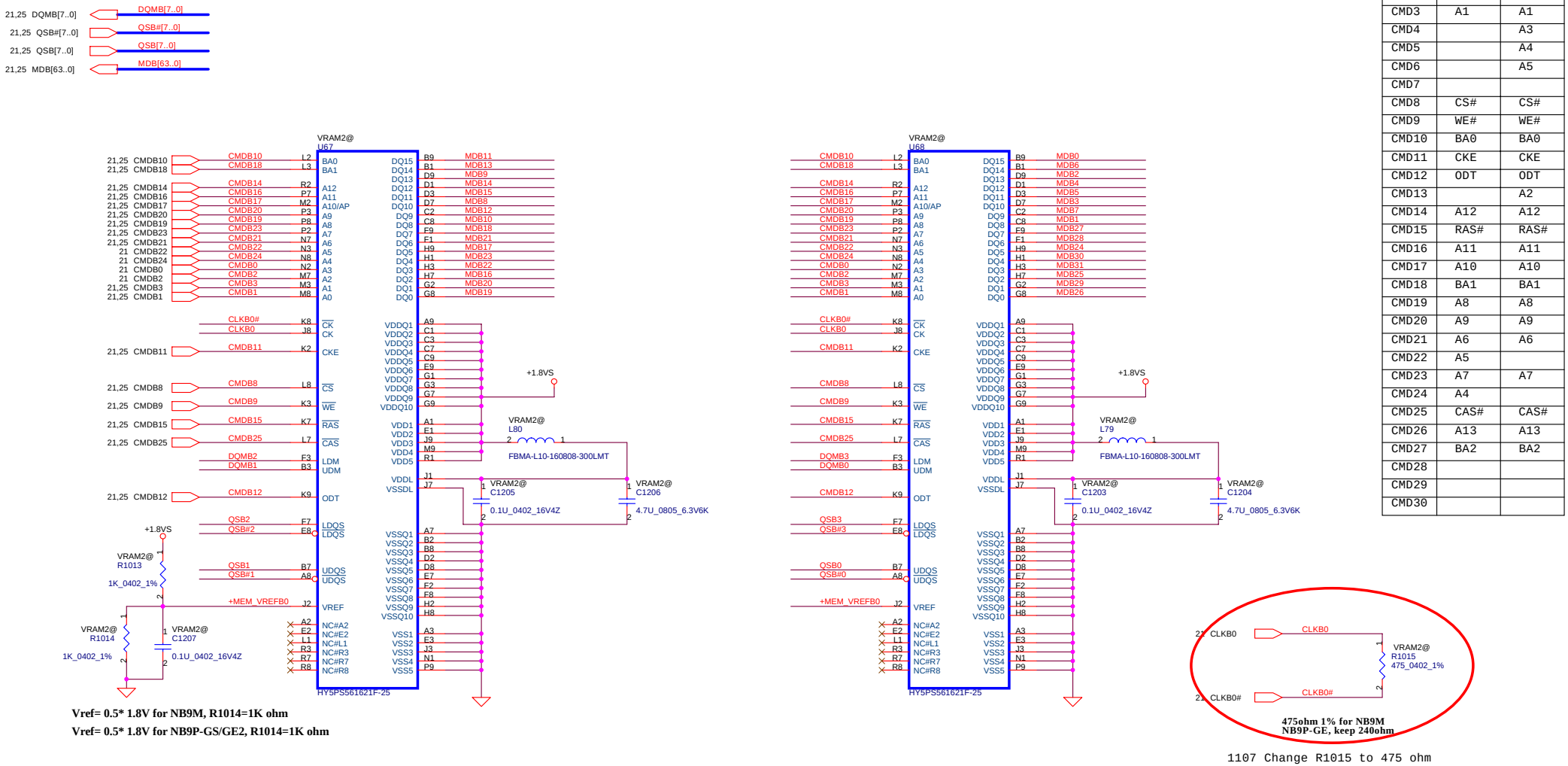
Size: Custom | Document Number: **LA-4082P Vader Discrete** | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 23 of 58

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



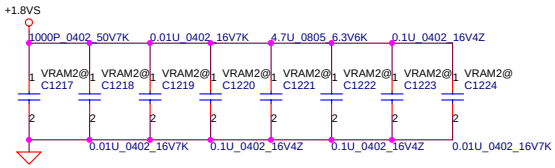
Vref= 0.5* 1.8V for NB9M, R1014=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1014=1K ohm

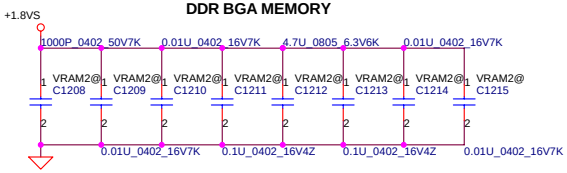
475ohm 1% for NB9M
NB9P-GE, keep 240ohm

1107 Change R1015 to 475 ohm

DDR2 BGA MEMORY



DDR BGA MEMORY

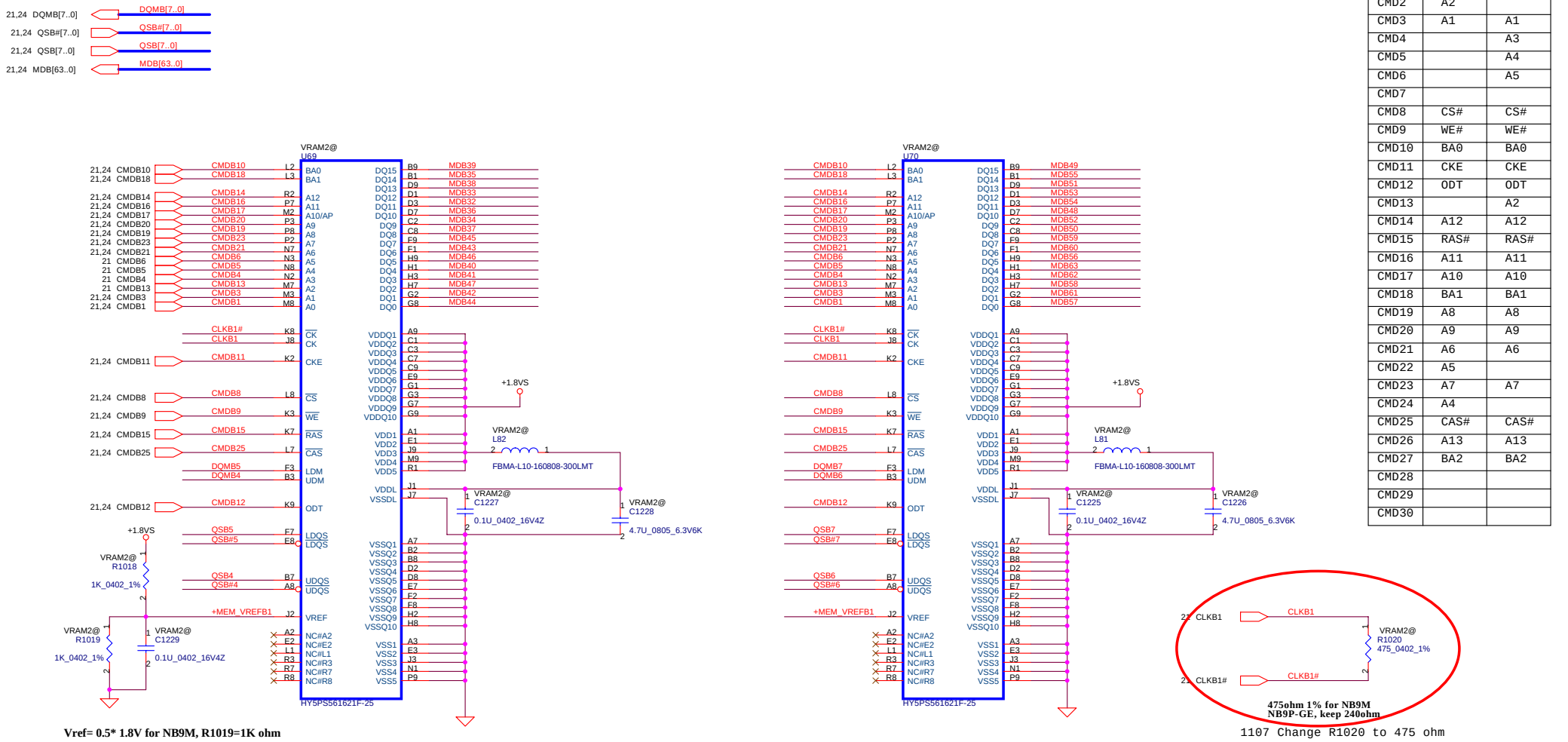


Compal Electronics, Inc.	
Title	CHANNEL B EXT. 256M_1
Size: Custom	Document Number: LA-4082P Vader Discrete
Rev	0.2
Date: Wednesday, December 26, 2007	Sheet 24 of 58

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

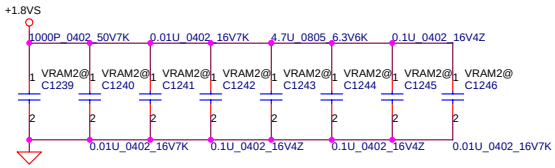


Vref= 0.5* 1.8V for NB9M, R1019=1K ohm

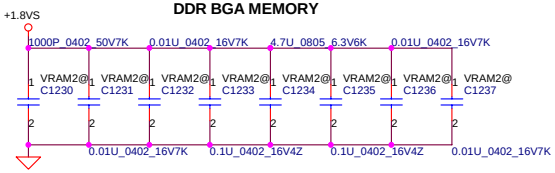
Vref= 0.5* 1.8V for NB9P-GS/GE2, R1019=1K ohm

1107 Change R1020 to 475 ohm

DDR2 BGA MEMORY

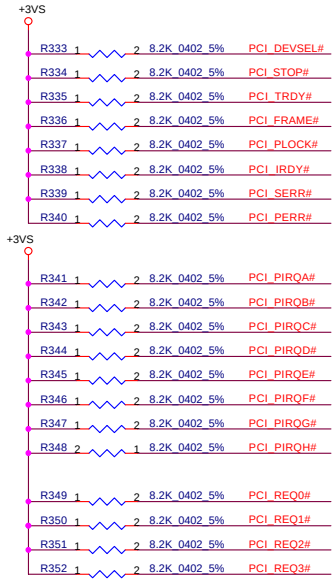


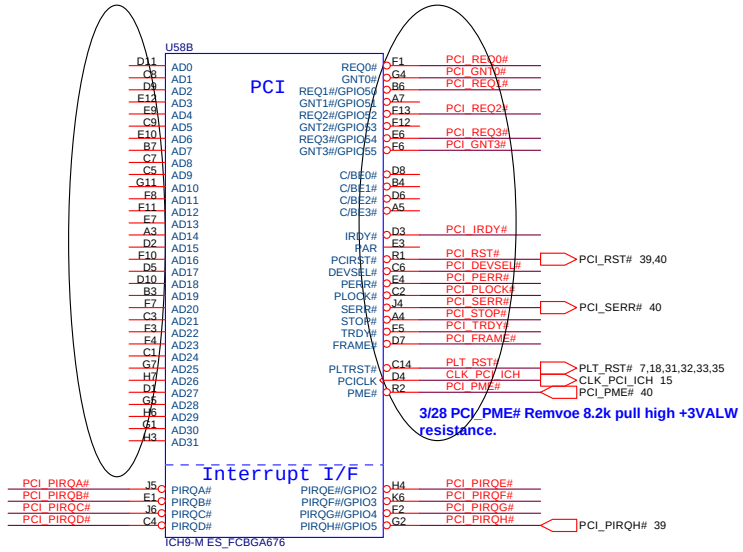
DDR BGA MEMORY



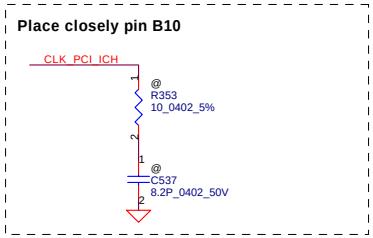
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	CHANNEL B EXT. 256M_2
Size: Custom	Document Number: LA-4082P Vader Discrete
Rev	0.2
Date:	Wednesday, December 26, 2007
Sheet	25 of 58



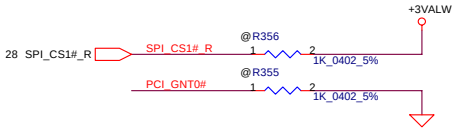


3/28 PCI_PME# Remvoe 8.2k pull high +3VALW resistance.



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(1/4)-PCI/INT

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 26 of 58

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

1015 add pull up to meet Intel design

+3VS R2058 10K_0402_5% SATA_LED#

+RTCVCC
R359 1M_0402_5% SM_INTRUDER#
R357 330K_0402_5% LAN100_SLP
R361 330K_0402_5% ICH_INTVRMEN
R363 180K_0402_5% ICH_SRTCRST#
C538 0.1U_0402_16V4Z
R364 @ 0_0402_5%
R360 @ 0_0402_5%

+3VS
GATEA20 R358 10K_0402_5%
KB_RST# R362 10K_0402_5%
+VCCP
H_DPRSTP# @R365 56_0402_5%
H_DPSLP# @R366 56_0402_5%

U58A

+RTCVCC R367 20K_0402_5%
C539 1U_0603_10V4Z
CLRP2 SHORT PADS

ICH_RTCX1 C23 RTCX1
ICH_RTCX2 C24 RTCX2
ICH_RTCRST# A25 RTCRST#
ICH_SRTCRST# F20 SRTCRST#
SM_INTRUDER# C22 INTRUDER#
ICH_INTVRMEN B22 INTVRMEN
LAN100_SLP A22 LAN100_SLP

RTC

LPC_AD[0..3] 32,39,40
FWH0/LAD0 K5 LPC_AD0
FWH1/LAD1 K4 LPC_AD1
FWH2/LAD2 L6 LPC_AD2
FWH3/LAD3 K2 LPC_AD3
FWH4/LFRAME# K3 LPC_FRAME# LPC_FRAME# 32,39,40
LDRQ0# J3
LDRQ1#/GPIO23 J1 T50 PAD

LPC

GLAN_CLK E25
LAN_RSTSYNC C13
LAN_RXD0 F14
LAN_RXD1 G13
LAN_RXD2 D14
LAN_TXD_0 D13
LAN_TXD_1 D12
LAN_TXD_2 E13
GPIO56 B10
GLAN_COMPI B28
GLAN_COMPO B27
+1.5VS R371 24.9_0402_1% GLAN_COMP

LAN / GLAN

A20GATE N7 GATEA20 GATEA20 40
A20M# AJ27 H_A20M# H_A20M# 4
DPRSTP# AJ25 H_DPRSTP_R# R369 0_0402_5% H_DPRSTP#
DPSLP# AE23 H_DPSLP# H_DPRSTP# 5,7,51
H_DPSLP# 5
FERR# AJ26 R_H_FERR# R370 56_0402_5% H_FERR#
H_FERR# 4
CPUPWRGD AD22 H_PWRGOOD H_PWRGOOD 4,5
IGNNE# AF25 H_IGNNE# H_IGNNE# 4
INIT# AE22 H_INIT# H_INIT# 4
INTR AG25 H_INTR H_INTR 4
RCIN# L3 KB_RST# KB_RST# 40
NMI AF23 H_NMI H_NMI 4
SMI# AF24 H_SMI# H_SMI# 4
STPCLK# AH27 H_STPCLK# H_STPCLK# 4
THRMTRIP# AG26 THRMTRIP_ICH# R379 54.9_0402_1% H_THERMTRIP# 4,7,40
TP12 AG27

CPU

+VCCP
R368 56_0402_5%
+VCCP
R374 56_0402_5%
within 2" from R379
placed within 2" from ICH9M

HDA_BITCLK AE6 HDA_BIT_CLK
HDA_SYNC AH4 HDA_SYNC
HDARST# AE7 HDA_RST#
34 HDA_SDIN0 HDA_SDIN0 AF4
35 HDA_SDIN1 HDA_SDIN1 AG4
19 HDA_SDIN2 HDA_SDIN2 AH3
HDA_SDIN3 AE5
HDA_SDOUT AG5 HDA_SDOUT
PAD T51 HDA_DOCK_EN#/GPIO33 AG7
PAD T52 HDA_DOCK_RST#/GPIO34 AE8

IHDA

SATA4RXN AH11 SATA_RXN4_C
SATA4RXP AJ11 SATA_RXP4_C
SATA4TXN AG12 SATA_TXN4_C C540 0.01U_0402_50V7K
SATA4TXP AF12 SATA_TXP4_C C541 0.01U_0402_50V7K
SATA_RXN4_C 30
SATA_RXP4_C 30
SATA_TXN4 30
SATA_TXP4 30

ODD

SATA5RXN AH9 SATA_RXN5_C
SATA5RXP AJ9 SATA_RXP5_C
SATA5TXN AE10 SATA_TXN5_C C542 0.01U_0402_50V7K
SATA5TXP AE10 SATA_TXP5_C C544 0.01U_0402_50V7K
SATA_RXN5_C 38
SATA_RXP5_C 38
SATA_TXN5 38
SATA_TXP5 38

e-SATA
De-feature disable

SATA_CLKN AH18 CLK_PCIE_SATA#
SATA_CLKP AJ18 CLK_PCIE_SATA
CLK_PCIE_SATA# 15
CLK_PCIE_SATA 15
SATARBIAS# AJ7
SATARBIAS AH7 R382 24.9_0402_1%
Within 500 mils

SATA

41 SATA_LED# SATALED# AG8

P- HDD
30 SATA_RXN0_C SATA_RXN0_C AJ16
30 SATA_RXP0_C SATA_RXP0_C AH16
C543 0.01U_0402_50V7K SATA_TXN0_C AF17
C545 0.01U_0402_50V7K SATA_TXP0_C AG17
30 SATA_TXN0
30 SATA_TXP0

S- HDD
30 SATA_RXN1_C SATA_RXN1_C AH13
30 SATA_RXP1_C SATA_RXP1_C AJ13
C546 0.01U_0402_50V7K SATA_TXN1_C AG14
C547 0.01U_0402_50V7K SATA_TXP1_C AE14
30 SATA_TXN1
30 SATA_TXP1

SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP

1212 Swap SATA1 and SATA4

ICH9-M ES_FCBGA676

XOR CHAIN ENTRANCE STRAP:RSVD

+3VS
@R383 1K_0402_5% HDA_SDOUT_CODEC
@R384 1K_0402_5% ICH_RSVD ICH_RSVD 28

1008 add them for Intel suggestion

19 HDA_VGA_BITCLK
35 HDA_BITCLK_MDC
34 HDA_BITCLK_CODEC
R439 33_0402_5%
R373 33_0402_5%
R372 33_0402_5%
HDA_BITCLK

19 HDA_VGA_SYNC
35 HDA_SYNC_MDC
34 HDA_SYNC_CODEC
R440 33_0402_5%
R375 33_0402_5%
R376 33_0402_5%
HDA_SYNC

19 HDA_VGA_RST#
35 HDA_RST#_MDC
34,40 HDA_RST#_CODEC
R442 33_0402_5%
R378 33_0402_5%
R377 33_0402_5%
HDARST#

19 HDA_VGA_SDOUT
35 HDA_SDOUT_MDC
34 HDA_SDOUT_CODEC
R444 33_0402_5%
R380 33_0402_5%
R381 33_0402_5%
HDA_SDOUT

VGA
MDC
CODEC
ICH9-M

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

ICH_RTCX1
R386 10M_0402_5%
C548 15P_0402_50V8J
C549 15P_0402_50V8J
Y3 32.768KHZ_12.5P_MC-146
ICH_RTCX2

HDA_BITCLK
@R385 10_0402_5%
@C550 10P_0402_25V8K

+RTCVCC
W=20mils
R875 0_0402_5%
W=20mils
D36 DAN202U_SC70
+3VL
W=20mils
R876 1K_0402_5%
BATT1.1
W=20mils
@BATT1
CR2032 RTC BATTERY
CONN@ JBATT1
1
2
3 GND
4 GND
ACES_85205-02001
C906 2.2U_0603_6.3V4Z
Place near ICH9

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,SATA,LPC

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 27 of 58

1025 change to follow IBT00 design for G-sensor

Place closely pin AF3

Place closely pin H1

0718 INSTALL R179

1102 Add test point
1212 Add R2095 for EC_SCI#

1108 For LAN DSM
1109 Add GPIO22 for card reader wake up event

SB_SPKR
low -->default
High -->No boot

WLAN

Robson

TV Tuner

1008 no stuff

GLAN

1394_CR1

New Card

1212 Swap PCIE GLAN and New Card

1212 For WLAN issue

1108 For LAN DSM

Within 500 mils

Within 500 mils

Board ID

Discrete-->H
UMA-->L

17" platform-->H
14" platform-->L

1008 add board ID detection

USB-0 Right side
USB-1 Right side
USB-2 E-SATA & USB Combo
USB-3 Dock
USB-4 USB Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Fingerprint
USB-8 MiniCard(TV)
USB-9 New Card
USB-10 Left Side
USB-11 Touch Screen

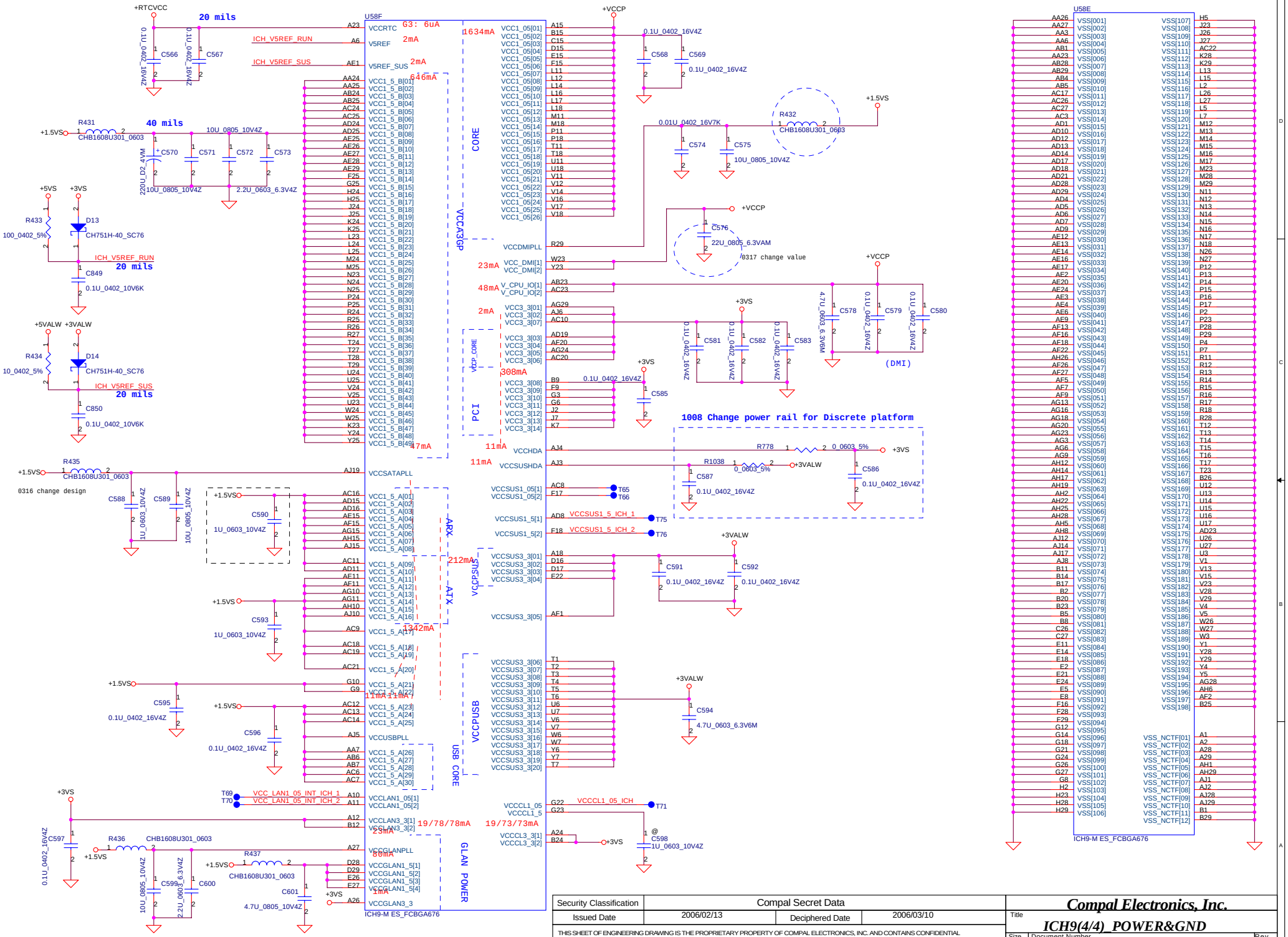
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(3/4)_DMI,USB,GPIO,PCIE

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 28 of 58



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

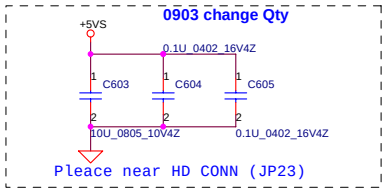
Compal Electronics, Inc.

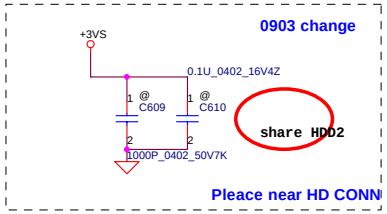
Title: **ICH9(4/4)_POWER&GND**

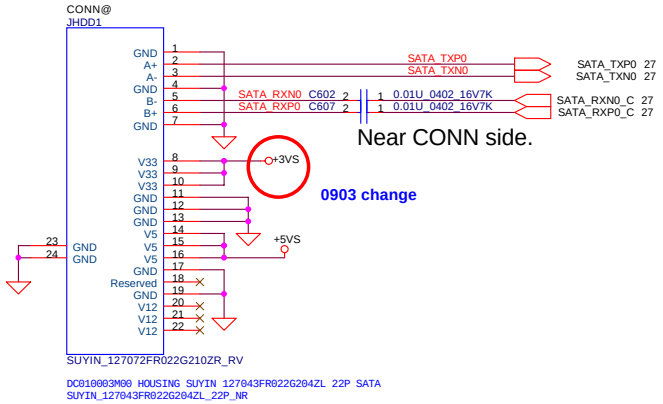
Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

Date: Wednesday, December 26, 2007 | Sheet 29 of 58

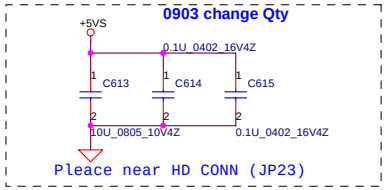
HDD Connector

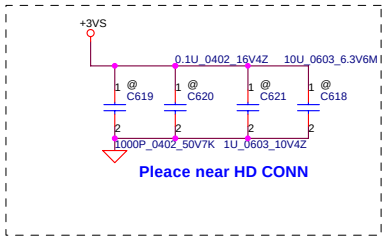


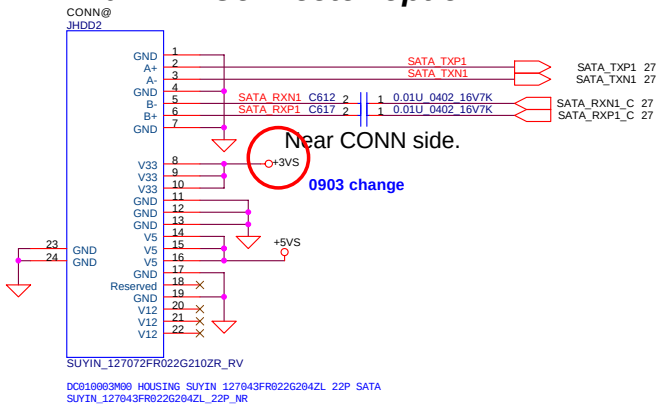




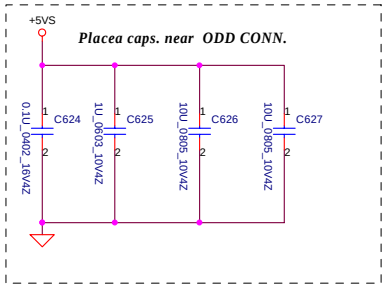
2nd HDD Connector-option

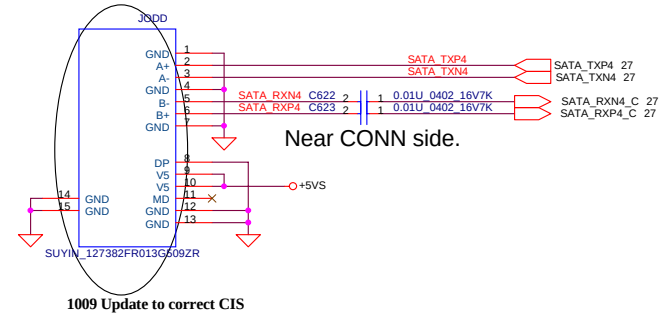






CD-ROM Connector





1009 Update to correct CIS

ZZZ1
LA-4082P

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

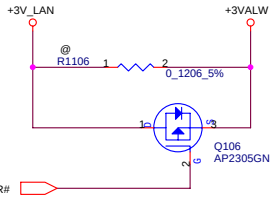
Compal Electronics, Inc.

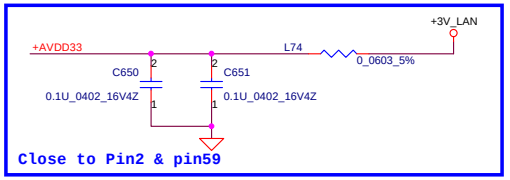
Title: **HDD & CDROM**

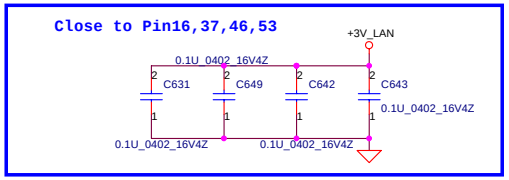
Size: Custom | Document Number: *LA-4082P Vader Discrete* | Rev: 0.2

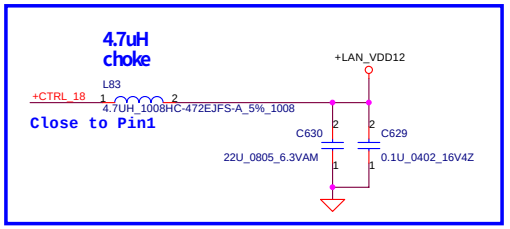
Date: Wednesday, December 26, 2007 | Sheet 30 of 58

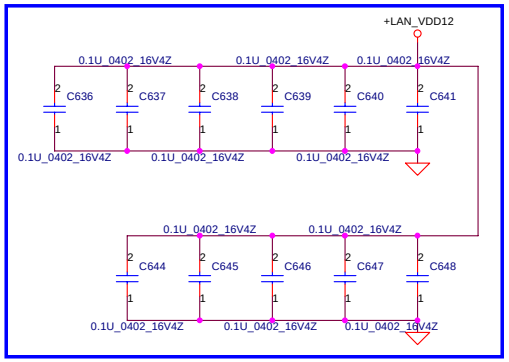
1025 add to meet HP request

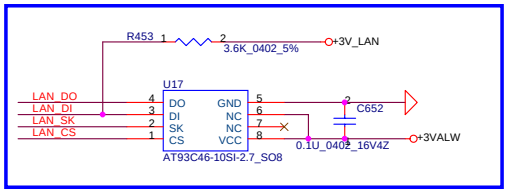


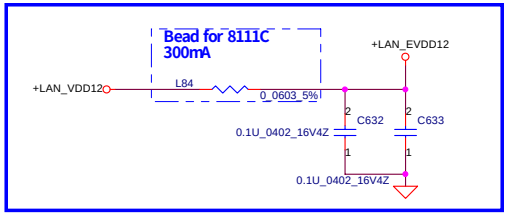




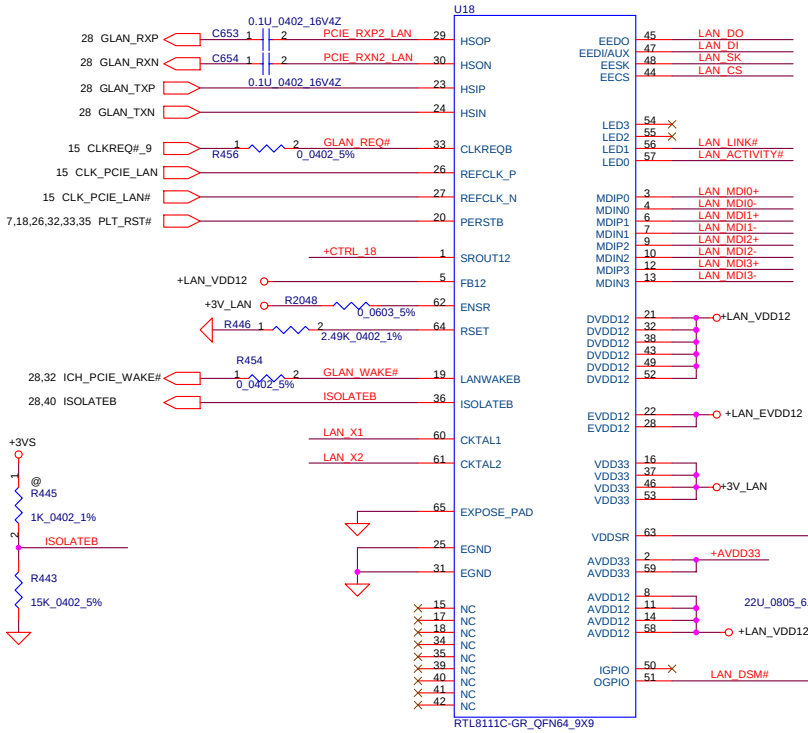


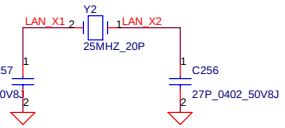


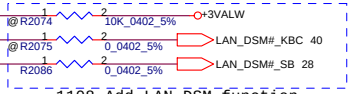




Place Close to Chip

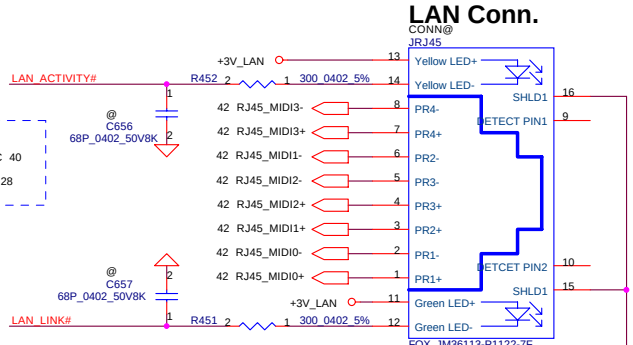


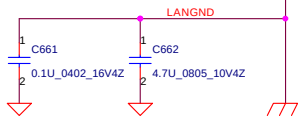


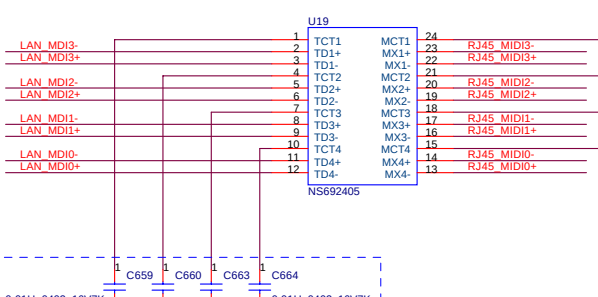


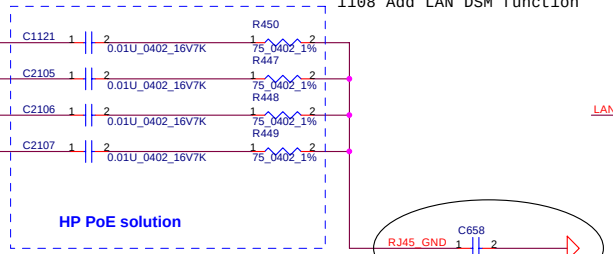
1108 Add LAN DSM function

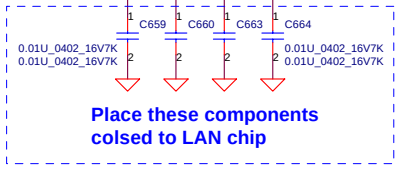
LAN Conn.











Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

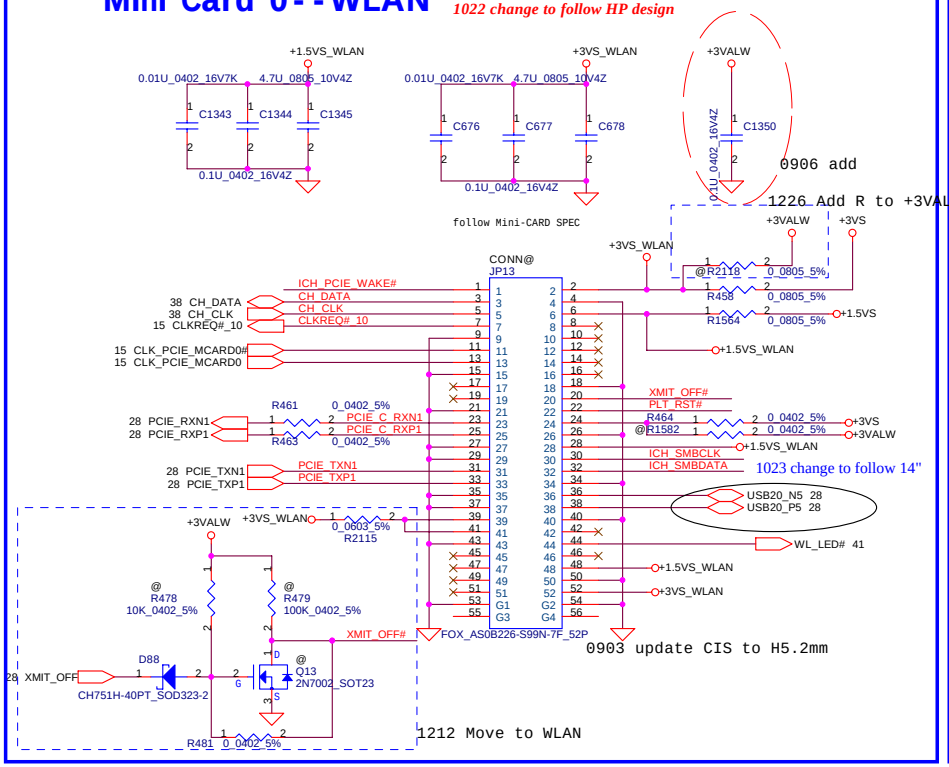
Title: **8111C GLAN**

Size: Custom | Document Number: **LA-4082P Vader Discrete** | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 31 of 58

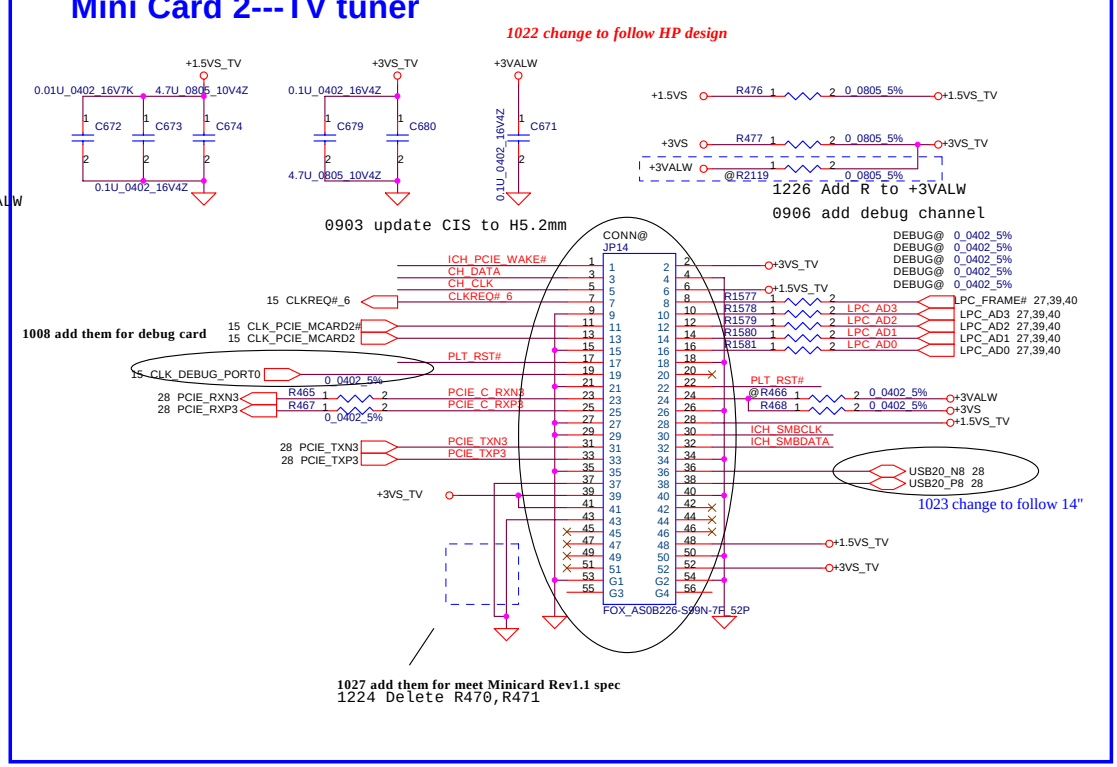
Mini Card 0--WLAN

1022 change to follow HP design

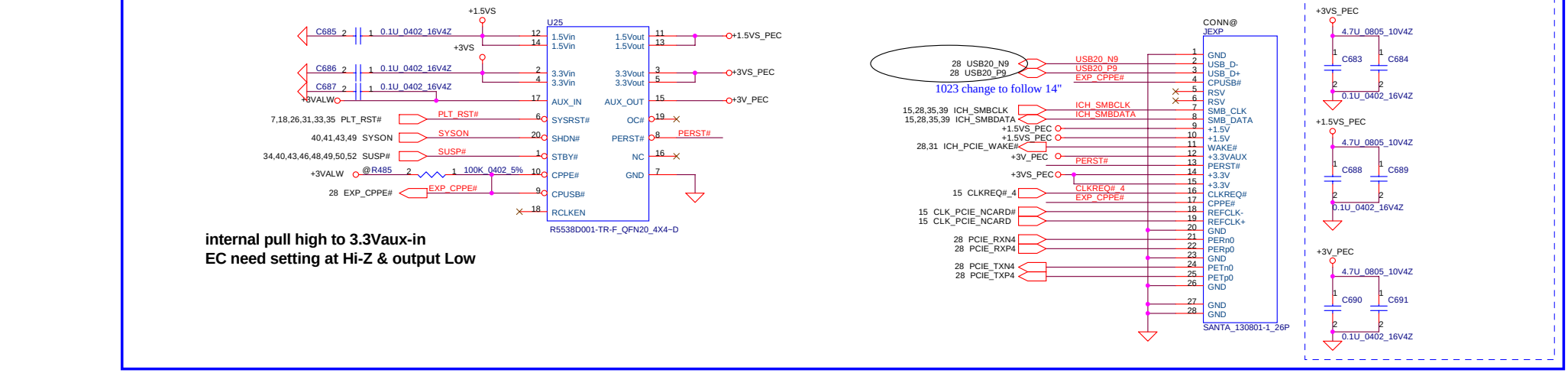


Mini Card 2---TV tuner

1022 change to follow HP design



New Card



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **WLAN, WWAN, New Card**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

Date: Wednesday, December 26, 2007 Sheet 32 of 58

Use 0603 type and over 20 mils trace width on both side

1102 Install R1553

need change to low active switch

40mil

reserved power circuit

Card Reader Connector

CONN@ JREAD

7 IN 1 CONN

TAITW_R015-B10-LM

1109 Do not install R2030

Strap pin for JMicro

1023 JMicro suggest to change

1212 Change XD_ALE to +3VS

Power Circuit

JMB380

JMB380-QGAZ0A_QFN48_7X7

1023 JMicro suggest to change

1109 Add D86 for card reader wake up

use for PWR_EN#

8mA sink current

White LED: VF=3V, IF = 5mA, Res = 56ohm

1009 lower LED power consumption

1212 Change to high active control

For JM380

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: JMB380/385 card reader/1394

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 33 of 58

1008 Change to +3V

1019 Change Size to 1206 for IDT request

CODEC POWER (4.75V) 300mA

0212_Change to +5VALW.

W=40Mil

0208_Change SLP_S3# to SUSP#.

1106 Add EC_BEEP

1107 Delete R515,R516,C916

1023 change detection circuit to solve Speaker can not work.

HP Jack & Dock

Jack MIC

Internal MIC

Internal SPKR.

DOCK MIC

1106 Change C746,C747,C748,C749 to 1000PF

1107 HP request

SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

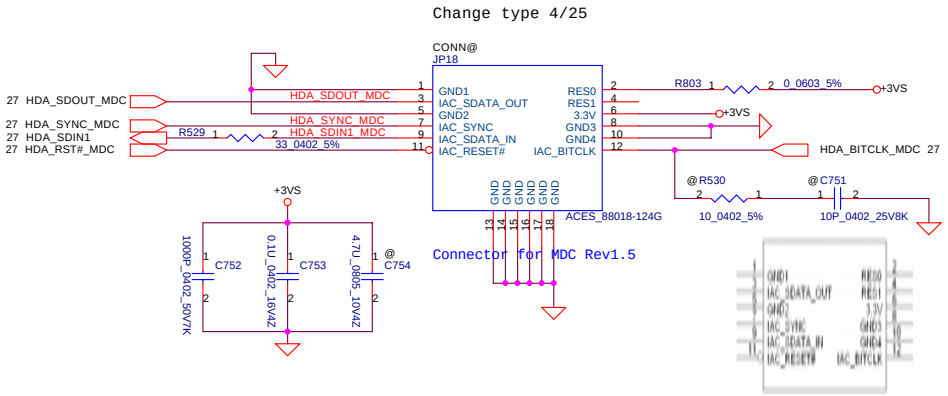
Compal Electronics, Inc.

Title: Codec_IDT9271B7

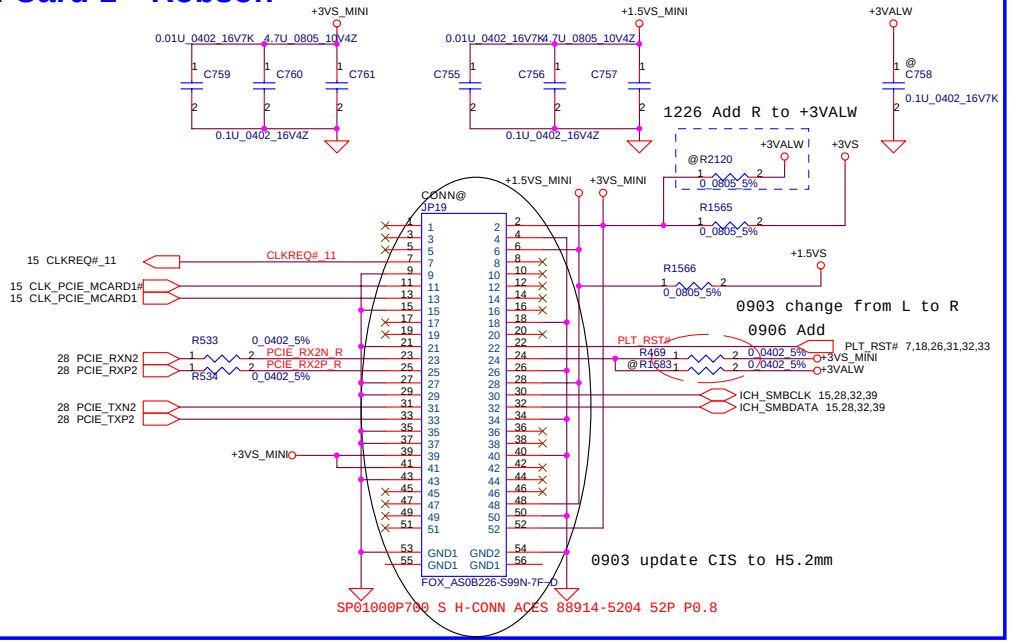
Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 34 of 58

MDC 1.5 Conn.



Mini Card 1---Robson



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **MDC 1.5 & Robson**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

Date: Wednesday, December 26, 2007 Sheet 35 of 58

0906 Change
3/28 from
NC7SZ04P5X_SC70-5
change to 2N7002

1224 Change value

1212 Change to 1uF

Keep 10 mil width

0906 Change pin define
Audio & USB board conn

1108 Change C970,C971 to 22uF

MIC INT In-L

1023 change to n channel FET to solve Speaker can not work.

SP02000D000 S W-CONN ACES 85204-04001 4P P1.25

SPEAKER

1023 add R1012 to solve Speaker can not work

1108 Add 0.01uF

1107 Add R2082,R2083

HP OUT For Docking

HP OUT For M/B

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: AMP & Audio Jack

Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 36 of 58

1107 Change C982 from 5900p to 0.039u

1107 Change C980,C984 from 5900p to 0.039u
1107 Change C983,C992 from 1000p to 100p

1224 C987 change from 0.47u to 0.056uF
Change C984, C980, C993, C990 to 0.027uF

1009 change Subwoofer power circuit

1107 Add pull down for Sub-Woofer shutdown and EC_MUTE#

1107 Change C1008,C1009 to 1UF and no install R936

1113 Remove L58,L60 for layout spacing

Sub-woofer Connector

1108 Change to dual package

Need check

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

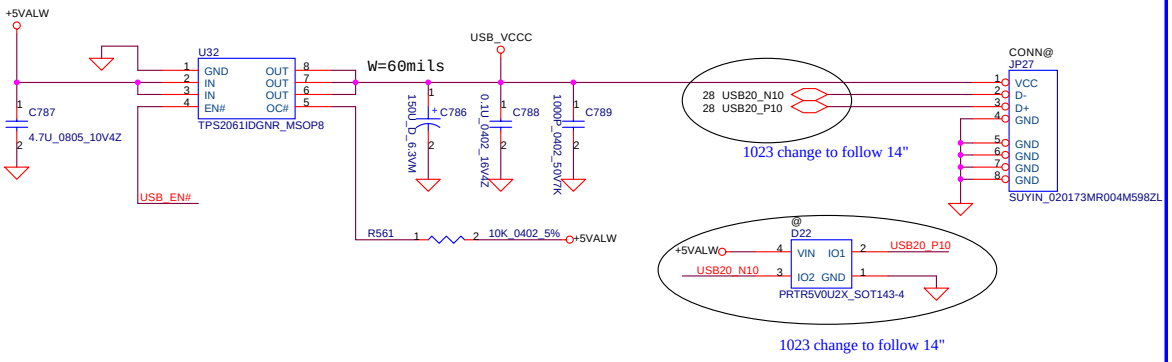
Compal Electronics, Inc.

Title: EQ & Sub Woofer

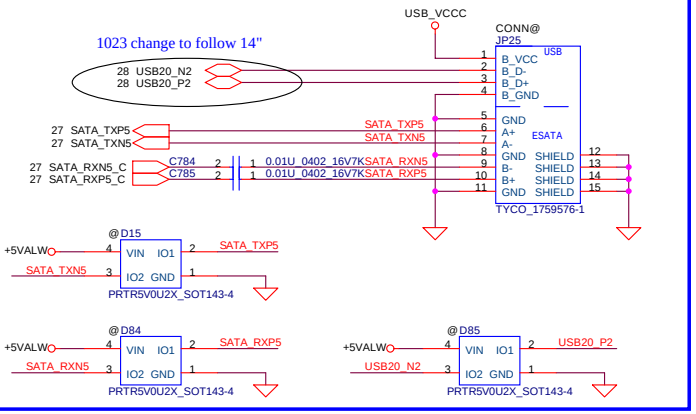
Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.2

Date: Wednesday, December 26, 2007 | Sheet 37 of 58

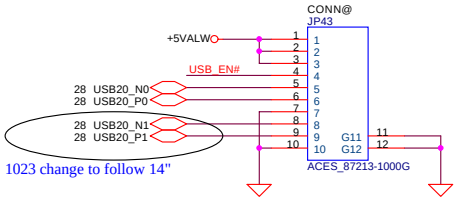
Left side USB Connector



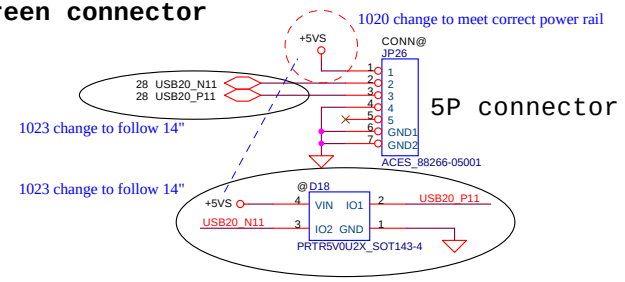
Left side ESATA/USB combination Connector



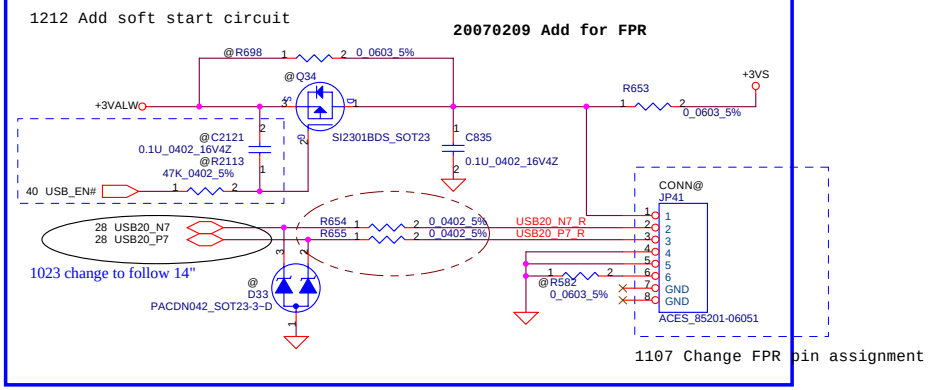
USB cable connector for Right side



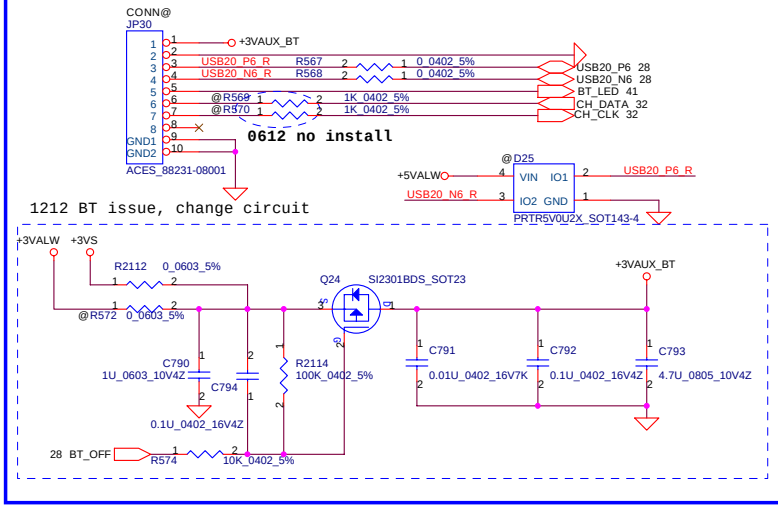
Touch screen connector



Finger printer



BT Connector



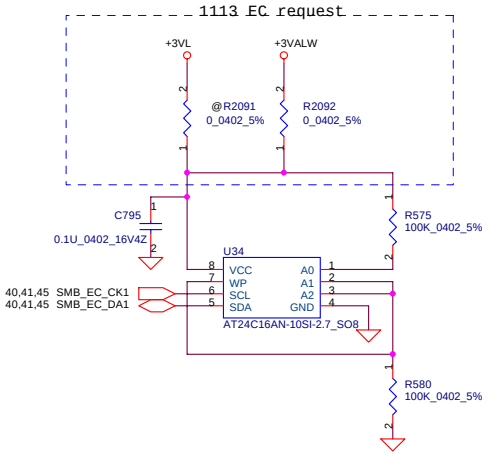
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

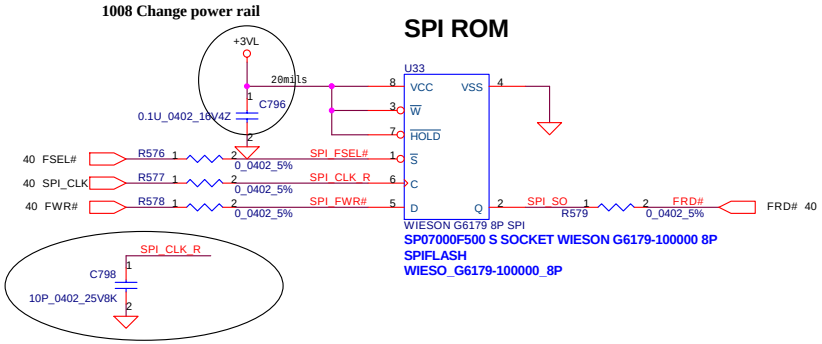
Compal Electronics, Inc.

Title: **USB, BT, eSATA**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

Date: Wednesday, December 26, 2007 | Sheet 38 of 58



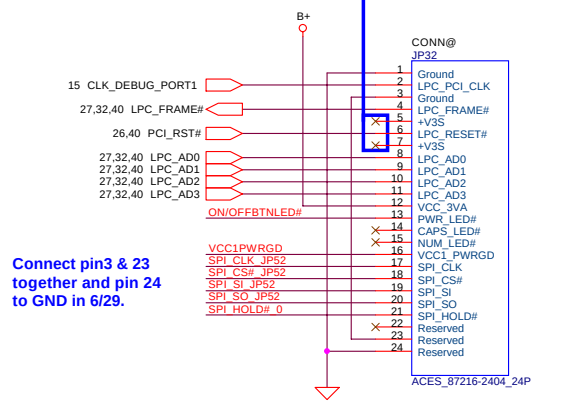


SPI ROM

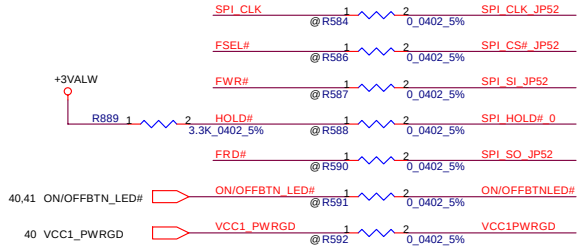
SP07000F500 S SOCKET WIESON G6179-100000 8P
SPIFLASH
WIESO_G6179-100000_8P

LPC Debug Port

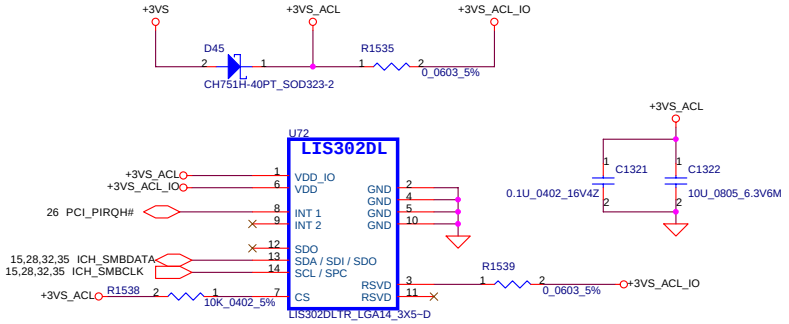
Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



Connect pin3 & 23 together and pin 24 to GND in 6/29.



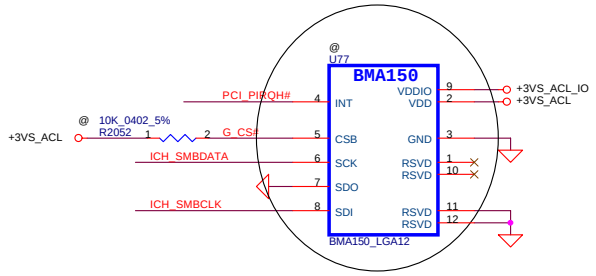
Acceleromter-1



Must be placed in the center of the system.

Acceleromter-2

U72 & U77 must be close
need to update CIS



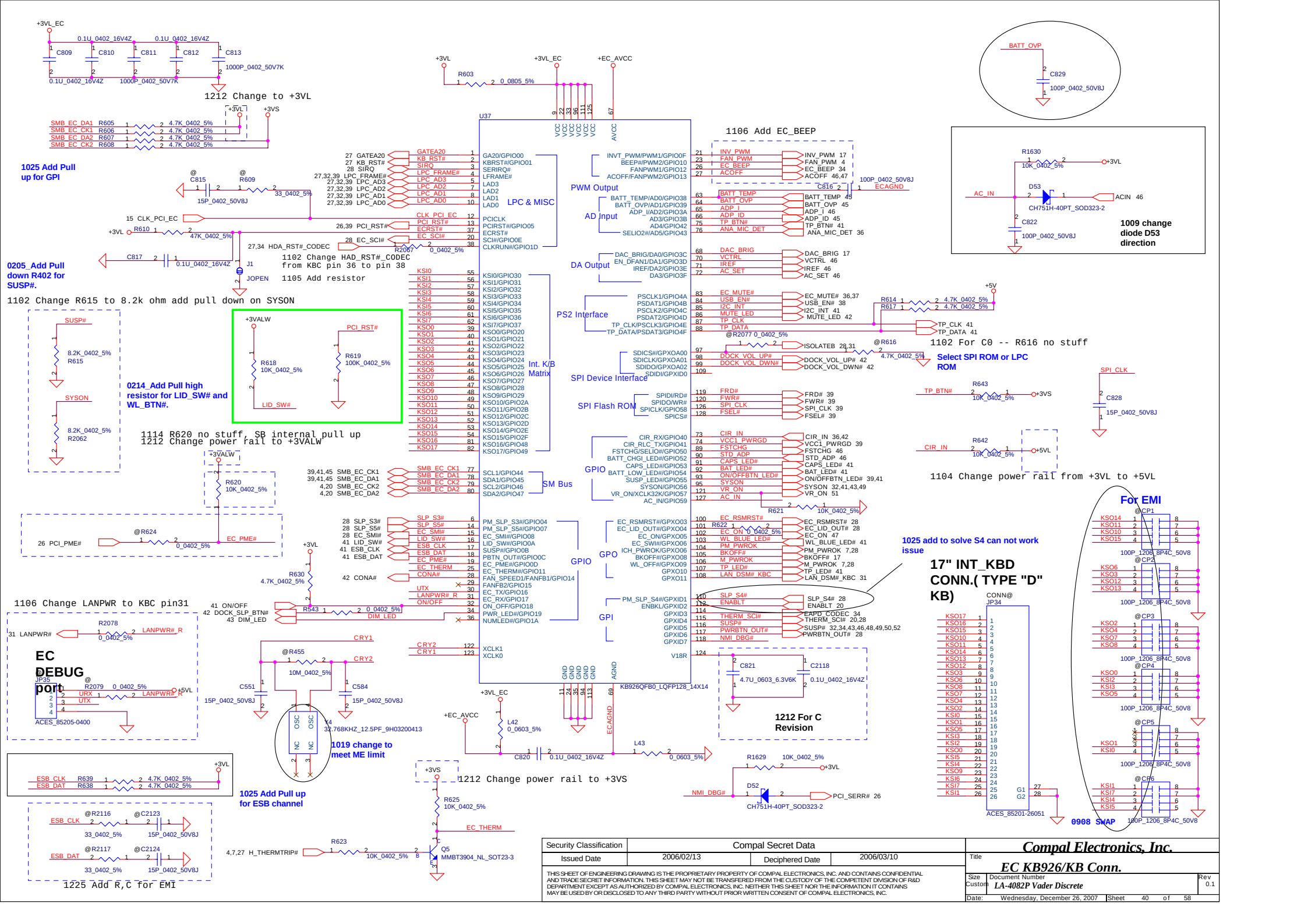
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **BIOS ROM**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.2

Date: Wednesday, December 26, 2007 | Sheet 39 of 58



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **EC KB926/KB Conn.**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.1

Date: Wednesday, December 26, 2007 | Sheet 40 of 58

LED

1009 lower LED power consumption

White

40 CAPS_LED# — D35 HT-F196BP5_WHITE — R1534 470_0402_5% — +5VS_LED

Cap Lock

White

ON/OFFBTN_LED# — D28 HT-F196BP5_WHITE — R648 470_0402_5% — +5VALW_LED

System status LED

White

40 BAT_LED# — D34 HT-F196BP5_WHITE — R631 470_0402_5% — +5VALW_LED

Battery Charge LED

27 SATA_LED# — D29 White — R633 820_0402_5% — +5VS_LED

28 GPIO19 — R667 0_0402_5% — D29 AMBER — R2031 470_0402_5% — +3VS

Amber QSMF-C16E_AMBER-WHITE

HDD LED

1009 lower LED power consumption

1025 change to follow IBT00 design
1102 Change GSENSOR LED control pin from SB to KBC
1106 Delete R668, control by SB

for debug only

1212 Delete SW5,SW6

K/B backlight

CONN@ JP51 — R2059 0_0805_5% — +5VS_LED

ACES_85201-04051

+3VS — Q115 DTA114YKAT146_SOT23-3 — 32 WL_LED#

WL_BLUE_LED# 40

38 BT_LED — 2N7002DW-7-F_SOT363-6 Q114A — R505 100K_0402_5%

+3VS — R2098 10K_0402_5%

1212 Add R2098 for LED

WL_LED — 2N7002DW-7-F_SOT363-6 Q114B — R506 100K_0402_5%

SWITCH BOARD.

1224 Add Cap

1009 Remove double pull up resisters

+3VL — C2122 4.7U_0805_10V4Z

+5VS_LED

CONN@ JP38

40 ESB_CLK — R652 2@0_0402_5%
40 ESB_DAT — R641 2@0_0402_5%
39,40,45 SMB_EC_CK1 — R644 2_0_0402_5%
39,40,45 SMB_EC_DA1 — R646 2_0_0402_5%

Updated @1029

39,40 ON/OFFBTN_LED# — CAP_CLK — CAP_DAT

40 IZC_INT
+5VALW_LED — R705 150_0402_5%
40 LID_SW#
40 ON/OFF — R666 1K_0402_5%

R640 10K_0402_5%

@D83 PJDLC05_SOT23-D

GND GND

ACES_85201-1005N

1025 change Capactivity board pin defination

T/P Board (Inculde T/P_ON/OFF)

1212 Change TP power rail to +5VALW

1212 EMI request

+5V — @C824 0.1U_0402_16V4Z

TP_BTN# — TP_LED# — D87 PSOT24C_SOT23-3

TP_DATA — TP_CLK — D31 PSOT24C_SOT23-3

+5VALW — Q29 SI2301BDS-T1-E3_SOT23-3 — +5V

R645 10K_0402_5%

CONN@ JP33

+5VS_LED

TP_CLK 40
TP_DATA 40
TP_BTN# 40
TP_LED# 40

32,40,43,49 SYSON — SYSON — Q31 2N7002_SOT23-3

@C825 100P_0402_50V8J — @C826 100P_0402_50V8J

ACES_85201-08051

0226_Change package from 0603 to 0402.

SP01000H300 S H-CONN ACES 85201-0405N 4P P1.0
ACES_85201-0405N_4P

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

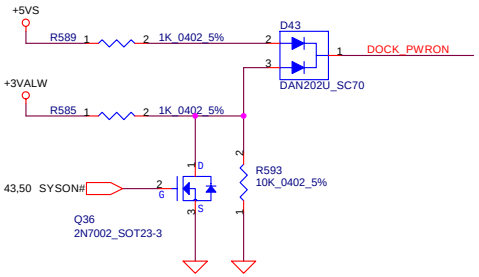
Compal Electronics, Inc.

Title: KBD, ON/OFF, SW, CIR

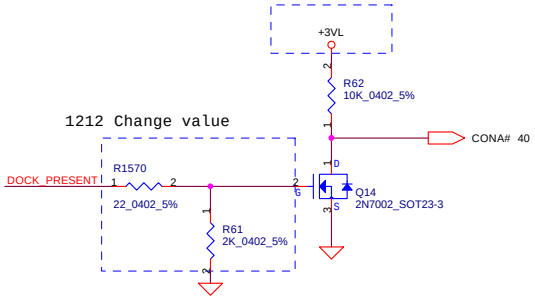
Size: Custom | Document Number: LA-4082P Vader Discrete | Rev: 0.1

Date: Wednesday, December 26, 2007 | Sheet 41 of 58

DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

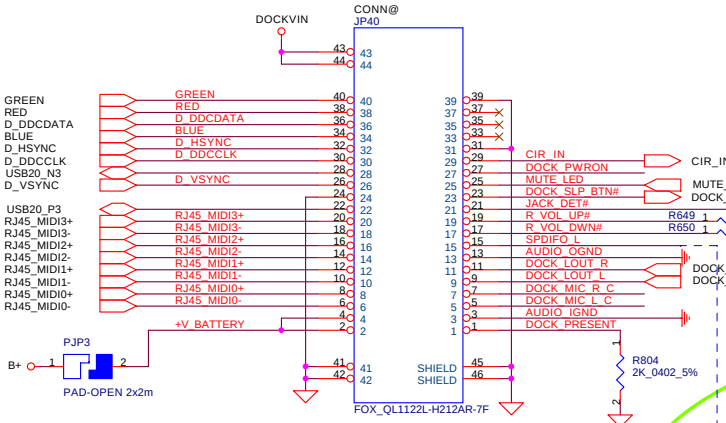


1112 Change power rail from +3VALW to +3VL



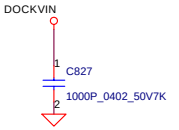
1009 Remove TV components

Atlas/ Saturn Dock

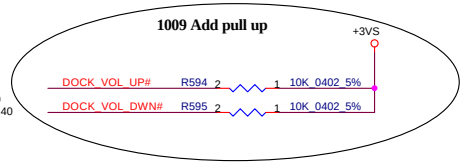


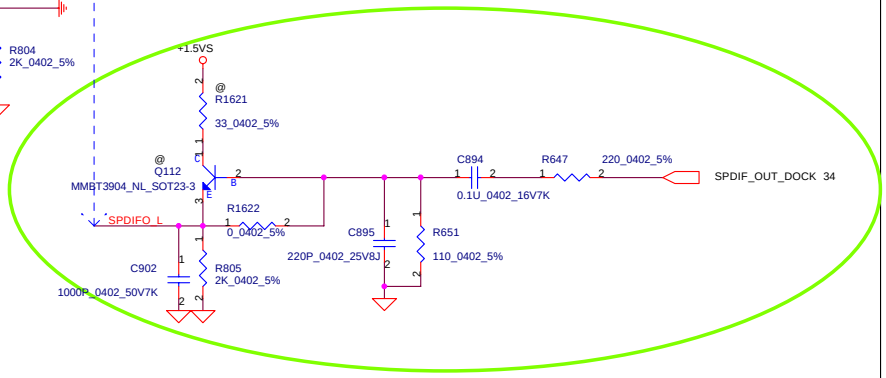
CIR_IN 36,40
MUTE_LED 40
DOCK_SLP_BTN# 40
JACK_DET# 34,36
R649 200_0402_5%
R650 200_0402_5%
DOCK_VOL_UP# 40
DOCK_VOL_DWN# 40
DOCK_LOUT_R 36
DOCK_LOUT_L 36

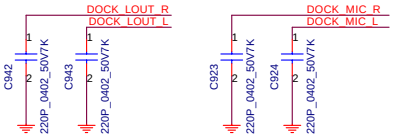
need change to reverse type connector

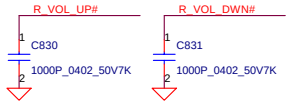


1009 Add pull up



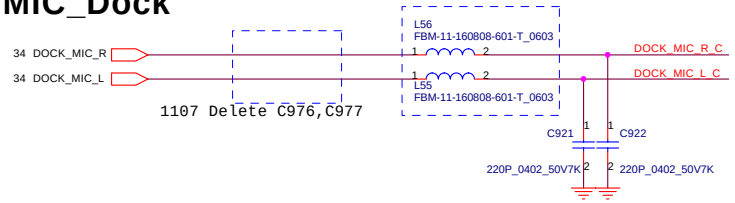




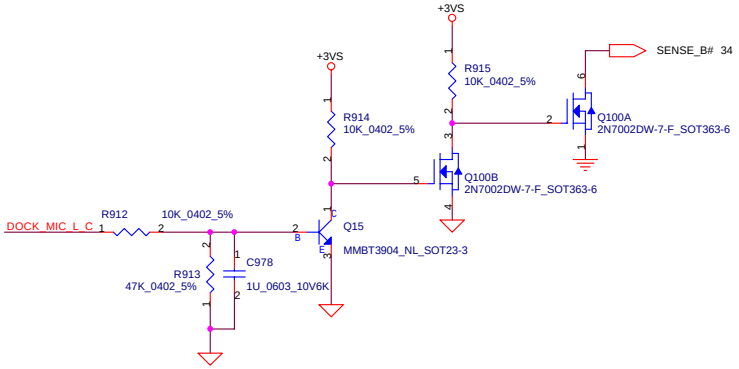


MIC_Dock

Need 600 Ohm 500 mA



1107 Delete C976,C977



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

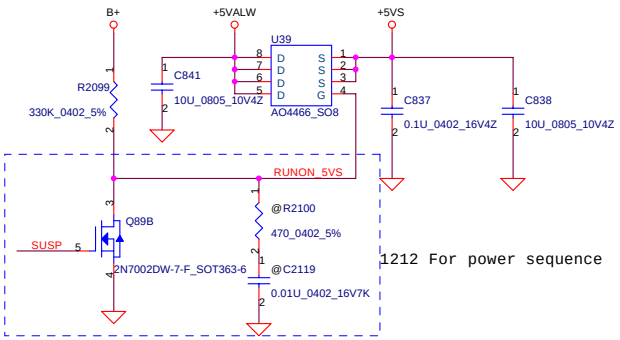
Compal Electronics, Inc.

Title: **DOCK CONN.**

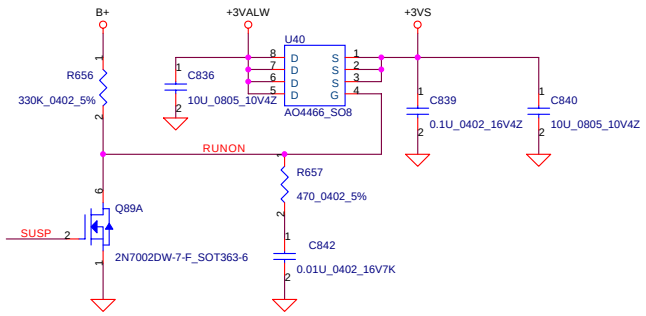
Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.1

Date: Wednesday, December 26, 2007 Sheet 42 of 58

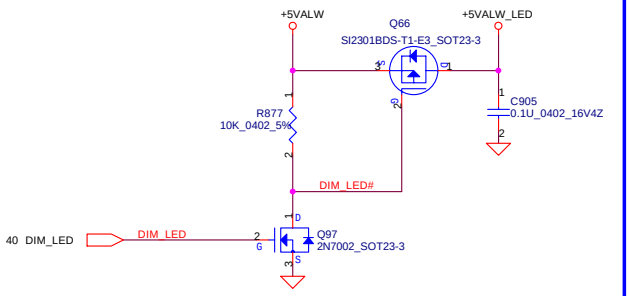
+5VALW to +5VS Transfer



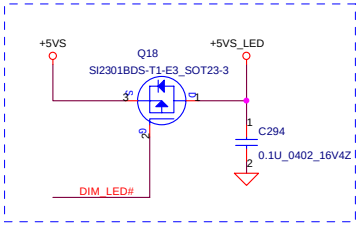
+3VALW to +3VS Transfer



DIMM LED

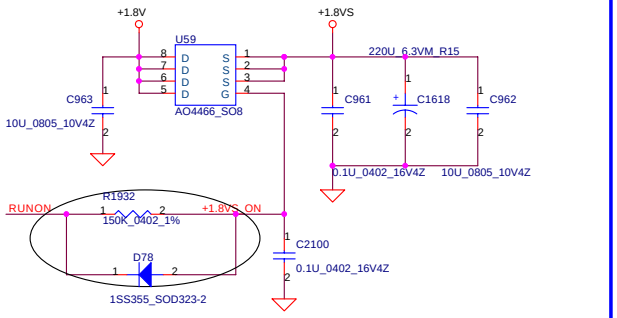


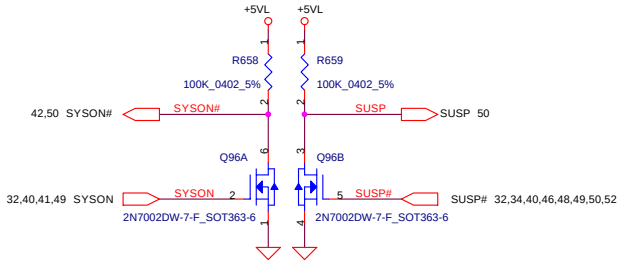
1009 Add for LED power

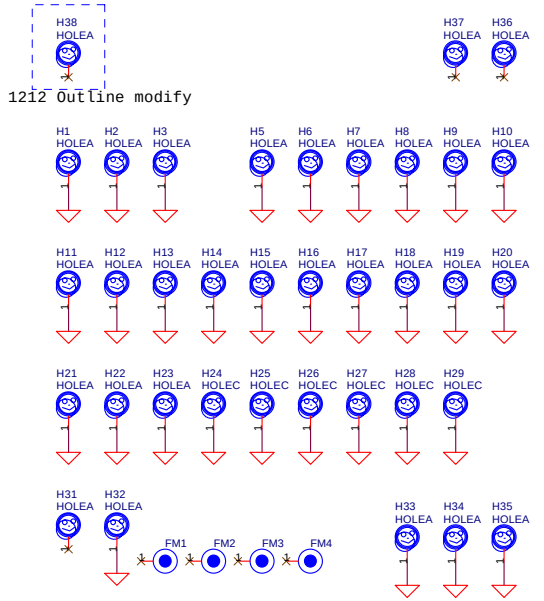


1212 Delete Q97B,R211

+1.8V to +1.8VS Transfer

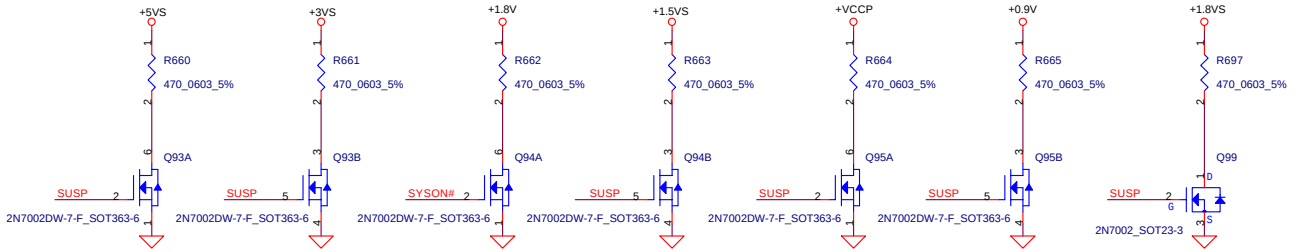






1212 Outline modify

Discharge circuit



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

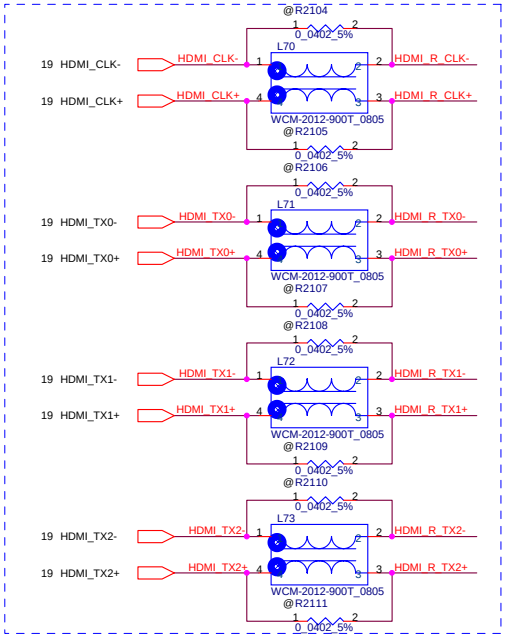
Compal Electronics, Inc.

Title: **DC/DC Interface**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.1

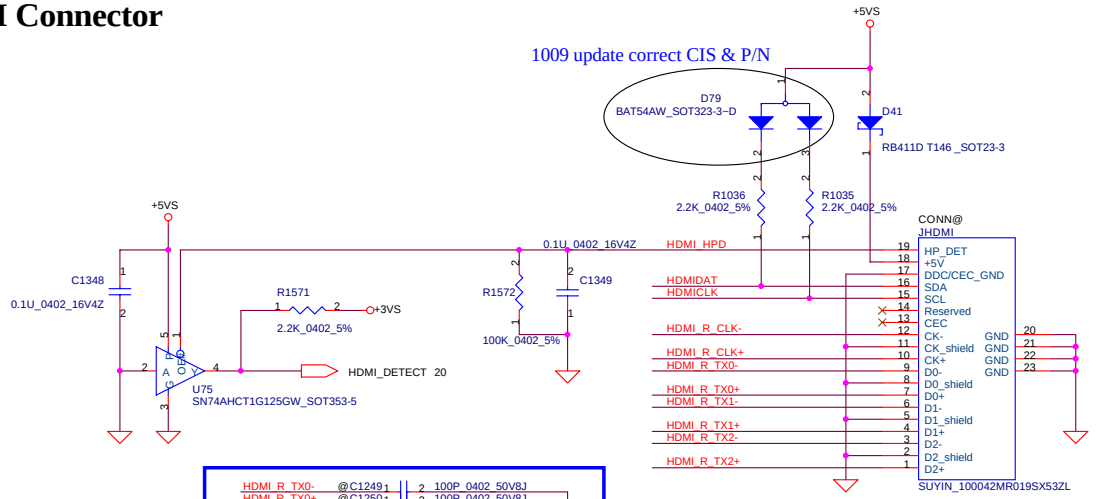
Date: Wednesday, December 26, 2007 | Sheet 43 of 58

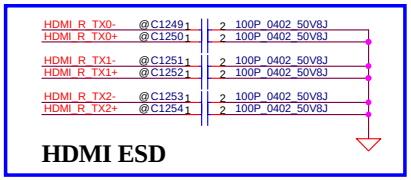
1212 Add 0 ohm



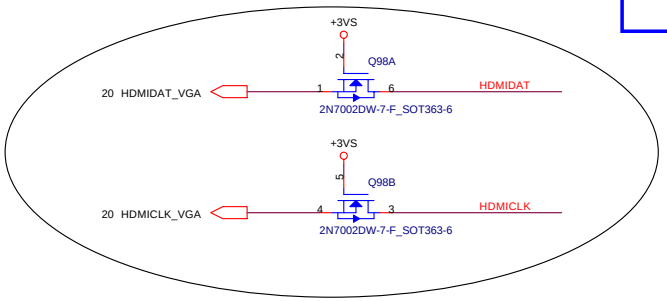
HDMI Connector

1009 update correct CIS & P/N





HDMI ESD



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **HDMI LS & Conn.**

Size	Document Number	Rev
Custom	LA-4082P Vader Discrete	0.1

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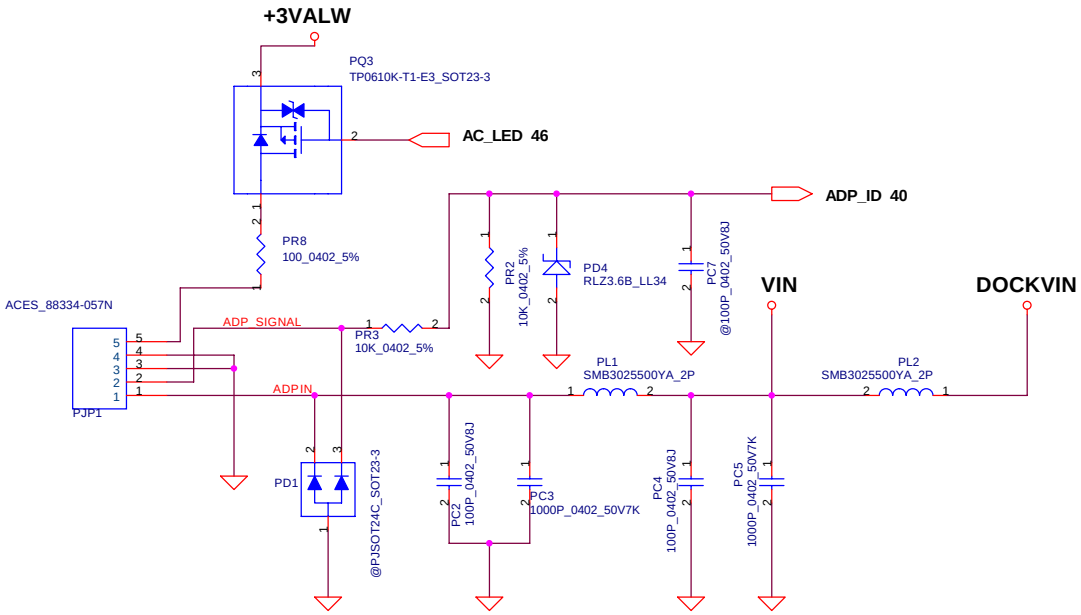
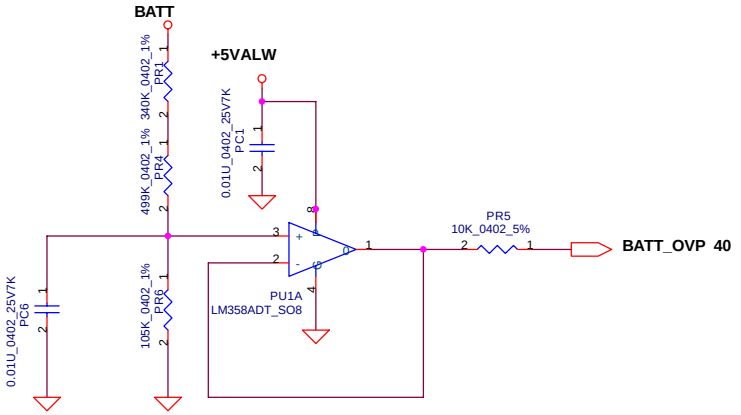
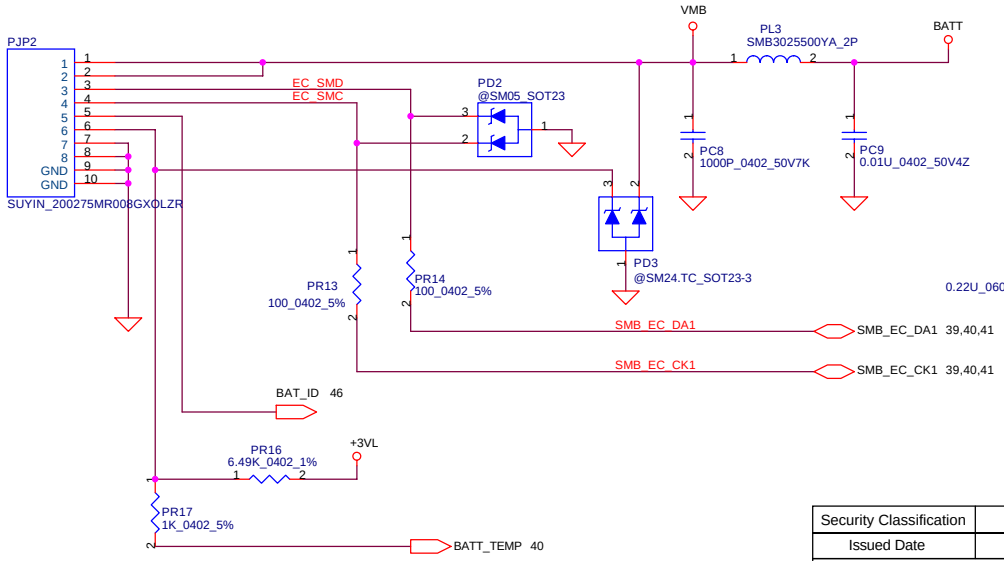
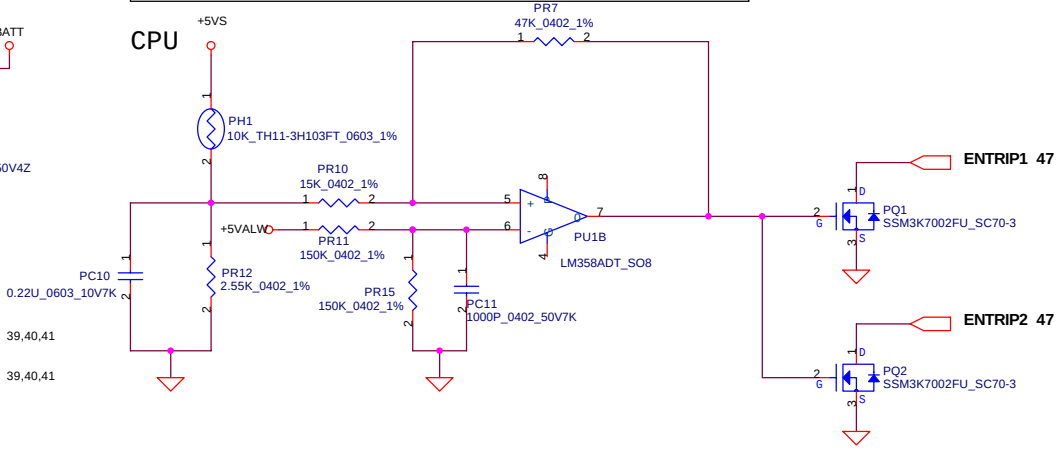




PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C





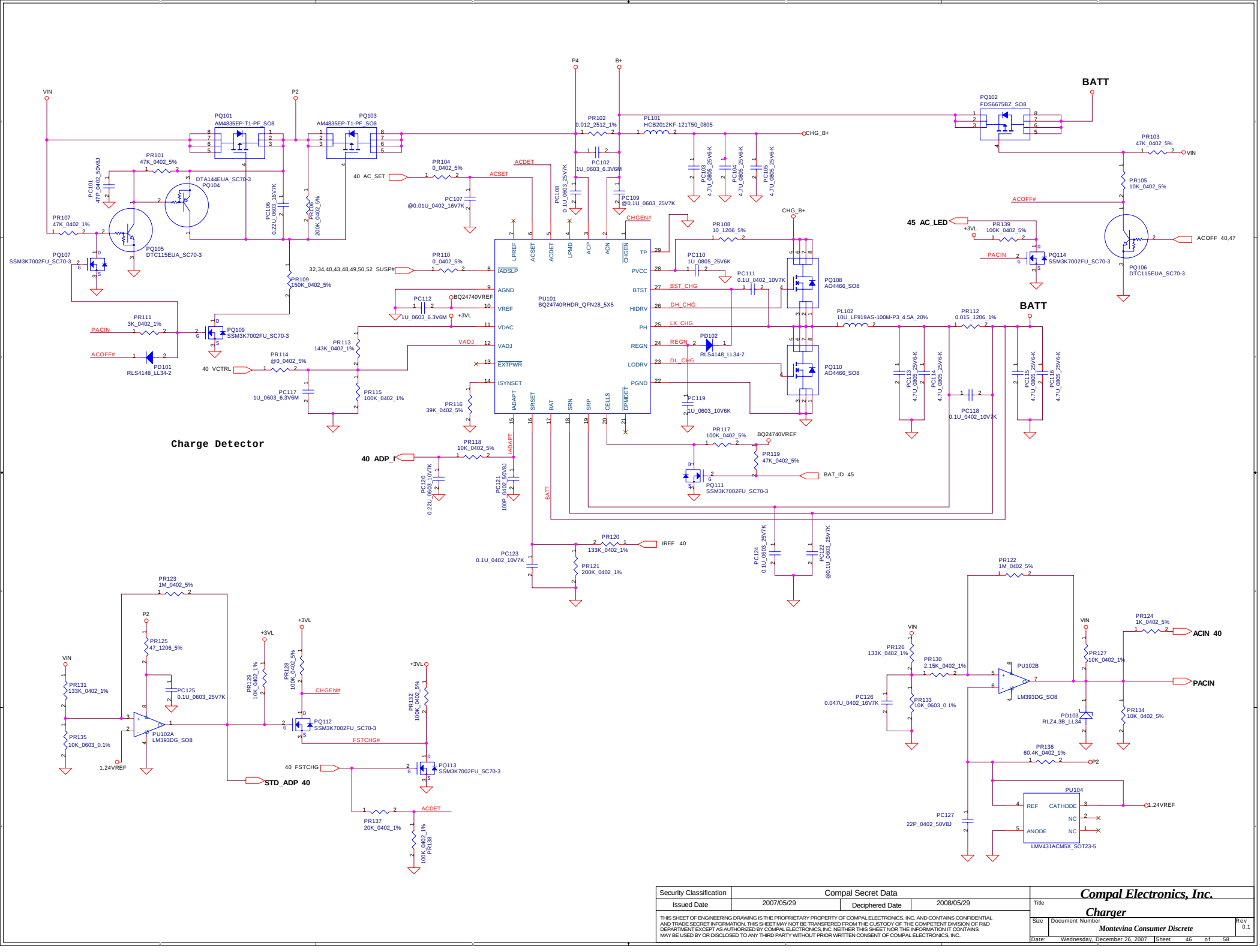
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

Size	Document Number	Rev
	Montevina Consumer Discrete	0.1

Date: Wednesday, December 26, 2007 | Sheet 45 of 58



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **Charger**

Size | Document Number: *Montevina Consumer Discrete* | Rev: 0.1

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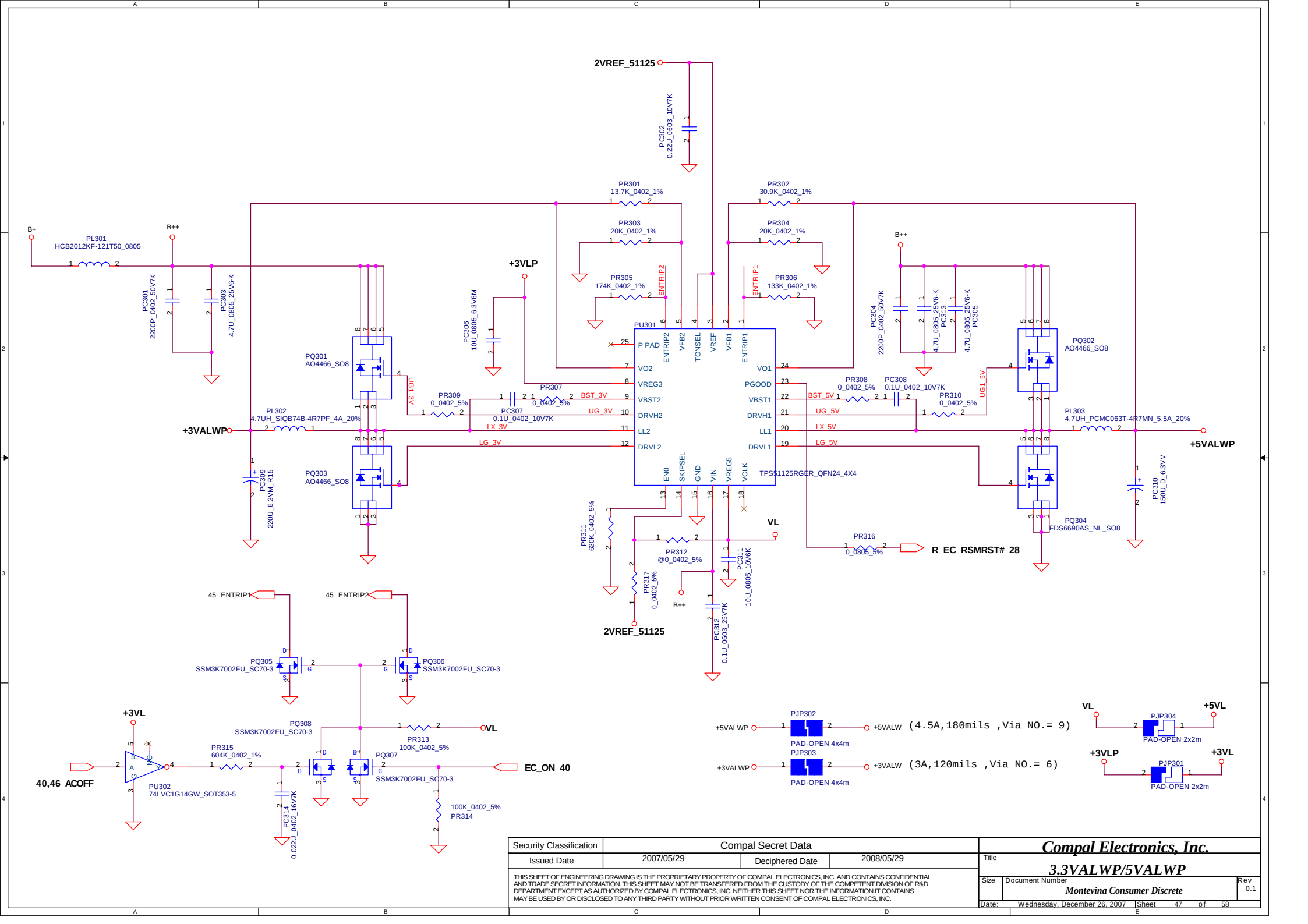

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
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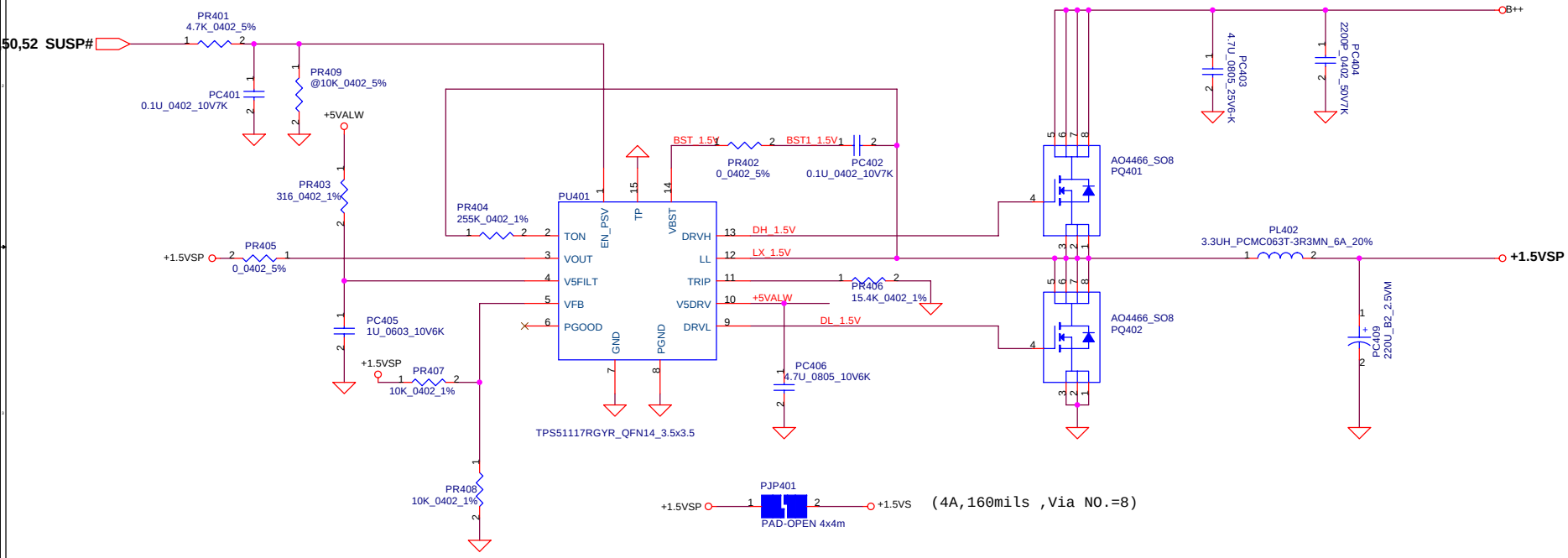

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.5VSP**

Size	Document Number	Rev
	Montevina Consumer Discrete	0.1

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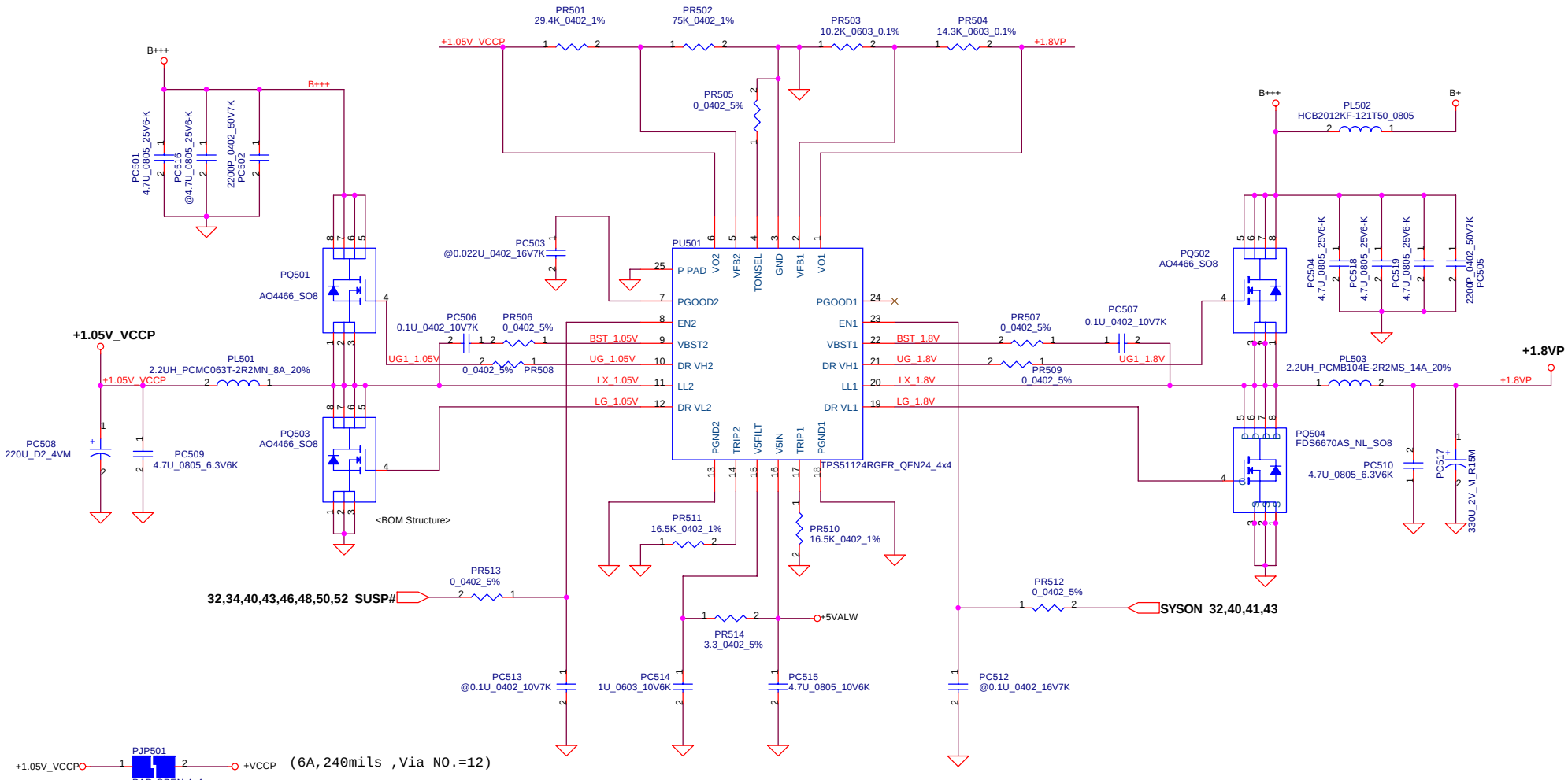

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.05V_VCCP/1.8VP**

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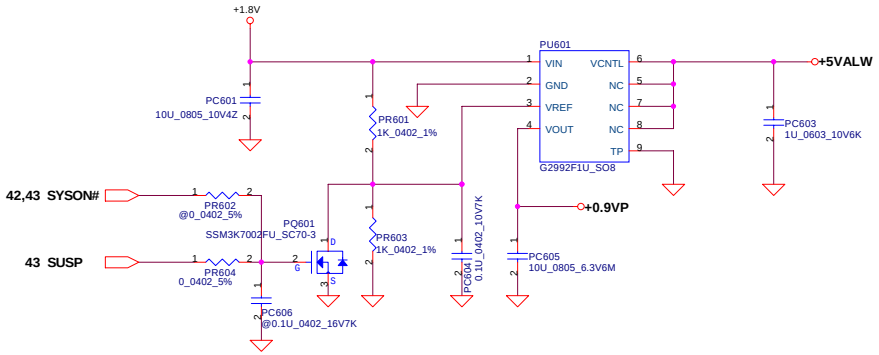
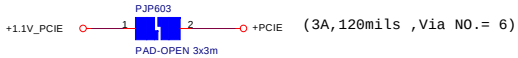
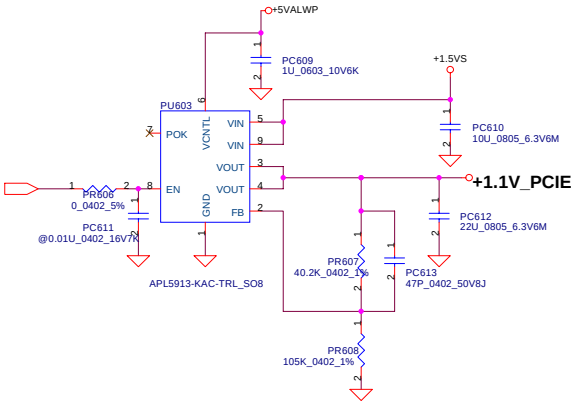


(2A,80mils ,Via NO.= 4)



(3A,120mils ,Via NO.= 6)



Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **0.9VSP/2.5VSP/1.2V_PCIE**

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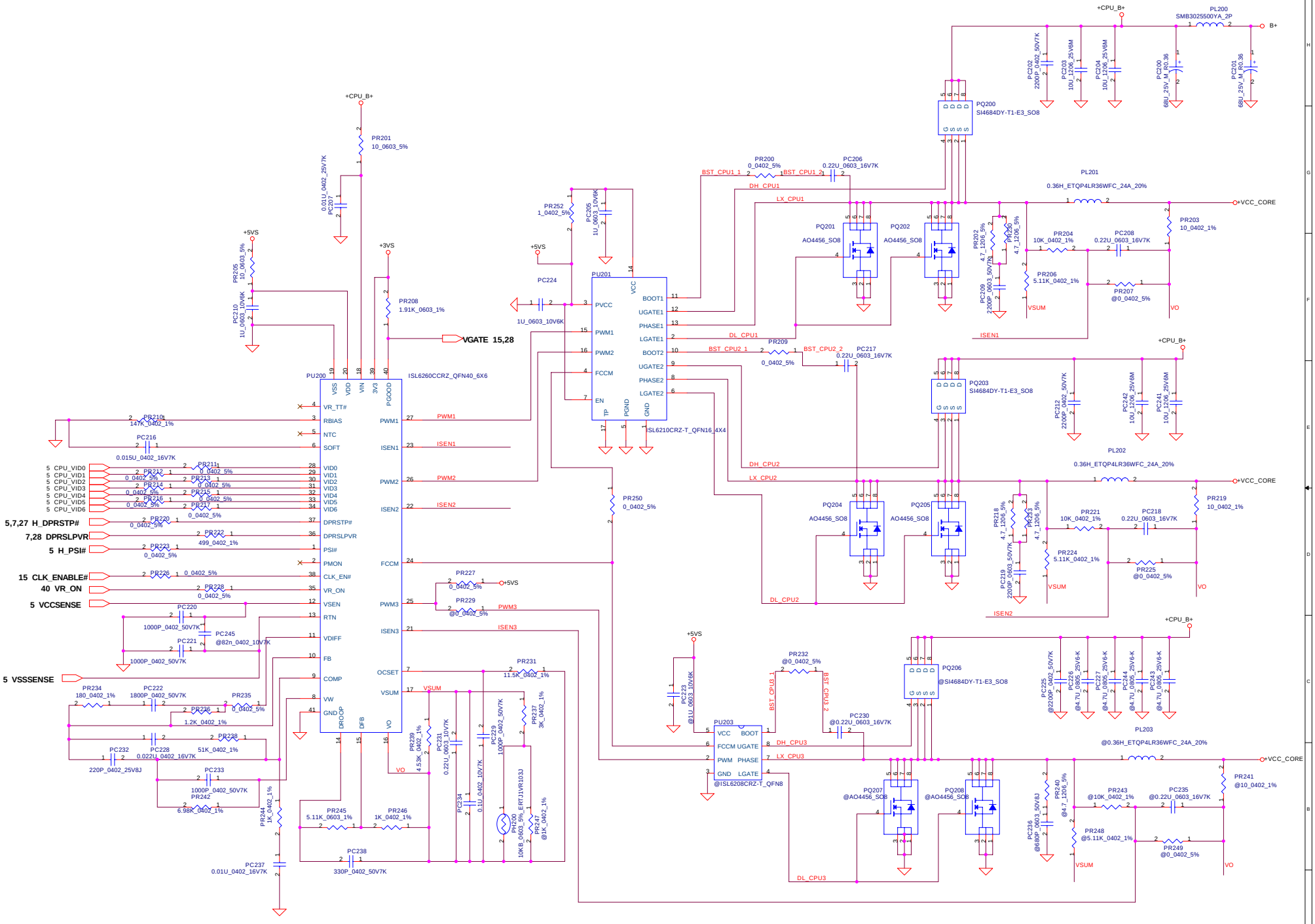

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CPU_CORE**

Size: C | Document Number: *Montevina Consumer Discrete* | Rev

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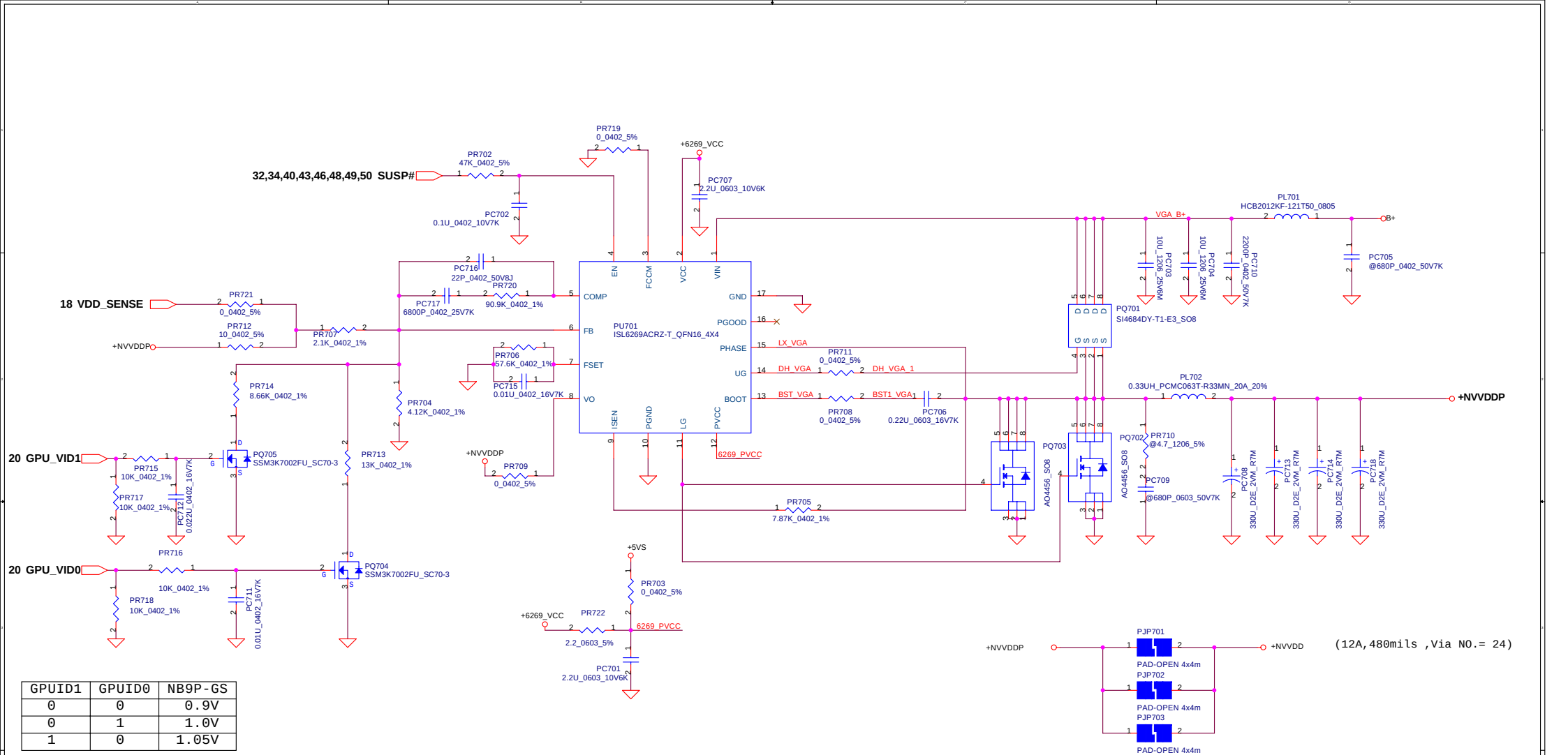

GPUID1	GPUID0	NB9P-GS
0	0	0.9V
0	1	1.0V
1	0	1.05V

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **VGA_CORE**

Size	Document Number	Rev
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as 1uf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2

	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.10.08>	1	Fix Audio disappear	follow Intel SB design suggestion to separate HDA Bus	27	Add R439, R440, R442, R444	0.2
	2		Add to determine board type and project	28	Add R777, R776, R774, R775	0.2
			Meet EC request	28	non-stuff R419, R695	
	3	Fix Audio disappear	follow Intel SB design suggestion	29	Change power rail from +1.5v to +3v	0.2
	4		meet SW debug request	32	Add Debug CLK and PLT_RST#	0.2
	5	Fix Audio disappear	follow Intel HDA bus design for Discrete platform	34	Change codec power rail from +1.5v to +3v	0.2
	6	Fix can not power on issue	Meet EC and SPI access sequence	39	change SPI power rail from+3valw to +3VL	0.2
	7		Follow Intel design guide	7	Change R30 value	0.2
<2007.10.09>	1	Fix HDMI can not detect	follow Nvidia design request	18	change HDMI I2C channel to I2C B channel	0.2
	2		Meet HP request to remove TV	18	Remove TV all components at VGA side	0.2
	3		update ODD footprint	30	update JODD footprint	0.2
	4	Fix ODD wrong pins	lower system power consumption	33	change Card Reader LED power rail	0.2
	5		Meet Sub-woofer pwoer request	37	change D81, D82	0.2
	6	Solve EC always damage	Solve EC always damage	40	change D53 direction	0.2
	7		Double pull up and pwoer rail is different	41	Remove pull up resisters	0.2
	8		lower system power consumption	41	change Cap-lock, HDD LED power rail	0.2
	9		Meet HP request to remove TV	42	Remove TV all components at Dock side	0.2
	10		lower system power consumption and meet LED status	43	Add +5VS_LED (Inculde DIM function)	0.2
	11		solve HDMI pull up	44	update D79 footprint	0.2
<2007.10.19>	1		Meet ME limit area at KBC	27	Change Y4 material	0.2
	2		Follow IDT suugestion	35	change R886 to 1206	0.2
	3		Follow Nvidia suggestion	25	Change R193, R196 size to 0603	0.2
<2007.10.20>	1		follow correct power rail	38	change Touch screen power rail	0.2
	2		Meet HP request	39	Change ST G-sensor P/N & package	0.2
	3		Meet HP request for WLAN &TV slot swap	32	Swapped WLAN and TV all support components	0.2
<2007.10.22>	1		Change LAN chip to meet Energy star spec	31	change LAN brand to Realtek	0.2
	2					

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Title: HW PIR(1)

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.10.23>	1	Fix USB loading of SB	follow 14" Blade USB channel design	28 17 32 38 38 42	Chnage all USB channel Change USB channel of Camera Change USB channel of WLAN & TV Tuner & New card Change USB channel of Left side, Right side, E-SATA Change USB channel of Touch screen, Finger print Change USB channel of Dock	0.2
	2		Follow JMicro CardReader Vendor Suggestion	33	Change R114 & R1546 value	0.2
	3		Solve Speak no sound issue	36 36 34	add pullup at HP_DET# Change Q203 to N-channel FET Change R524 pin2 connect to JACK_DET#	0.2
<2007.10.25>	1		Meet HP request for QC and DC co-lay	4 5 6	add GTLREF and XDP circuits	0.2
	2		Meet Intel request for CLK request	15	Add R127 to meet Intel CLK design	0.2
	3		Solve G-sensor LED control	28, 41	change G-sensor LED control to GPIO19 of SB	0.2
	4		Follow Capactivity board design	41	change Pin7 & 7 NET	0.2
<2007.10.31>	1			34	Use Audio Codec GPIO5 to shutdoown Sub-woofer	
	2			40	Connect HDA_RST#_CODEC to EC	
	3			34	Separate SPDIF out to VGA and Docking	
<2007.11.02>	1		Common design	16	R204,R205 no stuff	0.3
	2		Change +5VS_LOGO resistor size to 0805	17	R642 size to 0805	0.3
	3		Double pull up	20	R2046,R2047 no stuff	0.3
	4		For card reader power	33	install R1553	0.3
	5		For KBC C0 version	40	R616 no stuff	0.3
	6		Add pull down resistor for SUSP# and SYSON	40	Change R615 to 8.2k and add R2062	0.3
	7		Change HAD_RST#_CODEC from KBC pin 36 to pin 38	40		0.3
	8		Change GSENSOR LED control pin from SB to KBC	41	Install R668, no install R667	0.3
	9		Add pull down for sub-woofer power-down	37	Add R2063	0.3

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **HW PIR(2)**

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.11.04>	1		Move resistor from LS4086P to MB	41	Add R2064	0.3
	2		Change to dual type for layout space	16	Change Q69,Q70 to dual type	0.3
	3		Only use LIS302DLTR	39	U77, R2025 no install	0.3
	4		Change CIR_IN power rail	40	Connect R642.1 to +5VL	0.3
<2007.11.05>	1		nVIDIA suggestion for NB9M-GS/GE	22	R1005 change to 475 ohm	0.3
	2		nVIDIA suggestion -- add Pull up 2.2K on HDMIDAT_VGA and HDMICLK_VGA to +3VS. at VGA side	18	Add R2065,R2066	0.3
<2007.11.06>	1	EMI request	CRT add resistor for EMI	16	Add R2069,R2070,R2071	0.3
	2		HP suggestion	34	Change C746,C747,C748,C749 to 1000PF	0.3
	3		USB camere power and add GPO pin for shutdown	17	Add PJP5,R2072,R2073	0.3
	4		LAN DSM support	31	1. USB camera – SB GPIO20 2. ISOLATE – SB GPIO18 3. LAN OGPIO – SB GPIO14	0.3
	5		EC_BEEP	34	Add R2076	0.3
	6		G-sensor LED control by SB	41	Delete R668	0.3
<2007.11.07>	1		Modify FPR connector pin assignment	38	Modify JP41 pin assignment	0.3
	2		Modify Audio	34 36 37 42	1. Add C2108,C2109,R2080,R2081 2. Add R2082,R2083 3. Change C1008,C1009 to 1UF 4. Delete C976,C977 5. Delete R515,R516,C916 6. Change C982,C980,C984 from 5900p to 0.039u 7. Change C983,C992 from 1000p to 100p 8. Add EC_MUTE# to sub-woofer shutdown pin and R2084	0.3
	3		nVIDIA suggestion	20	1. Delete strap pin 2. Change R1020, R1015, R1010 to 475 ohm 3. Swap THERMDN and THERMDP	0.3
<2007.11.08>	1		EMI request	17	Add C2100,C2111	0.3
	2		Audio	36 37	Change C970,C971 to 22uF, add C2112, change D38 to dual type	0.3
<2007.11.09>	1		nVIDIA suggestion	19 20	Change HDMI DDC to I2CD R387,R388,R415,R422,R427 -- install Change R415 to 10 ohm and no install Delete R99, Change +IFPC_PLLVDD to +PCIE	0.3
	2		JMicron suggestion	33	Do not install R2030 Add D86 for card reader wake up Add SB GPIO22 for wake up event	0.3
<2007.11.12>	1		HP request	4	Add EMC1403 for Qaud core	0.3

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Title: HW PIR(3)

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	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.12.12>	1		MV DG for VDDC_QDAC	10	Chagne VCCD_QDAC to +1.5VS	0.4
	2		WLAN issue	32	Change XMIT_OFF#,WL_LED# and component to WLAN connector	0.4
	3		PCIE issue	28	Swap GLAN and NewCard PCIE port	0.4
	4		Modify CardReader LED	33	Use 2N7002 to control LED	0.4
	5		KBC	40	Change SMB_EC_DA1,SMB_EC_CK1 power rail from +5VL to +3VL Add C2118 for KBC pin124 Chagne EC_THERM power rail to +3VS	0.4
	6		WL_BLUE_LED# issue	41	Add R2089 pull up for WL_BLUE_LED#	0.4
	7		Power sequence	43	Add R2099,R2100,C2119 and Q89 change to dual type	0.4
	8		DIM_LED	43	Delete Q97B,R211	0.4
	9		EC_PME#	40	Change EC_PME# power rail to +3VALW	0.4
	10		WLAN issue	28	Add R2101	0.4
	11		Change TP power rail	41	Change TP power rail to +5VALW	0.4
	12		G-sensor	41	G-sensor -- R2031 change to 470 ohm and pull up to +3VS	0.4
	13		For Dock present	42	R1570 change to 22 ohm,R61 change to 2K ohm	0.4
	14		Clock generator	15	Add series R2102,R2103 for 27M_SSC and 27M_CLK	0.4
	15		HDCP ROM	19	R951 pull up,R959 no install	0.4
	16		EMI request	17	C272,C273,C2120 -- 470pF C828,C798 -- 10pF C2111 -- 220pF Add D87	0.4
	17		Modify BT/FPR circuit	38		0.4
<2007.12.24>	1		HP request	36 37	Change value	0.4
<2007.12.25>	1		For ENE cap board EMI issue	40	Add R and C	0.4

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Title: HW PIR(4)

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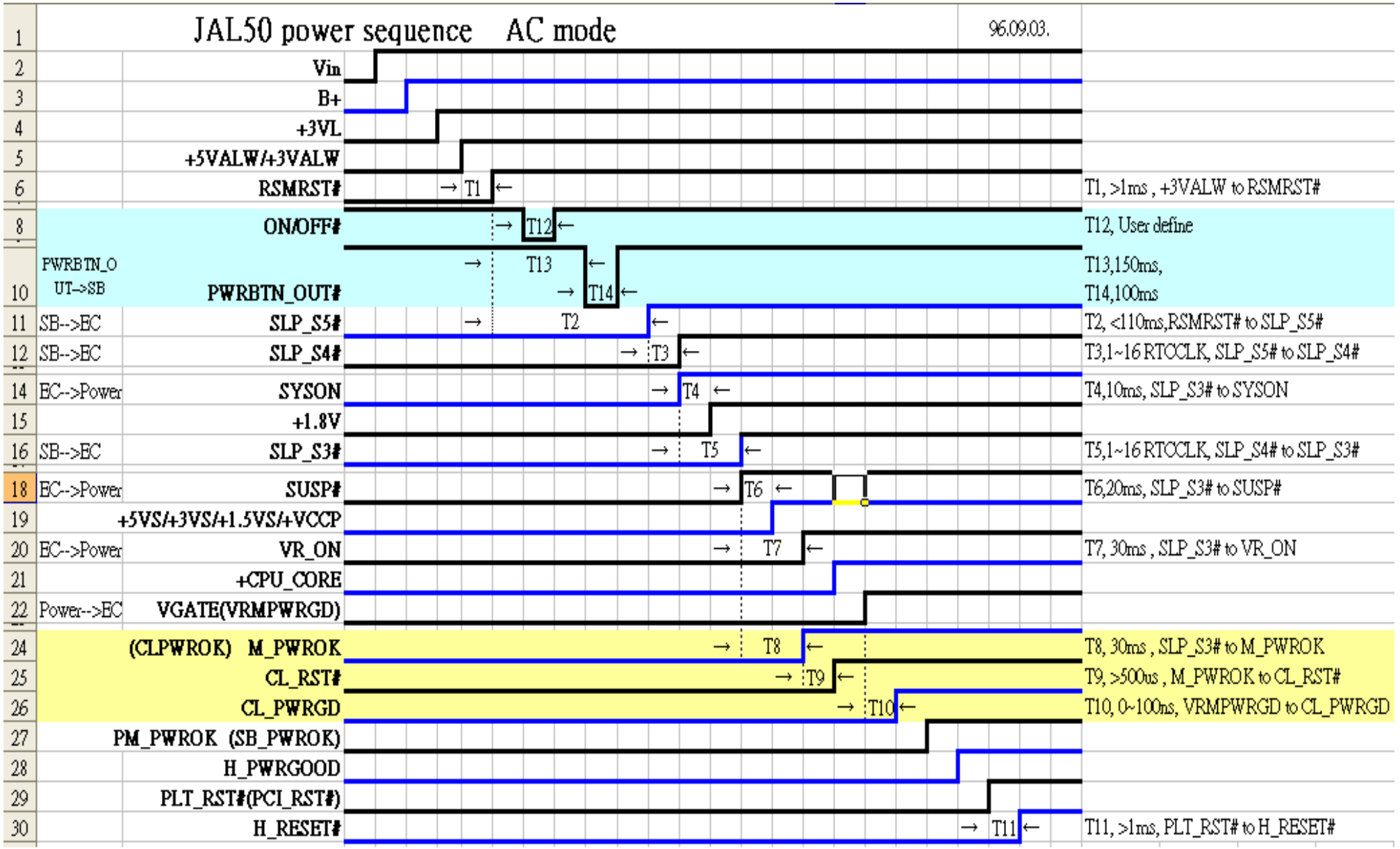

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Title: **Notes List**

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