Compal Confidential

Schematics Document

AUBURNDALE/CLARKSFIELD with Intel IBEX PEAK-M core logic

Dior DIS

2008-10-30

REV:0.1

機密	等級	硬體二部
		產出人員
		產出日期
		解密日期

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Title: **Cover Sheet**

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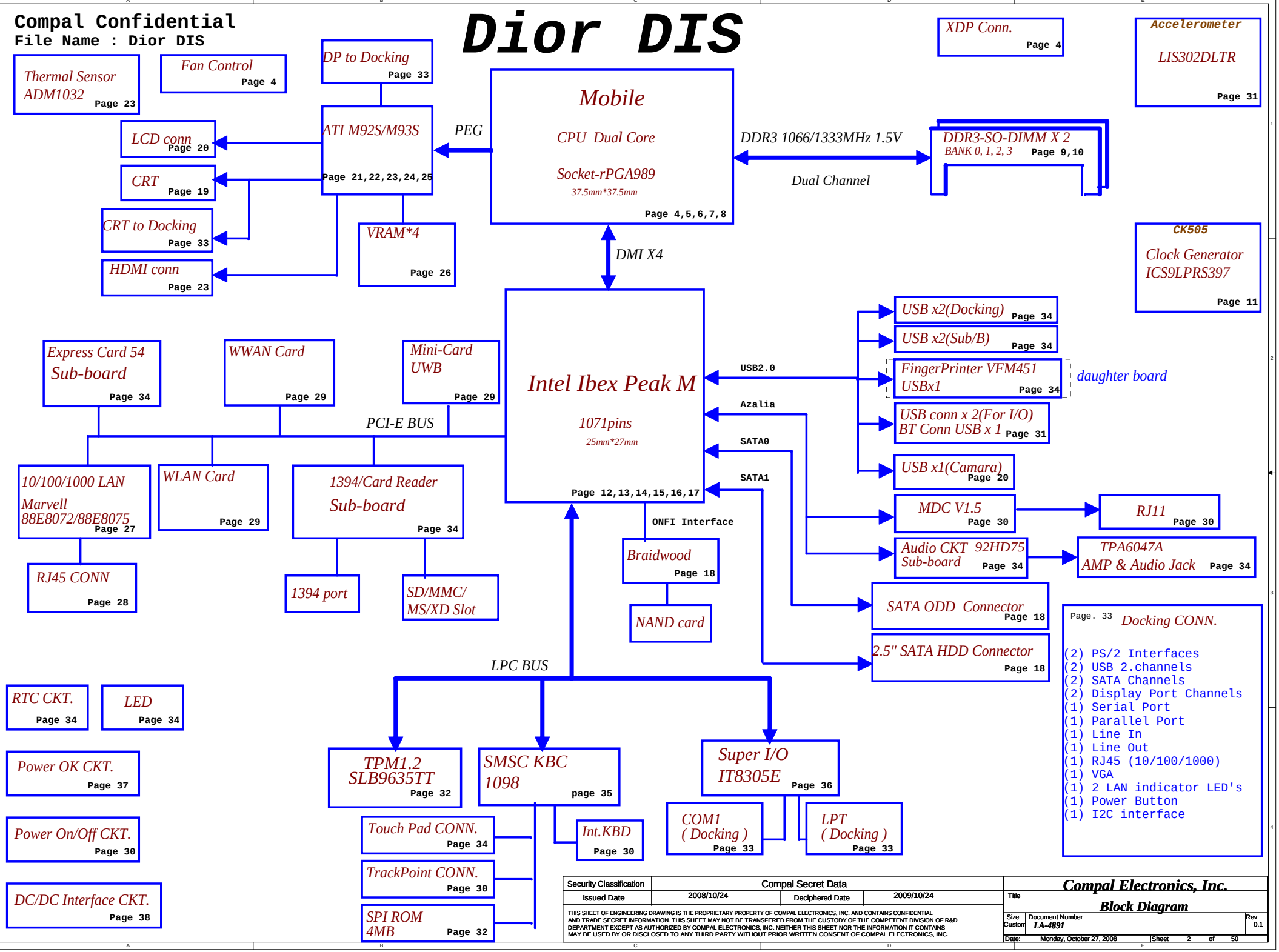
File Name : Dior DIS

Dior DIS



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Title: **Block Diagram**

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +NVVDD +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

Symbol Note :

: means Digital Ground

: means Analog Ground

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

M92@ : Install for M92 Graphic controller

8072@ : Install for 8072 NIC controller

1098@ : Install for 1098 KBC controller

CK32@ : Install for 32 pin CLOCK GEN

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.1

@ : means just reserve , no build

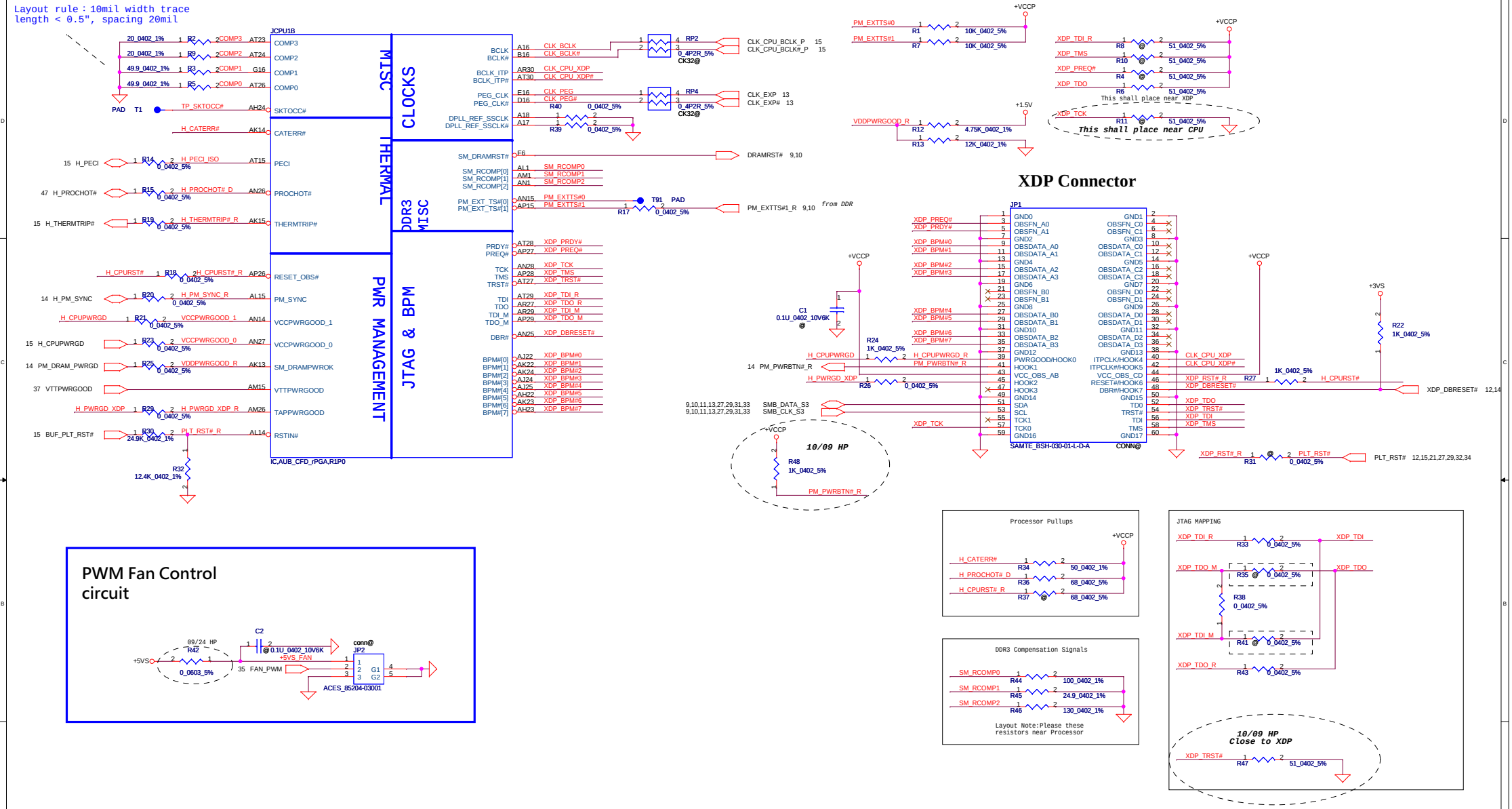
CONN@ : means ME part.

M93@ : Install for M93 Graphic controller

8075@ : Install for 8075 NIC controller

1091@ : Install for 1091 KBC controller

CK72@ : Install for 72 pin CLOCK GEN



PWM Fan Control circuit

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Title: **Auburndale(1/5)-Thermal/XDP**

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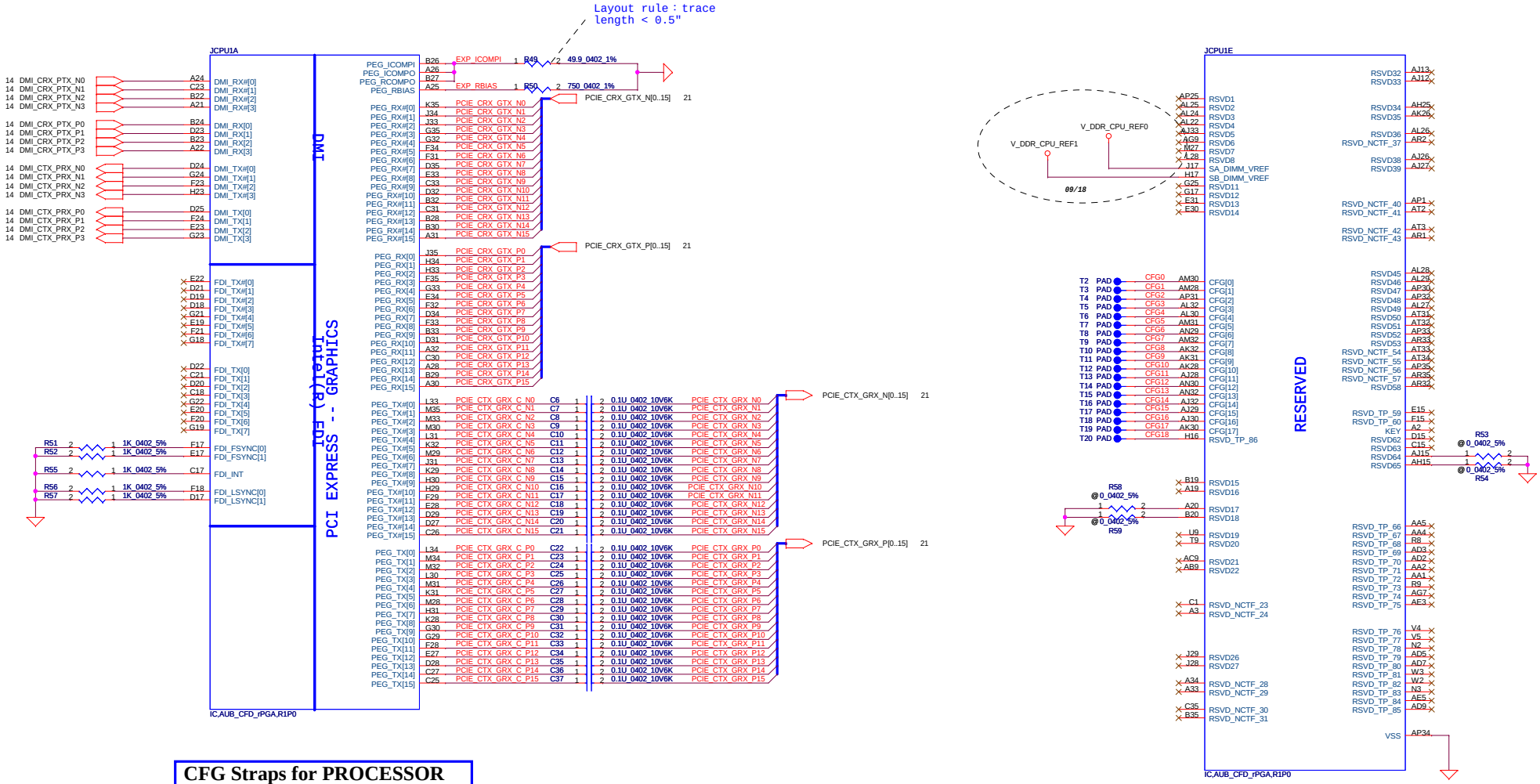

CFG Straps for PROCESSOR

CFG0 — R60 @3.01K_0402_1%

PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled

Not applicable for Clarksfield Processor

10/02

CFG3 — R62 3.01K_0402_1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 ->1, ...

R63

CFG4 — @3.01K_0402_1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 — R61 @3.01K_0402_1%

Only temporary for early CFD samples (rPGA/BGA)
No needed by MoW41.

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Title: **Auburndale(2/5)-DMI/PEG/FDI**

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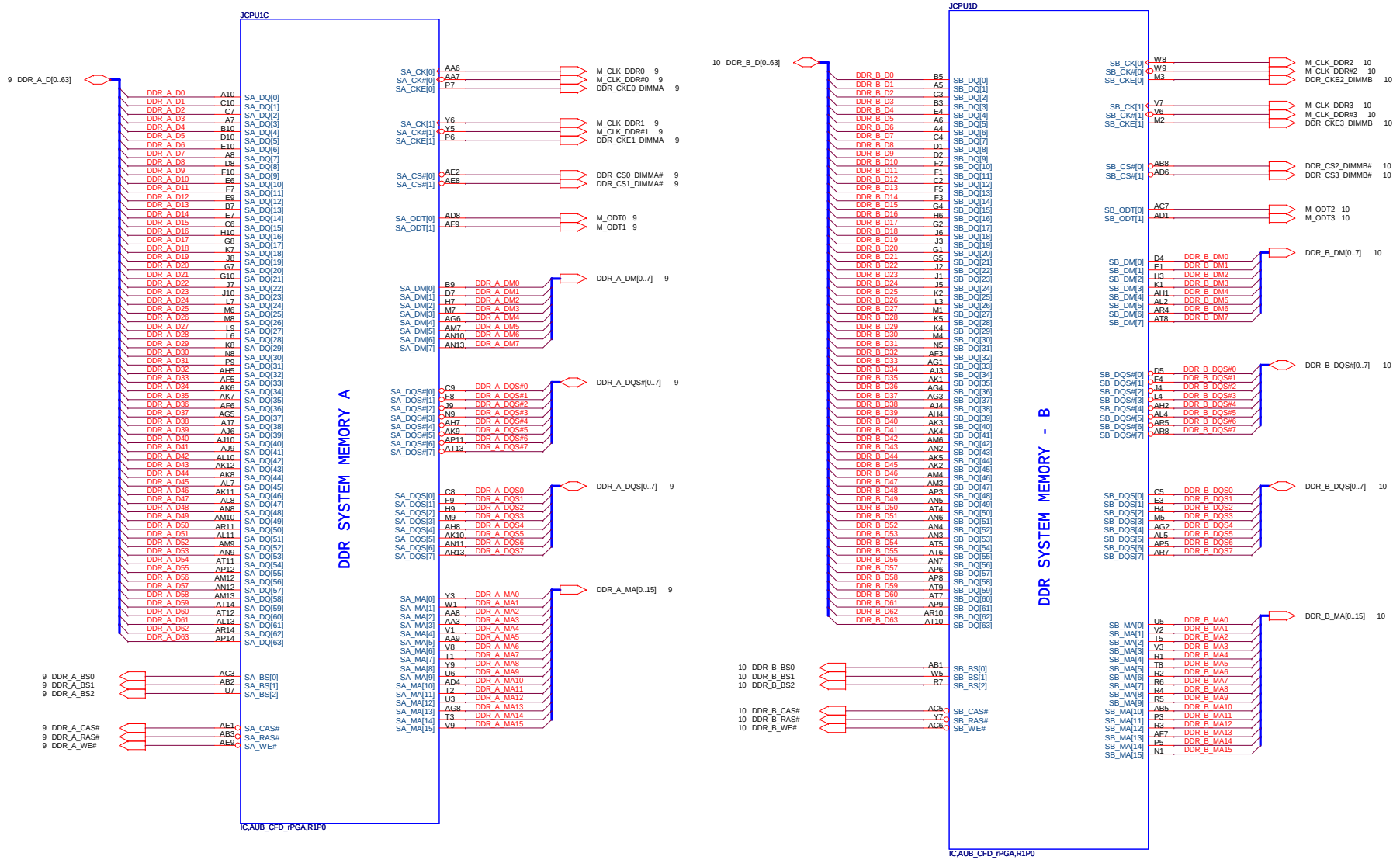

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Title: **Cantiga(2/6)-DDR2 A/B CH**

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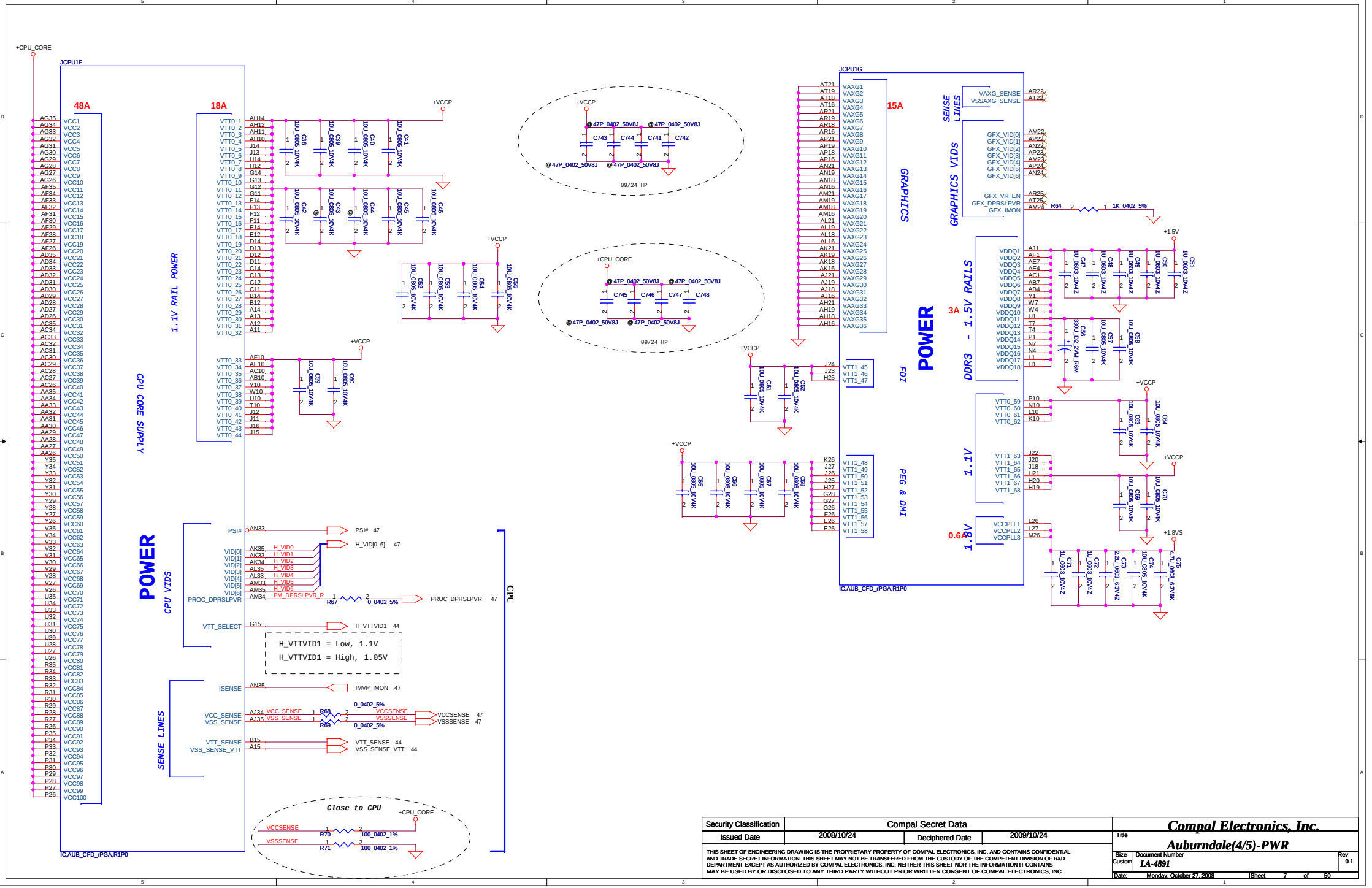

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Title: **Auburndale(4/5)-PWR**

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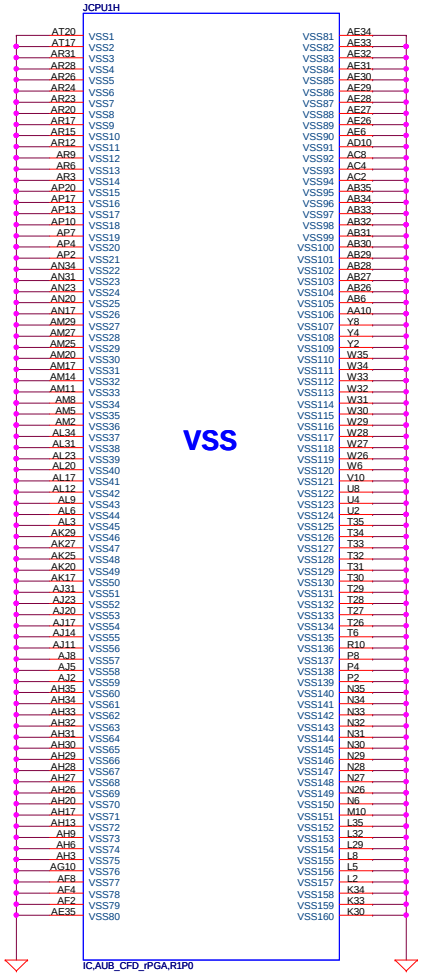

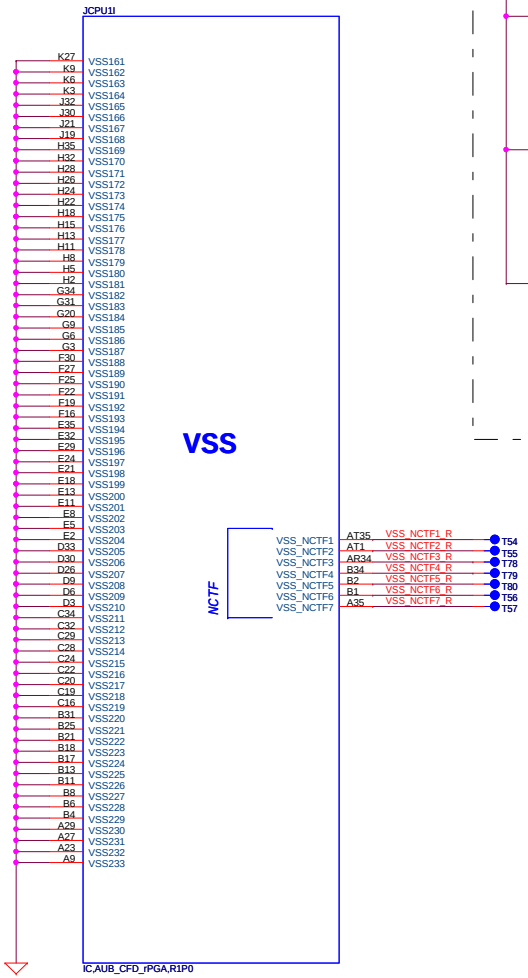

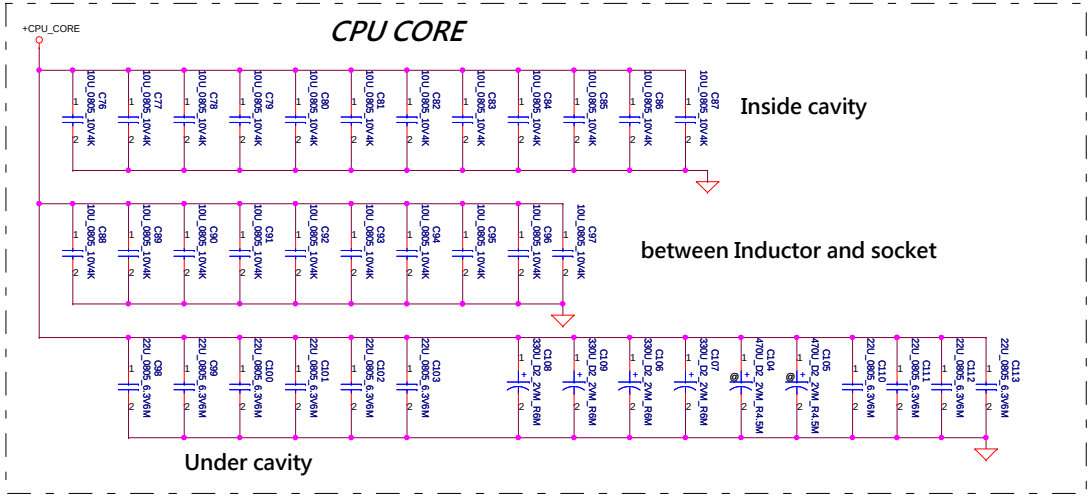

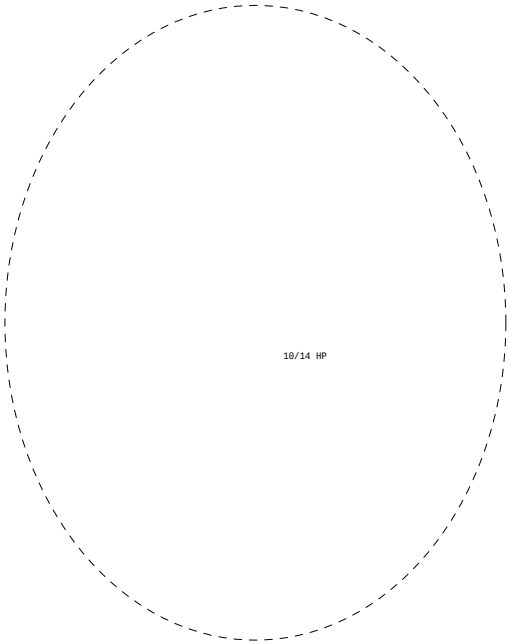

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Title: **Auburndale(5/5)-GND/Bypass**

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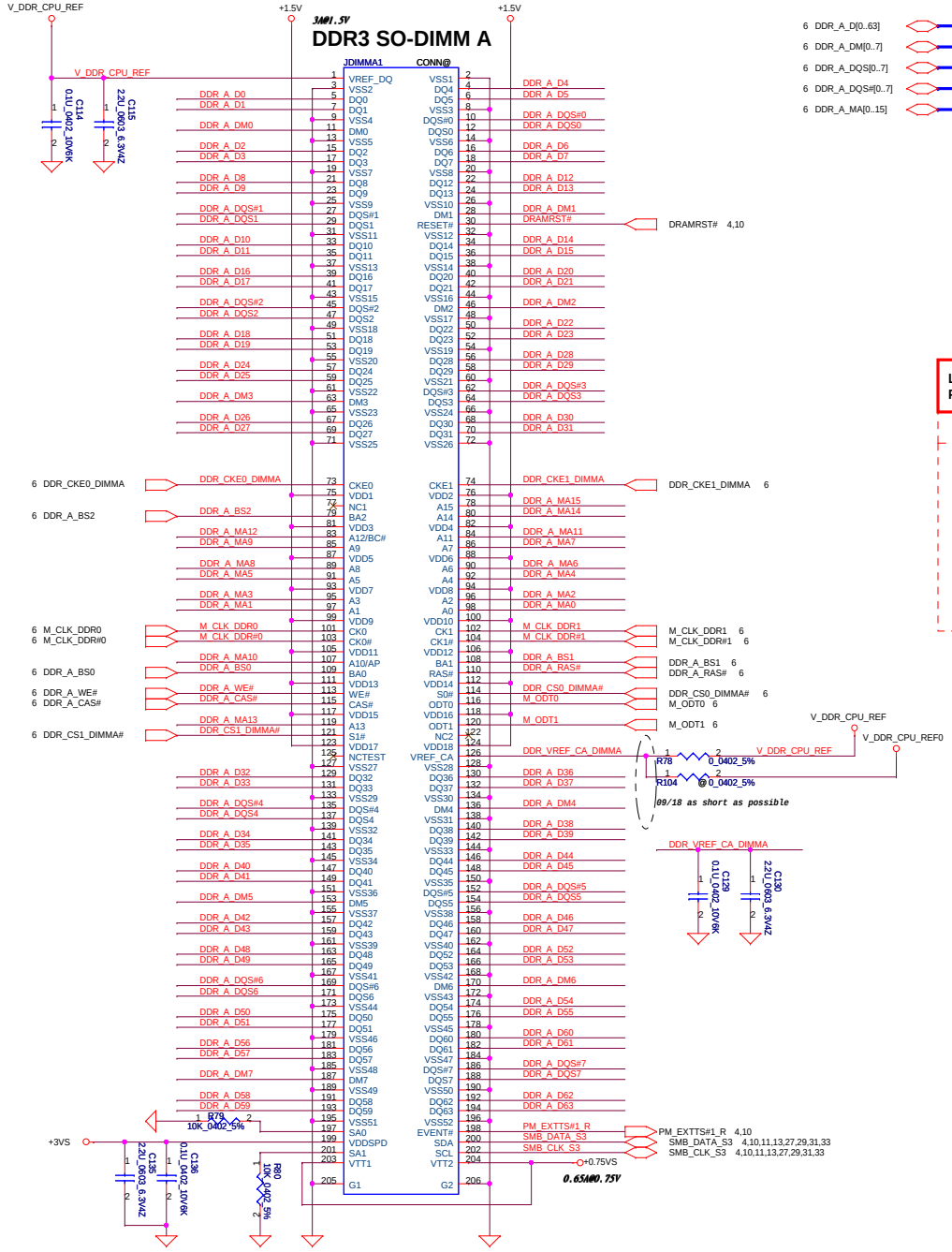
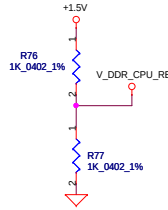
DDR3 SO-DIMM A

3A@1.5V

JDIMMA1 CONN@

6 DDR_A_D[0..63]
6 DDR_A_DM[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#[0..7]
6 DDR_A_MA[0..15]

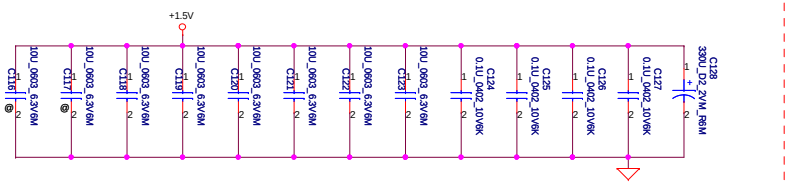




VREFDQ

M1	V_DDR_CPU_REF	R76, R77, R78, R81,
M3	V_DDR_CPU_REF0 V_DDR_CPU_REF1	R104, R110

Layout Note:
Place near DIMM



Layout Note:
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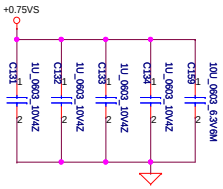

TOP SLOT

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Title: **DDRIII-SODIMM SLOT1**

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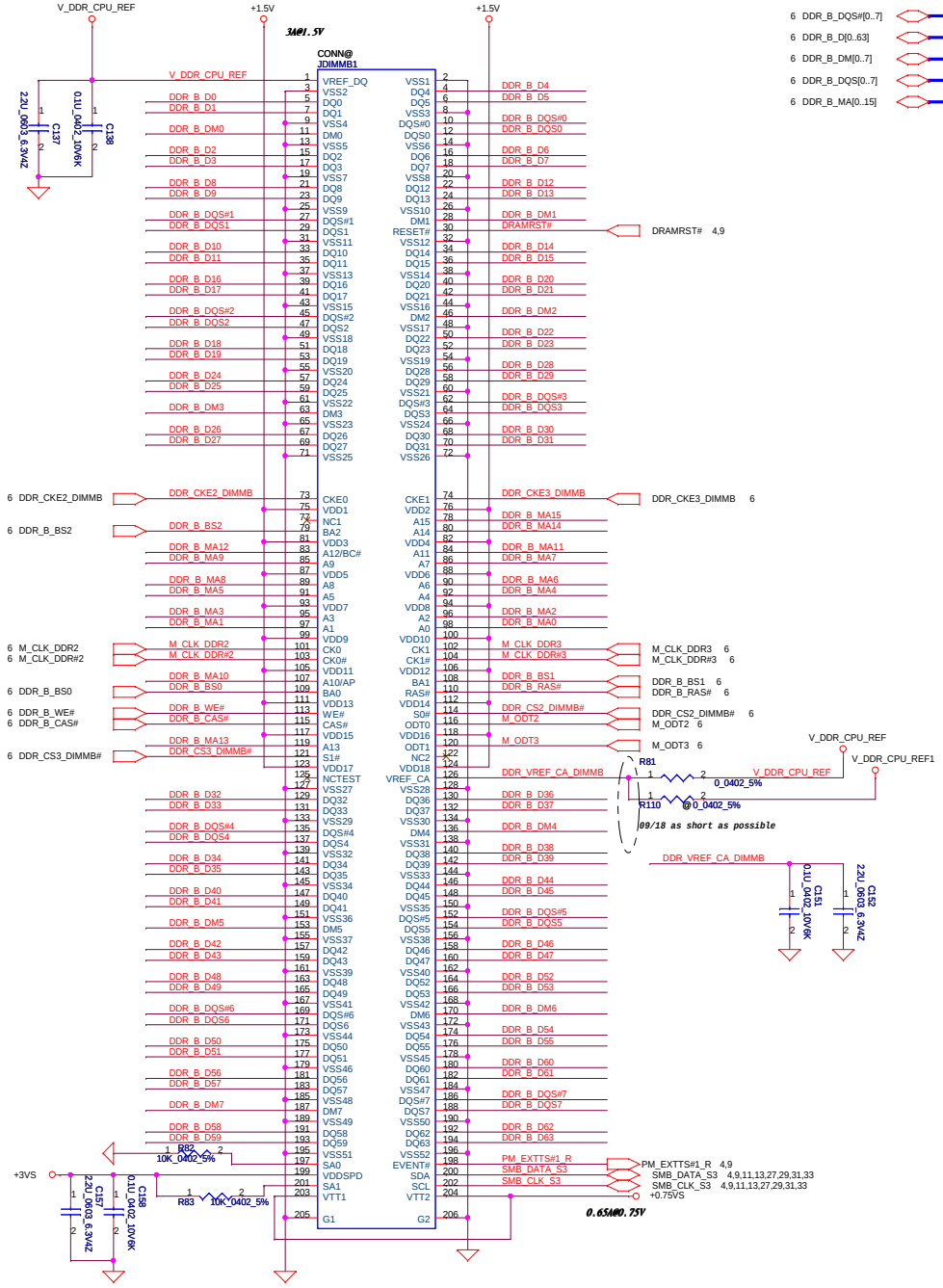
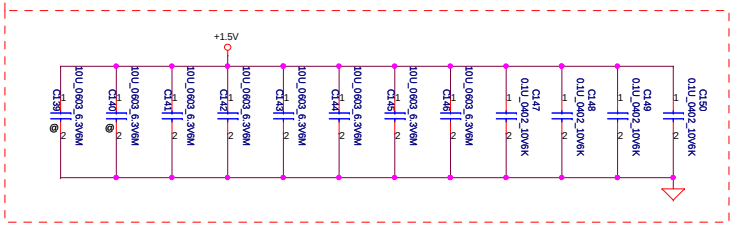
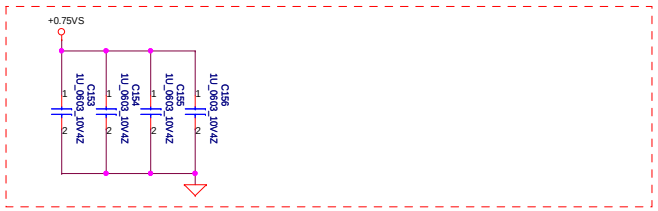


6 DDR_B_DQS#[0..7]
6 DDR_B_D[0..63]
6 DDR_B_DM[0..7]
6 DDR_B_DQS[0..7]
6 DDR_B_MA[0..15]

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



BOT SLOT

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Title: **DDRIII-SODIMM SLOT2**

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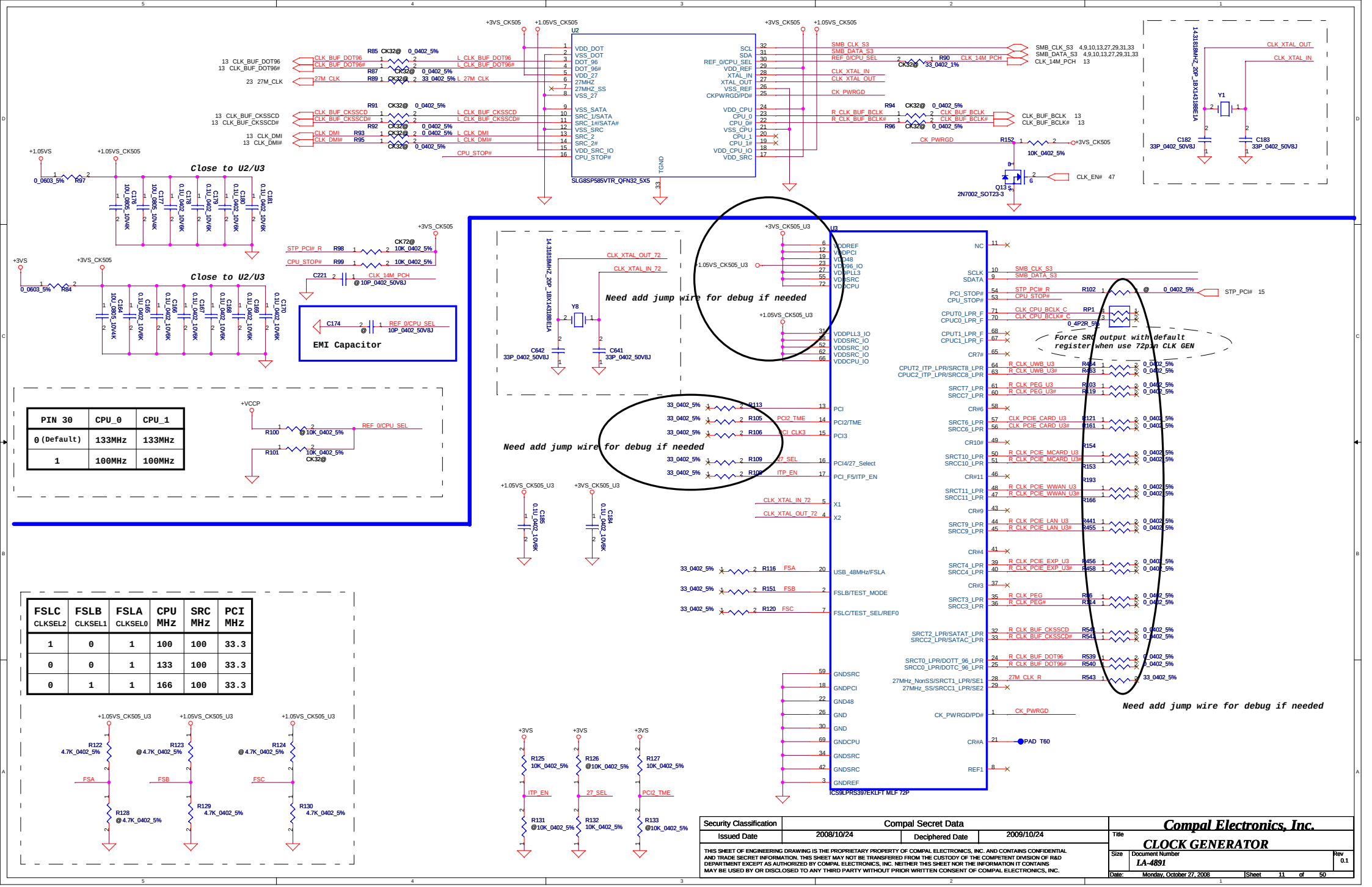

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3

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Compal Electronics, Inc.

Title: **CLOCK GENERATOR**

Size | Document Number: LA-4891 | Rev: 0.1

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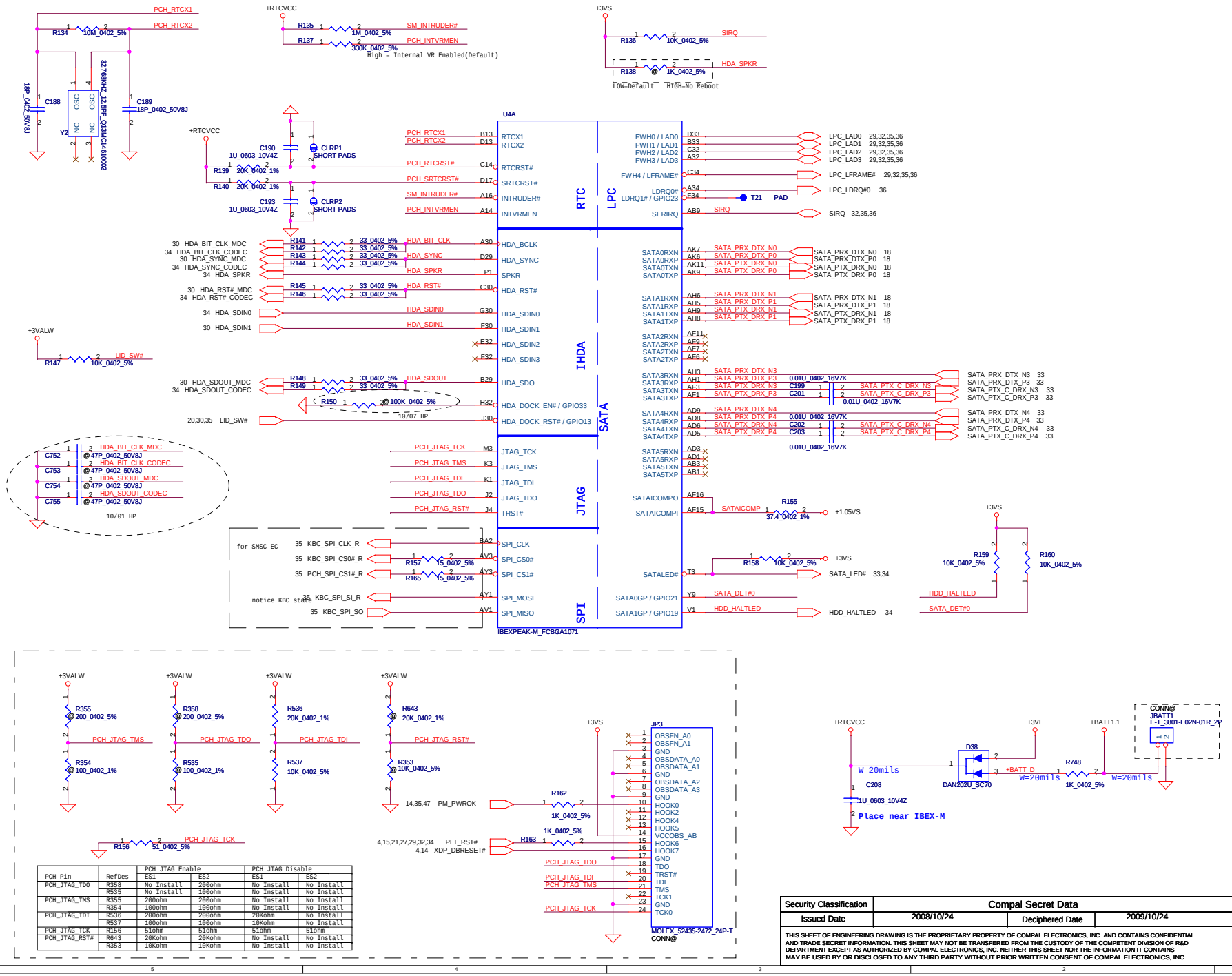

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable ES1	PCH JTAG Disable ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

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Title: **IBEX-M(1/6)-HDA/JTAG/SATA**

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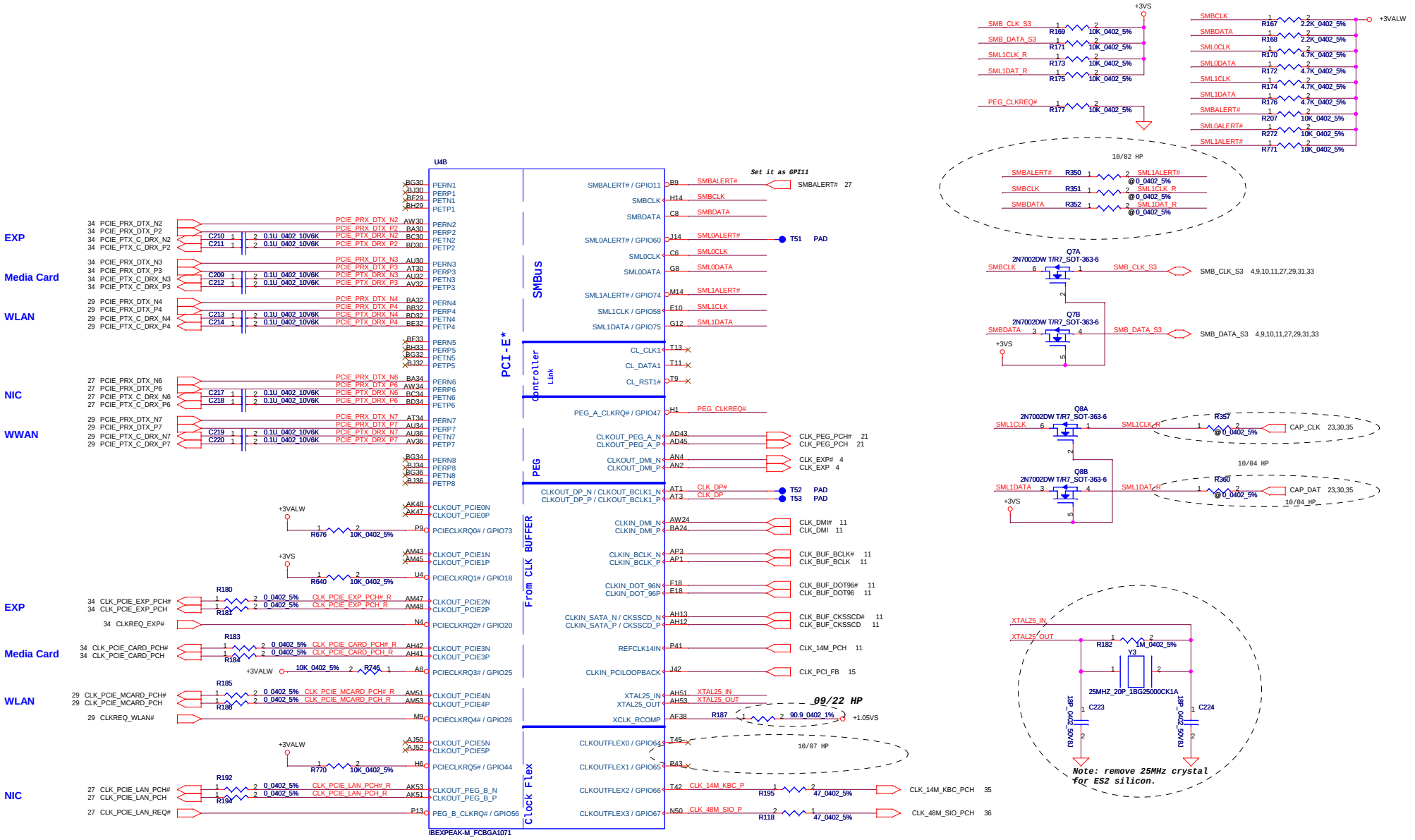

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Title: **IBEX-M(2/6)-PCI-E/SMBUS/CLK**

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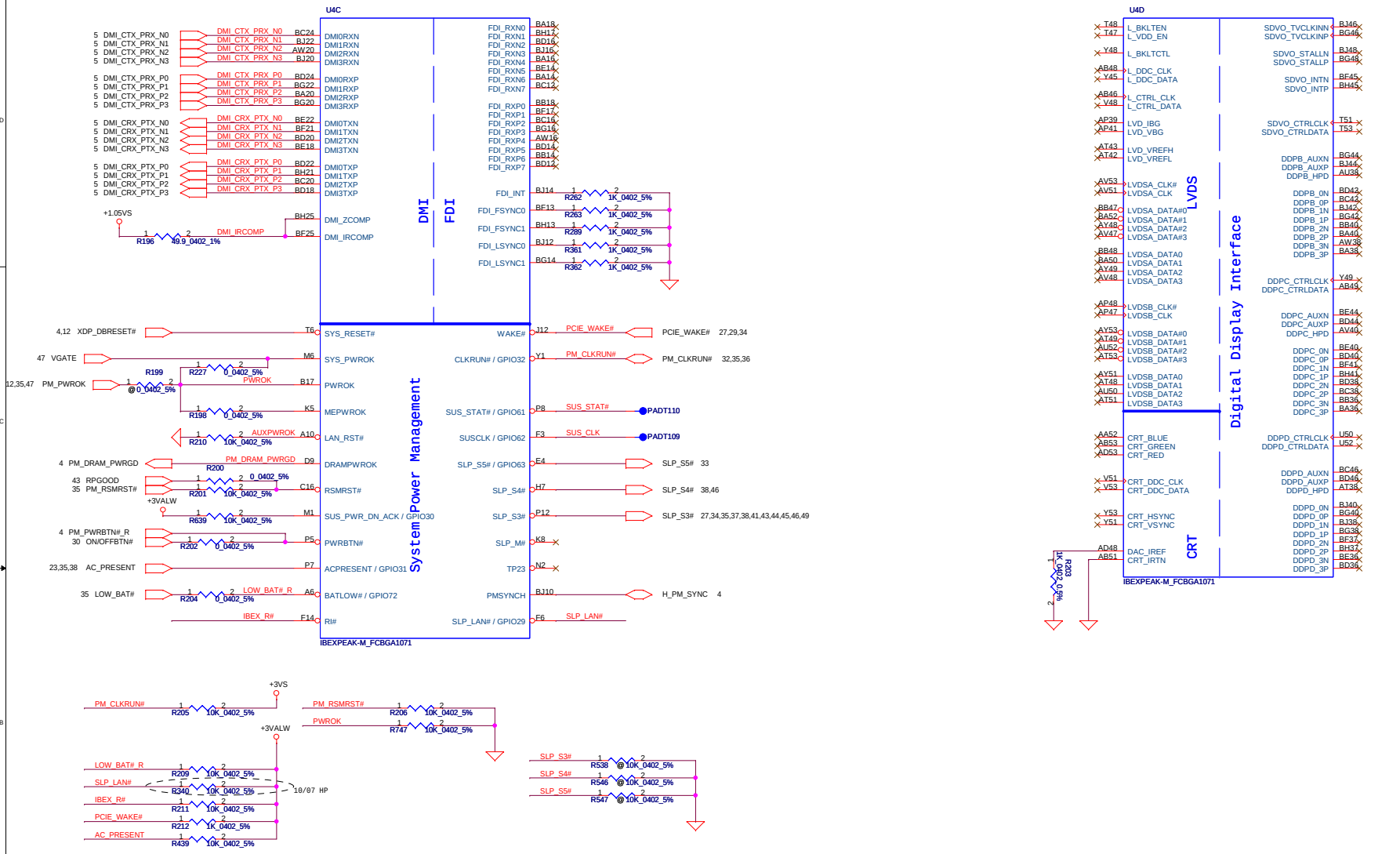

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Title: **IBEX-M(3/6)-DMI/GPIO/LVDS**

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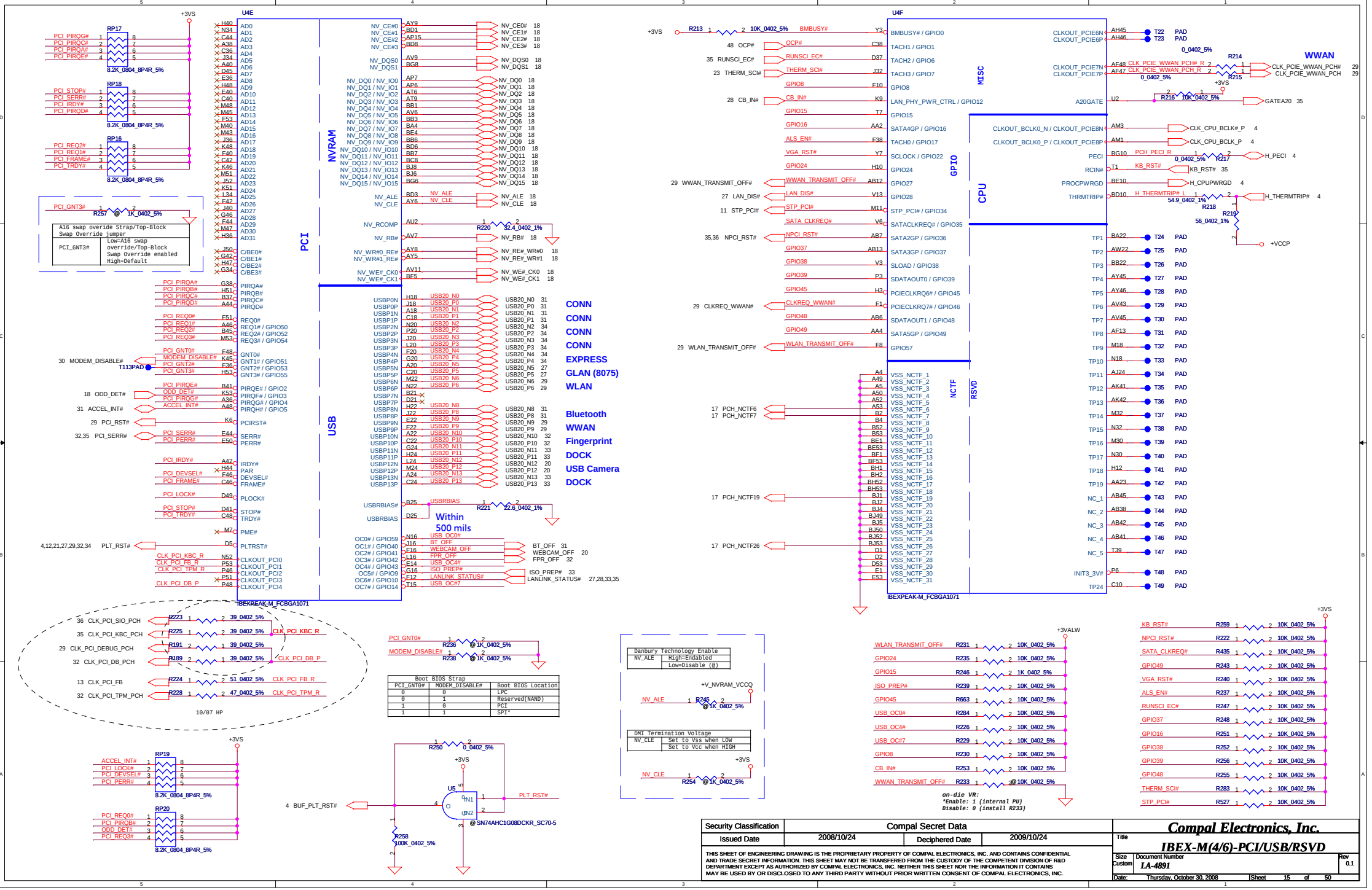
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NVRAM
USB
IBEXPEAK-M_FCBGA1071
U4F
MISC
GPIO
CPU
NCTF
RSVD
WWAN
CONN
CONN
CONN
CONN
EXPRESS
GLAN (8075)
WLAN
Bluetooth
WWAN
Fingerprint
DOCK
USB Camera
DOCK
Within 500 mils
A16 swap overide Strap/Top-Block Swap Override jumper
PCI_GNT3# Low=A16 swap override/Top-Block Swap Override enabled High=Default
Boot BIOS Strap
PCI_GNT0# MODEM_DISABLE# Boot BIOS Location
0 0 LPC
0 1 Reserved(NAND)
1 0 PCI
1 1 SPI*
Danbury Technology Enable
NV_ALE High=Endabled Low=Disable (@)
DMI Termination Voltage
NV_CLE Set to Vss when LOW Set to Vcc when HIGH
on-die VR:
*Enable: 1 (internal PU)
Disable: 0 (install R233)
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IBEX-M(4/6)-PCI/USB/RSVD
Size Custom
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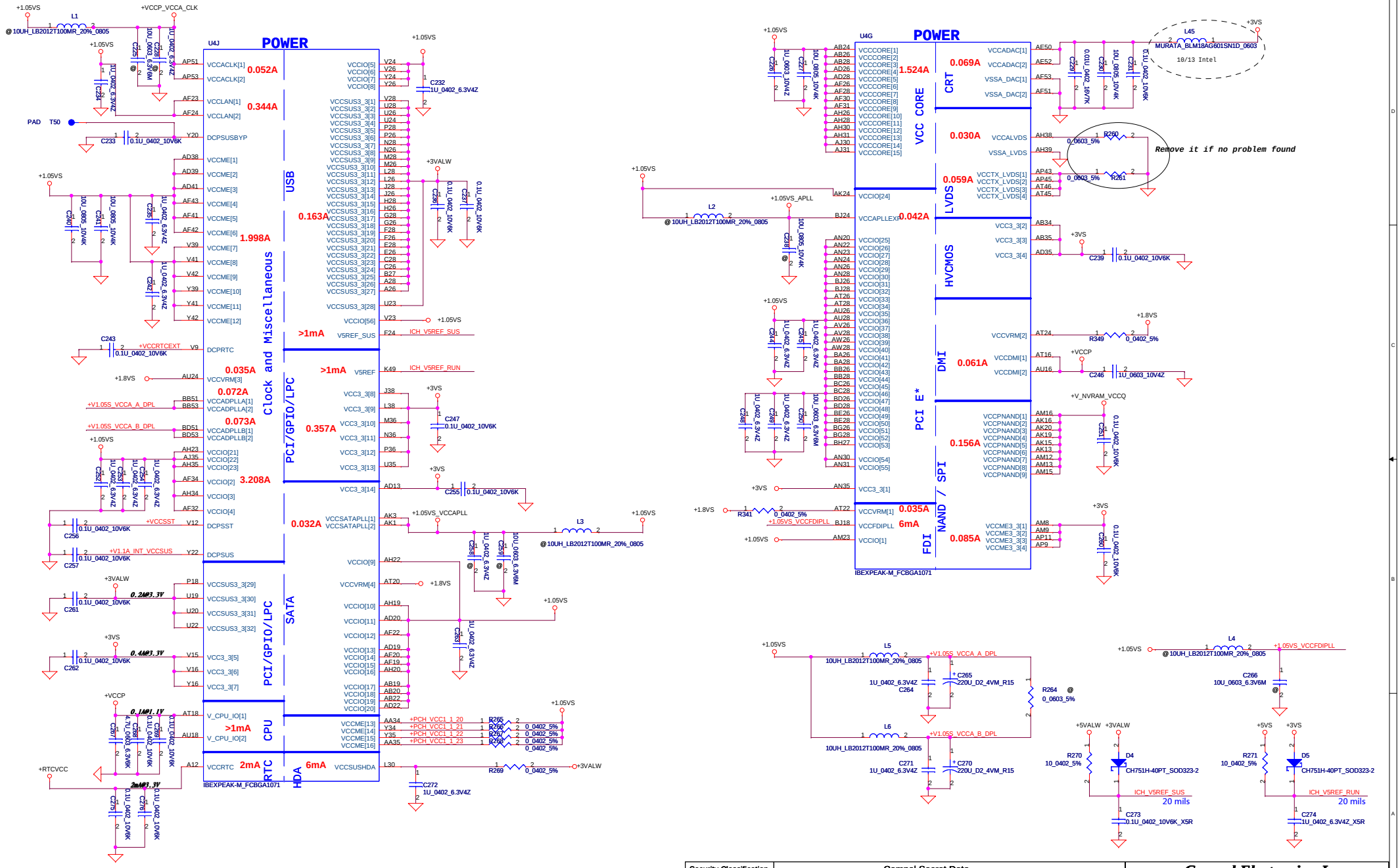

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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **IBEX-M(5/6)-PWR**

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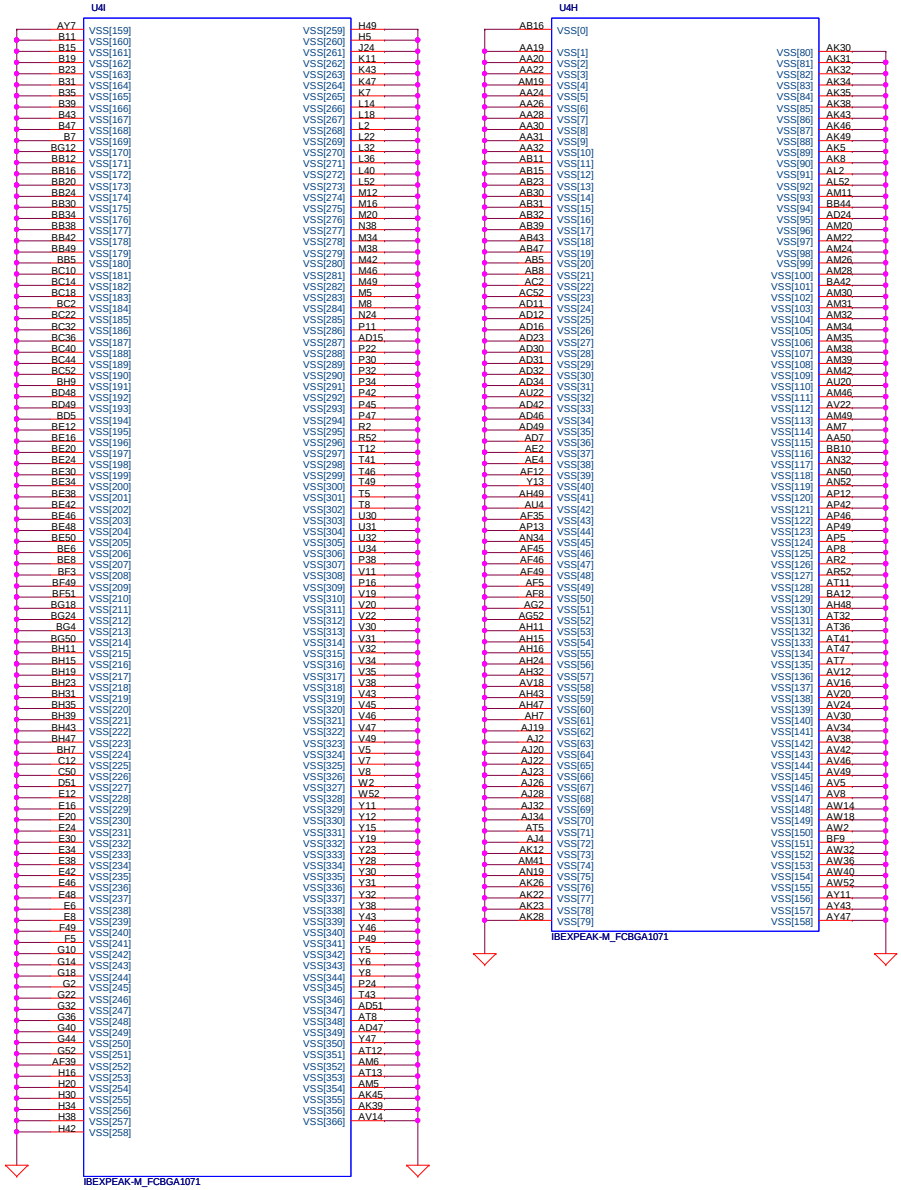
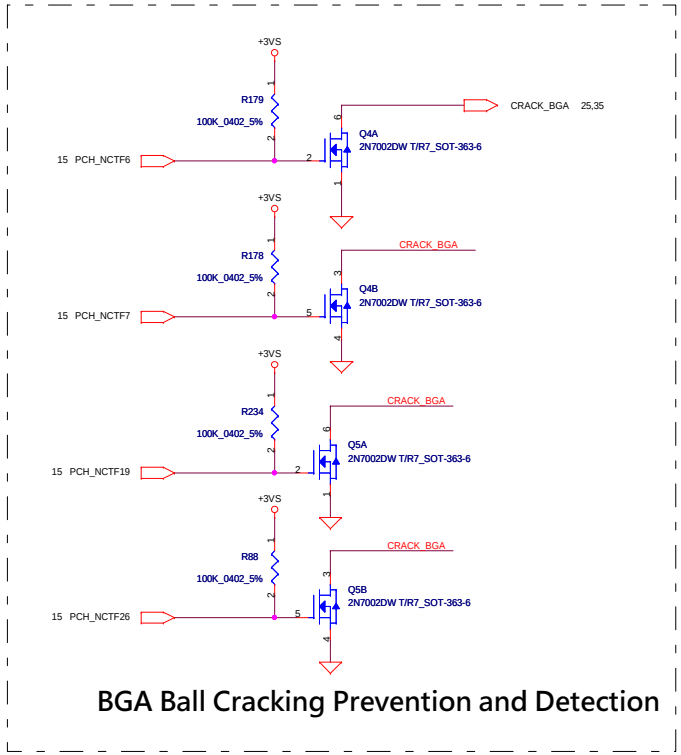
Date: Monday, October 27, 2008 | Sheet 16 of 50





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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **IBEX-M(6/6)-GND**

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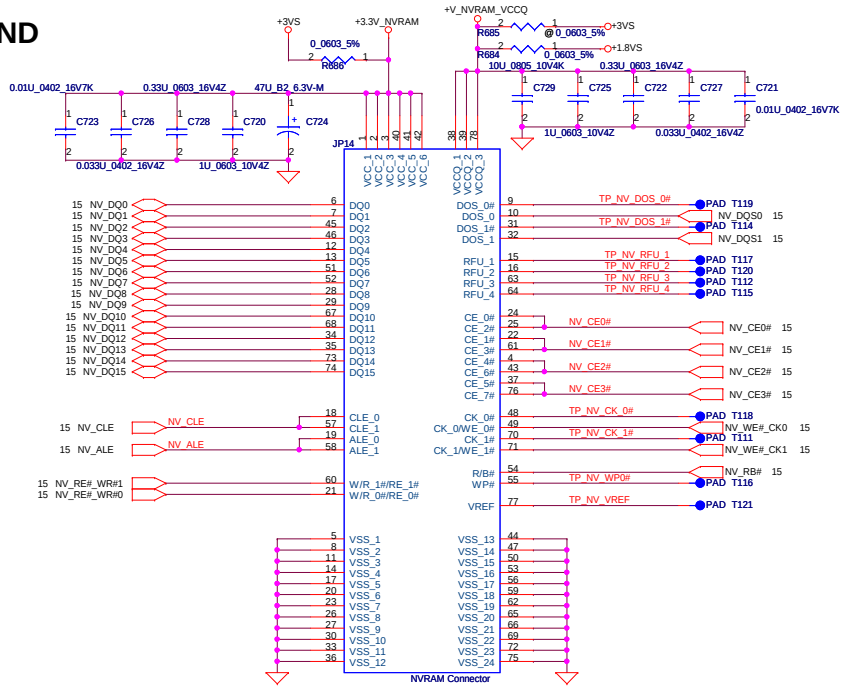
NAND



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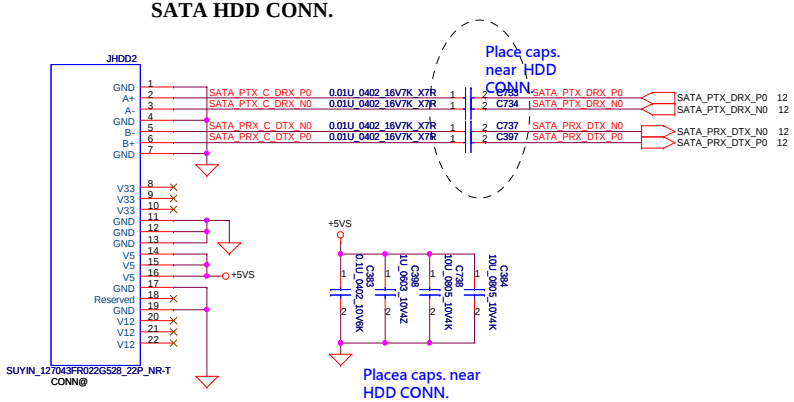

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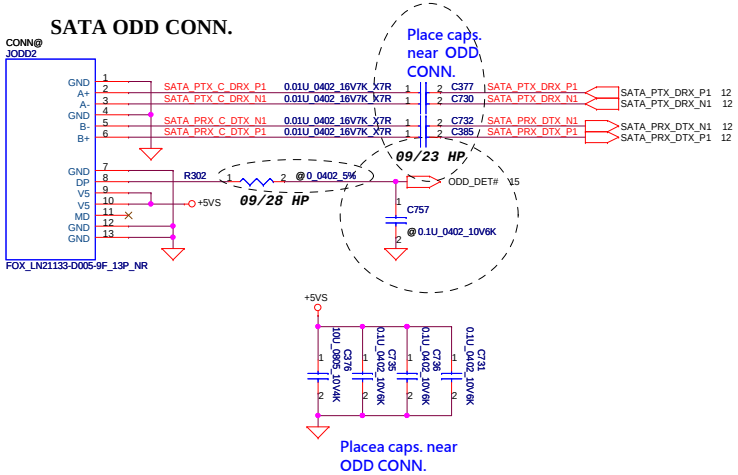

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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **IBEX-M(1/6)-HDA/JTAG/SATA**

Size: Custom | Document Number: LA-4891 | Rev: 0.1

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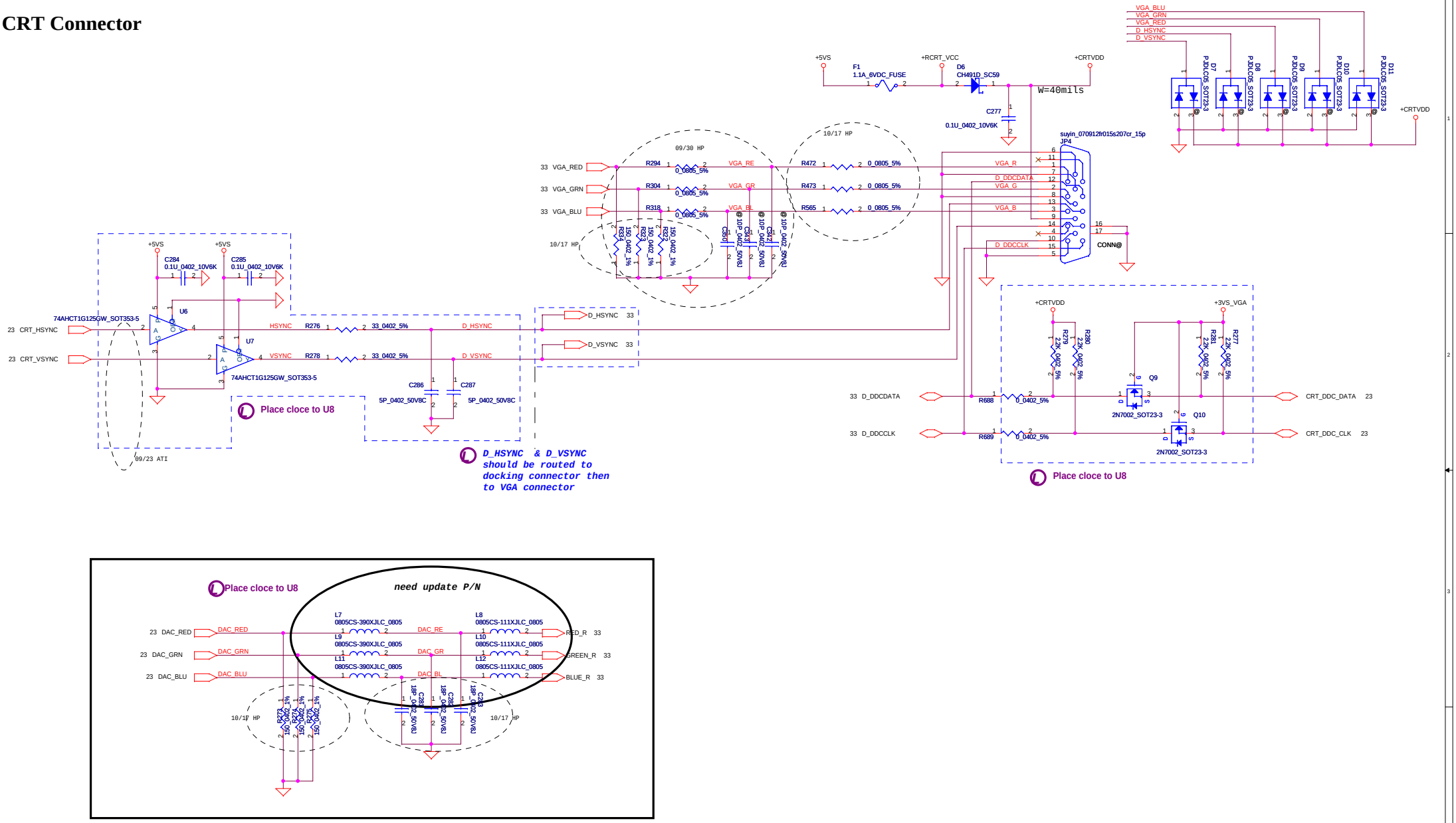
CRT Connector



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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **CRT Connector**

Size	Document Number	Rev
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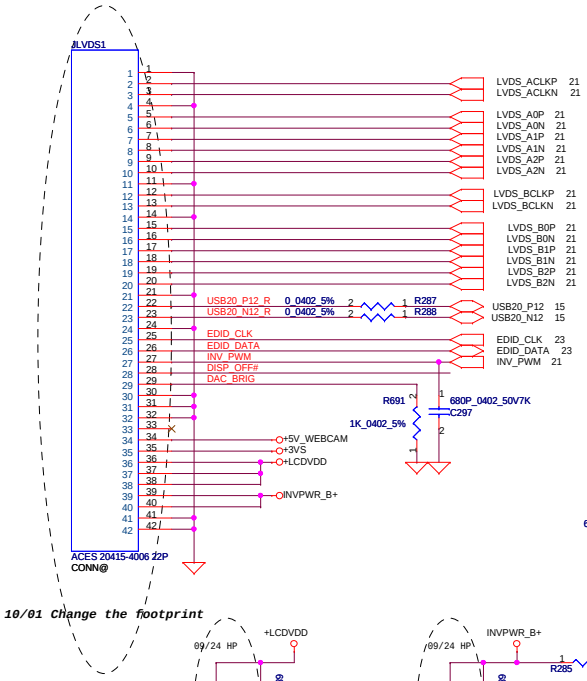
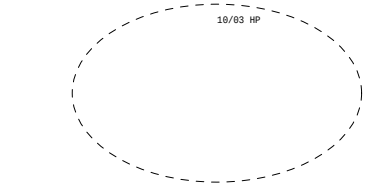
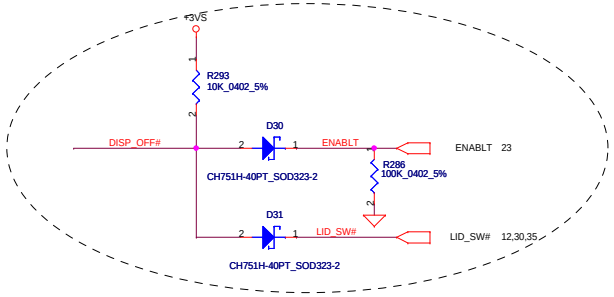
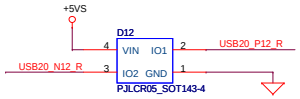
LCD/PANEL BD. CONN.

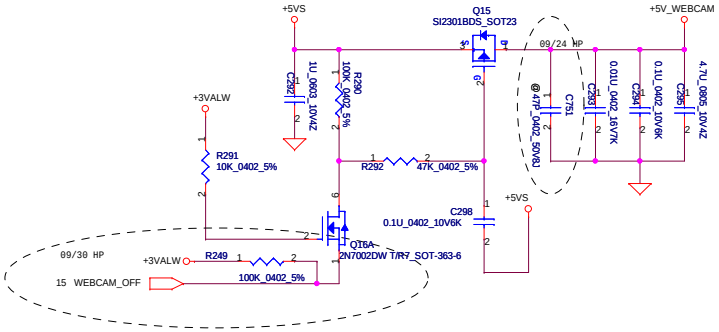


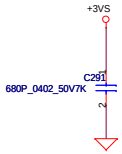
10/01 Change the footprint

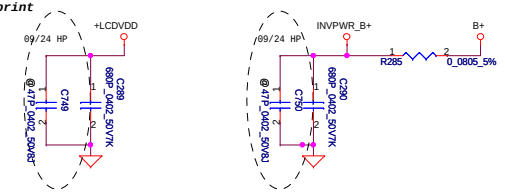




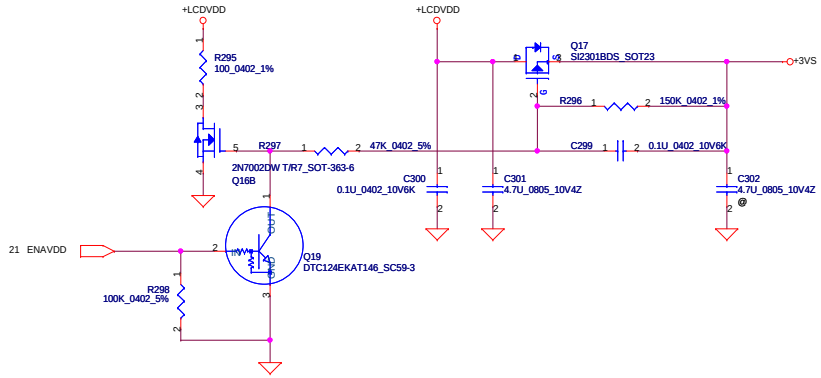








LCD POWER CIRCUIT



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Compal Electronics, Inc.

Title: **LCD CONN & Q-Switch & GPIO Ext.**

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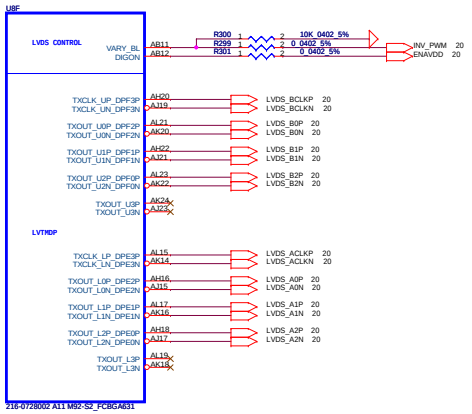
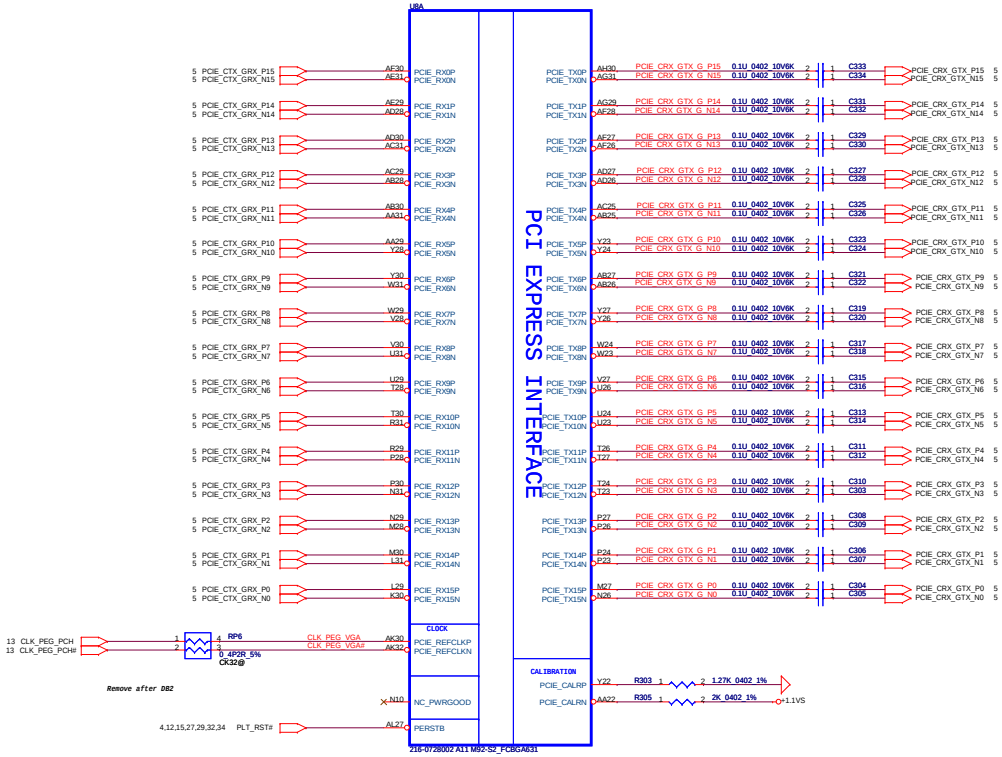
PEG Interface

LVDS Interface





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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: PEG & LVDS

Size: Custom | Document Number: LA-4891 | Rev: 0.1

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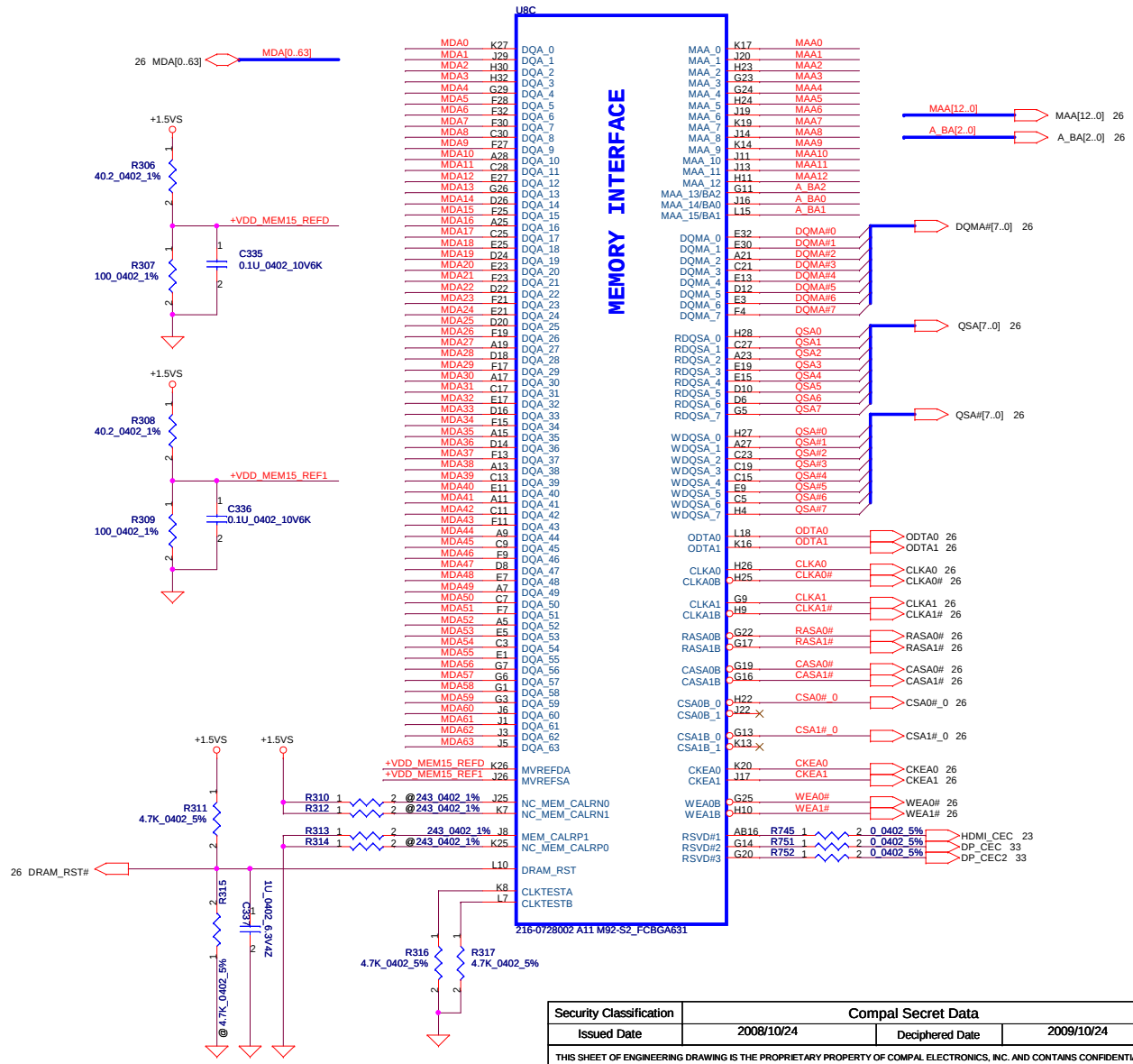

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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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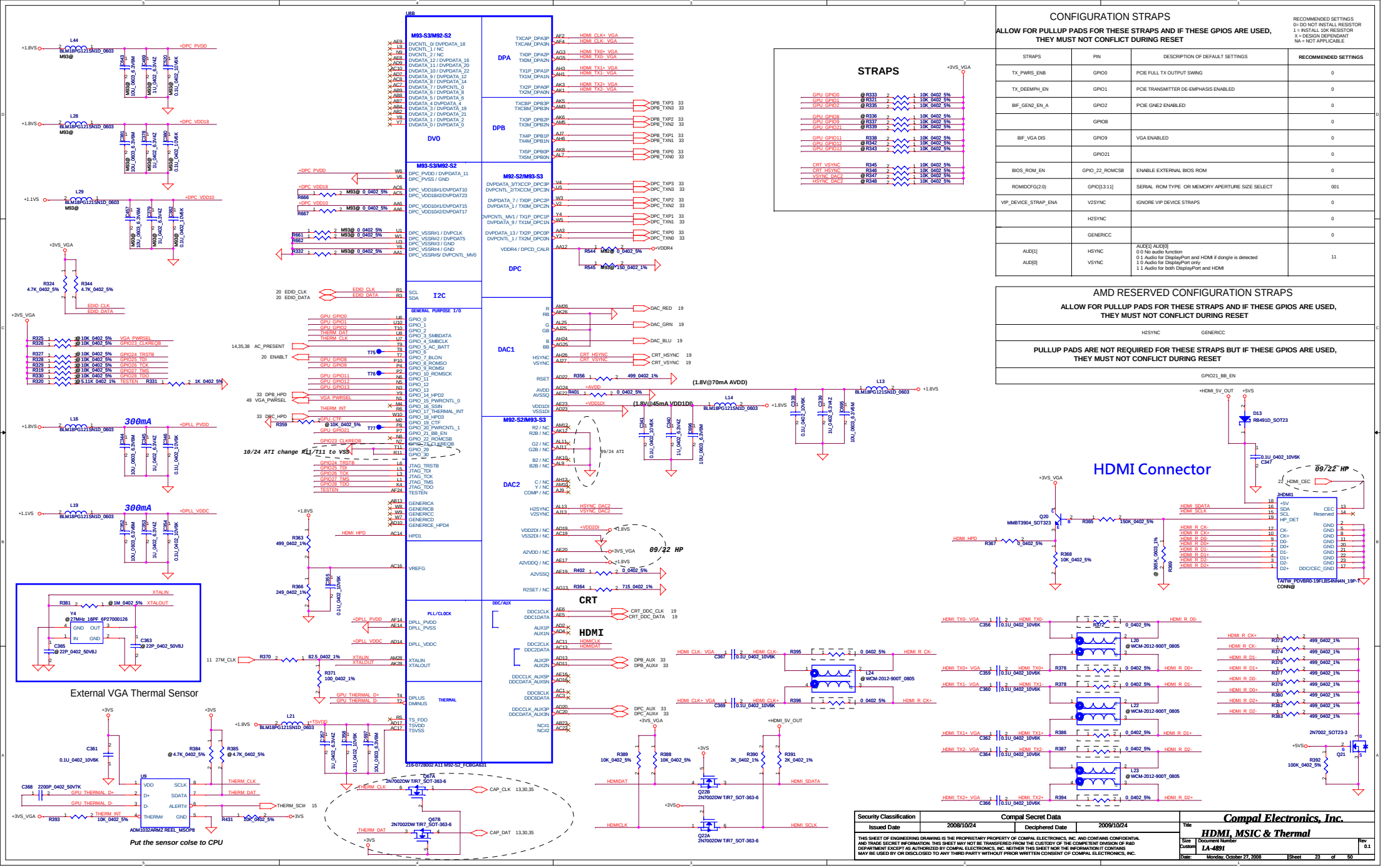
Compal Electronics, Inc.

Title: **Memory Interface**

Size: Custom | Document Number: LA-4891 | Rev: 0.1

Date: Monday, October 27, 2008 | Sheet 22 of 50



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
	GPIO8		0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **HDMI, MSIC & Thermal**

Size: Custom | Document Number: LA-4891 | Rev: 0.1

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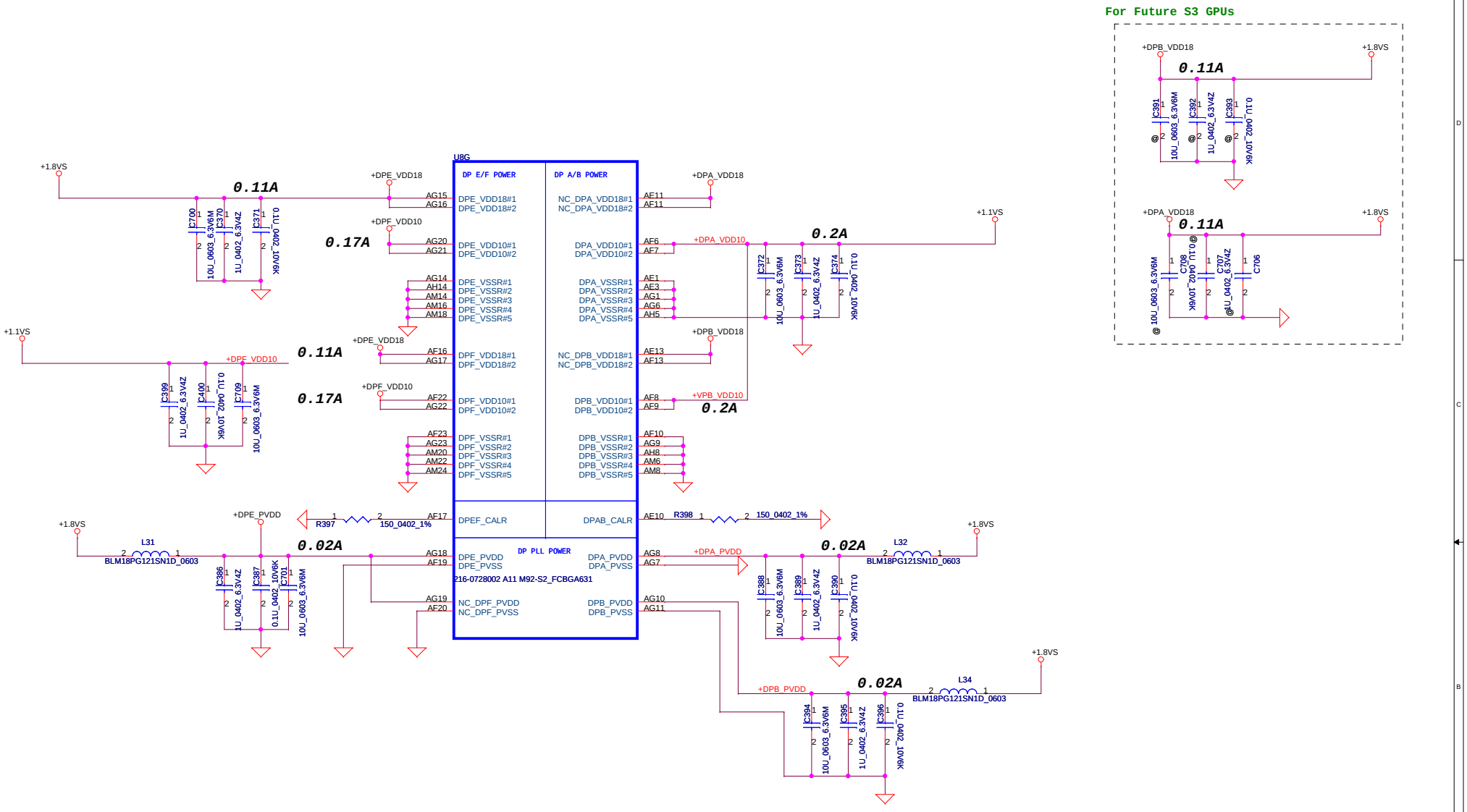

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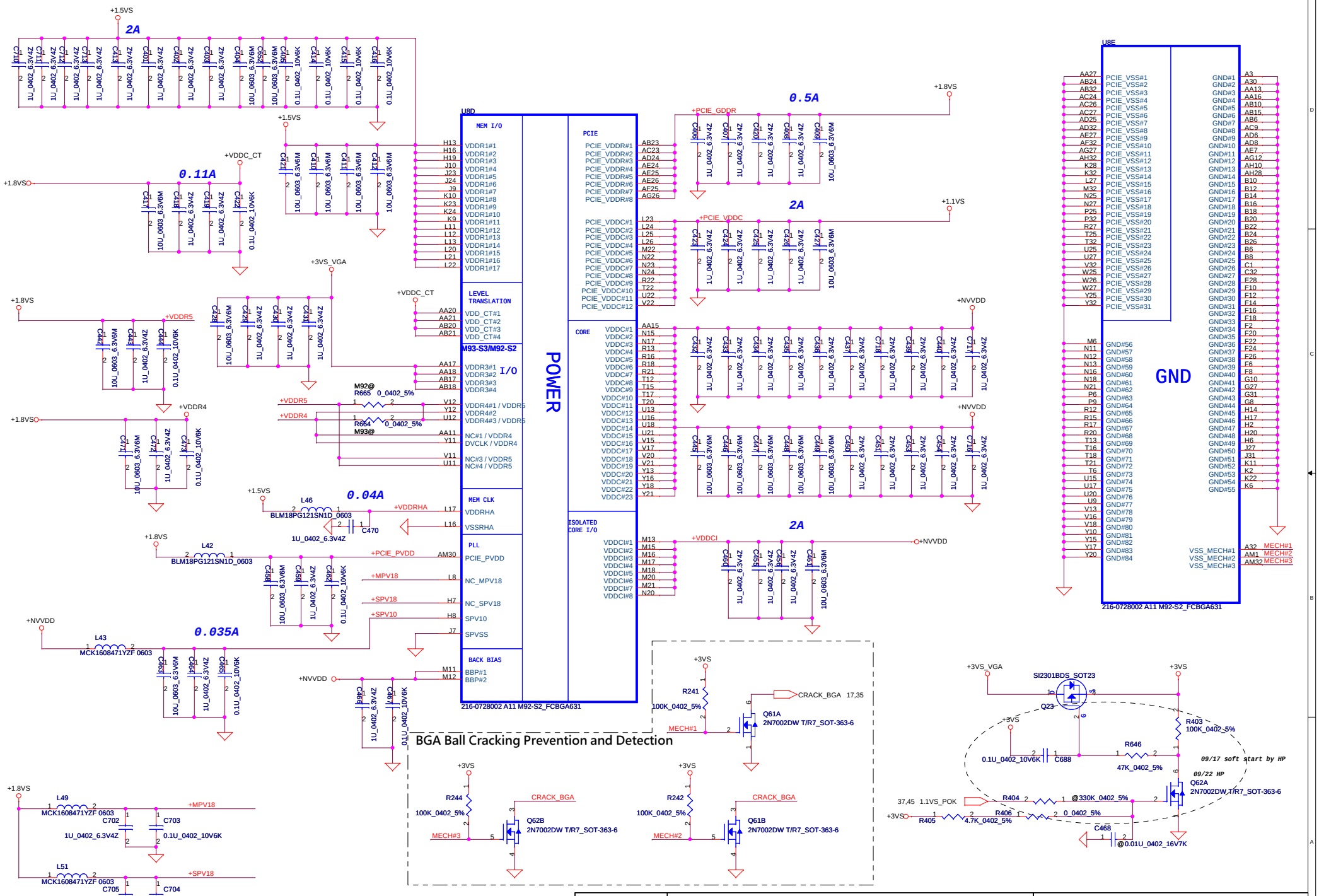
Compal Electronics, Inc.

Title: **DPX POWER**

Size: Custom | Document Number: LA-4891 | Rev: 0.1

Date: Monday, October 27, 2008 | Sheet 24 of 50



Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **Main Power**

Size	Document Number	Rev
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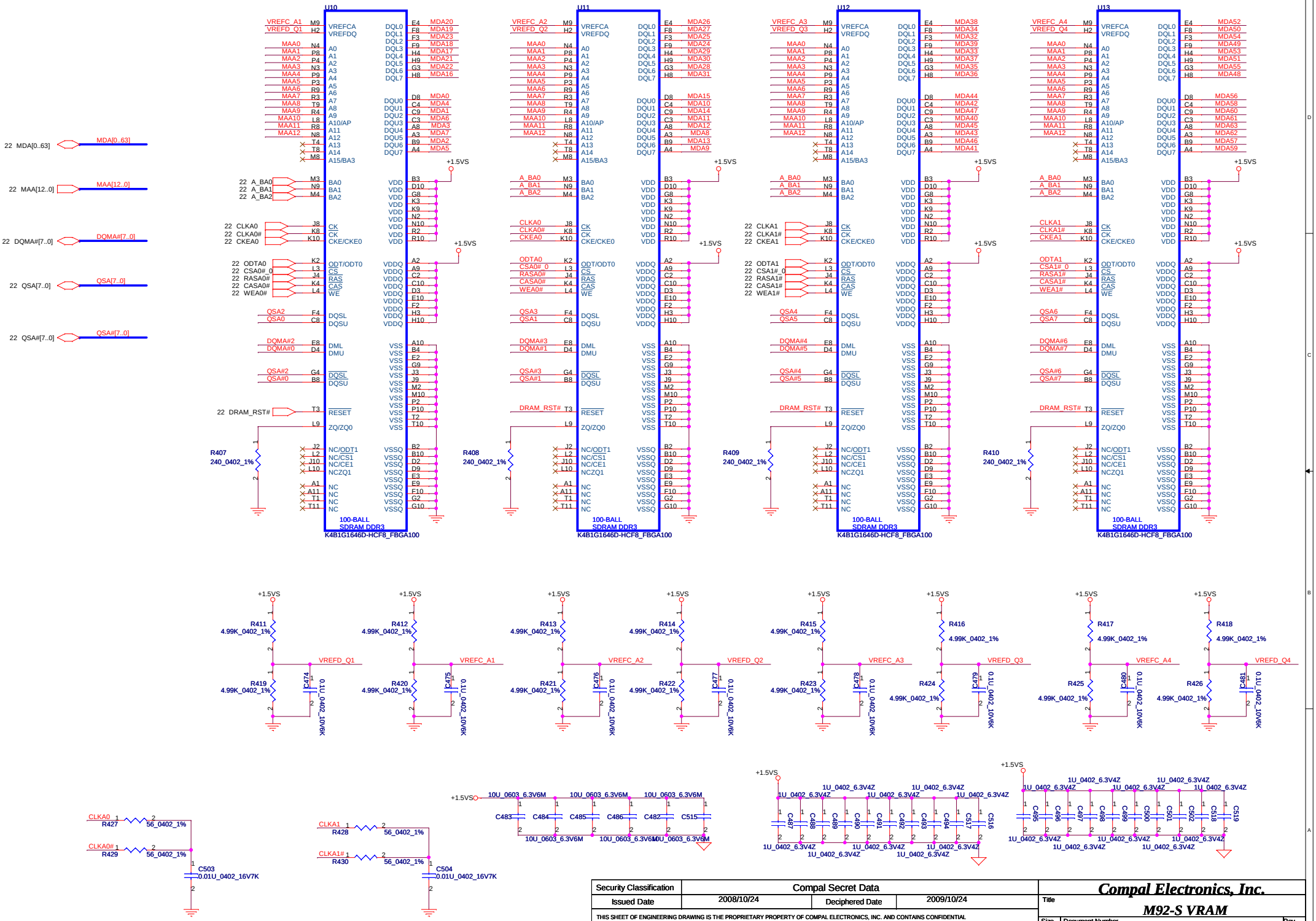

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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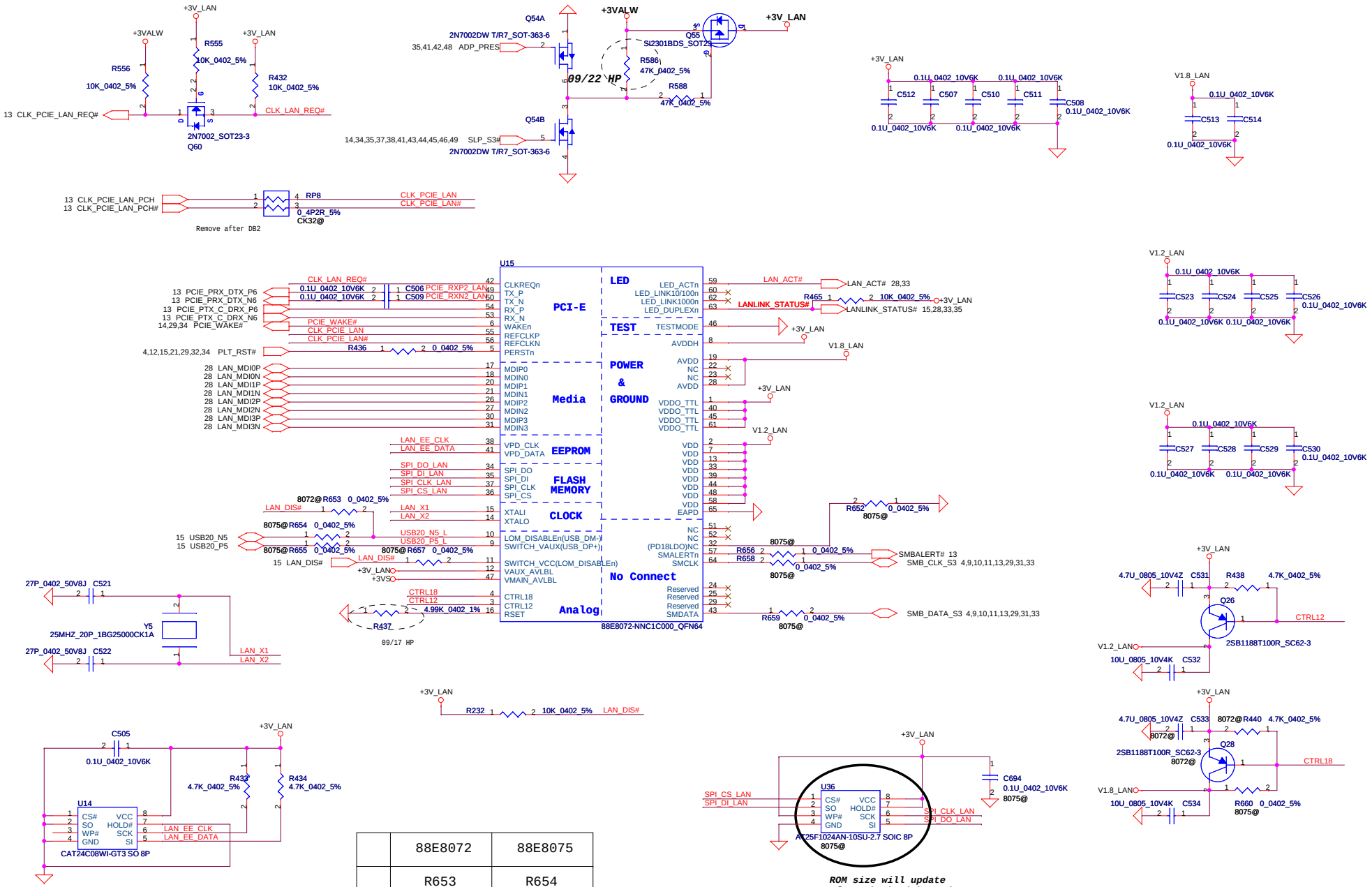
Compal Electronics, Inc.

Title: **M92-S VRAM**

Size | Document Number: *LA-4891* | Rev: 0.1

Date: Monday, October 27, 2008 | Sheet 26 of 50



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Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title

Size	Document Number	Rev
		0.1

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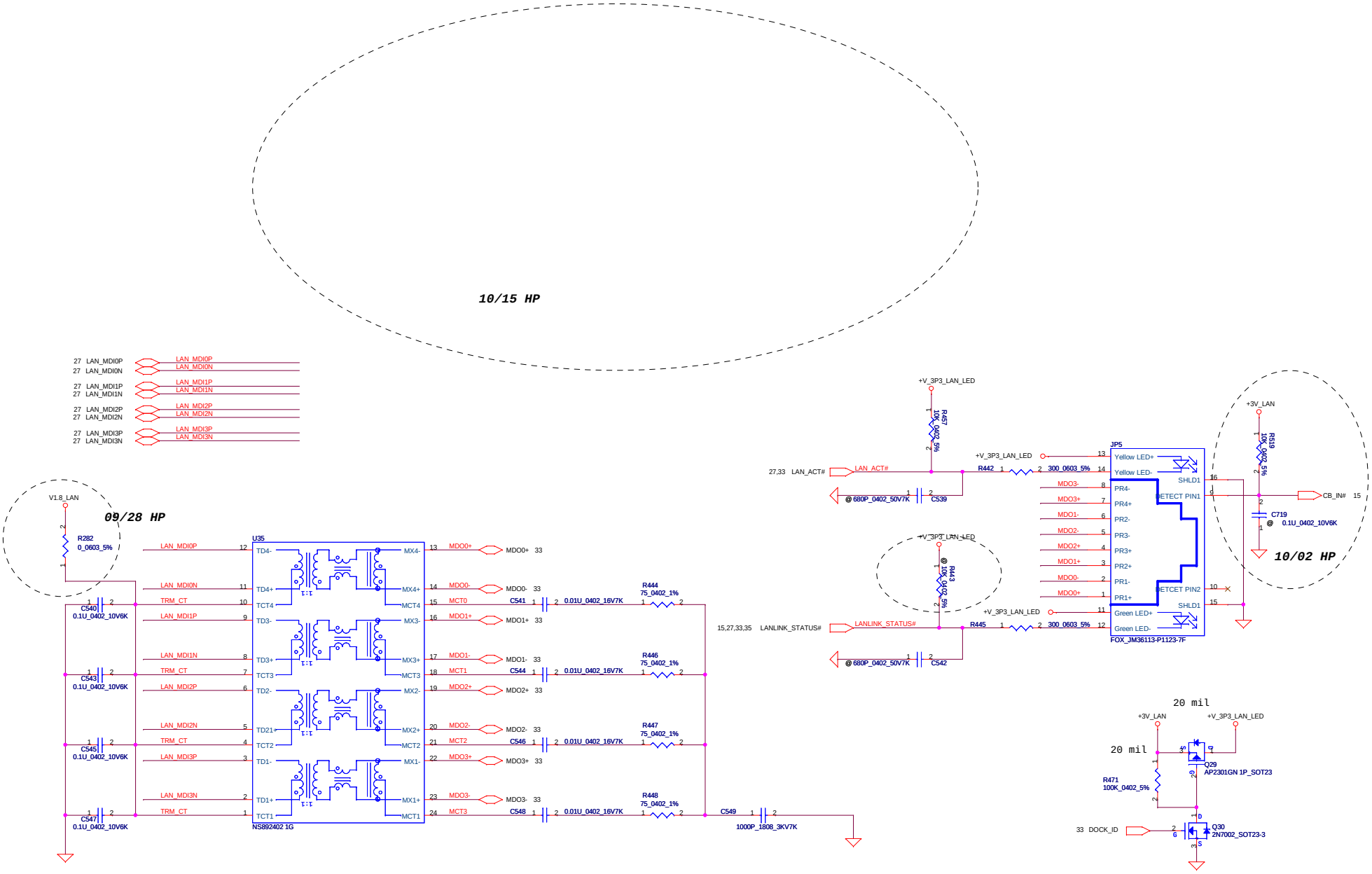

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Compal Electronics, Inc.

Title: **Magnetic & RJ45**

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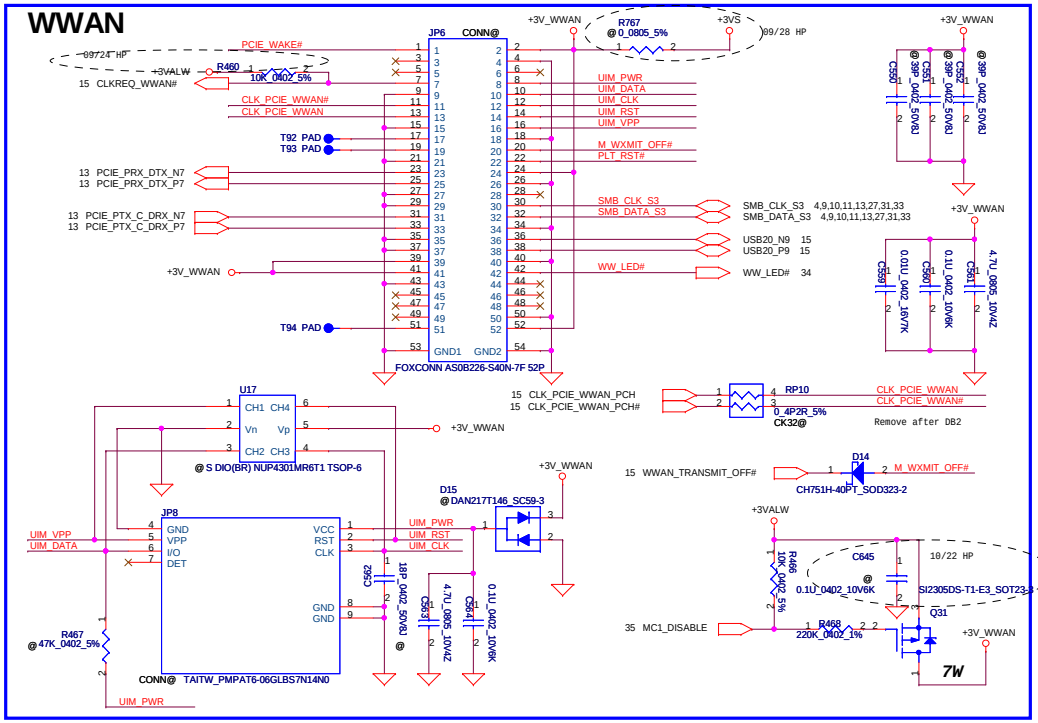

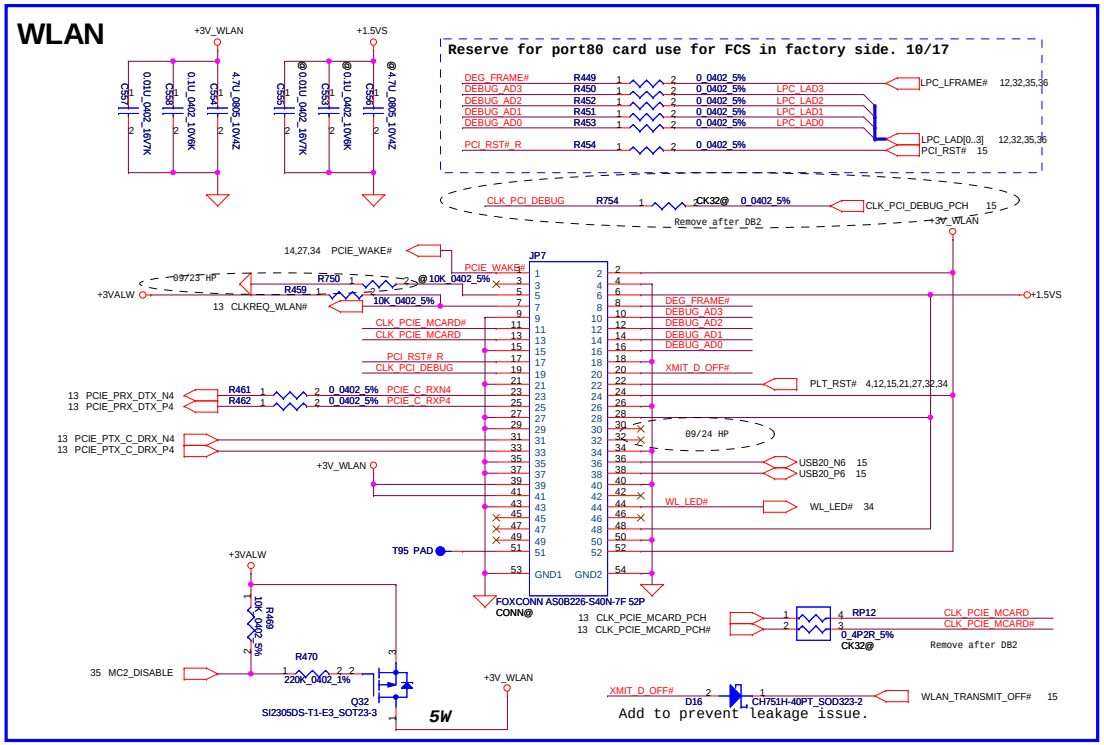

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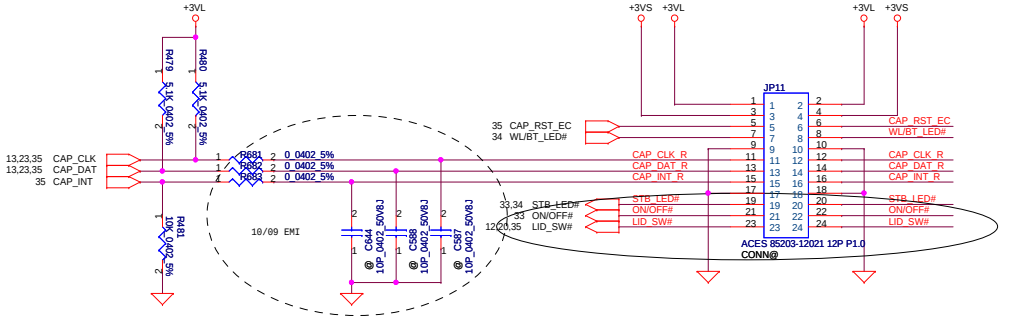
Compal Electronics, Inc.

Title: **WWAN/NAND mini**

Size | Document Number: LA-4891 | Rev: 0.1

Date: Wednesday, October 29, 2008 | Sheet 29 of 50

CAP SWITCH BOARD.



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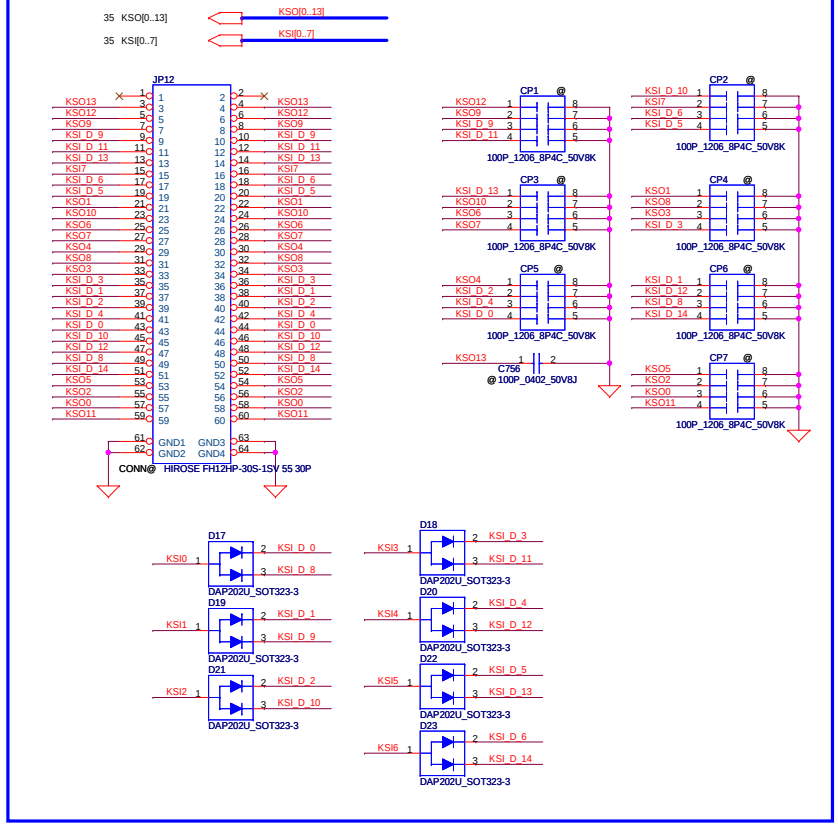
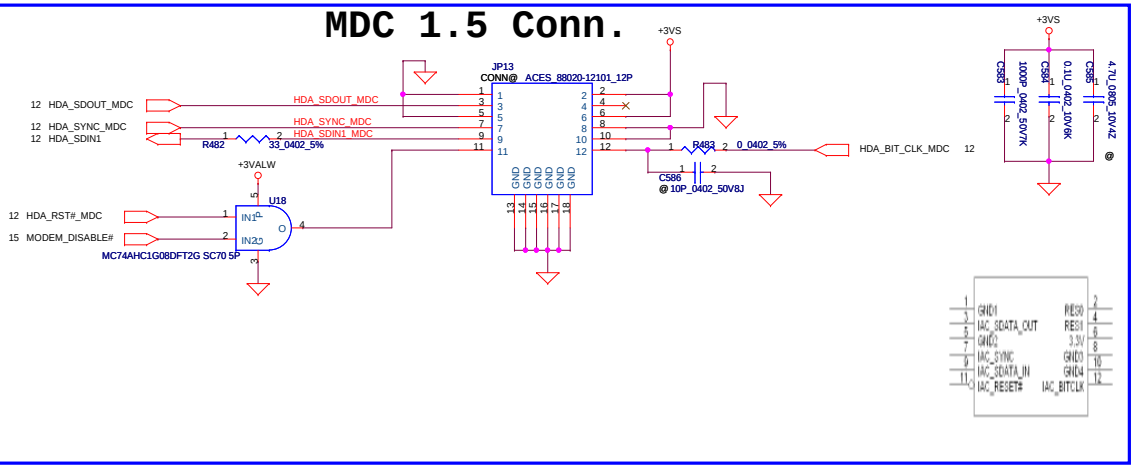
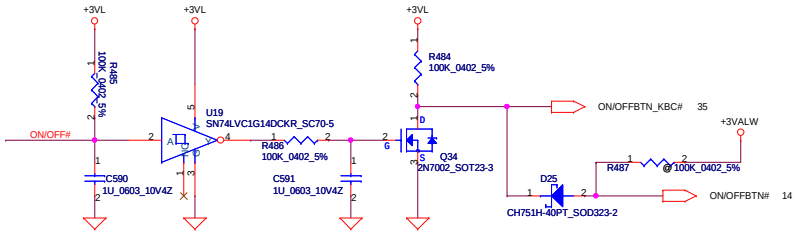


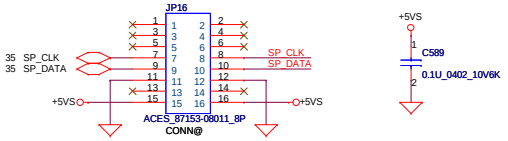
MDC 1.5 Conn.



Power button



TrackPoint CONN.



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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: MDC/KBD/ON_OFF/LID

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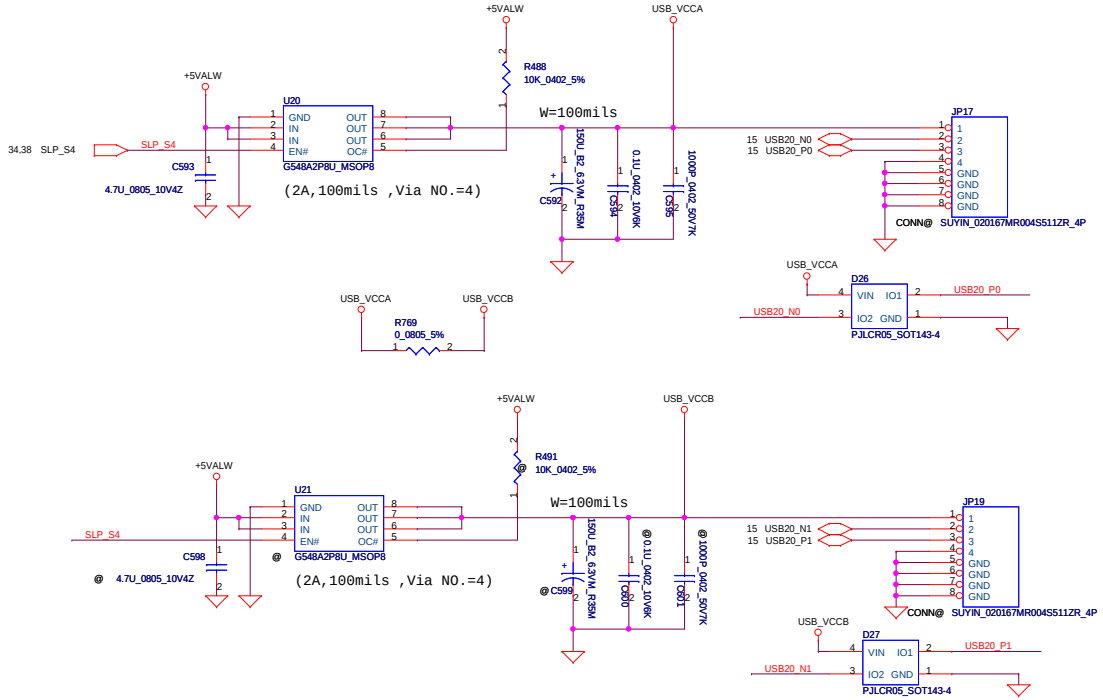
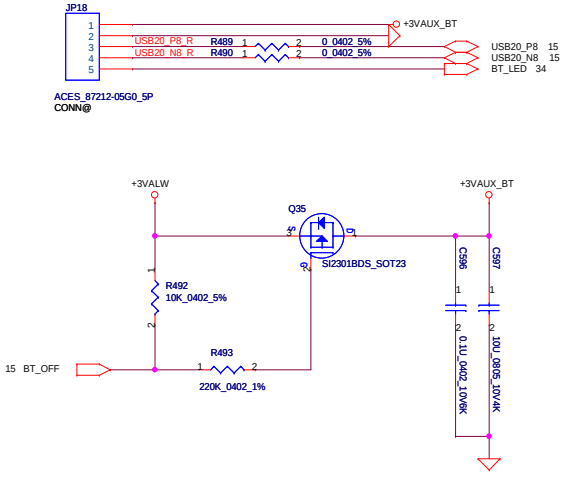
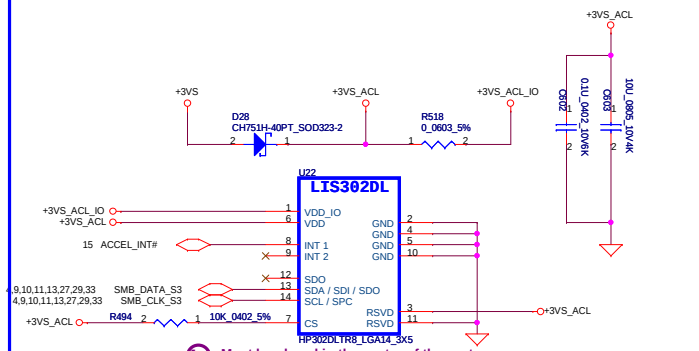


BT Connector



ACCELEROMETER



Must be placed in the center of the system.

Change U22 part description from
LIS302DLTR LGA to HP302DLTR8 as HP
change list. 12/03

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **USB & BT Connector & Acclerometer**

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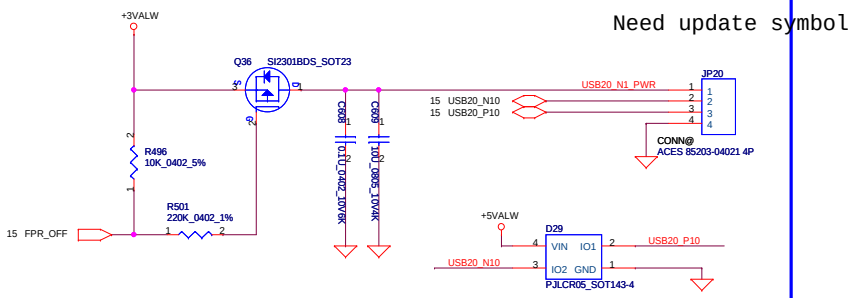
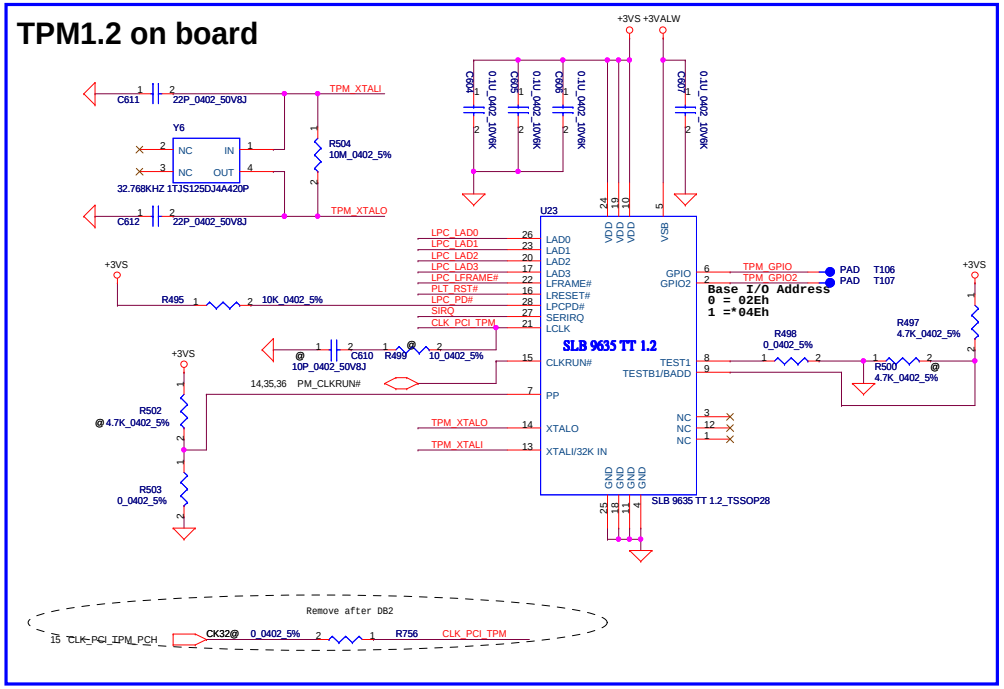
Finger printer

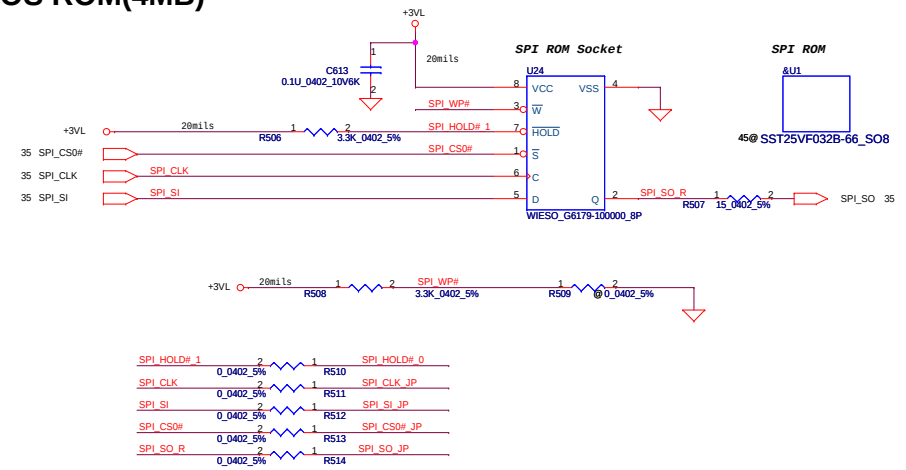
Need update symbol



TPM1.2 on board

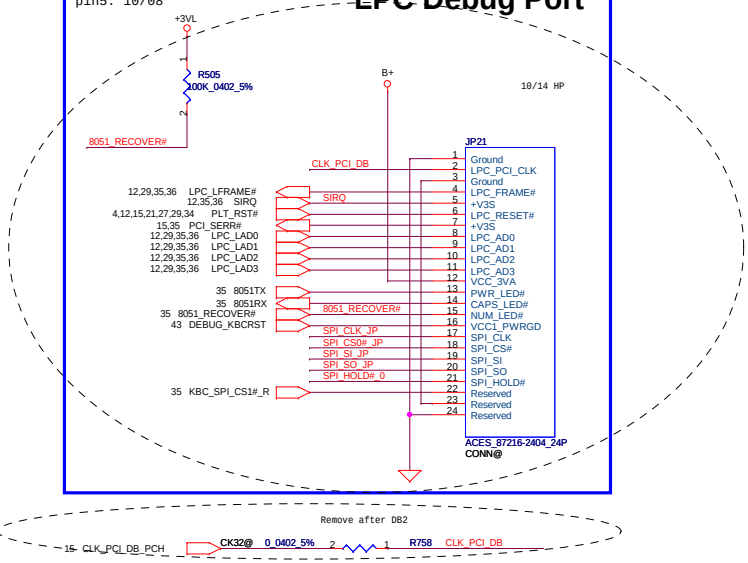


BIOS ROM(4MB)



LPC Debug Port

Add SIRQ and connect to pin5. 10/08



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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: TCG/BIOS ROM/PS2/SW LPC DEBUG

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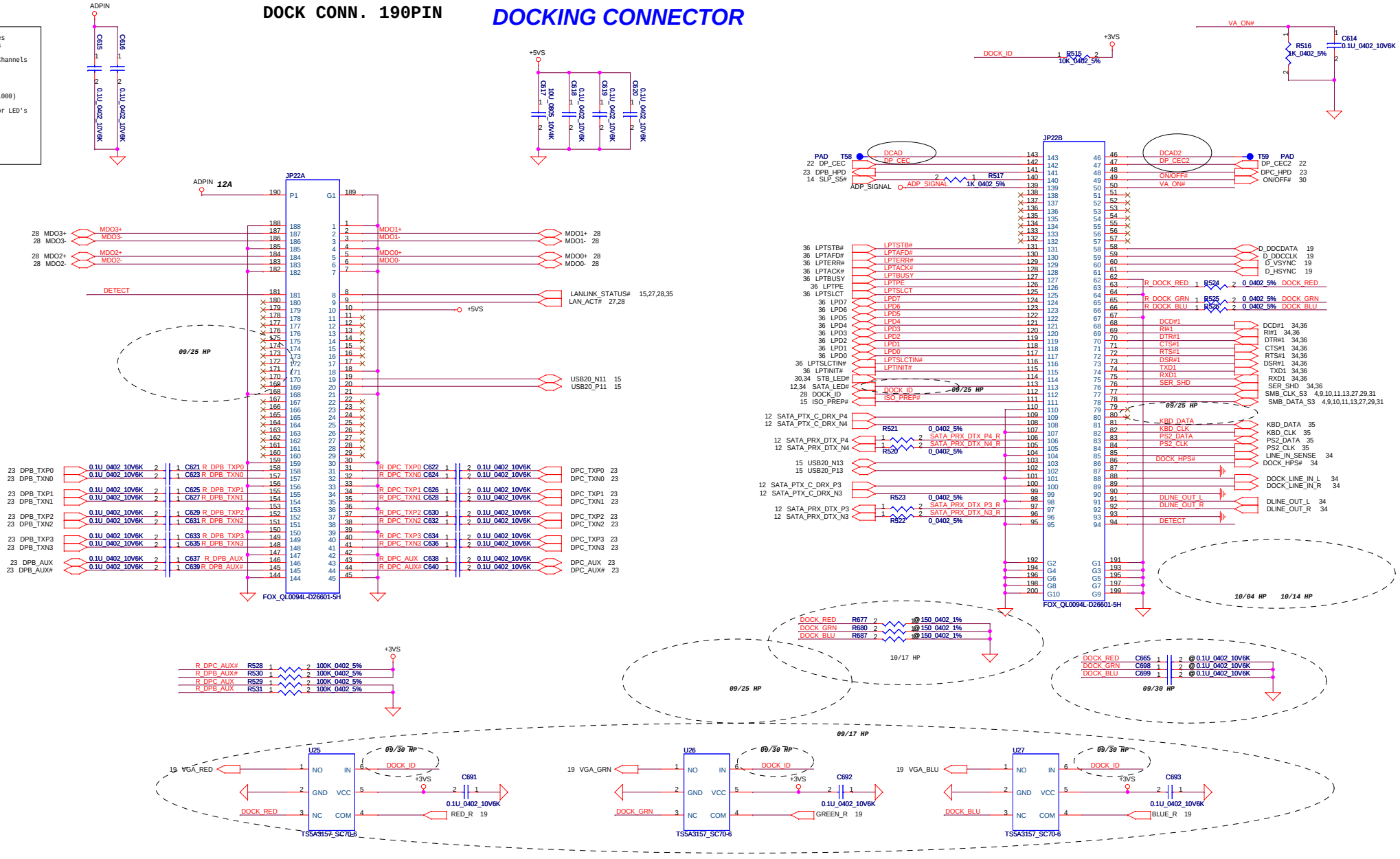
DOCK CONN. 190PIN

DOCKING CONNECTOR

(2) PS/2 Interfaces
(2) USB 2.channels
(2) SATA Channels
(2) Display Port Channels
(1) Serial Port
(1) Parallel Port
(1) Line In
(1) Line Out
(1) RJ45 (10/100/1000)
(1) VGA
(1) 2 LAN indicator LED's
(1) Power Button
(1) I2C interface



IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: DOCK CONN

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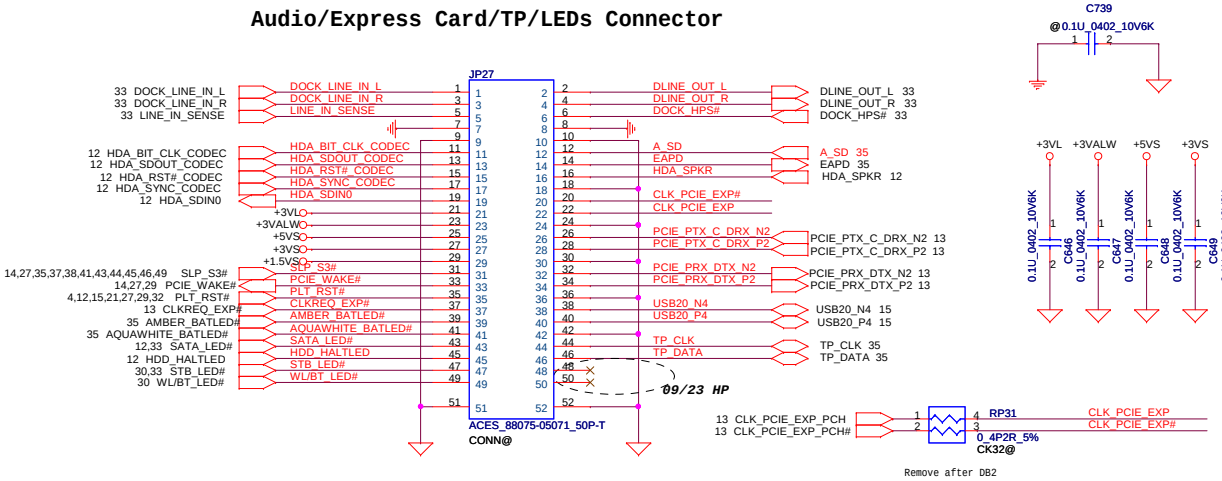
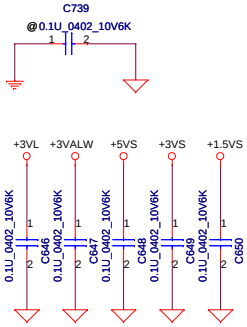
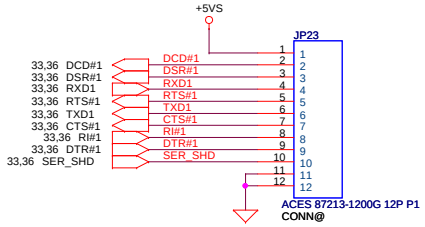
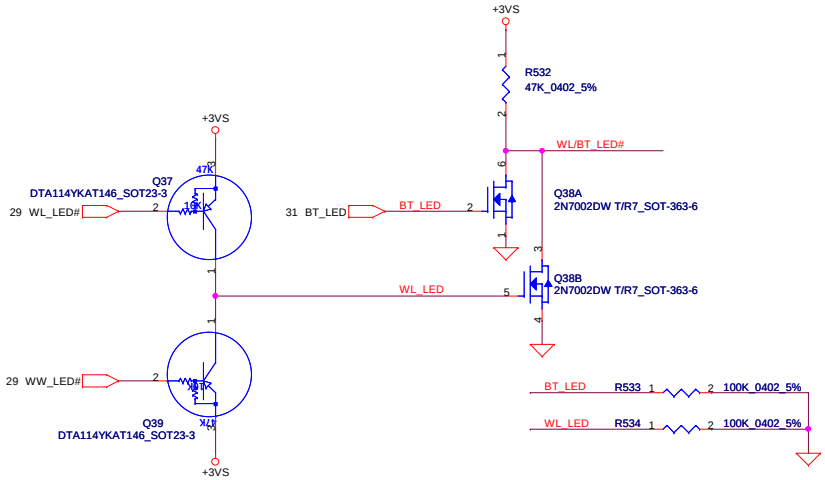
Audio/Express Card/TP/LEDs Connector

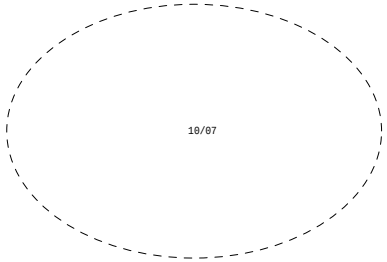




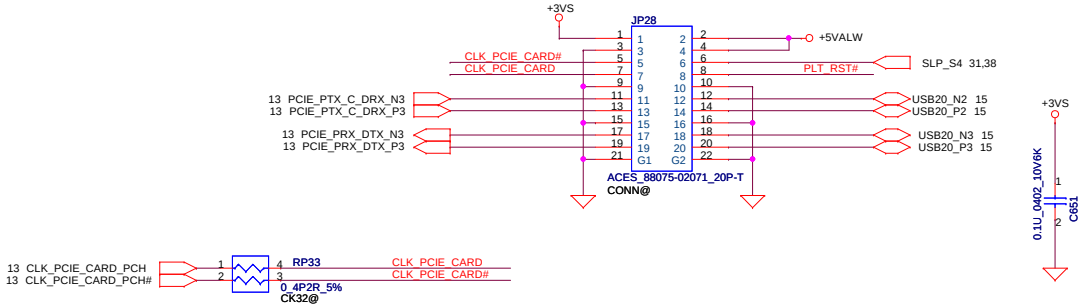
Serial Port CONN







Card Reader 7 in 1 + 2 Port USB Connector



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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **CR&LEDS&PW&Audio&Exp Conn**

Size: Custom | Document Number: LA-4891 | Rev: 0.1

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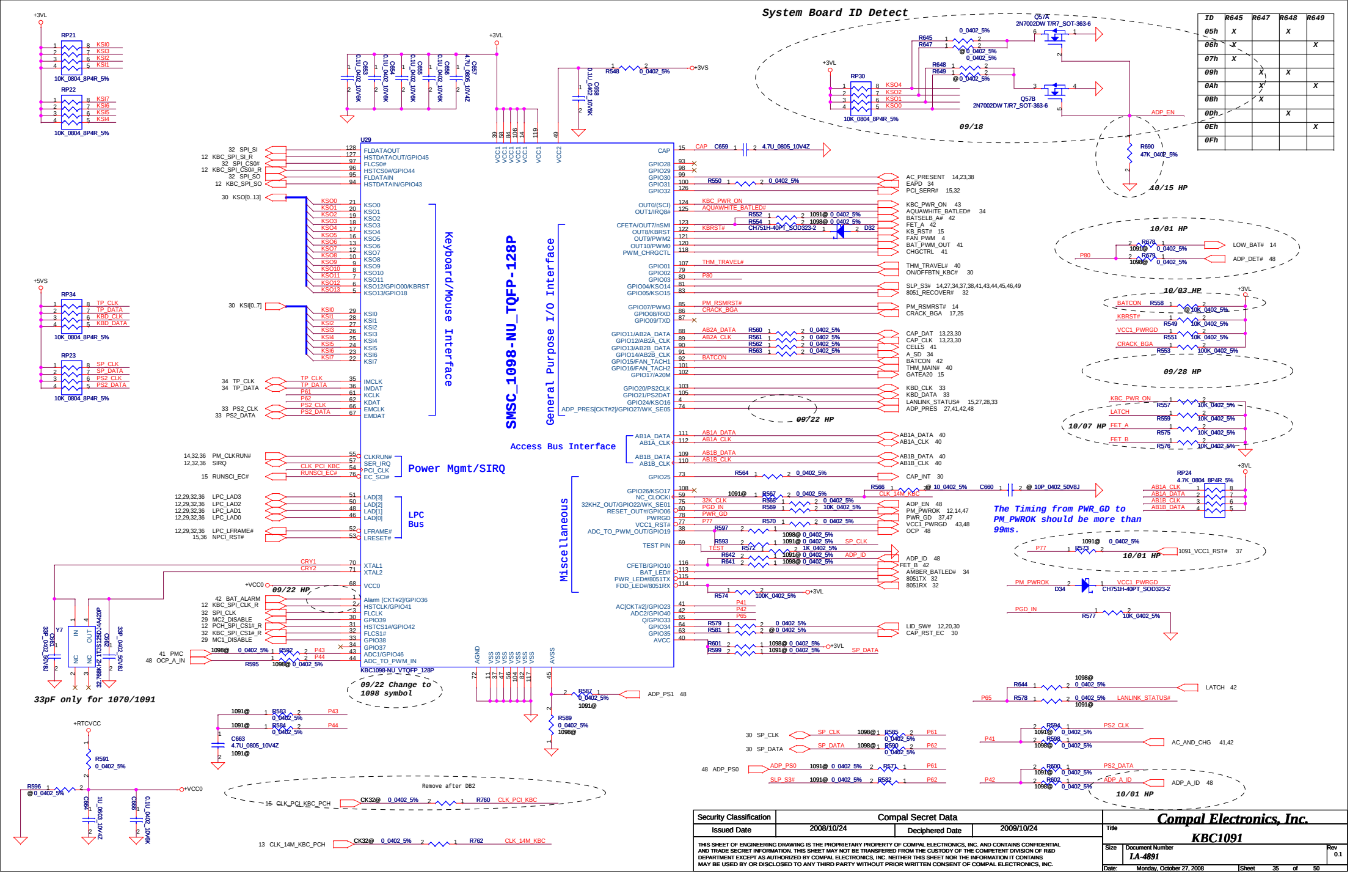

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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **KBC1091**

Size	Document Number	Rev
	LA-4891	0.1

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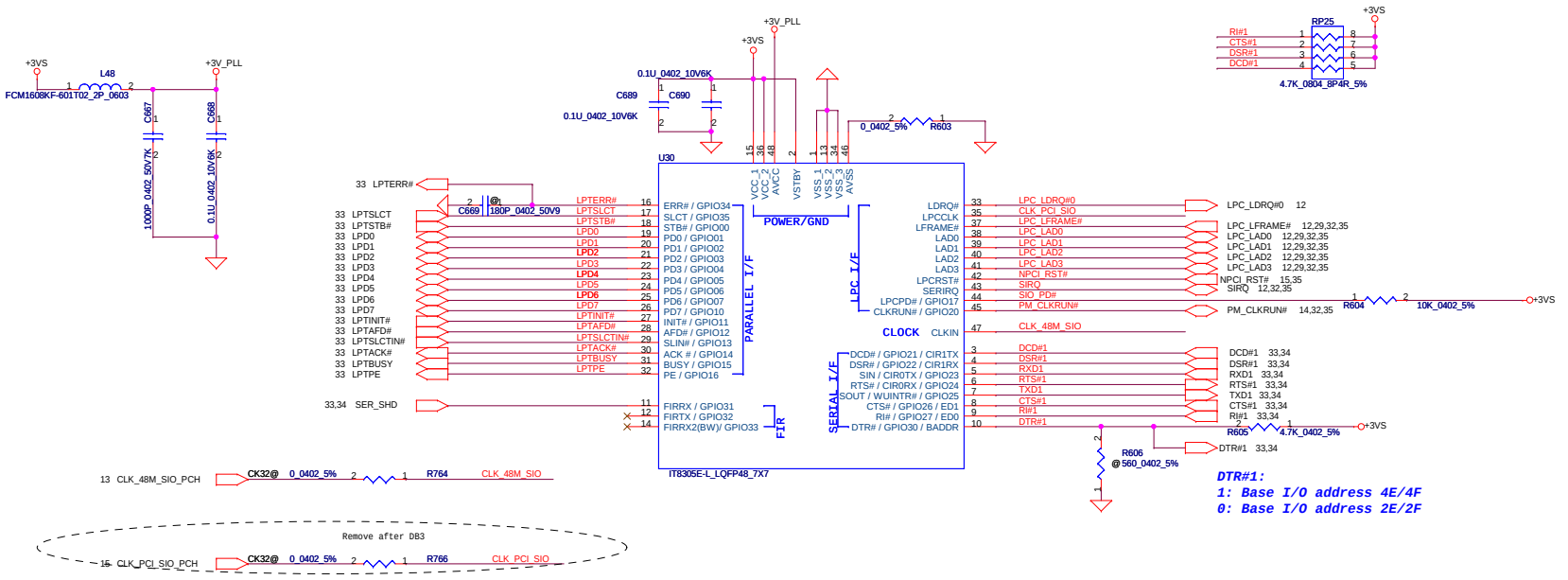
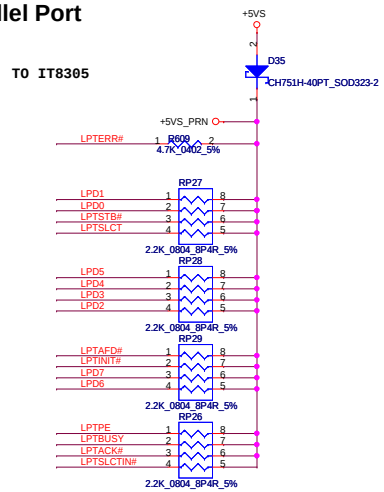


DTR#1:
1: Base I/O address 4E/4F
0: Base I/O address 2E/2F

Parallel Port



Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **Super I/O IT8305E**

Size: Custom | Document Number: LA-4891 | Rev: 0.1

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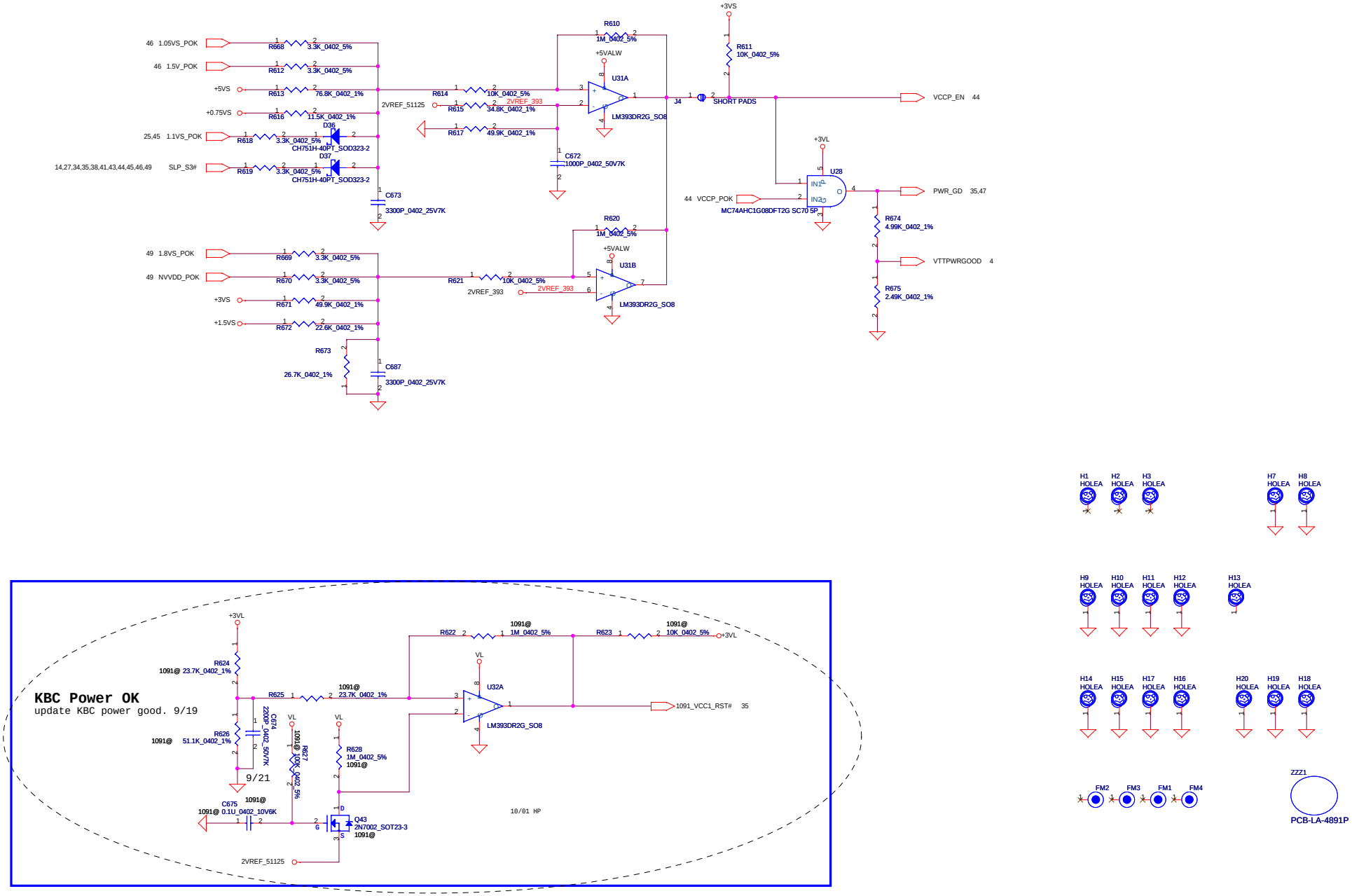

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **POK CKT**

Size | Document Number: *LA-4891* | Rev: 0.1

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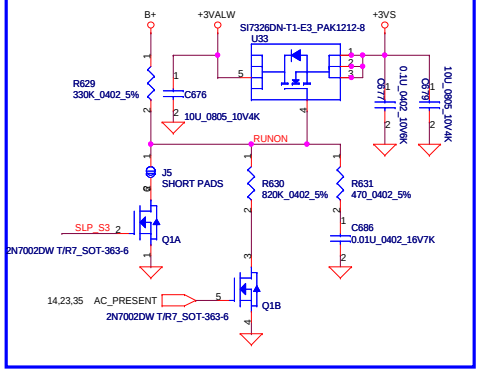
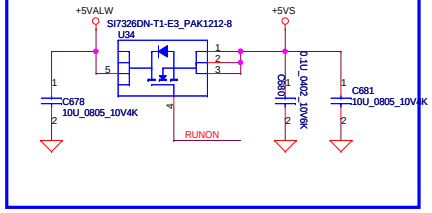
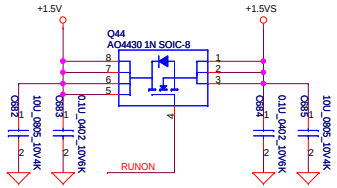
+3VALW to +3VS Transfer

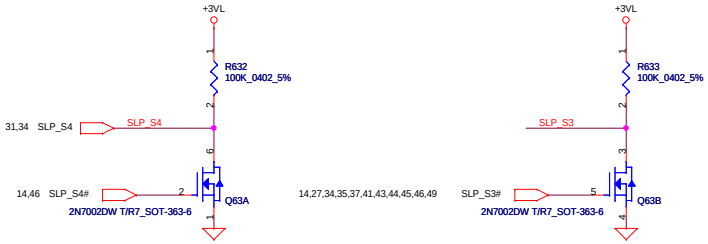


+5VALW to +5VS Transfer

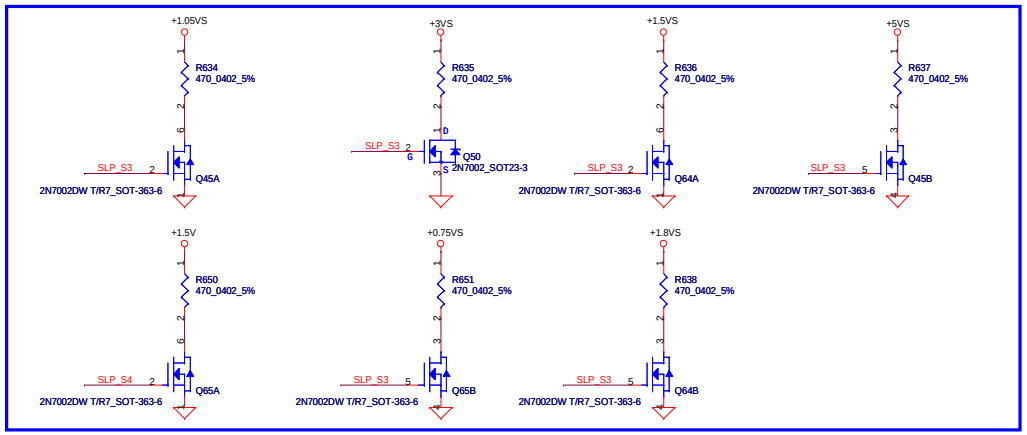


+1.5V to +1.5VS Transfer





Discharge circuit-1



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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **DC/DC Circuits**

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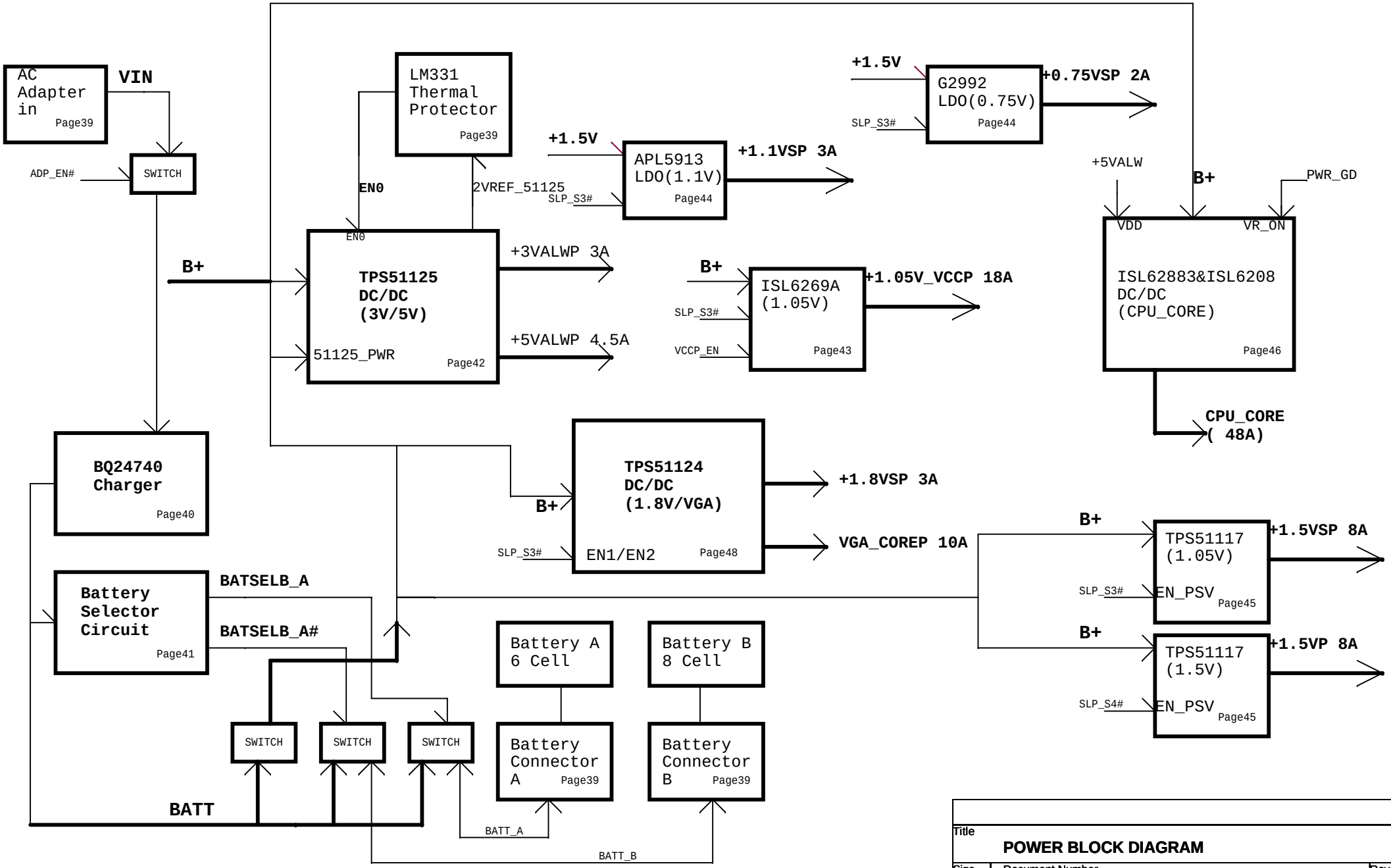
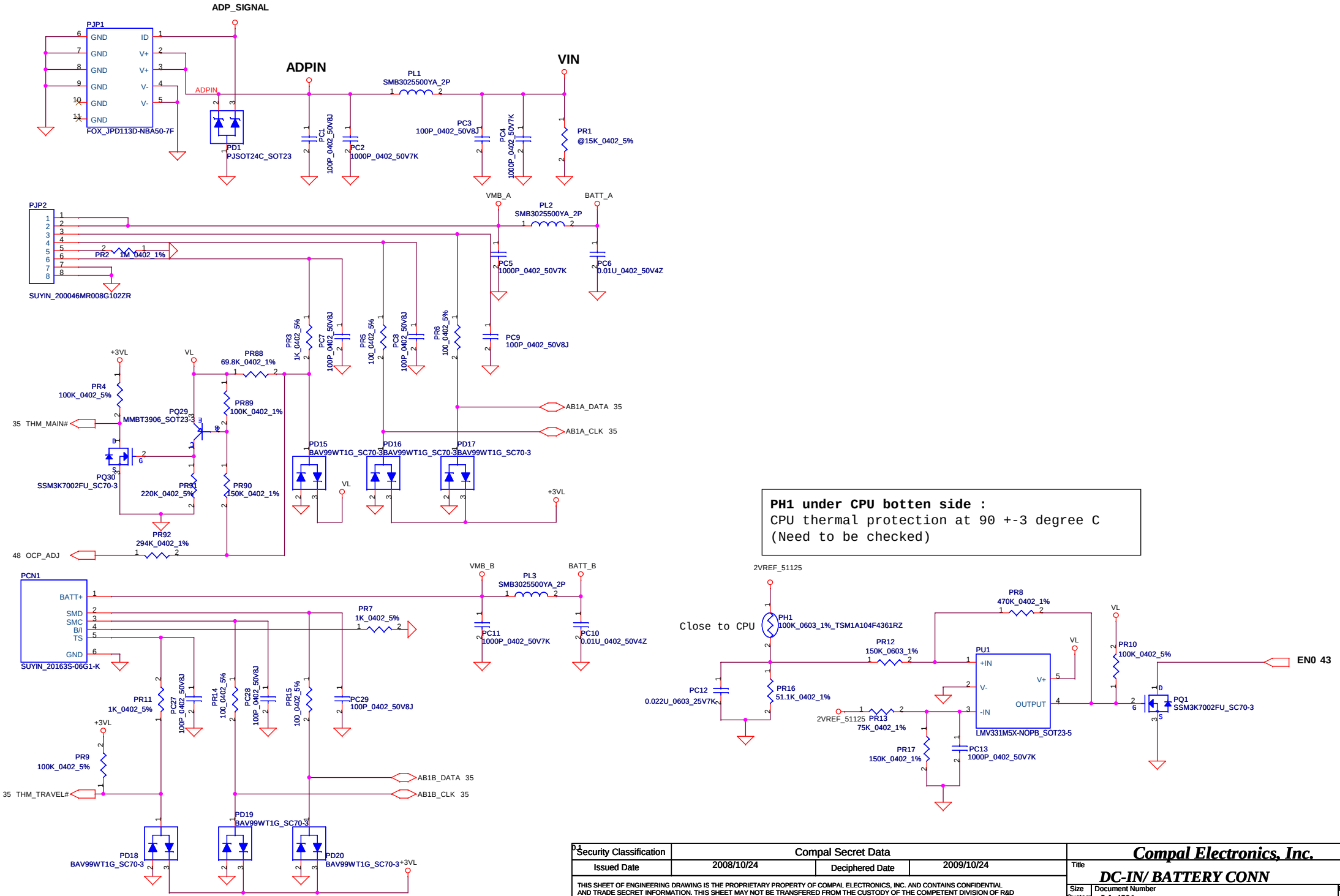


Title	POWER BLOCK DIAGRAM		
Size	Document Number		Rev
Date: Monday, October 27, 2008	Sheet 39 of 50		



PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
(Need to be checked)

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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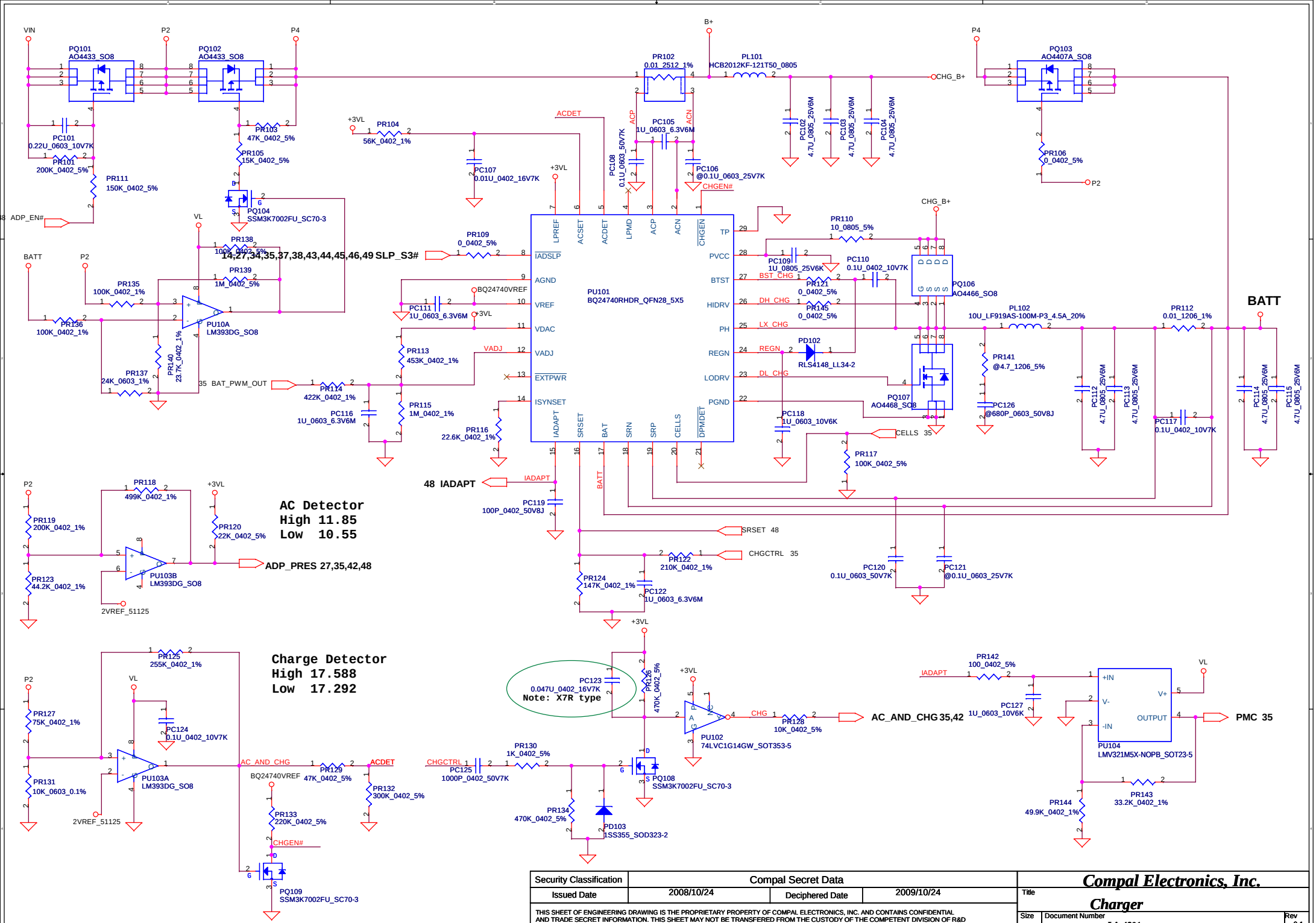
Compal Electronics, Inc.

Title: **DC-IN/ BATTERY CONN**

Size: Custom | Document Number: LA-4891 | Rev

Date: Monday, October 27, 2008 | Sheet 40 of 50



Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **Charger**

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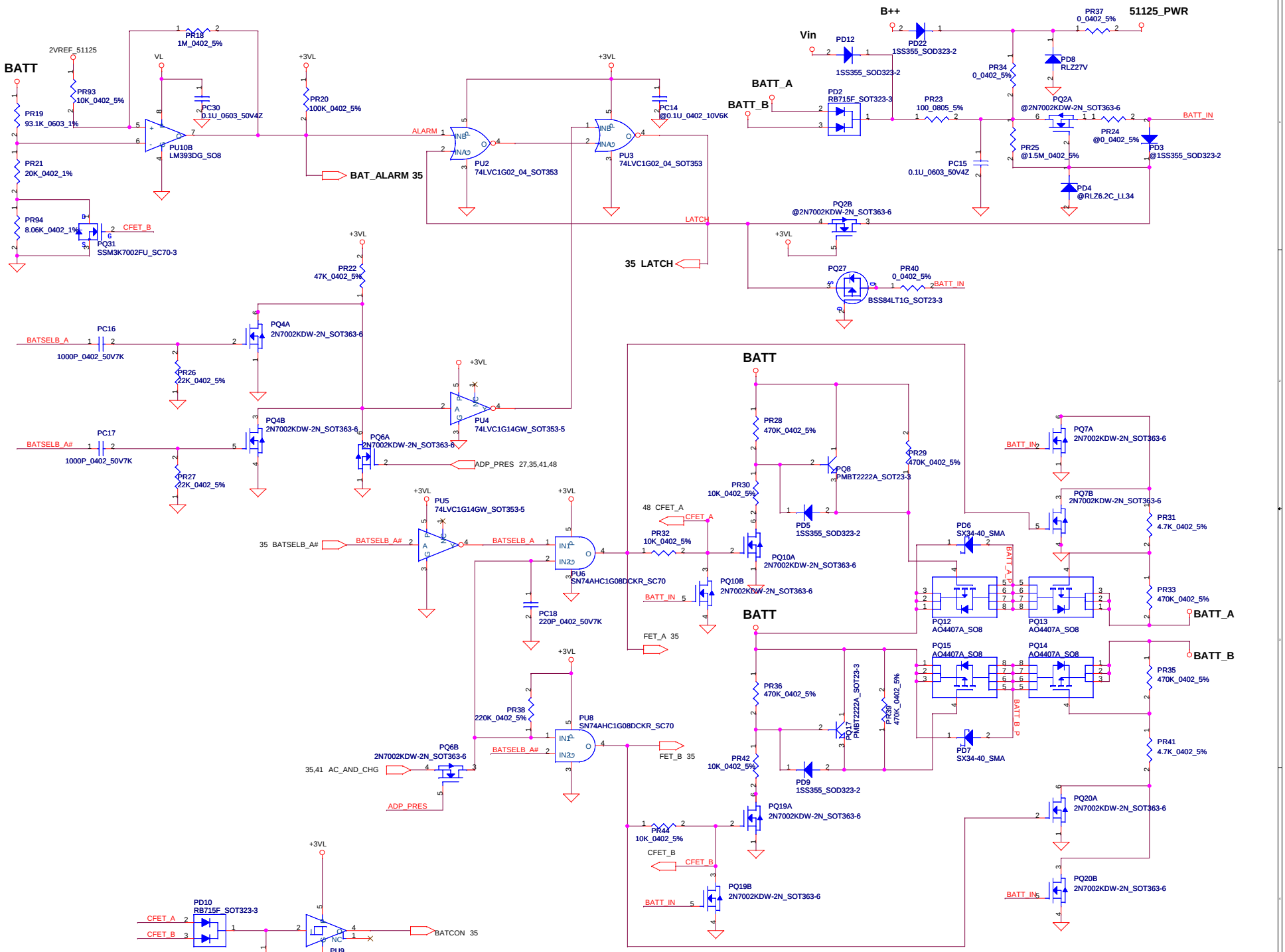

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **Battery selector**

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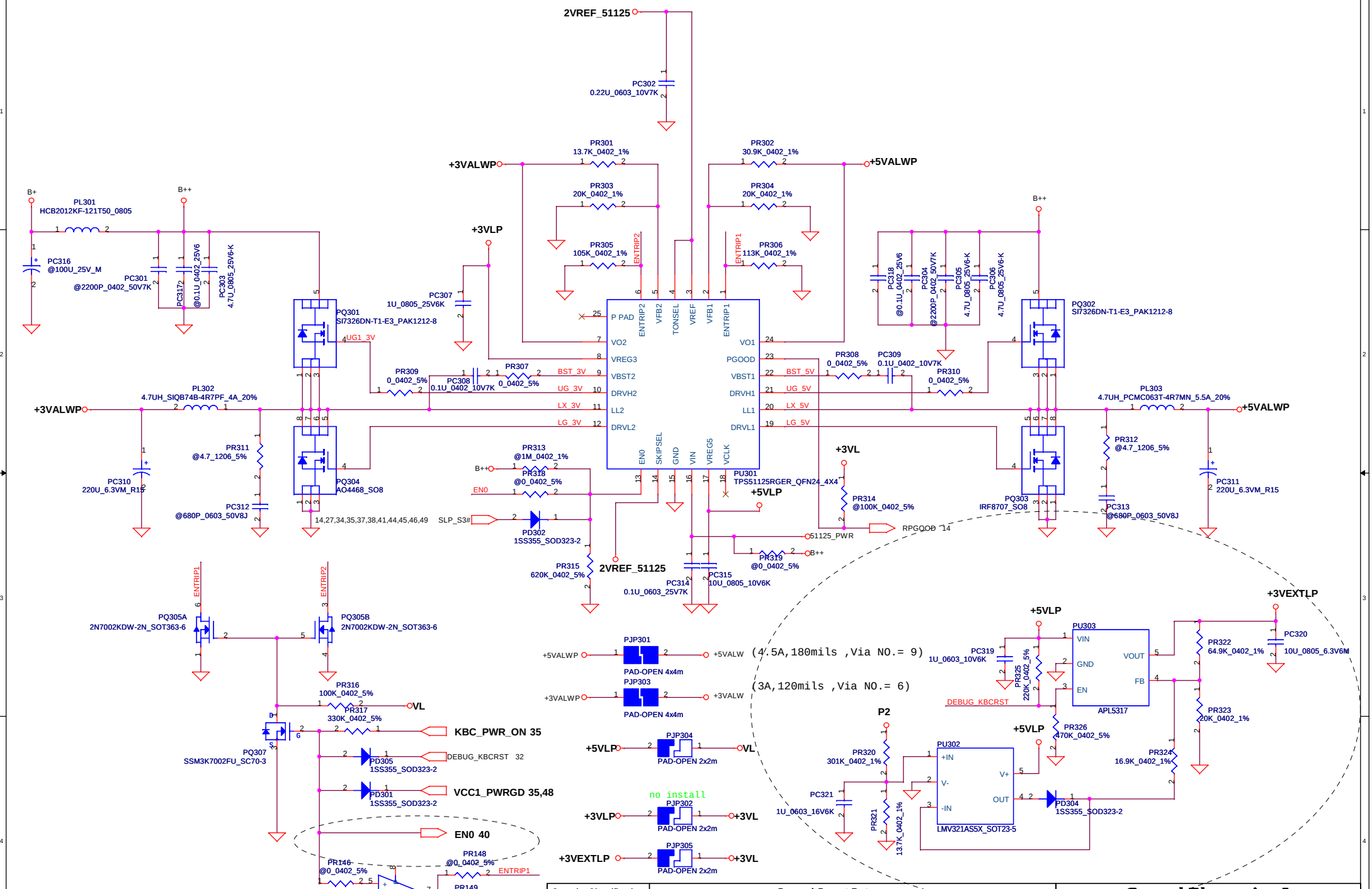

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

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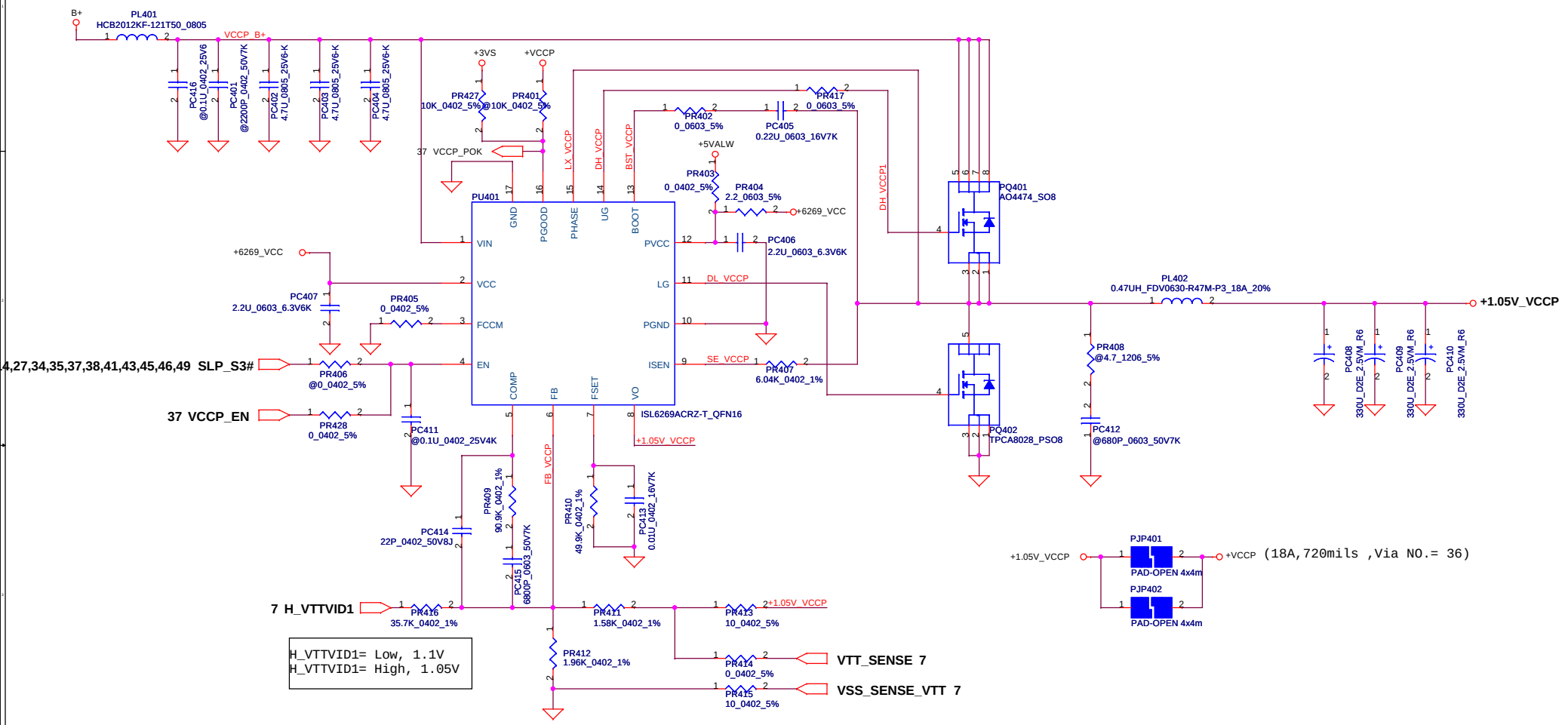

H_VTTVID1= Low, 1.1V
H_VTTVID1= High, 1.05V

Security Classification	Compal Secret Data		
Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **1.05V_VCCP**

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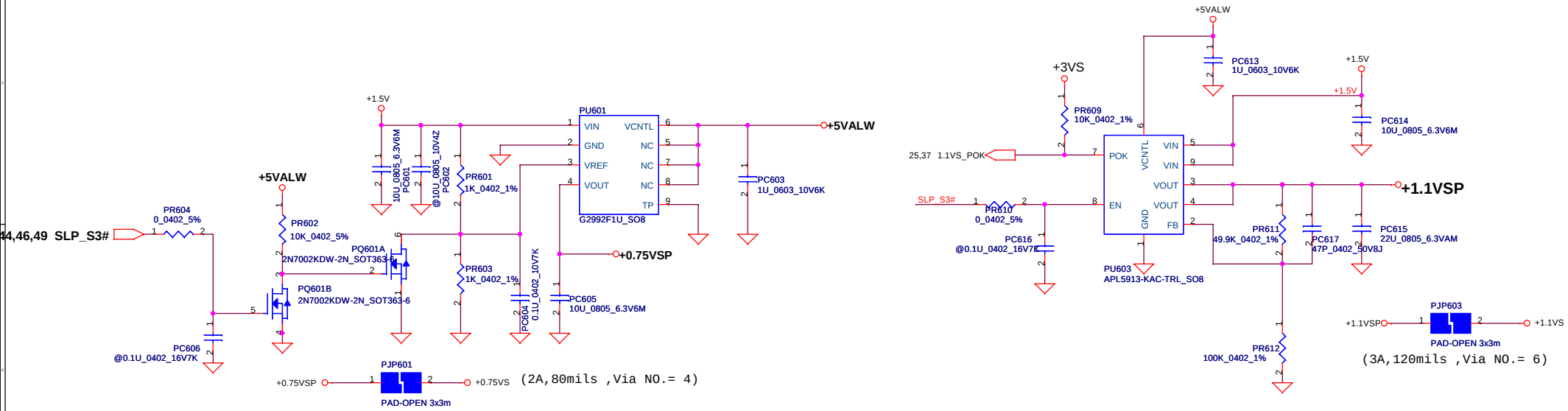

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Issued Date	2008/10/24	Deciphered Date	2009/10/24

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Compal Electronics, Inc.

Title: **0.75VSP/PCIE**

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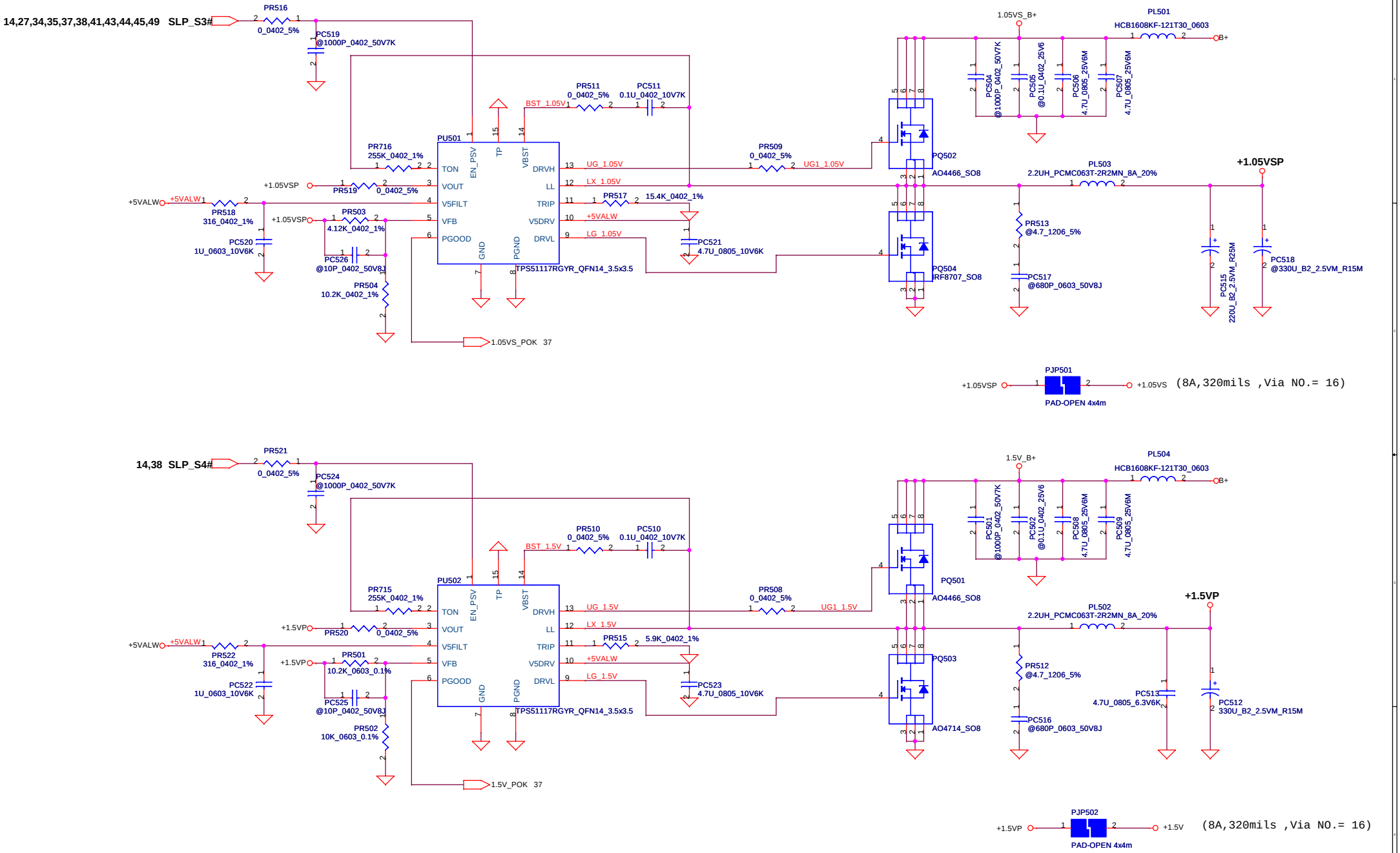

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Compal Electronics, Inc.

Title: **1.5VP/1.05VSP**

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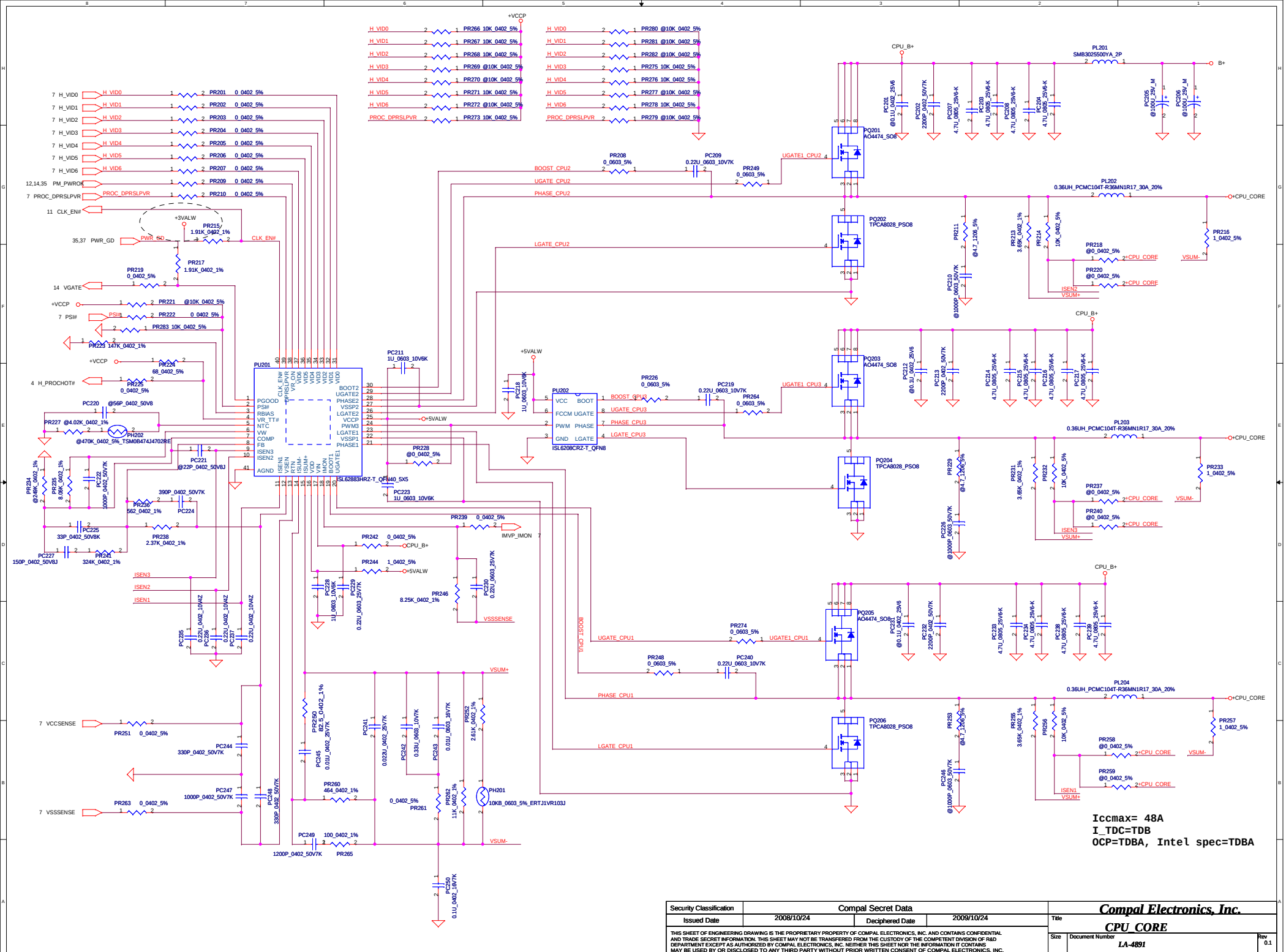

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Compal Electronics, Inc.

Title: **CPU_CORE**

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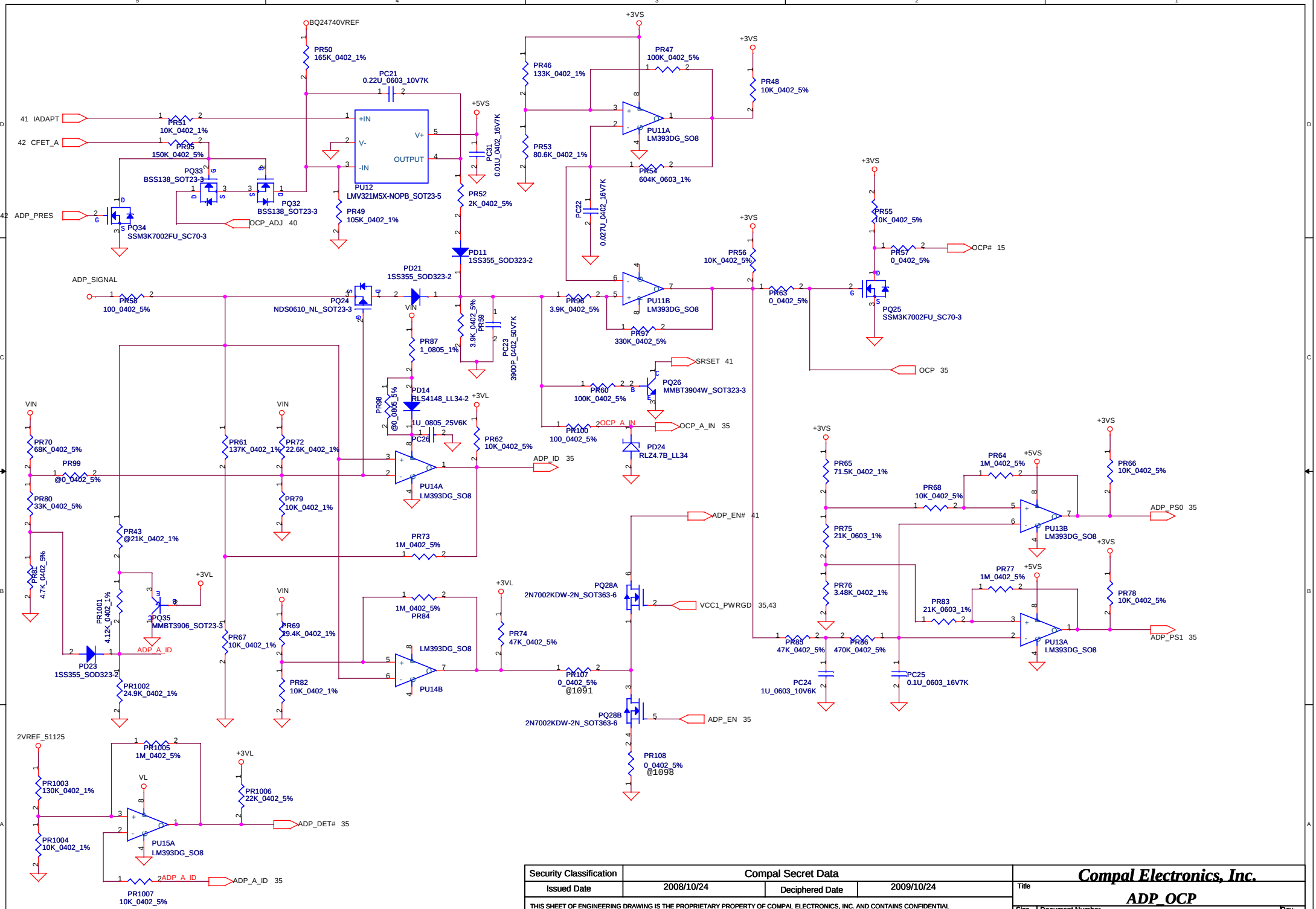

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Compal Electronics, Inc.

Title: **ADP_OCP**

Size: Custom | Document Number: *LA-4891* | Rev

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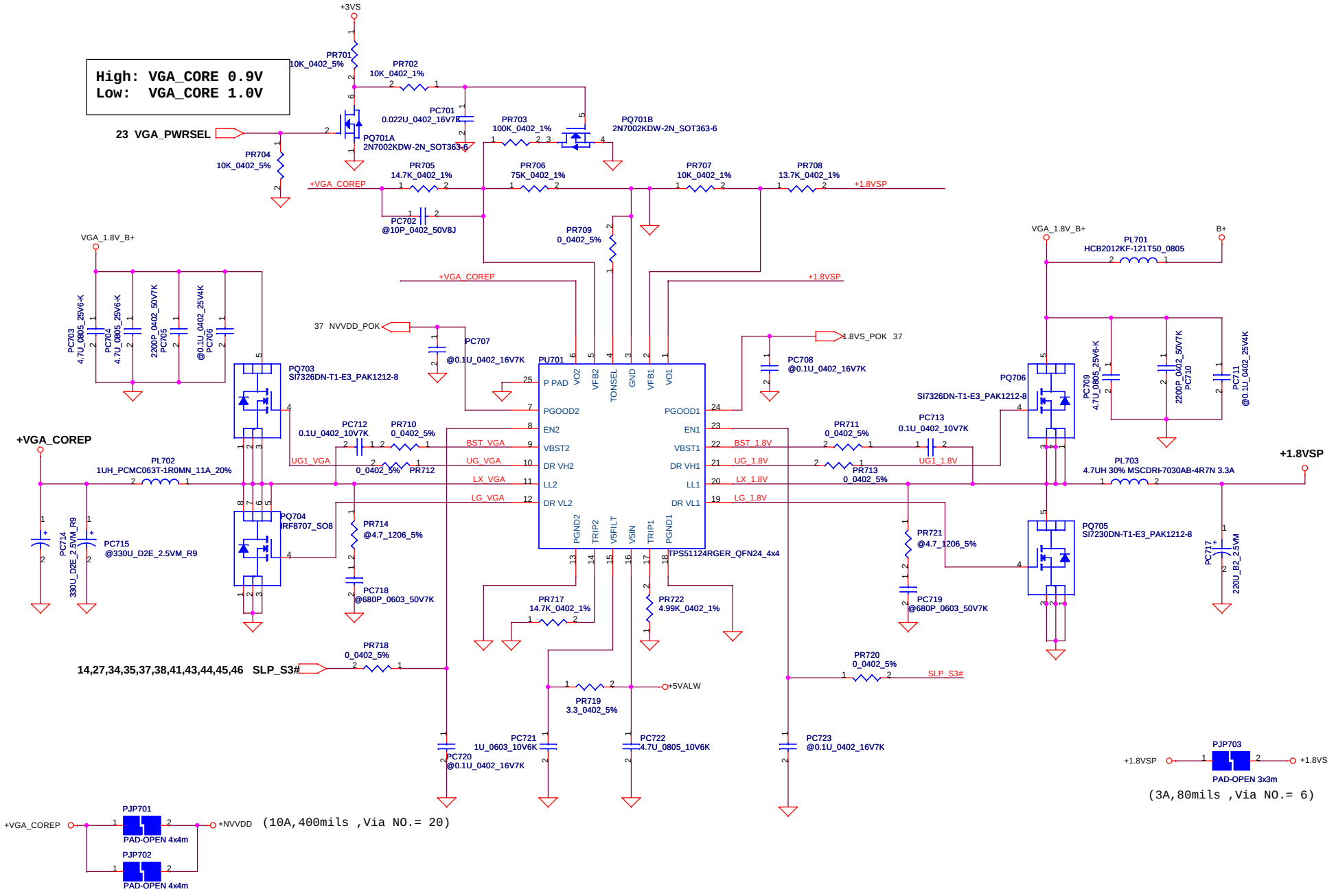

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Compal Electronics, Inc.

Title: VGA_CORE/ 1.8VSP

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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
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7					

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