Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2008-05-22
REV：0.3

機密 等級 研發二部 產品人員 產品日期 解密日期

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Title: *Cover Sheet*

Size: Custom | Document Number: *Montevina Consumer UMA* | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 1 of 44

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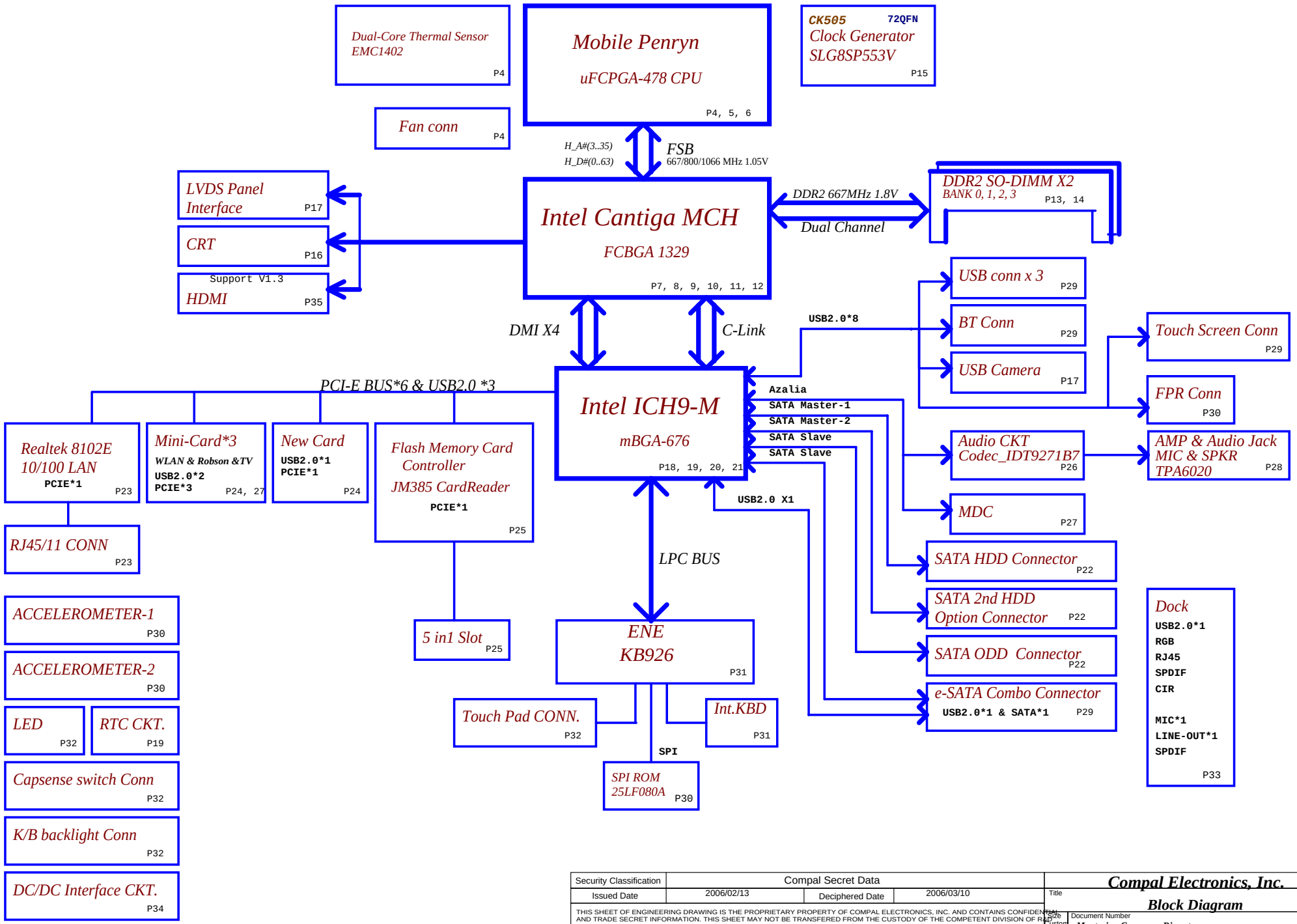
Montevina Consumer UMA



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Block Diagram			
Size: Custom	Document Number: Montevina Consumer Discrete		Rev: 0.3
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB assignment :	PCIe assignment :
USB-0 Right side port	PCIe-1 WLAN
USB-1 Right side port	PCIe-2 Robson
USB-2 Left side port (combo with ESATA)	PCIe-3 TV-tuner
USB-3 Dock	PCIe-4 LAN
USB-4 USB Camera	PCIe-5 Card reader
USB-5 WLAN	PCIe-6 New card
USB-6 Bluetooth	
USB-7 Finger Printer	
USB-8 TV-tuner	
USB-9 New card	
USB-10 Left side port	
USB-11 Touch screen	

Symbol Note :

: means Digital Ground

: means Analog Ground

45@ : stuff when 45 level assembly.
@ : just reserve , no stuff.
DEBUG@ : reserve for debug only.

SMBUS Control Table

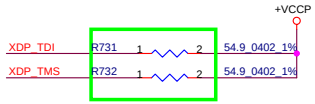
	SOURCE	INVERTER	Battery	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK Gen.	MINI CARD	LCD	Cap.board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V CY
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
ESB_CLK ESB_DAT	KB926	X	X	X	X	X	X	X	X	V ENE
DDC2_CLK DDC2_DAT	North Bridge	X	X	X	X	X	X	X	V	X
ICH_SMBCLK ICH_SMBDATA	South Bridge	X	X	X	X	V	V	V	X	X

I2C / SMBUS ADDRESSING

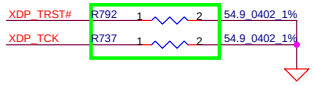
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

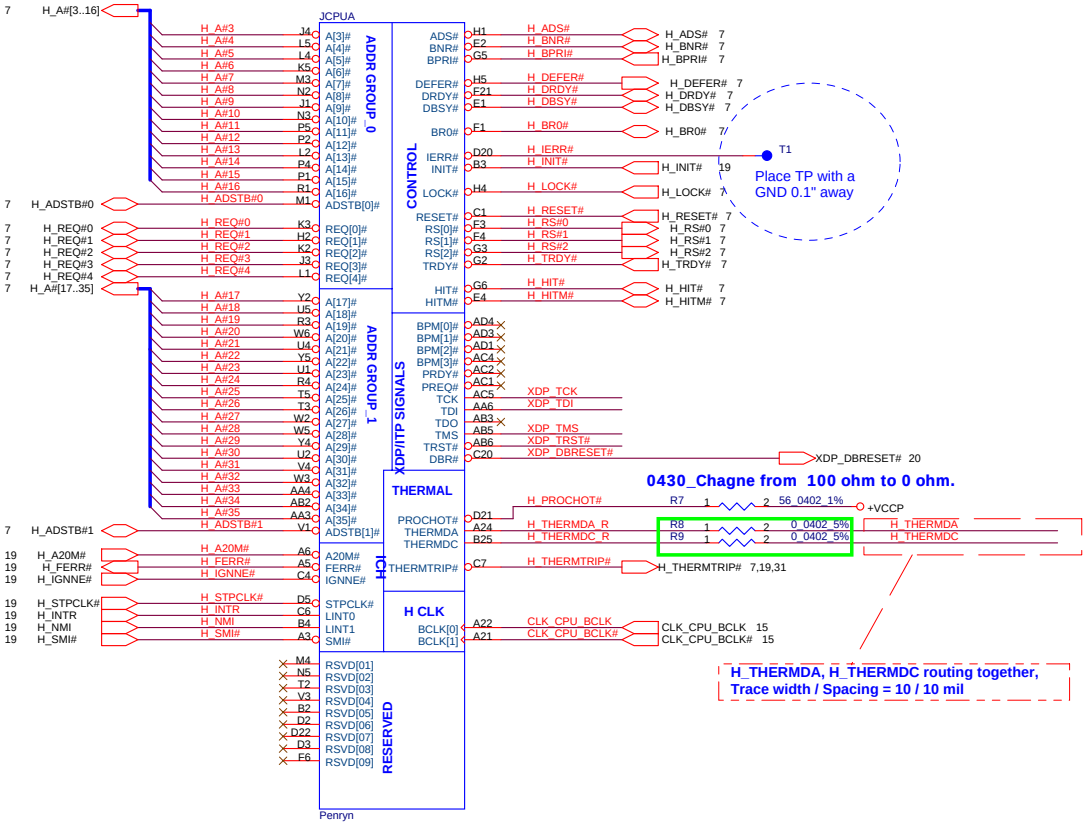
ITP-XDP Connector

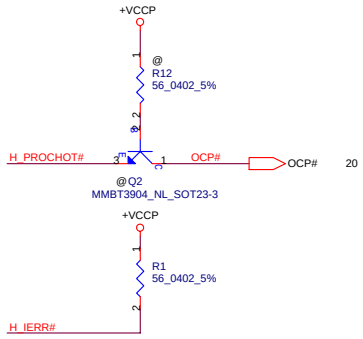
0512_Remove XDP debug port.

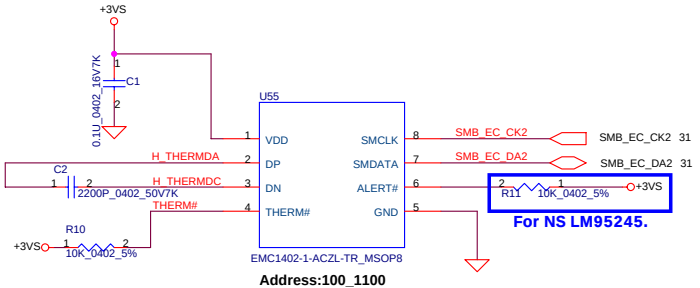


0512_Change value to 54.9 ohm if remove XDP port.

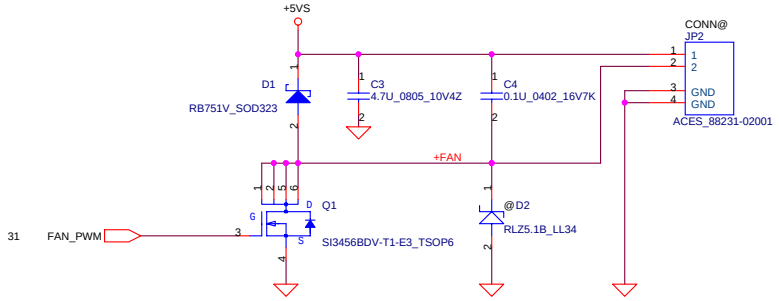








PWM Fan Control circuit



Security Classification	Compal Secret Data		
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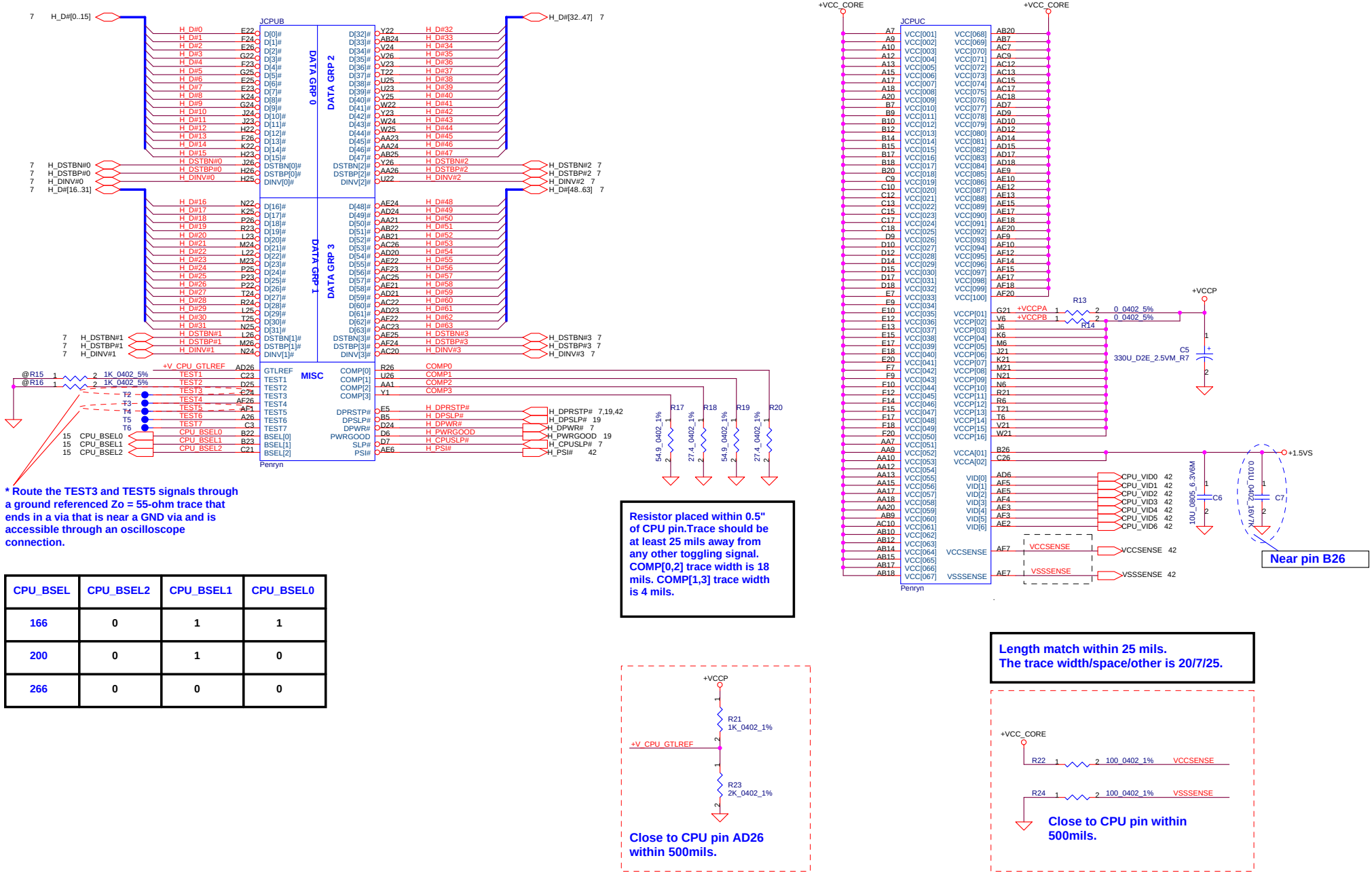
Compal Electronics, Inc.

Title: Penryn(1/3)-AGTL+/ITP-XDP

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Monday, May 26, 2008 | Sheet 4 of 44



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Penryn(2/3)-AGTL+/ITP-XDP

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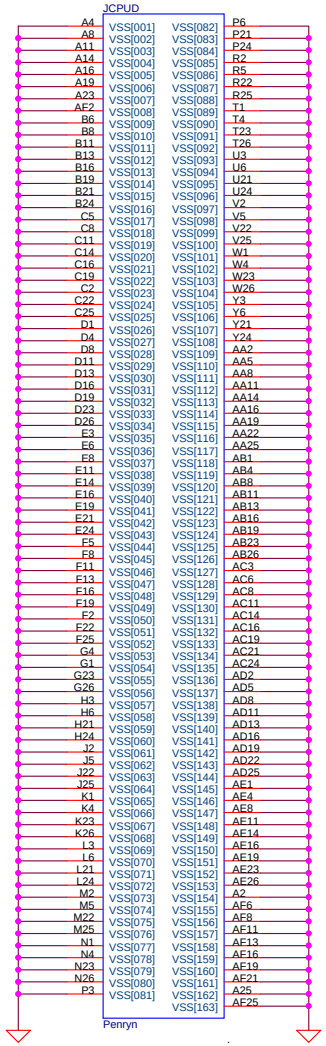
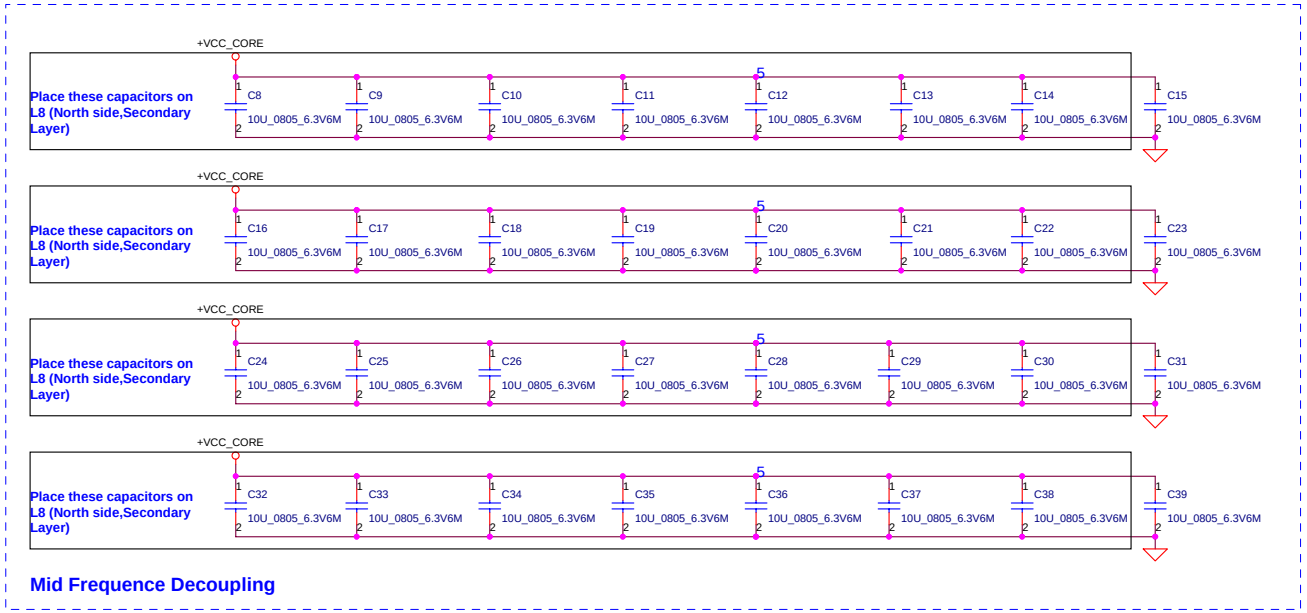
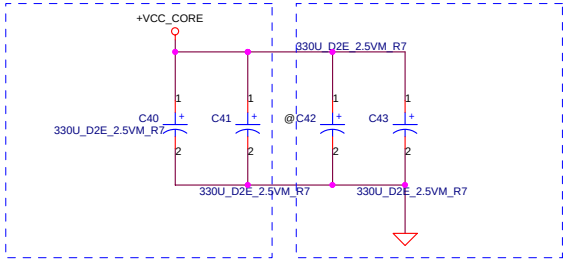
Date: Monday, May 26, 2008 | Sheet 5 of 44

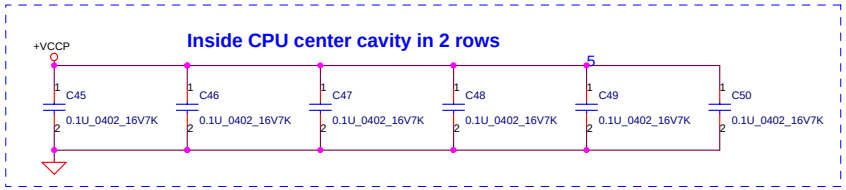




Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF





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Compal Electronics, Inc.			
Title: Penryn(3/3)-AGTL+/ITP-XDP			
Size: Custom	Document Number: Montevina Consumer Discrete		Rev: 0.3
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Layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC

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Compal Electronics, Inc.

Title: **Cantiga(1/6)-AGTL/DMI/DDR**

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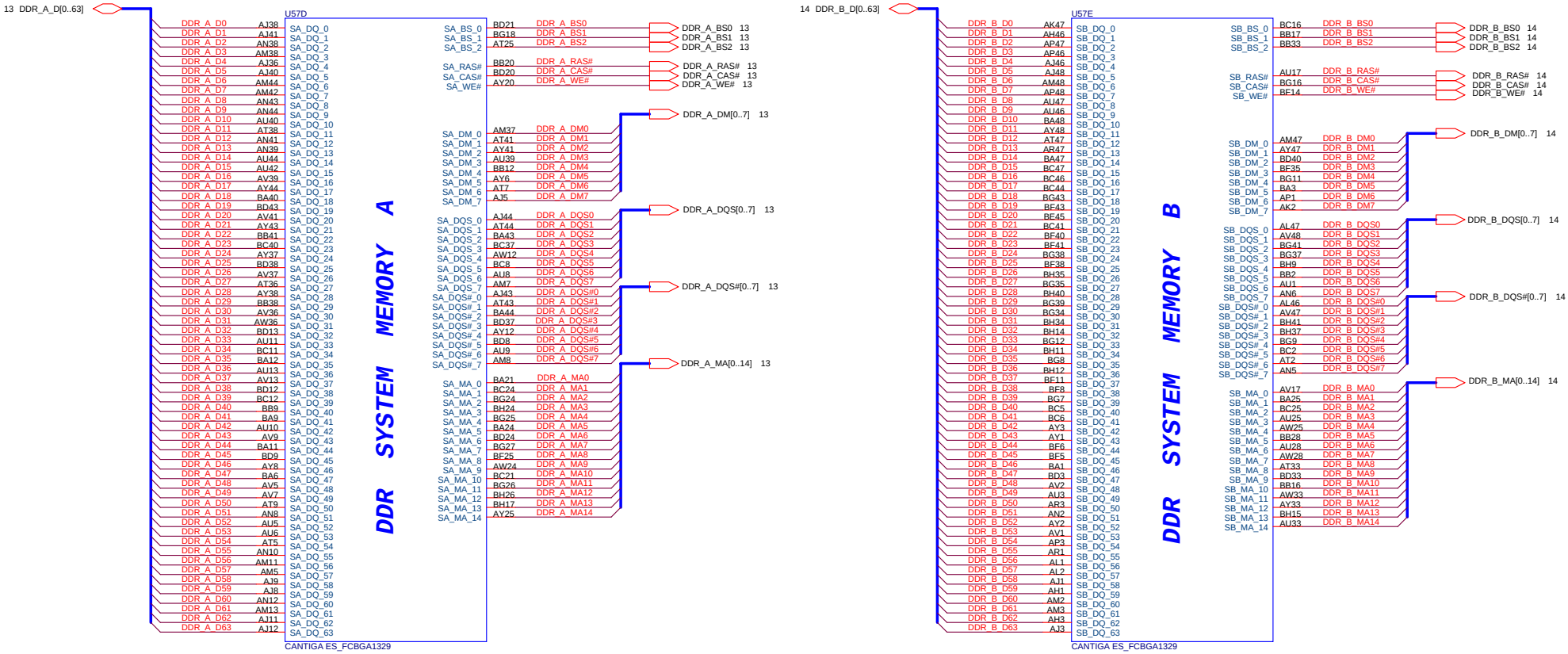

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

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Reserve for Intel DPST function.

Follow Intel DG & Checklist

Follow Intel DG & Checklist

Follow Intel DG & Checklist

0430_Remove C1018~C1025 (Reserve for WWAN issue)

Solve 3G WWAN issue

PEGCOMP trace width and spacing is 20/25 mils.

Reserve for Intel DPST function.

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

0505_Double confirm Strapping setting.

Useless Strapping

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Title: Cantiga(3/6)-VGA/LVDS/TV

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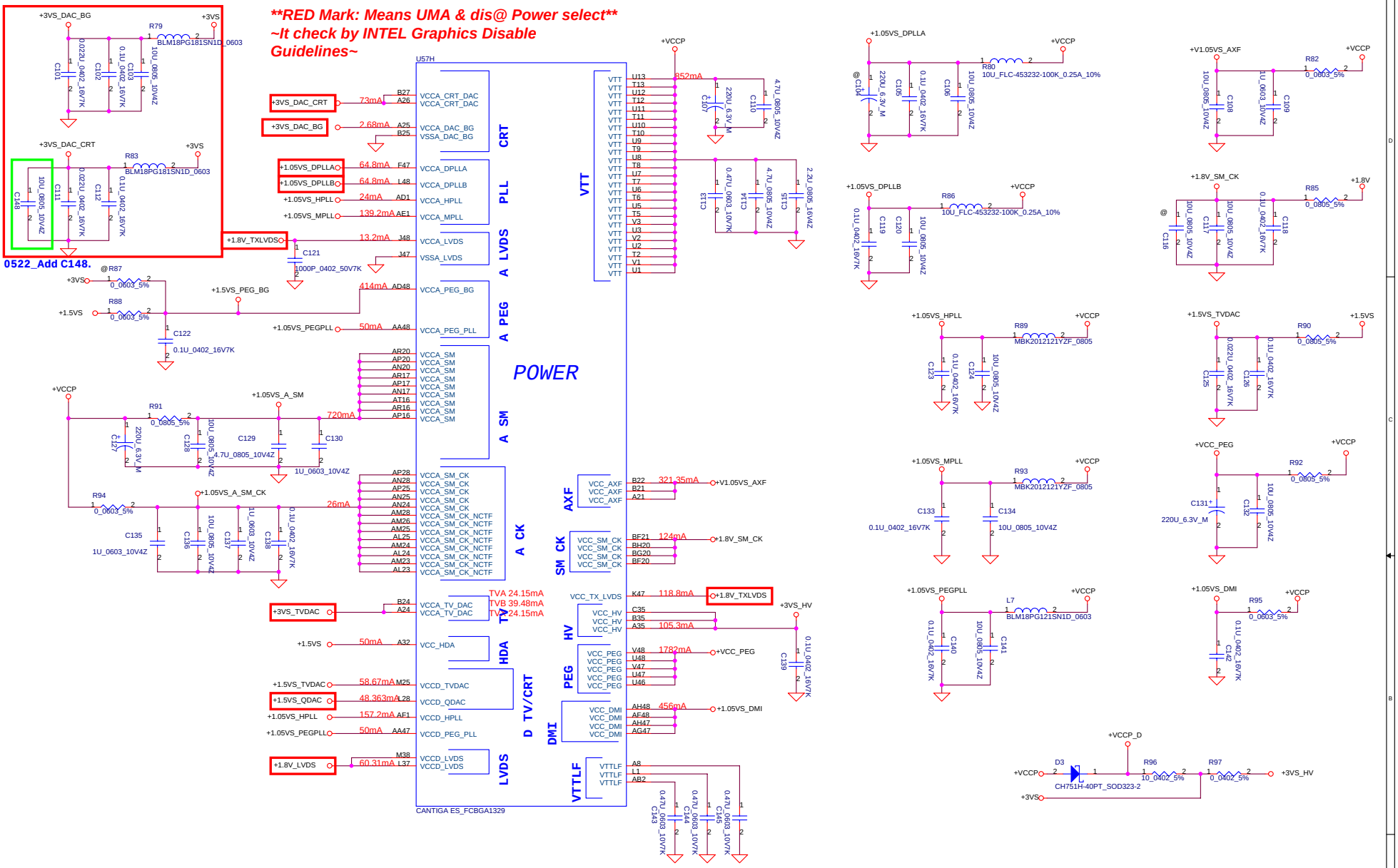
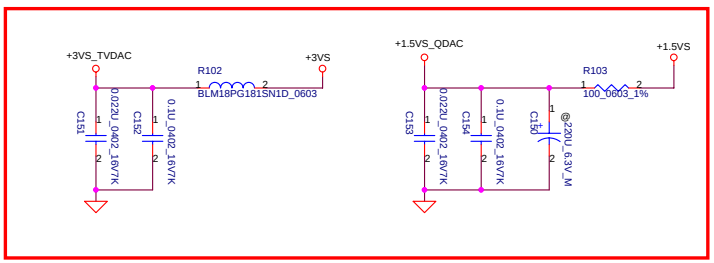
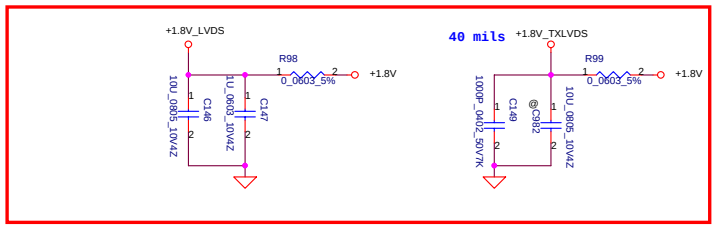
****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable Guidelines~

0522_Add C148.







Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(4/6)-PWR**

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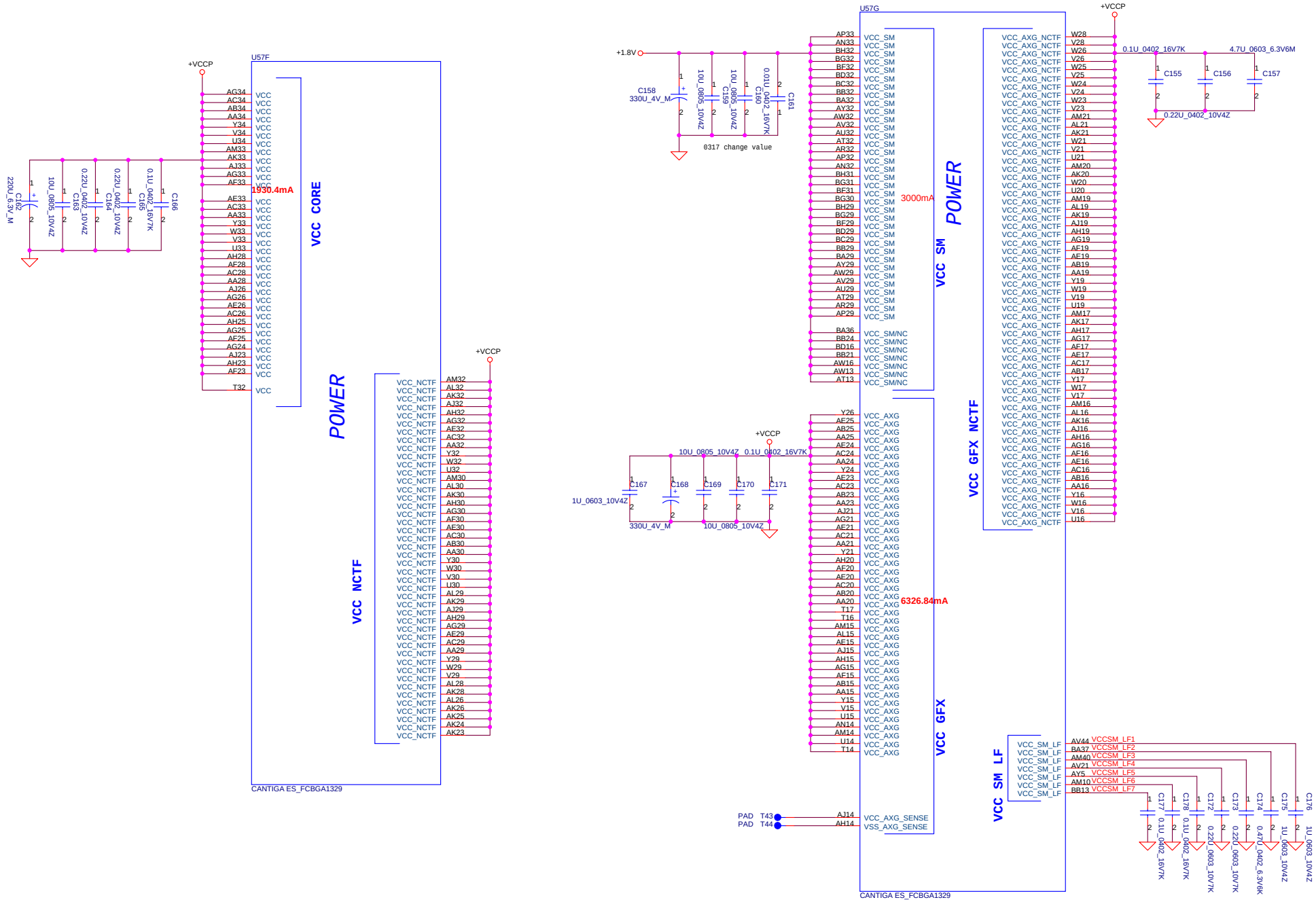

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Cantiga(5/6)-PWR/GND

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

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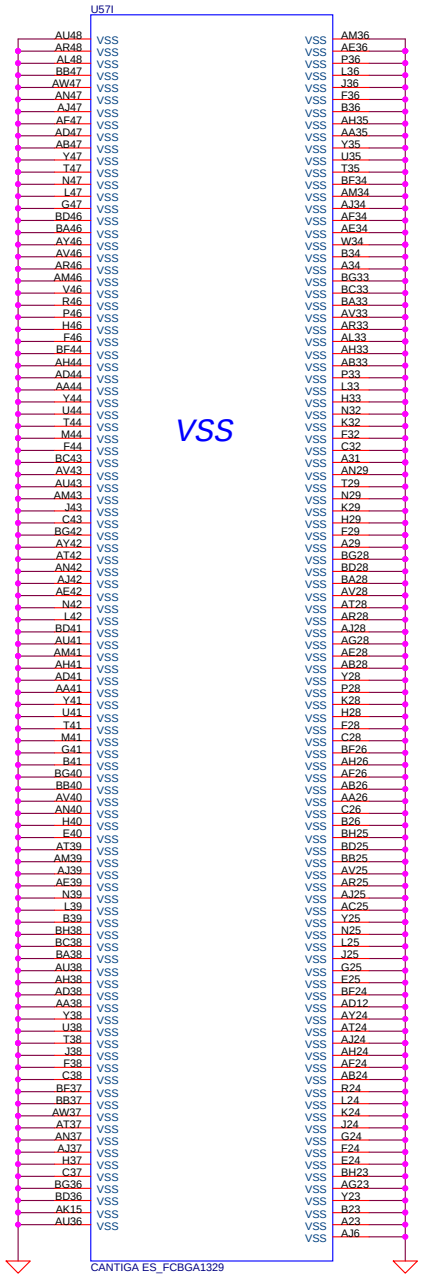

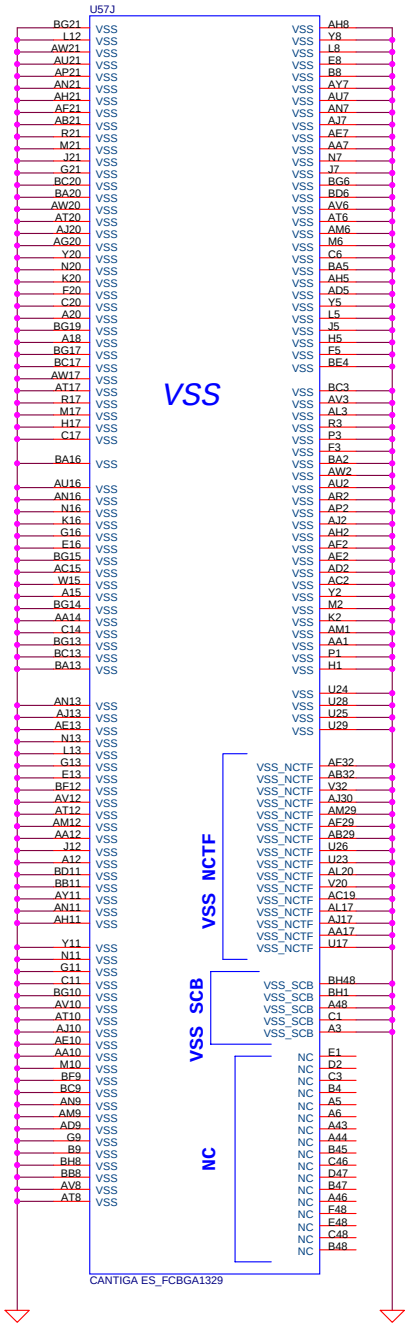

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(6/6)-PWR/GND**

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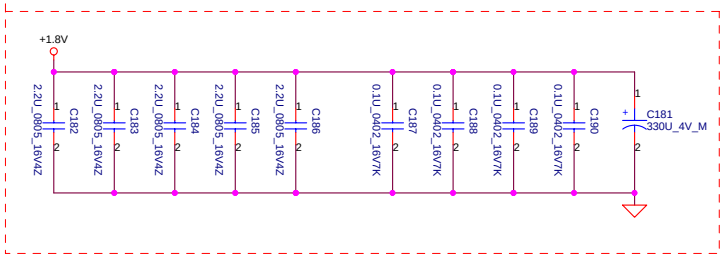
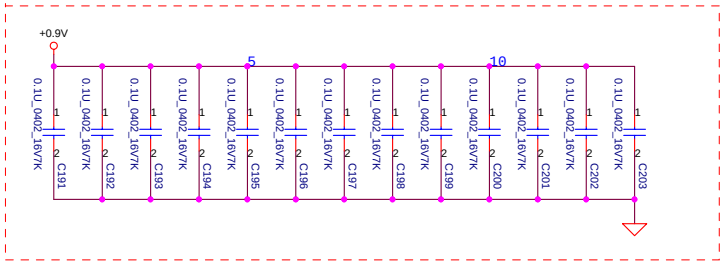
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..14]

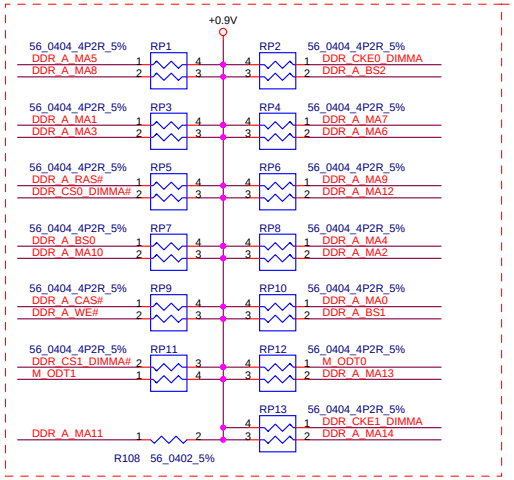
Layout Note:
Place near JDIMM1

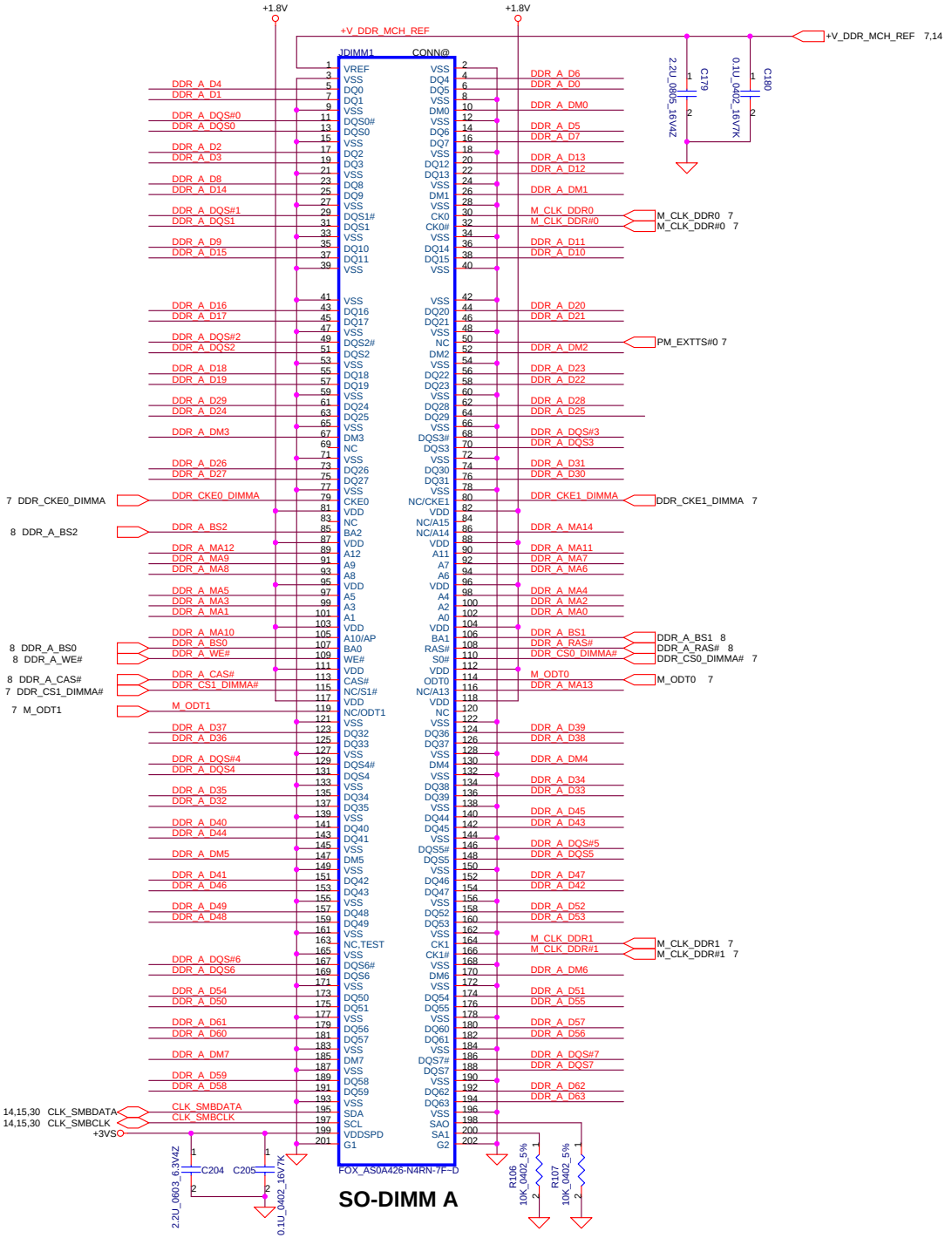


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

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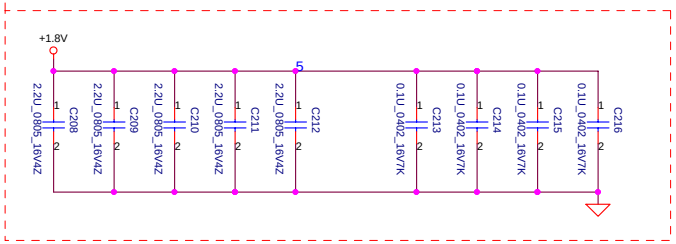
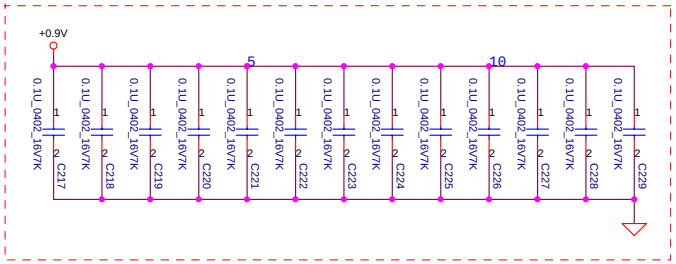
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..14]

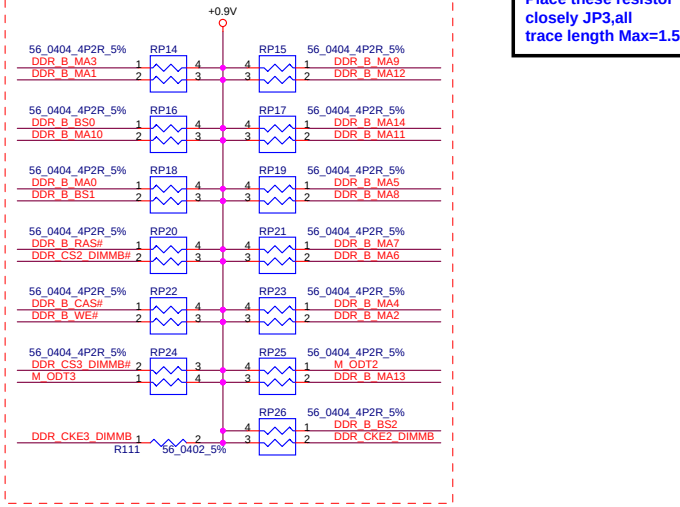
Layout Note:
Place near JDIMM2

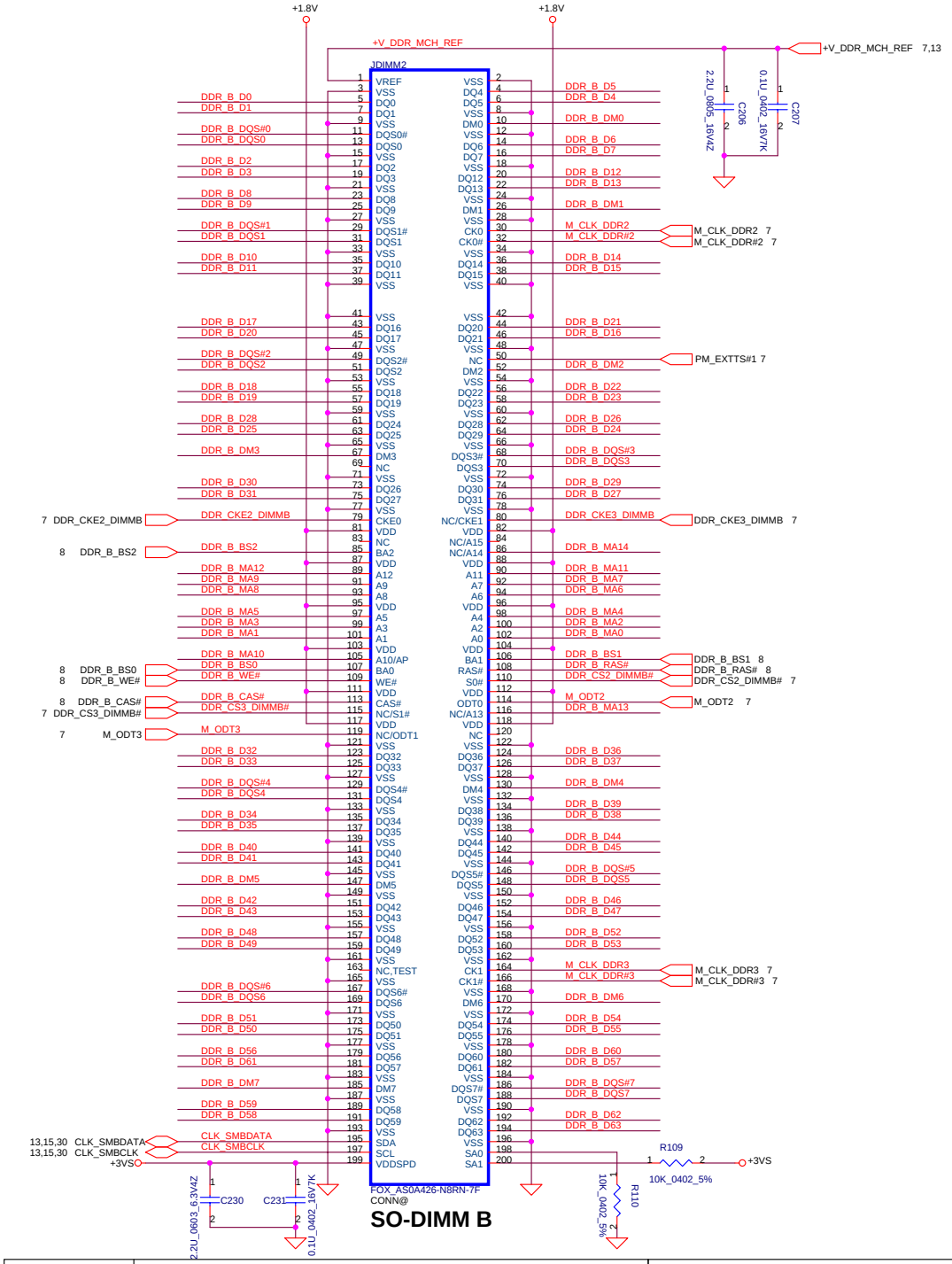


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

Size: | Document Number: **Montevina Consumer Discrete** | Rev: 0.3

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil

Place close to U51

NB CPU

Card Reader

XDP/ITP

3G_PLL

TV tuner

0512_Delete clock for XDP debug port.

0512_Reserve R126.

WLAN

Robson

LAN

New Card

SATA

ICH

NB_SSC (UMA)

No USB CardReader anymore

NB (UMA)

SB, MINI PCI

0507_Reserve R714.

ITP_EN	0 = SRC8/SRC8# (SRC8@) 1 = ITP/ITP# (XDP@)
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Clock Generator CK505

Size: | Document Number: Montevina Consumer Discrete | Rev: 0.3

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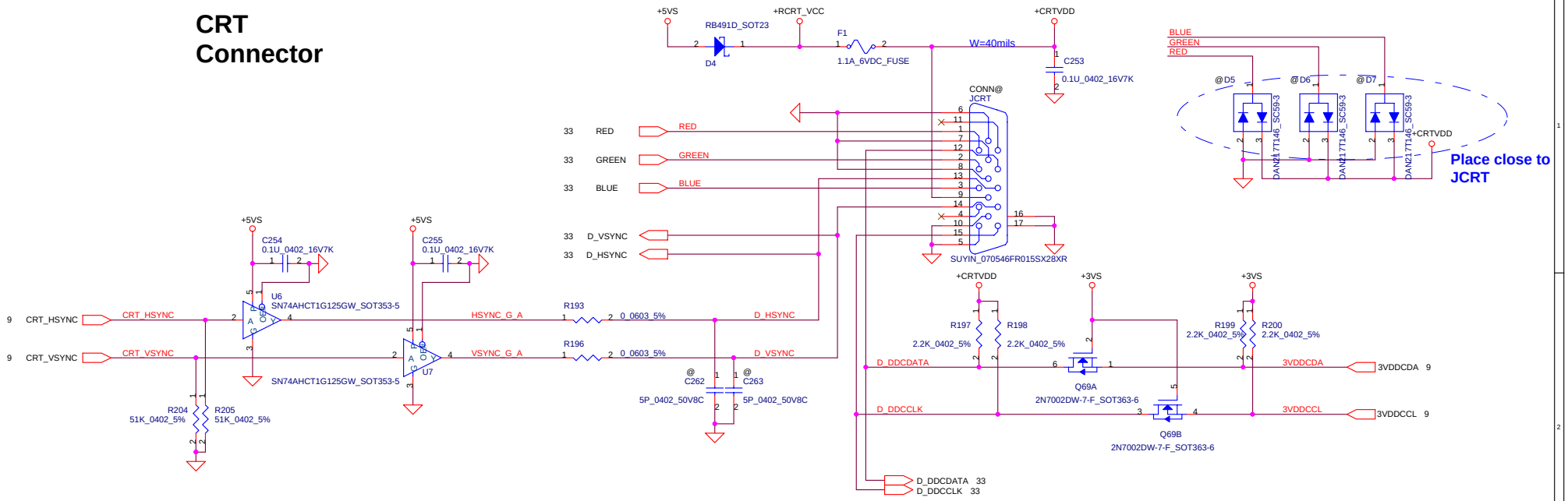
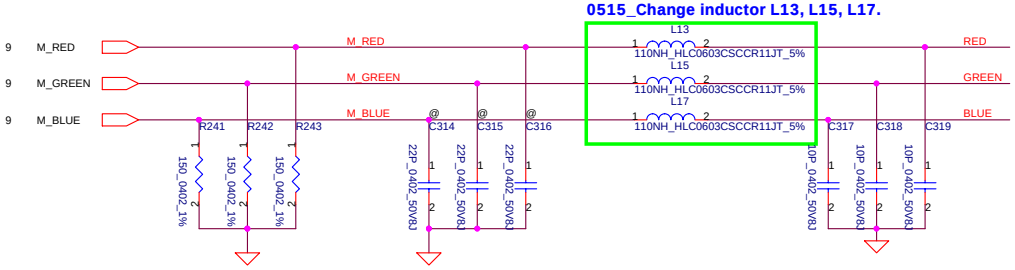
CRT Connector



CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

0515_Change inductor L13, L15, L17.



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **CRT Connector**

Size | Document Number: **Montevina Consumer Discrete** | Rev: 0.3

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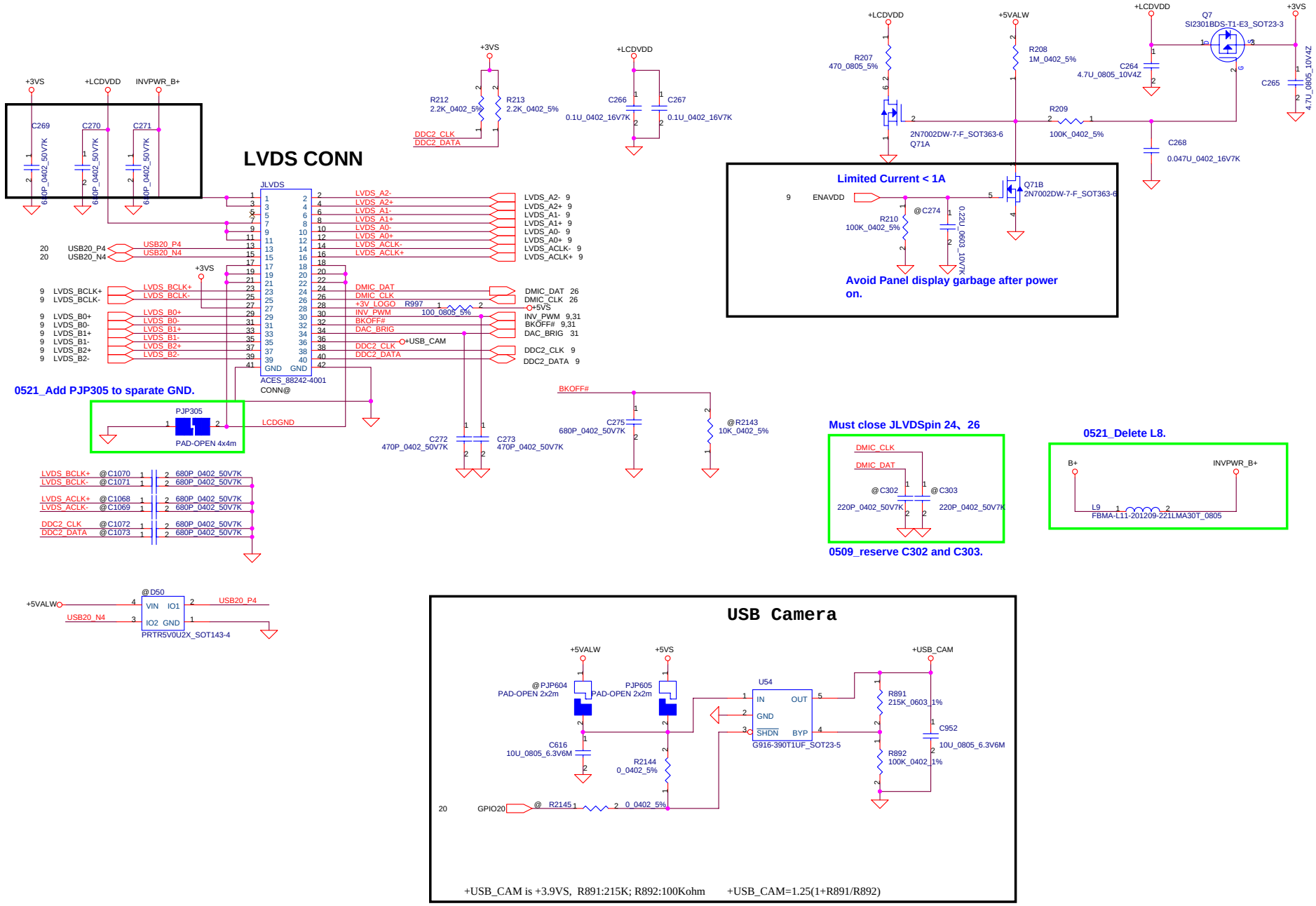

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: LCD CONN.			
Size	Document Number: Montevina Consumer UMA		Rev: 0.3
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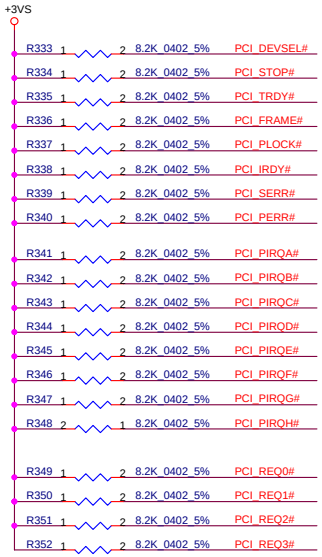
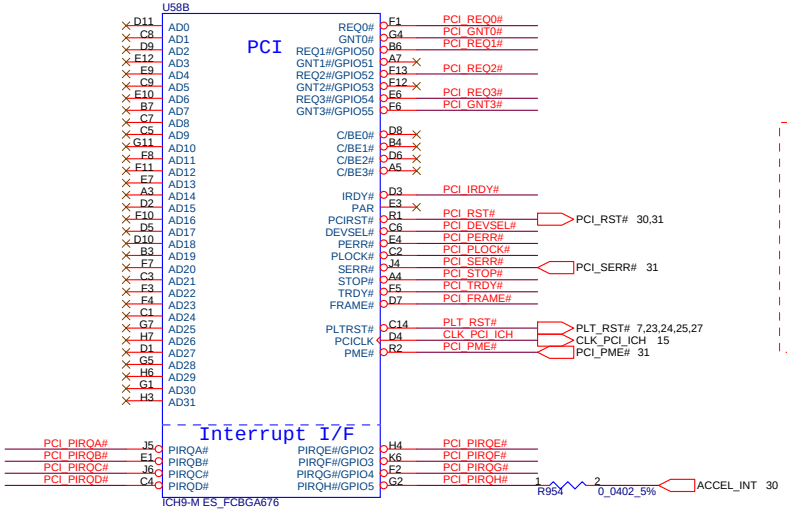
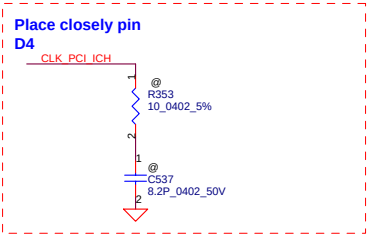
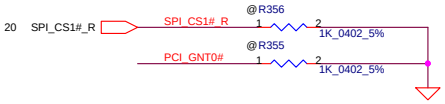






A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(1/4)-PCI/INT

Size: | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 18 of 44

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

0510_Follow Intel check list.

0506_Add R49.

HDD

2nd HDD

ODD

eSATA

placed within 2" from ICH9M

within 2" from R374

Within 500 mils

Place near ICH9

For HDA_BITCLK_NB crossmoat issue

XOR CHAIN ENTRANCE STRAP:RSVD

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

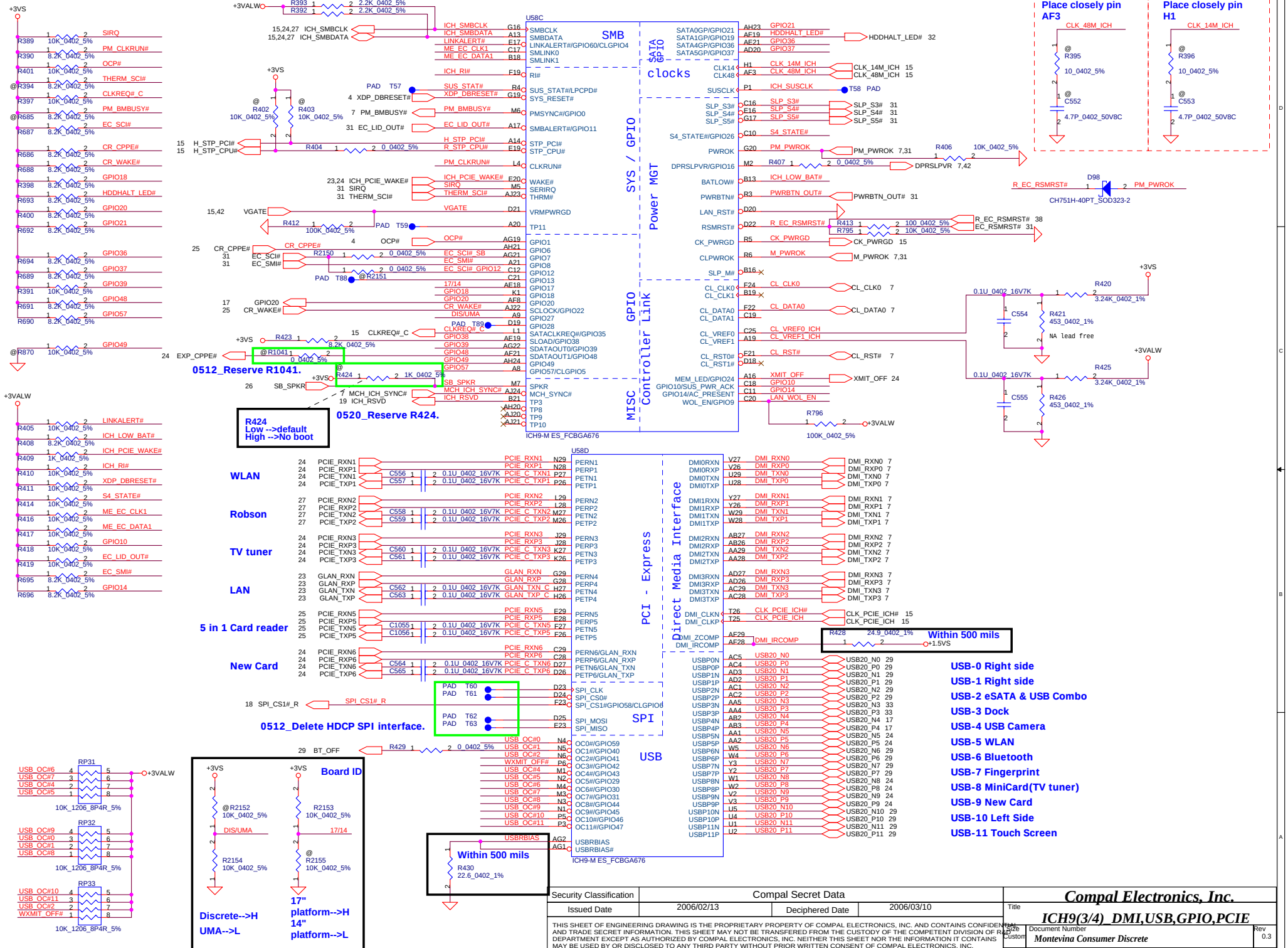
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

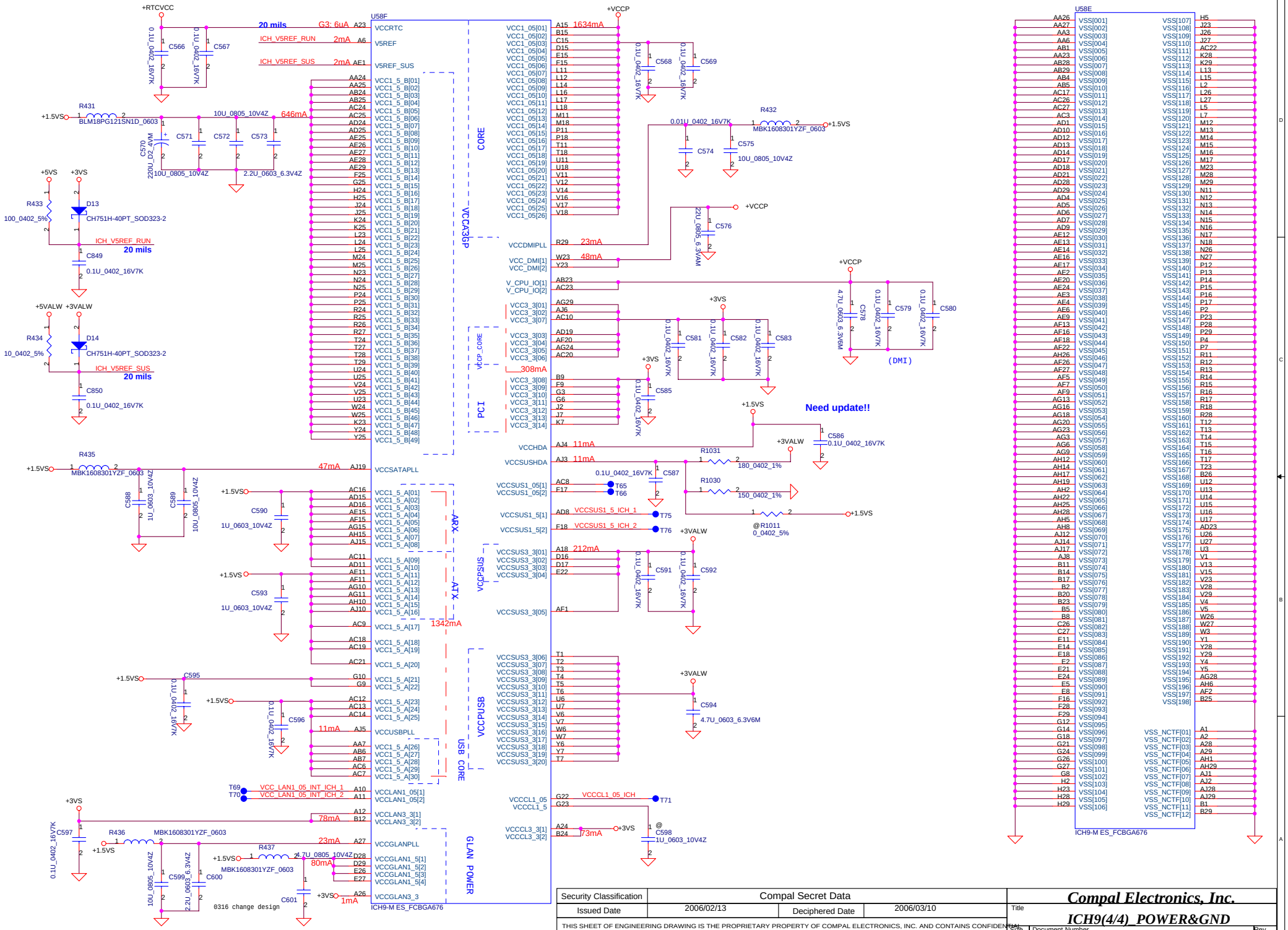
Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 19 of 44



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Title	*Compal Electronics, Inc.*		
	ICH9(3/4)_DMI,USB,GPIO,PCIE		
Size: Custom	Document Number: *Montevina Consumer Discrete*		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 20 of 44		



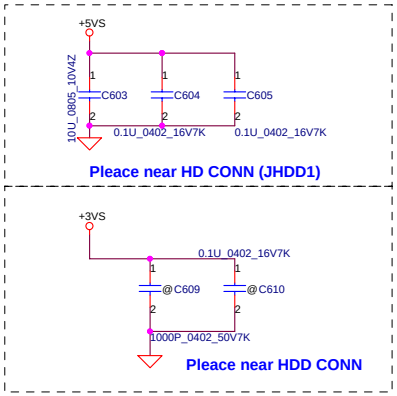
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

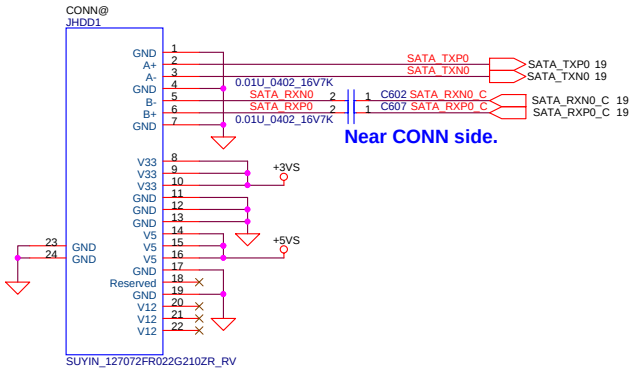
Compal Electronics, Inc.

Title: **ICH9(4/4)_POWER&GND**

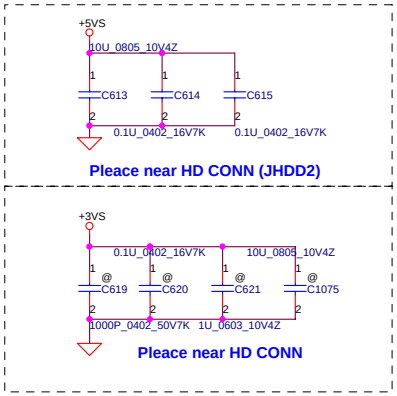
Size	Document Number	Rev
Custom	Montevina Consumer Discrete	0.3
Date: Friday, May 23, 2008	Sheet 21 of 44	

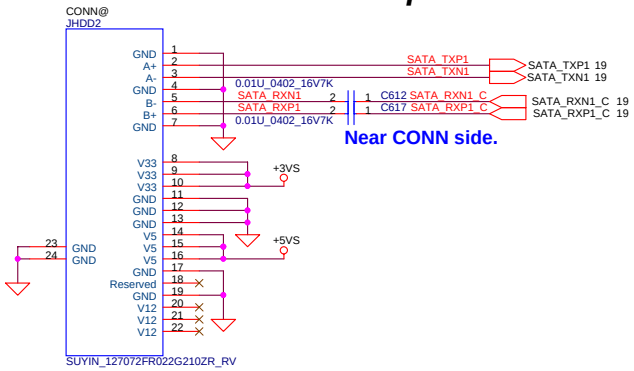
HDD Connector



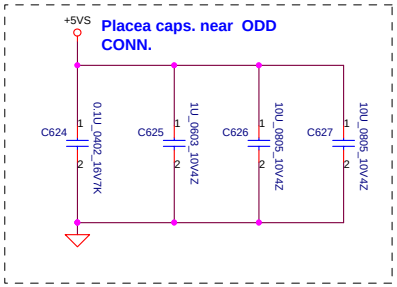


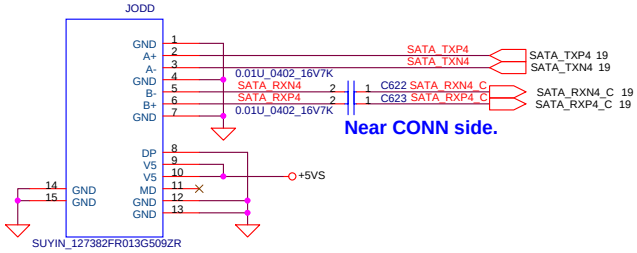
2nd HDD Connector-option





CD-ROM Connector





ZZZ1

PCB-MB

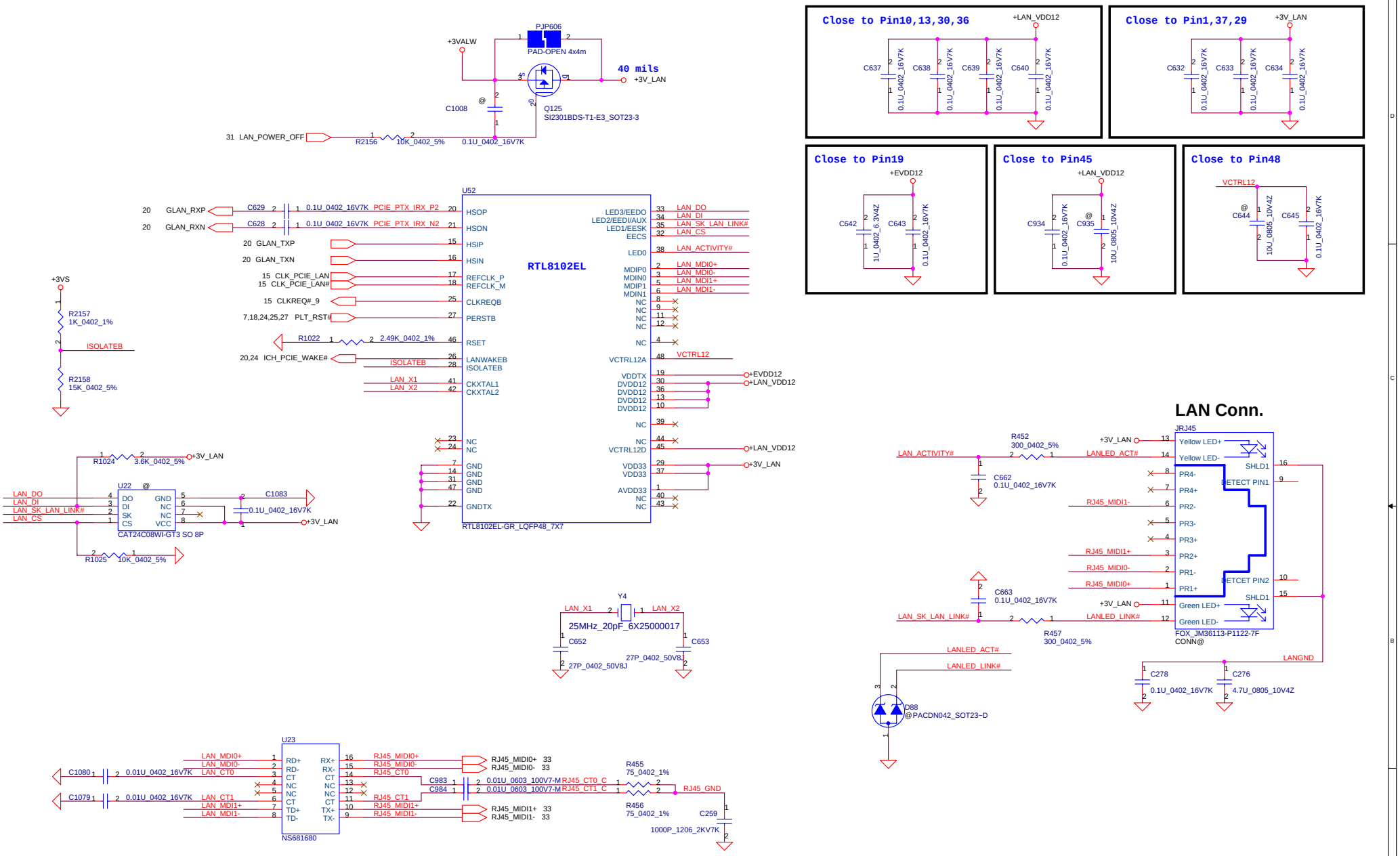
PCB 03W LA-4081P REV0 M/B UMA

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **HDD & CDROM**

Size: Custom	Document Number: *Montevina Consumer Discrete*	Rev: 0.3
Date: Friday, May 23, 2008	Sheet 22 of 44	



Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2007/06/30

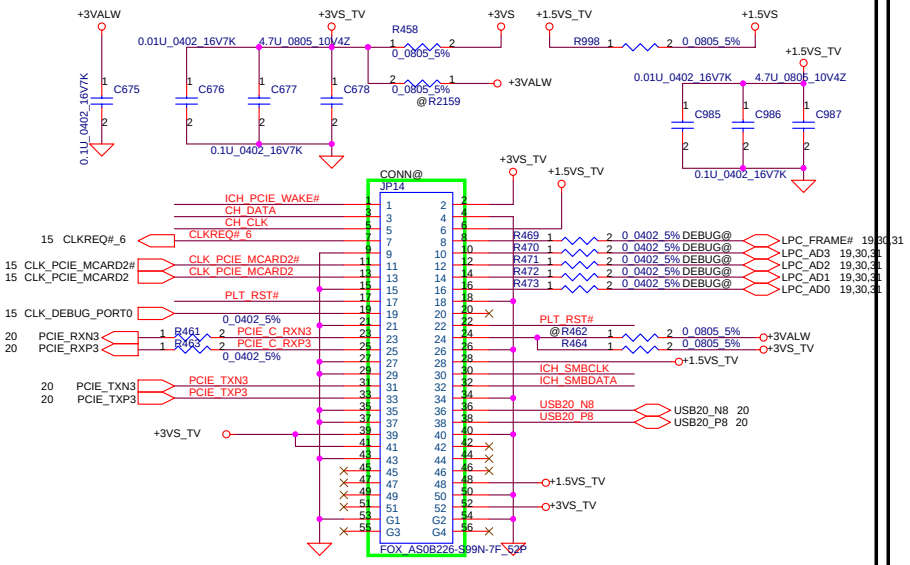
Compal Electronics, Inc.

Title: 88E8042 10/100 LAN

Size	Document Number	Rev
Custom	LA-4081P	0.3

Date: Friday, May 23, 2008 Sheet 23 of 44

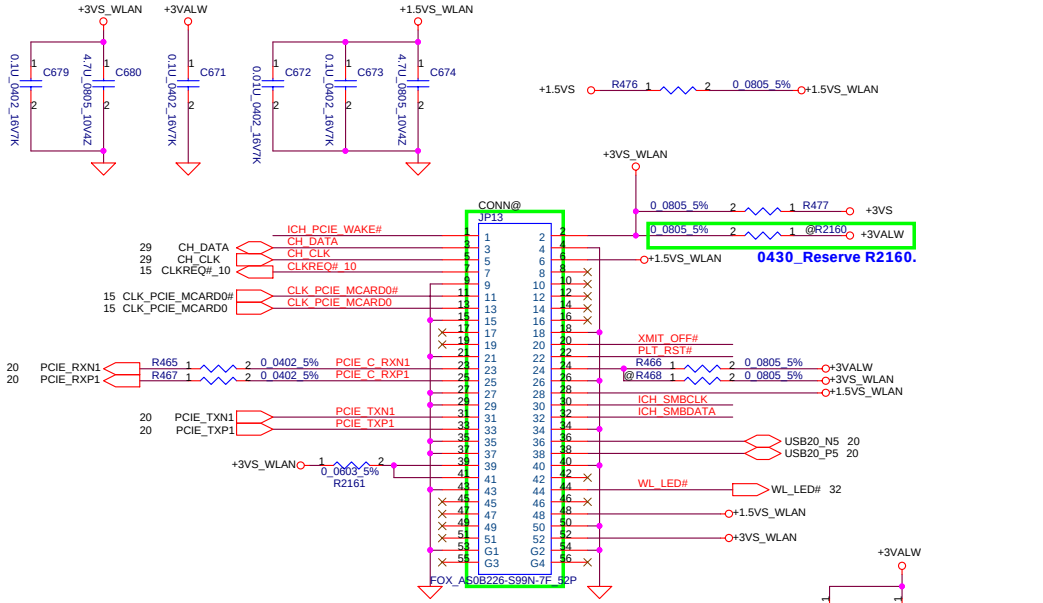
Mini Card 0--TV tuner



Follow 17" DIS.

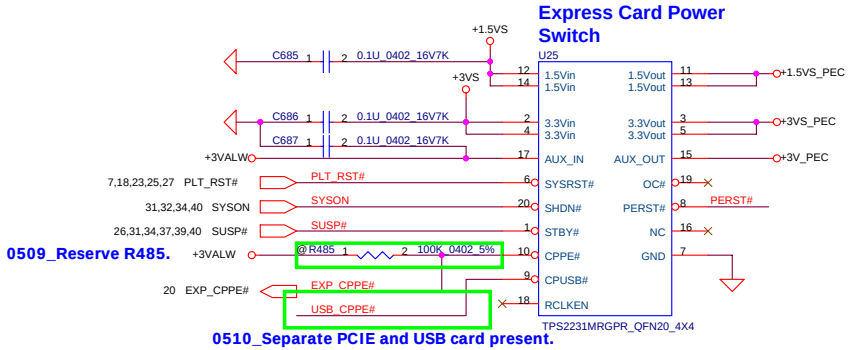
Power Rail	Voltage Tolerance	Primary Power		Auxiliary Power
		Peak (Max) mA	Normal (Max) mA	Normal (Max) mA
+3.3V	+/- 9%	1000	750	
3.3Vaux	+/- 9%	330	250	250 (Wake Enable) 5 (Wake Disable)
+1.5V	+/- 5%	500	375	N/A

Mini Card 2---WLAN



Follow 17" DIS.

New Card



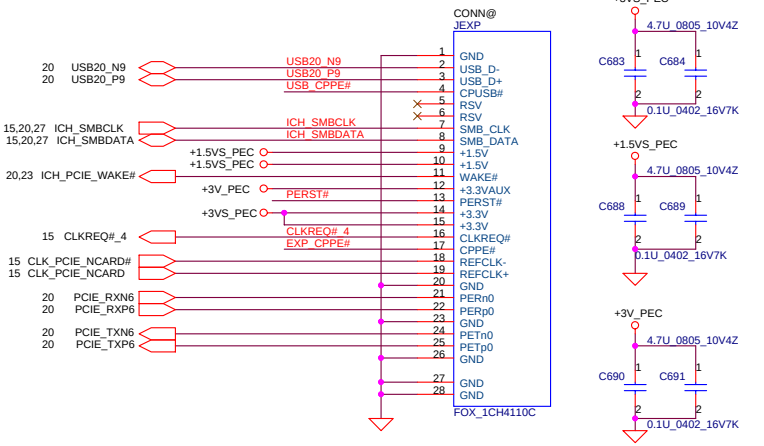
0509_Reserve R485.

0510_Separate PCIE and USB card present.

internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

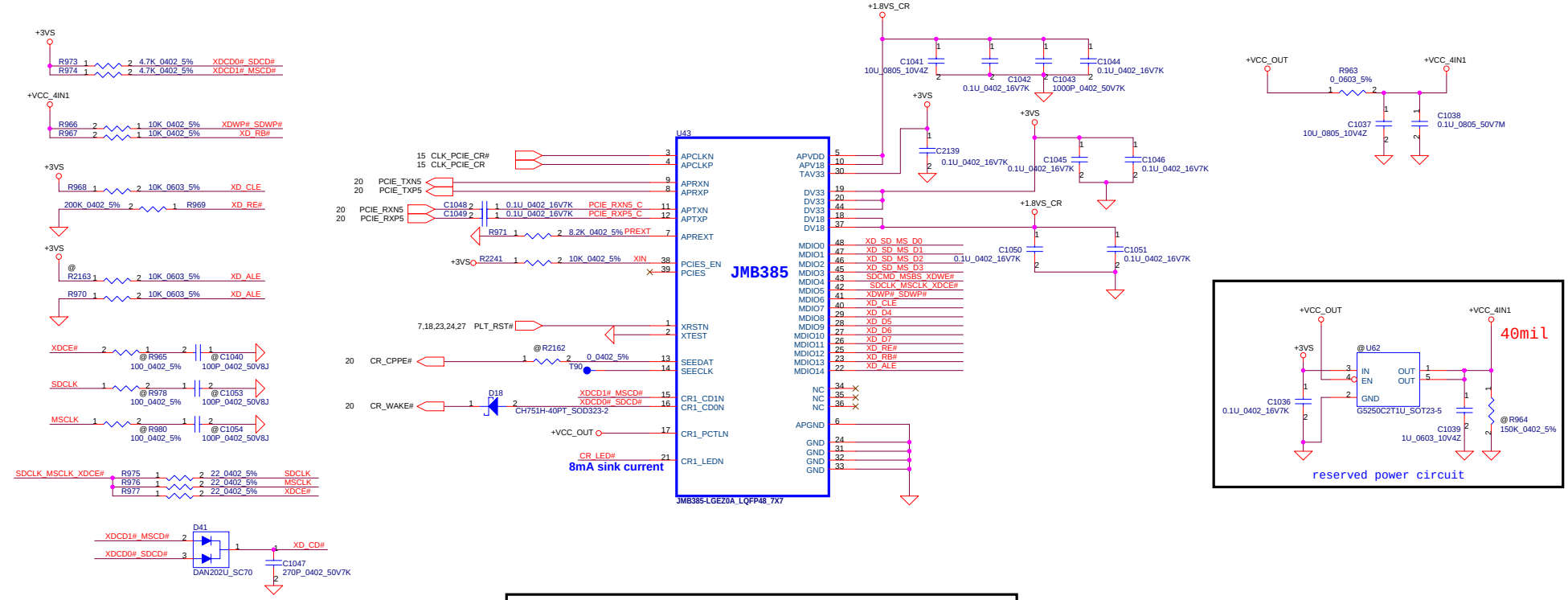
Follow 17" DIS.

Near to Express Card slot.

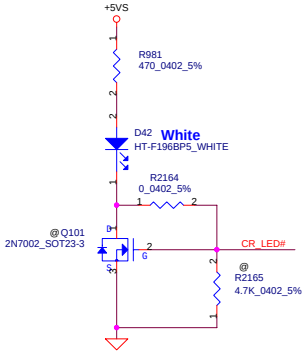


Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	WLAN, WWAN, New Card
Size	Document Number: Montevina Consumer Discrete
Rev	0.3
Date: Friday, May 23, 2008	Sheet 24 of 44

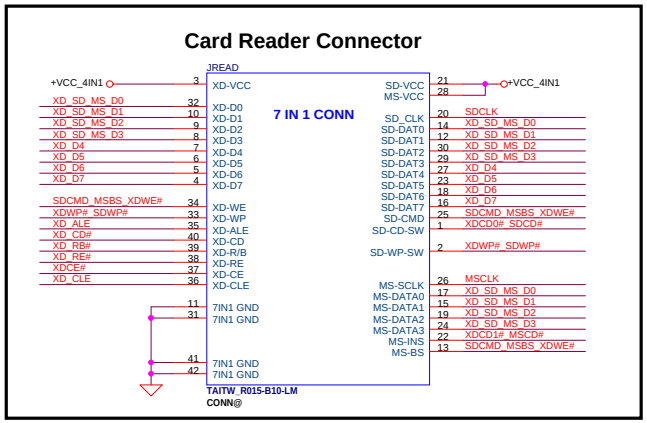


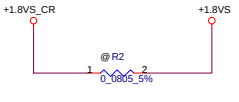
White LED: VF=3V, IF = 5mA, Res = 56ohm



01/03 Change Cardreader LED control

02/13 Direct driver LED





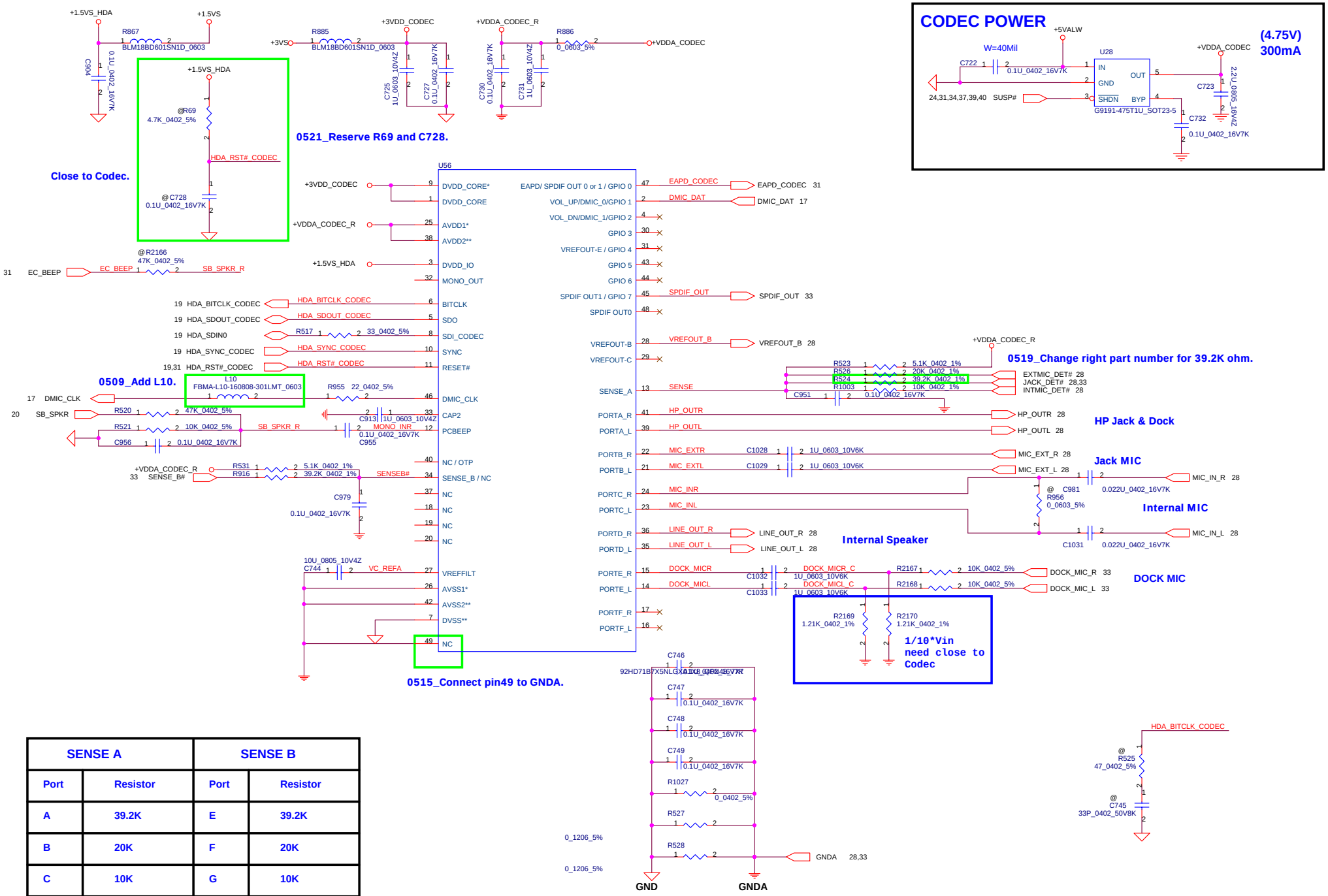
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: USB CardReader&CONN

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 25 of 44

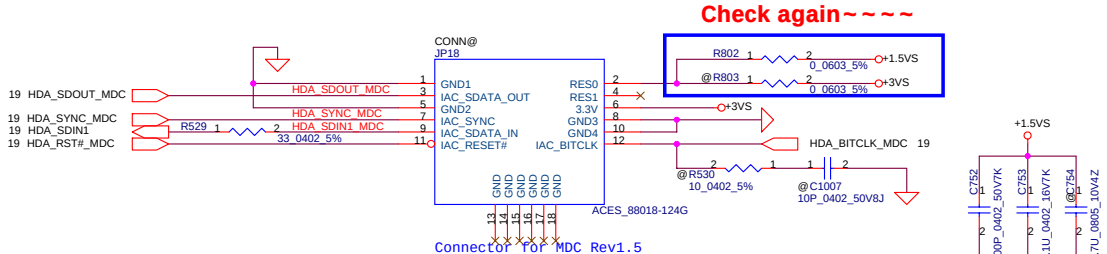


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

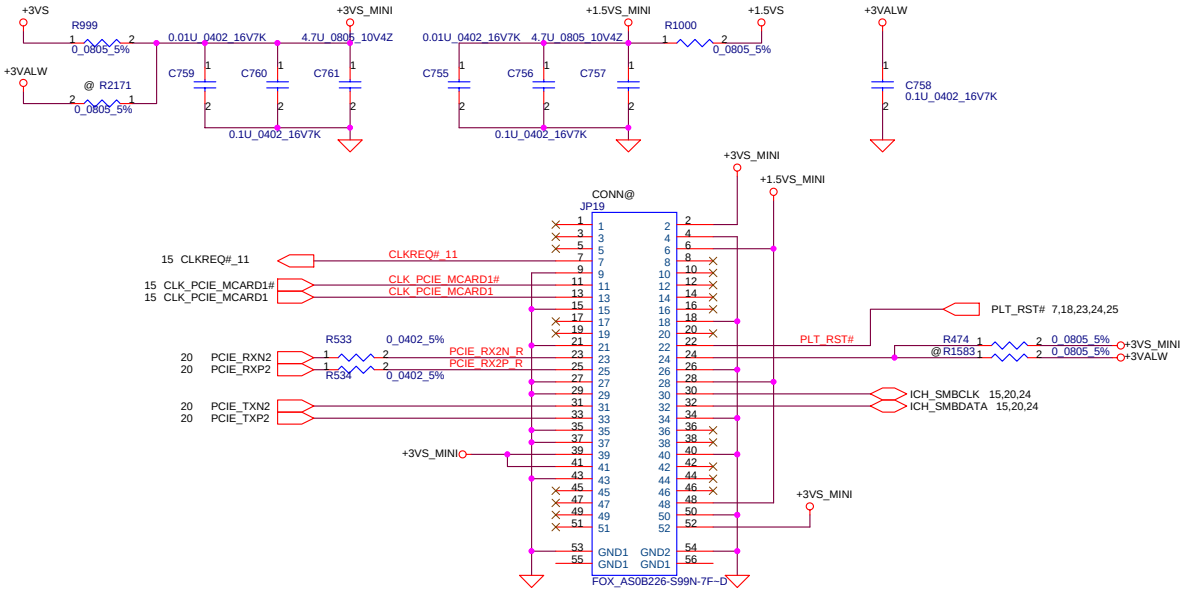
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

Title	Codec_IDT9271B7		
Size: Custom	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Monday, May 26, 2008	Sheet 26 of 44		

MDC 1.5 Conn.

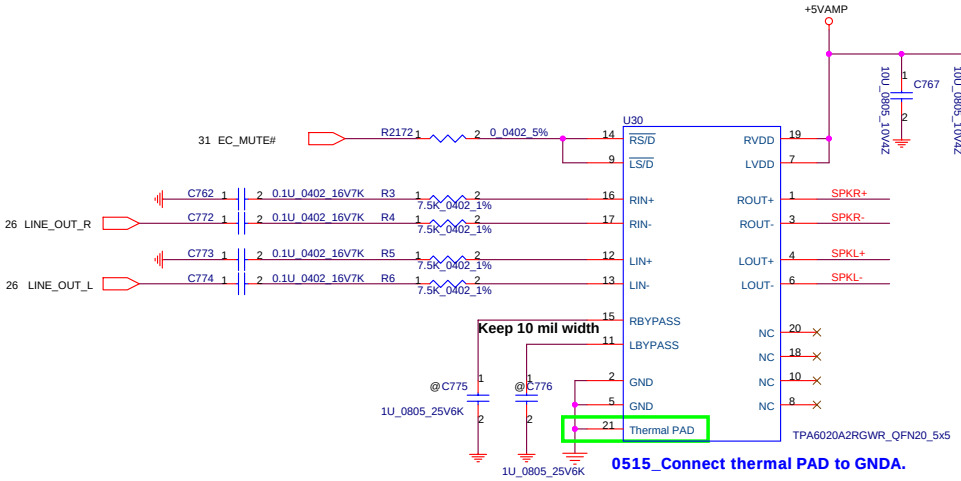


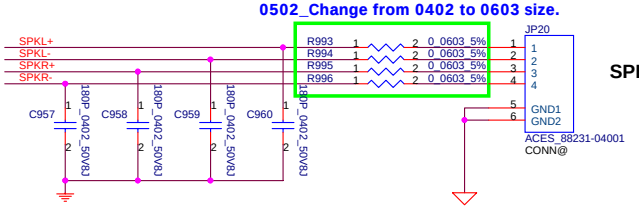
Mini Card 1---Robson



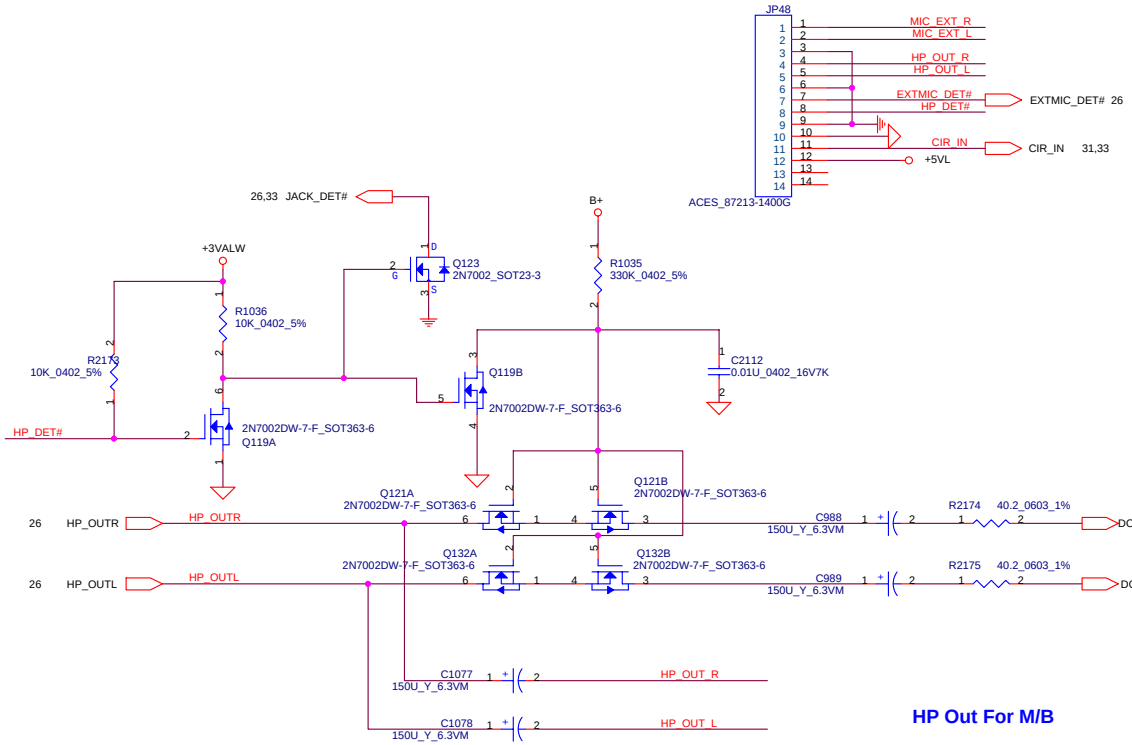
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: MDC 1.5 & Robson			
Size:	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 27 of 44		



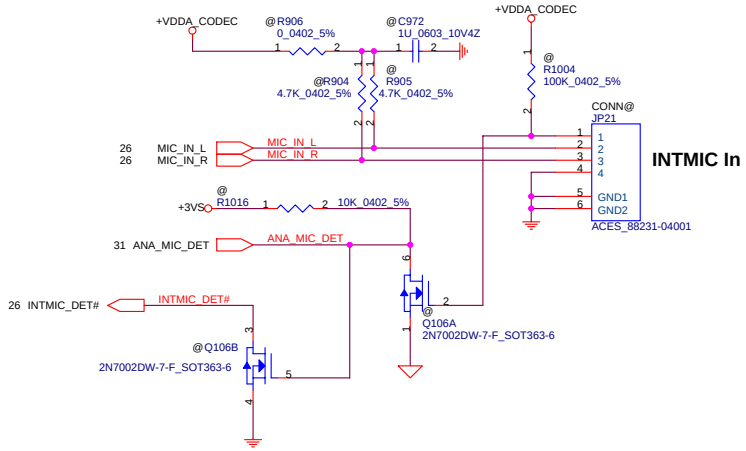


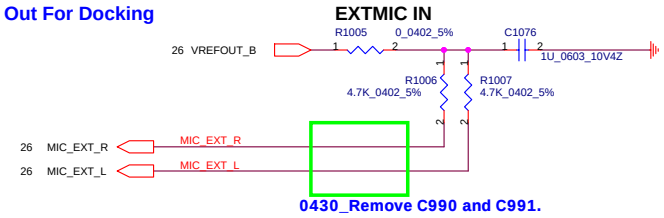
Audio & USB board conn



HP Out For Docking

HP Out For M/B

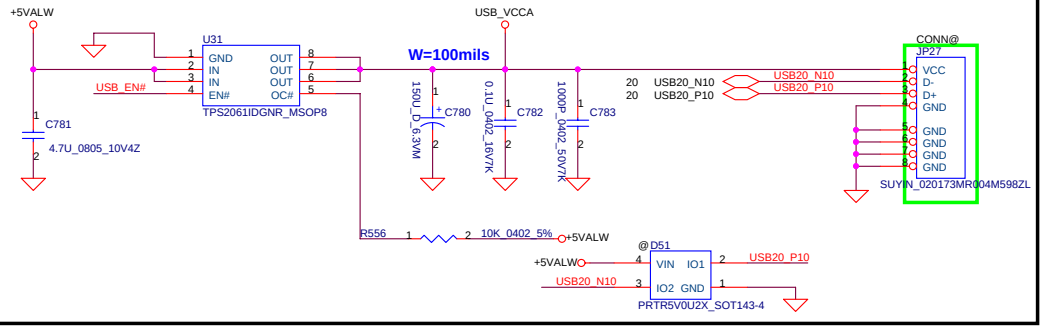




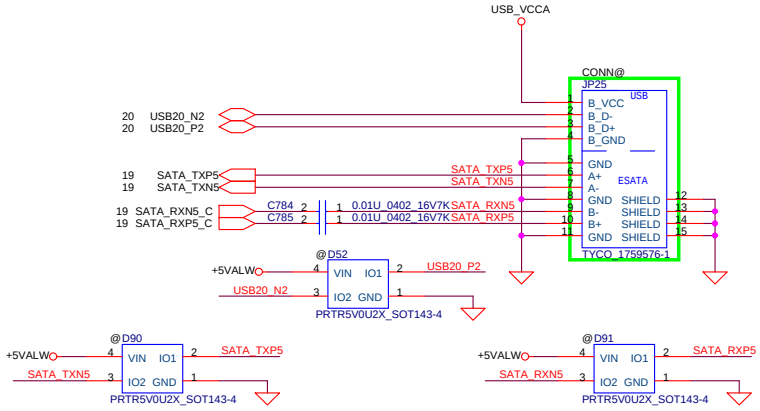
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

Title	AMP & Audio Jack		
Size: Custom	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Monday, May 26, 2008	Sheet 28 of 44		

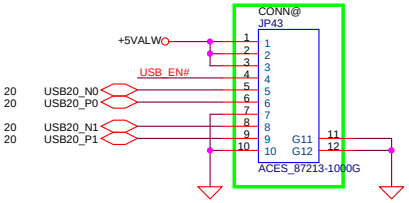
Left side USB CONNECTOR



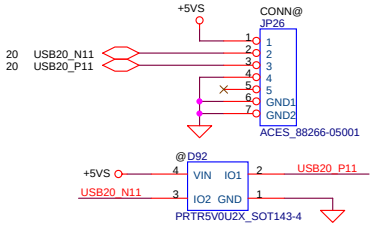
Left side eSATA/USB combination Connector



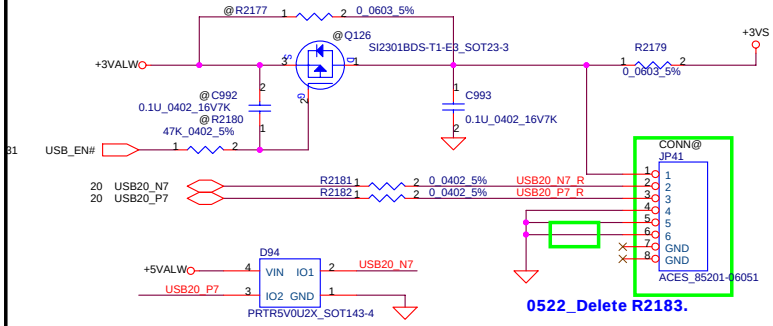
USB cable connector for Right side



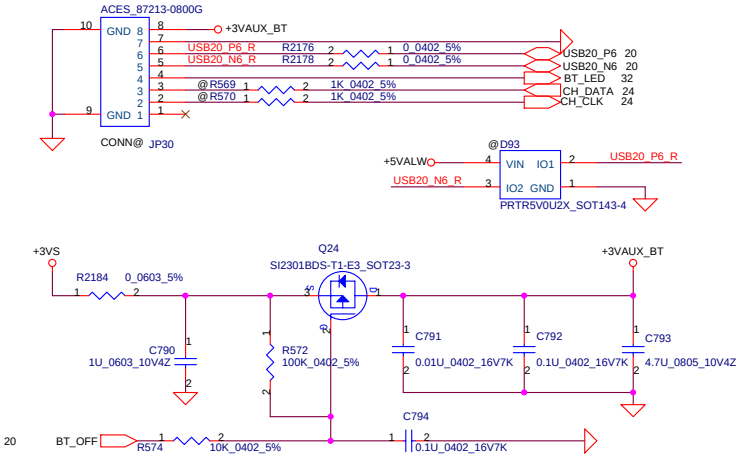
Touch screen connector



Finger printer

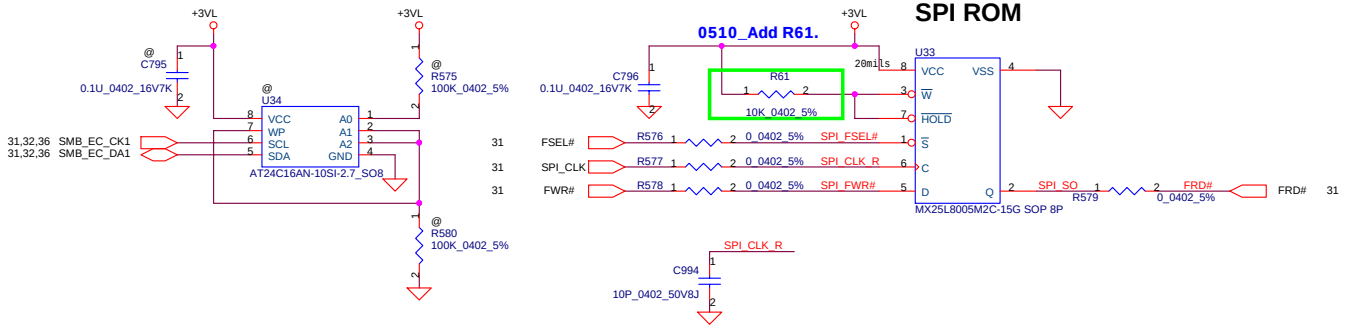


BT Connector



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

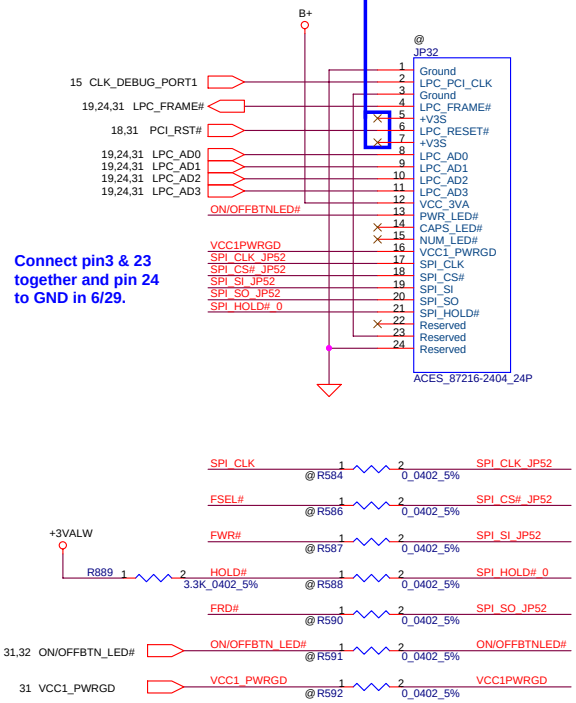
Compal Electronics, Inc.			
Title: USB, BT, eSATA			
Size	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 29 of 44		



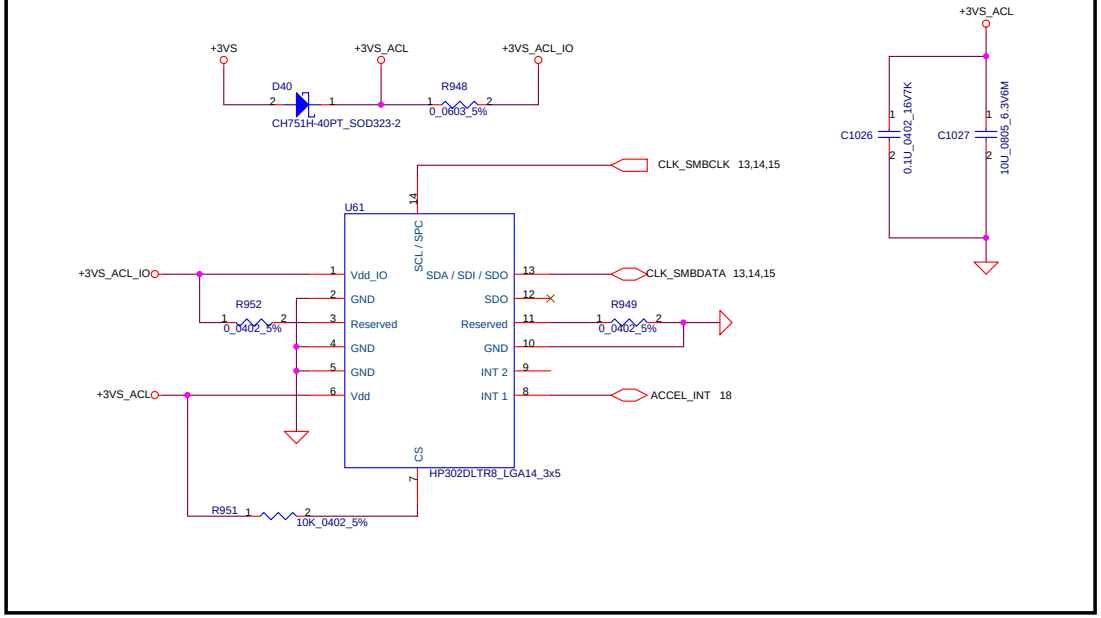
LPC debug port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13

Connect pin3 & 23 together and pin 24 to GND in 6/29.

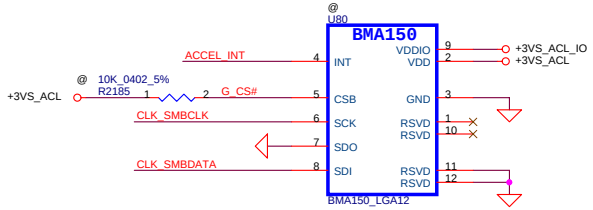


Acceleromter-1



Acceleromter-2

U61 & U80 must be close



HDCP ROM

0512_Remove HDCP SPI ROM.

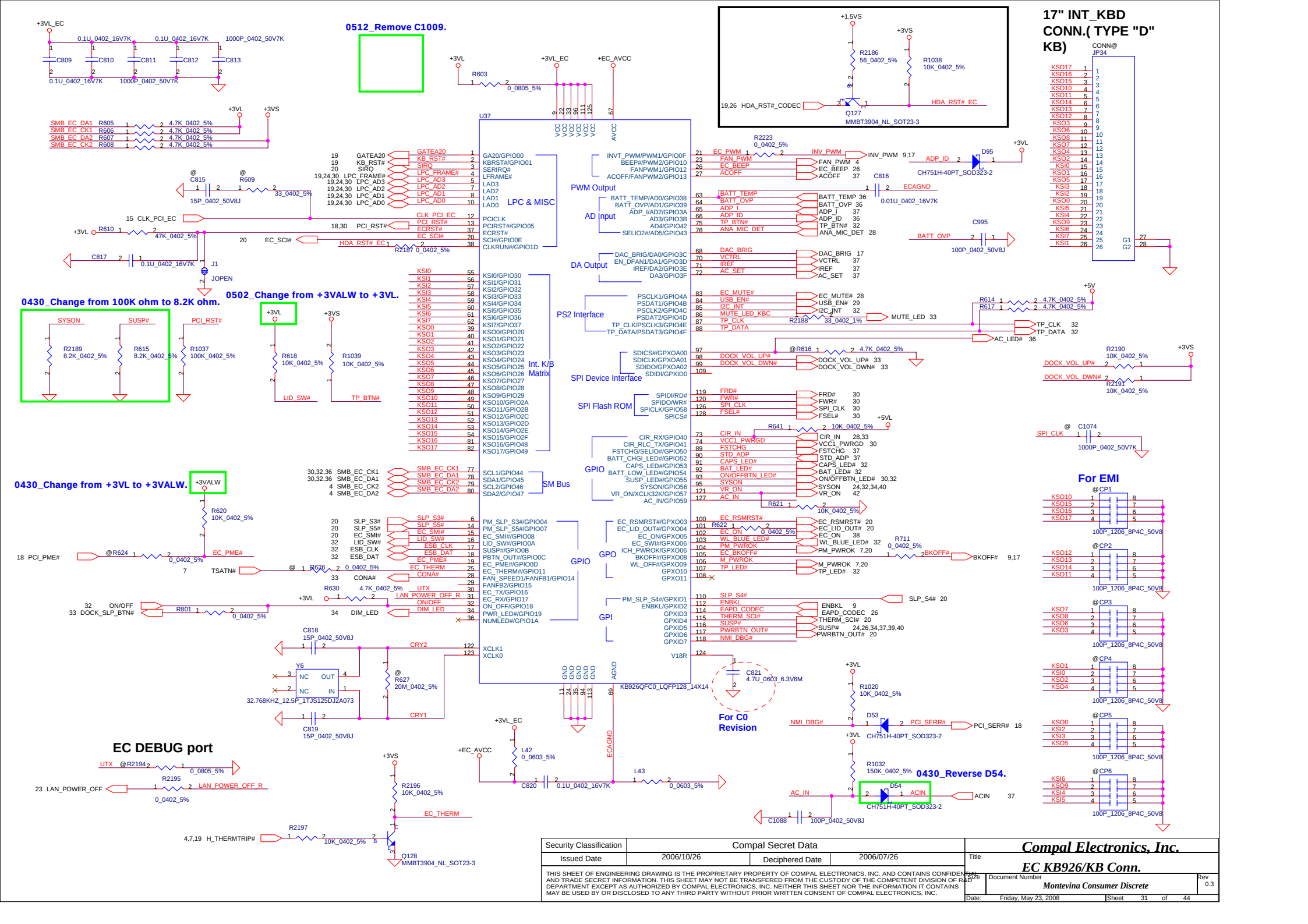
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

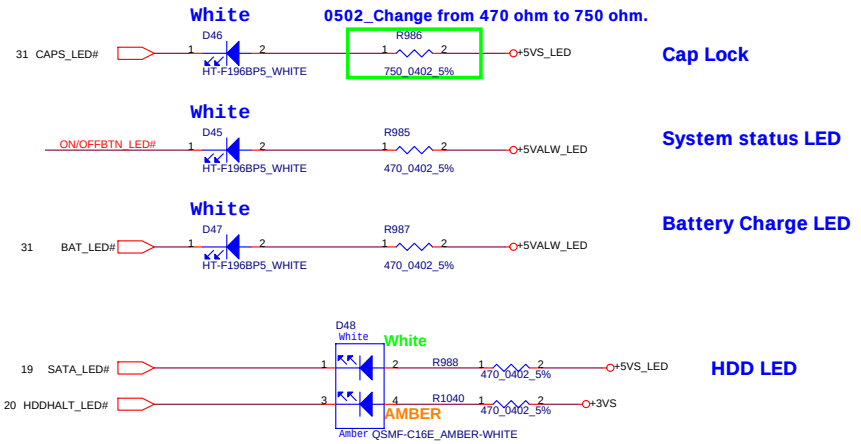
Title: BIOS ROM

Size | Document Number: Montevina Consumer Discrete | Rev: 0.3

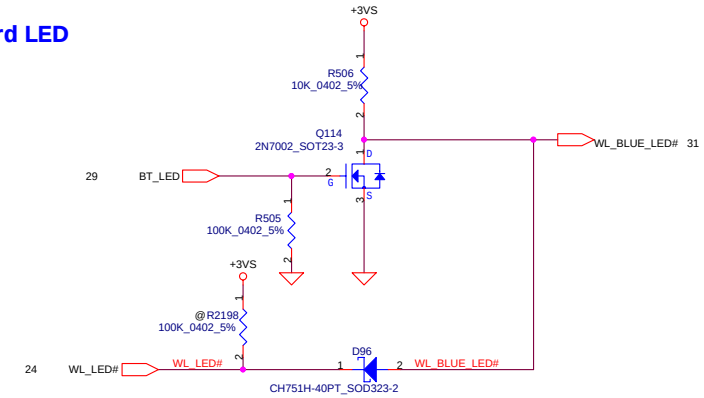
Date: Friday, May 23, 2008 | Sheet 30 of 44


0512_Remove C1009.
17" INT_KBD CONN.(TYPE "D" KB)
CONN@ JP34
0430_Change from 100K ohm to 8.2K ohm.
0502_Change from +3VALW to +3VL.
0430_Change from +3VL to +3VALW.
For EMI
For C0 Revision
EC DEBUG port
0430_Reverse D54.
U37
KB926QFC0_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Q127 MMBT3904_NL_SOT23-3
Q128 MMBT3904_NL_SOT23-3
JOPEN
Y6 32.768KHZ_12.5P_1TJS125DJ2A073
D95 CH751H-40PT_SOD323-2
D53 CH751H-40PT_SOD323-2
D54 CH751H-40PT_SOD323-2
Security Classification
Compal Secret Data
Issued Date
2006/10/26
Deciphered Date
2006/07/26
Compal Electronics, Inc.
EC KB926/KB Conn.
Document Number
Montevina Consumer Discrete
Rev
0.3
Date: Friday, May 23, 2008
Sheet 31 of 44

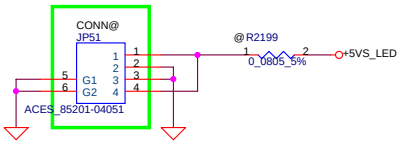
LED



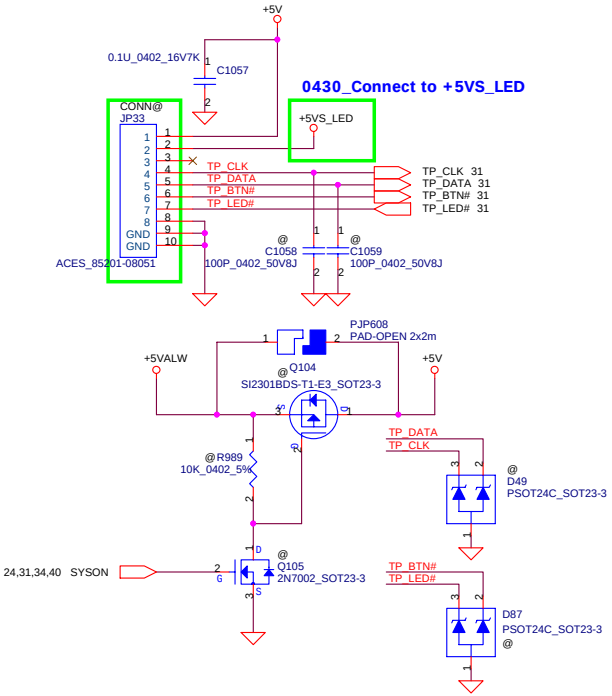
Mini-PCIE Card LED



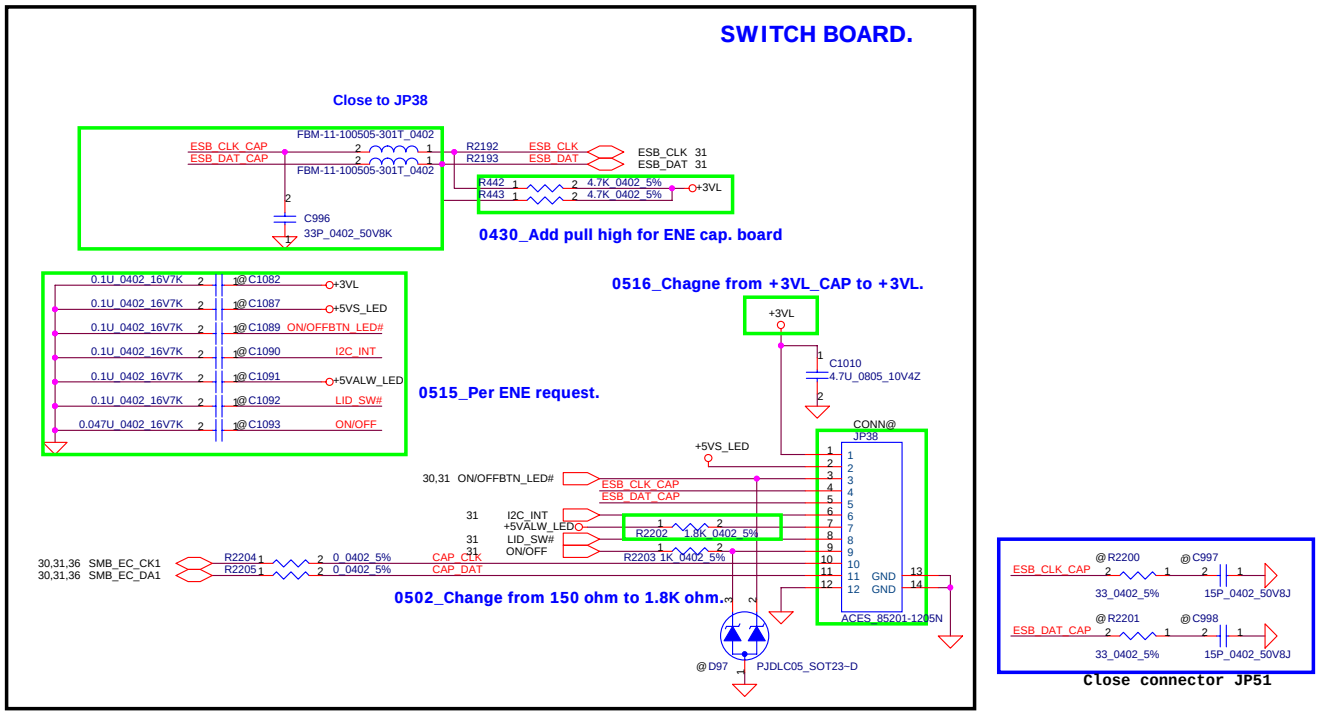
K/B backlight



T/P Board (Inculde T/P_ON/OFF)



SWITCH BOARD.



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

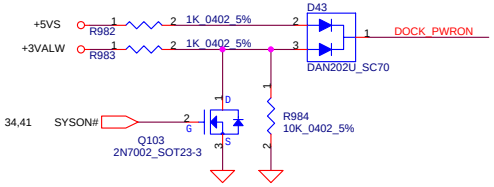
Title: KBD, ON/OFF, SW, CIR

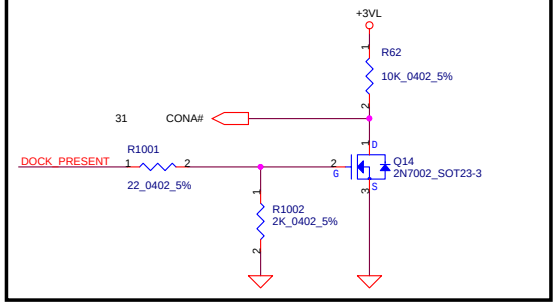
Size | Document Number: Montevina Consumer Discrete | Rev: 0.3

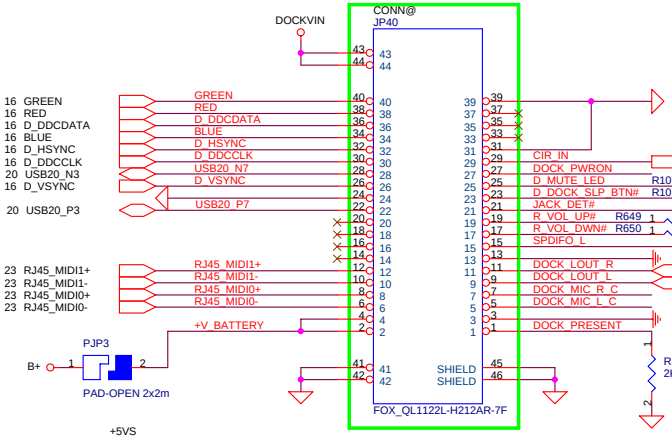
Date: Monday, May 26, 2008 | Sheet 32 of 44

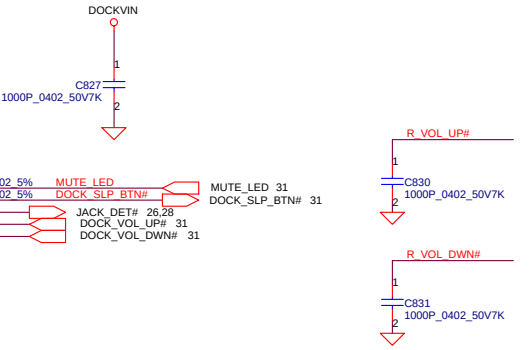
Atlas/ Saturn Dock

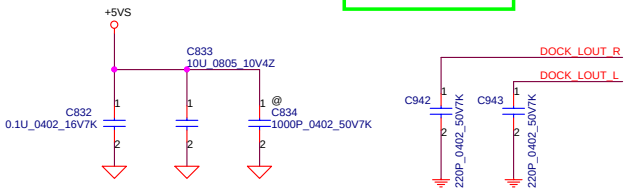
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

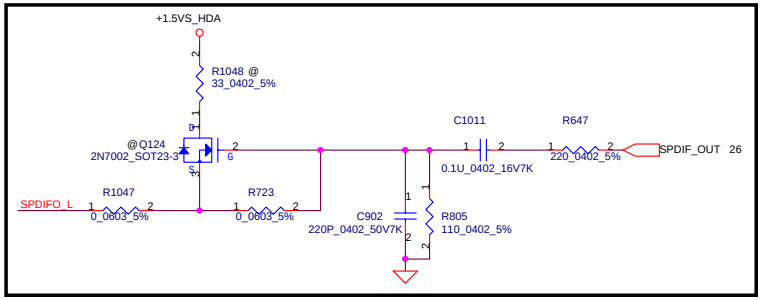


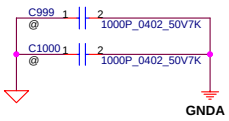




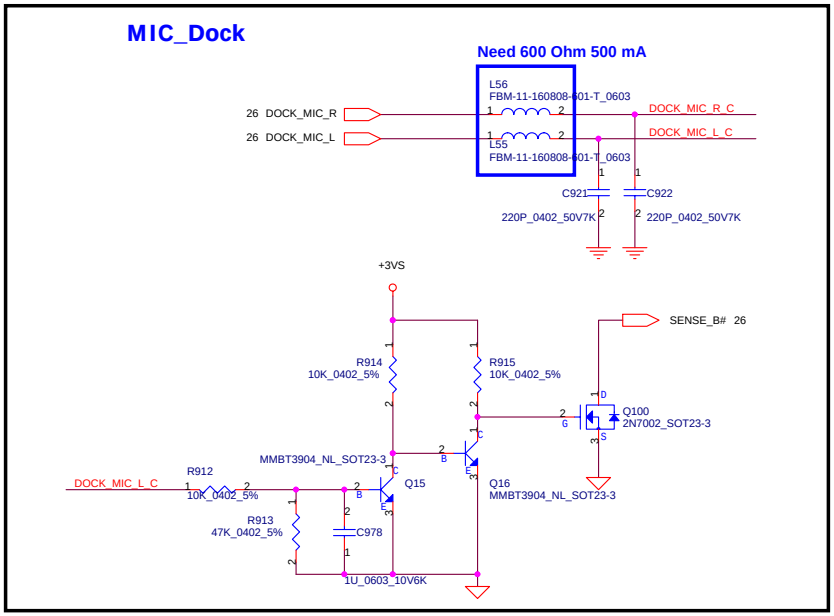








MIC_Dock



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **DOCK CONN.**

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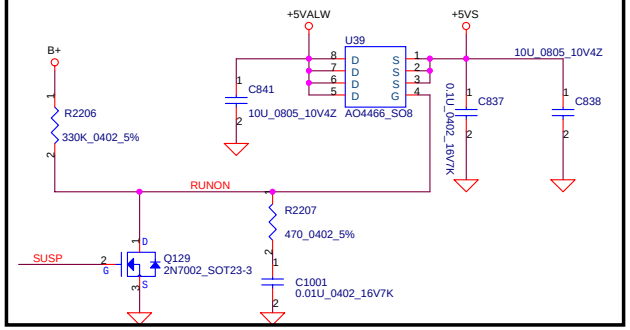
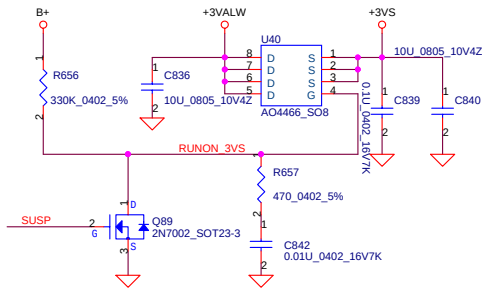
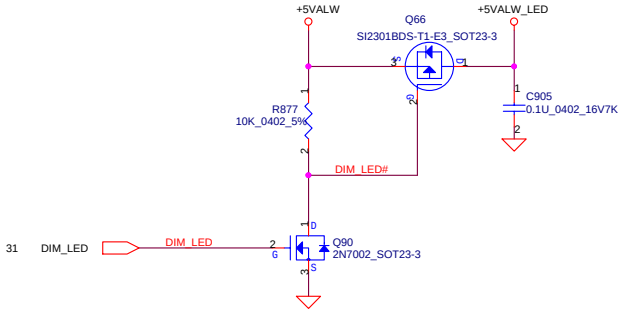
+5VALW to +5VS Transfer

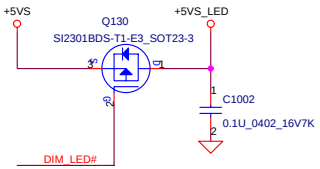


+3VALW to +3VS Transfer

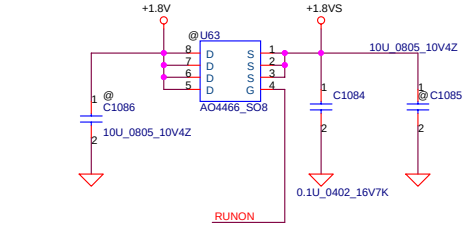


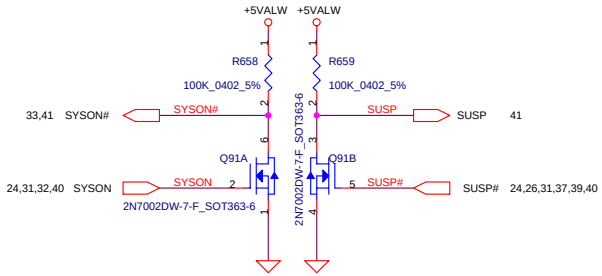
DIM LED





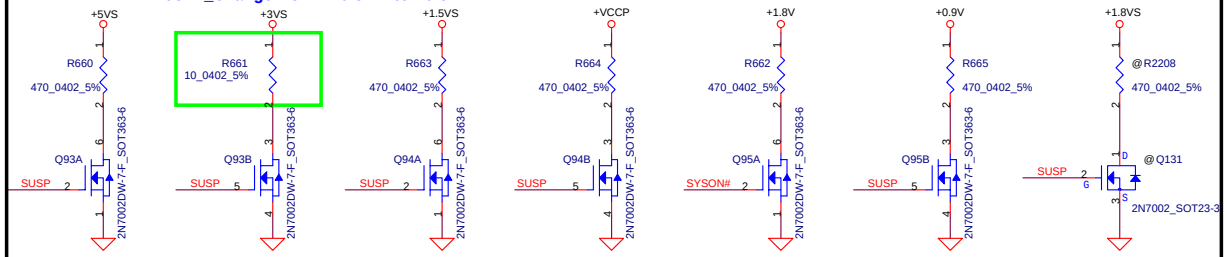
+1.8V to +1.8VS Transfer

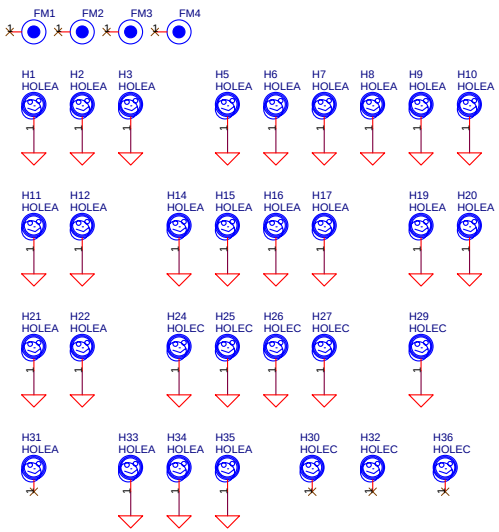




Discharge circuit

0512_Change from 470 ohm to 10 ohm.





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Title	*Compal Electronics, Inc.*		
	DC/DC Interface		
Size	Document Number		Rev
	Montevina Consumer Discrete		0.3
Date:	Friday, May 23, 2008	Sheet	34 of 44

EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommanded)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB

0512_change from 4.7K to 3.09K ohm.

0522_Add R712 and pull high to +3VS_LS.

0522_Change from STHDLS10QTR to STHDLS10TQTR.

0505_Reserve R45 for new HDMI level shifter.

0522_Stuff R45 and reserve Q102 and R563.

HDMI Connector

Internal pull down in STHDLS101.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: HDMI LS & Conn.

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

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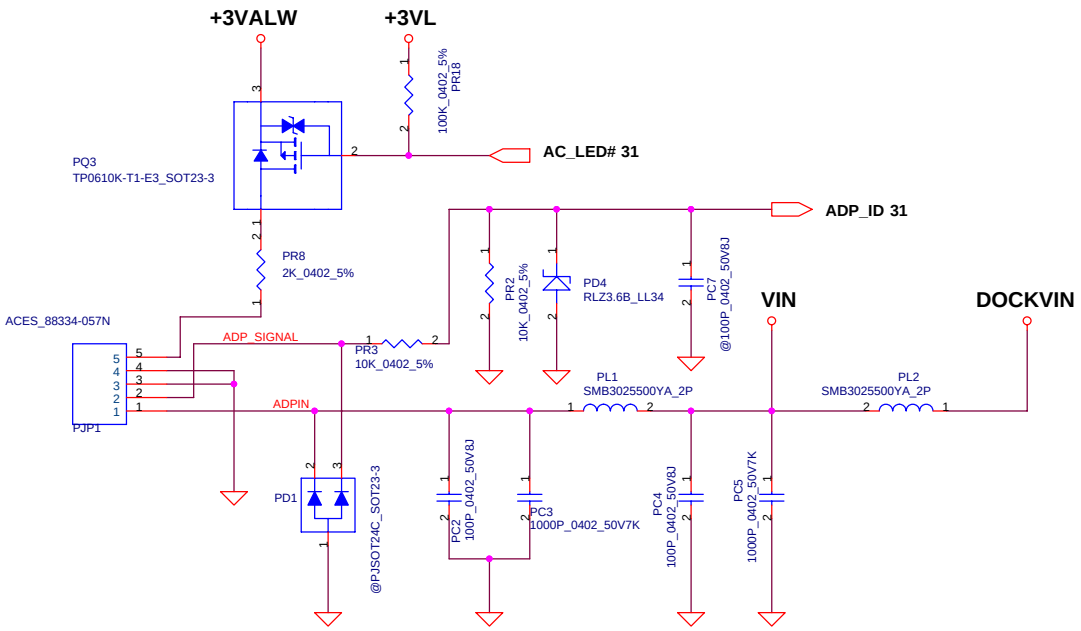
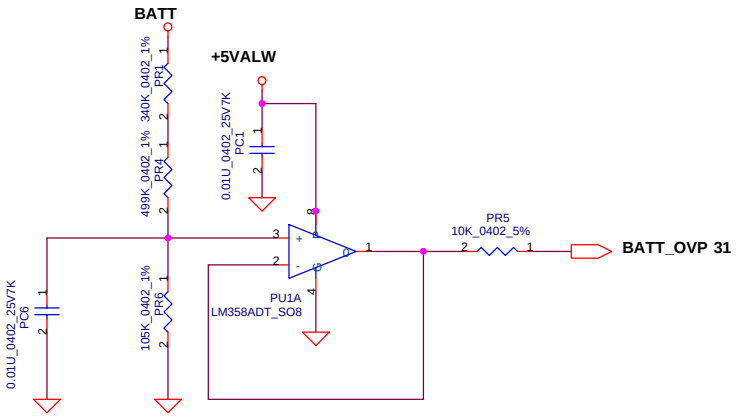
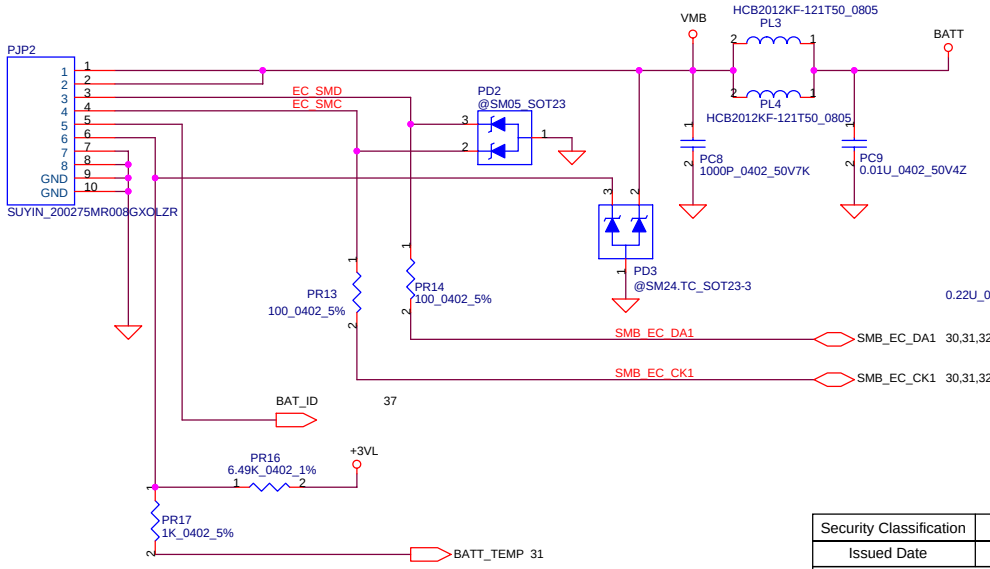
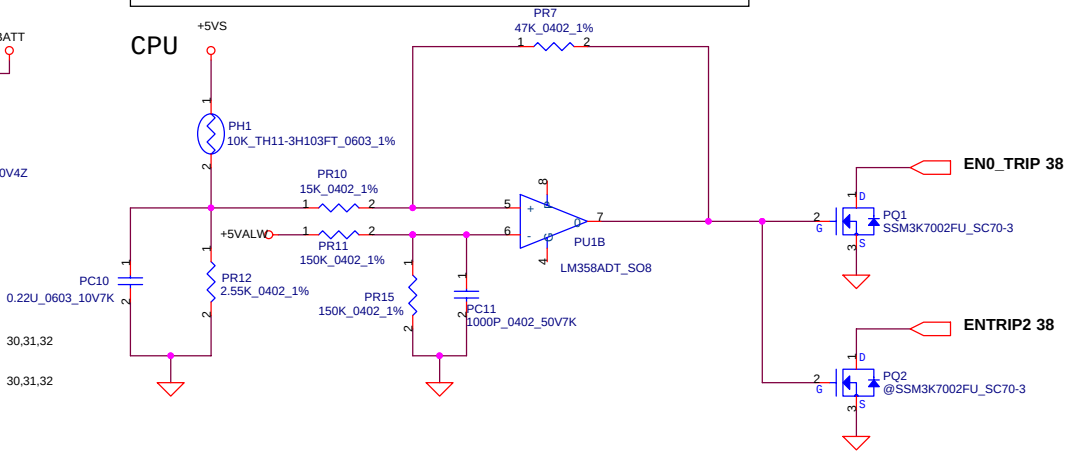




PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C





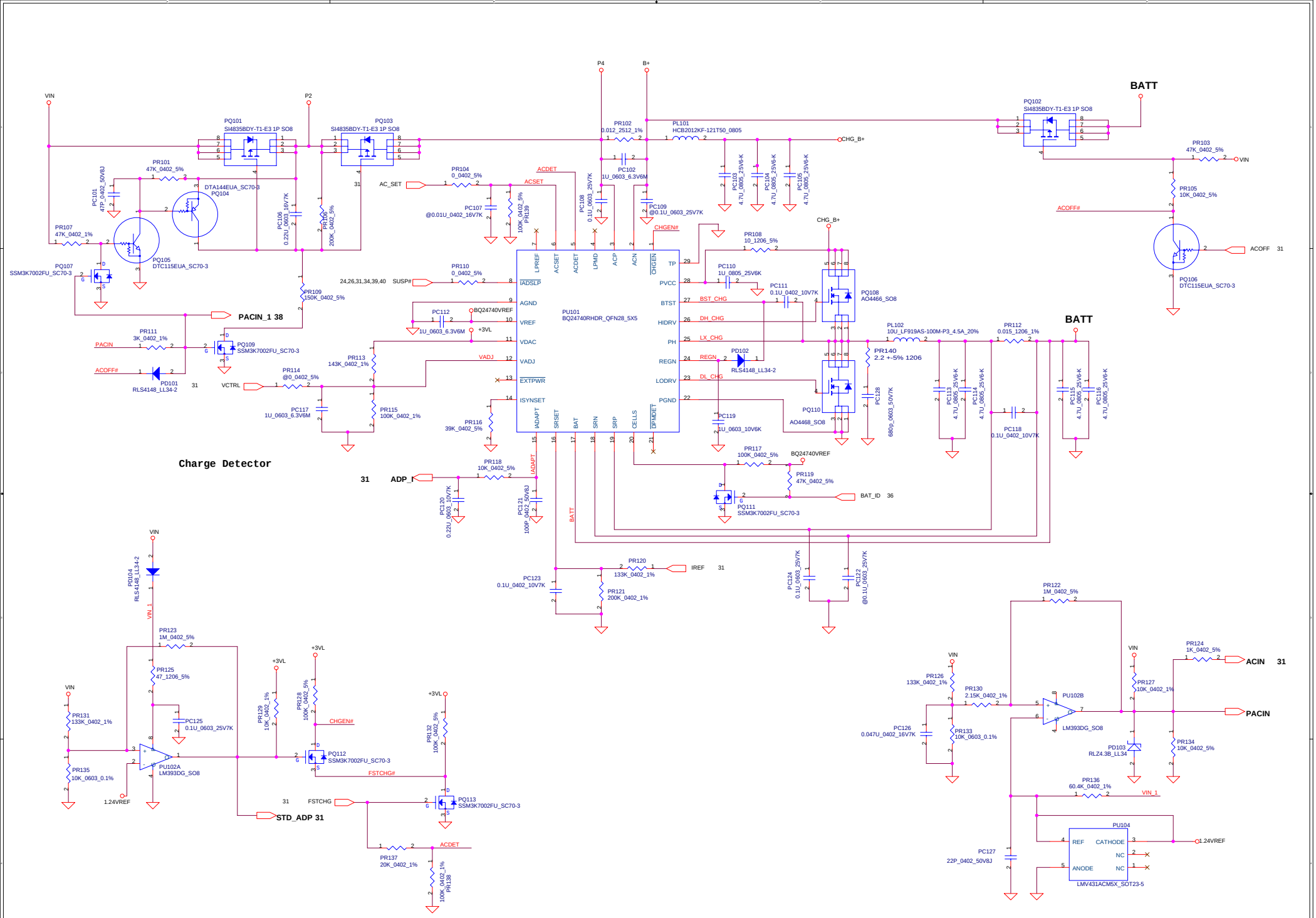
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

Size | Document Number: *Montevina Consumer Discrete* | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 36 of 44


Charge Detector
PU101
BQ24740RHDR_QFN28_5X5
PQ101
SI4835BDY-T1-E3 1P SO8
PQ102
SI4835BDY-T1-E3 1P SO8
PQ103
SI4835BDY-T1-E3 1P SO8
PL101
HC82012KF-121T50_0805
PL102
10U_LF919AS-100M-P3_4.5A_20%
PQ104
DTA144EUA_SC70-3
PQ105
DTC115EUA_SC70-3
PQ106
DTC115EUA_SC70-3
PQ107
SSM3K7002FU_SC70-3
PQ108
AO4466_SO8
PQ109
SSM3K7002FU_SC70-3
PQ110
AO4468_SO8
PQ111
SSM3K7002FU_SC70-3
PQ112
SSM3K7002FU_SC70-3
PQ113
SSM3K7002FU_SC70-3
PD101
RLS4148_LL34-2
PD102
RLS4148_LL34-2
PD103
RLZ4.3B_LL34
PD104
RLS4148_LL34-2
PU102A
LM393DG_SO8
PU102B
LM393DG_SO8
PU104
LMV431ACM5X_SOT23-5
VIN
P2
P4
B+
BATT
CHG_B+
ACOFF
ACOFF#
PACIN_1
PACIN
VCTRL
AC_SET
SUSP#
ADP_I
IREF
BAT_ID
STD_ADP
FSTCHG
1.24VREF
+3VL
BQ24740VREF
CHGEN#
ACDET
VIN_1
FSTCHG#
PR101 47K_0402_5%
PR102 0.012_2512_1%
PR103 47K_0402_5%
PR104 0_0402_5%
PR105 10K_0402_5%
PR106 200K_0402_5%
PR107 47K_0402_1%
PR108 10_1206_5%
PR109 150K_0402_5%
PR110 0_0402_5%
PR111 3K_0402_1%
PR112 0.015_1206_1%
PR113 143K_0402_1%
PR114 @0_0402_5%
PR115 100K_0402_1%
PR116 39K_0402_5%
PR117 100K_0402_5%
PR118 10K_0402_5%
PR119 47K_0402_5%
PR120 133K_0402_1%
PR121 200K_0402_1%
PR122 1M_0402_5%
PR123 1M_0402_5%
PR124 1K_0402_5%
PR125 47_1206_5%
PR126 133K_0402_1%
PR127 10K_0402_1%
PR128 100K_0402_5%
PR129 10K_0402_1%
PR130 2.15K_0402_1%
PR131 133K_0402_1%
PR132 100K_0402_5%
PR133 10K_0603_0.1%
PR134 10K_0402_5%
PR135 10K_0603_0.1%
PR136 60.4K_0402_1%
PR137 20K_0402_1%
PR138 100K_0402_1%
PR139 100K_0402_5%
PR140 2.2 +-5% 1206
PC101 47P_0402_50V8J
PC102 1U_0603_6.3V6M
PC103 4.7U_0805_25V6-K
PC104 4.7U_0805_25V6-K
PC105 4.7U_0805_25V6-K
PC106 0.22U_0603_16V7K
PC107 @0.01U_0402_16V7K
PC108 0.1U_0603_25V7K
PC109 @0.1U_0603_25V7K
PC110 1U_0805_25V6K
PC111 0.1U_0402_10V7K
PC112 1U_0603_6.3V6M
PC113 4.7U_0805_25V6-K
PC114 4.7U_0805_25V6-K
PC115 4.7U_0805_25V6-K
PC116 4.7U_0805_25V6-K
PC117 1U_0603_6.3V6M
PC118 0.1U_0402_10V7K
PC119 1U_0603_10V6K
PC120 0.22U_0603_10V7K
PC121 100P_0402_50V8J
PC122 @0.1U_0603_25V7K
PC123 0.1U_0402_10V7K
PC124 0.1U_0603_25V7K
PC125 0.1U_0603_25V7K
PC126 0.047U_0402_16V7K
PC127 22P_0402_50V8J
PC128 680p_0603_50V7K
LPREF
ACSET
ACDET
LPMD
ACP
ACN
CHGEN
IADSLP
AGND
VREF
VDAC
VADJ
EXTPWR
ISYNSET
IADAPT
SRSET
BAT
SRN
SRP
CELLS
DPMDET
TP
PVCC
BTST
HIDRV
PH
REGN
LODRV
PGND
BST_CHG
DH_CHG
LX_CHG
DL_CHG
REF
CATHODE
ANODE
NC
Security Classification
Compal Secret Data
Issued Date
2007/05/29
Deciphered Date
2008/05/29
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Compal Electronics, Inc.
Title
Charger
Size
Document Number
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0.3
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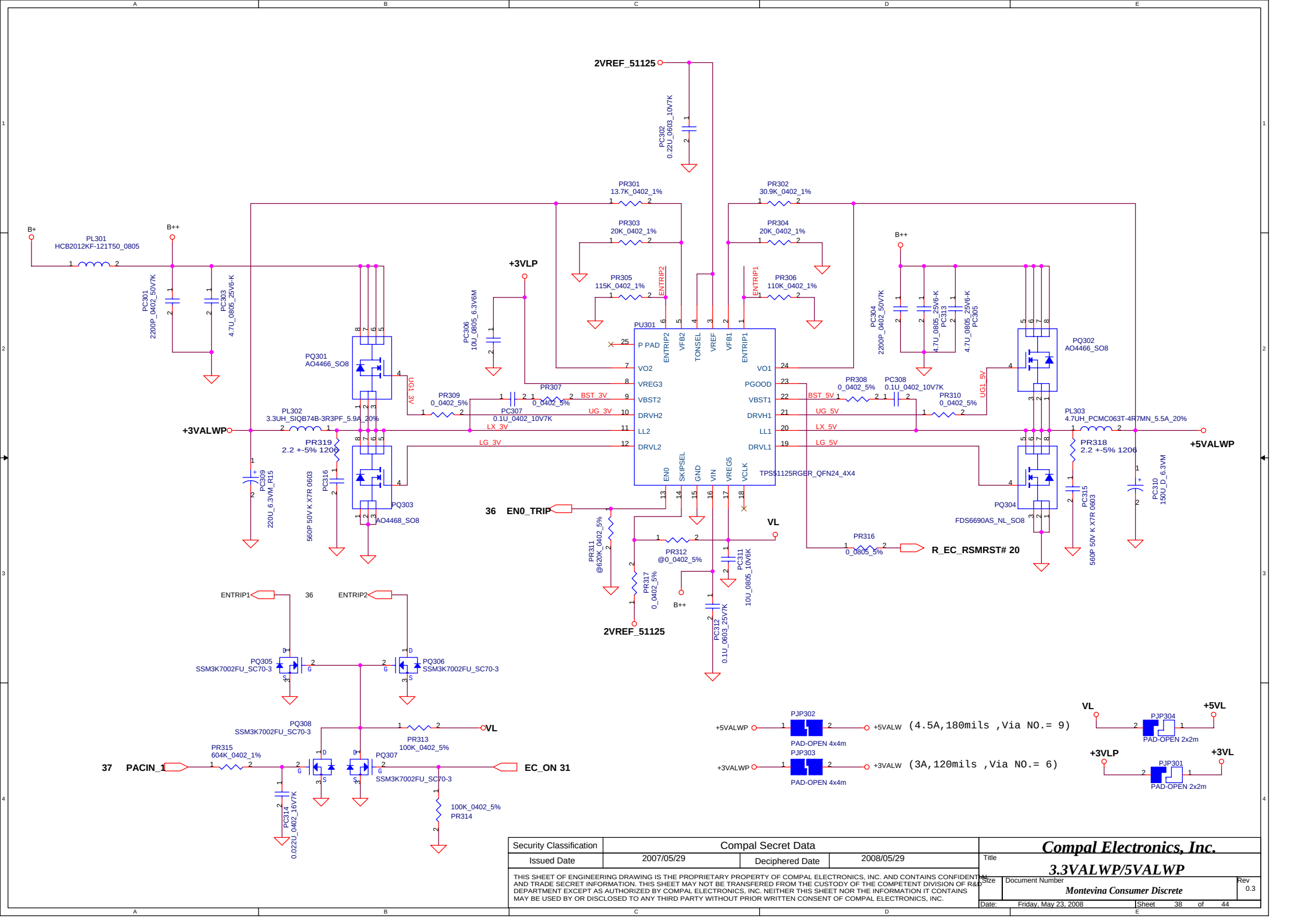

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size | Document Number: *Montevina Consumer Discrete* | Rev: 0.3

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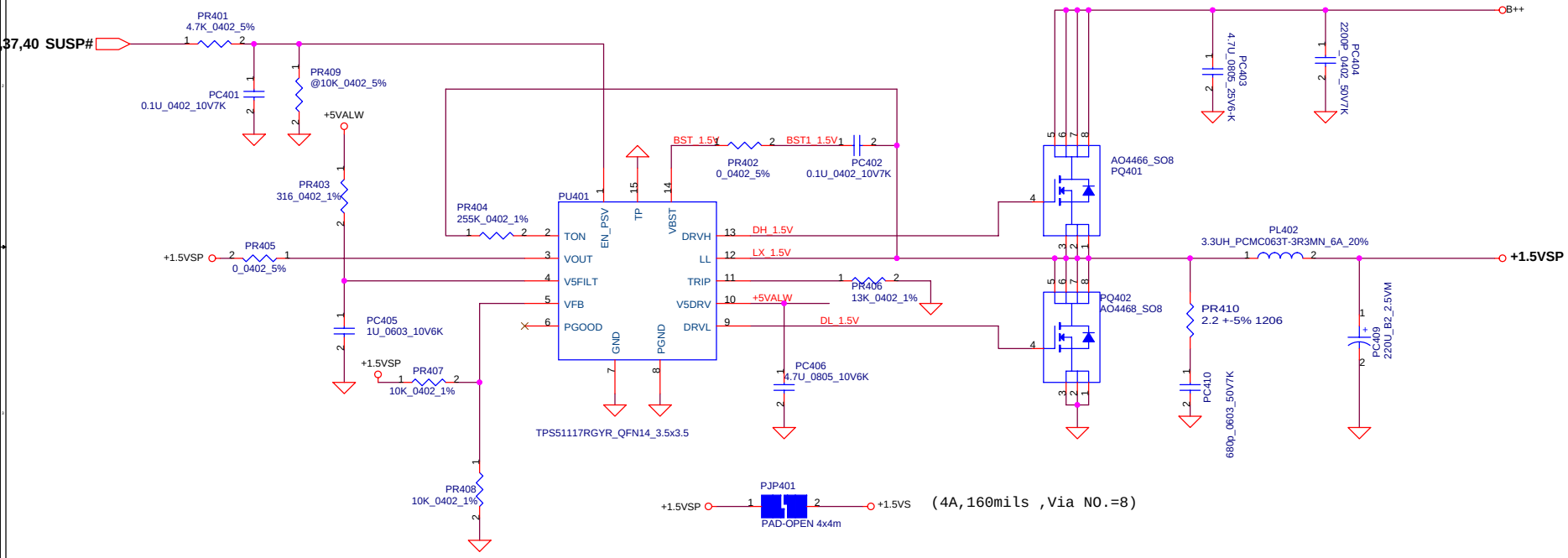

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.5VSP**

Size	Document Number	Rev
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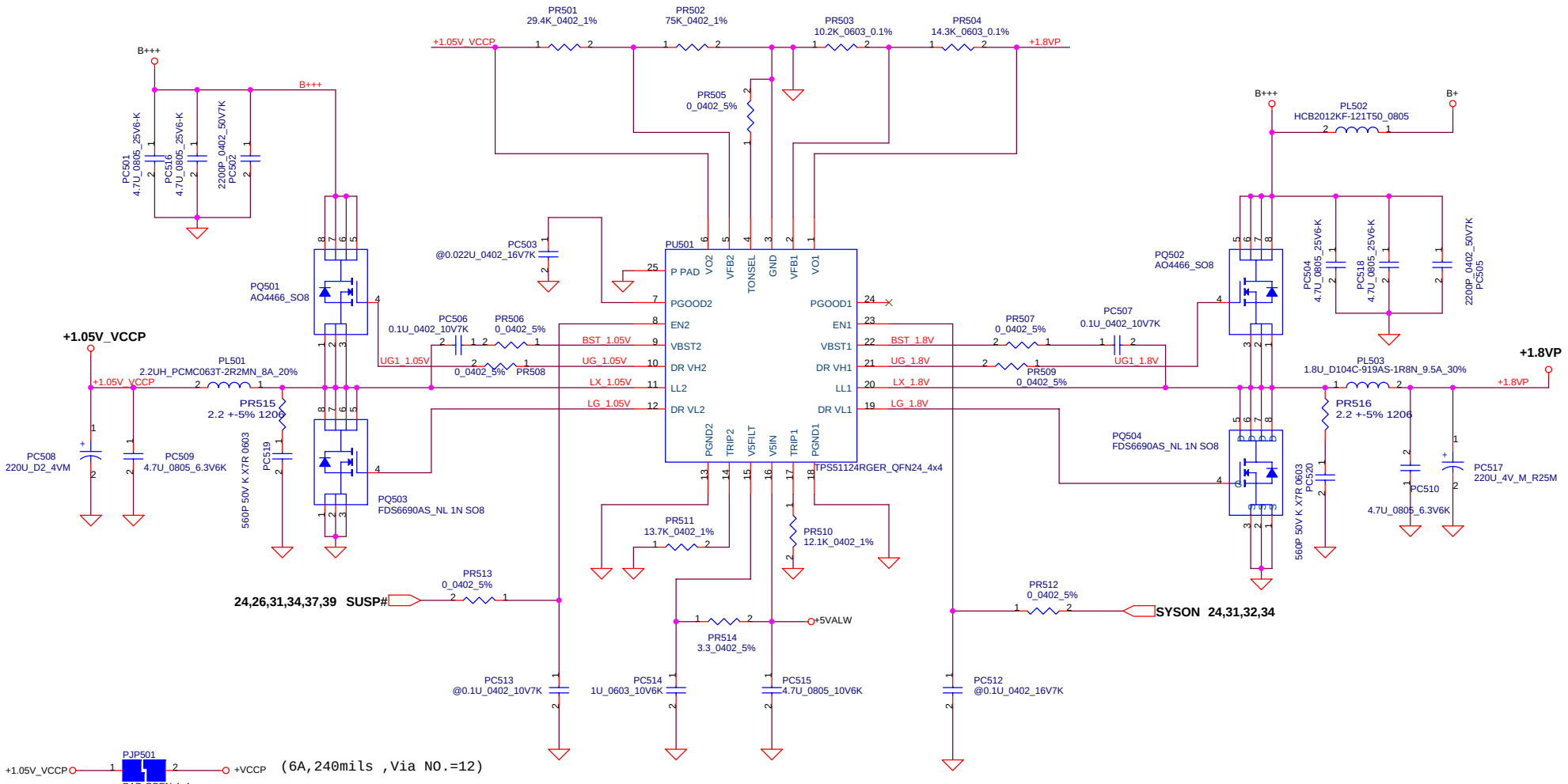


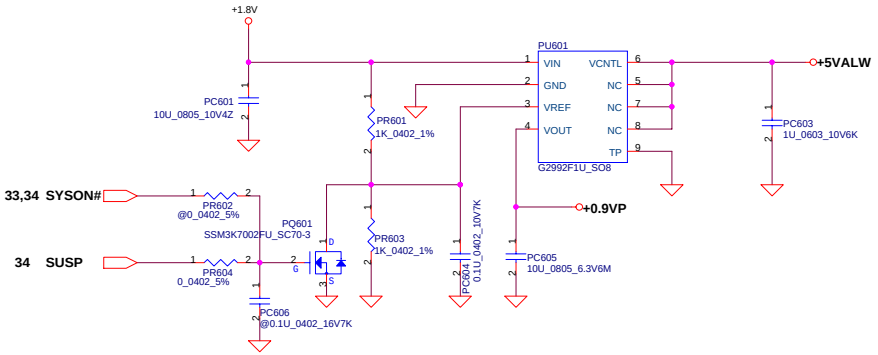
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.05V_VCCP/1.8VP**

Size | Document Number: *Montevina Consumer Discrete* | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 40 of 44



(2A,80mils ,Via NO.= 4)

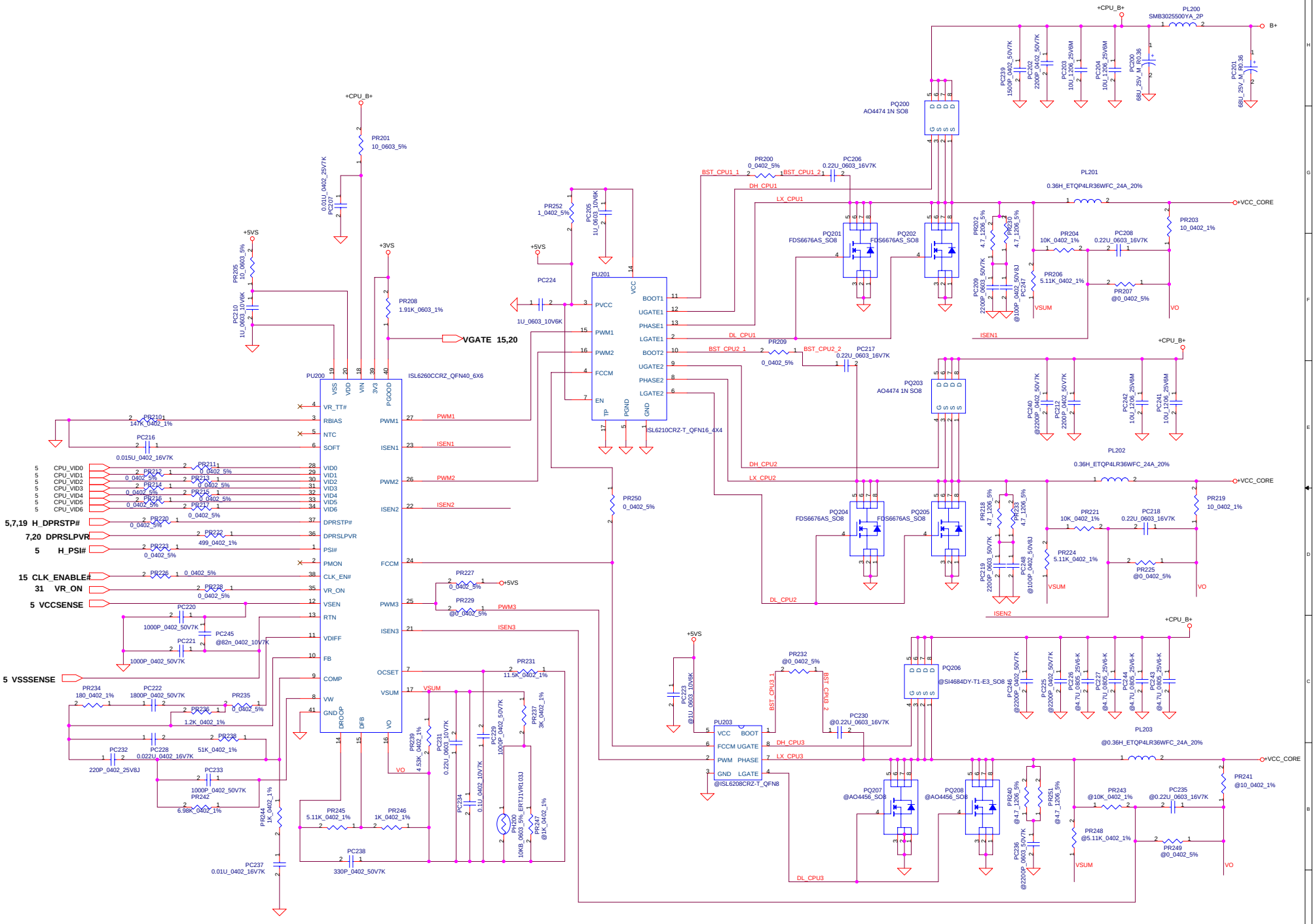
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **0.9VP**

Size | Document Number: **Montevina Consumer Discrete** | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 41 of 44



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CPU_CORE**

Size: C | Document Number: **Montevina Consumer Discrete** | Rev:

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Title	<Title>
Size A	Document Number <Doc>
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Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	04	System thermal shutdown when use NS thermal sensor	HW	Change R8 and R9 from 100 ohm to 0 ohm. Comfirm with SMSC this change is no risk for EMC1402.	0430	SI --> PV
02	31	Follow JAK00 DIS design	HW	Change R2189 and R615 from 100K ohm to 8.2K ohm.	0430	SI --> PV
03	31	Follow JAK00 DIS design	HW	Change EC_PME# pull high power rail from +3VL to +3VALW.	0430	SI --> PV
04	31	Solve AC LED always light even without AC adapter.	HW	Reverse D54 for AC_IN.	0430	SI --> PV
05	32	Solve T/P LED always light even power off.	HW	Change T/P LED power rail from +5VALW_LED to +5VS_LED.	0430	SI --> PV
06	24	Solve +3VS/+5VS has leakage power when S5 and S3.	HW	Reseve R2160.	0430	SI --> PV
07	09	Remove useless component because JAK00 do not support WWAN.	HW	Remove C1018~C1025.	0430	SI --> PV
08	28	Remove useless component.	HW	Remove C990 and C991 (1uF_0603).	0430	SI --> PV
09	31	For ENE cap. board.	HW	Add R442 and R443.	0430	SI --> PV
10	32	Fine-tune LED brightness (Power LED and Cap Lock LED).	HW	Change R2202 to 1.8K ohm and R986 to 750 ohm.	0502	SI --> PV
11	31	To avoid Lid function abnormal when battery mode only.	HW	Chagne Lid Switch power rail from +3VALW to +3VL.	0502	SI --> PV
12	28	Reserve 0603 package if EMI need to stuff bead.	HW	Change from 0402 to 0603 size.	0502	SI --> PV
13	35	To match ST new chipset (internal Hot Plug inverse circuit).	HW	Reserve R45.	0505	SI --> PV
14	09	Double confirm NB strapping setting with CRB. it can solve flash display	HW	Change R70 to pull low ; reserve R65 ; reserve R66, R77 (reserve R66, R77 to solve flash display)	0505	SI --> PV
15	19	Follow Intel design guild, add pull high 10k ohm for SATA_LED#	HW	Add R49 and pull high to +3VS.	0505	SI --> PV
16	15	Reserve R714 because already pull high near North Bridge.	HW	Reserve R714.	0505	SI --> PV
17	24	Solve +3VS power leakage when S3/S4/S5.	HW	Reserve R485.	0505	SI --> PV
18	17	Solve internal MIC has noise when recording.	HW	Reserve C302 and C303.	0509	SI --> PV
19	26	Solve EMI issue for digital MIC (follow Vader DIS).	EMI	Add L10.	0509	SI --> PV
20	30	Follow common design.	HW	Add pull high R61 for SPI WP# and HOLD#.	0510	SI --> PV
21	19	Follow Intel check list.	HW	Change R363 from 180K ohm to 20K ohm and C538 from 0.1uF to 1uF.	0510	SI --> PV
22	24	Follow vender's recommend.	HW	Separate PCIE and USB card present.	0510	SI --> PV
23	04	Delete XDP debug port to solve EMI issue.	EMI	Delete JP42, R730, R733~R735, R738~R741, C851.	0512	SI --> PV
24	15	Delete XDP debug port to solve EMI issue.	EMI	Delete R134 and R135 (Remove XDP clock for XDP port).	0512	SI --> PV
25	20	Remove external HDCP interface.	HW	Delete R440~R441, R1008~R1010.	0512	SI --> PV
26	30	Remove external HDCP ROM.	HW	Delete R438~R439, R415, R422, R427, C304, and U8.	0512	SI --> PV
27	20	Remove useless function.	HW	Reserve R1040.	0512	SI --> PV
28	35	Fine-tune HDMI signal quality.	HW	Change R706 from 4.7K to 3.09K ohm.	0512	SI --> PV
29	15	Solve EMI issue.	EMI	Reserve R126.	0512	SI --> PV
30	34	Solve leakage power for VCC_HV of north bridge when S3/S4/S5..	HW	Base on Intel recommend, change R661 of +3VS discharge circuit from 470 ohm to 10 ohm	0512	SI --> PV
31	31	Solve can not power on issue if +3VL output cap. total over 20uF.	HW	Delete C1009.	0512	SI --> PV
32	28	Audio fail for ESD test.	ESD	Connect U30 thermal PAD to GNDA.	0515	SI --> PV
33	26	Audio fail for ESD test.	ESD	Connect U56 thermal PAD to GNDA.	0515	SI --> PV
34	16	Follow Blade/Vader DIS use the same material.	HW	Change L13, L15, L17.	0515	SI --> PV
35	32	Solve EMI issue for ENE cap. board.	ENE	Stuff R2192, R2193, and C996.	0515	SI --> PV
36	32	Solve EMI issue for ENE cap. board.	ENE	Add C1082, C1087, C1089~C1093.	0515	SI --> PV
37	32	Remove useless parts (LDO for ENE cap. board).	HW	Remove U79, R2139, C2126, C2127, PJP607.	0516	SI --> PV
38	32	Remove useless parts (LDO for ENE cap. board).	HW	Chagne JP38 pin1 power from +3VL_CAP to +3VL.	0516	SI --> PV
39	26	Solve MIC jack detect abnormal when plug in Dock.	HW	Change to right part number for R524 (39.2K_0402).	0519	SI --> PV
40	20	Solve pop noise when press CTRL+ALT+DEL.	HW	Reserve R424.	0520	SI --> PV
41	17	Solve wavey issue in CRT monitor.	HW	Add PJP305 to sparate GND.	0521	SI --> PV
42	17	Remove useless part.	HW	Remove L8.	0521	SI --> PV
43	26	Solve ESD test fail for Audio.	HW	Reserve R69 and C728.	0521	SI --> PV
44	29	For ESD request.	ESD	Delete R2183.	0522	SI --> PV
45	35	There is inverse circuit internal in new version chipset for HPD signal.	HW	Change U50 from STHDLS10QTR to STHDLS10TQTR.	0522	SI --> PV
46	35	Reserve inverse circuit.	HW	Reserve Q102 and R563.	0522	SI --> PV
47	35	Follow vender's recommend.	HW	Add R712 and pull high to +3VS_LS.	0522	SI --> PV
48	10	To prevent wavy issue in CRT.	HW	Add C148.	0522	SI --> PV

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