

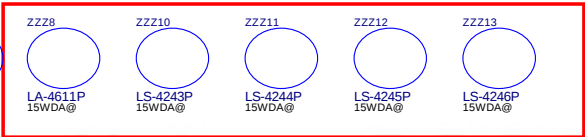
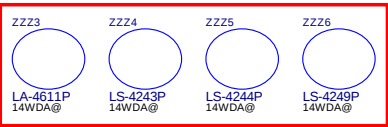
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KSW01/91 Schematics Document

Intel Merom Processor with SiSM672/FX + DDRII + SiS968 + SiS307ELV

2008-08-01

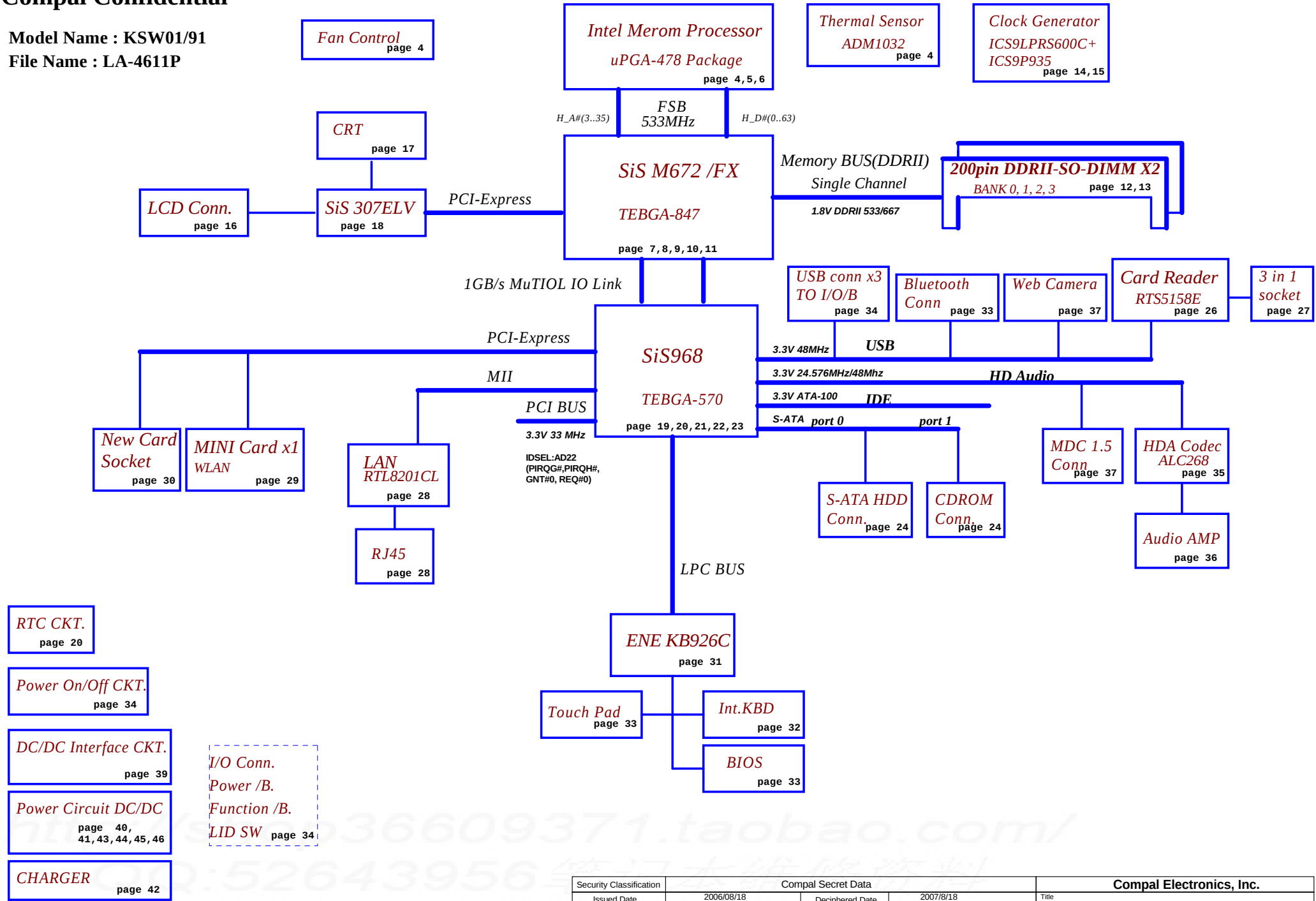
REV: 0.2



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		Deciphered Date		2009/05/18	
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Compal Confidential

Model Name : KSW01/91
File Name : LA-4611P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID
14W	R424 (Pull low)
15W	NA (Internal Pull High)

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

M672 SM Bus address

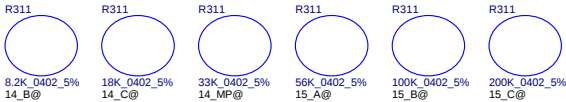
Device	Address
Clock Generator	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 001Xb

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Ra~ R312

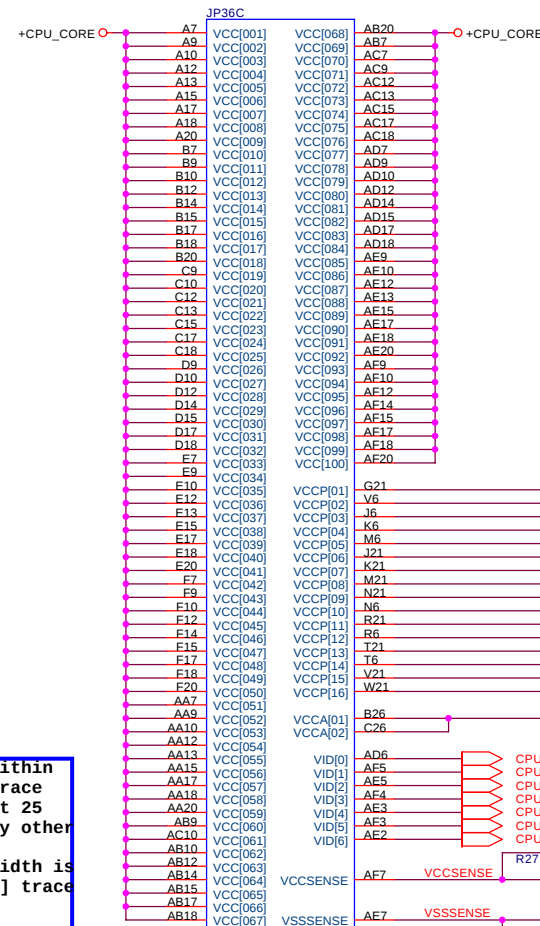
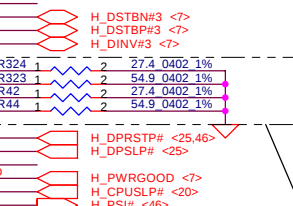
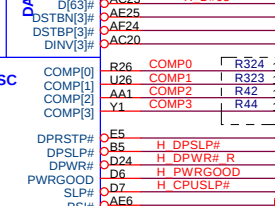
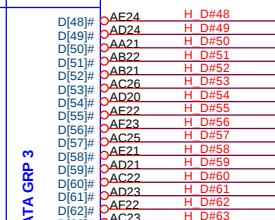
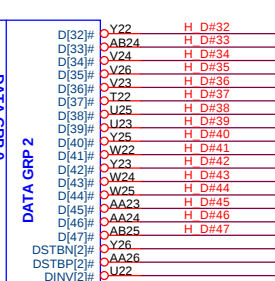
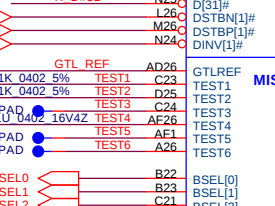
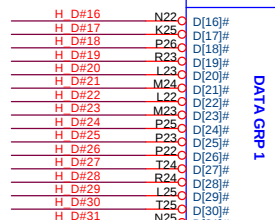
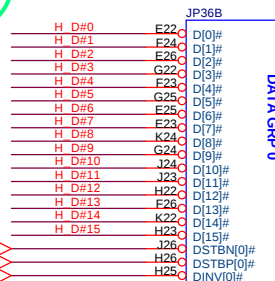
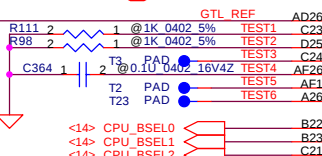
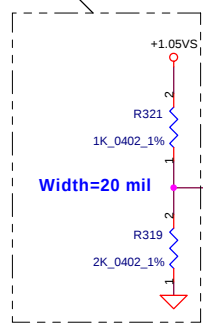
Rb~ R311



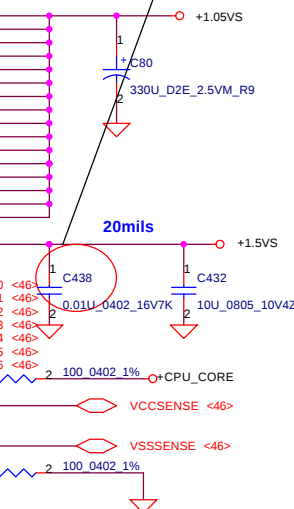
Board ID	Rb	VAD_BID Min	VAD_BID typ	VAD_BID Max	Rb BOM Structure
0	0	0 V	0 V	0 V	14_A@ ✓
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	14_B@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	14_C@
3	33K +/- 5%	0.721 V	0.819 V	0.926 V	14_MP@
4	56K +/- 5%	1.054 V	1.185 V	1.325 V	15_A@ ✓
5	100K +/- 5%	1.489 V	1.650 V	1.819 V	15_B@
6	200K +/- 5%	2.019 V	2.200 V	2.386 V	15_C@
7	NC	3.135V	3.300 V	3.465 V	15_MP@

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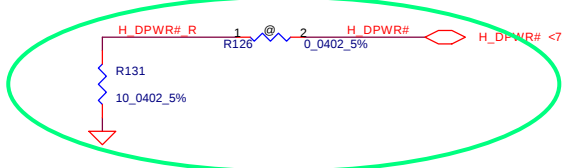
Place this cap more close to B26/C26 rather than 10UF



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

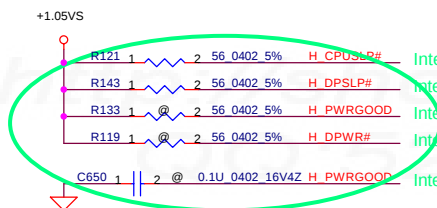
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils.
The trace width/space/other is
20/7/25.

Close to CPU pin
within 500mils.



Intel :Don't Pull-up SiS : Pull-up 56ohm (Mount)

Intel : Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

Intel : Don't Pull-up (Connecte to ICH) SiS : Pull-up 56ohm (Un-Mount)

Intel :Don't Pull-up SiS : Pull-up 56ohm (Un-Mount)

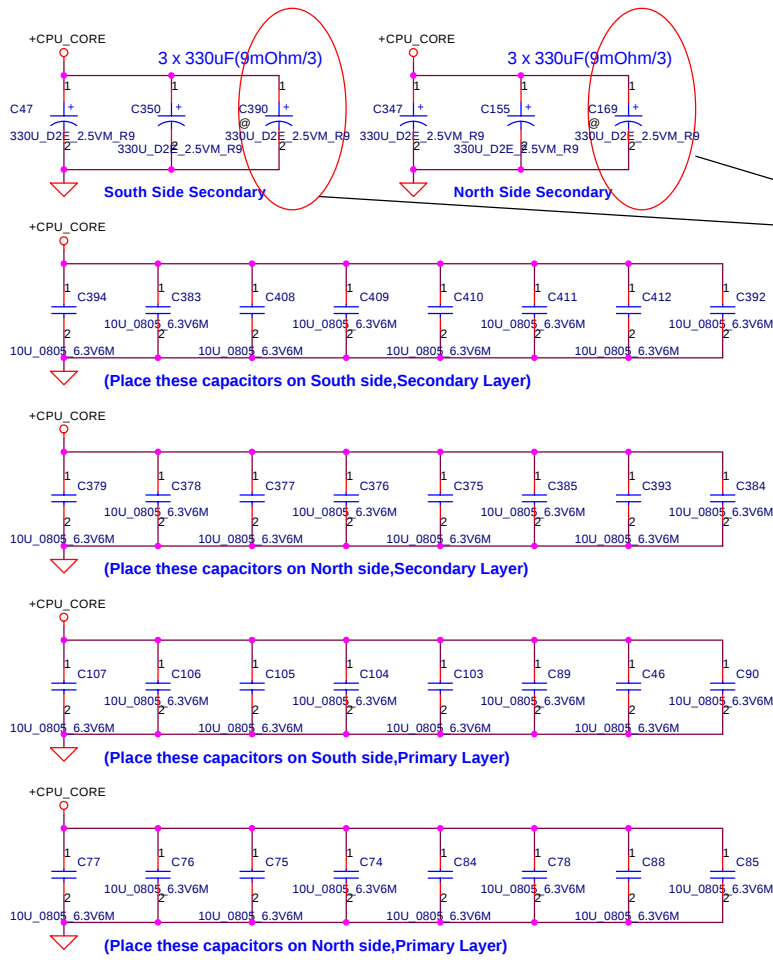
Intel :Don't Pull-down SiS :Pull-down Cap (Un-Mount)

SiS Recommend

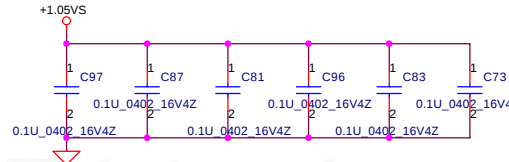
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JP36D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F16	VSS[047]	VSS[128]	AC6
F19	VSS[048]	VSS[129]	AC8
F2	VSS[049]	VSS[130]	AC11
F22	VSS[050]	VSS[131]	AC14
F25	VSS[051]	VSS[132]	AC16
G4	VSS[052]	VSS[133]	AC19
G1	VSS[053]	VSS[134]	AC21
G23	VSS[054]	VSS[135]	AC24
G26	VSS[055]	VSS[136]	AD2
H3	VSS[056]	VSS[137]	AD5
H6	VSS[057]	VSS[138]	AD8
H21	VSS[058]	VSS[139]	AD11
H24	VSS[059]	VSS[140]	AD13
J2	VSS[060]	VSS[141]	AD16
J5	VSS[061]	VSS[142]	AD19
J22	VSS[062]	VSS[143]	AD22
J25	VSS[063]	VSS[144]	AD25
K1	VSS[064]	VSS[145]	AE1
K4	VSS[065]	VSS[146]	AE4
K23	VSS[066]	VSS[147]	AE8
K26	VSS[067]	VSS[148]	AE11
L3	VSS[068]	VSS[149]	AE14
L6	VSS[069]	VSS[150]	AE16
L21	VSS[070]	VSS[151]	AE19
L24	VSS[071]	VSS[152]	AE23
M2	VSS[072]	VSS[153]	AE26
M5	VSS[073]	VSS[154]	A2
M22	VSS[074]	VSS[155]	A5
M25	VSS[075]	VSS[156]	A8
N1	VSS[076]	VSS[157]	AF6
N4	VSS[077]	VSS[158]	AF8
N23	VSS[078]	VSS[159]	AF11
N26	VSS[079]	VSS[160]	AF13
P3	VSS[080]	VSS[161]	AF16
	VSS[081]	VSS[162]	AF19
		VSS[163]	AF21
			A25
			AE25

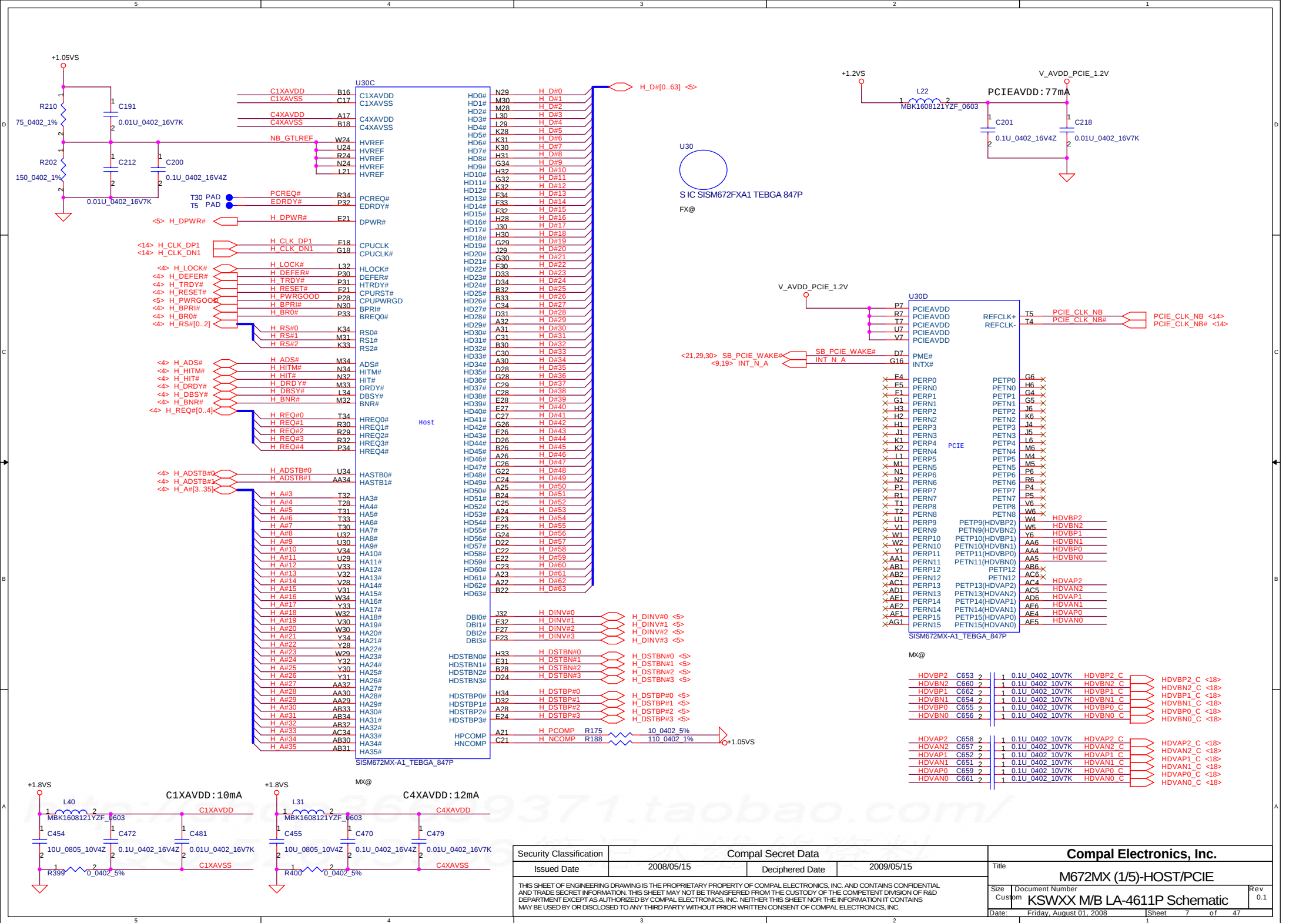
Merom Ball-out Rev 1a
conn@

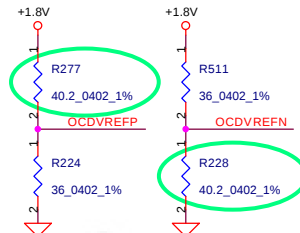
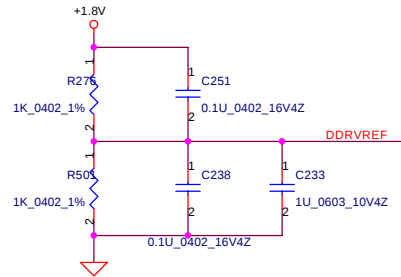
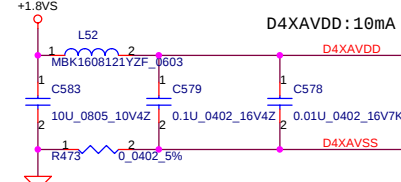
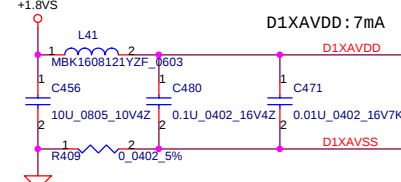
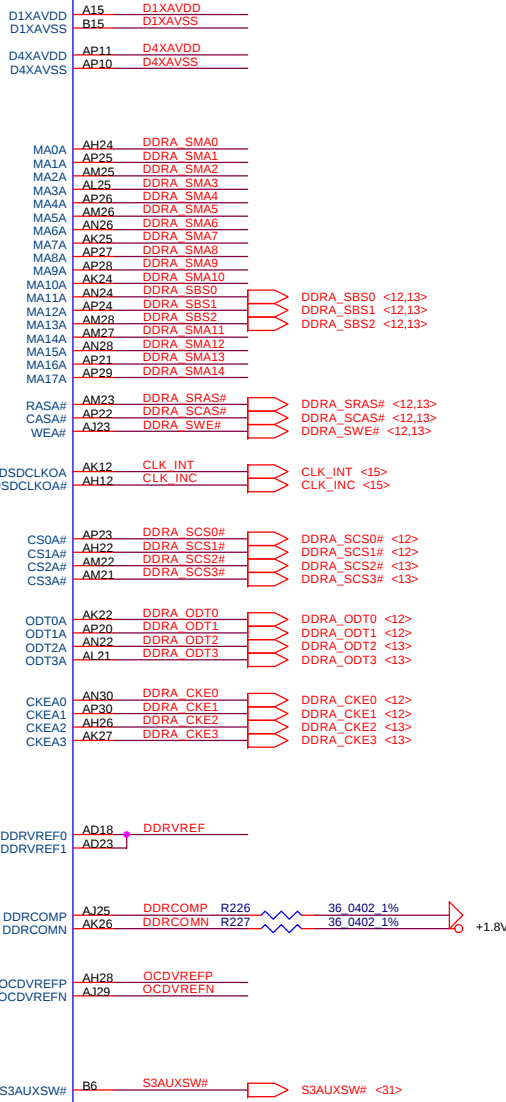
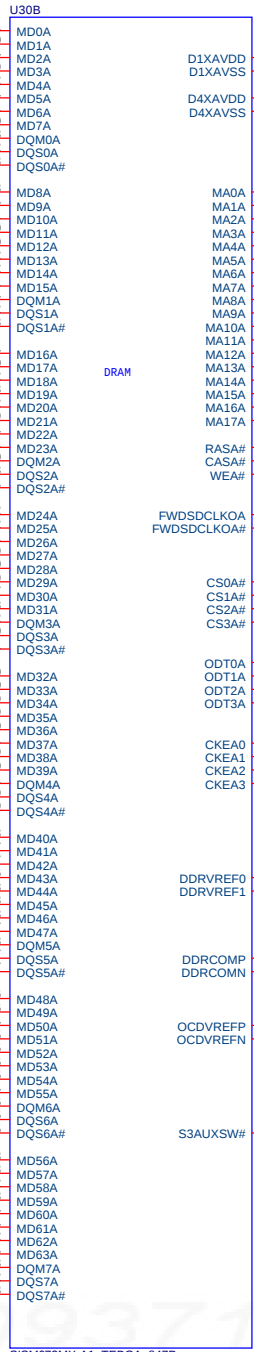


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



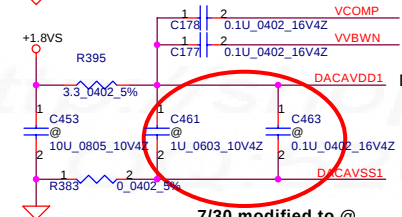
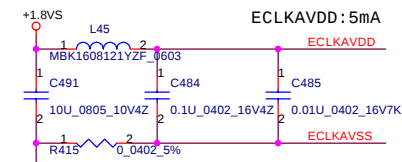
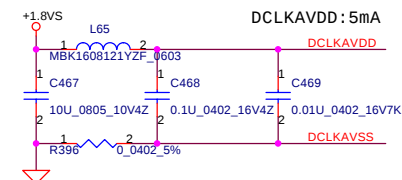
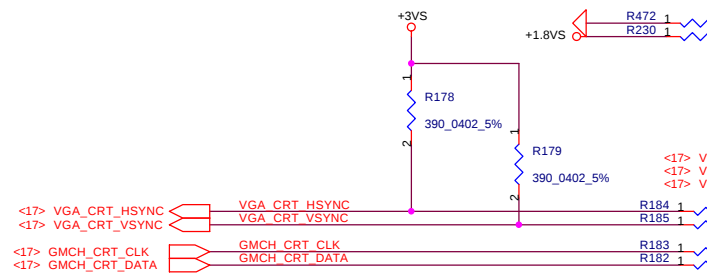
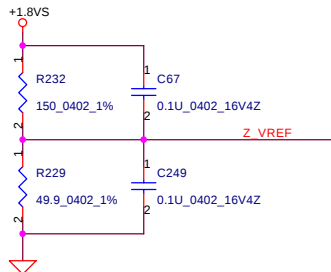
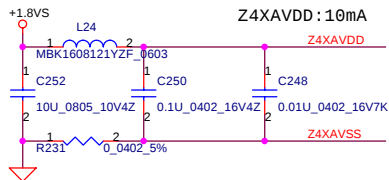
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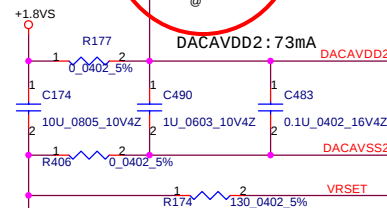


MX@

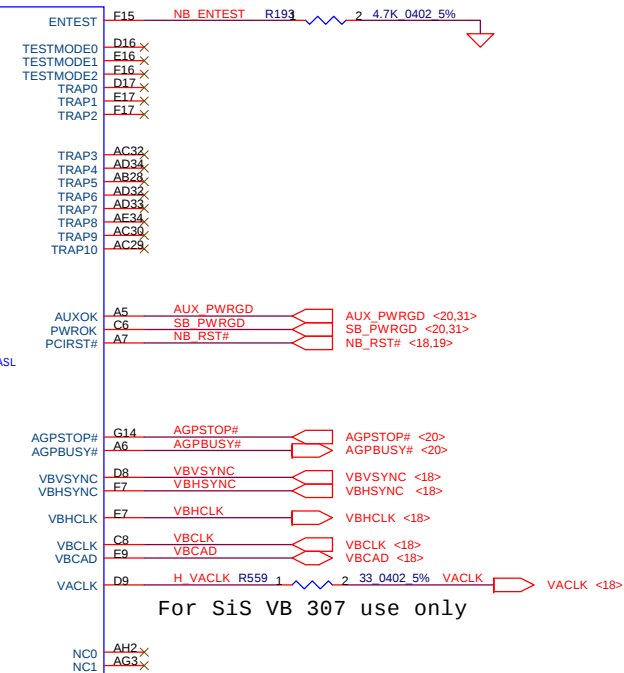
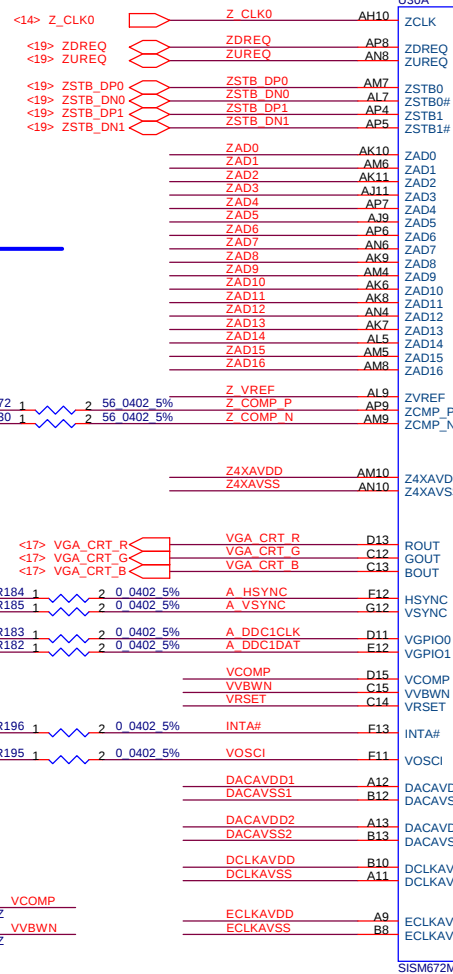
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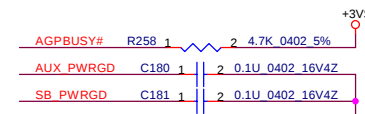
DACAVDD1 Spec.
Voltage : 1.5V +/- 5%
Current : 100mA



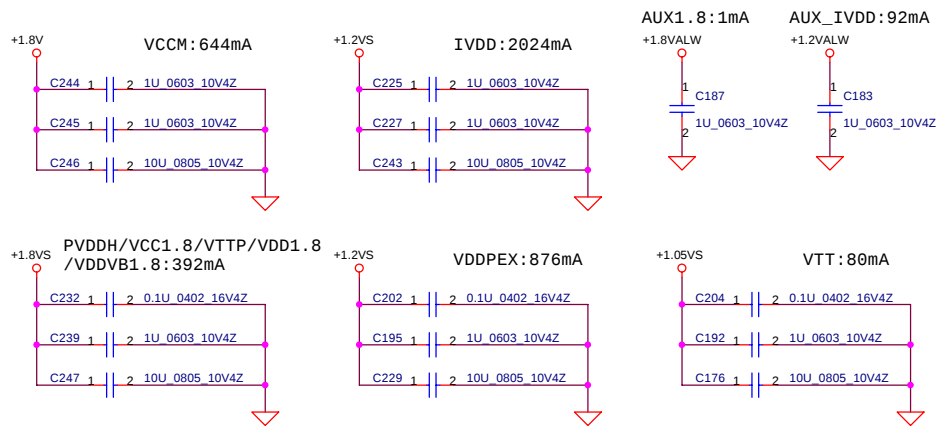
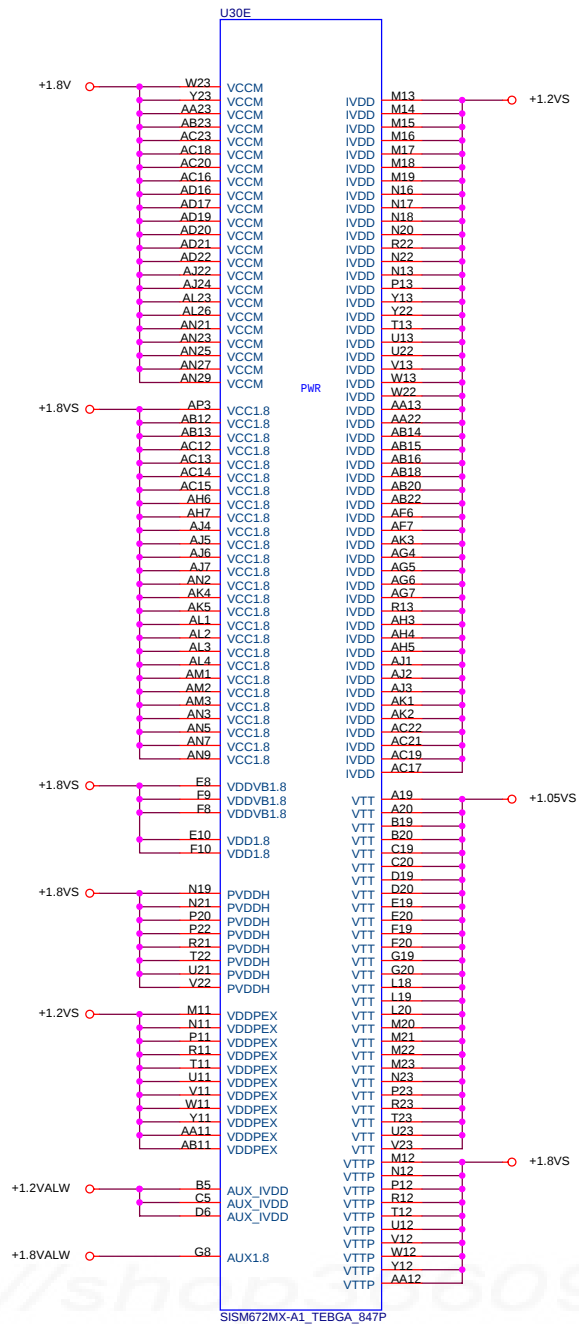
5/20 reserved by Ivan



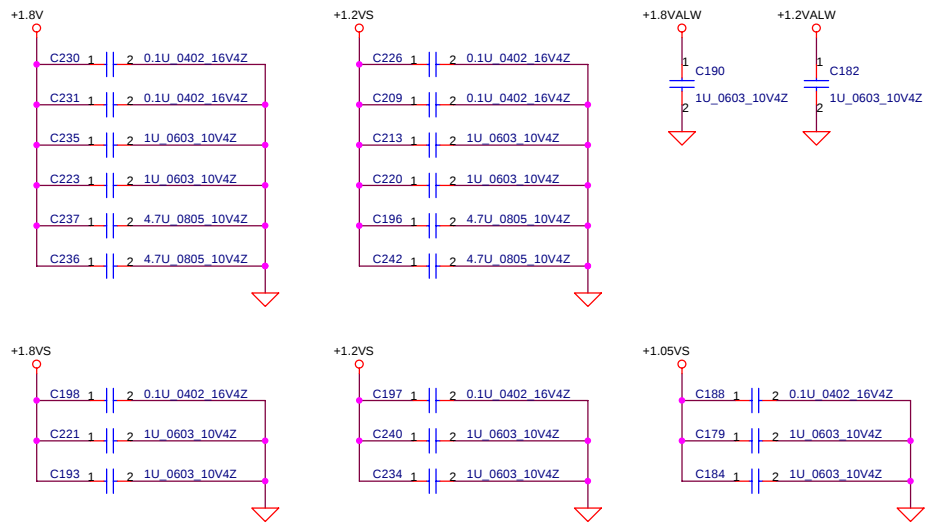
For SiS VB 307 use only



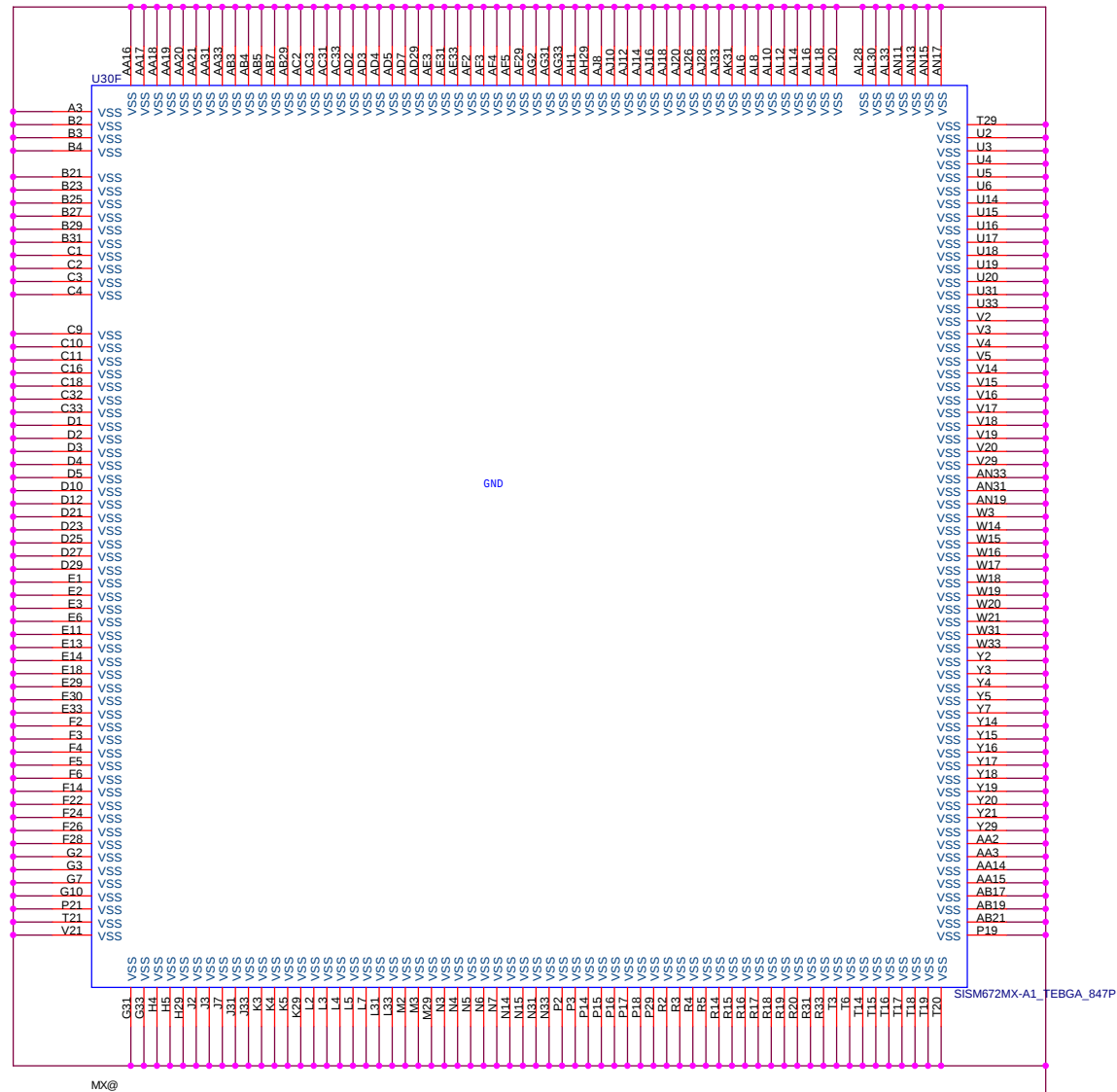
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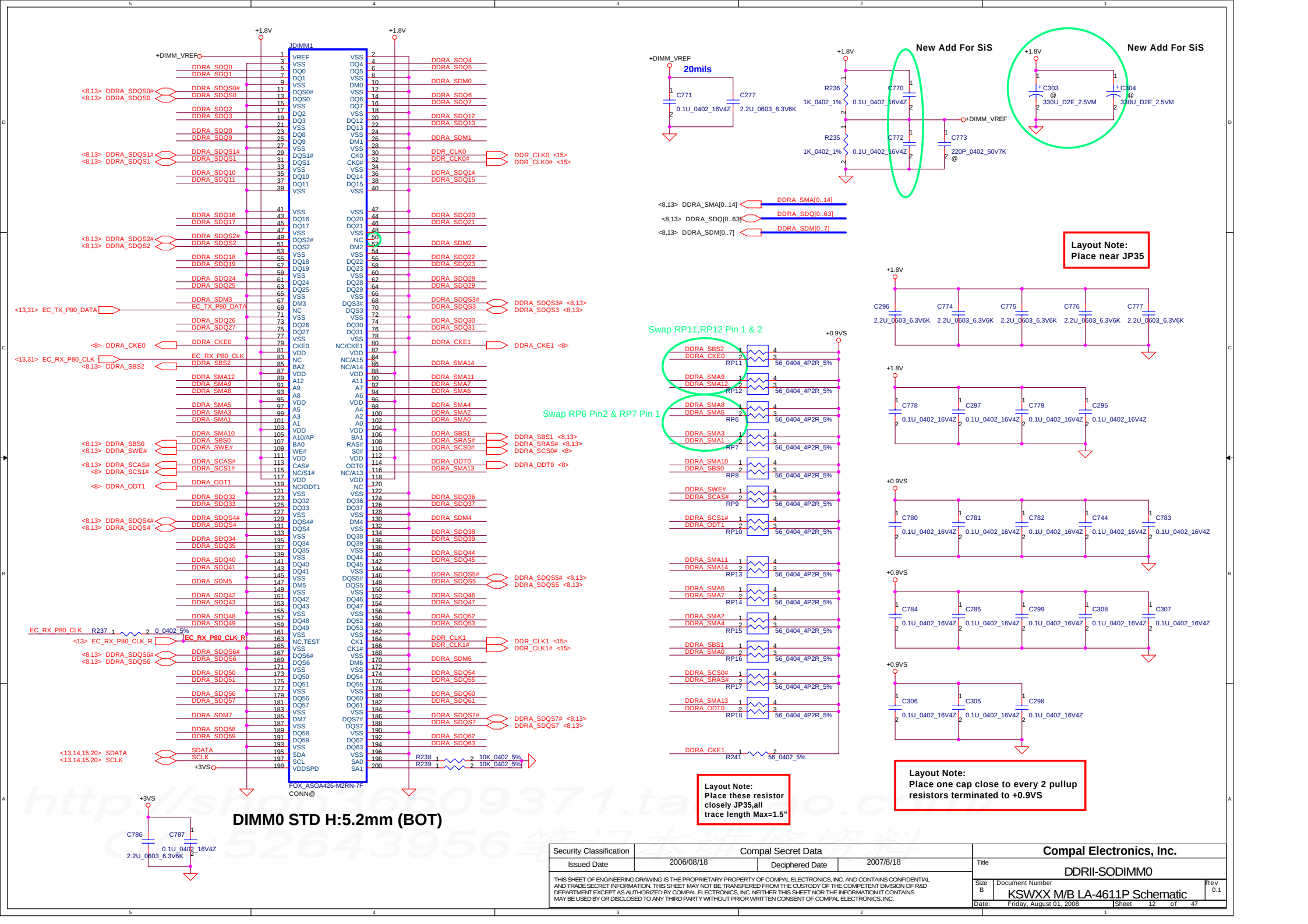
Place these Cap under M672MX solder side.

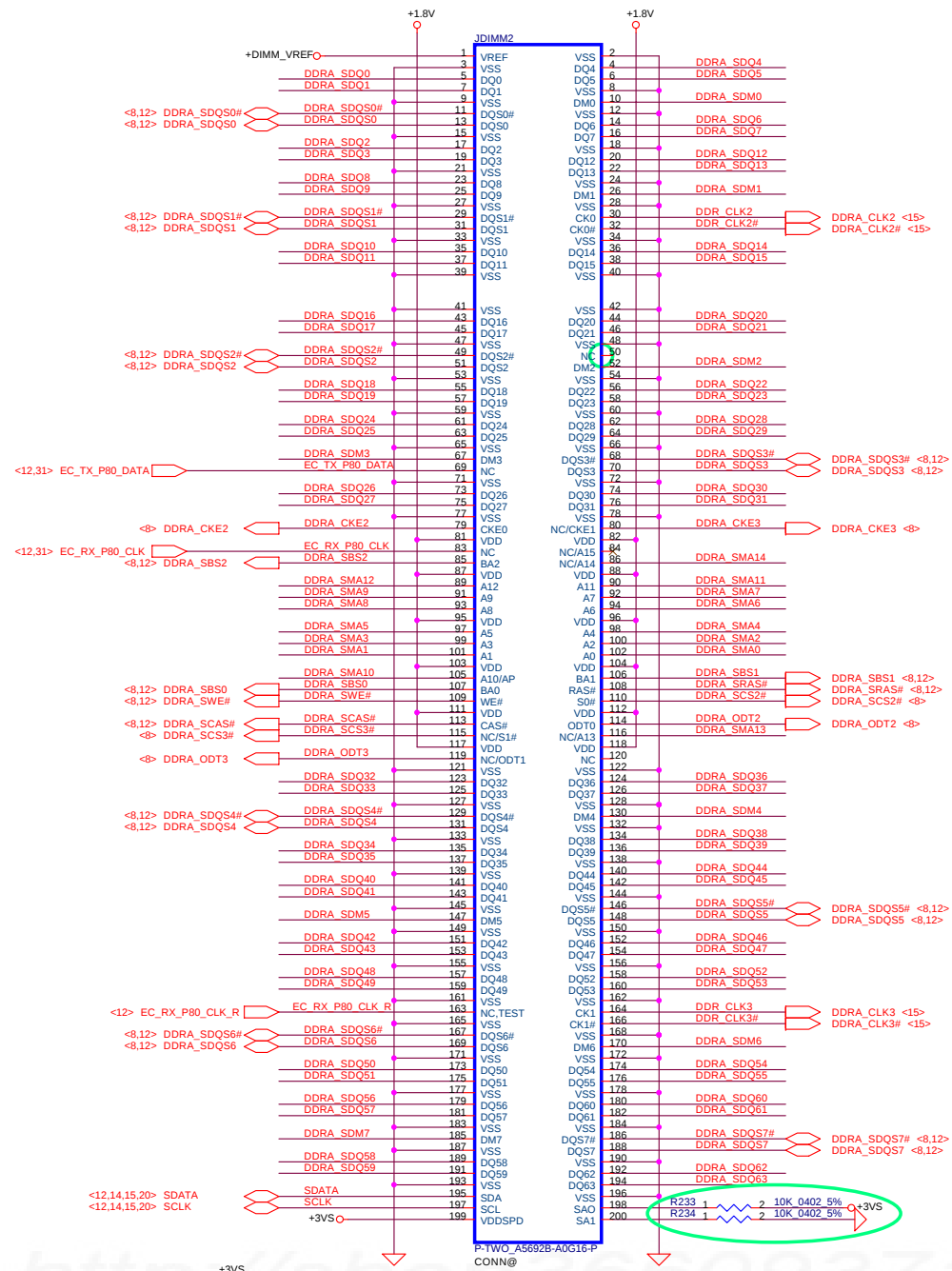


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Custom	Document Number	KSWXX M/B LA-4611P Schematic		Rev
Date:	Friday, August 01, 2008	Sheet	10	of	47

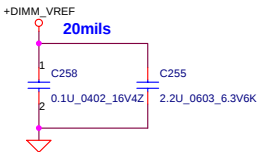


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		0.1	
Custom	KSWXX M/B LA-4611P Schematic				
Date:	Friday, August 01, 2008	Sheet	11	of	47



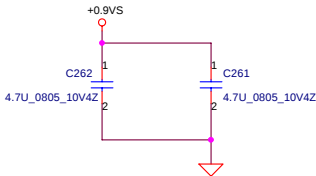
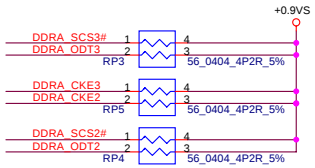
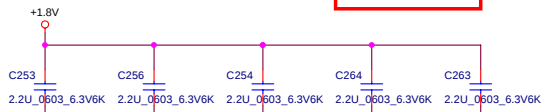


DIMM1 STD H:9.2mm (BOT)



<8,12> DDRA_SMA[0..14] <--> DDRA_SMA[0..14]
<8,12> DDRA_SDQ[0..63] <--> DDRA_SDQ[0..63]
<8,12> DDRA_SDM[0..7] <--> DDRA_SDM[0..7]

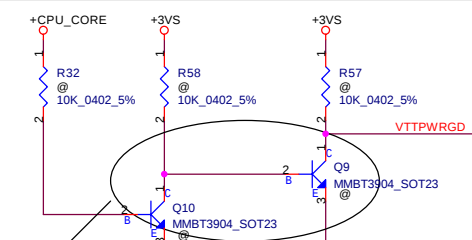
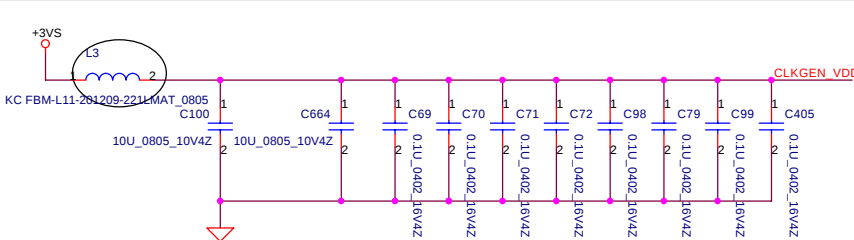
Layout Note:
Place near JP34



Layout Note:
Place these resistor
closely JP34,all
trace length Max=1.5"

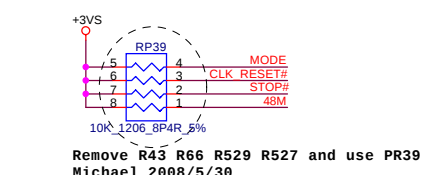
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

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				Date: Friday, August 01, 2008	Rev 0.1
				Sheet 13	of 47

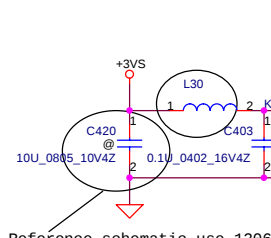
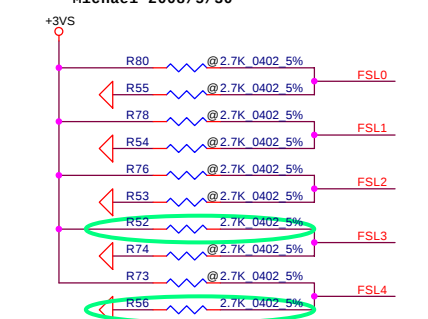


FSL4	FSL3	FSL2	FSL1	FSL0	CPU MHZ	PCIE MHZ	PCI MHZ	ZCLK MHZ
0	1	0	0	1	133	100	33.3	133
0	1	0	1	1	166	100	33.3	133
0	1	0	1	0	200	100	33.3	133

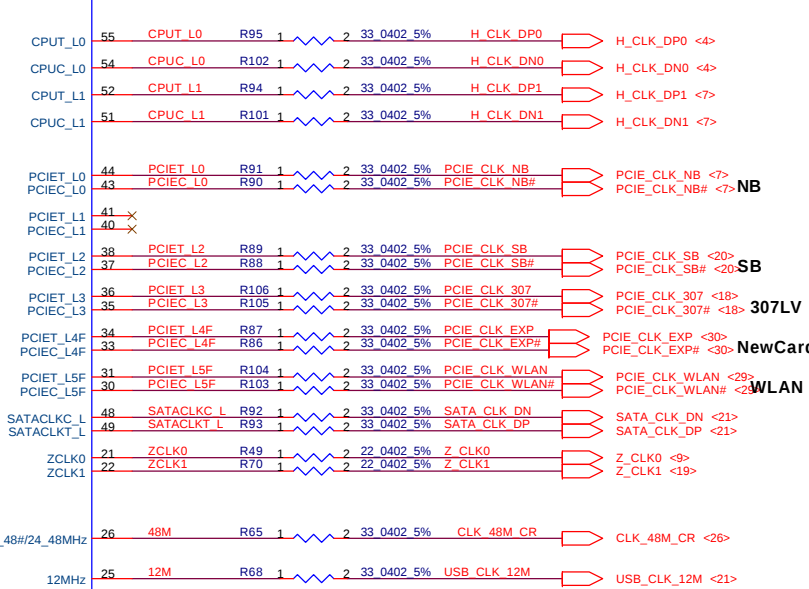
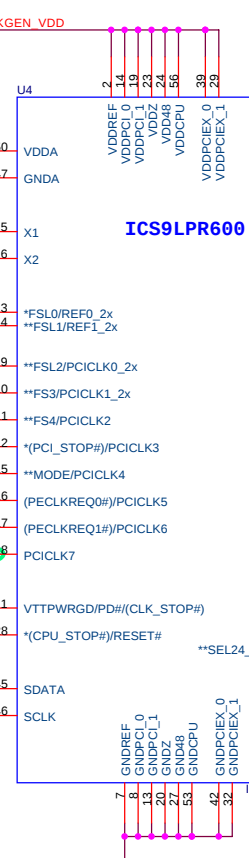
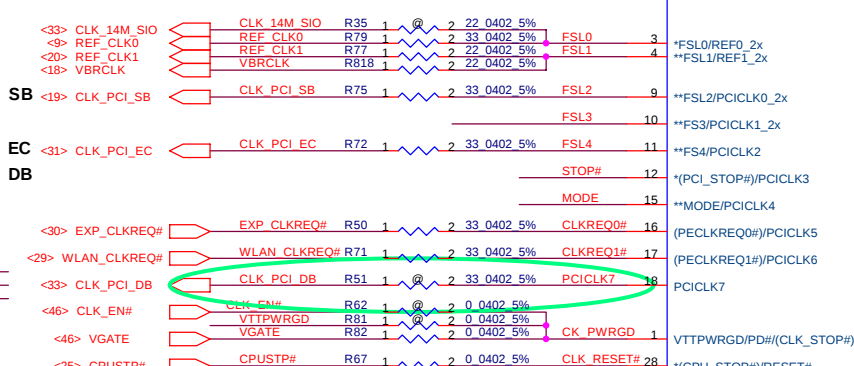
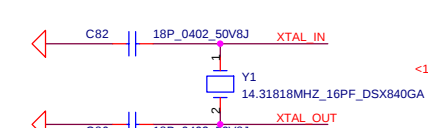
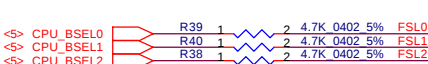
Use SB03904008L & SB000006A00 FootPrint



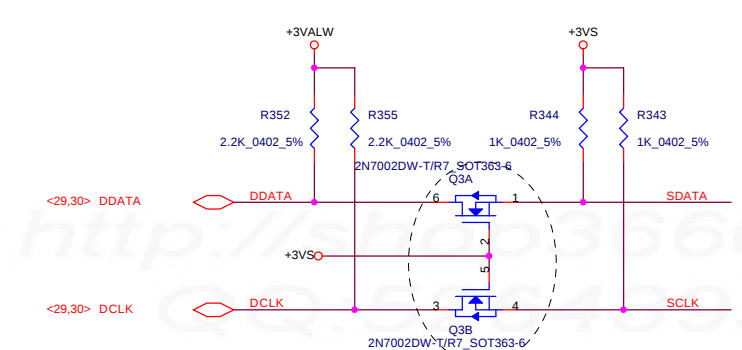
Remove R43 R66 R529 R527 and use PR39
Michael 2008/5/30



Reference schematic use 1206



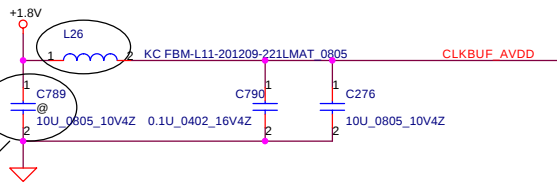
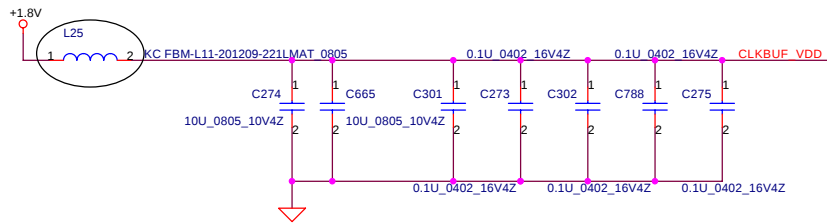
Pin 26 need BIOS to set disable,
for saving power & good EMI



Replace Package from SOT23 to SOT363-6
Michael 2008/5/30

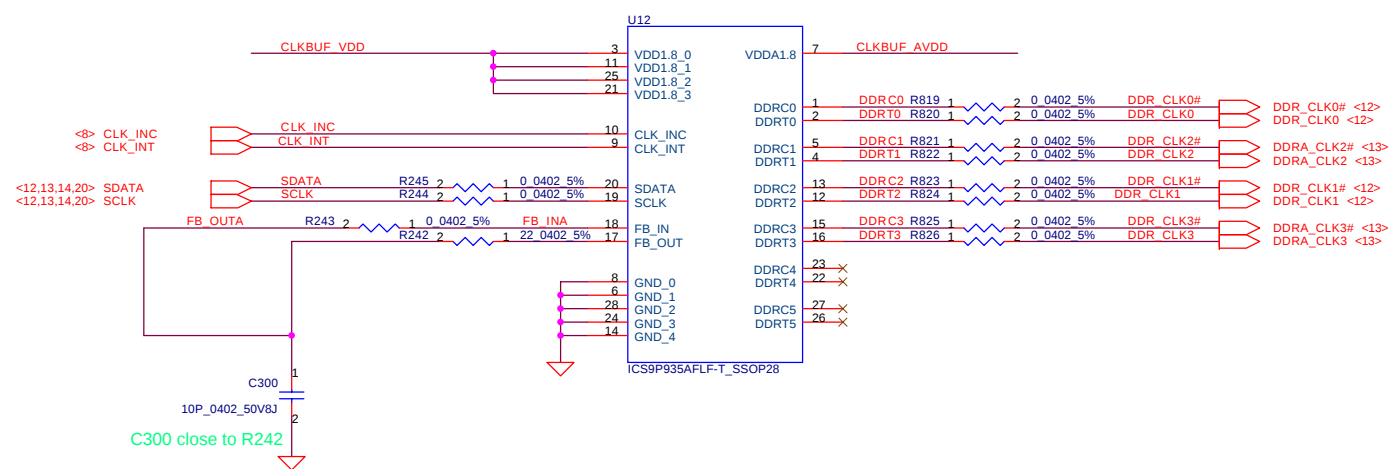
Z CLK0	C62	1	2	@10P 0402 50V8J
Z CLK1	C61	1	2	@10P 0402 50V8J
CLK PCI SB	C63	1	2	@10P 0402 50V8J
CLK PCI EC	C66	1	2	@10P 0402 50V8J
CLK PCI DB	C59	1	2	@10P 0402 50V8J
REF CLK0	C65	1	2	@10P 0402 50V8J
REF CLK1	C64	1	2	@10P 0402 50V8J

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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Clock Generator ICS9LPR600C	
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Reference schematic use 1206

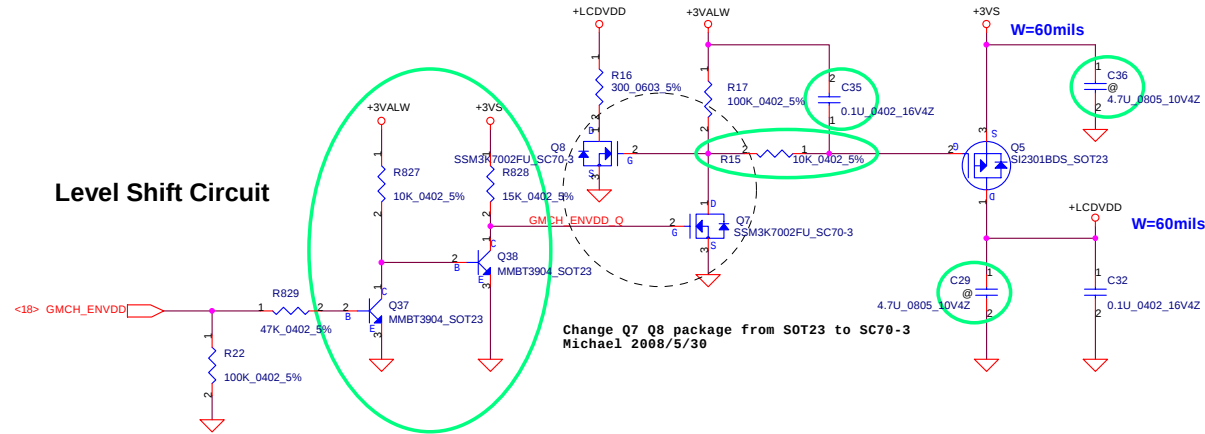
Horizontal rotate



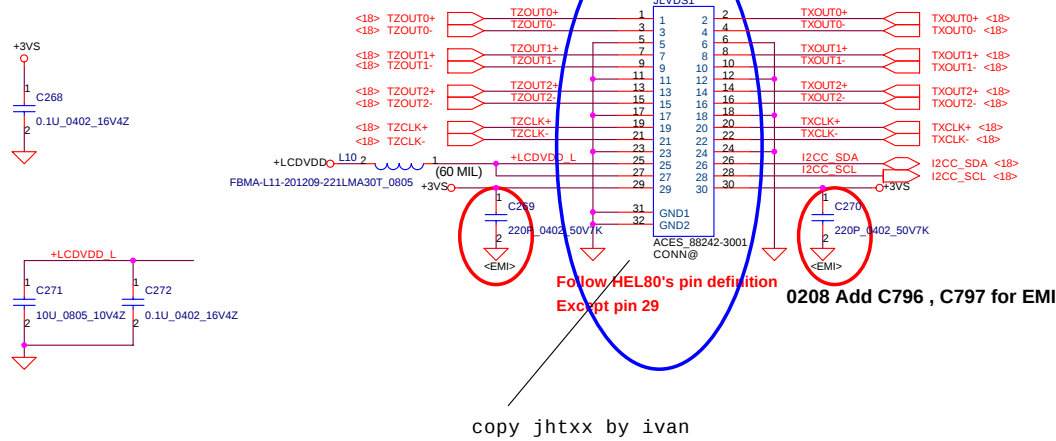
http://shop36609371.taobao.com/
QQ:52643956

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Clock Buffer ICS9P935	
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				Date: Friday, August 01, 2008	Rev 0.1
				Sheet 15 of 47	

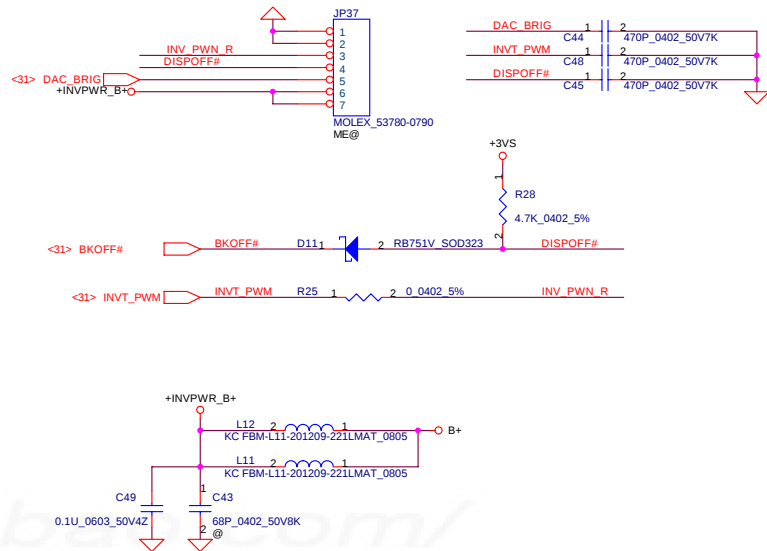
LCD POWER CIRCUIT



LCD/PANEL BD. Conn. (IFTXX)



INVERTER Conn.



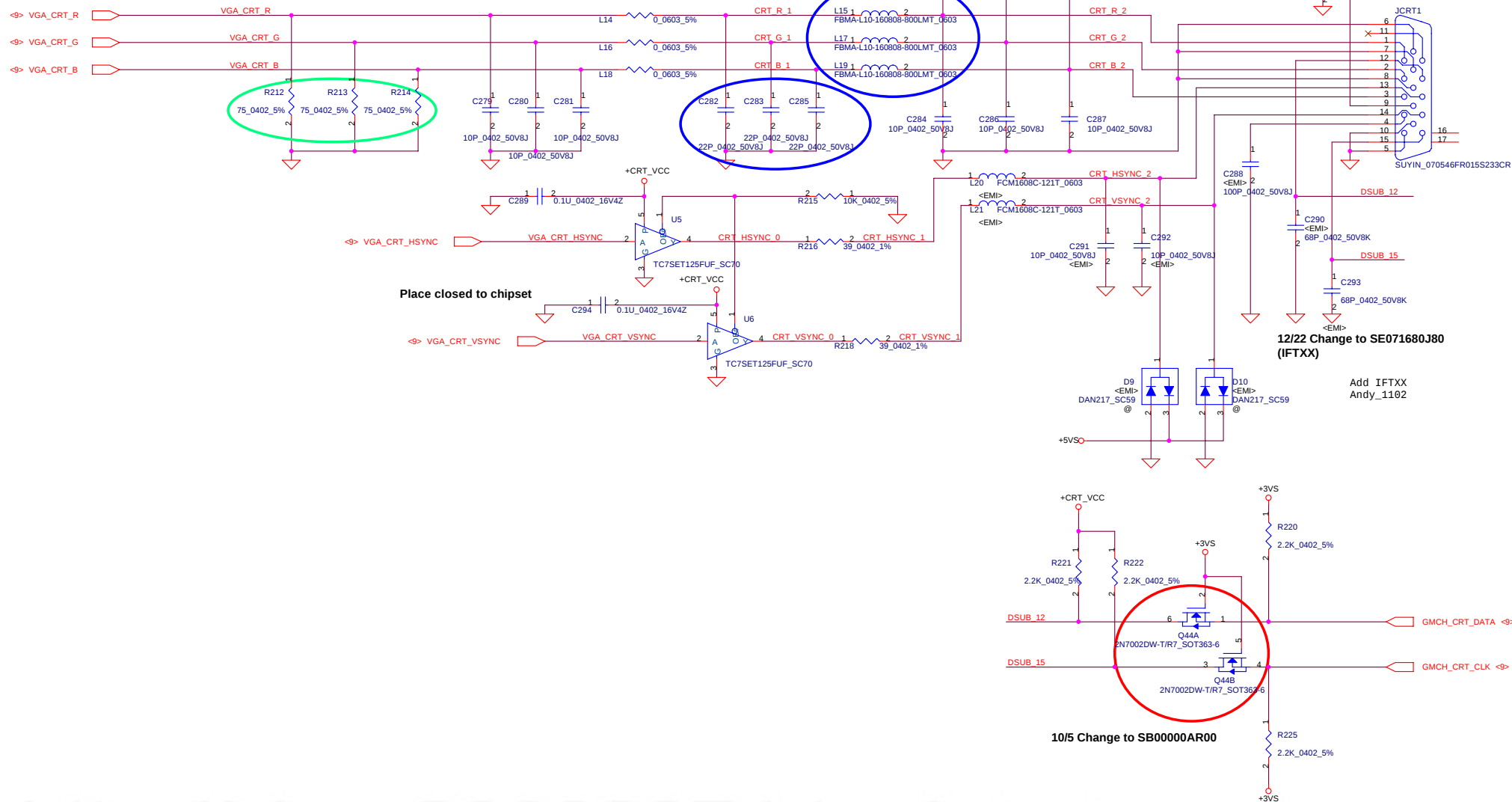
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				Document Number
				KSWXX M/B LA-4611P Schematic
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CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

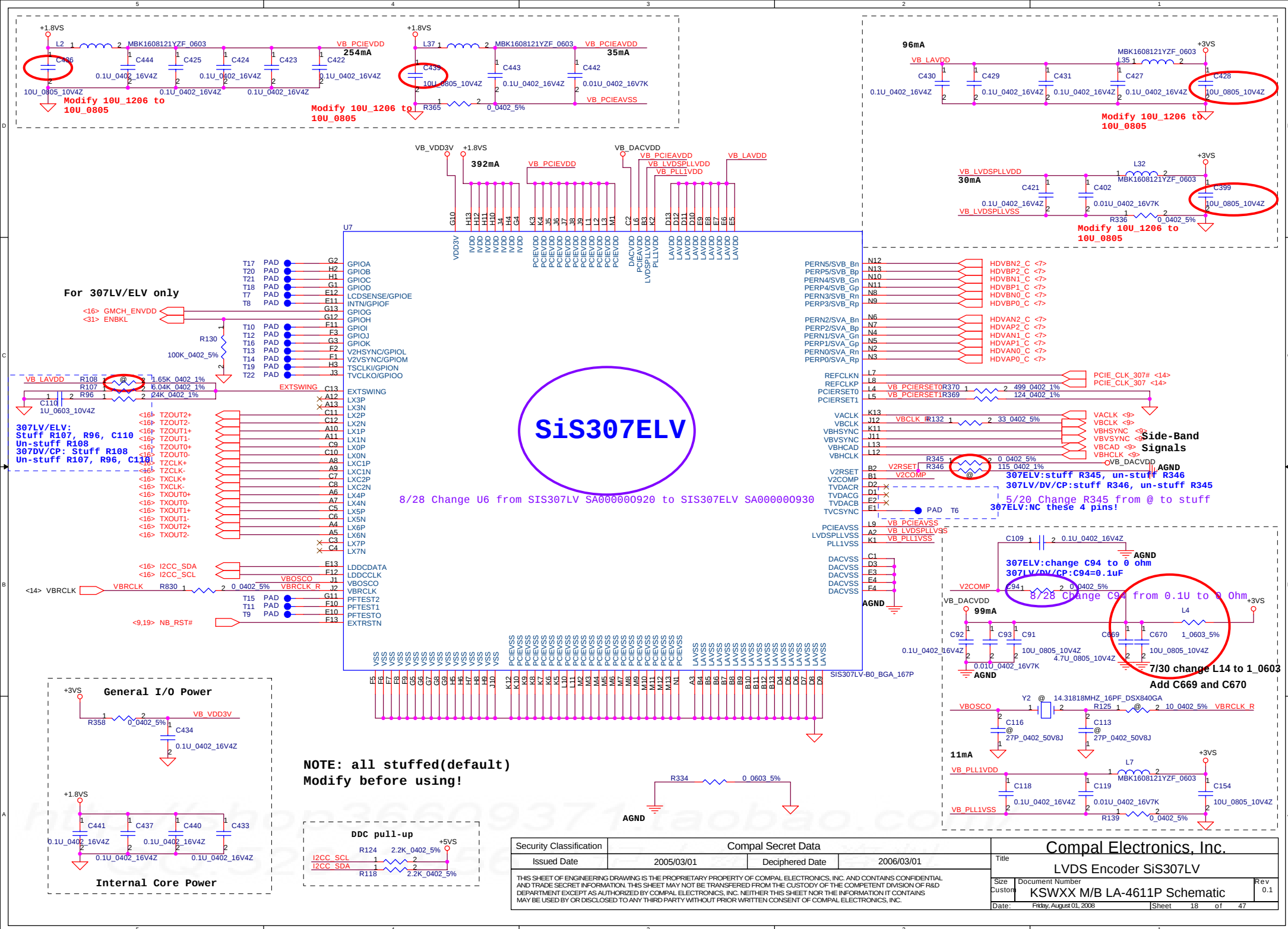
Place closed to chipset

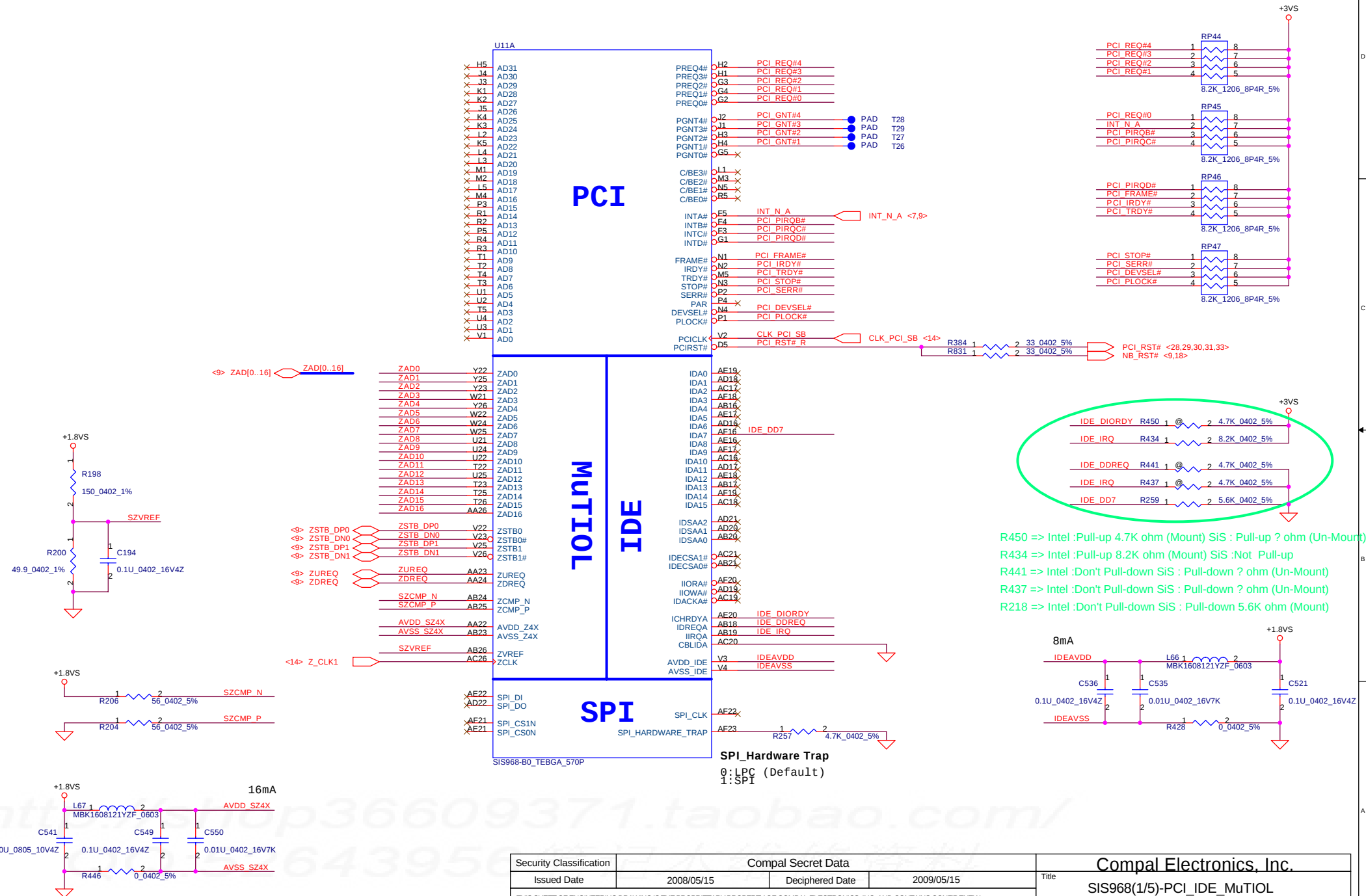
12/15 Modified. Note L26-L30 are 0 Ohm resistors (IFTXX)



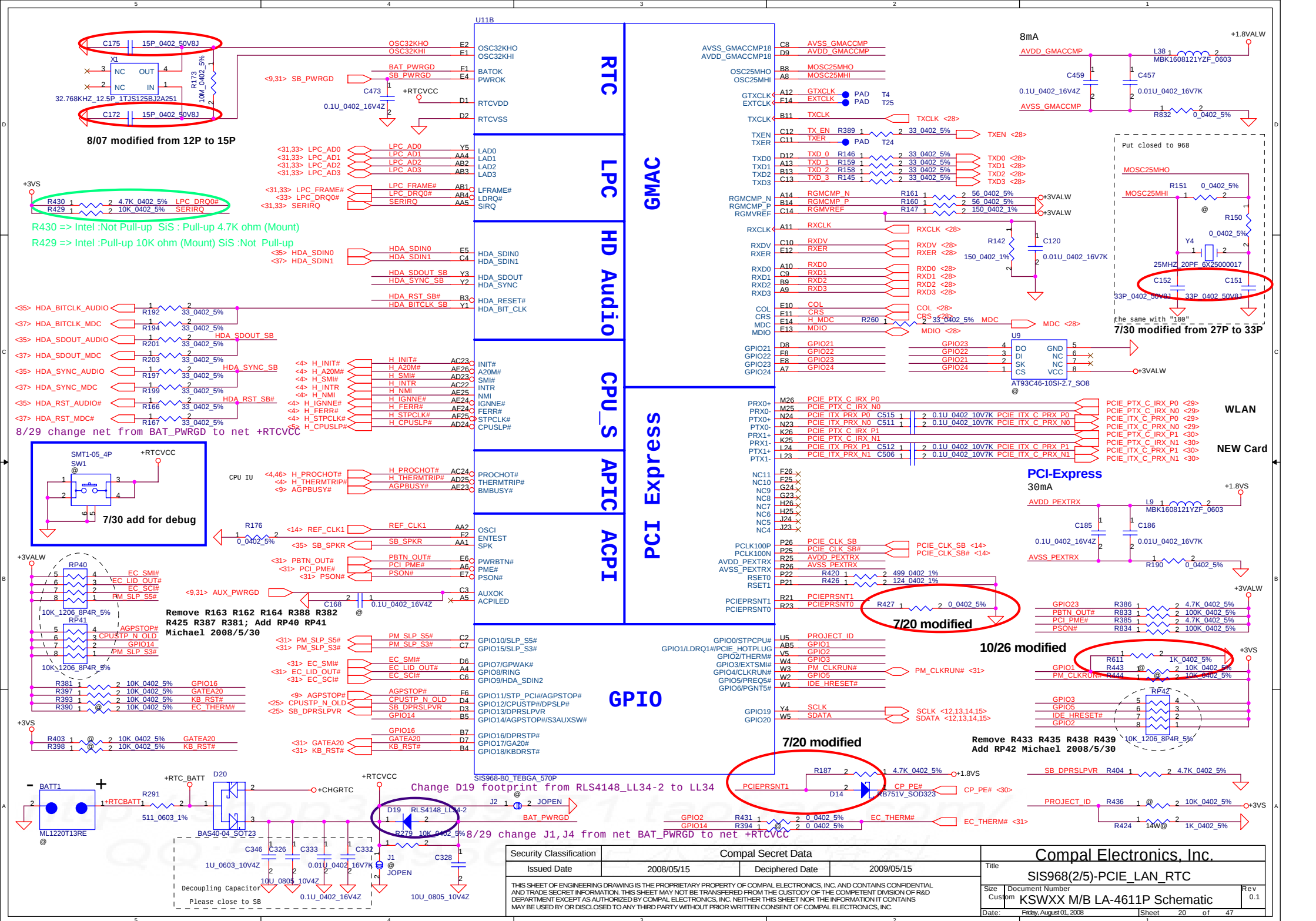
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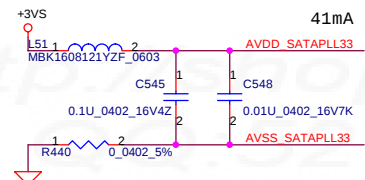
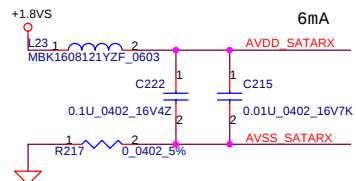
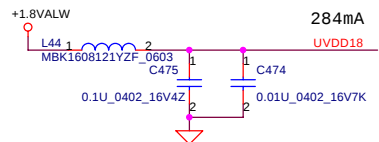
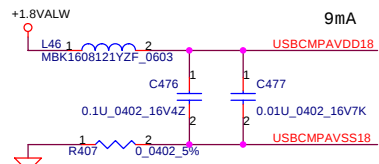
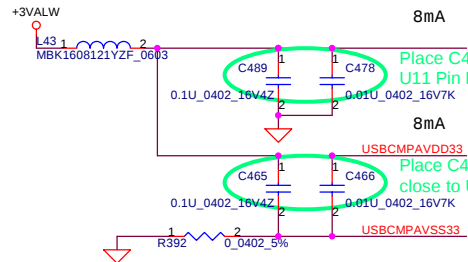
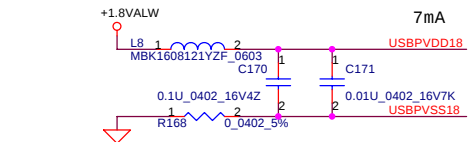
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Issued Date	2006/08/18	Deciphered Date	2007/8/18		Title		
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Size		Document Number		Rev	
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USB
BT
New Card
WLAN
USB
USB
Card Reader
CAMERA

<30> USB20_P0
<30> USB20_N0
<33> USB20_P1
<33> USB20_N1
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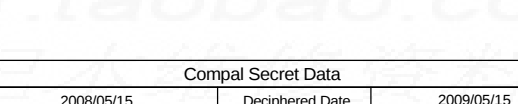
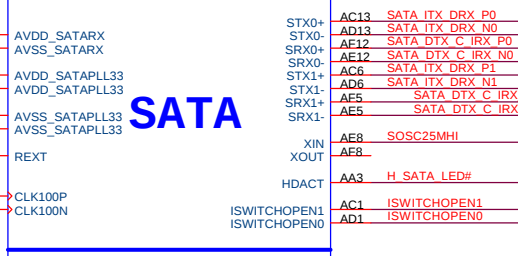
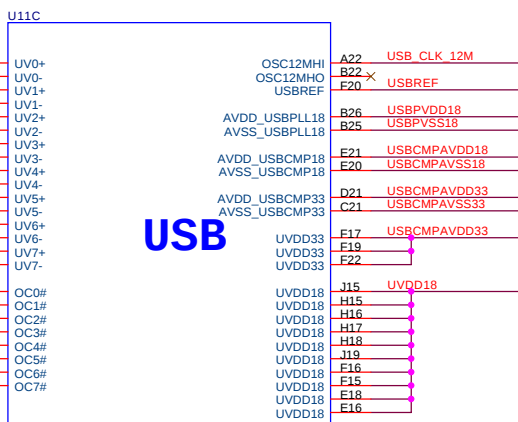
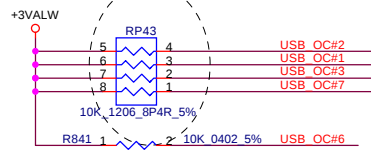
AVDD_SATARX
AVSS_SATARX
AVDD_SATAPLL33
AVSS_SATAPLL33
AVDD_SATAPLL33
AVSS_SATAPLL33
AVDD_SATAPLL33
AVSS_SATAPLL33

SATA_REXT
SATA_CLK_DP
SATA_CLK_DN
SATA_CLK_DP
SATA_CLK_DN

SB_PCIE_WAKE#
ATRAP
TRAP0
PCIEWAKE
ATRAP
TRAP0

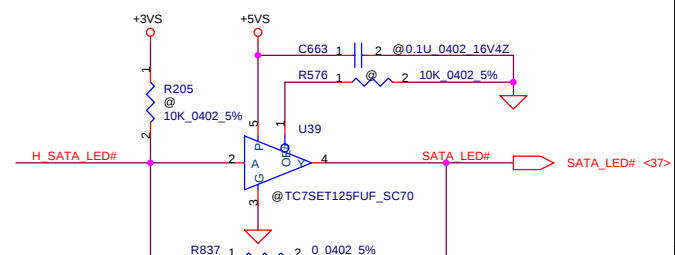
133MHz:Internal pull-down
66MHz:External pull-up

Remove R838 R839 R840 R552
Add RP43 Michael 2008/5/30

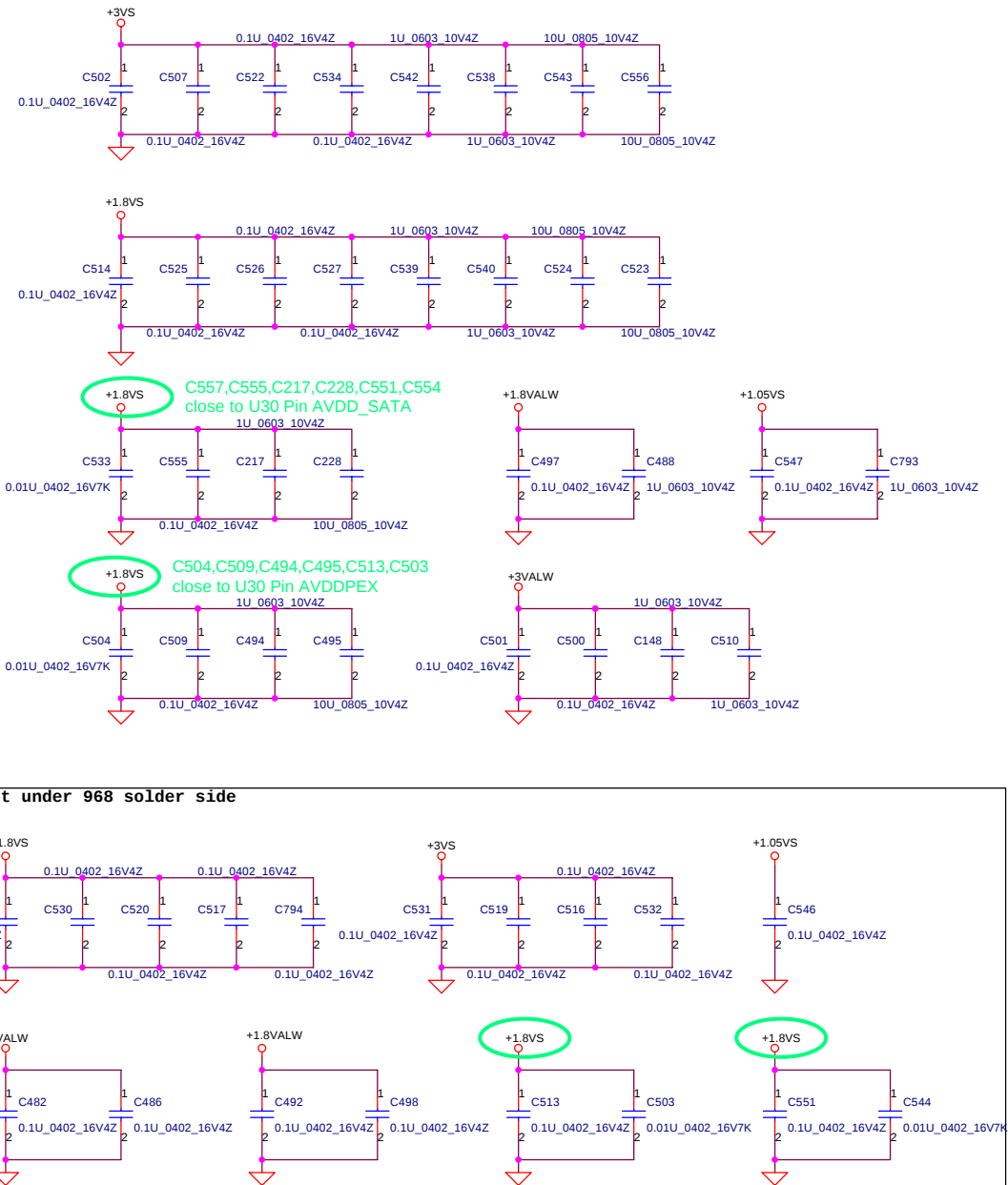
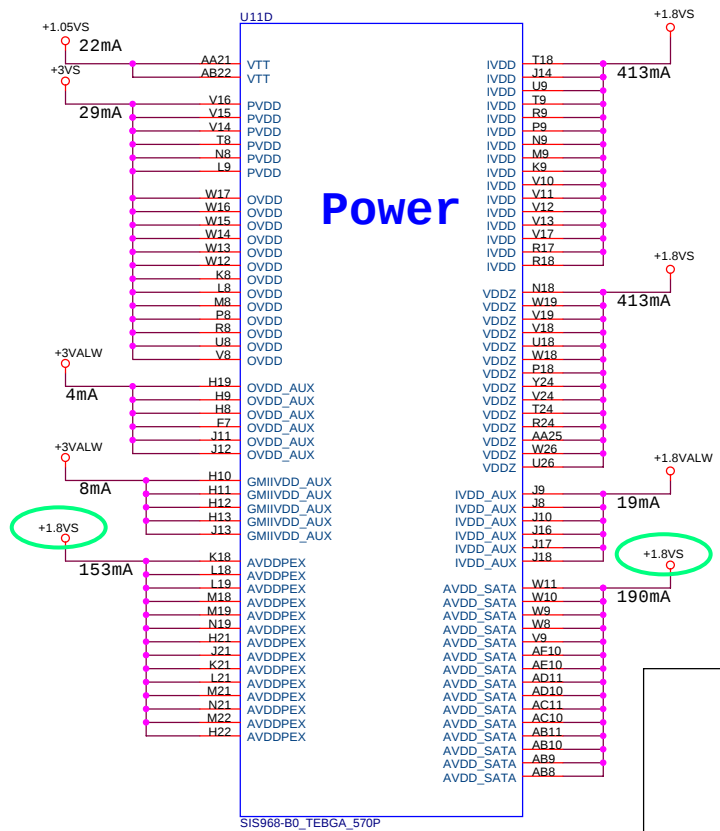


USB

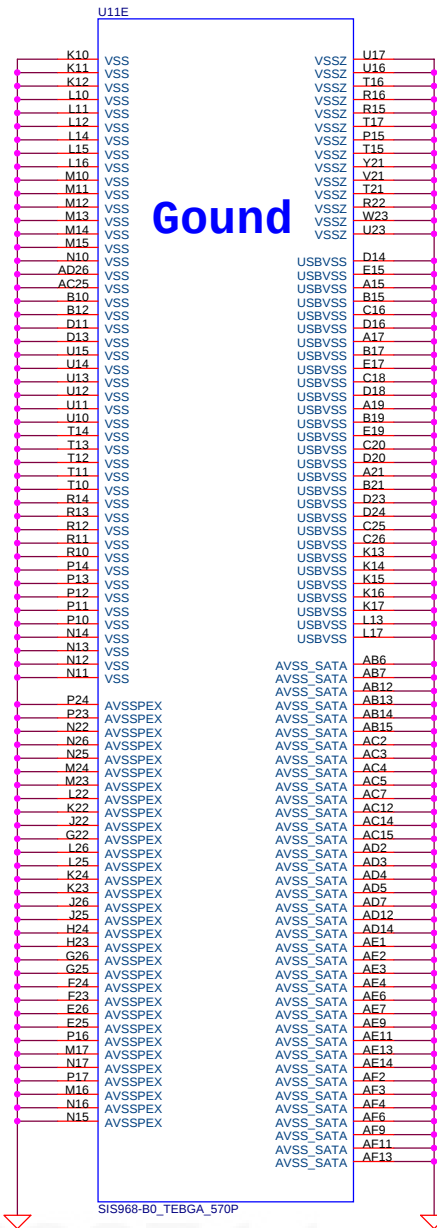
SATA



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				Custom	KSWXX M/B LA-3961P Schematic	0.1	
				Date:	Friday, August 01, 2008	Sheet	21 of 47

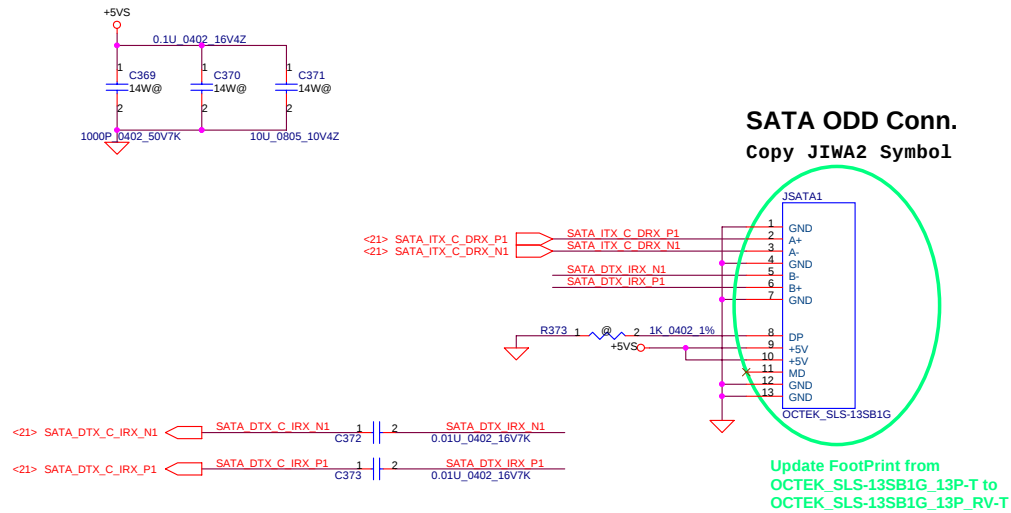


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Size	Custom	Document Number	KSWXX M/B LA-4611P Schematic		Rev 0.1
Date:	Friday, August 01, 2008	Sheet	22	of	47

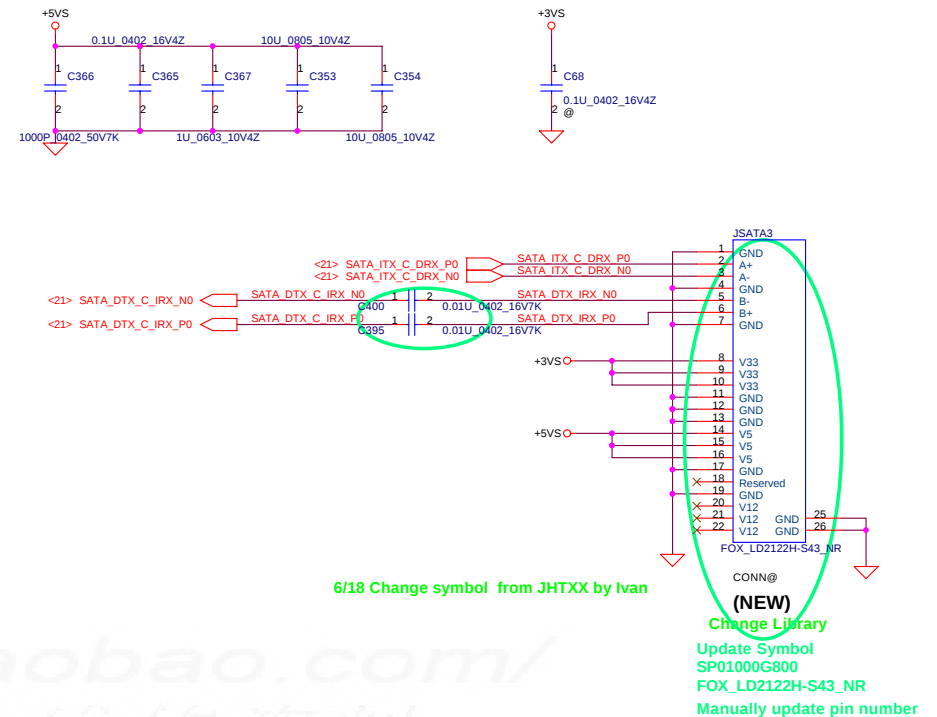


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				Size Custom	Rev 0.1
Date: Friday, August 01, 2008				Sheet 23 of 47	

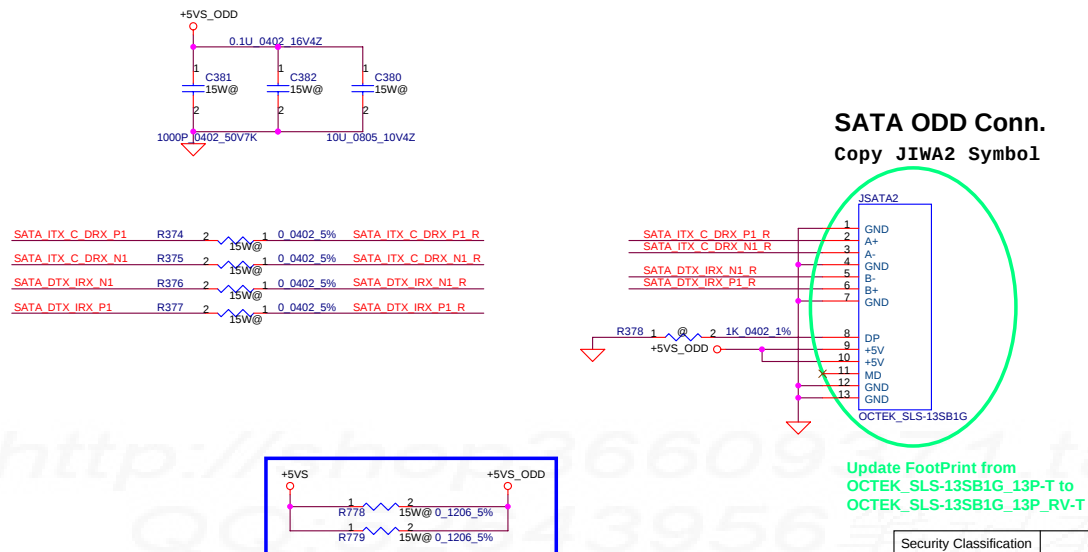
14W SATA ODD Conn.



SATA HDD Conn.

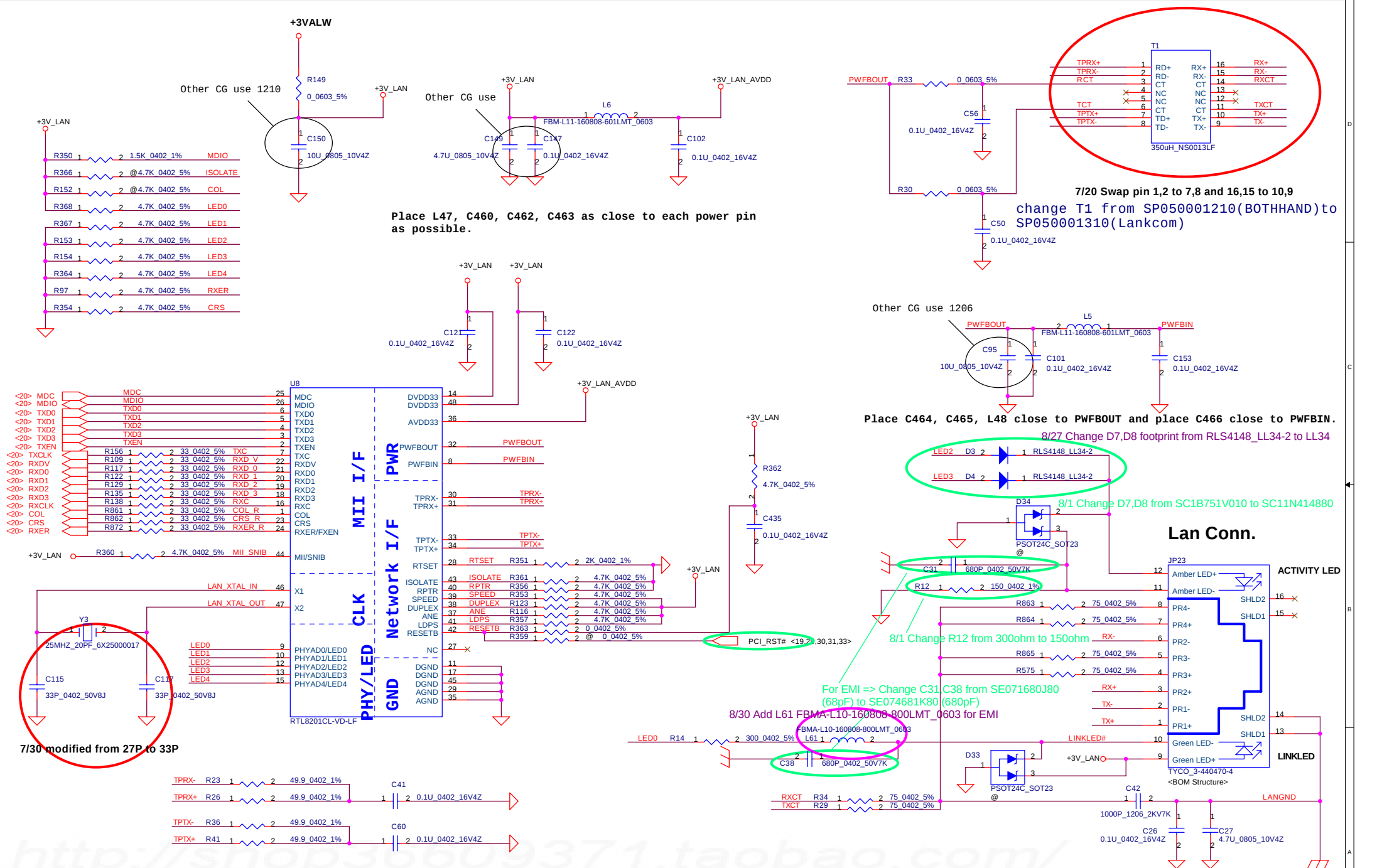


15W SATA ODD Conn.



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Issued Date	2008/05/15	Deciphered Date	2009/05/15	HDD & ODD Connector	
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				KSWXX M/B LA-4611P Schematic	
				Date: Friday, August 01, 2008	Rev 0.1
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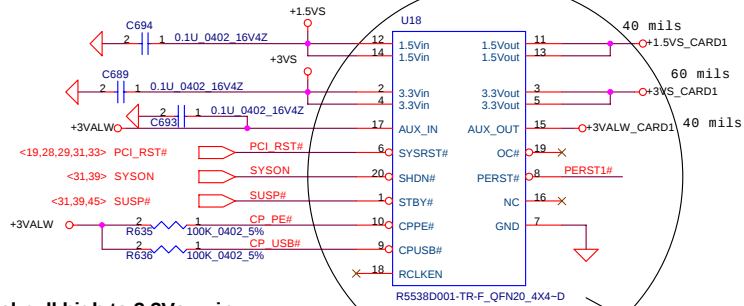
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D				D
C				C
B				B
A				A
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Security Classification		Compal Secret Data		Title
Issued Date	2008/05/15	Deciphered Date	2009/05/15	None
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		Custom	KSWXX M/B LA-4611P Schematic	0.1
Date: Friday, August 01, 2008		Sheet 27 of 47		
5	4	3	2	1



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/05/15	Deciphered Date	2009/05/15	Title Mini-Card/Kill SW		
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					KSWXX M/B LA-4611P Schematic	0.1
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New Card Power Switch

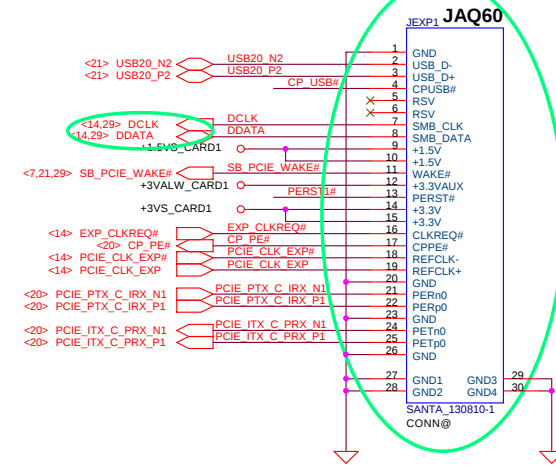
New Card



internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

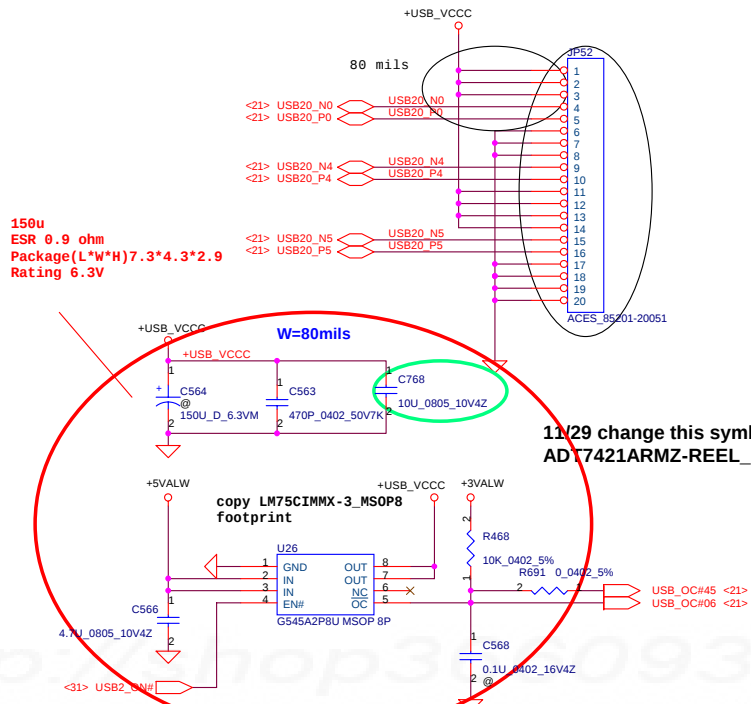
Change to GMT PartNumber

New Card Socket (Left/TOP)



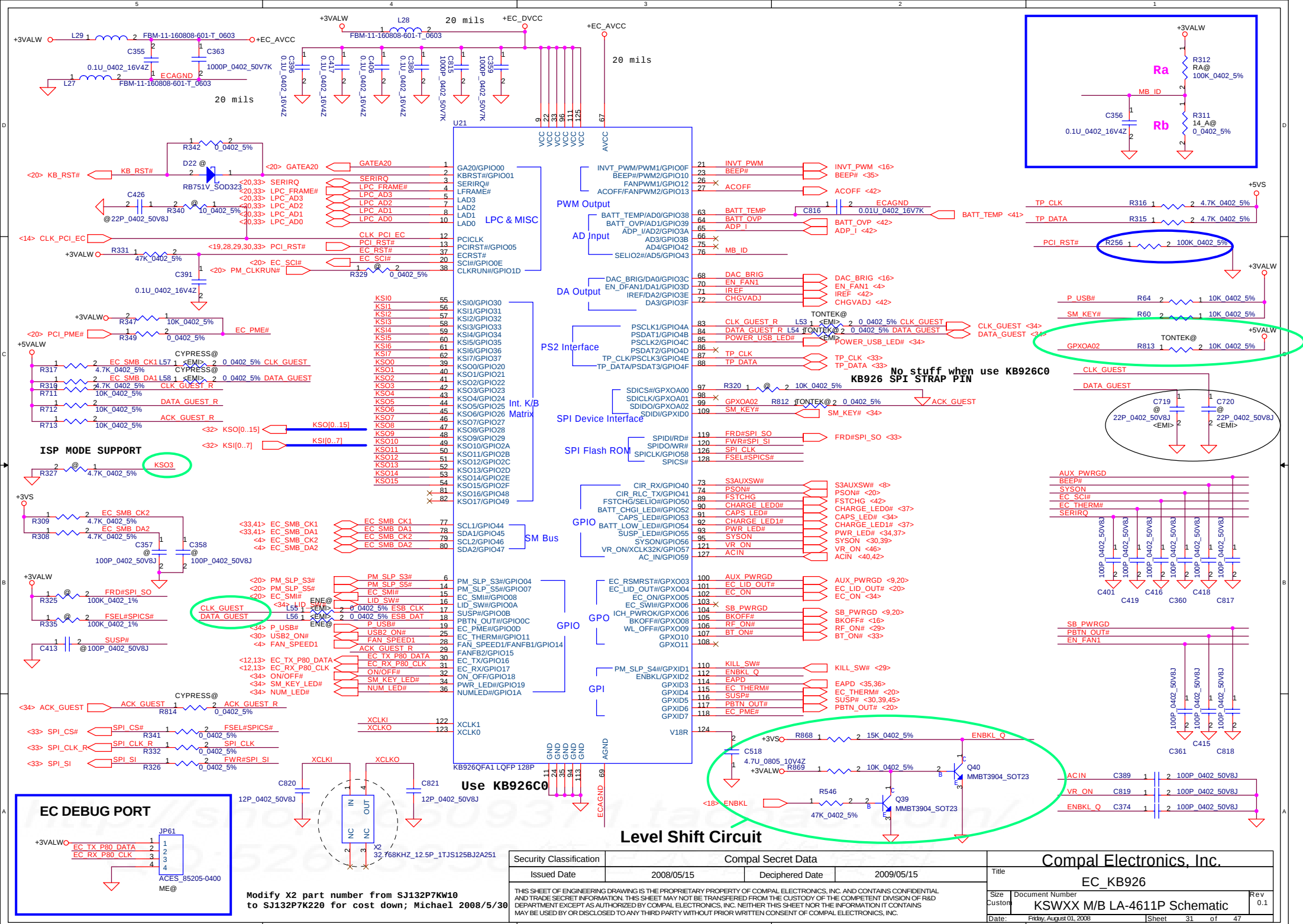
Update FootPrint from
SANTA_13181060-5_26P-T to
SANTA_130810-1_26P

USB IO Conn.



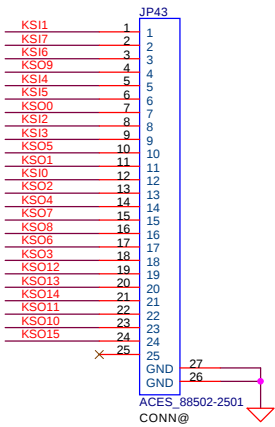
11/29 change this symbol's footprint as
AD7421ARMZ-REEL_MSOP8

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size B	Document Number	KSWXX M/B LA-4611P Schematic		Rev	0.1
Date:	Friday, August 01, 2008	Sheet	30	of	47

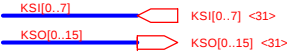
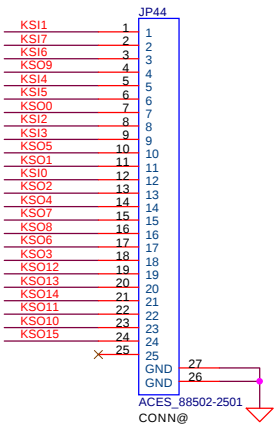


INT_KBD Conn.

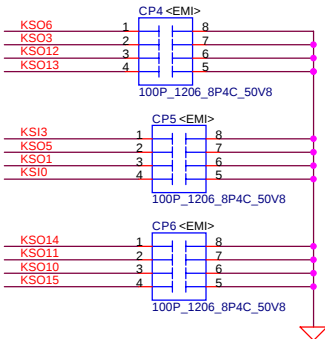
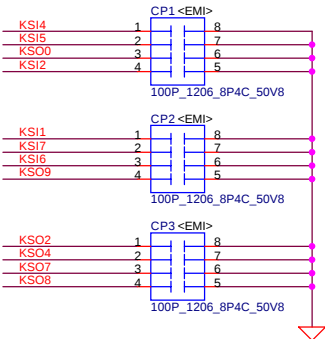
For KSW91



For KSW01

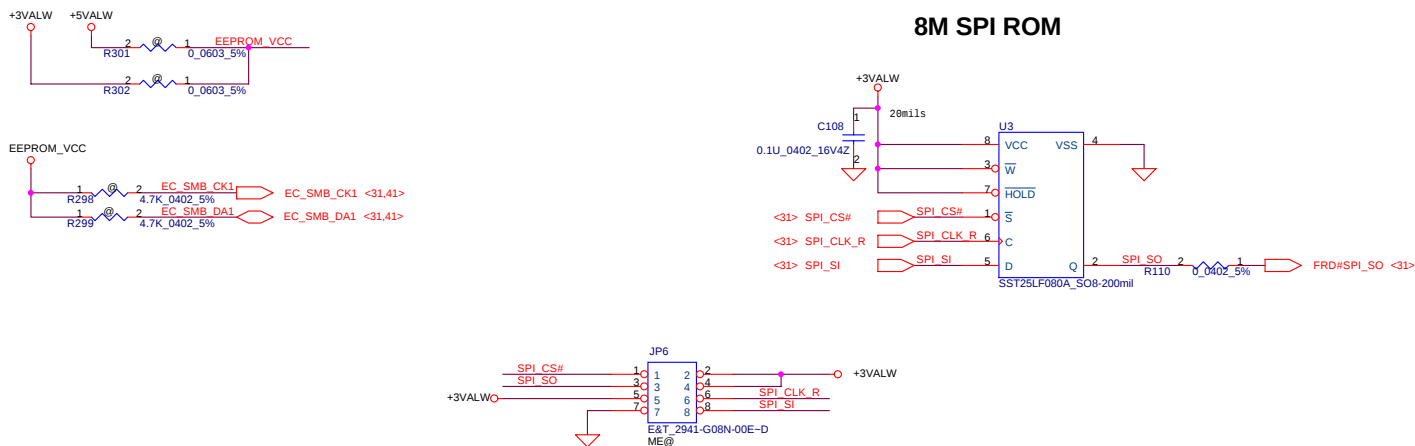


Delete C525~C548 SE071101J80 (100pF)
Add SI102101K80 (CP : 100pF)
(EMI Recommend)

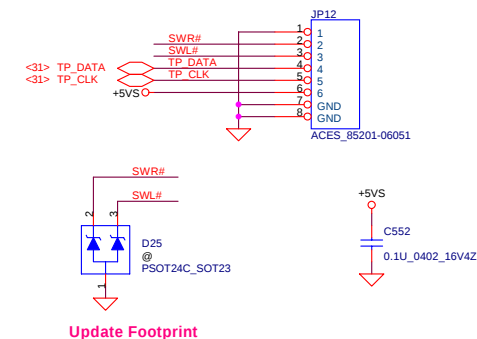


http://shop36609371.taobao.com/
QQ:52643956

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Size		Document Number			Rev
B		KSWXX M/B LA-4611P Schematic			0.1
Date:		Friday, August 01, 2008		Sheet	32 of 47

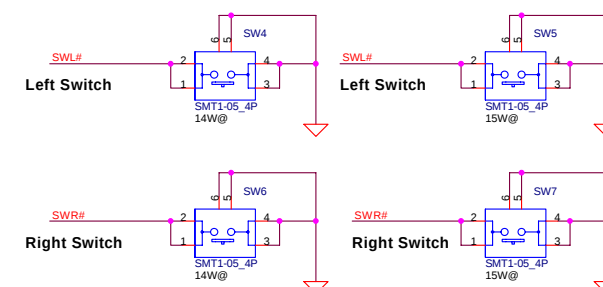


To TP/B Conn.



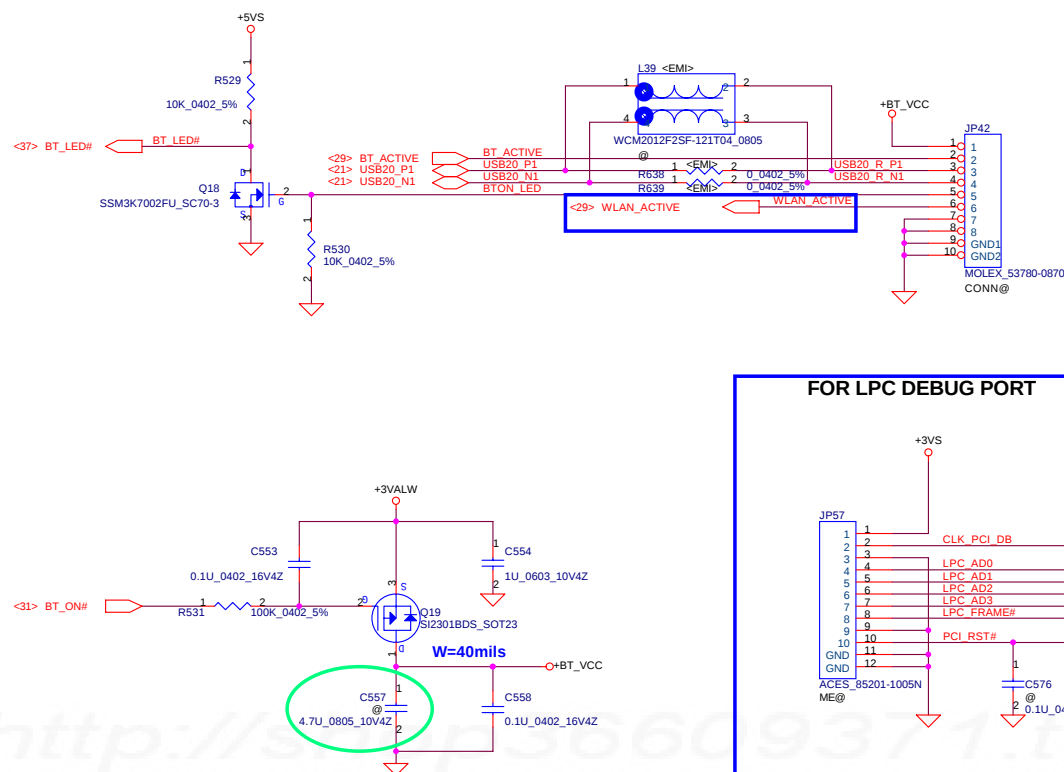
14W Use

15W Use

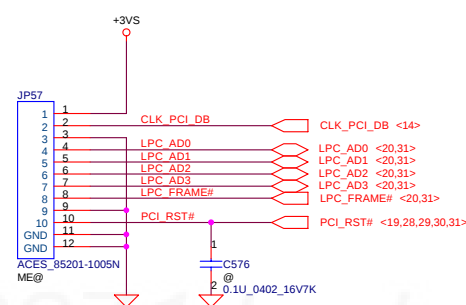


Bluetooth Conn.

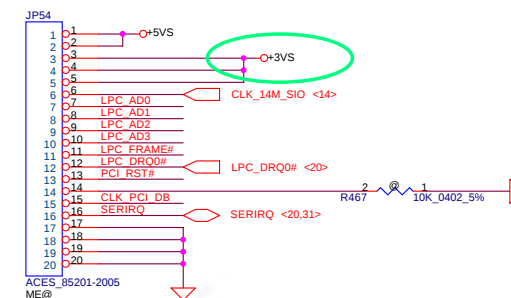
Need to check BT pin definition again!
9/20 modified this block



FOR LPC DEBUG PORT

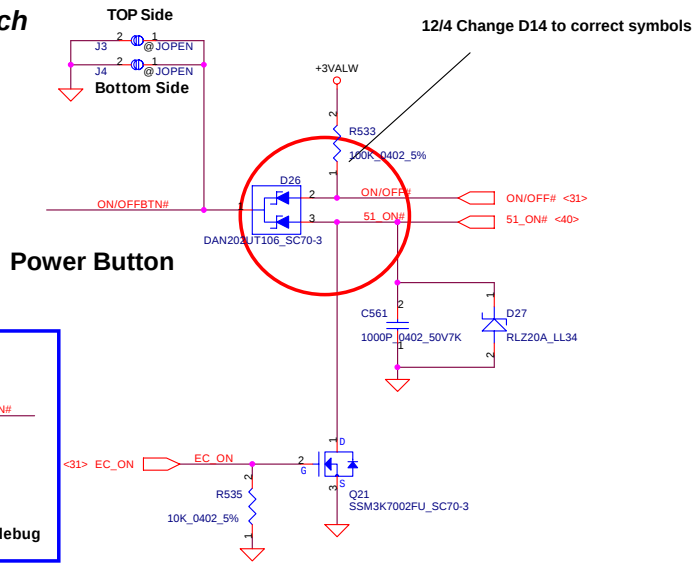
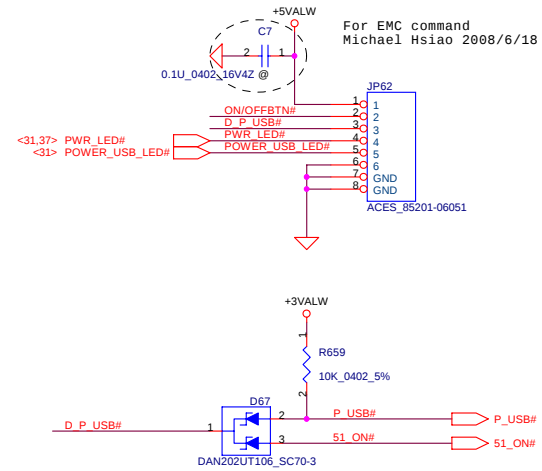
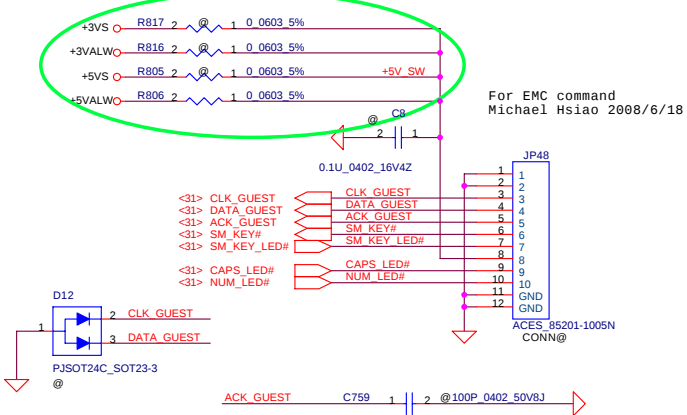


FOR LPC SIO DEBUG PORT

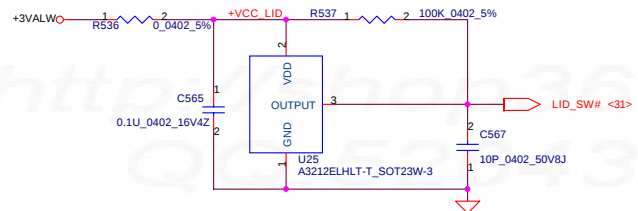


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Size B	Document Number	KSWXX M/B LA-4611P Schematic		Rev 0.1
Date:	Friday, August 01, 2008	Sheet	33 of 47	

ON/OFF switch

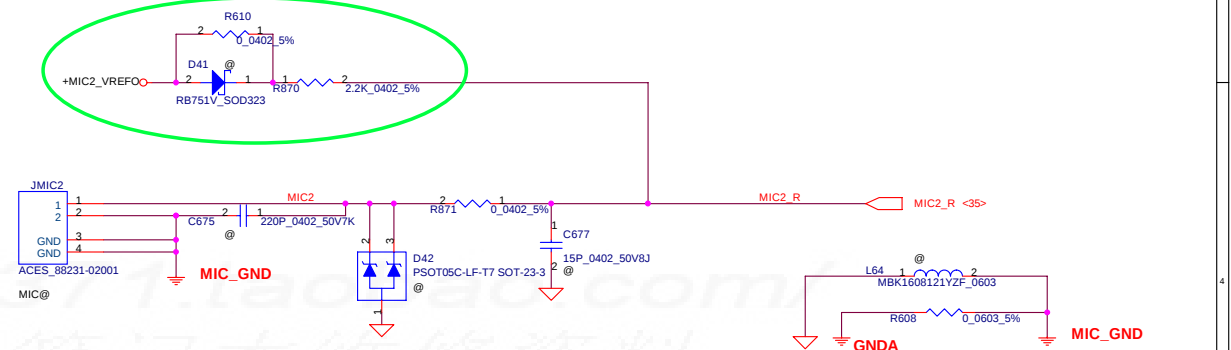
**Power USB Board Conn.****Function Board Conn.**

Lid Switch



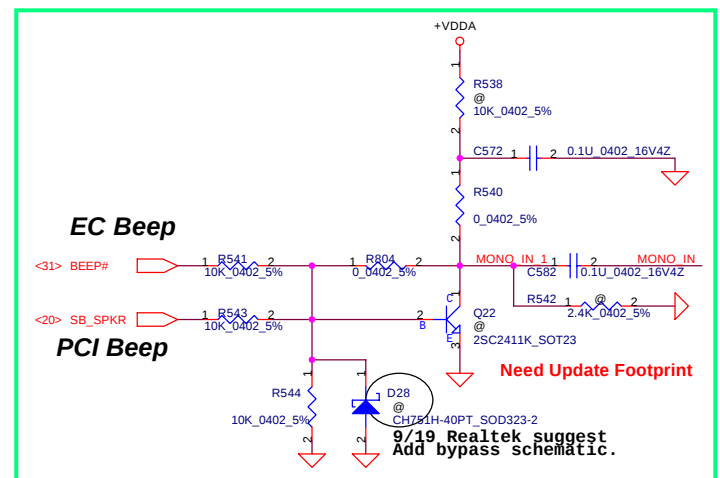
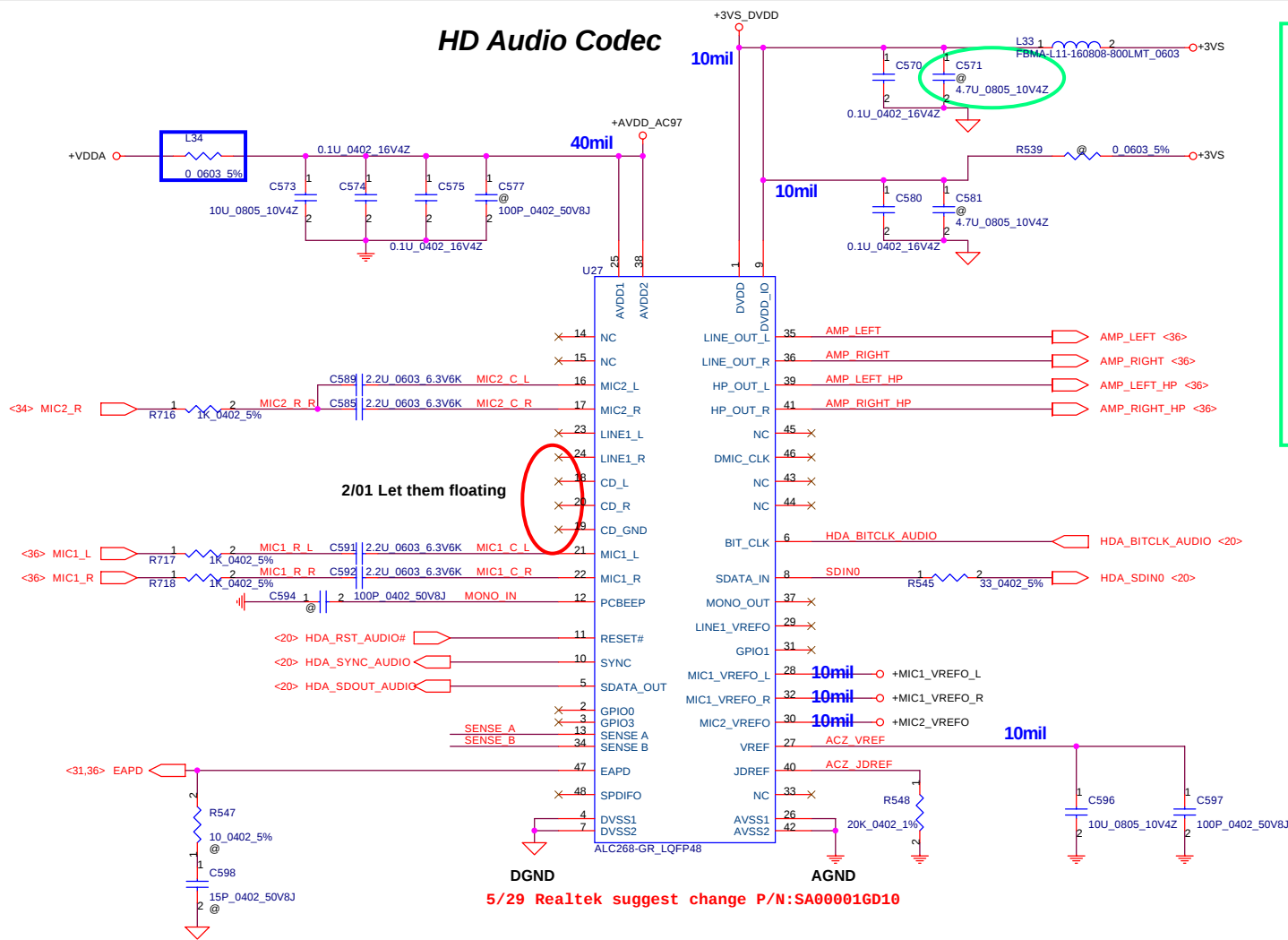
SINGLE INT MIC

05/29 close to codec



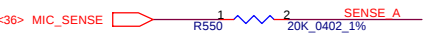
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2008/05/15	Deciphered Date	2009/05/15	Title			
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					Size B	Document Number		Rev 0.1
					KSWXX M/B LA-4611P Schematic			
Date:					Friday, August 01, 2008	Sheet	34 of 47	

HD Audio Codec

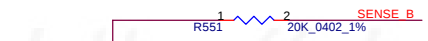


Sense Pin	Impedance	Codec Signals	Funnnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE OUT
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE OUT

SENSE FOR Ext. Mic.



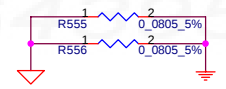
SENSE FOR Solo Int. Mic.



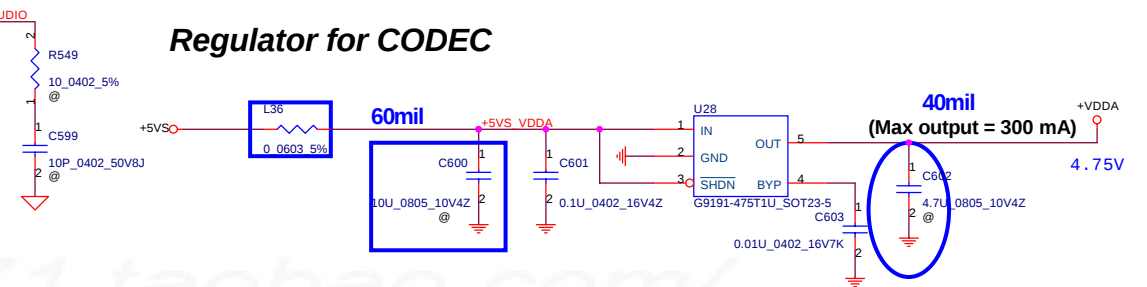
SENSE FOR HP



Moat Bridge



Regulator for CODEC



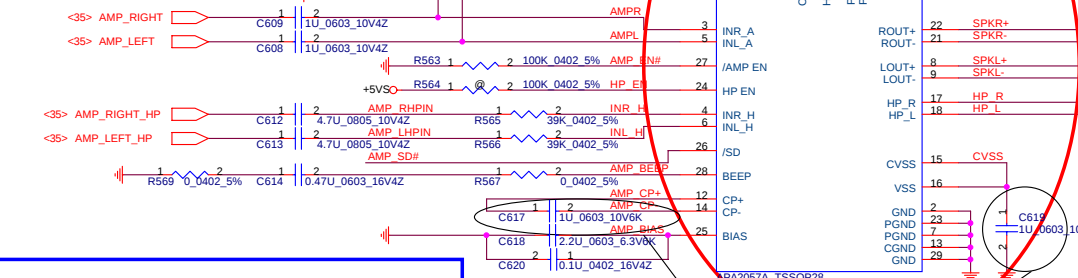
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/05/15	Deciphered Date	2009/05/15	Title <Title> HD Audio Codec ALC268	
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APA2057 SPK/HP Amplifier

10/2 U6 APA2057A P/N:SA00001QD00

$$f_0 = 1 / (2 * 3.14 * R * C) = 106\text{Hz}$$

$$R = 1.5\text{K} / C = 1\mu\text{F}$$

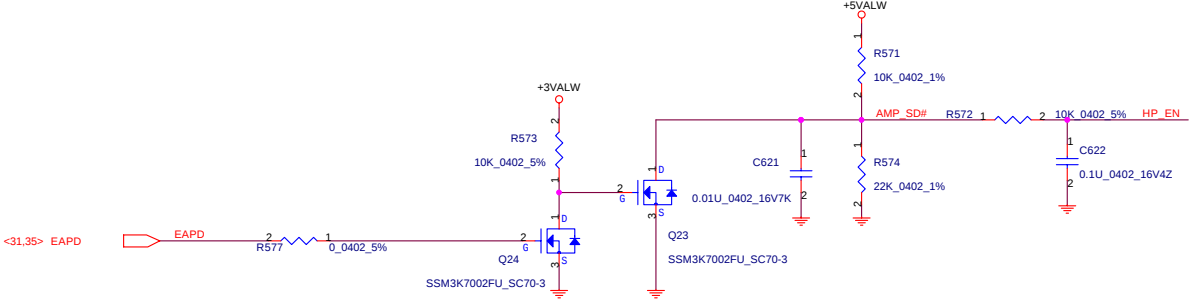


9/5 If implement AMP BEEP, Swap C641 and R524.
R524 change from 0 Ohm to 47K

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

11/28 Modified to X5R
11/28 Change to SE080105K80

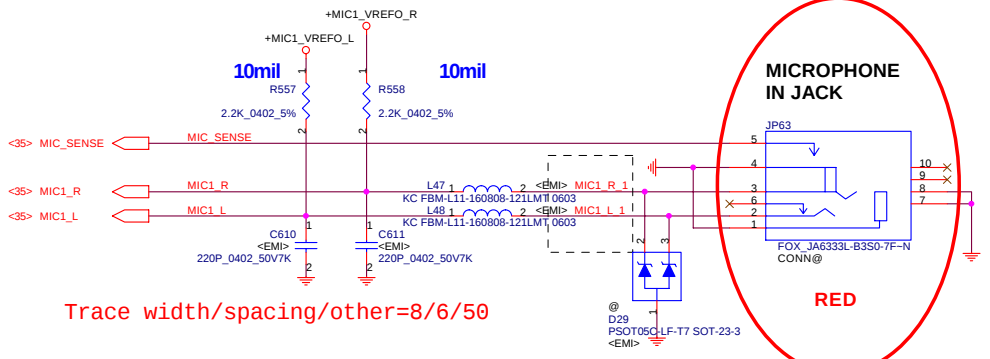
Add below circuit for APA2057 gain tuning use



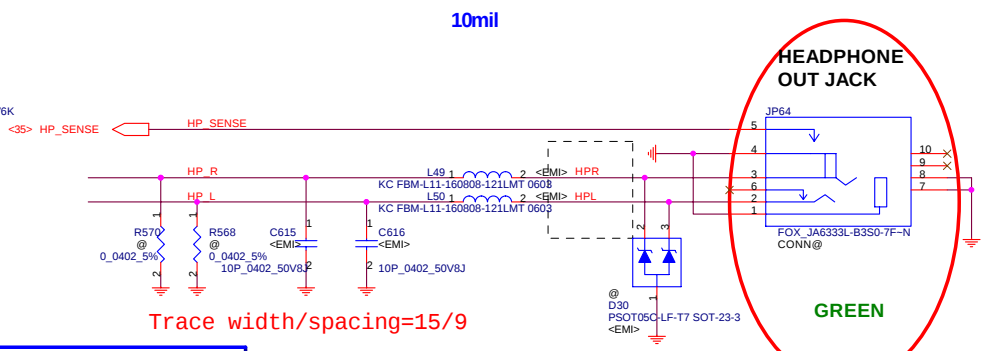
Gain= 10dB

Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

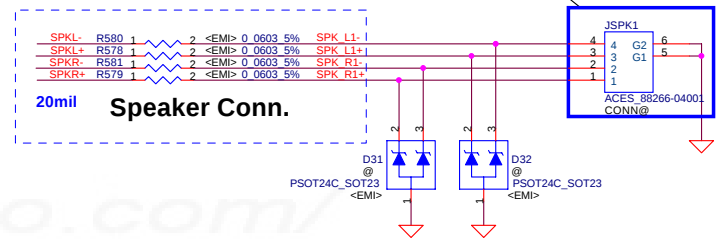
+5VALW assume equal 5.1V
10 dB ----> 5.1 x 220 / 320 = 3.5



Trace width/spacing/other=8/6/50



Trace width/spacing=15/9

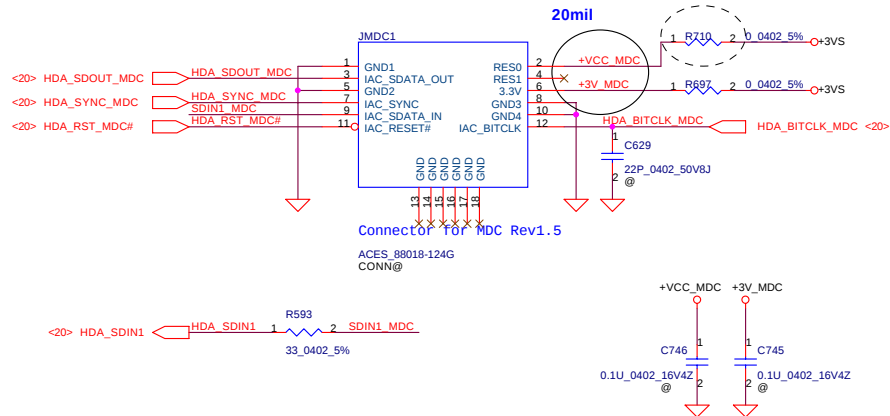


1/8 change JSPK1 following JAW91

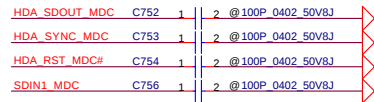
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	
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				Custom	KSWXX M/B LA-4611P Schematic
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MDC Conn.

Mount R710; Michael 2008/5/30

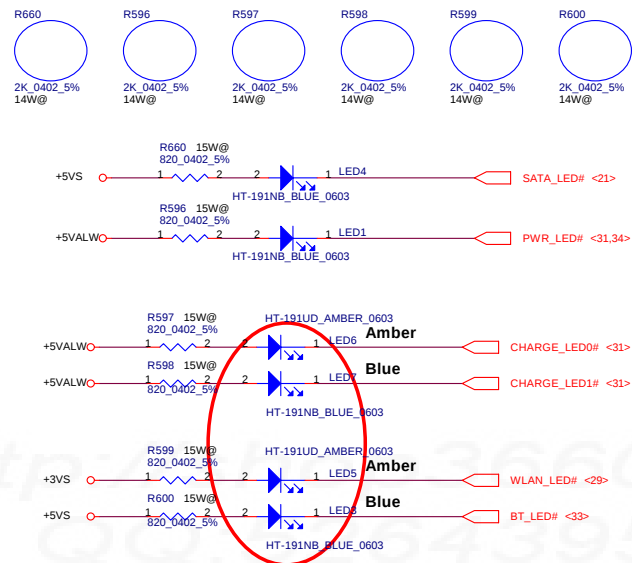


Please add these caps close to JMDC1 as close as possible,

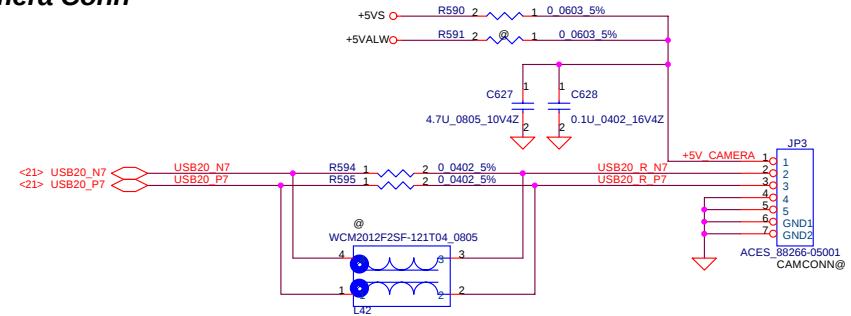


05/30 Change R660,R596,R597,R598,R599,R600 to 820ohm for 15W@
05/30 Add R660,R596,R597,R598,R599,R600 to 2kohm for 14W@; follow JHXXX

LED



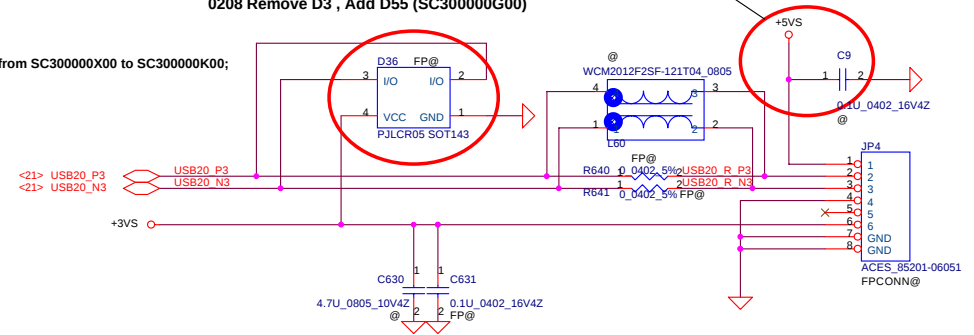
12/7 Modified LED footprint to LED_HT-297UD-CB_4P
12/15 Modified to correct LED symbol!

Camera Conn

Finger Print board

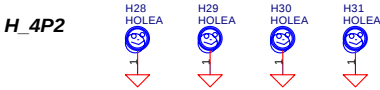
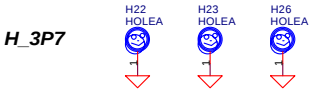
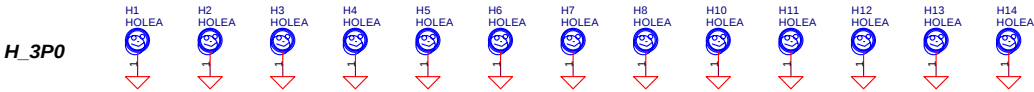
1/05 Modified D3 to SCA00000A00 For EMI 2/1 change JP4 pin 6 to +5VS for LTT FP use
0208 Remove D3 , Add D55 (SC300000G00)

05/26 Change D36 from SC300000X00 to SC300000K00;
Michael 2008/5/30



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								Size B	Document Number						Rev 0.1
								KSWXXX M/B LA-4611P Schematic							
								Date:		Friday, August 01, 2008			Sheet 37 of 47		

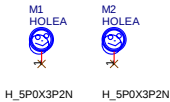
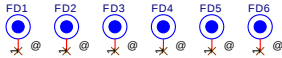
11/27 Add screw for layout request



2/22 change these from H_3P7 to H_3P8



2/22 change these from H_3P2 to H_3P3

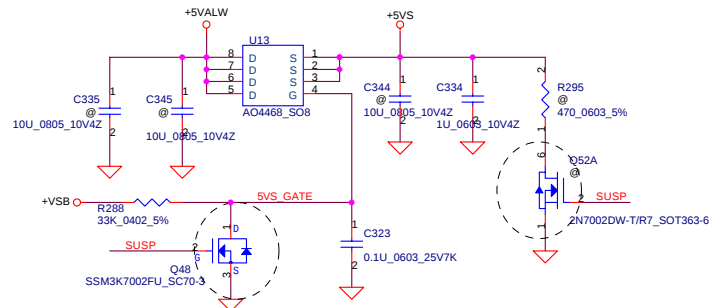


11/27 Add screw for layout request

<http://shop36609371.taobao.com/>
QQ:52643956

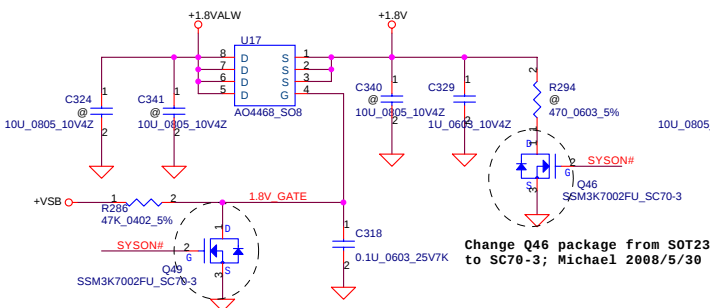
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/05/15		Deciphered Date	2009/05/15		Title
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				Size B	Document Number	Rev 0.1
				JFWXX M/B LA-3961P Schematic		
				Date:	Friday, August 01, 2008	Sheet 38 of 47

+5VALW TO +5VS



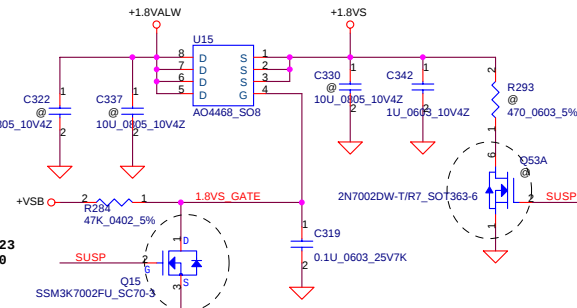
Change Q48 package from SOT23 to SC70-3; Michael 2008/5/30

+1.8VALW TO +1.8V



Change Q49 package from SOT23 to SC70-3; Michael 2008/5/30

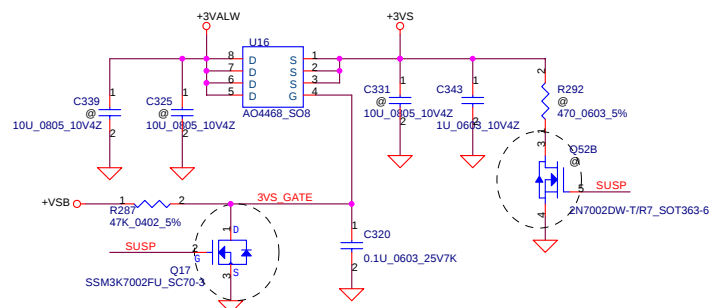
+1.8VALW to +1.8VS



Change Q15 package from SOT23 to SC70-3; Michael 2008/5/30

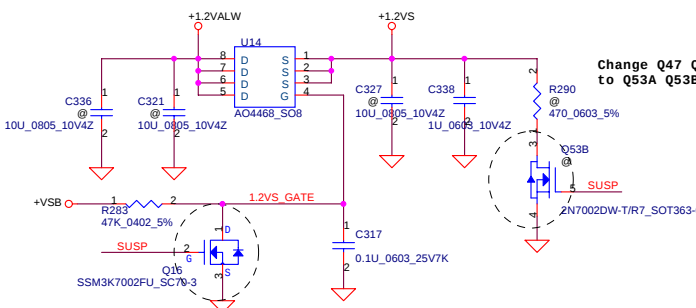
+3VALW TO +3VS

Change Q25 Q50 package from SOT23 to Q52A Q52B SOT363-6; Michael 2008/5/30



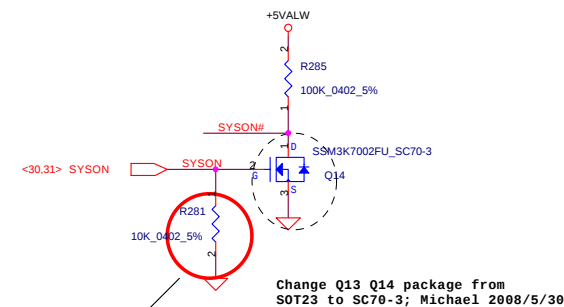
Change Q17 package from SOT23 to SC70-3; Michael 2008/5/30

+1.2VALW TO +1.2VS



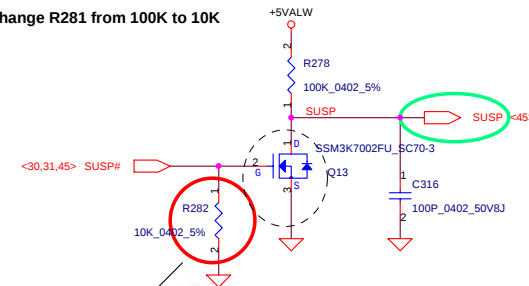
Change Q16 package from SOT23 to SC70-3; Michael 2008/5/30

Change Q47 Q51 package from SOT23 to Q53A Q53B SOT363-6; Michael 2008/5/30

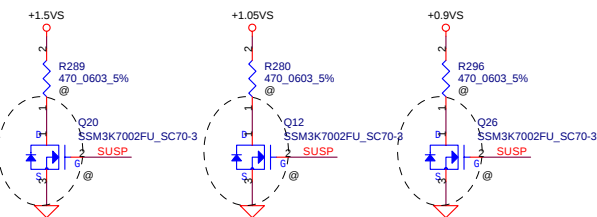


Change Q13 Q14 package from SOT23 to SC70-3; Michael 2008/5/30

7/24 Change R281 from 100K to 10K



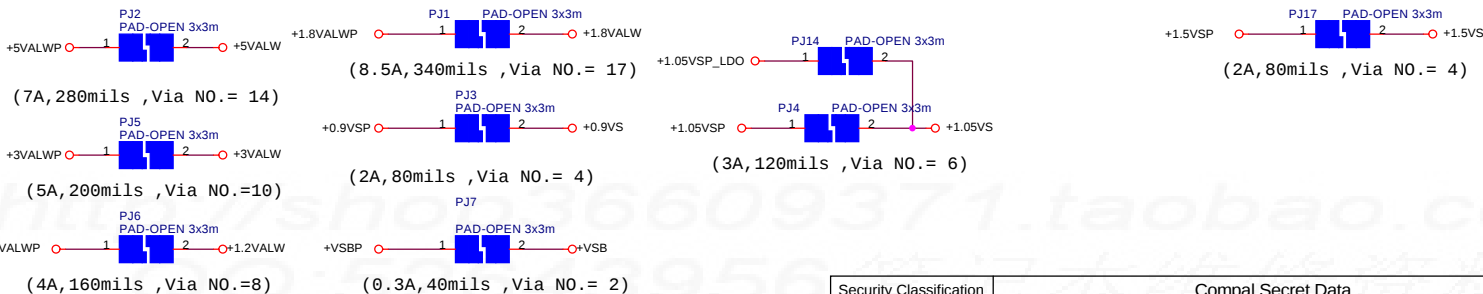
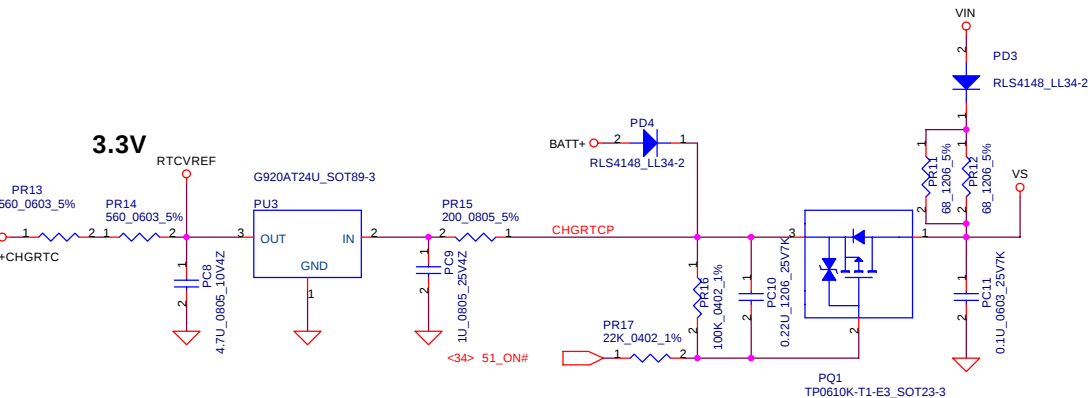
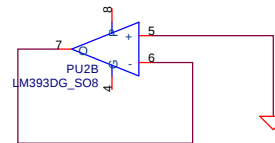
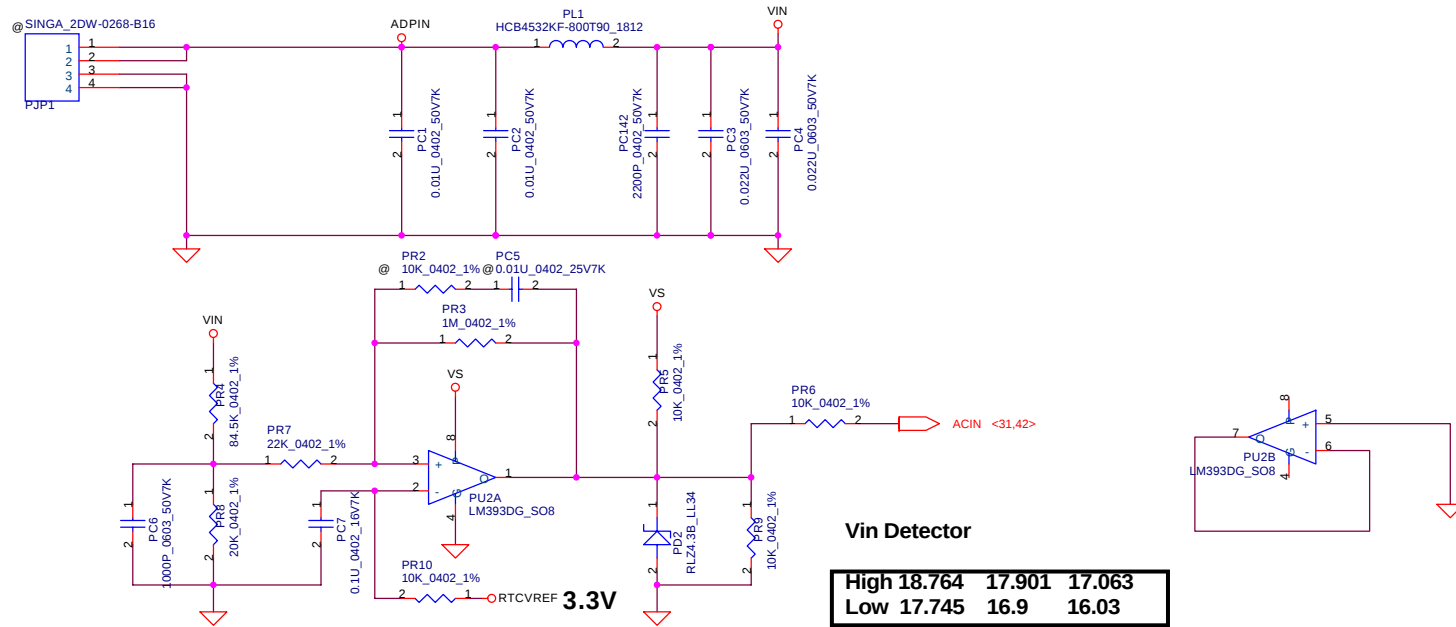
3/14 Change R16 from 100K to 10K



Change Q20 Q12 Q26 package from SOT23 to SC70-3; Michael 2008/5/30

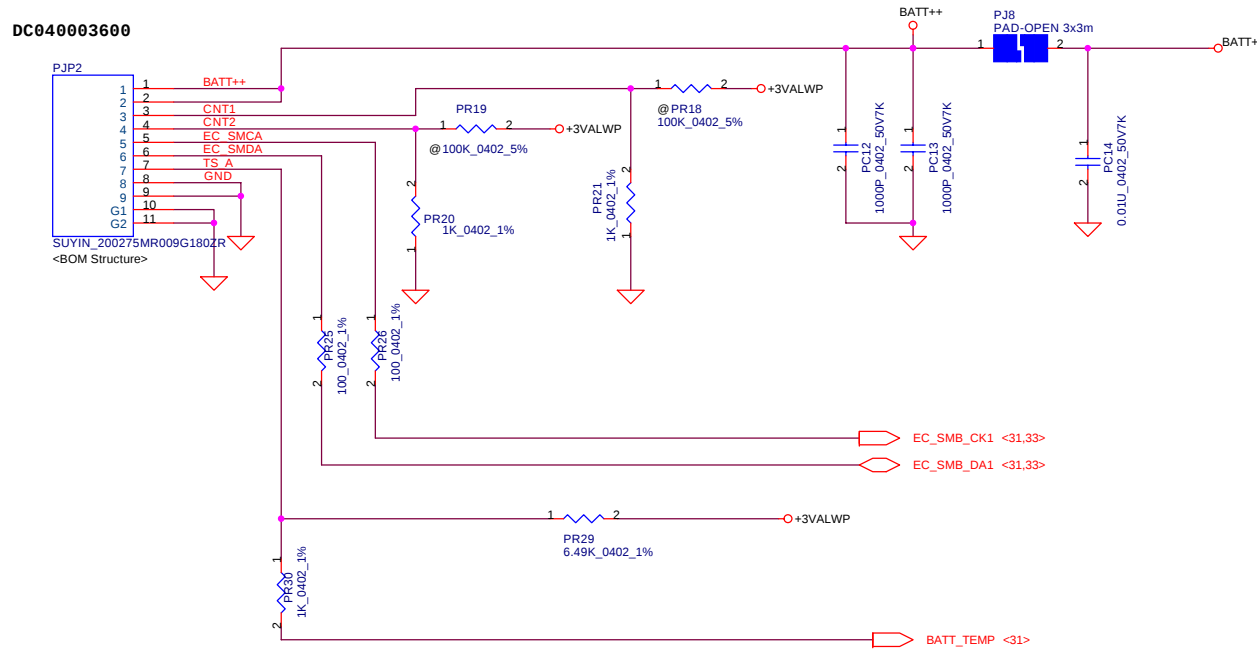
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Issued Date				2008/05/15				Title			
Deciphered Date				2009/05/15				DC Interface			
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								Rev 0.1			
								Date: Friday, August 01, 2008			
								Sheet 39 of 47			

DC301001Y00

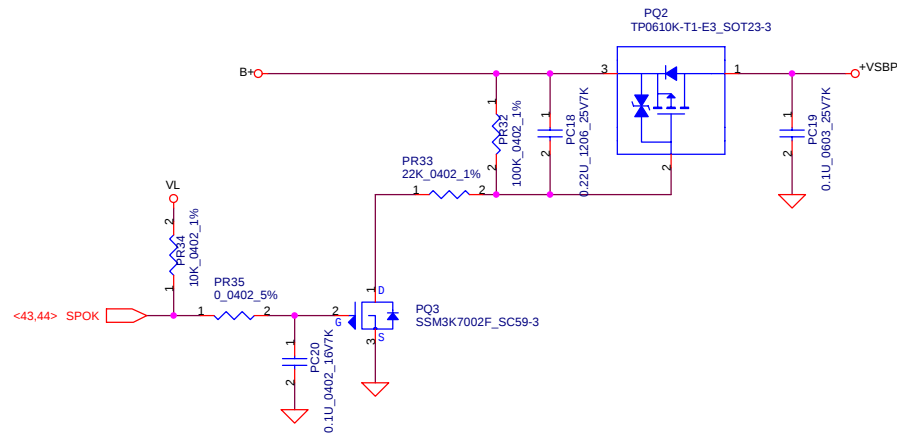
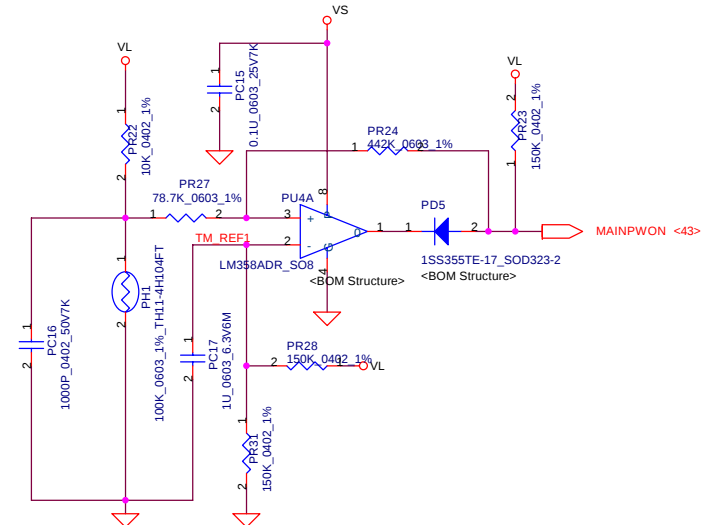


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				Deciphered Date				2006/10/17			
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								Rev			
								0.2			
								Date: Friday, August 01, 2008			
								Sheet 40 of 47			

DC040003600



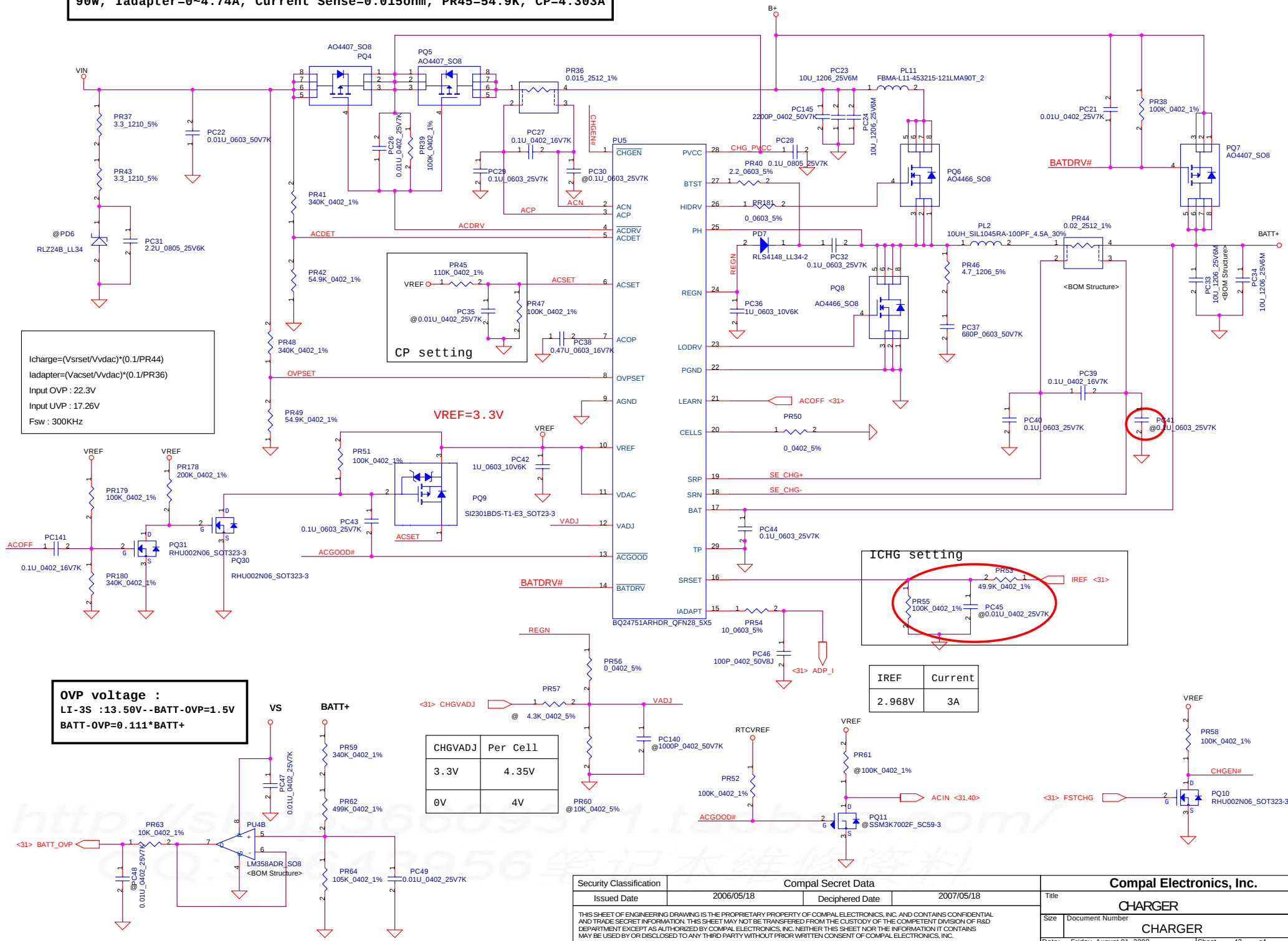
PH1 under CPU botten side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C

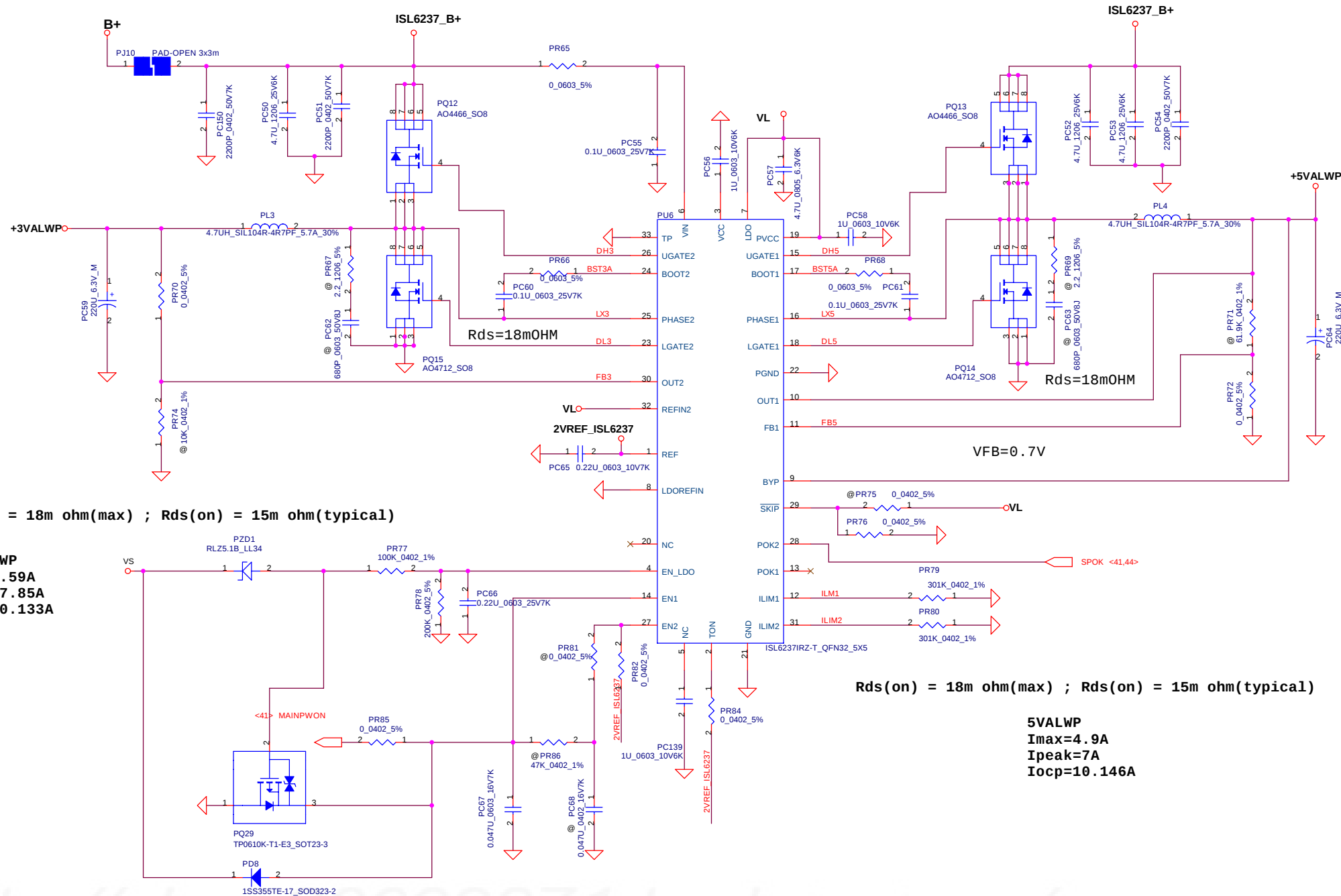


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QQ:52643956

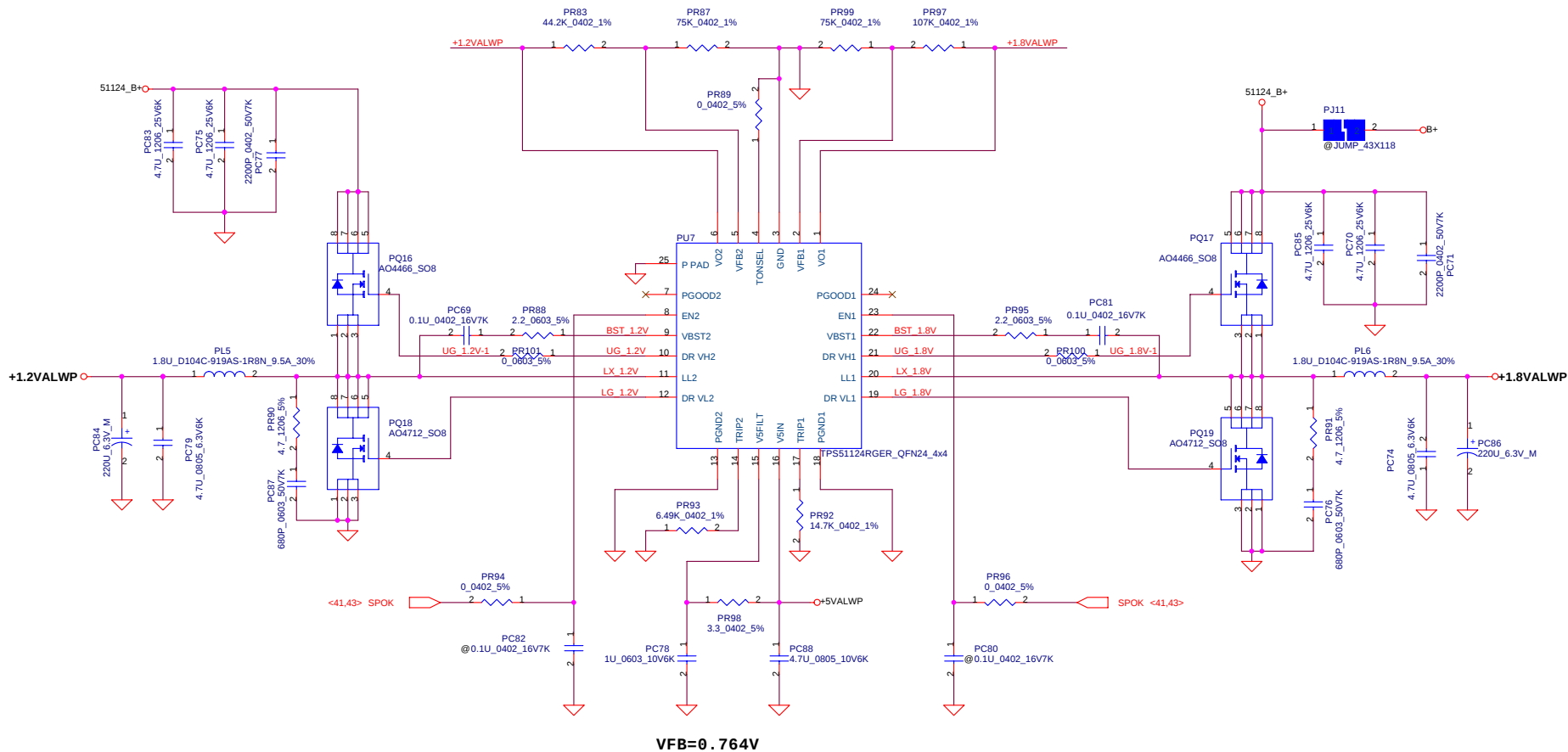
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Issued Date	2005/10/17	Deciphered Date	2006/10/17	Title	
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Date:	Friday, August 01, 2008			Sheet	41 of 47

65W, Iadapter=0~3.42A, Current sense=0.015ohm, PR45=110K, CP=3.175A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR45=54.9K, CP=4.303A

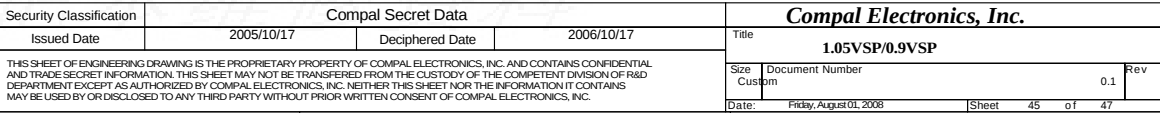




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				1.5VP/1.8VP	
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page	Reason for change	Modify list
PVT	Add PR46 & PC37 for EMI request	
	Add bead at charger B+ for EMI request	
	Add PR141,PR144,PC116,PR155,PR157,PC125 for EMI power board band noise.	
	Add PC87,PR90,PR88,PR95,PR91,PC76 for EMI power board band noise.	
	Add PR113,PR117,PC98 for EMI power board band niose.	
	Change 1.8V from 1.836 to 1.853. S0 PR97 to 107K for HW request	
	Change PR176 to 3.92K for adjust Loadline	
	Change PC97 to 220UF form EVT SMT MEMO	

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QQ:52643956 笔记本维修资料

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Date:	Friday, August 01, 2008	Sheet 47 of 47