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IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M
(With nVIDIA MXM/B)

2006-11-01

REV: 0.1

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(PIRQ#,PIRQD#,
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(PIRQ#,PIRQH#,
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

Close to CPU pin AD26
within 500mils.



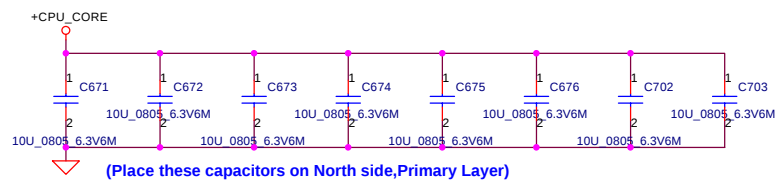
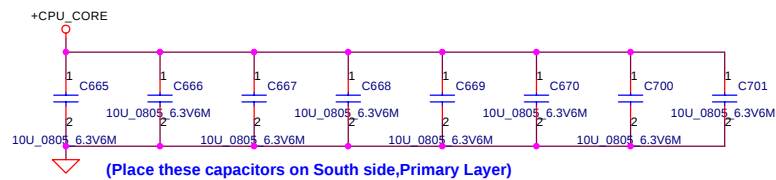
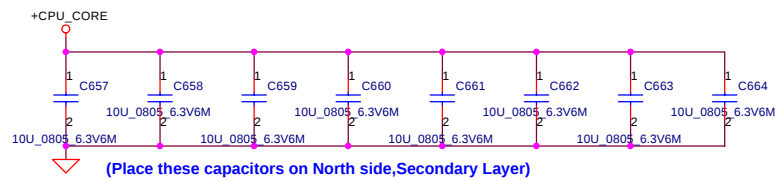
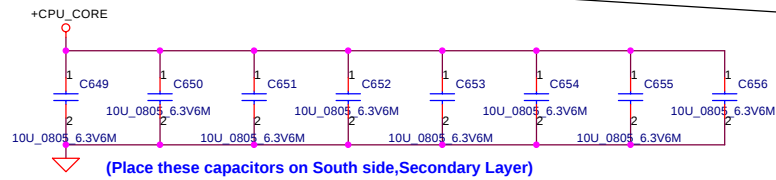
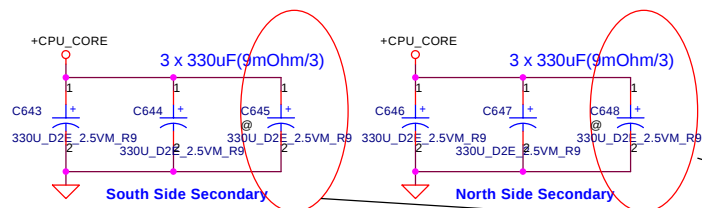
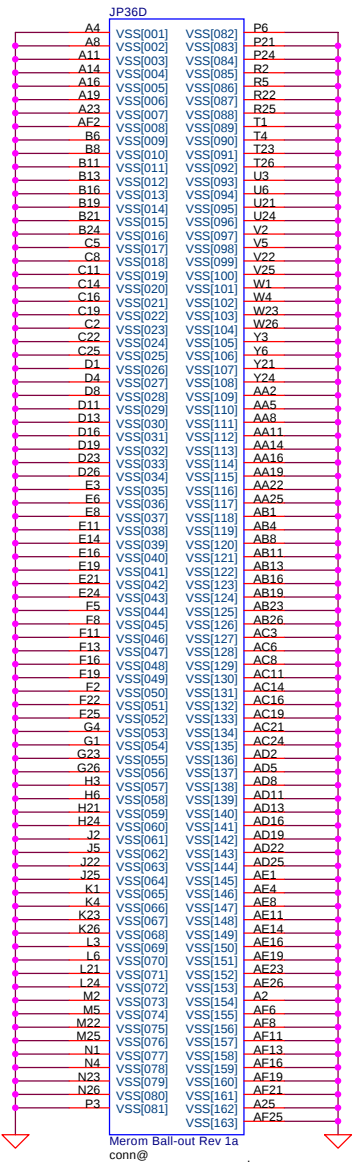
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

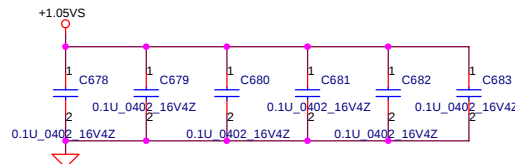
Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any other
toggling signal.
COMP[0,2] trace width is
18 mils. COMP[1,3] trace
width is 4 mils.

Length match within 25 mils.
The trace width/space/other is
20/7/25.

Close to CPU pin
within 500mils.



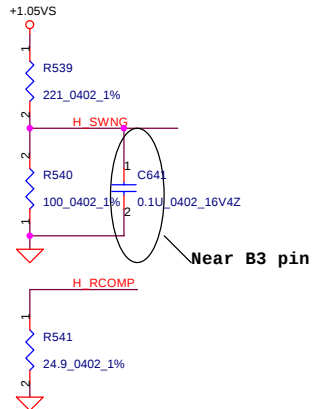
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



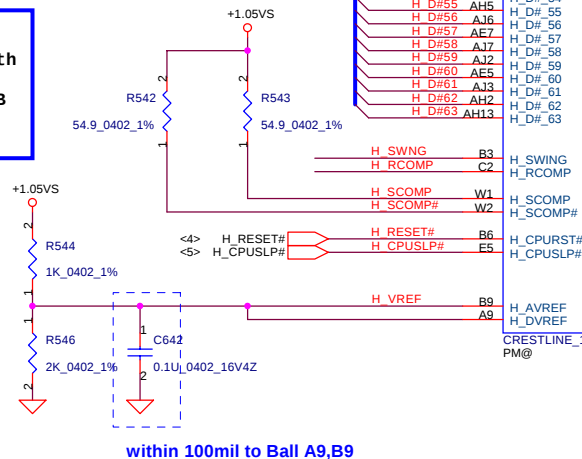
CRB no stuff. Reserved!

9/25 10U checked. OK for use!

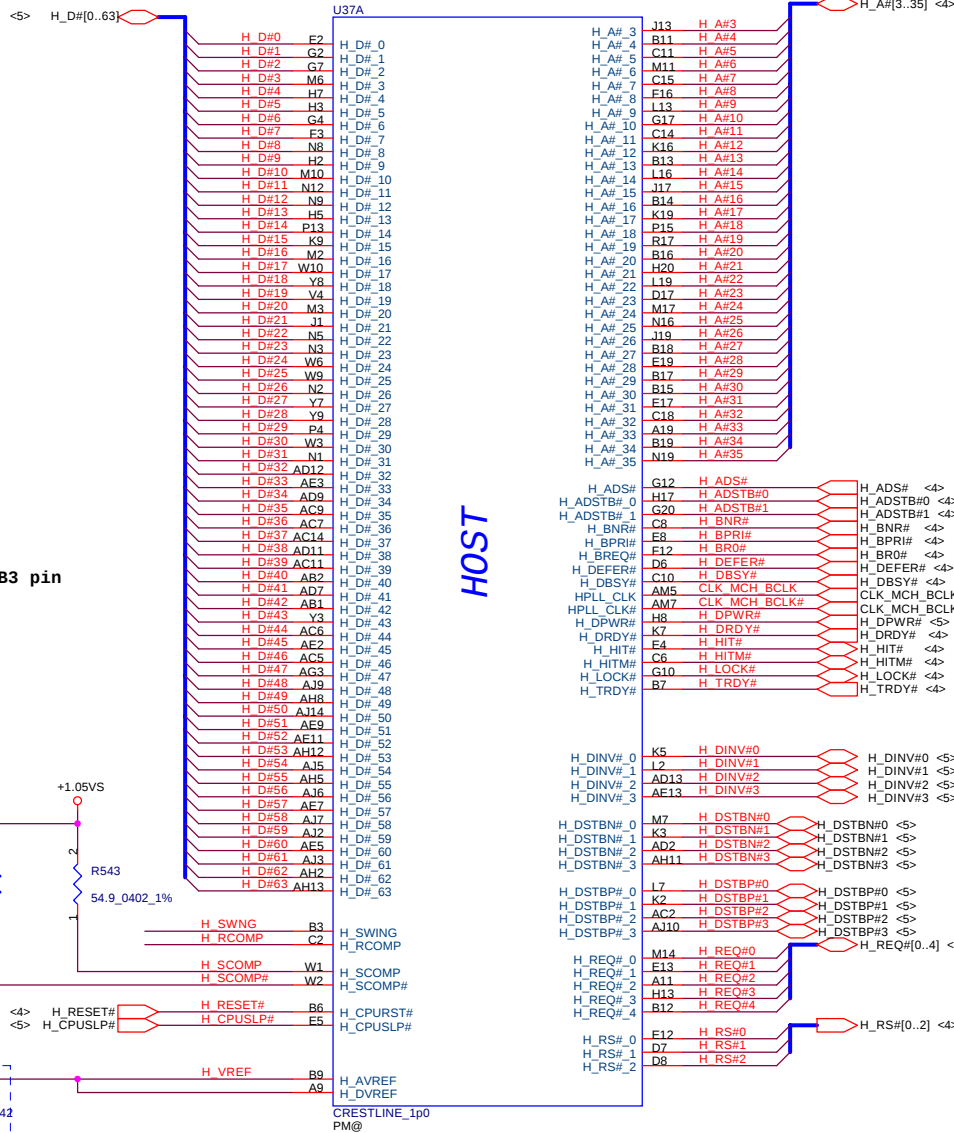
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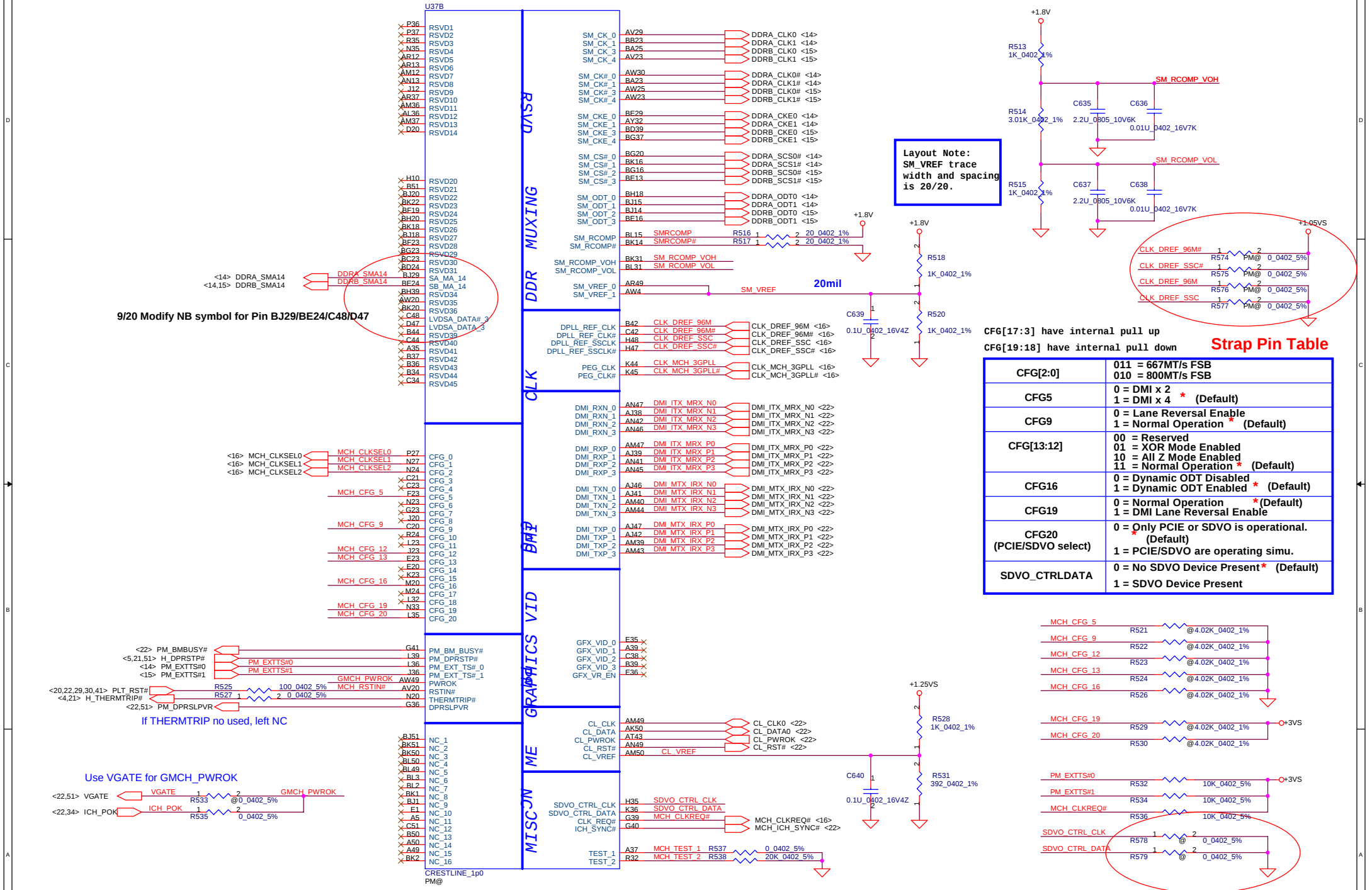
layout note:
Route H_SCOMP and H_SCOMP# with
trace width, spacing and
impedance (55 ohm) same as FSB
data traces



Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



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<14> DDRA_SDQ[0..63] <14> DDRA_SDM[0..7] <14> DDRA_SMA[0..13]

<15> DDRB_SDQ[0..63] <15> DDRB_SDM[0..7] <15> DDRB_SMA[0..13]

U37D
DDRA_SDQ0 AR43 SA_DQ_0
DDRA_SDQ1 AW44 SA_DQ_1
DDRA_SDQ2 BA45 SA_DQ_2
DDRA_SDQ3 AY46 SA_DQ_3
DDRA_SDQ4 AR41 SA_DQ_4
DDRA_SDQ5 AR45 SA_DQ_5
DDRA_SDQ6 AT42 SA_DQ_6
DDRA_SDQ7 AW47 SA_DQ_7
DDRA_SDQ8 BB45 SA_DQ_8
DDRA_SDQ9 BF48 SA_DQ_9
DDRA_SDQ10 BG47 SA_DQ_10
DDRA_SDQ11 BA45 SA_DQ_11
DDRA_SDQ12 BB47 SA_DQ_12
DDRA_SDQ13 BG50 SA_DQ_13
DDRA_SDQ14 BH49 SA_DQ_14
DDRA_SDQ15 BE45 SA_DQ_15
DDRA_SDQ16 AW44 SA_DQ_16
DDRA_SDQ17 BE44 SA_DQ_17
DDRA_SDQ18 BG42 SA_DQ_18
DDRA_SDQ19 BE40 SA_DQ_19
DDRA_SDQ20 BF44 SA_DQ_20
DDRA_SDQ21 BH45 SA_DQ_21
DDRA_SDQ22 BG40 SA_DQ_22
DDRA_SDQ23 BE40 SA_DQ_23
DDRA_SDQ24 AR40 SA_DQ_24
DDRA_SDQ25 AW40 SA_DQ_25
DDRA_SDQ26 AT39 SA_DQ_26
DDRA_SDQ27 AW36 SA_DQ_27
DDRA_SDQ28 AW41 SA_DQ_28
DDRA_SDQ29 AY41 SA_DQ_29
DDRA_SDQ30 AV38 SA_DQ_30
DDRA_SDQ31 AT38 SA_DQ_31
DDRA_SDQ32 AV13 SA_DQ_32
DDRA_SDQ33 AT13 SA_DQ_33
DDRA_SDQ34 AW11 SA_DQ_34
DDRA_SDQ35 AV11 SA_DQ_35
DDRA_SDQ36 AU15 SA_DQ_36
DDRA_SDQ37 AT11 SA_DQ_37
DDRA_SDQ38 BA13 SA_DQ_38
DDRA_SDQ39 RA11 SA_DQ_39
DDRA_SDQ40 BE10 SA_DQ_40
DDRA_SDQ41 BD10 SA_DQ_41
DDRA_SDQ42 BD8 SA_DQ_42
DDRA_SDQ43 AY9 SA_DQ_43
DDRA_SDQ44 BG10 SA_DQ_44
DDRA_SDQ45 AW9 SA_DQ_45
DDRA_SDQ46 BD7 SA_DQ_46
DDRA_SDQ47 BB9 SA_DQ_47
DDRA_SDQ48 BB5 SA_DQ_48
DDRA_SDQ49 AY7 SA_DQ_49
DDRA_SDQ50 AT5 SA_DQ_50
DDRA_SDQ51 AT7 SA_DQ_51
DDRA_SDQ52 AY6 SA_DQ_52
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DDRA_SDQ56 AR9 SA_DQ_56
DDRA_SDQ57 AN3 SA_DQ_57
DDRA_SDQ58 AM8 SA_DQ_58
DDRA_SDQ59 AN10 SA_DQ_59
DDRA_SDQ60 AT9 SA_DQ_60
DDRA_SDQ61 AN9 SA_DQ_61
DDRA_SDQ62 AM9 SA_DQ_62
DDRA_SDQ63 AN11 SA_DQ_63

CRESTLINE_1p0
PM@

DDR SYSTEM MEMORY A

SA_BS_0 BB19 DDRA_SBS0 <14>
SA_BS_1 BK19 DDRA_SBS1 <14>
SA_BS_2 BF29 DDRA_SBS2 <14>
SA_CAS# BL17 DDRA_SCAS# <14>
SA_DM_0 AT45 DDRA_SDM0 <14>
SA_DM_1 BD44 DDRA_SDM1 <14>
SA_DM_2 BD42 DDRA_SDM2 <14>
SA_DM_3 AW38 DDRA_SDM3 <14>
SA_DM_4 AW13 DDRA_SDM4 <14>
SA_DM_5 BG8 DDRA_SDM5 <14>
SA_DM_6 AV5 DDRA_SDM6 <14>
SA_DM_7 AN6 DDRA_SDM7 <14>
SA_DQS_0 AT46 DDRA_SDQS0 <14>
SA_DQS_1 BE48 DDRA_SDQS1 <14>
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SA_DQS_3 BC37 DDRA_SDQS3 <14>
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SA_DQS#_6 BC1 DDRA_SDQS6# <14>
SA_DQS#_7 AP2 DDRA_SDQS7# <14>
SA_MA_0 BJ19 DDRA_SMA0 <14>
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SA_MA_4 BL24 DDRA_SMA4 <14>
SA_MA_5 BK28 DDRA_SMA5 <14>
SA_MA_6 BJ27 DDRA_SMA6 <14>
SA_MA_7 BJ25 DDRA_SMA7 <14>
SA_MA_8 BL28 DDRA_SMA8 <14>
SA_MA_9 BA28 DDRA_SMA9 <14>
SA_MA_10 BC19 DDRA_SMA10 <14>
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SA_MA_12 BG30 DDRA_SMA12 <14>
SA_MA_13 BJ16 DDRA_SMA13 <14>
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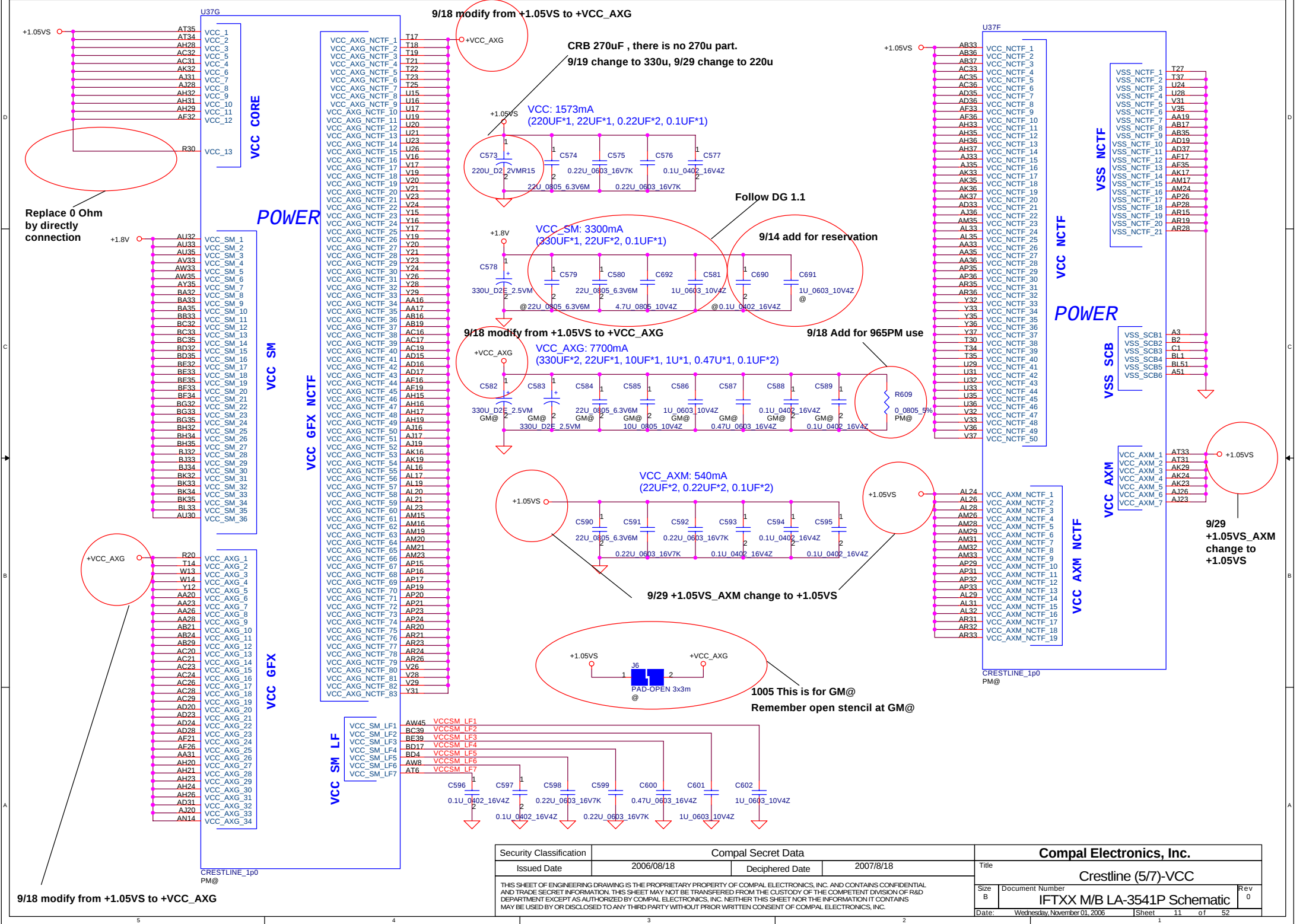
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DDRB_SDQ4 AN51 SB_DQ_4
DDRB_SDQ5 AN50 SB_DQ_5
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DDRB_SDQ18 BJ43 SB_DQ_18
DDRB_SDQ19 BK47 SB_DQ_19
DDRB_SDQ20 BK49 SB_DQ_20
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DDRB_SDQ23 BK42 SB_DQ_23
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DDRB_SDQ26 BJ37 SB_DQ_26
DDRB_SDQ27 BJ36 SB_DQ_27
DDRB_SDQ28 BK41 SB_DQ_28
DDRB_SDQ29 BJ40 SB_DQ_29
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DDRB_SDQ31 BK37 SB_DQ_31
DDRB_SDQ32 BK13 SB_DQ_32
DDRB_SDQ33 BE11 SB_DQ_33
DDRB_SDQ34 BK11 SB_DQ_34
DDRB_SDQ35 BC11 SB_DQ_35
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DDRB_SDQ38 BC12 SB_DQ_38
DDRB_SDQ39 BG12 SB_DQ_39
DDRB_SDQ40 BJ10 SB_DQ_40
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DDRB_SDQ42 BK5 SB_DQ_42
DDRB_SDQ43 BL5 SB_DQ_43
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DDRB_SDQ52 BK3 SB_DQ_52
DDRB_SDQ53 BE4 SB_DQ_53
DDRB_SDQ54 BD3 SB_DQ_54
DDRB_SDQ55 BJ2 SB_DQ_55
DDRB_SDQ56 BA3 SB_DQ_56
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DDRB_SDQ60 AY2 SB_DQ_60
DDRB_SDQ61 AY3 SB_DQ_61
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CRESTLINE_1p0
PM@

DDR SYSTEM MEMORY B

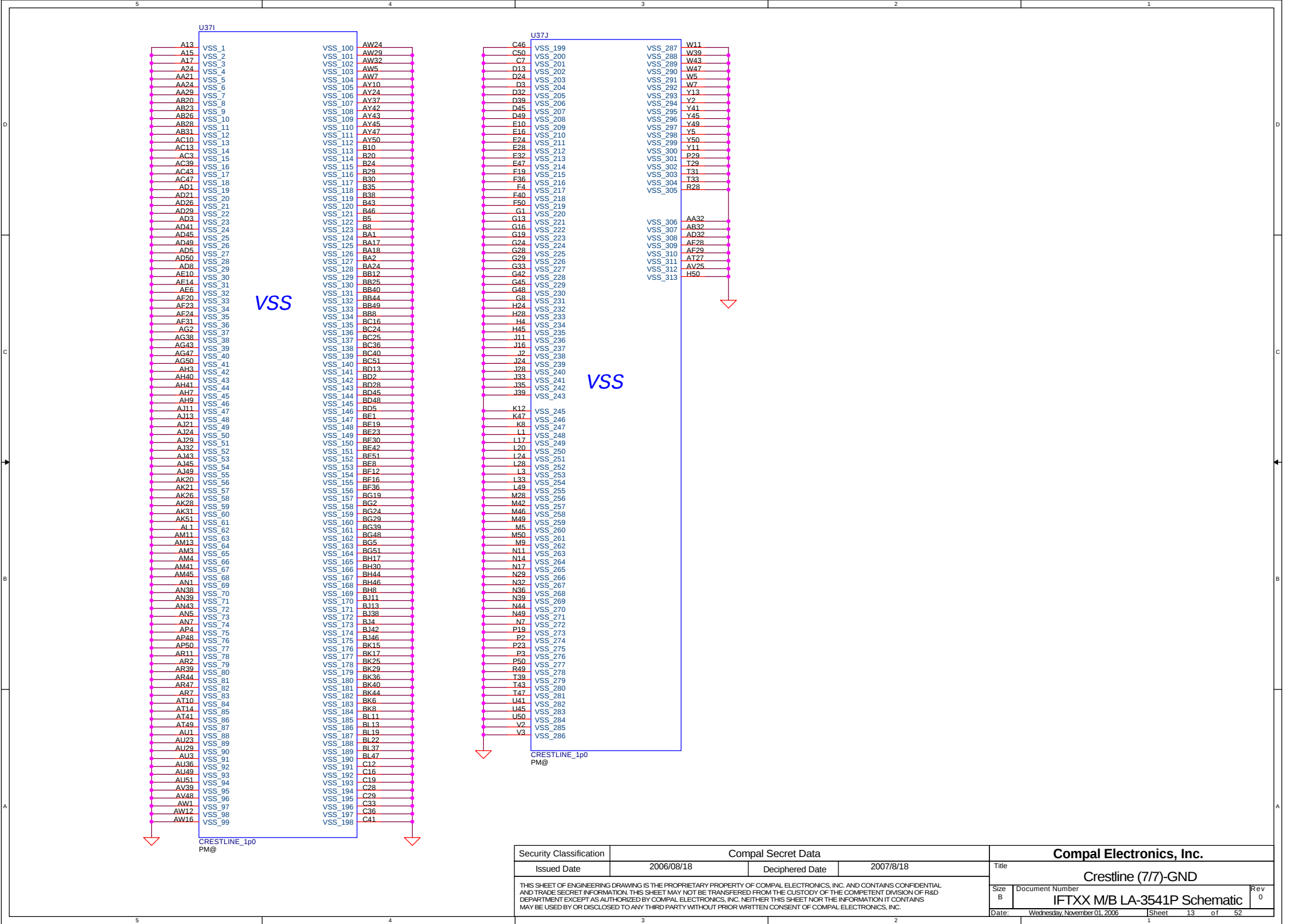
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SB_MA_12 BA39 DDRB_SMA12 <15>
SB_MA_13 BG13 DDRB_SMA13 <15>
SB_RAS# AV16 DDRB_SRAS# <15>
SB_RCVEN# AY18 DDRB_SRCVEN# <15>
SB_WE# BC17 DDRB_SWE# <15>

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Crestline (3/7)-DDR II		
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				Size B Document Number		
				IFTXX M/B LA-3541P Schematic		
				Rev 0		
Date: Wednesday, November 01, 2006				Sheet	9 of 52	



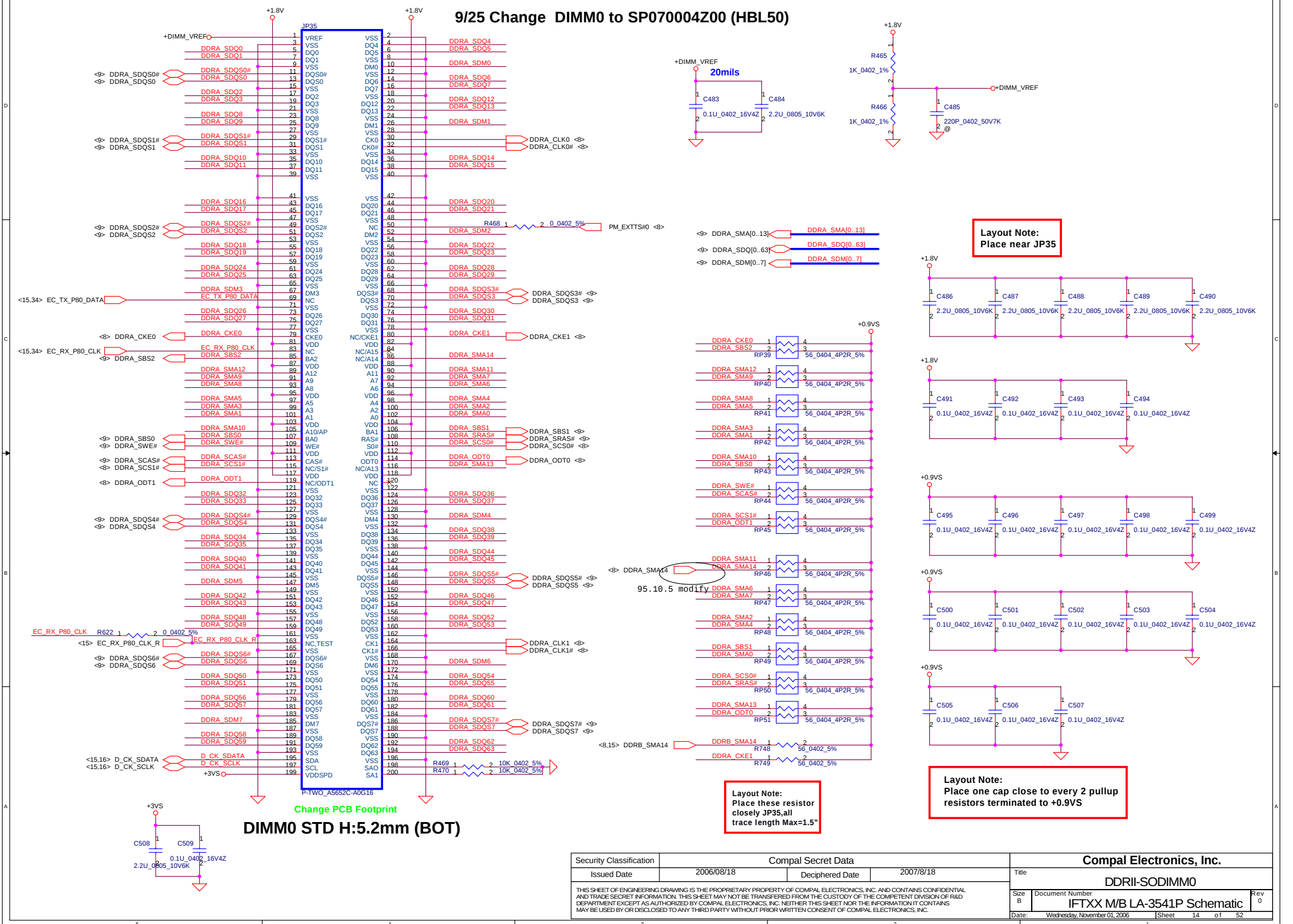
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	IFTXX M/B LA-3541P Schematic			Rev
B					0
Date:	Wednesday, November 01, 2006	Sheet	11	of	52



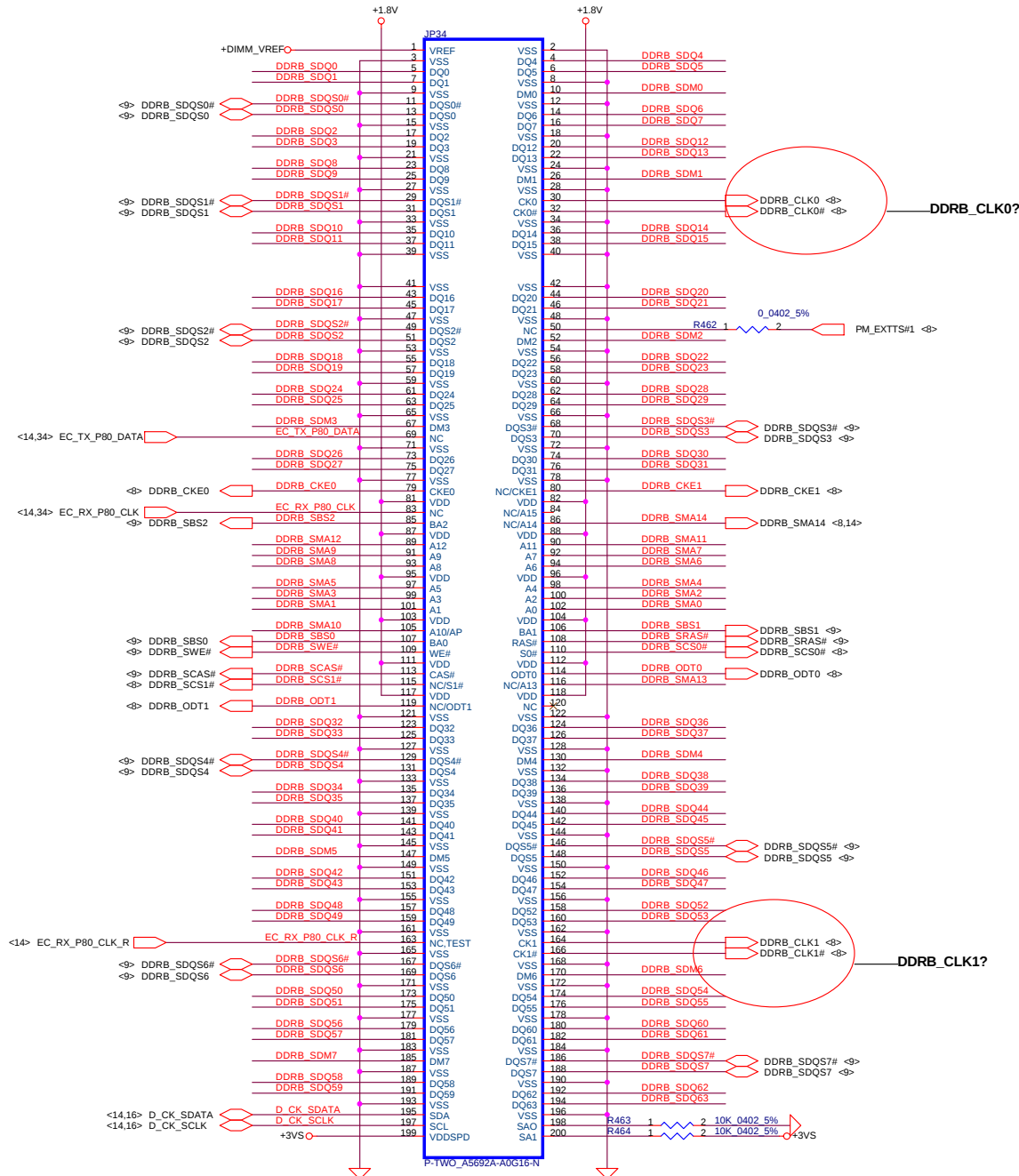


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						Crestline (7/7)-GND		
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Date:		Wednesday, November 01, 2006		Sheet		13 of 52		

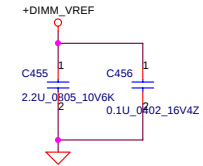
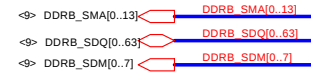
9/25 Change DIMM0 to SP070004Z00 (HBL50)



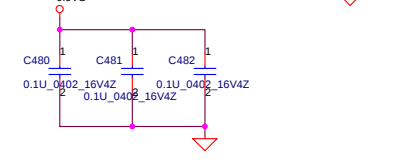
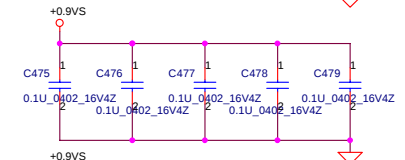
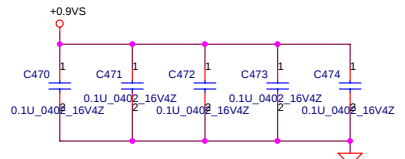
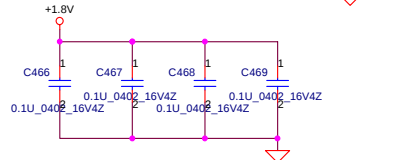
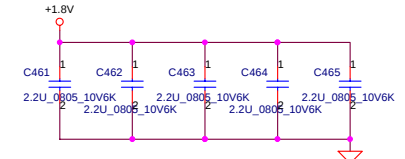
9/25 Change DIMM1 to SP070006F00



DIMM1 STD H:9.2mm (BOT)



Layout Note:
Place near JP34



Layout Note:
Place these resistor closely JP35, all trace length Max=1.5"

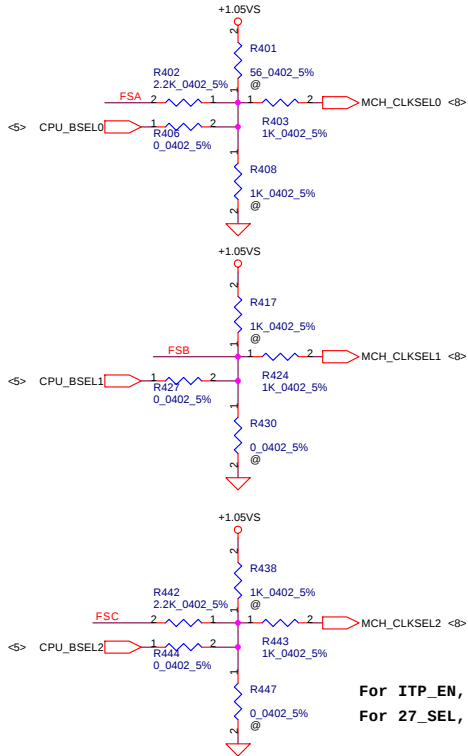
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

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					Size B	Document Number	Rev 0
					IFTXX M/B LA-3541P Schematic		
					Date:	Wednesday, November 01, 2006	Sheet 15 of 52

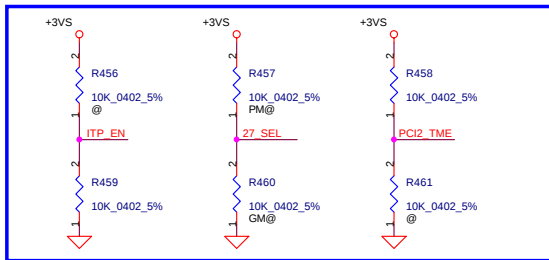
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

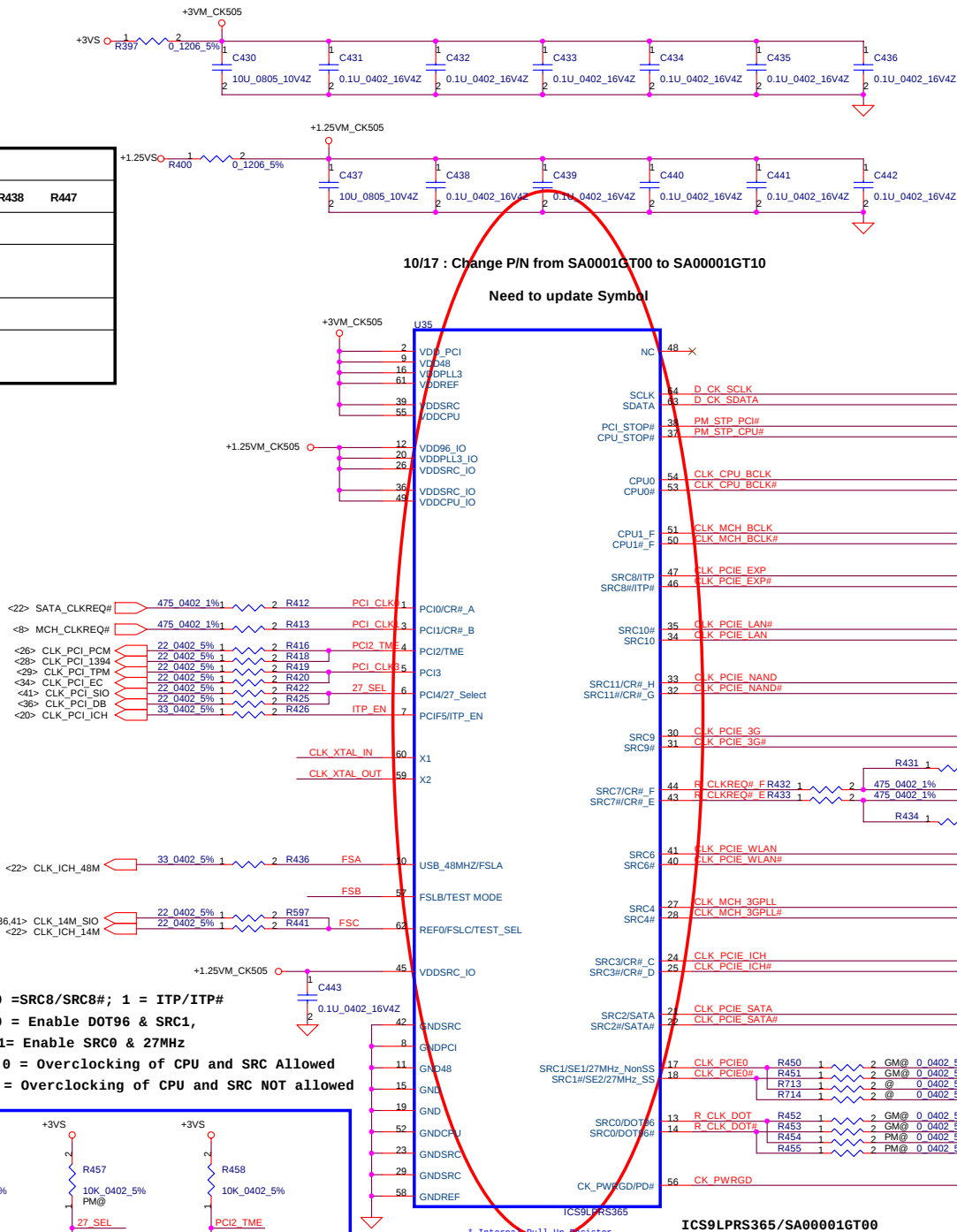
CPU Driven	Stuff	R401	R408	R417	R430	R438	R447
* (Default)	No Stuff	R401	R417	R447			
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed



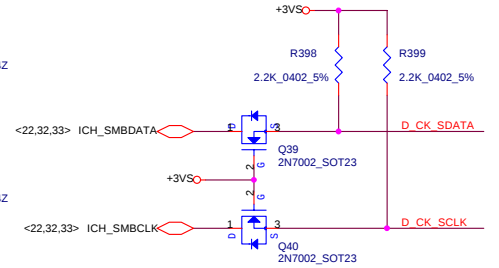
Routing the trace at least 10mil



10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol

ICS9LPRS365/SA00001GT00



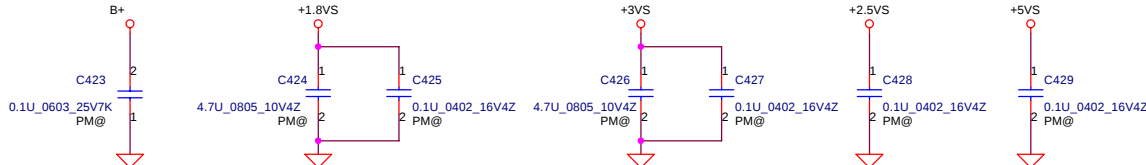
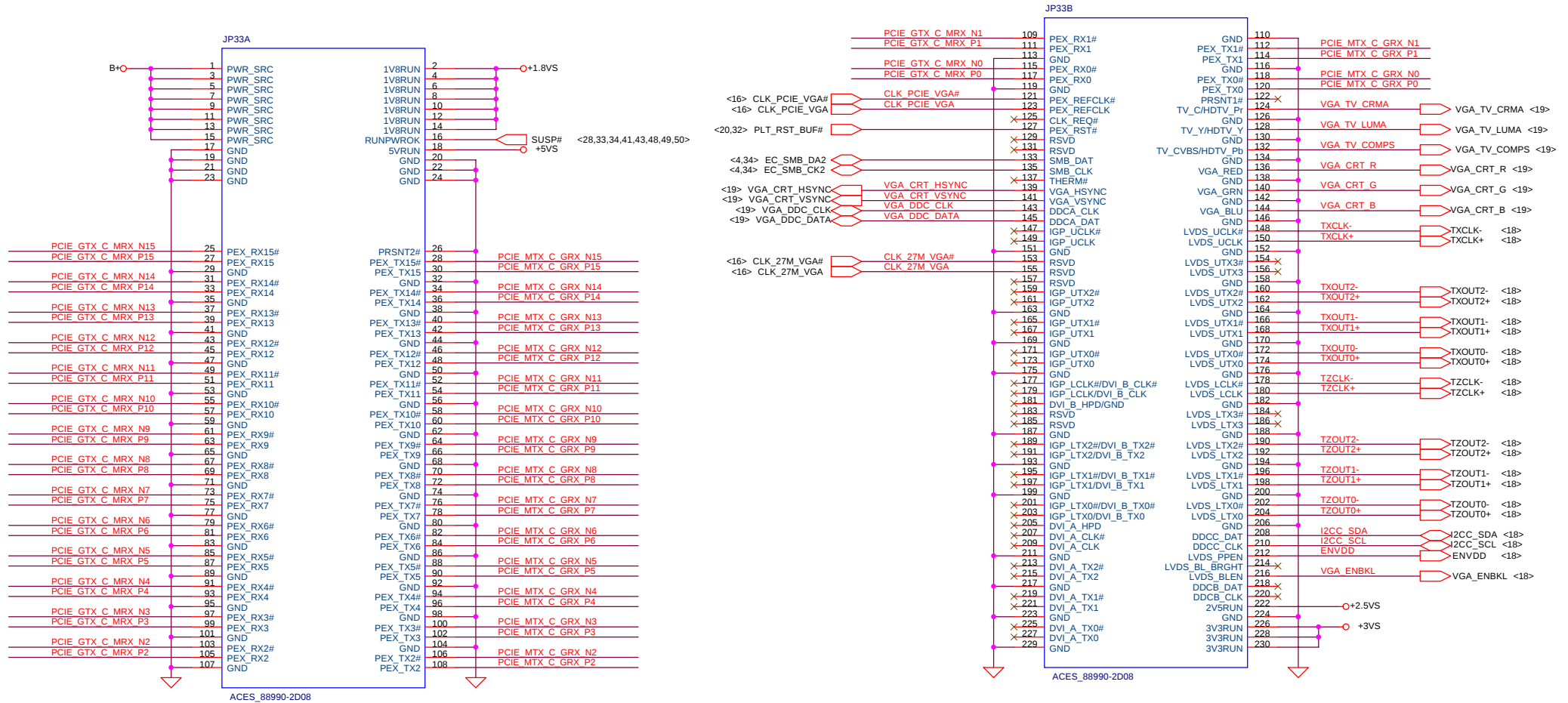
C444	2	1	CLK_ICH_48M
C445	2	1	CLK_ICH_14M
C446	2	1	CLK_PCI_ICH
C447	2	1	CLK_14M_SIO
C448	2	1	CLK_PCI_PCM
C449	2	1	CLK_PCI_EC
C450	2	1	CLK_PCI_SIO

Place close to U35

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/04				Clock generator			
Deciphered Date				2006/10/06				XXXX LA-3XXX			
Title				Size				Rev			
Document Number				Date				Wednesday, November 01, 2006			
Sheet				16				of			
1				0.1							

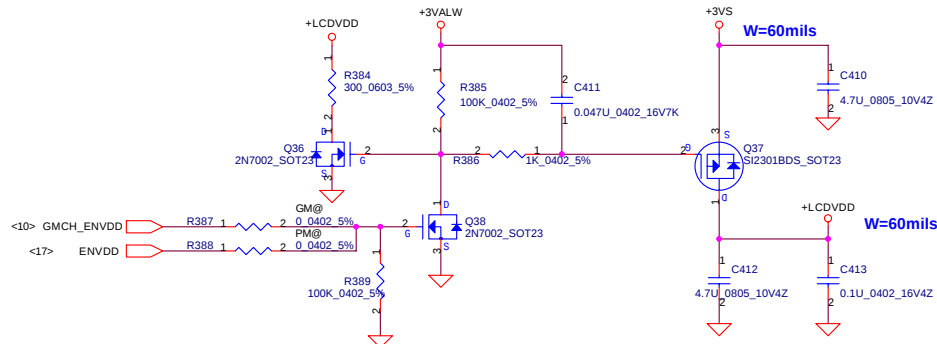
<10> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
<10> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
<10> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
<10> PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

9/13 modify this footprint from ACES_88990-2D08_230P to ACES_88990-2D28_230P

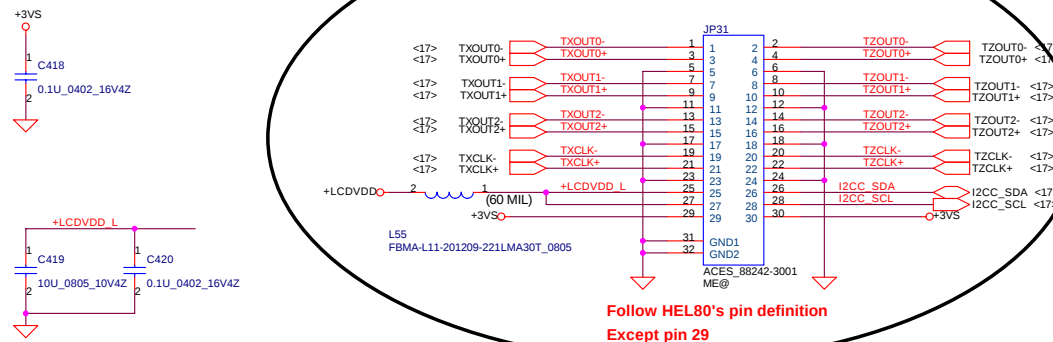


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Size	Document Number	Rev		Date	
Custpm	IFTXX M/B LA-3541P Schematic	0		Wednesday, November 01, 2006	
Sheet		17		of 52	

LCD POWER CIRCUIT

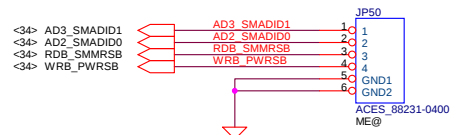


LCD/PANEL BD. Conn.

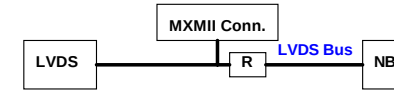


Follow HEL80's pin definition
Except pin 29

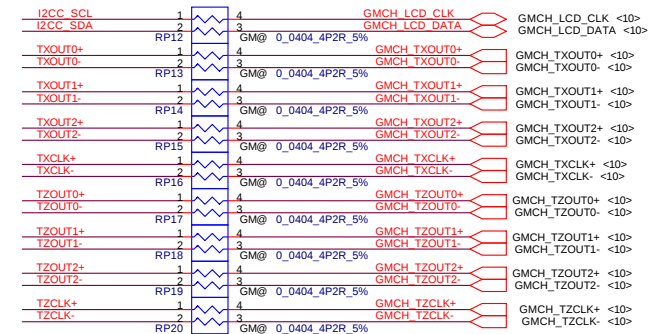
JEPICO Conn.



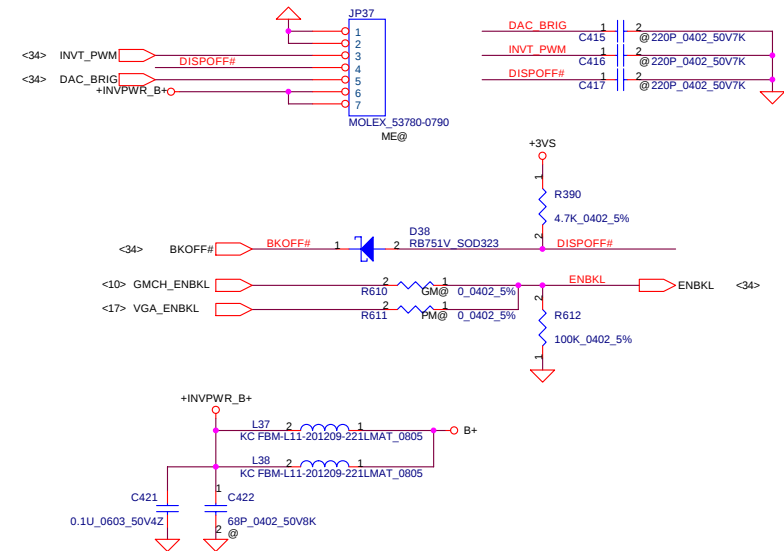
Routing Diagram



Use Daisy chain to route

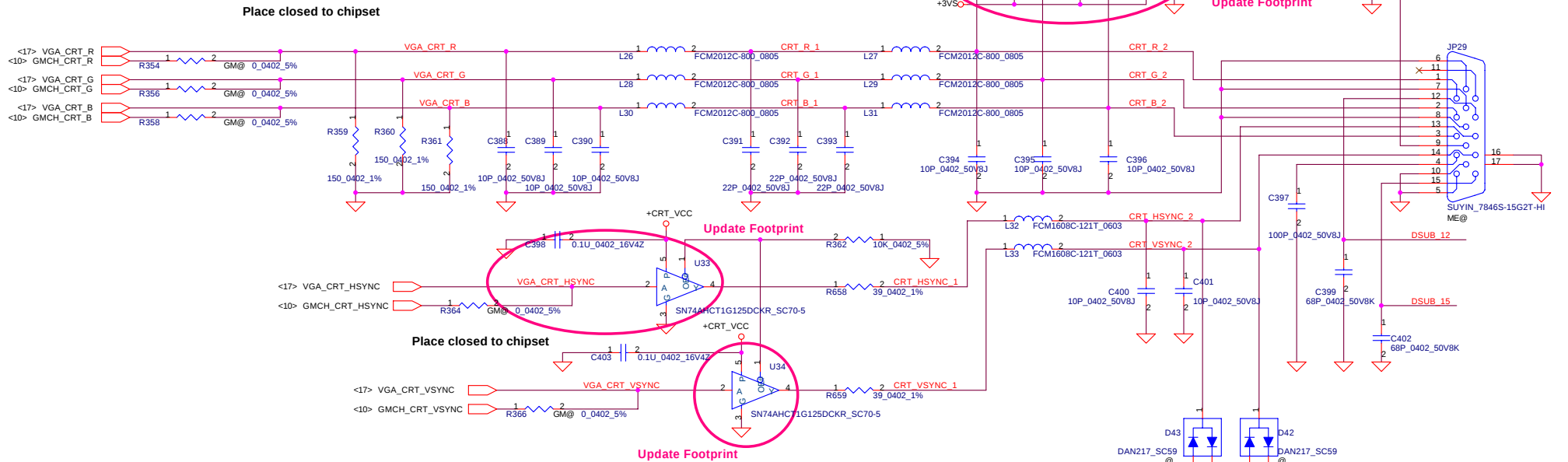


INVERTER Conn.

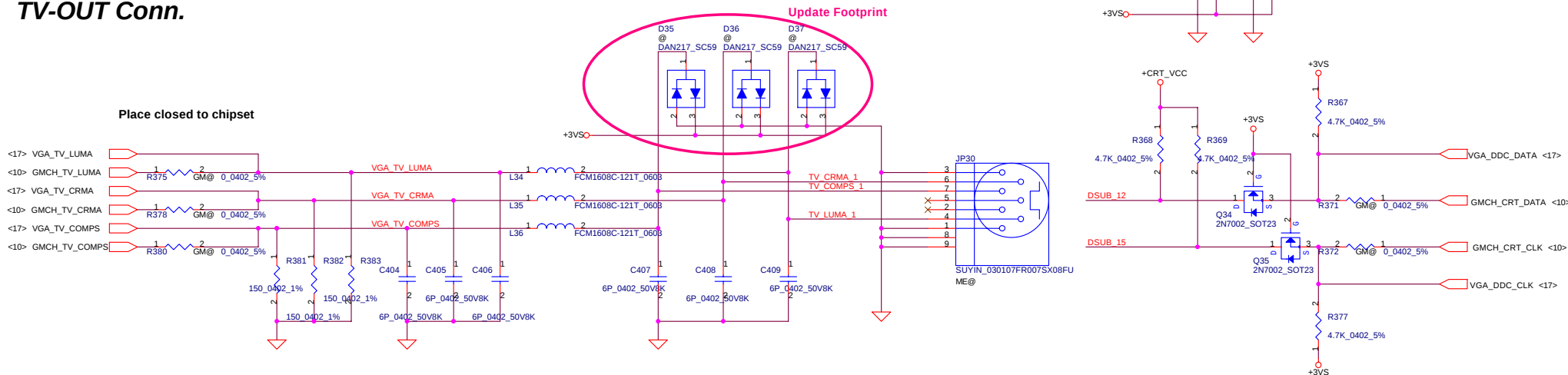


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Issued Date		2006/08/18		Deciphered Date		2007/8/18			
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				LVDS & DVI Connector					
				Size	Document Number			Rev 0	
				IFTXX M/B LA-3541P Schematic					
				Date: Wednesday, November 01, 2006					
				Sheet 18 of 52					

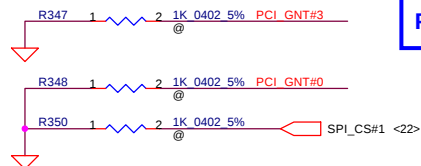
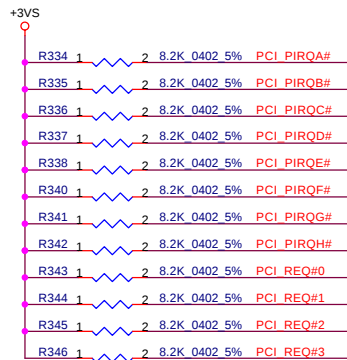
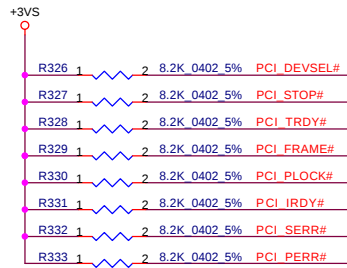
CRT Connector



TV-OUT Conn.



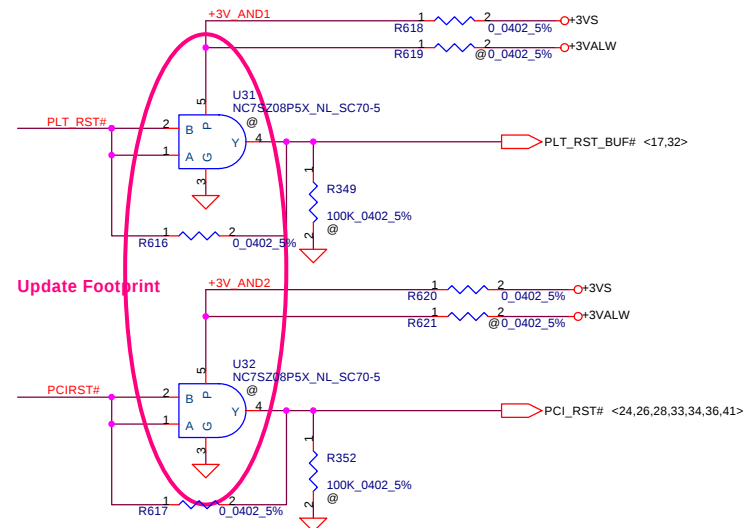
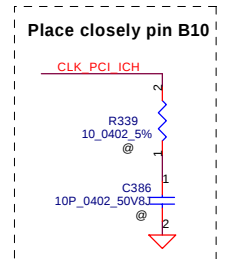
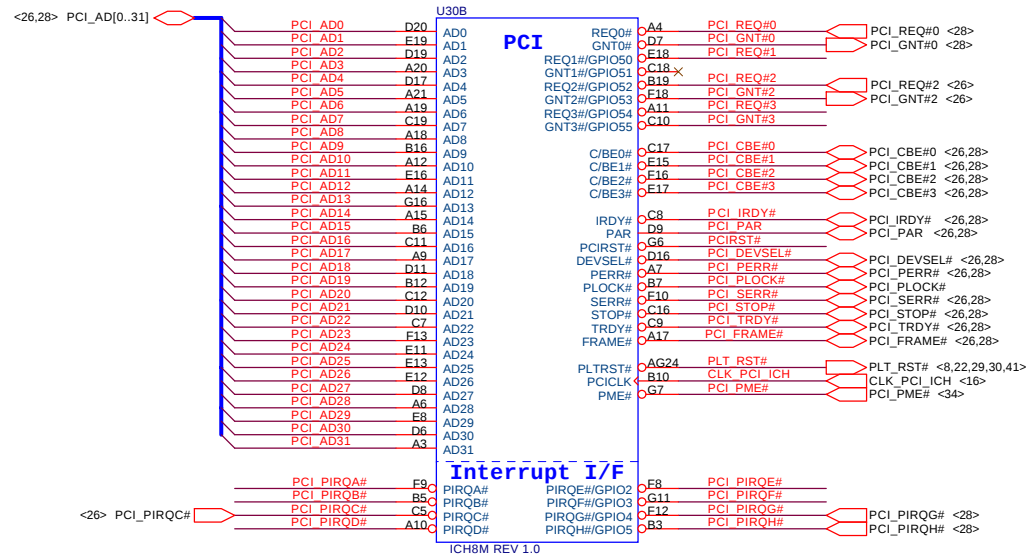
Security Classification	Compal Secret Data			Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	CRT & TV-OUT Connector	
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				IFTXX M/B LA-3541P Schematic	
				Date:	Wednesday, November 01, 2006
				Sheet	19 of 52

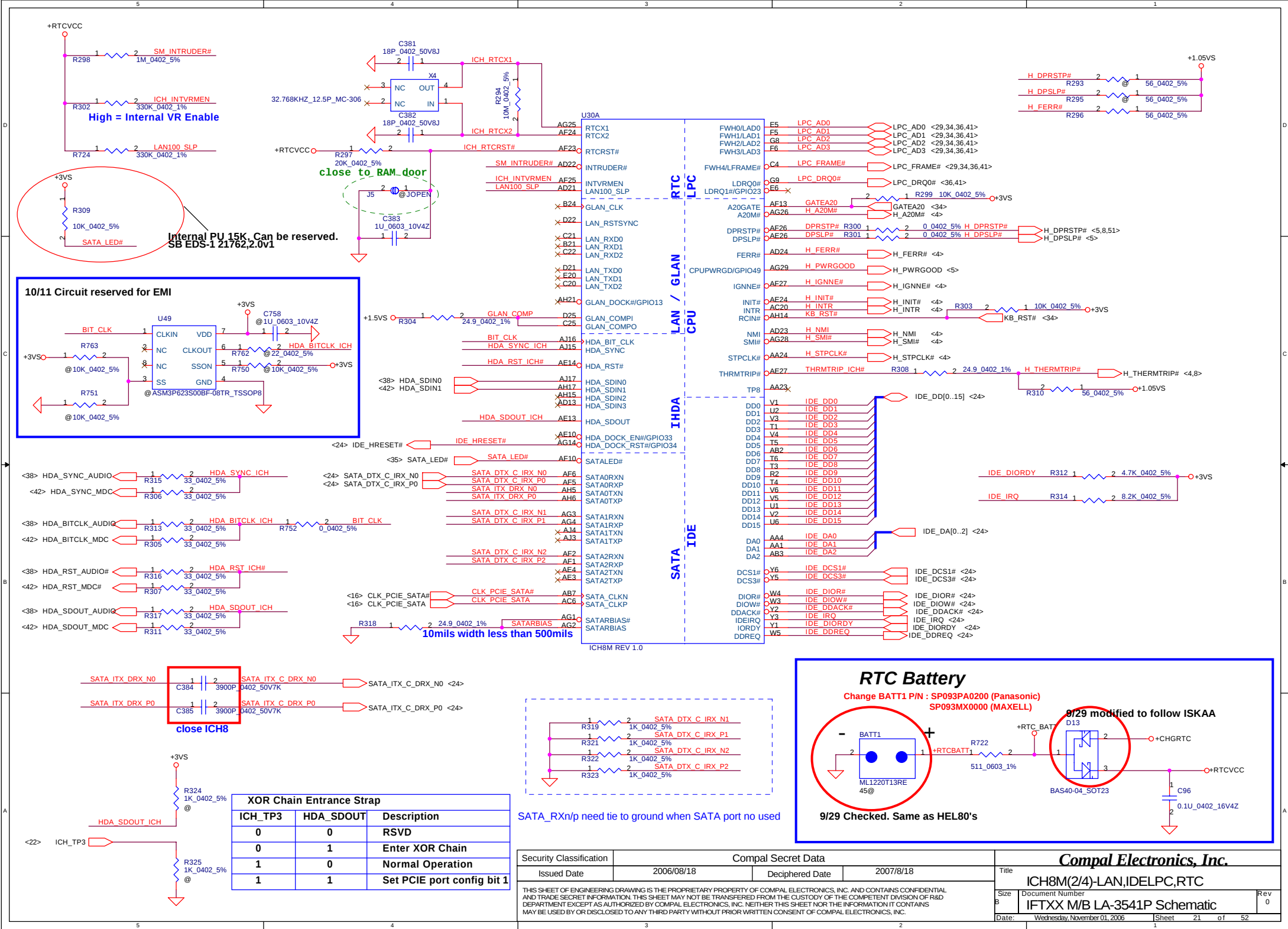


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

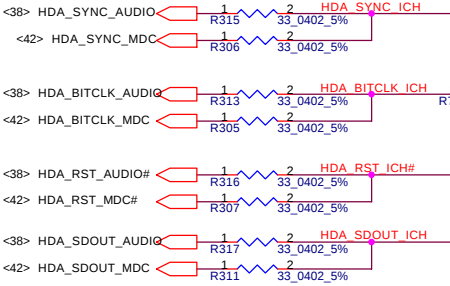
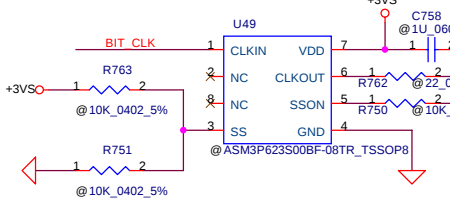
10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10





Internal PU 15K. Can be reserved.
SB EDS-1 21762,2.0v1

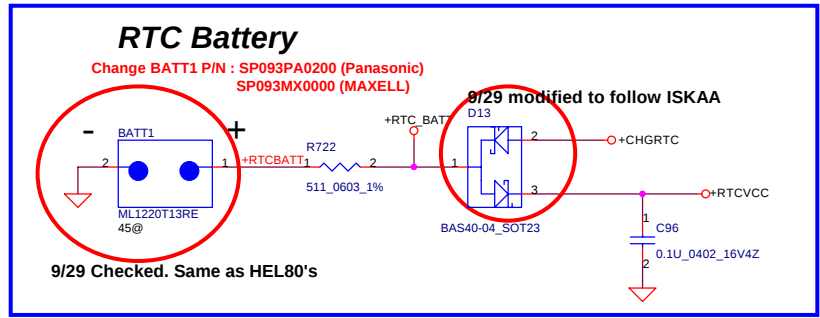
10/11 Circuit reserved for EMI

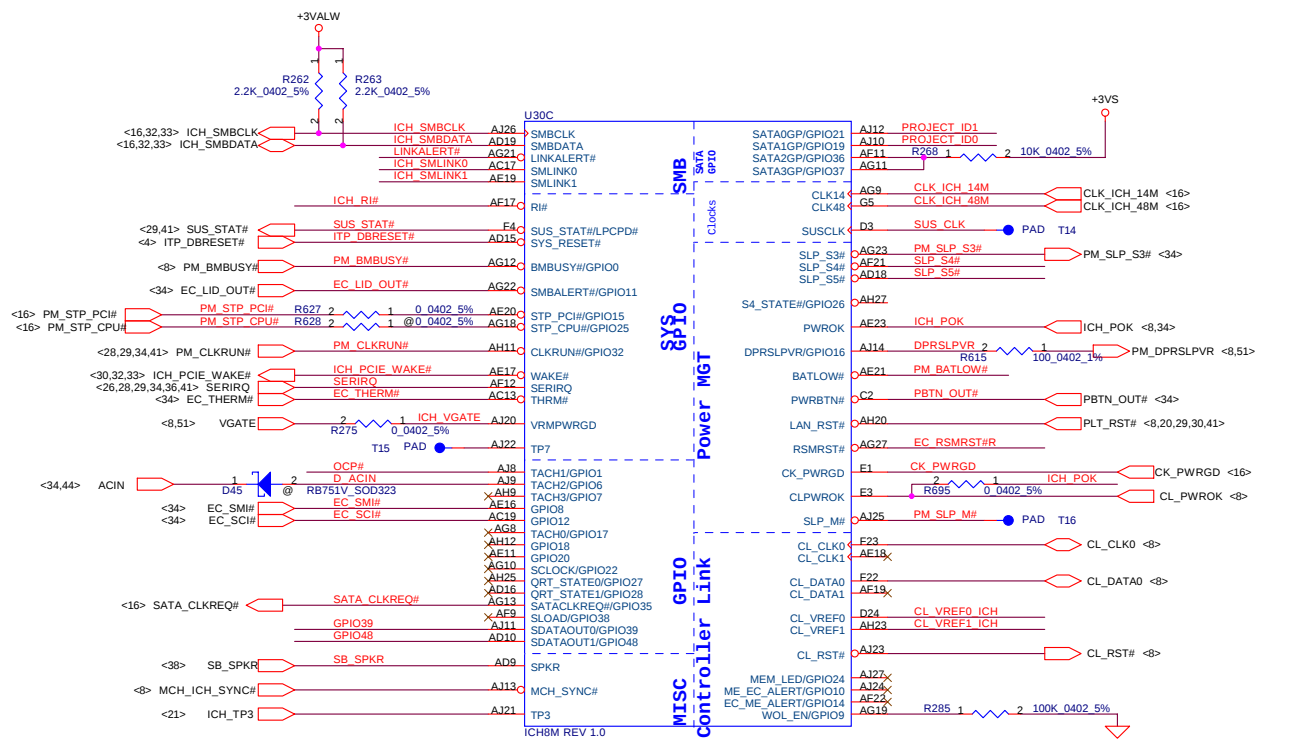
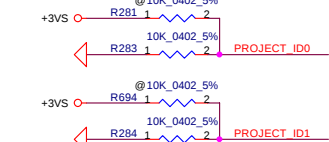


close ICH8

XOR Chain Entrance Strap			
ICH_TP3	HDA_SDOUT	Description	
0	0	RSVD	
0	1	Enter XOR Chain	
1	0	Normal Operation	
1	1	Set PCIE port config bit 1	

SATA_RXn/p need tie to ground when SATA port not used





LAN

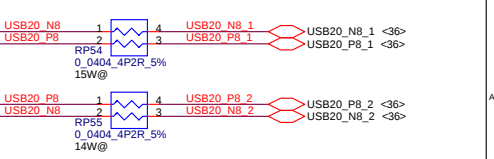
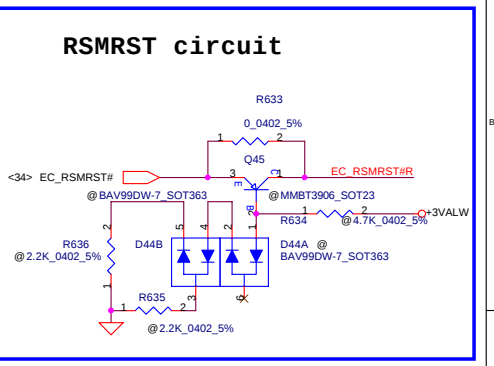
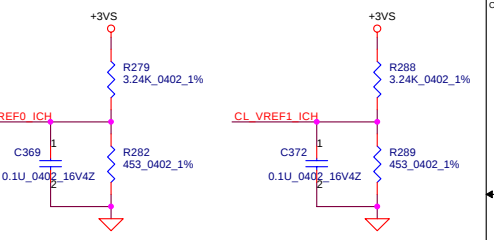
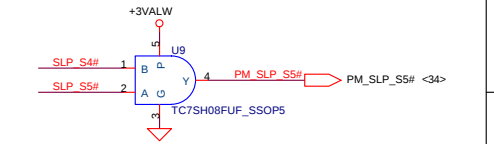
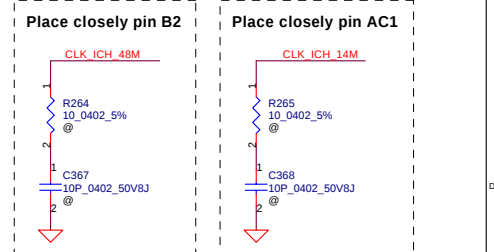
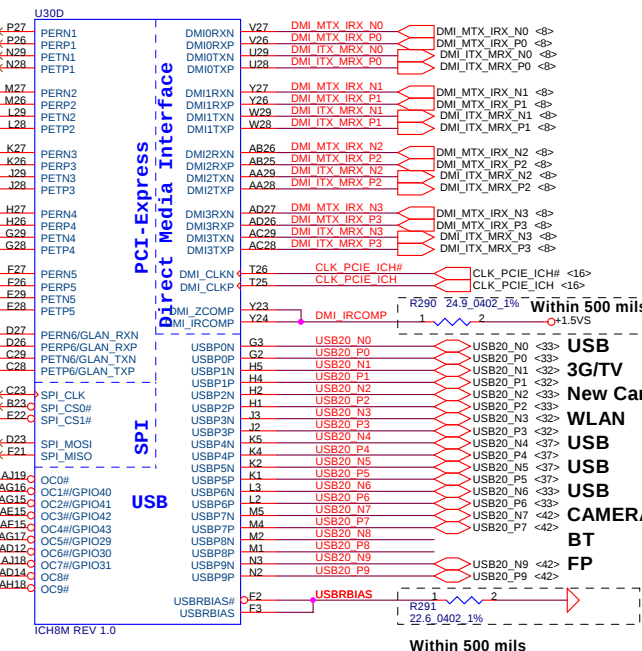
NEW Card

Robson

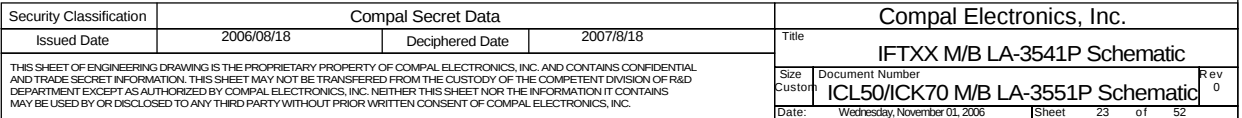
3G

WLAN

Need to define PROJECT ID



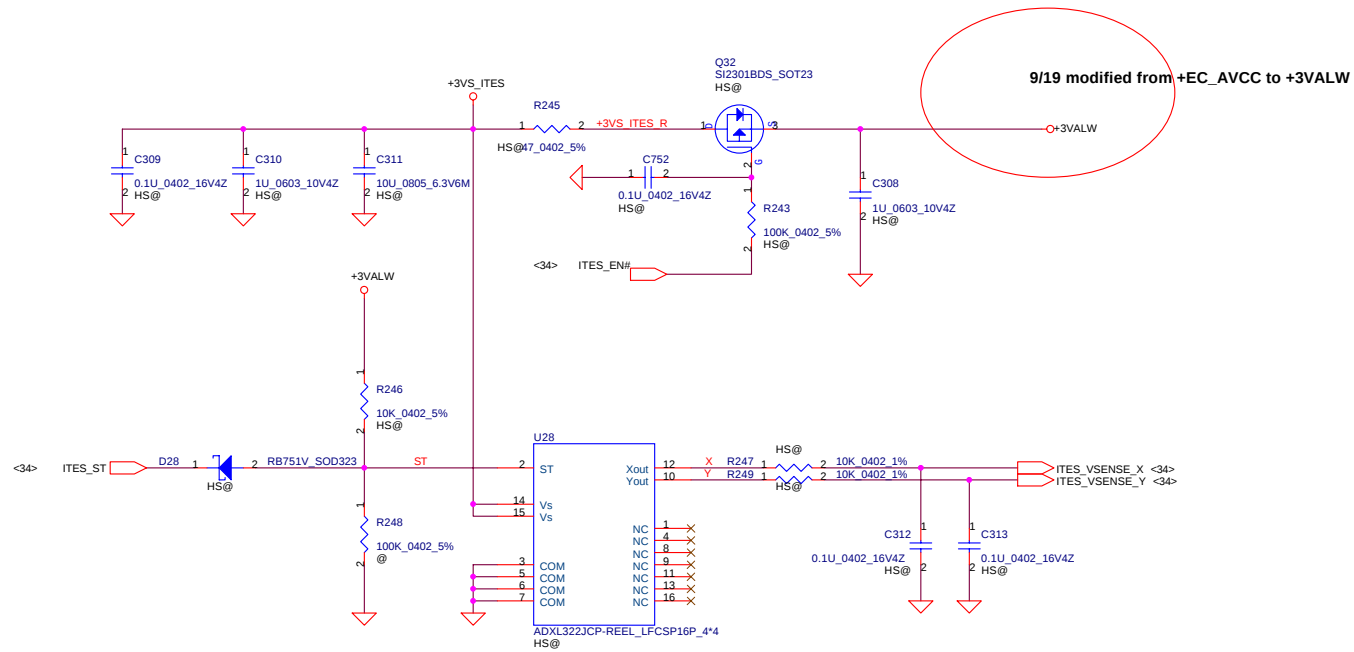
Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	ICH8M(34)-USB,GPIO,PCIE		
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				Customer	IFTXX M/B LA-3541P Schematic		0
				Date:	Wednesday, November 01, 2006	Sheet	22 of 52



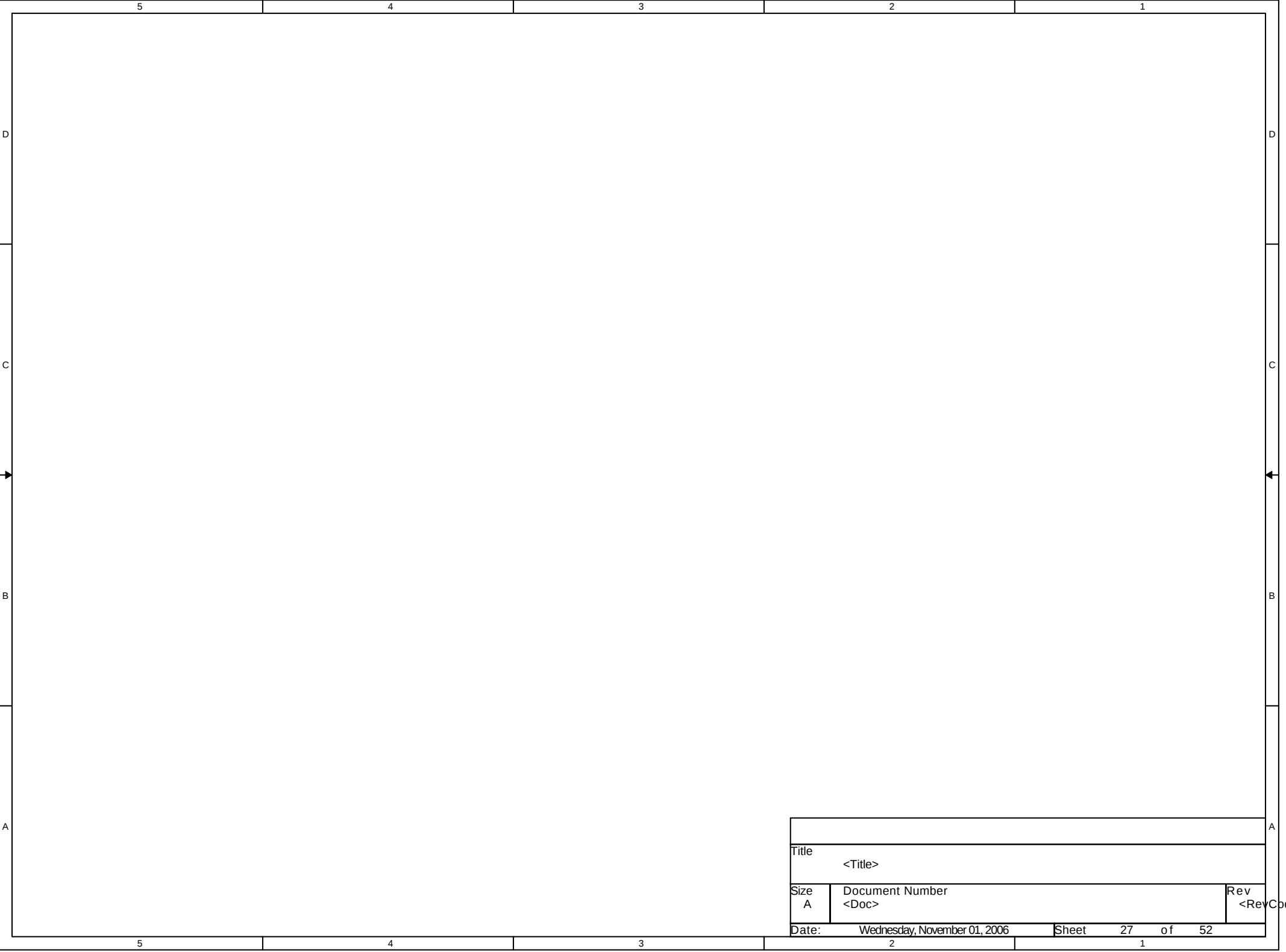
15W ODD Conn.

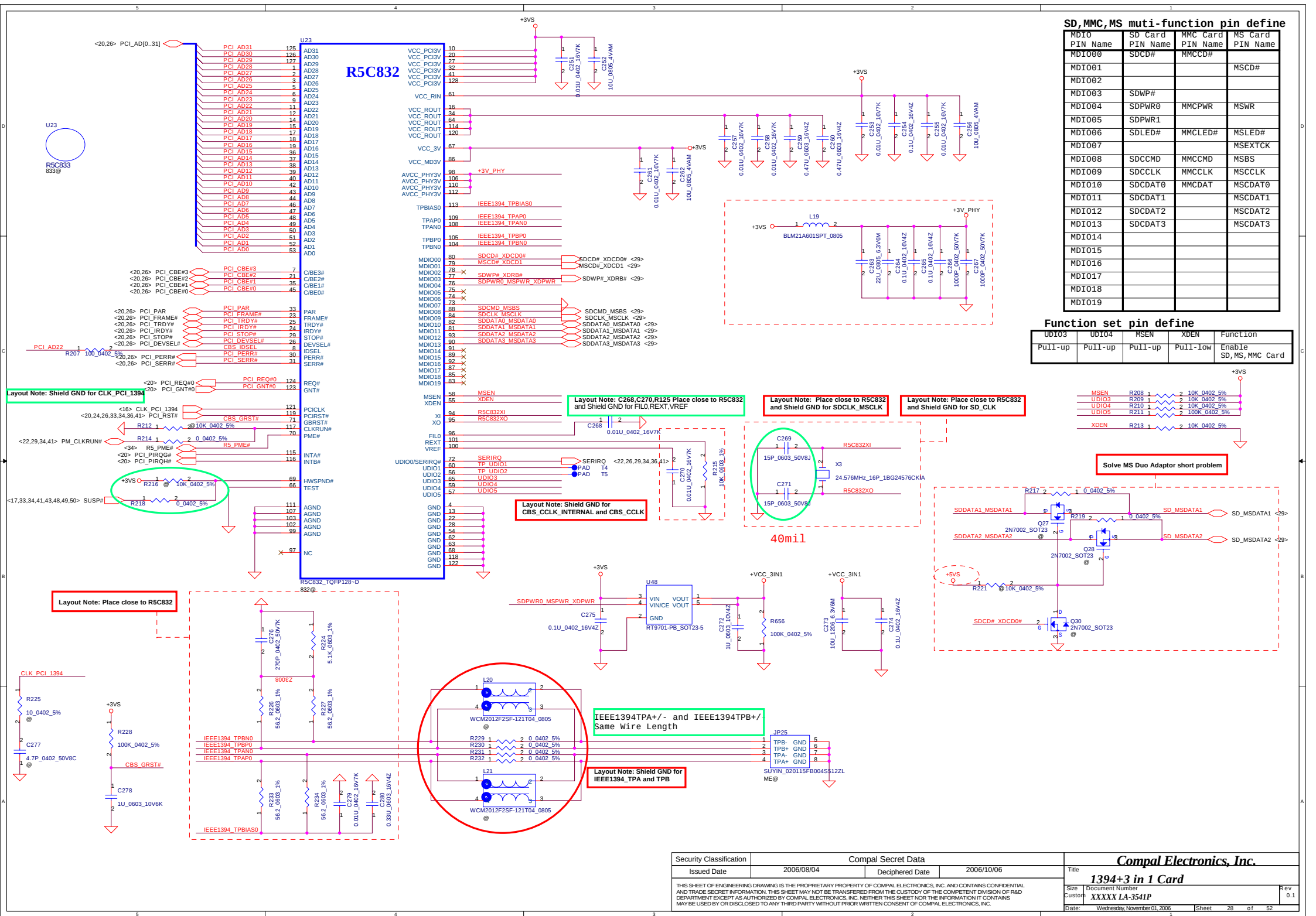
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	HDD & ODD Connector				
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				B			0		
				IFTXX M/B LA-3541P Schematic					
Date:				Wednesday, November 01, 2006	Sheet	24	of 52		

Note : BOM structure HS@ is for Heng shan IFT10/11 this model

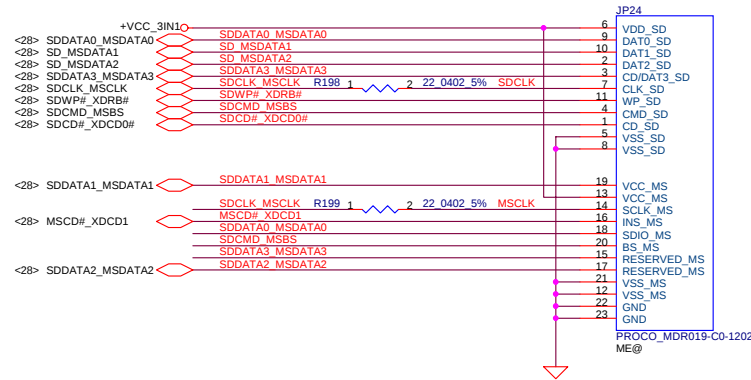


Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	CH7315A&HDMI Connector		
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				B	LA-3541P	0.1	
Date:				Wednesday, November 01, 2006	Sheet	25	of 52

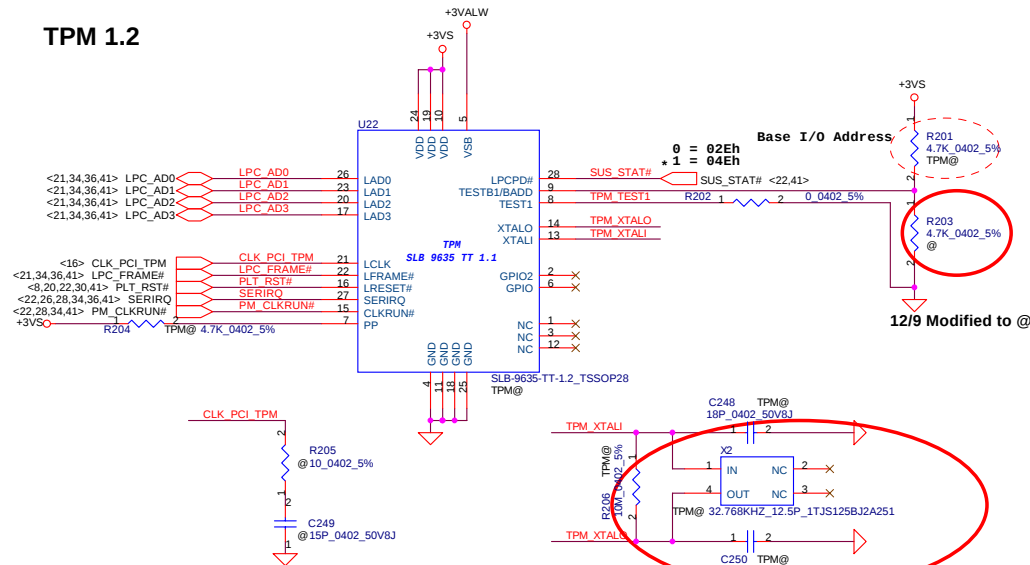




3 in 1 Card Reader

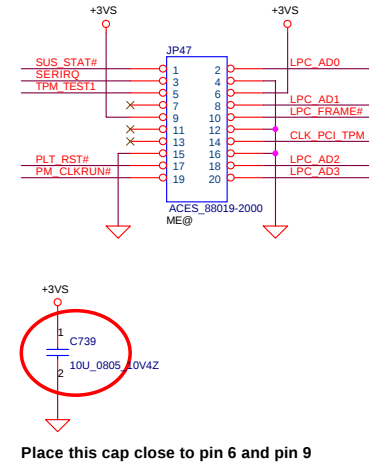


TPM 1.2

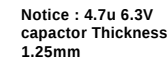
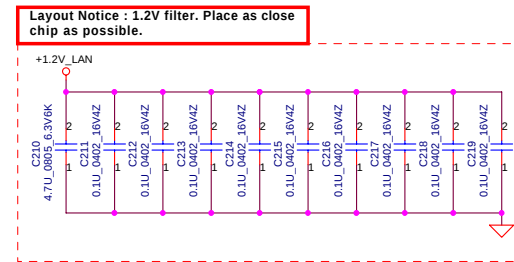
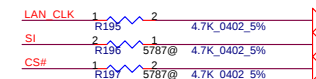
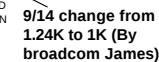
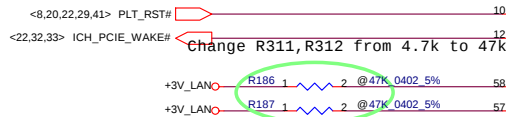
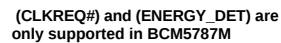
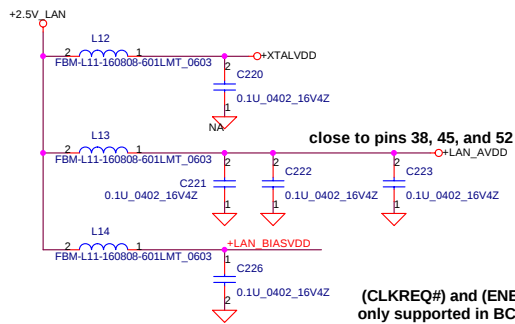


For A30

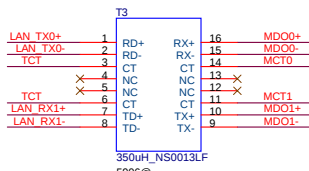
TPM Conn. For C38



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title
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Date: Wednesday, November 01, 2006				Size Custom XXXXX LA-3541P
Sheet 29 of 52				Rev 0.1



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	BCM5787MKML
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				Custom	XXXXX LA-3541P
				Date:	Wednesday, November 01, 2006
				Sheet	30 of 52

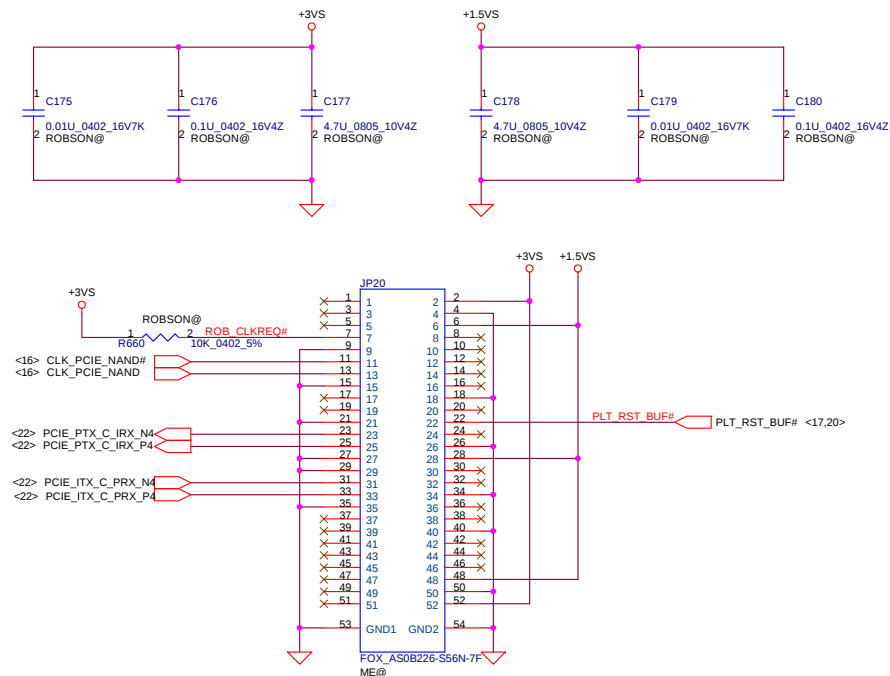


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

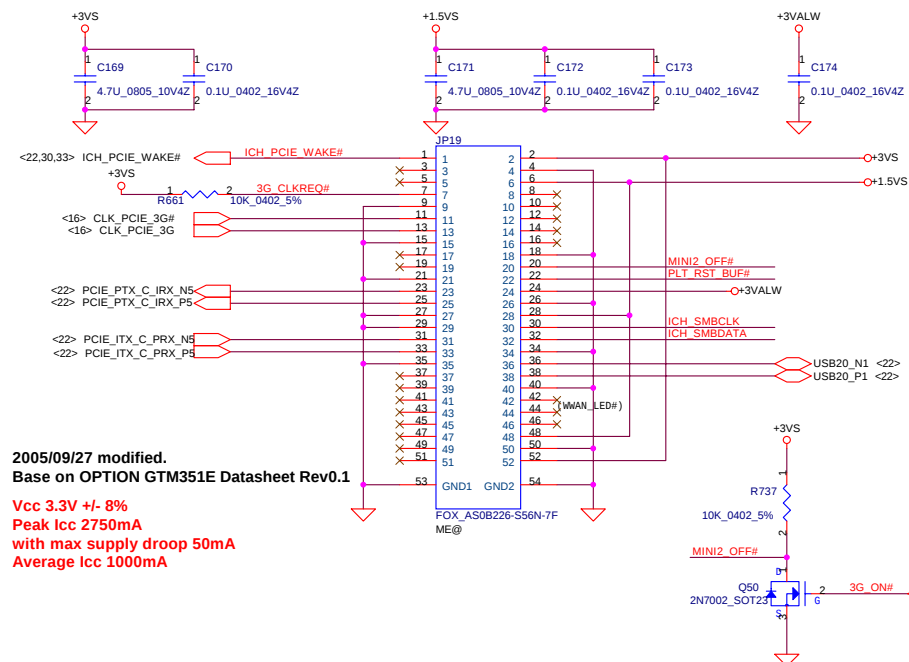
[illegible]

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				LAN CONTROLLER					
				Size		Document Number		Rev	
				Cust		XXXXX LA-3541P		0.1	
				Date:		Wednesday, November 01, 2006		Sheet 31 of 52	

NAND mini Card(Robson support)



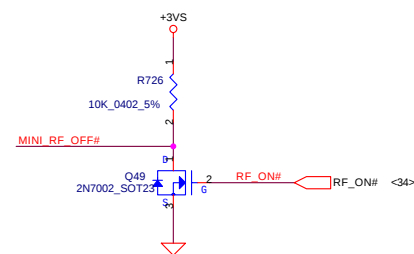
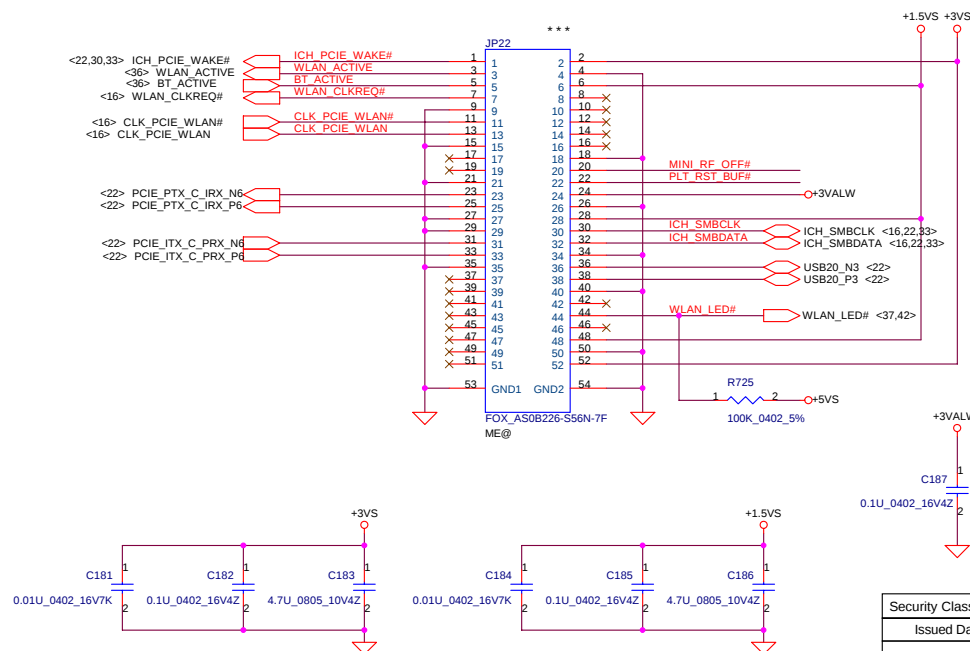
Mini-Express Card for 3G Or TV Tuner



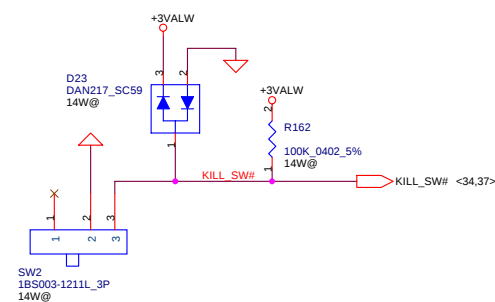
2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Mini-Express Card for WLAN

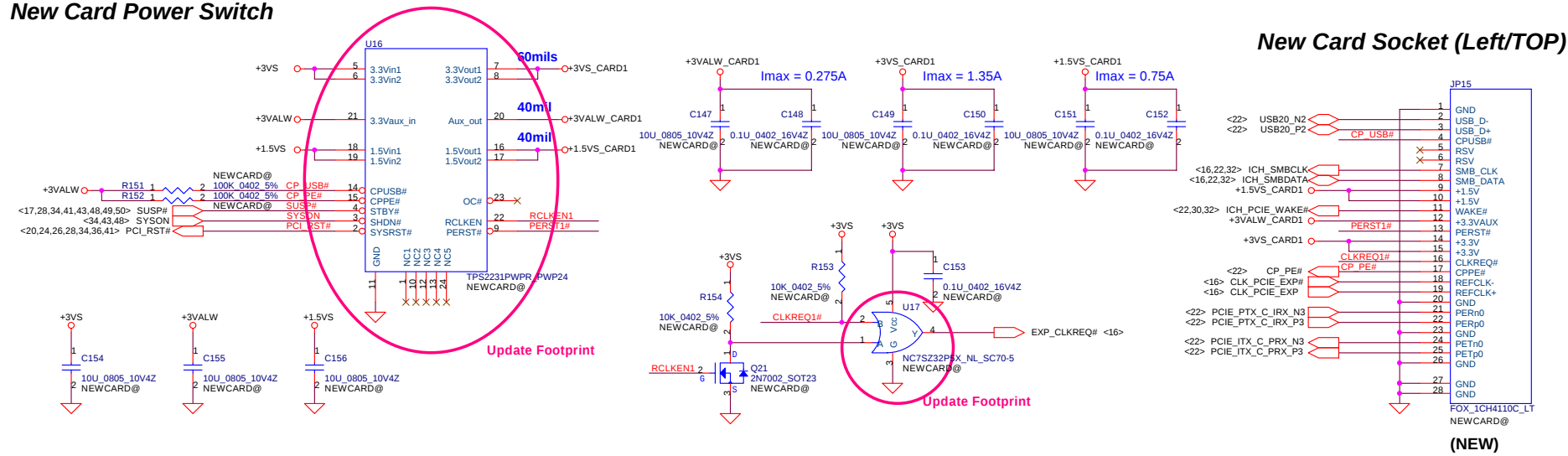


Kill SWITCH

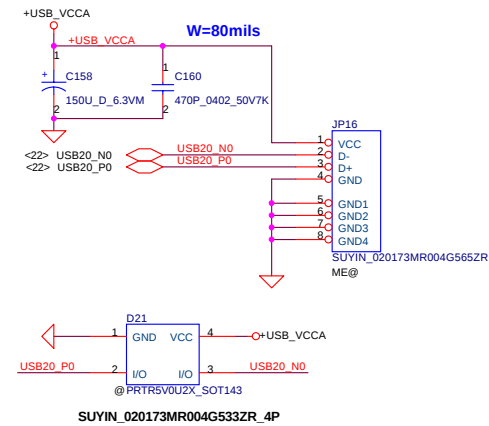


Security Classification		Compal Secret Data		Compal Electronics, Inc. Mini-Card/3G/FeliCa/FP		
Issued Date	2006/08/05	Deciphered Date	2007/08/05			
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				Size		
				Date: Wednesday, November 01, 2006	Sheet 32 of 52	

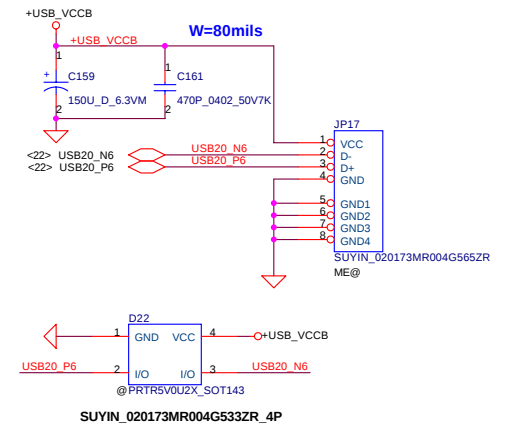
New Card Power Switch



USB CONN. 1



USB CONN. 2

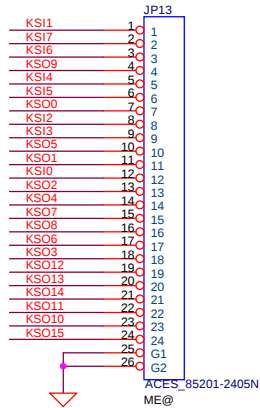


9/17 modified this block

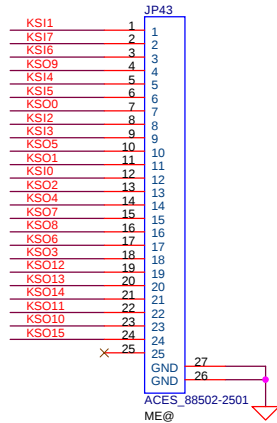
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/08/18	Deciphered Date	2007/08/18	Title	NEW CARD & USB Connector		
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				B	ITFTX M/B LA-3541P Schematic		0
				Date:	Wednesday, November 01, 2006		Sheet 33 of 52

INT_KBD Conn.

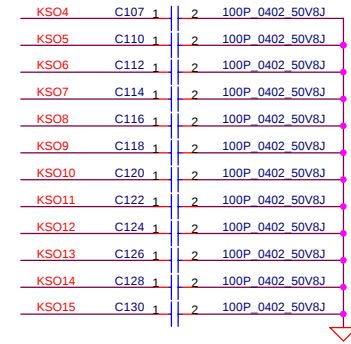
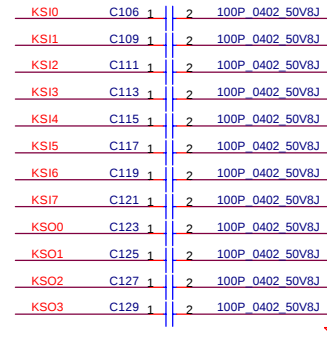
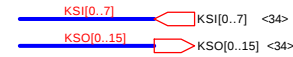
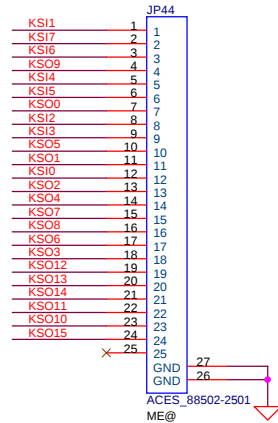
For IFT10



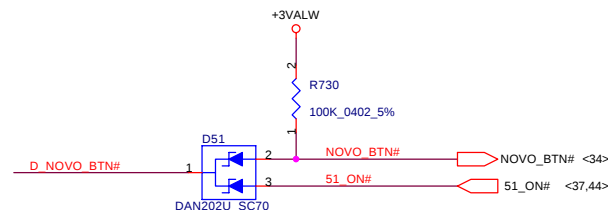
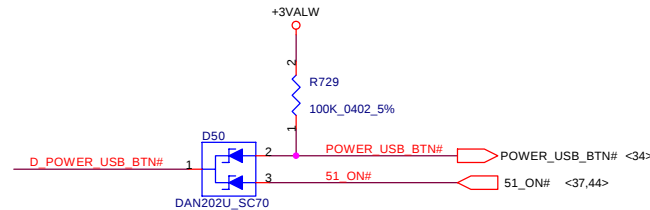
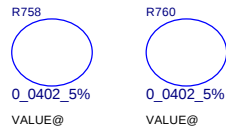
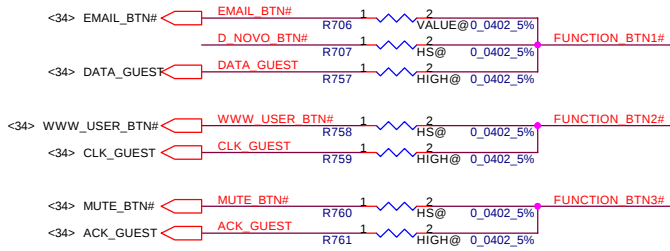
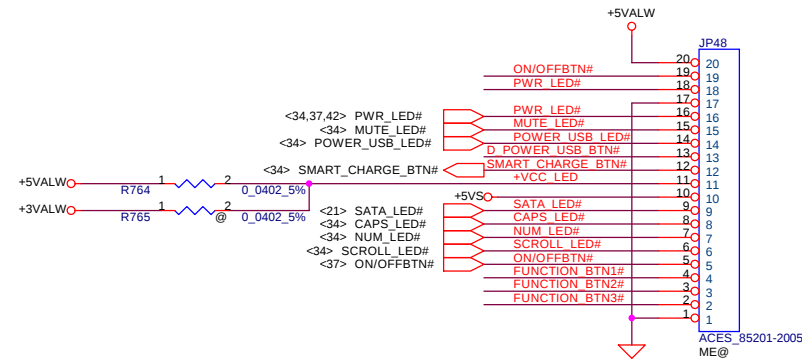
For IFL90



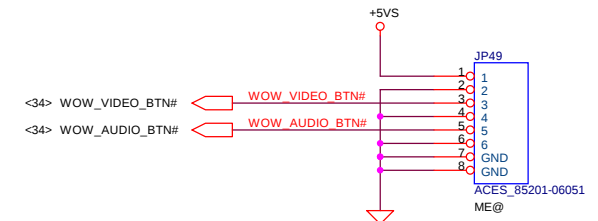
For IFT00



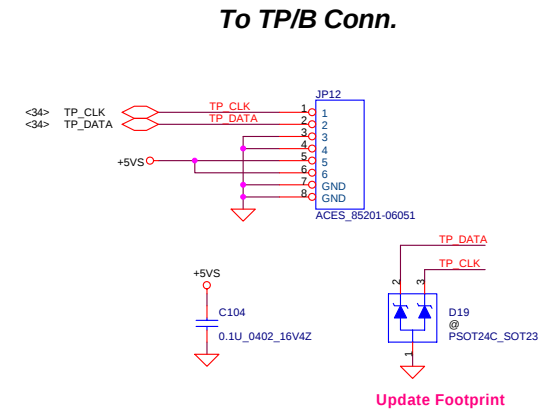
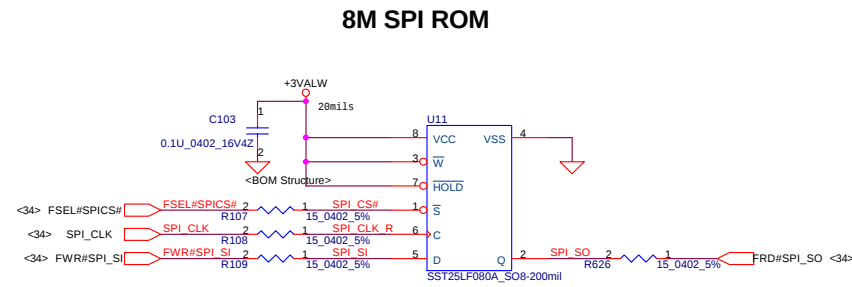
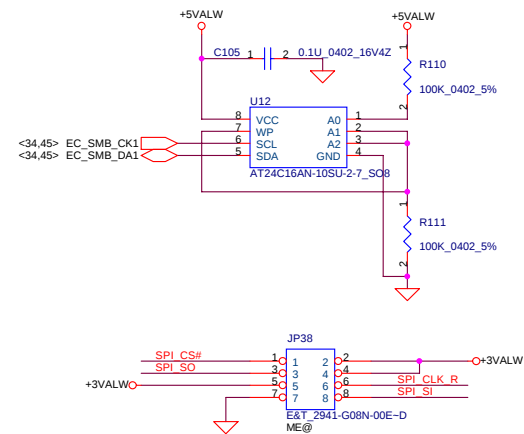
Switch Board Conn.



Video Switch Board Conn.

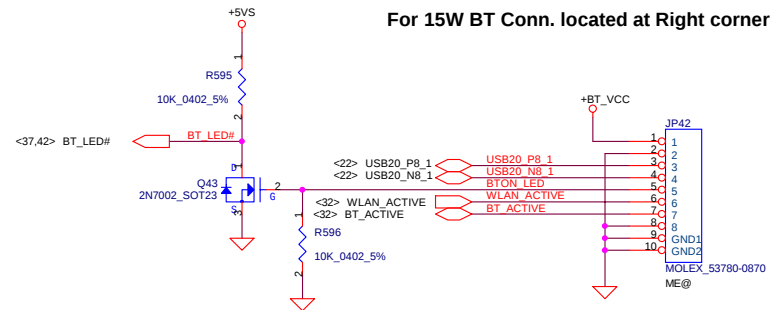


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Size	Document Number	Sheet		Rev	
B	IFTXX M/B LA-3541P Schematic	0		Date: Wednesday, November 01, 2006	
1		35		of 52	

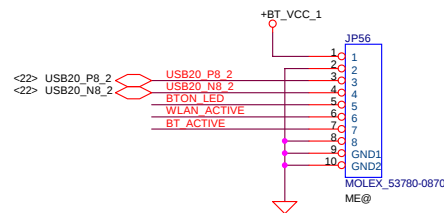


Bluetooth Conn.

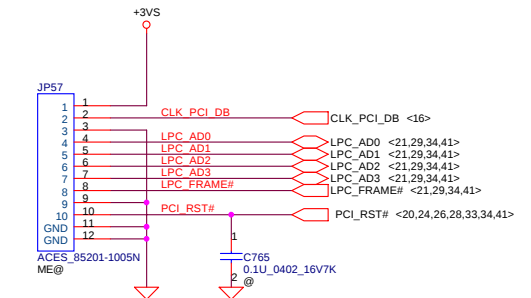
Need to check BT pin definition again!
9/20 modified this block



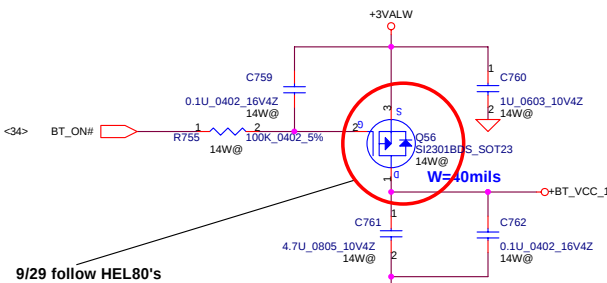
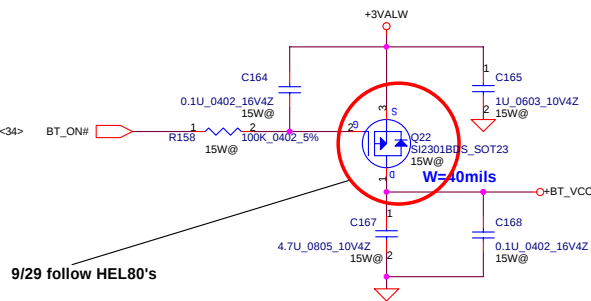
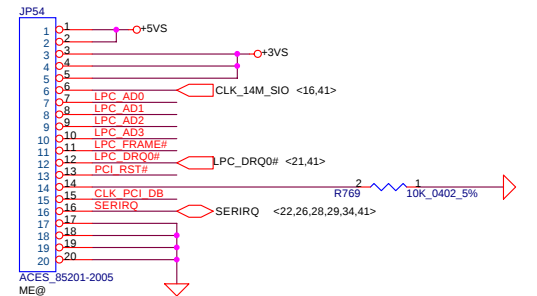
For 14W BT Conn. located at Left corner



FOR LPC DEBUG PORT

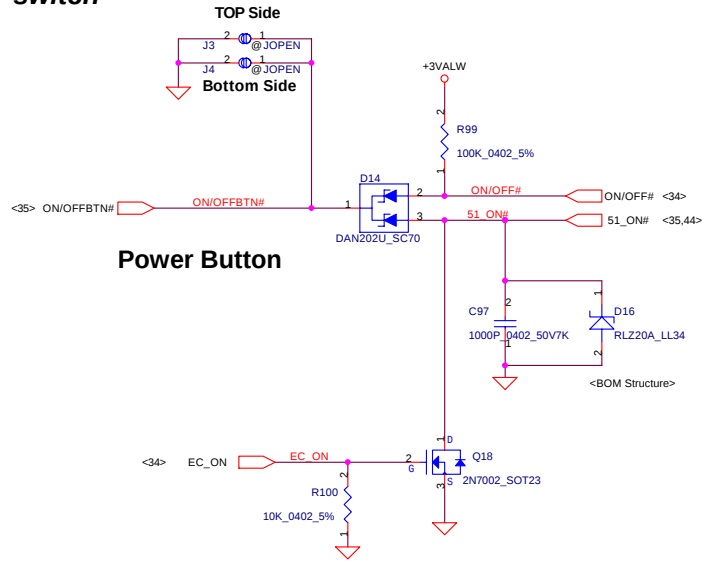


FOR LPC SIO DEBUG PORT

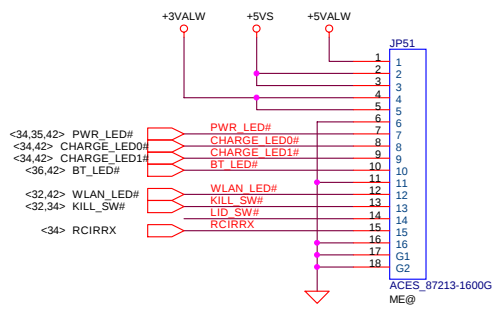


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2007/8/18				2007/8/18				Title			
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Size				Document Number				0			
B				IFTXX M/B LA-3541P Schematic				Date:			
Wednesday, November 01, 2006				Sheet				36 of 52			

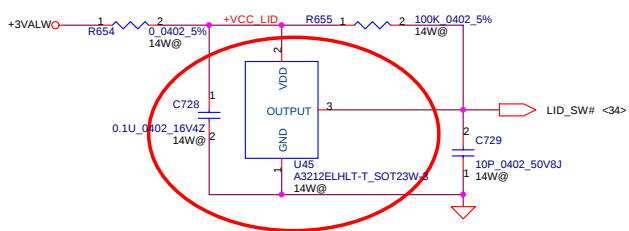
ON/OFF switch



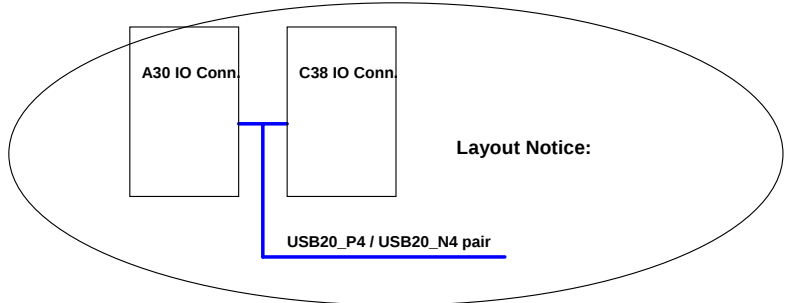
Front LED Board



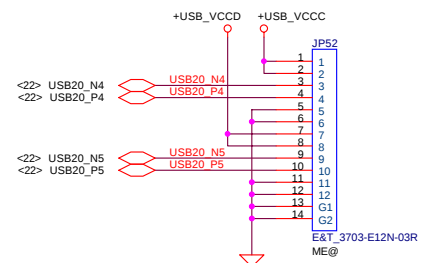
Lid Switch



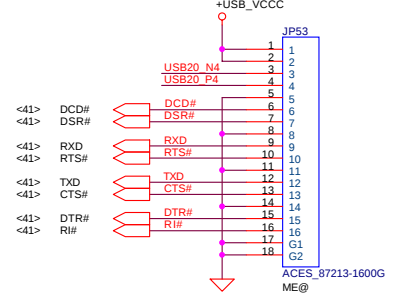
12/9 Change to SA032120010



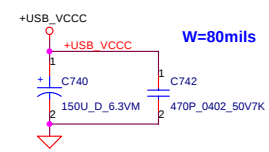
For A30 IO Conn.



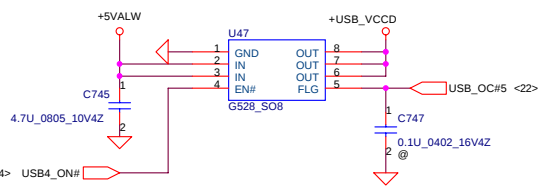
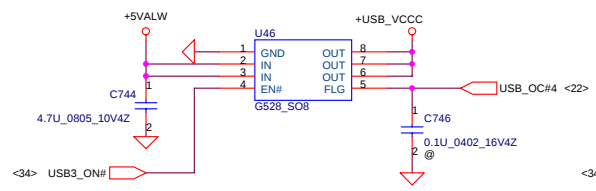
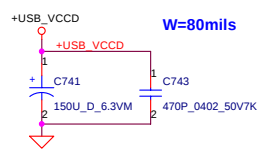
For C38 IO Conn.



To USB CONN. 3

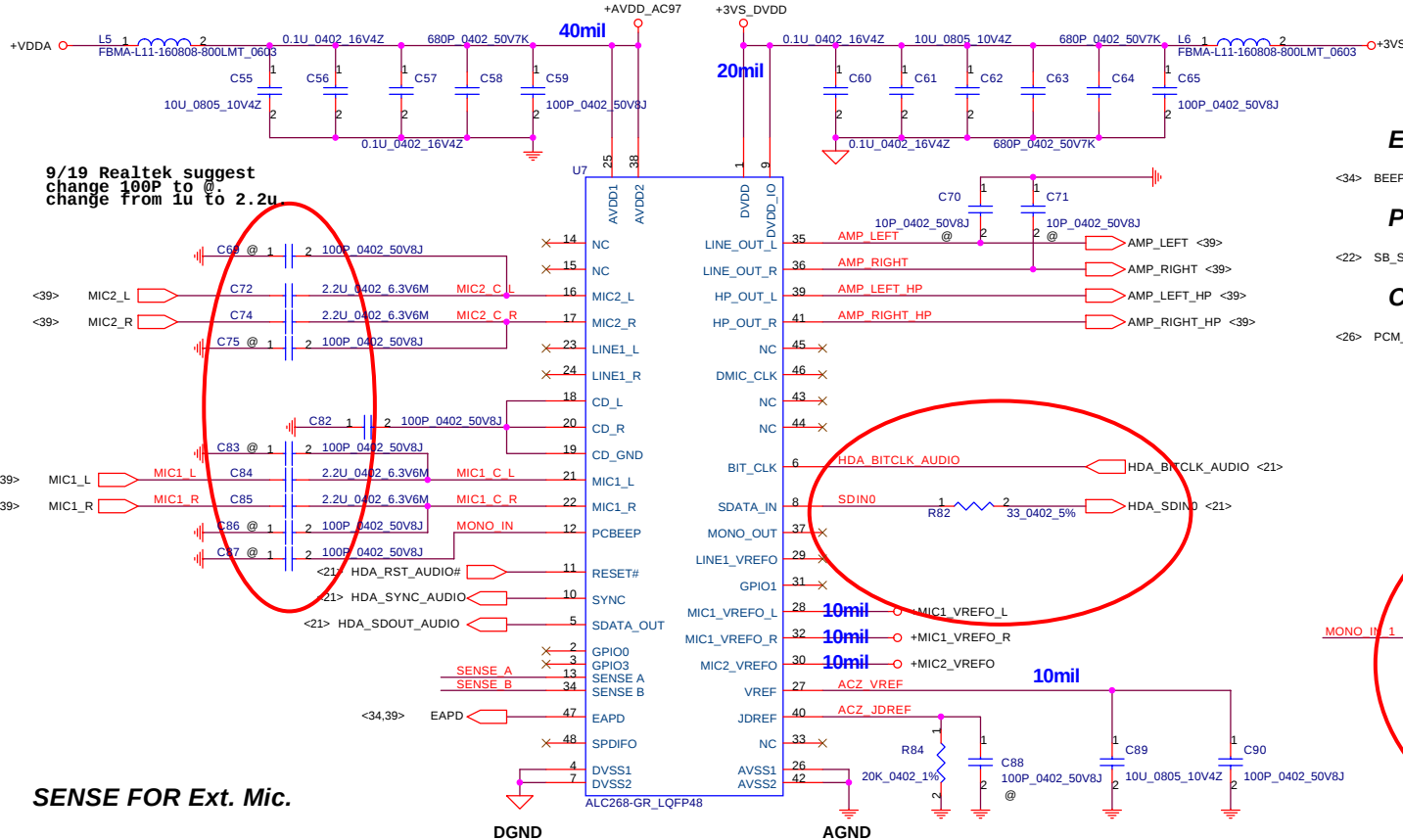


To USB CONN. 4



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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title							
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								Size B	Document Number			Rev 0			
								IFTXX M/B LA-3541P Schematic							
								Date:	Wednesday, November 01, 2006			Sheet	37	of	52
C				D				E							

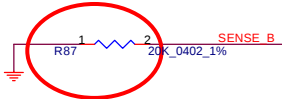
HD Audio Codec



SENSE FOR Ext. Mic.



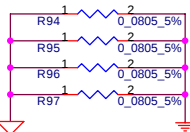
SENSE FOR Solo Int. Mic.



SENSE FOR HP

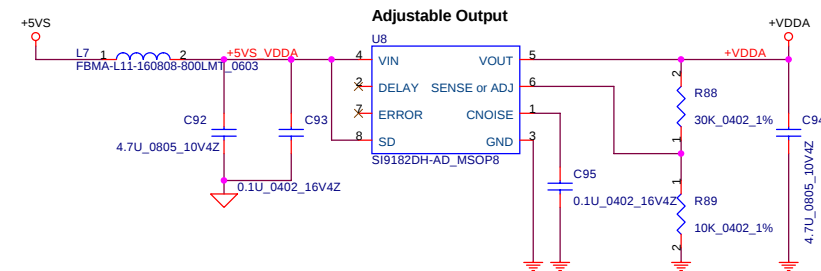


Moat Bridge

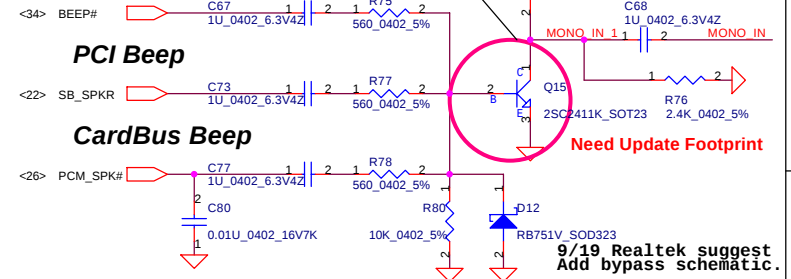


Sense Pin	Impedance	Codec Signals	Funnnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE Out
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

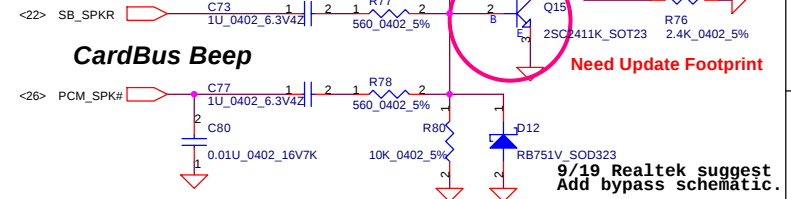
Regulator for CODEC



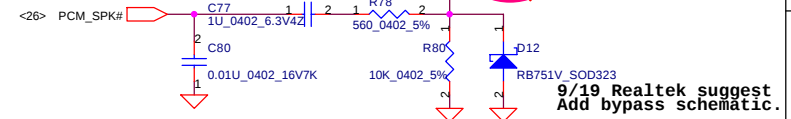
EC Bleep



PCI Bleep

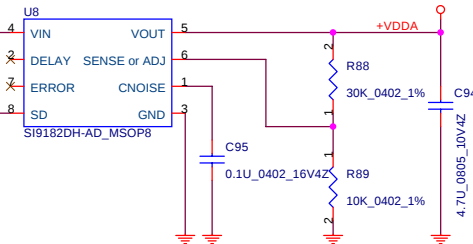


CardBus Bleep



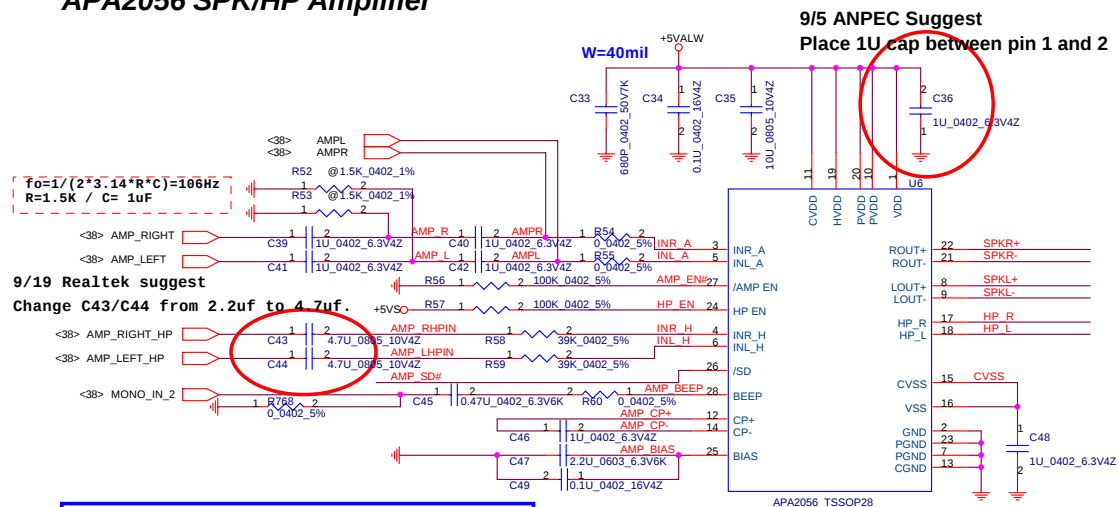
9/26 modified

Adjustable Output

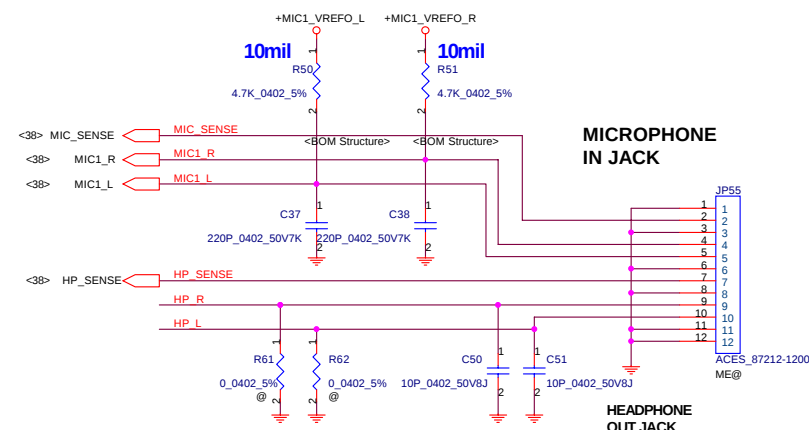


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	HD Audio Codec ALC268	
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				Custom	LA - 3541P	0.1
				Date:	Wednesday, November 14, 2006	Sheet 38 of 52

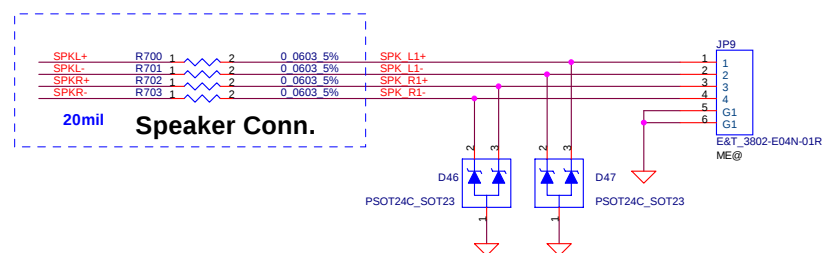
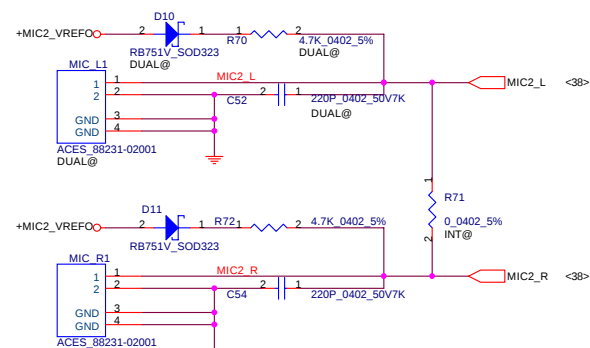
APA2056 SPK/HP Amplifier



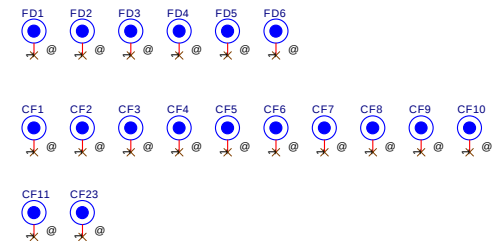
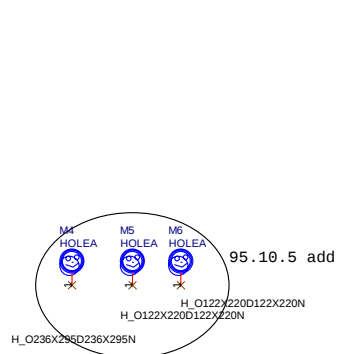
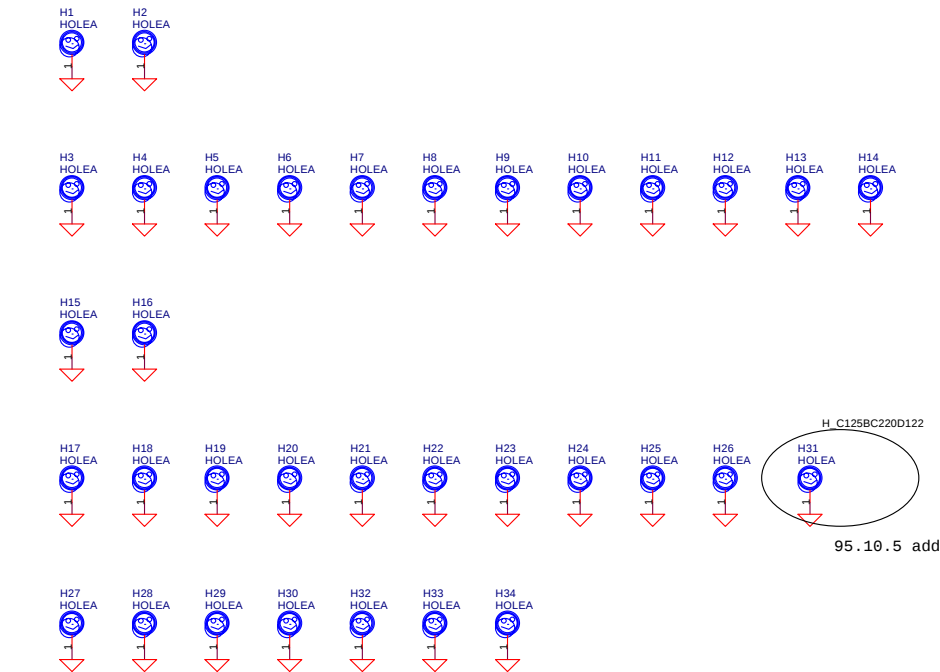
**9/5 If implement AMP BEEP, Swap C155 and R79.
R79 change from 0 Ohm to 47K**



SINGLE INT MIC/DUAL INT MIC

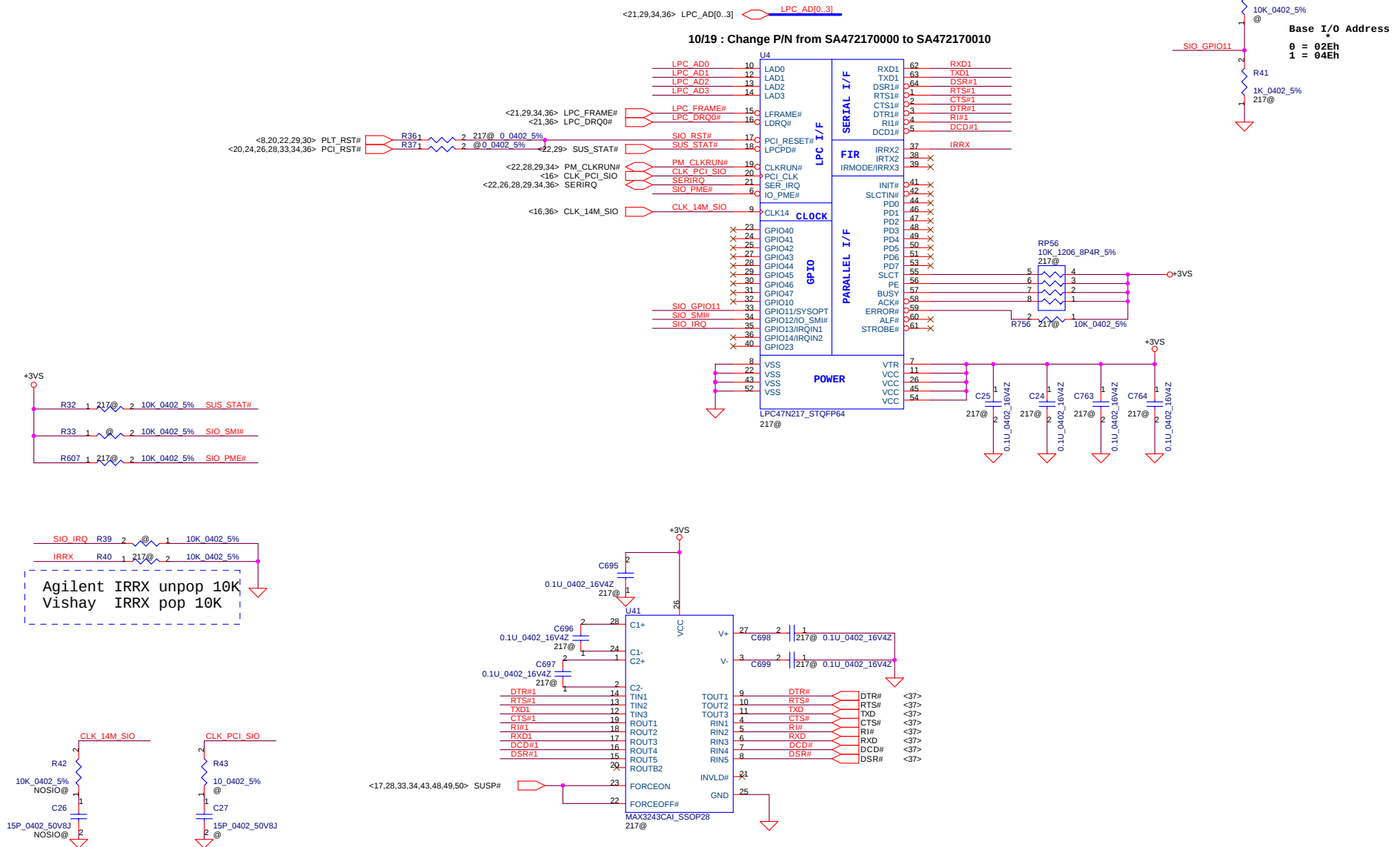


Security Classification		Compal Secret Data		Compal Electronics, Inc. Title AMP/VR/Audio Jack/MIC	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Size Document Number LA-3541P	Rev 0.1
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Size	Document Number	Rev			0
B	IFTXX M/B LA-3541P Schematic	Date:			Wednesday, November 01, 2006
Sheet		40		52	

SUPER I/O SMsC LPC47N217



9/18 modify this page following IGT1x

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				LA-3541P UMA	
				Date:	Wednesday, November 01, 2006
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				Rev	0.2

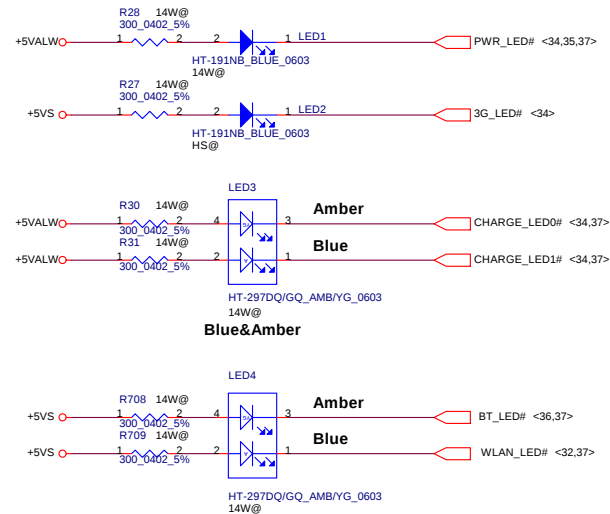
Diagram illustrating the MDC Rev1.5 connector (JP2) and its connections to the HDA (High Definition Audio) interface.

The connector (JP2) is a 18-pin connector. The connections are as follows:

- Pin 1: HDA_SDOUT_MDC
- Pin 2: HDA_SYNC_MDC
- Pin 3: HDA_SYNC_MDC
- Pin 4: HDA_SYNC_MDC
- Pin 5: HDA_SYNC_MDC
- Pin 6: HDA_SYNC_MDC
- Pin 7: HDA_SYNC_MDC
- Pin 8: HDA_SYNC_MDC
- Pin 9: HDA_SYNC_MDC
- Pin 10: HDA_SYNC_MDC
- Pin 11: HDA_SYNC_MDC
- Pin 12: HDA_SYNC_MDC
- Pin 13: HDA_SYNC_MDC
- Pin 14: HDA_SYNC_MDC
- Pin 15: HDA_SYNC_MDC
- Pin 16: HDA_SYNC_MDC
- Pin 17: HDA_SYNC_MDC
- Pin 18: HDA_SYNC_MDC

The HDA interface is connected to the MDC Rev1.5 connector via a 20mil signal trace. The HDA interface is labeled HDA_SYNC_MDC and HDA_RST_MDC#.

The MDC Rev1.5 connector is labeled **Connector for MDC Rev1.5** and **ACES_88018-124G ME@**.



Camera COM1

<34> CAMERA_ON#

R736

0.1U_0402_16V4Z

100K_0402_5%

Q52

Si2301BDS_SOT23

W=40mils

+5VS

+5VS_CMOS

C753

C754

C693

C755

4.7U_0805_10V4Z

0.1U_0402_16V4Z

1U_0603_10V4Z

USB20_N7

USB20_P7

JP3

1

2

3

4

5

6

7

8

GND1

GND2

ACES_88266-05001

ME@

D1

PSOT24C_SOT23

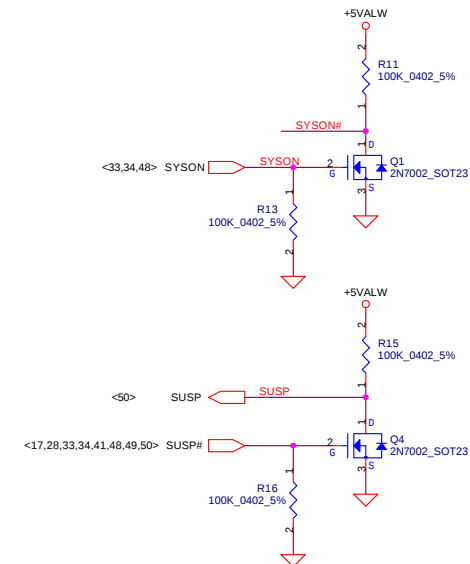
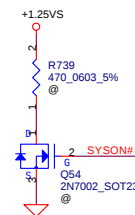
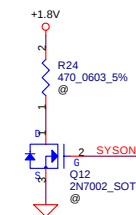
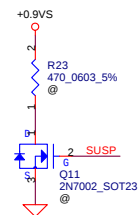
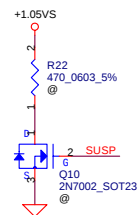
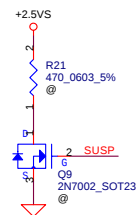
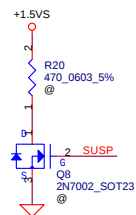
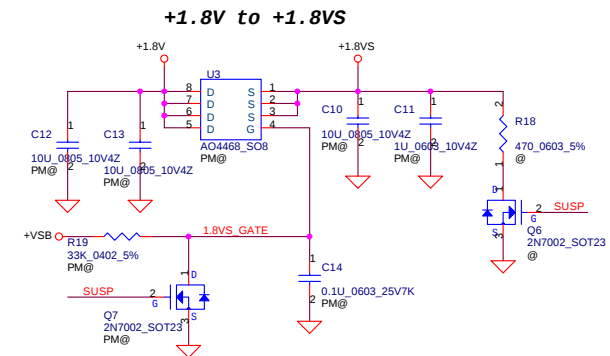
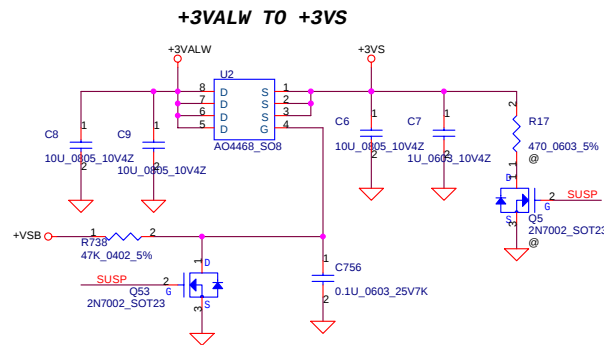
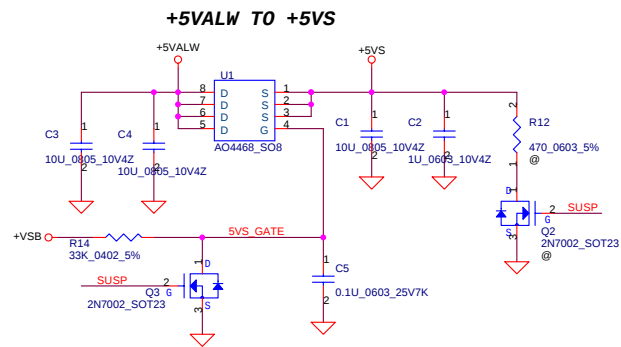
C17

C18

4.7U_0805_10V4Z

0.1U_0402_16V4Z

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				Size B	Document Number			Rev 0
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				IFTXX M/B LA-3541P Schematic	
				Date:	Wednesday, November 01, 2006
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