LA-1641 REV0.2 Schematic Document

Intel Mobile P4 uFCBGA/uFCPGA Northwood Celeron
with Montara GML / ICH4-M / Integrated VGA

2002-11-20

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Compal Electronics, Ltd.

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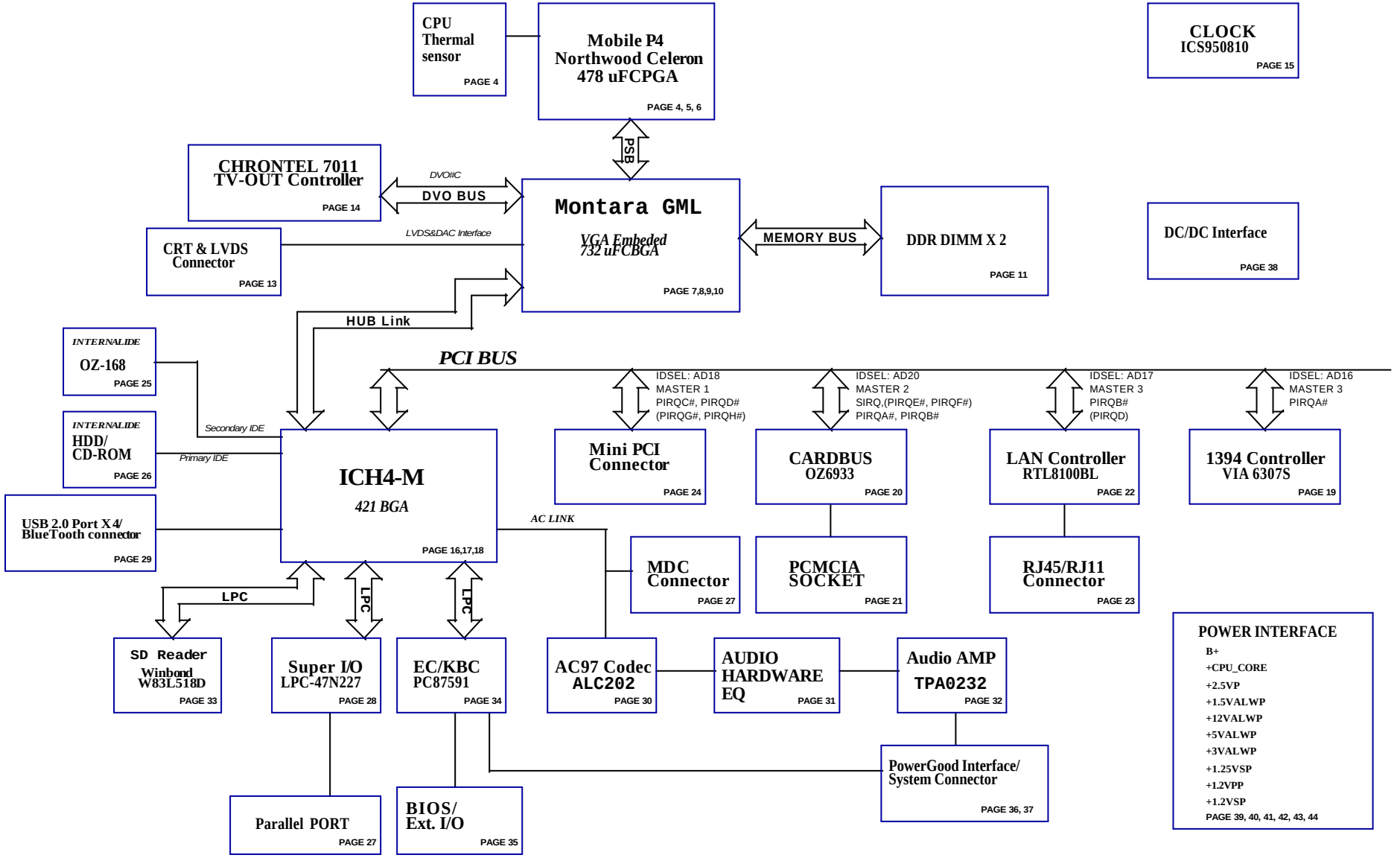
COMPAL CONFIDENTIAL

REV:0.3



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_VCC	Core voltage forCPU	ON	OFF	OFF
+1.2VP	1.2V switched power rail for CPU AGTLBus	ON	OFF	OFF
+1.2VS	1.2V switched power rail for Montara core	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB(PIRQE/PIRQF)
LAN	AD17	3	PIRQB(PIRQD)
Mini-PCI	AD18	1/1	PIRQC/PIRQD(PIRQG/PIRQH)
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b
OZ168	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH4 SM Bus address

Device	Address
Clock Generator (ICS-950810)	1101 001X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

Sapporo Z to ZJ BOM modify list :

1. Remove R594
2. Add R112

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Title: Note List

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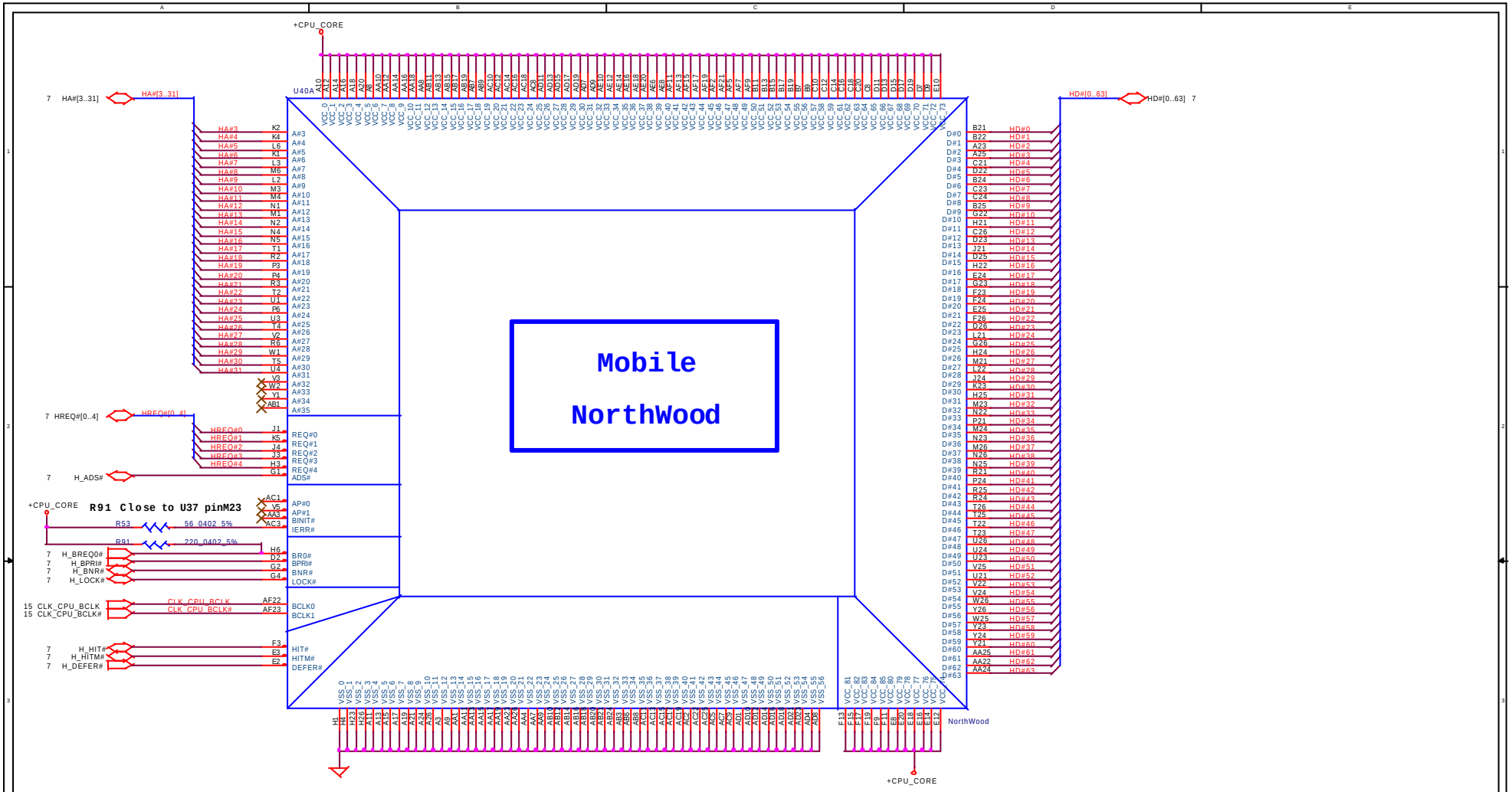
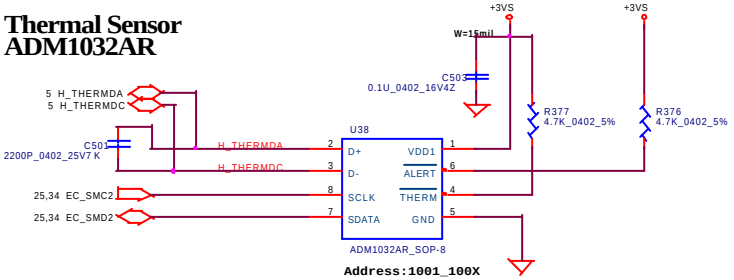


Thermal Sensor ADM1032AR



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Compal Electronics, Ltd.		
Title: Mobile P4-Celeron (1/2)		
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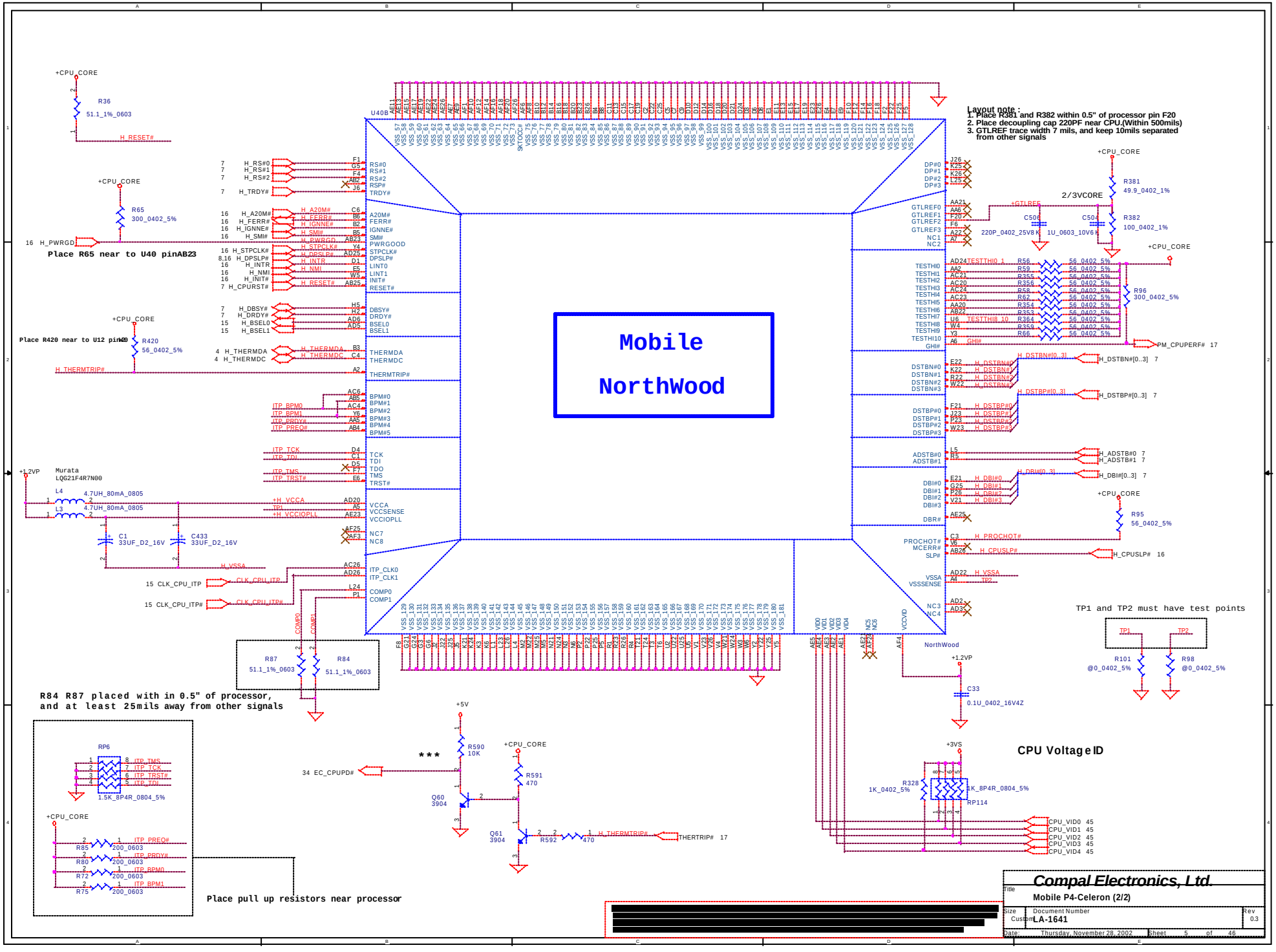
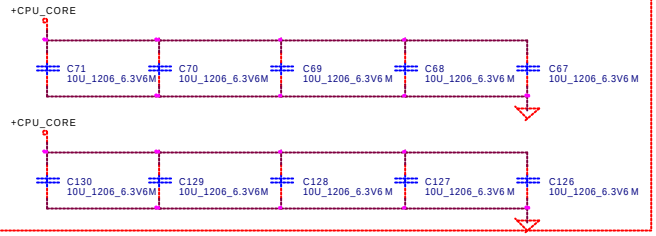

Mobile
NorthWood
U40B
Layout note :
1. Place R381 and R382 within 0.5" of processor pin F20
2. Place decoupling cap 220PF near CPU.(Within 500mils)
3. GTLREF trace width 7 mils, and keep 10mils separated from other signals
Place R65 near to U40 pinAB23
Place R420 near to U12 pin29
R84 R87 placed with in 0.5" of processor, and at least 25mils away from other signals
Place pull up resistors near processor
TP1 and TP2 must have test points
CPU VoltageID
NorthWood
Compal Electronics, Ltd.
Mobile P4-Celeron (2/2)
LA-1641
Thursday, November 28, 2002

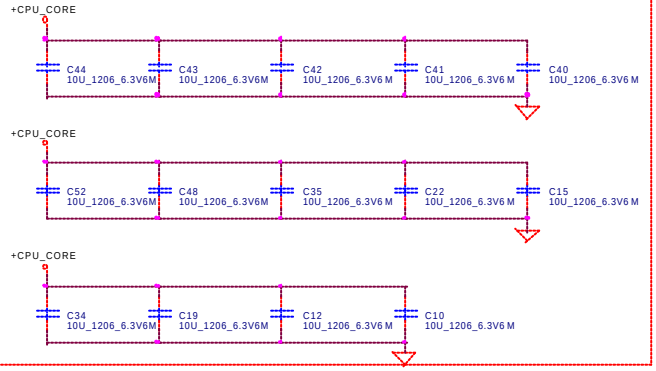
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

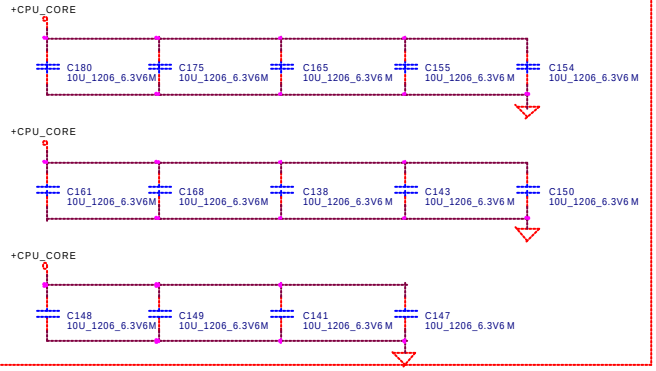
Please place these cap in the socket cavity area



Please place these cap on the socket north side



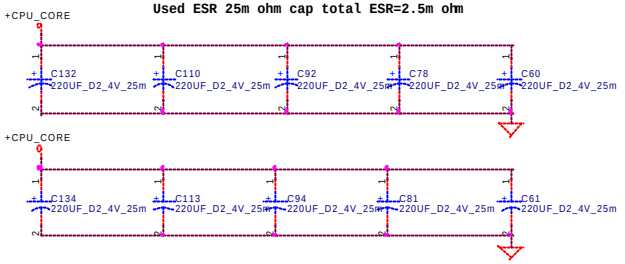
Please place these cap on the socket south side

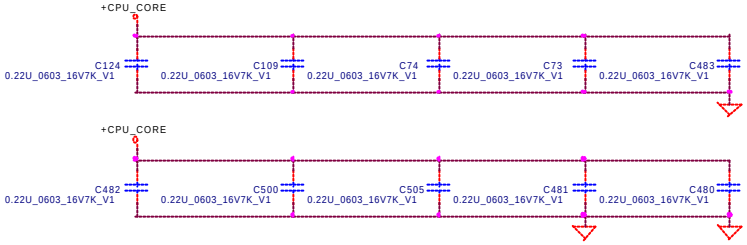


Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm





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Title: CPU Decoupling

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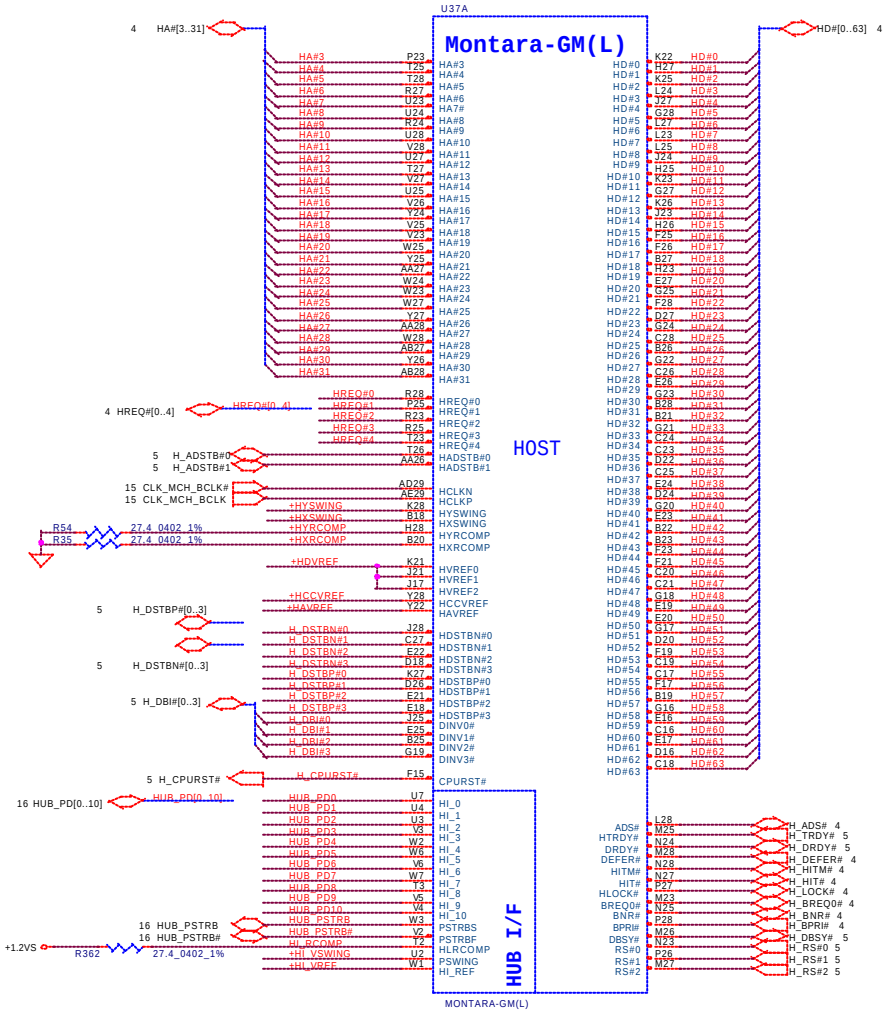
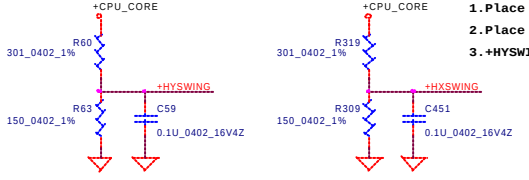


Layout Note:

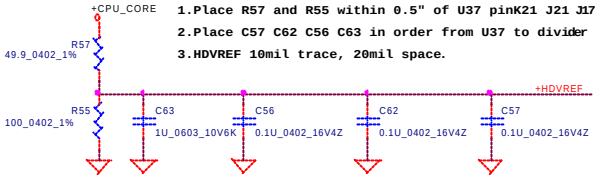
1. Place R35 and R54 within 0.5" of U37 pinH28 B20
2. Both HYRCOMP and HXRCOMP trace width are 18mil and 25mils away from other signals

HXSWING and HYSWING Ref. Voltage



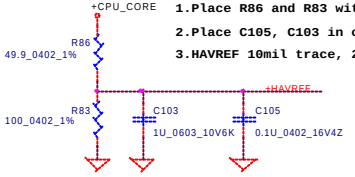
1. Place R60 and R63 within 0.5" of U37 pinK28
2. Place R319 and R309 within 0.5" of U37 pinB18
3. +HYSWING, +HXSWING 10mil trace, 20mil space.

Host data Ref. Voltage



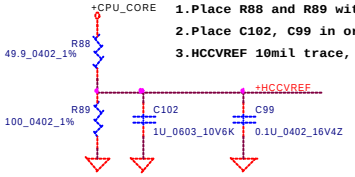
1. Place R57 and R55 within 0.5" of U37 pinK21 J21 J17
2. Place C57 C62 C56 C63 in order from U37 to divider
3. HDVREF 10mil trace, 20mil space.

Host address Ref. Voltage



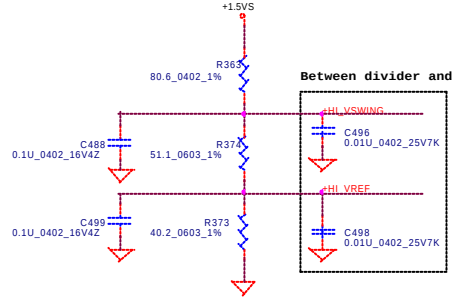
1. Place R86 and R83 within 0.5" of U37 pinY22
2. Place C105, C103 in order from U37 to divider
3. HAVREF 10mil trace, 20mil space.

Host common clock Ref. Voltage



1. Place R88 and R89 within 0.5" of U37 pinY28
2. Place C102, C99 in order from U37 to divider
3. HCCVREF 10mil trace, 20mil space.

HUB I/F REF VOLTAGE



Place this schematic close to GMCH

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Title	Montara-GML (HOST)	
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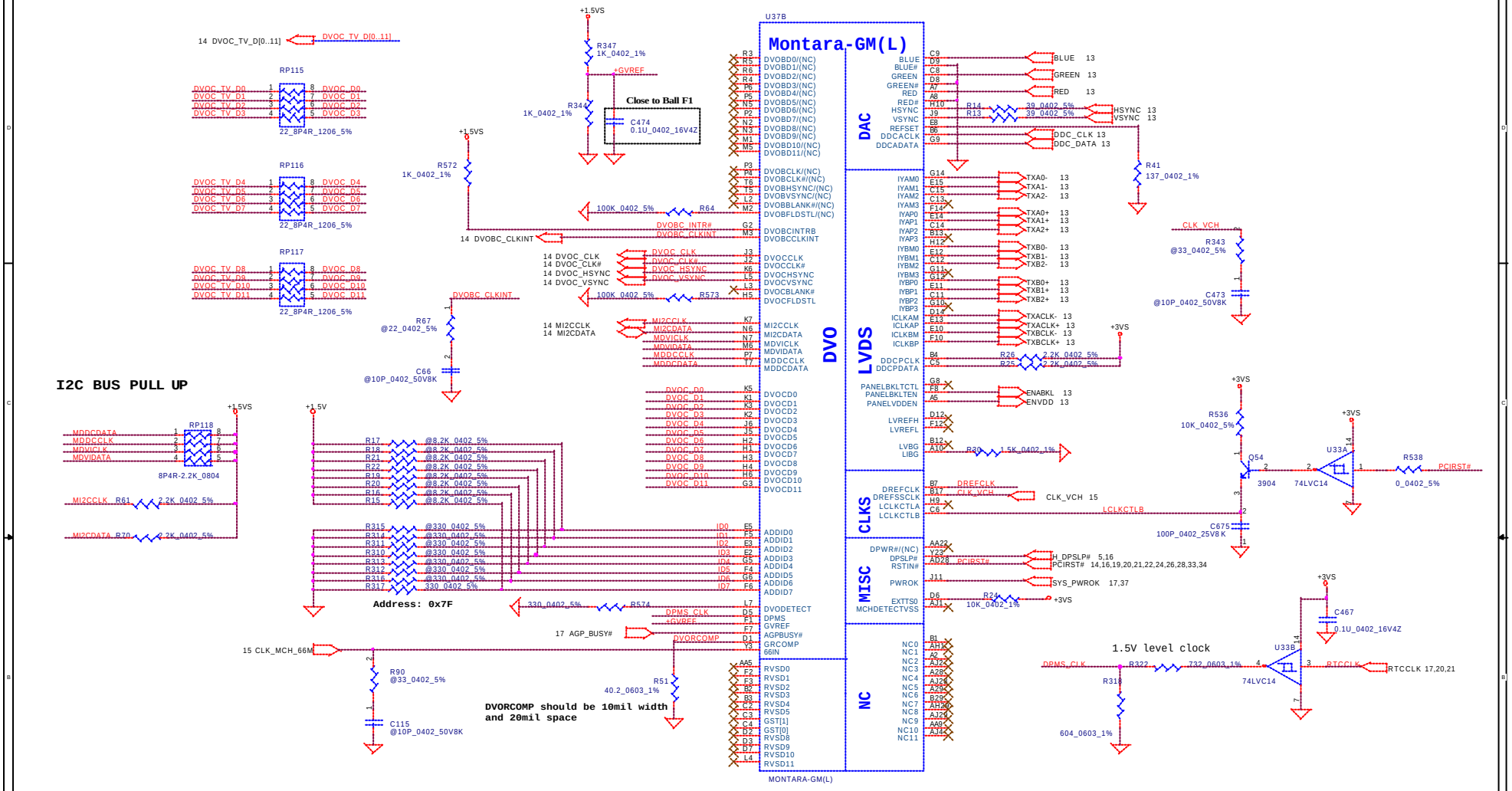

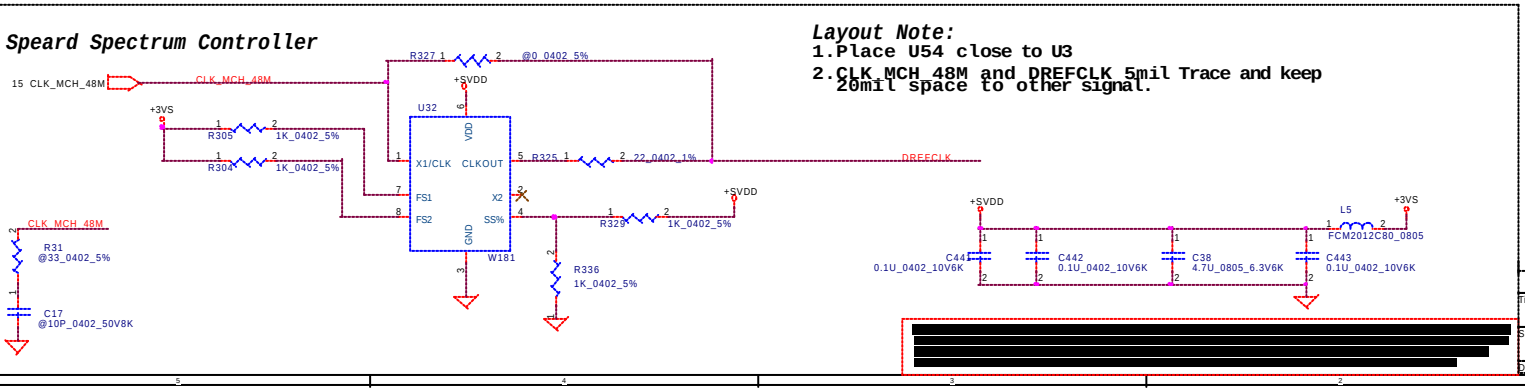

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Compal Electronics, Ltd.		
Title: Montara-GML (LVDS)		
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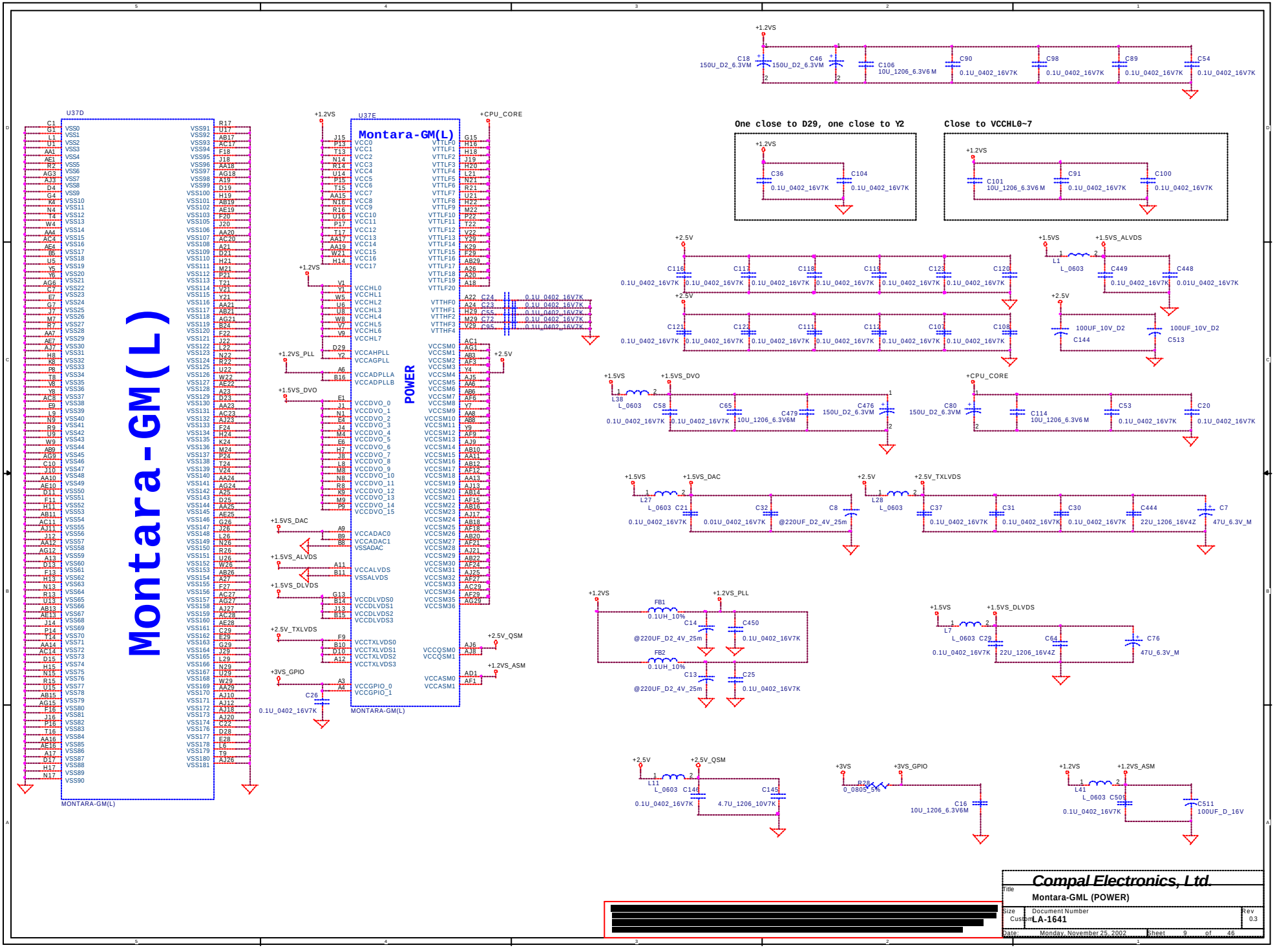
Montara-GM(L)
U37D
MONTARA-GM(L)
U37E
Montara-GM(L)
POWER
MONTARA-GM(L)
One close to D29, one close to Y2
Close to VCCHL0~7
+1.2VS
+CPU_CORE
+2.5V
+1.5VS
+1.5VS_ALVDS
+1.2VS_PLL
+1.5VS_DVO
+1.5VS_DAC
+1.5VS_DLVDS
+2.5V_TXLVDS
+2.5V_QSM
+1.2VS_ASM
+3VS_GPIO
+3VS
Compal Electronics, Ltd.
Montara-GML (POWER)
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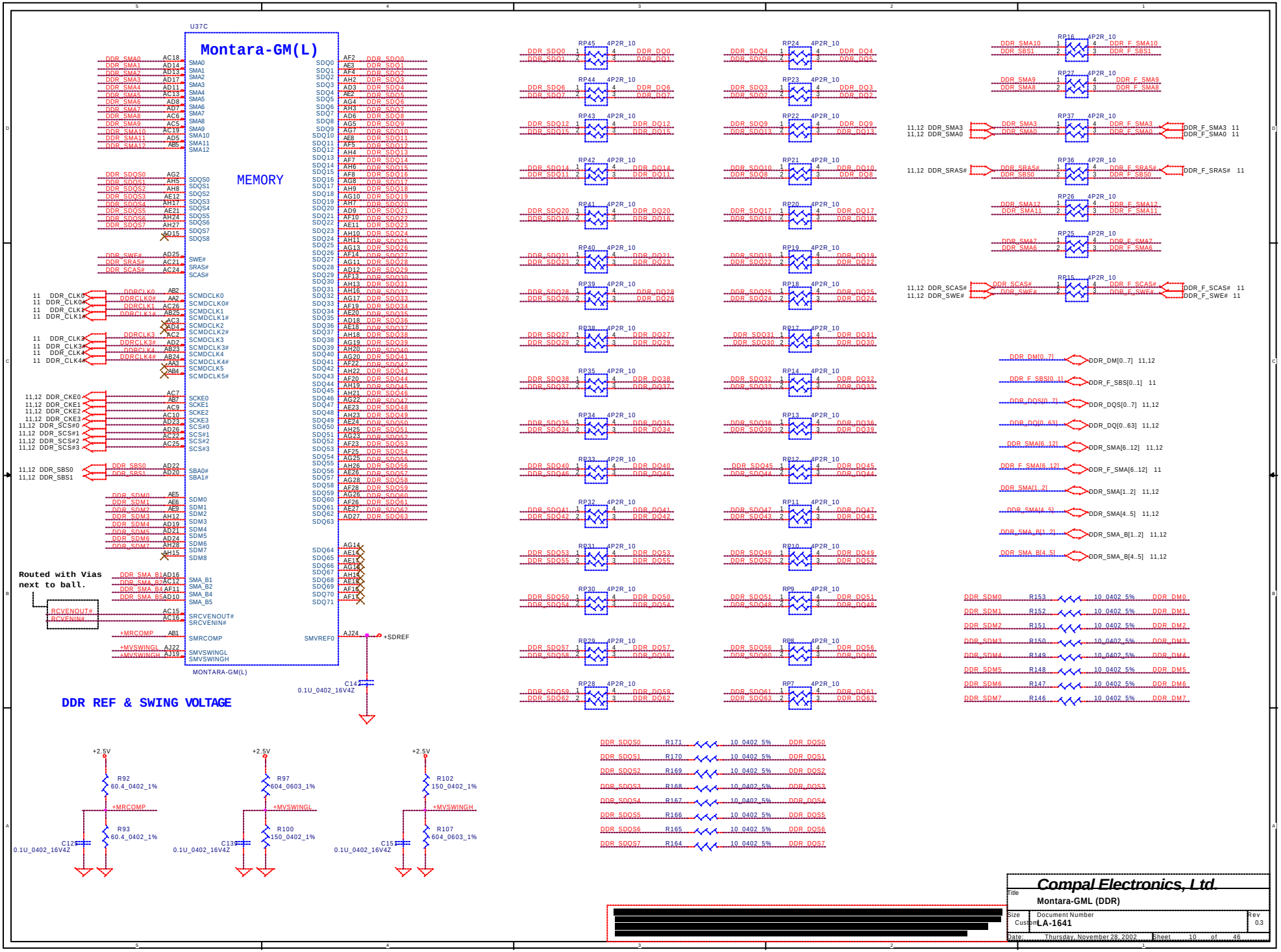
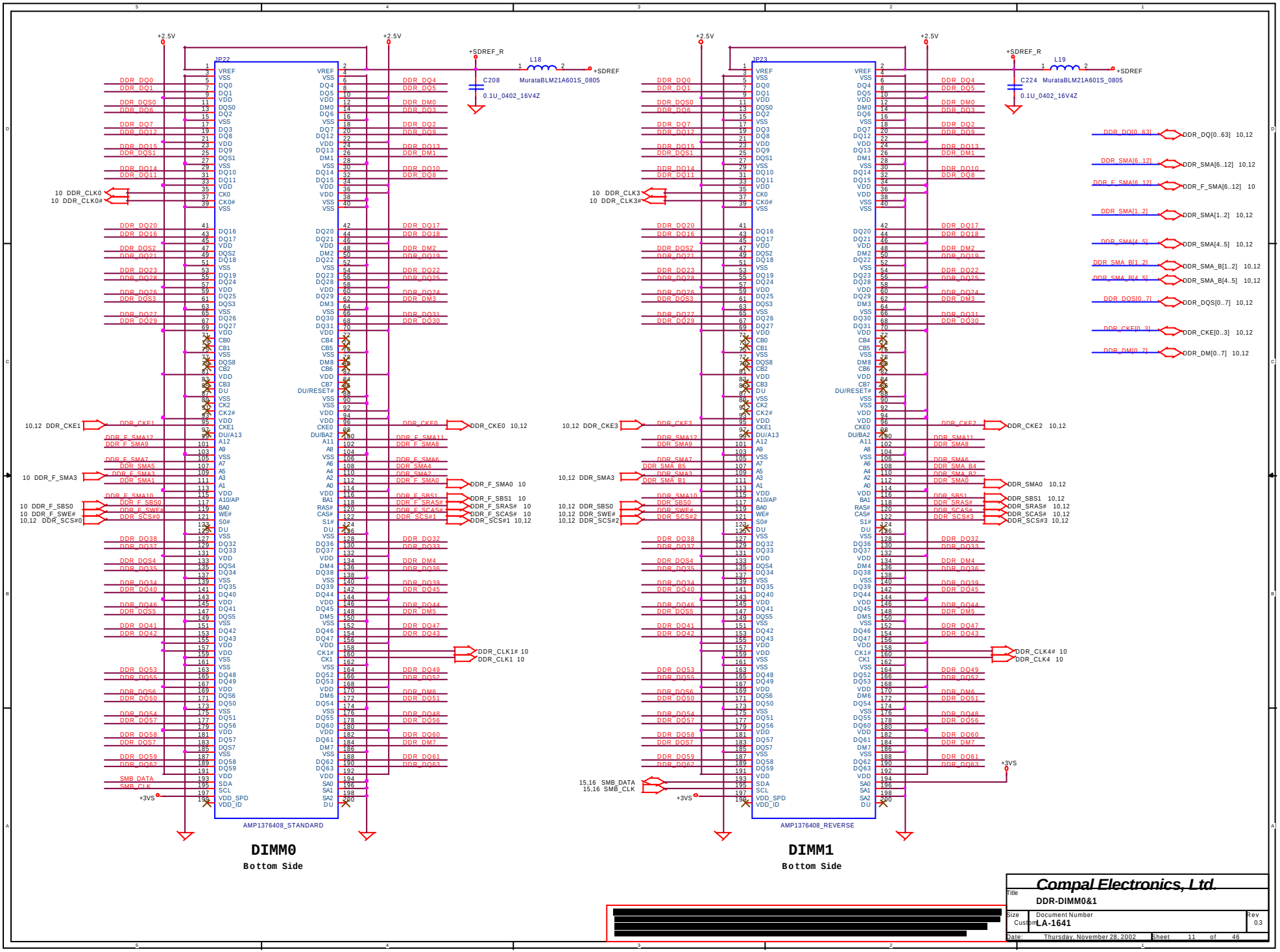

U37C
Montara-GM(L)
MEMORY
MONTARA-GM(L)
Routed with Vias
next to ball.
DDR REF & SWING VOLTAGE
Compal Electronics, Ltd.
Montara-GML (DDR)
LA-1641
Thursday, November 28, 2002



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Title	DDR-DIMM0&1	
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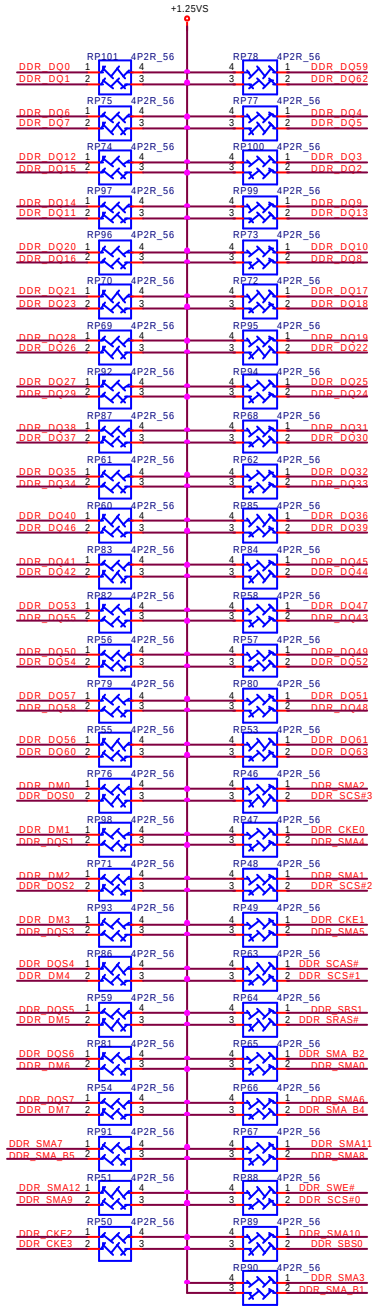
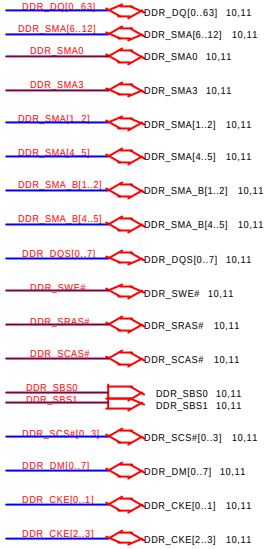
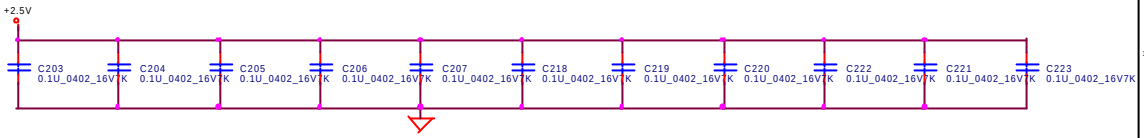
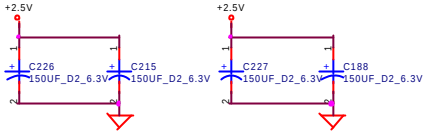


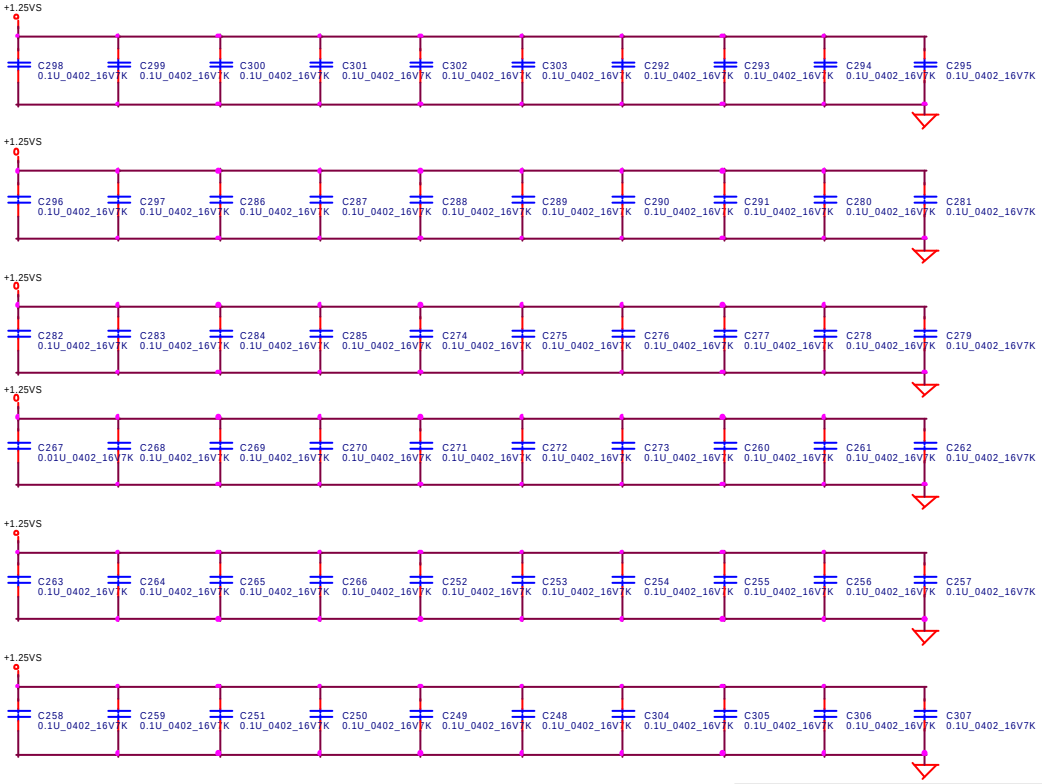


Layout note :
Distribute as close as possible to DDR-SODIMM.





Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



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Title: DDR Pull-up and Decoupling

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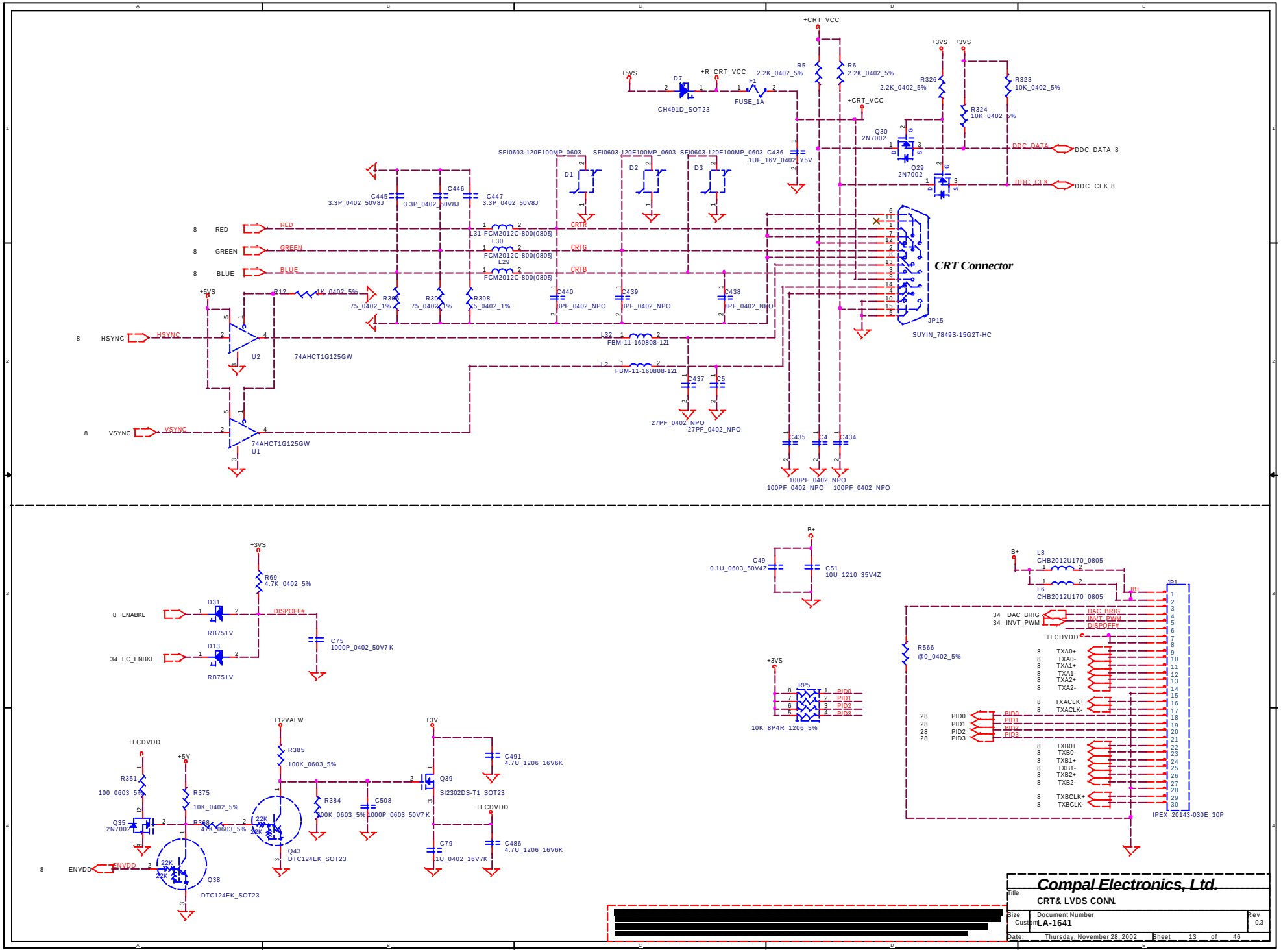
+CRT_VCC
+5VS
+R_CRT_VCC
D7
CH491D_SOT23
F1
FUSE_1A
R5
2.2K_0402_5%
R6
2.2K_0402_5%
+3VS
R326
2.2K_0402_5%
R323
10K_0402_5%
R324
10K_0402_5%
Q30
2N7002
Q29
2N7002
DDC_DATA
DDC_CLK
DDC_DATA 8
DDC_CLK 8
SFI0603-120E100MP_0603
D1
D2
D3
C436
.1UF_16V_0402_Y5V
C445
3.3P_0402_50V8J
C446
3.3P_0402_50V8J
C447
3.3P_0402_50V8J
8 RED
8 GREEN
8 BLUE
RED
GREEN
BLUE
CRTR
CRTG
CRTB
L31 FCM2012C-800(0805)
L30 FCM2012C-800(0805)
L29 FCM2012C-800(0805)
CRT Connector
JP15
SUYIN_7849S-15G2T-HC
R12
1K_0402_5%
R309
75_0402_1%
R307
75_0402_1%
R308
75_0402_1%
C440
8PF_0402_NPO
C439
8PF_0402_NPO
C438
8PF_0402_NPO
8 HSYNC
HSYNC
U2
74AHCT1G125GW
L32
FBM-11-160808-121
L2
FBM-11-160808-121
C437
27PF_0402_NPO
C5
27PF_0402_NPO
8 VSYNC
VSYNC
74AHCT1G125GW
U1
C435
100PF_0402_NPO
C4
100PF_0402_NPO
C434
100PF_0402_NPO
+3VS
R69
4.7K_0402_5%
D31
RB751V
D13
RB751V
8 ENABKL
34 EC_ENBKL
DISPOFF#
C75
1000P_0402_50V7 K
B+
C49
0.1U_0603_50V4Z
C51
10U_1210_35V4Z
L8
CHB2012U170_0805
L6
CHB2012U170_0805
JP1
34 DAC_BRIG
34 INVT_PWM
DAC_BRIG
INVT_PWM
DISPOFF#
+LCDVDD
R566
@0_0_0402_5%
8 TXA0+
8 TXA0-
8 TXA1+
8 TXA1-
8 TXA2+
8 TXA2-
8 TXACLK+
8 TXACLK-
8 TXB0+
8 TXB0-
8 TXB1+
8 TXB1-
8 TXB2+
8 TXB2-
8 TXBCLK+
8 TXBCLK-
28 PID0
28 PID1
28 PID2
28 PID3
RP5
10K_8P4R_1206_5%
IPEX_20143-030E_30P
+LCDVDD
+5V
+12VALW
+3V
R351
100_0603_5%
R375
10K_0402_5%
R385
100K_0603_5%
R384
100K_0603_5%
C508
1000P_0603_50V7 K
Q39
SI2302DS-T1_SOT23
C491
4.7U_1206_16V6K
C79
1U_0402_16V7K
C486
4.7U_1206_16V6K
Q35
2N7002
R368
47K_0603_5%
22K
22K
Q43
DTC124EK_SOT23
8 ENVDD
ENVDD
22K
22K
Q38
DTC124EK_SOT23
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CRT& LVDS CONN.
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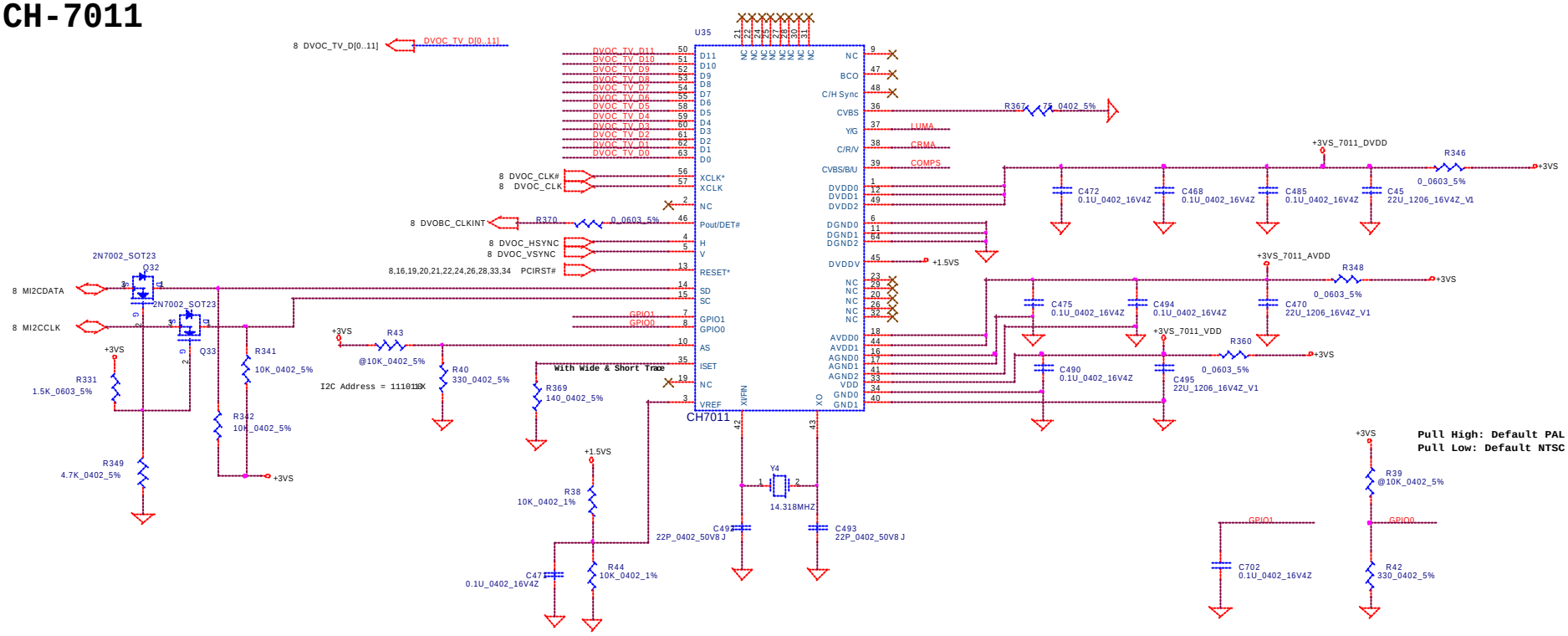
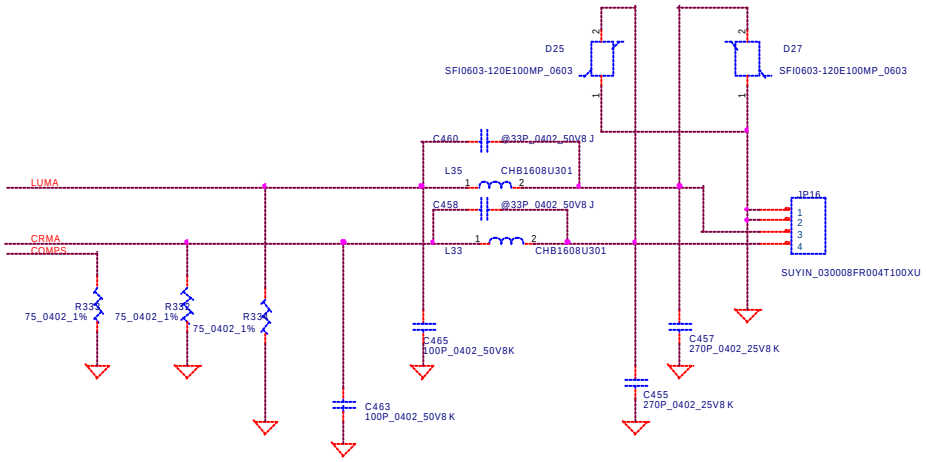
CH-7011



TV-OUT CONN.



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Compal Electronics, Ltd.

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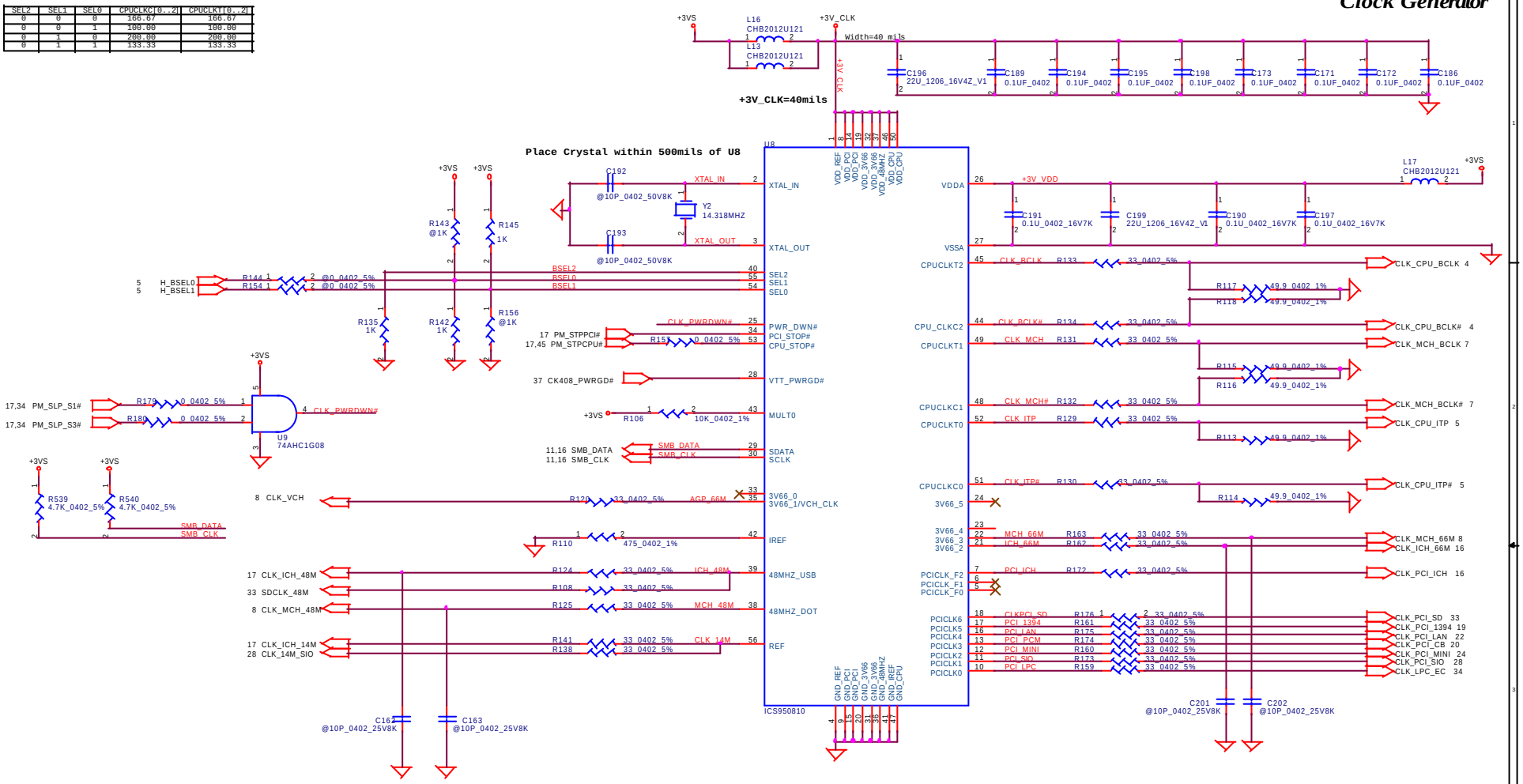
Clock Generator

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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Compal Electronics, Ltd.		
Title: Clock Generator		
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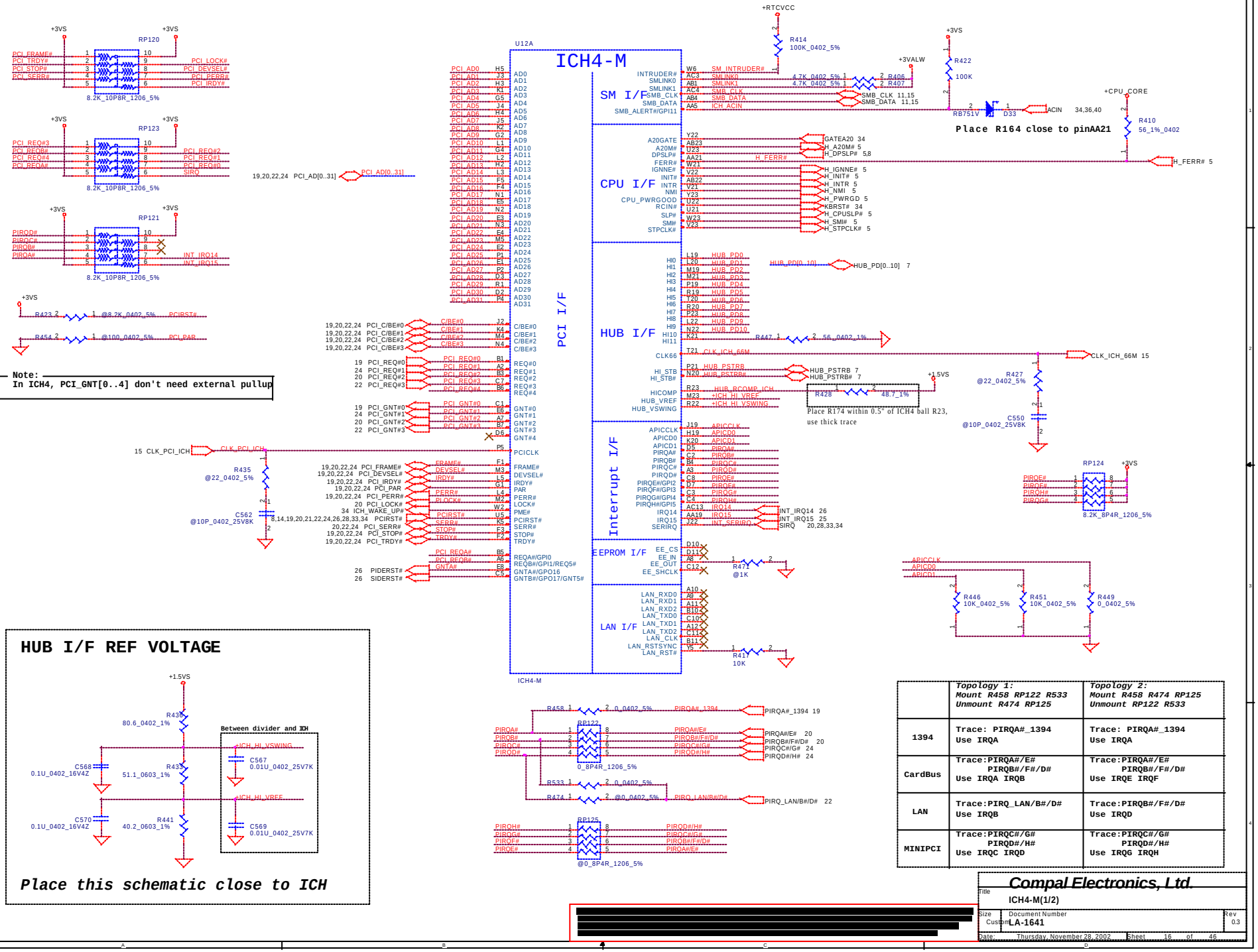
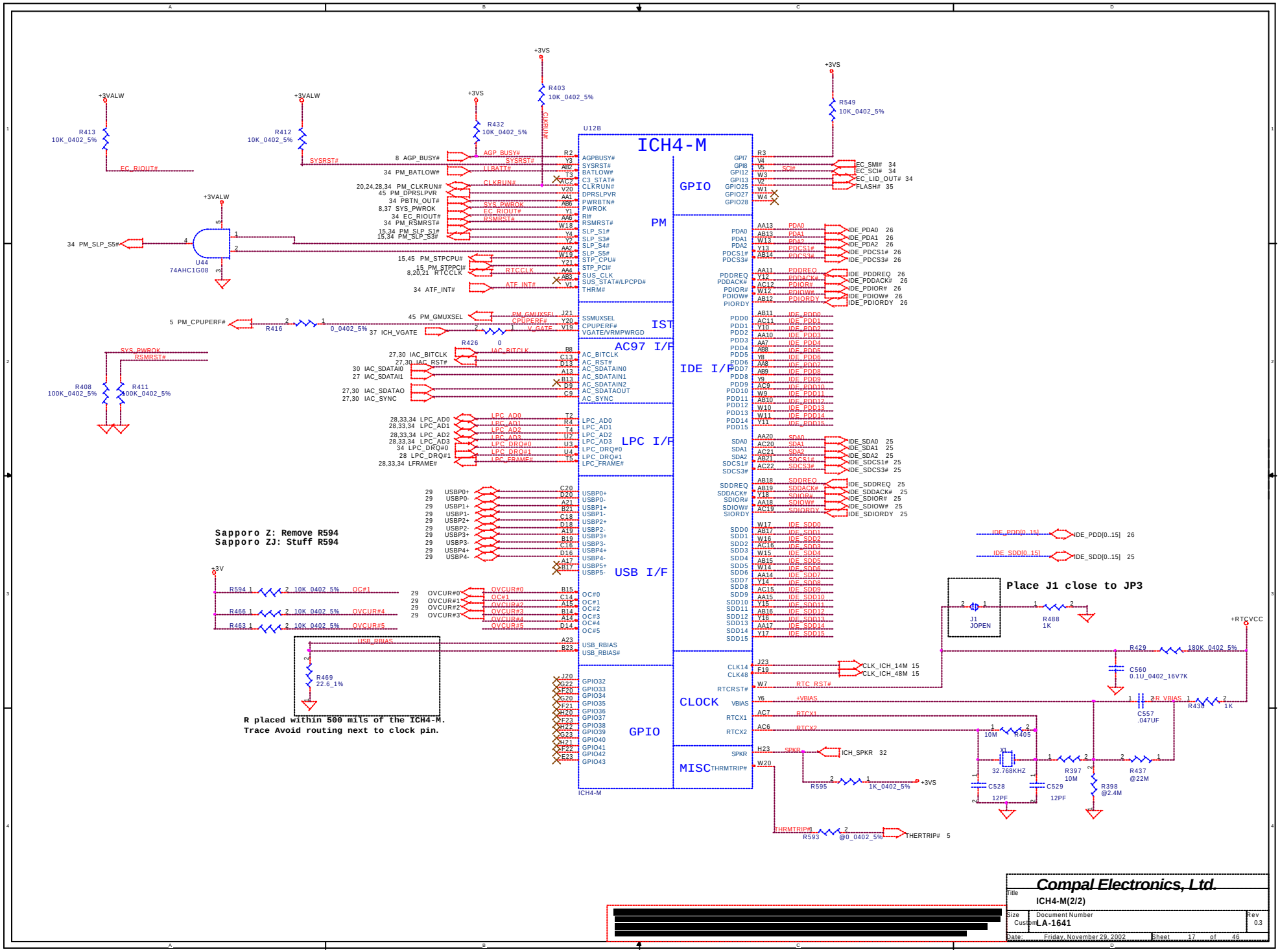

ICH4-M
U12A
PCI I/F
SM I/F
CPU I/F
HUB I/F
Interrupt I/F
EEPROM I/F
LAN I/F
Note:
In ICH4, PCI_GNT[0..4] don't need external pullup
Place R164 close to pinAA21
Place R174 within 0.5" of ICH4 ball R23, use thick trace
HUB I/F REF VOLTAGE
Between divider and ICH
Place this schematic close to ICH
Topology 1: Mount R458 RP122 R533 Unmount R474 RP125
Topology 2: Mount R458 R474 RP125 Unmount RP122 R533
1394
CardBus
LAN
MINIPCI
Trace: PIRQA#_1394 Use IRQA
Trace:PIRQA#/E# PIRQB#/F#/D# Use IRQA IRQB
Trace:PIRQ_LAN/B#/D# Use IRQB
Trace:PIRQC#/G# PIRQD#/H# Use IRQC IRQD
Trace:PIRQA#/E# PIRQB#/F#/D# Use IRQE IRQF
Trace:PIRQB#/F#/D# Use IRQD
Trace:PIRQC#/G# PIRQD#/H# Use IRQG IRQH
Compal Electronics, Ltd.
ICH4-M(1/2)
LA-1641
Thursday, November 28, 2002



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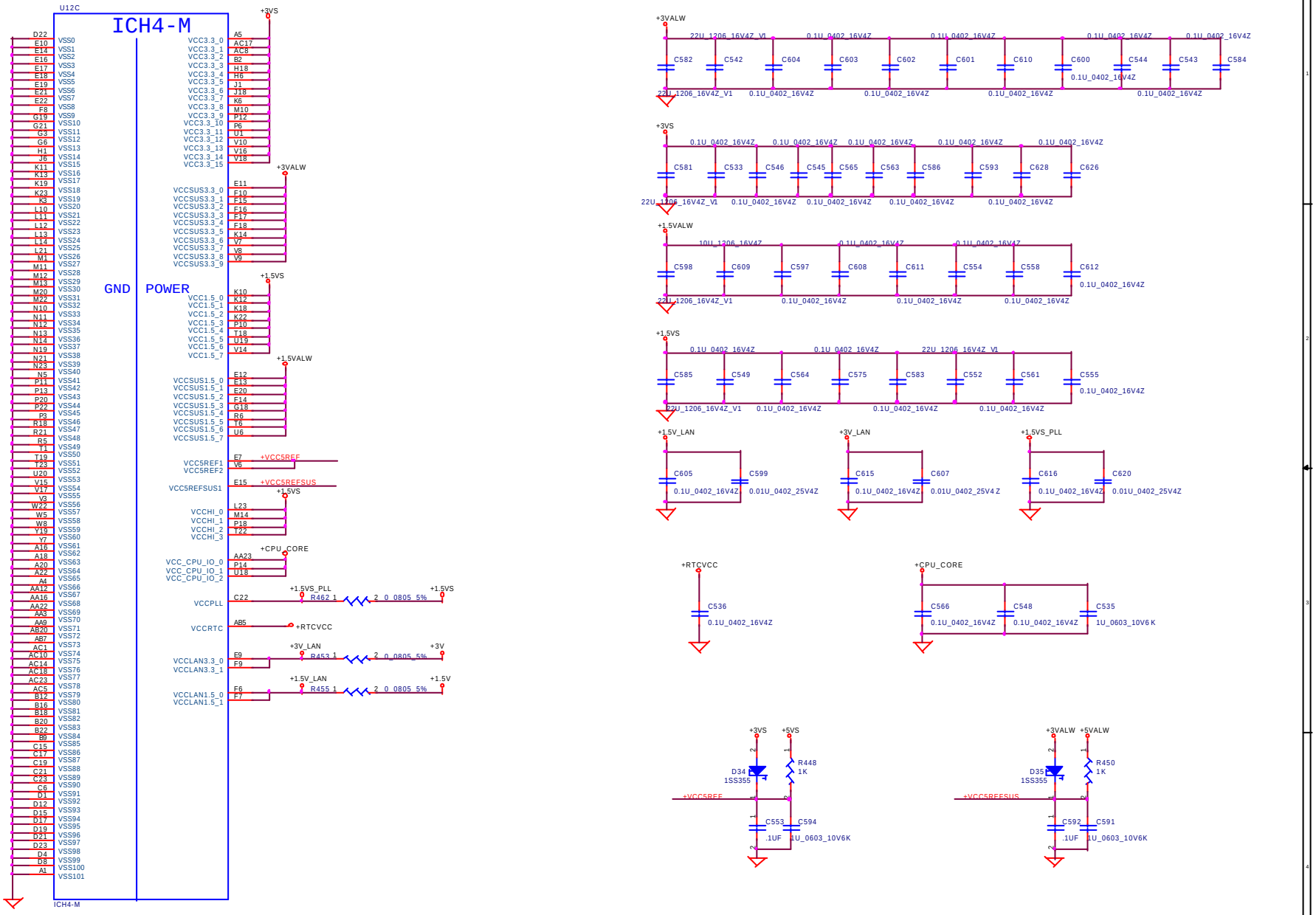
Compal Electronics, Ltd.

Title	ICH4-M(2/2)	
Size: Custom	Document Number: LA-1641	Rev: 0.3
Date: Friday, November 29, 2002	Sheet 17 of 46	



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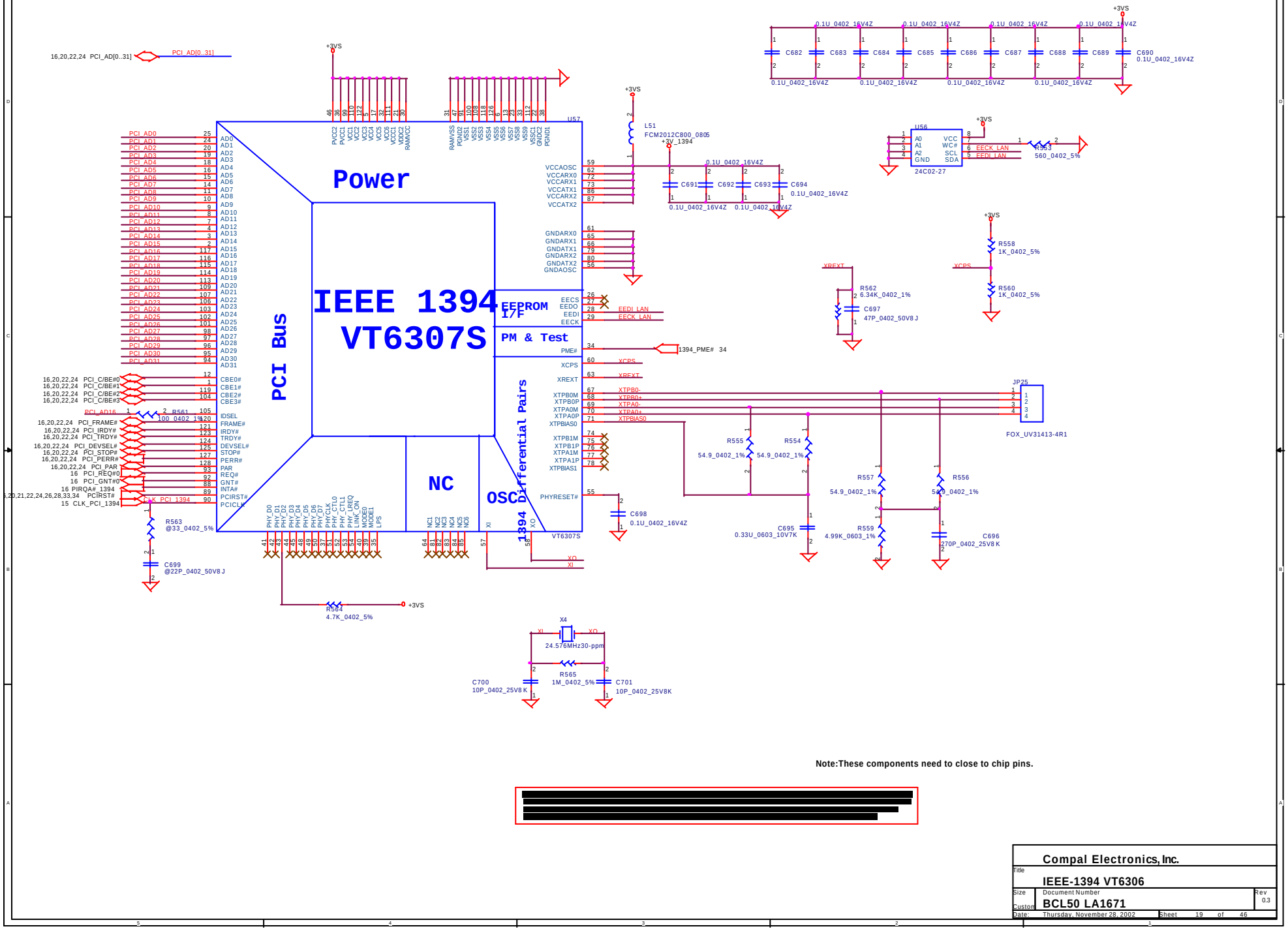
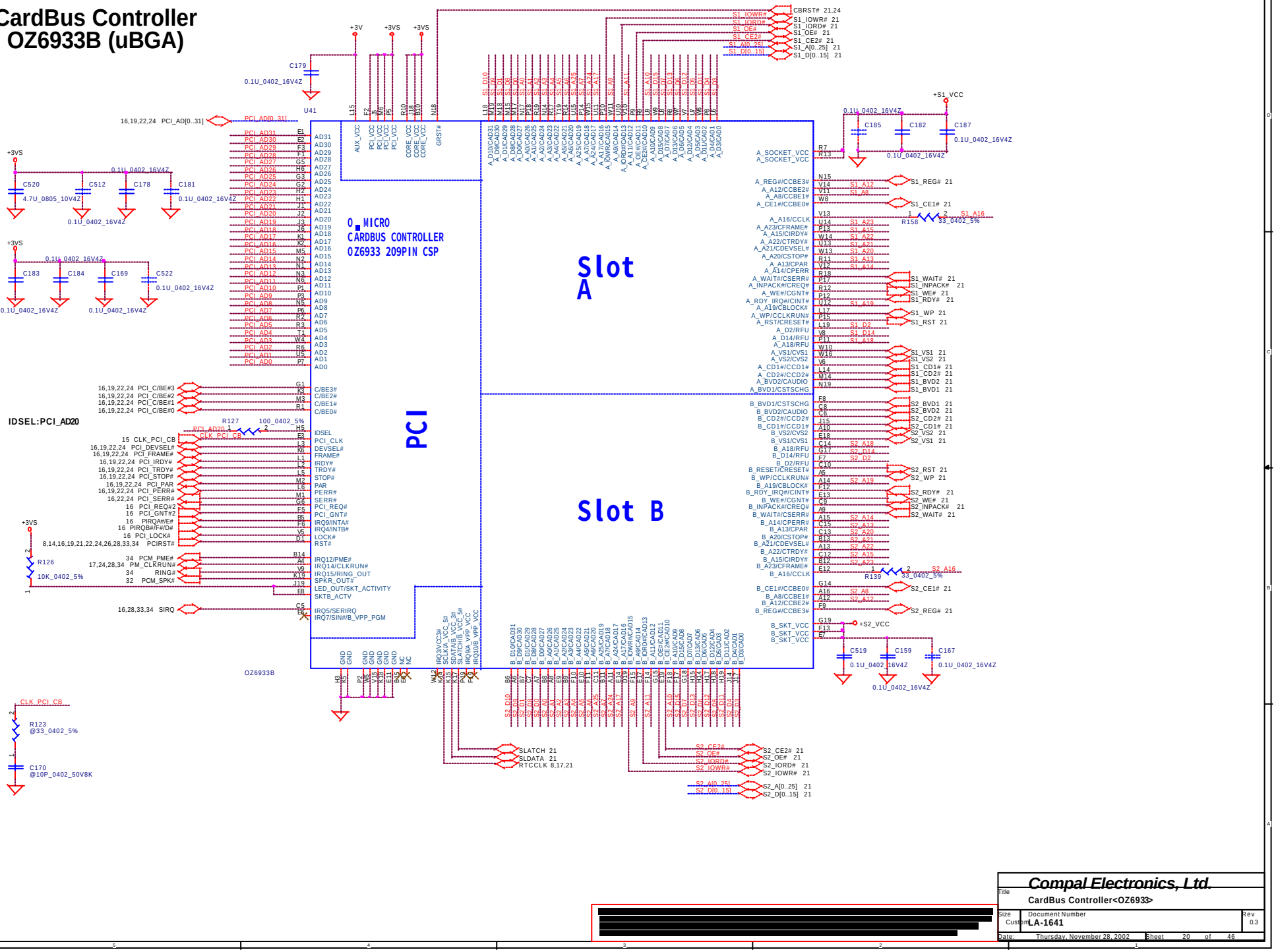
Compal Electronics, Ltd.		
Title: ICH4-M Pullups & Decoupling		
Size: Custom	Document Number: LA-1641	Rev: 0.3
Date: Monday, November 25, 2002	Sheet 18 of 46	



Compal Electronics, Inc.	
Title	IEEE-1394 VT6306
Size / Document Number	BCL50 LA1671
Rev	0.3
Date: Thursday, November 28, 2002	Sheet 19 of 46

CardBus Controller
OZ6933B (uBGA)



Compal Electronics, Ltd.			
Title: CardBus Controller<OZ6933>			
Size: Custom	Document Number: LA-1641	Rev: 0.3	
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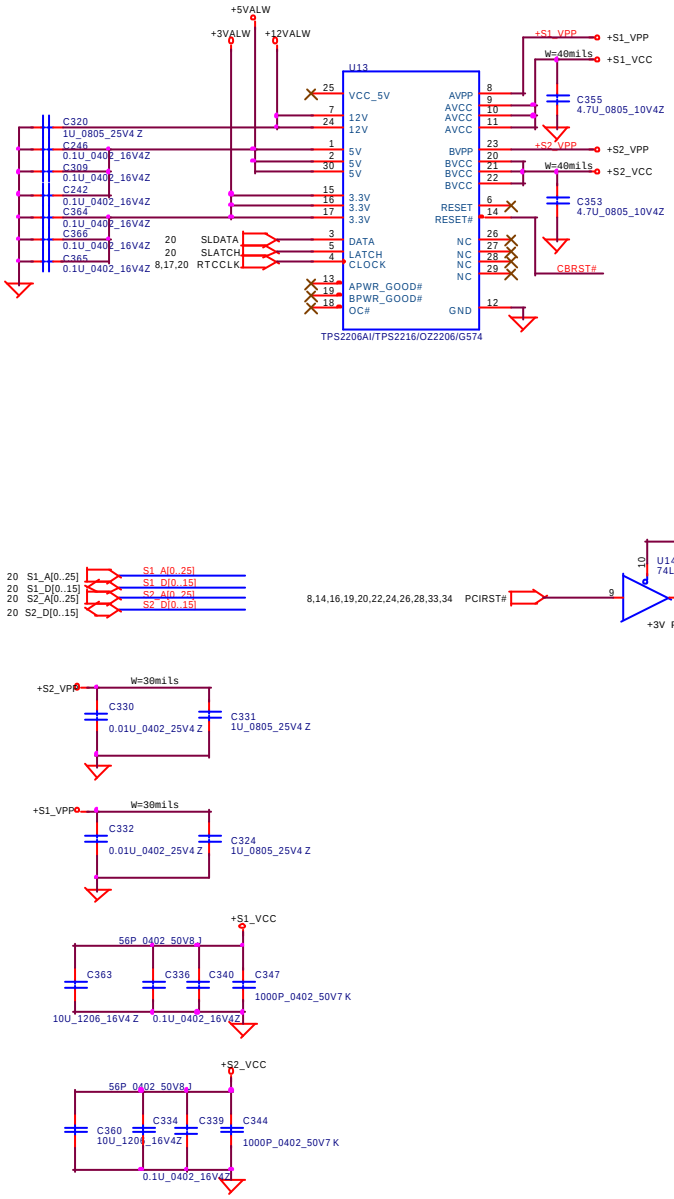
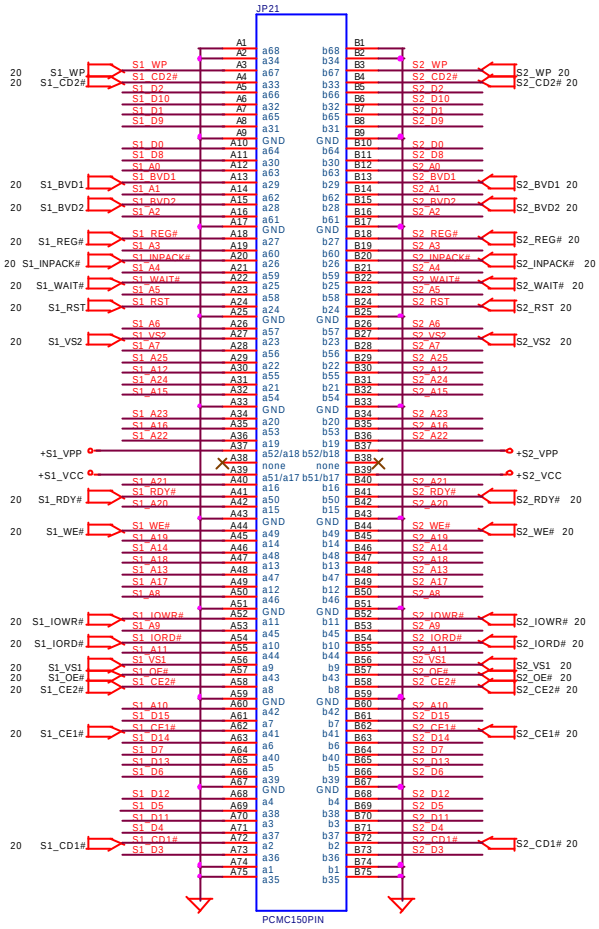
PCMCIA POWER CTRL.



CARDBUS SOCKET



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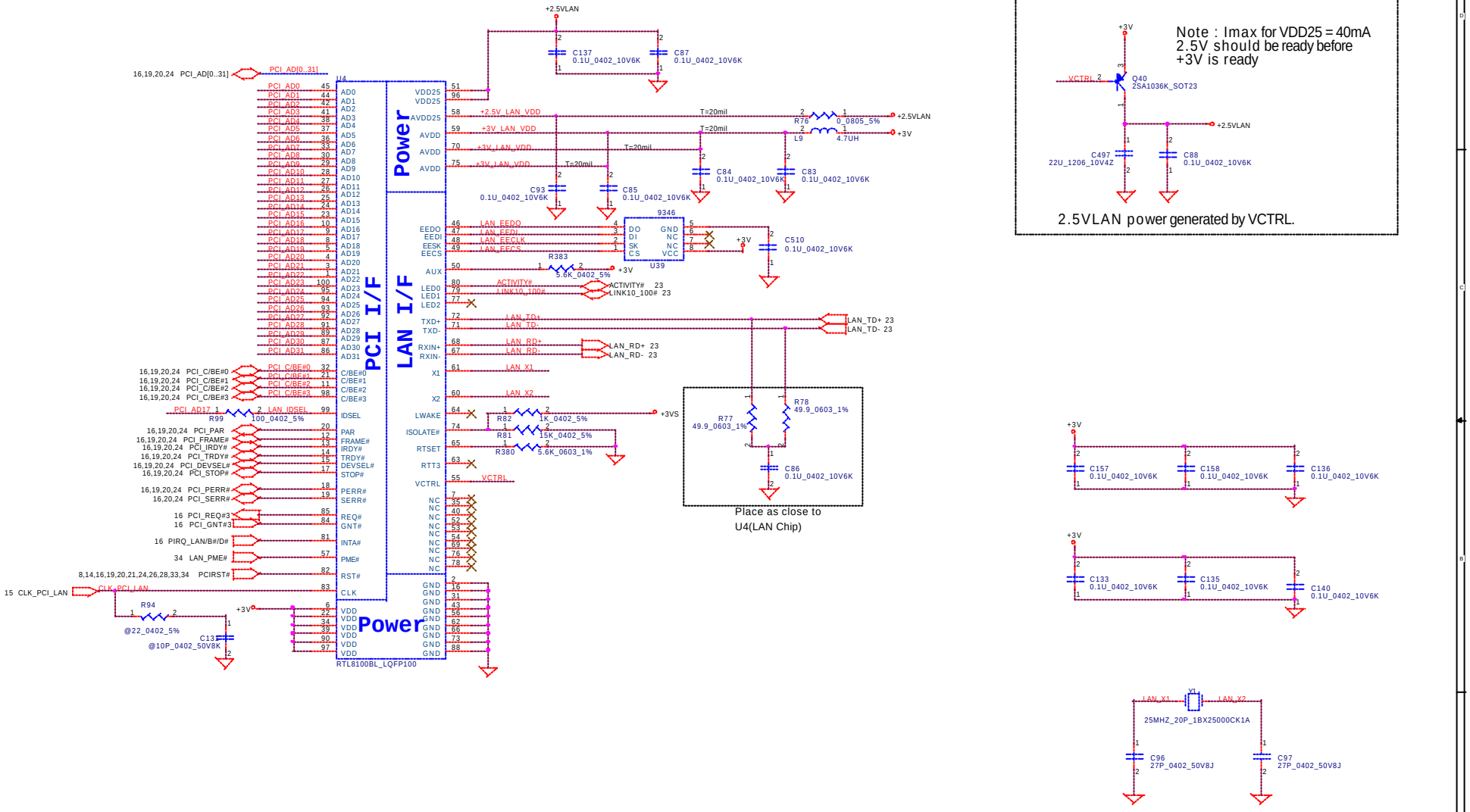
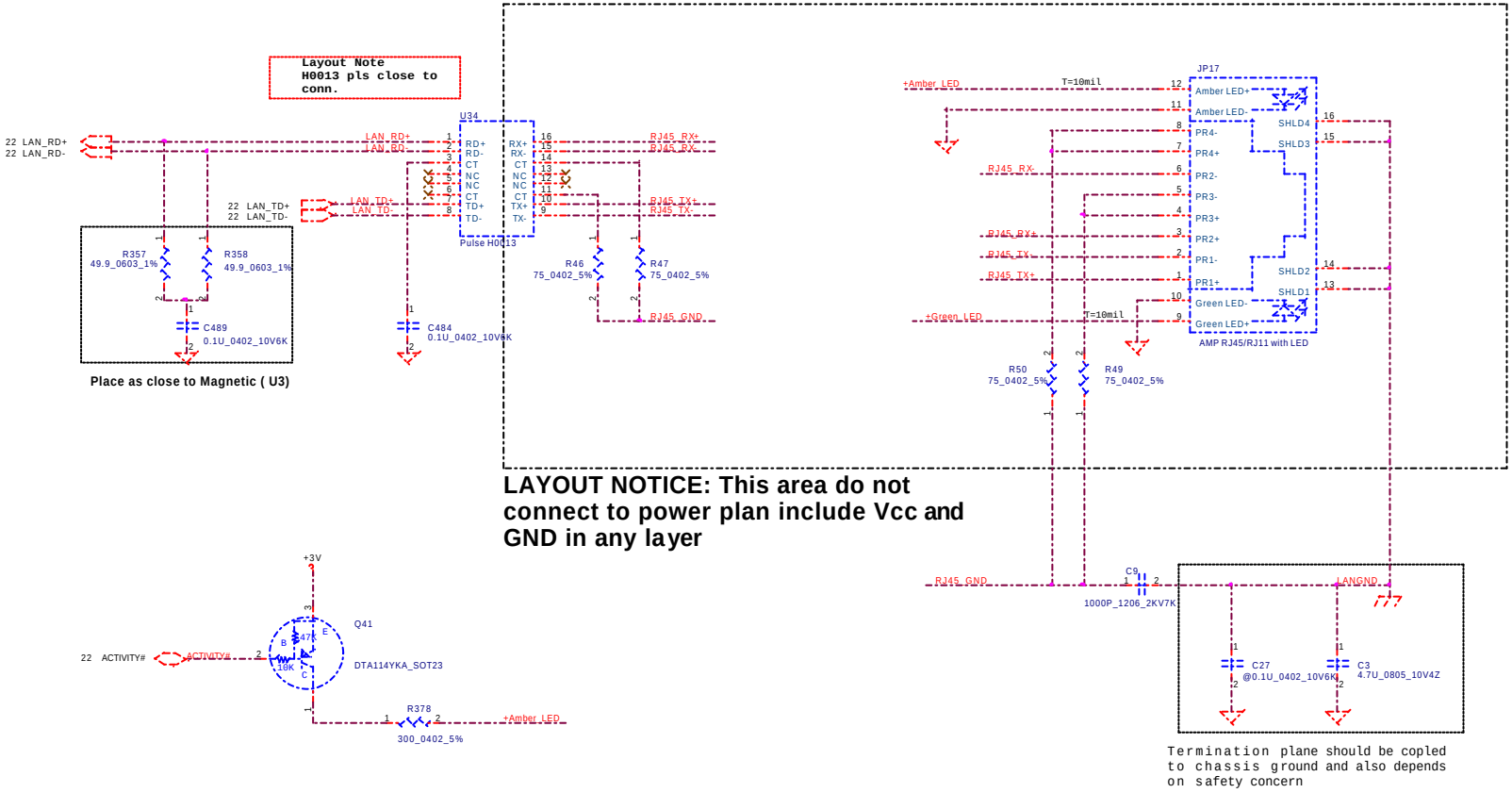
Compal Electronics, Ltd.

Title	FOXCONN PCMCIA SOCKET	
Size: Custom	Document Number: LA-1641	Rev: 0.3
Date: Thursday, November 28, 2002	Sheet 21 of 46	


PCI I/F
LAN I/F
Power
Power
U4
RTL8100BL_LQFP100
U39
9346
PCI_AD[0..31]
+2.5VLAN
+3V
+3VS
VCTRL
LAN_EEDO
LAN_EEDI
LAN_EECLK
LAN_EECS
LAN_X1
LAN_X2
LAN_TD+
LAN_TD-
LAN_RD+
LAN_RD-
ACTIVITY#
LINK10_100#
CLK_PCI_LAN
PCIRST#
PCI_REQ#3
PCI_GNT#3
PIRQ_LAN/B#/D#
LAN_PME#
LAN_IDSEL
Place as close to
U4(LAN Chip)
2.5VLAN power generated by VCTRL.
Note : Imax for VDD25 = 40mA
2.5V should be ready before
+3V is ready
1.Q40 pin2 close to U4 pin55
2.C497 and C88 close to Q40 pin1
25MHZ_20P_1BX25000CK1A
Compal Electronics, Ltd.
LAN-Realtek RTL8100BL
LA-1641
Thursday, November 28, 2002

Keep Out 40mil



LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer

[redacted]

Compal Electronics, Ltd.		
Title: RJ11/RJ45 Connector		
Size: Custom	Document Number: LA-1641	Rev: 0.3
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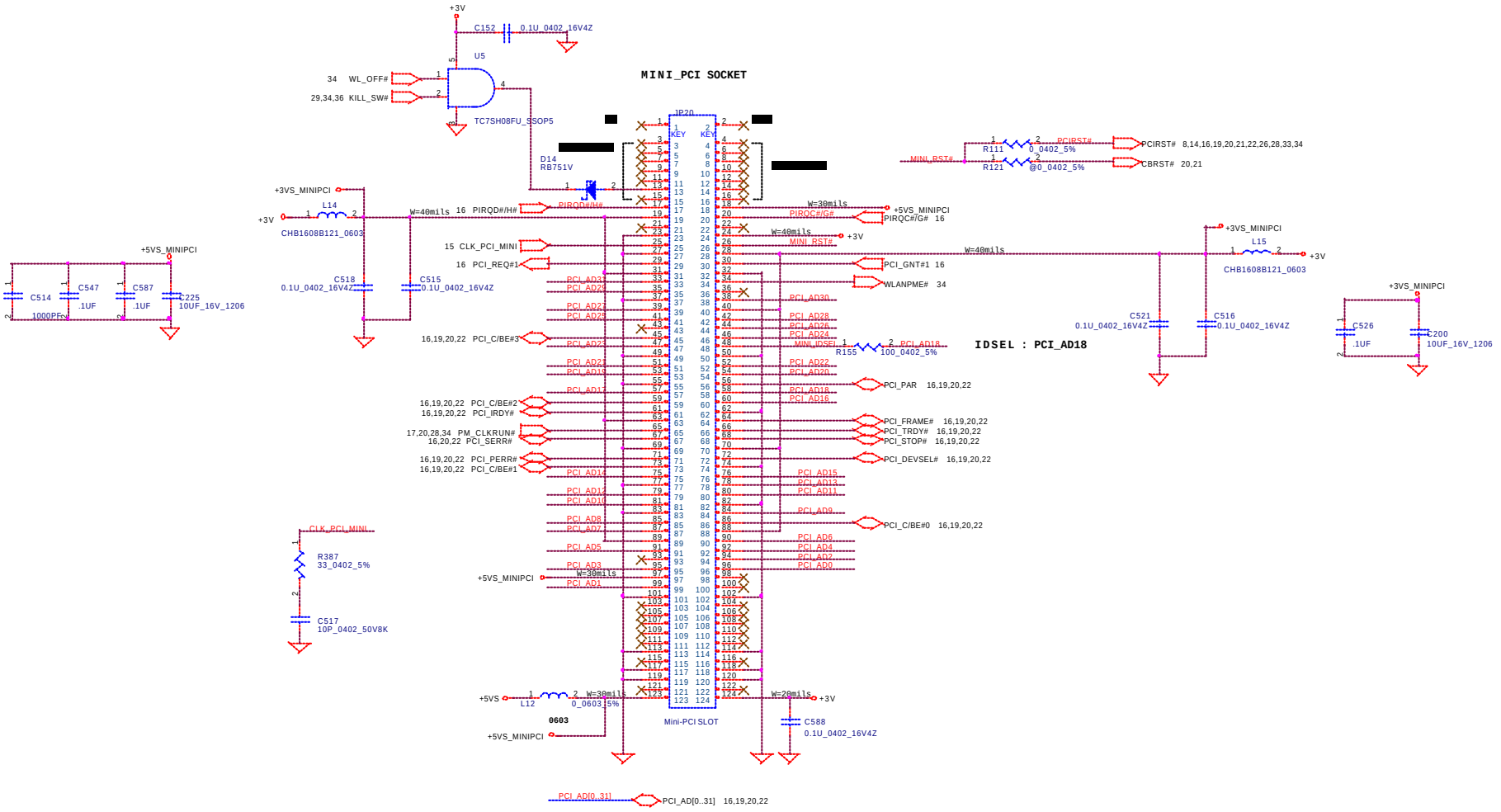

Compal Electronics, Ltd.

Title: Mini PCI Slot

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Custom	LA-1641	0.3

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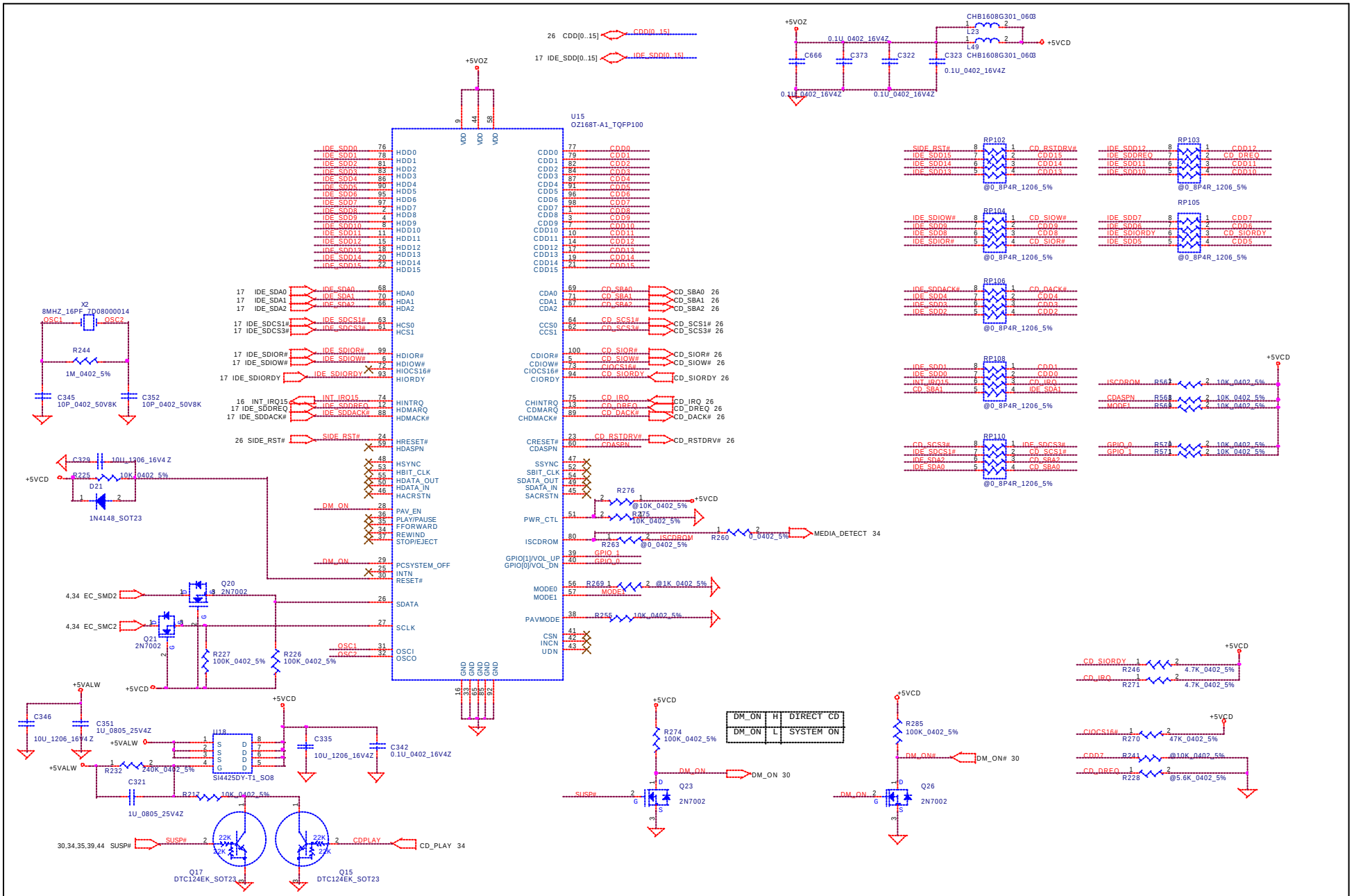
U15
OZ168T-A1_TQFP100
+5VOZ
+5VCD
+5VALW
X2
8MHZ_16PF_7D08000014
R244
1M_0402_5%
C345
10P_0402_50V8K
C352
10P_0402_50V8K
C329
10U_1206_16V4 Z
R225
10K_0402_5%
D21
1N4148_SOT23
Q20
2N7002
Q21
2N7002
R227
100K_0402_5%
R226
100K_0402_5%
C346
10U_1206_16V4 Z
C351
1U_0805_25V4Z
U18
SI4425DY-T1_SO8
R232
240K_0402_5%
C321
1U_0805_25V4Z
R217
10K_0402_5%
C335
10U_1206_16V4Z
C342
0.1U_0402_16V4Z
Q17
DTC124EK_SOT23
Q15
DTC124EK_SOT23
SUSP#
CDPLAY
CD_PLAY 34
R276
@10K_0402_5%
R275
10K_0402_5%
R263
@0_0402_5%
R260
0_0402_5%
MEDIA_DETECT 34
R269
@1K_0402_5%
R255
10K_0402_5%
R274
100K_0402_5%
Q23
2N7002
R285
100K_0402_5%
Q26
2N7002
DM_ON 30
DM_ON# 30
DM_ON | H | DIRECT CD
DM_ON | L | SYSTEM ON
CHB1608G301_0603
L23
L49
C666
C373
C322
C323
0.1U_0402_16V4Z
RP102
RP103
RP104
RP105
RP106
RP108
RP110
@0_8P4R_1206_5%
R246
4.7K_0402_5%
R271
4.7K_0402_5%
R270
47K_0402_5%
R241
@10K_0402_5%
R228
@5.6K_0402_5%
R562
R563
R569
R571
10K_0402_5%
Compal Electronics, Inc
OZ-168 CD_PLAY
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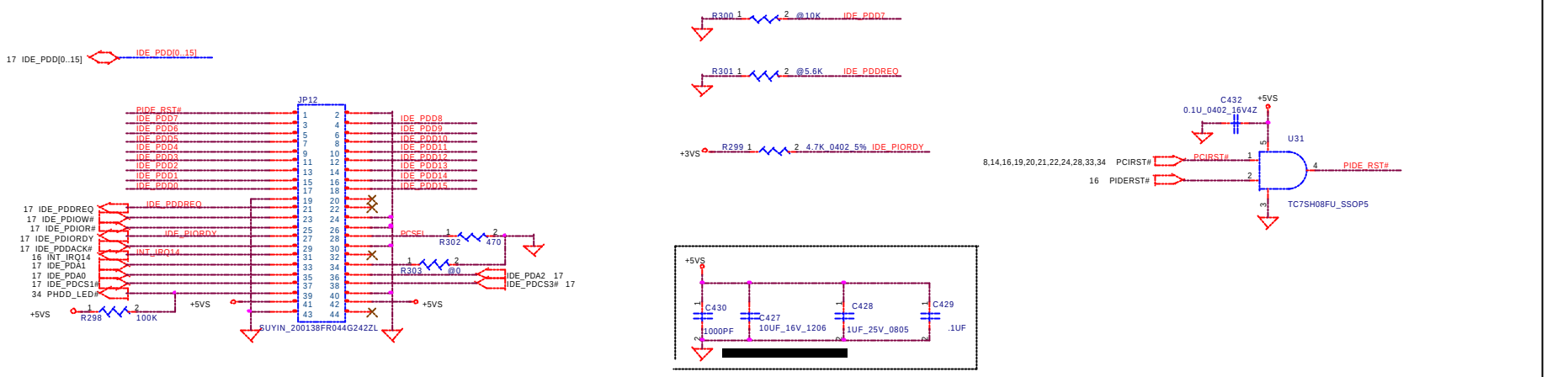
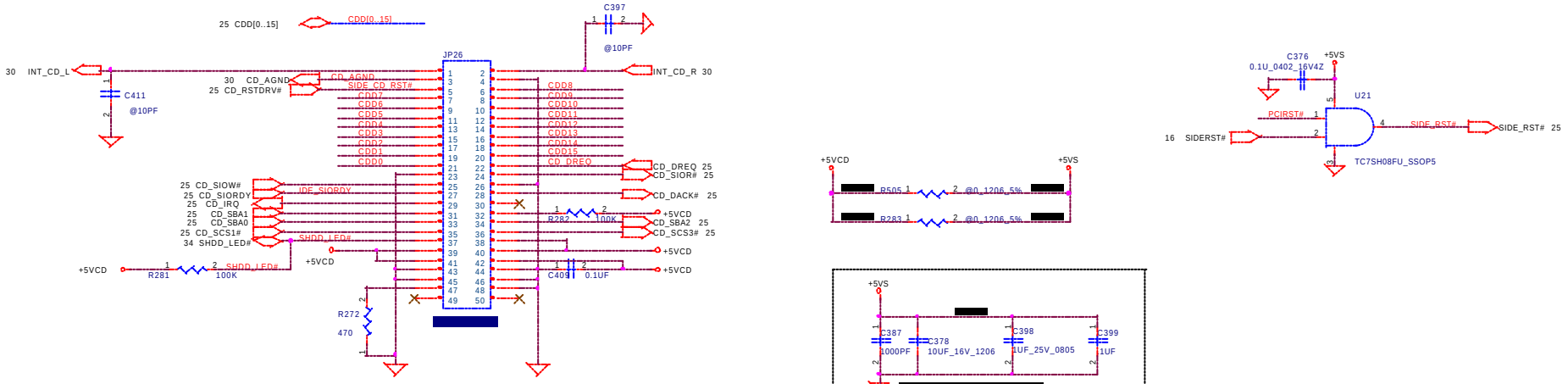
46

IDE Module CONN.



CD-ROM Module CONN.



[redacted]

Compal Electronics, Ltd.

Title	IDE & CD-ROM Connector	
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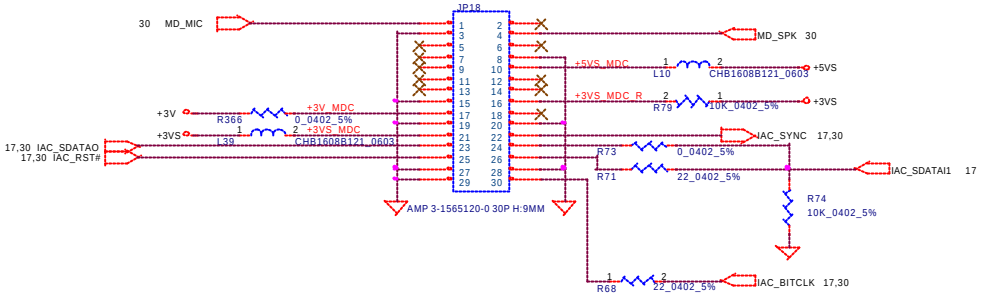
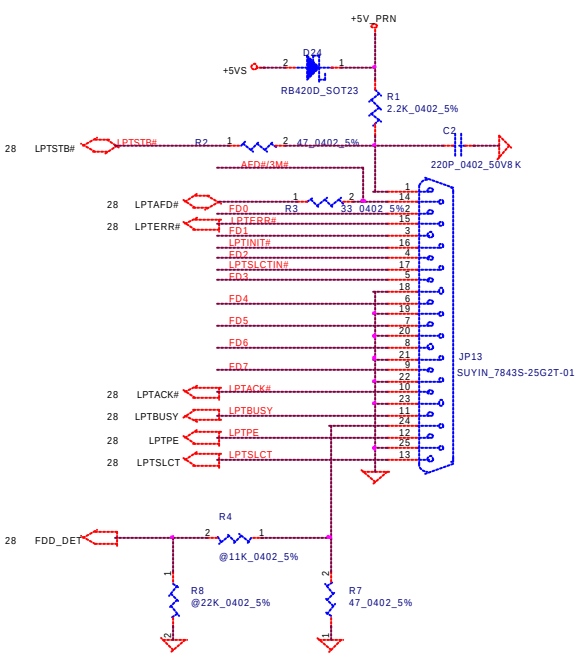
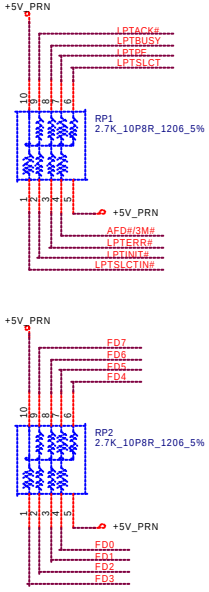
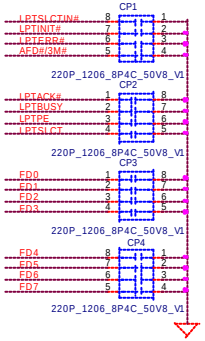
MDC Connector

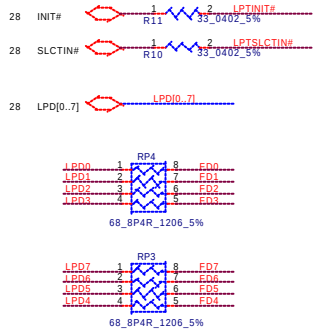


Parallel Port









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Compal Electronics, Ltd.

Title	Parallel & MDC	
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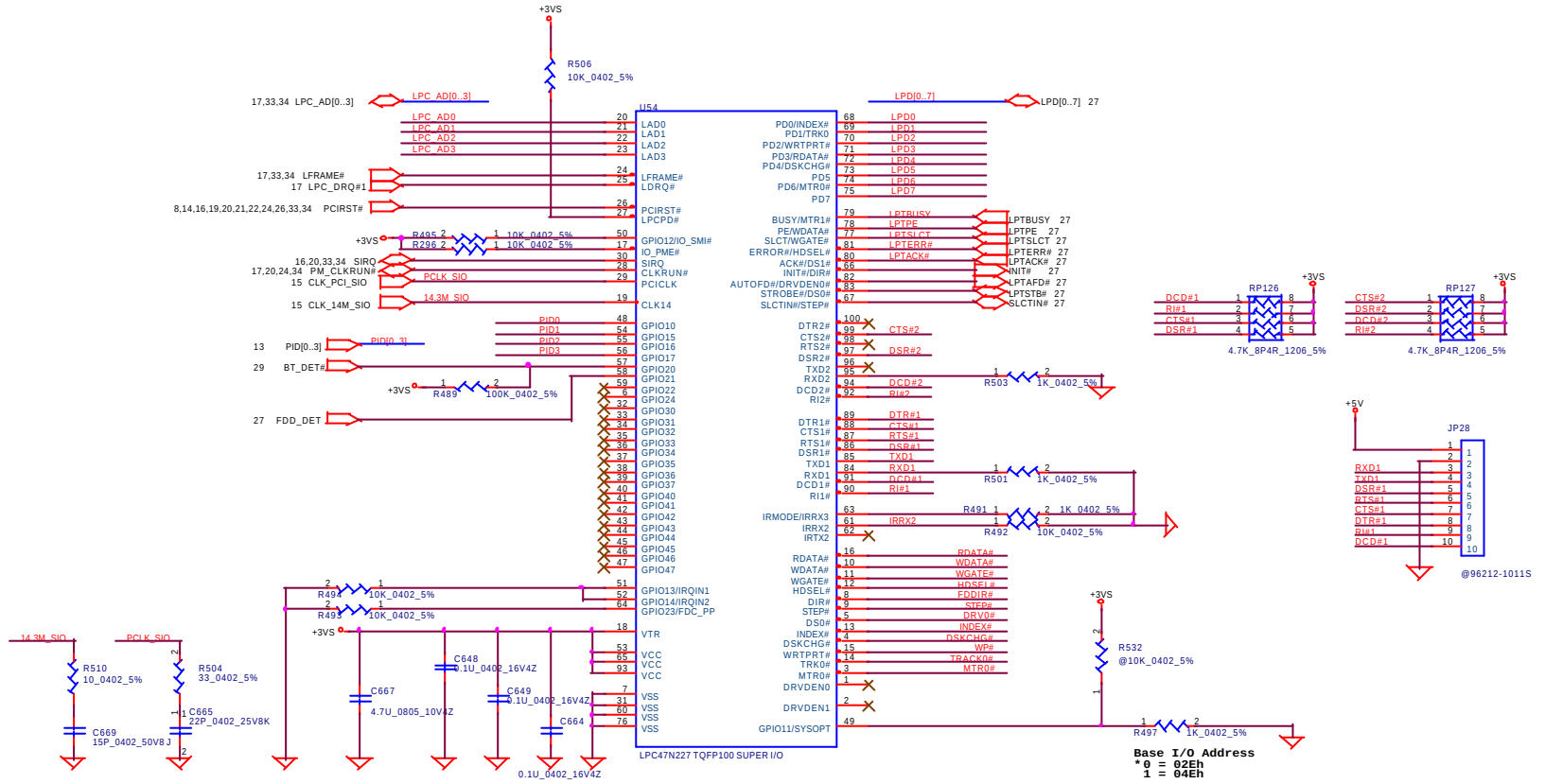
SUPER I/O SMsC FDC47N227



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Compal Electronics, Ltd.			
Title: LPC-Super I/O			
Size: Custom	Document Number: LA-1641	Rev: 0.3	
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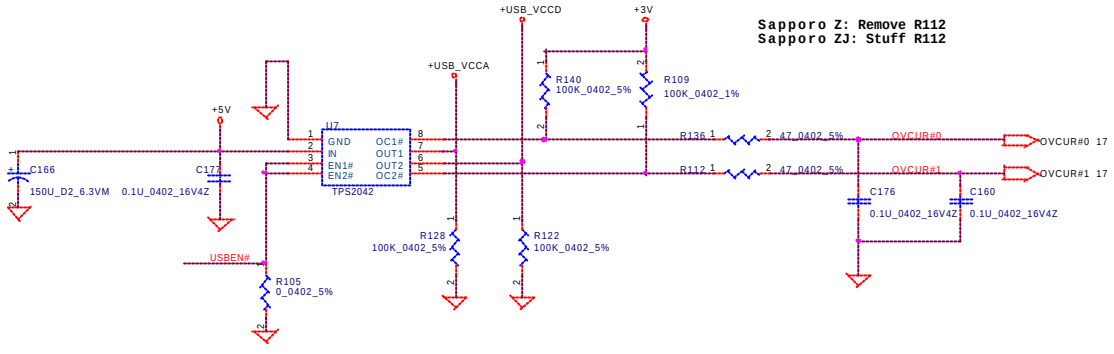
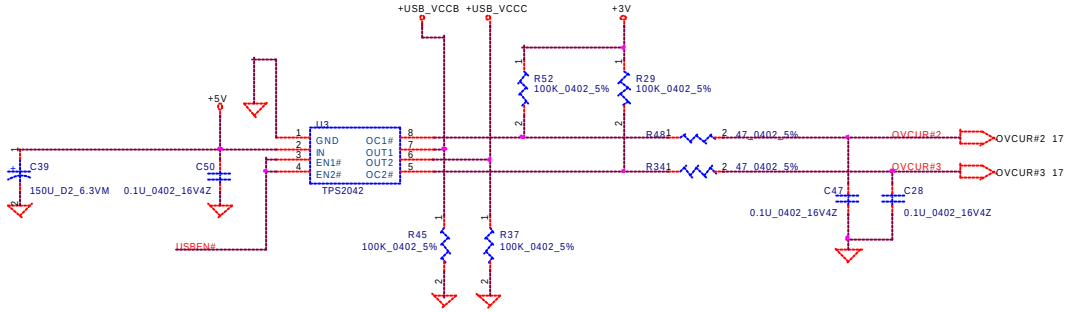
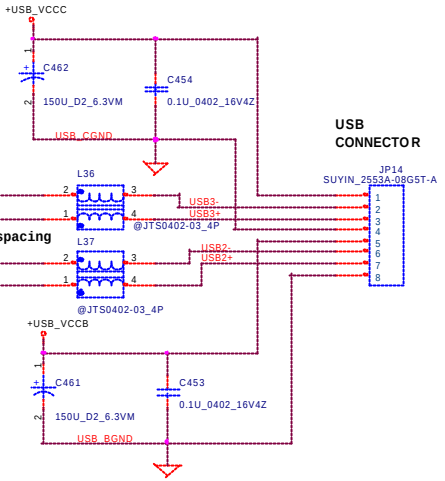
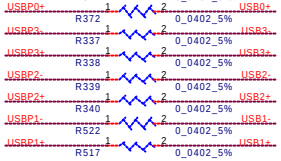
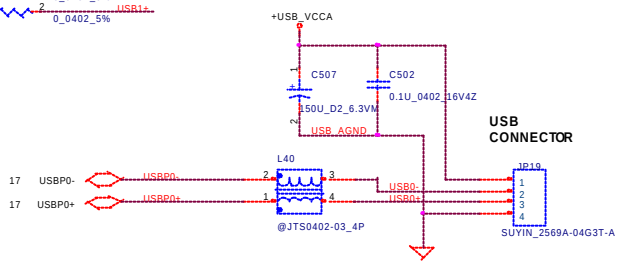


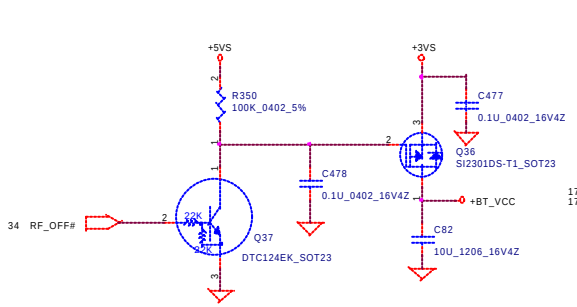


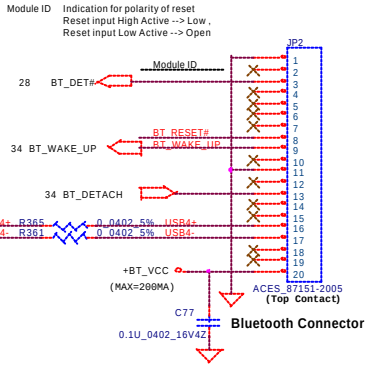


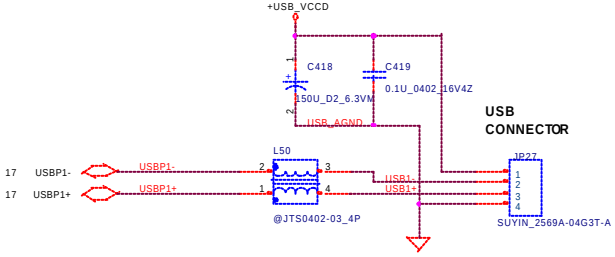


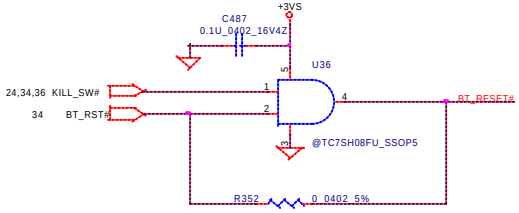


BlueTooth Interface









[redacted]

Compal Electronics, Ltd.

Title: USB & Bluetooth

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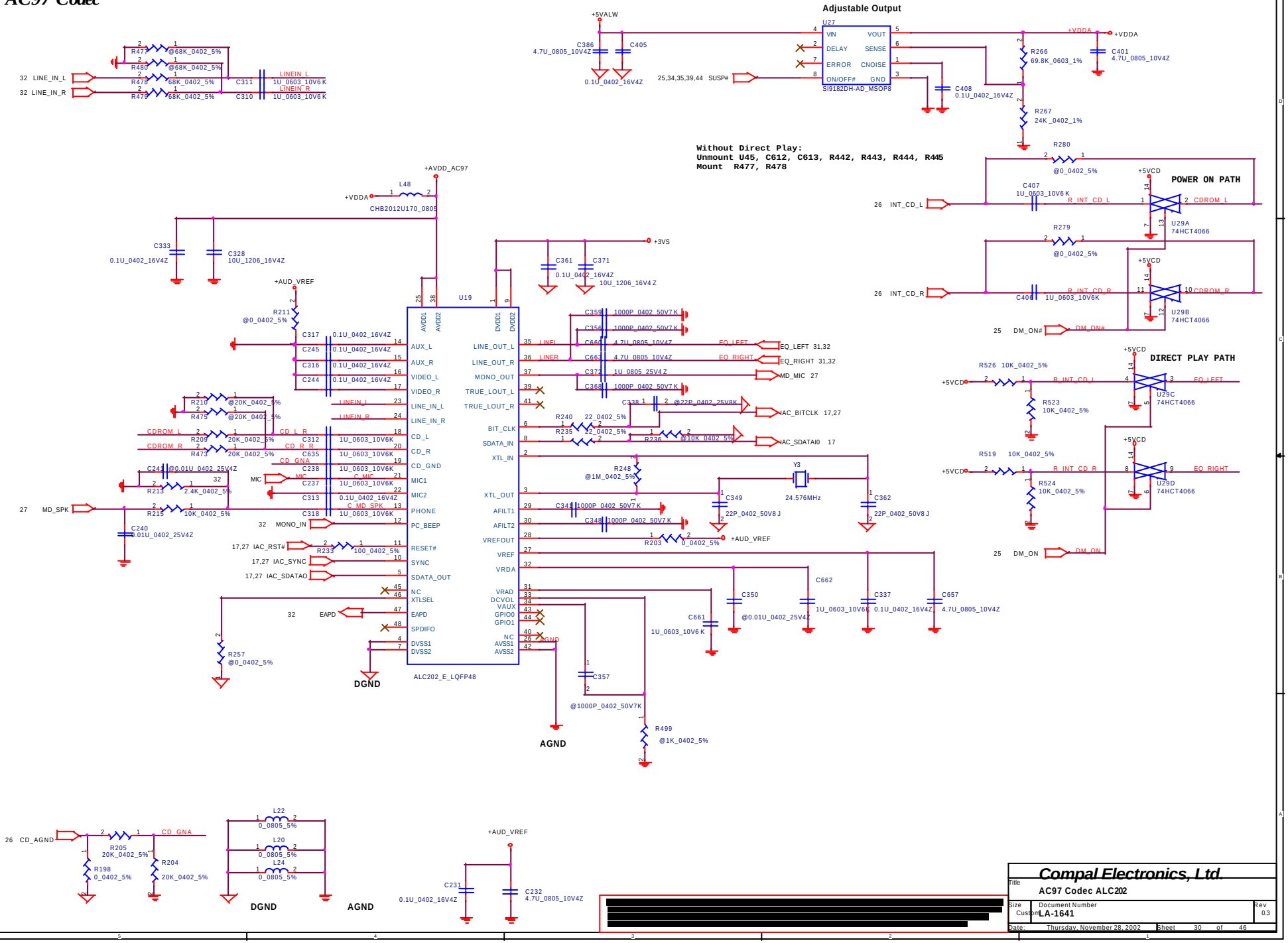
AC97 Codec


Adjustable Output
U27
SI9182DH-AD_MSOP8
Without Direct Play:
Unmount U45, C612, C613, R442, R443, R444, R445
Mount R477, R478
POWER ON PATH
DIRECT PLAY PATH
U19
ALC202_E_LQFP48
DGND
AGND
+AVDD_AC97
+AUD_VREF
+3VS
+5VALW
+VDDA
+5VCD
CHB2012U170_0805
Y3
24.576MHz
LINEIN_L
LINEIN_R
CD_L_R
CD_R_R
CD_GNA
C_MD_SPK
C_MIC
EQ_LEFT
EQ_RIGHT
R_INT_CD_L
R_INT_CD_R
DM_ON
DM_ON#
IAC_BITCLK
IAC_SDATAI0
MD_MIC
MONO_IN
IAC_RST#
IAC_SYNC
IAC_SDATAO
EAPD
SUSP#
CD_AGND
U29A
U29B
U29C
U29D
74HCT4066
Compal Electronics, Ltd.
AC97 Codec ALC202
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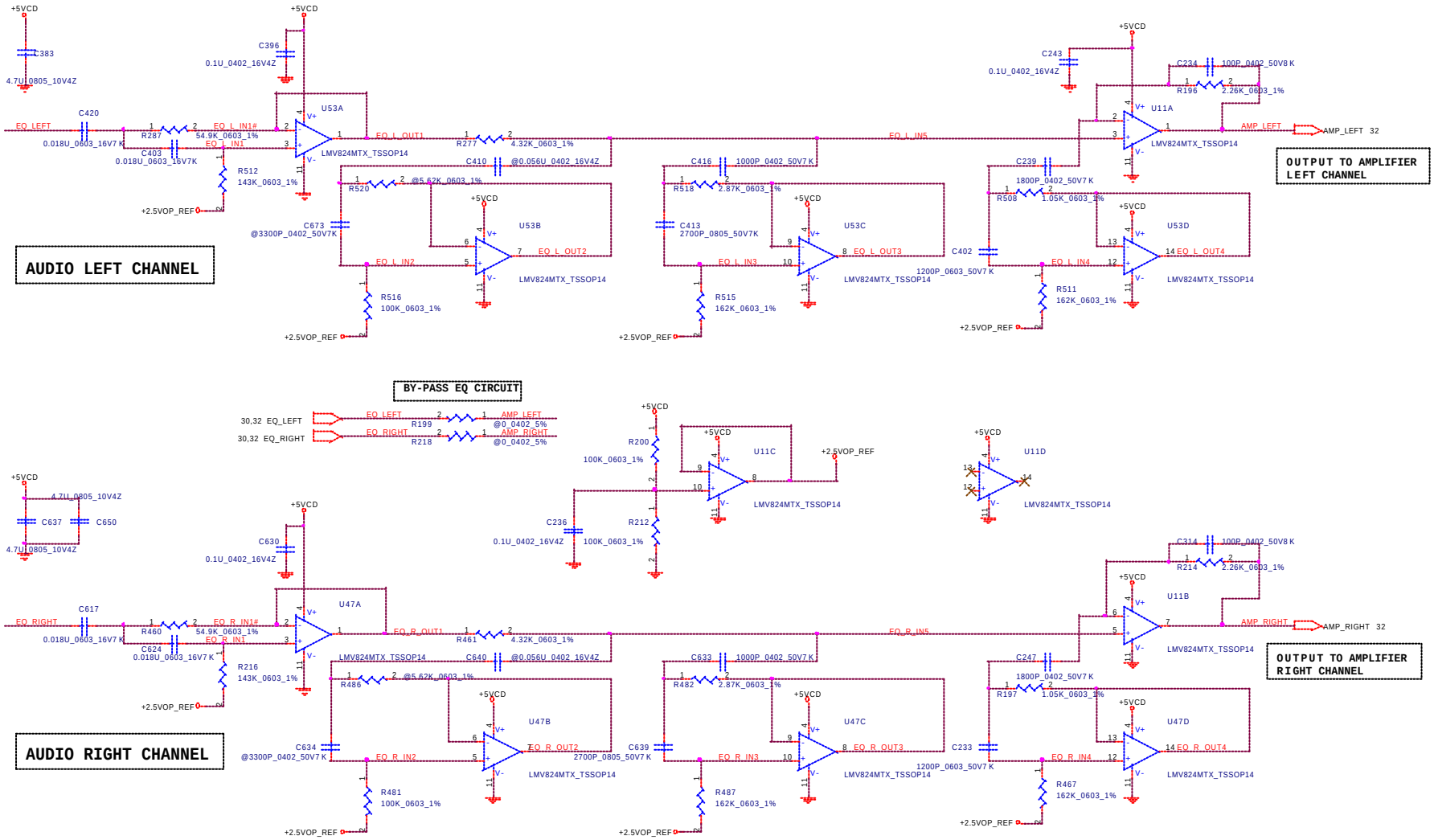

[redacted]

Compal Electronics, Ltd.

Title	H/W EQ	
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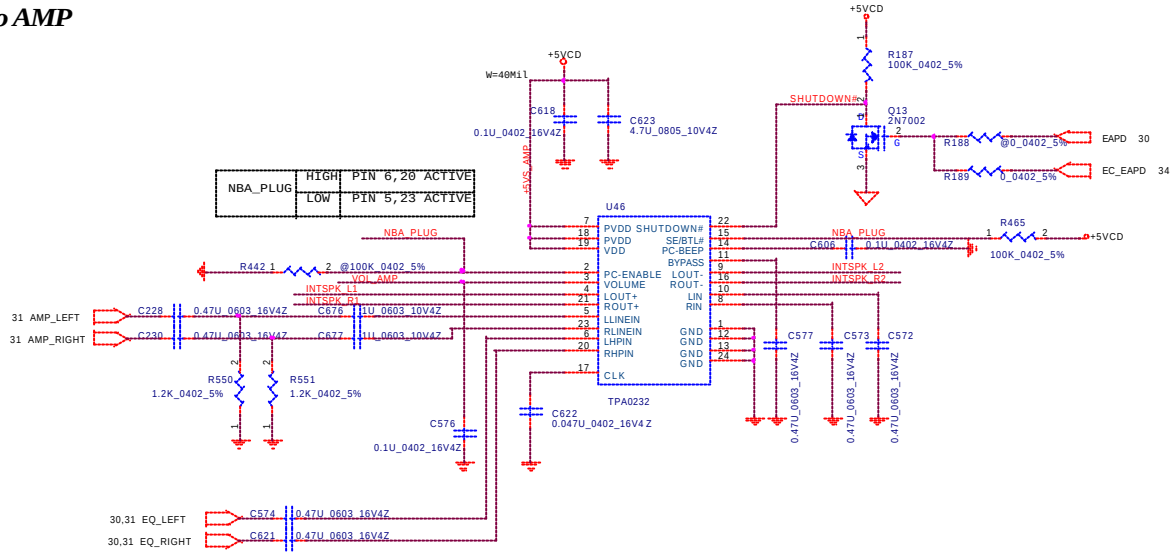
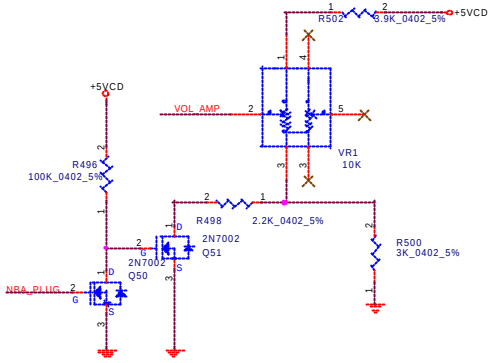
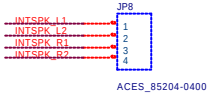
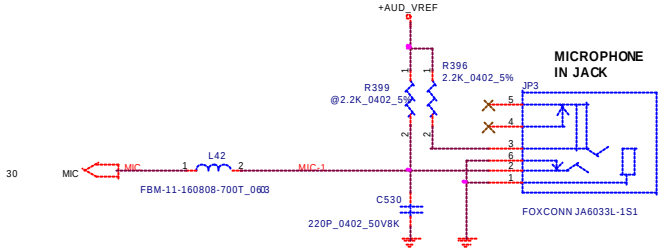
Audio AMP



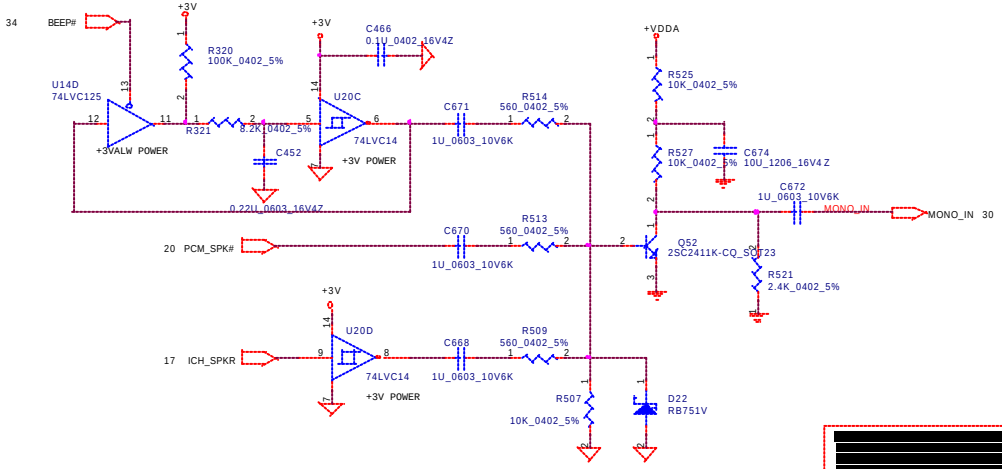


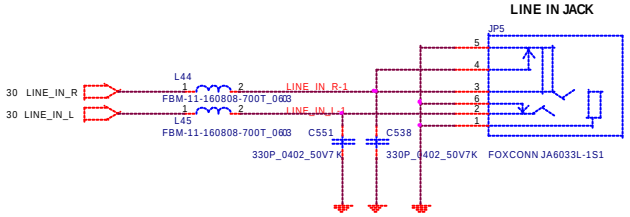
Speaker Connector

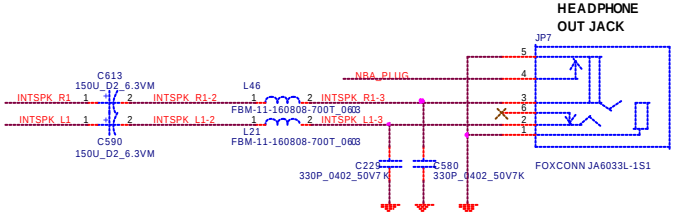




System Sound







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Compal Electronics, Ltd.

Title	Audio AMP & JACK	
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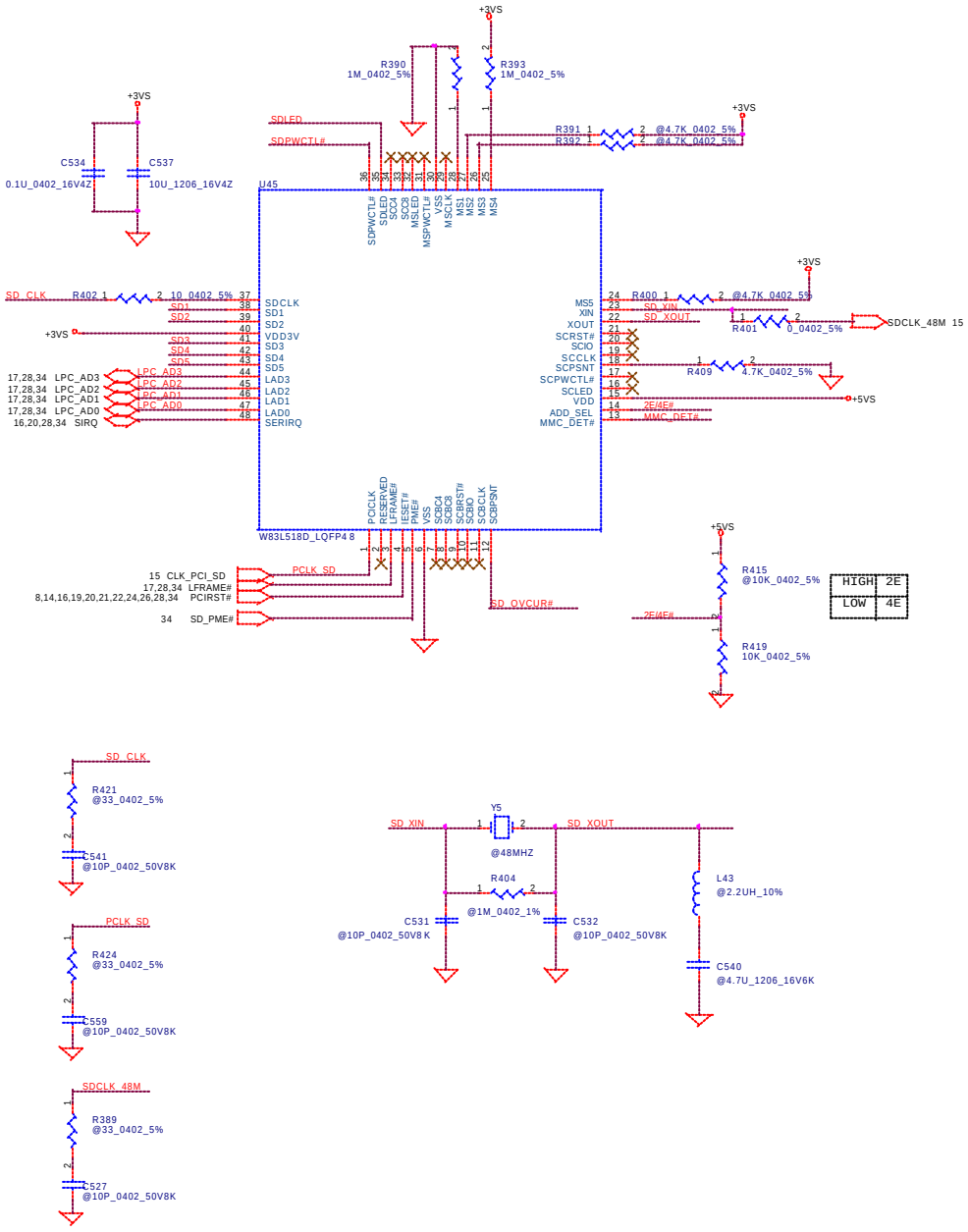
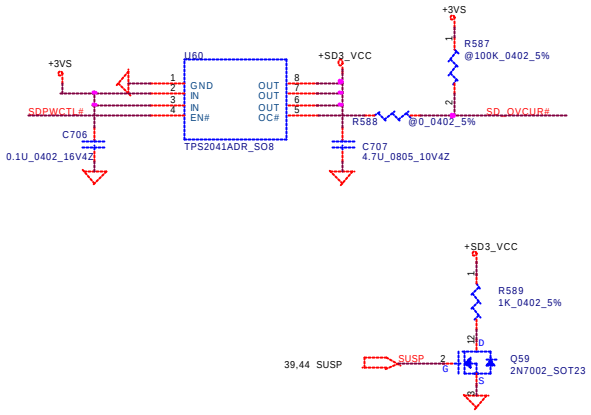
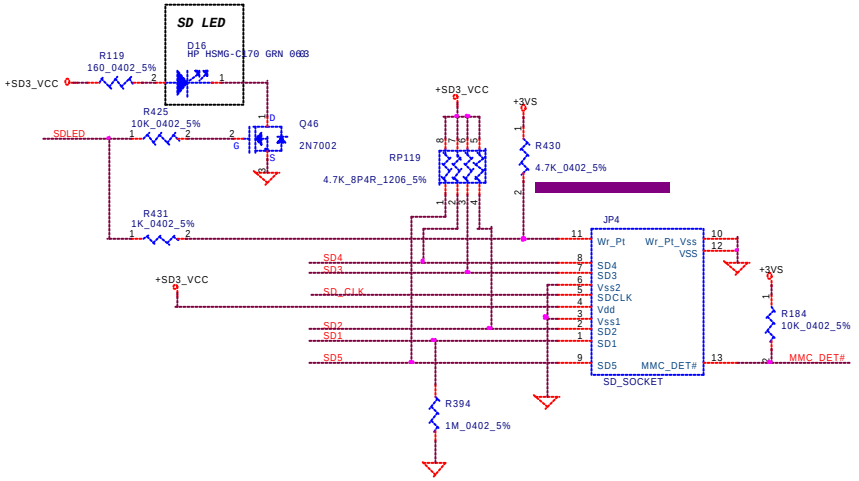
SD Card Reader



SD Power Switch



SD SOCKET



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Compal Electronics, Ltd.		
Title: SD Controller W83L518D		
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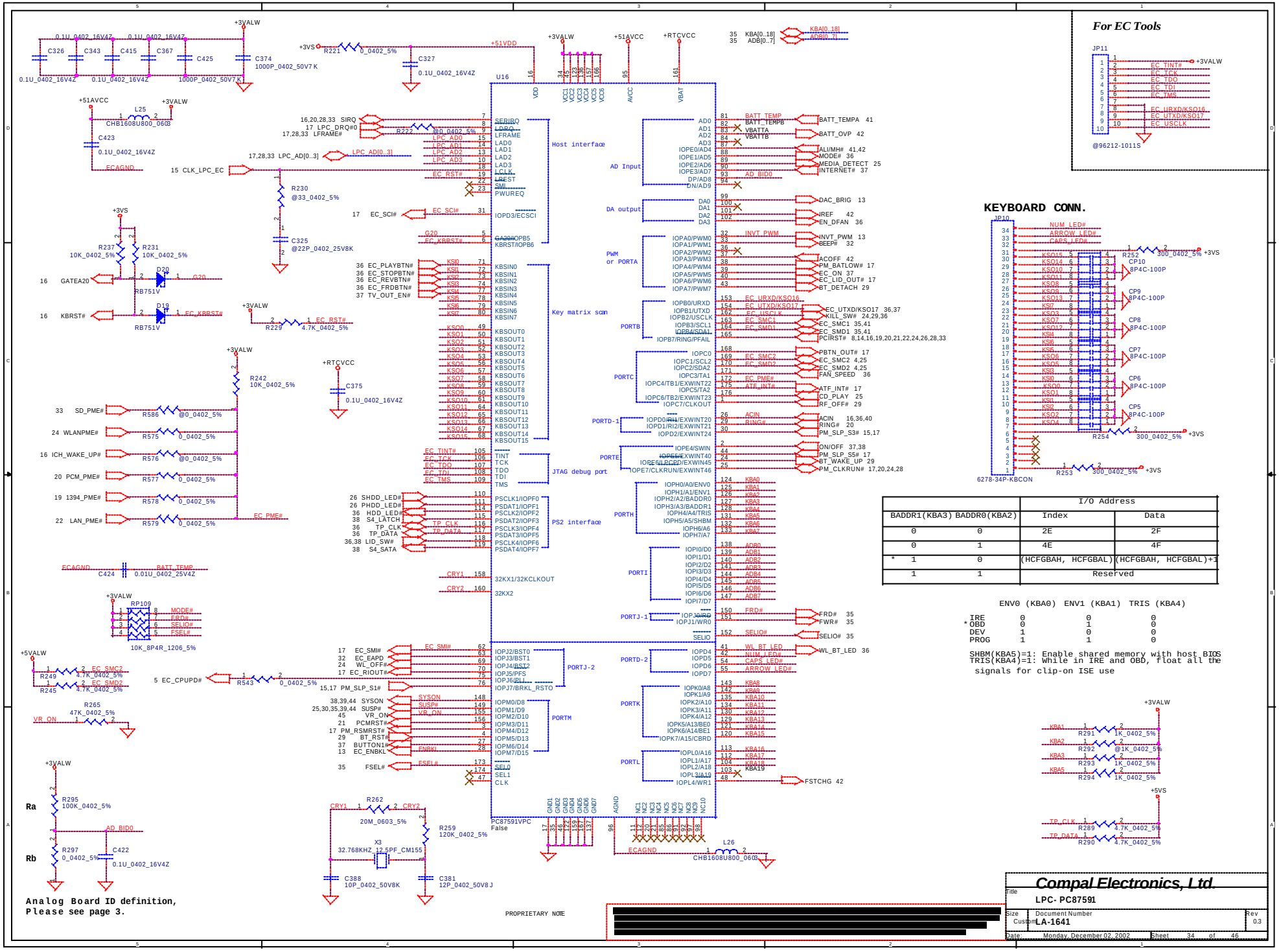
For EC Tools
JP11
EC_TINT#
EC_TCK
EC_TDO
EC_TDI
EC_TMS
EC_URXD/KSO16
EC_UTXD/KSO17
EC_USCLK
@96212-1011S
KEYBOARD CONN.
JP10
6278-34P-KBCON
U16
PC87591VPC
False
Host interface
Key matrix scan
JTAG debug port
PS2 interface
AD Input
DA output
PWM or PORTA
PORTB
PORTC
PORTD-1
PORTE
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
I/O Address
BADDR1(KBA3) BADDR0(KBA2)
Index
Data
(HCFGBAH, HCFGBAL)
(HCFGBAH, HCFGBAL)+1
Reserved
ENV0 (KBA0) ENV1 (KBA1) TRIS (KBA4)
IRE 0 0 0
*OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use
Analog Board ID definition,
Please see page 3.
PROPRIETARY NOTE
[redacted]
Compal Electronics, Ltd.
Title
LPC- PC87591
Size
Custom
Document Number
LA-1641
Rev
0.3
Date: Monday, December 02, 2002
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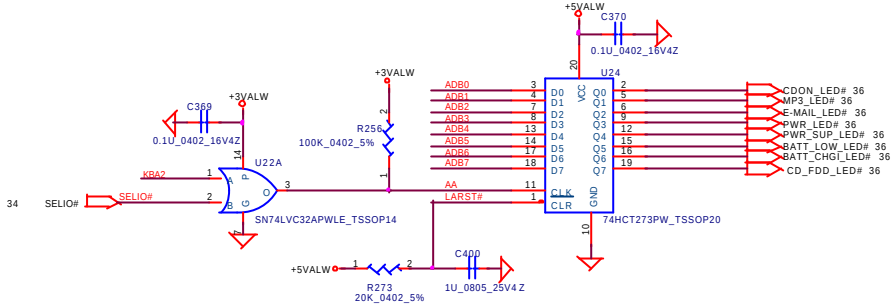
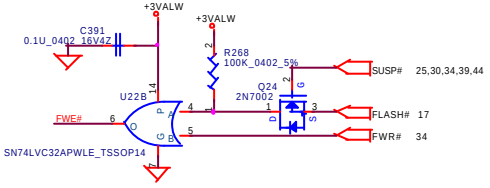
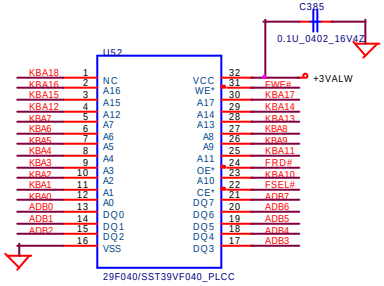
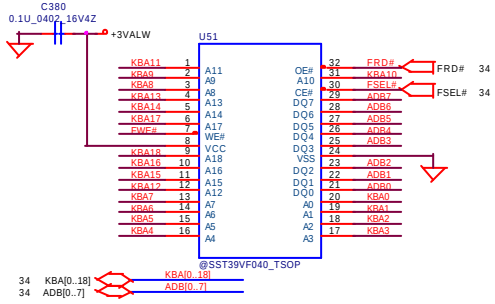
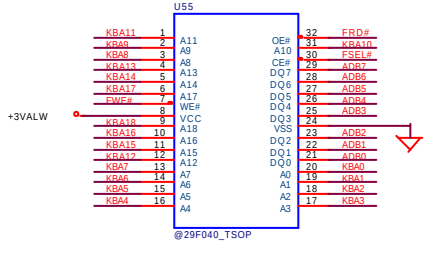


System BIOS

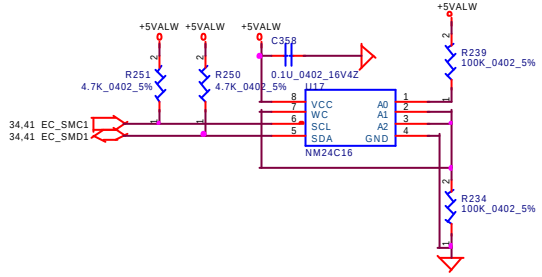








SMBus EEPROM



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Compal Electronics, Ltd.

Title: BIOS & Ext.I/O

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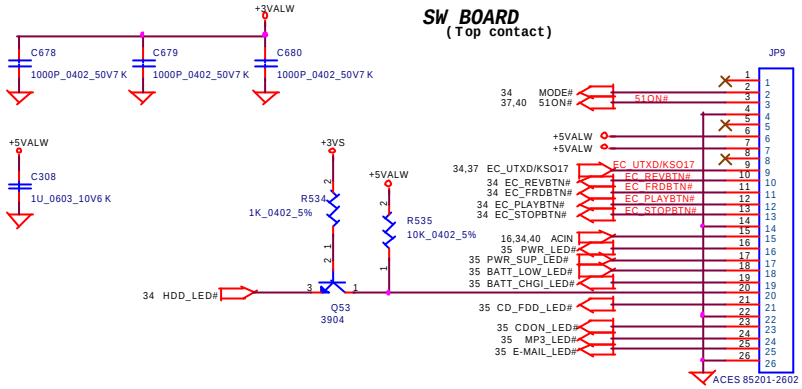
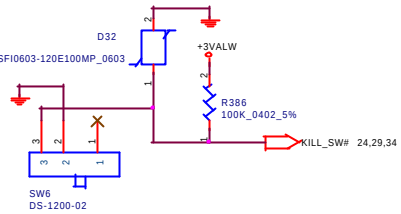
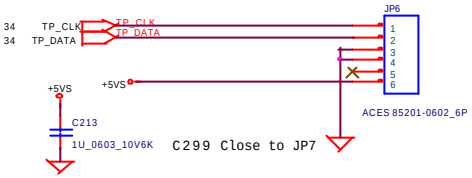
SW BOARD
(Top contact)



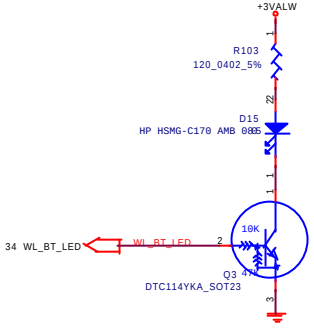
Kill SWITCH



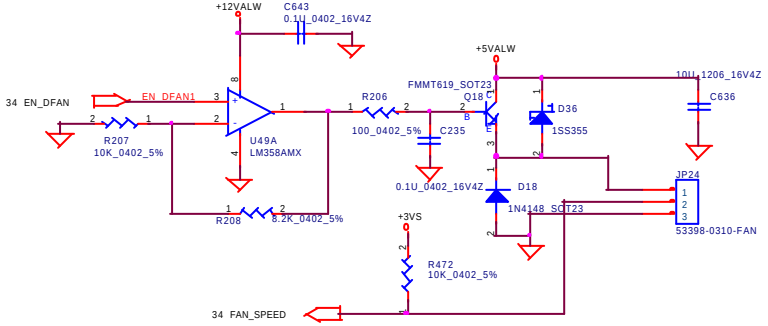
Touch Pad Connector



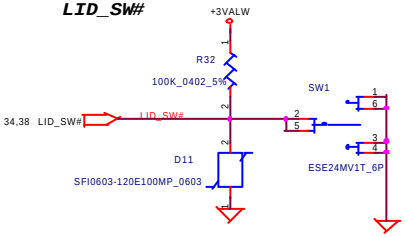
WIRELESS ACTIVE AMB LED



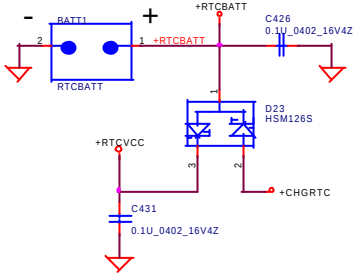
FAN CONN



LID_SW#



RTC BATT



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Compal Electronics, Ltd.

Title: System Connectors		
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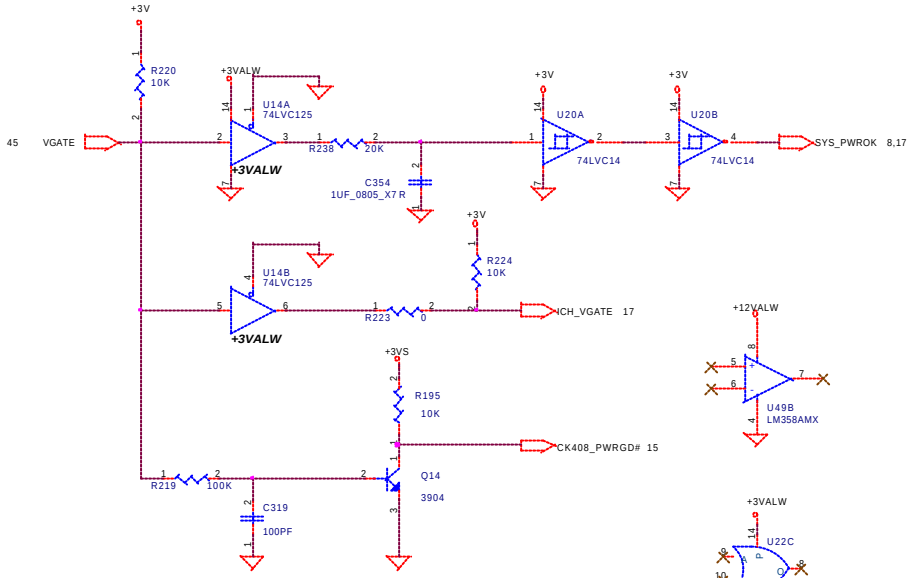
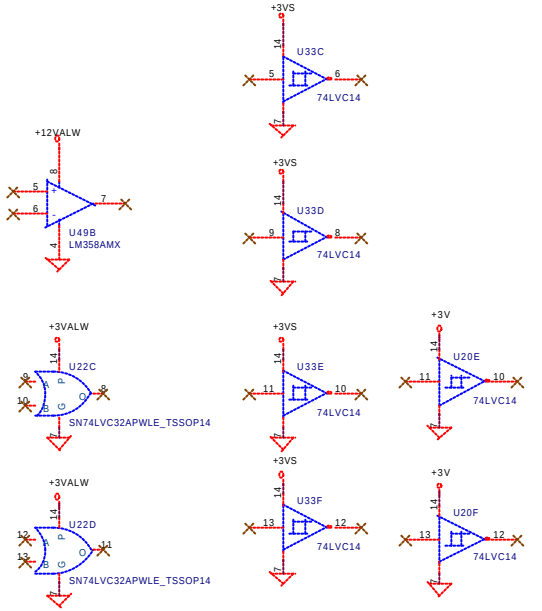
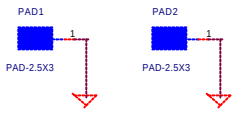
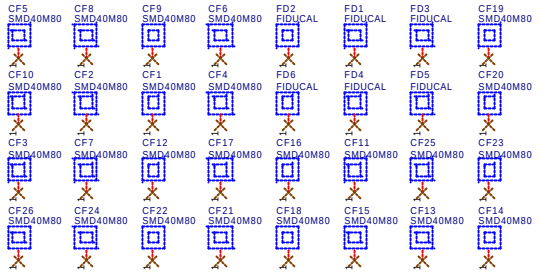
Power Good Circuit

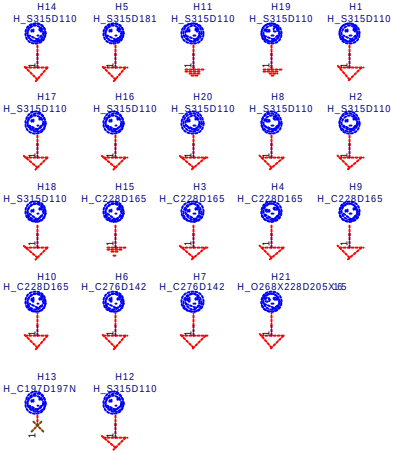




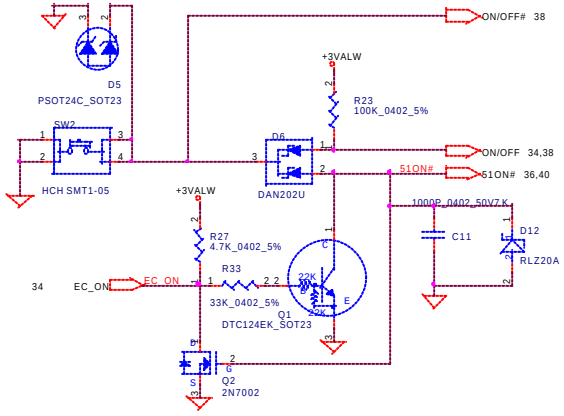
EMI Clip PAD for CPU



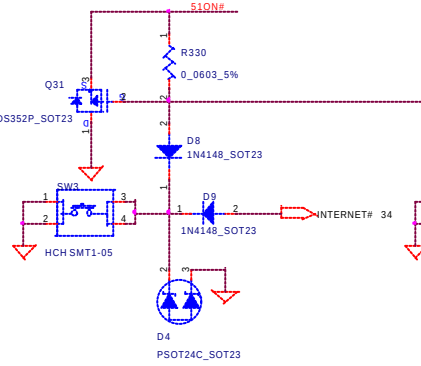




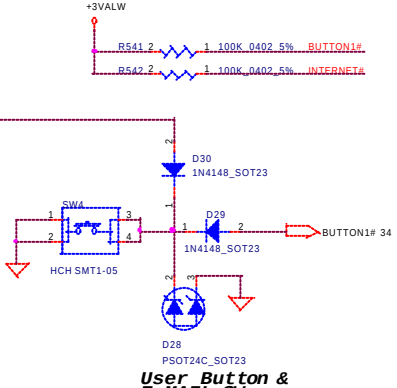
Power Button



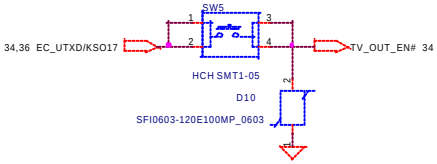
Internet Button



User Button & E-MAIL SW



TV-OUT BUTTON



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Compal Electronics, Ltd.

Title	PowerGood	
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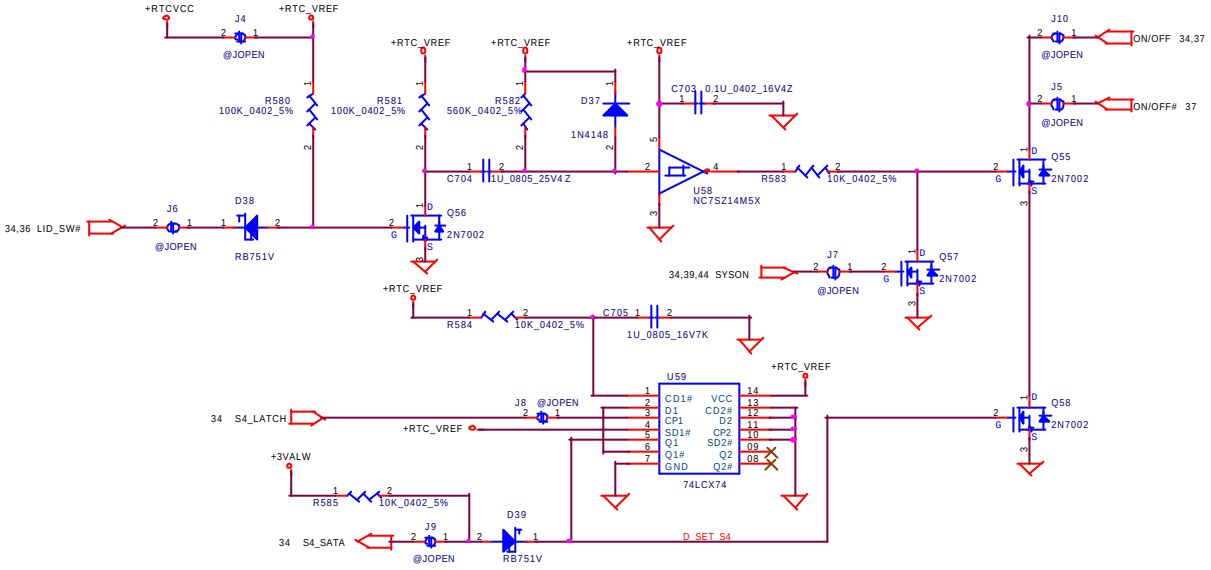

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Compal Electronics, Ltd.

Title: RESET		
Size: Custom	Document Number: LA-1641	Rev: 0.3
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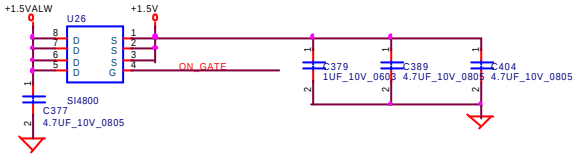
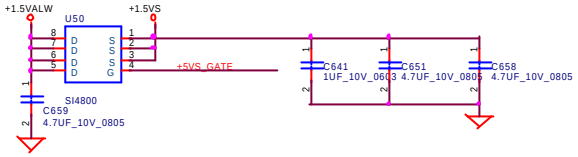
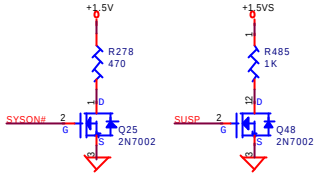
+1.5VALW To +1.5V Transfer



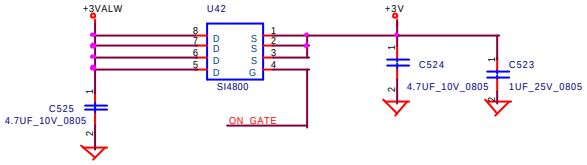
+1.5VALW To +1.5VS Transfer



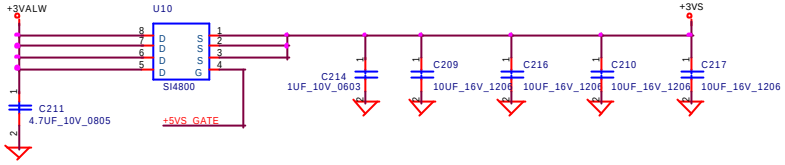
+1.5V & +1.5VS Discharge



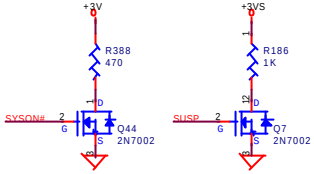
+3VALW To +3V Transfer



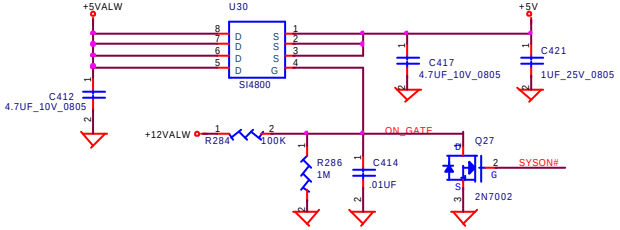
+3VALW To +3VS Transfer



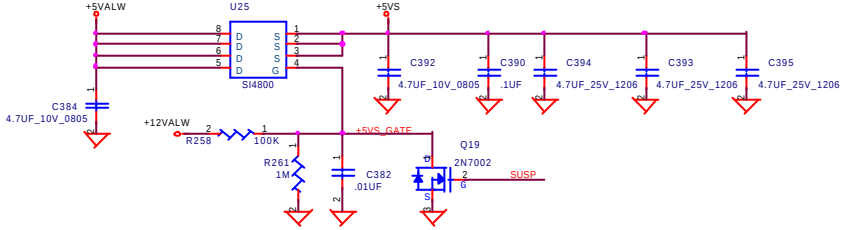
+3V & +3VS Discharge



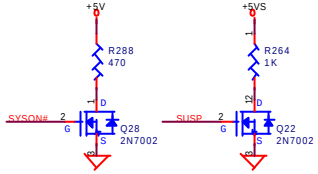
+5VALW To +5V Transfer



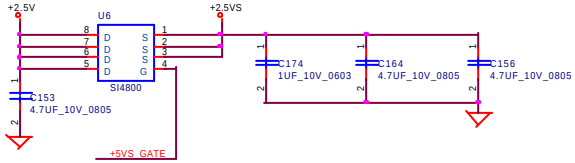
+5VALW To +5VS Transfer

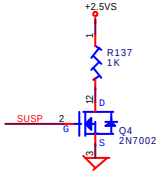


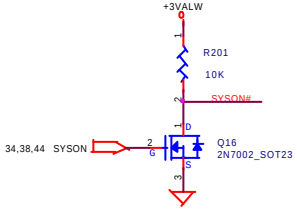
+5V & +5VS Discharge

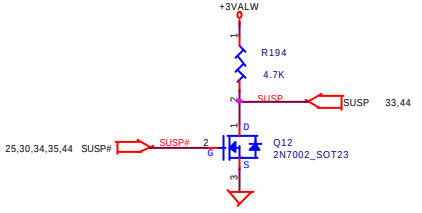


+2.5V To +2.5VS Transfer









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Compal Electronics, Ltd.

Title	DC/DC Interface	
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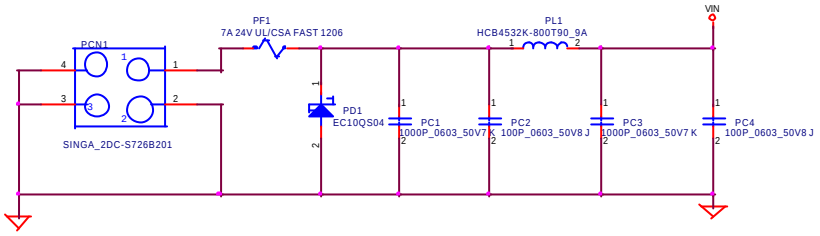
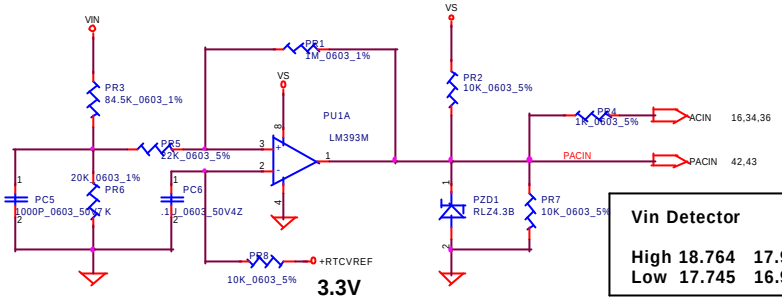
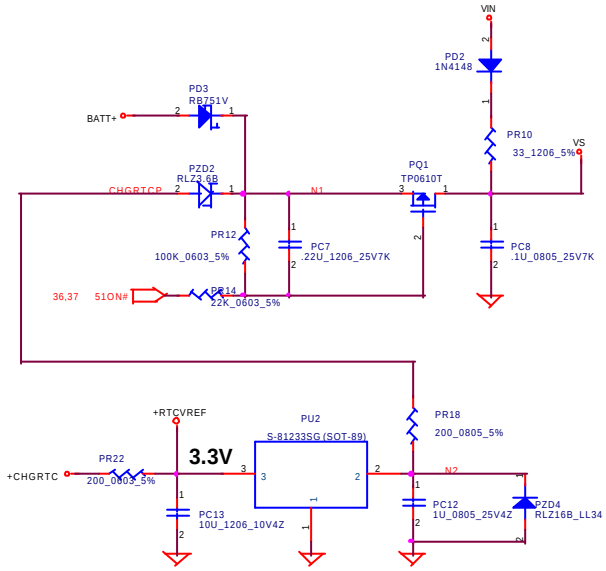
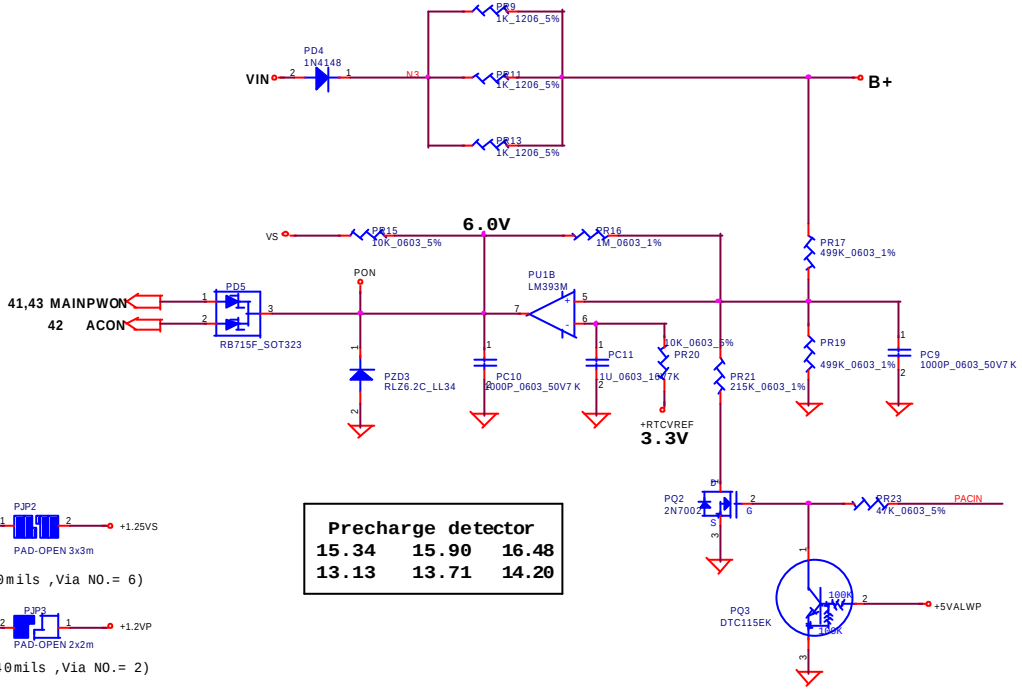


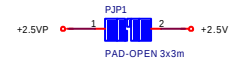


Vin Detector			
High	18.764	17.901	17.063
Low	17.745	16.903	16.038



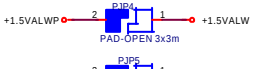


Precharge detector			
15.34	15.90	16.48
13.13	13.71	14.20



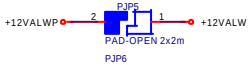
(6A,240mils ,Via NO.= 12)

(3A,120mils ,Via NO.= 6)

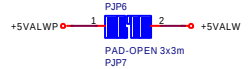


(3A,120mils ,Via NO.= 6)

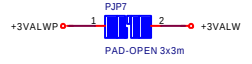
(300mA,40mils ,Via NO.= 2)



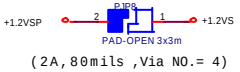
(120mA,20mils ,Via NO.= 1)



(5A,200mils ,Via NO.= 10)



(5A,200mils ,Via NO.= 10)



(2A,80mils ,Via NO.= 4)

Compal Electronics, Inc.

Title: DCIN & DETECTOR

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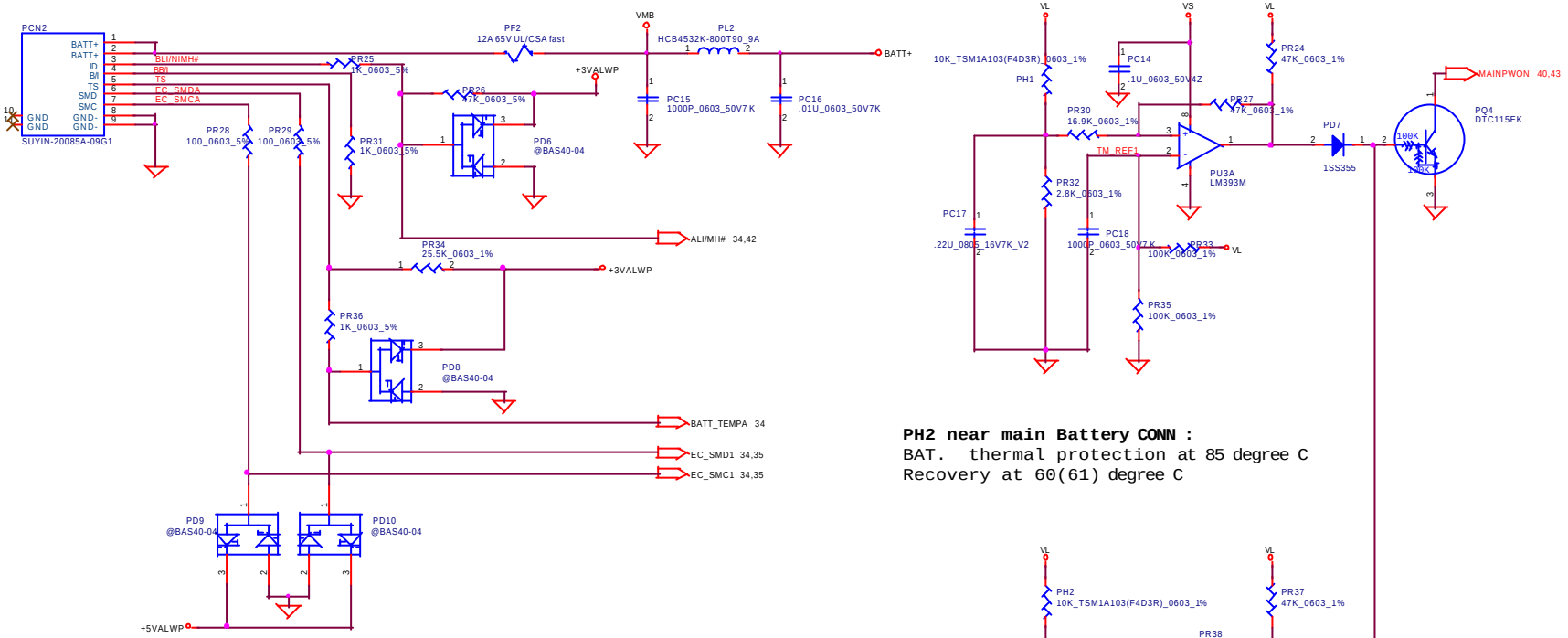
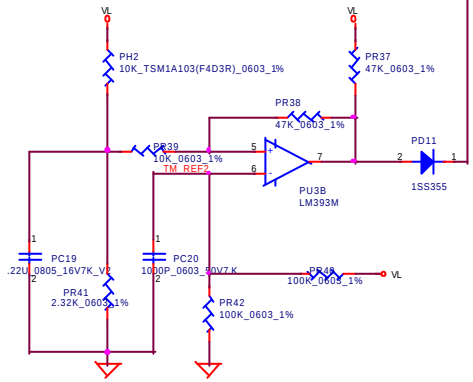
PH1 under CPU botten side :
CPU thermal protection at 90(91) degree C
Recovery at 50 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 85 degree C
Recovery at 60(61) degree C



Compal Electronics, Inc.

Title: BATTERY CONN / OTP

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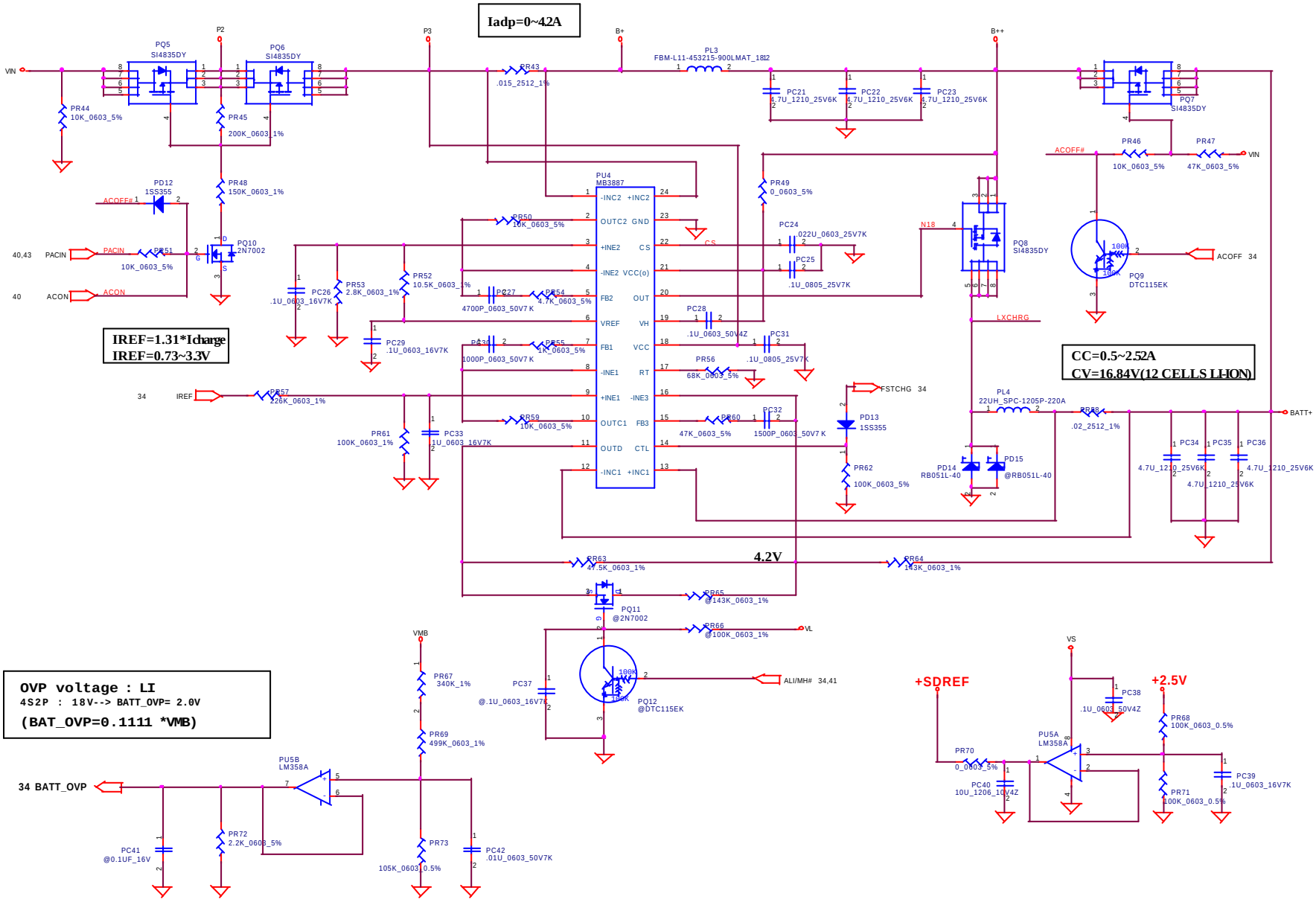

Compal Electronics, Inc.

Title: CHARGER

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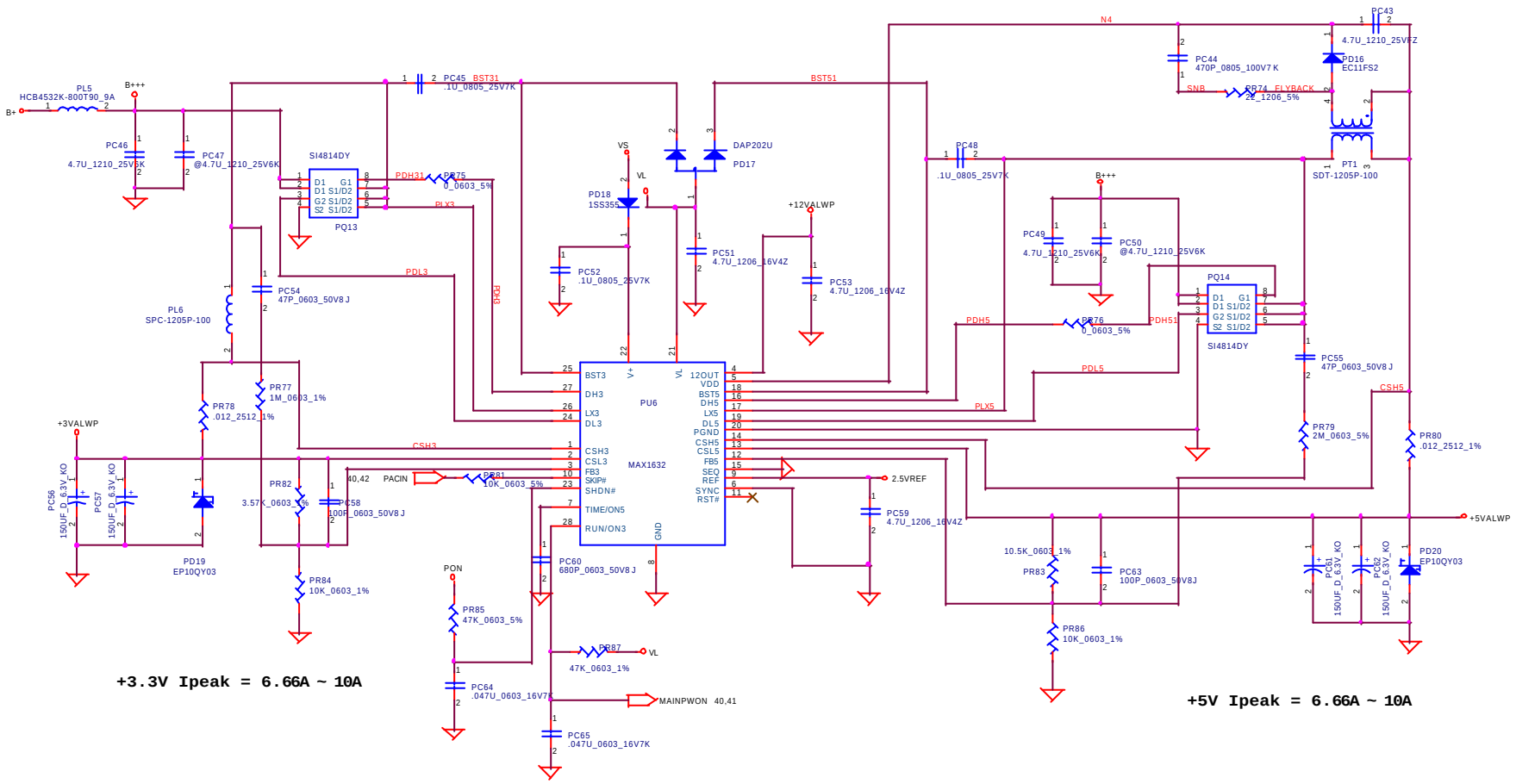

Compal Electronics, Inc.

Title: 5V/3.3V/12V

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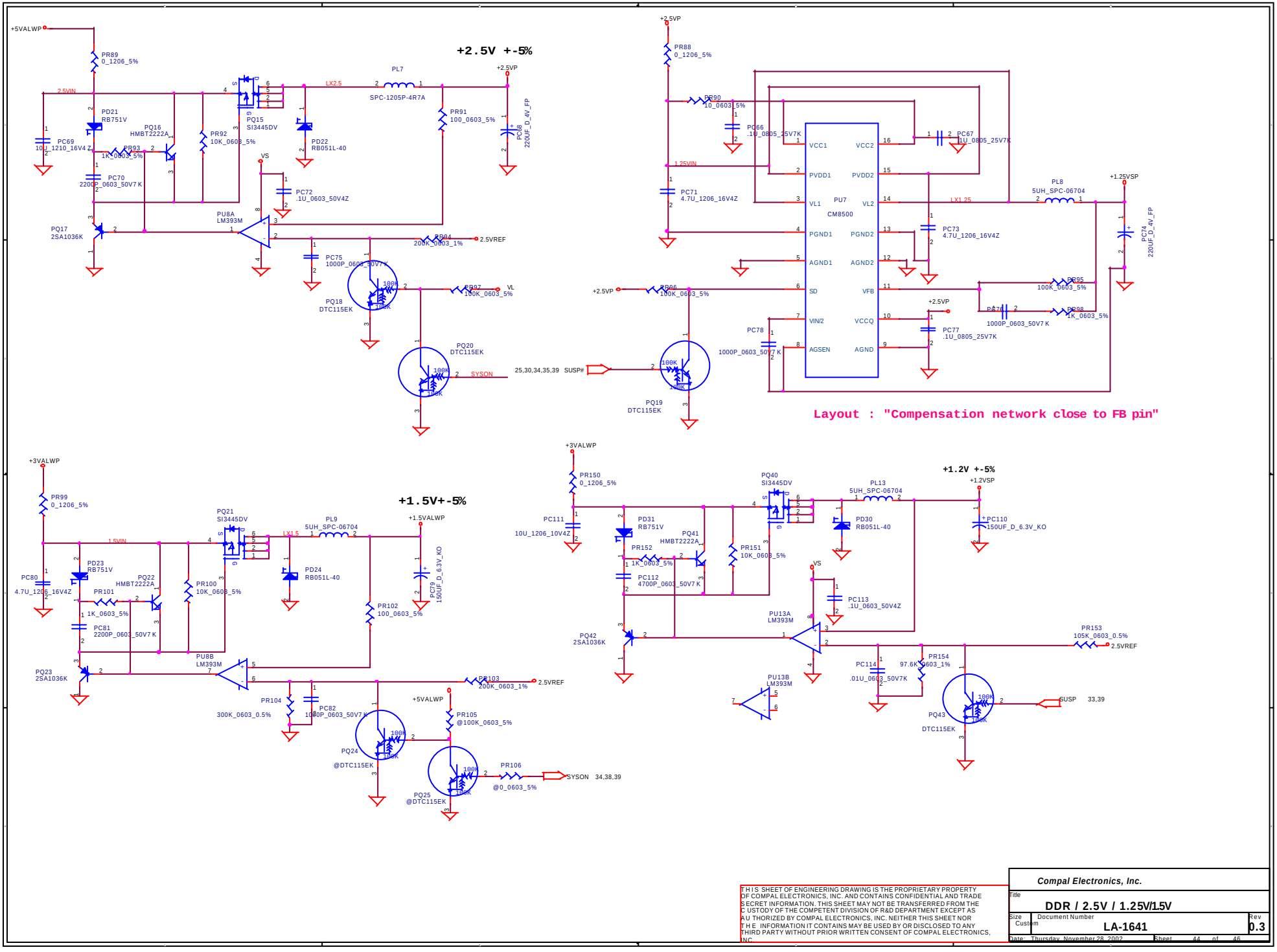

Compal Electronics, Inc.

Title: DDR / 2.5V / 1.25V/1.5V

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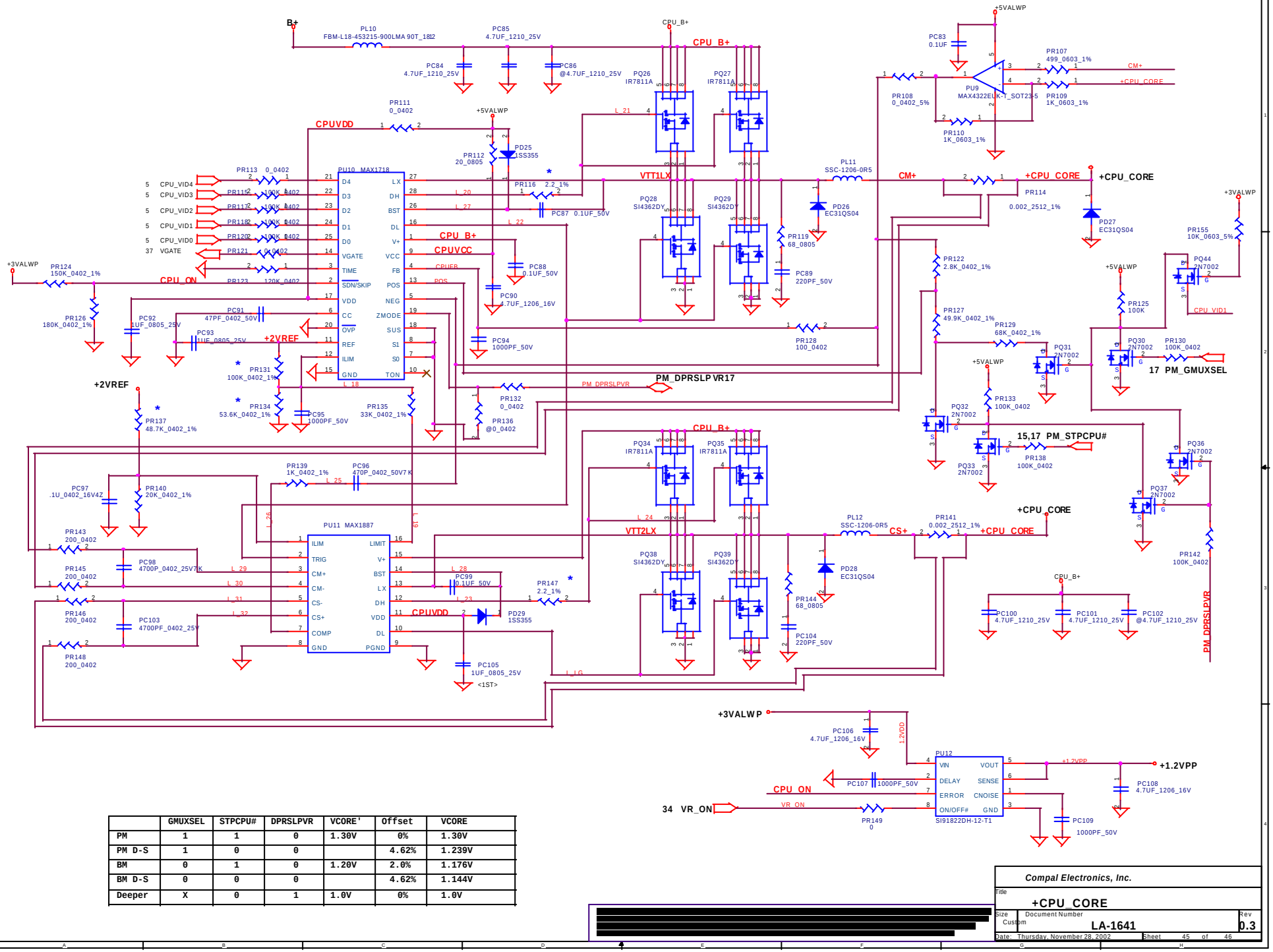

	GMUXSEL	STPCPU#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

[redacted]

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Title: +CPU_CORE

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REV 0.2

Date	Page	Description
09/27		Update Rev0.1 to Rev.0.2
10/16	8	Change U32(SSC) source from CLK_VCH to CLK_MCH_48M
	8	Change Q55 R537 R538 to U33A
	13	Add zero Ohm resistor between pin3 of JP1 and GND.
	15	Add R539 R540 2.2K pull high to +3VALW on net SMB_DATA and SMB_CLK
10/17	17	Add R549 on ICH4 GPI7 pull high to +3VS
	26	Add J3 between +5VS and +5VS_IDE
	17	Delete net USB_EN# and PAL/NTSC# on U12 pinW4 & pinW1
	29	Modify BlueTooth schematic
	32	Add Pass-High Filter (R550, R551, C676, C677) on net AMP_LEFT, AMP_RIGHT
	32	Change R465 power plan from +5VS to +5VCD
	34	Add Net Thertrip#, PM_SLP_S1#, BT_RST# on EC
	35	Change U23 to U22B
10/18	36	Change FAN Schematic from PWM to RPM
	37	Add R541 and R542 100K pull high to +3VALW on net Button1#, Internet#
10/22		Formal release Schematic Rev0.2
10/24	44	Add P4-M/P4-C auto detection schematic, PQ44, PR155
11/18	42	Change PC43 to 4.7U
11/18	40	Change PR32 to 2.8K, PR41 to 2.32K
11/20	34	Add R575, R576, R577, R578, R579 between device PME#s and EC_PME#

[redacted]

Compal Electronics, Ltd.

Title: PIR

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