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# Compal Confidential

## HTW20 LA-3171P Schematics Document

### Intel Yonah/Merom with 945PM/GM + DDRII + ICH7M

### (+VGA/B ATi M52P/M54P/56P)

**2006-04-26**

**REV: 1.0**

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Title: Cover Sheet

Size | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 1 of 44

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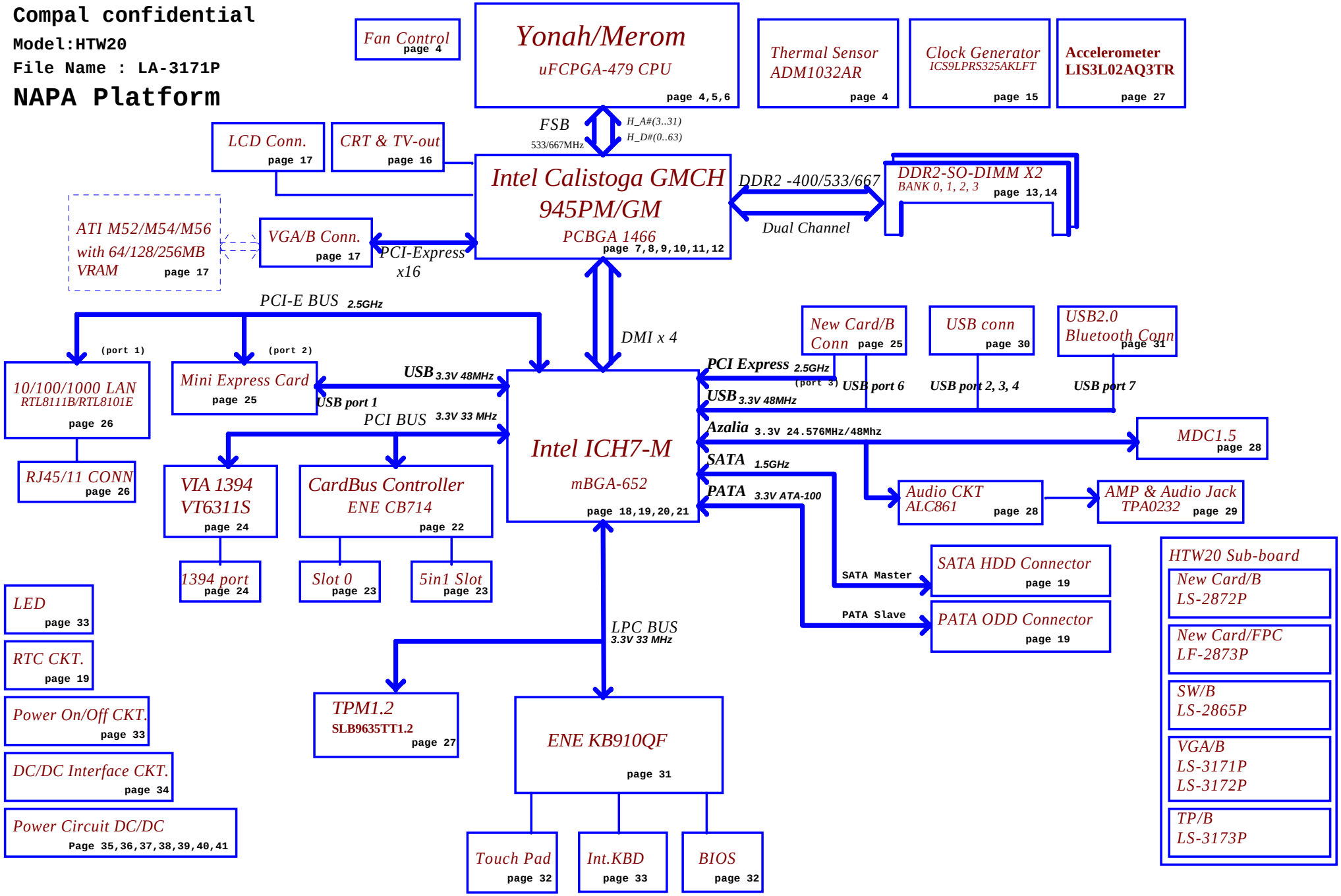
**Model:HTW20**

**File Name : LA-3171P**

# NAPA Platform

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Title: Block Diagram

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## Voltage Rails

| Power Plane | Description | S1 | S3 | S5 |
|---|---|---|---|---|
| VIN | Adapter power supply (19V) | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +0.9VS | 0.9V switched power rail for DDR terminator | ON | OFF | OFF |
| +VCCP | 1.05V switched power rail | ON | OFF | OFF |
| +1.5VS | 1.5V switched power rail | ON | OFF | OFF |
| +1.8V | 1.8V power rail for DDR | ON | ON | OFF |
| +1.8VS | 1.8V switched power rail | ON | OFF | OFF |
| +2.5VS | 2.5V switched power rail | ON | OFF | OFF |
| +3VALW | 3.3V always on power rail | ON | ON | ON* |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON* |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +VSB | +VSB always on power rail | ON | ON | ON* |
| +RTCVCC | RTC power | ON | ON | ON |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

| DEVICE | PCI Device ID | IDSEL # | REQ/GNT # | PIRQ |
|---|---|---|---|---|
| 1394 | D0 | AD16 | 0 | E |
| CARD BUS | D4 | AD20 | 2 | A,B |
| 5IN1 | D4 | AD20 | 2 | A,B |

## KB910 I2C / SMBUS ADDRESSING

| DEVICE | HEX | ADDRESS |
|---|---|---|
| SM1 24C16 | A0H | 1 0 1 0 0 0 0 X b |
| SM1 SMART BATTERY | 16H | 0 0 0 1 0 1 1 X b |
| SM2 ADM0132<br>CPU THERMAL MONITOR | 98H | 1 0 0 1 1 0 0 X b |

## ICH7-M SM Bus address

| DEVICE | HEX | ADDRESS |
|---|---|---|
| DDR SO-DIMM 0 | A0 | 1 0 1 0 0 0 0 0 |
| DDR SO-DIMM 1 | A4 | 1 0 1 0 0 1 0 0 |
| CLOCK GENERATOR (EXT.) | D2 | 1 1 0 1 0 0 1 0 |

## Board ID / SKU ID Table for AD channel

| | |
|---|---|
| Vcc | 3.3V +/- 5% |
| Ra | 100K +/- 5% |

| Board ID | Rb | $V_{AD_BID}$ min | $V_{AD_BID}$ typ | $V_{AD_BID}$ max |
|---|---|---|---|---|
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| 0 | 0.1 |
| 1 | 0.2 |
| 2 | 0.3 |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## SKU ID Table

| SKU ID | SKU |
|---|---|
| 0 | |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## BTO Option Table

| BTO Item | BOM Structure |
|---|---|
| VGA | GM@<br>PM@ |
| New Card | NEWCARD@ |
| Giga LAN | 100M@<br>1000M@ |
| KILL SW | WLAN@ |
| BlueTooth | BT@ |
| 5IN1 | 5IN1@ |
| | |
| | |
| | |




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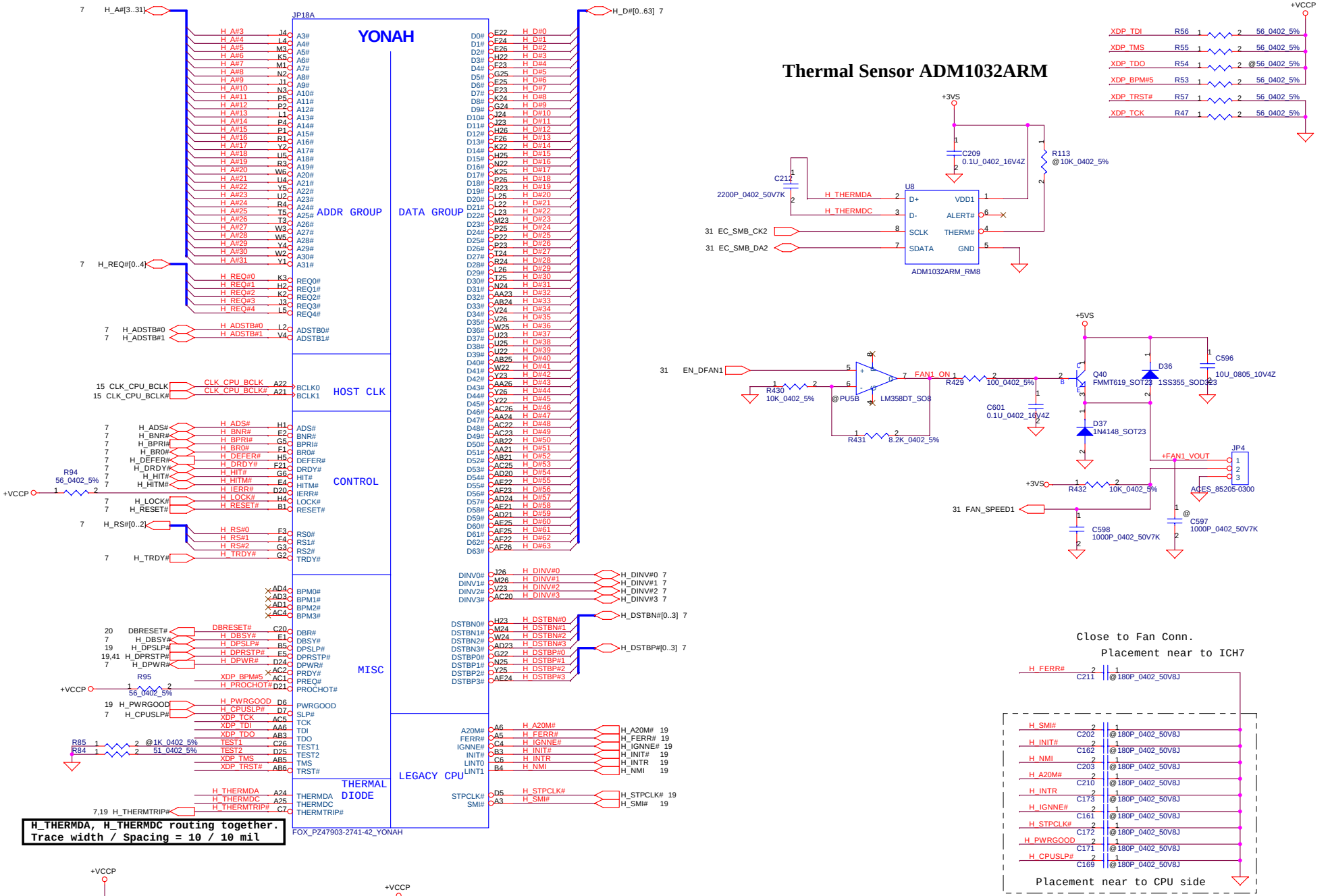


**H_THERMDA, H_THERMDC routing together.**
**Trace width / Spacing = 10 / 10 mil**

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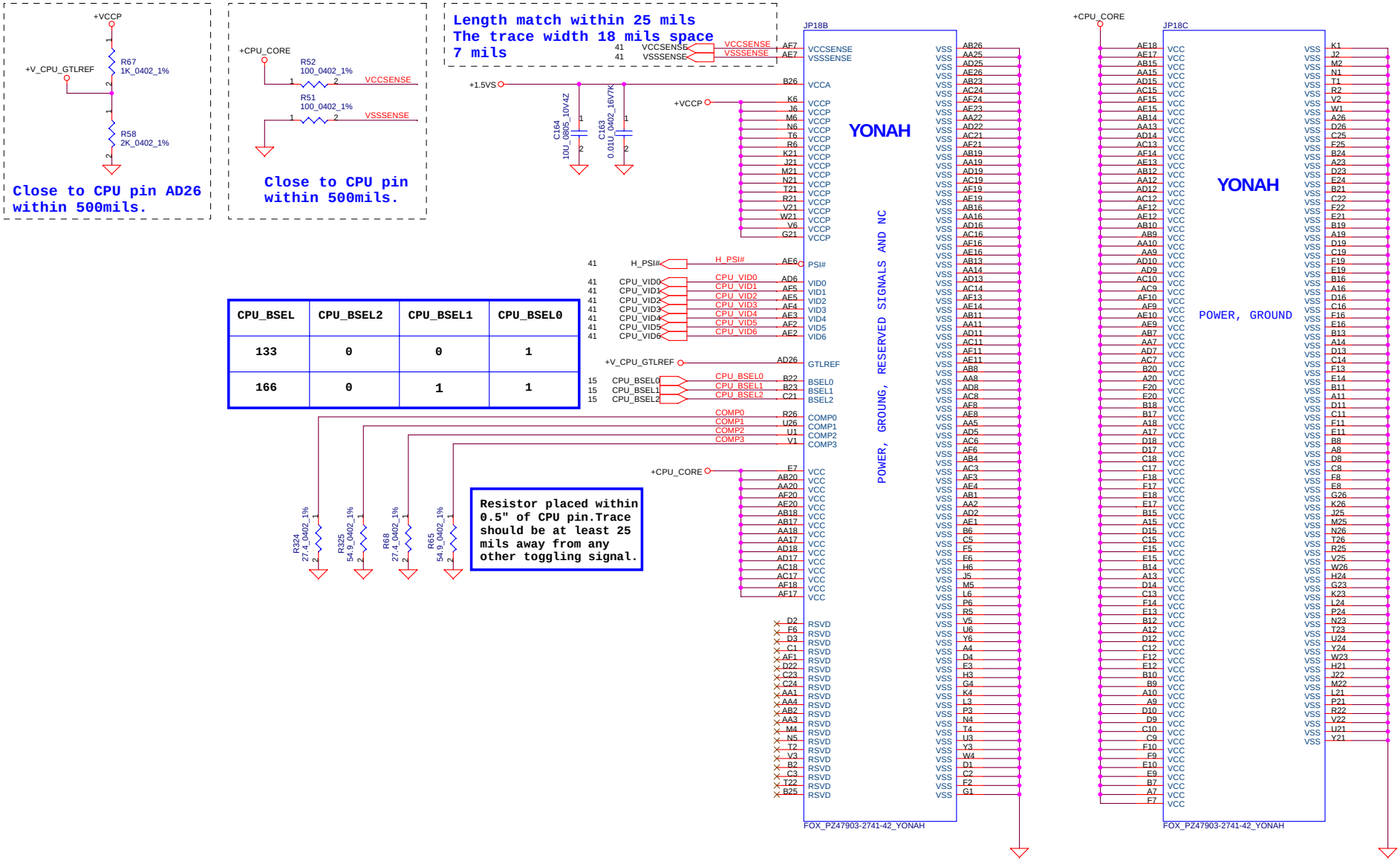
**Compal Electronics, Inc.**

Title: **Yonah CPU in mFCPGA479**

Size: | Document Number: **HTW20 M/B LA-3171P** | Rev: 1.0

Date: Tuesday, May 02, 2006 | Sheet 4 of 44




| CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0 |
|---|---|---|---|
| 133 | 0 | 0 | 1 |
| 166 | 0 | 1 | 1 |

| | | | |
|---|---|---|---|
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Title: **Yonah CPU in mFCPGA479**

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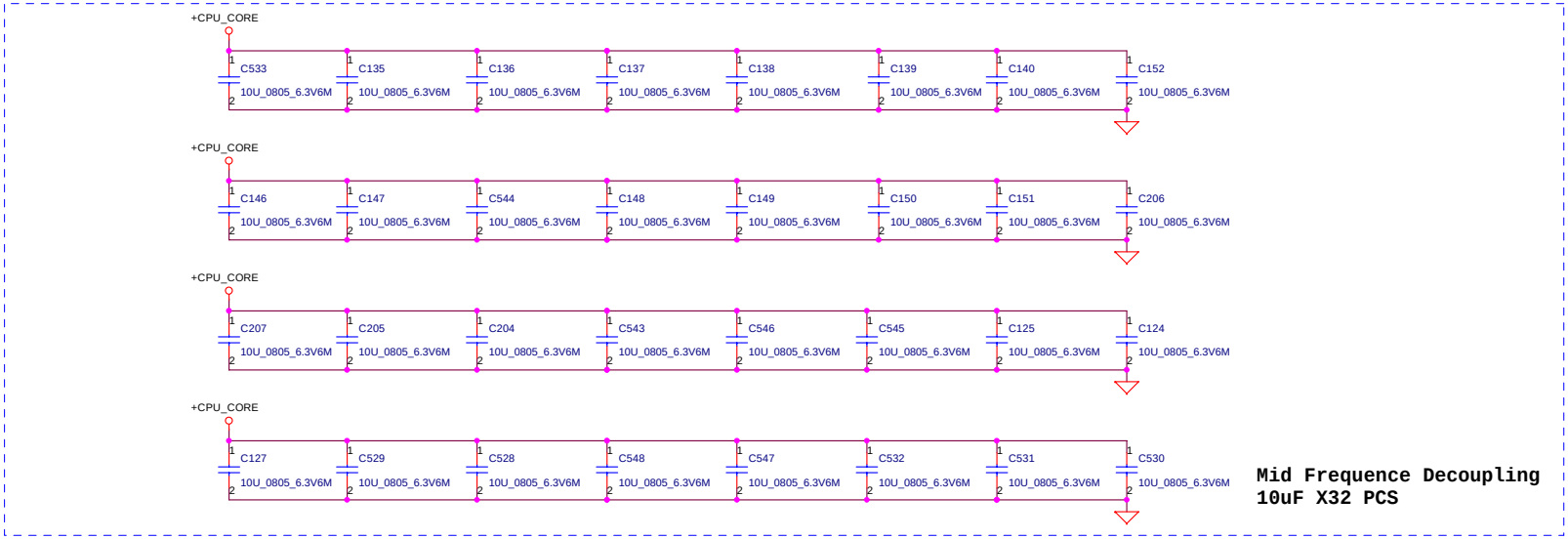
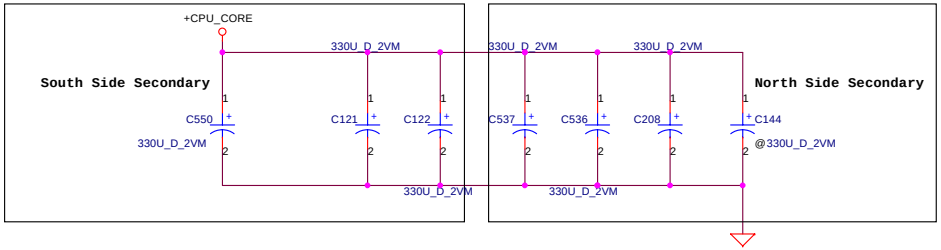
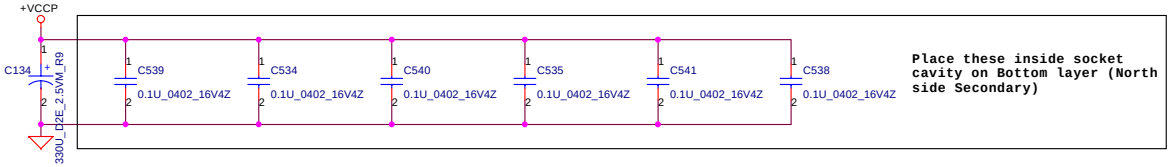



**ESR <= 1.5m ohm**
**Capacitor > 1980uF**

**330uF ESR 7m ohm X 6 PCS**

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**Compal Electronics, Inc.**

Title: **CPU Bypass capacitors**

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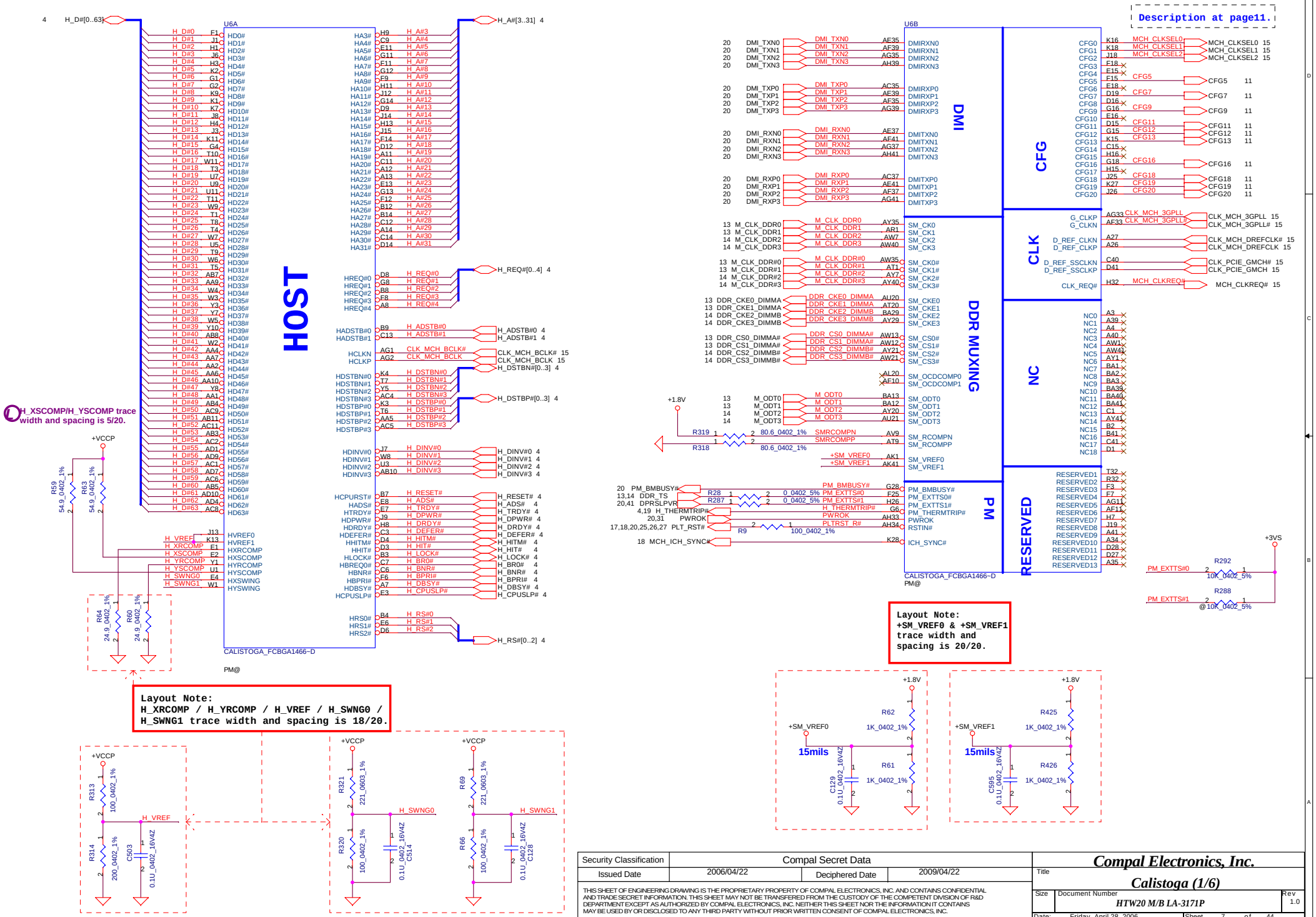


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Title: **Calistoga (1/6)**

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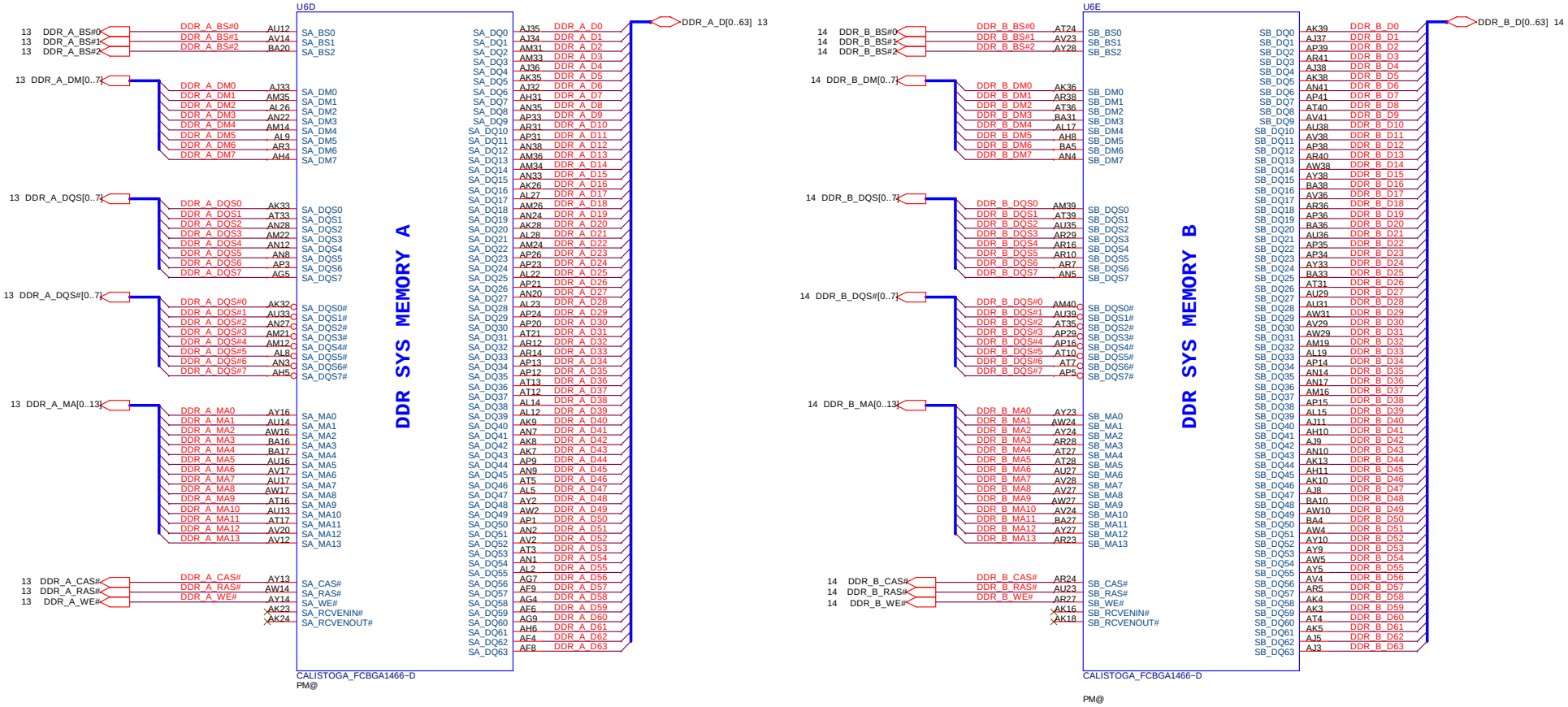


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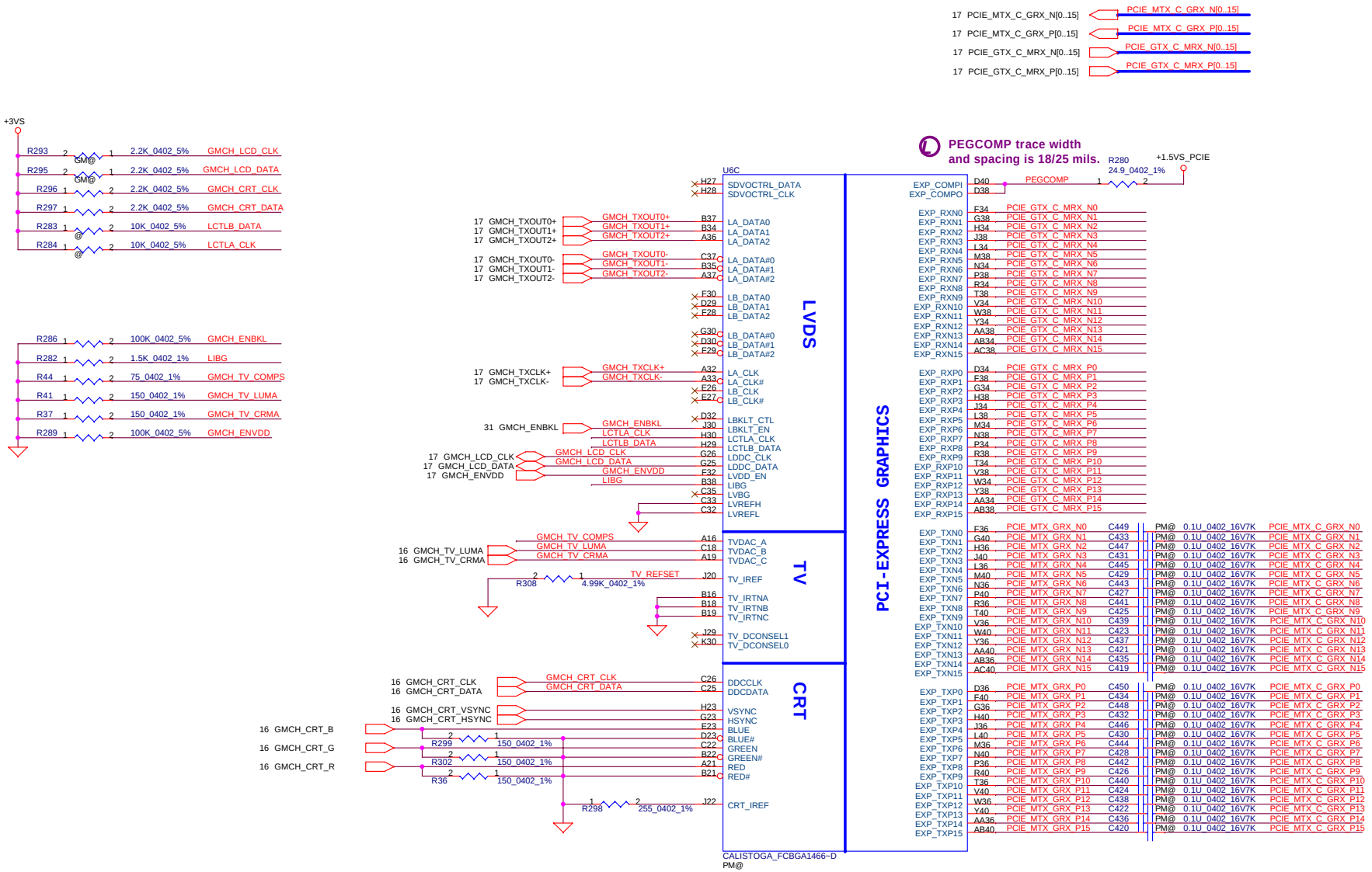


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Title: **Calistoga (3/6)**

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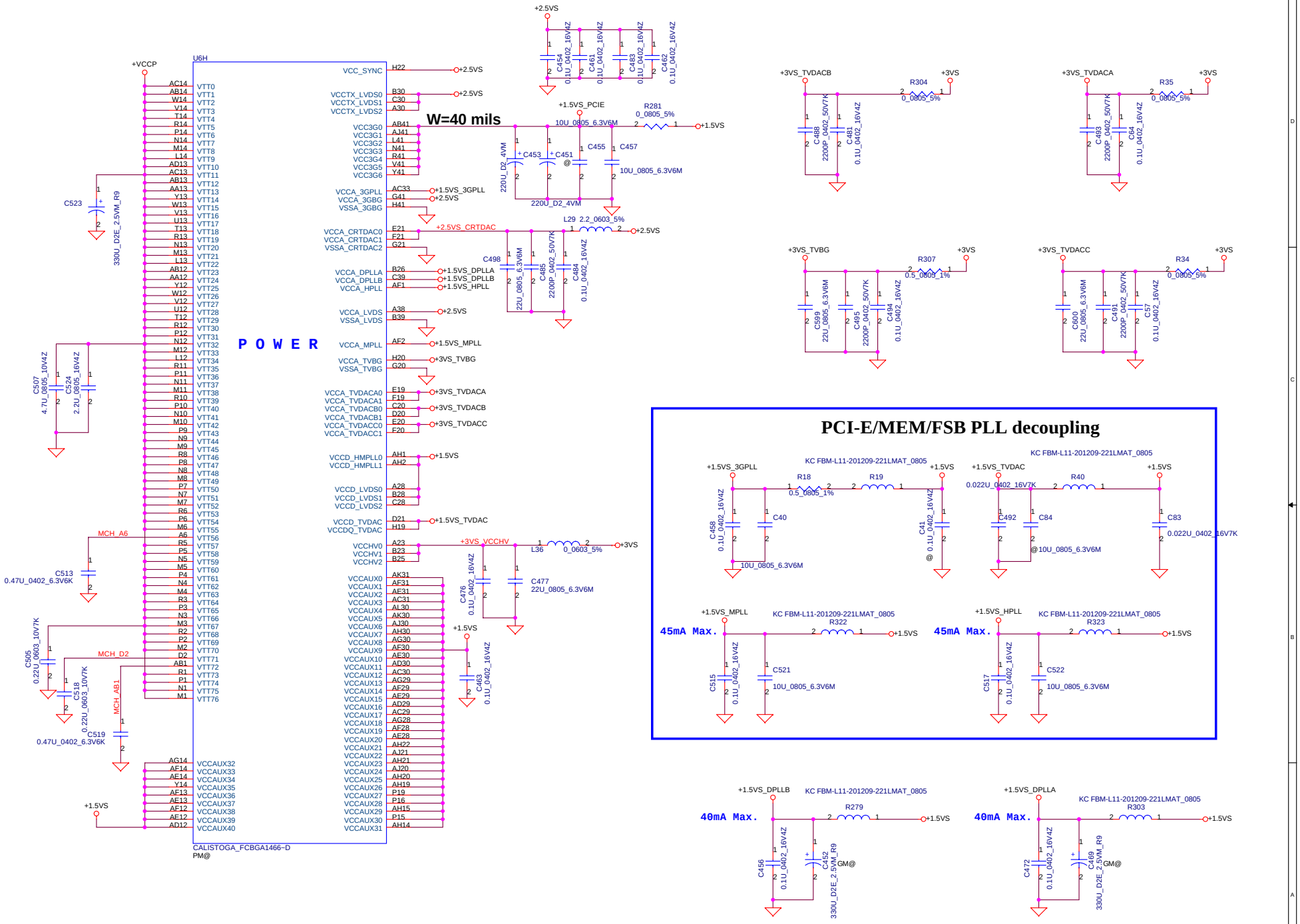


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Title: **Calistoga (4/6)**

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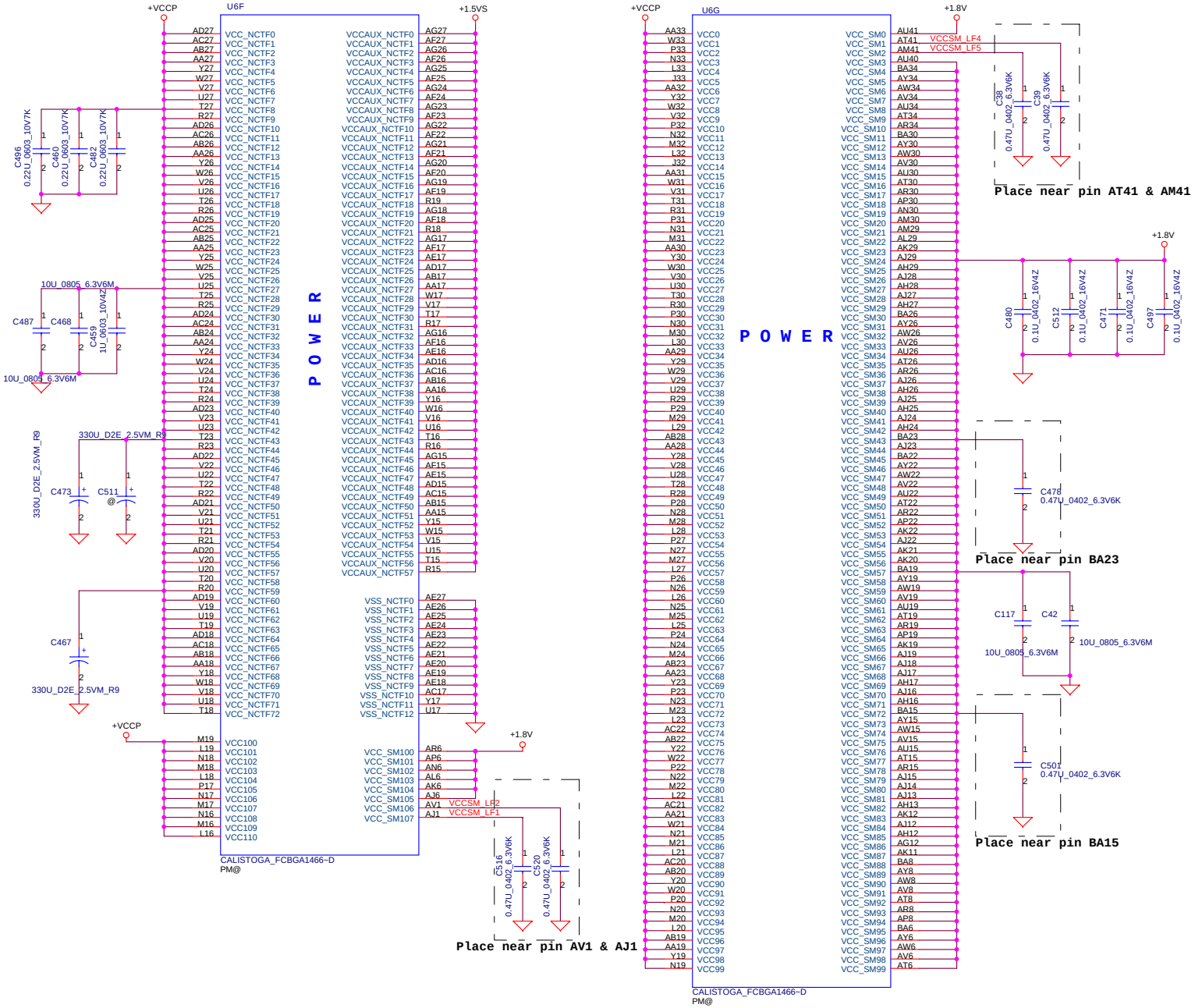


# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

| | |
|---|---|
| CFG[2:0] | 011 = 667MT/s FSB<br>001 = 533MT/s FSB |
| CFG5 | 0 = DMI x 2<br>1 = DMI x 4 *(Default) |
| CFG7 | 0 = Reserved<br>1 = Mobile Yonah CPU*(Default) |
| CFG9 | 0 = Lane Reversal Enable<br>1 = Normal Operation (Default)* |
| CFG11 | 0 = Reserved<br>1 = Calistoga * |
| CFG[13:12] | 00 = Reserved<br>01 = XOR Mode Enabled<br>10 = All Z Mode Enabled<br>11 = Normal Operation *(Default) |
| CFG16 | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled *(Default) |
| CFG18 | 0 = 1.05V *(Default)<br>1 = 1.5V |
| CFG19 | 0 = Normal Operation * (Default)<br>1 = DMI Lane Reversal Enable |
| SDVO_CTRLDATA | 0 = No SDVO Device Present * (Default)<br>1 = SDVO Device Present |
| CFG20 (PCIE/SDVO select) | 0 = Only PCIE or SDVO is operational. *(Default)<br>1 = PCIE/SDVO are operating simu. |

| | | | |
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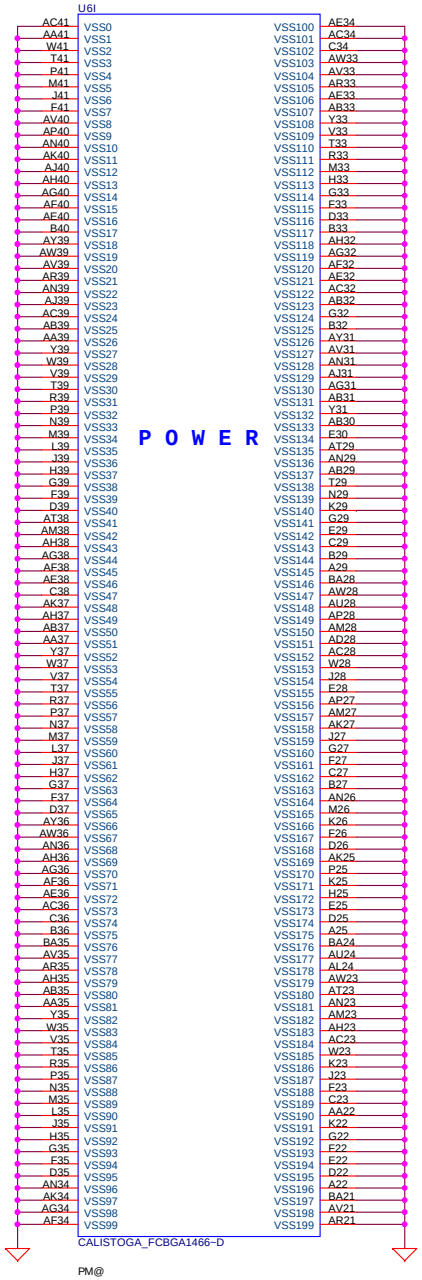


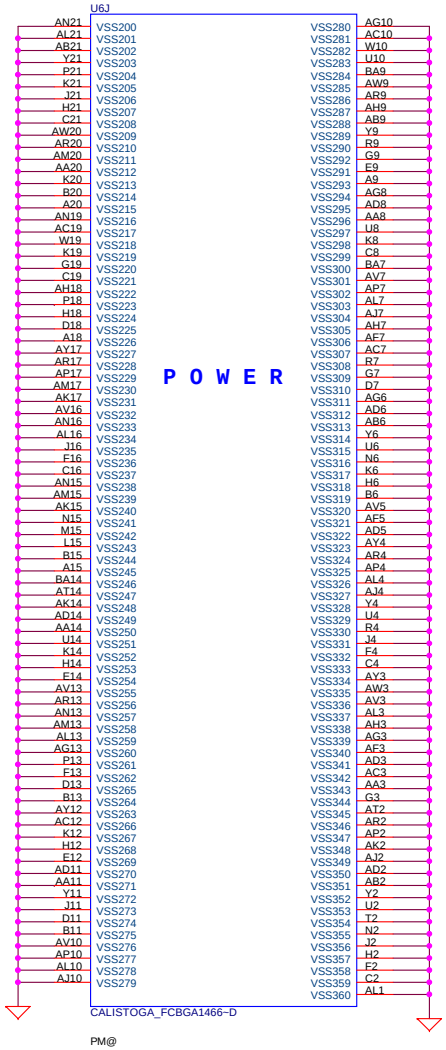


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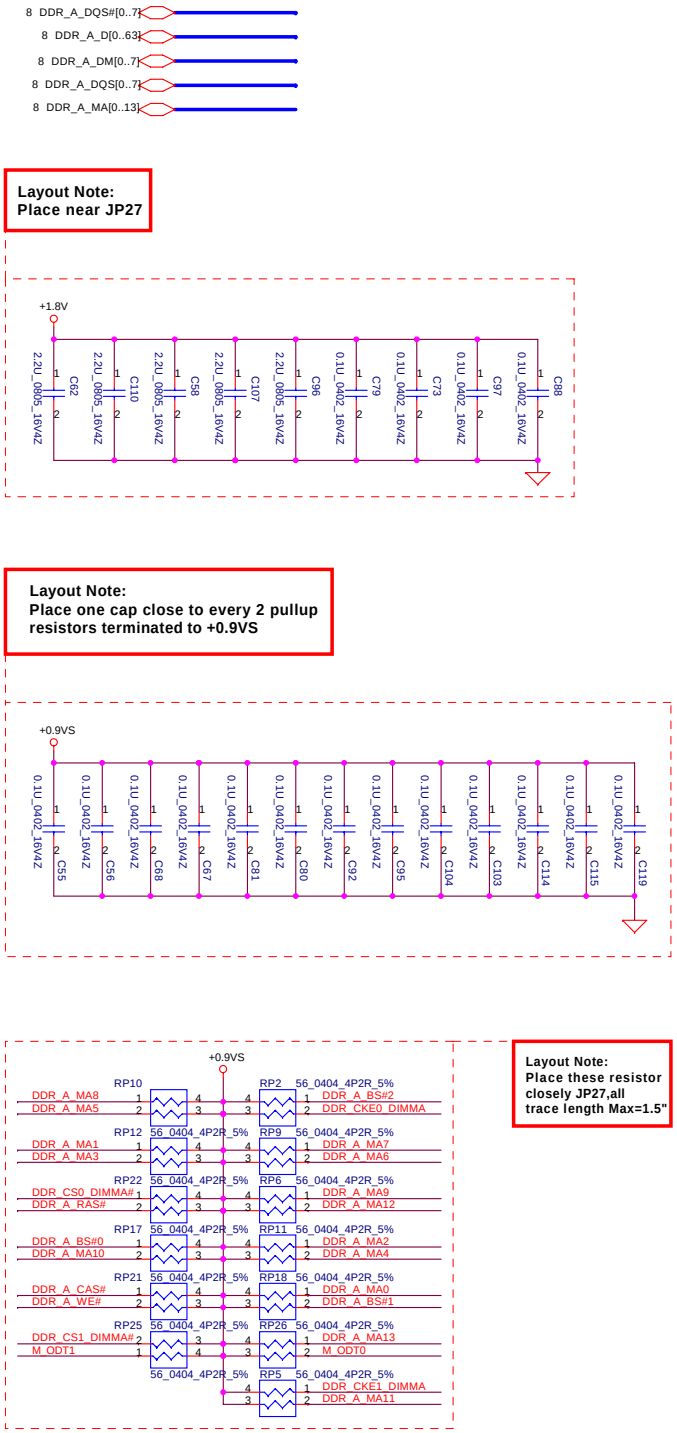


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**Compal Electronics, Inc.**

Title: **DDRII-SODIMM SLOT1**

Size | Document Number: *HTW20 M/B LA-3171P* | Rev 1.0

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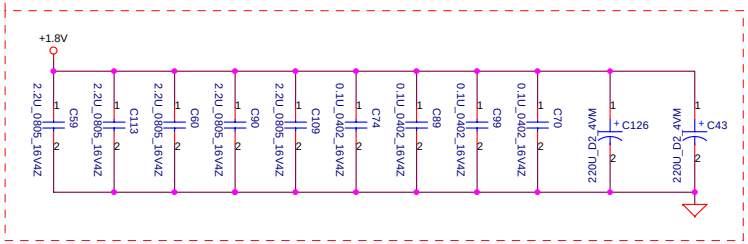
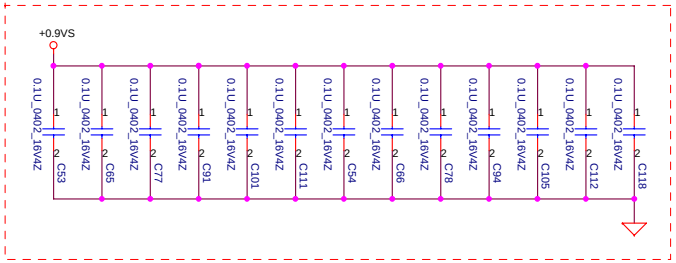
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

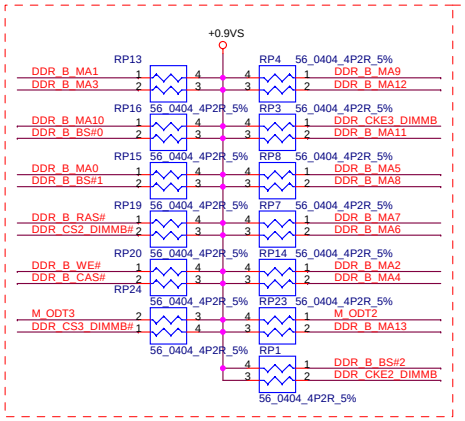
**Layout Note:**
**Place near JP26**

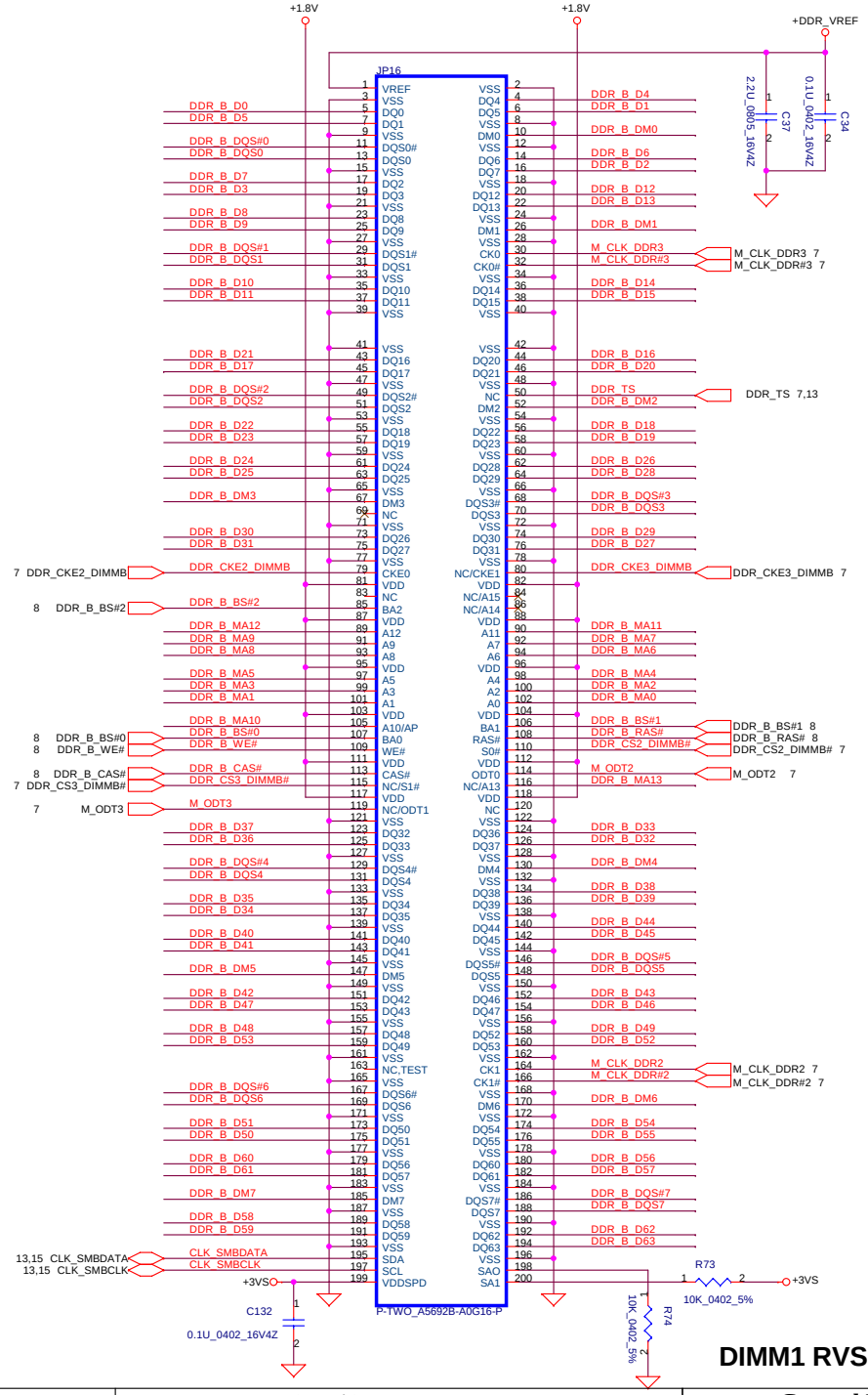



**Layout Note:**
**Place one cap close to every 2 pullup resistors terminated to +0.9VS**




**Layout Note:**
**Place these resistor closely JP26,all trace length Max=1.5"**




# DIMM1 RVS H:9.2mm (BOT)

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**Compal Electronics, Inc.**

Title: **DDRII-SODIMM SLOT2**

Size | Document Number: **HTW20 M/B LA-3171P** | Rev 1.0

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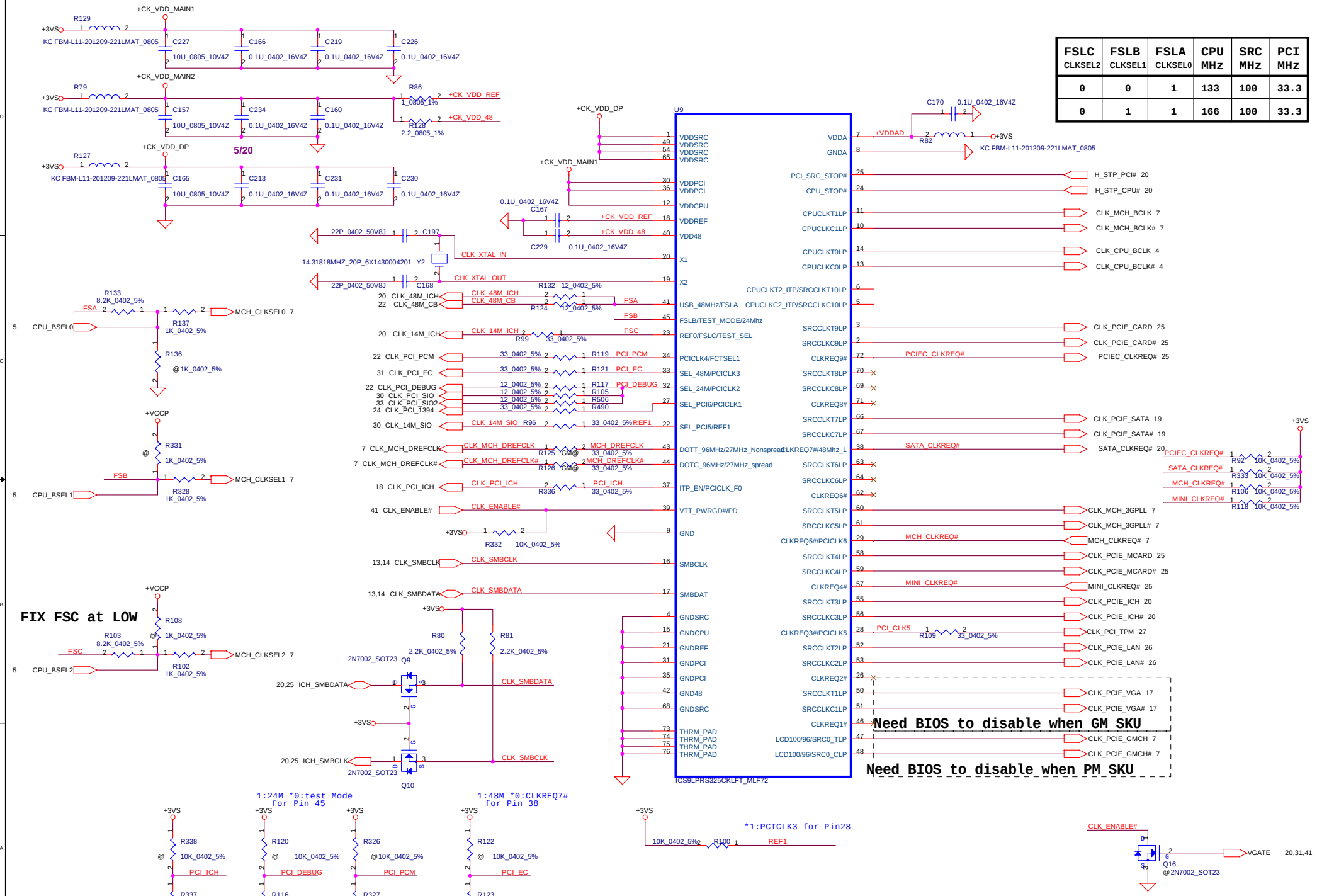
| FSLC CLKSEL2 | FSLB CLKSEL1 | FSLA CLKSEL0 | CPU MHz | SRC MHz | PCI MHz |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 133 | 100 | 33.3 |
| 0 | 1 | 1 | 166 | 100 | 33.3 |




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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**Compal Electronics, Inc.**

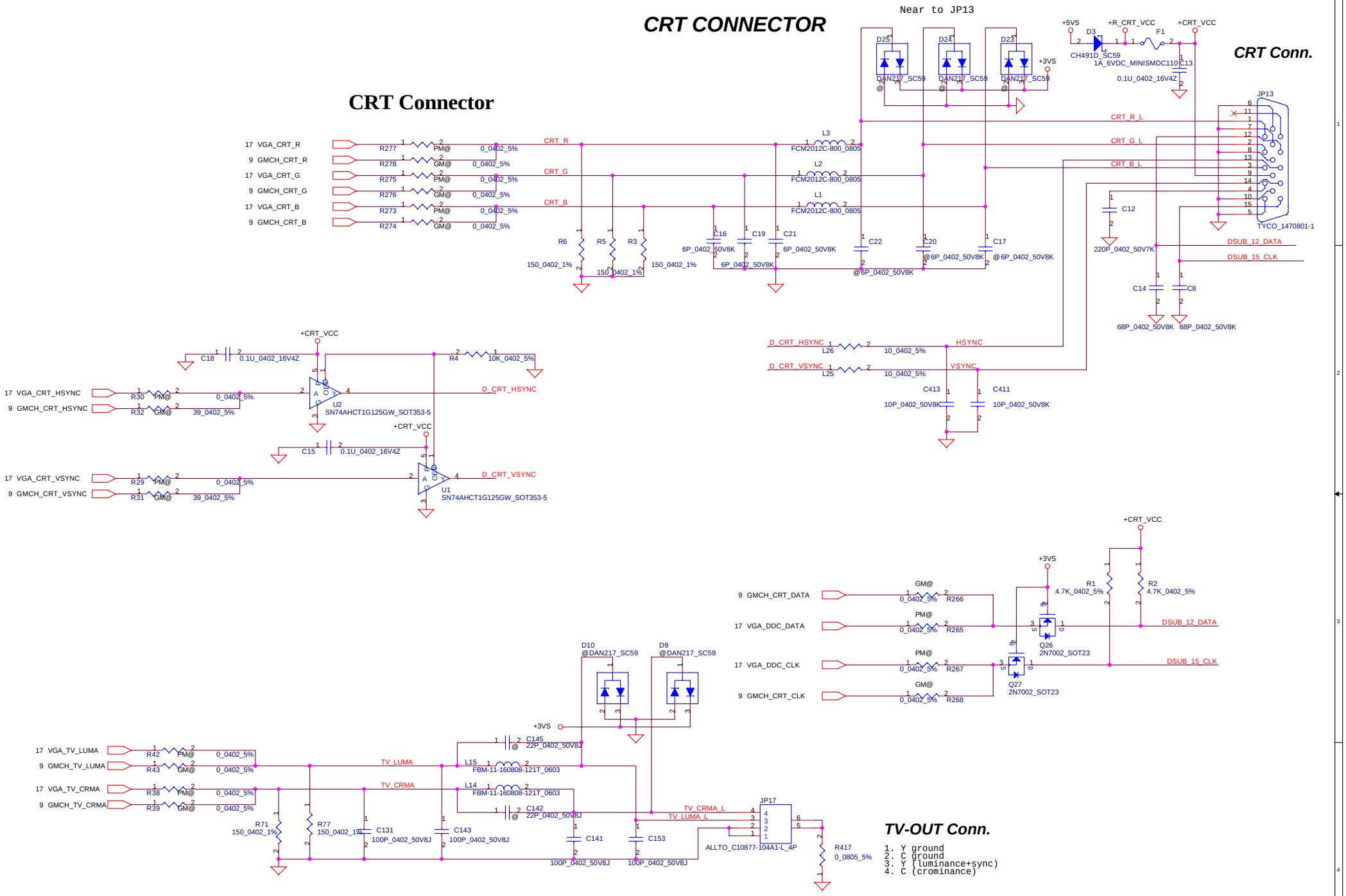
Title: **Clock generator**

Size: | Document Number: *HTW20 M/B LA-3171P* | Rev: 1.0

Date: Tuesday, May 02, 2006 | Sheet 15 of 44

# CRT CONNECTOR

## CRT Connector




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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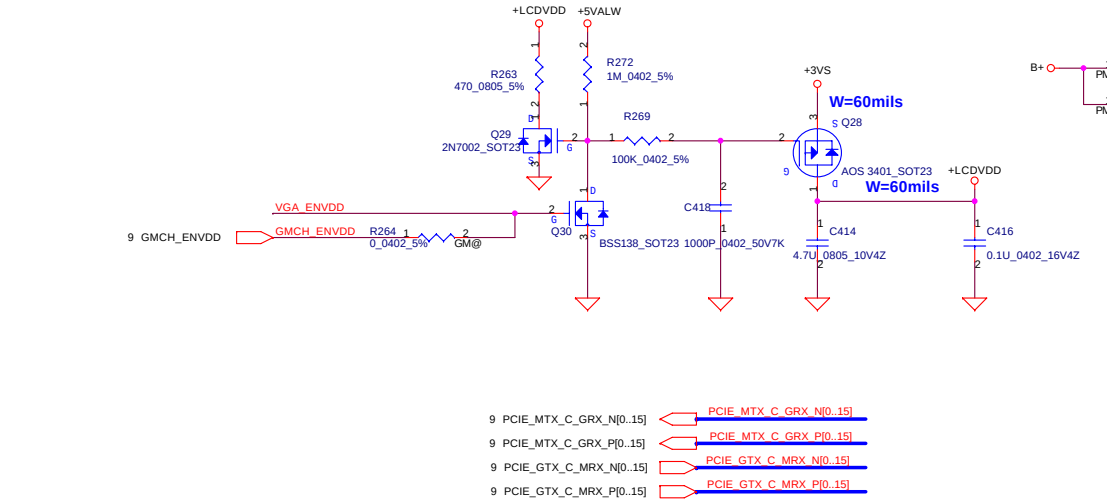
**Compal Electronics, Inc.**

Title: *CRT & TVout Connector*

Size | Document Number: *HTW20 M/B LA-3171P* | Rev 1.0

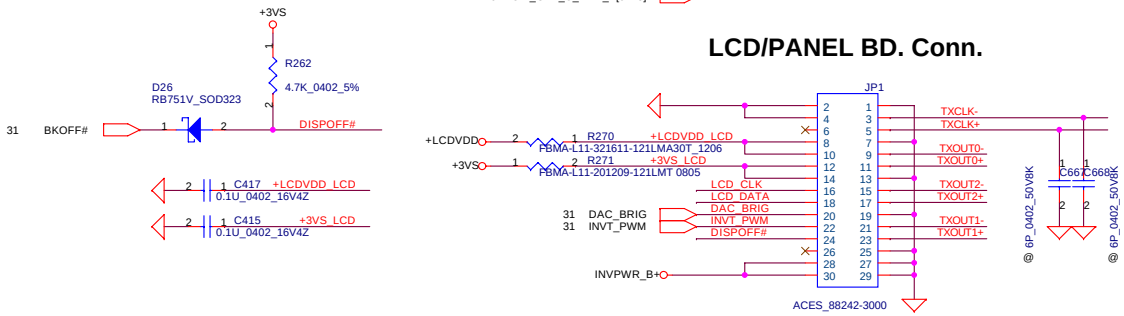
Date: Tuesday, May 02, 2006 | Sheet 16 of 44

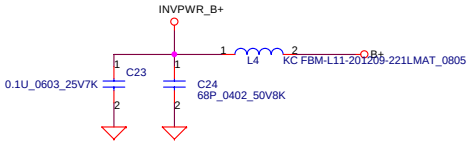
# LCD POWER CIRCUIT

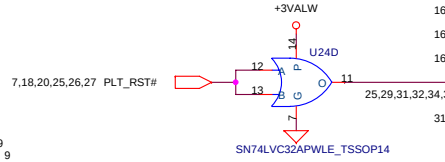


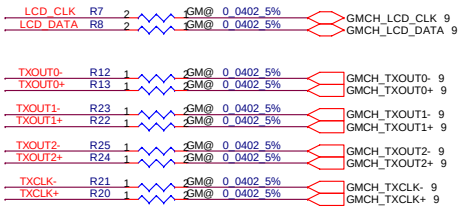

# VGA BOARD Conn.

# LCD/PANEL BD. Conn.




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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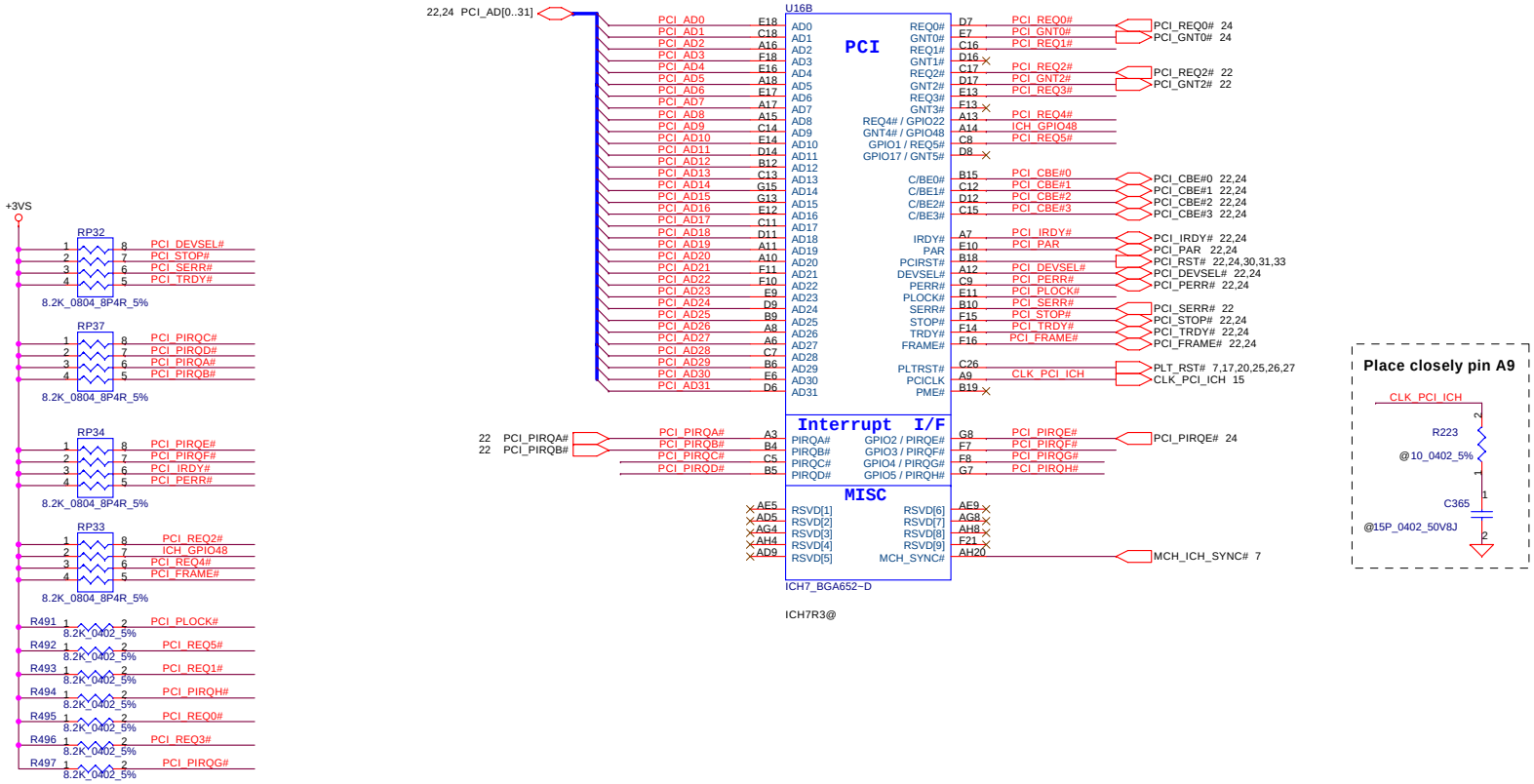
**Compal Electronics, Inc.**

Title: ***VGA / LCD CONN.***

Size | Document Number: ***HTW20 M/B LA-3171P*** | Rev 1.0

Date: Friday, April 28, 2006 | Sheet 17 of 44




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
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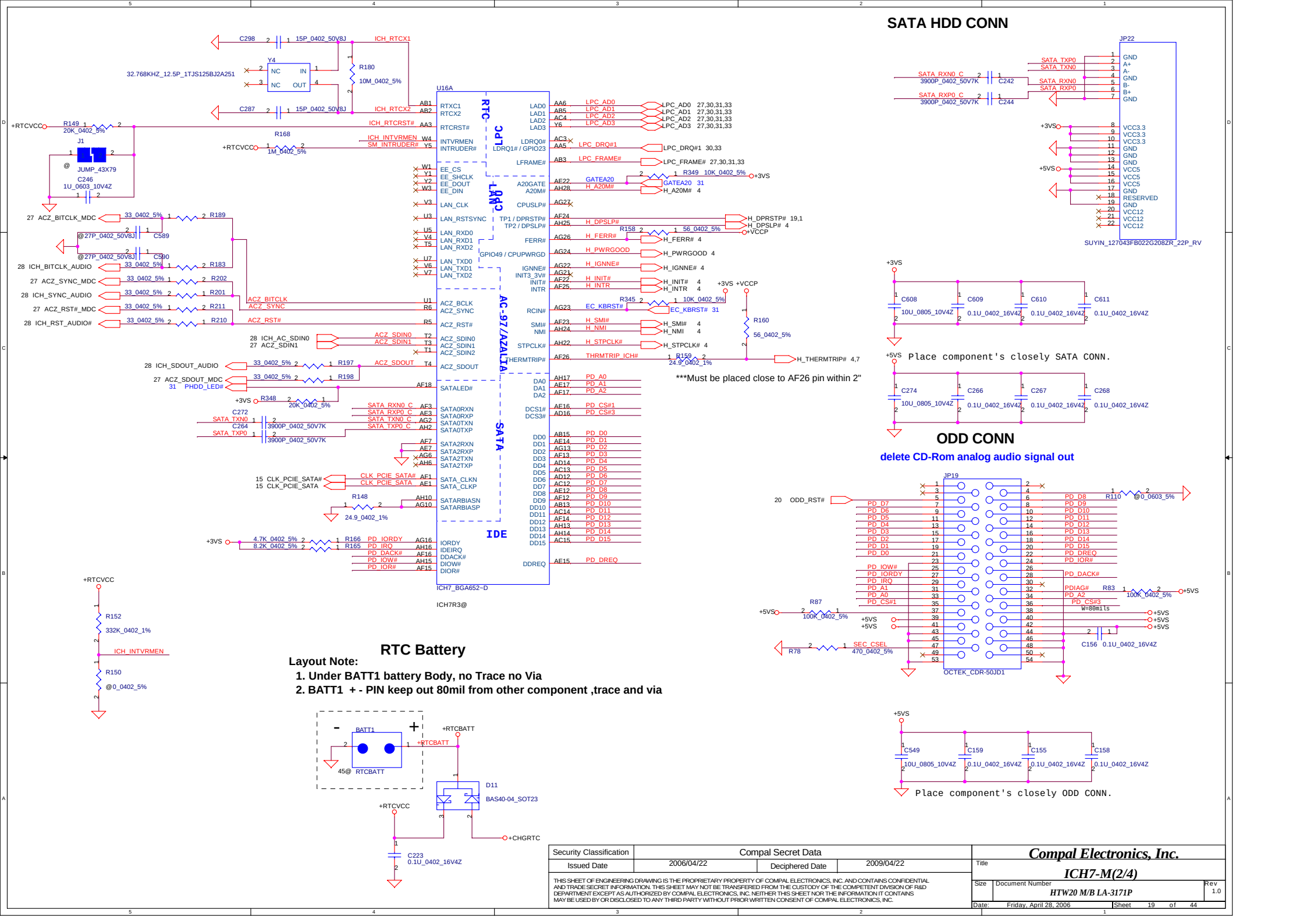
**Compal Electronics, Inc.**

Title: **ICH7-M(1/4)**

Size | Document Number: *HTW20 M/B LA-3171P* | Rev 1.0

Date: Friday, April 28, 2006 | Sheet 18 of 44


SATA HDD CONN
JP22
SUYIN_127043FB022G208ZR_22P_RV
Place component's closely SATA CONN.
ODD CONN
delete CD-Rom analog audio signal out
JP19
OCTEK_CDR-50JD1
Place component's closely ODD CONN.
U16A
ICH7_BGA652-D
ICH7R3@
***Must be placed close to AF26 pin within 2"
RTC Battery
Layout Note:
1. Under BATT1 battery Body, no Trace no Via
2. BATT1 + - PIN keep out 80mil from other component ,trace and via
BATT1
RTCBATT
D11
BAS40-04_SOT23
+CHGRTC
Compal Electronics, Inc.
ICH7-M(2/4)
HTW20 M/B LA-3171P
Rev 1.0
Date: Friday, April 28, 2006
Sheet 19 of 44
Security Classification
Compal Secret Data
Issued Date
2006/04/22
Deciphered Date
2009/04/22
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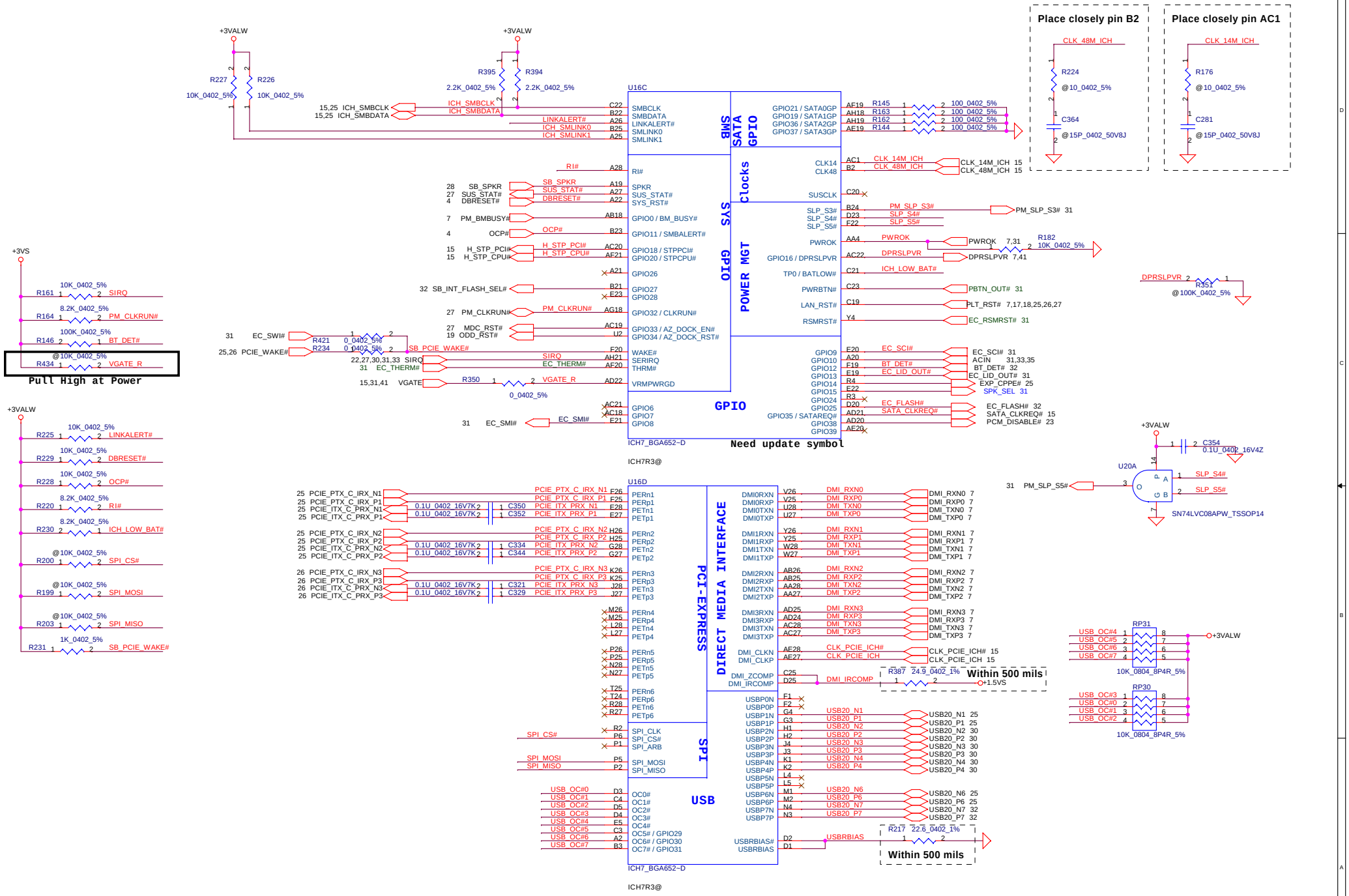


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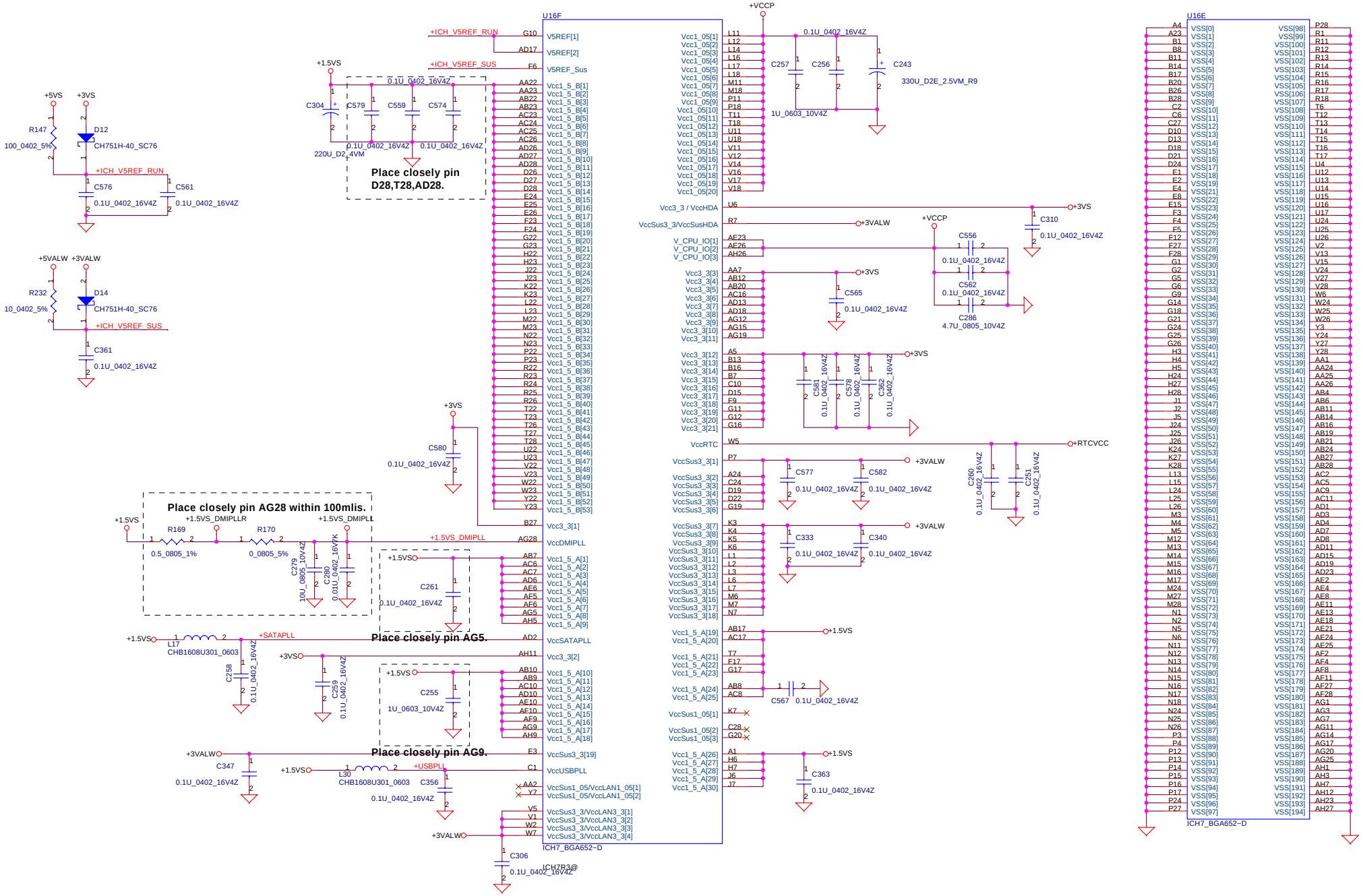
**Compal Electronics, Inc.**

Title: **ICH7-M(3/4)**

Size: | Document Number: **HTW20 M/B LA-3171P** | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 20 of 44

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|---|---|---|---|
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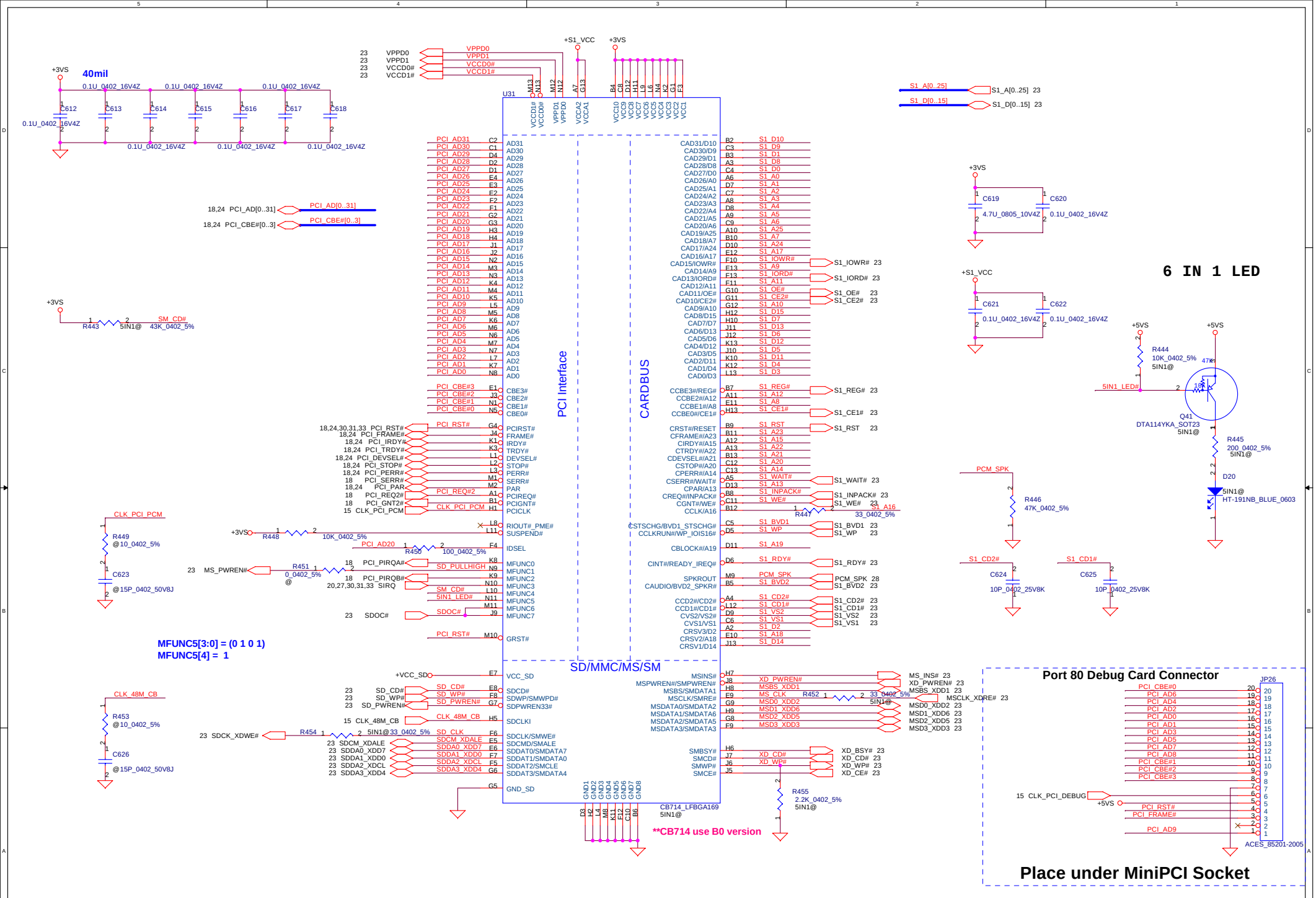
**Compal Electronics, Inc.**

Title: **ICH7-M(4/4)**

Size | Document Number: **HTW20 M/B LA-3171P** | Rev 1.0

Date: Tuesday, May 02, 2006 | Sheet 21 of 44




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
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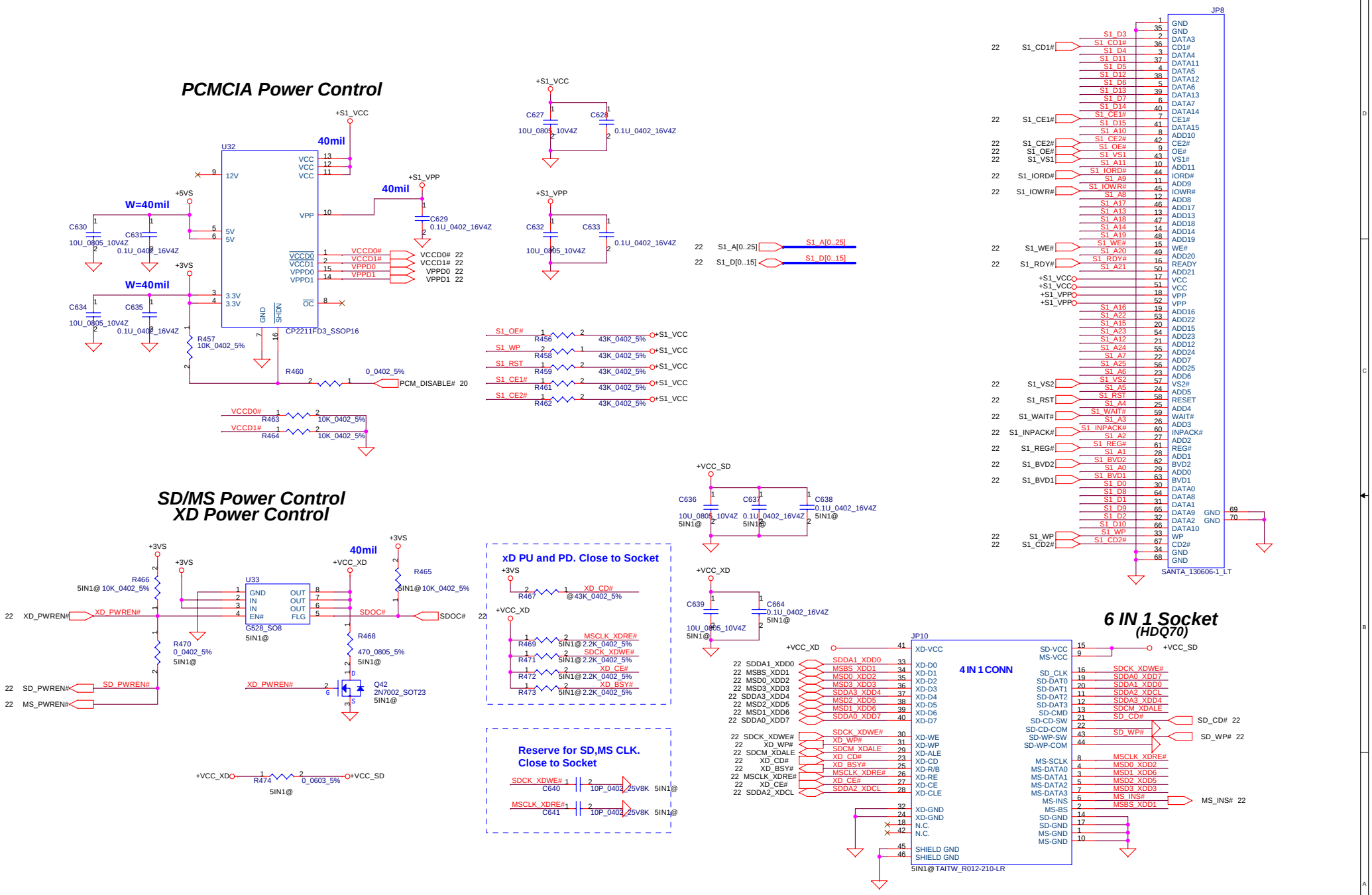
**Compal Electronics, Inc.**

Title: **ENE CB714**

Size: Custom | Document Number: **HTW20 M/B LA-3171P** | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 22 of 44

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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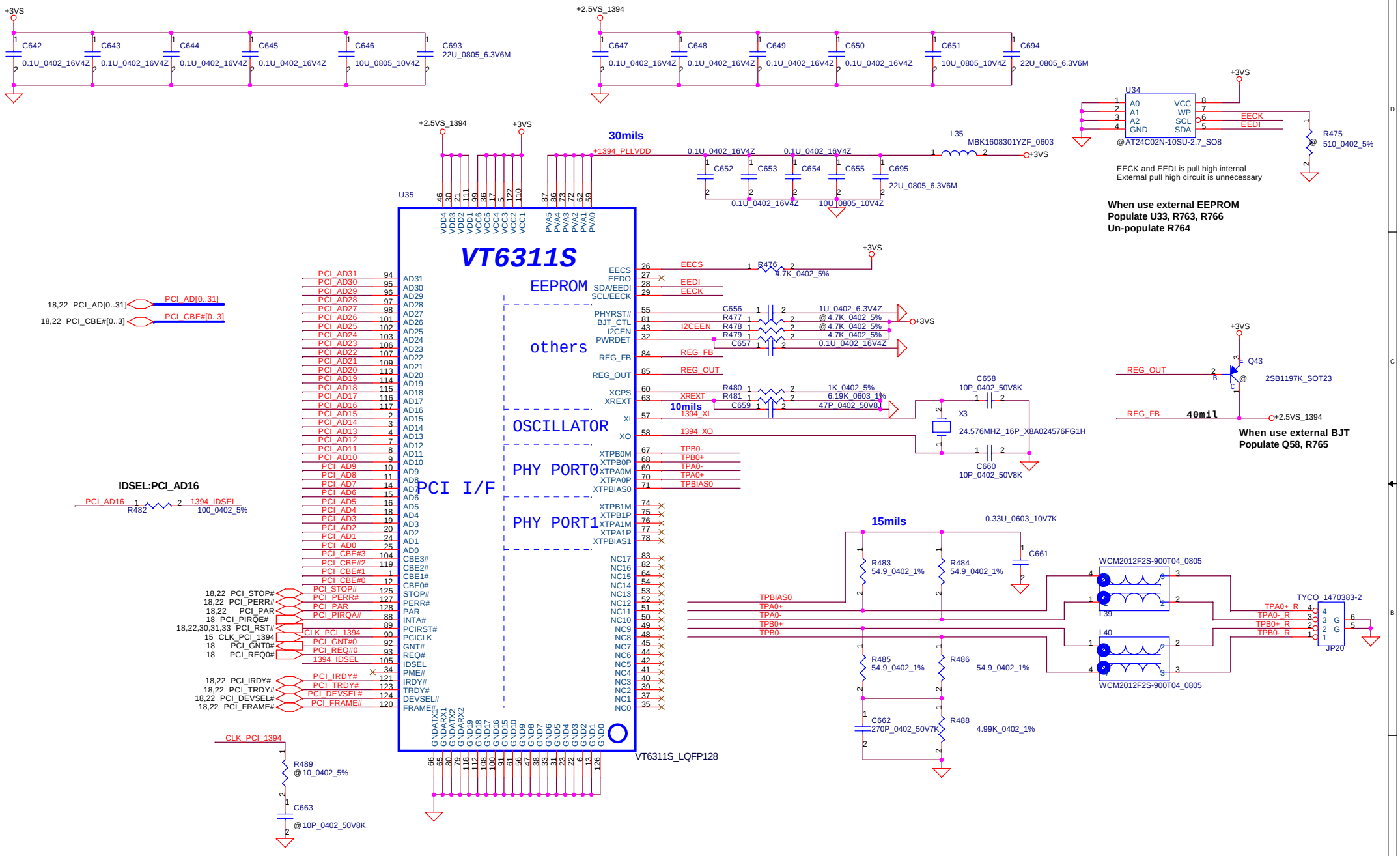
**Compal Electronics, Inc.**

Title: **PCMCIA& 4in1 socket**

Size: Custom | Document Number: **HTW20 M/B LA-3171P** | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 23 of 44

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|---|---|---|---|
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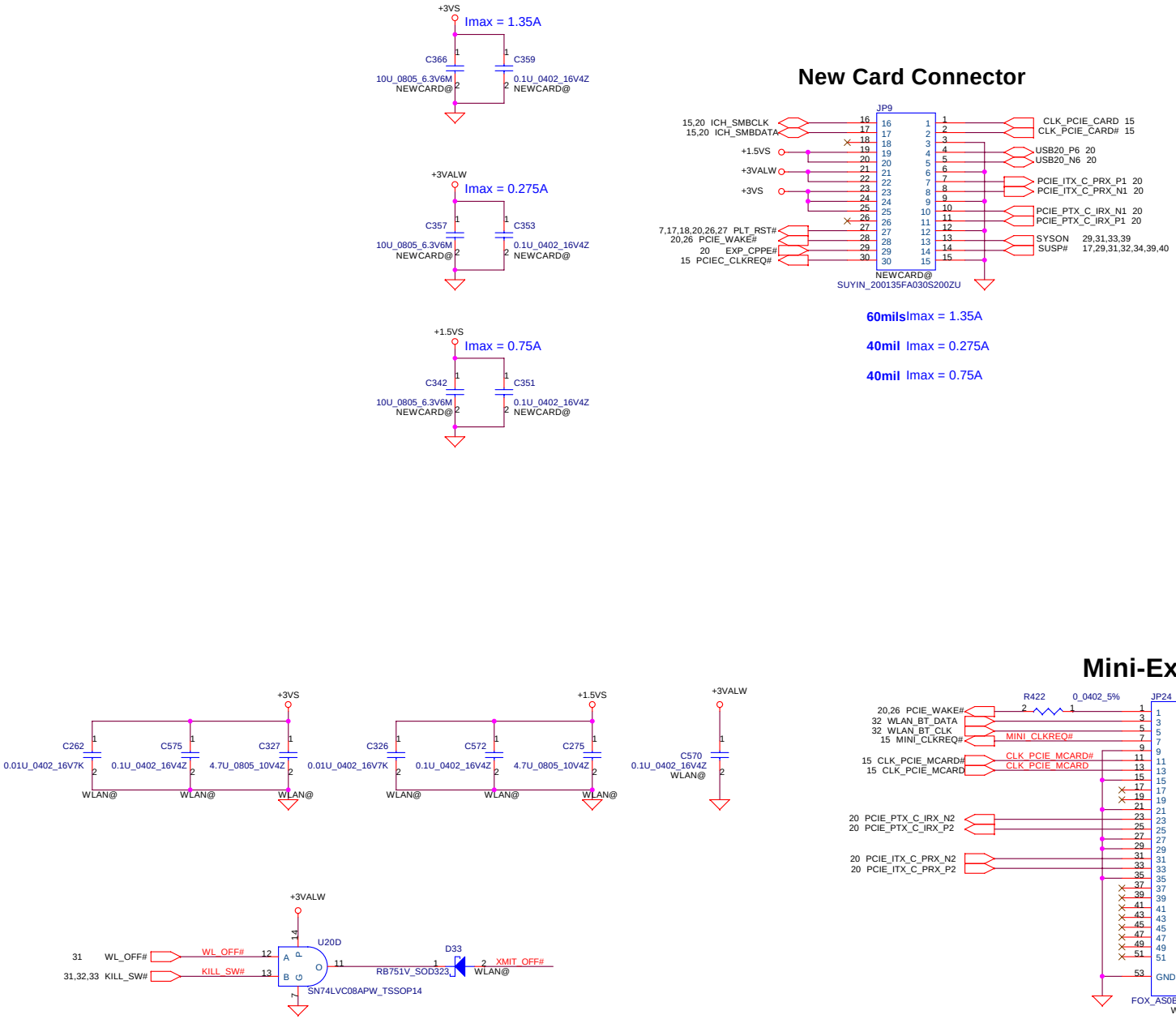
Compal Electronics, Inc.

Title: IEEE1394 VIA VT6311S

Size: B | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 24 of 44

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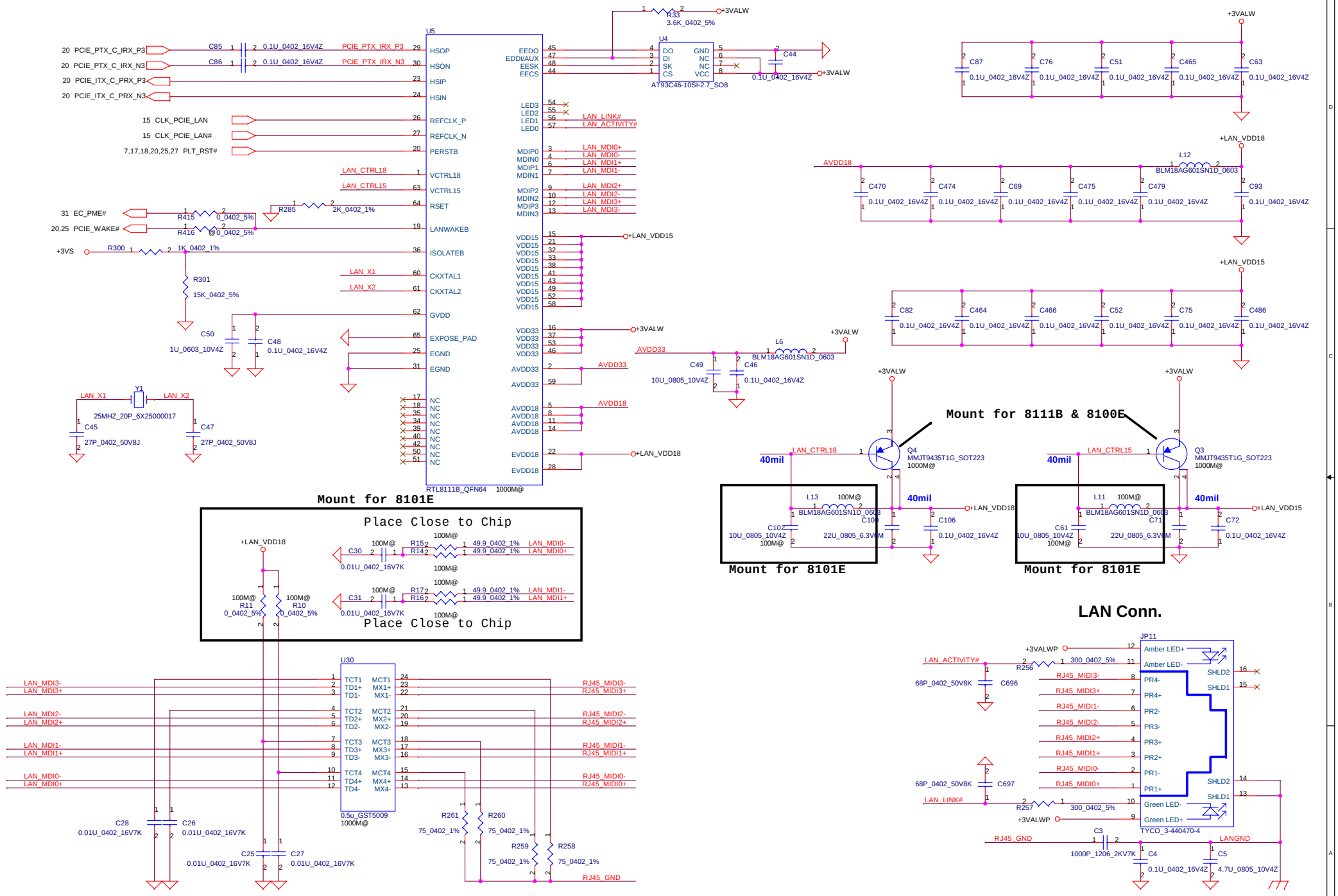
**Compal Electronics, Inc.**

Title: **MiniCard Conn &NewCard/B Conn**

Size: Custom | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 25 of 44




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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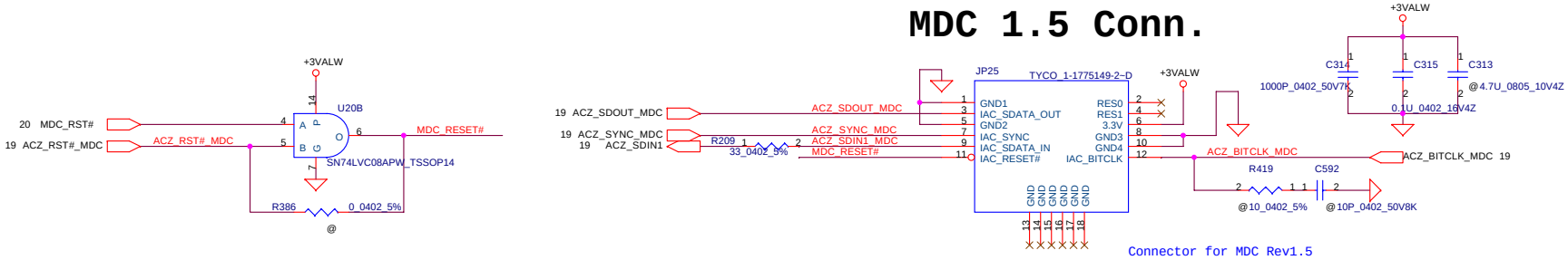
**Compal Electronics, Inc.**

Title: RTL8111B/8101E 10/100/1000 LAN

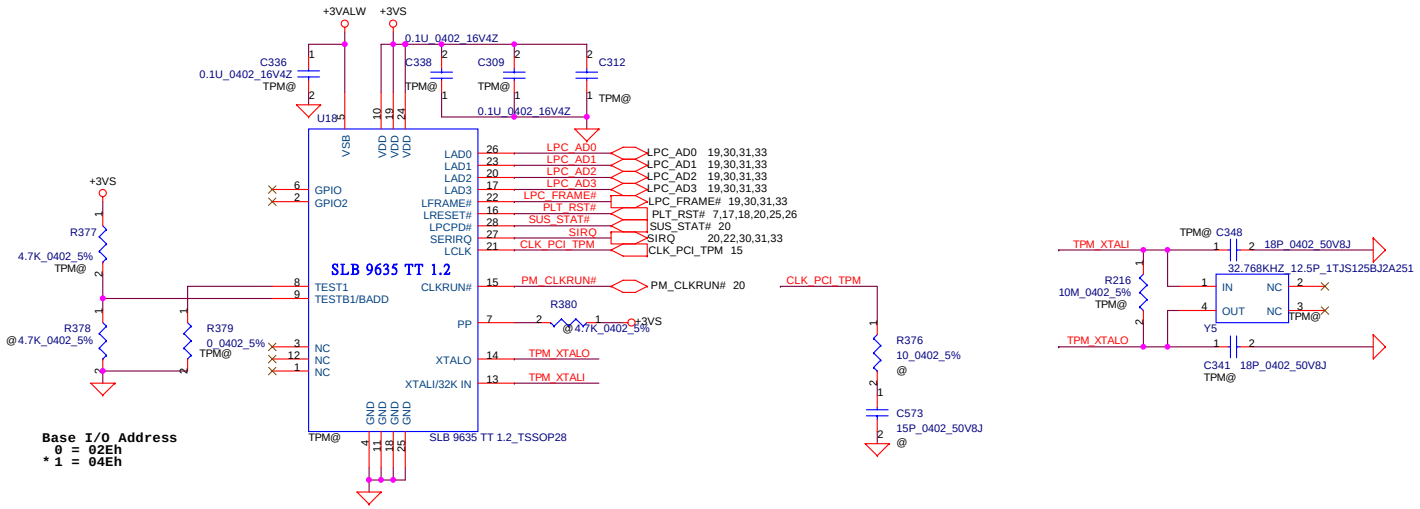
Size: Custom | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Tuesday, May 02, 2006 | Sheet 26 of 44

# MDC 1.5 Conn.




# TPM1.2 on board

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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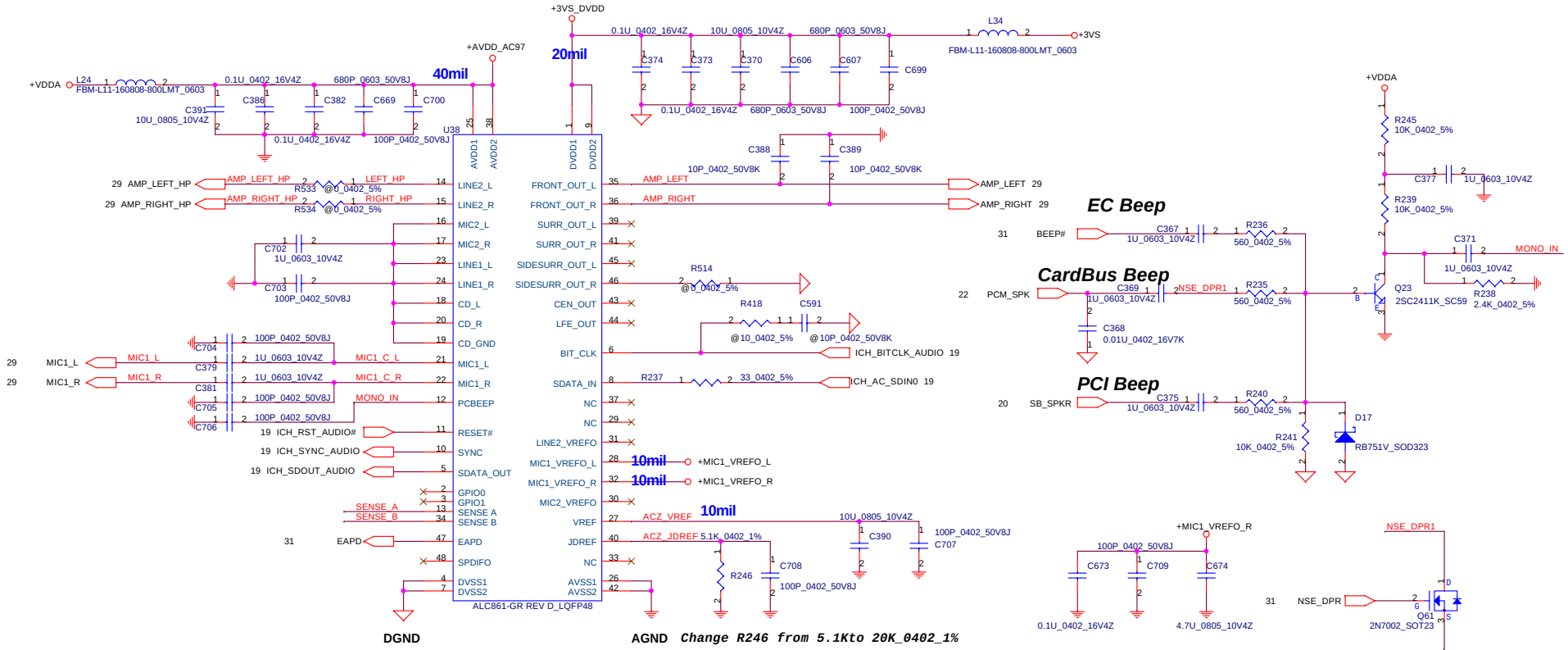
**Compal Electronics, Inc.**

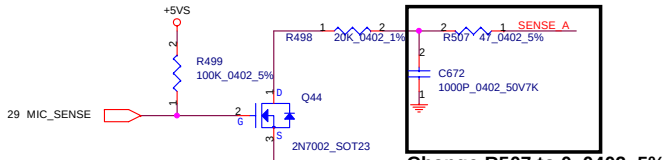
Title: **TPM/G Accelerometer senser**

Size | Document Number: **HTW20 M/B LA-3171P** | Rev 1.0

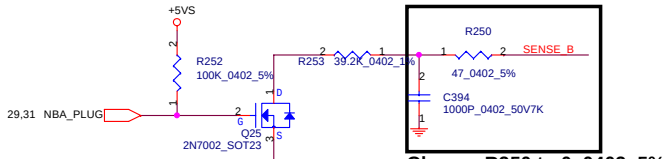
Date: Tuesday, May 02, 2006 | Sheet 27 of 44

# HD Audio Codec




**Change R507 to 0_0402_5%**
**Delete C672**
**for ALC861 ver. D**




**Change R250 to 0_0402_5%**
**Delete C394**
**for ALC861 ver. D**

| Sense Pin | Impedance | Codec Signals |
|---|---|---|
| SENSE A | 39.2K | PORT-A (PIN 39, 41) |
| | 20K | PORT-B (PIN 21, 22) |
| | 10K | PORT-C (PIN 23, 24) |
| | 5.1K | PORT-D (PIN 35, 36) |
| SENSE B | 39.2K | PORT-E (PIN 14, 15) |
| | 20K | PORT-F (PIN 16, 17) |
| | 10K | PORT-G (PIN 43, 44) |
| | 5.1K | PORT-H (PIN 45, 46) |

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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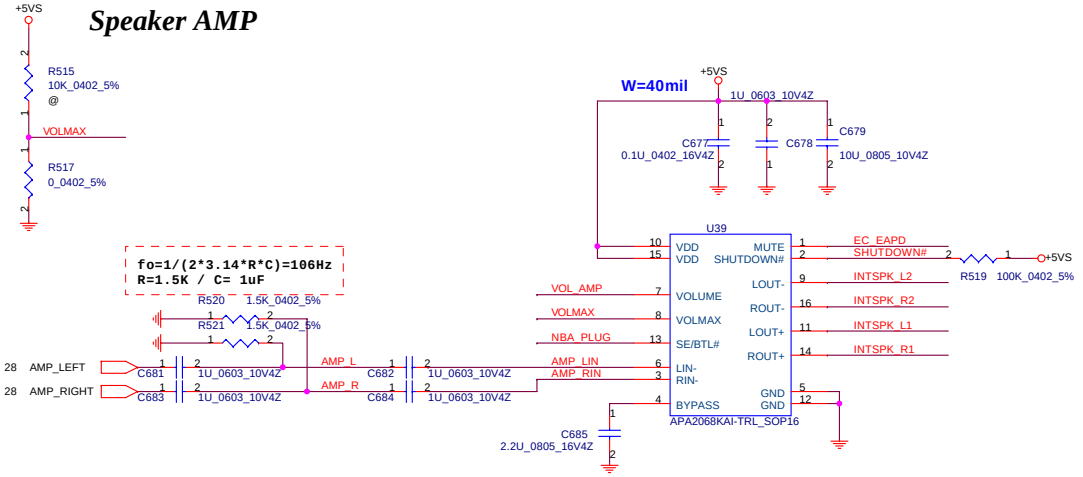
**Compal Electronics, Inc.**

Title: HD Audio Codec ALC861D

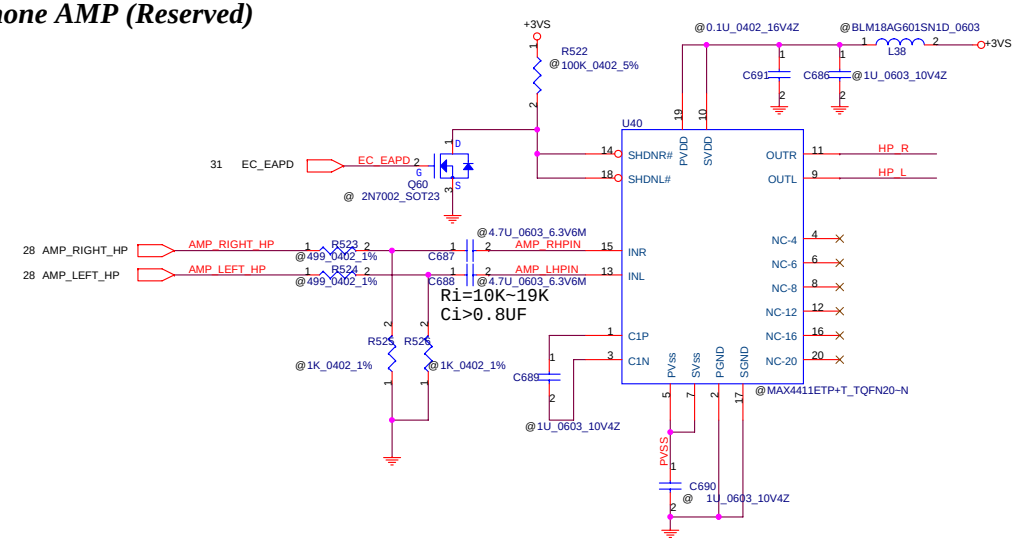
Size: Custom | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 28 of 44

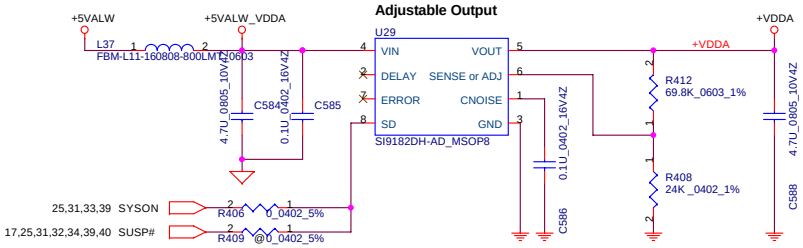
# Speaker AMP



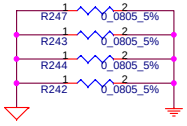

# Headphone AMP (Reserved)

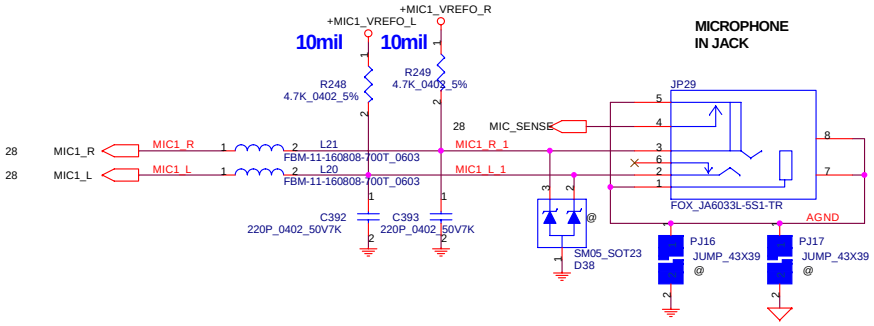



# Regulator for CODEC



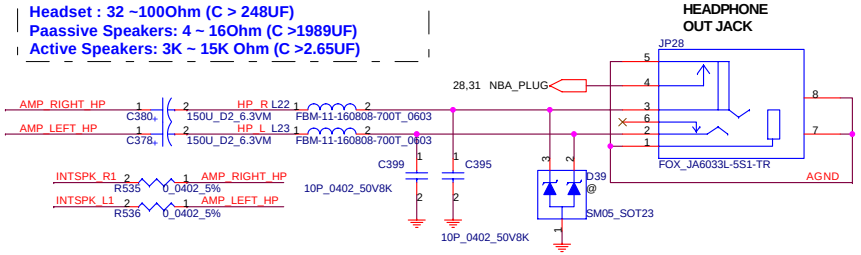

# Moat Bridge



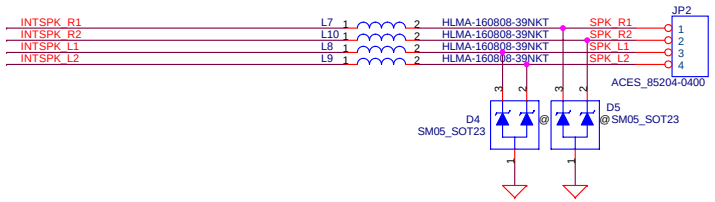




**Microsoft Audio Hardware Design, Section "Analog Audio Classification Using Device Impedance" recommand Audio Device Impedance:**

**Headset : 32 ~100Ohm (C > 248UF)**
**Paassive Speakers: 4 ~ 16Ohm (C >1989UF)**
**Active Speakers: 3K ~ 15K Ohm (C >2.65UF)**

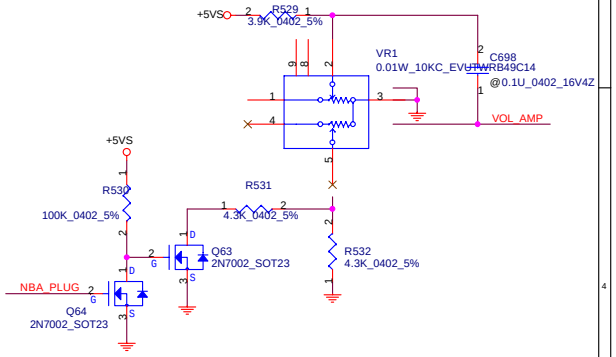



# Speaker Connector




| Gain Setting | | |
|---|---|---|
| | DB | VOL AMP |
| SPK | 10 | 0.66-3.7 |
| HP | 0 | 1.18-3.9 |

# Variable Resistor




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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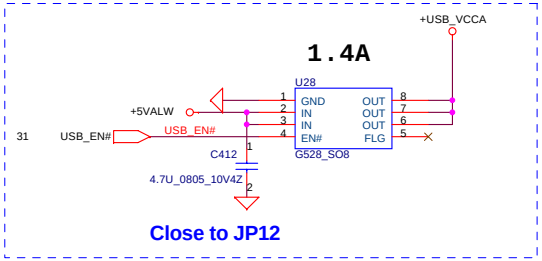
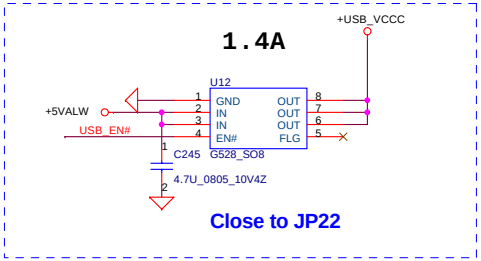
**Compal Electronics, Inc.**

Title: AMP/VR/Audio Jack

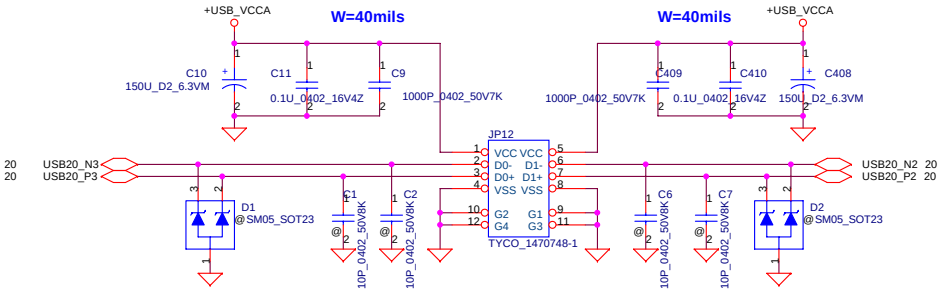
Size: Custom | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 29 of 44



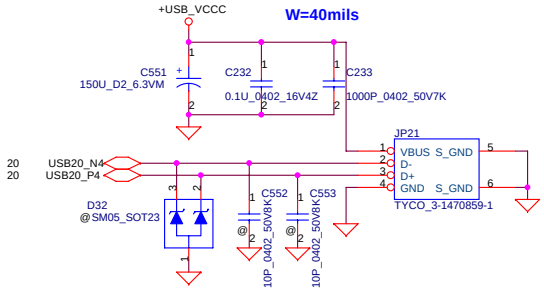

## USB CONN. 1

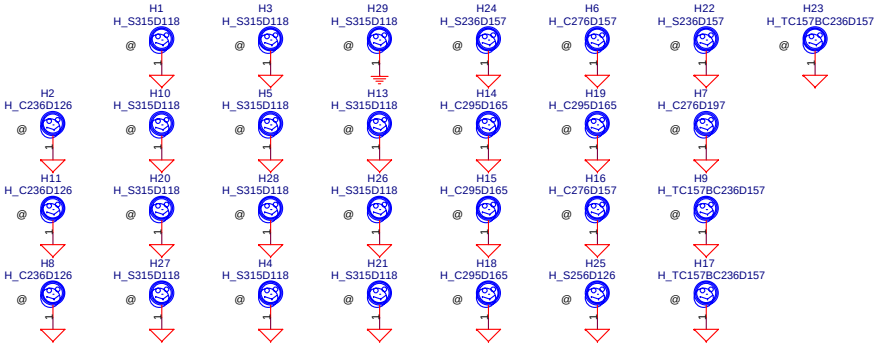


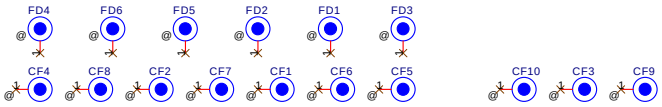

## USB CONN. 2



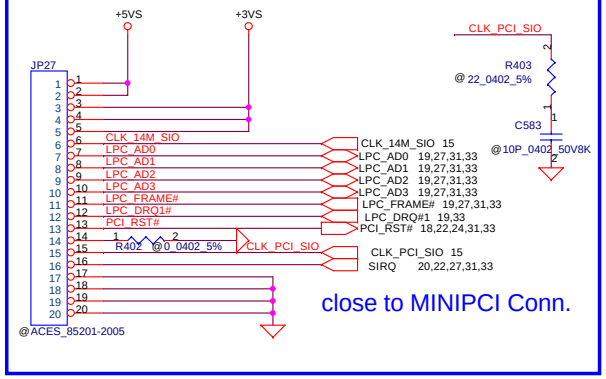

## USB CONN. 3






## LPC Debug Port

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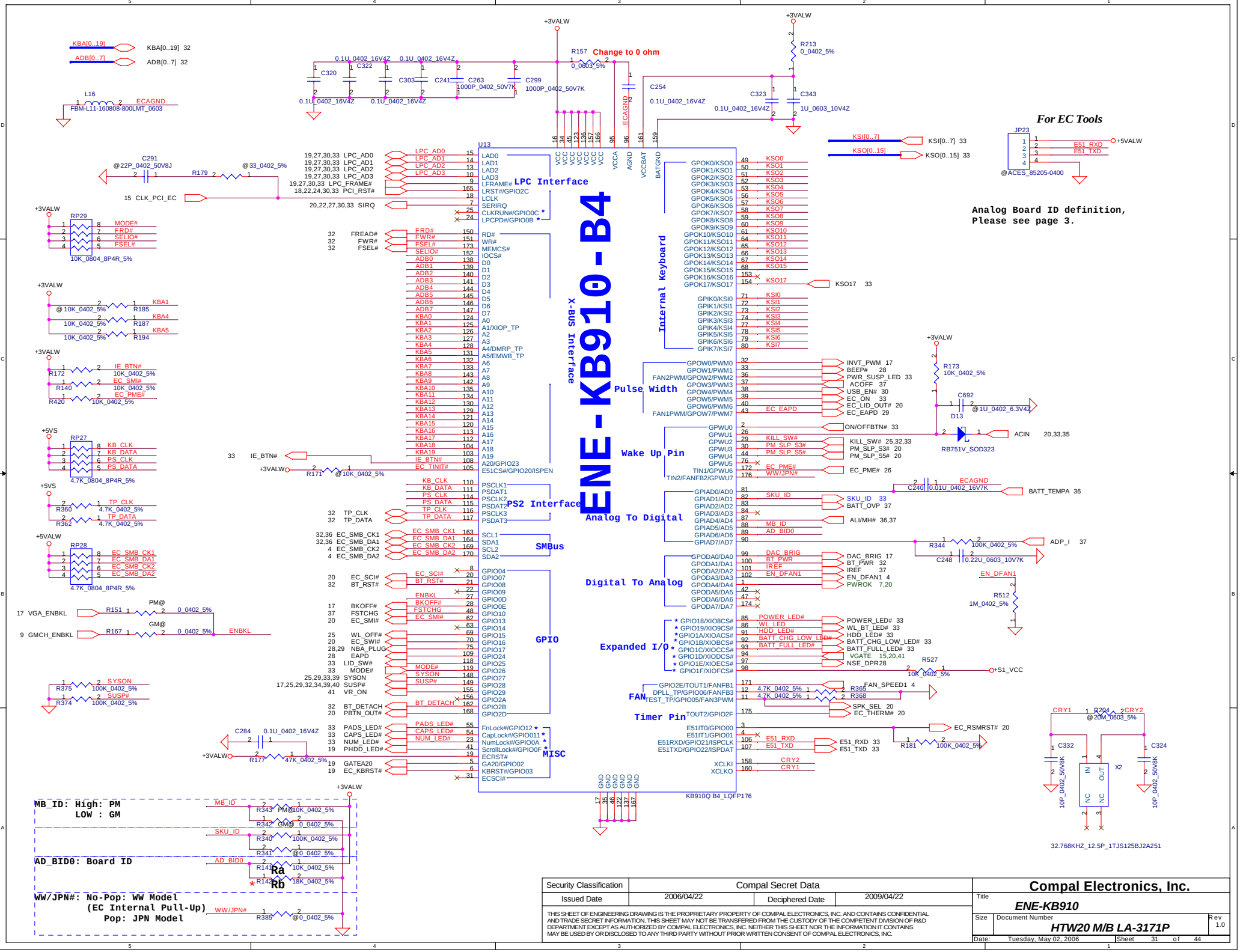
**Compal Electronics, Inc.**

Title: Screw Hole/USB/LPC Conn

Size | Document Number: HTW20 M/B LA-3171P | Rev 1.0

Date: Friday, April 28, 2006 | Sheet 30 of 44

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| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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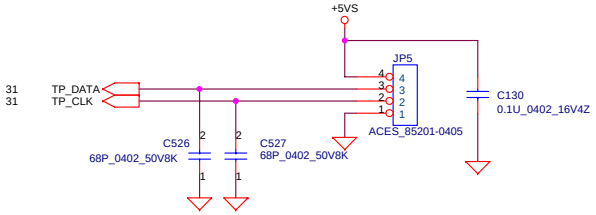
**Compal Electronics, Inc.**

Title: *ENE-KB910*

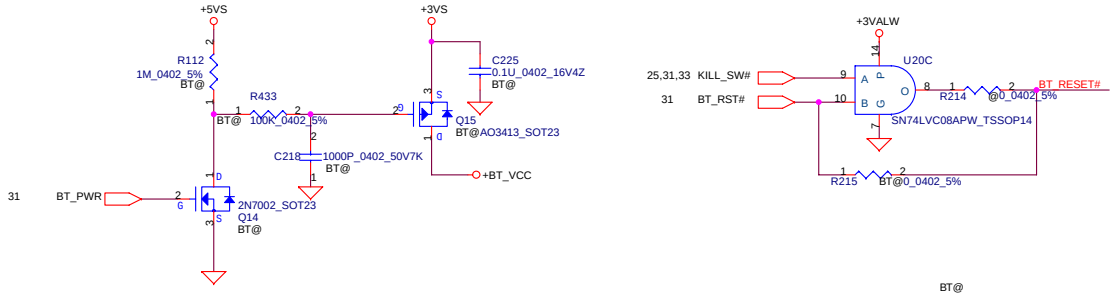
Size | Document Number: *HTW20 M/B LA-3171P* | Rev 1.0

Date: Tuesday, May 02, 2006 | Sheet 31 of 44

# TP CONN.

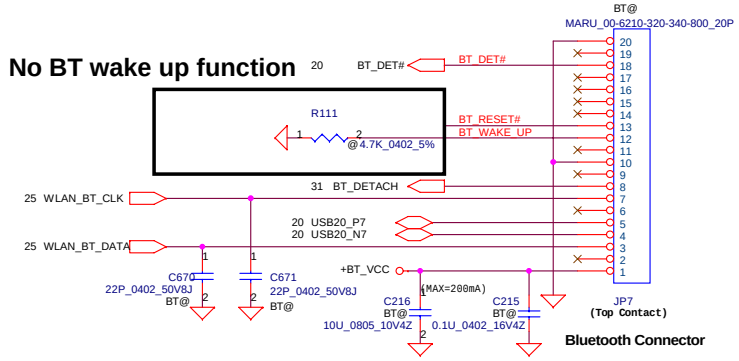



# BlueTooth Interface

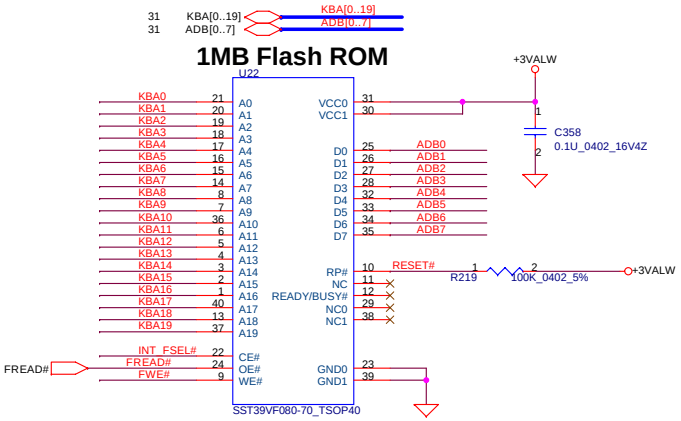


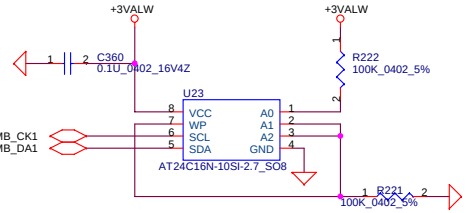

Module ID
Indication for polarity of reset
Reset input High Active --> Low ,
Reset input Low Active --> Open

## No BT wake up function

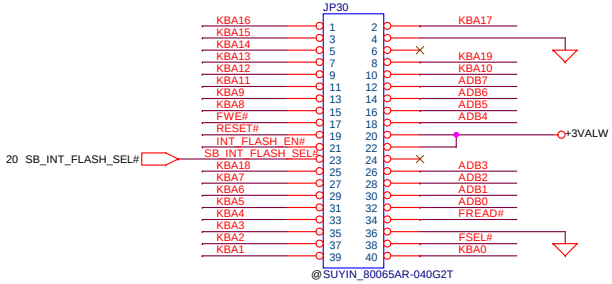


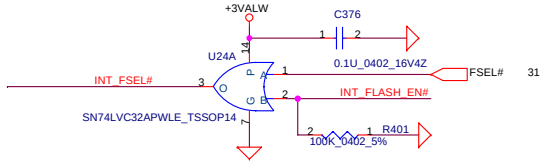

# 1MB Flash ROM

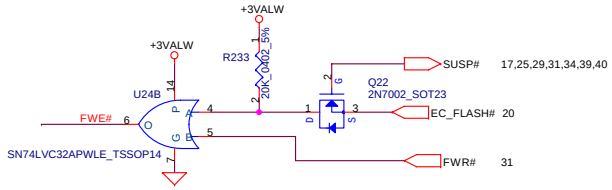



# 1MB ROM Socket

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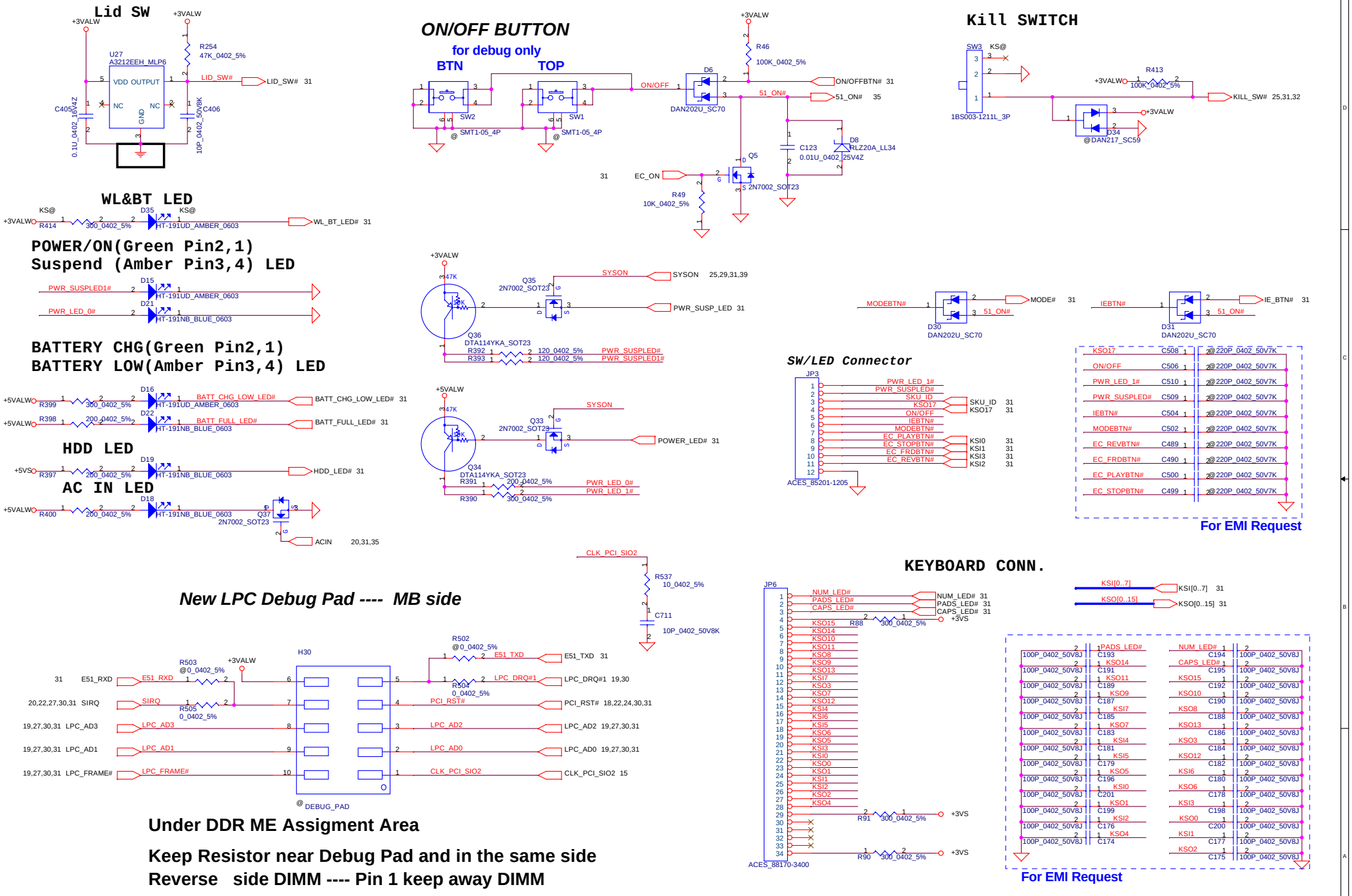
**Compal Electronics, Inc.**

Title: 1MB BIOS/ TP Conn/ BT Conn

Size | Document Number: HTW20 M/B LA-3171P | Rev 1.0

Date: Friday, April 28, 2006 | Sheet 32 of 44




**Under DDR ME Assigment Area**

**Keep Resistor near Debug Pad and in the same side**

**Reverse side DIMM ---- Pin 1 keep away DIMM**

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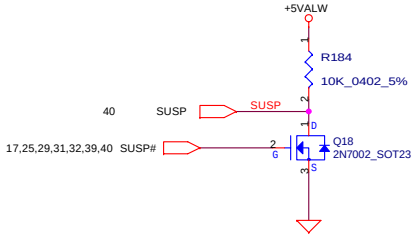
**Compal Electronics, Inc.**

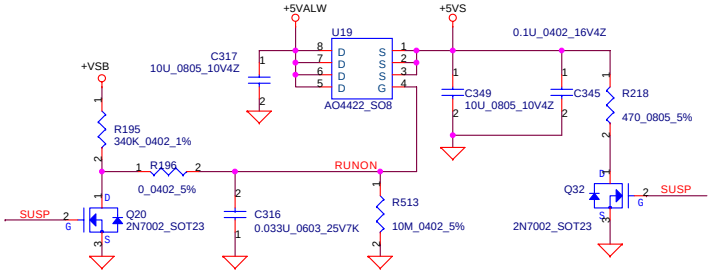
Title: S4R/LID/KS/KB/LED/SW-B Conn

Size | Document Number: HTW20 M/B LA-3171P | Rev 1.0

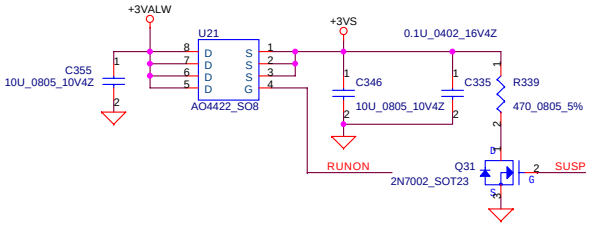
Date: Tuesday, May 02, 2006 | Sheet 33 of 44

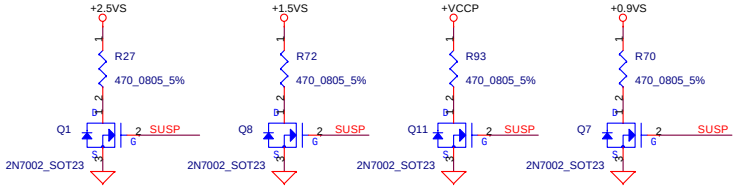



## +5VALW to +5VS Transfer

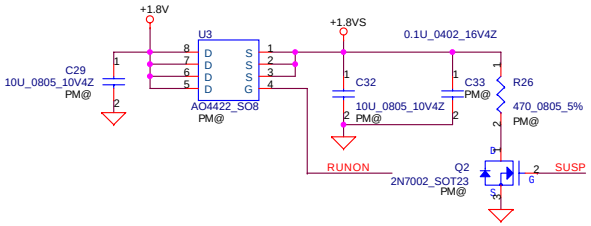



## +3VALW to +3VS Transfer




## +1.8V to +1.8VS Transfer

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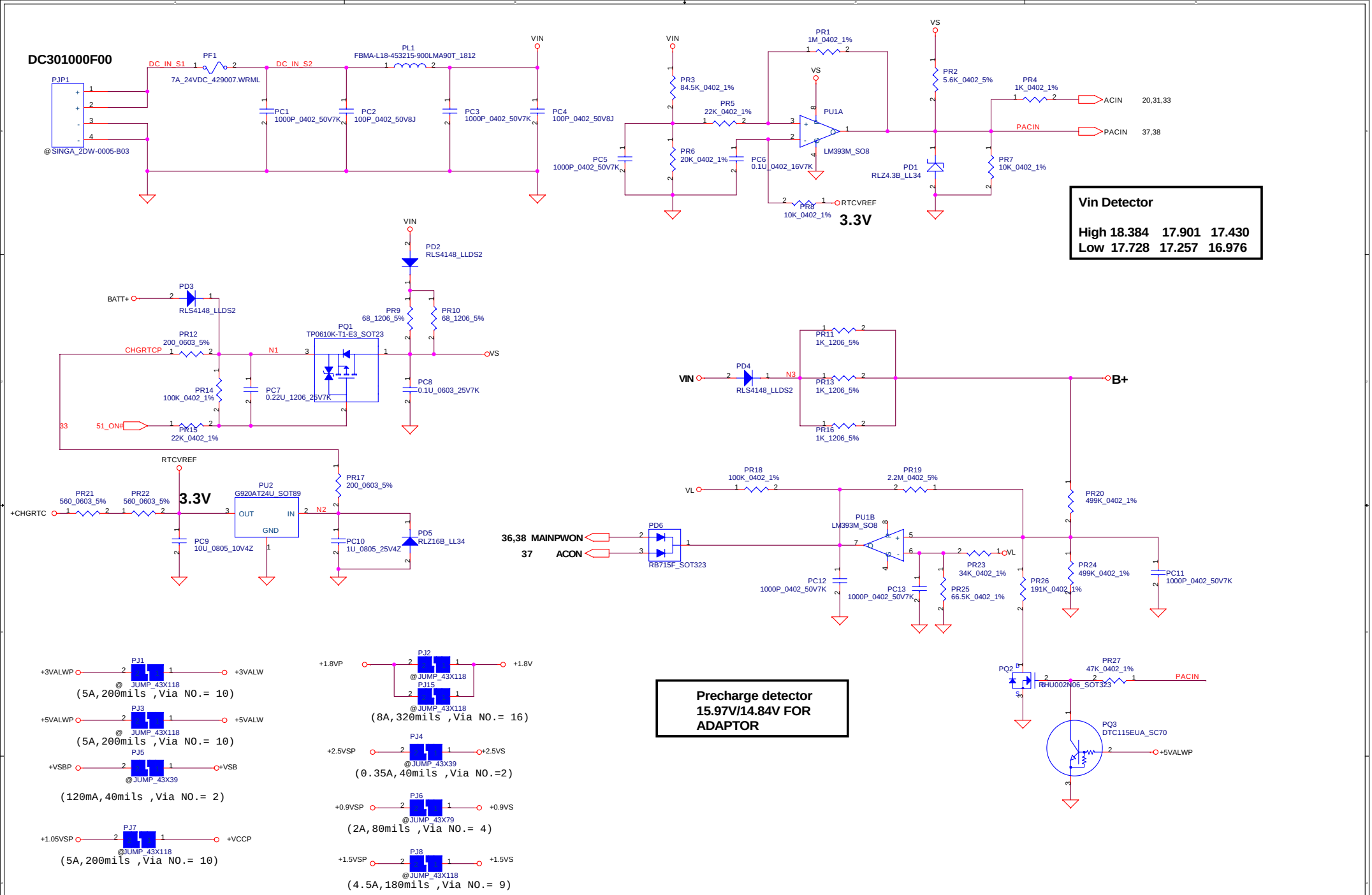
**Compal Electronics, Inc.**

Title: **DC/DC Circuits**

Size | Document Number: **HTW20 M/B LA-3171P** | Rev 1.0

Date: Friday, April 28, 2006 | Sheet 34 of 44

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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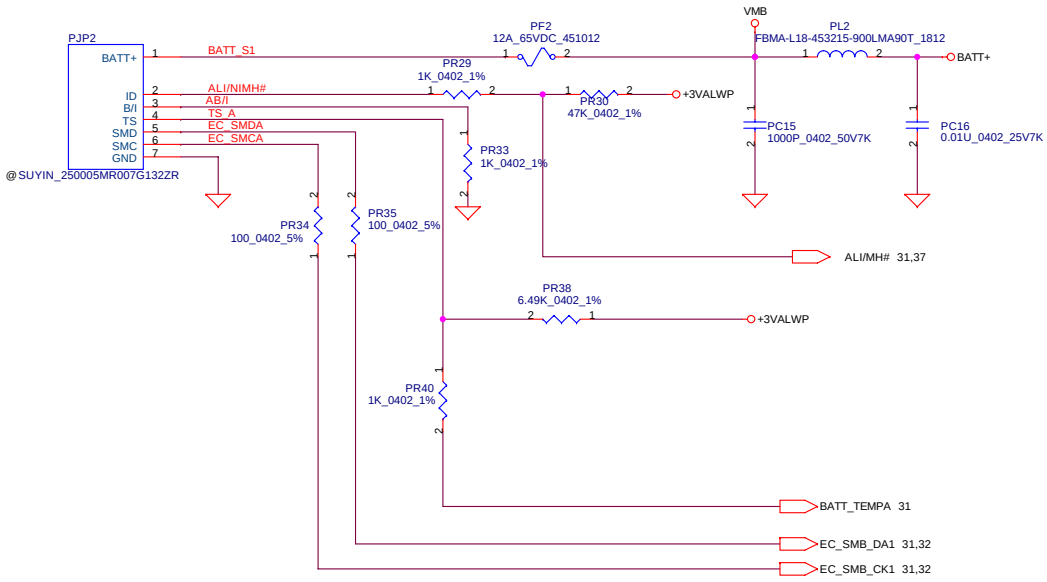
**Compal Electronics, Inc.**

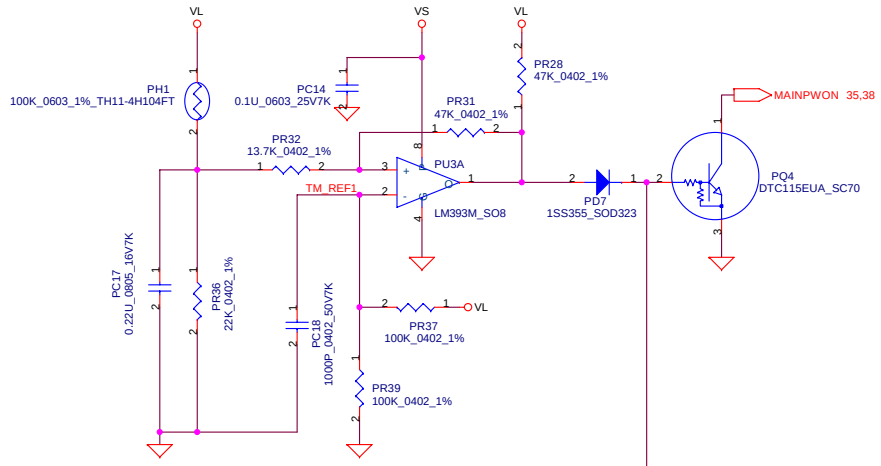
Title: DCIN & DETECTOR

Size | Document Number | Rev 1.0

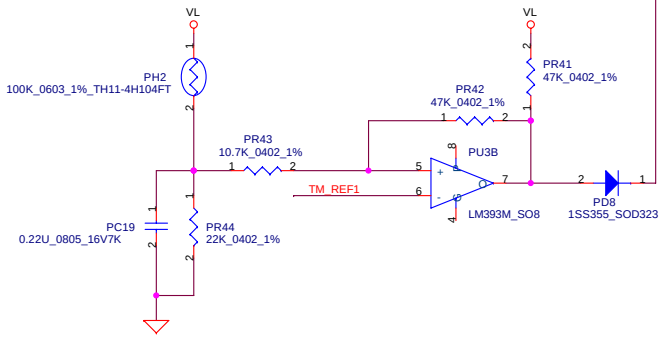
Date: Tuesday, May 02, 2006 | Sheet 35 of 44

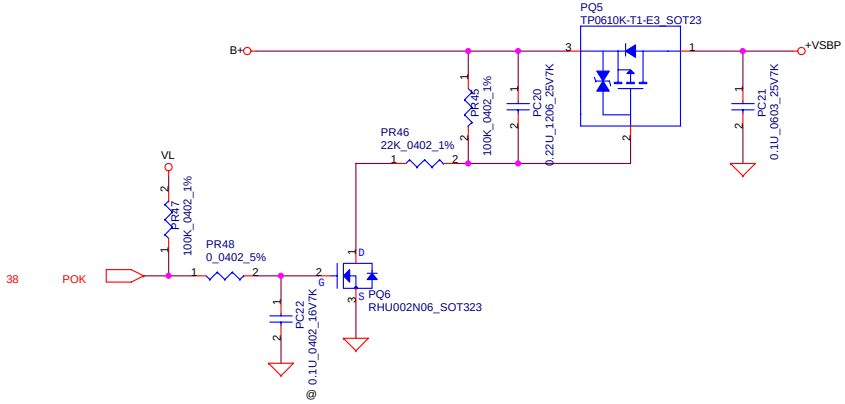
**PH1 under CPU botten side :**
CPU thermal protection at 84 degree C
Recovery at 45 degree C




**PH2 near main Battery CONN :**
BAT. thermal protection at 79 degree C
Recovery at 45 degree C




| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. |
|---|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 | Title: BATTERY CONN / OTP |
| | | | | Size: Document Number: Rev. 1.0 |
| | | | | Date: Tuesday, May 02, 2006 Sheet 36 of 44 |

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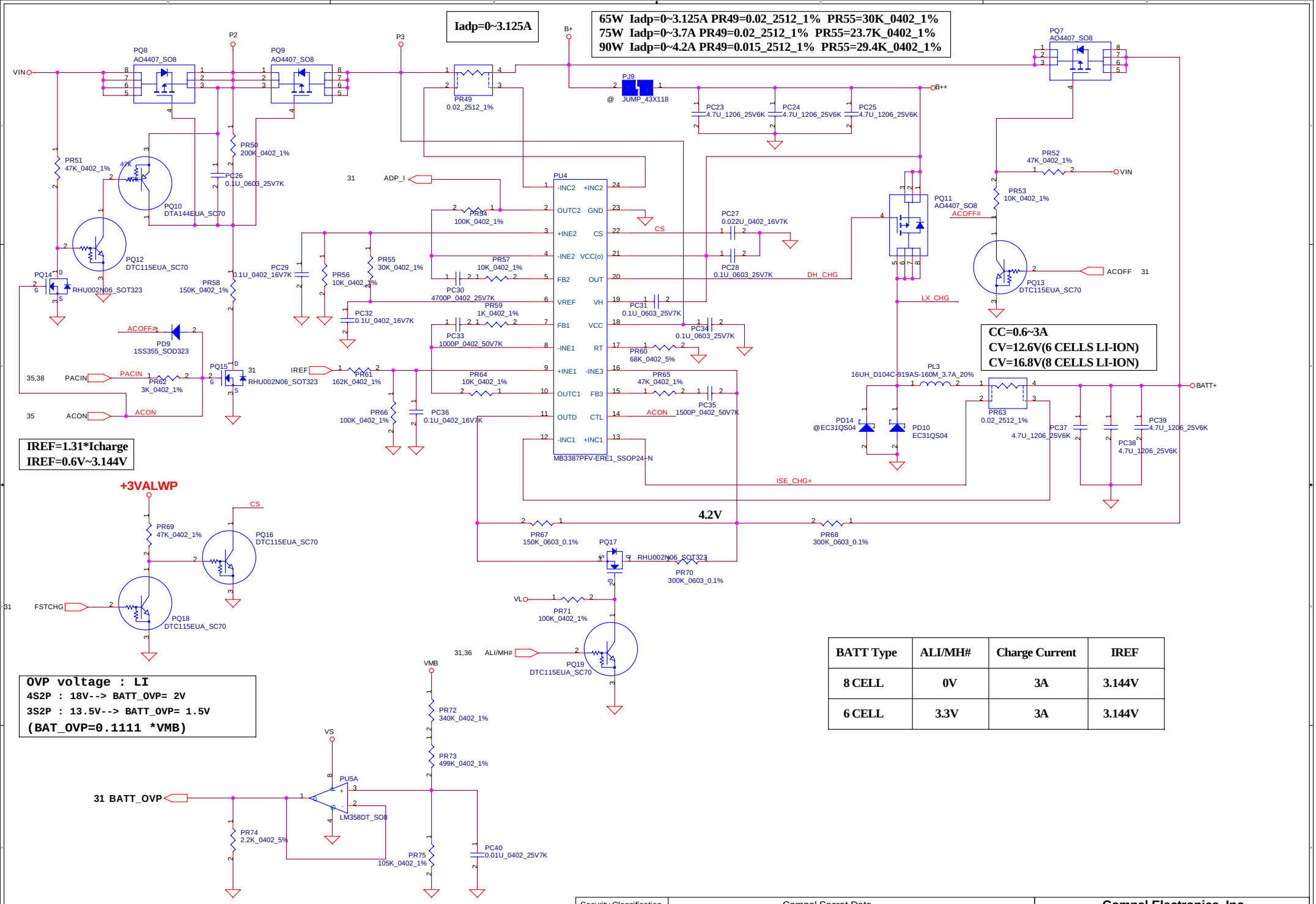


| BATT Type | ALI/MH# | Charge Current | IREF |
|---|---|---|---|
| 8 CELL | 0V | 3A | 3.144V |
| 6 CELL | 3.3V | 3A | 3.144V |

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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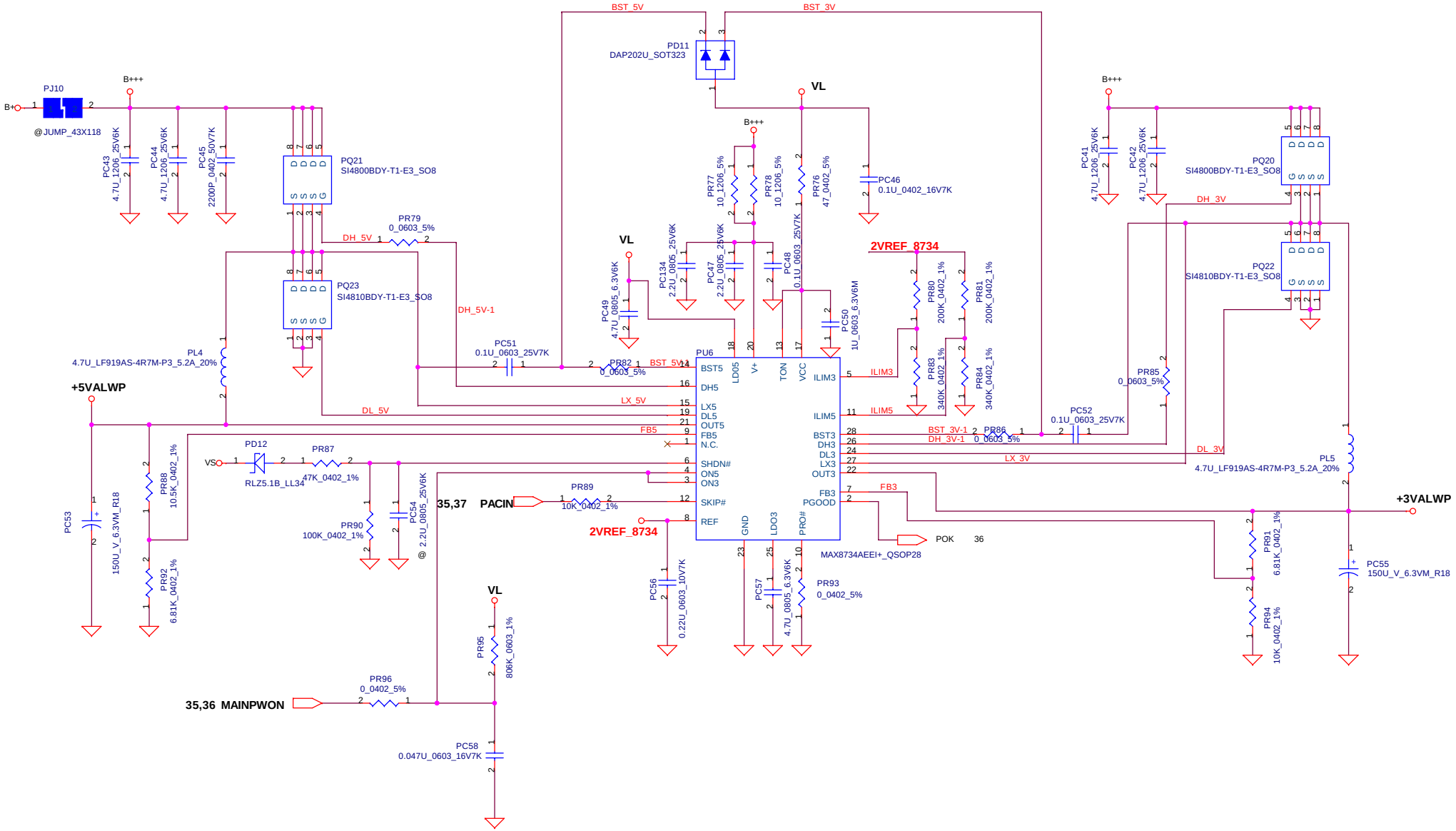
**Compal Electronics, Inc.**

Title: CHARGER

Size | Document Number | Rev 1.0

Date: Tuesday, May 02, 2006 | Sheet 37 of 44

# +3.3VALWP/+5VALWP

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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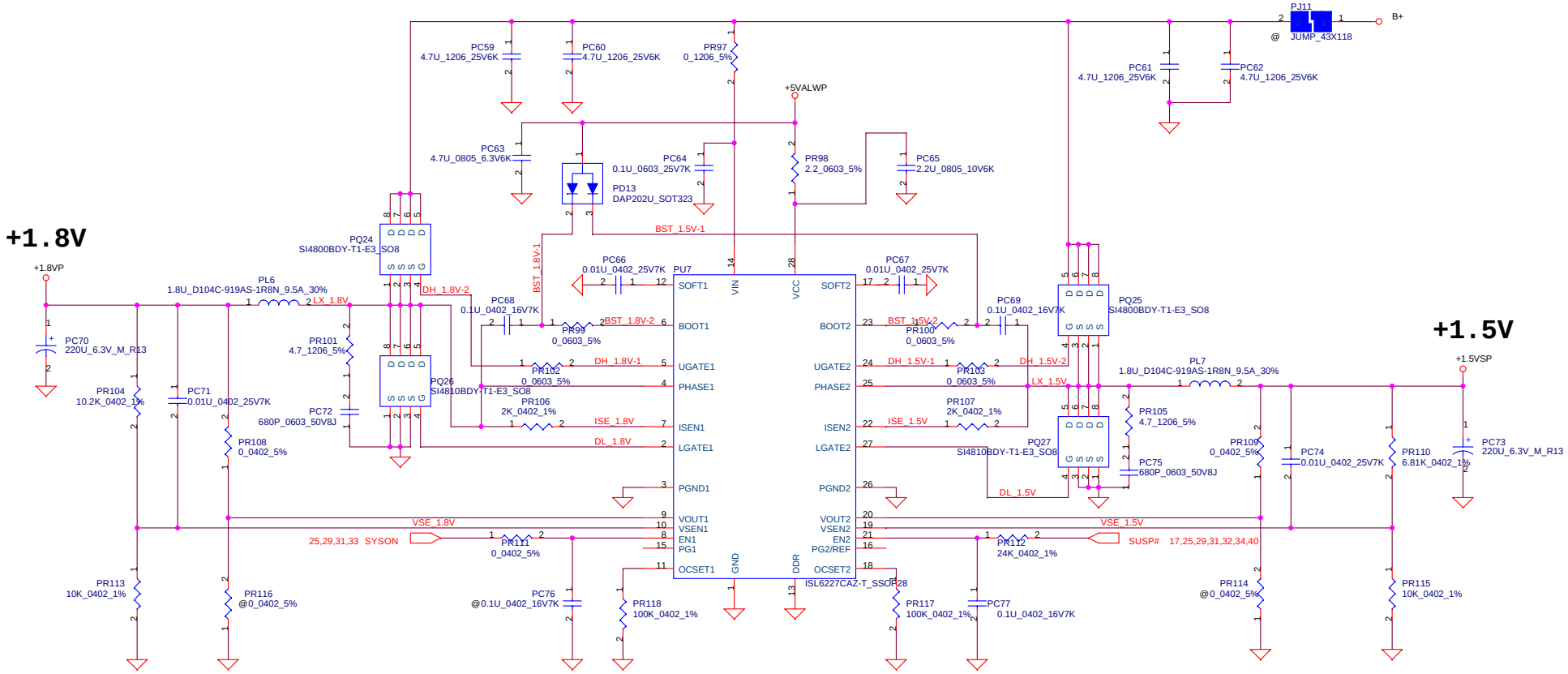
**Compal Electronics, Inc.**

Title: +5V/+3V

Size: Custom | Document Number: HTW20 M/B LA-3171P | Rev: 1.0

Date: Tuesday, May 02, 2006 | Sheet 38 of 44

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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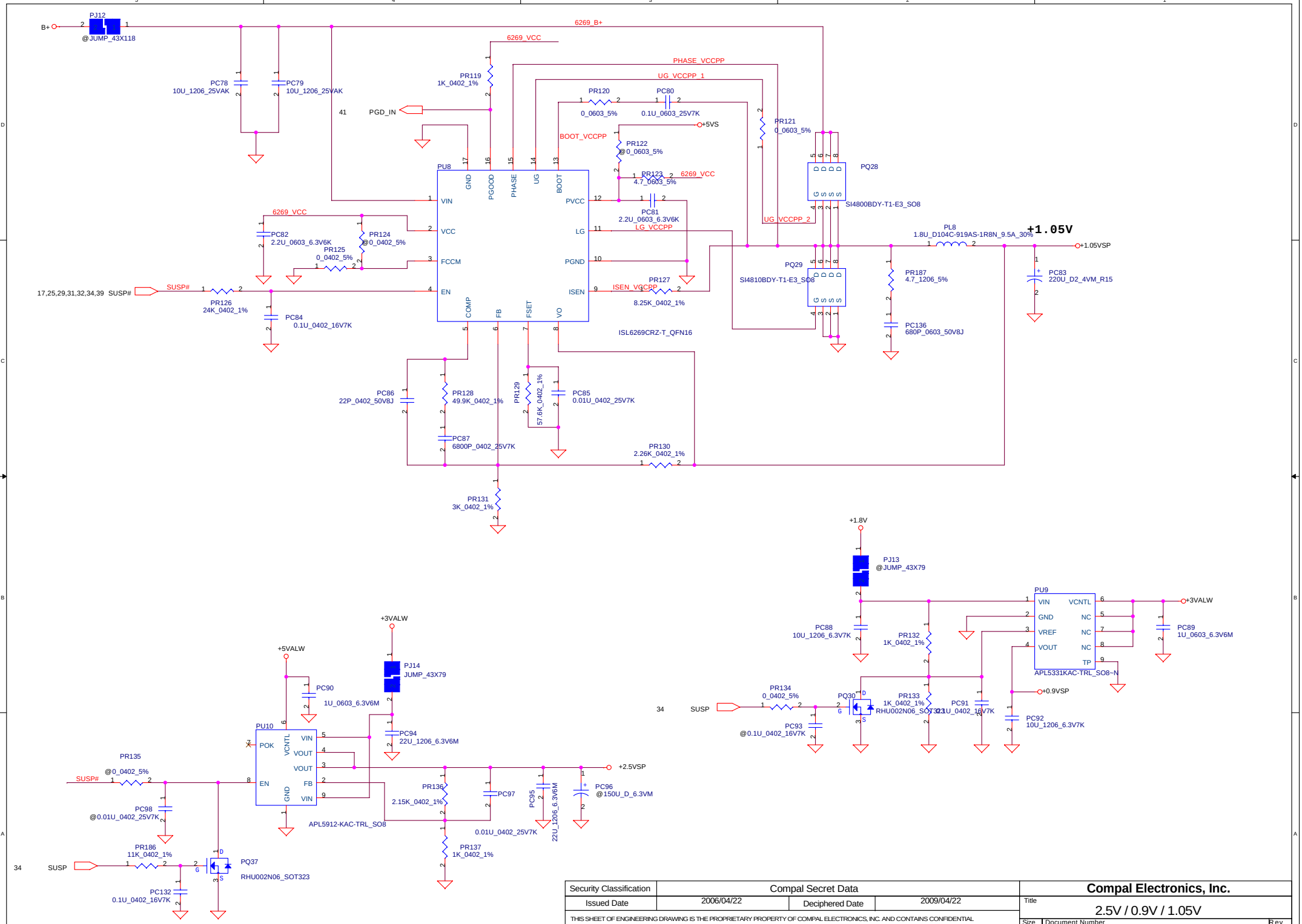
**Compal Electronics, Inc.**

Title: 1.8V / 1.5V

Size | Document Number | Rev 1.0

Date: Tuesday, May 02, 2006 | Sheet 39 of 44

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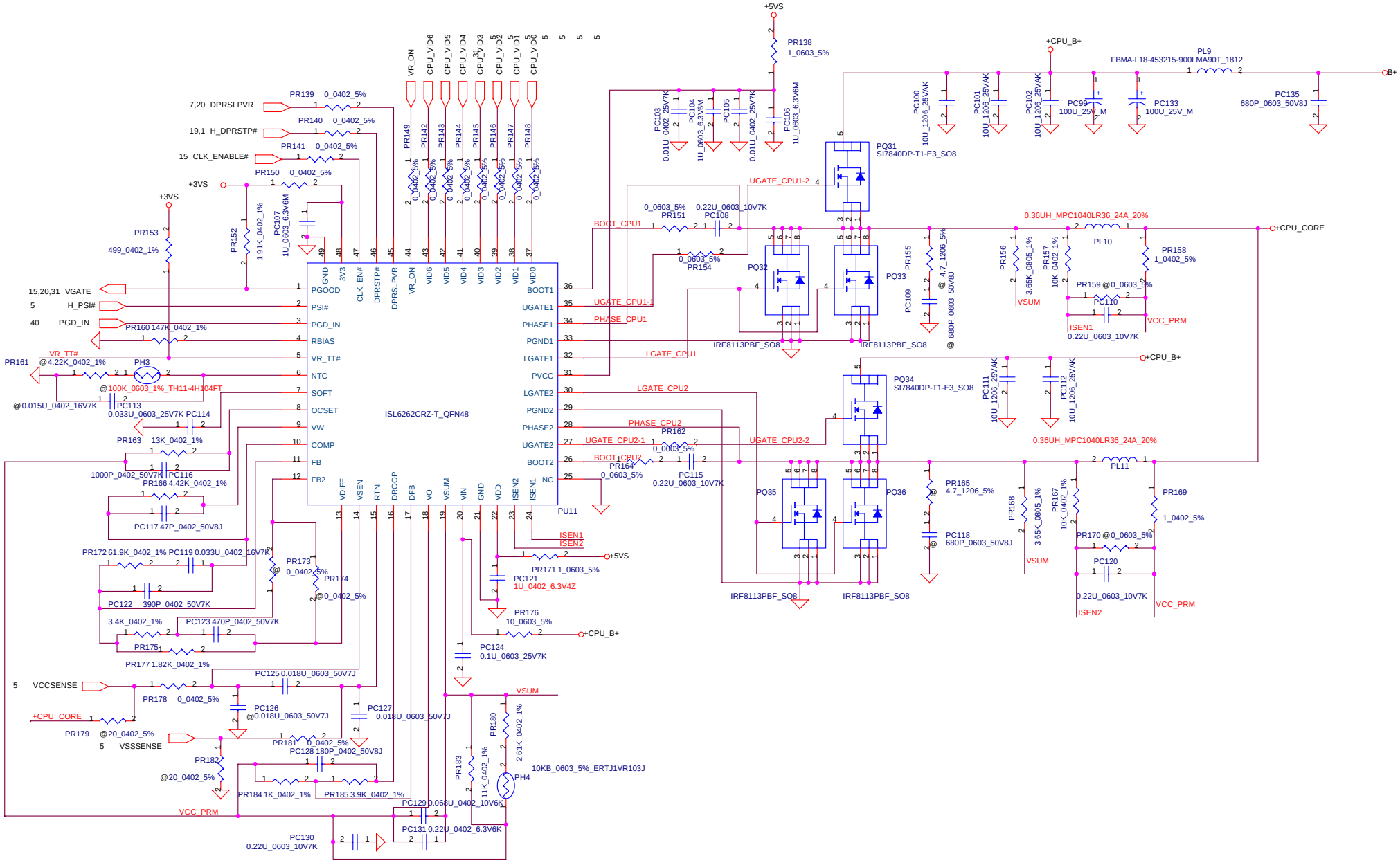
**Compal Electronics, Inc.**

Title: 2.5V / 0.9V / 1.05V

Size | Document Number | Rev 1.0

Date: Tuesday, May 02, 2006 | Sheet 40 of 44

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**Compal Electronics, Inc.**

Title: **+CPU_CORE**

Size: Custom | Document Number | Rev: 1.0

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# POWER PIR LIST

| page | Reason for change | Modify list |
|---|---|---|
| **EVT->DVT** | | |
| 40 | Add 680P at B+ for EMI | Add 680P_0402_25V at B+ |
| 38 | Change 1.5V sequence for HW | Change PR112 from 22K_0402_1% to 24K_0402_1% |
| 39 | Change 2.5V sequence for HW | Unpop PR135,PC98<br>Pop PR186=11_K0402_1%, PQ37, PC132=0.1u_0402_16V |
| 39 | Change 2.5V sequence for HW | Change PR104 from 10K_0402_1% to 10.2K_0402_1% |
| 38 | Adjust 3V/5V OCP to 8A | Change PR80,PR81 to 200K_0402_1%, PR83,PR84 to 340K_0402_1% , PL4,PL5 to 4.7uH |
| 41 | Adjust CPU loadlone | Change PC119 to 33n_0402_16V, PR185 to 3.9K_0402_1% |
| **DVT->PVT** | | |
| 40 | Add snubber at 1.05V | Add 4.7_1206_5% and 680P_0603_50V at PR187,PC136 |
| 41 | Adjust switching frequence for intersil suggest | Change PC117 from 5600P to 47P_0402_50V<br>Change PR166 from 3.57K to 4.42K_0402_1% |
| 40 | Adjust 1.05 OCP to 8A | Change PR127 from 11.5K to 8.25K_0402_1% |

PROPRIETARY NOTE

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|---|---|---|---|
| Issued Date | 2006/04/22 | Deciphered Date | 2009/04/22 |

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# HW4 Product Improvement Record (P.I.R.)

| Phase: A to B | | Date: 2006/01/04 | | | Writer: Lion Wang | | |
|---|---|---|---|---|---|---|---|
| Page# | Action Plan (add; del; change) | Location or Net_List | Before value (Attached file) | After value (Attached file) | Detail Discretion and Root Cause | Rev. | DL/DM Check |
| 22,23 | none | none | | | change TI8412 to ENE 714 for CB & 5in1 function | 0.2 | |
| 24 | none | none | | | change TI8412 to VIA6311S for 1394 function | 0.2 | |
| 28 | Add | C606,C607 | | | Add for EMI request | 0.2 | |
| 28 | Add | L32 | | | Add for EMI request | 0.2 | |
| 31 | Unmount | R171,R185 | | | update after check ENE FAE | 0.2 | |
| 31 | Change | R365,R368<br>R187,R194 | 1K_5%_0402 | 10K_5%_0402 | update after check ENE FAE | 0.2 | |
| 31 | Change | L33 | Bead | 0_5%_0603 | update after check ENE FAE | 0.2 | |
| 19 | Change | JP22 | | | change HDD CONN. | 0.2 | |
| 31 | Change | R142 | 0_5%_0402 | 8.2k_5%_0402 | update BID from REV0.1 to REV0.2 | 0.2 | |
| 29 | | | | | change U27,D38 ,D39 connect from GND to AGND | 0.2 | |
| 26 | Del | L33 | | | LAN PCIE detect issue cause system boot black screen | 0.2 | |
| 29 | Change | SW4 | | | Change VR to Rock Type switch | 0.2 | |
| 29 | Change | R514,R517,R516 | | | Change AMP HP gain from -6 dB to 0 dB | 0.2 | |
| 28 | Add | Q44,R507,R498<br>C672,R499 | | | Add for MIC Jack present function | 0.2 | |
| 26 | Change | R10,R11 | | | change R10,R11 connect to U30 PIN7 & PIN10 to fix 10/100 Lan cannot connect issue | 0.3 | |
| 20 | Change | | | | change ODD_RST# from GPIO 24 to GPIO34 | 0.3 | |
| 24 | Change | | | | delete R508~R511 and add L39 & L40 for EMI request | 0.3 | |
| | | | | | | 0.3 | |




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HTW20 LA-3171P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 0.4

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| 1 | 0327 | 29 | REMOVE C680,R516,R518 | MODIFY VOL_AMP FUNCTIONAL CIRCUIT |
| | | | REMOVE SW4 | |
| | | | REMOVE CONNECTION OF VOL_UP,VOL_DOWN,VOL_MUTE,KSO17 | |
| | | | ADD CONNECTION OF NBA_PLUG ON U39.13 | ADD VR CIRCUIT |
| | | | ADD R529_3.9K_0402_5%,R530_100K_0402_5%,R531_4.3K_0402_5% | |
| | | | R532_4.3K_0402_5%,Q62,Q63 | |
| | | | RESERVE C698_0.1U_0402 | |
| 2 | 0327 | 28 | RESERVE R533 CONNECT BETWEEN AMP_LEFT_HP & LEFT_HP | MODIFY EARPHONE GAIN CONTROL |
| | | | RESERVE R534 CONNECT BETWEEN AMP_RIGHT_HP & RIGHT_HP | CIRCUIT |
| | | 29 | ADD R535 CONNECT BETWEEN INTSPK_R1 & AMP_RIGHT_HP | |
| | | | ADD R536 CONNECT BETWEEN INTSPK_L1 & AMP_LEFT_HP | |
| 3 | 0327 | 28 | ADD C699_100P_0402 ON +3VS_DVDD | FOR EMI PURPOSE |
| | | | ADD C700_100P_0402 ON +AVDD_AC97 | |
| | | | ADD C702_1U,C703_100P ON U38 PIN 16,17,18,19,20,23,24 | |
| | | | ADD C704_100P_0402 ON MIC1_C_L | |
| | | | ADD C705_100P_0402 ON MIC1_C_R | |
| | | | ADD C706_100P_0402 ON MONO_IN | |
| | | | ADD C707_100P_0402 ON ACZ_VREF | |
| | | | ADD C708_100P_0402 ON ACZ_JDREF | |
| | | | ADD C709_100P_0402 ON +MIC1_VREFO_R | |
| | | | ADD C710_100P_0402 ON +MIC1_VREFO_L | |

HTW20 LA-3171P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4 TO 1.0

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| 1 | 0417 | 33 | ADD R537 10_0402 AND C711 10P_0402 ON CLK_PCI_SIO2 | PREVENT PCI CLOCK TRACE FLOATING |
| 2 | 0419 | 16 | CHANGE L26,L25 TO 39_0402 | BASE ON INTEL CRB SCHEMATIC TO DO |
| | | | CHANGE C411,C413 TO RESERVED | MODIFICATION (CRB REV:1.601) |
| 3 | 0419 | 29 | CONNECT VR1.1,VR1.2 TO AGAD | BASE ESD TEST RESULT, CONNECT TO AGND |
| | | | | TO PASS ESD TEST |
| 4 | 0419 | 29 | CHANGE L7,L8,L9,L10 TO BEAD 39OHM@100MHZ | TO SOLVE 3G NOISE ISSUE |
| | | | CHANGE C395,C399 TO 10P_0402 | |
| | | 28 | CHANGE C388,C389 TO 10P_0402 | |
| 4 | 0426 | 06 | Add C122,C537 to 330UF | TO SOLVE ESD ISSUE |

**LAN**

U5
RTL8101E
100M@

**TRANSFORMER**

U30
TST1284-LF
100M@

**PCB**

ZZZ1
PCB ZKU LA-3171P REV0

**Card BUS**

U31
CB 1410
1410@

**SB**

U16
ICH7
ICH7R1@

**NB**

U6
945GM
GMR3@

U6
945GM
GMR1@

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